SERVICE MANUAL FOR

8355

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MiTAC

8355 N/B MAINTENANCE

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1. Hardware Engineering Specification

1.1 Introduction

The 8355 motherboard would support the AMD ClawHammer K8 processor with uPGA Package, 2700+/3000+/3300+/3600+/3900+/4200+, FSB 800MHz

This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides ico LEDs to display system status, such as AC Power, Battery Power, Battery status, CD-ROM, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK, WIRELESS LAN status. It also equipped 4 USB2.0 ports.

The memory subsystem supports 0MB on board; Expandable up to 1024MB Expandable with combination of optional 128/256/512 MB memory 200-pin DDR 266/333/400 Memory Module x2, PC-2100/2700/3200 specification

The **K8T800** North Bridge plus **VT8235** South Bridge chipset is a high performance, cost-effective and energy efficient solution for the implementation of desktop personal computer systems with 8 / 16-bit 800 / 600 / 400 / 200 MHz HyperTransport. CPU host interface based on AMD K8 / ClawHammer. processors.

The VT8235 “V-Link Client Controller” is a highly integrated PCI /LPC controller. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI bridge chips. The VT8235 also provides a 533 MB/sec bandwidth Host / Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports six PCI slots of arbitration and decoding for all integrated functions and LPC bus.

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The RADEON MOBILITY 9600 provides the fastest and most advanced 2D, 3D, and multimedia graphics performance for the latest applications in full 32-bit color. Its architecture introduces the latest achievements in the graphics industry, which enable the use of the progressive new features in upcoming applications, but without compromising performance. ATI's exclusive support of DirectX® 9.0 features, highly optimized OpenGL® support, and flexible memory configurations allow implementations targeted at both gaming enthusiast and workstation platforms.

To provide for the increasing number of multimedia applications, the AC97 CODEC CMI9738-S is integrated onto the motherboard

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows XP and Windows 2000 to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Part

CPU	AMD ClawHammer K8 processor with uPGA Package 2700+/3000+/3300+/3600+/3900+/4200+ FSB 800MHz
Core logic	VIA K8T800 + VT8235
VGA Control	ATI M10P with 64MB External VRAM (Reserve for 128MB VRAM)
System BIOS	Insyde 256 KB Flash EPROM (Include System BIOS and VGA BIOS) ACPI 2.0; DMI 2.3.1 compliant Plug & Play capability
Memory	0MB on board; Expandable up to 1024MB Expandable with combination of optional 128/256/512 MB memory 200-pin DDR 266/333/400 DRAM Memory Module x2, PC-2100/2700/3200 specification
Clock Generator	ICS 950403
IEEE1394	VT6307L
Audio System	AC97 CODEC: C-MEDIA ELECTRONICS INC., CMI9738-S Power Amplifier: Anpec APA2020
Super I/O	PC87397
Modem	56Kbps(V.90, worldwide) MDC Modem
PHY of LAN	VT6103 10/100 base -T PHY
PCMCIA	ENE710
CARD READER	ENE710

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1.2.1 CPU_ ClawHammer PROCESSOR

The ClawHammer processor family is designed to support performance desktop and workstation applications. It provides a high-performance HyperTransport. link to I/O, as well as a single 64-bit high-performance DDR memory controller.

- **Compatible with Existing 32-bit Code Base**

  Including support for SSE, SSE2, MMX™, 3DNow!™, technology and all legacy x86 instructions

  Runs existing operating systems and drivers

  Local APIC on-chip

- **AMD x86-64 Technology**

  AMD.s 64-bit x86 instruction set extensions

  64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses

  Eight new 64-bit integer registers (16 total)

  Eight new 128-bit SSE/SSE2 registers (16 total)

- **Integrated Memory Controller**

  Low-latency, high-bandwidth

  72-bit DDR at 200, 266, 333, and 400 MHz (64-bits + 8-bits ECC)

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- **HyperTransport. Technology to I/O Devices**

  Two 8-bit links each support 1600 mega-transfers (MT) per second or 1.6 Gbytes/s in each direction

  Can be configured as single 16-bit link supporting 1600 MT/s or 3.2 Gbytes/s in each direction

- **64-Kbyte 2-way Associative ECC-Protected L1 Data Cache**

  Two 64-bit operations per cycle, 3-cycle latency

- **64-Kbyte 2-way Associative Parity-Protected L1 Instruction Cache**

  With advanced branch prediction

- **16-way Associative ECC-Protected L2 Cache**

  Exclusive cache architecture.storage in addition to L1 caches

  256 KB, 512 KB, and 1 MB options

- **Machine Check Architecture**

  Includes hardware scrubbing of major ECC-protected arrays

- **Power Management**

  Multiple low-power states

  System Management Mode (SMM)

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ACPI 2.0 compliant, including support for processor performance states

- **Power Supplies**

  VDD (core): 1.50-V at 52 Amps (max)

  VDDIO: 2.5-V at 3.0 Amps (max) for DDR I/O

  VLDT: 1.2-V at 0.5 Amps for HyperTransport

  VTT: 1.25-V at 0.5 Amps required for 2.5-V I/Os

  Target CPU Core Power: 78.00 Watts

  Target Maximum Thermal Power: 89 Watts

- **Electrical Interfaces**

  HyperTransport. Technology: LVDS-like differential, unidirectional

  DDR: SSTL per JEDEC DDR specification

  Clock, reset, and test signals also use DDR-like electrical specifications

- **Packaging**

  754-pin lidded micro PGA

  1.27-mm pin pitch

  29x29 row pin array

  40mm x 40mm organic substrate, Organic C4 die attach

1.2.2 System frequency

1.2.2.1 System frequency synthesizer_ICS950402

Programmable Timing Control Hub™ AMD-K8™ processor

General Description

The **ICS950403** is a main system clock solution for desktop designs using the AMD K8 CPU. It provides all necessary clock signals for Clawhammer and Sledgehammer systems.

The **ICS950403** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Recommended Application:

- AMD K8 System Clock with AMD or VIA Chipset
- Output Features:
- 2 - Differential pair push-pull K8 CPU clocks
- 9 - PCICLK (Including 1 free running) @3.3V
- 3 - Selectable PCICLK/HTTCLK @3.3V
- 1 - HTTCLK @3.3V

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- 1 - 48MHz, @3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 3 - REF @3.3V, 14.318MHz.

Features:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew..
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.
- Supports Hyper Transport Technology (HTTCLK).

1.2.3 VIA K8T800+VT8235

1.2.3.1 K8T800

The **K8T800** is a high performance, cost-effective and energy efficient solution for the implementation of desktop personal computer systems with 8 / 16-bit 800 / 600 / 400 / 200 MHz HyperTransport. CPU host interface based on AMD K8 / ClawHammer. processors.

Defines Highly Integrated Solutions for Performance PC Desktop Designs

- High performance North Bridge with HyperTransport. interface to AMD. K8 CPU plus AGP 8x external bus to external Graphics Controller plus high-speed V-Link interface to chipset South Bridge
- Combines with VIA K8T400M V-Link South Bridge for integrated LAN, Audio, ATA133 IDE, and 6 USB 2.0 ports
- 578 Ball Grid Array package with 35 x 35 mm body size, 1.27mm ball pitch, and heat spreader
- 2.5V core, 0.22 u process

High Performance K8 CPU Interface

- Chipset support for AMD. K8 / ClawHammer. processor
- Processor interface via HyperTransport. bus
- Separate transmit and receive buses for no lost bus turnaround cycles
- All transmit and receive signals use 2 pin low-voltage-swing differential signalling for high-reliability and high speed

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- 8 or 16-bit control / address / data transfer both directions
- 800 / 600 / 400 / 200 MHz Double Data Rate operation both directions
- Default 8-bit / 200 MHz operation on startup for high reliability with speedup to dual 16-bit, 800 MHz operation (3.2 GB/sec total bandwidth) under software control (transmit and receive may be different widths and / or speeds)

Full Featured Accelerated Graphics Port (AGP) 8x Controller

- Supports 533 MHz 8x, 266 MHz 4x, and 133 MHz 2x transfer modes for AD and SBA signaling
- AGP v3.0 compliant with 8x transfer mode
- Pseudo-synchronous with the host CPU bus with optimal skew control
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
- AGP pipelined split-transaction long-burst transfers up to 1GB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (256 bytes)
- Sixteen level (quadwords) write data FIFO (128 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
- One level TLB structure
- Sixteen entry fully associative page table

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- LRU replacement scheme
- Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / 2000 / XP miniport driver support

High Bandwidth 533 MB / Sec 8-bit V-Link Host Controller South Bridge Interface

- Supports 66 MHz V-Link Host interface with total bandwidth of 533 MB/sec
- Operates in 2x, 4x, and 8x modes
- Full duplex commands with separate command / strobe
- Request / Data split transaction
- Configurable outstanding transaction queue for Host to V-Link Client accesses
- Supports Defer / Defer-Reply transactions
- Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency
- All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
- Highly efficient V-Link arbitration with minimum overhead
- All V-Link transactions have predictable cycle length with known command / data duration

1.2.3.2 VT8235

The VT8235 South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 includes standard intelligent peripheral controllers:

a) IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHYceiver.

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 also supports the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235 includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

i) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of onboard peripherals for Windows family compliance. The VT8235 also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

1.2.4 RADEON MOBILITY 9600

General Description

The RADEON MOBILITY 9600 provides the fastest and most advanced 2D, 3D, and multimedia graphics performance for the latest applications in full 32-bit color. Its architecture introduces the latest achievements in the graphics industry, which enable the use of the progressive new features in upcoming applications, but without compromising performance. ATI's exclusive support of DirectX® 9.0 features, highly optimized OpenGL® support, and flexible memory configurations allow implementations targeted at both gaming enthusiast and workstation platforms.

SMARTSHADER™ — Advanced Shader Technology

- Provides complete hardware-accelerated support for the new DirectX® 9.0 programmable shader model, enabling more complex and realistic texture and lighting effects than ever before.
- Significant improvement over first-generation shaders introduced in DirectX® 9.0, with a much more powerful and intuitive instruction set.
- Offers full support for this feature in OpenGL® applications.

SMOOTHVISION™ — Flexible Anti-Aliasing and Anisotropic Filtering

- The most flexible and efficient anti-aliasing implementation available to date.
- Eliminates "jaggies" on the edges of objects, shimmering pixels on distant surfaces, and other visual artifacts for smoother-looking images.
- Offers full support for this feature in OpenGL® applications.

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- The most flexible and efficient anti-aliasing implementation available to date.
- Eliminates “jaggies” on the edges of objects, shimmering pixels on distant surfaces, and other visual artifacts for smoother-looking images.
- Unique adaptive process can independently select the anti-aliasing pattern for each pixel within a 4x4 region, rather than relying on a fixed pattern for the whole image.
- Better visual quality with minimal performance degradation.
- Supports DirectX® 9.0 multisampling and related effects, including motion blur and depth-of-field.

High Performance Memory Support

- Incorporates support for DDR SDRAM/SGRAM at up to 350 MHz.
- Features ATI’s second generation HYPER Z™III technology that conserves memory bandwidth for improved performance in demanding applications.
- Boosts effective memory bandwidth by over 20%.

Dual Display Support

- Leading-edge technology, fully optimized with HYDRA VISION™, flexibly supports multiple combinations of traditional CRT monitors, flat panel displays and TV.
- Features Dual Channel DVI support.
- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support.

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- Comprehensive AGP support including 1.5 Volt (AGP 4X) and 0.8 Volt (AGP8X) mode operation, sideband addressing, AGP texturing (direct memory execution), and support for AGP reads and writes, including fast write capability.
- Single channel 128/64-bit memory interface using SGRAM or SDRAM to build 8/16/32/64 MB configurations. Operating frequency is 67MHz minimum to 350MHz maximum, SDR or DDR.
- 16-bit Zoom Video port.
- Support for ROM or Flash RAM parallel or serial video BIOS.
- Two independent CRT controllers to support two asynchronous simultaneous display paths.
- Integrated DAC for CRT with stereoscopic display support.
- Integrated second DAC for the second CRT (TV) support.
- Integrated LVDS interface: single and dual pixel per clock, up to 85MHz per channel.
- LCD panel detection.
- Integrated TMDS transmitter running up to 165MHz (when matched with coherently clocked receiver; otherwise, 135MHz) for support up to 1600x1200 at 60Hz. Fully compliant with DVI and DFP connection standards. Radiometric expansion.

Ideal for Windows 2000 and Windows XP

- RADEON MOBILITY 9600 provides comprehensive support for all new Windows 2000 and Windows XP display-oriented features, including acceleration of new GDI extensions like Alpha BLTs, Transparent BLTs, and Gradient Fills, as well as exclusive, patent-pending hardware alpha cursor support.

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1.2.4.1 General and Interfacing Features

- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support.
- Comprehensive AGP support including 1.5 Volt (AGP 4X) and 0.8 Volt (AGP8X) mode operation, sideband addressing, AGP texturing (direct memory execution), and support for AGP reads and writes, including fast write capability.
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- Support for external TMDS transmitter via 24-bit digital output to drive most popular TMDS transmitters up to 165MHz frequency.
- Internal and external Spread Spectrum support.
- Integrated enhanced TV encoder with 10-bit DAC (shared between second CRT DAC and TV).

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- Independent DDC lines for DAC and TMDS connections. Also full AppleSense support on DAC connection. Static and dynamic Power Management support (APM as well as ACPI) with full VESA DPMS and Energy Star compliance.
- PCI bus power management 1.1 and AGP Busy and Stop signals Rev 1.61 and Solano 2-M.
- Full POWERPLAYTM and POWER ON DEMAND support.
- Comprehensive testability including full internal scan, memory BIST, I/O XOR tree and Iddq. Ideal accelerator for Windows 2000 and Windows XP - includes patent pending hardware support for the Windows 2000 and Windows XP alpha cursor, as well as acceleration of new GDI extensions such as Alpha BLTs, Transparent BLTs, and Gradient Fills.
- Fully compliant with PC 2001 requirements.
- Fully compliant with Mobile PCI rev 1.0.
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management, including PCI power management registers.
- Bi-endian support for compliance on a variety of processor platforms.
- Unique enhanced TCA (Triple-Cache Architecture) incorporates texture, pixel and vertex caches to maximize effective memory bandwidth.
- CCE high-speed pull architecture software interface optimized for Pentium III/4 and Athlon systems:
  - Bus mastering of 2D&3D display lists.
  - Direct walk of Direct3D/OpenGL vertex list.
  - Ultra-thin driver layer.
  - Maximizes concurrency between RADEON MOBILITY 9000 and host.
- Triple 10-bit palette DAC supports pixel rates to 400MHz.

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- DDC1 and DDC2ci for plug and play monitors.
- Hydravision for dual monitor support.
- Hardware I2C.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- High quality components through at-speed testing, built-in Scan, Iddq, CRC, chip diagnostics, and XOR tree.
- Single chip solution in 0.15 micron, 1.2V-1.5V CMOS technology in 696 BGA and 648 BGA package.
- Flexible memory support:
  - SGRAM or SDRAM.
  - SDR or DDR.
  - DDR support for both system memory SDRAM and graphics SGRAM devices.
  - 128-bit or 64-bit interface.
  - 8MB to 64MB.
- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language support (contact ATI for current list).
- Dual RGB CRT output with DDC.
- Integrated enhanced TV encoder based on Rage Theater support at 1024x768.
- HDCP 1.0 support on integrated TMDS transmitter.
- Digital interface with external TMDS Tx with dedicated DDC, configurable as a 24 bit SDR bus or a 12 bit DDR bus.
- Independent h/w icon & h/w cursor on both display paths (simultaneous h/w cursor & icon).
- IEEE 1149.1 Scan path interface.
- VIP 2.0 with multi channel DMA transfer. Support for Rage Theater via VIP.

1.2.5 AC'97 AUDIO SYSTEM: C-MEDIA ELECTRONICS INC., CMI9738-S

The CMI9738-S is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems,including host/soft audio and AMR/CNR based designs. The CMI9738-S incorporates proprietary converter technology to achieve a high SNR, greater than 90 dB. The CMI9738-S AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The CMI9738-S CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs.

Features

- Single chip audio CODEC with high S/N ratio (>90dB)
- Compliant with AC'97 2.2 & WHQL specifications
- Support of S/PDIF out is compliant with AC'97 rev2.2 specifications
- Meets performance requirements for audio on PC2001 systems
- Meets Microsoft PC99 & WLP 2.0 audio requirements
- 18-bit Stereo full-duplex CODEC with independent and variable sampling rate
- 18-bit ADC and 20-bit DAC resolution
- Four analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO, AUX
- High quality differential CD input
- Two analog line-level mono input: PC_BEEP,PHONE_IN
- Supports double sampling rate (96KHz) of DVD audio playback
- Two software selectable MIC inputs

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- +30dB boost preamplifier for MIC input
- Stereo output with 6-bit volume control
- Mono output with 5-bit volume control
- Headphone output with 50mW/8. Driving capability
- Line output with 50mW/8. driving capability
- Headphone jack-detect function to mute LINE/MONO/HP output, and to control S/PDIF output
- 3D Stereo Enhancement
- Multiple CODEC extension capability
- External Amplifier Power Down (EAPD) capability
- High performance converter technology
- Power management and enhanced power saving features
- 2 GPIO pins
- No external crystal/clock required
- 14.318MHz 24.576MHz PLL saves crystal
- DC Voltage volume control
- Auxiliary power (VAUX) to support Power Off CD function
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-Pin LQFP Package

1.2.6 MDC: PCTel MODEM DAUGHTER CARD PCT2303W

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chip set is fully programmable to meet worldwide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

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Operating System Compatibility

- Windows 98 / NT4.0 /Win 2K /Win XP

Compatibility

ITU-T V.90	56000,54667,53333,52000,50667,49333,48000,46667,45333, 42667,41333,40000,38667,37333,36000,34667,33333,32000, 30667,29333, 28000bps
K56Flex	56000,54000,52000,50000,48000,46000,44000,42000,40000, 38000,36000, 32000bps.
ITU-T V.34Annex	33600,31200 bps.
ITU-T V.34	28800 bps
ITU-T V.32bis	14400 bps
ITU-T V.32	9600,4800 bps
ITU-T V.22bis	2400 bps
ITU-T V.22	1200 bps
ITU-T V.21	300 bps
ITU-T V.23	1200/75 bps
ITU-T V.17	14400,12000,9600,7200 bps
ITU-T V.29	9600,7200 bps
ITU-T V.27ter	4800,2400 bps

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- Bell 212A 1200 bps
- Bell 103 300 bps

Modulation

- 56000bps(V90&K56Flex) PCM
- 33600 bps (V.34Annex) TCM
- 28800 bps (V.34) TCM
- 14400 bps (V.32bis) TCM
- 12000 bps (V.32bis) TCM
- 9600 bps (V.32bis) TCM
- 7200 bps (V.32bis) QAM
- 9600 bps (V.32) TCM, QAM
- 4800 bps (V.32) QAM
- 14400 bps (V.17) TCM
- 12000 bps (V.17) TCM
- 9600 bps (V.29) QAM
- 7200 bps (V.29) QAM
- 4800 bps (V.27ter) DPSK
- 2400 bps (V.27ter) DPSK
- 2400 bps (V.22bis) QAM

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- 1200/75bps (V.23) FSK
- 1200bps(V.22/Bell 212A) DPSK
- 300bps(V.21/Bell 103) FSK

Data Compression

- V.42bis, MNP5

Error Correction

- V.42 LAPM, MNP 2-4

DTE interface

DTMF Tone Frequency

Low Group Frequency (Hz)

		697	770	852	941
High Group	1209	1	4	7	*
Frequency	1336	2	5	8	0
(Hz)	1477	3	6	9	#
	1633	A	B	C	D

DTMF signal level

2.6.1.1 High group -10+/-2dBm

2.6.1.2 Low group -12+/-2dBm

Dialing Type

- Tone or pulse dialing

Telephone Line interface

- RJ-11

Return Loss

- 300HZ - 3400HZ >= 10db

Flow Control

- XOFF/XON or RTS/CTS

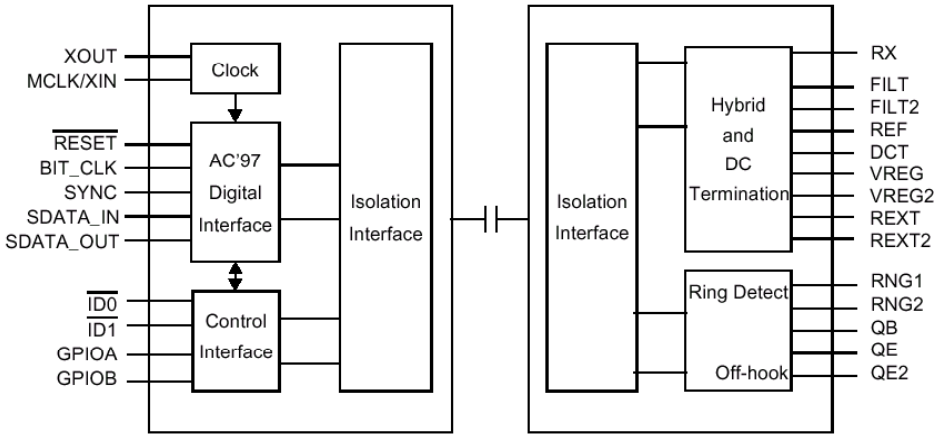
Receive Level

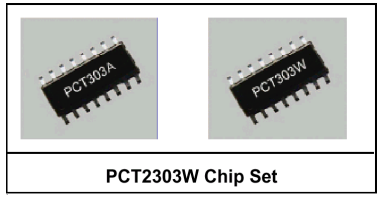
- -35 +/- 2dBm

Transmit Level

- >-15 dBm

Specification and features subject to change without notice!





PCT2303W Chip Set

2.6 MDC: PCTel MODEM DAUGHTER CARD PCT2303W

1.2.7 VT6307L PCI 1394a Integrated Host Controller

1.2.7.1 Overview

The VT6307L IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus a specification release 1.0 and 1394a P2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface.

The VT6307L supports 100, 200 and 400 Mbit/sec transmission via an integrated 2-port PHY. The VT6307L services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The VT6307L is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6306 is built into Microsoft Windows 98, Windows ME, and Windows 2000.

1.2.7.2 Integrated 400 Mbit 2-Port PHY

- Supports provisions of IEEE 1394-1995 Standard for High Performance Serial Bus and the P1394a P2000.
- Fully interoperable with IEEE Std 1394-1995 devices
- Provides two 1394a fully compliant cable ports at 100 / 200 / 400 Mbit per second
- Host notification of PHY LinkOn events
- Full 1394a P2000 Support includes:

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- Arbitrated short reset
- Enhanced priority arbitration
- Connection debounce
- Multispeed packet concatenation
- Ack accelerated arbitration
- Fly-by concatenation
- Per port disable, suspend, resume, through register write and remote command packet
- Remote access packet
- Boundary node short reset
- No PHY_ID wrap past 63

- Logic performs bus initialization and arbitration functions
- Encode and decode functions included for data-strobe bit-level encoding
- Incoming data resynchronized to local clock.
- 24.576 MHz crystal oscillator and PLL provide TX/RX data at 100/200/400 Mbps and Link-Layer Controller clock at 49.152 MHz.
- Cable power presence monitoring.
- Programmable node power class information for system power management
- Fully Compliant 1394a P2000 PHY register map
- Separate TPBIAS for each port
- Cable ports monitor line conditions for active connection to remote node
- Automatic power down inactive circuit and logic for low power application
- Self power up reset and pinless PLL to reduce passive component counts on system

- Automatic configuration to single-port, two-port, and three-port applications; unused ports power down automatically
- Dedicated power supply pins separate from link core
- 2KV ESD protection

1.2.8 EMBEDDED CONTROLLER-H8

I. OVERVIEW

H8/300 CPU, a high-speed processor with an architecture featuring powerful bit-manipulation instructions, ideally suited for real time control applications.

1.2.8.1 Main Features

CPU

- Two-way generate register configuration
  - Eight 16-bit registers, or
  - Sixteen 8-bit registers
- High-speed operation Maximum clock rate (ø clock): 16 MHz at 5 V, 12 MHz at 4 V or 10 MHz at 3V
  - 8- or 16-bit register-register add/subtract: 125 ns (16 MHz), 167 ns (12 MHz), 200 ns (10 MHz)
  - 8 x 8-bit multiply: 875 ns (16MHz), 1167 ns (12 MHz), 1400 ns (10 MHz)
  - 16 ÷8-bit divide: 875 ns (16MHz), 1167 ns (12 MHz), 1400 ns (10 MHz)
- Streamlined, concise instruction set

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- Instruction length: 2 or 4 bytes
- Register-register arithmetic and logic operations
- MOV instruction for data transfer between registers and memory

- Instruction set features
  - Multiply instruction (8 bits x 8 bits)
  - Divide instruction (16 bits ÷8 bits)
  - Bit-accumulator instructions
  - Register-indirect specification of bit positions

Memory

- 1. 60-kbytes ROM with 2-kbytes RAM

Timer

- One 16-bit free running timer
- Two 8-bit timers
- Two PWM timers (duty cycle 0-100%, resolution: 1/250)
- One Watchdog timer

Interface

- Two Serial Communication Interfaces

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- One I^2C bus interface
- Host Interface
  - 8-bit host interface port
  - Three host interrupt requests (HIRQ1, HIRQ11, HIRQ12)
  - Regular and fast A20 gate output
  - Two register sets, each with two data registers and a status register

A/D converter –

- 10-bit resolutions
- 8 channels – single or scan mode (selectable)
- Start of A/D conversion can be externally triggered
- Sample-and-hold function

D/A converter –

- 8-bit resolutions
- 2 channels

I/O ports –

- 74 input/output lines (16 of which can drive LEDs)
- 8 input-only lines

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Interrupts –

- 9 external interrupt lines: NMI, IRQ0, to IRQ7
- 26 on-chip interrupt sources

Wait control –

- Three selectable wait modes

Operating modes –

- Expanded mode with on-chip ROM disabled (mode 1)
- Expanded mode with on-chip ROM enabled (mode 2)
- Single-chip mode (mode 3)

Power-down modes –

- Sleep mode
- Software Standby mode
- Hardware Standby mode

Other features –

- On-chip oscillator

1.2.8.2 Features

- Operating voltage: 2.4V~5.5V
- 32/34 bidirectional I/O lines
- One 8-bit programmable timer counter with overflow
- interrupts
- Crystal or RC oscillator
- Watchdog Timer
- 3K_16 program EPROM
- 160_8 data RAM
- One external interrupt pin (shared with PC2)
- HALT function and wake-up feature reduce power
- consumption
- Six-level subroutine nesting
- Bit manipulation instructions
- 16-bit table read instructions
- 63 powerful instructions
- All instructions in 1 or 2 machine cycles
- 20/28-pin SOP, 40-pin DIP, 48-pin SSOP package

1.2.9 System Flash Memory (BIOS)

- 2 M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program.

1.2.10 Memory System

64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)

- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.11 VT6103 FAST ETHERNET 10/100 1-PORT PHY/TRANSCEIVER

OVERVIEW

The VT6103 is a Physical Layer device for Ethernet 10Base-T and 100Base-TX using category 5 Unshielded, Type 1 Shielded, and Fiber Optic cables. This VLSI device is designed for easy implementation of 10 / 100 Mb/s Fast Etherent LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

PRODUCT FEATURES

- Single Chip 100Base-TX / 10Base-T Physical Layer Solution

- Dual Speed – 100 / 10 Mbps
- Half and Full Duplex
- MII Interface to Ethernet Controller
- MII Interface to Configuration & Status
- Optional Repeater Interface
- Auto Negotiation: 10 / 100, Full / Half Duplex
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards
- On Chip Wave Shaping – No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs
  - Link Status
  - Duplex status
  - Speed Status
  - Collision
- 48 Pin SSOP Package

1.2.12 Cardbus/MediaReader Controller

Features

3.3V operation with 5V tolerant

8355 N/B MAINTENANCE

208-pin LQFP / 209-ball LFBGA package for CB710

PCI Interface

- Compliant with PCI Local Bus Specification, Revision 2.2
- PCI Bus Power Management Interface Specification, Revision 1.1
- PCI Mobile Design Guide, Version 1.1
- Advanced Configuration and Power Interface Specification, Revision 1.0

CardBus Interface

- Compliant with PC Card Standard 8.0
- Support Standardized Zoomed Video Register Model
- Support CardBay PC card interface

Smart Card Interface

- Compliant with PC/SC Specification 1.0
- Support ISO7816 T=0 and T=1 asynchronous communication protocols
- Two power enable pins to support 5V and 3V smart cards
- Support programmable card clock frequencies
- Programmable F and D parameters to support different data rates
- One traffic LED pin.

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Secure Digital Interface

- Compliant with SD Memory Card Specification Version 1.0
- Support 4 parallel data lines
- Has an optional reference clock source to control the operating clock frequency
- Up to 10MByte/sec Read/Write rate when the optional reference clock source
- Contains 16 Bytes of data buffer to regulate the data flow between PCI interface

interface

- Support Write Protect Switch
- Support Card Detect either by DAT3 or by dedicated Card Detect Switch
- One Traffic LED pin
- One power enable pin.

Memory Stick Interface

- Compliant with Memory Stick Standard Format Specification Version 1.3
- Has an optional reference clock source to control the operating clock frequency of Memory Stick
- Up to 2.5MByte/sec Read/Write rate when the optional reference clock source is used
- Contains 16 Bytes of data buffer to regulate the data flow between PCI interface and the Memory

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Stick interface

- One Traffic LED pin
- One power enable pin

SmartMedia Interface

- Compliant with SmartMedia Standard 2000.
- Compliant with SmartMedia Interface Library (SMIL) version 1.0
- Two power enable pins to support 5V and 3V SmartMedia cards
- Support hardware ECC (1-bit correction and 2-bits detection) generation
- One traffic LED pin

Interrupt configuration

- Supports parallel PCI interrupts
- Supports parallel IRQ and parallel PCI interrupts
- Supports serialized IRQ and parallel PCI interrupts
- Supports serialized IRQ and PCI interrupts

Power Management Control Logic

- Supports CLKRUN# protocol

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- Supports SUSPEND#
- Supports PCI PME# from D3, D2, D1 and D0
- Supports PCI PME# from D3Cold
- Supports D3STATE#

Supports Zoomed Video port.

Power Switch Interface

- Supports parallel 4-wire power switch interface

Misc Control Logic

- Supports socket activity LED
- Supports 12 GPIOs and GPE#
- Supports SPKROUT, CAUDIO and RIOUT#
- Supports PCI LOCK

1.2.13 SuperI/O-PC87393

General Description

National Semiconductor's PC87393 of LPC SuperI/O devices is targeted for a wide range of portable applications. PC99 and ACPI compliant, the PC87393 features an X-Bus Extension for read and write operations over the X-Bus, a full IEEE 1284 Parallel Port with a Parallel Port Multiplexer (PPM) for external Floppy Disk Drive (FDD) support, a Musical Instrument Digital Interface (MIDI) port, and a

Game port. Like all National LPC SuperI/O devices, the PC87393 offers a single-chip solution to the most commonly used PC I/O peripherals.

The PC87393 also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serializer for Parallel IRQs and an enhanced WATCHDOG™ timer.

Outstanding Features

- X-Bus Extension for read and write operations
- LPC bus interface, based on Intel's LPC Interface Specification Rev. 1.01, February 1999 (supports CLKRUN and LPCPD signals) and Intel FWH transactions
- PC99 and ACPI compliant
- Serial IRQ support (15 options)
- Interrupt Serializer (four Parallel IRQs to Serial IRQ)

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- PPM for external FDD signal support
- MIDI interface compatible with MPU-401 UART mode
- Game port inputs for up to two joysticks
- Protection features, including GPIO lock and pin configuration lock
- 32 GPIO ports (16 standard, 16 with Assert IRQ/SMI)
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 100-pin TQFP Package

1.3 Other Functions

1.3.1 Hot Key Function

Keys combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Reserve	
Fn + F4	Reserve	
Fn + F5	Display switch	LCD->CRT->LCD&CRT, TV-out will be not TV present. TV->CRT->TV&CRT, TV-out is connected.
Fn + F6	Brightness down	Adjust LCD panel backlight darkness.
Fn + F7	Brightness up	Adjust LCD panel backlight lightness.
Fn + F8	MAX brightness toggle	Toggle LCD brightness maximum or user setting
Fn + F9	Reserved	
Fn + F10	Battery Low Warning Beep toggle	Toggle to enable/mute the “Battery Low Warning” Beep sound
Fn + F11	LCD panel toggle on/off	Toggle LCD panel on or off.
Fn + F12	System sleep	System sleep button function.

1.3.2 Power ON/OFF/Suspend/Resume Button

APM mode

At APM mode, Power button is on/off system power.

ACPI mode

At ACPI mode. Power button behavior was set by windows power management control panel.

You could set “standby” , “power off” or “hibernate”(must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

System has eight status LED indicators at front side which to display system activity. From left to right that indicate, AC POWER, BATTERY POWER, BATTERY STATUS, WIRELESS LAN, CD-ROM, HARD DISK, NUM LOCK, CAPS LOCK and SCROLL LOCK.

AC POWER: This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.

BATTERY POWER: This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.

BATTERY STATUS: During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

1.3.5 Fan power on/off management

FAN is controlled by H8 embedded controller-using AD2201 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.6 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.
- Battery was put in battery holder, can be replaced.

1.3.7 I/O Port

- Bi-directional Parallel Port (EPP/ECP) x 1
- USB port (2.0, backward compatible with USB1.1) x 4
- RJ-11 port x 1
- RJ-45 port x 1
- IR port x 1, complies with IrDA 1.1
- DC input x 1
- VGA monitor port x1
- Audio-out x 1 (S/P DIF)
- Mic-in x 1
- Hardware Volume Control
- S Video TV-Out x 1 (NTSC/PAL)

- IEEE1394a x 1

1.3.8 Mini PCI (type III B)Battery current limit and learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Peripheral Components

ROM Drive	- 12.7mm Height - 24X CD ROM Drive - 8X DVD ROM Drive - 24X10X8X24 Combo or above - Super Combo DVD-RW module
HDD	- 2.5" 9.5 mm height: 20/30/40/60 GB; Support Ultra DMA 66/100/133 - Changeable for Distributor
FDD	- Support External FDD w/z USB I/F; 3.5 Format for 720KB/1.2MB/1.44MB
Display	- 14.1" XGA TFT Display; Resolution: 1024x768 - 15" XGA/ SXGA+ TFT Display; Resolution: 1024X768 /1400x1050
Keyboard	- 19mm key pitch/ 3.0mm key stroke/ 307mm length - Windows Logo Key x 1; Application Key x 1
I/O Port	- Bi-directional Parallel Port (EPP/ECP) x 1 - USB port (2.0, backward compatible with USB1.1) x 4 - RJ-11 port x 1 - RJ-45 port x 1 - IR port x 1, complies with IrDA 1.1 - DC input x 1 - VGA monitor port x1 - Audio-out x 1 (S/P DIF) - Mic-in x 1 - Hardware Volume Control - S Video TV-Out x 1 (NTSC/PAL) - IEEE1394a x 1 - Mini PCI (type III B)
Communication	- Built-in 56Kbps V.90 modem - Built-in 10/100 M based-T LAN - One Mini PCI slot and one antenna reserved for wireless LAN(Type III B)
Battery	- 12 cell (2200mAH/3.7V) Li-ion standard
AC adapter	- Universal AC adapter 150W ; Input: 100-240V, 50/60Hz AC (support power on charge)

1.5 Power Management

The 8355 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

Full on mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.
The CPU power consumption and temperature is lower in this mode.

Standby mode

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- CPU: Stop grant
- LCD: backlight off

- HDD: spin down

Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

Suspend to DRAM

CPU: off
VT8235: Partial off
VGA: Suspend
PCMCIA: Suspend
Audio: off
SDRAM: self refresh

Suspend to HDD

All devices are stopped clock and power-down
System status is saved in HDD
All system status will be restored when powered on again

1.5.2 Other Power Management Functions

HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 Appendix 1: VT 8235 GPIO Definition

Signal Name	MUX Function	Mitac Definition	Buffer Type	Power Plane	Default Value	Type
GPI0		RESERVE	I	RTC	Hi-Z	TTL
GPI1		RESERVE	I	AUX	Hi-Z	TTL
GPI2	EXTSMI#	EXTSMI#	I	AUX	Defined	TTL
GPI3	RING#	WAKE_UP#	I	AUX	Defined	TTL
GPI4	LID#	RESERVE	I	AUX	Defined	TTL
GPI5	BATLOW#	SCI#	I	AUX	Defined	TTL
GPI6	AGPBZ#	RESERVE	I	MAIN	Defined	TTL
GPI7	REG5#	RESERVE	I	MAIN	Hi-Z	TTL
GPI16	INTRUDER#	RESERVE	I	RTC	Defined	TTL
GPI17	CPUMISS	RESERVE	I	MAIN	Defined	TTL
GPI18	THRM# / AOLGPI	THRM#	I	MAIN	Defined	TTL
GPI19	IORDY	RESERVE	I	MAIN	Defined	TTL
GPO0		RESERVE	O	AUX	H	TTL
GPO1	SUSA#	SUSA#	O	AUX	Defined	TTL
GPO2	SUSB#	SUSB#	O	AUX	Defined	TTL
GPO3	SUSST1#	SB_SUSST#	O	AUX	Defined	TTL
GPO4	SUSCLK	RESERVE	O	AUX	Defined	TTL
GPO5	CPUSTP#	RESERVE	O	MAIN	Defined	TTL
GPO6	PCISTP#	PCISTOP#	O	MAIN	Defined	TTL
GPO7	GNT5#	RESERVE	O	MAIN	Defined	TTL

Continued to the previous table

GPIO8	PCREQA / VGATE	MB_ID0	I/O	MAIN	Hi-Z	TTL
GPIO9	PCREQB	MB_ID1	I/O	MAIN	Hi-Z	TTL
GPIO10		KBD_CS0	I/O	MAIN	Hi-Z	TTL
GPIO11		KBD_CS1	I/O	MAIN	Hi-Z	TTL
GPIO12	INTE# / PCGNTA	RESERVE	I/O	MAIN	Hi-Z	TTL
GPIO13	INTF# / PCGNTB	RESERVE	I/O	MAIN	Hi-Z	TTL
GPIO14	INTG#	CRT_IN	I/O	MAIN	Hi-Z	TTL
GPIO15	INTH#	MPCIACT#	I/O	MAIN	Hi-Z	TTL
GPIO20	ACSDIN2 / PCS0#	RESERVE	I/O	MAIN	Hi-Z	OD
GPIO21	ACSDIN3 / PCS1# / SLPBTN#	RESERVE	I/O	MAIN	Hi-Z	OD
GPIO22	GHI#	FAN3_SPDCTR	I/O	MAIN	Hi-Z	OD
GPIO23	DPSLP#	LDTSTOP#	I/O	MAIN	Hi-Z	OD
GPIO24	GPIOA	SPKR_MUTE#	I/O	MAIN	Hi-Z	OD/TTL
GPIO25	GPIOC	FAN2_SPDCTR	I/O	MAIN	Hi-Z	OD/TTL
GPIO26	SMBDT2	RESERVE	I/O	AUX	Hi-Z	OD
GPIO27	SMBCK2	RESERVE	I/O	AUX	Hi-Z	OD
GPIO28	VIDSEL	RESERVE	I/O	MAIN	Hi-Z	OD
GPIO29	VRDSLP	RESERVE	I/O	MAIN	Hi-Z	OD
GPIO30	GPIOD	FAN1_SPDCTR	I/O	MAIN	Hi-Z	OD/TTL
GPIO31	GPIOE	MINIPCI_PD	I/O	MAIN	Hi-Z	OD/TTL

1.7 Appendix 2: H8 Pins Definition

Hitachi H8 3437S to VT8235 pin function definitions for Insyde code

the shadowed block is the selected function

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
MD0	6	H8_MODE0	I ↑	I	H	I	H	I	H	H
MD1	5	H8_MODE1	I ↑	I	H	I	H	I	H	H mode3 single chip mode
STBY#	8	H8_STBY#	I ↑	I	H	I	H	I	H	H8 Hardware Standby input pull high
NMI#	7	PWRBTN#	I ↑	I	H	I	HLH	I	H	Power button
RESET#	1	H8_RESET#	I	I	LH	I	H	I	H	H8 chip reset
XTAL	2	Crystal	I	I		I		I		Crystal input
EXTAL	3	Crystal	I	I		I		I		
RESET OUT#	100	RESERVE	O	O		O		O		
Port A CMOS input level (input high min=3.5v, input low max=1.0v)										
PA0	48	LID#	T ↑	I	H	I		I	H	
PA1	47	ADEN#	T ↑	I	H/L	I		I	H/L	AC adaptor in detect
PA2	31	CARD_RI#	T ↑	I	H	I		I	H	Ring detect
PA3	30	BATT DEAD#	T ↑	I	H	I		I	H	Battery low low detect
PA4	21	H8 SUSC	T ↑	I	H	I		I	L	System resume from S4 soft off through RTC Alarm
PA5	20	H8 SUSC#	T ↑	I	L	I		I	H	System to S4 soft off
PA6	11	BAT_CLK	T ↑	I	L	I		I	H	
PA7	10	H8_SUSB	T ↑	I	H	I	L	I	H	Invert from SUSA# to wake up H8 when system resumed by MDC modem and internal LAN. Inform system power management status

8355 N/B MAINTENANCE

Charging 1

PCI reset gate

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF	ON		STANDBY		Function
Port B TTL input voltage (input high min=2v, input low max=0.8v)									
PB0	91	SB_PWRBTN#	T	O	L	LHL	O	Keep H	Power button trigger via8231 on /off Duplicate Power BTN# 5→3V
PB1	90	H8_WAKE UP#	T	O	H	O	O	Keep H	Wake up SB at ACPI mode 5→3V?
PB2	81	LEARNING	T	O			O	Keep H	Power button trigger via8231 on 5→3V
PB3	80	CHARGING_RP	T	O		O	O	Keep	Battery charge control
PB4	69	VDD5 SW	T↓	O	LLH	O H	O	Keep H	H8 vdd5 power source switch
PB5	68	H8_PWROK	T	O	L	O LH	O	Keep H	
PB6	58	RESERVE	T	O		O	O	Keep	
PB7	57	RESERVE	T	O		O	O	Keep	
Port 1 TTL input voltage (input high min=2v, input low max=0.8v)									
P10/A0	79	KB OUT0	L	O	L	O LH	O	Keep L	Key matrix scan output 0
P11/A1	78	KB OUT1	L	O	L	O LH	O	Keep L	Key matrix scan output 1
P12/A2	77	KB OUT2	L	O	L	O LH	O	Keep L	Key matrix scan output 2
P13/A3	76	KB OUT3	L	O	L	O LH	O	Keep L	Key matrix scan output 3
P14/A4	75	KB OUT4	L	O	L	O LH	O	Keep L	Key matrix scan output 4
P15/A5	74	KB OUT5	L	O	L	O LH	O	Keep L	Key matrix scan output 5
P16/A6	73	KB OUT6	T	O	L	O LH	O	Keep L	Key matrix scan output 6
P17/A7	72	KB OUT7	T	O	L	O LH	O	Keep L	Key matrix scan output 7

Continued to the previous table

Port 2 TTL input voltage (input high min=2v, input low max=0.8v)										
P20/A8	67	KB OUT8	L	O	L	O	LH	O	Keep L	Key matrix scan output 8
P21/A9	66	KB OUT9	L	O	L	O	LH	O	Keep L	Key matrix scan output 9
P22/A10	65	KB OUT10	L	O	L	O	LH	O	Keep L	Key matrix scan output 10
P23/A11	64	KB OUT11	L	O	0	O	LH	O	Keep L	Key matrix scan output 11
P24/A12	63	KB OUT12	L	O	0	O	LH	O	Keep L	Key matrix scan output 12
P25/A13	62	KB OUT13	L	O	0	O	LH	O	Keep L	Key matrix scan output 13
P26/A14	61	KB OUT14	L	O	0	O	LH	O	Keep L	Key matrix scan output 14
P27/A15	60	KB OUT15	L	O	0	O	LH	O	Keep L	Key matrix scan output 15
Port 3 TTL input voltage (input high min=2v, input low max=0.8v)										
P30/HDB0/D0	82	ISA SD0	T	I/O		I/O		I/O	Keep	ISA DATA bit 0
P31/HDB1/D1	83	ISA SD1	T	I/O		I/O		I/O	Keep	ISA DATA bit 1
P32/HDB2/D2	84	ISA SD2	T	I/O		I/O		I/O	Keep	ISA DATA bit 2
P33/HDB3/D3	85	ISA SD3	T	I/O		I/O		I/O	Keep	ISA DATA bit 3
P34/HDB4/D4	86	ISA SD4	T	I/O		I/O		I/O	Keep	ISA DATA bit 4
P35/HDB5/D5	87	ISA SD5	T	I/O		I/O		I/O	Keep	ISA DATA bit 5
P36/HDB6/D6	88	ISA SD6	T	I/O		I/O		I/O	Keep	ISA DATA bit 6
P37/HDB7/D7	89	ISA SD7	T	I/O		I/O		I/O	Keep	ISA DATA bit 7
Port 4 TTL input voltage (input high min=2v, input low max=0.8v)										
P40/TMCI0	49	H8 PWRON	T↓	O	L	O	LH	O	Keep	System power on, need pull down to define initial state during reset
P41/TMO0	50	H8 THRM#	T	O	L	O	H	O	Keep H	Thermal throttling control to Southbridge
P42/TMRI0	51	SCI#/ FAN SPD SW	T	O	H			O	Keep	SCI output and Fan Speed Tachometer Switch
P43/TMCI1/HIRQ1	52	SCI#/ FAN SPEED	T	O/I		O		O	Keep	Need invert to SCI# sending to SB 5→3V/ Fan speed tachometer
P44/TMCO1/HIRQ1	53	ISA IRQ1	T	O	0	O		O	Keep	Keyboard IRQ1
P45/TMRI1/HIRQ1	54	ISA IRQ12	T	O	0	O		O	Keep	PS2 mouse IRQ12
P46/PWM0	55	FAN ON#0	T	O	1	O		O	Keep	Fan power PWM control
P47/PWM1	56	FAN ON#1	T	O	1	O		O	Keep	Fan power PWM control

Continued to the previous table

Port 5 TTL input voltage (input high min=2v, input low max=0.8v)									
P50/TXD0	14	LED DATA	T	O		O	O	Keep	LED indicator shift data
P51/RXD0	13	H8 SMI#	T	O		O	O	Keep	External SMI# 5→3V
P52/SCK0	12	LED CLK	T	O		O	O	Keep	LED indicator shift clock
Port 6 Schmitt trigger input voltage (min=1.0v max=3.5v)									
P60/KEYIN0/FTCI	26	KEY IN0	T ↑	I		I	I	Keep	Key matrix input 0 need pull high
P61/KEYIN1/FTOA	27	KEY IN1	T ↑	I		I	I	Keep	Key matrix input 1 need pull high
P62/KEYIN2/FTIA	28	KEY IN2	T ↑	I		I	I	Keep	Key matrix input 2 need pull high
P63/KEYIN3/FTIB	29	KEY IN3	T ↑	I		I	I	Keep	Key matrix input 3 need pull high
P64/KEYIN4/FTIC	32	KEY IN4	T ↑	I		I	I	Keep	Key matrix input 4 need pull high
P65/KEYIN5/FTID	33	KEY IN5	T ↑	I		I	I	Keep	Key matrix input 5 need pull high
P66/KEYIN6/IRQ6	34	KEY IN6	T ↑	I		I	I	Keep	Key matrix input 6 need pull high
P67/KEYIN7/IRQ7	35	KEY IN7	T ↑	I		I	I	Keep	Key matrix input 7 need pull high
Port 7 TTL input voltage (input high min=2v, input low max=0.8v)									
P70/AN0	38	BAT VOLT1	T	I		I	I	T	Battery voltage measure
P71/AN1	39	I_LIMIT	T	I		I	I	T	
P72/AN2	40	H8_I_DISCHG	T	I		I	I	T	Monitor system on/off state
P73/AN3	41	H8_I_CHG	T	I		I	I	T	
P74/AN4	42	BAT TEMP1	T	I		I	I	T	Battery thermister temperature
P75/AN5	43	VCC CORE	T	I		I	I	T	
P76/AN6/DA0	44	H8_I_CTR	T	O		O	O	T	Charging current adjust
P77/AN7/DA1	45	BL ADJ	T	O		O	O	T	Backlight inverter brightness adjust
Port 8 TTL input voltage (input high min=2v, input low max=0.8v)									
P80/HA0	93	ISA SA2	T	I		I	I	Keep	
P81/GA20	94	RESERVE	T	O		O	O	Keep	
P82/CS1	95	H8 KBCS#	T	I		I	I	Keep	IO port 60/64 chip select
P83/IOR	96	ISA IOR#	T	I		I	I	Keep	ISA I/O read#
P84/IRQ2/TXD1	97	ISA IOW#	T	I		I	I	Keep	ISA I/O write
P85/IRQ4/RXD1	98	H8 MCCS#	T	I		I	I	Keep	IO port 62/66 chip select
P86/IRQ5/SCK1	99	BAT CLK	T ↑	I/O		I/O	I/O	Keep	SM BUS clock need pull high 5→3V

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Continued to the previous table

Port 9 TTL input voltage (input high min=2v, input low max=0.8v)									
P90/IRQ2/ESC2	25	PORT90	T ↑	I/O		I/O	I/O	Keep	
P91/IRQ1/EIOW	24	PORT91	T ↑	I/O		I/O	I/O	Keep	
P92/IRQ0	23	H8/T CLK	T ↑	I/O		I/O	I/O	Keep	need pull high
P93/RD	22	RSMRST	T ↑	I/O		I/O	I/O	Keep	
P94/WR	19	RESERVE	T ↑	I/O		I/O	I/O	Keep	need pull high
P95/AS	18	T DATA	T ↑	I/O		I/O	I/O	Keep	need pull high
P96/0	17	H8_ENABKL	T ↑	I		I	I	T	Read H8 send A20gate status
P97/WAIT/SDA	16	BAT DATA	T ↑	I/O		I/O	I/O	Keep	SM BUS clock need pull high 5→3V

↑ Pull High
↓ Pull Low
5→3V Level shift

1.8 Appendix 3: 8355 product spec.

CPU	- AMD ClawHammer K8 processor with uPGA Package - 2700+/3000+/3300+/3600+/3900+/4200+ - FSB 800MHz
Core Logic	- VIA K8T800 + VT8235
L2 Cache	- 512KB OD
System BIOS	- Insyde 256 KB Flash EPROM (Include System BIOS and VGA BIOS) - ACPI 2.0; DMI 2.3.1 compliant - Plug & Play capability
Memory	- 0MB on board; Expandable up to 1024MB - Expandable with combination of optional 128/256/512 MB memory - 200-pin DDR 266/333/400 DRAM Memory Module x2, PC-2100/2700/3200 specification
ROM Drive	- 12.7mm Height - 24X CD ROM Drive - 8X DVD ROM Drive - 24X10X8X24 Combo or above - Super Combo DVD-RW module
HDD	- 2.5" 9.5 mm height: 20/30/40/60 GB; Support Ultra DMA 66/100/133 - Changeable for Distributor
FDD	- Support External FDD w/z USB I/F; 3.5 Format for 720KB/1.2MB/1.44MB
Display	- 14.1" XGA TFT Display; Resolution: 1024x768 - 15" XGA/ SXGA+ TFT Display; Resolution: 1024X768 /1400x1050
Video Controller	- ATI M10P with 64MB External VRAM (Reserve for 128MB VRAM)
Keyboard	- 19mm key pitch/ 3.0mm key stroke/ 307mm length - Windows Logo Key x 1; Application Key x 1
Button	- 1x Wireless RF switch button with LED
Pointing Device	- Glide pad with 2x buttons and 4 direction scroll button
PCMCIA	- TypeII X1 Without ZV -Cardbus Support
4 in 1 Card reader	- Card Reader SD/SM/MMC

Continued to the previous table

Indictor	- 3 LEDs for Power/Battery status (on display housing) - 1 LED for Radio wave status Power LED (with switch button) - 5 LEDs for HDD Access, ODD Access , Num lock, Cap lock and Scroll Lock . - 1 LED for Card reader status
Audio System	- Sound Blaster Pro compatible - AC97 V2.1 Codec - Built-in Mono Microphone - 2X Speaker (w/z sound chamber)
I/O Port	- Bi-directional Parallel Port (EPP/ECP) x 1 - USB port (2.0, backward compatible with USB1.1) x 4 - RJ-11 port x 1 - RJ-45 port x 1 - IR port x 1, complies with IrDA 1.1 - DC input x 1 - VGA monitor port x1 - Audio-out x 1 (S/P DIF) - Mic-in x 1 - Hardware Volume Control - S Video TV-Out x 1 (NTSC/PAL) - IEEE1394a x 1 - Mini PCI (type III B)
Communication	- Built-in 56Kbps V.90 modem - Built-in 10/100 M based-T LAN - One Mini PCI slot and one antenna reserved for wireless LAN(Type III B)
AC adapter	- Universal AC adapter 150W (3 pins); Input: 100-240V, 50/60Hz AC (support power on charge)
Battery	- 12 cell (2200mAH/3.7V) Li-ion standard
Dimensions	- 332x285x37.1~41.1(max)
Weight	- 3.6kg
Accessories	- Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title
Manual Printings	- EN, GR, CH, Pan-EU

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Continued to the previous table

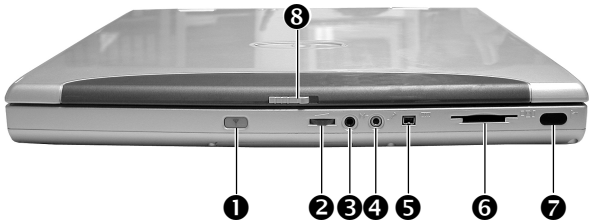
Agency	- FCC, CE, UL, TUV, CB, BSMI
Architecture	- Support PC2001 Specification, Designed for Windows XP(driver ready for 98,ME, and 2000)
Options	- 128/256/512MB DDR SDRAM, AC Adapter w/o Power Cord, Notebook Carry Bag

2. System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Hold Switch
❷ Volume Control
❸ Audio Output
❹ Microphone Input
❺ 1394 port
❻ Card Reader Slot
❼ IR Module
❽ Top Cover Latch

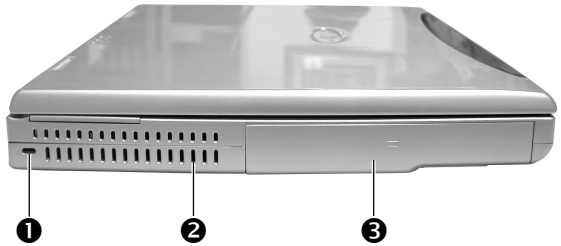


2.1.2 Left-side View

❶ PCMCIA Card Socket
❷ CD/DVD-ROM Drive
❸ RJ-11 Connector
❹ RJ-45 Connector
❺ USB Port*2

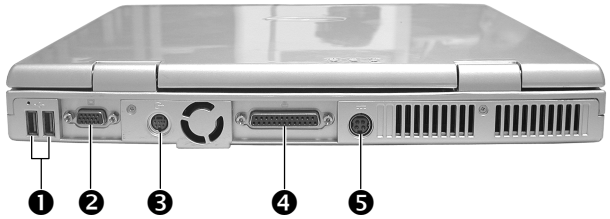
2.1.3 Right-side View

❶ Kensington Lock
❷ Ventilation Openings
❸ Battery pack

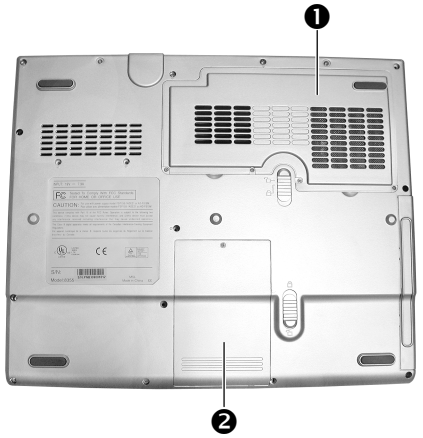


2.1.4 Rear View

❶ USB Port*2
❷ VGA Port
❸ S-Video Output Connector
❹ Parallel Port
❺ Power Connector

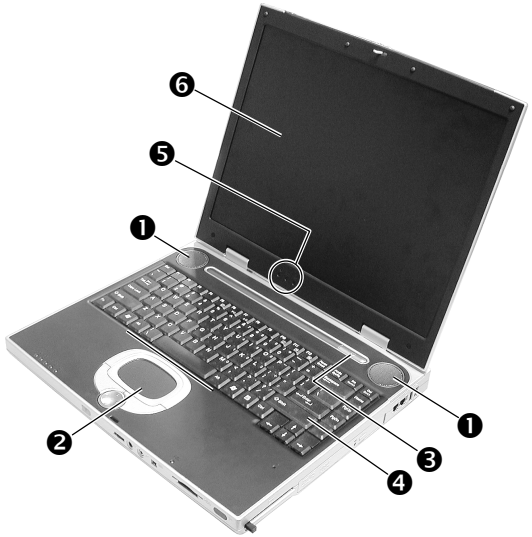


2.1.5 Bottom View



1. CPU Cover
2. Hard Disk Drive Cover

2.1.6 Top View



1. Stereo Speaker
2. Touch Pad
3. Power Button
4. Keyboard
5. Device Indicators
6. LCD Screen

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *1. Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

2. During disassembly, 1) Label each cable as you disconnect it, noting its position and routing;
2) Keep all the screws.

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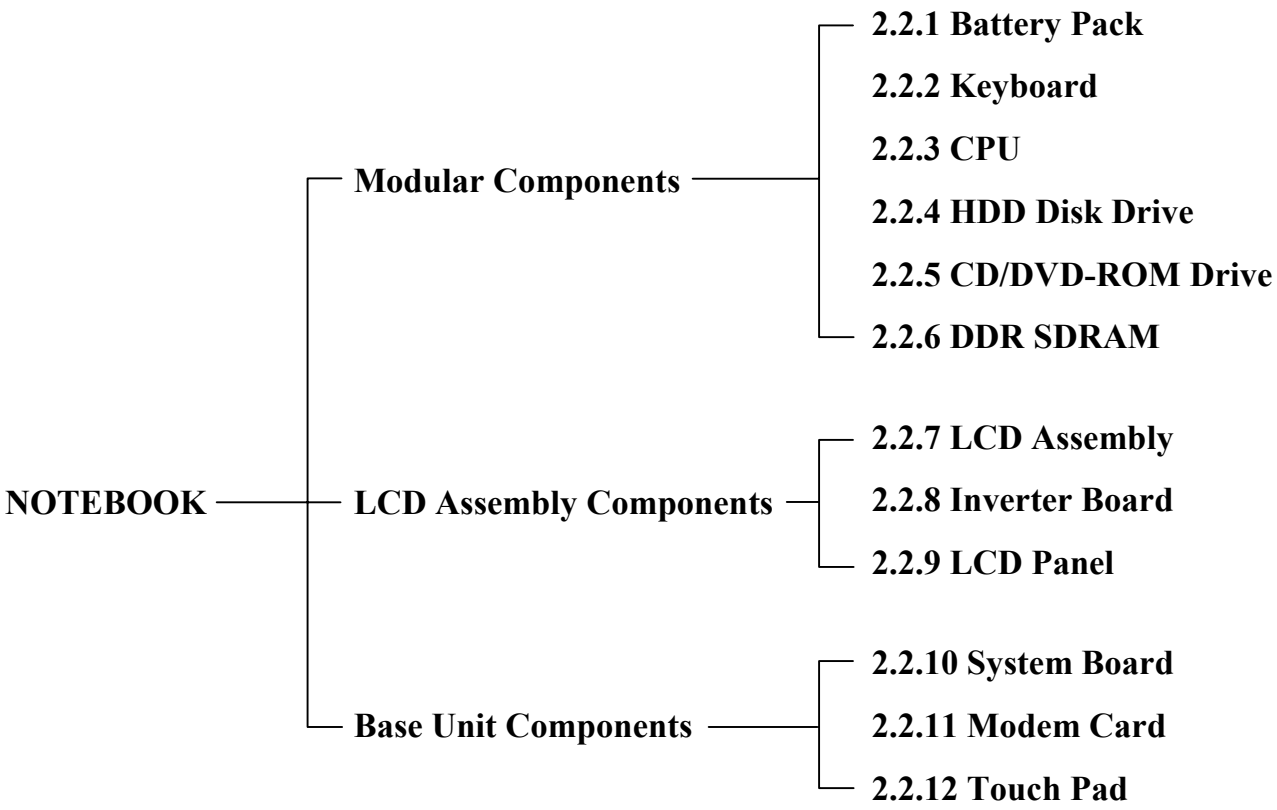


2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide and keep the upper release lever on “unlock” ( ) position (❶), and then pull the battery pack out of the compartment (❷) while sliding the lower release lever downwards to “unlock” ( ) position (❷). (Figure 2-1)

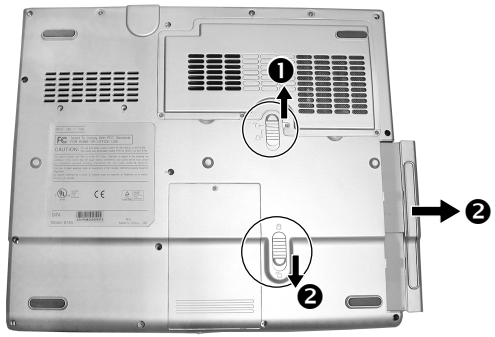


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove three screws that fastening the keyboard cover on the bottom of the notebook. (Figure 2-2)

Figure 2-2 Remove three screws

Figure 2-3 Insert a rod easy to remove

3. Insert a small rod, such as a straightened paper clip, into the eject hole near the USB ports of the notebook. (Figure 2-3)

4. Open the top cover. Slide out the keyboard cover. (Figure 2-4)
5. Remove two screws fastening the keyboard. (Figure 2-5)

Figure 2-4 Slide out the keyboard cover

Figure 2-4 Remove two screws

5. Disconnect the cable from system board. (Figure 2-6)

Figure 2-6 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable.
2. Replace the keyboard and secure with two screws.
3. Replace the keyboard cover and secure with three screws.
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.3 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove four screws that fasten the heatsink compartment covers. (Figure 2-7)

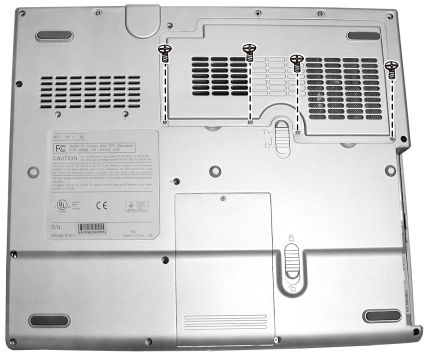


Figure 2-7 Remove four screws

Figure 2-8 Remove the heatsink compartment cover

4. Remove four spring screws fastening the heatsink. (Figure 2-8)

5. Disconnect the fan's power cord to detach the heatsink from the CPU compartment. (Figure 2-9)
6. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-10)

Figure 2-9 Disconnect the fan's cord

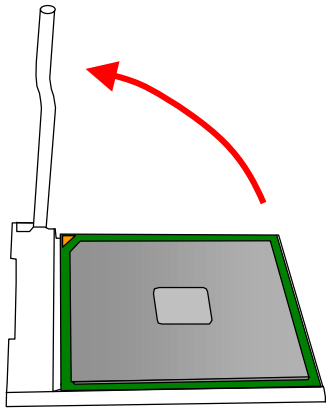


Figure 2-10 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left .
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four spring screws.
3. Replace the heatsink compartment cover and secure with four screws.
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove one screw fastening the HDD compartment cover. Then sliding it outward. (Figure 2-11)

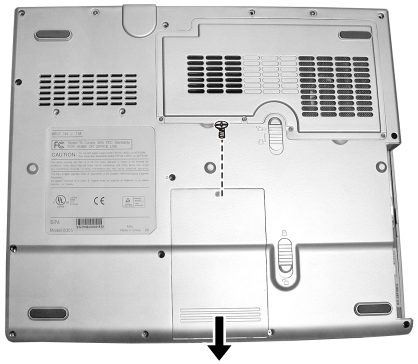


Figure 2-11 Remove HDD compartment cover

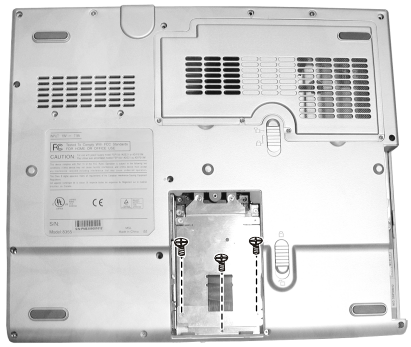


Figure 2-12 Remove three screws that secure the top shielding

4. Remove three screws that secure the top shielding of the hard disk drive. (Figure 2-12)

5. Unscrew two screws to slide out the hard disk drive from the compartment. (Figure 2-13)

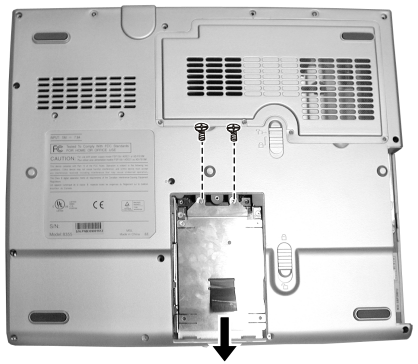


Figure 2-13 slide out the hard disk drive

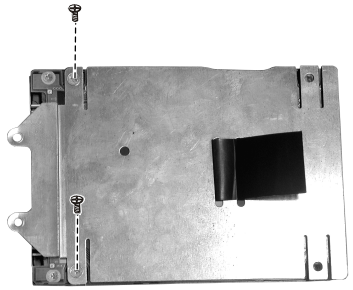


Figure 2-14 Free the hard disk

6. To free the hard disk drive, remove two screws that secure the holding. (Figure 2-14)

Reassembly

1. Fit the hard disk drive into the holding and secure with two screws.
2. Replace the hard disk drive into compartment and secure with two screws.
3. Fit the top shielding and secure with three screws.
4. Replace the HDD's cover and secure with one screw.
5. Then replace battery pack. (See section 2.2.1 Reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove three screws fastening the CD/DVD-ROM drive. (Figure 2-15)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(❷). (Figure 2-15)

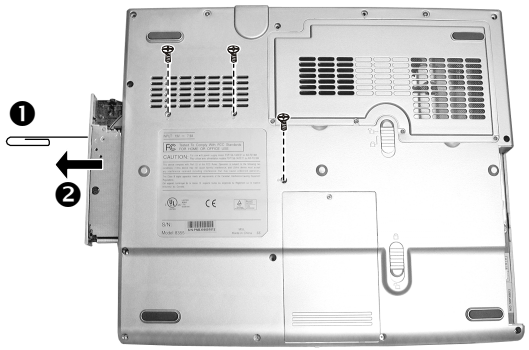


Figure 2-15 Remove the CD/DVD -ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with three screws.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-16)

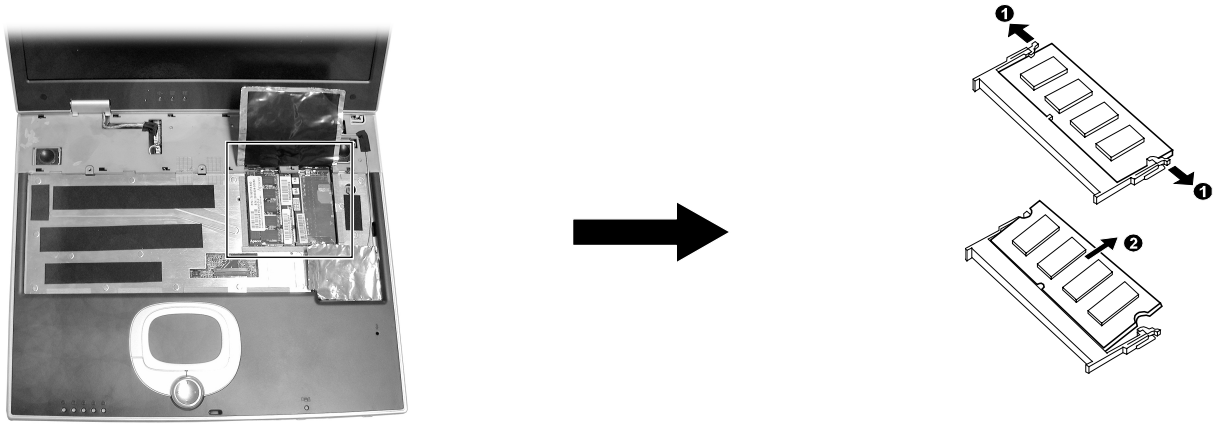


Figure 2-16 Remove the SO-DIMM

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the battery pack and the keyboard. (See sections 2.2.1 and 2.2.2 reassembly)

2.2.7 LCD Assembly

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Remove two screws on the rear side of notebook. (Figure 2-17)
3. Open the top cover. Rip the insulating tape off to free the antenna. (Figure 2-18)

Figure 2-17 Remove two screws

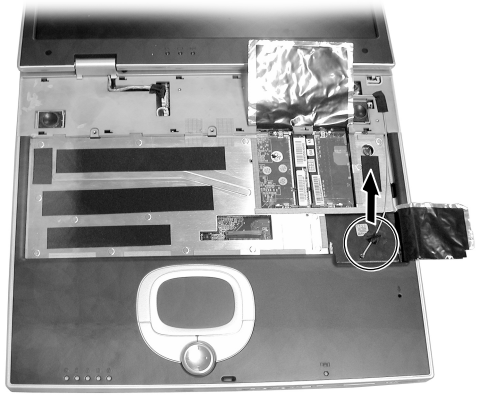


Figure 2-18 Free the antenna

6. Then remove the two hinge covers. (Figure 2-19)
7. Remove two screws of the hinges and disconnect the two LCD wires from the system board. (Figure 2-20)

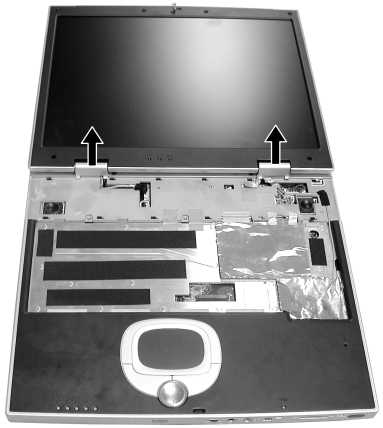


Figure 2-19 Remove the hinge cover

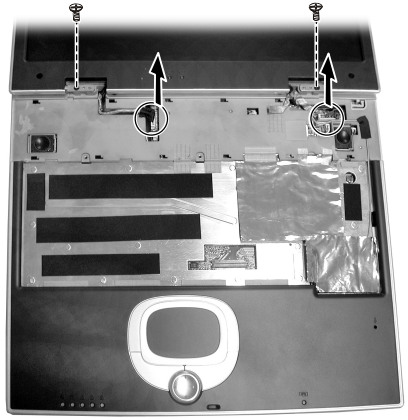


Figure 2-20 Disconnect the two LCD wires

8. Carefully put the notebook upside down,remove two screws of the hinges,Now you can separate the LCD assembly from the base unit. (Figure 2-21)

Figure 2-21 Remove the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws of the hinges.
2. Reconnect the LCD wires to the system board..
3. Fit two hinge covers and secure with two screws.
4. Replace the battery pack and the keyboard. (See section 2.2.1 and 2.2.2 reassembly) .

2.2.8 Inverter Board

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
3. Remove the four rubber pads and four screws. (figure 2-22)
4. Insert a flat screwdriver to the lower part of the top cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
5. Disconnect one wire from inverter board and remove two screws fastening the inverter board. (Figure 2-23)

Figure 2-22 Unscrew four screws

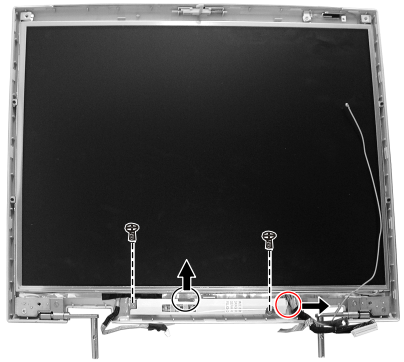


Figure 2-23 Disconnect one cable

Reassembly

1. Fit the inverter board back into place and secure with two screws, and reconnect the wire to the inverter board. .
2. Fit the LCD top cover back into the housing and secure with four screws and four rubber pads
3. Replace the LCD Assembly. (See section 2.2.7 Reassembly)
4. Replace the battery pack and the keyboard. (See section 2.2.1 and 2.2.2 reassembly) .

2.2.9 LCD Panel

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
4. Disconnect one wire from inverter board and remove two screws fastening the inverter board. (Figure 2-22)
5. Remove eight screws. And then lift up LCD panel. (Figure 2-24)
6. To free the LCD panel, remove eight screws. (Figure 2-25)

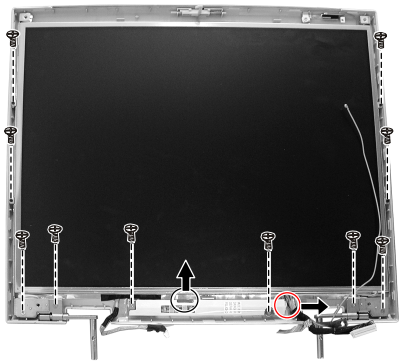


Figure 2-24 Separate the LCD panel

Figure 2-25 Unscrew eight screws

Reassembly

1. Attach the LCD panel holding to panel and secure with eight screws.
2. Fit the LCD panel into place and secure with eight screws.
3. Replace the inverter board. (See section 2.2.8 Reassembly)
4. Replace the LCD assembly. (See section 2.2.7 Reassembly)
5. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.10 System Board

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove nine screws on the bottom of notebook. (Figure 2-26)
5. Turnover the notebook. Remove two screws. And disconnect three wires. (Figure 2-27)

Figure 2-26 Unscrew nine screws

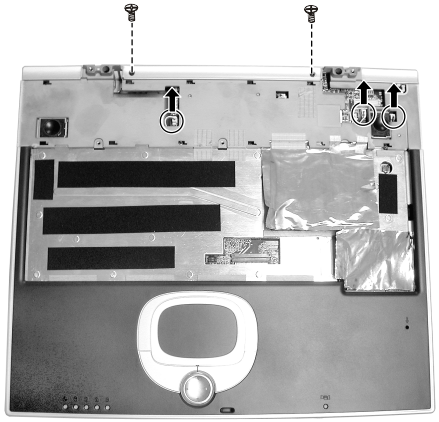


Figure 2-27 Remove two screws

6. Disconnect the touch pad's cable. Then lift up the system top cover. (Figure 2-28)

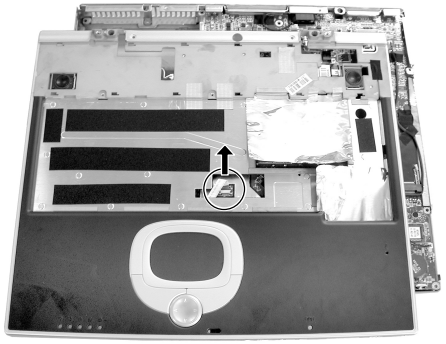


Figure 2-28 Remove the top cover

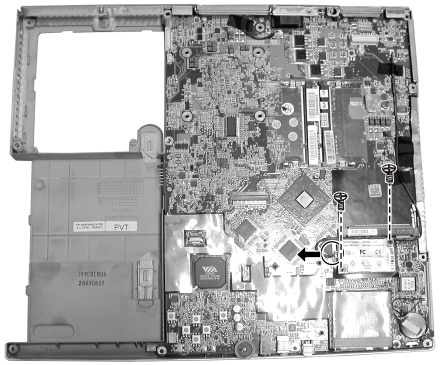


Figure 2-29 Remove the modem card

7. To remove the modem card, remove two screws and disconnect the wire. (Figure 2-29)

8. Unscrew one screw and disconnect fan's cord. (Figure 2-30)

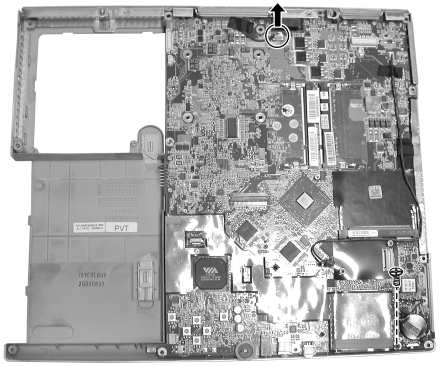


Figure 2-30 Unscrew one screw and disconnect one cord

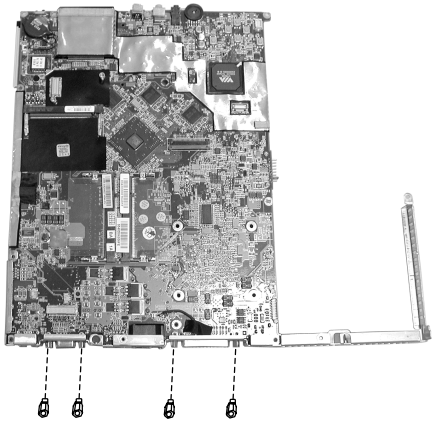


Figure 2-31 Remove four hex nuts

9. Remove four hex nuts beside the VGA port. Now you can lift up system board from housing. (Figure 2-31)

Reassembly

1. Fit the system board back into housing and secure with one screw and four hex nuts.
2. Reconnect the fan's cord.
3. Reconnect the modem card's wire. Fit the modem card and secure with two screws.
4. Fit the top cover. Reconnect the touch pad's cable to system board.
5. Reconnect the speaker's cords to system board.
6. Fasten the top cover by two screws.
7. Put up the notebook upside down. Reconnect the other speaker's cord.
8. Fasten the housing by nine screws.
9. Reassemble the notebook. (See the previous sections Reassembly)

2.2.11 Modem Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps1 to 6 of section 2.2.10 Disassembly)
5. Remove two screws fastening the modem card. disconnect cord from system board. (Figure 2-32)

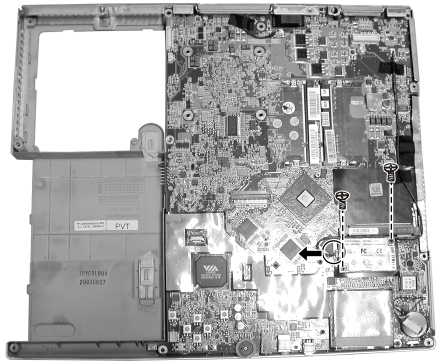


Figure 2-32 Remove the modem card

Reassembly

1. Reconnect the cord. Then fit the modem card and secure with two screws.
2. Reassemble the notebook. (See the previous sections Reassembly)

2.2.12 Touch Pad

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps1 to 6 of section 2.2.10 Disassembly)
5. Remove two screws fastening the touch pad bracket. Then remove it. (Figure 2-33)
6. Remove the click holder and touch pad panel. (Figure 2-33)

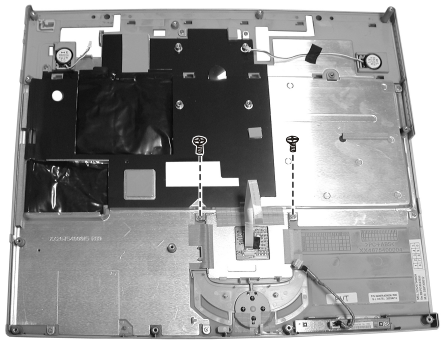


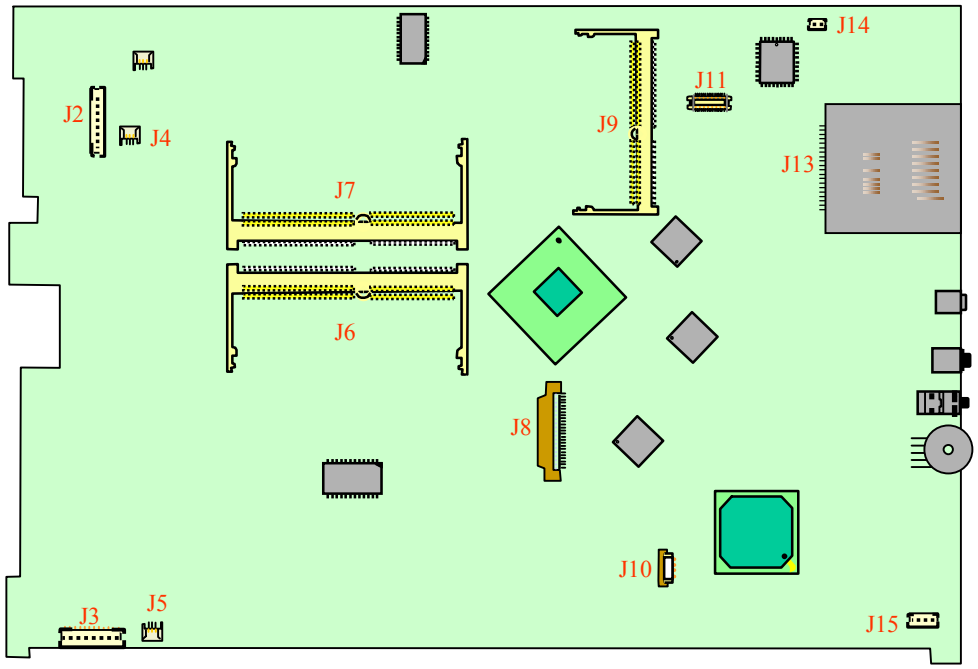
Figure 2-33 Free the touch pad

Reassembly

1. Fit the touch pad panel and click holder
2. Then fit the touch pad bracket and secure with two screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Main Board (Side A) – 1

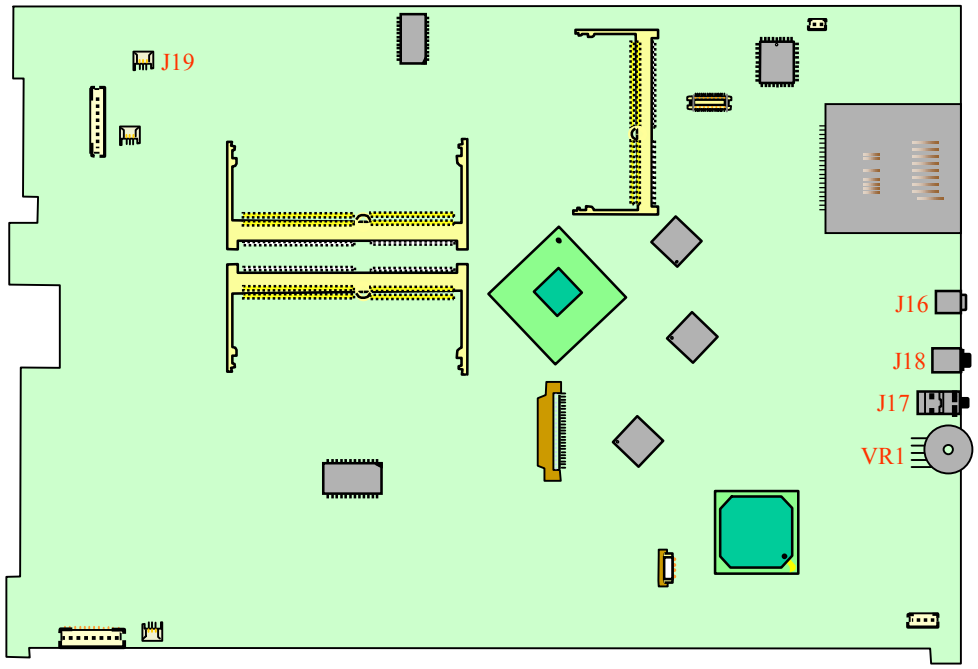


- J2,J3 : LCD Connector
- J4 : Right Internal Speaker Connector
- J5 : Left Internal Speaker Connector
- J6-7 : DDR SO-DIMM Module Socket
- J8 : Internal Keyboard Connector
- J9 : Mini PCI Socket
- J10 : Touch-pad Connector
- J11 : MDC Connector
- J13 : Card Reader Connector
- J14 : RTC Battery Connector
- J15 : LED Indicator Board Connector

------ To next page ------

3. Definition & Location of Connectors/ Switches

3.1 Main Board (Side A) – 2



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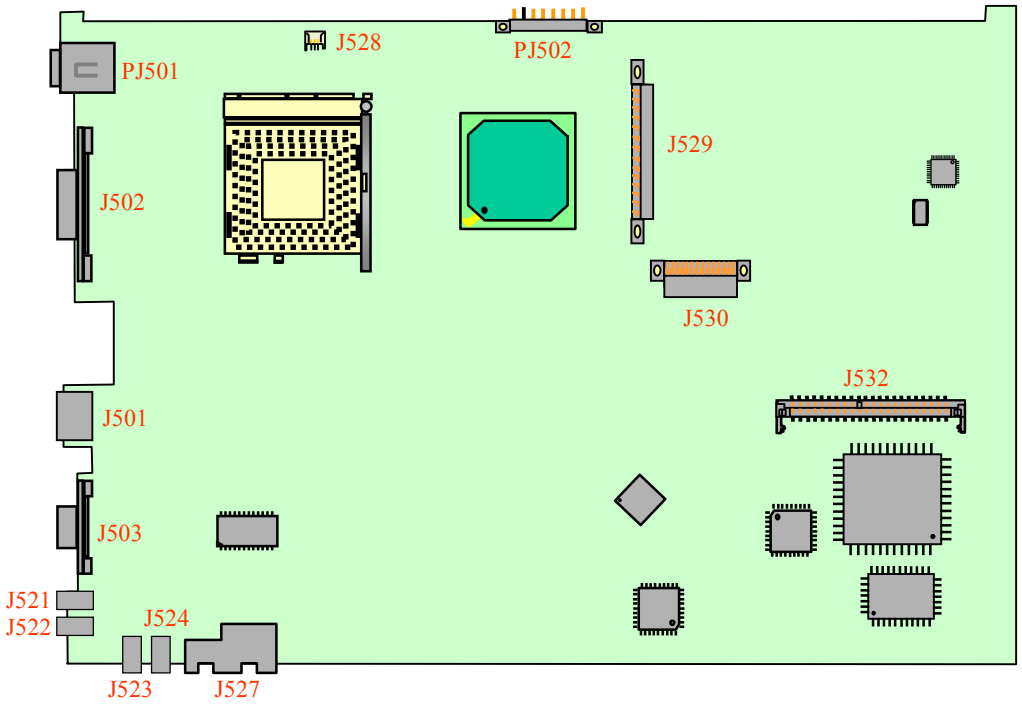
- **J16 : IEEE1394 Connector**
- **J17 : External Audio Output**
- **J18 : External Microphone Input**
- **J19 : MDC Jump Wire Connector**
- **VR1 : Volume Controller**

3. Definition & Location of Connectors/ Switches

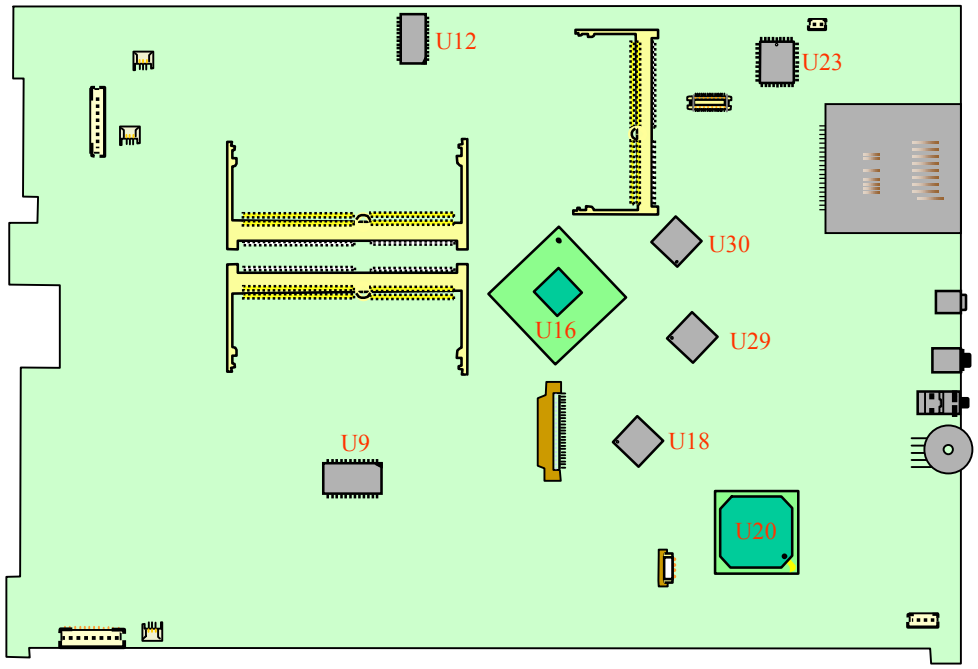
3.1 Main Board (Side B)



- PJ501 : AC Power Jack
- PJ502 : Battery Connector
- J501 : S-Video Connector
- J502 : Parallel Port Connector
- J503 : CRT Connector
- J521-524 : USB Ports Connector
- J527 : RJ45/RJ11 Connector
- J528 : FAN Connector
- J529 : HDD Connector
- J530 : CDROM Connector
- J532 : PCMCIA Card Bus Socket

4. Definition & Location of Major Components

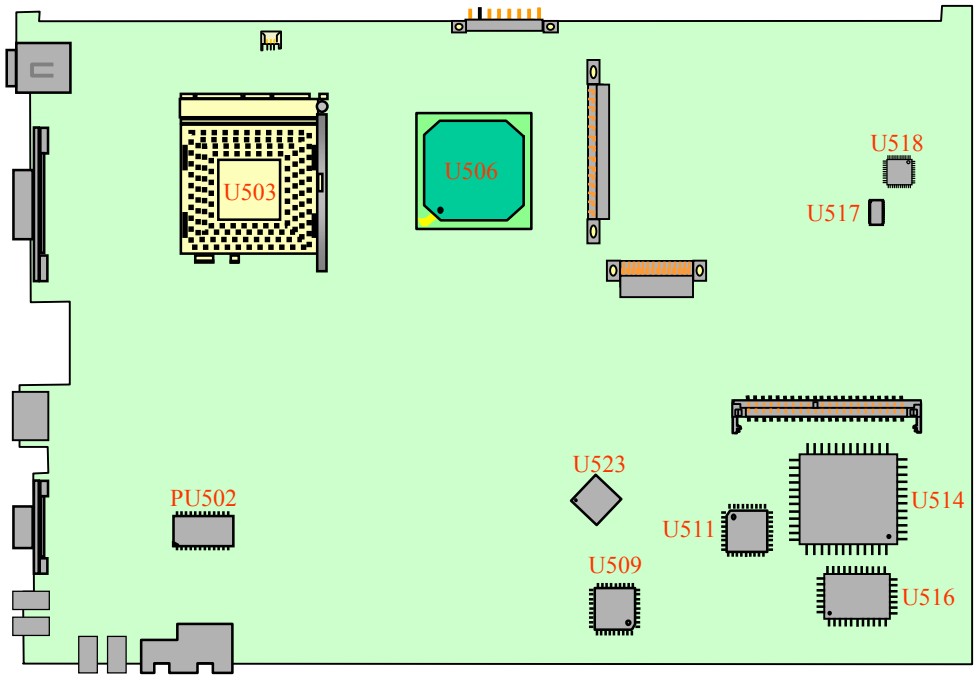
4.1 Main Board (Side A)



- U9 : ICS950403 Clock Generator
- U12 : VT6103 LAN Controller
- U16 : VGA Control Chip ATI M10
- U18,U29,U30 : On Board External VRAM
- U20 : South Bridge VT8235
- U23 : Flash ROM (BIOS)

4. Definition & Location of Major Components

4.1 Main Board (Side B)



- U503 : CPU Socket
- U506 : North Bridge VT8385
- U509 : PC87393 Super I/O Controller
- U511 : H8/F3437 Micro Controller
- U514 : ENE CP710 PCMCIA &Reader Controller
- U516 : VT6307L IEEE1394 Controller
- U517 :TPA0202 Audio Amplifier
- U518 : CMI9738 Audio CODEC
- U523 : On Board External VRAM
- PU502 :CPU Power Controller

5. Pin Descriptions of Major Components

5.1 AMD ATHLON™ 64 Processor-1

DDR SDRAM Memory Interface

Signal Name	Type	Description
MEMCLK_H/L[7]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[6]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[5]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[4]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[3]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.[1]
MEMCLK_H/L[2]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs. [1]
MEMCLK_H/L[1]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.[1]
MEMCLK_H/L[0]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.[1]
MEMCKEA **MEMCKEB**	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality.[1]
MEMDQS[17:0]	B-IOS	DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.[1]
MEMDATA[63:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[7:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects[1]
MEMRASA_L **MEMRASB_L**	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.[1]
MEMCASA_L **MEMCASB_L**	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMWEA_L **MEMWEB_L**	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.[1]
MEMADDA[13:0] **MEMADDB[13:0]**	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.[1]

DDR SDRAM Memory Interface Continue

Signal Name	Type	Description
MEMBANKA[1:0] **MEMBANKB[1:0]**	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.[1]
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference[1]
MEMZP	A	Compensation Resistor tied to VSS[1]
MEMZN	A	Compensation Resistor tied to 2.5 V[1]

Notes:

1. For connection details and proper resistor values, see the AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Clock

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

5.1 AMD ATHLON™ 64 Processor-2

HyperTransport™ Technology

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input[2]
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency
L0_REF1	A	Compensation Resistor to VLDT[1]
L0_REF0	A	Compensation Resistor to VSS[1]

Notes:

1. *These pins are used in an alternating fashion to compensate RTT by internal comparison to 3/4 VLDT and 1/4 VLDT and compensate RON by comparison to each other around 1/2 VLDT. For proper resistor value, see the* AMD Athlon™ 64 Processor Motherboard Design Guide*, order # 24665.*
2. *The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and the complement is pulled Low. Refer to the* AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details.*

Debug

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Request

Miscellaneous

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125oC.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENS	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VDDLDT_A **VDDLDT_B**	S	HyperTransport™ I/O ring power supply for side A and side B of the package
VTT_A **VTT_B**	S	VTT regulator voltage for side A and side B of the die
VS	S	Ground

5.2 K8T800M(VT8385) North Bridge-1

"Hyper Transport" transmit Interface

Signal Name	Type	I/O	Description
TCAD15/TCAD15#	E20,D21	O	Transmit Differential Control/Address/Data Pair 15
TCAD14/TCAD14#	D19,C19	O	Transmit Differential Control/Address/Data Pair 14
TCAD13/TCAD13#	E18,E19	O	Transmit Differential Control/Address/Data Pair 13
TCAD12/TCAD12#	D17,C17	O	Transmit Differential Control/Address/Data Pair 12
TCAD11/TCAD11#	D15,C15	O	Transmit Differential Control/Address/Data Pair 11
TCAD10/TCAD10#	E14,E15	O	Transmit Differential Control/Address/Data Pair 10
TCAD9/TCAD9#	D13,C13	O	Transmit Differential Control/Address/Data Pair 9
TCAD8/TCAD8#	E12,E13	O	Transmit Differential Control/Address/Data Pair 8
TCAD7/TCAD7#	B20,C20	O	Transmit Differential Control/Address/Data Pair 7
TCAD6/TCAD6#	A19,A20	O	Transmit Differential Control/Address/Data Pair 6
TCAD6/TCAD5#	B18,C18	O	Transmit Differential Control/Address/Data Pair 5
TCAD6/TCAD4#	A17,A18	O	Transmit Differential Control/Address/Data Pair 4
TCAD6/TCAD3#	A15,A16	O	Transmit Differential Control/Address/Data Pair 3
TCAD6/TCAD2#	B14,C14	O	Transmit Differential Control/Address/Data Pair 2
TCAD6/TCAD1#	A13,A14	O	Transmit Differential Control/Address/Data Pair 1
TCAD6/TCAD0#	B12,C12	O	Transmit Differential Control/Address/Data Pair 0
TCLK0/TCLK0#	B16,C16	O	Transmit Differential Clock Pair 0. Clock for TCAD 0-7
TCLK0/TCLK1#	E16,E17	O	Transmit Differential Clock Pair 1. Clock for TCAD 8-15
TCTL/TCTL#	A21,A22	O	Transmit Differential Control

"Hyper Transport" Receive Interface

RCAD15/RCAD15#	G24,G23	I	Receive Differential Control/Address/Data Pair 15
RCAD14/RCAD14#	J22,H22	I	Receive Differential Control/Address/Data Pair 14
RCAD13/RCAD13#	J24,J23	I	Receive Differential Control/Address/Data Pair 13
RCAD12/RCAD12#	L22,K22	I	Receive Differential Control/Address/Data Pair 12
RCAD11/RCAD11#	N22,M22	I	Receive Differential Control/Address/Data Pair 11
RCAD10/RCAD10#	N24,N23	I	Receive Differential Control/Address/Data Pair 10
RCAD9/RCAD9#	R22,P22	I	Receive Differential Control/Address/Data Pair 9
RCAD8/RCAD8#	R24,R23	I	Receive Differential Control/Address/Data Pair 8
RCAD7/RCAD7#	H26,G26	I	Receive Differential Control/Address/Data Pair 7
RCAD6/RCAD6#	H24,H25	I	Receive Differential Control/Address/Data Pair 6
RCAD5/RCAD5#	K26,J26	I	Receive Differential Control/Address/Data Pair 5
RCAD4/RCAD4#	K24MJ25	I	Receive Differential Control/Address/Data Pair 4
RCAD3/RCAD3#	M24,M25	I	Receive Differential Control/Address/Data Pair 3
RCAD2/RCAD2#	P26,N26	I	Receive Differential Control/Address/Data Pair 2
RCAD1/RCAD1#	P24,P25	I	Receive Differential Control/Address/Data Pair 1
RCAD0/RCAD0#	T26,R26	I	Receive Differential Control/Address/Data Pair 0
RCLK0/RCLK0#	M26,L26	I	Receive Differential Control Clock Pair0.Clock for RCAD0-7
RCLK1/RCLK1#	L24,L23	I	Receive Differential Control Clock Pair1.Clock for RCAD8-15
RCTL/RCTL#	F24,F25		Receive Differential Control

5.2 K8T800M(VT8385) North Bridge-2

"Hyper Transport" Control

HTRST#	B11	O	Hyper Transport Reset.Connect to RESET# pin of K8 CPU.2.5V swing.Active when the RESET# input is active
HTSTP#	A12	I	Hyper Transport Stop. Connect to South Bridge DPSLP# pin

V-Link Interface

Signal Name	Type	I/O	Description
VAD7, **VAD6** **VAD5** **VAD4** **VAD3** **VAD2** **VAD1,** **VAD0**	AF25 AD24 AF20 AE19 AE24 AF24 AD21 AD20	IO IO IO IO IO IO IO IO	Address/Data Bus.Also used to pass strap information from the south bridge to the north bridge (the physical strap is not on the north bridge VAD pin of the south bridge with the information passed over to the north bridge at reset time) VAD7-Test Mode: Connection L=Disable, H=Enable; Register n/a; SB Pin SDCS3# VAD6-ROMSIP: Connection L=Disable, H=Enable; Register Rx51[7]; SB Pin SDA2 VAD5-Loop Test Mode: Connection L=Disable, H=Enable; Register n/a; SB Pin SDA1 VAD4-reserved: Connection n/a; Register n/a; SB Pin SAD0 VAD3-Fast Command: Connection L=Disable, H=Enable; Register Rx53[7]; SB Pin SA19 VAD2-HT Bus Width: Connection L=8 bits, H=16 bits; Register n/a; SB Pin SA18 VAD1-HT Bus Frequency Msb: Connection LL=200MHz LH=400MHz; Register RxCC[9]; SB Pin SA17 VAD0-HT Bus Frequency Lsb: Connection LL=600MHz LH=800MHz; Register RxCC[8]; SB Pin SA16
VPAR	AF19	IO	Parity
VBE#	AE21	IO	Byte Enable
UPCMD	AF26	I	Command from Client(South Bridge) to Host(North Bridge)
UPSTB	AE23	I	Strobe from Client to Host
UPSTB#	AF23	I	Complement Strobe form Client to Host
DNCMD	AD23	O	Command from Host(North Bridge) to Client(South Bridge)
DNSTB	AF22	O	Strobe from Host to Client
DNSTB#	AD22	O	Complement Strobe form Host to Client

AGP Bus Interface

Signal Name	Type	I/O	Description
GD[31:0]	(See pin list	IO	Address / Data Bus. Address is deiven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-stle trafers.
GBE[3:0] **(GBE[3:0#] for 4x mode**	AC7 AD11 AF11 AD11	IO	Command /byte Enable (interpreted as C/BE# for AGP 2x/4x And (C# /BE# for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# 2x/4x only as GPIPE# isn't used in 8x mode). These pin provide valide byte information during AGP write transaction And are driven by master. Thfe target (this chip) drives these line to "0000" during the return of AGP read data. For PCI cycles, commands are driven on gollowing clocks
GPAR	AC16	IO	AGP Parity A single parity bit is provided over GD[31:0] and GBE[3:0]..
GDBIH /GPIPE# **GDBIL**	AC5 AC4	IO	Dynamic Bus inversion High /Low. AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group should be inverted). Used to limit thenamber of simultaneously switching outputs to 8 for each 16-pin group. Pipelined Request. Not used by AGP 8x. Asserted by the master external graphics the master enqueues one request is to be enqueued by the target (North bridge) The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus Note: See RxAE[1] for GPIPE# GDBIH pin function selection
GDS0F (GDS0 for 4x) **GDS0S (GDS0# for 4x)**	AE15 AF15	IO	Bus Strobe 0. Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals) GDS0 provides timing for 2x data transfer mode: GDS0 and GDS0# Provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First strobe) and GDS0# as GDS0S("second" strobe)
GDS1F (GDS1 for 4x) **GDS1S GDS1# for 4x)**	AE7 AF7	IO	Bus Strobe 1. Source synchronous strobes for GD[31:16] (i. e , the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode: GDS1 and GDS1F ("first" strobe) and GDS1# as GDSIS ("second" strobe)
GFRM (GFRM# for 4x)	AC9	IO	Frame. Assertion indicates the address phase of a PCI/ transfer . Negation indicates that one more date transfer is desired by the cycle initiator interpreted as active high for AGP 8x.

5.2 K8T800M(VT8385) North Bridge-3

AGP Bus Interface (Continued)

Signal Name	Type	I/O	Description
GIRDY (GIRDY# for 4x)	AC10	IO	Initiator Ready. (interpreted as active low for PCI/ AGP2x/4x And high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is assertion the master is ready to transfer a subsequent block of read data. The master is never allowed to insert a wait state during the Initial block transfers. For PCI cycles asserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AC14	IO	Target Ready. (interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks). Or is ready to transfer a (initial or subsequent). Block of data when The transfer requires more than four clock to complete. The target is allowed to insert wait states after each block transfer for both read write transaction. For PCI cycles asserted when The target is ready for data transfer
GDSEL (GDSEL# for 4x mode)	AC11	IO	Device Select (PCI transaction only). This signal is driven by the north bridge when a PCI initiator is attempting to access Main memory. It is an input when the chip is acting as PCI Initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GSTOP (GSTOP# for 4x)	AC12	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
AGP8XDT#	Y2	I	**AGP 8x transfer mode Detect.** Low indicates that the extemal graphics card can support 8x transfer mode. Value is visible in AGP3.0 Status register Rx84[3].
GRBF (GRBF# for 4x)	AD6	I	**Read buffer ful**l. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the north bridge will not return low priority read data to the graphics controller.
SBA[7:0]# (SBA[7:0] for 4x)	(see pin list)	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (north bridge). These pins are ignored until enabled.
SBSF (SBS for 4x), SBSS (SBS# for 4x)	AF1	I	**Sideband Strobe.** Driven by the master to provide timing for SBA[7:]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF (First" strobe) and SBS# as SBSS ("Second" strobe).
GWBF (GWBF# for 4x)	AC1	I	**Write buffer Full.**

AGP Bus Interface(continued)

Signal Name	Type	I/O	Description
ST[2:0]	AB1 AA1 AA2	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested low priority read is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue. May be defined in future). 101 Reserved. (arbiter must not issue. May be defined in future). 110 Reserved. (arbiter must not issue. May be defined in future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. Then master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#.ST[2:0] are always outputs from the target (north bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	Y1	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AA3	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AC15	IO	**AGP System Error.**

Note: Separate system interrupt are not provided for AGP. The AGP connector provides interrupts via PCI bus INIA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses).
Note: Two mechanisms are provided by AGP bus to qnqueu master request: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AAGP master implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an the internal pullup to maintain it in the deasserted state incase it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).
Note: AGP 8x signal levels are 0V and0.8V AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

5.2 K8T800M(VT8385) North Bridge-4

Clock, Reset, Power Control and Test

Signal Name	Type	I/O	Description
GCLK	A11	I	**AGP Clock.** 66 MHz clock for AGP logic.
RESET#	AD25	I	**Reset.** Input from the south Bridge chip. 3.3V tolerant input. When asserted, this signal resets the chip and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options. In addition, HTRST# is driven active to reset the K8 CPU.
PWROK	AE26	I	**Power Ok.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to PULL-up to disable.
SUSST	AD26	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
TESTIN	AC26	I	**Test In.** This pin is used for terssting and must be left unconnected or tied high (4.7K Ω to 2.5V) on all board designs.
DEBUG	AC17		Debug.
NC	(see pin list)		**No Connect.** Reserved for graphics functions in pin-compatible “K8M800” chipset north bridge.

5.3 VT8235 South Bridge-1

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD[15:0]	K22,J22,G24,H22, G22,G23,F23,D25, K26,K24,E24,E26, J25,J26,F26,F25	IO	Address /Data Bus. Bits 0-7 are implemented and bits 8-15 are reserved for future use. VAD[6:0]are used to send strap information o he chipset north bridge. A power up VAD[6:4]reflect he state of straps on pins SDA[2:0] and VAD[3:0]reflect the state of straps on pins SA[19:16].The specific interpretation of these straps is north bridge chip design dependent.
VPAR	D26	IO	Parity. If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800,KT400).If VPAR is not implemented in the north bridge chip or is incompatible with he 8235 (4x V-Link north bridges) connect this pin to an 8.2K pull up to 2.5V (Pro266,Pro266T,KT266, KT266A, KT333, P4X266, PN266,KN266,KM266, P4M266, P4N266).See app note AN222 for details.
VBE[1:0]#	L26,F24	IO	Byte Enables.VBE0#is used with VAD[7-0]and VBE1# is used with VAD[15-8](VBE1#and VAD[15-8]are reserved for future use).
VCLK	L24	I	V-Link Clock.
UPCMD	K25	O	Command from Client-to-Host.
DNCMD	J24	I	Command from Host-to-Client.
UPSTB	H24	O	Strobe from Client-to-Host.
UPSTB#	H26	O	Complement Strobe from Client-to-Host.
DNSTB	G25	I	Strobe from Host-to-Client.
DNSTB#	G26	I	Complement Strobe from Host-to-Client.
VLVREF	J23	I	Voltage Reference.
VLCOMP	K23	I	V-Link Compensation.
VCCVK	(see pin list)	P	V-Link VK Power.

Advanced Programmable Interrupt Controller (APIC)Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	V23	O	Internal APIC Data 1.Function 0 Rx58[6]=1
APICD0	T22	O	Internal APIC Data 0.Function 0 Rx58[6]=1
APICCLK	U23	I	APIC Clock.

Straps

Signal Name	Pin #	I/O	Signal Description
Strap /SDCS3#	AD23	I	Strap. State reflected on VAD[7]at powerup. No internal function.
Strap /SDA2	AF23	I	Strap. State reflected on VAD[6]at powerup. No internal function.
Strap /SDA1	AC22	I	Strap. State reflected on VAD[5]at powerup. No internal function.
Strap /SDA0	AE23	I	Strap. State reflected on VAD[4]at powerup. No internal function.
Strap /SA19	AC11	I	Strap. State reflected on VAD[3]at powerup. No internal function.
Strap /SA18	AD11	I	Strap. State reflected on VAD[2]at powerup. No internal function.
Strap /SA17	AE11	I	Strap. State reflected on VAD[1]at powerup. No internal function.
Strap /SA16	AF11	I	Strap. State reflected on VAD[0]at powerup. No internal function.
Strap /SOE#	AD12	I	Strap. Strap low o enable (high o disable)auto reboot.
Strap /SPKR	AE9	I	Strap. Strap low o enable (high o disable)CPU frequency s rapping
Strap /ROMCS#/KBCS#	AF12	I	Strap. Strap high to enable LPCBIOSROM

5.3 VT8235 South Bridge-2

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VGATE /GPIO8 /PCREQA	C8	I	Voltage Gate. Signal from he CPU voltage regulator. High indicates he voltage regulator output is stable. This pin performs he VGATE function if Device 17 Function 0 Rx53[7]=0,E5[4]=1 and E4[3]=0.
VIDSEL /GPIO28	P25	OD	Voltage Regulator ID Select. Connected o he CPU voltage regulator. Low selects the voltage ID from the CPU; high selects a different fixed voltage ID (the lower voltage used for CPU deep sleep mode). This pin performs the VIDSEL function if Function 0 RxE5[3]=0.
VRDSLP /GPIO29	P24	OD	Voltage Regulator Deep Sleep. Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This pin performs he VRDPSLP function if Function 0 RxE5[3]=0.
GHI#/GPIO22	R24	OD	CPU Speed Select. Connected o he CPU voltage regulator, used to select high speed (L) or low speed (H).This pin performs the GHI# function if Function 0 RxE5[3]=0.
DPSLP#/GPIO23	P26	OD	CPU Deep Sleep.
CPUMISS /GPI17	Y1	I	CPU Missing. Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of he CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ#/GPI6	A8	I	AGP Busy. Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if his input is asserted low).Connected to the AGP Bus AGPBZ# pin.

Summary of Internal Pull-Up /Pull-Down Resistor Implementation Internal Pullups are present on pins KBCK,KBDT,MSCK,MSDT,SERIRQ,LAD [3:0]Internal Pulldowns are present on pins SA [19-16] and all LAN pins

Low Pin Count (LPC)Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	AE7	IO		LPC Frame.
LREQ#	AD7	IO		LPC DMA /Bus Master Request.
LAD[3-0]	AF7,AD8,AE8, AF8	IO	PU	LPC Address /Data.

Note: Connect the LPC interface LPCRST#(LPC Reset)signal to PCIRST#

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	T25	OD	A20 Mask. Connect to A20 mask input of he CPU to control address bi -20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit -1 (Fast_A20).
FERR#	U26	I	Numerical Coprocessor Error. This signal is tied o he coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T26	OD	Ignore Numeric Error. This pin is connected to the CPU “ignore error” pin.
INIT#	R25	OD	Initialization. The VT8235 asserts INIT# if it detects a shut-down special cycle on he PCI bus or if a soft reset is initiated by he register
INTR	T23	OD	CPU Interrupt. INTR is driven by he VT8235 to signal he CPU hat an interrupt request is pending and needs service.
NMI	R23	OD	Non-Maskable Interrupt. NMI is used o force a non-maskable interrupt to the CPU. The VT8235 generates an NMI when PCI bus SERR# is asserted.
SLP#	U25	OD	Sleep. Used to put the CPU to sleep.
SMI#	T24	OD	System Management Interrupt. SMI# is asserted by he VT8235 o he CPU in response to different Power-Management events.
STPCLK#	R26	OD	Stop Clock. STPCLK# is asserted by he VT8235 to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 .pullup resistors to VCC_CMOS (see Design Guide).

Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	A13	O		Serial EEPROM Chip Select.
EECK	C14	O		Serial EEPROM Clock.
EEDO	A14	O		Serial EEPROM Data Output.
EEDI	B14	I		Serial EEPROM Data Input.

These pins are disabled if the SDCS1#pin is strapped low to enable serial EEPROM connection via the MII interface.

5.3 VT8235 South Bridge-3

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	see pin list)	IO	Address /Data Bus. Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	L1,A4, D1,F4	IO	Command /Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	B3	IO	Device Select. The VT8235 asserts his signal o claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	B4	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C4	IO	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	A3	IO	Target Ready. Asserted when the target is ready for data transfer.
STOP#	C3	IO	Stop. Asserted by the target to request the master to stop the current transaction.
SERR#	C1	I	System Error. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 can be programmed o generate an NMI to the CPU.
PAR	D3	IO	Parity. A single parity bi is provided over AD[31:0]and C/BE[3:0]#.
INTA# INTB# INTC# INTD# INTE# /GPIO12 /PCGNTA, INTF# /GPIO13 /PCGNTB, INTG# /GPIO14, INTH# /GPIO15	P1, P2, P3, R1 A7, B8, D8, C7	I	PCI Interrupt Request .The INTA# through INTD# pins are typically connected to the PCI bus INTA#-INTD# pins per the able below. INTE-H# are enabled by setting Device 17,Function 0 Rx5B[1]=1. BIOS settings must match the physical connection method. PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#

PCI Bus Interface Continue

Signal Name	Pin #	I/O	Signal Description
REQ5#/GPI7, REQ4#, REQ3#, REQ2#, REQ1#, REQ0#	N4 L4 H4 D4 C5 D6	I	PCI Request. These signals connect to the VT8235 from each PCI slot (or each PCI master)o request he PCI bus. To use pin N4 as REQ5#, Function 0 RxE4 must be set to 1 otherwise his pin will function as General Purpose Input 7.
GNT5#/GPO 7, GNT4#, GNT3#, GNT2#, GNT1#, GNT0#	P4 M4 J4 E4 D5 E6	O	PCI Grant. These signals are driven by he VT8235 to grant PCI access to a specific PCI master. To use pin P4 as GNT5#,Function 0 RxE4 must be set to 1 otherwise this pin will function as General Purpose Output 7.
PCIRST#	R2	O	PCI Reset. This signal is used o reset devices attached to the PCI bus.
PCICLK	R22	I	PCI Clock. This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AF5	IO	PCI Bus Clock Run. This signal indicates whether he PCI clock is or will be stopped high) or running (low).The VT8235 drives his signal low when he PCI clock is running default on reset)and releases it when it stops the PCI clock. External devices may assert this signal low o request hat he PCI clock be restarted or prevent it from stopping. Connect his pin o ground using a 100 .resistor if he function is not used. Refer to the “PCI Mobile Design Guide” and he VIA “VT8633 Apollo Pro266 Design Guide” for more details.

PC /PCI DMA

Signal Name	Pin #	I/O	PU	Signal Description
PCREQA/GPIO8/VGA TE	C8	I		PC /PCI Request A. Device 17 Function 0 Rx53[7]=1
PCREQB /GPIO9	B7	I		PC /PCI Request B. Device 17 Function 0 Rx53[7]=1
PCGNTA /GPIO12	A7	O		PC /PCI Grant A. Device 17 Function 0 Rx53[7]=1
PCGNTB /GPIO13	B8	O		PC /PCI Grant B. Device 17 Function 0 Rx53[7]=1

5.3 VT8235 South Bridge-4

LAN Controller -Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	C13	I	*PD*	MII Collision Detect. From he external PHY.
MCRS	B13	I	*PD*	MII Carrier Sense. Asserted by the external PHY when the media is active.
MDCK	C9	O	*PD*	MII Management Data Clock. Sent to the external PHY as a timing reference for MDIO
MDIO	B9	IO	*PD*	MII Management Data I/O. Read from he MDI bit or written to the MDO bit.
MRXCLK	B10	I	*PD*	MII Receive Clock.2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	A9,D9,D10,E10	I	*PD*	MII Receive Data. Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	C10	I	*PD*	MII Receive Data Valid.
MRXERR	A10	I	*PD*	MII Receive Error. Asserted by the PHY when it detects a data decoding error.
MTXCLK	A12	I	*PD*	MII Transmit Clock. Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	C11,B11,A11,C12	O	*PD*	MII Transmit Data. Parallel transmit data lines synchronized to MTXCLK.
MTXENA	B12	O	*PD*	MII Transmit Enable. Signals that transmit is active from the MII port to the PHY.
MIIVCC	D11,D12,E11,E12	Power		MII Interface Power.3.3V ±5%.
MIIVCC25	D13,E13	Power		MII Suspend Power.2.5V ±5%.
RAMVCC	E7	Power		Power For Internal LAN RAM.2.5V ±5%.
RAMGND	E8	Power		Ground For Internal LAN RAM.

General Purpose I/O

Signal Name	Pin #	I/O	Signal Description
GPIOA /GPI24/GPO24	AE5	IO	**General Purpose I/O A /24**. RxE6[0]=1
GPIOC /GPI25/GPO25	AE6	IO	**General Purpose I/O C /25**.
GPIOD /GPI30/GPO30	AD6	IO	**General Purpose I/O D /30.**
GPIOE /GPI31/GPO31	AC6	IO	**General Purpose I/O E /31.**

The output type of he above pins may be selected as either OD or TTL (see Device 17 Function 0 RxE7)

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	A21	IO	USB 2.0 Port 0 Data +
USBP0 –	B21	IO	USB 2.0 Port 0 Data –
USBP1+	E21	IO	USB 2.0 Port 1 Data +
USBP1 –	D21	IO	USB 2.0 Port 1 Data –
USBP2+	A19	IO	USB 2.0 Port 2 Data +
USBP2 –	B19	IO	USB 2.0 Port 2 Data –
USBP3+	E19	IO	USB 2.0 Port 3 Data +
USBP3 –	D19	IO	USB 2.0 Port 3 Data –
USBP4+	A17	IO	USB 2.0 Port 4 Data +
USBP4 –	B17	IO	USB 2.0 Port 4 Data –
USBP5+	E17	IO	USB 2.0 Port 5 Data +
USBP5 –	D17	IO	USB 2.0 Port 5 Data –
USBCLK	D23	I	USB 2.0 Clock.48MHz clock input for he USB interface
USBOC0#	A15	I	USB 2.0 Port 0 Over Current Detect. Port 0isdisablediflow.
USBOC1#	B15	I	USB 2.0 Port 1 Over Current Detect. Port1isdisablediflow.
USBOC2#	C15	I	USB 2.0 Port 2 Over Current Detect. Port2isdisablediflow.
USBOC3#	E15	I	USB 2.0 Port 3 Over Current Detect. Port 3isdisablediflow.
USBOC4#	D14	I	USB 2.0 Port 4 Over Current Detect. Port 4isdisablediflow.
USBOC5#	E14	I	USB 2.0 Port 5 Over Current Detect. Port 5isdisablediflow.
USBVCC	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Voltage.3.3V
USBGND	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Ground.
VSUSUSB	D15	Power	USB 2.0 Suspend Power.2.5V ±5%.
VCCUPLL	A23,D22	Power	USB 2.0 PLL Analog Voltage.2.5V ±5%.
GNDUPLL	B23,E22	Power	USB 2.0 PLL Analog Ground.

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0#/GPIO20 /ACSDIN2	U2	O	Programmable Chip Select 0.RxE4[6]=1,E5[1]=1
PCS1#/GPIO21/ACSDIN3 /SLPBTN#	V1	O	Programmable Chip Select 1.RxE4[6]=1,E5[2]=1

5.3 VT8235 South Bridge-5

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY / PDDMARDY / PDSTROBE	Y26	I	EIDE Mode: **Primary I/O Channel Ready.**Device read indicator UltraDMA Mode:**Primary Device DMA Ready** .Output flow control. The device may assert DDMARDY o pause output transfers **Primary Device Strobe** .Input data strobe (both edges).The device may s op DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	AD15	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready** .Output flow control. The device may assert DDMARDY to pause output transfers Secondary Device Strobe .Input data strobe (both edges).The device may stop DSTROBE o pause input data transfers
PDIOR#/ PHDMARDY / PHSTROBE	Y24	O	EIDE Mode: Primary Device I/O Read. Device read strobe UltraDMA Mode: Primary Host DMA Ready .Primary channel input flow control .The host may assert HDMARDY o pause input transfers Primary Host Strobe .Output data strobe (both edges).The host may stop HSTROBE o pause output data transfers
SDIOR#/ SHDMARDY / SHSTROBE	AF22	O	EIDE Mode: Secondary Device I/O Read. Device read strobe UltraDMA Mode: Secondary Host DMA Ready .Input flow control. The host may assert HDMARDY to pause input transfers Host Strobe B .Output strobe (both edges).The host may stop HSTROBE to pause output data transfers
PDIOW#/ PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device wri te strobe UltraDMA Mode: **Primary Stop.**Stop transfer: Asserted by the host prior to initiation an UltraDMA burst; negated by the host before data is transferred an UltraDMA burst. Assertion of STOP by he host during or after transfer in UltraDMA mode signals the nation of the burst
SDIOW#/ SSTOP	AC21		EIDE Mode: **Secondary Device I/O Write.**Device writ strobe UltraDMA Mode: **Secondary Stop** .Stop transfer Asserted by the host prior to initiation of an UltraDMA burst;negated by the host before data is transferted in an ULtraDMA burst Assert of Stop by the host during or after data transfer in ULtraDMA mode signals the termination of the burst

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface Continue

Signal Name	Pin #	I/O	Signal Description
PDDRQ	Y22	I	Primary Device DMA Request.Primary channel DMA request
SDDRQ	AE15	I	Secondary Device DMA Request.Secondary channel DMA request
PDDACK#	W26	O	Primary Device DMA Acknowledge.Primary channel DMA acknowledge
SDDACK#	AD22	O	Secondary Device DMA Acknowledge.Secondary channel DMA acknowledge
IRQ14	AE24	I	Primary Channel Interrupt Request.
IRQ15	AF24	I	Secondary Channel Interrupt Request.
PDCS1#	V24		Primary Master Chip Select.This signal corresponds toCS1FX#on the primary IDM connector
PDCS3#	W24		Primary Slave Chip Select.This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#/srap	AC23		Secondary Master Chip Select.This signal corresponds o CS17X# on he secondary IDE connector.S rap low (resistor o ground) to enable serial EEPROM interface via he MII bus (this disables the EExx pins).This pin has an internal pullup to default to serial EEPROM interface via the EEPROM interface via the Eexx pine
SDCS3#/s rap	AD23		Secondary Slave Chip Select. This signal corresponds toCS37X#on the secondary IDE connector. Strap information is communicated to the north bridge via VAD[7].
PDA[2-0]	V26,V25,Y23		Primary Disk Address. PDA[2:0]are used o indicate which by e in either the ATA command block or control block is being accessed.
SDA[2-0]/srap	AF23,AC22,AE23		Secondary Disk Address. SDA[2:0]are used o indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VAD[6:4].
PDD[15-0]	(see pin list)		Primary Disk Data.
SDD[15-0]/SA[15-0]	(see pin list)		Secondary Disk Data.
PDCOMP	W23		Primary Disk Compensation.
SDCOMP	AC15		Secondary Disk Compensation.

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AE10	I	Serial IRQ. This pin has an internal pull-up resistor.

5.3 VT8235 South Bridge-6

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 *(VBAT)*	AE3	I	**General Purpose Input 0**.Status on PMIO Rx20[0]
GPI1 *(VSUS33)*	AC3	I	**General Purpose Input 1**.Status on PMIO Rx20[1]
GPI2 /EXTSMI#*(VSUS33)*	AA1	I	**General Purpose Input 2**.Status on PMIO Rx20[4]
GPI3 /RING#*(VSUS33)*	Y2	I	**General Purpose Input 3**.Status on PMIO Rx20[8]
GPI4 /LID#*(VSUS33)*	AC1	I	**General Purpose Input 4**.Status on PMIO Rx20[11]
GPI5 /BATLOW#*(VSUS33)*	W4	I	**General Purpose Input 5**.Status on PMIO Rx20[12]
GPI6 /AGPBZ#	A8	I	**General Purpose Input 6**.Status on PMIO Rx20[5]
GPI7 /REQ5#	N4	I	**General Purpose Input 7**.RxE4[2]=0
GPI8 /GPO8 /PDREQA /VGATE	C8	I	**General Purpose Input8**. RxE4[3]=0, E5[4]=0, 53[7]=0
GPI9 /GPO9 /PDREQB	B7	I	**General Purpose Input 9**. RxE4[3]=0,53[7]=0
GPI10 /GPO10	D7	I	**General Purpose Input 10**.RxE4[3]=0
GPI11 /GPO11	A6	I	**General Purpose Input 11**.RxE4[3]=0
GPI12 /GPO12 /INTE#/PDGNTA	A7	I	**General Purpose Input 12**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI13 /GPO13 /INTF#/PDGNTB	B8	I	**General Purpose Input 13**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI14 /GPO14 /INTG#	D8	I	**General Purpose Input 14**.RxE4[4]=0,5B[1]=0
GPI15 /GPO15/INTH#	C7	I	**General Purpose Input 15**.RxE4[4]=0,5B[1]=0
GPI16 /INTRUDER#*(VBAT)*	AD3	I	**General Purpose Input 16**.Status on PMIO Rx20[6]
GPI17 /CPUMISS	Y1	I	**General Purpose Input 17**.Status on PMIO Rx20[5]
GPI18 /THRM#/AOLGPI	Y4	I	**General Purpose Input 18**.Rx8C[3]=0
GPI19 /IORDY	AD10	I	**General Purpose Input 19**.RxE5[0]=1
GPI20 /GPO20/ACSDIN2/PCS0#	U2	I	**General Purpose Input 20**.RxE4[6]=1,E5[1]=0, PMIO 4C[20]=1
GPI21 /GPO21/ACSDIN3/PCS1#/SLP BTN#	V1	I	**General Purpose Input 21**.RxE4[6]=1,E5[2]=0 PMIO 4C[21]=1
GPI22 /GPO22 /GHI#	R24	I	**General Purpose Input 22**.RxE5[3]=1,PMIO 4C[22]=1
GPI23 /GPO23 /DPSLP#	P26	I	**General Purpose Input 23**.RxE5[3]=1,PMIO 4C[23]=1
GPI24 /GPO24/GPIOA	AE5	I	**General Purpose Input 24**.RxE6[0]=0
GPI25 /GPO25/GPIOC	AE6	I	**General Purpose Input 25**.RxE6[1]=0
GPI26 /GPO26/SMBDT2 *(VSUS33)*	AD1	I	**General Purpose Input 26**.Rx95[2]=1,95[3]=0

General Purpose Inputs Continue

Signal Name	Pin #	I/O	Signal Description
GPI27 /GPO27 /SMBCK2 *(VSUS33)*	AE1	I	**General Purpose Input 27**.Rx95[2]=1,95[3]=0
GPI28 /GPO28 /VIDSEL	P25	I	**General Purpose Input 28**.RxE5[3]=1,PMIO 4C[28]=1
GPI29 /GPO29/VRDSLP	P24	I	**General Purpose Input 29**.RxE5[3]=1,PMIO 4C[29]=1
GPI30 /GPO30 /GPIOD	AD6	I	**General Purpose Input 30**.RxE6[6]=0
GPI31 /GPO31/GPIOE	AC6	I	**General Purpose Input 31**.RxE6[7]=0

Note:Defaul pin function is underlined in he signal name column above.
Note:Input pin s a us for he above GPI pins 31-0 is also available on PMIO Rx4B-48 [31-0]
Note:See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx4C.General purpose input pins 20-31 are shared with OD (open drain)general purpose output functions,so to use one of these pins as an input pin,a one must be written to the corresponding bit of PMIO Rx4C.

Resets,Clocks,and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	AF4	I	**Power Good.** Connected o he Power Good signal on he Power Supply. Internal logic powered by VBAT.
PWROK#	AE2	O	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	R2	O	**PCI Reset.** Active low reset signal for he PCI bus. The VT8235 will assert his pin during power-up or from he control register.
OSC	AC12	I	**Oscillator.**14.31818 MHz clock signal used by he in ernal Timer.
RTCX1	AD4	I	**RTC Crystal Input :**32.768 KHz crystal or oscilla or input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	AF3	O	**RTC Crystal Output :**32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	AF9	I	Test.
TPO	U24	O	**Test Pin Output.** Output pin for est mode.
NC	W22,AD17	-	**No Connect.** Reserved for future use,do not connect.

5.3 VT8235 South Bridge-7

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	AD2	I	**Power Button.**Used by the Power Management subsystem to monitor an external system on/off but on or switch. Internal logic powered by VSUS33.
SLPBTN#/GPIO21 /ACSDIN3 /PCS1#	V1	I	**Sleep Button.** Used by he Power Management subsystem to monitor an external sleep but on or switch.RxE4[6]=1,80[6]=1,E5[2]=0 and PMIO Rx4C[21]=1
RSMRST#	AD5	I	**Resume Reset.** Resets he internal logic connected o he VSUS33 power plane and also resets portions of he internal RTC logic. Internal logic powered by VBAT.
EXTSMI#/GPI2	AA1	IOD	**External System Management Interrupt.** When enabled o allow it ,a falling edge on this input causes an SMI# to be generated o he CPU o enter SMI mode.(10K PU to VSUS33 if not used)(3.3V only)
PME#	W3	I	**Power Management Event.**(10K PU o VSUS33 if not used)
SMBALRT#	AB2	I	**SMB Alert** .When programmed to allow it (SMB I/O Rx8[3]=1),assertion generates an IRQ, SMI,or power management event.(10K PU o VSUS33 if not used)
LID#/GPI4	AC1	I	**Notebook Computer Display Lid Open /Closed Monitor.** Used by he Power Management subsystem to monitor he opening and closing of the display lid of notebook computers. Can be used o detect either low-to-high or high-to-low transitions o generate an SMI#.(10K PU o VSUS33 if not used)
INTRUDER#/GPI16	AD3	I	Intrusion Indicator. The value of his bi may be read at PMIO Rx20[6]
THRM#/GPI18 /AOLGPI	Y4	I	**Thermal Alarm Monitor.**Rx8C[3]=1.Rising or falling edges (selectable by PMIO Rx2C[6])may be detected to status at used a PMIO Rx20[10].Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#)o automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-3]).
RING#/GPI3	Y2	I	**Ring Indicator.** May be connected to external modem circuitry to allow he system to be re-activated by a received phone call.(10K PU to VSUS33 if not used)
BATLOW#/GPI5	W4	I	**Battery Low Indicator.** (10K PU to VSUS33 if not used)(3.3V only)

Power Management and Event Detection Continue

Signal Name	Pin #	I/O	Signal Description
CPUSTP#/GPO5	AC7	O	**CPU Clock Stop** (RxE4[0]=0).Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP#/GPO6	AF6	O	**PCI Clock Stop** (RxE4[1]=0).Signals the system clock generator o disable he PCI clock outputs. Not connected if not used.
SUSA#/GPO1	AA2	O	**Suspend Plane A Control** (Rx94[2]=0).Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.(10K PU to VSUS33 if not used)
SUSB#/GPO2	AF2	O	**Suspend Plane B Control** (Rx94[3]=0).Asserted during power management STR and STD suspend states. Used o control he secondary power plane.(10K PU o VSUS33 if not used)
SUSC#	AF1	O	**Suspend Plane C Control**. Asserted during power management STD suspend state. Used to control he tertiary power plane. Also connected to ATX power-on circuitry. (10K PU o VSUS33 if not used)
SUSST1#/GPO3	Y3	O	**Suspend Status 1** (Rx94[4]=0).Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend statues. Connect 10K PU to VSUS33.
SUSCLK	AB1	O	**Suspend Clock.**32.768 KHz output clock for use by the North Bridge (e.g.,VT8633 or VT8366)for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS /GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to he CPUMISS pin of the CPU socket.The state of his pin may be read in the SMBus 2 registers.This pin may be used as CPUMISS and GPI17 a the same time.
AOLGPI /GPI18 /THRM#	R2	I	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pin may be used as AOLGPI, GPI18andTHRM#alla the same time.

5.3 VT8235 South Bridge-8

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK /IRQ1	W2	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Clock**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 1** .Interrupt input 1.
MSDT /IRQ12	W1	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Data**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK /KA20G	V3	IO /I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 Keyboard Clock. From internal keyboard controller Rx51[0]=0 Gate A20.Input from external keyboard controller.
KBDT /KBRC	V2	IO/I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data**. From internal keyboard controller. Rx51[0]=0 **Keyboard Rese**t. From external keyboard controller (KBC)for CPURST# generation
KBCS#/ROMCS#/srap	AF12	O/O		**Keyboard Chip Select** (Rx51[0]=0).To external keyboard controller chip. Strap high o enable LPC ROM:

Note: KBCK,KBDT,MSCK,and MSDT are powered by the VSUS33 suspend voltage plane.

AC97 Audio /Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	R3	O	AC97 Reset.
ACBTCK	T3	I	AC97 Bit Clock.
ACSYNC	T1	O	AC97 Sync.
ACSDO	U1	O	AC97 Serial Data Out.
ACSDIN0 (VSUS33)	T2	I	AC97 Serial Data In 0.
ACSDIN1 (VSUS33)	U3	I	AC97 Serial Data In 1.
ACSDIN2 /GPIO20 /PCS0#	U2	I	AC97 Serial Data In2.RxE4[6]=0,E5[1]=0,PMIO Rx4C[20]=1
ACSDIN3/GPIO21 /PCS1#/SLPBTN#	V1	I	AC97 Serial Data In 3.RxE4[6]=0,E5[2]=0,PMIO Rx4C[21]=1

The supply voltage for ACSDIN0-1 is VSUS33 so these inputs can support wake-up on modem ring

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)v	P	**I/O Power.**3.3V ±5%
VCC	(see pin list)	P	**Core Power.**2.5V ±5%.This supply is turned on only when he mechanical switch on the power supply is turned on and he PWRON signal is conditioned high . Note: The VT8235L core voltage is 2.5V so board designs that are intended t all w use of either VT8235 or VT8235L should take this difference into account and allow the core voltage to be selected as either 2.5V (for the VT8235)or 3.3V (for the VT8235L).
GND	(see pin list)	P	Ground. Connect o primary motherboard ground plane.
VSUS33	AA4,AB4, AC4,AC5	P	**Suspend Power.**3.3V ±5%.Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be Connected to VCC33.Signals powered by or referenced o this plane are:PWRGD, RSMRST#,PWRBTN#,SMBCK1/2, SMBDT1/2,GPO0,SUSA#/GPO1,SUSB#/ GPO2,SUSC#, SUSST1#/GPO3,SUSCLK /GPO4,GPI1,GPI2/EXTSMI#,GPI3 /RING#,GPI4 /LID,GPI5 /BATLOW#,GPI6 /PME#, SMBALRT#
VSUS25	T4,U4	P	**Suspend Power.**2.5V ±5%.
VSUSUSB	D15	P	**USB Suspend Power**.2.5V ±5%.
VBAT	AE4	P	**RTC Battery.** Battery input for internal RTC (RTCX1,RTCX2)
VLVREF	J23	P	**V-Link Voltage Reference.**0.9V ±5%.0.34 xVCC25to0.38 xVCC25.
VCCVK	(see pin list)	P	V-Link Compensation Circuit Voltage.2.5V ±5%
MIIVCC	D11,D12, E11,E12	P	**LAN MII Power.**3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY).Connect o VCC33 through a ferrite bead.
MIIVCC25	D13,E13	P	**LAN MII Suspend Power.**2.5V ±5%.
RAMVCC	E7	P	**LAN RAM Power.**2.5V ±5%.Power for LAN internal RAM. Connect to VCC through a ferrite bead.
RAMGND	E8	P	**LAN RAM Ground.** Connect o GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.**3.3V ±5%.Power for USB differential outputs (USBP0+,P0 – ,P1+,P1 – ,P2+, P2 – , P3+, P3 – ,P4+,P4 – ,P5+,P5 –).Connect o VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.

5.3 VT8235 South Bridge-9

Power and Ground Continue

Signal Name	Pin #	I/O	Signal Description
VCCUPLL	A23,D22	P	**USB 2.0 PLL Analog Voltage**.2.5V ±5%.Connect to VCC through a ferrite bead.
GNDU PLL	B23,E22	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	P22	P	**PLL Analog Power.**2.5V ±5%.Connect to VCC through a ferrite bead.
PLLGND	P23	P	**PLL Analog Ground.** Connect o GND through a ferrite bead.

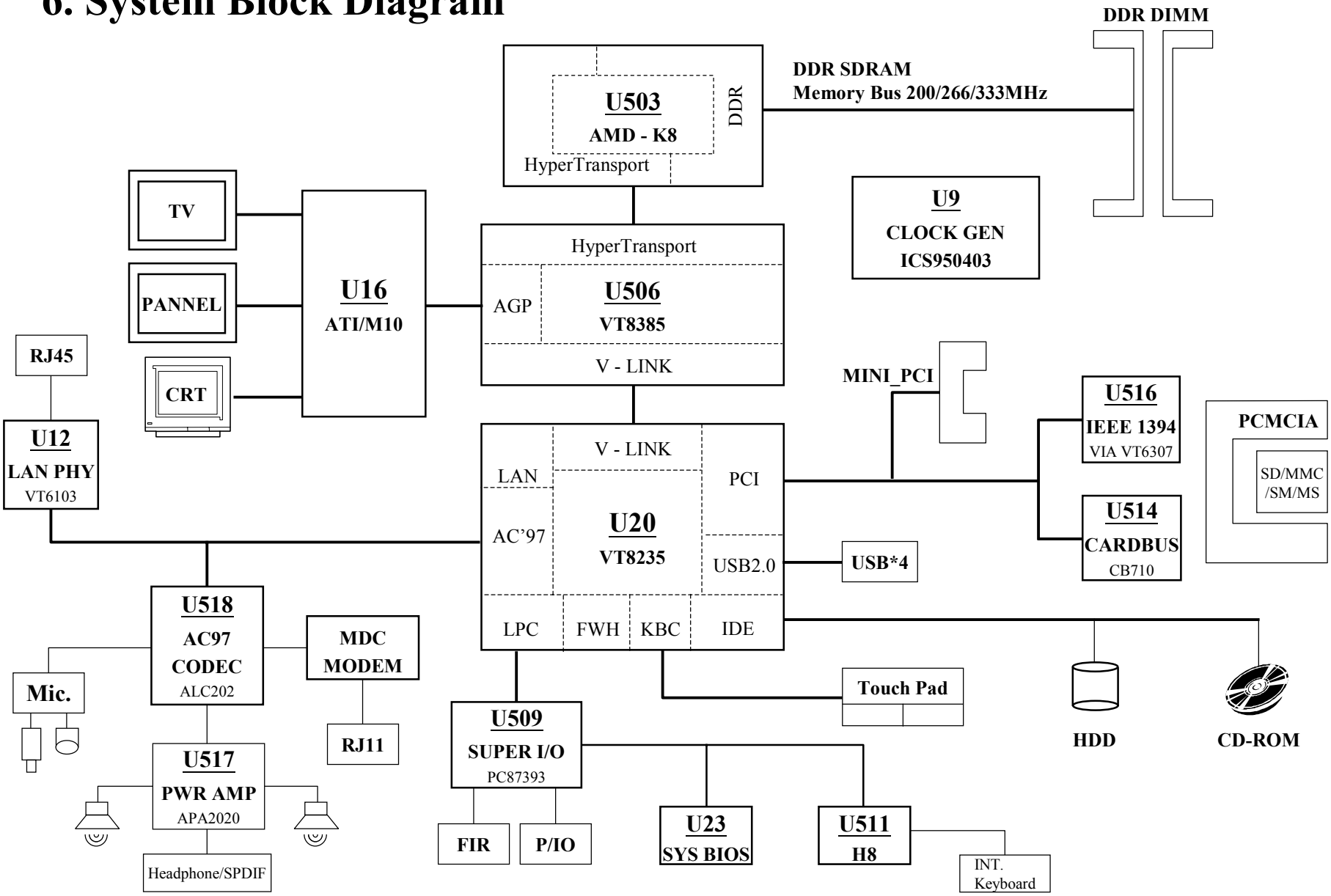
ISA Subset /Parallel BIOS ROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
ROMCS#/KBCS#/ strap	AF12	O		**ROM Chip Select** (Rx51[0]=1).Chip Select o the BIOS ROM. Strap high to enable LPCROM.
SPKR /srap	AE9	O		**Speaker**. Strap low to enable (high o disable)CPU frequency strapping.
MEMR#	AE12	O		**Memory Read.**
MEMW#	AF10	O		**Memory Write.**
IOR#	AC10	O		**I/O Read.**
IOW#	AD9	O		**I/O Write.**
IORDY /GPI19	AD10	I		**I/O Ready**. Used to insert wait states in I/O or memory cycles. RxE5[0]=0
SOE#/s rap	AD12	O		**XD Bus Tranceiver Output Enable**. Strap low to enable auto reboot.
XD[7-0]	AD13,AE13, AF13,AD14, AE14,AF14, AC13,AC14	IO		**XD Bus**. For input of BIOS ROM data or data from to her on-board I/O or memory devices.
SA[19-16]/GPO[19-16] /sraps	AC11,AD11, AE11,AF11	O	*PD*	**System Address 19-16**.Strap states are passed to North Bridge via VAD[3-0].Functions as SA[19-16]if RxE4[5]=0.
SA[15-0]/SDD[15-0]	(see pin lis)	O		**System Address 15-0**.

System Management Bus (SMB)Interface (I 2 CBus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AB3	IO	SMB /I^2 C Channel 1 Clock.
SMBCK2 /GPI27/GPO27	AE1	IO	SMB /I^2 C Channel 2 Clock.Rx95[2]=0
SMBDT1	AC2	IO	SMB /I^2C Channel 1 Data.
SMBDT2 /GPI26/GPO26	AD1	IO	SMB /I^3C Channel 2 Data.Rx95[2]=0
SMBALRT#	AB2	I	SMB Alert.(enabled by System Management Bus I/O space Rx08[1]When the chip is enabled to allow it, assertion generates an IRQ SMI interrupt or a power management resume event. Connect o a ohm pull up to VSUS33 if not used.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot or by the PIO debug board plug at PIO port.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes

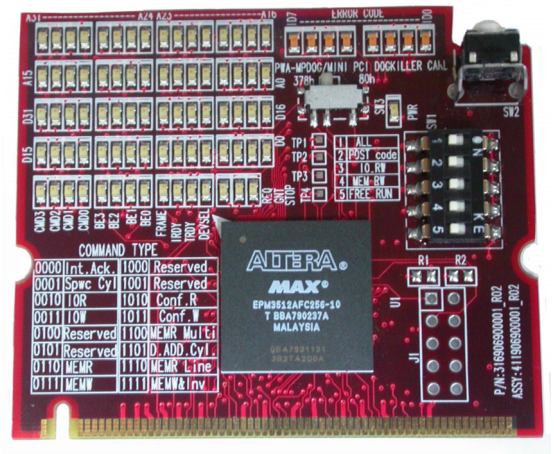
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville CPU init
52h	USB HC init

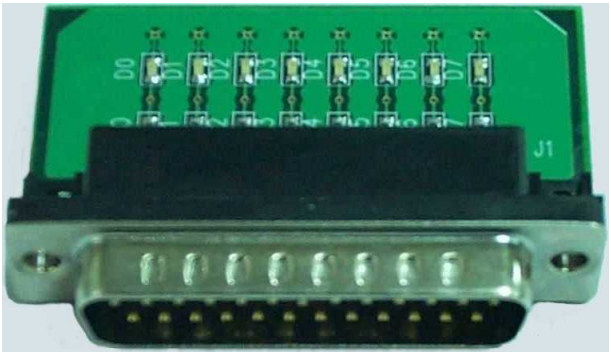
7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-MPDOG/MINI PCI DOGKILLER CARD
Note: Order it from MIC/TSSC

7.3.2 Diagnostic Tool for PIO Port :



P/N:411904800001
Description: PWA; PWA-378Port Debug BD
Note: Order it from MIC/TSSC

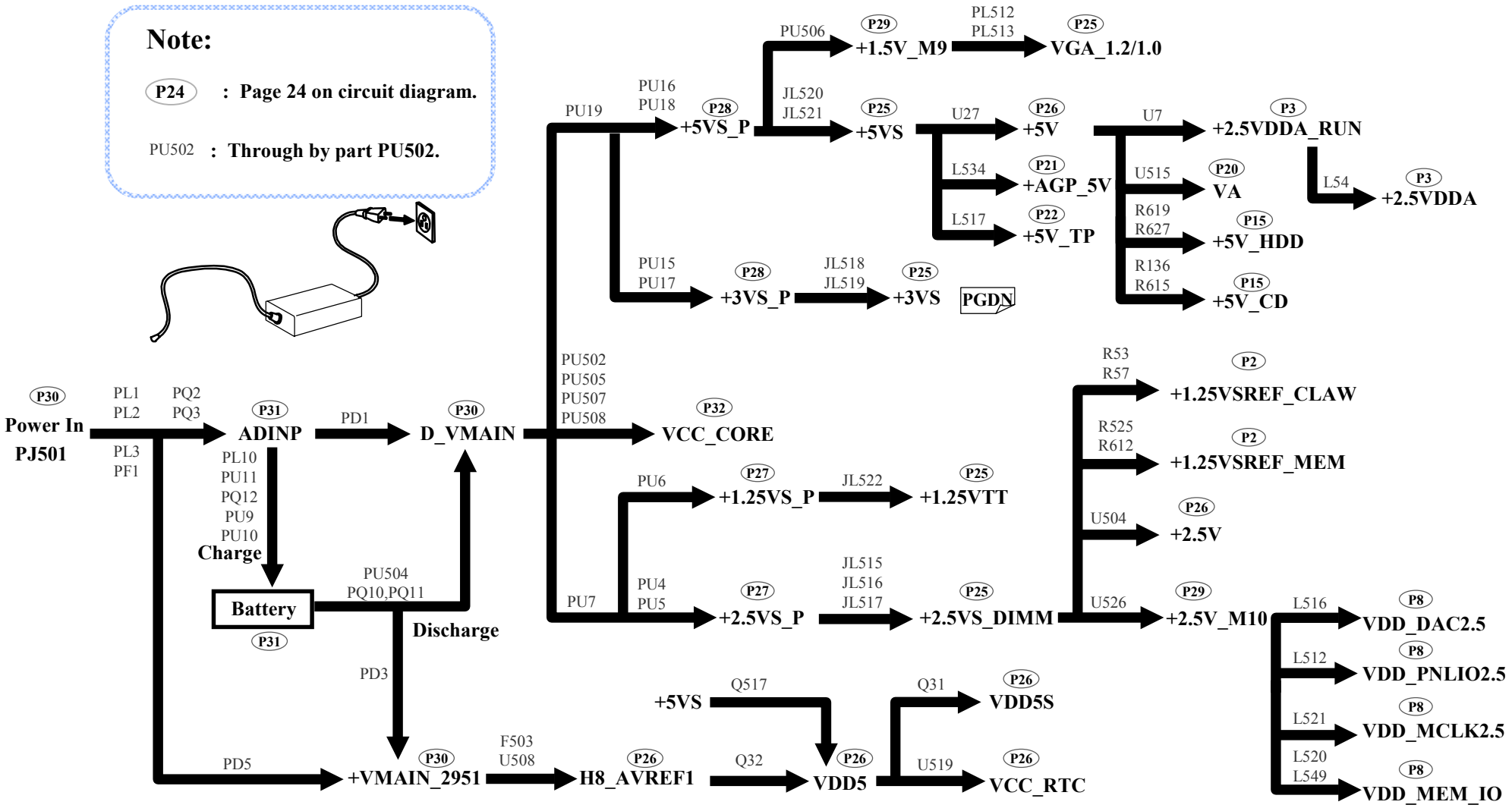
8. Trouble Shooting

- 8.1 No Power
- 8.2 Battery Can not Be Charged
- 8.3 No Display
- 8.4 AGP Controller Failure LCD No Display
- 8.5 External Monitor No Display
- 8.6 Memory Test Error
- 8.7 Keyboard and Touch Pad Test Error
- 8.8 Hard Disk Drive Test Error
- 8.9 CD-ROM Driver Test Error
- 8.10 USB Port Test Error
- 8.11 PC Card Socket Test Error
- 8.12 Memory-Card Socket Failure
- 8.13 IEEE1394 Test Error
- 8.14 LAN Test Error
- 8.15 Audio Failure

8355 N/B MAINTENANCE

8.1 No Power

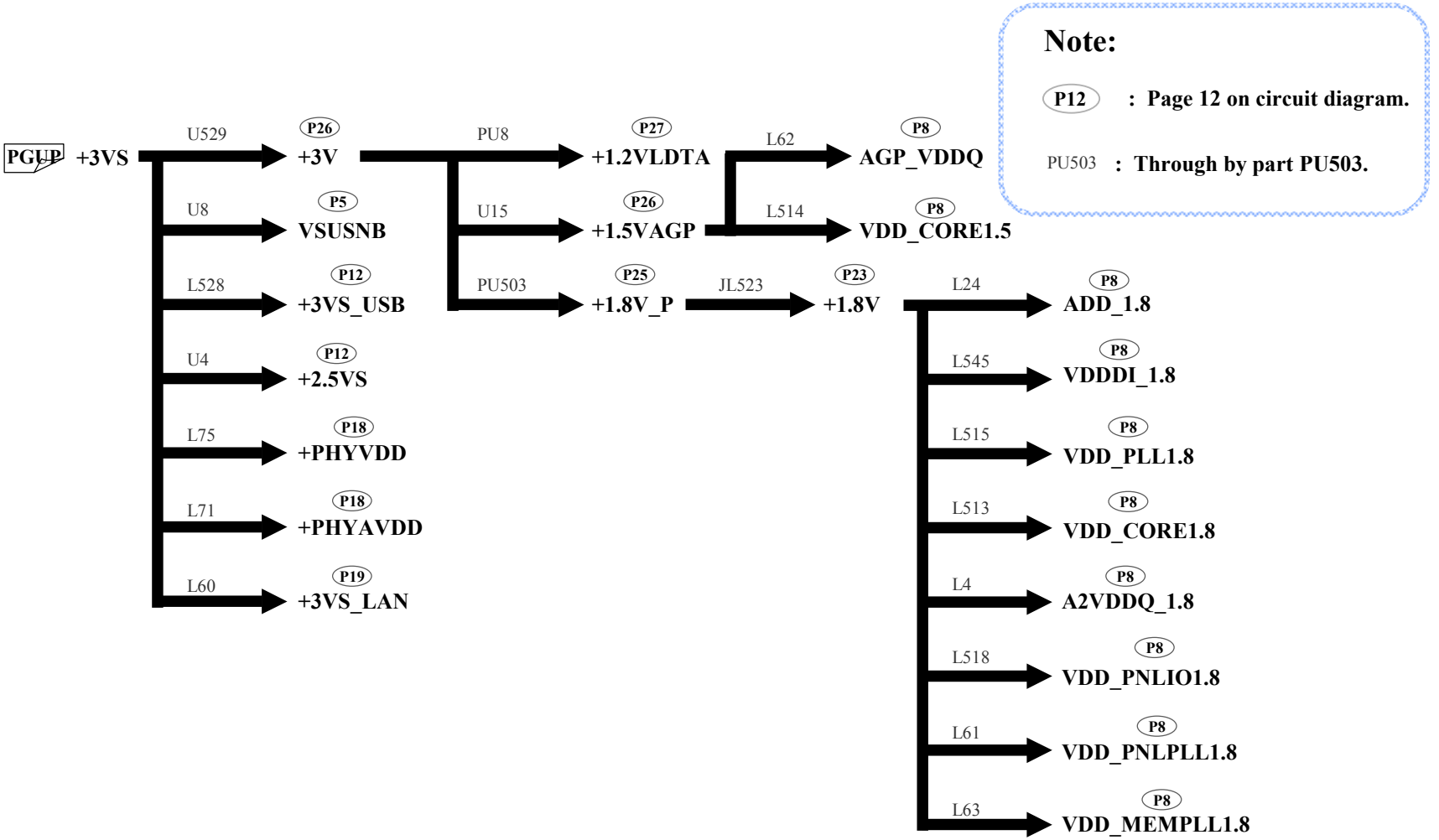
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8355 N/B MAINTENANCE

8.1 No Power

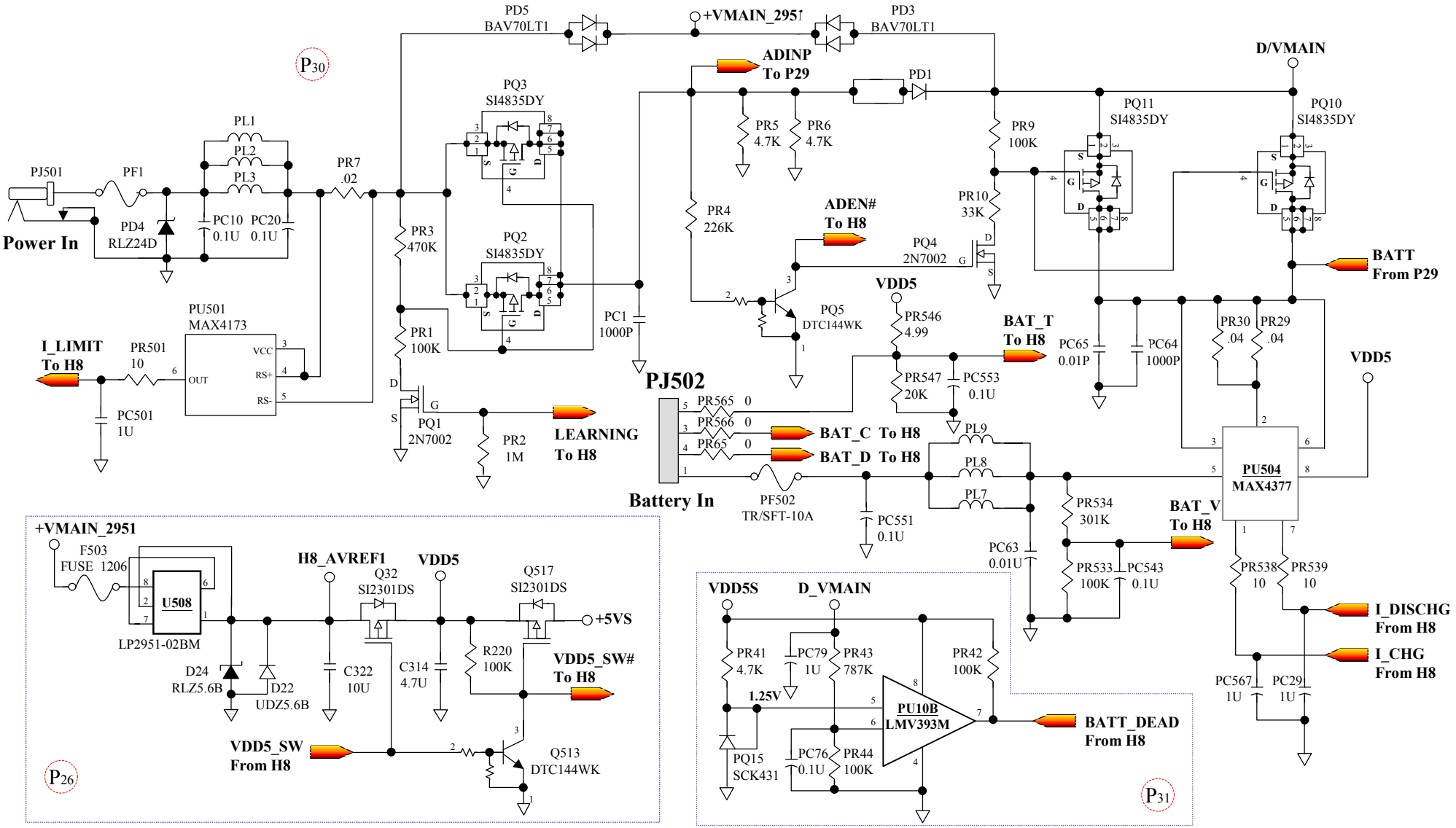
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8355 N/B MAINTENANCE

8.1 No Power:

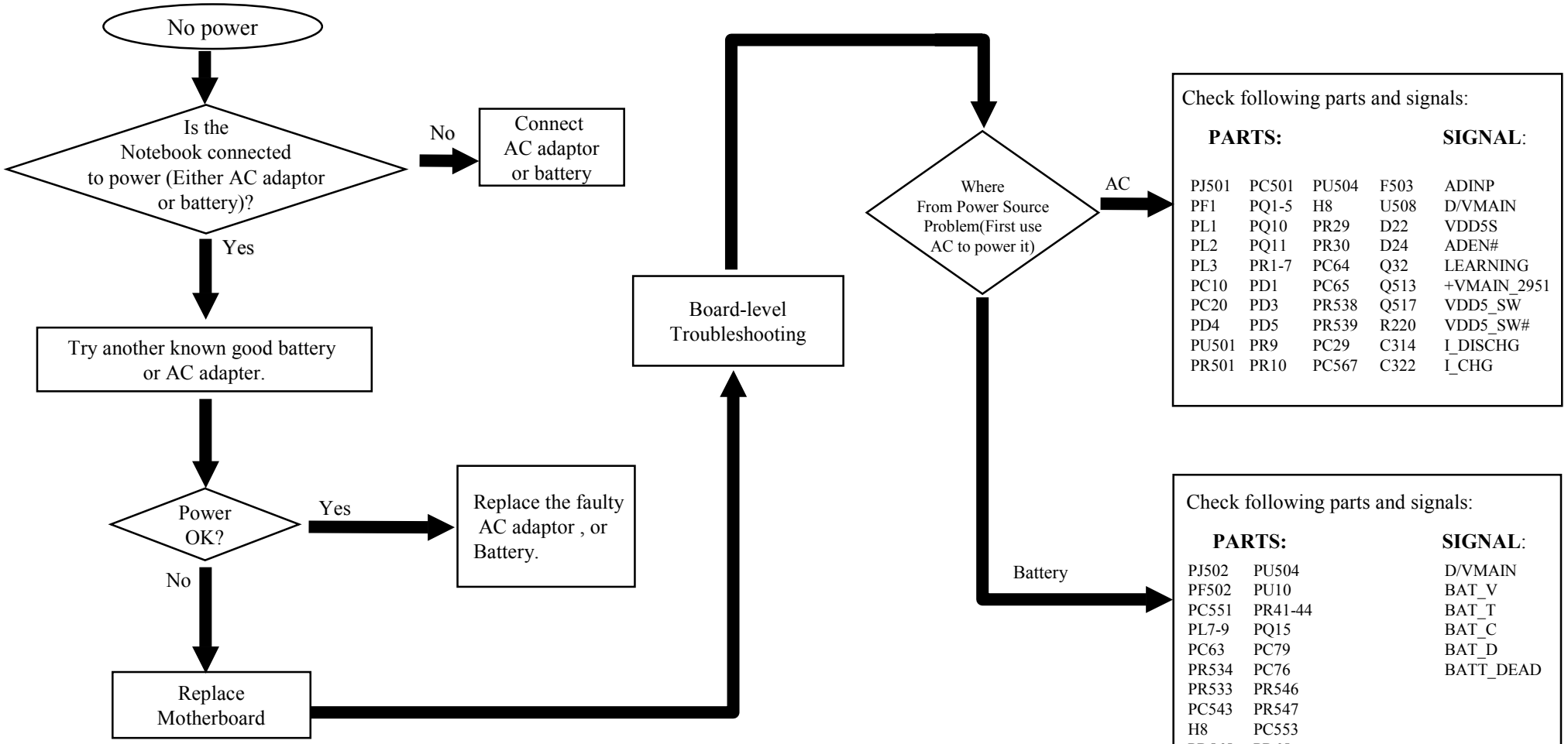
When the power button is pressed, nothing happens ,power indicator does not light up.



8355 N/B MAINTENANCE

8.1 No Power:

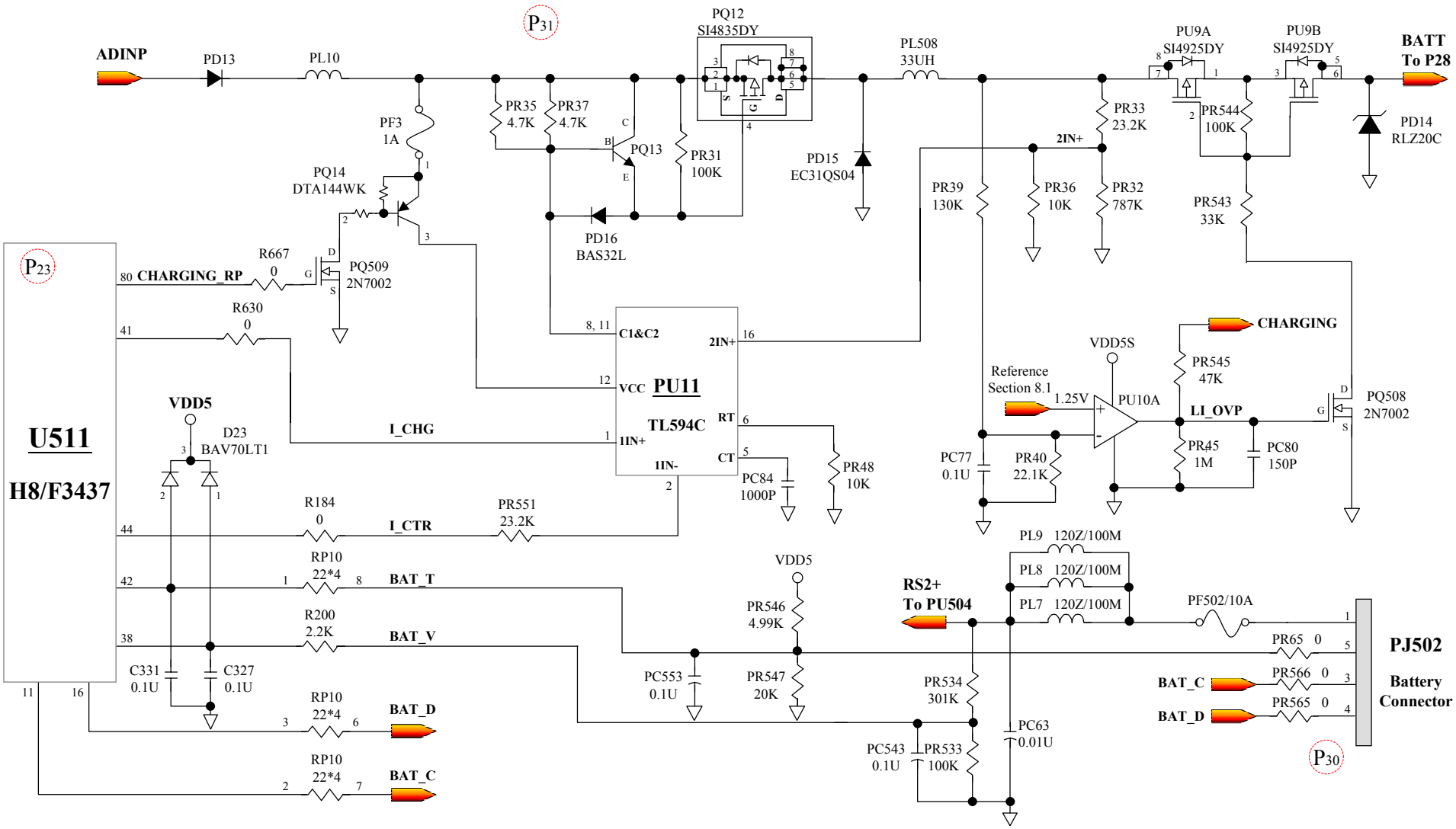
When the power button is pressed, nothing happens ,power indicator does not light up.



8.2 Battery Can not Be Charged

Symptom:

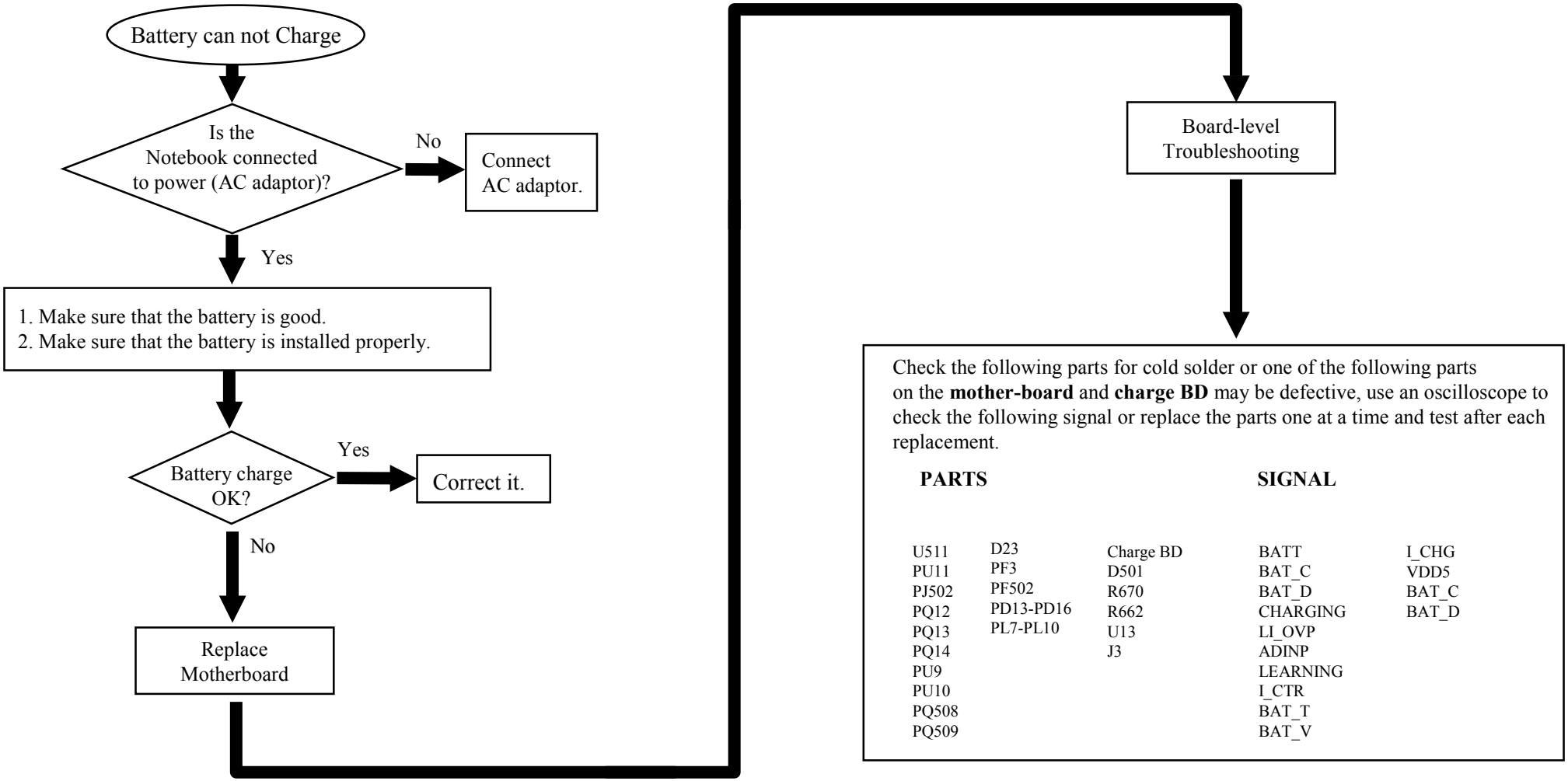
When the battery is installed but the battery status indicate LED display abnormal.



8.2 Battery Can not Be Charged

Symptom:

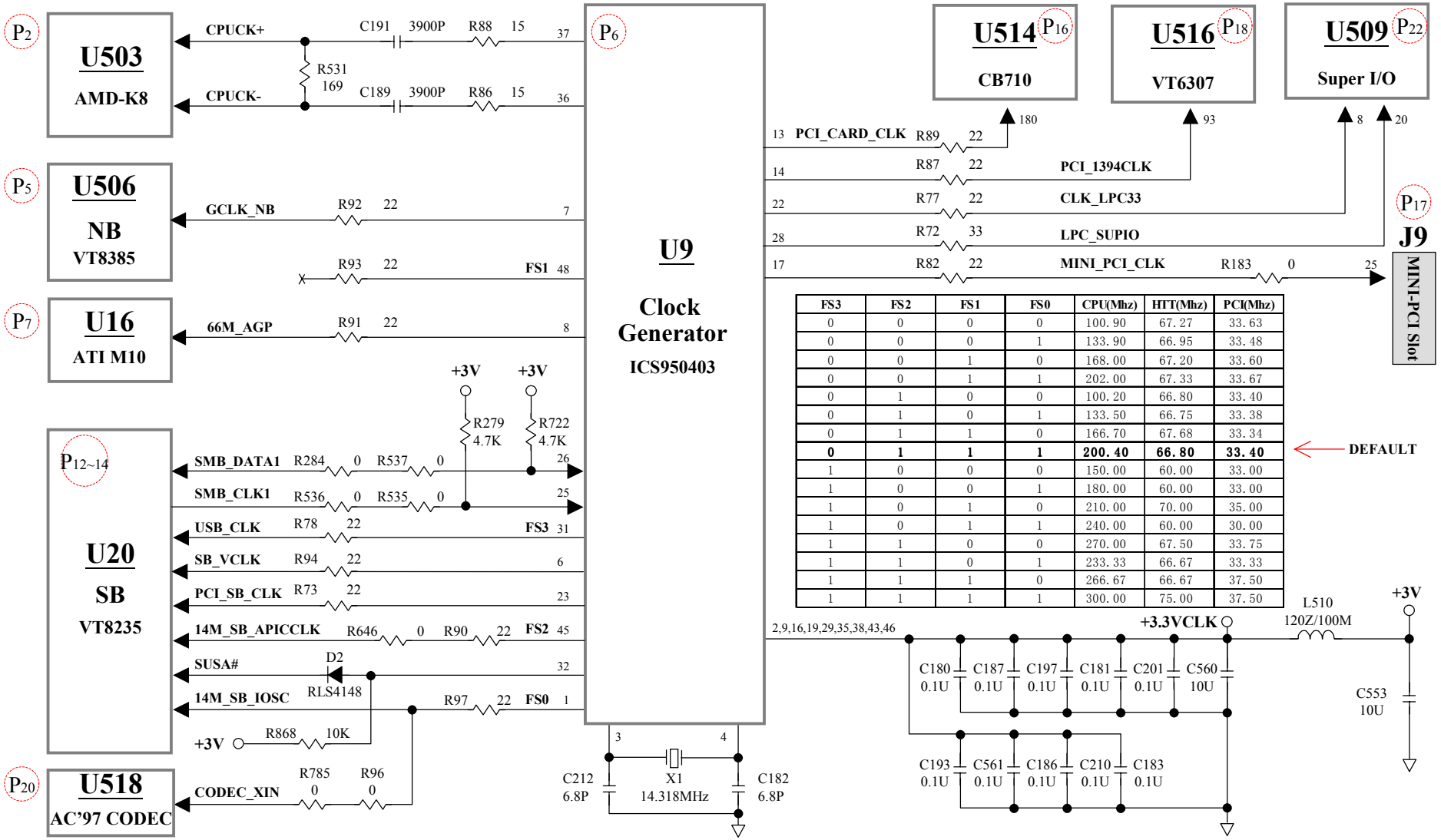
When the battery is installed but the battery status indicate LED display abnormal.



8355 N/B MAINTENANCE

8.3 No Display

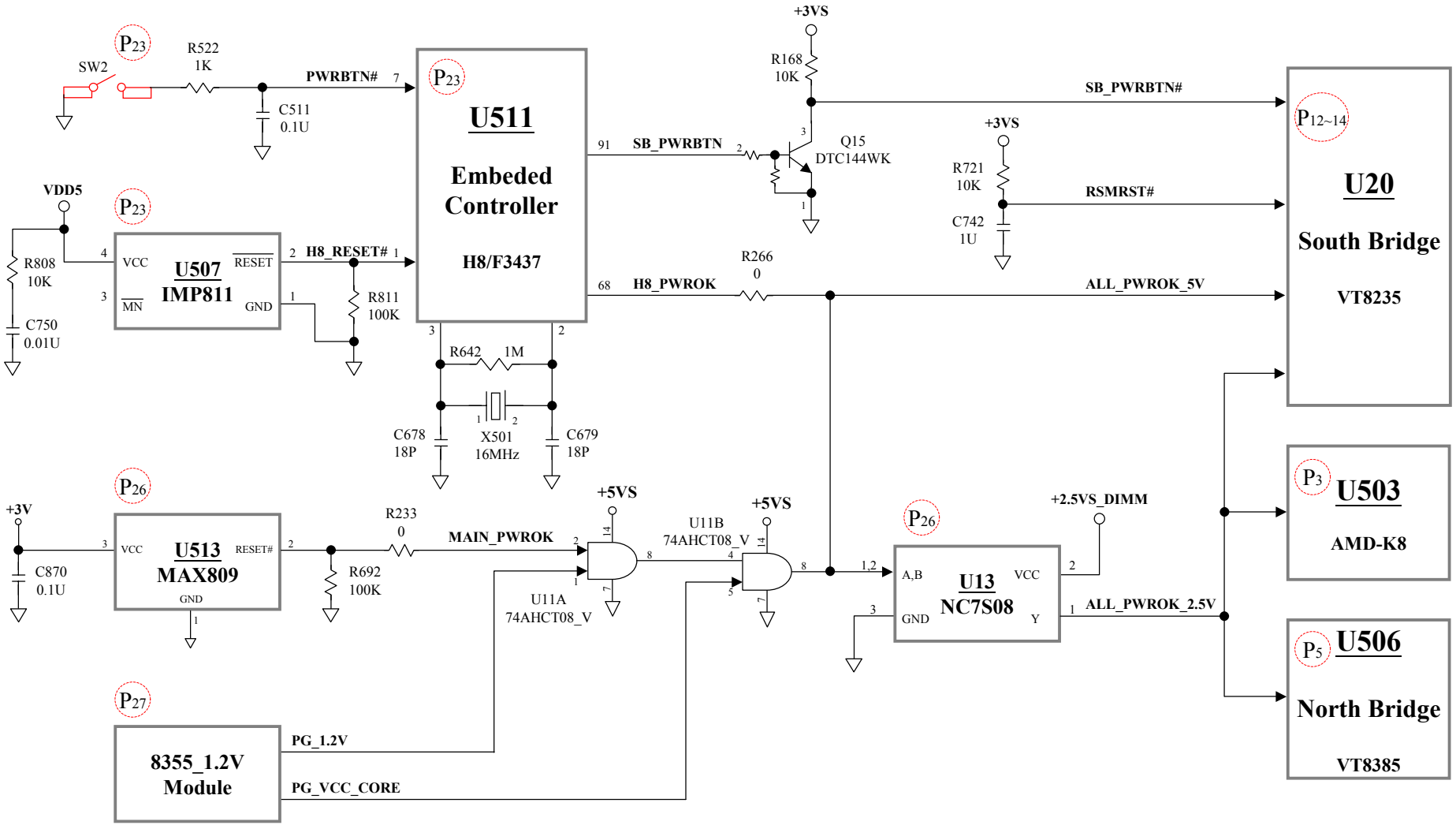
******System Clock Check******



FS3	FS2	FS1	FS0	CPU(Mhz)	HTT(Mhz)	PCI(Mhz)
0	0	0	0	100.90	67.27	33.63
0	0	0	1	133.90	66.95	33.48
0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	67.68	33.34
0	**1**	**1**	**1**	**200.40**	**66.80**	**33.40**
1	0	0	0	150.00	60.00	33.00
1	0	0	1	180.00	60.00	33.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	30.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	37.50
1	1	1	1	300.00	75.00	37.50

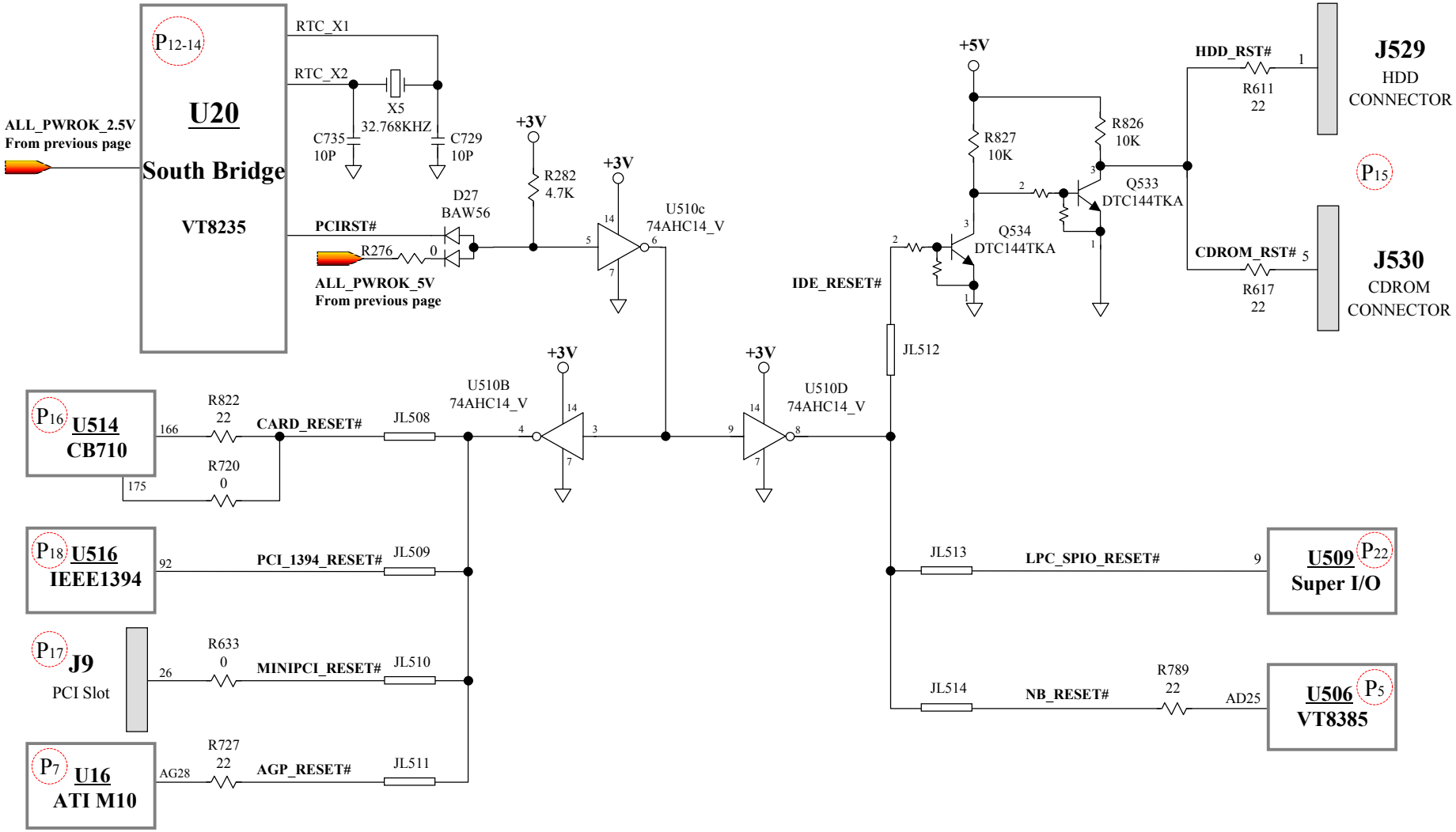
8.3 No Display (System Failure)

******Reset Circuit Checking(1)******

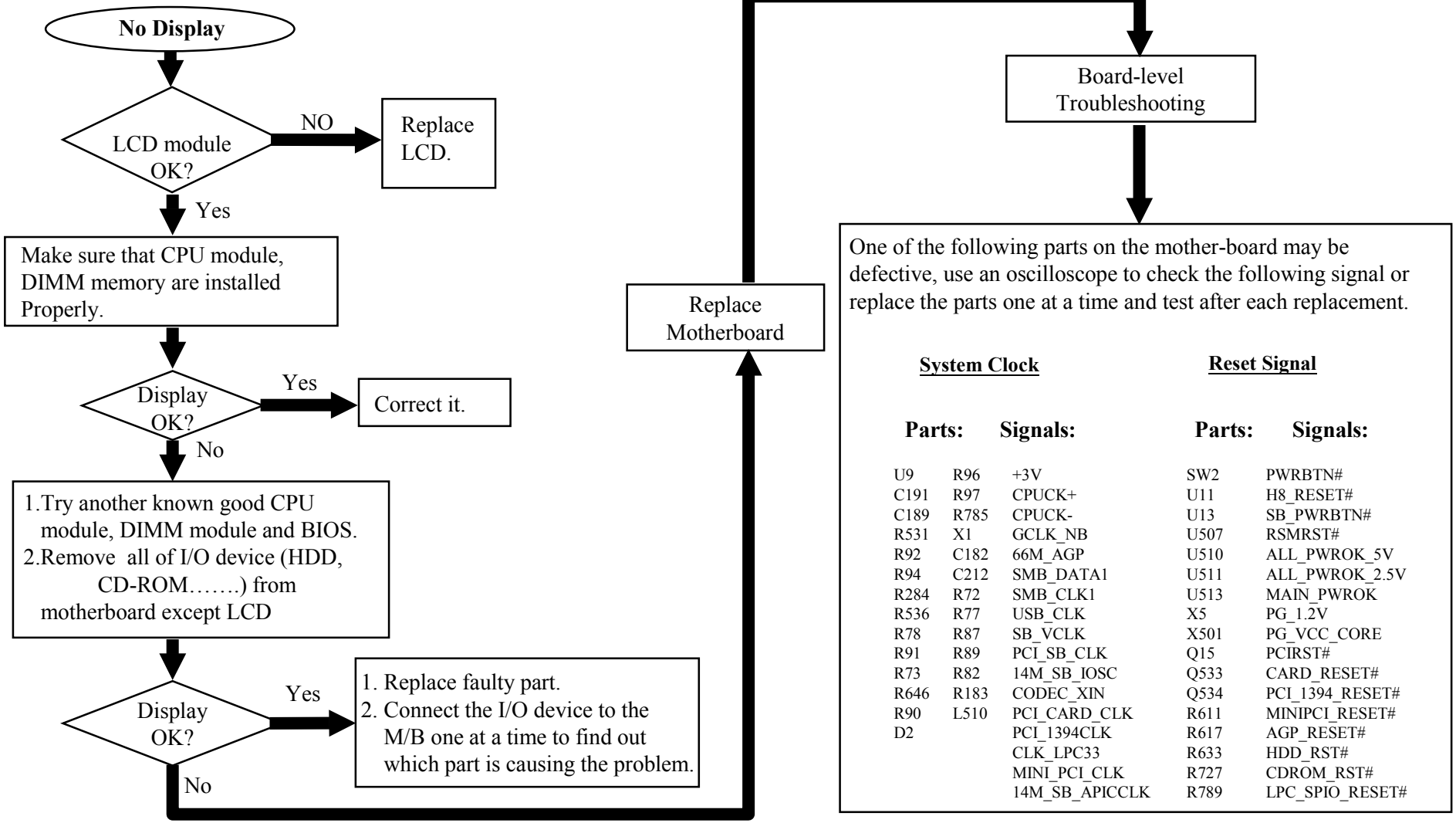


8.3 No Display (System Failure)

******Reset Circuit Checking(2)******



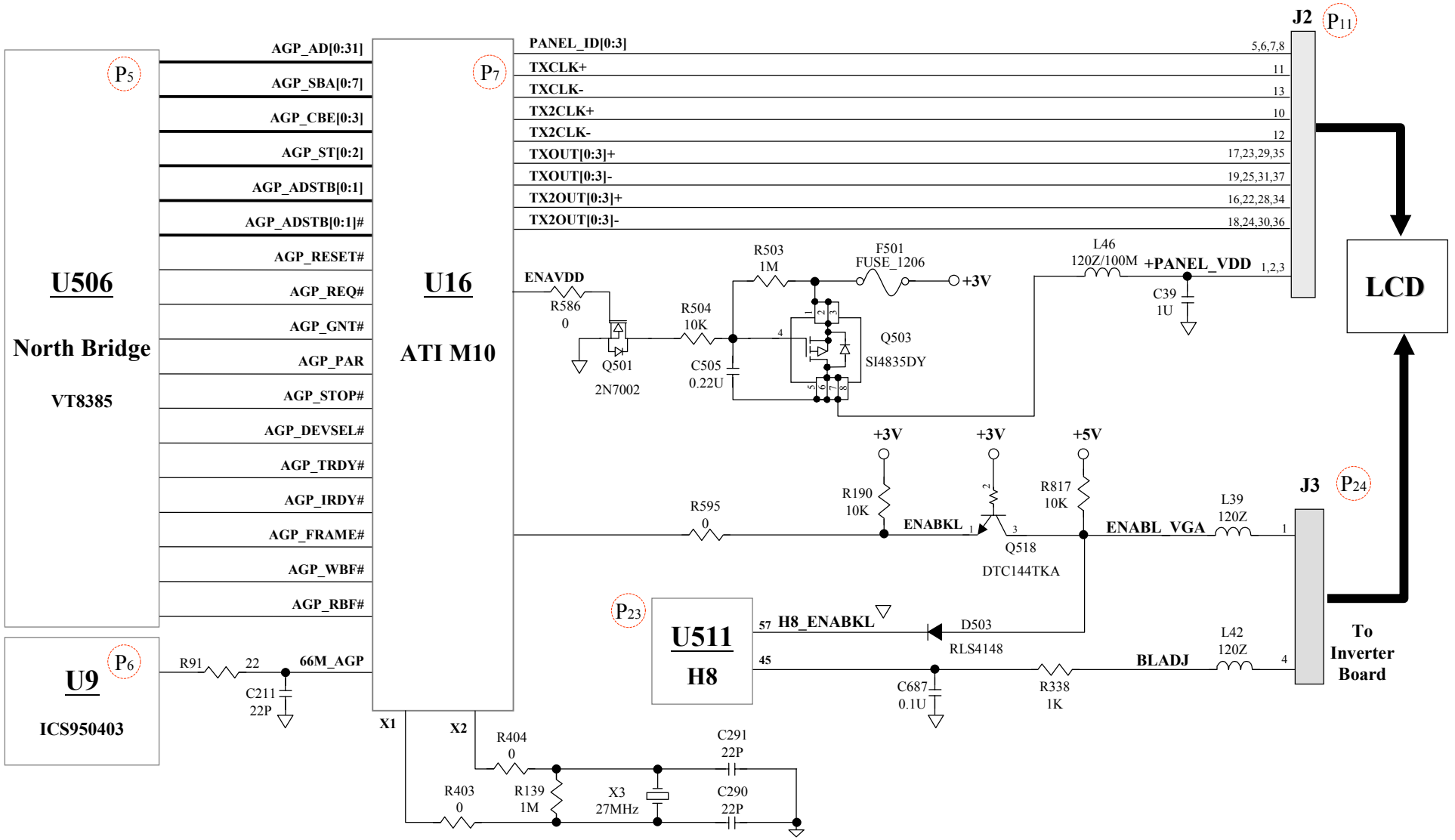
8.3 No Display (System Failure)



8.4 AGP Controller Failure LCD No Display

Symptom:

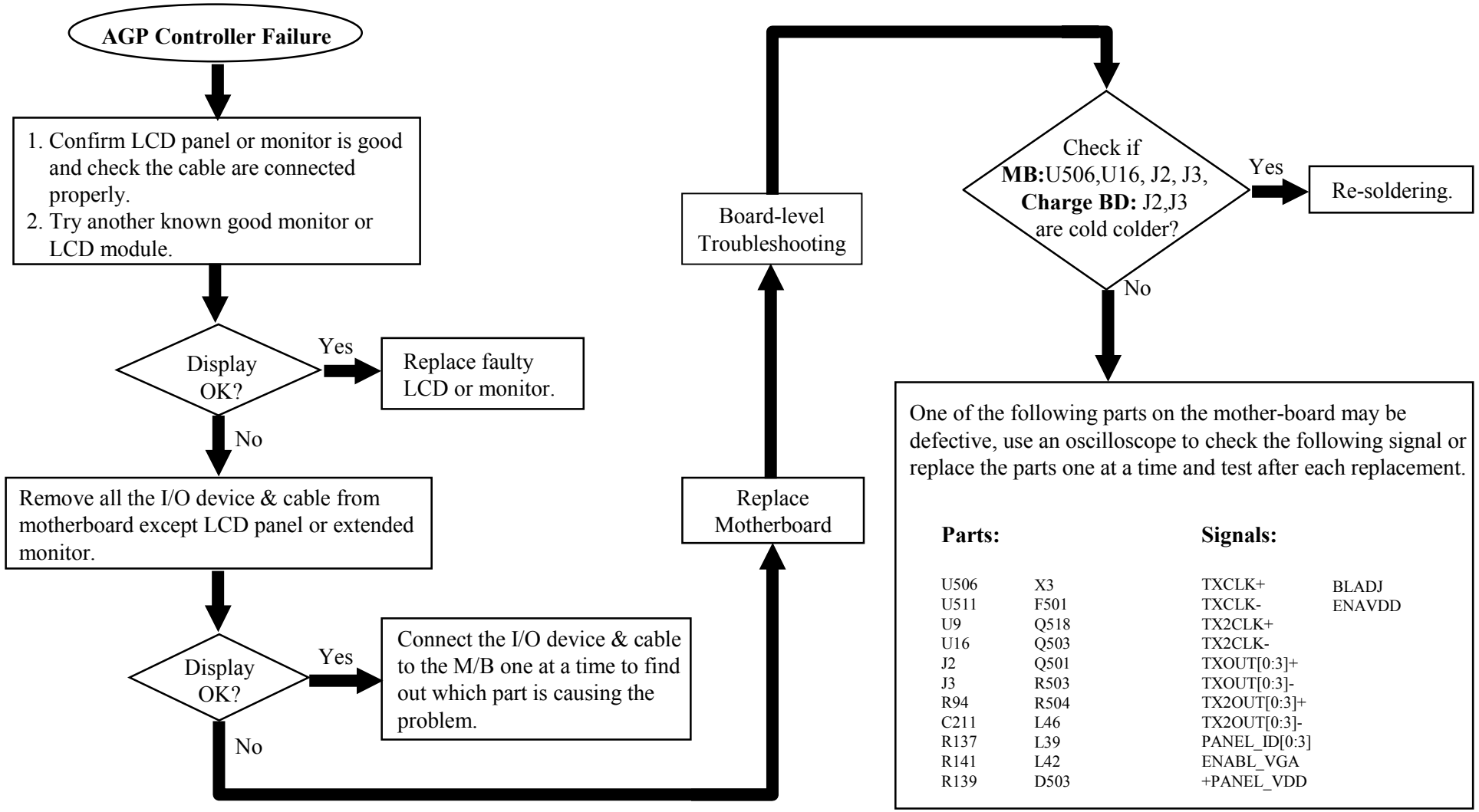
There is no display on LCD although power-on-self-test is passed.



8.4 AGP Controller Failure LCD No Display

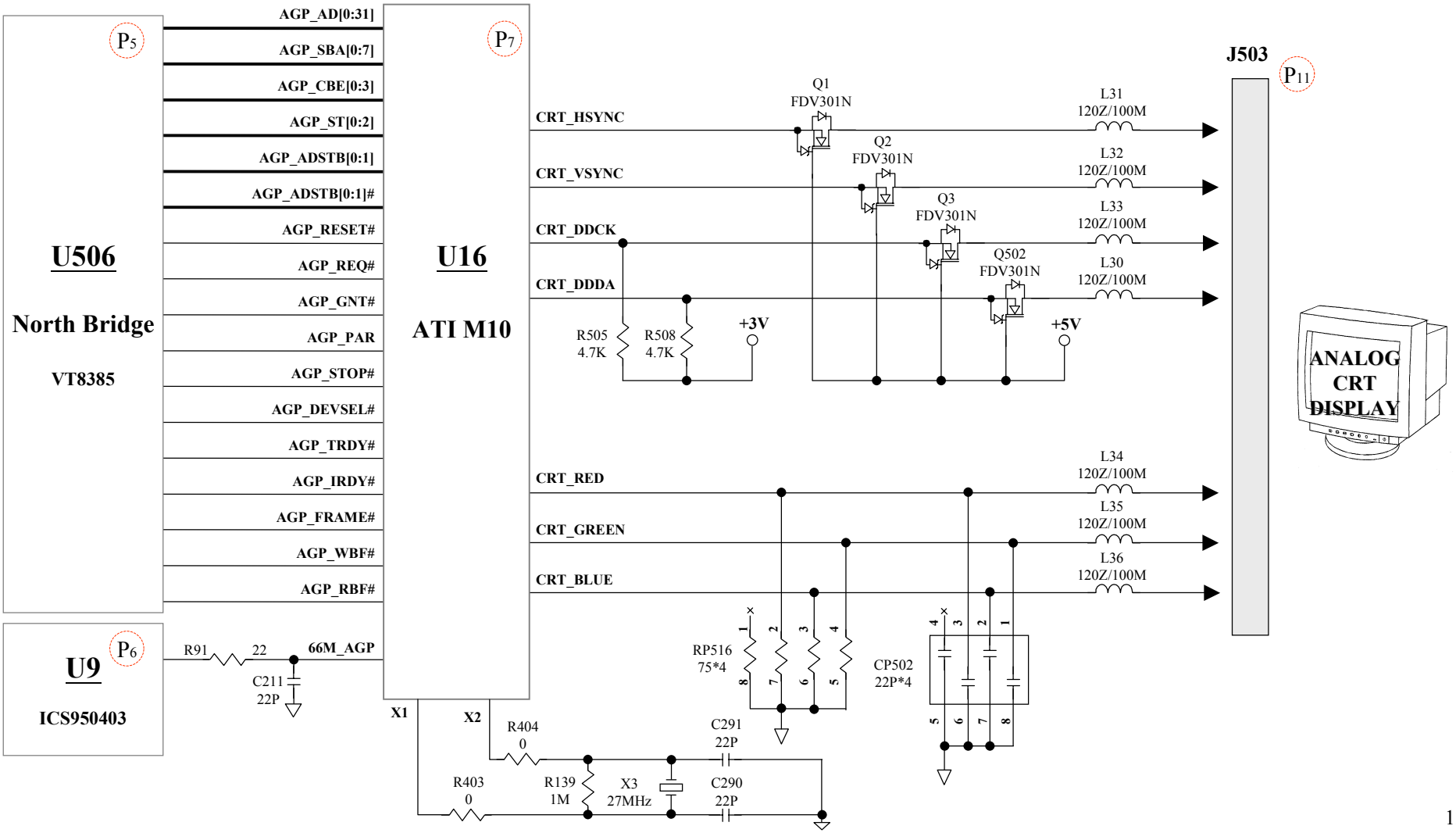
Symptom:

There is no display on LCD although power-on-self-test is passed.



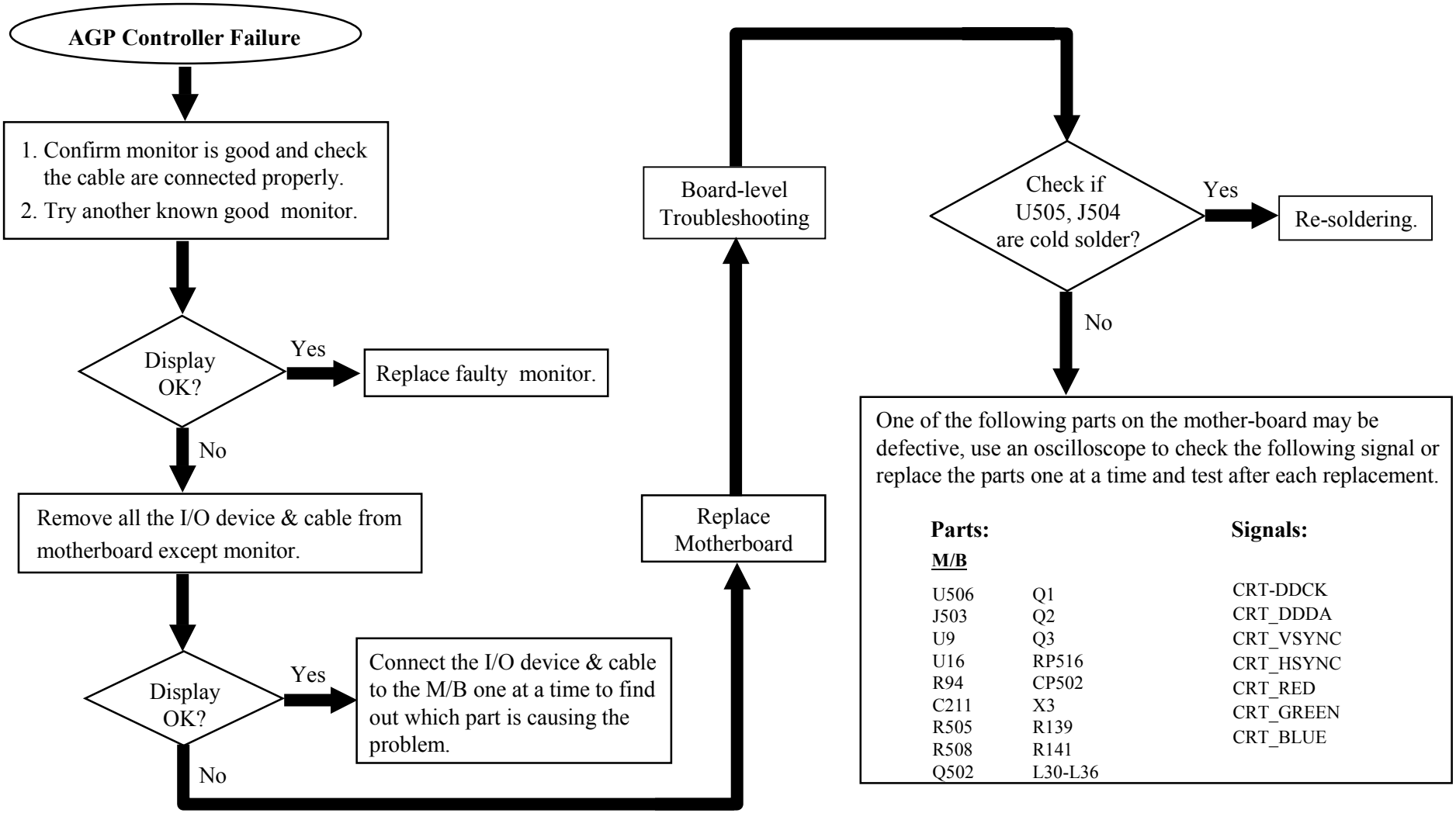
8.5 External Monitor No Display

Symptom:
The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



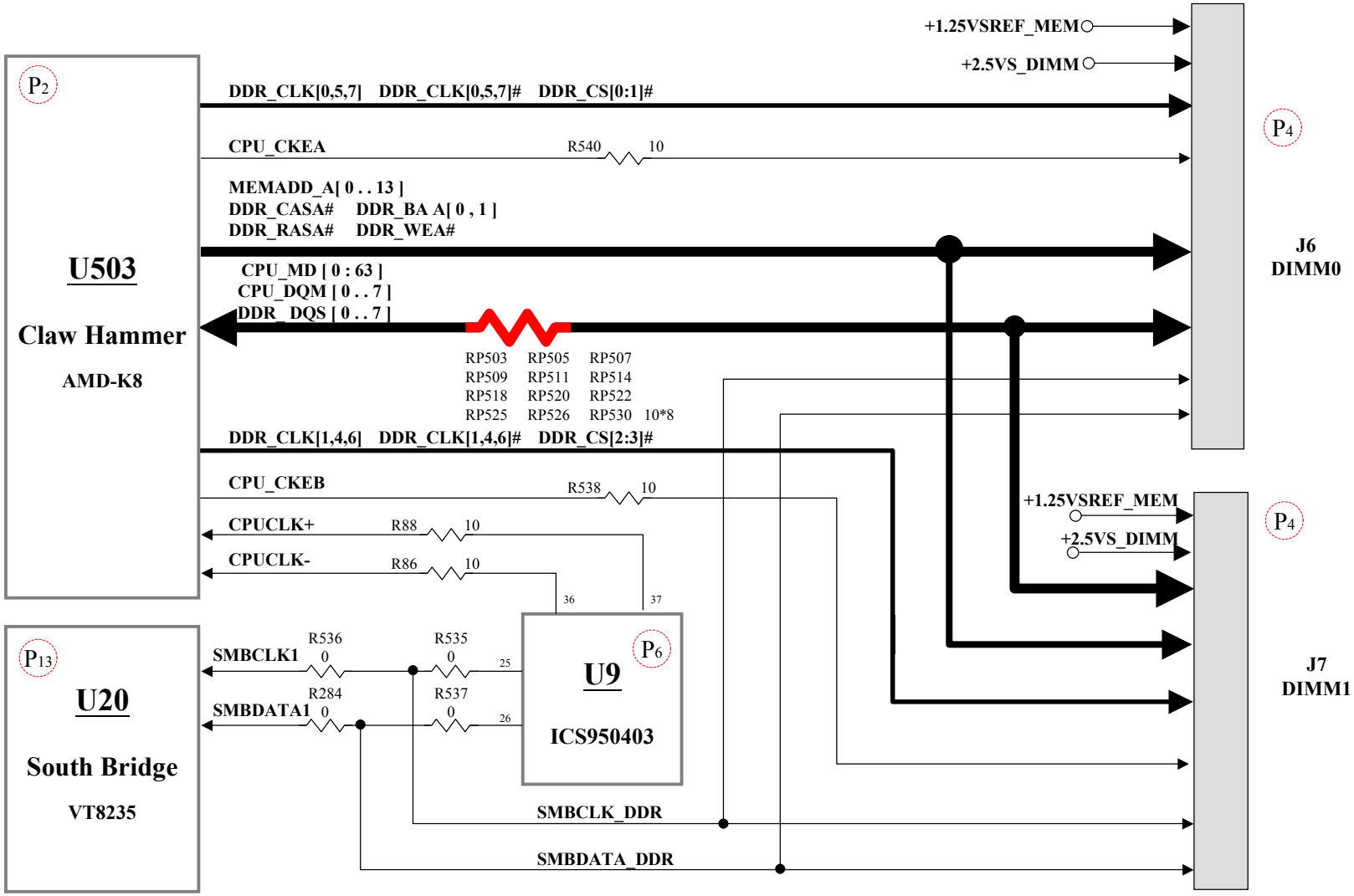
8.5 External Monitor No Display

Symptom:
The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



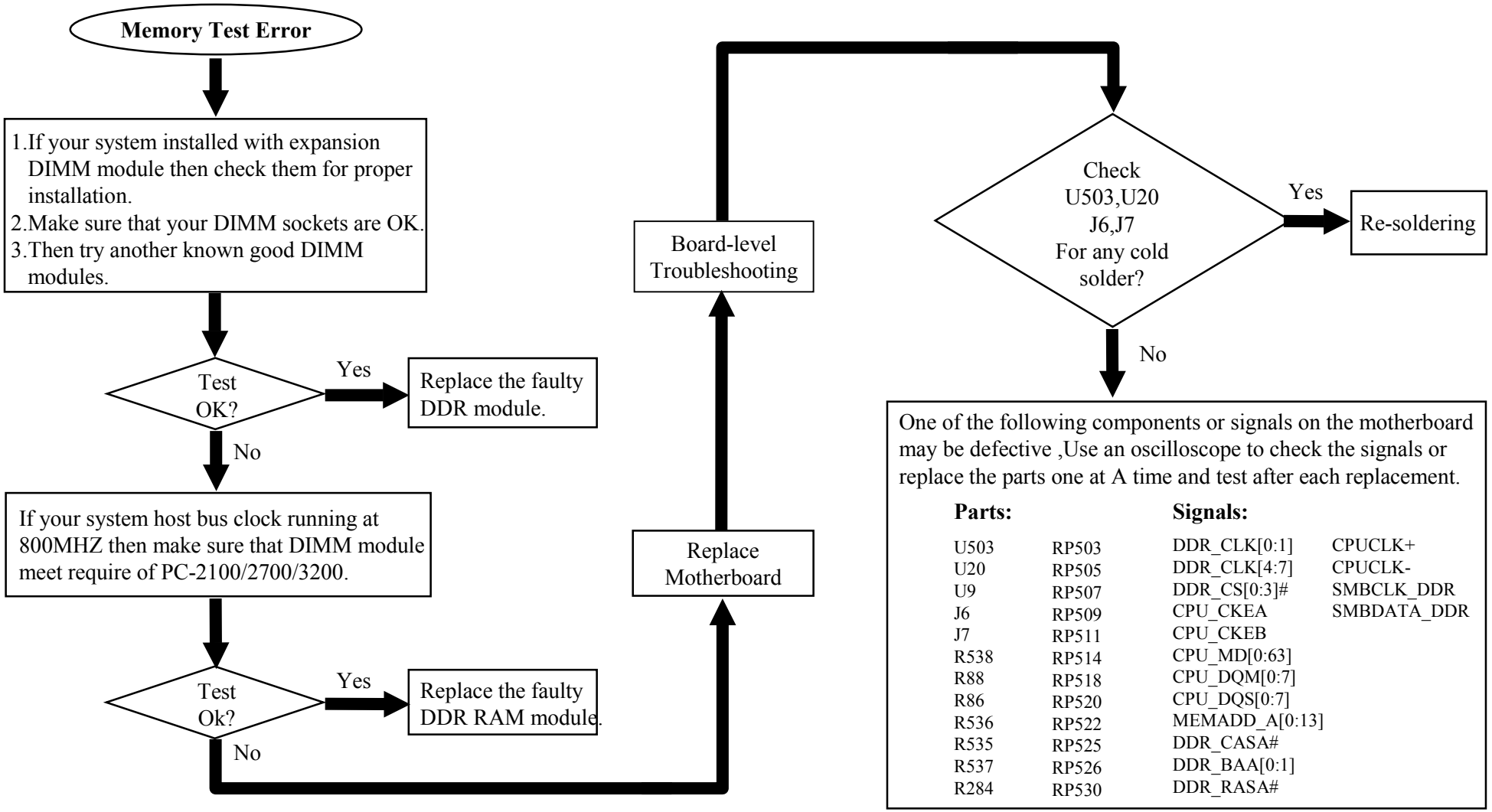
8.6 Memory Test Error

Symptom: The extend DDR RAM is failure or system hangs up.



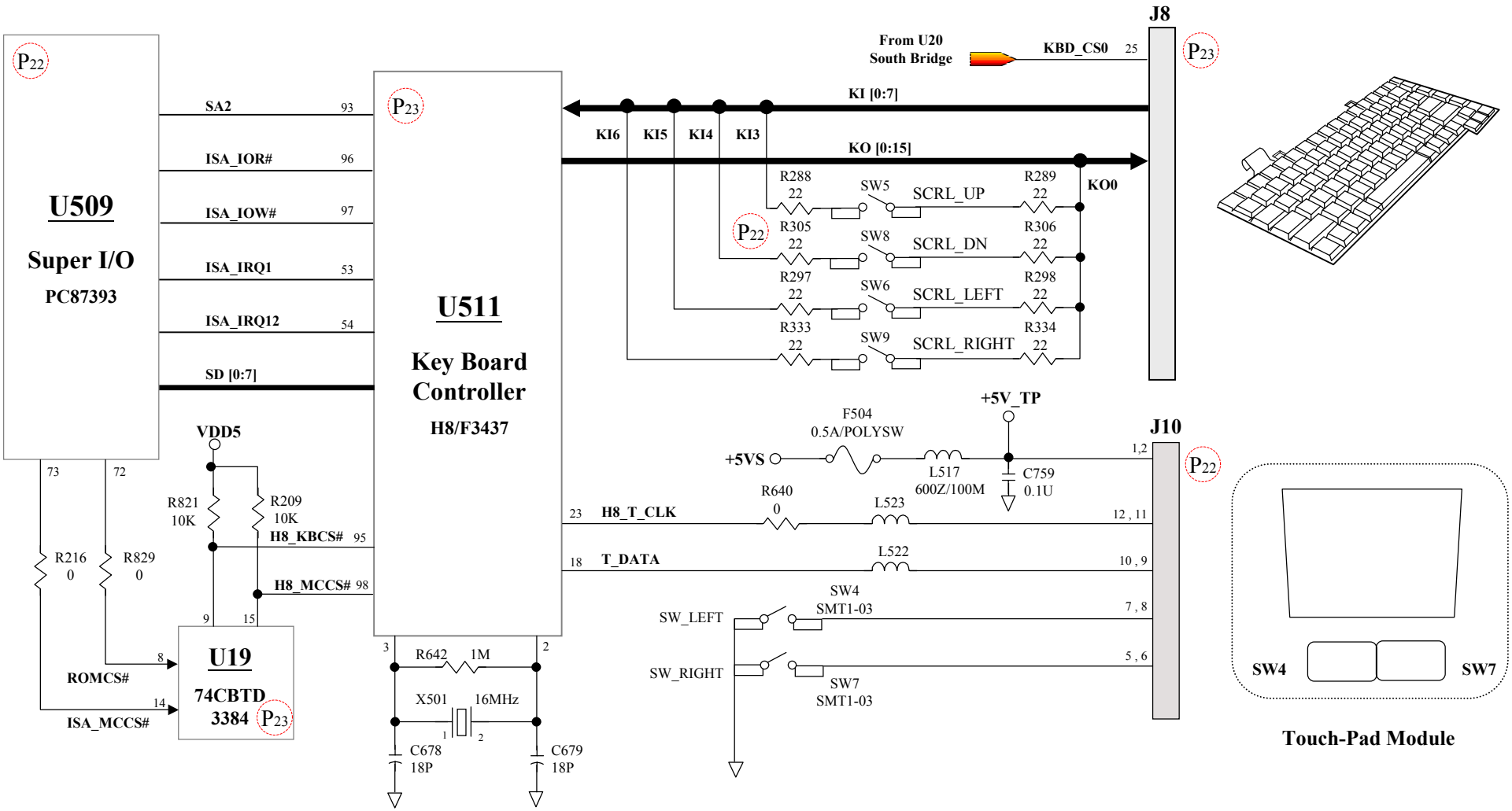
8.6 Memory Test Error

Symptom:
Either on board or extend DDR RAM is failure or system hangs up.



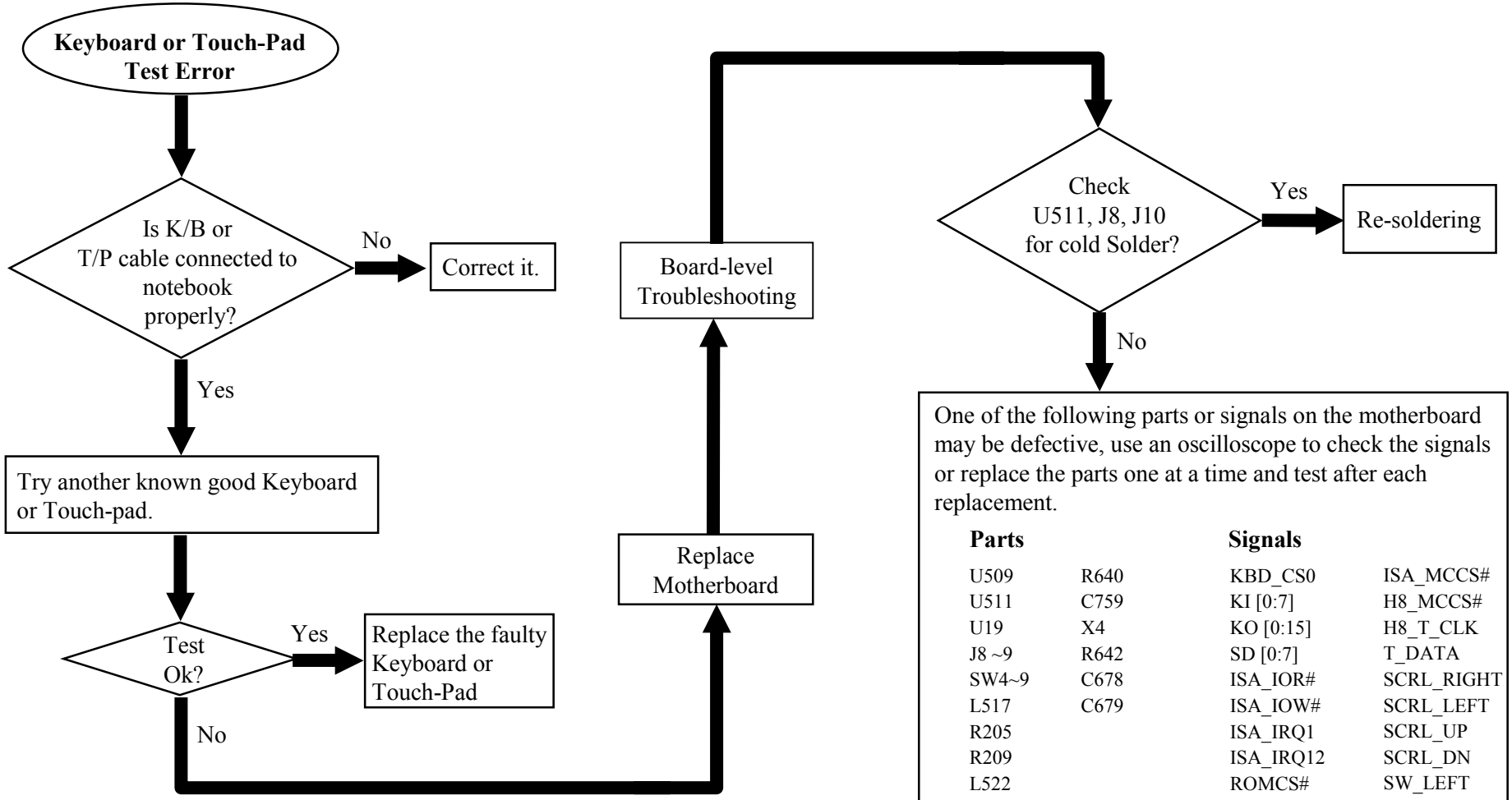
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

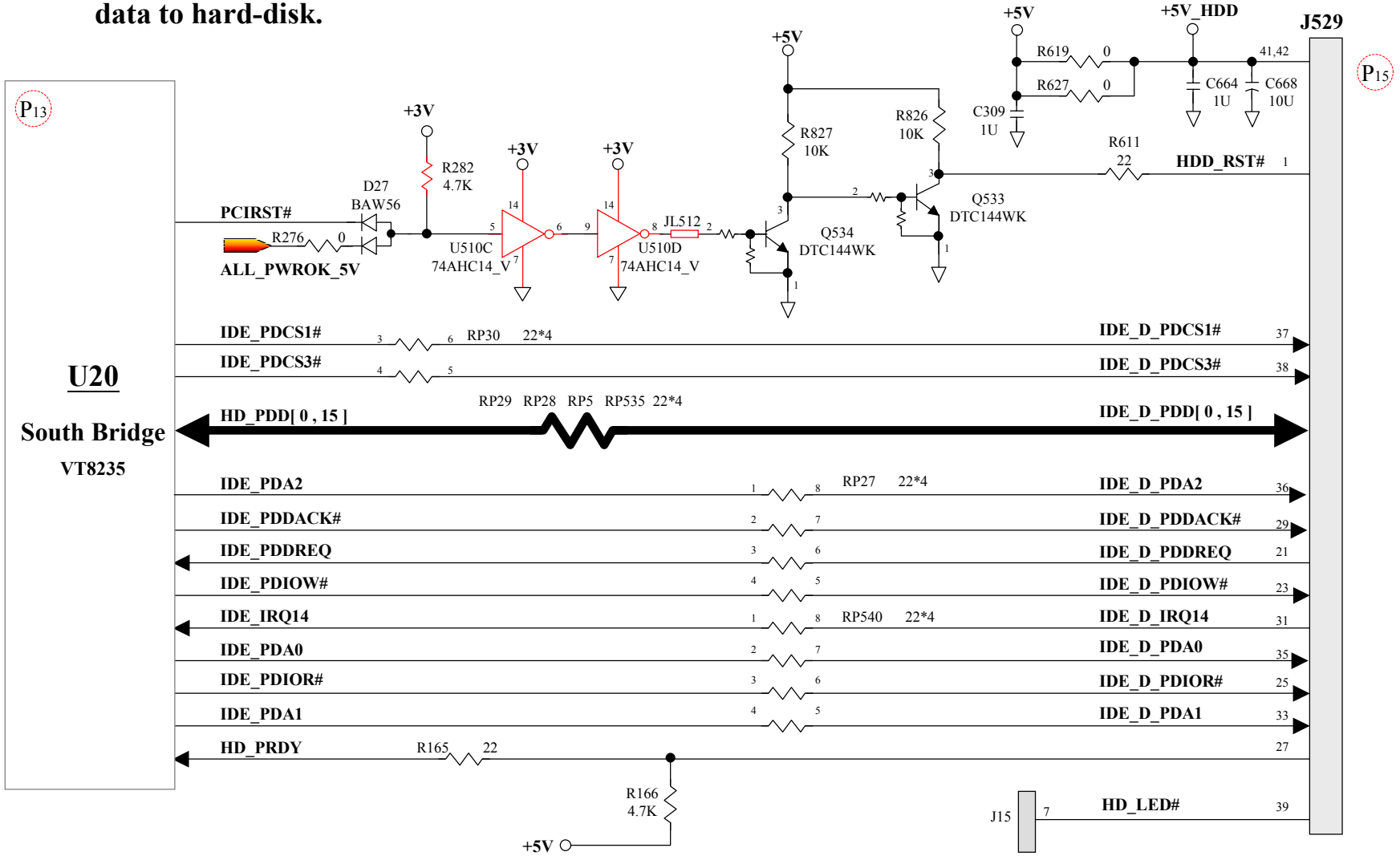
Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.8 Hard Disk Driver Test Error

Symptom:

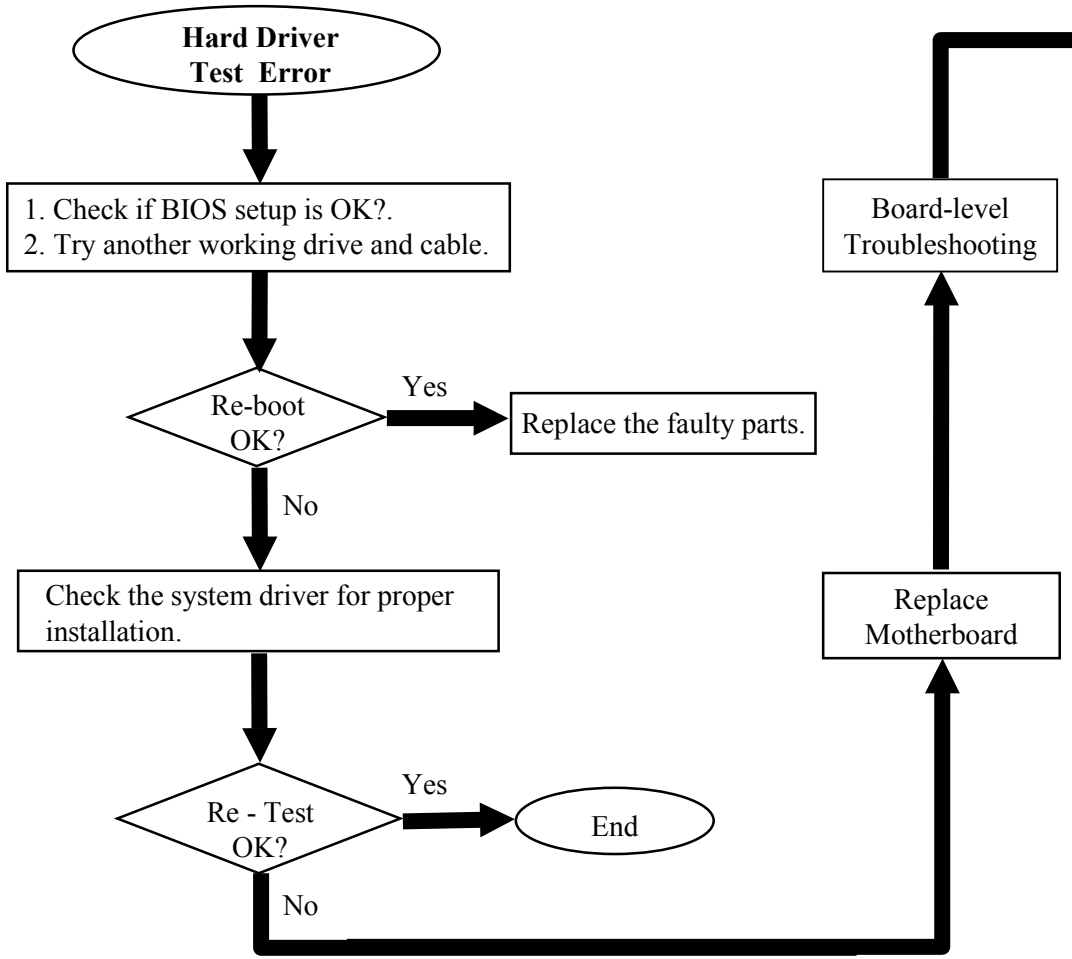
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



8.8 Hard Disk Driver Test Error

Symptom:

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



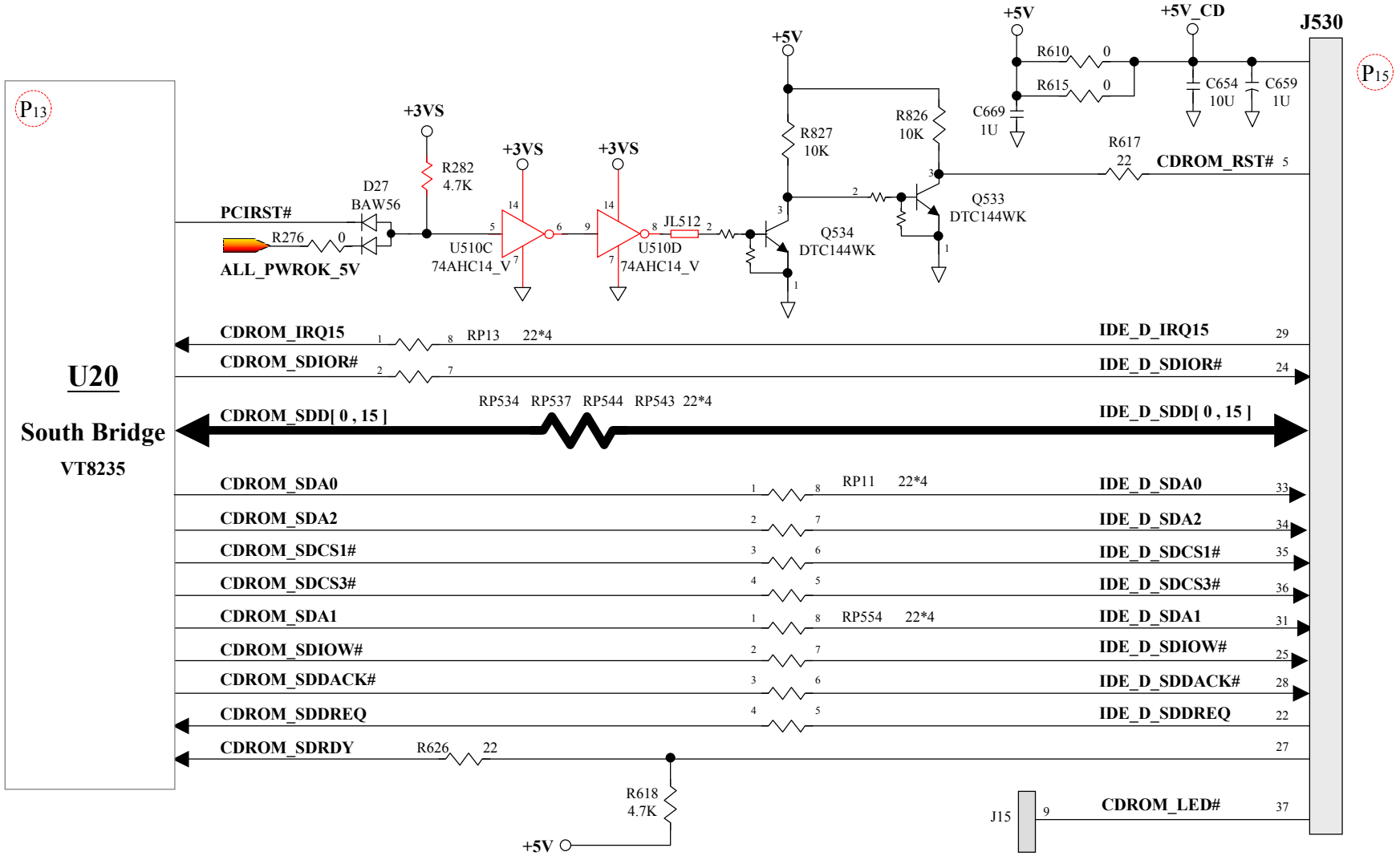
One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:		SIGNALS:
U20	Q534	+5V_HDD
U510	R611	PCIRST#
J529	R282	ALL_PWROK_5V
J15	R617	IDE_PDCS1#
RP27	R627	IDE_PDCS3#
RP540	R827	HD_PDD[0:15]
R165	R826	IDE_PDA2
R166	C664	IDE_PDDACK#
RP29	C668	IDE_PDIOW#
RP28	JL512	IDE_IRQ14
RP5		IDE_PDA0
RP535		IDE_PDIOR#
RP30		IDE_PDA1
D27		HD_PRDY
R282		HDD_RST#
Q533		HD_LED#

8.9 CD-ROM Driver Test Error

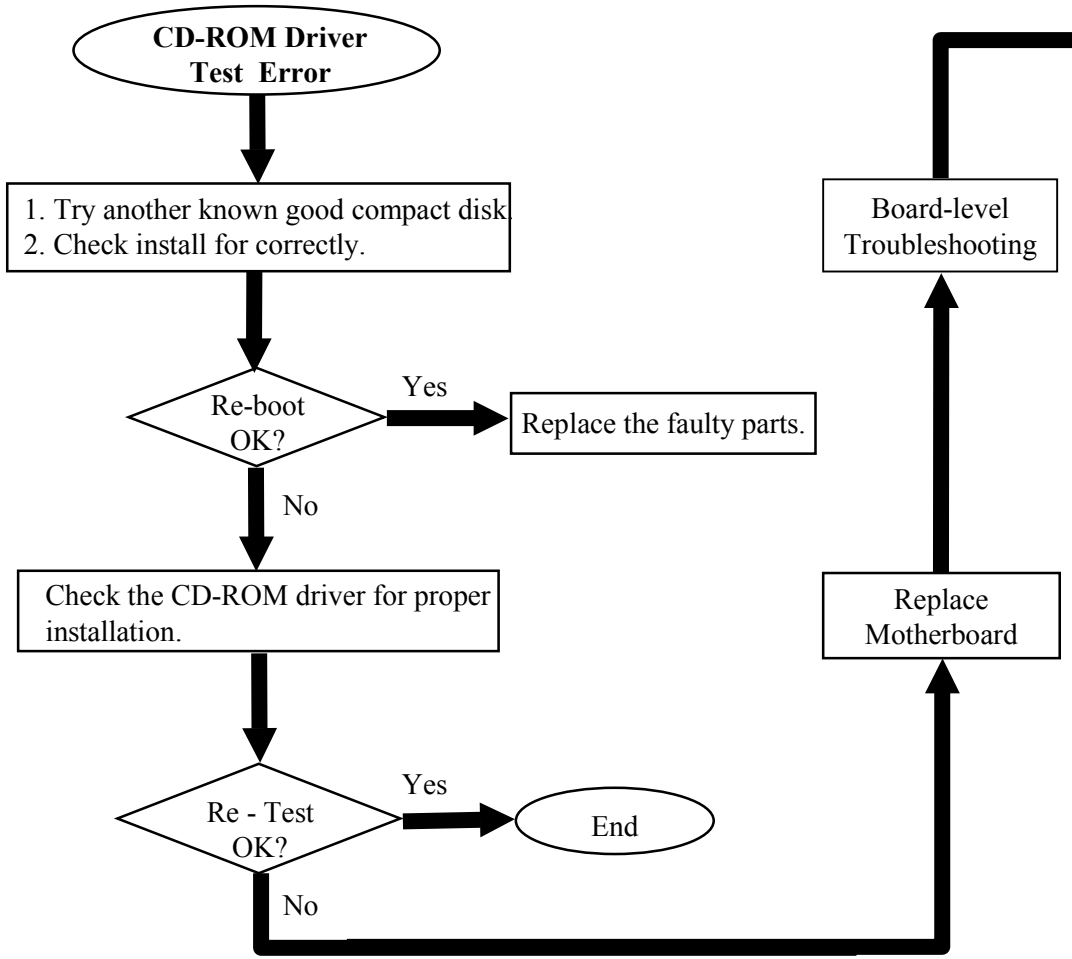
Symptom:

An error message is shown when reading data from CD-ROM drive.



8.9 CD-ROM Driver Test Error

Symptom:
An error message is shown when reading data from CD-ROM drive.

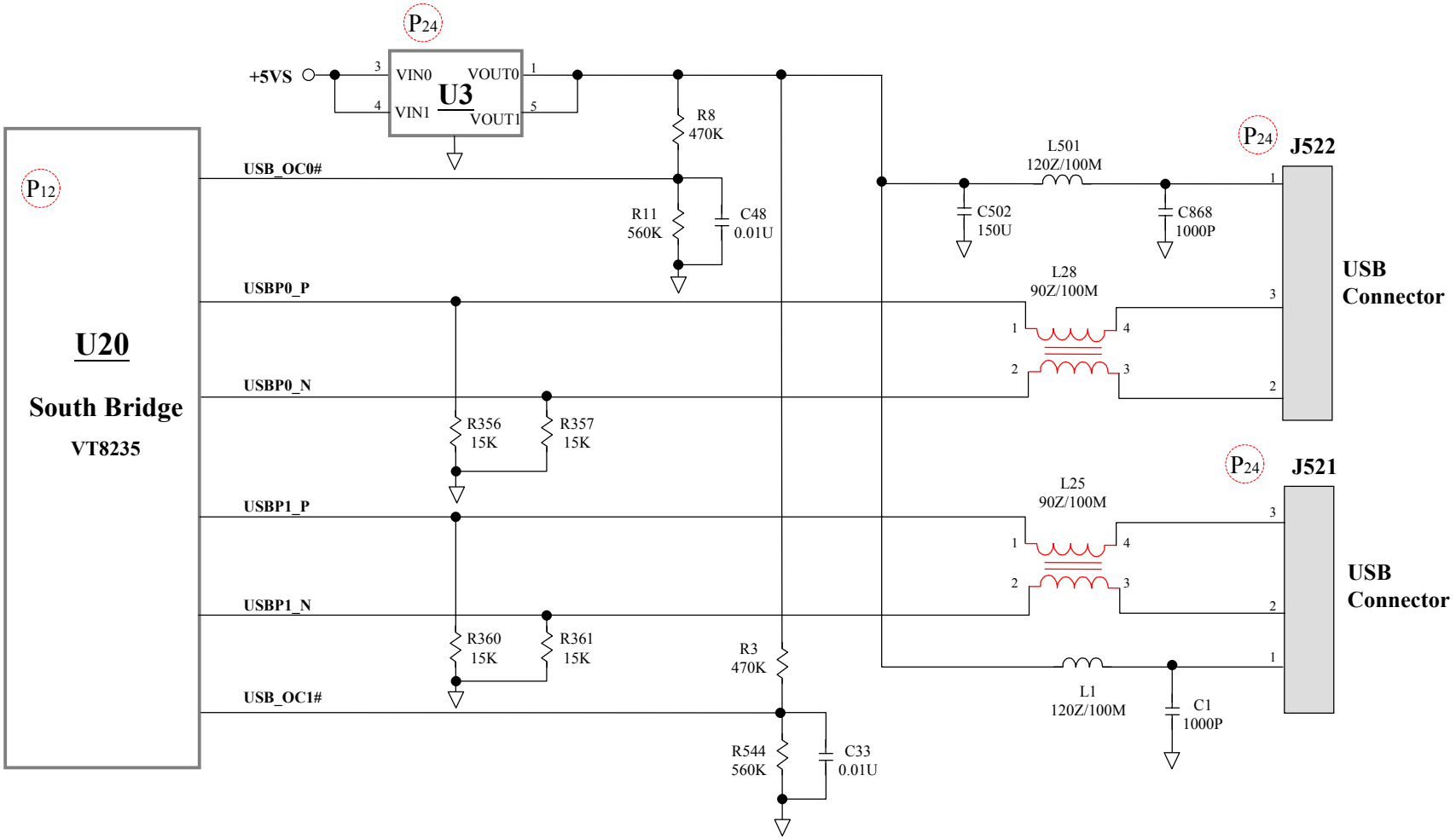


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:		SIGNALS:
U20	R617	+5V_CD
D27	R626	PCIRST#
R276	RP13	ALL_PWROK_5V
R282	RP11	CDROM_SDCS1#
JL512	RP554	CDROM_SDCS3#
U510	R618	CDROM_SDD[0:15]
Q533	J530	CDROM_SDA2
Q534	J15	CDROM_SDDACK#
R827		CDROM_SDIOW#
R826		CDROM_IRQ15
R610		CDROM_SDA0
R615		CDROM_SDIOR#
C654		CDROM_SDA1
C659		CDROM_SDRDY
		CDROM_RST#
		CDROM_LED#

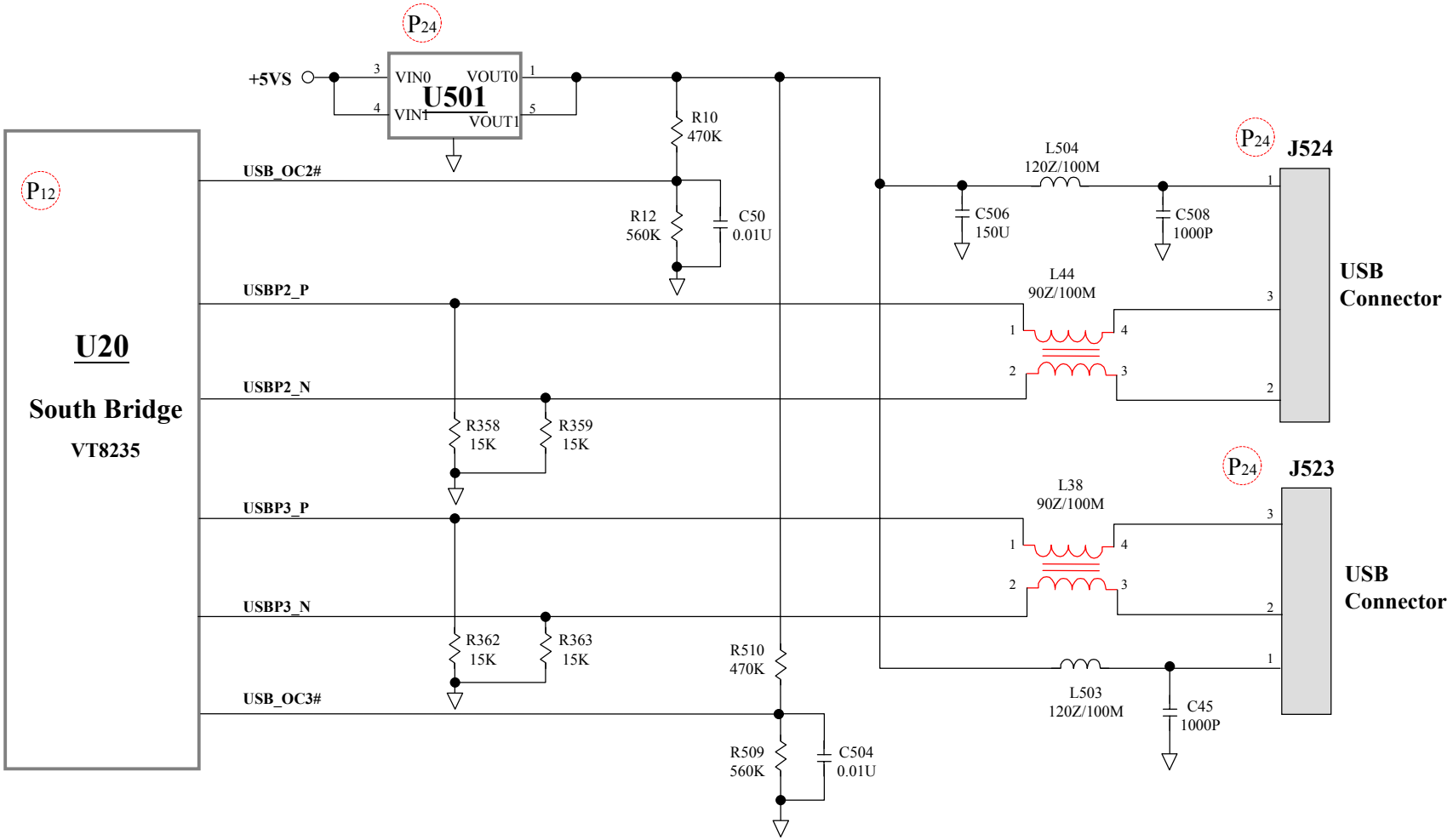
8.10 USB Test Error (1)

Symptom: An error occurs when a USB I/O device is installed.



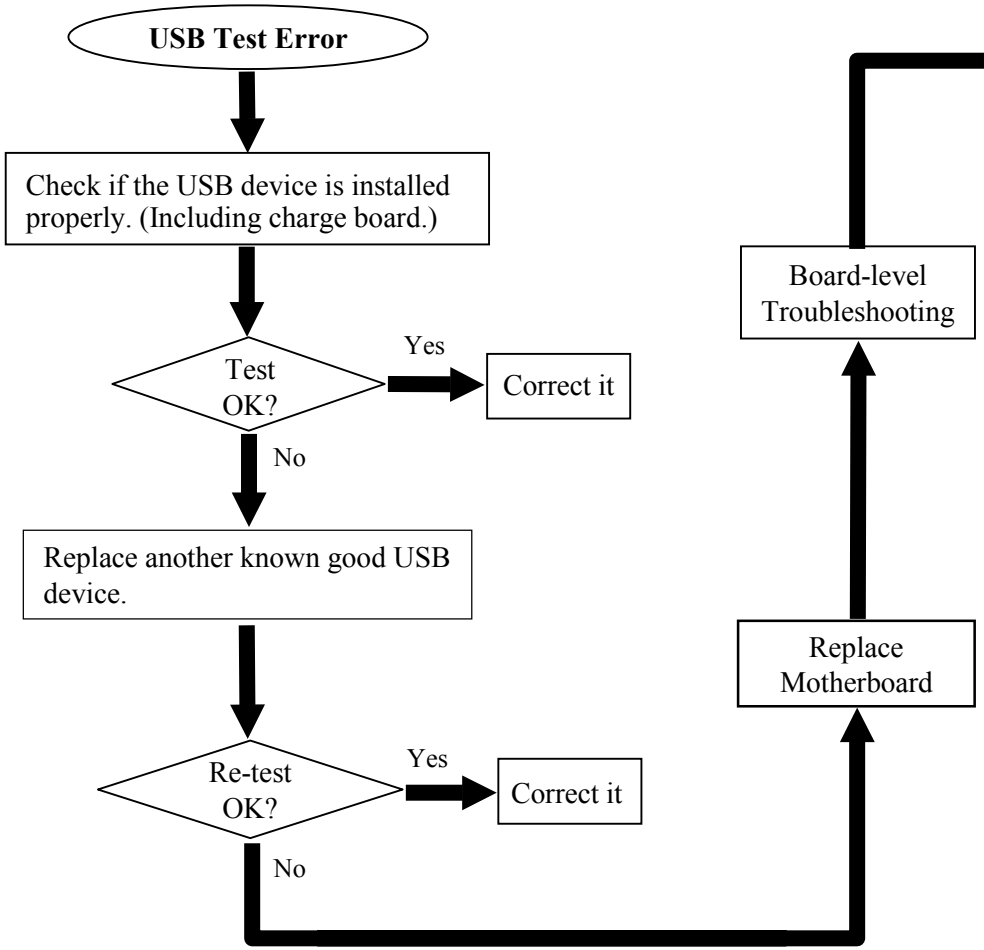
8.10 USB Test Error (2)

Symptom: An error occurs when a USB I/O device is installed.



8.10 USB Test Error

Symptom:
An error occurs when a USB I/O device is installed.

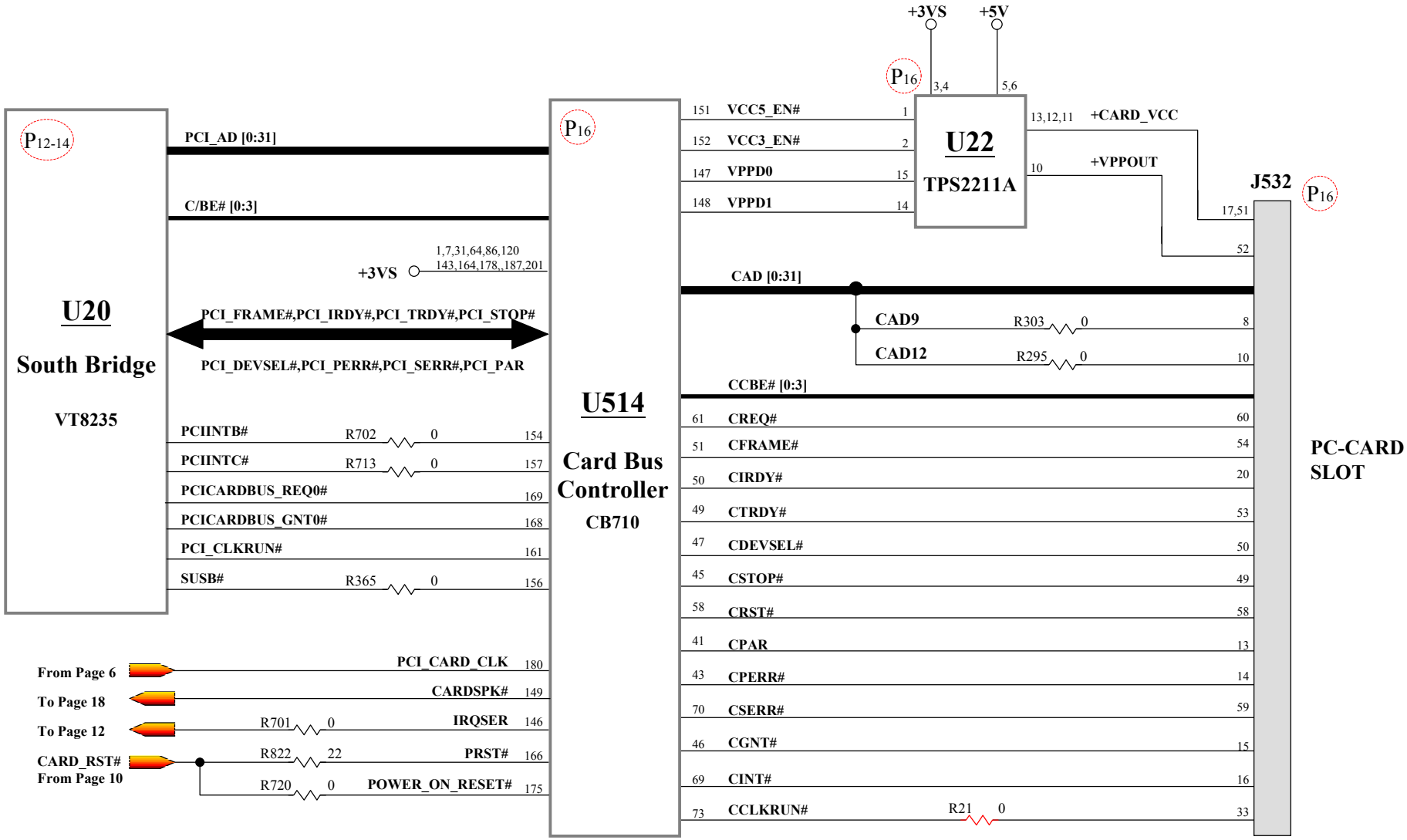


Check the following parts for cold solder or one of the following parts on the MB and Charge BD may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:			**Signals:**
U20	L28	C45	+5VS
U3	L14	R510	USB_OC[0:3]#
U501	L38	R509	USBP0_P
J521-524	R360-363	C504	USBP0_N
R8	R356-359		USBP1_P
R10-12	C502		USBP1_N
C48	C868		USBP2_P
C50	C506		USBP2_N
L501	C508		USBP3_P
L503	R3		USBP3_N
L504	R544		
L1	C33		
L25	C1		

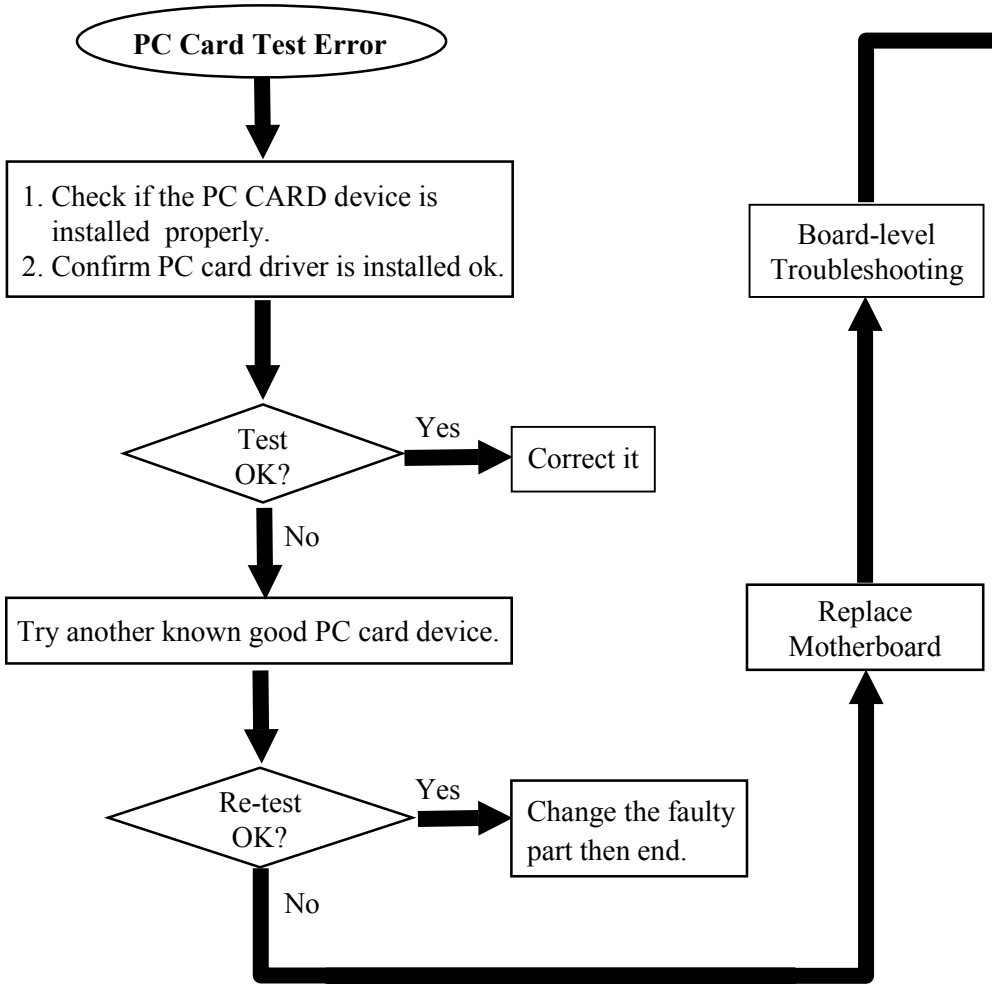
8.11 PC-Card Socket Failure

Symptom : An error occurs when a PC card device is installed.



8.11 PC-Card Socket Failure

Symptom : An error occurs when a PC card device is installed.

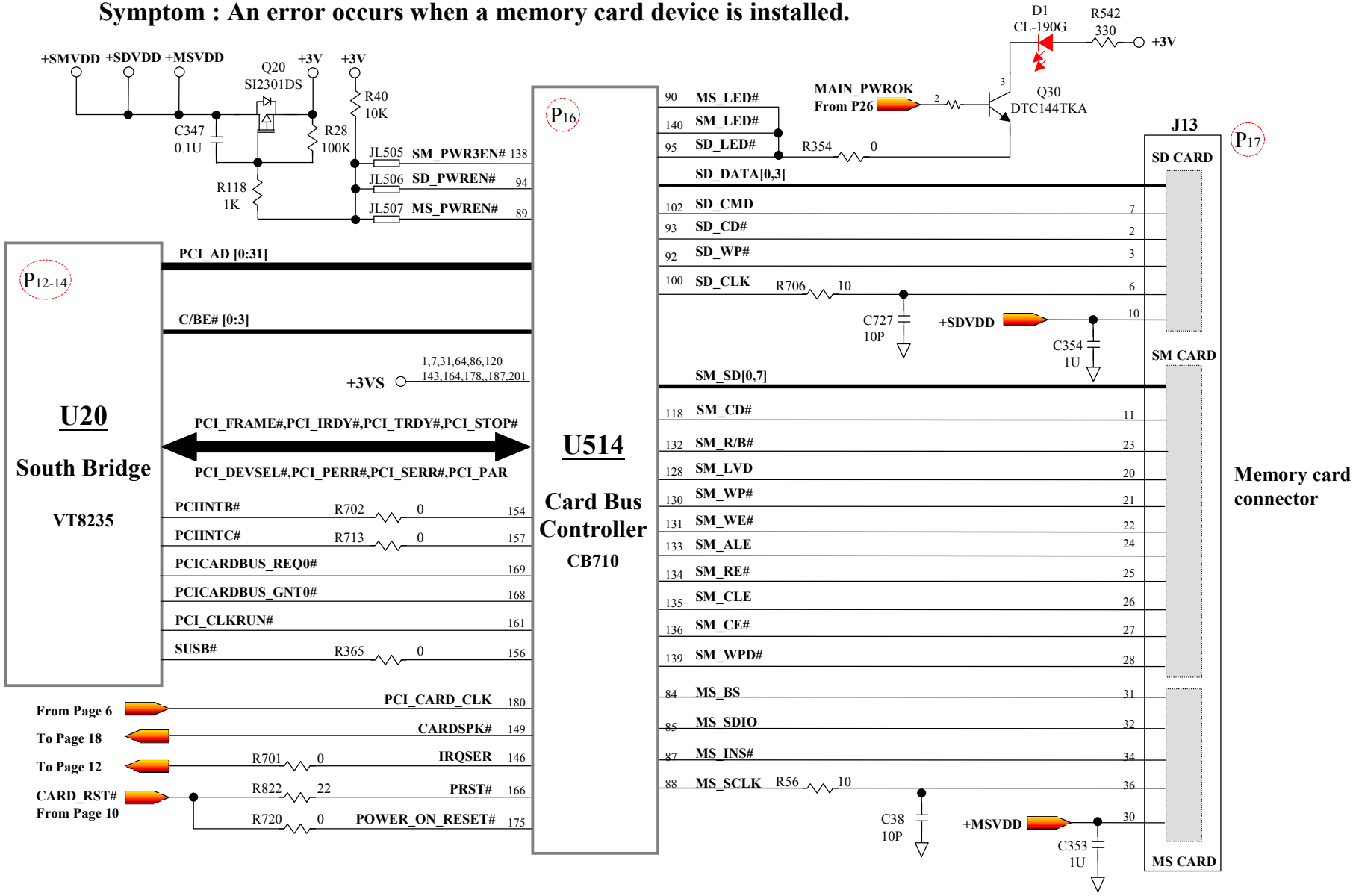


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals		
U20	PCI_AD[0:31]	CAD[0:31]	VCC5-EN#
U514	C/BE# [0:3]	CCBE# [0:3]	VCC3-EN#
U22	PCICARDBUS_REQ0#	CREQ#	VPPD0
J532	PCI_FRAME#	CFRAME#	VPPD1
R702	PCI_IRDY#	CIRDY#	+CARD-VCC
R713	PCI_TRDY#	CTRDY#	+VPPOUT
R365	PCI_DEVSEL#	CDEVSEL#	
R701	PCI_STOP#	CSTOP#	
R822	PCIINTB#	CGNT#	
R720	PCIRST#	CRST#	
R303	PCICARDBUS_GNT0#	CSERR#	
R295	PCI_SERR#	CPAR#	
R21	PCI_CLKRUN#	CPERR#	

8.12 Memory-Card Socket Failure

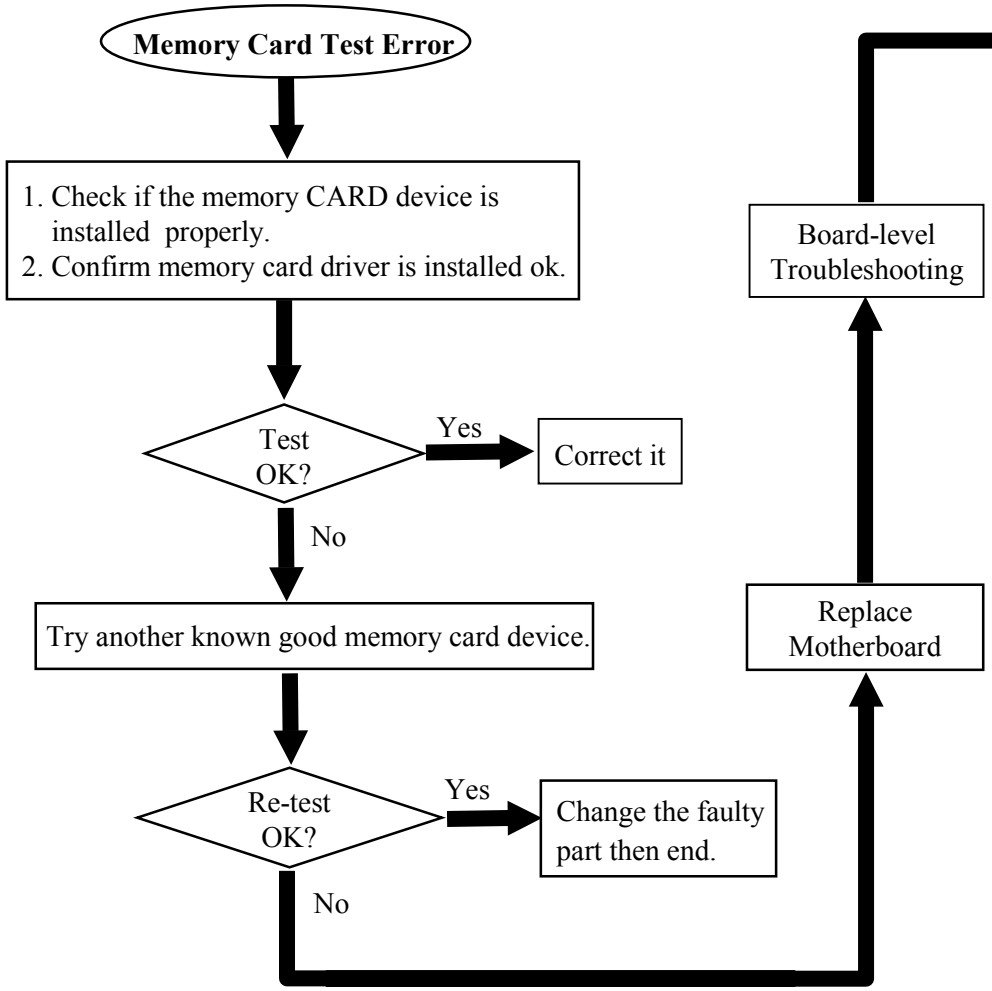
Symptom : An error occurs when a memory card device is installed.



Memory card connector

8.12 Memory-Card Socket Failure

Symptom : An error occurs when a memory card device is installed.

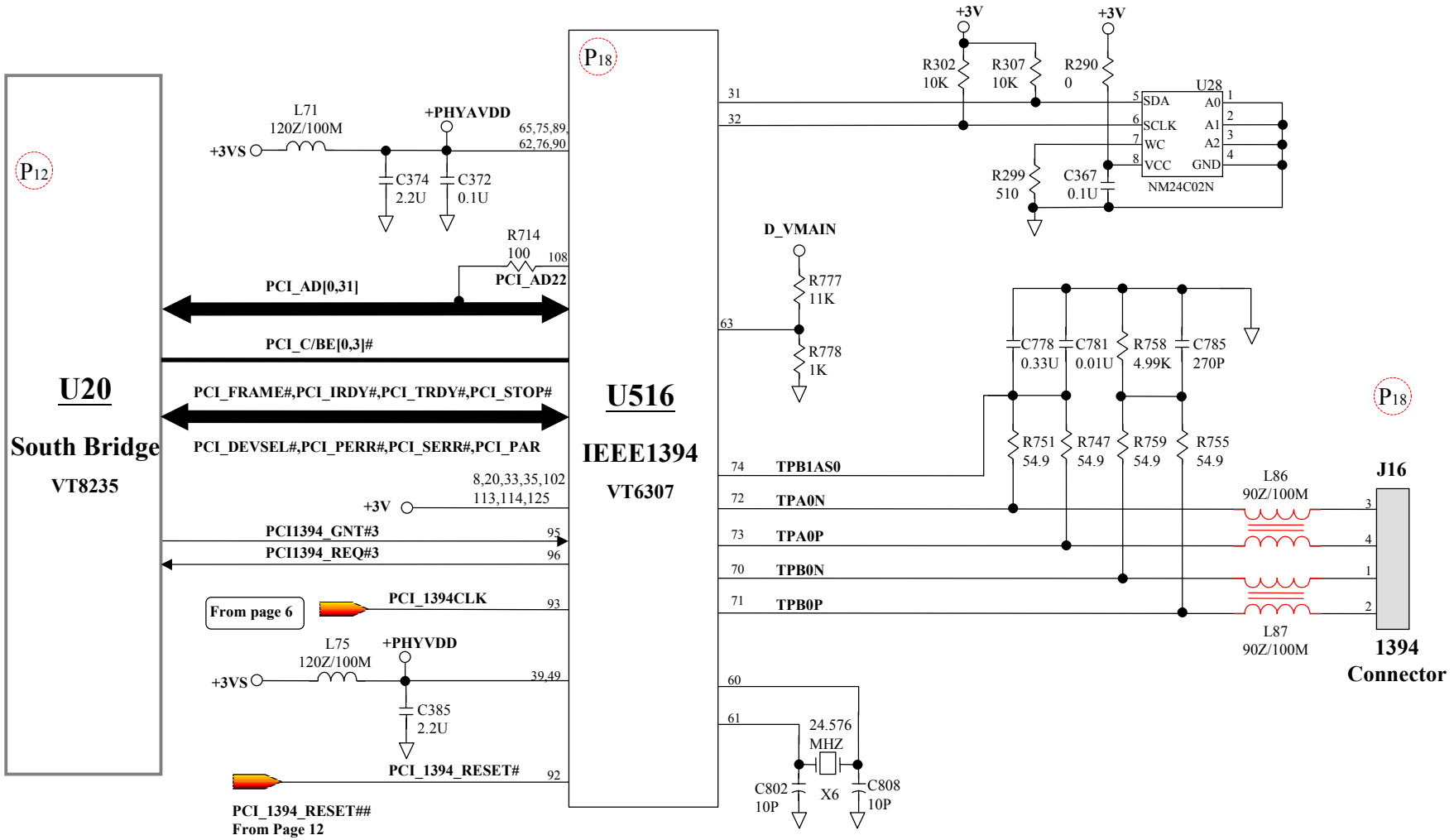


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals**		
U20	R701	PCI_AD[0:31]	SD_CD#	+MSVDD
U514	R822	C/BE# [0:3]	SD_ WP#	+SDVDD
J13	R720	PCICARDBUS_REQ0#	SM_CD#	
Q20	R706	PCI_FRAME#	SM_IVD	
C347	C727	PCI_IRDY#	SM_WP#	
R28	C354	PCI_TRDY#	SM_WE#	
R118	R56	PCI_DEVSEL#	SM_R/B#	
R40	C38	PCI_STOP#	SM_ALE	
JL505	C353	PCIINTB#	SM_RE#	
JL506		PCIRST#	SM_CLE	
JL507		PCICARDBUS_GNT0#	SM_CE#	
R702		PCI_SERR#	SM_WPD#	
R713		PCI_CLKRUN#	MS_BS	
R365			MS_SDIO	
			MS_INS#	
			MS_SCLK	

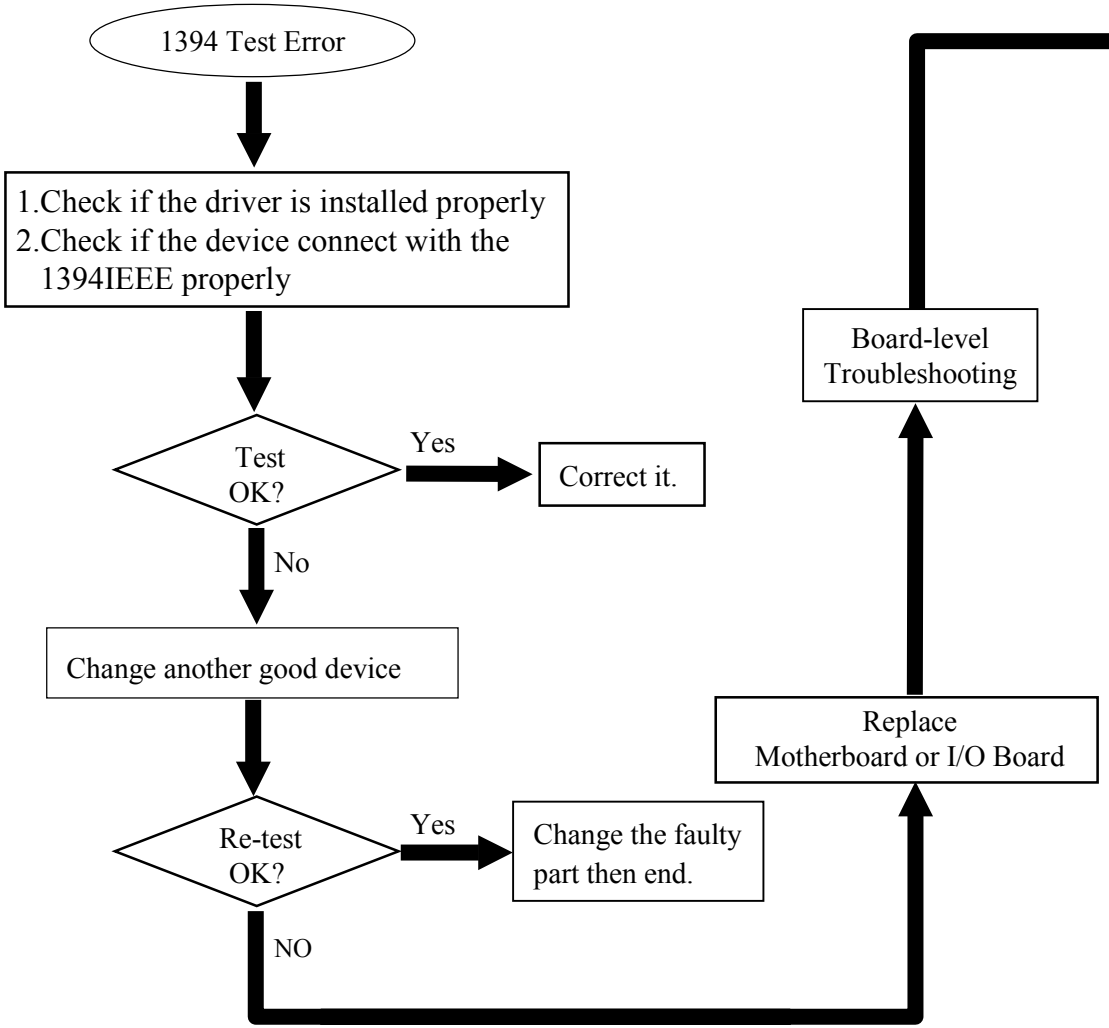
8.13 IEEE1394 Test Error

Symptom: An error occurs when IEEE1394 device is installed.



8.13 IEEE1394 Test Error

Symptom: An error occurs when IEEE1394 device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board and I/O board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

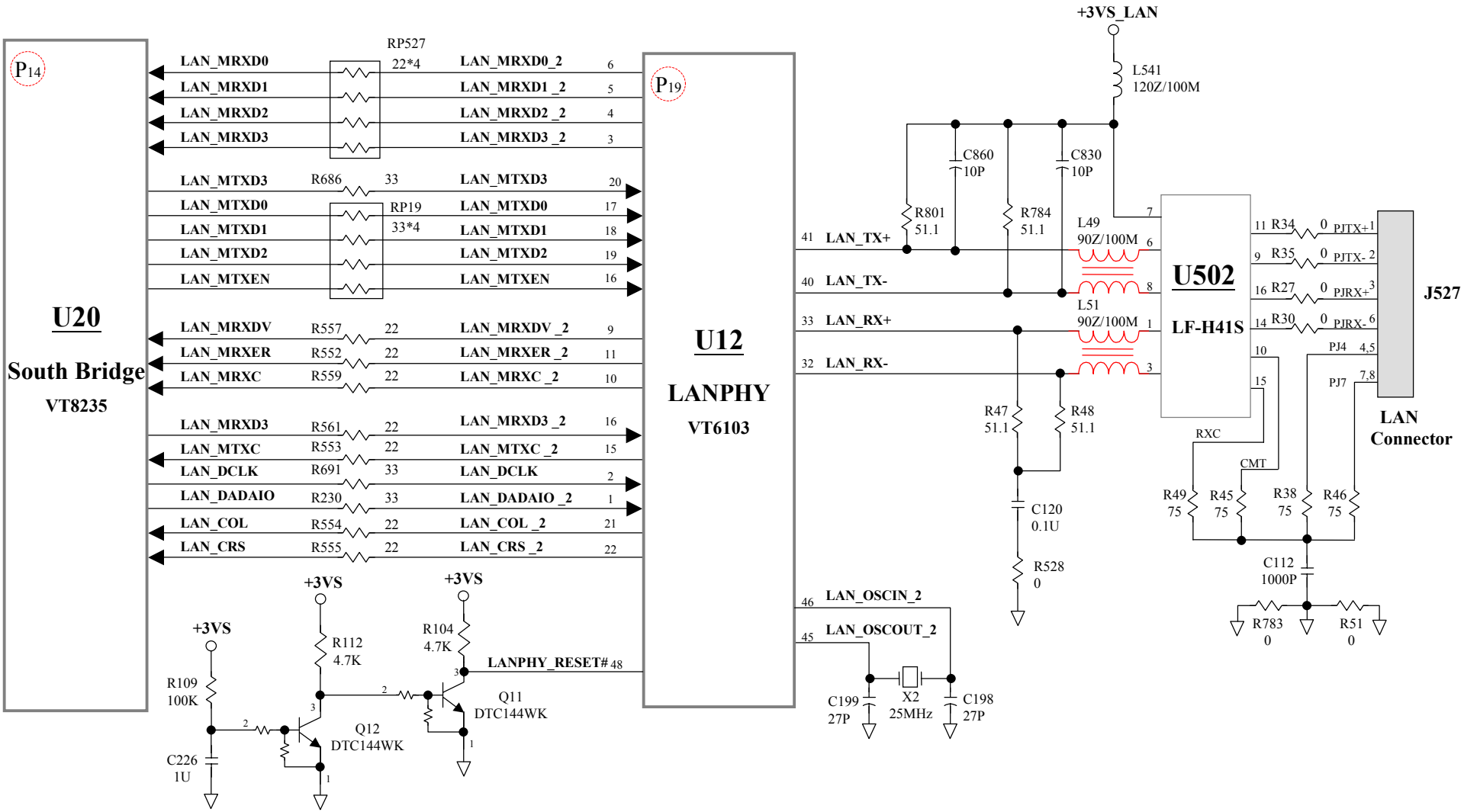
U20	L86
U516	L87
U28	R751
J16	R747
L71	R759
C374	R755
C372	C778
R714	C781
L75	R758
C385	C785
R302	
R307	
R290	
R299	
C367	
R777	
R778	

Signals

TPA0P	PCI_STOP#
TPA0N	PCI_PERR#
TPB0P	PCI_SERR#
TPB0N	PCI_PAR
TPB1AS0	+3V
PCI_AD[0,31]	D_VMAIN
PCI_C/BE#[0,3]	+PHYAVDD
GROM_SDA	+PHYVDD
GROM_SCL	
PCI_FRAME#	
PCI_DEVSEL#	
PCI_TRDY#	
PCI_IRDY#	
PCI1394_REQ#3	
PCI1394_GNT#3	
PCI_1394CLK	
PCI_1394_RESET#	

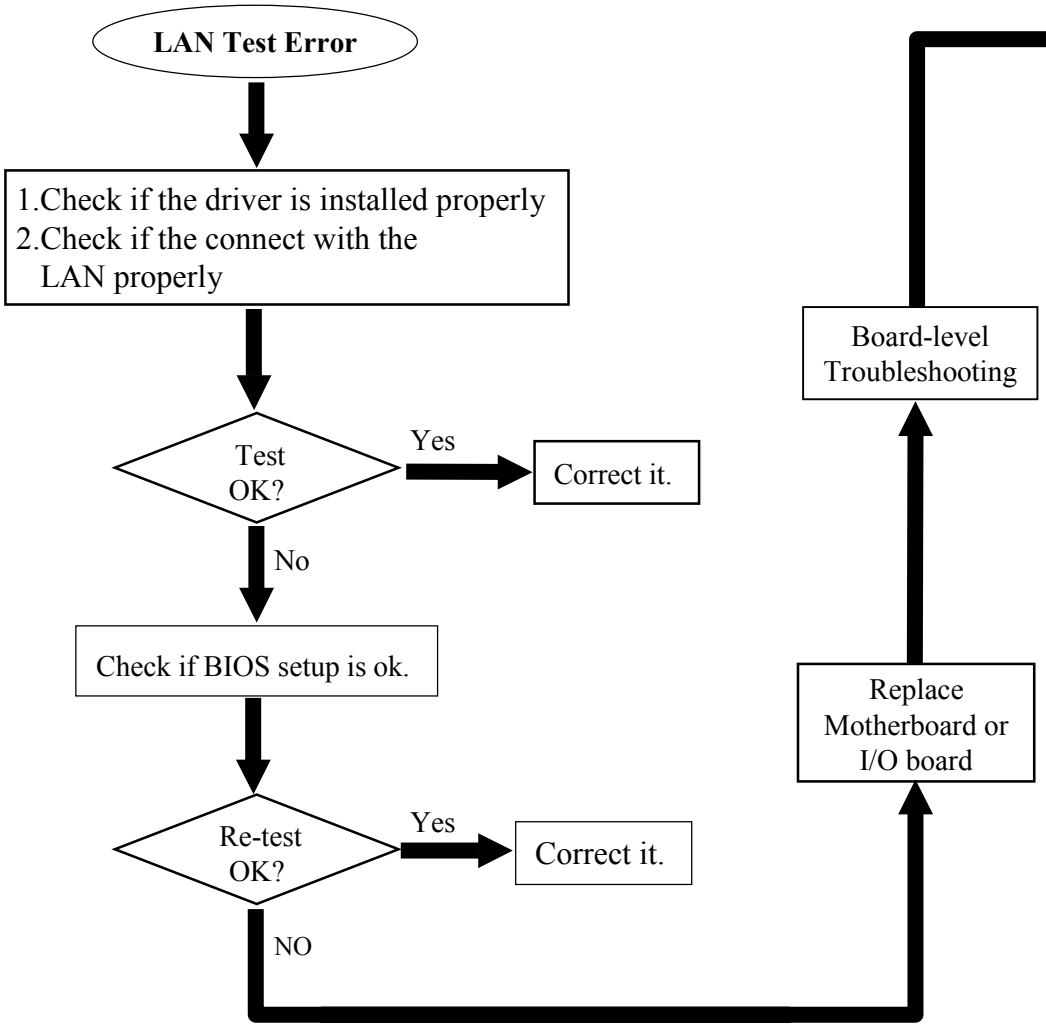
8.14 LAN Test Error

Symptom: An error occurs when LAN device is installed.



8.14 LAN Test Error

Symptom: An error occurs when LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

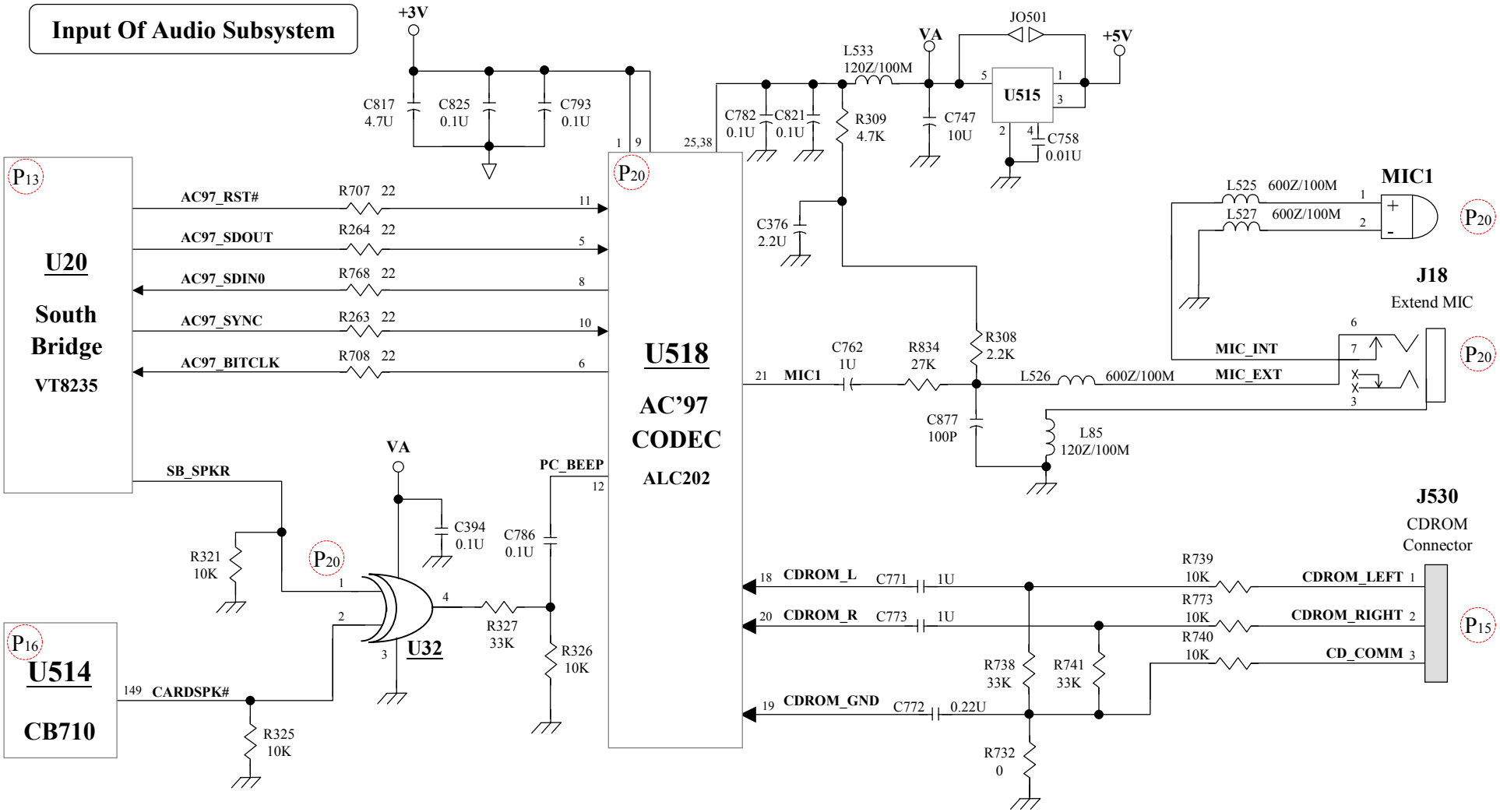
U20, U12, U502, J527, RP527, RP19, R686, R557, R552, R559, R561, R553, R691, R230, R554, R555, Q11, Q12, X2, L541, L49, L51, R34, R35, R27, R30, R49, R45, R38, R46, C112, R51, R783, C120

Signals

LAN_MRXD0, LAN_MRXD1, LAN_MRXD2, LAN_MRXD3, LAN_MRXDV, LAN_MRXER, LAN_MRXC, LAN_MTXD0, LAN_MTXD1, LAN_MTXD2, LAN_MTXD3, LAN_MTXE, LAN_MTXC, LAN_DCLK, LAN_TX+, LAN_TX-, LAN_RX+, LAN_RX-, PJTX+, PJTX-, PJRX+, PJRX-, PJ4, PJ7, LAN_COL, LAN_CRS, LAN_DATAIO, LANPHYI_RESET#

8.15 Audio Failure

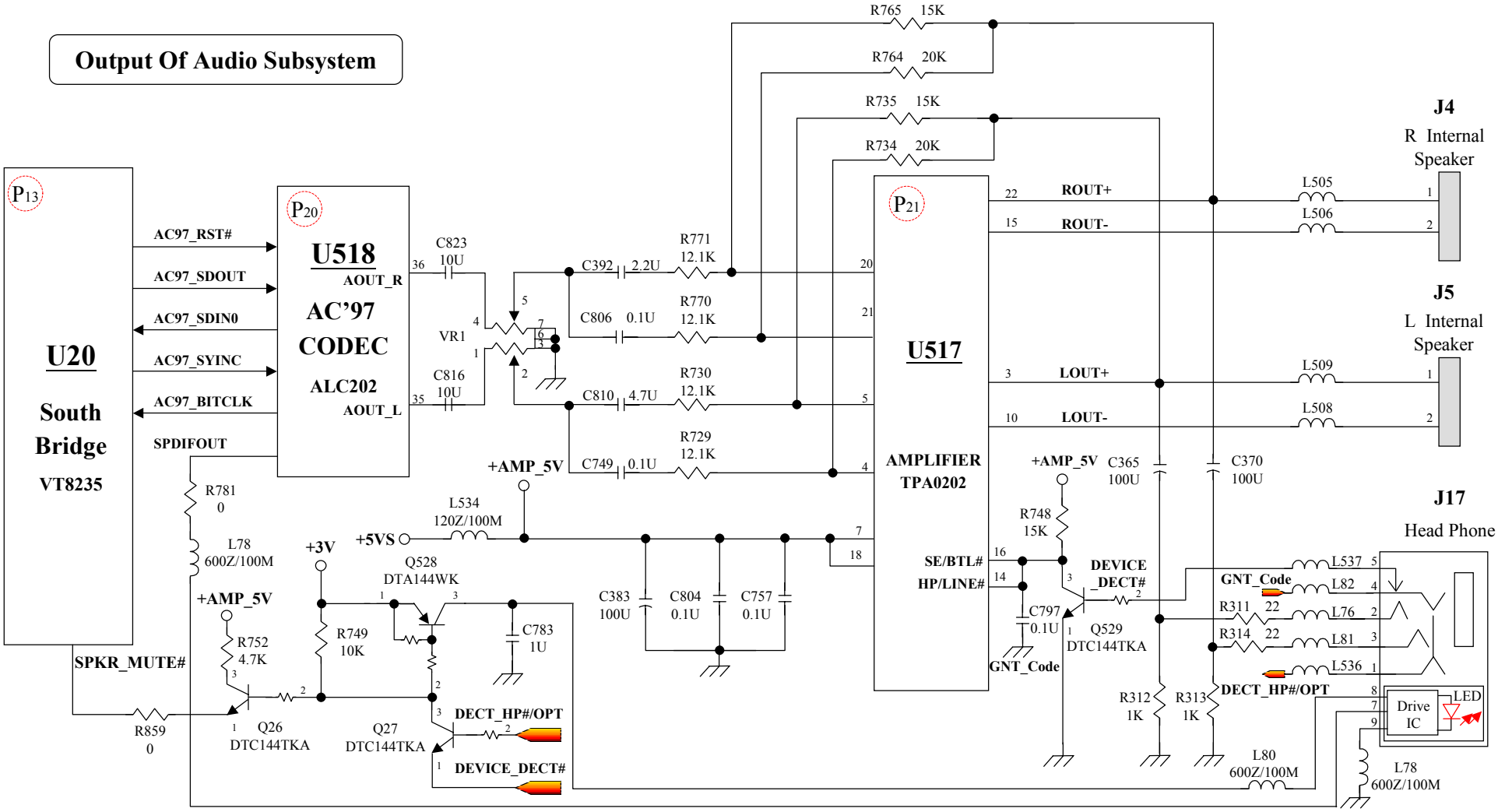
Symptom:
No sound from speaker after audio driver is installed.



8.15 Audio Failure

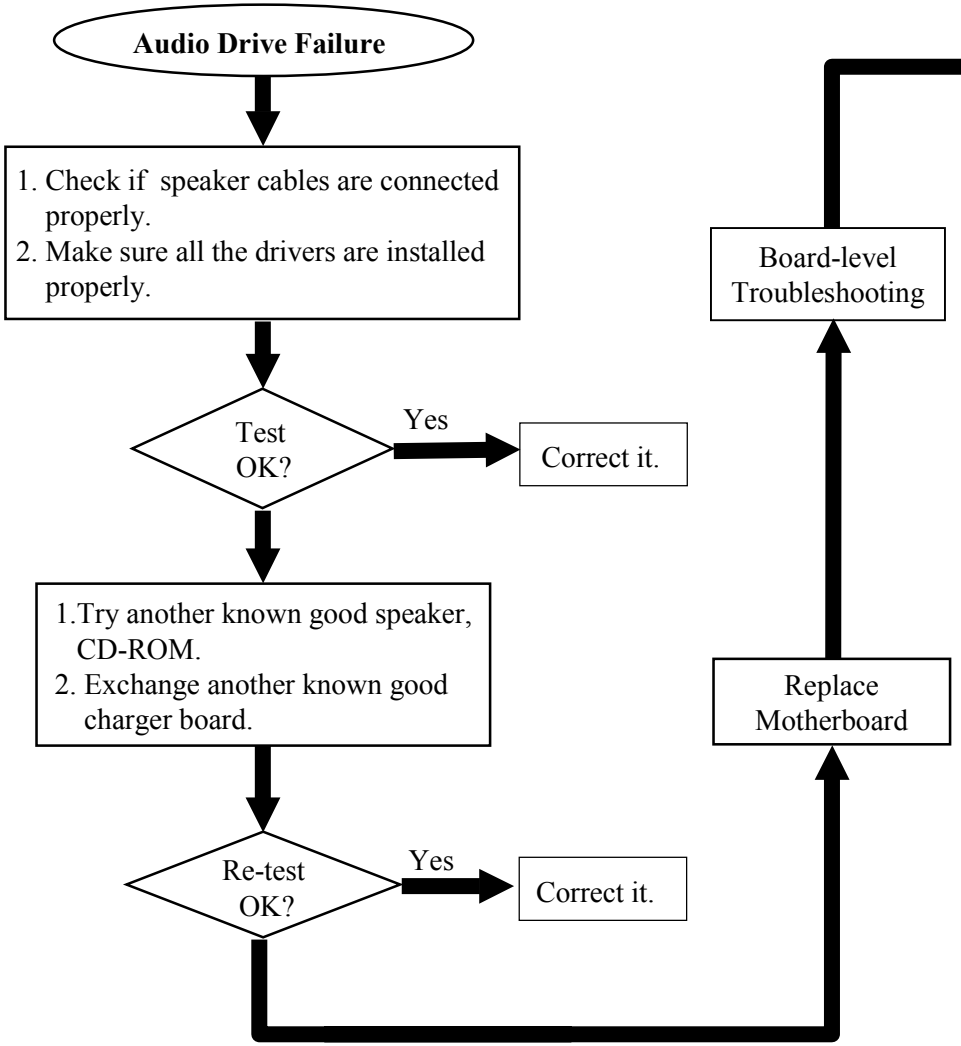
Symptom:

No sound from speaker after audio driver is installed.



8.15 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:		Signals:
U20	VR1	AOUT_R
U518	C392	AOUT_L
U517	C806	ROUT+
J4	R771	ROUT-
J5	R770	LOUT+
L505	C810	LOUT-
L506	C749	AC97_RST#
L508	R730	
L509	R729	
C83	R765	
C816	R764	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U518	MIC1
C762	MIC_INT
L526	MIC_EXT
L85	
L25	
L527	
J18	
MIC1	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U20	CDROM_L
U518	CDROM_R
C771	CDROM_GND
C773	CDROM_LEFT
C772	CDROM_RIGHT
R738	CD_COMM
R741	
R739	
R773	
R740	
J530	

9. Spare Part List-1

Part Number	Description	Location(S)
422675400021	AC ADPT ASSY;19V,7.9A,SPI,150W,S	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667540019	AK;19-UN,BOX,8355	
541667540031	AK;8355,UTILITY ONLY	
340675400034	AL PLATE ASSY;CHOCK,M/B,8355	
441999900085	BATT ASSY OPTION;LI-ION,MTC,8355	
442675400003	BATT ASSY;14.8V/6.6AH,LI,W/O GAU	
442675400005	BATT ASSY;14.8V/6.6AH,LI,W/O GAU	
441675400002	BATT ASSY;8355 SANYO,WO_GAUGE	
338536010052	BATTERY;LI,3.7V/2.2AH,18650,SANY	
242670800113	BFM-WORLD MARK;WINXP,7521N	
343675400001	BOSS;STANDOFF,MB,8355	MTG501,MTG502,MTG503
221677040001	BOX,AK,LYNX	
340675400011	BRACKET ASSY;TOUCH-PAD,8355	
342675400013	BRACKET;IO,8355	
342675400006	BRACKET;LCD 15",SPWG,L,8355	
342675400005	BRACKET;LCD 15",SPWG,R,8355	
342675400012	BRACKET;ROM,8355	
421673400005	CABLE ASSY;TV-OUT,8640S	
272075103501	CAP;.01U ,50V ,20%,0603,X7R,SMT	
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C750,C952,C956,C960,C964,C969
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C103,C145,C146,C171,C225,C228
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC112,PC114,PC506,PC533,PC54
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C7,C8

Part Number	Description	Location(S)
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C257
272072473402	CAP;.047U,16V ,10%,0603,X7R,SMT	C160,C867
272075473401	CAP;.047U,50V,10%,0603,X7R,SMT	C244,C991
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C313,C318,C320,C321,C323,C327
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C110,C111,C115,C117,C120,C125
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C10,C11,C12,C18,C21,C6,C8
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C277,C312,C941,C943,C947,C951
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C1,C4,C16,C13
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C297,C619,C683,C690,C789,PC54
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC106,PC107,PC43,PC505,PC52,
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C157,C219,C304,C407,C505,C588
272072224402	CAP;.22U ,16V ,10%,0603,X7R,SMT	C108,C118,C121,C139,C208,C209
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C166,C778
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C112
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C1,C130,C133,C140,C153,C256,C
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C3,C4
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C156,C203,C220,C230,C515,C54,1
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C2,C206,C24,C25,C27,C34,C35,C6
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C379,C615,C877,PC116,PC117
272075101302	CAP;100P ,CR,50V,5%,0603,NPO,SMT	C11
272010101301	CAP;100P,2KV,5%,1206,NPO,SMT,onl	
272010101302	CAP;100P,2KV,5%,1206,NPO,SMT,onl	C15
272431107507	CAP;100U,6.3V,TPC,7343,POSCAP,H=	
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C154,C155,C336,C38,C727,C729,(

9. Spare Part List-2

Part Number	Description	Location(S)
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC32,PC42,PC563
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C279,C303,C307,C308,C322,C324
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	PC102,PC48,PC50,PC528
272001106703	CAP;10U,10V,+80-20%,0805,Y5V,SMT	
272001106705	CAP;10U,10V,+80-20%,0805,Y5V,SMT	C654,C668,C680,C685,C686,C688
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC11,PC12,PC22,PC23,PC26,PC2
272023106002	CAP;10U,25V,M,1210,T2.8MM,X5R,SM	
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C102,C107,C169,C253,C254,C302
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C502,C506,PC91
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	
272431157509	CAP;150U,KOCAP,6.3V,20%,7343,SMT	C161,C172,C235,C282,C361,C371
272075180304	CAP;18P ,50V ,5% ,0603,NPO,SMT	C182,C212,C678,C679
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	C742,PC104
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C9
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C147,C162,C194,C224,C226,C231
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SM	C6
272012105702	CAP;1U ,CR,16V ,+80-20%,1206,Y	C298,PC542,PC61
272072105702	CAP;1U ,CR,16V,+80-20%,0603,Y5	C5,C9
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,Y	PC79
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	C239,C258,C309,C39,C659,C664,C
272001225401	CAP;2.2U ,CR,10V ,10%,0805,X7R,S	C5
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C343,C374,C376,C385,C392,C677
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C510,PC119

Part Number	Description	Location(S)
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C1,C2,C3,C4
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C10,C11,C12,C13,C14,C15,C16,C1
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC54,PC55,PC56,PC57
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	
272431227527	CAP;220U,4V,+/-20%,H2.8,PT,NCC	
272431227527	CAP;220U,4V,+/-20%,H2.8,PT,NCC	PC62
272431227526	CAP;220U,PC-CON,2V,+/-20%,10mOHM	PC13,PC16,PC17,PC18,PC25,PC2
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C163,C177,C184,C190,C192,C202
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C785
272075270302	CAP;27P ,50V ,5%,0603,COG,SMT	C198,C199
272073332401	CAP;3300P,CR,25V ,10%,0603,X7R,S	C175
272075331301	CAP;330P ,CR,50V,5% ,0603,NPO,SM	C12
272075330302	CAP;33P ,50V,5% ,0603,NPO,SMT	C30,C31,C32
272073392401	CAP;3900P,50V,10%,0603,X7R,SMT	C189,C191
272075390301	CAP;39P ,50V ,5% ,0603,NPO,SMT	C150
272011475401	CAP;4.7U ,10%,10V ,1206,X7R,SMT	C164,C314
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C104,C105,C134,C144,C159,C168
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C14
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	C880,PC523
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C337,C915,C919,C937
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C375,C798
272431476502	CAP;47U ,6.3V,20%,SP-CAP,7343,S	C2
272431476504	CAP;47U,6.3V,20%,AO-CAP,7343,SMT	
272431476503	CAP;47U,6.3V,20%,PC-CON,7343,SMT	
272075561701	CAP;560P ,CR,50V ,20%,0603,X7R,S	C7

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Part Number	Description	Location(S)
272075560301	CAP;56P ,50V,5%,0603,NPO,SMT	PC522
272030050301	CAP;5P,3KV,5%,1808,NPO,SMT,only	
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only	C17
272075060301	CAP;6.8P,50V,+-0.5PF ,0603,NPO,S	C100,C101,C106,C109,C113,C114
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C151
221675450007	CARD BOARD;W/AK BOX,FRAME,PALLET	
221675450008	CARD BOARD;W/AK BOX,T/B,PALLET,8	
221600020252	CARTON;BATTERY,CAIMAN,PWR	
221675420004	CARTON;W/AK BOX,N-B,8355	
431675400001	CASE KIT;8355 ID1	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
313000020360	CHOKE COIL;1.25uH,+30-0%,4.5Ts,D	PL503,PL504,PL505
273000500092	CHOKE COIL;2.2UH ,20%,16A,3.5MM	PL5,PL509
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5	L507
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L25,L28,L38,L44,L49,L51,L86,L8
273000150314	CHOKE COIL;90OHM/100MHZ,20%,2012	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
523467540907	COMBO ASSY OPTION;8355	
523467540007	COMBO ASSY;KME,UJDA750,8355	
523467540011	COMBO ASSY;Liteon,LSC-24082K,835	
523467540006	COMBO ASSY;QSI,SBW-242,8355	
523467540008	COMBO ASSY;TEAC,DW-224E-93,8355	
340672300026	COMBO BEZEL ASSY;QSI,SBW-081,MAN	
331000008038	CON;BAT,8P,2.5MM,SUYIN	PJ502
331000004036	CON;BATTERY,0402A120,4P,R/A,8500	PJ501

Part Number	Description	Location(S)
331000007015	CON;BATTERY,FM,7P,R/A,8175,PRC	
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J503
331720025005	CON;D,FM,25P,2.775,R/A	J502
291000025027	CON;FM,0.8MM,25P*2,R/A,SMT,Allt	J530
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J10,J525
291000152604	CON;FPC/FFC,26P,1MM,R/A,ELCO,SMT	J8
291000144004	CON;HDR,20P*2,1.0MM,H=4.6,ST,SMT	J2
291000141002	CON;HDR,5P*2,1.0MM,H=4.6,ST,SMT,	J501
291000141002	CON;HDR,5P*2,1.0MM,H=4.6,ST,SMT,	J15
291000023002	CON;HDR,FM,15P*2,0.8MM.H4.4,R/A,	J11
291000014409	CON;HDR,FM,22P*2,2.0MM,SMT,SPEED	J529
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-	J1
291000021101	CON;HDR,MA,11P*1,1.25,R/A,DF13-1	
291000021103	CON;HDR,MA,11P,1.25MM,R/A,SMT,DF	
291000011201	CON;HDR,MA,12P*1,1.25MM,ST,SMT	J3
291000010201	CON;HDR,MA,2P*1,1.25MM,ST,SMT	J14,J19,J4,J5
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000010301	CON;HDR,MA,3P*1,1.25MM,ST,SMT	J1,J528
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J16
291000253701	CON;MEMORY CARD,37P,SD,SM,SSFDC,	J13
331000007018	CON;MINI DIN,7P,R/A,W/GROUND,ALL	J501
291000616801	CON;PCMCIA CARD,68P,TAI-SOL,WEAS	J532
291000811007	CON;PHONE JACK,10P,R/A,RJ45,RJ11	J527
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J17

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Part Number	Description	Location(S)
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J18
331000004029	CON;USB,MA,R/A,4P*1,2551A-04G5T-	J521,J522,J523,J524
346675400029	CONDUCTIVE TAPE;DC IN,MB,8355	
346675400028	CONDUCTIVE TAPE;KB,8355	
345678300011	CONDUCTIVE TAPE;T/P BRAKCET,UP,8	
225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR,RIG	
225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR,RIG	
345678300012	CONDUCTIVE TAPE;TP BRAKCET,LEFT,	
345678300013	CONDUCTIVE TAPE;TP BRAKCET,RIGHT	
345678300013	CONDUCTIVE TAPE;TP BRAKCET,RIGHT	
342668200003	CONTACT PLATE;2,W4L20T0.15	
342504300005	CONTACT PLATE;W5L102T0.13,8500	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400006	CONTACT PLATE;W5L45T0.13,7170LI,	
340675400014	COVER ASSY;CPU,8355	
340675400007	COVER ASSY;LCD 15",8355	
340675400010	COVER ASSY;SPEAKER,K/B,8355	
340675400008	COVER ASSY;TOP,8355	
344675400021	COVER;BATTERY,8355	
344675400024	COVER;HDD,8355	
344675400016	COVER;HINGE,8355	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2,CP502
291000612005	DIMM SOCKET;DDR 200P,0.6MM,H4,SM	
291000612014	DIMM SOCKET;DDR REVERSE,200P,0.6	J7
291000612013	DIMM SOCKET;DDR STANDARD,200P,0.	J6

Part Number	Description	Location(S)
291000612004	DIMM SOCKET;DDR,200P,0.6MM,H4,SM	
288100340008	DIODE;B340LA,40V,3A,SMA,DIODES,S	
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD12,PD16,PD22,PD23,PD505,P
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT2	D28
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D23,PD3,PD5
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D3,D5,D6
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D27
288105224002	DIODE;BZT52C2V4,ZENER,2.2-2.6V,0	
288105233002	DIODE;BZT52C3V3,ZENER,3.1-3.5V,0	
288105243001	DIODE;BZT52C4V3,ZENER,4.0-4.6V,0	
288105524002	DIODE;BZV55-C2V4,ZENER,5%,SOD-80	PD502,PD504,PD8
288105533001	DIODE;BZV55-C3V3,ZENER,5%,SOD-80	PD503
288105543001	DIODE;BZV55-C4V3,ZENER,5%,SOD-80	PD20
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD13,PD15,PD18,PD19,PD2,PD5
288100050001	DIODE;RB050L-40,40V,3A,SMT	
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D14,D2,D25,D4,D503,D511,D7
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD14
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD4
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D24,PD21
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD1
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D22
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D3,D4,ZD3
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	ZD1,ZD2

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Part Number	Description	Location(S)
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	
523408610080	DVD COMBO DRIVE;8X24X10X24X,SBW-	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C365,C370,C383
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC554
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃	PC558,PC559
312272263511	EC;22U,25V,20%,RA,8*10.5,105℃,O	PC508,PC509,PC515,PC516
312276206161	EC;620U,6.3V,+50% -10%,RA,10*10.	PC561
312278206151	EC;820U ,4V,+-20%,100*10.5,SP.OS	PC560
312278206151	EC;820U ,4V,+-20%,100*10.5,SP.OS	
312278206155	EC;820U,4V,+-20%,D10X12.5,4PS820	PC510,PC519,PC524,PC527
227675400004	END CAP;W/AK BOX,8355	
227675400003	EPE PAD;K/B,8355	
481675400002	F/W ASSY;KBD CTRL,8355	U511
481675400001	F/W ASSY;SYS/VGA BIOS,8355	U23
340675400029	FAN ASSY;IO,8355	
340678300018	FAN ASSY;IO,YS,8555	
273000610013	FERRITE ARRAY;120OHM100MHZ,3216,	FA501
273000150307	FERRITE BEAD;120 OHM/100MHZ,3A,0	L1,L24,L27,L3,L4,L501,L503,L5(
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L26,L41,L46,L47,L520,L535,L54
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L15,L16,L1
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L505,L506,L508,L509,L525,L526
422675400001	FFC ASSY;TOUCH-PAD,8355	
288001001001	FIR,GP2W1001YP,GDE VIEW,10P,SMT,	U33
245600010016	FLOW CARD;SPS,GRAY	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F502

Part Number	Description	Location(S)
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F504
295000010111	FUSE;1.5A,NORMAL,1206,SMT	PF2
295000010105	FUSE;1A,NORMAL,1206,SMT	PF3
295000010057	FUSE;228R,139C',5A/250V,SMT,PRC	
295000010106	FUSE;2A,NORMAL,1206,SMT	
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF1,PF502
295000010029	FUSE;FAST,.75A,63V,1206,THIN FIL	F503
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433	
295000010134	FUSE;FAST,2A,63VDC,1206,SMT,PRC	F1
295000100006	FUSE;FAST,2A/63V,R433002,1206,SM	F501
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
295000010077	FUSE;NANO,10A/32V,R451,SMT	
295000010009	FUSE;NORMAL,5A/32VDC,3216,SMT	PF4,PF501
345675400040	GASKET;1394,SLD,MB,8355	
345678300001	GASKET;CARDREADER,MB,8555	
345675400035	GASKET;DOWN,TOP SHIELDING,8355	
345675400030	GASKET;KB,8355	
345675400011	GASKET;M/B ASSY,1394,8355	
345675400012	GASKET;M/B ASSY,MIC-IN,8355	
345675400039	GASKET;MIC,SLD,MB,8355	
345675400038	GASKET;PCMCIA,8355	
345675400037	GASKET;ROM,MB,BIG,8355	
345675400036	GASKET;ROM,MB,SMALL,8355	
345678300005	GASKET;S-TERMINAL ,MB,8555	
345678300010	GASKET;TUNER,MB,8555	

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Part Number	Description	Location(S)
451675400111	HDD ME KIT;8355	
340675400025	HEATSINK ASSY;CPU,AMD K8 DTM,MPT	
340675400024	HEATSINK ASSY;CPU,AMD K8 DTM,UNP	
343675400003	HEATSINK;NORTH BRIDGE,MPT,8355	
340675400006	HINGE;L,15",8355	
340675400005	HINGE;R,15",8355	
344674300038	HOLDER;PCMCIA,TAI-SOL,P2P2601-22	J532
340675400015	HOUSING ASSY;HOUSING,8355	
340675400003	HOUSING ASSY;LCD 15",8355	
451675400051	HOUSING KIT;8355 ID1	
344675400022	HOUSING;BATTERY,8355	
291000617542	IC SOCKET;AMD K8 BGA-PGA754-SKT,	
291000617544	IC SOCKET;AMD K8 BGA-PGA754-SKT,	U503
286304377001	IC; MAX4377F,I-SENSEAMP ,MSOP8,S	PU504
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U10
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U510
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U512
282674008001	IC;74AHCT08,2I/P AND GATE,TSSOP,	U11
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U32
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U19
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U24
286308800001	IC;AME8800,0.3A,1.5%,LDO,SOT89	U4
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	U519
286308800016	IC;AME8800DEET,300mA,LDO REGULAT	U8
286308801011	IC;AME8801DEEV,VOL REG.,SOT25,5P	U7

Part Number	Description	Location(S)
284508807001	IC;AME8807AEHA,600mA,CMOS LDO,AM	U15
286308824002	IC;AME8824,0.3A,LDO REG.,SOT26	PU503,PU8
286302020001	IC;APA2020ARI,AUDIO AMP,2W,TSSOP	U517
284500010003	IC;ATI MOBILITY M10-P,AGP,BGA 70	U16
286300710001	IC;CB710,PCI/CARDBUS,LQFP,208P,S	U514
284509738002	IC;CMI9738-S,AC97 CODEC,LQFP,48P	U518
286302211002	IC;CP2211,POWER DISTRI SW,SSOP16	U22
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U21
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U28
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U5
283767540002	IC;EM6A9320BI-3.6M,DDR SDRAM,4MX	
283410310001	IC;FLASH,256K*8,PLCC32, W49F002	
283480404001	IC;FLASH,256K*8-70,PLCC32,A29002	
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF	
286369438001	IC;G692L438T,RESET CIRCUIT,4.38V	
286300690001	IC;GMT690B,RESET CIRCUIT,2.93V,S	
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
283767630002	IC;HY8250128323,DDR SDRAM,4MX32,	
284595040301	IC;ICS950403,TIMING CTL HUB FOR	U9
286300811002	IC;IMP811,RESET CIRCUIT,4.38,SOT	U507
286306207001	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PU505,PU507,PU508
286306559002	IC;ISL6559,MULTI-PHASE PWM CTL,S	PU502
283767540001	IC;K4D263238E,DDR SDRAM,4MX32,BG	U18,U29,U30,U523

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Part Number	Description	Location(S)
284500086001	IC;LM86,TEMPERATURE MTR,SO8	U5
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU10
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U508
286303728001	IC;LTC3728L,PWM CTRL,LTC,5X5QFN,	
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU19
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU501
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U513
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	U1
281300708001	IC;NC7SZ08,SINGLE AND GATE,SOT23	U13
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
284587393002	IC;PC87393F,TQFP,100P	U509
286309167001	IC;RT9167-47CB,200MA LDO REGULAT	U515
286309202001	IC;RT9202CS,PWM CONTROLLER,SOP-8	PU506
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U3,U501
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	U2
286301486001	IC;SC1486,PWM CTRL,SC,TSSOP-28	PU7
286300431011	IC;SC431CSK-.5,.5%,ADJ REG,SOT23	PQ15
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU11
284508800001	IC;VIA K8T800,N.B.,BGA578,SMT	U506
284506103002	IC;VT6103,LAN-PHY,SSOP,48P,SMT	U12
284506307001	IC;VT6307L,PCI-1394,2PORT,LQFP,1	U516
284508235006	IC;VT8235,SOUTH BRIDGE,BGA,487P,	U20
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL508
273000990129	INDUCTOR;4.7UH,20%,D124C,H4.5,TO	PL510
273000990123	INDUCTOR;4.7UH,20%,D128C,H7.8,TO	PL511

Part Number	Description	Location(S)
273000990163	INDUCTOR;6.2UH,20%,A916CY-6R2M,S	PL6
345675400025	INSULATOR;1394,SLD,MB,8355	
346675400016	INSULATOR;AL-FOIL ,M/B,8355	
346678300026	INSULATOR;ASSY,6CELL,SINGLE FACE	
346503100301	INSULATOR;BATT ASSY,6CELLS,7521C	
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,	
346503400502	INSULATOR;BATT ASSY,L22R9.2,8175	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346503200101	INSULATOR;BATT ASSY,POLY,W30L64,	
346674500002	INSULATOR;BATT ASSY,W7L11 (FOR G	
346674500001	INSULATOR;BATTERY ASSY (FOR GP3)	
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346673100023	INSULATOR;FOR 4 CELLS ,8060	
346673800021	INSULATOR;FOR 4 CELLS,DOUBLE FA	
346669900004	INSULATOR;INVERTER,7170	
346675400023	INSULATOR;M/B,MDC,8355	
346675400017	INSULATOR;MINI PCI,8355	
346675400018	INSULATOR;ROM ,8355	
531067540913	KBD OPTION;DM,8355	
531017240124	KBD;88,DA,3000170024,ZIPPY,8355	
531020237629	KBD;88,DM,K011718B1,8355	
451675400002	LABEL KIT;N-B,8355	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242662300009	LABEL;25*10MM,3020F	

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Part Number	Description	Location(S)
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242675400001	LABEL;AGENCY-GLOBAL,8355	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242669600005	LABEL;LOT NUMBER,RACE	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441675400036	LCD ASSY;15",SXAG+,AU,8355 ID1	
451675400036	LCD ME KIT;15",SXAG+,AU,8355 ID1	
413000021005	LCD;AU-B150PG01,TFT,15",SXGA+	
294011200155	LED;BLUE,H0.8,SF0603-B70140-30,S	D8
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED1,LED2,LED3,LED4
294011200034	LED;GREEN,H.8,0603,19-21VGC/TR,S	
294011200160	LED;GREEN,H=0.8,0603,SF0603-G651	D1

Part Number	Description	Location(S)
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D1,D10,D3,D5,D7
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED5,LED6
416267540903	LT PF OPTION;15",SXGA+,8355 ID1	
416267540010	LT PF;15",SXAG+,AU,8355 ID1	
526267540015	LTXNX;8355/S5XX/XXM/3DM1/L3D3A/X	
561567540025	MANUAL;QSG,EN,8355	
339115000051	MICROPHONE;-56+-3dB,2KOHM,3V,FCE	MIC1
291000611245	MINIPCI SOCKET;124P,0.8MM,H=4,S	
291000611247	MINIPCI SOCKET;124P,0.8MM,H=4.0,	J9
344675400015	NAME-PLATE;SPEAKER COVER,8355	
451675400072	ODD ME KIT;8355	
461675400002	PACKING KIT;8355, SANYO,WO_GAUGE	
461675400006	PACKING KIT;N-B,8355	
224673130001	PALLET;COMPLEX,1300x1100x126,806	
221600050218	PARTITION;BATTERY,MARLIN,CAIMAN,	
221675350014	PARTITION;HDD ME KIT,8080	
221600050219	PARTITION;TOP/BTM,BATTERY,MARLIN	
221675450009	PARTITION;W/AK BOX,PALLET,8355	
412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I,	
316675400003	PCB;PWA-8355/BATT PROTECTION BD	
316675400002	PCB;PWA-8355/LED TRANS BD	R00
316675400001	PCB;PWA-8355/MOTHER BD	R01
316600000041	PCB;PWA-INVERTER BD (DA1-05A01-A	R0A
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	

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Part Number	Description	Location(S)
222668820003	PE BUBBLE BAG;160X270MM,ANTI-STA	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
230000000003	PEN;OIL,BLUE,PRC	
411675400008	PWA,PWA-8355 BOARD, SANYO,WO_GAU	
411675400009	PWA; PWA-8355BATT PROTECTION,WO_	
411675400004	PWA;PWA-8355,LED BD	
411675400001	PWA;PWA-8355,MOTHER BD	
411675400003	PWA;PWA-8355,MOTHER BD,SMT	
411675400002	PWA;PWA-8355,MOTHER BD,T/U	
411672900001	PWA;PWA-INVERTER BD DA1-05A01	
332810000199	PWR CORD;250V/10~16A,3P,BLK,EU	
297212000003	RELAY;REED,200V,.5A,NORMAL OPEN,	SW1
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR554
271046057102	RES;.005,1.5W,1%,2512,SMT	
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR553,PR7
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR29,PR30
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L65,L88,PR567,R192,R285,R304,
271061000002	RES;0 ,1/16W,0402,SMT	R163,R164,R170,R183,R215,R216
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R2
271071000002	RES;0 ,1/16W,5% ,0603,SMT	C28,PR11,PR13,PR14,PR18,PR28
271072102111	RES;1.02K,1/10W,1% ,0603,SMT	R665
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R25,R26
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R556
271002100301	RES;10 ,1/10W,5% ,0805,SMT	PR549,PR550,PR569,R367
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR501,PR519,PR520,PR535,PR53

Part Number	Description	Location(S)
271071101101	RES;100 ,1/16W,1% ,0603,SMT	PR19,R525,R53,R57,R612,R777
271071101301	RES;100 ,1/16W,5% ,0603,SMT	PR25,R106,R58,R636,R714
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R3,R41,R42
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R16,R13
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR533
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R220,R811
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR1,PR16,PR26,PR27,PR31,PR42
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R10,R4
271071105311	RES;105K ,1/16W,1% ,0603,SMT	PR59
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR504
271071103701	RES;10K ,1/16W,.1%,0603,SMT	PR36
271071103101	RES;10K ,1/16W,1% ,0603,SMT	R8,R18,R19
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR17,PR23,PR38,PR526,PR529,P
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R100,R122,R128,R130,R168,R171
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR505,R138,R152,R173,R185,R18
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R43,R44
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR563,R729,R730,R770,R771
271071121301	RES;120 ,1/16W,5% ,0603,SMT	R22,R23,R346,R347,R54,R59
271071124101	RES;120K ,1/16W,1% ,0603,SMT	R4
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR39
271071150301	RES;15 ,1/16W,5% ,0603,SMT	R9
271071151103	RES;15 ,1/16W,1% ,0603,SMT	R86,R88
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R1
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR48
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R356,R357,R358,R359,R360,R361

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Part Number	Description	Location(S)
271071169011	RES;169 ,1/16W,1% ,0603,SMT	R531
271071174311	RES;174K ,1/16W,1% ,0603,SMT	PR44
271061102105	RES;1K ,1/16W,1% ,0402,SMT	R154,R156,R198,R199,R214,R217
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R14
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR511,PR56,R135,R137,R194,R19
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R2
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R118,R187,R292,R312,R313,R338
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11,R14,R5,R9
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR2,PR45,R116,R139,R503,R642,
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R12
271071221111	RES;2.21K,1/16W,1% ,0603,SMT	R563,R712
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R200,R308
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R1,R2
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	R390
271071274111	RES;2.74K,1/16W,1% ,0603,SMT	PR508,PR509,PR510
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R207,R223,R225,R226,R527,R662
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R30,R17
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR525,PR547,PR57,PR60
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R127,R148,R210,R572,R734,R764
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R208
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R142,R165,R218,R263,R264,R288
271071221211	RES;22.1K,1/16W,1% ,0603,SMT	PR40
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R115,R933
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR4
271071232271	RES;23.2K,1/16W,.1%,0603,SMT	PR33,PR551

Part Number	Description	Location(S)
271061240302	RES;24,1/16W,5%,0402,SMT	R201,R203,R205,R206,R212,R213
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR557
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R762
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R11
271071348111	RES;3.48K,1/16W,1% ,0603,SMT	PR506
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR534
271071303101	RES;30K ,1/16W,1% ,0603,SMT	R3
271071324011	RES;324 ,1/16W,1% ,0603,SMT	R779
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R230,R602,R603,R675,R681,R686
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R542,R652,R670
271071332311	RES;332K ,1/16W,1% ,0603,SMT	PR62,PR63
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR10,PR543,R327,R738,R741
271071348812	RES;34.8 ,1/16W,1%,0603,SMT	R24,R521
271071361101	RES;360 ,1/16W,1% ,0603,SMT	R599,R648,R661,R678
271002383011	RES;383 ,1/10W,1% ,0805,SMT	R666,R674
271071394101	RES;390K ,1/16W,1% ,0603,SMT	R8
271071302101	RES;3K ,1/16W,1% ,0603,SMT	R147,R658
271071402111	RES;4.02K,1/16W,1% ,0603,SMT	PR52,PR53
271001435301	RES;4.3M,1/10W,5%,0805,SMT	R10
271071478301	RES;4.7 ,1/16W,5% ,0603,SMT	PR49
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	R324,R329
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR5,PR6
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R161,R162
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR35,PR37,PR41,R104,R112,R11
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR507,PR542,PR546,R758

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Part Number	Description	Location(S)
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R794
271071433301	RES;43K ,1/16W,5% ,0603,SMT	R246,R247,R249,R250,R252,R254
271071442812	RES;44.2,1/16W,1% ,0603,SMT	R52,R55
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R134,R373,R374,R375,R376
271071471101	RES;470 ,1/16W,1% ,0603,SMT	R21,R23,R27
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R3,R4,R5,R6,R7
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR503,R158,R294,R787,R835
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R40,R6
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R7
271061474501	RES;470K ,1/16W,5% ,0402,SMT	R13,R211,R687
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR22,PR3,PR523,PR571,PR572,P
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR545
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R107,R108,R37,R41
271071499011	RES;499 ,1/16W,1% ,0603,SMT	R123
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	R663
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R167,R753
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R45
271071511812	RES;51.1,1/16W,1% 0603,SMT	R47,R48,R784,R801
271071511301	RES;510 ,1/16W,5% ,0603,SMT	R299
271071536211	RES;53.6K,1/16W,1% ,0603,SMT	R5
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R747,R751,R755,R759
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R180,R181,R871,R872,R877,R878
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R22,R24,R28
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R11,R12,R509,R544
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR51

Part Number	Description	Location(S)
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R310
271071649111	RES;6.49K,1/16W,1% ,0603,SMT	R549
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R562,R567
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR58
271071680301	RES;68 ,1/16W,5% ,0603,SMT	R545,R546
271071681101	RES;680 ,1/16W,1% ,0603,SMT	R18,R19,R515,R516,R517,R518,R
271071713102	RES;715 ,1/16W,1% ,0603,SMT	R124
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R1,R38,R45,R46,R49,R5,R6
271071751101	RES;750 ,1/16W,1% ,0603,SMT	R15
271071750311	RES;750K,1/16W,1% ,0603,SMT	PR20,PR521
271071787311	RES;787K ,1/16W,1% ,0603,SMT	PR32,PR43
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R101,R153,R157,R169,R174,R196
271071866111	RES;8.66K,1/16W,1% ,0603,SMT	PR21
271071806812	RES;80.6 ,1/16W,1% ,0603,SMT	R67
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR524
271071825211	RES;82.5K,1/16W,1% ,0603,SMT	R12,R6,R7
271071821301	RES;820 ,1/16W,5% ,0603,SMT	R533,R534
271611471303	RP; 470*4 ,8P ,1/16W,5% ,0612,S	RP7,RP8
271571680302	RP; 68*8 ,16P,1/16W,5% ,1606,SM	RP504,RP508,RP510,RP513,RP51
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP38,RP40,RP42,RP44,RP46
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP505,RP511,RP520,RP528
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP503,RP507,RP509,RP514,RP51
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP22,RP3
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP12,RP16,RP24,RP4,RP546,RP5
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP17

9. Spare Part List-12

Part Number	Description	Location(S)
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP11,RP13,RP27,RP28,RP2
271611240302	RP;24*4 ,8P ,1/16W,5% ,0612,SMT	RP15,RP25,RP26,RP31,RP32,RP3
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP19
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP23,RP523
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP18,RP20,RP21,RP515,RP536,R
271611470301	RP;47*4 ,8P ,1/16W,5% ,0612,SMT	RP14
271571470301	RP;47*8 ,16P ,1/16W,5% ,1606,SM	RP6,RP9
271611680301	RP;68*4 ,8P ,1/16W,5% ,0612,SMT	RP506,RP512,RP521,RP529
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP516
345675400023	RUBBER;DOWN LCD,8355	
345675930001	RUBBER;LCD,UPPER,8677T	
565167540001	S/W;CD ROM,SYSTEM DRIVER,8355	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
565167000013	S/W;CD-ROM,B'S RECORDER GOLD2.0	
340675400038	SCREW ASSY;CPU,8355	
371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	
371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
340675400030	SHIELDING ASSY;HDD UP,8355	
342675400017	SHIELDING;HDD TOP,8355	
333020000002	SHRINK TUBE;600V,105'C,D0.8*11.5	
333050000107	SHRINK TUBE;UL,600V,105'C,ID2.5*	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003037	SOLDER CREAM;SH-6309,SHENMAO,63/	

Part Number	Description	Location(S)
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010005	SOLDER WIRE;63/37,0.8,NA,N/C,PRC	
370102611902	SPC-SCREW;M2.6L19,K-HEAD,NIW	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NL	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
340678300005	SPEAKER ASSY; L,20*16,2W,MEI-SHA	
340678300006	SPEAKER ASSY; R,20*16,2W,MEI-SHA	
340678300017	SPEAKER ASSY;L,20*16,2W,FENG-CHI	
340678300016	SPEAKER ASSY;R,20*16,2W,FENG-CHI	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
345668900016	SPONGE;BIOS BATT,M722	
377102010361	S-STANDOFF;M2.0DP3.0H3.6L1.1,NIW	MTG18
377102610047	S-STANDOFF;M2.6DP3.5H5L1.1,NW	MTG12,MTG17
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	

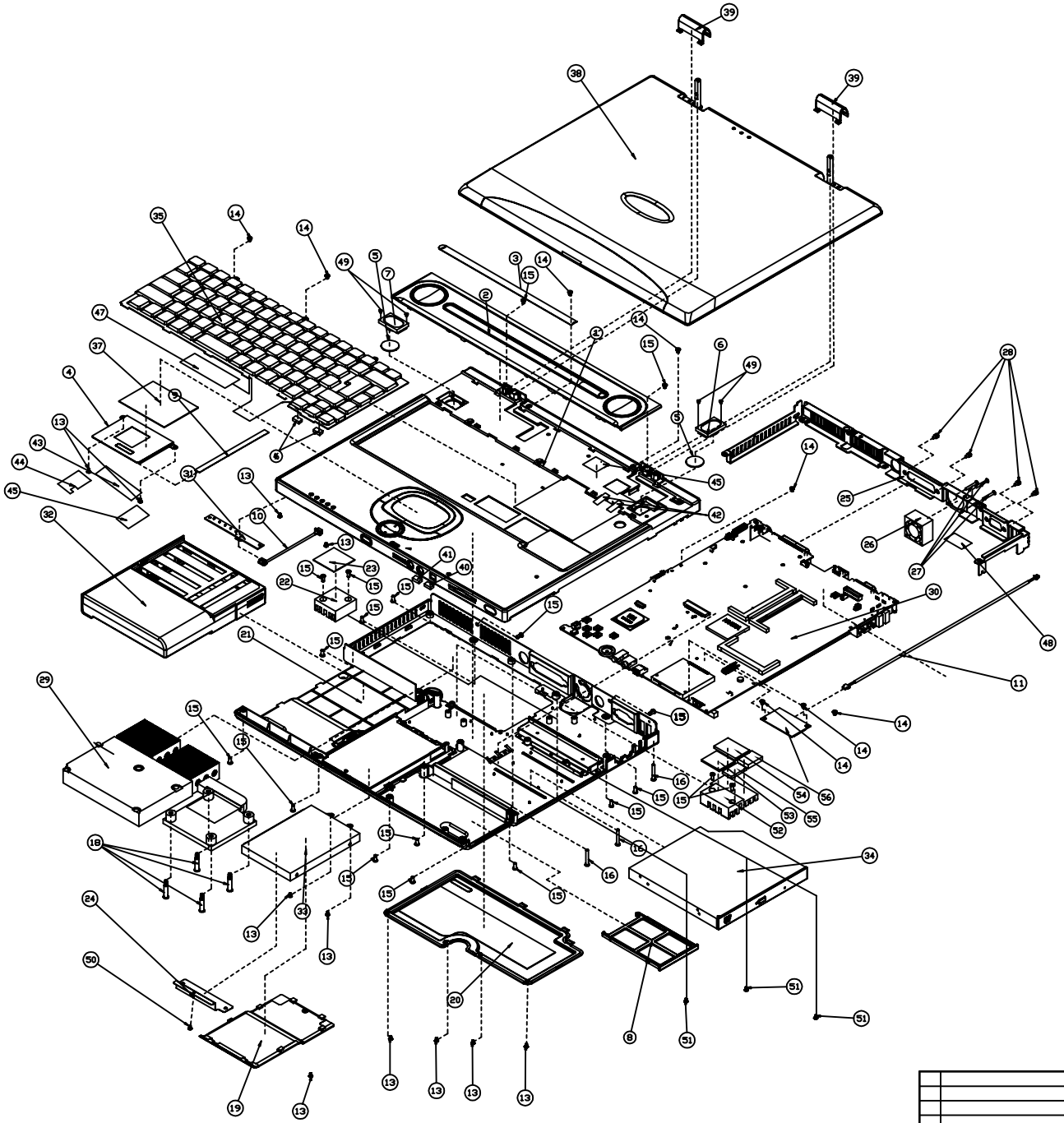
9. Spare Part List-13

Part Number	Description	Location(S)
297120101007	SW;DIP,SPST,4P,24VDC,.025A,SMT	SW3
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW2
297040200001	SW;PUSH BUTTON,DPDT,4P,12V/50MA	SW10
297040102002	SW;PUSH BUTTON,SPST,15V/20MA,H3.	SW4,SW5,SW6,SW7,SW8,SW9
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225600000310	TAPE;ADHENSIVE,DOUBLE-FACE,W8,UL	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
345675400007	THERMAL PAD;NORTH BRIDGE,MPT,835	
310111103011	THERMISTOR;10K,1%,RA,DISK,103AT-	
441675400051	TOUCH PAD MODULE;Synaptics,TM41P	
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ16,PQ17,PQ18,PQ22,PQ2
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	Q13,Q18,Q29,Q30,Q35,Q501,Q50
288200301004	TRANS;3LN01S,N-MOSFET,SMCP	Q2
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU6
288204532002	TRANS;AP4532M,P&N-MOSFET,SO8	
288200144010	TRANS;DDTA144WCA,PNP,SOT-23,SMT	
288200144011	TRANS;DDTC144TCA,NPN,SOT-23,SMT	
288200144009	TRANS;DDTC144WCA,NPN,SOT-23,SMT	
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	Q3,Q4
288200144002	TRANS;DTA144WK,PNP,SMT	PQ14,Q528
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q11,Q12,Q16,Q26,Q27,Q33,Q34,(
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ5,Q15,Q17,Q19,Q23,Q24,Q25,(
288206676003	TRANS;FDB6676,30V/84A,.0075OHM,N	
288206035005	TRANS;FDD6035AL,46A,30V,16mOHM,T	
288206676005	TRANS;FDS6676S,14.5A,30V,9mOHM,S	

Part Number	Description	Location(S)
288206690003	TRANS;FDS6690S,N-MOS,.022OHM,SO8	
288206982003	TRANS;FDS6982S,N-MOSFET,DUAL,SO8	
288207764001	TRANS;FDS7764A,N-MOS,.0075OHM,SO	
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q1,Q2,Q3,Q502
288200503001	TRANS;IPB05N03L,80A,30V,7.2mOHM,	PQ6,PQ7,PQ8
288201403002	TRANS;IPD14N03L,30A,30V,20mOHM,T	PQ19,PQ20,PQ21
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ13
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q1
288204350001	TRANS;PBSS4350Z,50V,5A,SOT223	PQ9
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q20,Q31,Q32,Q4,Q517,Q6
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PU14,PU18,PU5
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	U2
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	U27,U529
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU13,PU15,PU16,PU4,U504,U52
288204810001	TRANS;SI4810DY,N-MOS,.0155OHM,SO	
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU17
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ10,PQ11,PQ12,PQ2,PQ3,Q503
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU9
288208107001	TRANS;TPC8107,13A/30V,P-MOSFET,S	Q10,Q11,Q12,Q7,Q8,Q9
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
271911103906	VR;10K,20%,0.05W,RN101GAC10KPHJ-	VR1
421675400011	WIRE ASSY;ANTENNA,HSD,LCD,8355	
421675400008	WIRE ASSY;ANTENNA,H-T,LCD,8355	
421675400012	WIRE ASSY;BIOS,BATTERY,8355	
421675400001	WIRE ASSY;INVERTER,8355	

9. Spare Part List-14

Part Number	Description	Location(S)
421675400004	WIRE ASSY;LCD,AU-B150PG01,8355	
421675400009	WIRE ASSY;LED BD,TOP,8355	
421675400010	WIRE ASSY;MDC,8355	
332110020021	WIRE;#20,UL1007,31MM,BLANK,PRC	
332110020042	WIRE;#20,UL1007,70MM,RED,PRC	
332110026115	WIRE;#26,UL1007,45MM,BLACK,PRC	
332100000017	WIRE;#28,UL1061,100MM,YELLOW,PR	
332110028109	WIRE;#28,UL1061,40MM,BLUE,PRC	
332110028098	WIRE;#28,UL1061,55MM,RED,PRC	
273001050080	XFMR;CI8.5,16T/2600T,220mH,SMT,o	T1
273001050081	XFMR;CI8.5,16T/2600T,220mH,SMT,o	
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U502
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	X1
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X501
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X6
274012500415	XTAL;25MHZ,20PF,30PPM,8.0*4.5,SM	X2
274012700406	XTAL;27MHZ,20PF,20PPM,8.0*4.5,SM	X3
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X5
		P/N:526267540015



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
56	370102010405	THERMAL PAD4;HEATSINK,CHOCK,M/B,8555	1	PART	
55	370102010205	THERMAL PAD3;HEATSINK,CHOCK,M/B,8555	1	PART	
54	371101630301	THERMAL PAD2;HEATSINK,CHOCK,M/B,8555	1	PART	
53	346675400029	THERMAL PAD1;HEATSINK,CHOCK,M/B,8555	1	PART	
52	343678300001	HEATSINK;MOS,8555,MPT	1	PART	
51	370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	3	PART	
50	370102010205	SPC-SCREW;M2L2(t0.3),NIW/WLK	1	PART	
49	371101630301	SCREW;M1.6L3,K-HD(+),NIB/NLK	4	PART	
48	346675400029	CONDUCTIVE TAPE;DC-IN,MB,8355	1	PART	
47	346675400028	CONDUCTIVE TAPE;KB,8355	1	PART	
46	345675400030	GASKET;KB,8355	2	PART	
45	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	PART	
44	345678300012	CONDUCTIVE TAPE;TP BRACKET,LEFT,8555,ID1	1	PART	
43	345678300011	CONDUCTIVE TAPE;TP BRACKET,UP,8555,ID1	1	PART	
~~42~~	~~225675400001~~	~~CONDUCTIVE TAPE;TOP ASSY,DBR,RIGHT,8355~~	~~2~~	~~PART~~	
41	345675400012	GASKET;M/B ASSY,MIC-IN,8355	1	PART	
40	345675400011	GASKET;M/B ASSY,1394,8355	1	PART	
39	344675400016	COVER;HINGE,8355	2	PART	
38	441675400031	LCD ASSY;14"XGA,QDI,8355	1	ASSY	
37	441675400051	TOUCH PAD MODULE;Synaptics,TM41P	1	PART	
36	412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I	1	ASSY	
35	531017240112	KBD;88,US,3000170042,ZIPPY,8355	1	ASSY	
34	451675400071	CD-ROM TEAC ME KIT;8355	1	ASSY	
33	451675400111	HDD ME KIT;8355	1	ASSY	
32	441676200001	BATT ASS'Y;14.8V,6.6AH,LI,BL4366G03	1	ASSY	MSL
31	411675400004	PWA;PWA-8355,LED BD	1	ASSY	MSL
30	411675400001	PWA;PWA-8355,MOTHER BD,T/U	1	ASSY	MSL
29	340675400024	HEATSINK ASSY;CPU,AMD K8 DTM,8355	1	ASSY	MPT
28	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	PART	
27	371102011502	SCREW;M2L15 FLT(+) NIW/NLK	3	PART	
26	340675400029	FAN ASSY;ID,8355	1	ASSY	SUNON
25	342675400013	BRACKET;ID,8355	1	PART	MPT
24	342675400017	SHIELDING;HDD TOP,8355	1	PART	MPT
23	345675400007	THERMAL PAD;NB,DW,8355,MPT	1	PART	MPT
22	343675400003	HEATSINK;NB,8355,MPT	1	PART	MPT
21	340678300013	HOUSING ASSY;HOUSING,8555	1	ASSY	ShenJI
20	340675400014	COVER ASSY;CPU,8355	1	ASSY	ShenJI
19	344675400024	COVER;HDD,8355	1	PART	ShenJI
18	340672400009	SCREW ASSY;CPU,8640S	4	ASSY	
17	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	2	PART	
16	370102611902	SPC-SCREW;M2.6L19,K-HEAD,NIW	3	PART	
15	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	17	PART	
14	370102610302	SPC-SCREW;M2.6L3 NIB,K-HD,NYLOK	8	PART	
13	370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	11	PART	
~~12~~	~~346675400025~~	~~PAD;CHOCK,M/B,8355~~	~~1~~	~~PART~~	~~MPT~~
11	421675400010	WIRE ASSY;MDC,8355	1	ASSY	MPT
10	421675400009	WIRE ASY;LED BD,TOP,8355	1	ASSY	MPT
9	422675400001	FFC ASSY;TOUCH-PAD,8355	1	PART	??
8	344672300025	DUMMY CARD;PCMCIA,MANGUSTA	1	PART	MPT
7	340678300005	SPEAKER ASSY;L,.20*16*2W,MEI-SHAN,8555	1	ASSY	??
6	340678300006	SPEAKER ASSY;R,20*16.,2W,MEI-SHAN,8555	1	ASSY	??
~~5~~	~~345675400004~~	~~SPONGE;SPEAKER,8355~~	~~2~~	~~PART~~	~~MPT~~
4	340675400011	BRACKET ASSY;TOUCH-PAD,8355	1	ASSY	MPT
3	344675400015	NAME-PLATE;SPEAKER COVER,8355	1	PART	ShenJI
2	340675400010	COVER ASSY;SPEAKER,K/B,8355	1	ASSY	ShenJI
1	340678300002	COVER ASSY;TOP,8555	1	ASSY	ShenJI

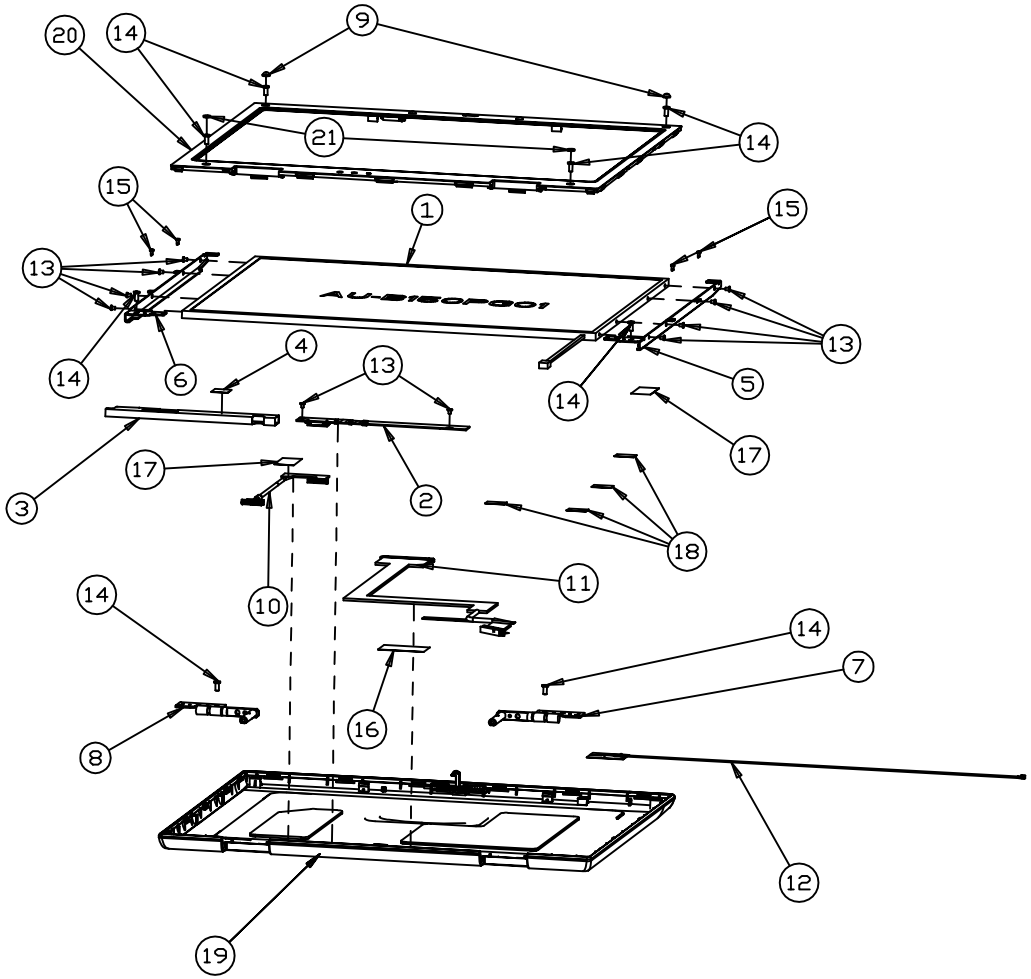
ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	20-Feb-03	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.500	DRAWING NAME	8555 CASE KIT		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	526267830001	R00A

MITAC Technology Corp.

SHEET NO. 1 OF 1



ITEM	PART NO	DESCRIPTION	Q'TY	REMARK
21	345675400023	RUBBER;DOWN LCD,8355	2	
20	340675400007	COVER ASSY;LCD 15",8355	1	
19	340675400003	HOUSING ASSY;LCD 15",8355	1	
18	225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR,RIGHT,8355	4	
17	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	
16	345678300022	CONDUCTIVE TAPE;LCD PANEL,8555	1	
15	371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	4	
14	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	8	
13	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	10	
12	421675400011	WIRE ASSY;ANTENNA,HSD,LCD,8355	1	
11	421675400004	WIRE ASSY;LCD,AU-B150PG01,8355	1	
10	421675400001	WIRE ASSY;INVERTER,8355	1	
9	345675930001	RUBBER;LCD,UPPER,8677T	2	
8	340675400006	HINGE;L,15",8355	1	
7	340675400005	HINGE;R,15",8355	1	
6	342675400006	BRACKET;LCD 15",SPWG,L,8355	1	
5	342675400005	BRACKET;LCD 15",SPWG,R,8355	1	
4	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	
3	346669900004	INSULATOR;INVERTER,7170	1	
2	411672900001	PWA;PWA-INVERTER BD DAI-05A01	1	
1	413000021005	LCD;AU-B150PG01,TFT,15",SXGA+	1	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± / RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	19-Sep-03	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.250	DRAWING NAME	LCD ASSY;AUO,15",INV/SMD,8355 ID1		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441675400036	R00

MiTAC Technology Corp.

model nameLCD-ASSY-15-8355

file nameLCD_ASSY_B150PG01_ID1_8355

MODEL : 8355 Revision 01

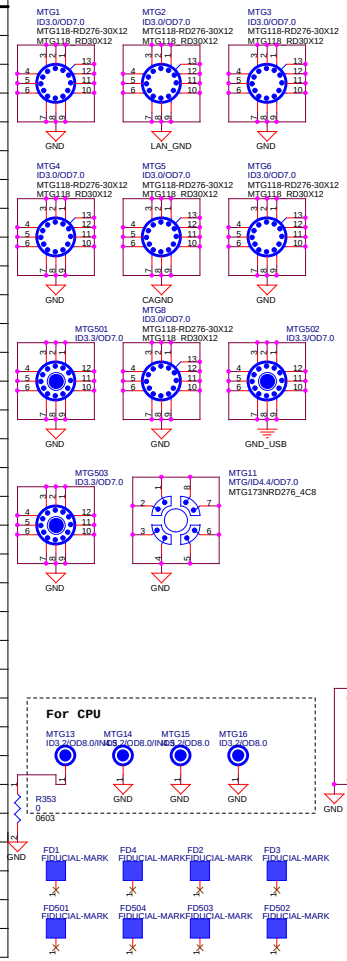
PROJECT CODE	**G039**	**PCB P/N**	**316675400001**
PRODUCT CODE	**6754**	**ASSY P/N**	**411675400001**

FUNCTION	CHIP	INTERRUPT	REQ/GNT	IDSEL
VGA	ATI M9-CSP64	PCIINTA#		
PCMCIA	ENE710	PCIINTB#	REQ0#/GNT0#	AD20
CARDREADER	ENE710	PCIINTC#	REQ0#/GNT0#	AD20
MINIPCI	WIRELESS LAN B/D	PCIINTC#	REQ2#/GNT2#	AD21
IEEE1394	VT6107L	PCIINTD#	REQ3#/GNT3#	AD22

X1	14.318Mhz	CLOCK GENERATOR
X3	27Mhz	VGA- ATI M9-CSP64
X5	32.768KhZ	RTC
X6	24.576Mhz	IEEE 1394- VT6107L
X2	25MhZ	LAN PHY
X7	24.576Mhz	AUDIO CODEC
X4	16Mhz	H8

Contexts

For M/B and machine



REVISION	TAPEOUT DAY	HISTORY
R00	2002/11/6	DESIGN FOR EVT
R0A	2002/12/23	PAGE2 CHANGE R520,R518 TO 680OHM DEL C148,C151,C168,C155,R64,L53 FOR DDR_CLK ADD R346,R347 DEL R529,R40,R36,R39 FOR HDT CHANGE R66,R71,R19,R517,R519,R18,R516 CHANGE R17,R15,R53,R62,R514,R511,R512 TO 470OHM PAGE3 CHANHE U4 AND VID CIRCUIT CHANGE L54 TO 0OHM,DEL R69 DISABLE VDDA RESERVE CIRCUIT PAGE4 CHANGE RP515,RP516,RP517 TO 47OHM ADD C865,C94,C869,C108,C874,DEL C519 FOR DDR_CLK DEL R541,R542,R543,R544 PAGE5 FOR VGA ADD R802 TO +2.5V FOR COST DOWN ADD U8,C194,C168 DEL Q14,R144,R150,C293,C292,R149,R143 PAGE6 FOR CLK_GEN STRAP ADD R345,R825,R260 FOR EMI ADD C177,C192,C190,C184,C154,C155,C163 PAGE7 FOR AGP_VREF ADD R161,R160,C303,C660 DEL R616 FOR SW_1.5V/1.25V ADD U6A PAGE8 ADD L542,L540(RESERVE) DISABLE L514,C600,C280,C592 PAGE9 FOR CRT LEAKAGE DEL R507,R7 FOR EMI ADD RP4,CP502 DEL R501,R502 PAGE10 ADD U4,C147,C879,C841(RESERVE) DEL L529,L526,RP14,RP15 PAGE11 ADD C148,C151,C883,R852,R854 PAGE12 ADD R186,Q29,R364,U10B FOR V_LINK CHANGE R658 TO 3K,R672 TO 1K,R648 FOR SMB ADD R537,R535 DEL Q523,Q22,R725,R273 PAGE13 FOR IDE_RESET ADD Q534,Q533,R827,R826 PAGE14 ADD R365 PAGE15 FOR INDICATOR ADD Q30,Q507,R828 DELR260,R711,D516,D517 PAGE17 FOR EMI ADD L541,R529 PAGE18 FOR CMI9738 ADD R834,C880 DEL R732 FOR EMI DEL L84,C824 ADD C391 CHANGE R733,R739 TO 10K, R741,R738 TO 33K PAGE19 FOR DEPOP CIRCUIT ADD U17,R367,D520,C890 CHANGE VR1 PAGE20 INVERSEJ10 PAGE21 FOR FAN SOFT-START ADD C876,C115,C135 ADD R348,R381,Q31,R355,Q535 PAGE22 ADD R356,R357,R358,R359,R360,R361,R362,R363 SHORT U501,U3 PIN1,2 PAGE24 CHANGE R111,R294,R318 TO 470OHM ADD U13,R791,C889,C84,R350
R0B		PAGE 2 CHANGE R15,R17,R62,R63,R511,R512,R514 to 680 OHM PAGE 8 FOR M9_1.8V ADD C896,C897,C898,C899 PAGE 10 CHANGE R721 to 10K,C742 to 1U PAGE 17 DEL D15,D16,ADD R862 PAGE 20 FOR FIR ADD R864,C901,C902,C395;CHANGE R324,R329 FOR TP DEL D19 PAGE 21 FOR CPU ADD RT500,R865,R866 PAGE 24 FOR CHIPSET APNOTE CHANGE U10 TO U520
R0C	2003/05/02	PAGE 2 Delete R15,R17,R62,R63,R511,R512,R514 Add U34(LM99) PAGE 6 For ICS950403 Add R868,D2,Delete R83,R867 PAGE 7 Add R779,R777,R749,R870,R130,R122,U524,C665 Delete RP532,R595,Q506,R813,R719,R718,R791 PAGE 8 Add R571,R584,C361,L549,R575 Delete R570,R566,R576 PAGE 9,10 For M10P request PAGE 20 Add R308,R309,R834,C788,C880,R733,R739,R741,R738 Delete C775, C776, C774, C761, C779, C820,C819,C812 PAGE 23 Change C678,C679 Add R370,R369,R368 Delete R717,R796,R797,R798,R799,R300,Q531,Q532,Q28 C826,C876,C827,C828,C829,D519,L539 PAGE 26 For +2.5V Add U504,L26,C244,R116,R115,Q18 Delete U505,R111 For +1.5V Add U15,L27,C301,R390,R391,C381,C384
R0D	2003/05/07	For PCB layout only
R01		PAGE 2 For M10P add MTG18 AMD request change R24,R521 from 44.2 to 34.8 PAGE 3 Remove RP1,RP2,SW501 PAGE 5 Add pull up for AGP4x(reserve) PAGE 7 For ATI modify U524,Add SW3 for MEM_ID change R794 to 40 ohm,Add RP655 Reserve SUSST# ,STPAGP# from M10 to SB DEL TP510,TP511 Add spread spectrum IC Add pull up for AGP4x(reserve) PAGE 8 Change VDD_MCLK2.5 that follow the VDDR1 PAGE 9 Change VGA resistor pack to 1206 PAGE 14 For K8T800 connect LDTSTOP# to SLP# Connect AGPBZ# to M10 PAGE 15 Change J530 shape to CONN_C12437_50B PAGE 17 Change R542 from +3V to +5V PAGE 18 For EMI Add L86,L87,Del R323,R328,R331,R335 For ESD mount R322 PAGE 19 For EMI Add L49,L51, Del R31,R32,R42,R43 PAGE 20 Change R733,R739,R738,R741 For CD_ROM noise add R732 For ESD change SW4-9 to 2070401000l5(w/ GND) PAGE 21 For EMI change C798,C378,C379 to CAGND PAGE 22 Change J10 power ,GND pin and add Fuse on TP PAGE 23 Add R950,R951,R952,R953 PAGE 25 Del JL524,JL525,JL526,JL527 PAGE 27 Change PF2 from 1A to 1.5A PAGE 29 Add L547,L548 PAGE 32 PR502 pull up VDD5

DRAWN	DESIGN	CHECK	ISSUES

<Core Design>

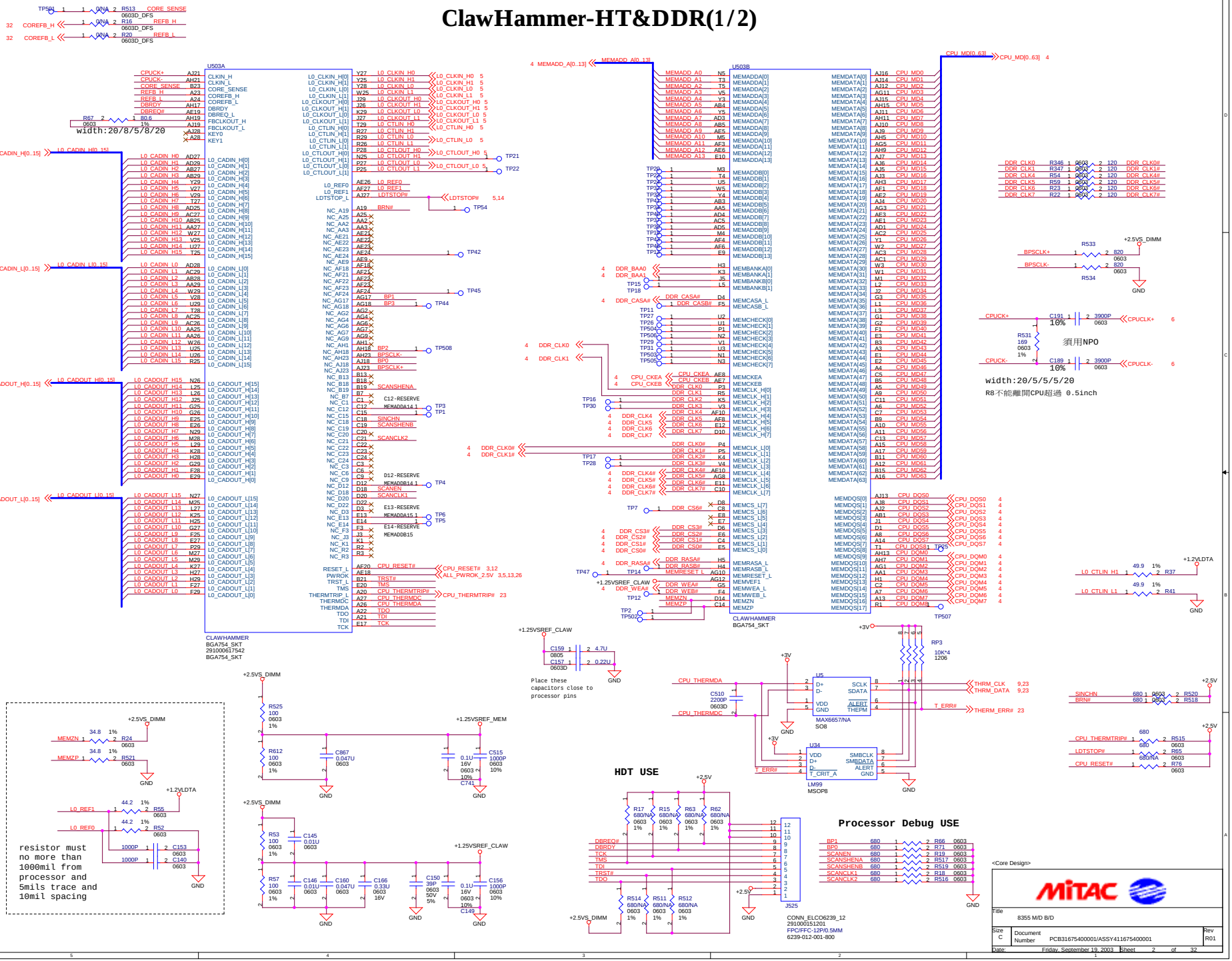
MiTAC

Title: 8355 M/D B/D

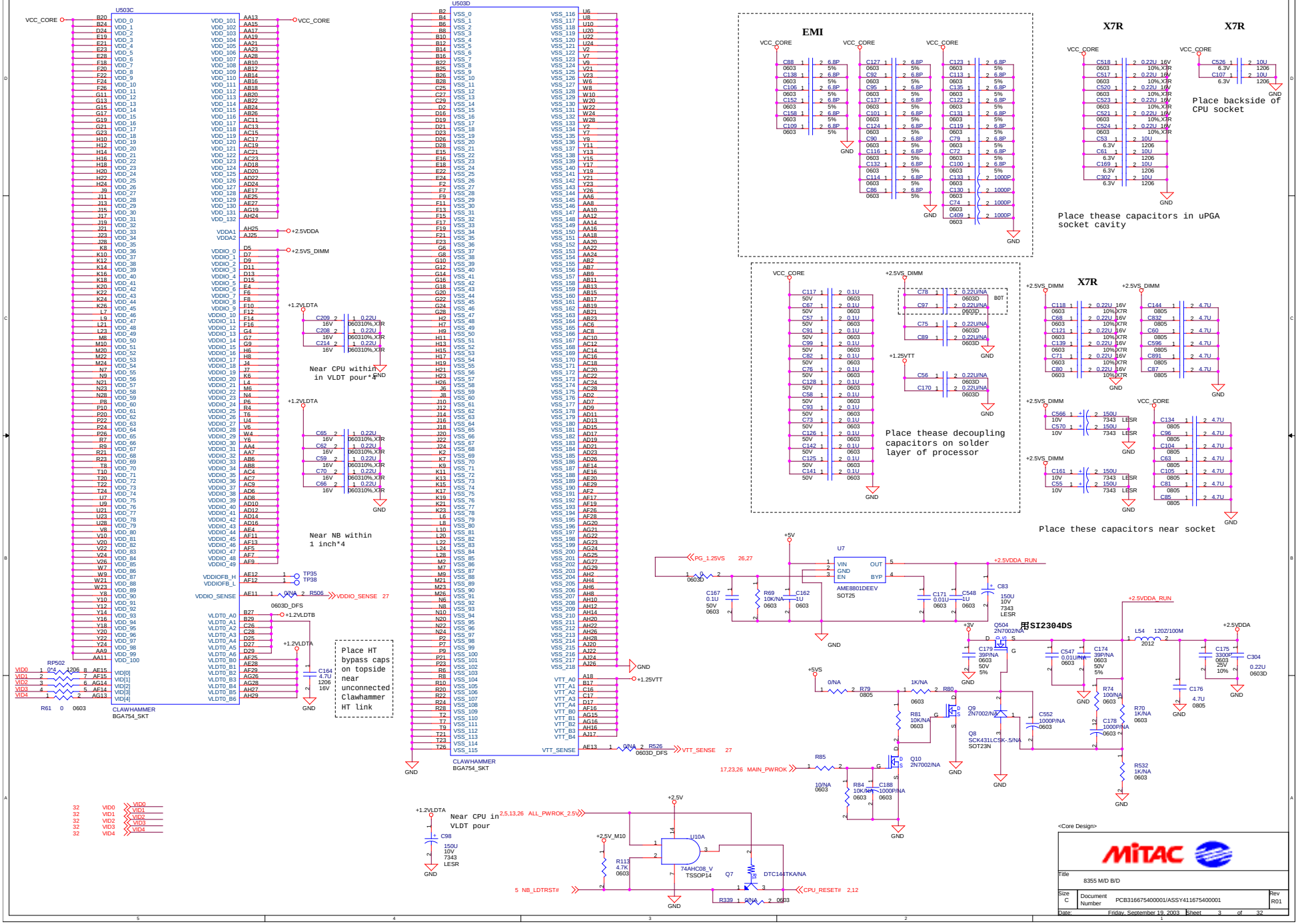
Size: C | Document Number: PCB316675400001/ASSY411675400001 | Rev: R01

Date: Friday, September 19, 2003 Sheet 1 of 32

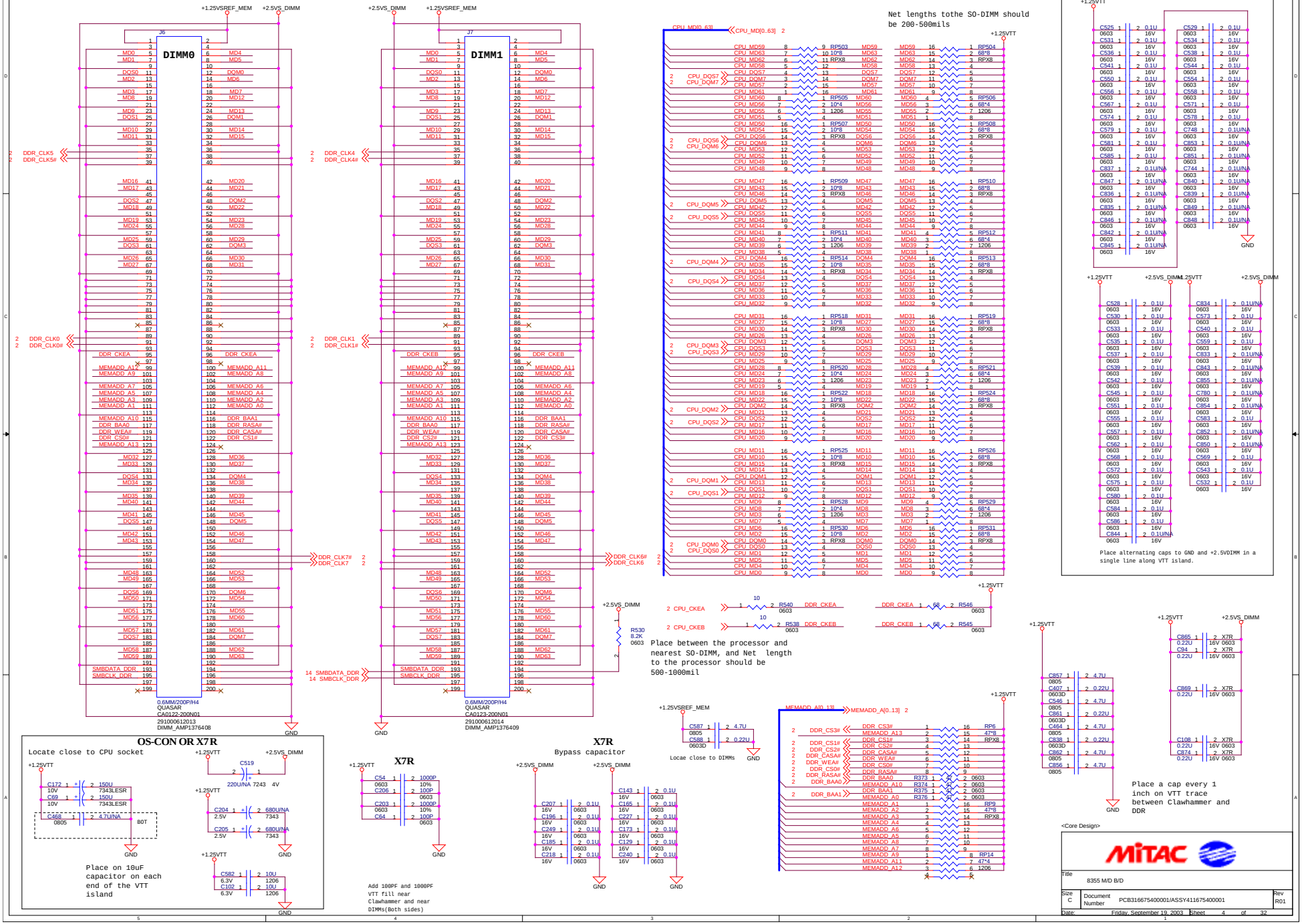
ClawHammer-HT&DDR(1/2)

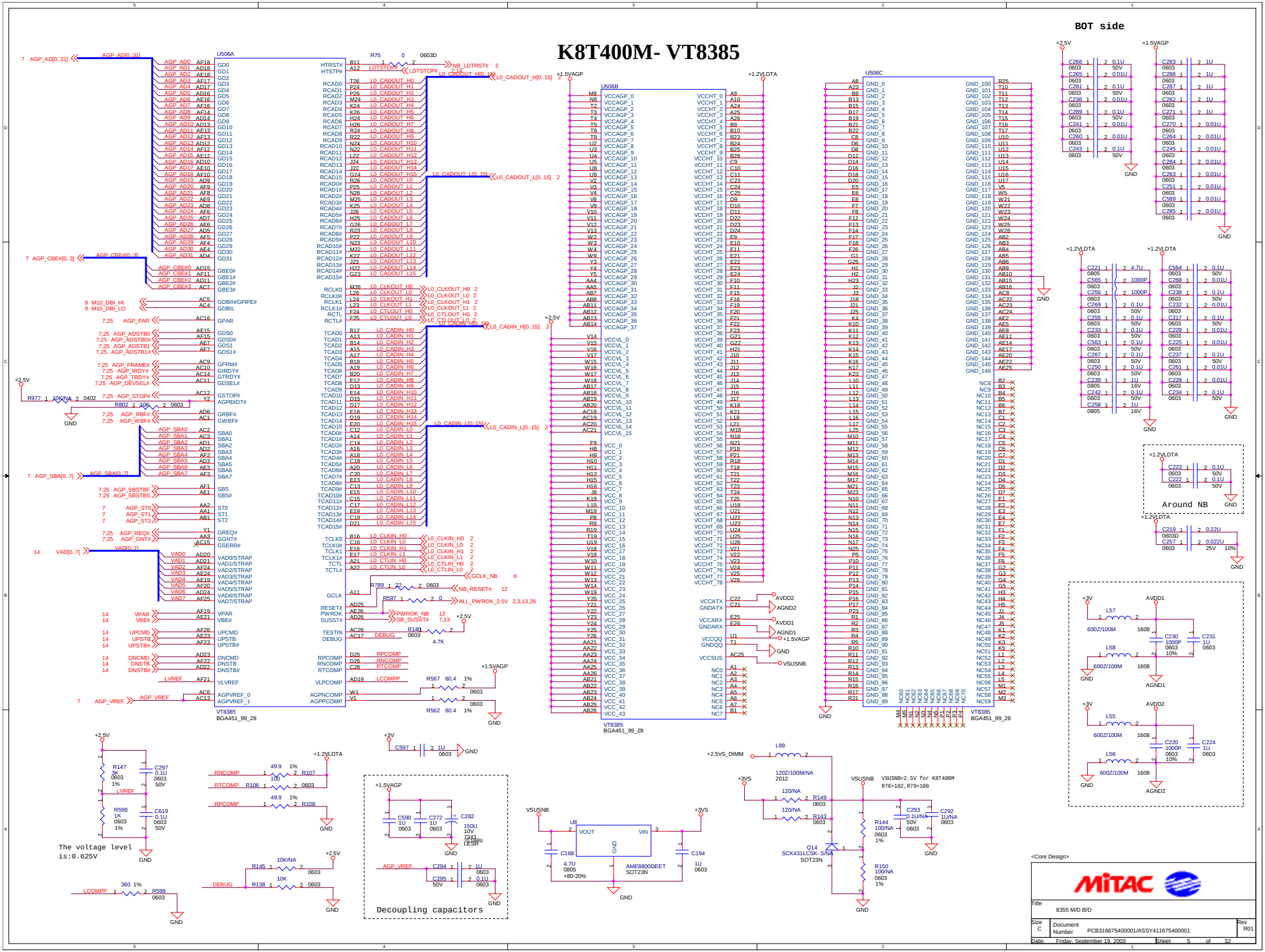


ClawHammer-Power plane(2/2)

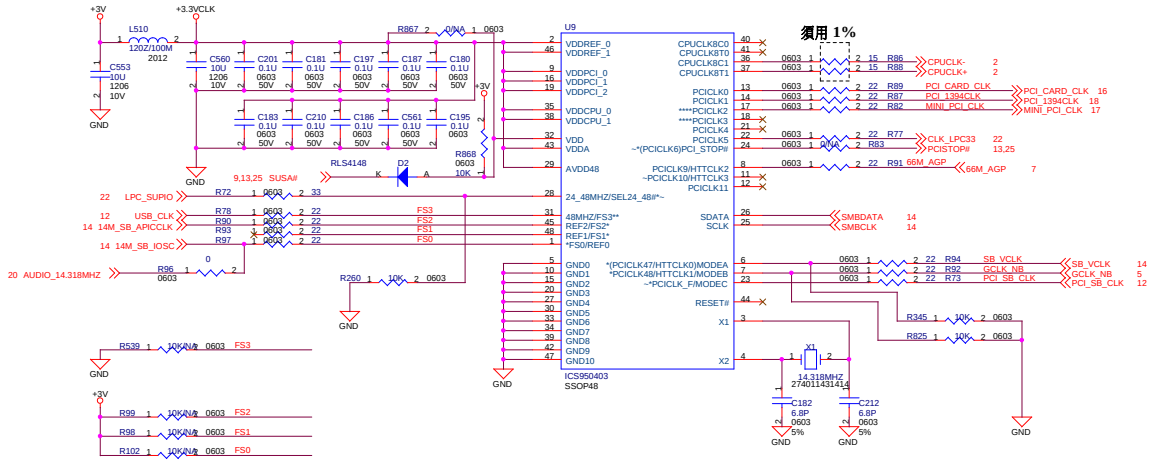


DIMM-SLOT & Termination

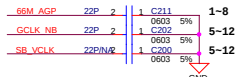




CLOCK GENERATOR(ICS950403)

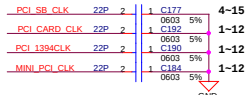


AGP Clock Signal

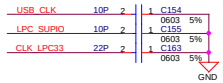


1. 6 : 24
2. Series resistors less than 1
3. GCLK_NB & SB_VCLK is 4 longer than 66M_AGP

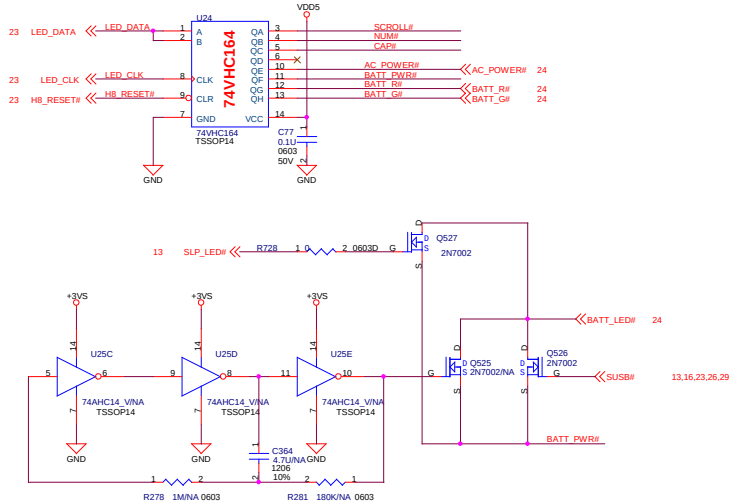
AGP Clock Signal

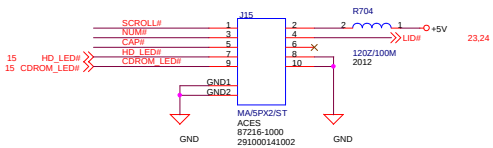


1. 6 : 24
2. Series resistors less than 1
3. PCI_SB_CLK is 3 more than the longest PCI clock



LED INDICIATOR





LED INDICATOR

FS3	FS2	FS1	FS0	CPU Mhz	HTT Mhz	PCI Mhz	
0	0	0	0	100.90	67.27	33.63	
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	67.68	33.34	
0	1	1	1	200.40	66.80	33.40	DEFAULT
1	0	0	0	150.00	60.00	33.00	
1	0	0	1	180.00	60.00	33.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	

<Core Design>

MiTAC

Title: 8355 M/D B/D

Size: C | Document Number: PCB316675400001/ASSY411675400001 | Rev: R01

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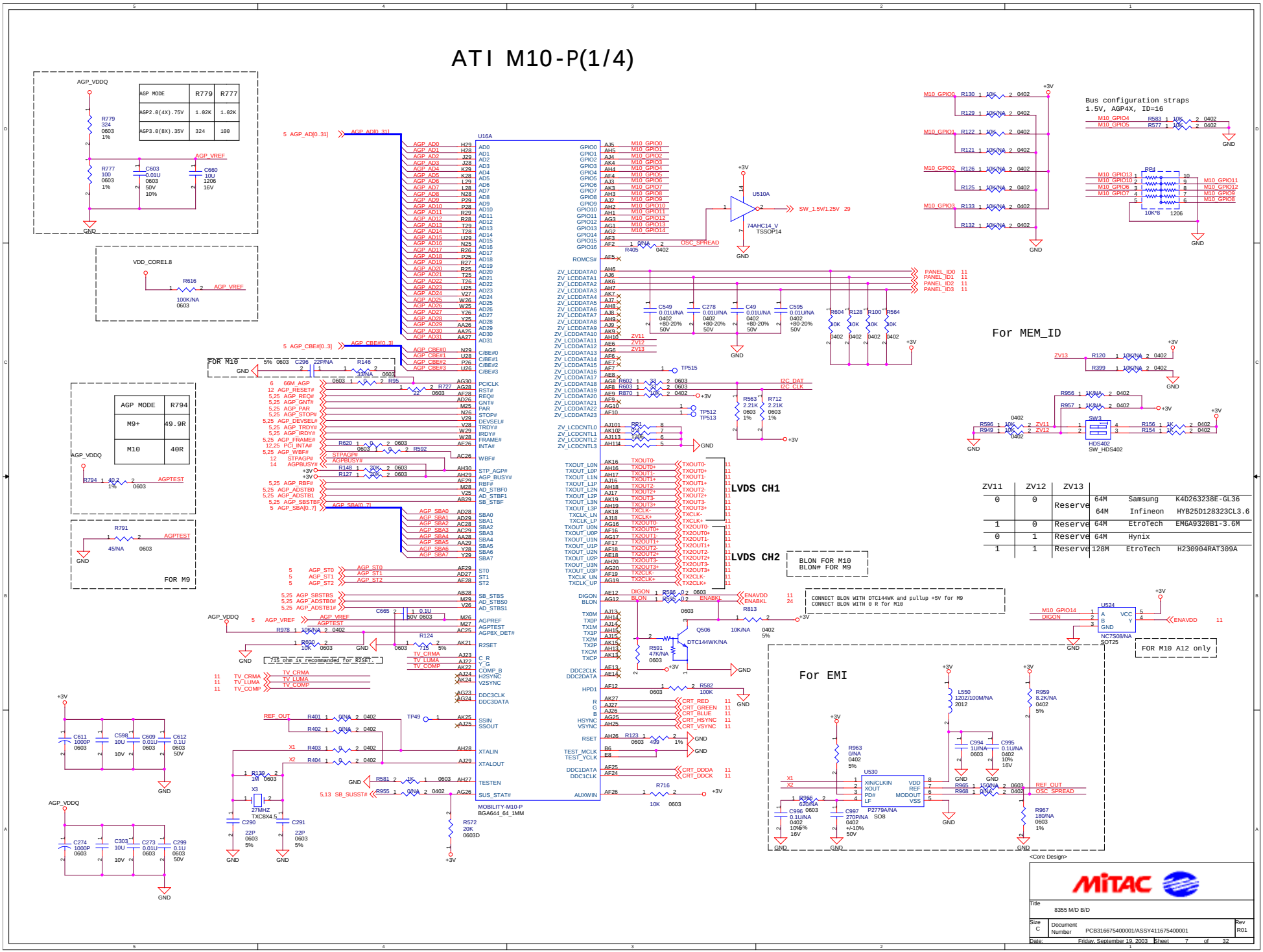
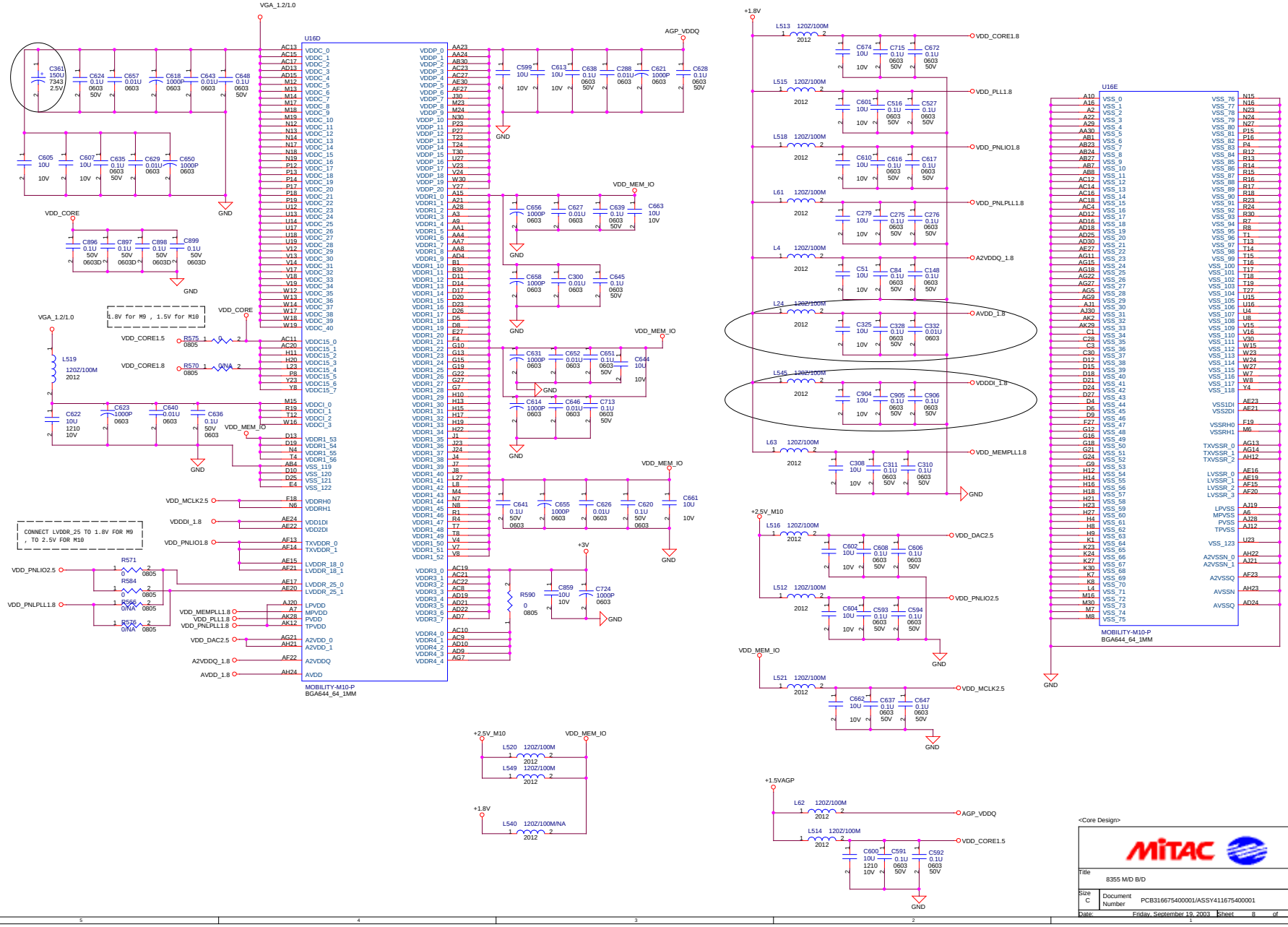
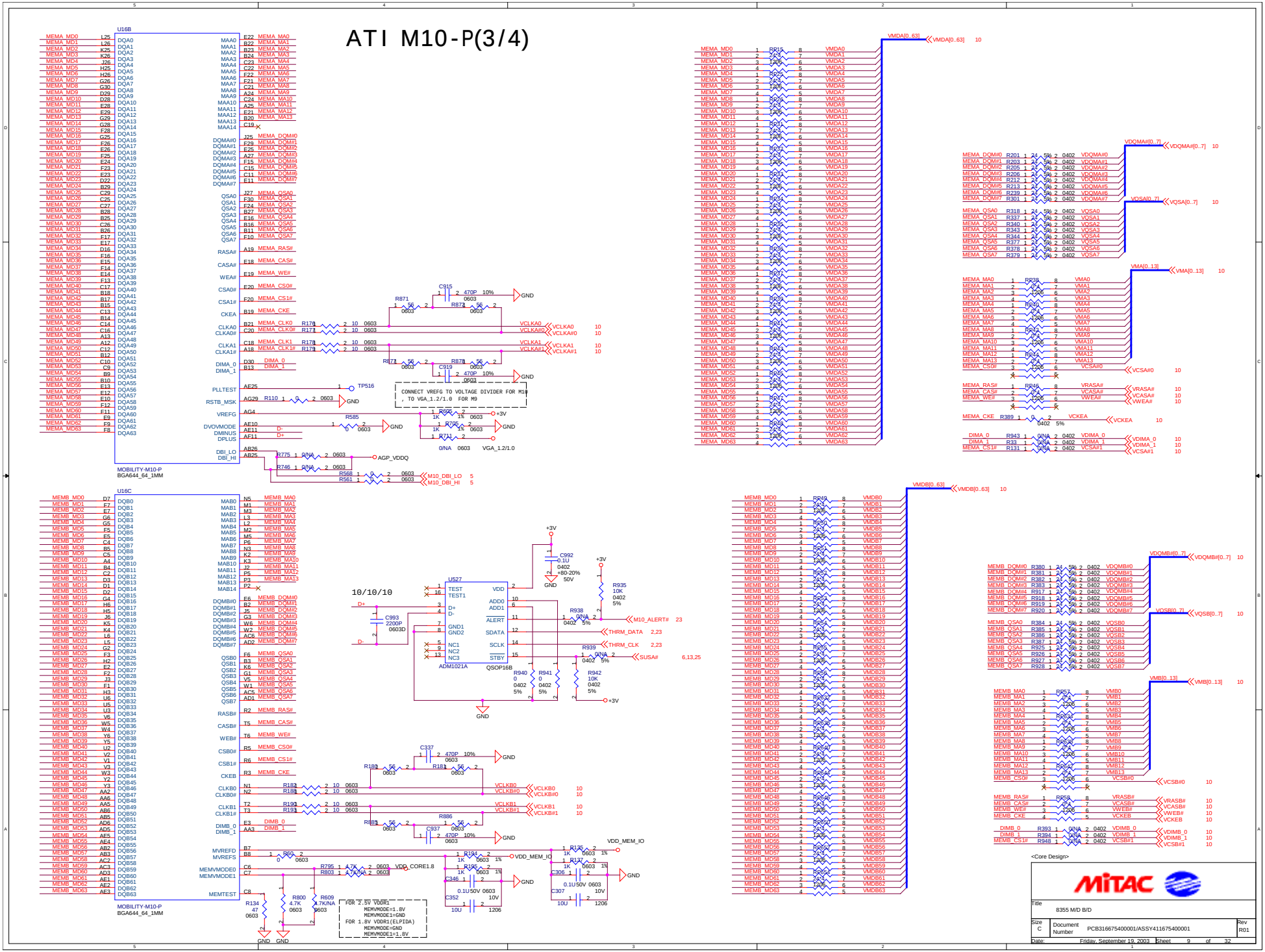


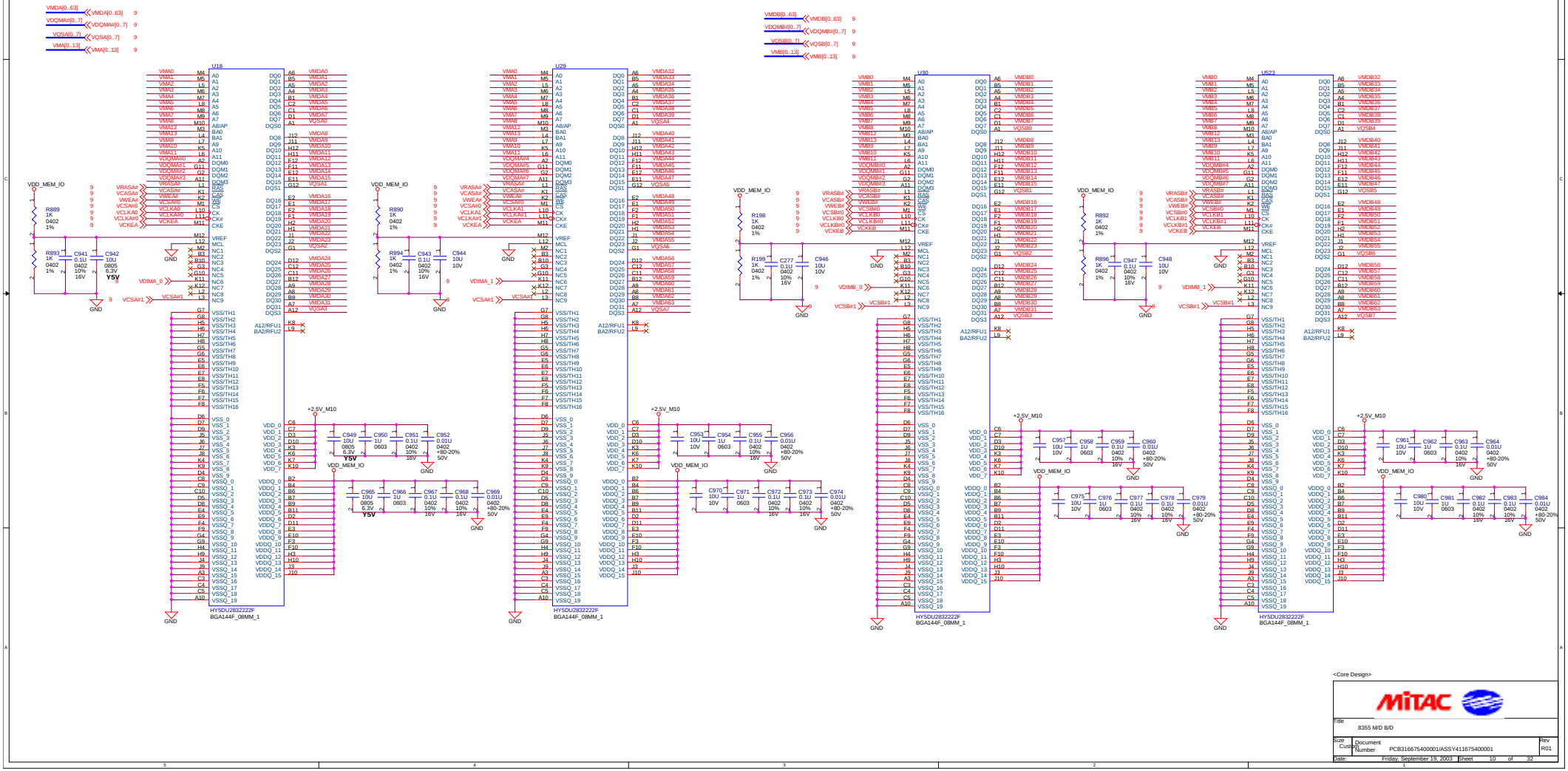
ZV11	ZV12	ZV13			
0	0	Reserve	64M	Samsung	K4D263238E-GL36
			64M	Infineon	HYB25D128323CL3.6
1	0	Reserve	64M	EtroTech	EM6A9320B1-3.6M
0	1	Reserve	64M	Hynix	
1	1	Reserve	128M	EtroTech	H230904RAT309A

ATI M10-P(2/4)

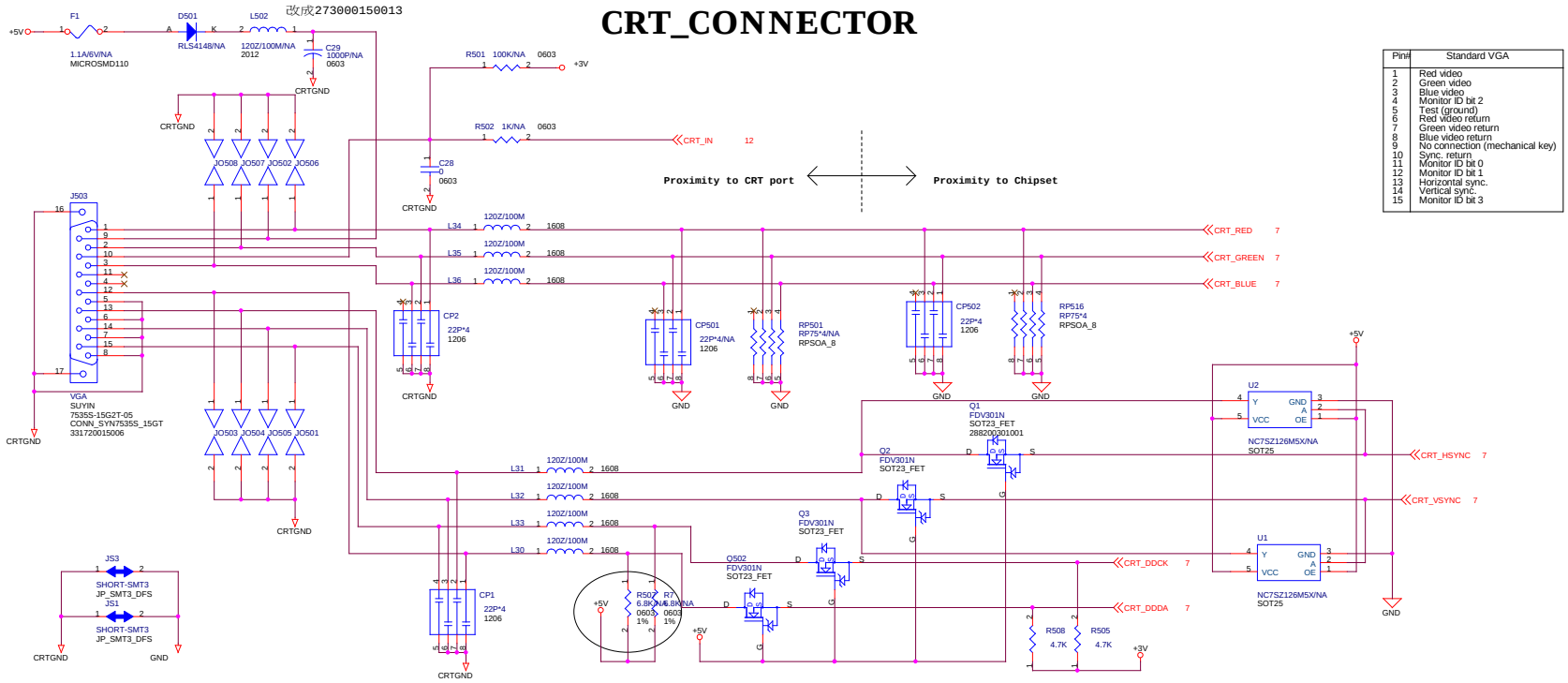




ATI M10-P(4/4)



CRT_CONNECTOR

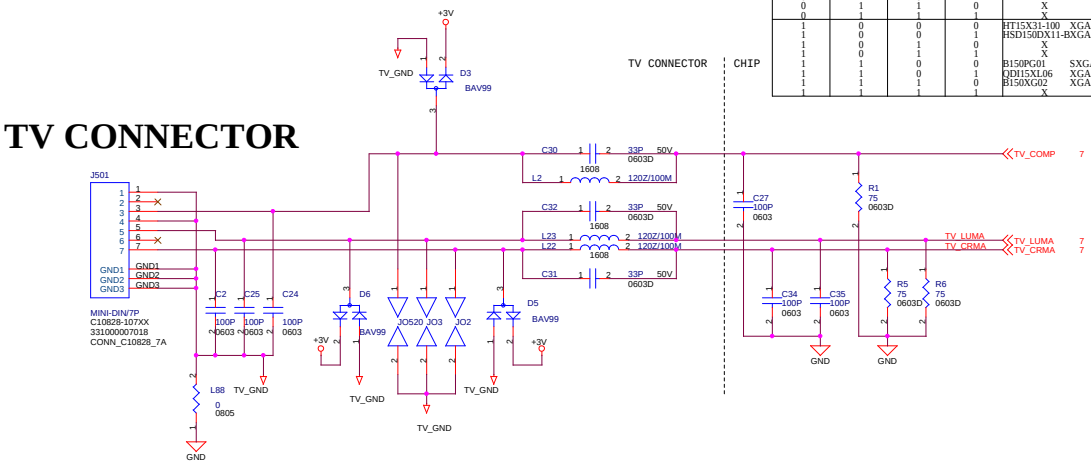


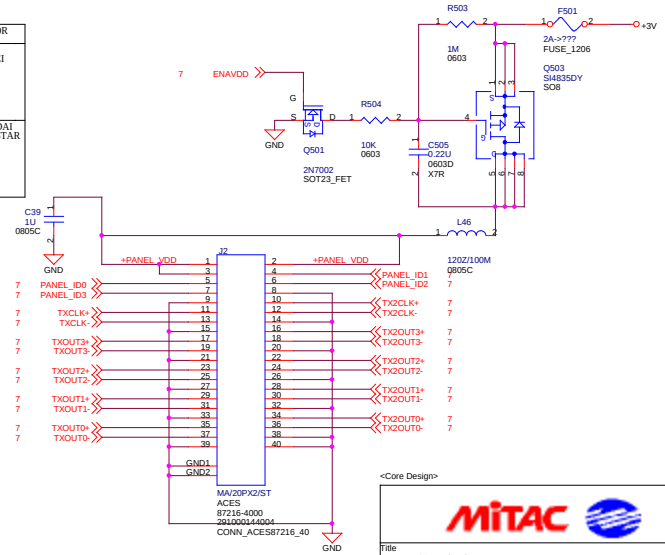
Pin#	Standard VGA
1	Red video
2	Green video
3	Blue video
4	Monitor ID bit 2
5	Test (ground)
6	Red video return
7	Green video return
8	Blue video return
9	No connection (mechanical key)
10	Sync. return
11	Monitor ID bit 0
12	Monitor ID bit 1
13	Horizontal sync.
14	Vertical sync.
15	Monitor ID bit 3

LCD CONNECTOR

LCDID3	LCDID2	LCDID1	LCDID0	PANEL	VENDOR
0	0	0	0	X	
0	0	0	1	N141X6-L01 XGA	CHI MEI
0	0	1	0	QDI141X1LH12XGA	QDI
0	0	1	1	B141XN04-2 XGA	AU
0	1	0	0	X	
0	1	0	1	X	
0	1	1	0	X	
0	1	1	1	X	
1	0	0	0	HT15X31-100 XGA	HYUNDAI
1	0	0	1	HSD150DX11-BXGA	HANNSTAR
1	0	1	0	X	
1	0	1	1	X	
1	1	0	0	B150PG01 SXGA+	AU
1	1	0	1	QDI15XL06 XGA	QDI
1	1	1	0	B150XG02 XGA	AU
1	1	1	1	X	

TV CONNECTOR





<Core Design>

MiTAC

Title	8355 M/D B/D	
Size C	Document Number PCB316675400001/ASSY411675400001	Rev R01
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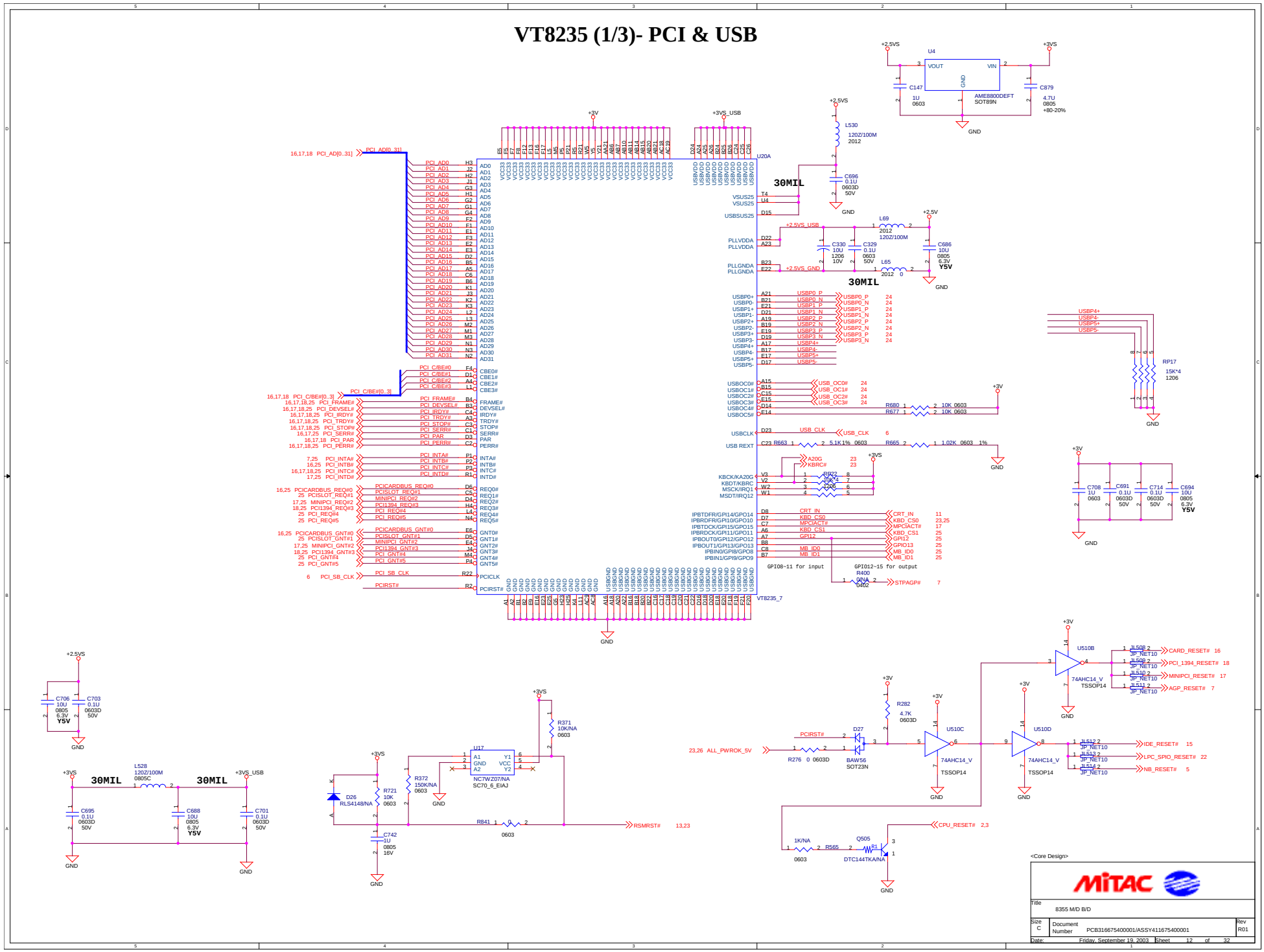
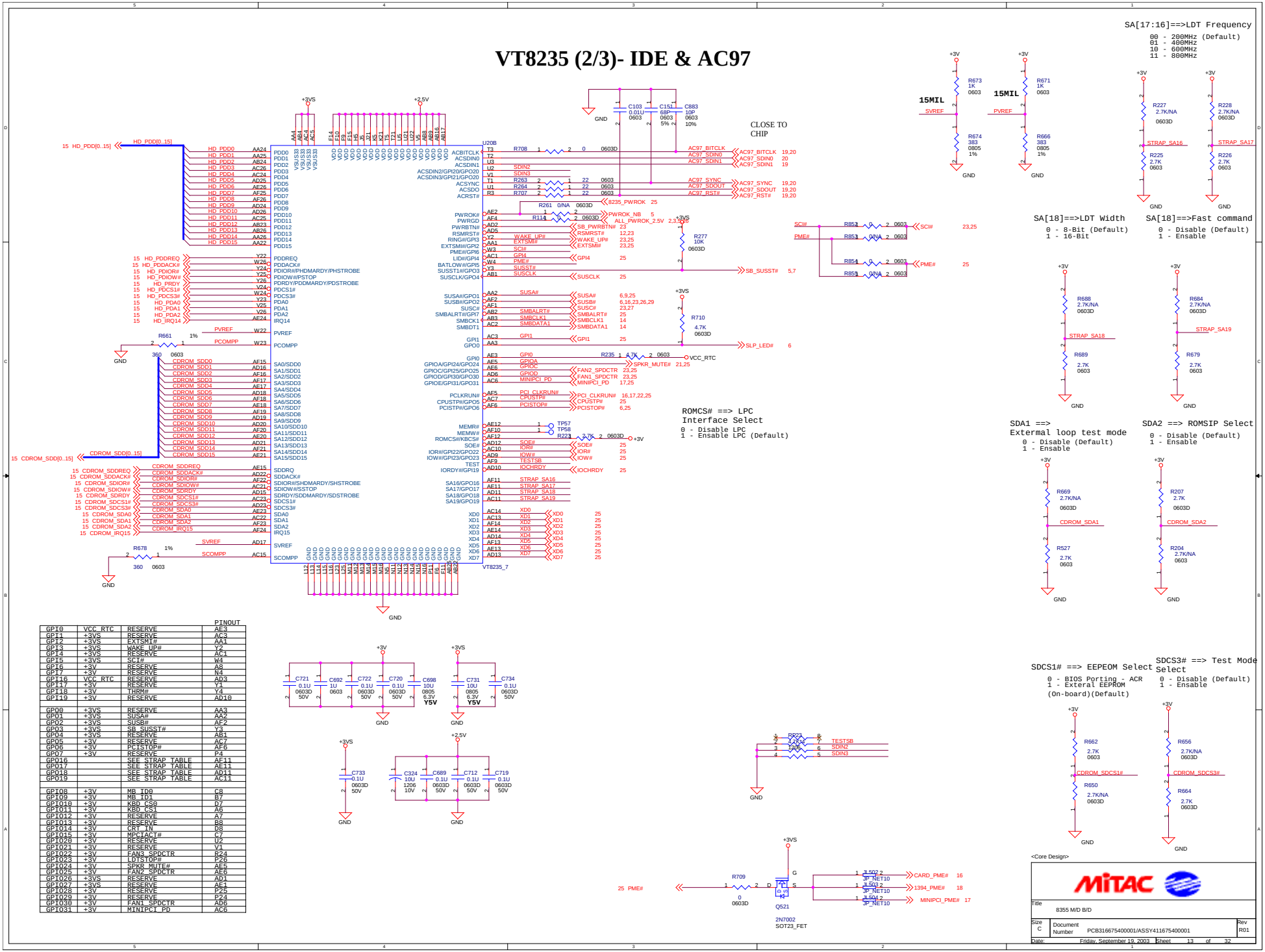
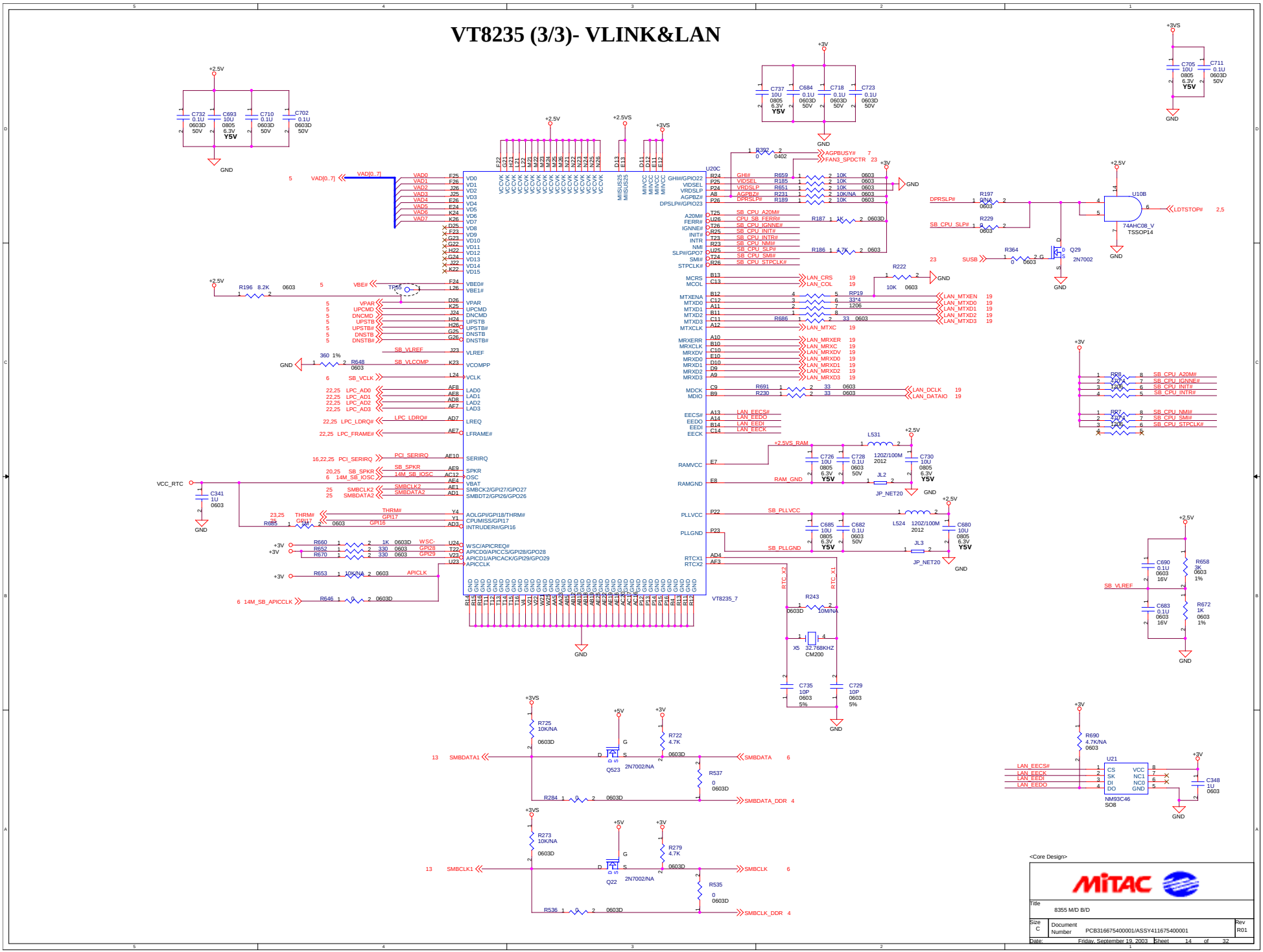


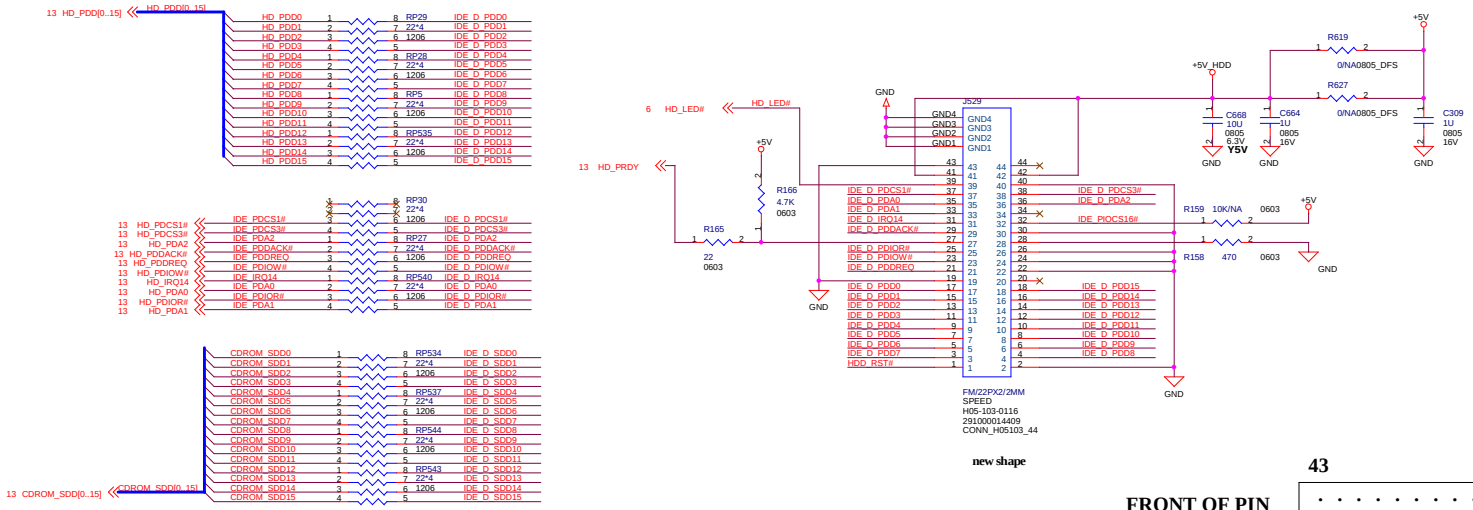
VT8235 (2/3)- IDE & AC97

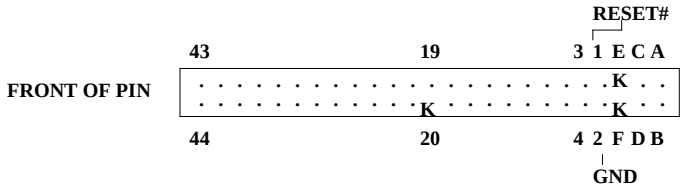


		PINOUT	
GPI0	VCC_RTC	RESERVE	AE3
GPI1	+3VS	RESERVE	AC3
GPI2	+3VS	EXTSMI#	AA1
GPI3	+3VS	WAKE_UP#	Y2
GPI4	+3VS	RESERVE	AC1
GPI5	+3VS	SCI#	W4
GPI6	+3V	RESERVE	A8
GPI7	+3V	RESERVE	N4
GPI16	VCC_RTC	RESERVE	AD3
GPI17	+3V	RESERVE	Y1
GPI18	+3V	THRM#	Y4
GPI19	+3V	RESERVE	AD10
GPO0	+3VS	RESERVE	AA3
GPO1	+3VS	SUSA#	AA2
GPO2	+3VS	SUSB#	AF2
GPO3	+3VS	SB_SUSST#	Y3
GPO4	+3VS	RESERVE	AB1
GPO5	+3V	RESERVE	AC7
GPO6	+3V	PCISTOP#	AF6
GPO7	+3V	RESERVE	P4
GPO16		SEE STRAP TABLE	AF11
GPO17		SEE STRAP TABLE	AE11
GPO18		SEE STRAP TABLE	AD11
GPO19		SEE STRAP TABLE	AC11
GPI08	+3V	MB ID0	C8
GPI09	+3V	MB ID1	B7
GPI010	+3V	KBD CS0	D7
GPI011	+3V	KBD CS1	A6
GPI012	+3V	RESERVE	A7
GPI013	+3V	RESERVE	B8
GPI014	+3V	CRT IN	D8
GPI015	+3V	MPCTACT#	C7
GPI020	+3V	RESERVE	U2
GPI021	+3V	RESERVE	V1
GPI022	+3V	FAN2 SPDCTR	B24
GPI023	+3V	LDTSTOP#	P26
GPI024	+3V	SPKR MUTE#	AE5
GPI025	+3V	FAN2 SPDCTR	AE6
GPI026	+3VS	RESERVE	AD1
GPI027	+3VS	RESERVE	AE1
GPI028	+3V	RESERVE	P25
GPI029	+3V	RESERVE	P24
GPI030	+3V	FAN1 SPDCTR	AD6
GPI031	+3V	MINIPCI PD	AC6

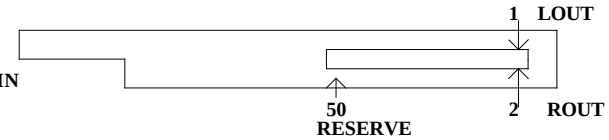


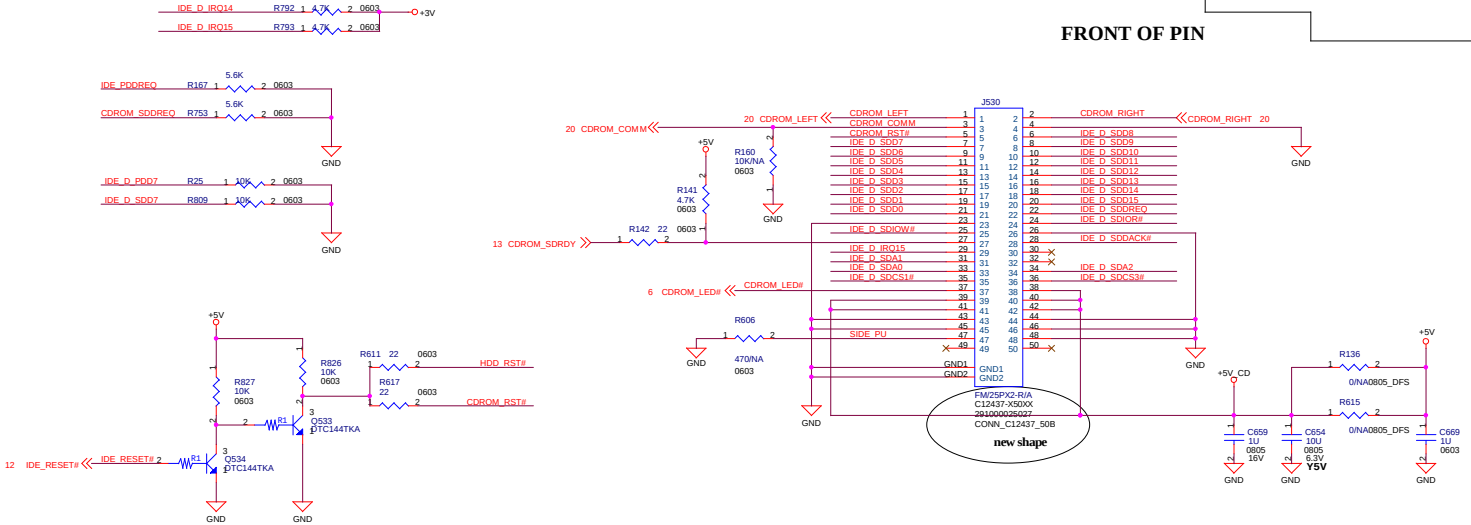
HDD CONNECTOR





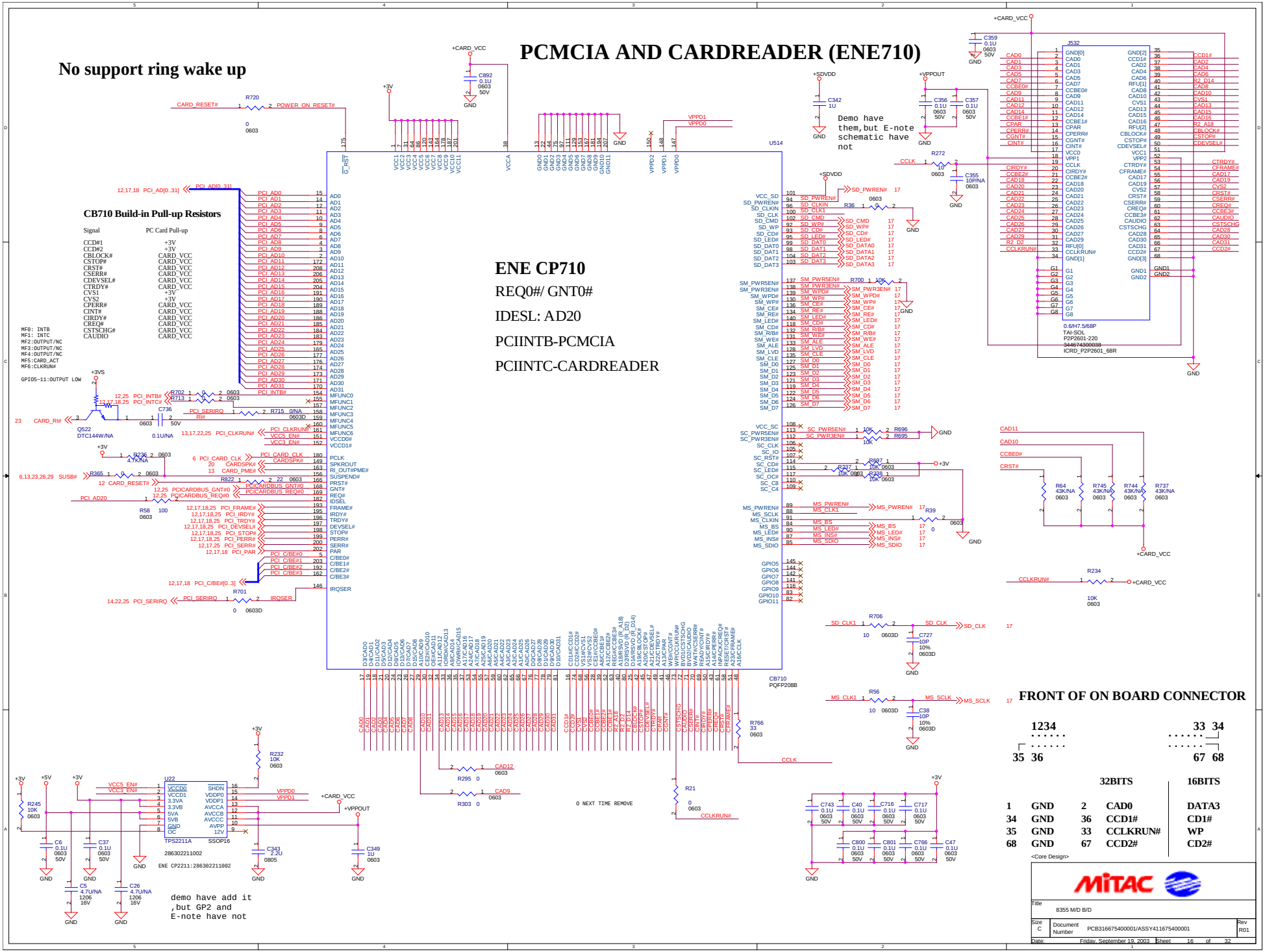
CDROM CONNECTOR



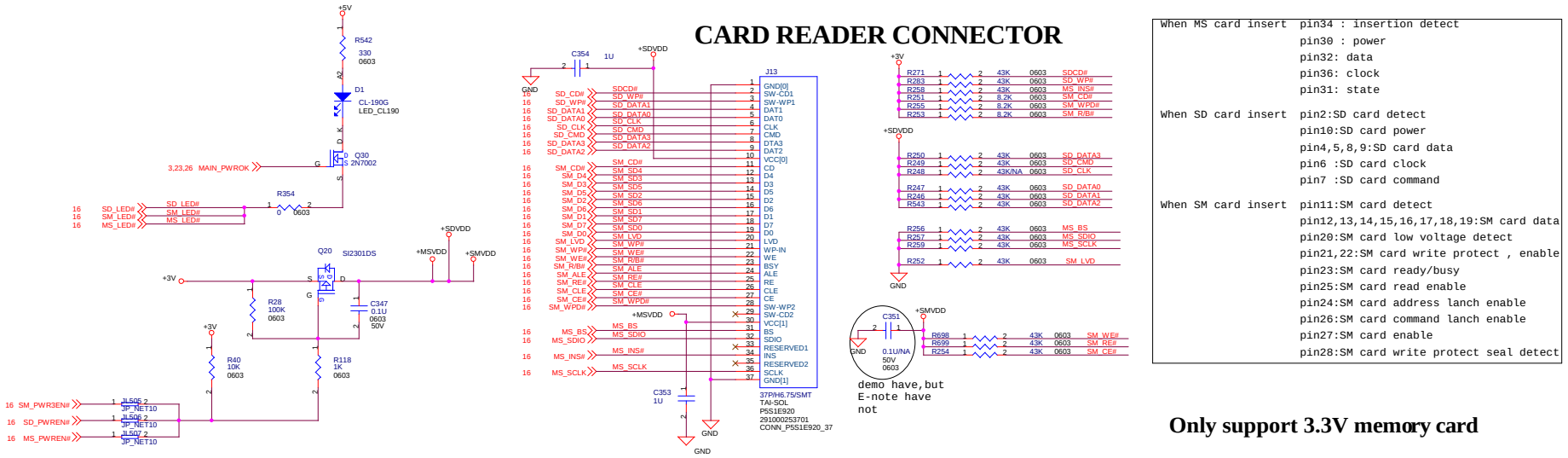


PCMCIA AND CARDREADER (ENE710)

No support ring wake up



CARD READER CONNECTOR

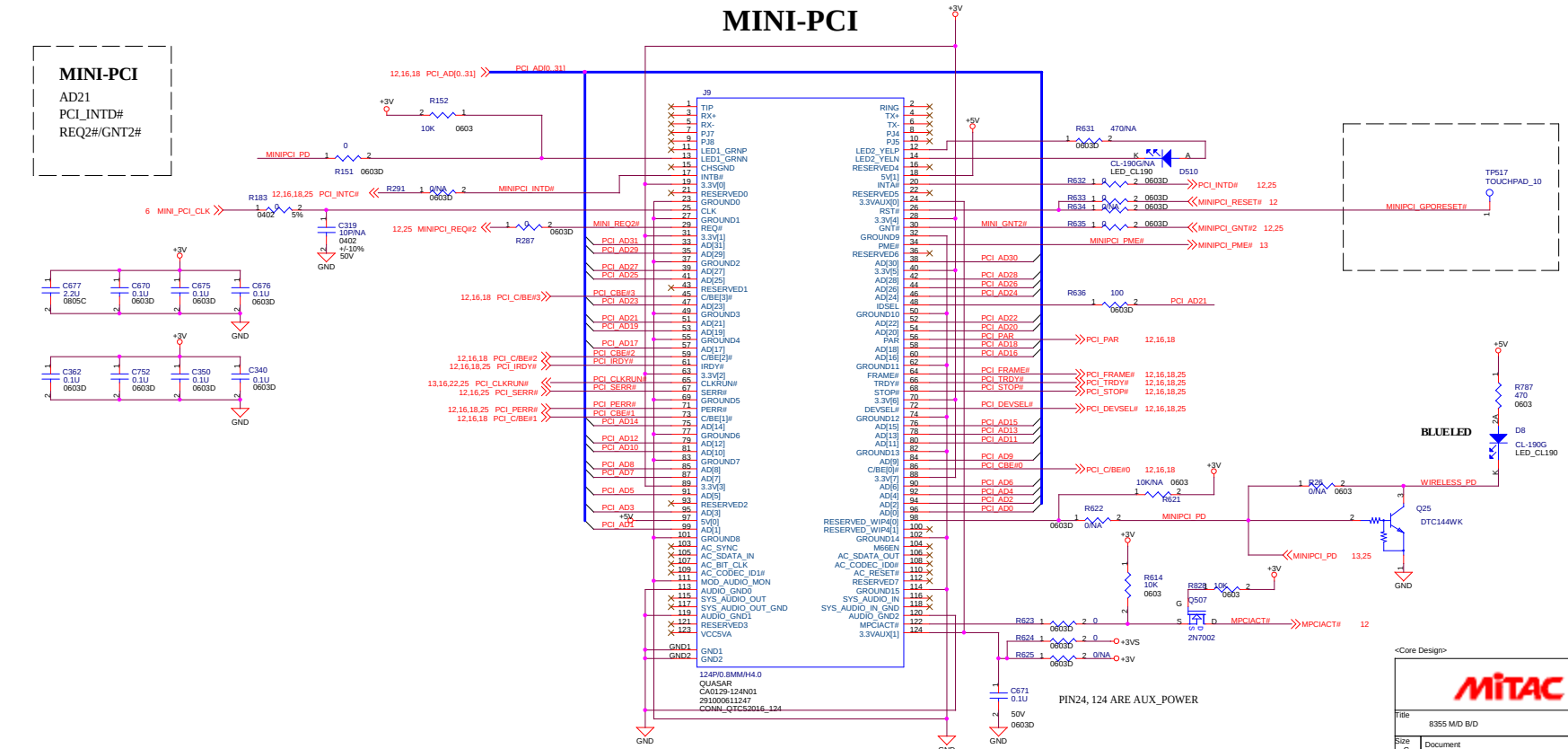


When MS card insert	pin34 : insertion detect
	pin30 : power
	pin32: data
	pin36: clock
	pin31: state
When SD card insert	pin2:SD card detect
	pin10:SD card power
	pin4,5,8,9:SD card data
	pin6 :SD card clock
	pin7 :SD card command
When SM card insert	pin11:SM card detect
	pin12,13,14,15,16,17,18,19:SM card data
	pin20:SM card low voltage detect
	pin21,22:SM card write protect , enable
	pin23:SM card ready/busy
	pin25:SM card read enable
	pin24:SM card address lanch enable
	pin26:SM card command lanch enable
	pin27:SM card enable
	pin28:SM card write protect seal detect

Only support 3.3V memory card

MINI-PCI

MINI-PCI
AD21
PCI_INTD#
REQ2#/GNT2#



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MiTAC

Title: 8355 M/D B/D

Size: C | Document Number: PCB316675400001/ASSY411675400001 | Rev: R01

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<core_design_block_end />

IEEE139- VT6307L

1394
REQ3
GNT3
INTC

ALL Capacator must close to power pin

VT6307L

pin52: 1 bus manager, 0 no bus manager
pin46: 1 enable 2-wire i2c eeprom , 0 4-wire i2c eeprom
pin48: 1eeprom fast mode , 0 disable
pin47: 1 card bus mode , 0 disable

default high
default low
default low
default low

mode1 0 internal pull down

00 normal
01 phy test
10 link test
11 watch mode

The length TPA0P and TPA0N must be the same.Also,TPB0P and TPB0N must be the same.Both pair need to be as close the same length as possible.

Title	8355 M/D B/D		
Size C	Document Number	PCB316675400001/ASSY411675400001	Rev R01
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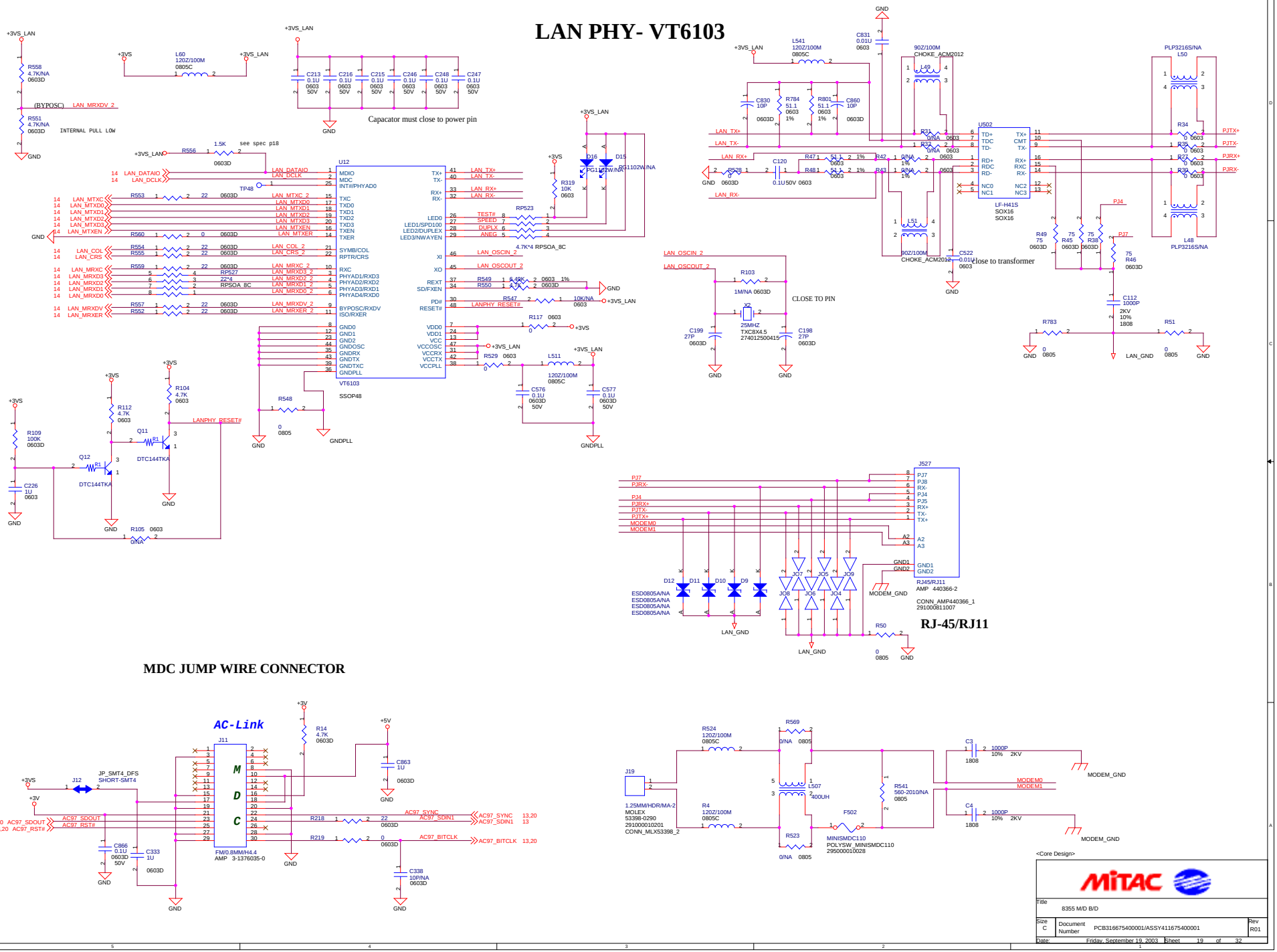
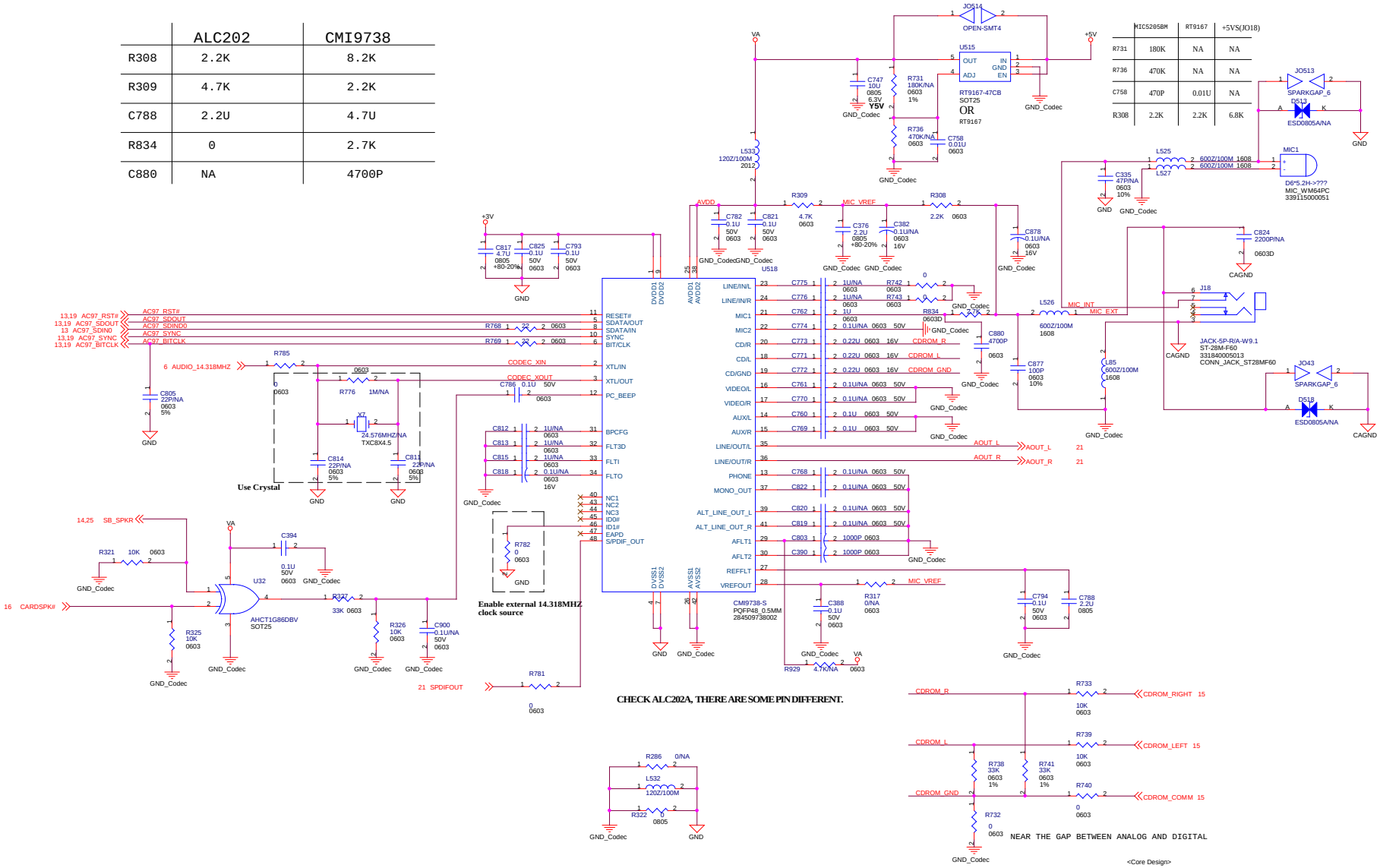
LAN PHY- VT6103



AUDIO CODEC(CMI9738)

	ALC202	CMI9738
R308	2.2K	8.2K
R309	4.7K	2.2K
C788	2.2U	4.7U
R834	0	2.7K
C880	NA	4700P



	MIC5205BM	RT9167	+5VS(JO18)
R731	180K	NA	NA
R736	470K	NA	NA
C758	470P	0.01U	NA
R308	2.2K	2.2K	6.8K

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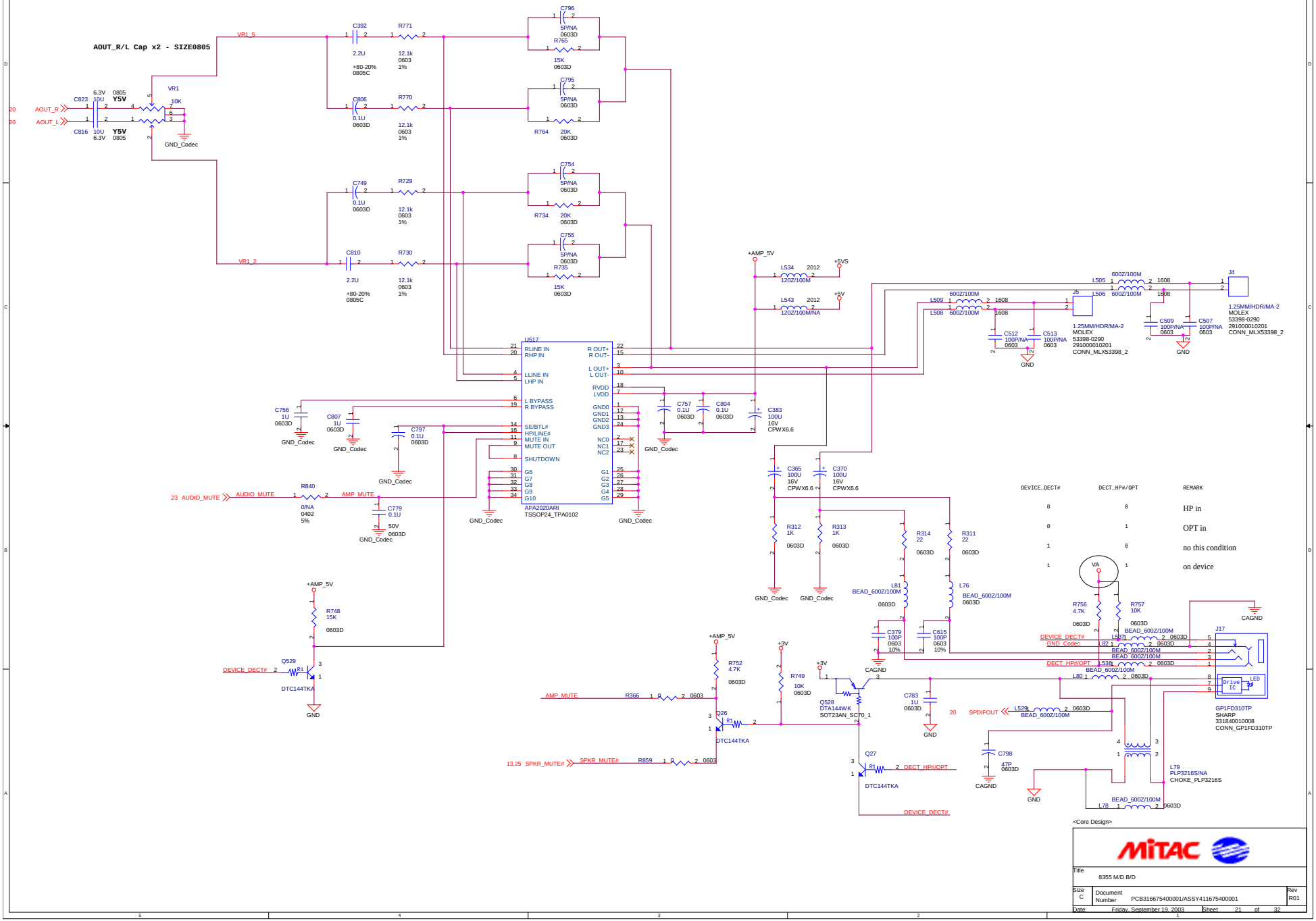
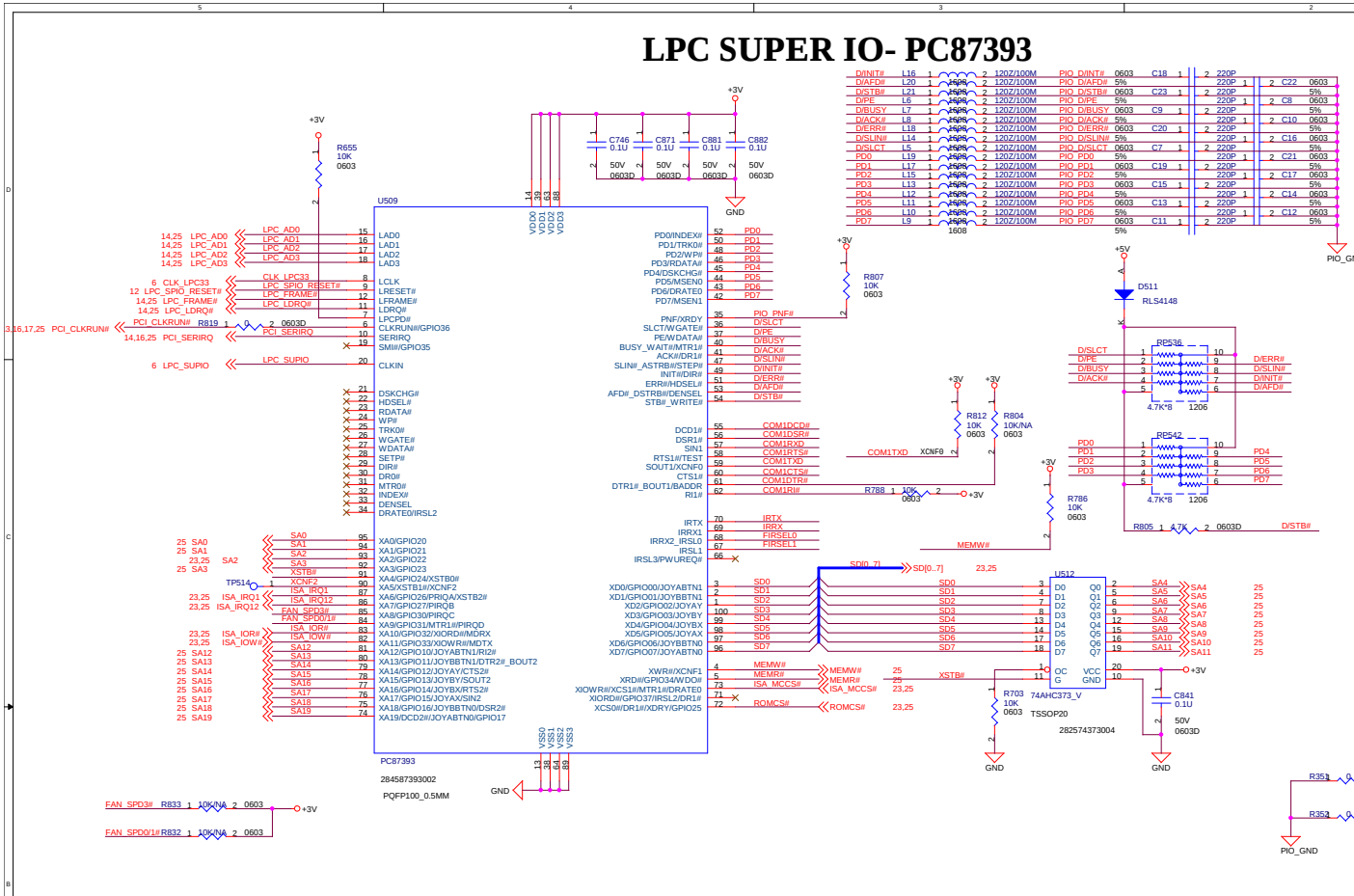
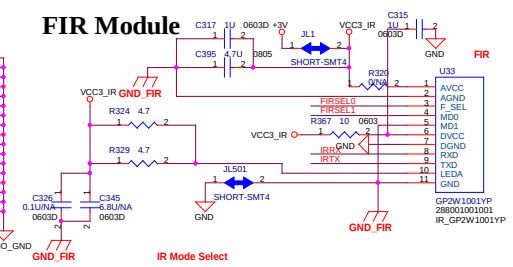
AUDIO AMPLIFIER - TPA0202



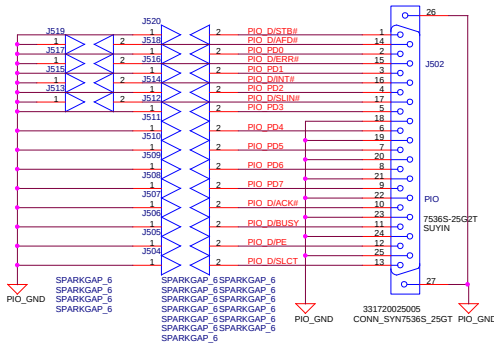
LPC SUPER IO- PC87393



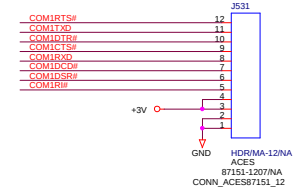
FIR Module



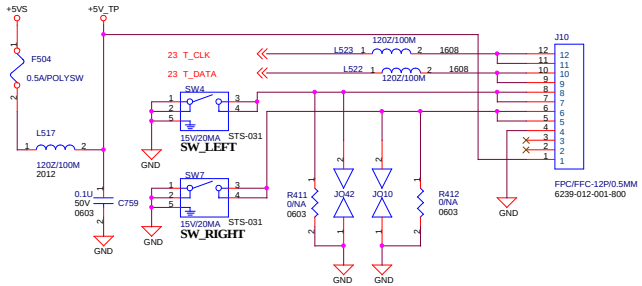
PIO



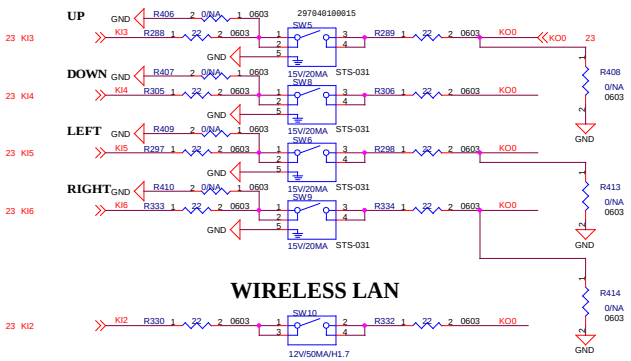
SIO



Touch PAD Connector



SCROLL BUTTON AND WIRELESS ENABLE BUTTON



STRAP OPTION

XCNF2	XCNF1	XCNF0	FUNCTIONALITY
X	0	0	NO BIOS
X	0	1	NORMAL MODE , XRDYDISABLE
0	1	0	LATCH MODE ,XA12-19, XRDY ENABLE
1	1	0	LATCH MODE , GPIO 10-17 , XRDY ENABLE
0	1	1	LATCH MODE , XA12-19, XRDY DISABLE
1	1	1	LATCH MODE , GPIO 10-17 ,XRDY DISABLE

BASE ADDRESS SELECT

R724	INDEX REGISTER	DATA REGISTER
MOUNTED	4EH	4FH
OPEN	2EH	2FH

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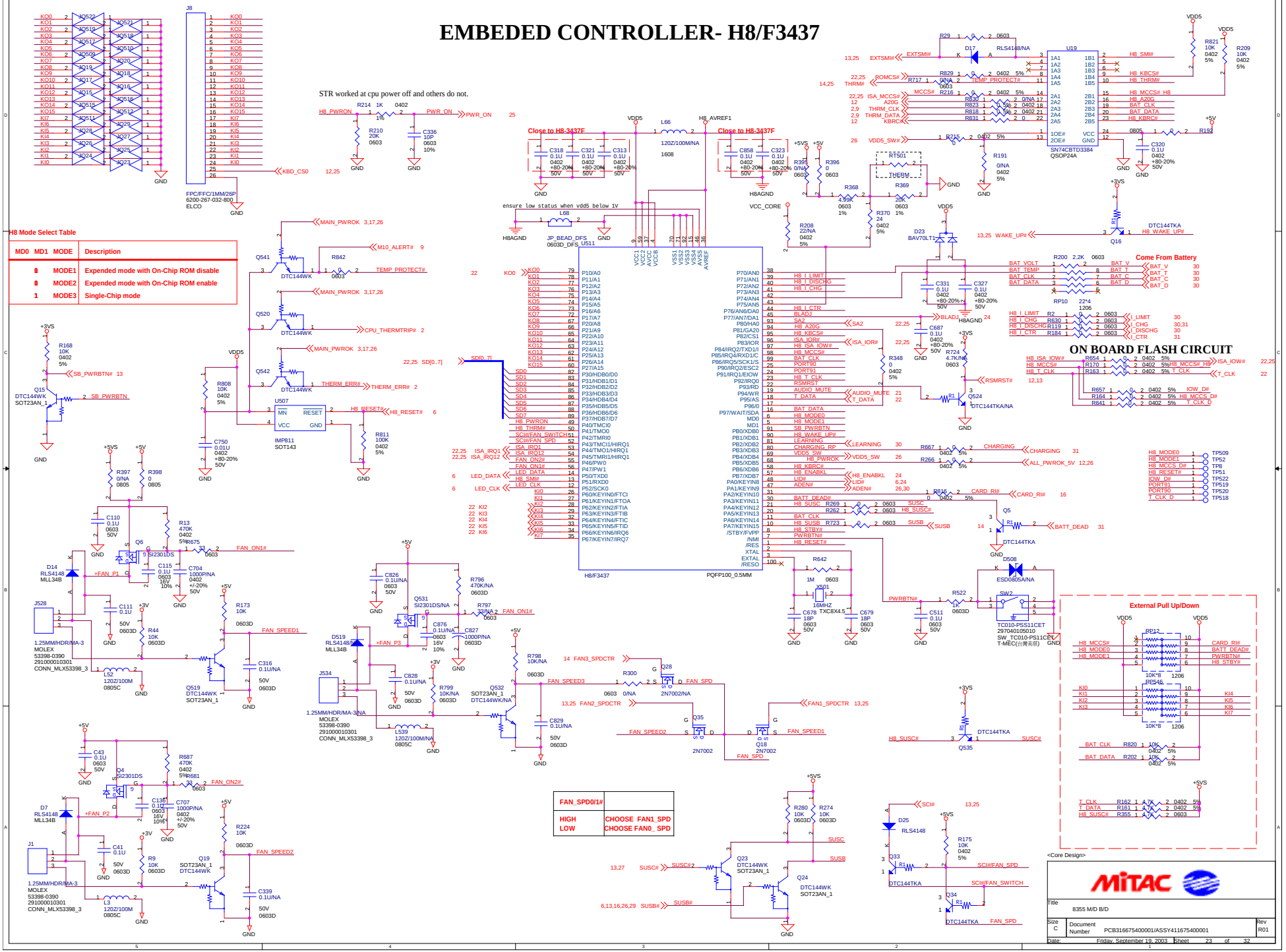
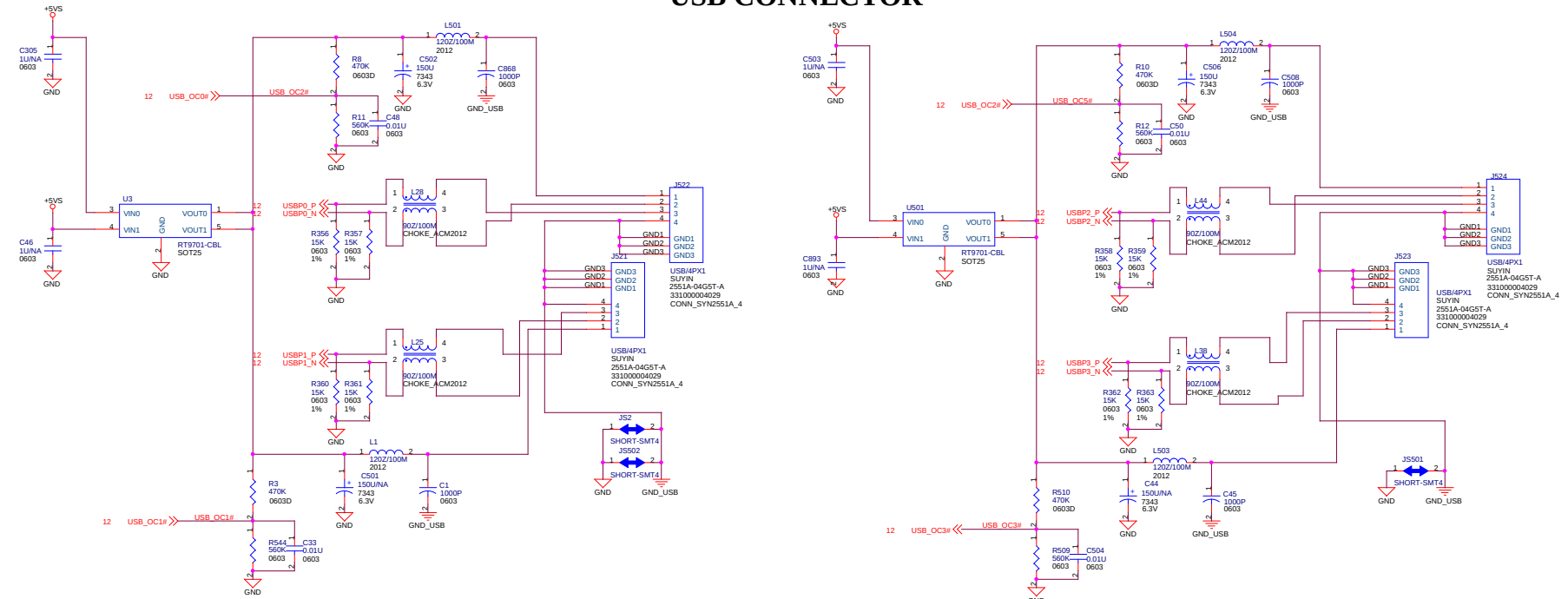
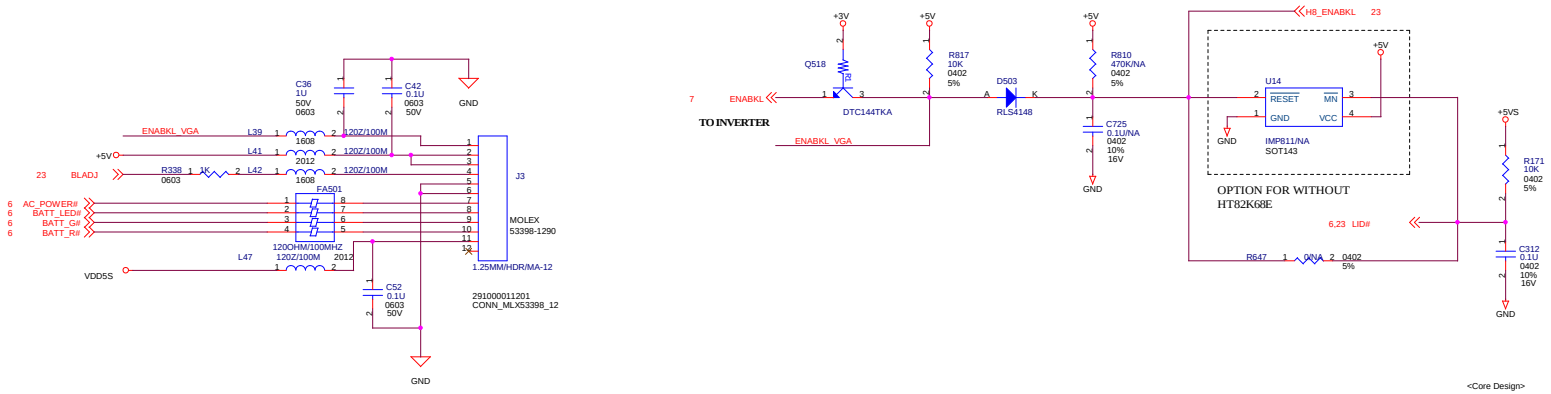
EMBEDED CONTROLLER- H8/F3437



USB CONNECTOR



BACKLITE CONNECTOR



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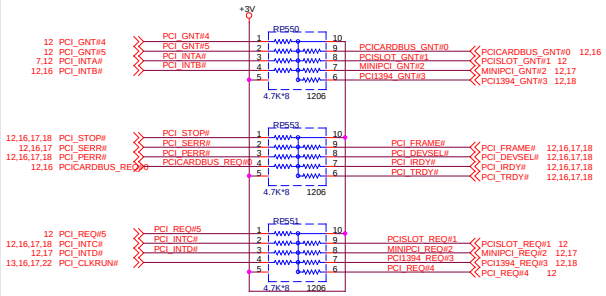
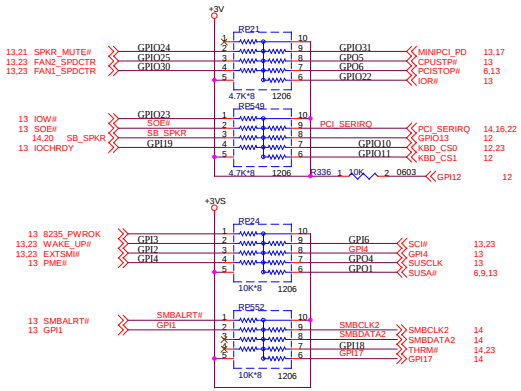
PULL HIGH AND BIOS

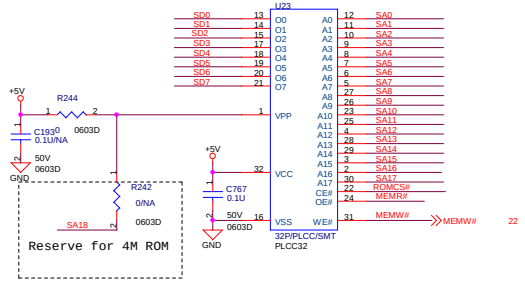
PCI PULL HIGH



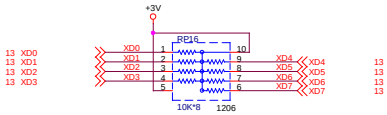
SB GPIO PULL HIGH



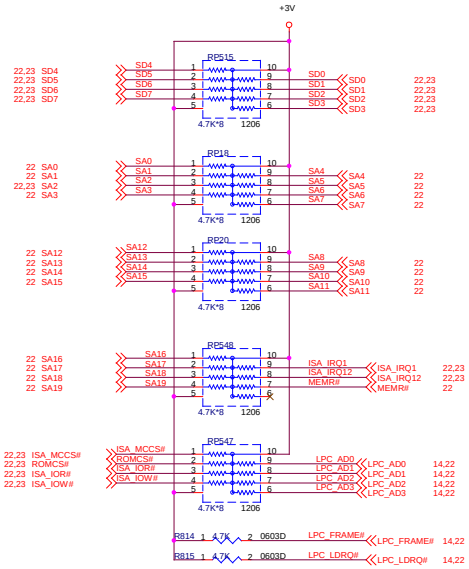
SYSTEM BIOS

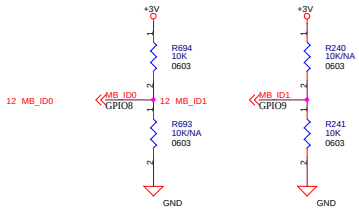


SB X-BUS PULL HIGH

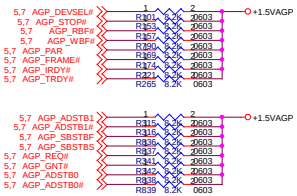


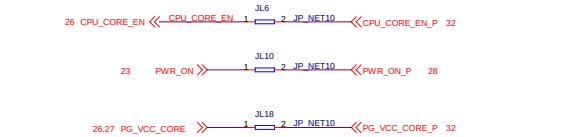
ISA AND LPC PULL HIGH

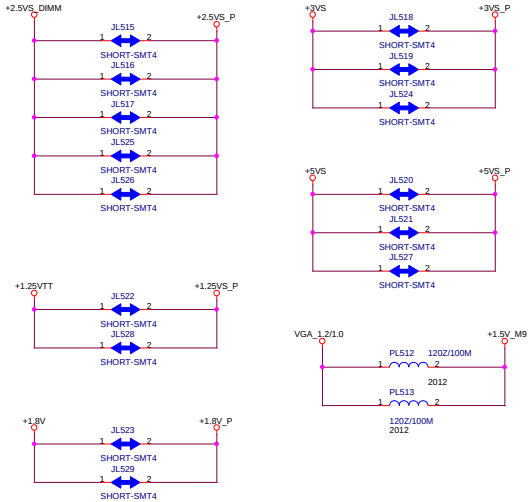




AGP PULL HIGH







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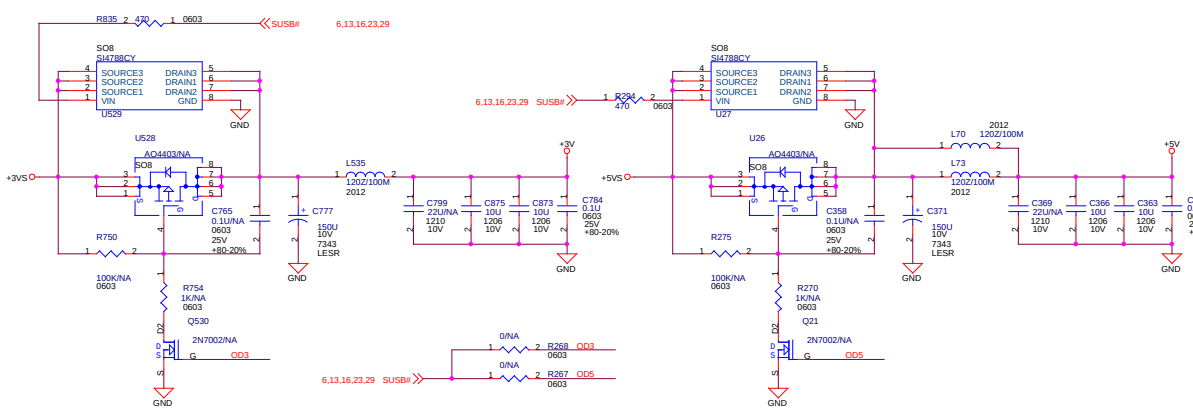
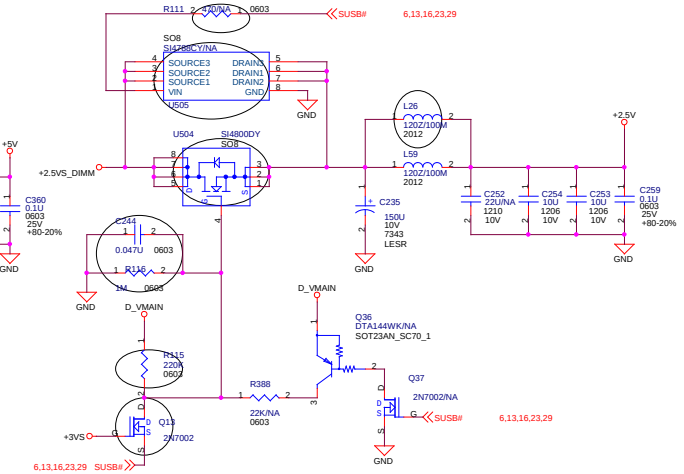
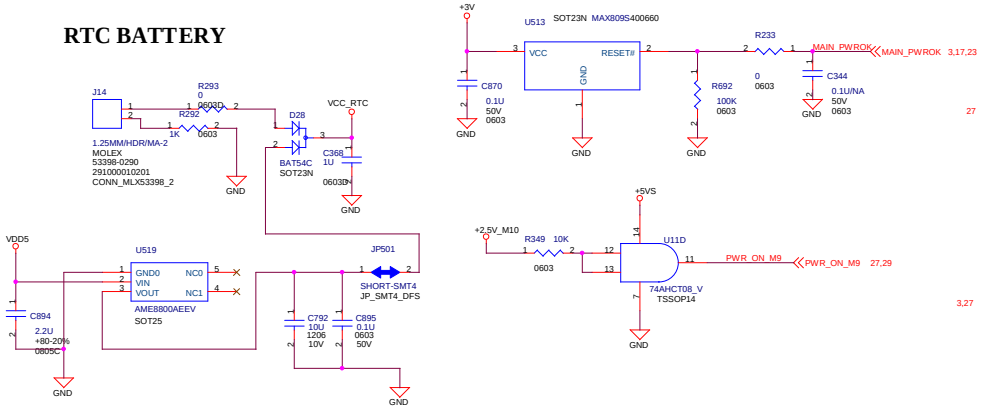
POWER PERPHERIAL

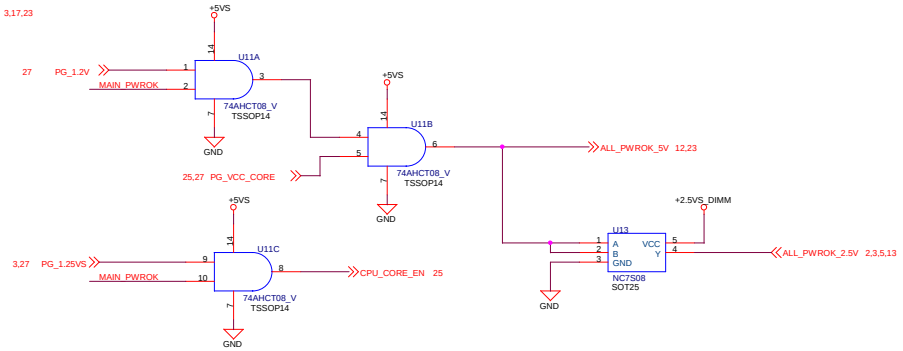
AUX switch to MAIN



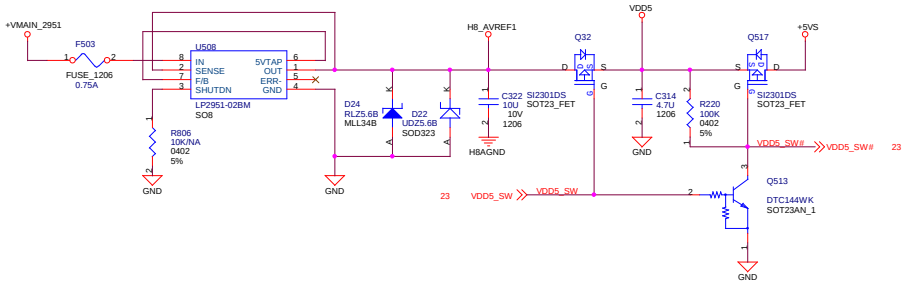


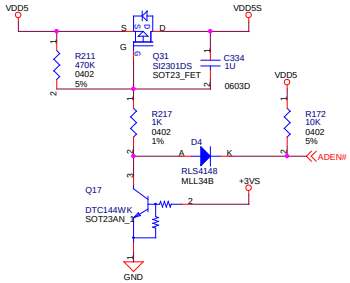
RTC BATTERY



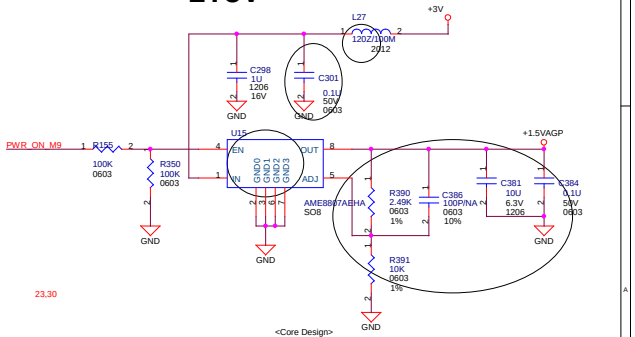


VDD5





+1.5V



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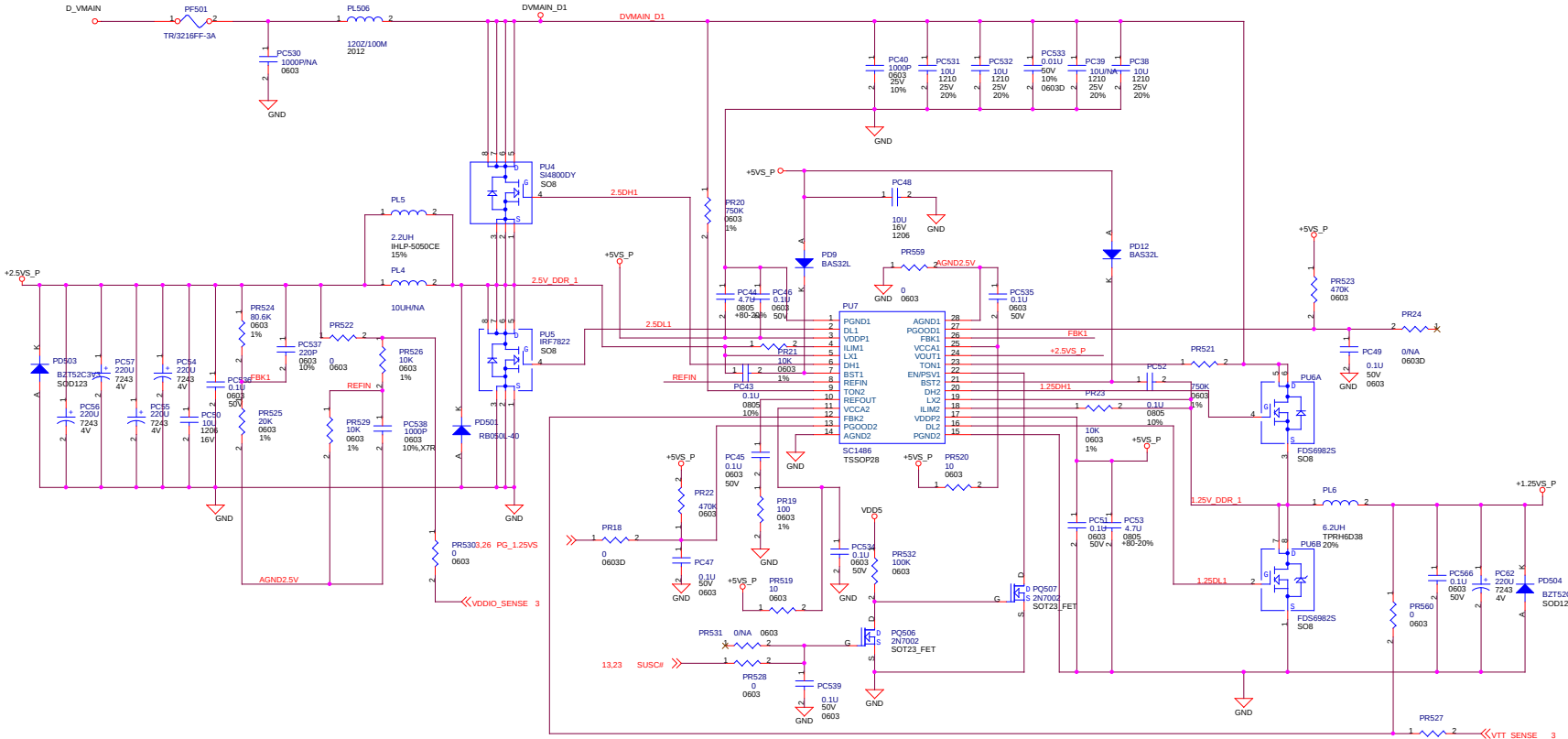
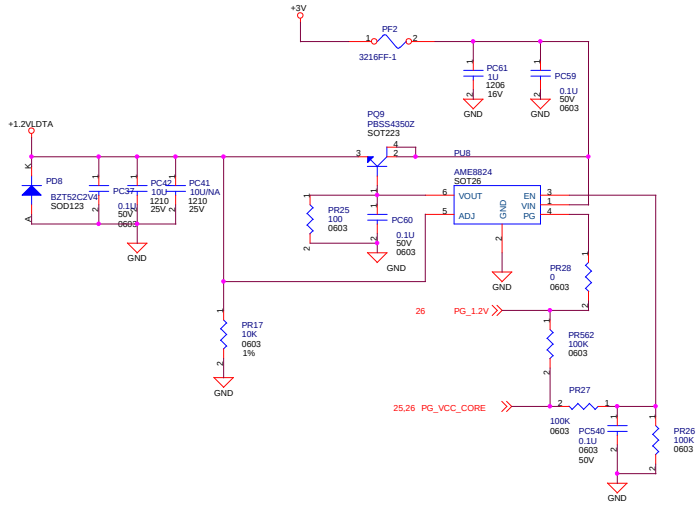
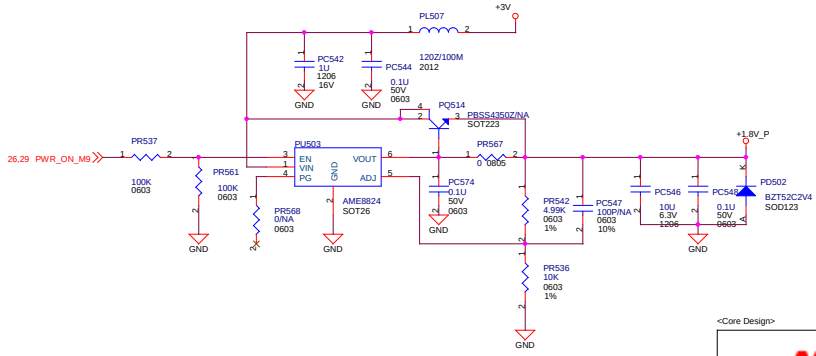
+2.5VS&+1.25VS&+1.8V&+1.2V



+1.2V



+1.8V



<Core Design>

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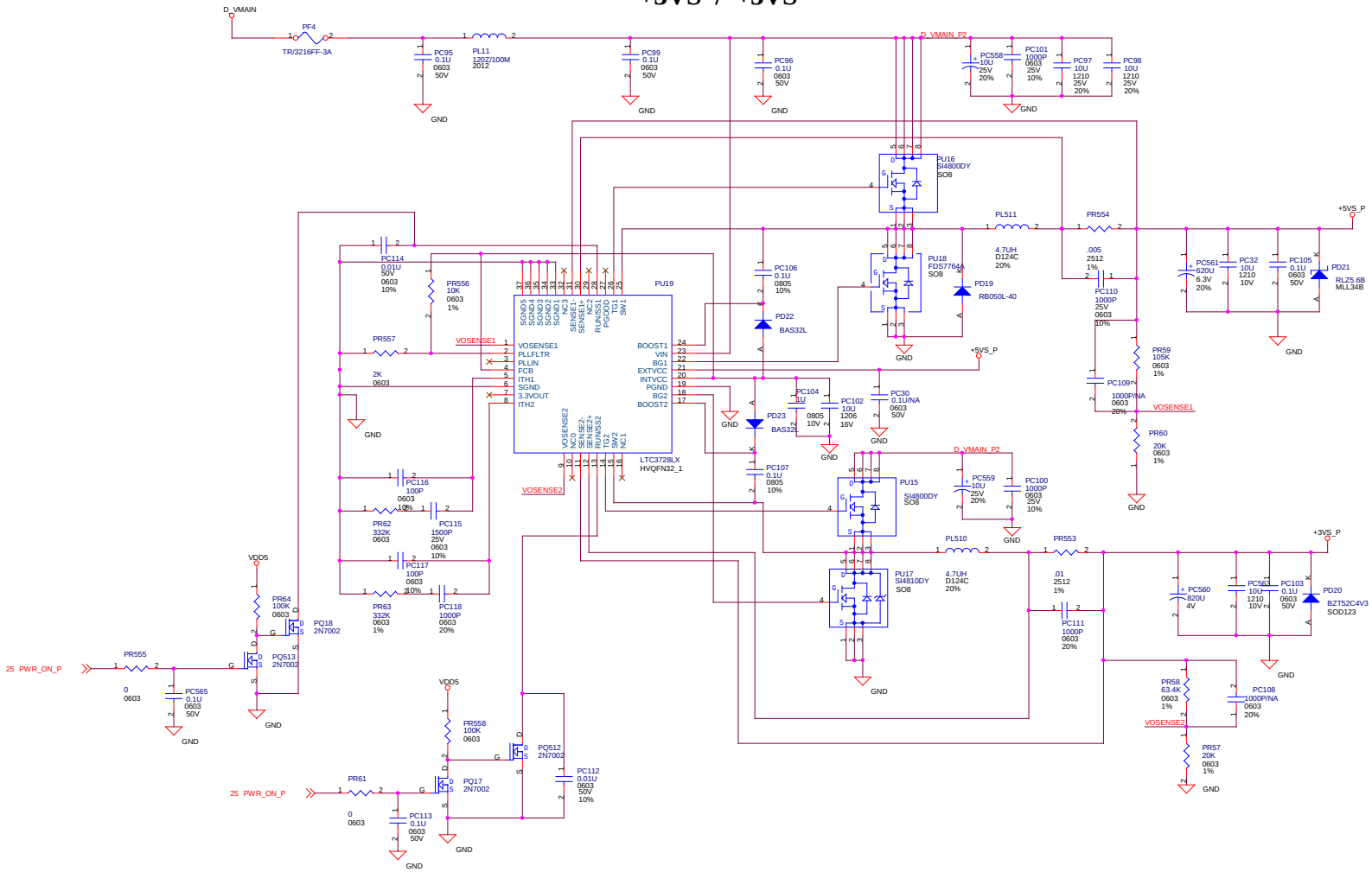
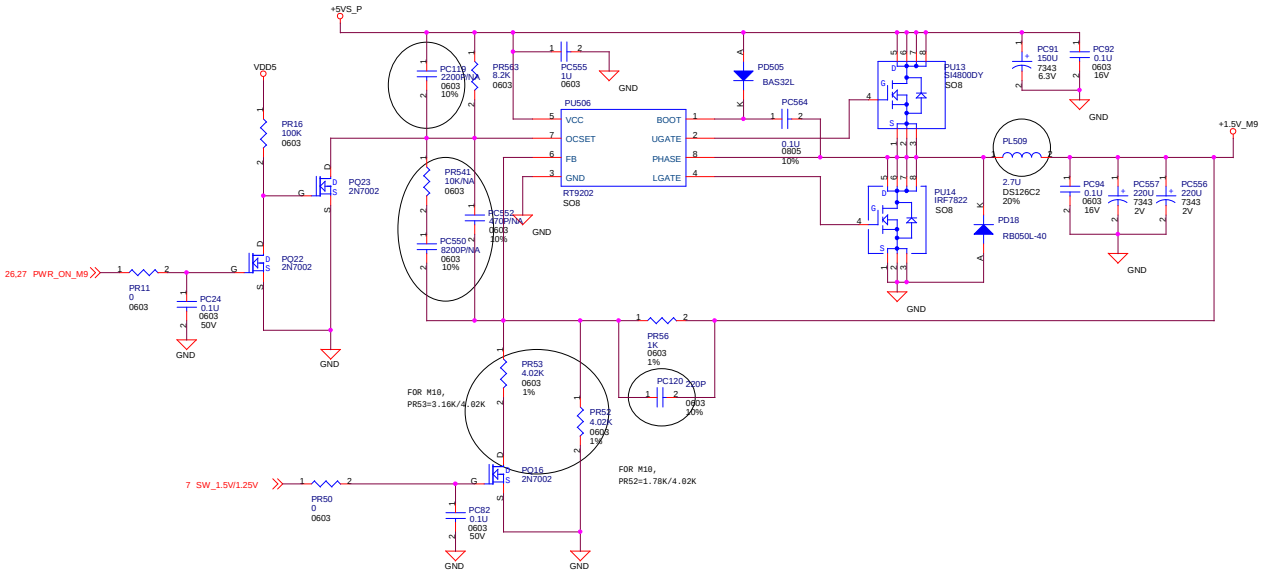
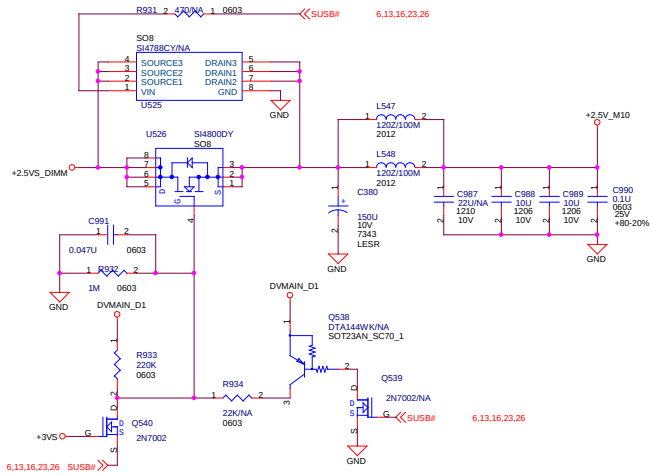
+3VS / +5VS



FOR M10 +1.2V&+1.0V



FOR M10 +2.5V(Backup)



<Core Design>

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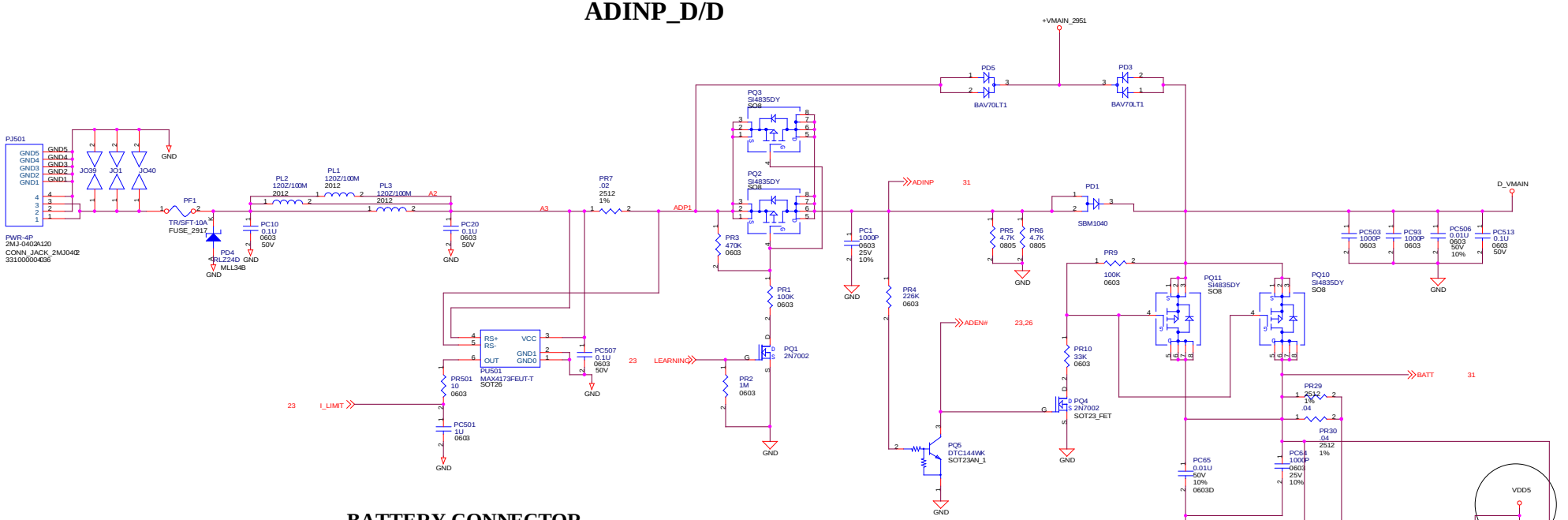
ADINP_D/D



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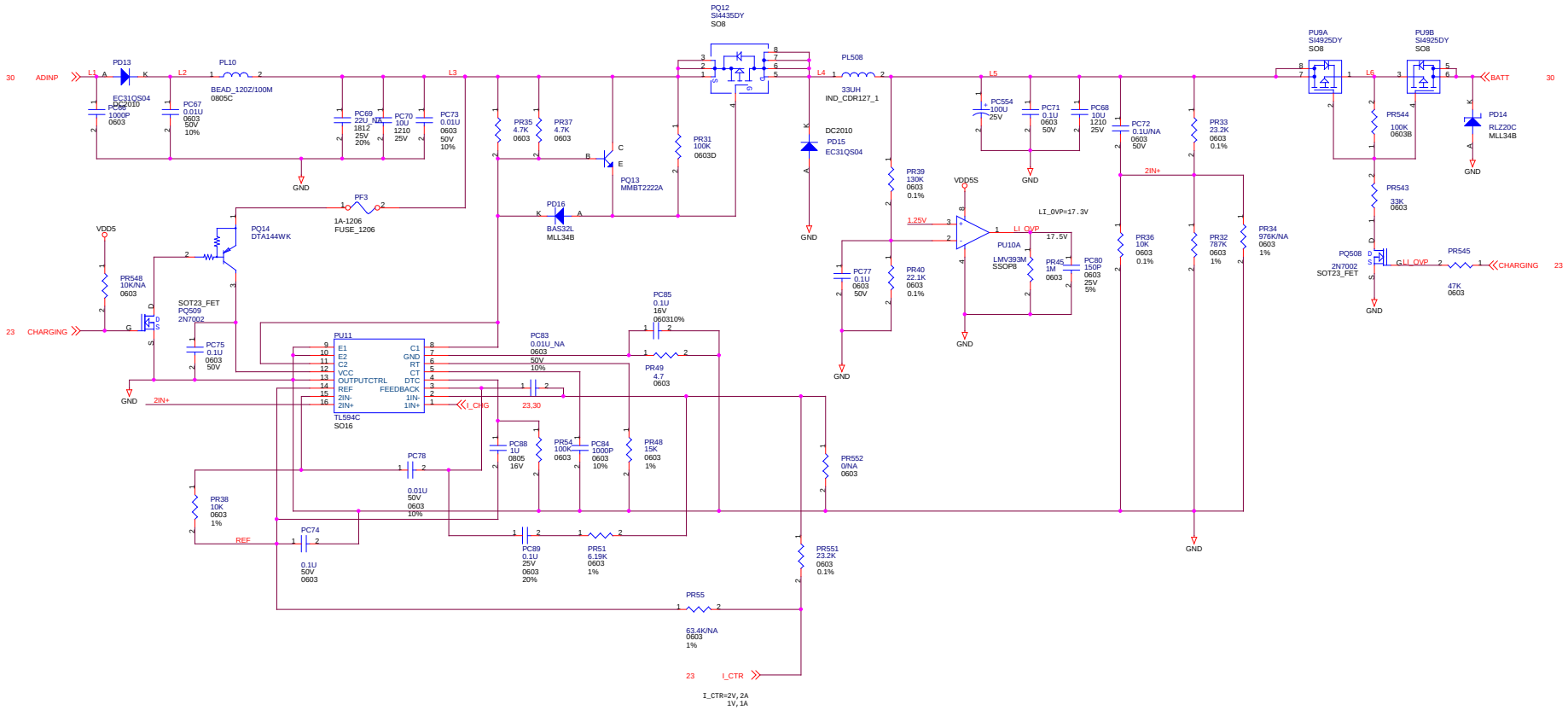
CHARGER



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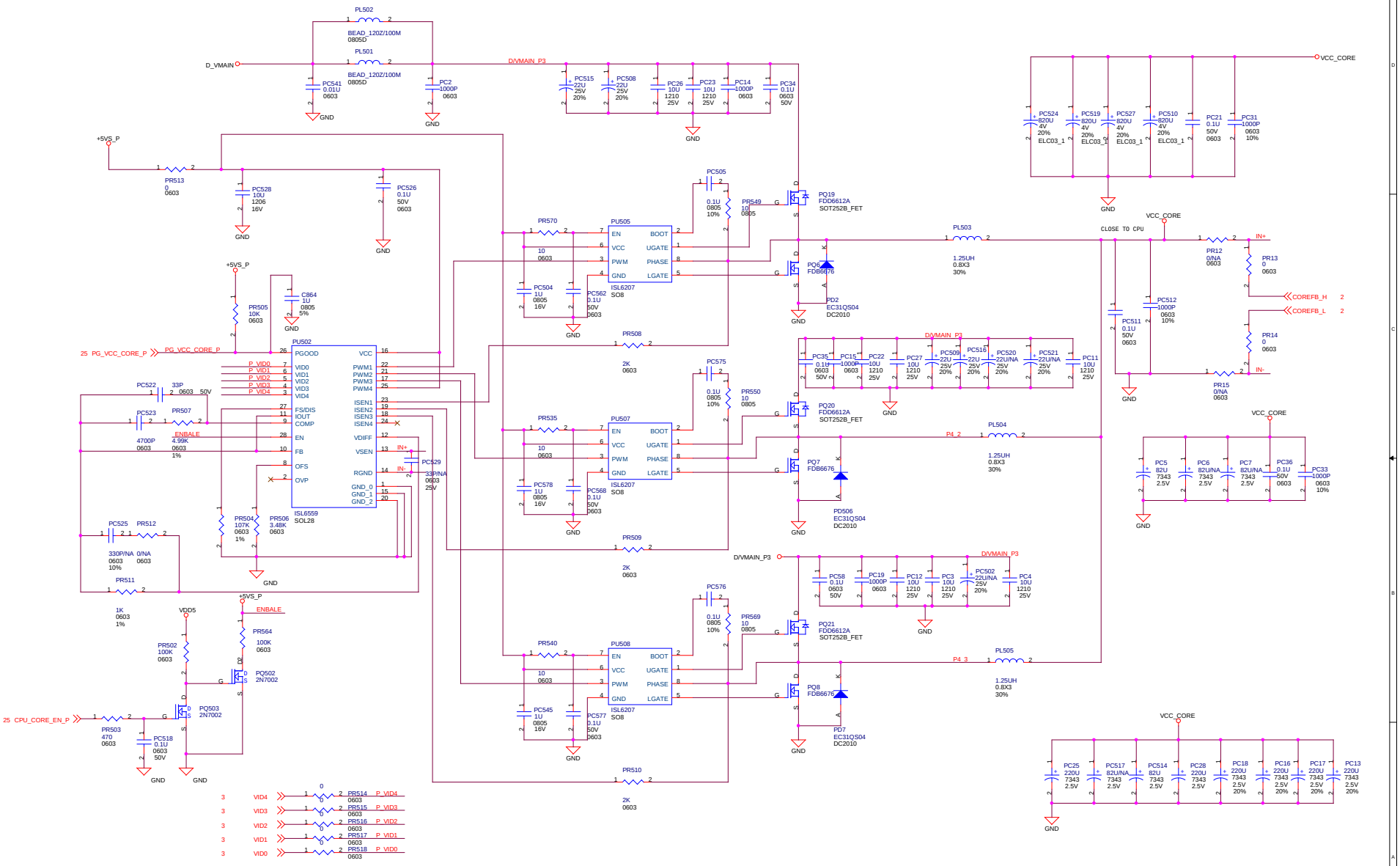
VCC_CORE



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Reference Material

- **AMD Athlon™ 64** ..... *AMD. INC*
- **VIA K8T800M VT8385 North Bridge** ..... *VIA. INC*
- **VIA VT8235 South Bridge** ..... *VIA. INC*
- **Frequency Generator ICS950403** ..... *ICS. INC*
- **ENE CB710 PC Card Interface Controller** ..... *TI. INC*
- **8355 Engineer Hardware Specification** ..... *Technology.Corp/MiTAC*

SERVICE MANUAL FOR 8355

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