SERVICE MANUAL FOR

8081

BY: Sissel Diao

Repair Technology Research Department /EDVD

Jul. 2003

MiTAC

8081 N/B Maintenance

Contents

1. Hardware Engineering Specification 4

1.1 Introduction 4

1.2 Hardware System 8

1.3 Other Functions 28

1.4 Peripheral Components 34

1.5 Power Management 36

1.6 Appendix 1 : Intel 82801DBM ICH4-M GPIO Definitions 39

1.7 Appendix 2 : MiTAC 8081 Product Specification 40

2. System View and Disassembly 41

2.1 System View 41

2.2 System Disassembly 44

3. Definition & Location of Connectors / Switches 69

3.1 Mother Board 69

3.2 DC to DC Board 71

4. Definition & Location of Major Components 72

4.1 Mother Board 72

5. Pin Description of Major Component 74

5.1 Intel Banias Pentium M Processor 74

8081 N/B Maintenance

Contents

5.2 Intel 82855GM Memory Controller Hub (GMCH) 78
5.3 Intel 82801DBM I/O Controller Hub Mobile (ICH4-M) 84

6. System Block Diagram **92**

7. Maintenance Diagnostics **93**

7.1 Introduction 93
7.2 Error Codes 94
7.3 Maintenance Diagnostics 96

8. Trouble Shooting **97**

8.1 No Power 98
8.2 No Display 103
8.3 VGA Controller Failure LCD No Display 106
8.4 External Monitor No Display 108
8.5 Memory Test Error 110
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error 112
8.7 Hard Driver Test Error 114
8.8 CD-ROM Driver Test Error 116
8.9 USB Port Test Error 118
8.10 Audio Failure 120
8.11 LAN Test Error 123
8.12 PC Card & 1394 Socket Failure 125

8081 N/B Maintenance

Contents

9. Spare Parts List …….. 127

10. System Exploded Views …… 139

11. Circuit Diagram …… 140

12. Reference Material ……... 171

8081 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8081 portable notebook computer system.

1.1.2 System Overview

The MiTAC 8081 model is designed for Intel Banias/Dothan processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.3GHz~1.7GHz CPU/Dothan CPU with 1.8GHz or above.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Wireless on/off indicator, Battery status indicator, CD-ROM, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK. It also equipped with LAN, 56K Fax MODEM, 4 USB port, 3D stereo audio functions, and audio line out, external microphone in function.

The memory subsystem supports one expansion DDR SDRAM slot with unbuffered PC1600/PC2100 DDR-SDRAM, and 16Mx16 DDR RAM on board 256MB.

8081 N/B Maintenance

The Montara-GM GMCH Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Intel Hub interface Technology connecting with Intel 82801DBM ICH4-M.

The Intel ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Intel Hub interface technology.

The VIA VT6105LOM “Rhine III” Ethernet controller is a cutting edge, feature-rich, and cost-competitive single ASIC chip solution for PC “LAN On Motherboard” applications or Low Cost NIC applications. The 6105LOM eases server processor utilization by optimizing throughput between NIC and PCI bus allowing data transfers of up to at 200Mbps in full duplex mode, without using the system CPU. The VT6105LOM contains advanced power management feature for low power consumption including Wake On LAN (WOL) and is implemented using a low power 0.22-micron design.

The R5C551 is the single chip solution offering single PCI bus-PC Card Bridge. The R5C551 is compliant with the latest specification in both PC card and IEEE 1394. The R5C551 has two PCI functions compliant, the PC Card interface and the IEEE 1394 interface. The PC Card controller of the R5C551 is compliant with PC Card Standard Release 7.0. The R5C551 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports any combination of 16-bit (Card-16), and CardBus (Card-32) PC Cards in one socket, powered at 5V or 3.3V, as required. The R5C551 provides the IEEE1394 OHCI-Link and two ports the IEEE1394 PHY that are compliant with the IEEE1394-1995, IEEE1394a-2000 and the latest 1394 OHCI specifications. The R5C551 data rate is capable of 100, 200, and 400Mbits per second.The R5C551 is compliant with the latest PCI Bus Power Management Specification, and provides several low-power modes that enable the host power system to further reduce power consumption.

8081 N/B Maintenance

The NS PC87393 LPC Super I/O device is targeted for a wide range of portable applications. PC99 and ACPI compliant, it also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serialize for Parallel IRQs and an enhanced WATCHDOG timer.

The NS PC87393 Super I/O controller integrates the standard PC I/O functions: LPC bus interface, X-Bus Extension for read and write operations, floppy disk interface and one EPP/ECP capable parallel port. Like all LPC Super I/O devices, the PC87393 offers a single-chip solution to the most commonly used PC I/O peripherals to provide for the increasing number of multimedia application.

CMI9738-S is a 4CH AC97 CODEC, applicable for major MB chipsets of Intel, VIA, Ali, and SIS. CMI9738-S is ideal for PC2001-compliant desktops, notebooks, and home entertainment PCs where high-quality audio is a must. The specially-designed 4CH hardware architecture of CMI9738-S allows multi-channel south bridge to playback 4CH audio. As to the cost concern, CMI9738-S integrates the earphone buffer, analog CD differential interface, and analog switch for rear channel audio to Line-in for traditional 3 jacks audio port to output 4 channels audio. CMI9738-S also has built-in PLL to save additional crystal. Last but not least, CMI9738-S provides HRTF 3D audio which interface compatible with EAX™/ A3D™/DirectSound3D™. In addition, it provides Sensaura™ 3D audio option. In that regard, the audio quality of CMI9738-S is fabulous beyond general expectation.

The H8/F3437 is a high performance micro controller with a fast H8/300 CPU core and a set of on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.1.3 System Parts

- **CPU :** Intel Banias/Dothan processors in Micro-FCPGA package
- **Synthesizer :** ICS950810
- **North Bridge :** Montara-GM GMCH
- **South Bridge :** ICH4-M
- **Super I/O controller :** NS PC87393
- **Keyboard System :** Hitachi H8/F3437 Universal Controller
- **FAX/MODEM :** Billonton MDC56S-I 56Kbps Fax Modem
- **LAN single chip :** VT6105LOM
- **PCMCIA controller :** R5C551
- **AC'97 Codec :** CMI9738-S
- **Thermal sensor :** ADM1021A
- **System Flash Memory (BIOS)**

1.2 Hardware System

1.2.1 CPU Module

- Intel Banias/Dothan Processors with 478 pins Micro-FCPGA package .
- The first Intel mobile processor with the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).
- The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.
- Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.
- Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Synthesizer

- System frequency synthesizer: ICS950810
- Programmable output frequency, divider ratios, output rise/fall time, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watchdog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Use external 14.318MHz crystal.

1.2.3 Montara-GM GMCH IGUI 3D Graphic DDR/SDR Chipset

Montara-GM GMCH IGUI Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and Intel®' I/O Hub architecture INTEL 82801DBM ICH4-M.

Montara-GM GMCH Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Banias processors. Montara-GM GMCH provides a 12-deep In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Banias series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition

to integrated GUI, Montara-GM GMCH also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara-GM GMCH and INTEL 82801DBM ICH4-Mtogether. Intel®' I/O Hub architecture is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in INTEL 82801DBM ICH4-M to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from Montara-GM GMCH, and the Multi-threaded I/O Link Encoder/Decoder in Montara-GM GMCH to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from Intel 82801DBM ICH4-M.

An Unified Memory Controller supporting DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The Montara-GM GMCH adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

Features :

- **Processor/Host Bus Support**
  - Intel® Banias processor
  - 2X Address, 4X data
  - Support host bus Dynamic Bus Inversion (DBI)
  - Supports system bus at 400MT/s (100 MHz)
  - Supports 64-bit host bus addressing
  - 8-deep In-Order-Queue

8081 N/B Maintenance

- AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05V)
- Supports Enhanced Intel® SpeedStep™ Technology (EIST) and Geyserville III
- Support for DPWR# signal to Banias processor for PSB power management

- **Memory System**

- Directly supports one DDR channel, 64-bts wide (72-b with ECC).
- Supports 200-MHz and 266-MHz DDR devices with max of 2 Double-Sided SO-DIMMs(4 rows populated) with unbuffered PC1600/PC2100 DDR(with ECC).
- Supports 128-Mb, 256-Mb and 512-Mbit technologies providing maximum capacity of 1-GB with only x 16 devices.
- All supported devices have 4 banks.
- Supports up to 16 simultaneous open pages.
- Supports page sizes of 2KB, 4KB, 8KB, and 16KB. Page size is individually selected for every row.
- UMA support only.

- **System interrupt**

- Supports 8259 and Processor System Bus interrupt delivery mechanism
- Supports interrupts signaled as upstream Memory Writes from PCI and Hub interface
- MSI sent to the CPU through the system Bus
- From IOxAPIC in ICH4-M
- Provides redirection for upstream interrupts to the System Bus
- Video Stream Decoder
- Improved HW Motion Compensation for MPEG2
- All format decoder (18 ATSC formats) supported
- Dynamic Bob and Weave support for Video Streams

8081 N/B Maintenance

- Software DVD at 60 fields/second and 30 frames/second full screen
- Support for 720x480 pixel resolution DVD quality encoding at low CPU utilization
- Video Overlay
- Single high quality scalable overlay and second Sprite to support second overlay
- Multiple overlay functionality provided via Arithmetic Stretch Blt
- Direct YUV from Overlay to TV-out
- Independent Gamma Correction
- Independent Brightness / Contrast / Saturation
- Independent Tint / Hue support
- Destination Color keying
- Source Chromakeying
- Maximum source resolution of 1920x1080 pixels
- Maximum overlay clock of 133 MHz/200 MHz provides a pixel resolution up to 1600x1200@ 60Hz or 1280x 1024@ 85 Hz

Display

- Analog Display Support
- 350 MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor up to 1800 x1350@ 85 Hz.
- Accompanying I2C and DDC channels provided through multiplexed interface Hot-plug and display support
- Dual independent pipe with single display support Simultaneous: Same images and native display timings on each display device
- DVO (DVOB) support
- Digital video out port DVOB with 165-MHz dot clock on 12-bit interface

8081 N/B Maintenance

-- Variety of DVO devices channel
-- Compliant with DVI Specification 1.0, thereby providing support for a flat panel up to 2048x1536 pixel resolution, or digital CRT up to 1920x1080 pixel resolution

- Dedicated LFP (local flat panel) interface
  -- Single or dual channel LVDS panel support up to SXGA+ panel resolution with frequency range from 25MHz to 112MHz per channel
  -- SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  -- Supports data format of 18bpp
  -- Direct YUV from Overlay to TV-out
  -- LCD panel power sequencing compliant with SPWG timing specification
  -- Compliant with ANSI/TIA/EIA –644-1995 spec
  -- Integrated PWM interface for LCD backlight inverter control
  -- Bi-linear Panel fitting
- Tri-view support through LFP interface, DVO ports and CRT
- Internal Graphics Features
- Core Frequency
  -- Display Core frequency of 133MHz
  -- Render Core frequency of 133MHz
- 2D Graphics Engine
- Optimized 128 bit BLT engine
- Ten programmable and predefined monochrome patterns
- Alpha Stretch Blt (via 3D pipeline)
- Anti-aliased lines
- Hardware-based BLT Clipping & Scissoring
- 32-bit Alpha Blended cursor

8081 N/B Maintenance

- Programmable 64*64 3-color Transparent cursor
- Color Space Conversion
- 3 Operand Raster BLTs
- 8-bit, 16-bit, and 32-bit color
- ROP support
- DIB translation and Linear/Title addressing
- 3D Graphics Engine
- 3D Setup and Render Engine
- Viewpoint Transform and Perspective Divide
- Triangle Lists, Strips and Fans support
- Indexed Vertex and Flexible Vertex formats
- Pixel accurate Fast Scissoring and Clipping operation
- Back-face Culling support
- DirectX™ and OGL Pixelization rules
- Anti-Aliased Lines support
- Sprite Points support
- Zone Rendering
- Provides the highest sustained fill rate performance in 32-bit color and 24-bit W mode
- High quality performance Texture Engine
- 266 MegaTexel/speak performance
- Per Pixel Perspective corrected Texture Mapping
- Single Pass Texture Composting (Multi-Texture) at rate
- Enhanced Texture Blending functions

8081 N/B Maintenance

- Twelve Level of Detail MIP Map Sizes from 1x1 to 2Kx2K
- Numerous Texture formats including 32-bit RGBA
- Alpha and Luminance Maps
- Texture Chromakeying
- Bilinear, Trilinear, Anisotropic MIP-Mapped Filtering
- Cubic Environment Reflection Mapping
- Embossed Bump-mapping
- DXTn Texture Decompression
- 3D Graphics Rasterrization enhancements
- One Pixel per Clock
- Flat and Gouraud Shading
- Color Alpha Blending for Transparency
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Color Specular Lighting
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Z Bais support
- Dithering
- Line and Full-Scence Anti-Aliasing
- 16 and 24-bit Z Buffering
- 16 and 24-bit W Buffering
- 8-bit Stencil Buffering
- Double and Triple Render Buffer support
- 16 and 32 –bit color

8081 N/B Maintenance

- Destination Alpha
- Vertex Cache
- Maximum 3D resolution of 1600x1200 x32 bpp at 85 Hz
- Optimal 3D resolution supported
- Fast Clear support
- ROP support

- **HUB Interface for ICH4**

- 266 MB/s point to point hub interface to ICH4-M
- 66-M Hz base clock
- Supports the following traffic types to the ICH4-M
- Hub interface-to DRAM
- CPU-to-Hub interface
- Messaging
- MSI interrupt messages
- Power Management state change
- SMI, SCI, and SERR error indication
- Power Management
  -- SMRAM space remapping to A0000h (128-KB)
  -- Supports extended SMRAM space above 256- MB ,additional 1 MB TSEG from top of Memory, cacheable (cacheability controlled by CPU)
  -- APM rev 1.2 compliant power management
  -- Supports Suspend to System Memory(S3),Suspend to Disk(S4) and Hard Off/Total Reboot(S5)
  -- ACPI 1.0b,2.0 Support

1.2.4 I/O Controller Hub : Intel 82801DBM

The Intel 82801DBM ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the IDE Master/Slave controllers, and Intel®' I/O Hub architecture. The PCI to LPC Bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The integrated Universal Serial Bus Host Controllers features Dual Independent UHCI Compliant Host controllers with six USB ports delivering 480 Mb/s bandwidth and rich connectivity. Besides, Legacy USB devices as well as over current detection are also implemented.

The Integrated AC97 v2.3 compliance Audio Controller that features a 7-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode transfers up to 16 Mbytes/sec and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

Intel 82801DBM ICH4-M supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 82C37 compatible DMA controllers, Channels 0-3 are hardwired to 8 bit, three 8254 compatible programmable 16-bit counters channels 5-7, hardwired keyboard controller and PS2 mouse interface (not use in MiTAC 8080 model), Real Time clock with 512Bytes CMOS SRAM and two 82C59 compatible Interrupt controllers. Besides, the I/O APIC managing up to 14 interrupts with both Serial and FSB interrupt delivery modes is supported.

8081 N/B Maintenance

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the Intel 82801DBM ICH4-M supports Deeper Sleep power state for Intel Mobile processor.

A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara and Intel 82801DBM ICH4-M Hub interface together. Intel®' I/O Hub architecture is developed.

Features :

- PCI Bus Interface
- Supports PCI Revision 2.2 Specification at 33 MHz
- 133 MB/sec maximum throughput
- Supports up to six master devices on PCI
- One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- Support for 44-bit addressing on PCI using DAC protocol Integrated LAN Controller
- WfM 2.0 and IEEE 802.3 compliant
- LAN Connect Interface (LCI)
- 10/100 Mbit/sec Ethernet support_ Integrated IDE Controller
- Supports "Native Mode" register and interrupts
- Independent timing of up to 4 drives, with separate primary and secondary IDE cable connections

8081 N/B Maintenance

- Ultra ATA/100/66/33, BMIDE and PIO modes
- Tri-state modes to enable swap bay
- USB
- Includes three UHCI host controllers that support six external ports
- New: Includes one EHCI high-speed USB 2.0 Host Controller that supports all six ports
- New: Supports a USB 2.0 high-speed debug port
- Supports wake-up from sleeping states S1–S5
- Supports legacy keyboard/mouse software AC-Link for Audio and Telephony CODECs
- Supports AC ’97 2.3
- New: Third AC_SDATA_IN line for three codec support
- New: Independent bus master logic for seven channels (PCM In/Out, Mic 1 input, Mic 2 input, modem in/out, S/PDIF out)
- Separate independent PCI functions for audio and modem
- Support for up to six channels of PCM audio output (full AC3 decode)
- Supports wake-up events Interrupt Controller
- Support up to eight PCI interrupt pins
- Supports PCI 2.2 message signaled interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts

8081 N/B Maintenance

- Supports serial interrupt protocol
- Supports processor system bus interrupt delivery New: 1.5 V operation with 3.3 V I/O
- 5 V tolerant buffers on IDE, PCI, USB over current and legacy signals Timers Based on 82C54
- System timer, refresh request, speaker tone output Power Management Logic
- ACPI 2.0 compliant
- ACPI-defined power states (C1–C2, S3–S5)
- Supports Desktop S1 state (like C2 state, only STPCLK# active)
- ACPI power management timer
- PCI PME# support
- SMI# generation
- All registers readable/restorable for proper resume from 0 V suspend states External Glue Integration
- Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
- Integrated Pull-down and Series resistors on USB Enhanced Hub Interface Buffers Improve Routing flexibility (Not available with all Memory Controller Hubs)

1.2.5 Super I/O_NS PC87393

National Semiconductor's PC8739x family of LPC Super I/O devices is targeted for a wide range of portable applications. PC99 and ACPI compliant, the PC8739x family features an X-Bus Extension for read and write operations over the X-Bus, a full IEEE 1284 Parallel Port with a Parallel Port Multiplexer (PPM) for external Floppy Disk Drive (FDD) support, a Musical Instrument Digital Interface (MIDI) port, and a Game port. Like all National LPC Super I/O devices, the PC8739x offers a single-chip solution to the most commonly used PC I/O peripherals.

The PC8739x family also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serializer for Parallel IRQs and an enhanced WATCH DOG timer.

1.2.6 Keyboard controller Hitachi H8/3437

The H8/3437 Series is a series of high-performance micro-controllers with a fast H8/300 CPU core and a set of on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I2C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high-performance systems can be implemented easily. The series includes the H8/3437 with 60kbyte ROM and 2kbyte RAM, the H8/3436 with 48kbyte ROM and 2kbyte RAM, and the H8/3434 with 32kbyte ROM and 1kbyte RAM.

The H8/3437, H8/3436, and H8/3434 are available in mask-ROM versions. The H8/3437 and H8/3434 are also available in ZTAT™*1 (zero turn-around time) versions, providing a quick and flexible response to conditions from ramp-up through full-scale volume production, even for applications with frequently-changing specifications. In addition, the H8/3434 and H8/3437 have F-ZTAT™*2 (flexible-ZTAT) versions with on-board programmability.

1.2.7 Fast Ethernet Controller VT6105LOM

The VIA Rhine III VT6105LOM is a 10/100Mbps Fast Ethernet controller designed to provide system designers an easy to integrate single chip solution, with advanced management and power conservation features. Featuring a 3-in-1 design the VIA VT6105LOM integrates the physical, media, and management layers into a single chip.

Features :

- Single chip full/half duplex 10/100Mbps Fast Ethernet Management Controller
- IEEE 802.3/802.3u 10BASE-T and 100BASE-T Compatible
- 32bit PCI Bus-Master Interface
- VIA Rhine based CSR definition provides efficiency PCI bus-mastering
- Low power 100base-TX transceiver embedded Support 10Mbps and 100Mbps N-way Auto-negotiation operation Support Auto-MDIX function
- Enhancement MAC functions for 802.3 networking 802.1 Priority Transmit Maximum eight priority queues by drivers programmable 802.1q Multiple VLAN support VLAN long frames support (1518+4bytes) VLAN tag auto inserting and extracting on TX and RX side (VT6105LOM) NIC auto filtering on VLAN ID optional (VT6105LOM)
- IP header Checksum Offload supporting for Ipv4 frames. Support both of TCP and UDP protocol (VT6105LOM)
- Support Physical, Broadcast, and Multicast addresses filtering using both hashing table look-up and perfect-match mechanisms (VT6105LOM)
- 12 sets hardware 16 bit MIB counters (VT6105LOM)
- Fiber Optic network support (VT6105LOM)

- Fiber Optic network support (VT6105LOM)
- WFM 2.0 (VT6105LOM)
- DMI 2.0 (H/W)
- IO 3.3v with PCI bus 5V tolerant / Core 2.5v power, using low power 0.22um TSMC CMOS process, 128pin PQFP package.

1.2.8 Fax/Modem module

- Made by Billionton Computer corporation
- Integrated PCI v2.2 Interface
- Host-based ITU V.70 DSVD.
- Operation support: Windows 95/NT/ME/2000
- K56flex for internet connection rates approaching 56kbits/s.
- Data Modes capabilities
- On Chip PnP Logic
- ACPI support “On Now”
- Support “Call ID”
- PC 97 Compliant – Unimodem/V Compliant
- Low Power Consumption
- Operation Voltage 3.3V

1.2.9 PCMCIA Controller R5C551 + G571

R5C551

The R5C551 is the single chip solution offering single PCI bus-PC Card Bridge. The R5C551 is compliant with the latest specification in both PC card and IEEE 1394. The R5C551 has two PCI functions compliant, the PC Card interface and the IEEE 1394 interface. The PC Card controller of the R5C551 is compliant with PC Card Standard Release 7.0. The R5C551 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports any combination of 16-bit (Card-16), and CardBus (Card-32) PC Cards in one socket, powered at 5V or 3.3V, as required. The R5C551 provides the IEEE1394 OHCI-Link and two ports the IEEE1394 PHY that are compliant with the IEEE1394-1995, IEEE1394a-2000 and the latest 1394 OHCI specifications. The R5C551 data rate is capable of 100, 200, and 400Mbits per second.The R5C551 is compliant with the latest PCI Bus Power Management Specification, and provides several low-power modes that enable the host power system to further reduce power consumption.

Features :

- PC98/99/2001 compliant
- Low Power consumption
- Single Chip PCI-CardBus / 1394 bridge
- PCI Bus Interface
- CardBus PC card Bridge
- PC Card-16 Bridge
- 1394 OHCI-LINK bridge

8081 N/B Maintenance

- 1394 PHY
- System Interrupt
- Supports General Purpose IO
- Supports Posting Write and Prefetching Read for PC Card bridge
- Supports 16-bit Legacy mode (3E0/3E2 I/O port)
- Supports Zoomed Video Port
- Supports LED active pins for Card LED and 1394 LED
- Pin Compatible with R5C475
- 208pin CSP (size=16x16mm, pitch=0.8mm, t=1.5mm)

G571 (Power Switch)

- Fully integrated V_{CC} and V_{PP} switching
- Low $r_{DS(ON)}$: 90-mΩ 5V and 3.3V V_{CC} Switches
- Compatible with industry standard controllers
- 12V supply not required unless the PC Card uses 12V for flash programming or other applications
- 3.3V low voltage mode
- Short-circuit and thermal protection
- Compatible with 3.3V, 5V, and 12V PC Cards

1.2.10 AC”97 Codec_CMI9738-S

Features :

- Intel® AC’97 (Rev 2.2) compatible, meeting Microsoft’s® PC2001 requirements
- Built-in earphone buffer and internal PLL, the latter saving additional crystal.
- Line-in/rear out share the same jack.
- Digital S/PDIF IN/OUT support
- 48 LQFP package.
- CRL® 3D: HRTF based DS3D compatible audio engine.
- EAX™ 1.0 & 2.0 compatible.
- Sensaura™ 3D audio enhancement (optional).
- 18-20bit DAC interface for SPDIF I/O (ICH4).

1.2.11 System Flash Memory (BIOS)

- 4M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program.

1.2.12 Thermal Sensor_ADM1021A

- On-Chip and Remote Temperature Sensing
- No Calibration Necessary
- 1_C Accuracy for On-Chip Sensor
- 3_C Accuracy for Remote Sensor
- Programmable Over/Under Temperature Limits
- Programmable Conversion Rate
- 2-Wire SMBus Serial Interface
- Supports System Management Bus (SMBus) Alert
- 200 _A Max Operating Current
- 1 _A Standby Current
- 3 V to 5.5 V Supply
- Small 16-Lead QSOP Package

1.3 Other Functions

1.3.1 Hot Key Function

Keys combination	Feature	Meaning
Fn + F1	Enable/disable wireless LAN card signal	To switch wireless LAN card signal on/off
Fn + F2	Reserve	
Fn + F3	Volume Down with repeating function	KBC will send scan code to OS. User does not hear beep sound when press Fn+F3
Fn + F4	Volume Up with repeating function	KBC will send scan code to OS. User does not hear beep sound when press Fn+F4
Fn + F5	Display Switching	Only Support LCD->CRT->LCD&CRT. System didn't do display switch function When No connecting CRT, system always display on LCD. If system connects to TV, we can't switch to TV by Fn+F5 hot keys. This feature is disabling in SCU mode.
Fn + F6	Brightness Down	Adjust LCD panel backlight darkness
Fn + F7	Brightness Up	Adjust LCD panel backlight lightness
Fn + F8	To switch to high brightness or currently brightness	To switch to high brightness or currently brightness
Fn + F9	Reserve	
Fn + F10	Battery beep enable/disable	Battery low beep sound enable/disable
Fn + F11	Display device toggle on/off	Toggle Display Screen on or off
Fn + F12	System sleep	System sleeps button function

Note1 : In APM mode, we only support Fn+F5, Fn+F6, Fn+F7, Fn+F11. In ACPI mode, we support all hotkey function.

Note2 : When play DVD or mpeg file, press Fn+F5 no function. Because VGA BIOS block display switching when DVD active. Also cannot use the VGA utility “Graphics Properties” to switch.

Note3 : VGA BIOS did not allow display switching when in full screen DOS box. So press Fn+F5 no function when in full screen DOS box. Following is when in full screen DOS box behavior.

1.3.2 Power On/Off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode. Power button behavior was set by windows power management control panel.

You could set “standby” , “power off” or “hibernate”(must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

1.3.4.1 Three LED indicators on LCD panel:

From left to right that indicate: AC POWER, BATTERY STATUS and Wireless on/off.

8081 N/B Maintenance

	LED Color	Description
AC POWER	OFF	Power-off
	Green	Normal operation
	Flash Green	System was in stand—by mode
BATTERY STATUS	OFF	Battery not exists
	Green	Battery was full charged (Note #1)
	Orange	Battery was in charging
	Flash Red	Battery capacity was under 10% with Battery Power on (Note #2)
	Flash Orange	Charging abnormal state (Note #3)
Wireless on/off	OFF	Inactive mode (Wireless LAN OFF)
	Green	Normal operation in active mode (Wireless LAN ON)

Note :

#1 Battery capacity may not be 100% due to self-discharge.

#2 Two LEDs support –

Low – Flash once in four seconds – Battery capacity <10%.

Critical – Flash once in two seconds – Battery capacity <5%.

#3 Charging abnormal state.

1.3.4.2 Five LED indicators at front side:

From left to right that indicates CD-ROM/HARD DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.3.5 Fan Power On/Off Management

FAN is controlled by H8 embedded controller using ADM1021A to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.6 CMOS Battery

- CR2032 3V 220mAh lithium battery.
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exist, CMOS battery life at less (220mAh/5.8uA) 4 years.
- Battery was put in battery holder, can be replaced.

1.3.7 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- Supports four USB2.0 port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- Microphone Input Jack.
- Audio line out Jack
- One CardBus Sockets for one type II PC card extension
- One IEEE 1394a port for all firewire devices

1.4 Peripheral Components

1.4.1 LCD Panel

- QDI 14.1" QD141X1LH12
- AU 14.1" B141XN04-2

1.4.2 Ext. Floppy Disk Drive

- External USB 3.5” Mitsumi : D353FUE FDD (Option)

1.4.3 HDD

- Fujitsu : 30GB : MHT2030AT
- Hitachi Global : 30G : IC25N030ATMR04-0

1.4.4 CD ROM Drive

- Quanta : SCR-242
- TEAC : CD224E C92

1.4.5 DVD ROM Drive

- Quanta : SDR-083
- MKE : SR-8178

1.4.6 DVD COMBO Drive

- Quanta : SBW-242
- KME : UJDA750

1.4.7 DVD RW Drive

- KME : UJDA811

1.4.8 Keyboard

- US K/B - Zippy

1.4.9 Track Pad

- Synaptics TM41PUC2311-2

1.5 Power Management

The MiTAC 8081 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

1.5.1.1 Full On Mode

In this mode, each devices is running with the maximal speed. CPU clock is up to its maximum.

1.5.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.5.1.3 Standby Mode

For more power saving, it turns off the peripheral components. In this mode, the following is the status of each device:

CPU: Stop grant
LCD: backlight off
HDD: spin down

1.5.1.4 Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

Suspend to DRAM

- CPU: off
- NB: Partial off
- VGA: Suspend
- PCMCIA: Suspend
- Audio: off
- SDRAM: self Refresh

Suspend to HDD

- All devices are stopped clock and power-down

- System status is saved in HDD
- All system status will be restored when powered on again

1.5.2 Other Power Management Functions

1.5.2.1 HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 Appendix 1: Intel 82801DBM ICH4-M GPIO Definitions

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO0	CRT_IN#	GPI	MAIN
GPIO1	X	GPI	MAIN
GPIO2	INT_PIRQE#	GPI	MAIN
GPIO3	INT_PIRQF#	GPI	MAIN
GPIO4	INT_PIRQG#	GPI	MAIN
GPIO5	X	GPI	MAIN
GPIO6	AGP_BUSY#	GPI	MAIN
GPIO7	KB_US/JP#	GPI	MAIN
GPIO8	EXTSMI#	GPI	RESUME
GPIO11	SMBALERT#	GPI	RESUME
GPIO12	SCI#	GPI	RESUME
GPIO13	WAKE_UP#	GPI	RESUME
GPIO16	SIDE_OFF#	GPO	MAIN
GPIO17	PIDE_OFF#	GPO	MAIN
GPIO18	STOP_PCI	GPO	MAIN
GPIO19	SUSA#	GPO	MAIN
GPIO20	STOP_CPU	GPO	MAIN
GPIO21	X	GPO	MAIN
GPIO22	CPUPERF#	OD	MAIN

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO23	X	O	MAIN
GPIO24	PCLKRUN#	GPIO	RESUME
GPIO25	X	GPIO	RESUME
GPIO27	X	GPIO	RESUME
GPIO28	X	GPIO	RESUME
GPIO32	WIRELESS_PD#	GPIO	MAIN
GPIO33	LCDID0	GPIO	MAIN
GPIO34	LCDID1	GPIO	MAIN
GPIO35	LCDID2	GPIO	MAIN
GPIO36	SIDE_IN#	GPIO	MAIN
GPIO37	ICH_SIDE_IN#	GPIO	MAIN
GPIO38	IDERST#	GPIO	MAIN
GPIO39	MINIPCI_ACT#	GPIO	MAIN
GPIO40	DEBIG_EN	GPIO	MAIN
GPIO41	SIDEDET	GPIO	MAIN
GPIO42	SPK_OFF	GPIO	MAIN
GPIO43	SIDERST#	GPIO	MAIN

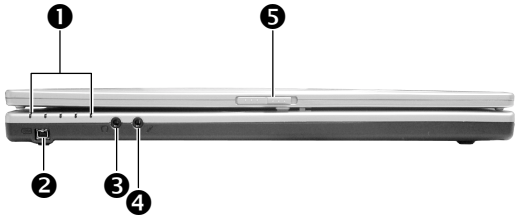
1.7 Appendix 2: MiTAC 8081 Product Specification

CPU	- Intel Banias /Dothan Processor CPU Support 1.8GHz or above - FSB 400MHz
Chipset	- Montara-GM + ICH4-M
L2 Cache	- 1M(Banias) /2M(Dothan)
System BIOS	- 4M bit Flash memory Flash (Include System BIOS and VGA BIOS)
H8	- Hitachi H8/F3437S
Memory	- 256MB on board; Expandable to 512MB - Expandable with combination of optional 128MB/256MB/512MB (P) memory - One 200-pin DDR SDRAM Memory Module, PC 2100/1600 specifications
CD-ROM Drive	- Quanta: SCR-242 - TEAC: CD224E C92
DVD-ROM Drive	- Quanta: SDR-083 - MKE: SR-8178
DVD Combo	- Quanta: SBW-242 - KME:UJDA750
DVD RW	- KME: UJDA811
HDD	- Fujitsu: 30GB: MHT2030AT - Hitachi Global: 30G: IC25N030ATMR04-0
LCD	- QDI 14.1" QD141X1LH12 - AU 14.1" B141XN04-2
Video Controller	- Integrate in Northbridge - Support Multi Monitor - Ultra AGP
Keyboard	- US (Zippy)
Touch Pad	- Synaptics TM41PUC2311-2
PCMCIA	- Type II x 1 - CardBus Support - RICOH R5C551
Audio System	- CMI9738-S
I/O Port	- Standard USB2.0 port x 4 - RJ-11 port x 1 - RJ-45 port x 1 - DC input x 1 - VGA monitor port x1 - Audio-out x 1 - Mic-in x 1 - IEEE1394a Port x 1
Communication	- JATE 56K V.90 MC97 Modem 56K Billionton MDC56S-1 - 10/100 Base-TX PCI LAN use VIA VT6105 LOM - Built-in antenna for Mini-PCI wireless communication use Intel Calexico Wireless LAN Module
Battery	- 6 cell Li-ION(2200mAh/3.7V)

2. System View and Disassembly

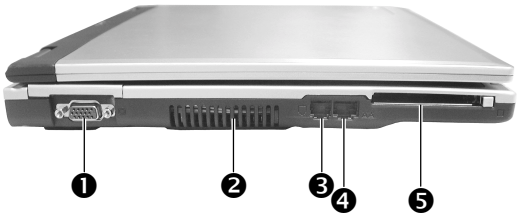
2.1 System View

2.1.1 Front View



❶ Device LED indicator
❷ 1394 Jack
❸ Line Out Phone Jack
❹ External Microphone Jack
❺ Top Cover Latch

2.1.2 Left-side View



❶ VGA Port
❷ Ventilation Openings
❸ RJ-11 Connector
❹ RJ-45 Connector
❺ PC Card Slot

2.1.3 Right-side View

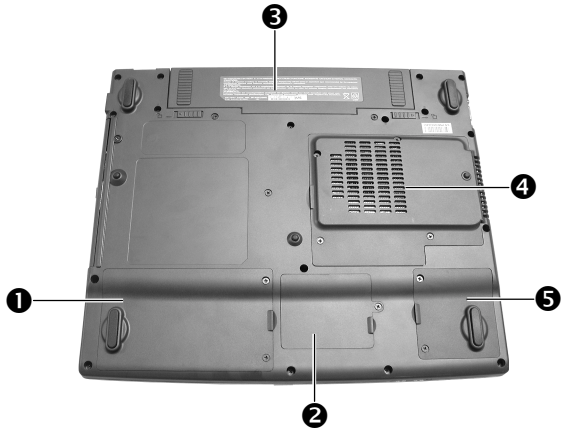
❶ CD-ROM/DVD-ROM Drive
❷ USB Ports *2
❸ Power Connector

2.1.4 Rear View

❶ USB Ports *2
❷ Kensington Lock

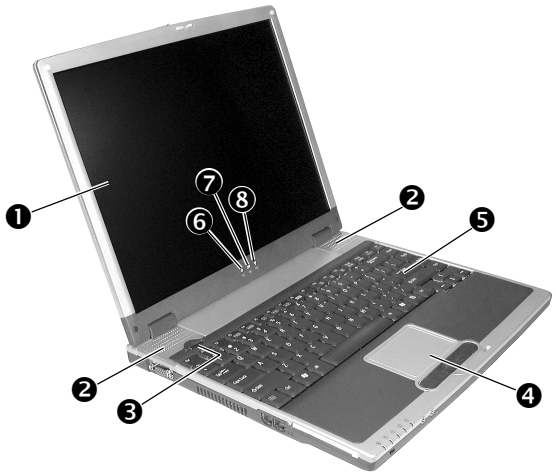
8081 N/B Maintenance

2.1.5 Bottom View



❶ Hard Disk Drive
❷ Modem Card
❸ Battery Park
❹ CPU
❺ Wireless Card

2.1.6 Top-open View

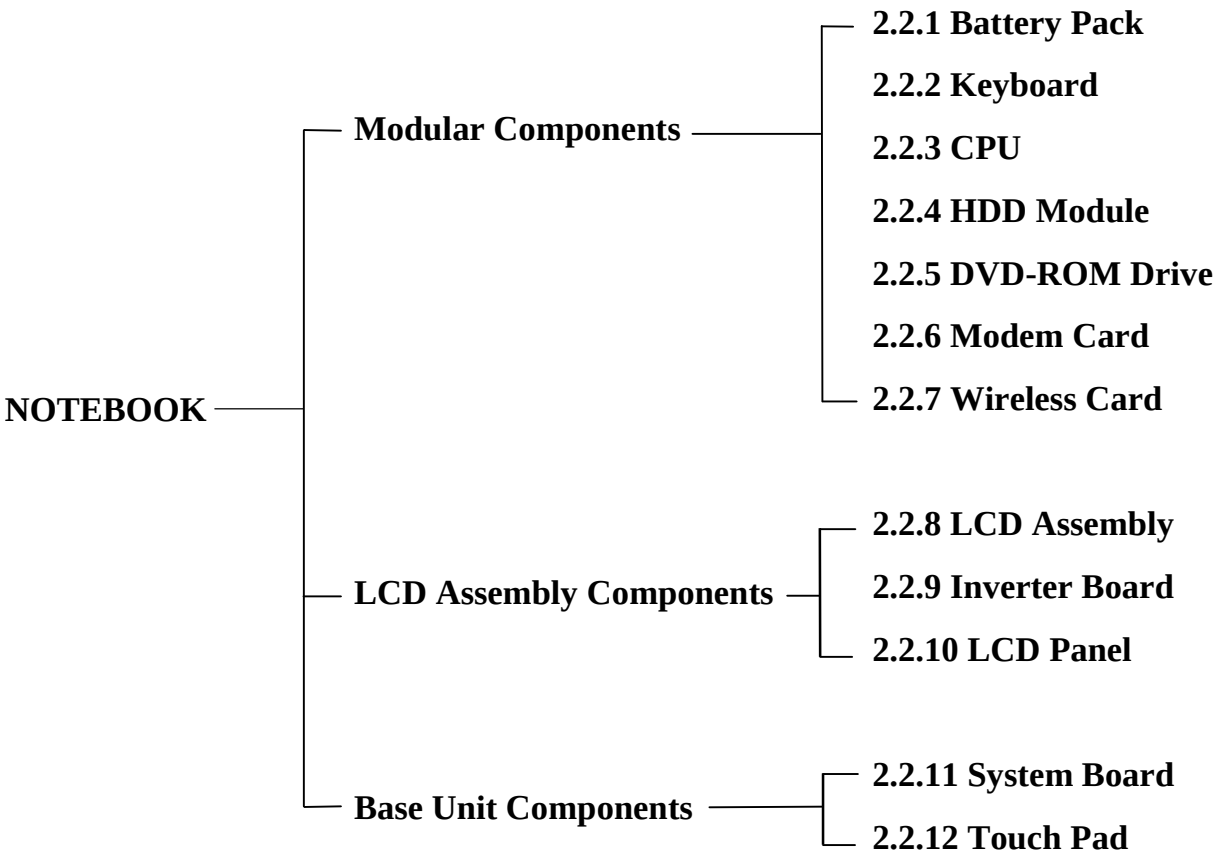


❶ LCD Screen
❷ Stereo Speaker Set
❸ Power Button
❹ Touch Pad
❺ Keyboard
❻ Hard Disk Drive Indicator
❼ Battery Power Charging Indicator
❽ Power Indicator

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

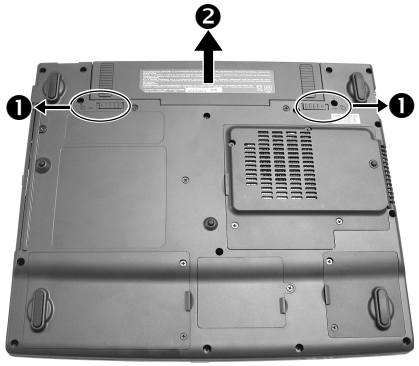


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove one screw that secure the speaker cover. (Figure 2-2)
3. Open the top cover.
4. Remove the speaker cover. (Figure 2-3)

Figure 2-2 Remove one screw

Figure 2-3 Remove the speaker cover

5. Remove three screws that secure the keyboard cover. (Figure 2-4)
6. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-5)

Figure 2-4 Remove three screws

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back.
2. Replace the keyboard into place with three screws.
3. Replace the keyboard cover into place with one screw.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the heatsink cover. (Figure 2-6)
3. Remove four spring screws that secure the heatsink upon the CPU. (Figure 2-7)

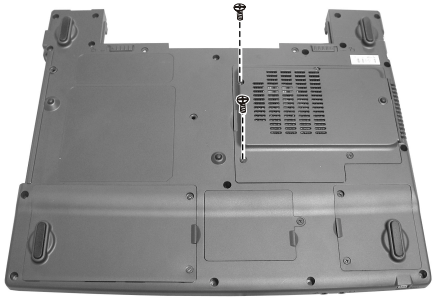


Figure 2-6 Remove two screws

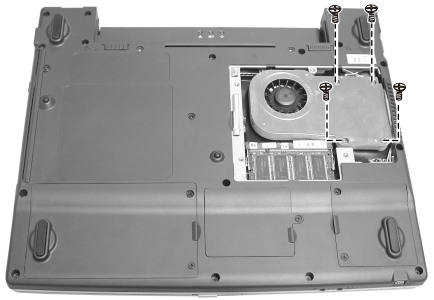


Figure 2-7 Remove four screws

4. Disconnect the fan's power cord from system board. (Figure 2-8)
5. To remove the existing CPU, Loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-9)

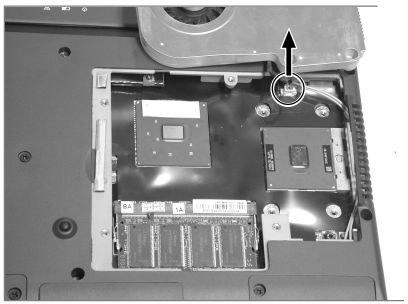


Figure 2-8 Remove the fan's power cord

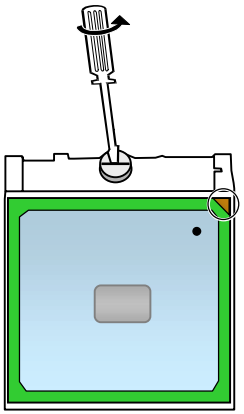


Figure 2-9 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-10)
3. Slide the HDD module out of the compartment. (Figure 2-11)

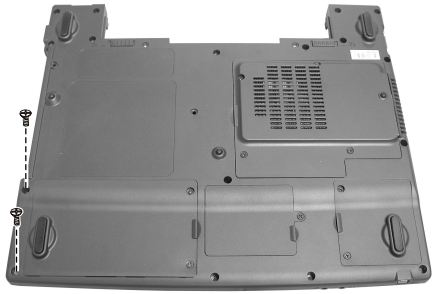


Figure 2-10 Remove the HDD compartment cover

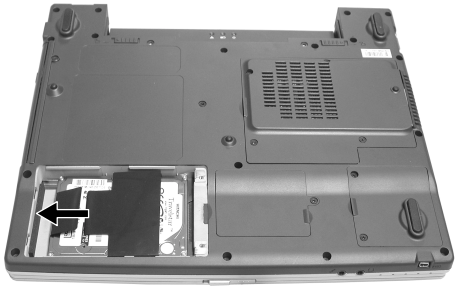


Figure 2-11 Remove HDD module

4. Remove four screws to To separate the hard disk drive from the bracket, remove four screws. (Figure 2-12)

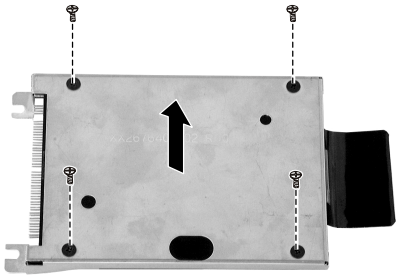


Figure 2-12 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the CD/DVD-ROM drive. (Figure 2-13)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-14)

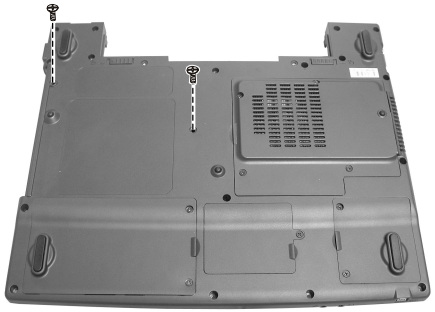


Figure 2-13 Remove two screws

Figure 2-14 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with two screws.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove one screw fastening modem card's compartment cover. (Figure 2-15)
3. Remove two screws fastening the modem card. (Figure 2-16)

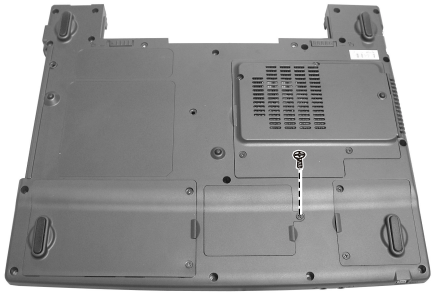


Figure 2-15 Remove one screw

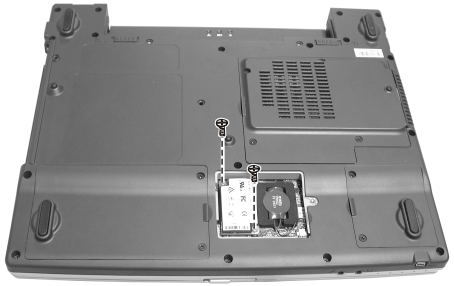


Figure 2-16 Remove two screws

4. Lift up the modem card and disconnect the cord. (Figure 2-17)

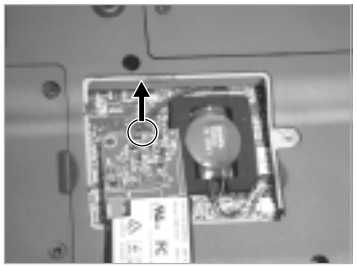


Figure 2-17 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the modem card's compartment cover by one screw.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Wireless Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.2.1 Disassembly)
2. Remove the two screws fastening the Mini PCI compartment cover. (Figure 2-18)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-19)

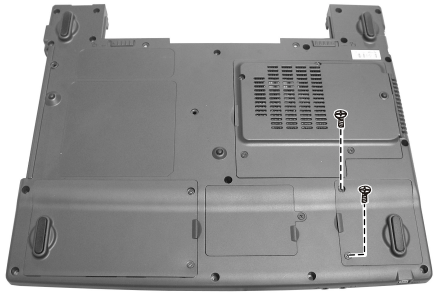


Figure 2-18 Remove two screws

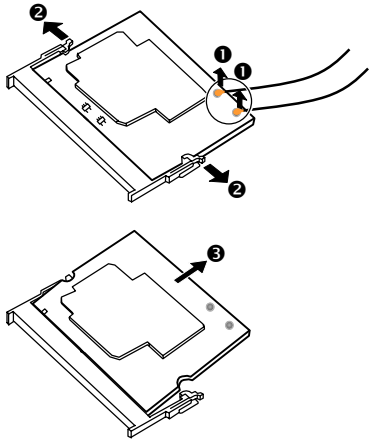


Figure 2-19 Remove the Wireless card

Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Tighten the screws to secure the wireless card compartment cover to the housing.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.8 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.2.1,2.2.2 , 2.2.4 and 2.2.5 Disassembly)
2. Remove the seventeen screws on the bottom of notebook. (Figure 2-20)
3. Remove the two screws fastening the Mini PCI compartment cover (Figure 2-21)

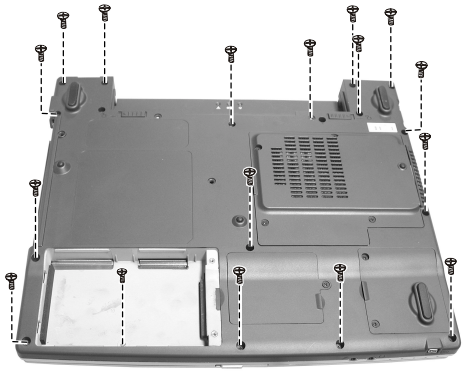


Figure 2-20 Remove seventeen screws

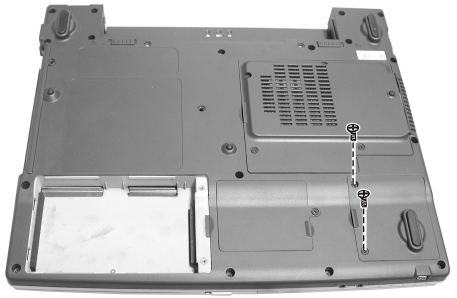


Figure 2-21 Remove two screws

4. Disconnect the antennae. (Figure 2-22)

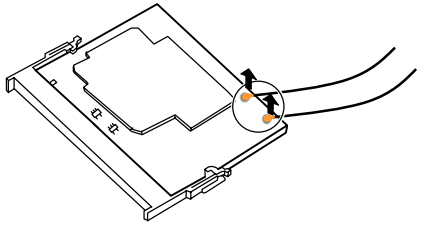


Figure 2-22 Disconnect the antennae

Figure 2-23 Remove two screws

5. Remove the two screws that secure the hinge cover (Figure 2-23)

6. Remove the two rear covers. (Figure 2-24)
7. Remove three screws. And disconnect the touch pad's cable. Then separate the top cover. (Figure 2-25)

Figure 2-24 Remove two rear covers

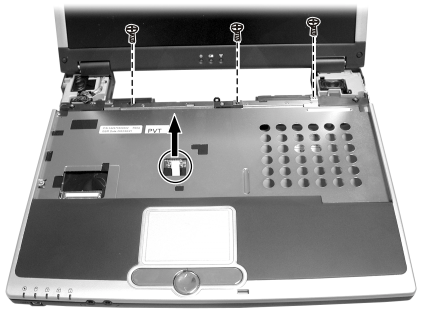


Figure 2-25 Remove the top cover

8. Remove the two hinge covers and disconnect two cables. (Figure 2-26)
9. Remove four screws and disconnect two cables. Carefully pull the antenna wires out. (Figure 2-27)

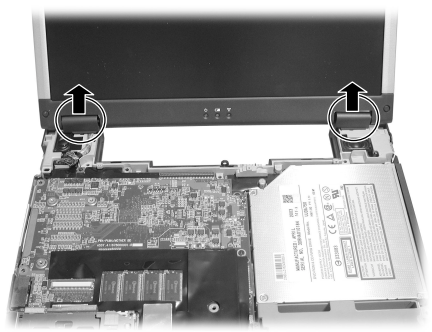


Figure 2-26 Remove two hinge covers

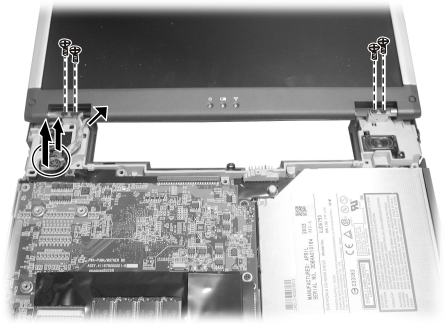


Figure 2-27 Remove four screws

10. Now you can lift up the LCD ASSY from base unit.

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Rip the antenna wires back into Min-PCI compartment.
3. Reconnect the two cables to the system board. Screw the hinge covers by two screws.
5. Replace the top cover and secure with three screws. And reconnect the touch pad's cable.
6. Replace the rear cover.
7. Upside down the notebook. secure the top cover by seventeen screws.
8. Reconnect the antennae. And Secure the Mini PCI compartment cover by two screws.
9. Replace the CD/DVD-ROM, hard disk drive, keyboard and battery pack. (Refer to sections 2.2.5, 2.2.4, 2.2.2 and 2.2.1 reassembly)

2.2.9 Inverter Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.4, 2.2.5 and 2.2.8 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-28)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the two screws fastening the inverter board. (Figure 2-29)

Figure 2-28 Remove LCD cover

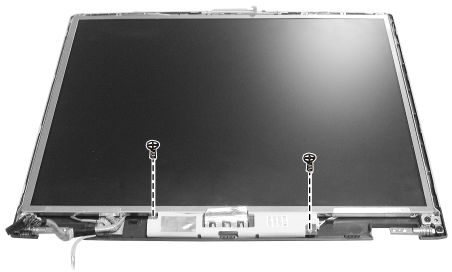


Figure 2-29 Remove two screws

5. To remove the inverter board on the lower part of the LCD housing , disconnect two cables. (Figure 2-30)

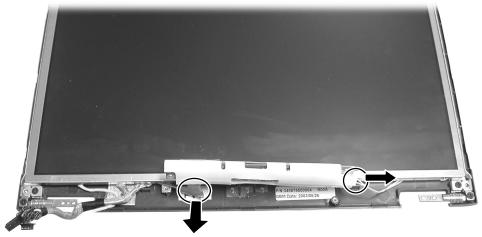


Figure 2-30 Remove the inverter board

Reassembly

1. Reconnect the cables. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover and secure with two screws and rubber pads.
3. Replace the LCD assembly. (Refer to section 2.2.8 reassembly)
4. Replace the CD/DVD-ROM drive, hard disk drive, keyboard and battery pack. (Refer to sections 2.2.5, 2.2.4, 2.2.2 and 2.2.1 reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, hard disk drive and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.4 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer for two steps 2,3 of section 2.2.9 Disassembly)
3. Remove six screws fastening the LCD panel. And lift it up. (Figure 2-31)
4. To remove the inverter board on the lower part of the LCD housing, disconnect two cables. (Figure 2-32)

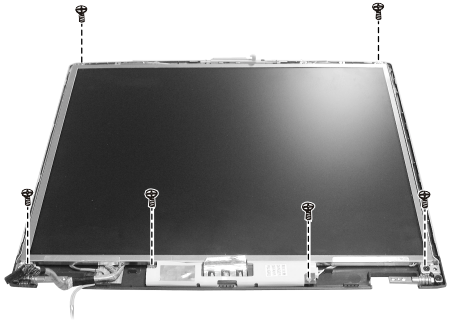


Figure 2-31 Remove the LCD panel

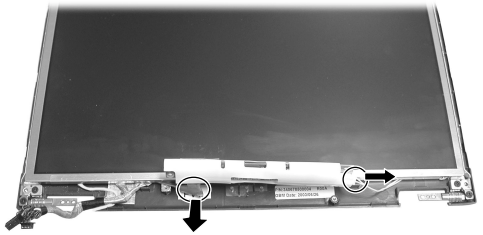


Figure 2-32 Remove the inverter board

5. Remove the four screws to free the LCD panel. (Figure 2-33)

Figure 2-33 Free the LCD panel

Reassembly

1. Attach the LCD panel's bracket back to LCD panel and secure with four screws.
2. Replace the LCD panel into place.
3. Reconnect two cables to inverter board and secure with two screws.
4. Fasten the LCD panel by six screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, CD/DVD-ROM drive, hard disk drive, keyboard, battery pack. (See sections 2.2.8, 2.2.4, 2.2.2, and 2.2.1 reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CPU, CD/DVD-ROM drive and modem card. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6 Disassembly)
2. Remove the top cover approach the system board. (Refer to steps 1-7 of section 2.2.8 Disassembly)
3. Remove four screws that secure the system board. Then lift it up form the housing. (Figure 2-34)

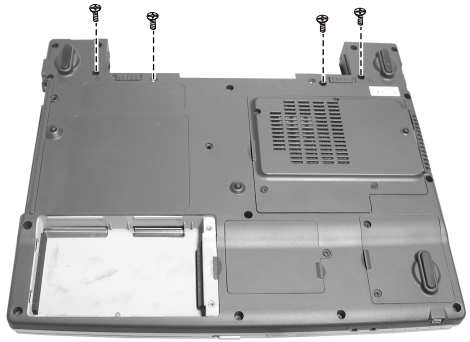


Figure 2-34 Remove four screws

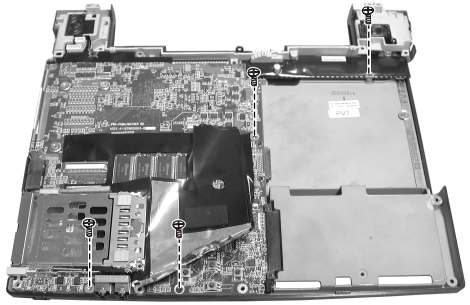


Figure 2-35 Remove four screws

4. Remove four screws that secure the system board. (Figure 2-35)

5. Remove two hex nuts and disconnect two speaker's cords from system board. (Figure 2-36)
6. Carefully put the system board upside down. And remove one screw. Then separate the bracket. (Figure 2-37)

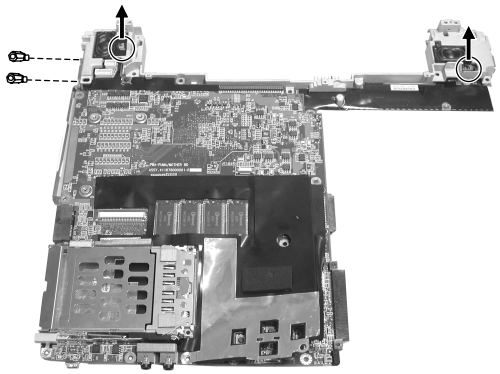


Figure 2-36 Remove two hex nuts

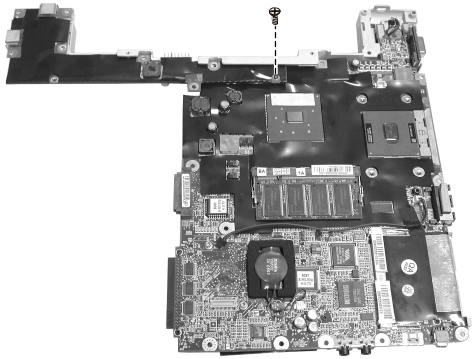


Figure 2-37 Remove the bracket

7. Now you can separate the D/D board from system board. (Figure 2-38)

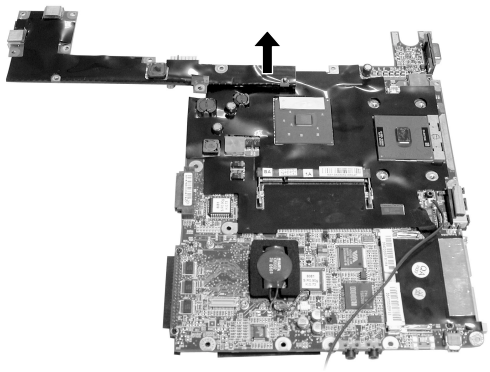


Figure 2-38 Free the system board

Reassembly

1. Replace the D/D board to the system board.
2. Fit the bracket and secure with one screw and two hex nuts.
3. Turn over the system board. Reconnect the speaker's cords.
4. Replace the system board back into the housing and secure with four screws.
5. Fasten the housing and secure four screws on the bottom of the notebook.
6. Replace the LCD assembly, CD/DVD-ROM, HDD, keyboard and battery pack. (Refer to previous section reassembly)

2.2.12 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.2.1,2.2.2 , 2.2.4 and 2.2.5 Disassembly)
2. Remove the top cover. (See steps 1-7 in section 2.2.7 Disassembly)
3. Disconnect the cable. (Figure 2-39)
4. Touch Pad can't be taken apart from Top Cover. It is necessary to replace the Top Cover, if defect.

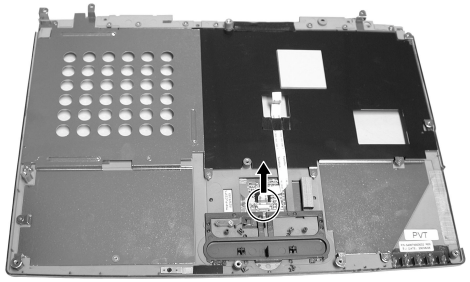


Figure 2-39 Disconnect the cable

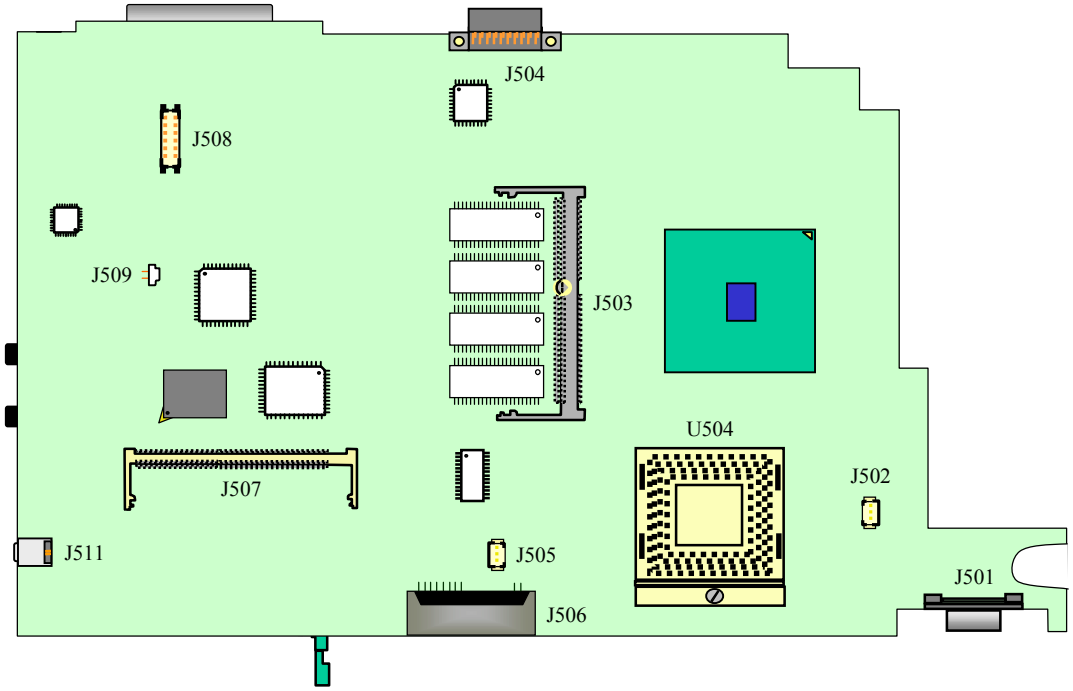
Reassembly

1. Reconnect the cable.
2. Reassemble the notebook. (See the previous sections reassembly)

8081 N/B Maintenance

3. Definition & Location of Connectors / Switches

3.1 Main Board (Side A)

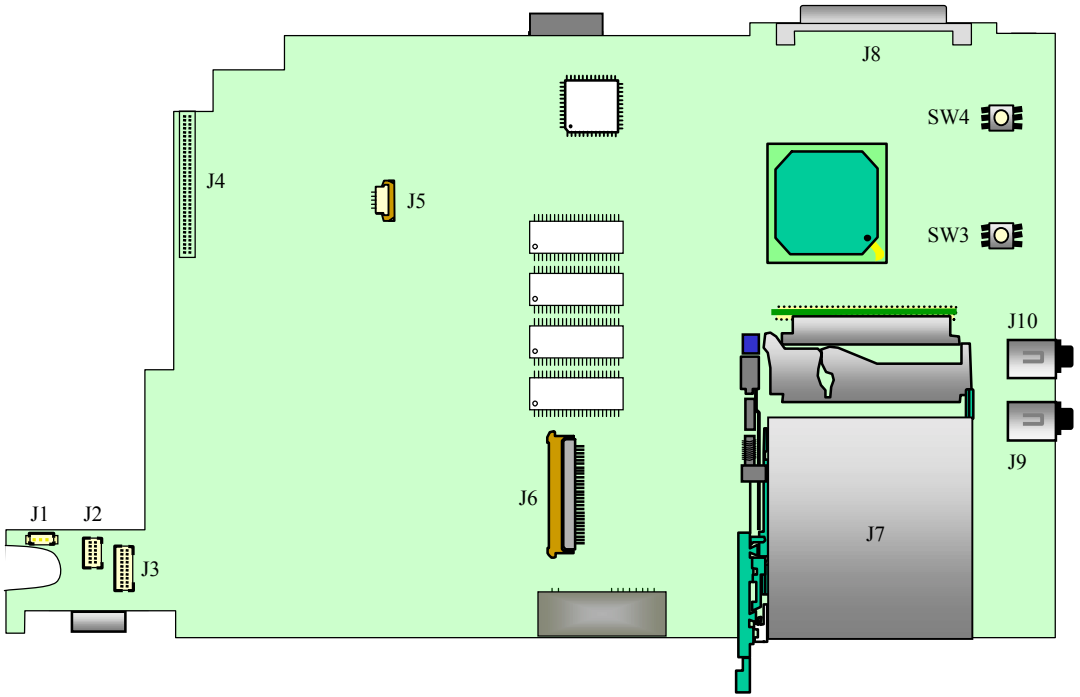


- **J501 : External VGA Connector**
- **J502 : CPU Fan Connector**
- **J503 : Extend DDR SDRAM Socket**
- **J504 : Secondary EIDE Connector**
- **J505 : MDC Jump Wire Connector**
- **J506 : RJ11 & RJ45 Connector**
- **J507 : Mini PCI Socket**
- **J508 : MDC Board Connector**
- **J509 : RTC Battery Connector**
- **J511 : IEEE 1394 Connector**
- **U504 : Intel Banias Processor Socket6**

8081 N/B Maintenance

3. Definition & Location of Connectors/ Switches

3.1 Main Board (Side B)

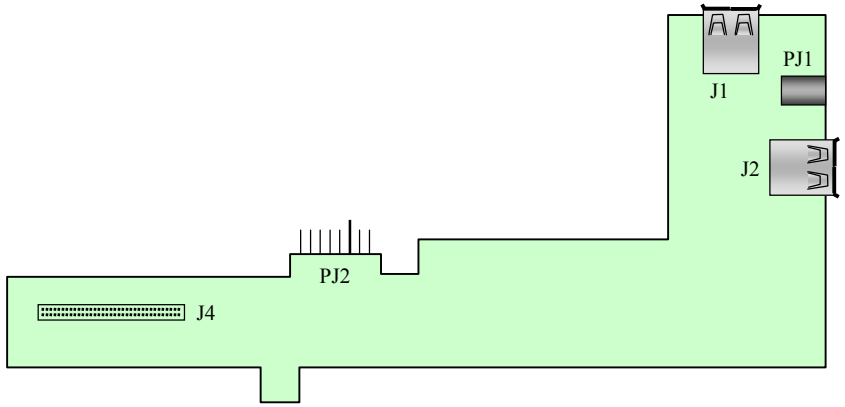


- J1 : Internal Left Speak Connector
- J2 : LCD Inverter Board Connector
- J3 : LCD Connector
- J4 : DC to DC Board Connector
- J5 : Touch-Pad Connector
- J6 : Internal Keyboard Connector
- J7 : PCMCIA Card Socket
- J8 : Primary EIDE Connector
- J9 : Line Out Jack
- J10 : MIC In Jack
- SW3 : Touch-Pad Left Button
- SW4 : Touch-Pad Right Button

8081 N/B Maintenance

3. Definition & Location of Connectors / Switches

3.2 DC to DC Board

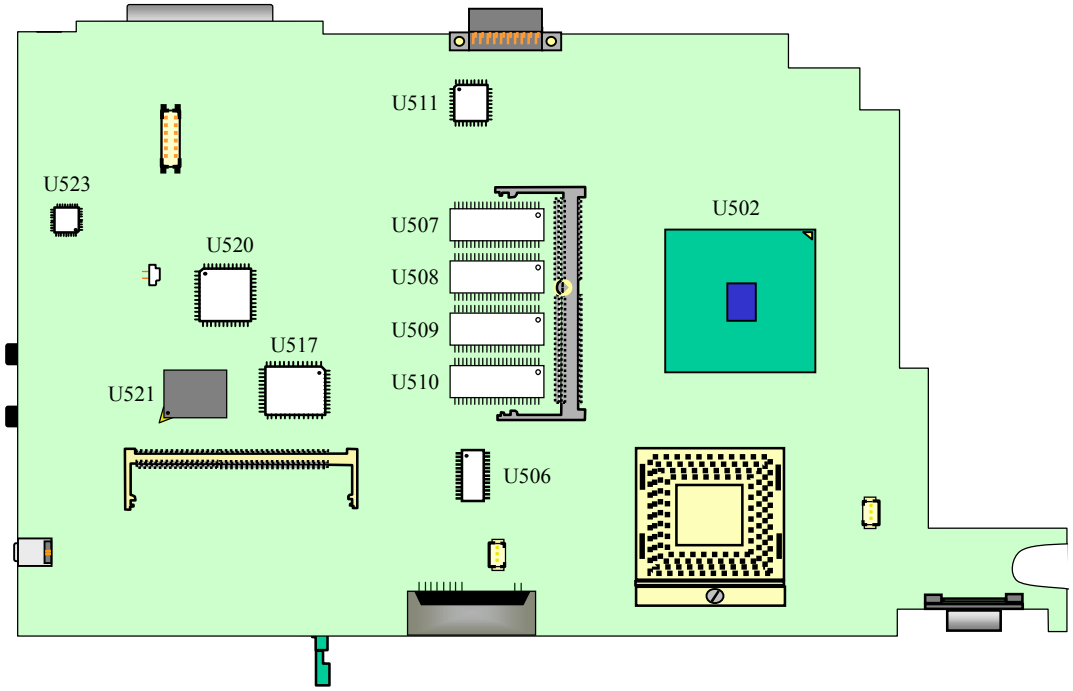


- **J1 : USB Port Connector**
- **J2 : USB Port Connector**
- **J4 : DC to DC Board Connector**
- **PJ1 : Power Jack**
- **PJ2 : Battery Connector**

8081 N/B Maintenance

4. Definition & Location of Major Components

4.1 Main Board (Side A)

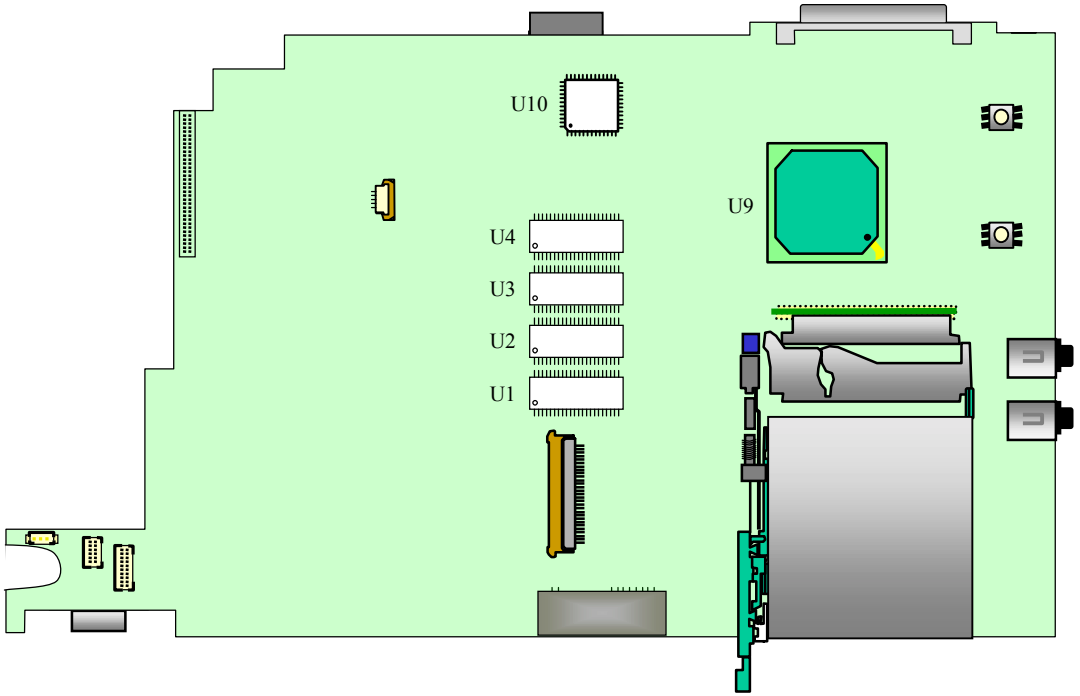


- **U502 : Intel 82855 MCH (Montara-GM)**
- **U506 : ICS950810 Clock Generator**
- **U507 : On Board DDR RAM**
- **U508 : On Board DDR RAM**
- **U509 : On Board DDR RAM**
- **U510 : On Board DDR RAM**
- **U511 : Flash BIOS ROM**
- **U517 : VT6105LOM LAN Controller**
- **U520 : H8/F3437 Micro Controller**
- **U521 : R5C551 CardBus & 1394 Controller**
- **U523 : CMI9738S Audio Codec**

8081 N/B Maintenance

4. Definition & Location of Major Components

4.1 Main Board (Side B)



- **U1 : On Board DDR RAM**
- **U2 : On Board DDR RAM**
- **U3 : On Board DDR RAM**
- **U4 : On Board DDR RAM**
- **U9 : Intel 82801DBM ICH4-M**
- **U10 : PC87393 Super I/O Controller**

5. Pin Descriptions of Major Components

5.1 Intel Banias Pentium M Processor

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group** / **DSTBN#/DSTBP#** / **DINV#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Banias Pentium M Processor

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Banias Pentium M Processor

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Banias Pentium M Processor

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ**0#** signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for PSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURS**T#** allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the PSB VTT power plane.
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

Host Interface Signals (Continued)

Signal Name	Type	Description
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV#** — **Data Bits** DNIV[3]# — HD[63:48]# DNIV[2]# — HD[47:32]# DINV[1]# — HD[31:16]# DINV[0]# — HD[15:0]#
HA[31:0]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub Interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** — **Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP[3]#, HDSTBN[3]# — HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# — HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# — HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# — HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with **HITM#** by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub Interface snoopable access to System Memory is allowed when HLOCK# is asserted by the CPU.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Host Interface Signals (Continued)

Signal Name	Type	Description
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates type of response according to the following the table: **RS[2:0]** — **Response type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by MCH-M) 100 — Hard Failure (not driven by MCH-M) 101 — No data response 110 — Implicit Write back 111 — Normal data response

DDR SDRAM Interface Signals

Signal Name	Type	Description
SCS [3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **Note:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge.
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the System Memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the System Memory commands.

DDR SDRAM Interface Signals(Continued)

Signal Name	Type	Description
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** ECC error detection is supported: by the SDQ[71:64] signals.
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	I SSTL_2	**Clock Input:** Reserved, NC.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Hub Interface Signals

Signal Name	Type	Description
HI_[10:0]	I/O Hub	**Packet Data:** Data signals used for HI read and write operations.
HI_STB	I/O Hub	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HI_STB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

Clock Signals

Signal Name	Type	Description
Host Processor Clocking		
BC.LK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that are in the Host clock domain (Host, Hub and System Memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
System Memory Clocking		
SCK[5:0]	O SSTL_2	**Differential DDR SDRAM Clock:** SCK and SCK# pairs are differential clock outputs. The crossing of the positive edge of SCK and the negative edge of SCK# is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each SO-DIMM. **NOTE:** ECC error detection is supported by the SCK[2] and SCK[5] signals.
SCK[5:0]#	O SSTL_2	**Complementary Differential DDR SDRAM Clock:** These are the complimentary differential DDR SDRAM clock signals. **NOTE:** ECC error detection is supported by the SCK[2]# and SCK[5]# signals.
DVO/Hub Input Clocking		
GCLKIN	I CMOS	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/Hub Interface.
DVO Clocking		
DVOBC.LK **DVOBCLK#**	O DVO	**Differential DVO Clock Output:** These pins provide a differential pair reference clock that can run up to 165-MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out. DVOBCLK and DVOBCLK# should be left as NC (“Not Connected”) if the DVO B port is not implemented.

Clock Signals (Cotinued)

Signal Name	Type	Description
DVOCC.LK **DVOCCLK#**	O DVO	**Differential DVO Clock Output**: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOCCLK corresponds to the primary clock out. DVOCCLK# corresponds to the primary complementary clock out. DVOCCLK and DVOCCLK# should be left as NC (“Not Connected”) if the DVO C port is not implemented.
DVOBCCLKINT	I DVO	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 85 -MHz. DVOBC Pixel Clock Input: When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. DVOBC Interrupt: When configured as an interrupt input, this interrupt can support either DVOB or DVOC. DVOBCCLKINT needs to be pulled down if the signal is NOT used.
DPMS	I DVO	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during
DAC Clocking		
DREFCLK	I LVTTL	**Display Clock Input:** This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.
LVDS LCK Flat Panel Clocking		
DREFSSCLK	I LVTTL	**Display SSC Clock Input:** This pin provides a 48-MHz or 66-MHz input clock (SSC or non-SSC) to the Display PLL B.

Dedicated LVDS LCD Flat Panel Interface Signals

Signal Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V± 225 mV	**Channel A differential data pair 3:0 output (true):** 245-800 MHz.
IYAM[3:0]	O LVDS	1.25 V± 225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Dedicated LVDS LCD Flat Panel Interface Signals (Continued)

Signal Name	Type	Voltage	Description
ICLKBP	O LVDS	1.25 V± 225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V± 225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (true):** 245-800 MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

Digital Video Output B (DVOB) Port Signals

Signal Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

Digital Video Output C (DVOC) Port Signals

Signal Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indicatio**n: **DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

DVOB and DVOC Port Common Signals

Signal Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrup**t: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0**]: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Note**: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	**DVODETEC**T: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Analog CRT Display Signals

Signal Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronizatio**n: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronizatio**n: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output**): This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm. CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output**): This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm . CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-ohm. CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

GPIO Signals

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the System Memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.

GPIO Signals (Continued)

GPIO I/F Total	Type	Comments
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI).
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPADATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Voltage Reference, PLL Power Signals

Signal Name	Type	Description
Host Processor		
HXRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HYRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HXSWING	Analog	**Host Voltage Swing (RCOMP reference voltage):** These signals provide a reference voltage used by the PSB RCOMP circuit.
HYSWING	Analog	**Host Voltage Swing (RCOMP reference voltage**): These signals provide a reference voltage used by the PSB RCOMP circuit.
HDVREF[2:0]	Ref Analog	**Host Data (input buffer) VREF**: Reference voltage input for the data signals of the Host AGTL+ Interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	**Host Address (input buffer) VREF**: Reference voltage input for the address signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	**Host Common Clock (Command input buffer) VREF**: Reference voltage input for the common clock signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	**PSB Power Supply:** VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	**PSB Power Supply:** VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. **NOTE:** Not to be connected to power rail.
System Memory		
SMRCOMP	Analog	**System Memory RCOMP**: This signal is used to calibrate the memory I/O buffers.
SMVREF_0	Ref Analog	**Memory Reference Voltage(Input buffer VREF**):Reference voltage input for Memory Interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	Ref Analog	**RCOMP reference voltage:** This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	Ref Analog	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	Power	Power supply for Memory I/O.
VCCQSM	Power	Power supply for System Memory clock buffers.
VCCASM	Power	Power supply for System Memory logic running at the core voltage (isolated supply, not connected to the core).

Voltage Reference, PLL Power Signals (Continued)

Signal Name	Type	Description
Hub Interface		
HLRCOMP	Analog	**Hub Interface RCOMP**: This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub Interface buffers
DVO		
DVORCOMP	Analog	**Compensation for DVO**: This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO.
GPIO		
VCCGPIO	Power	Power supply for GPIO buffers
DAC		
REFSET	Ref Analog	**Resistor Set:** Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
LVDS		
LIBG	Analog	LVDS reference current: signal connected to reference resistor.
VCCDLVDS	Power	Digital power supply.
VCCTXLVDS	Power	Data/Clk Tx power supply.
VCCALVDS	Power	Analog power supply.
VSSALVDS	Power	Ground supply for LVDS.
Clocks		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
Core		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STB/HI_STBS	I/O	**Hub Interface Strobe/ Hub Interface Strobe Second:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	**Hub Interface Strobe Complement / Hub Interface Strobe First:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HI_VSWING	I	**Hub Interface Voltage Swing:** Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock**: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In**: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out**: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# **Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri- stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Signal Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]#/** REQ[B]#/ GPIO[1]	I	**PCI Requests:** The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]#/** GNT[B]#/ GPIO[17]	O	**PCI Grants:** The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:** This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non- exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1-M–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	**PCI Clock Run:** Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. **NOTE:** An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] **REQ[B]#/** REQ[5]#/ GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] **GNT[B]#/** GNT[5]#/ GPIO[17]	O	**PC/PCI DMA Acknowledges [A: B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], **SDA[2:0]**	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE Interface Signals (Continued)

Signal Name	Type	Description
PDD[15:0], **SDD[15:0]**	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, **SDDREQ**	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, **SDDACK#**	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMARDY#) **SDIOR#/** (SDWSTB/SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) **SDIOW#/** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

IDE Interface Signals (Continued)

Signal Name	Type	Description
PIORDY#/ (PDRSTB/PWDMARDY#) **SIORDY#/** (SDRSTB/SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME#/ FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
OC[5:0]#	I/O	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	**S1 Sleep Control:** SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M–S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Power Management Interface Signals (Continued)

Signal Name	Type	Description
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	**C3_STAT#:** This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. **NOTE:** This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	**AGP Bus Busy:** To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	**Stop CPU Clock:** Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	**Battery Low:** This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M–S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	**CPU Performance:** CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	**SpeedStep Mux Select:** SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/ VRMPWRGD	I	**VGATE/VRM Power Good:** VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals (Continued)

Signal Name	Type	Description
DPRSLPVR	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When the signal is low (default), the voltage regulator outputs the higher "Normal" voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. **NOTE:** DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.

Processor Interface Signals (Continued)

Signal Name	Type	Description
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4's other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. To allow for Intel ® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	**66 MHz Clock:** This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **NOTES:** 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	**AC '97 Reset:** This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	**AC '97 Sync:** This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	**AC97 Bit Clock:** This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	**AC97 Serial Data In 2:**0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

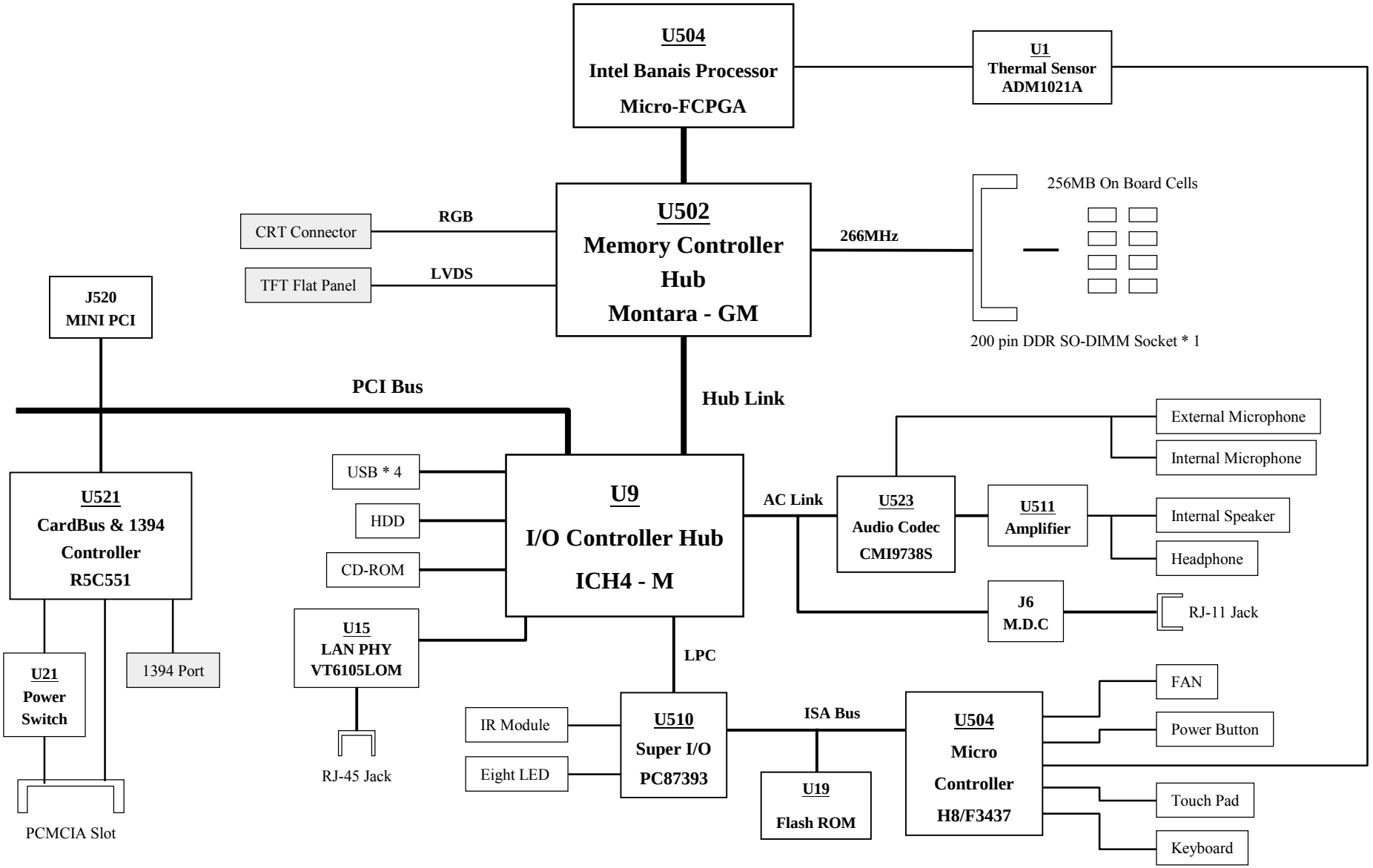
NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

8081 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

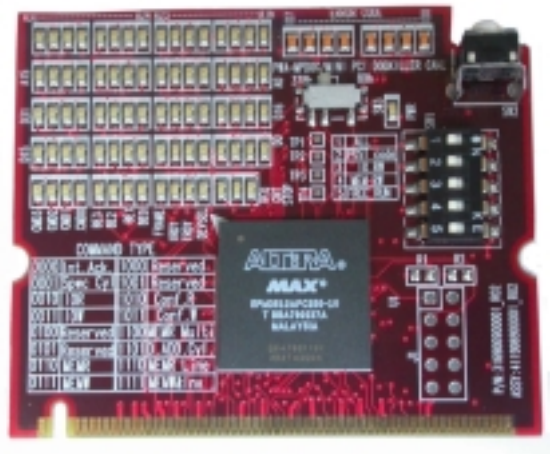
Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

8081 N/B Maintenance

7.3 Maintenance Diagnostics

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-378 Port Debug BD
Note: Order it from MIC/TSSC

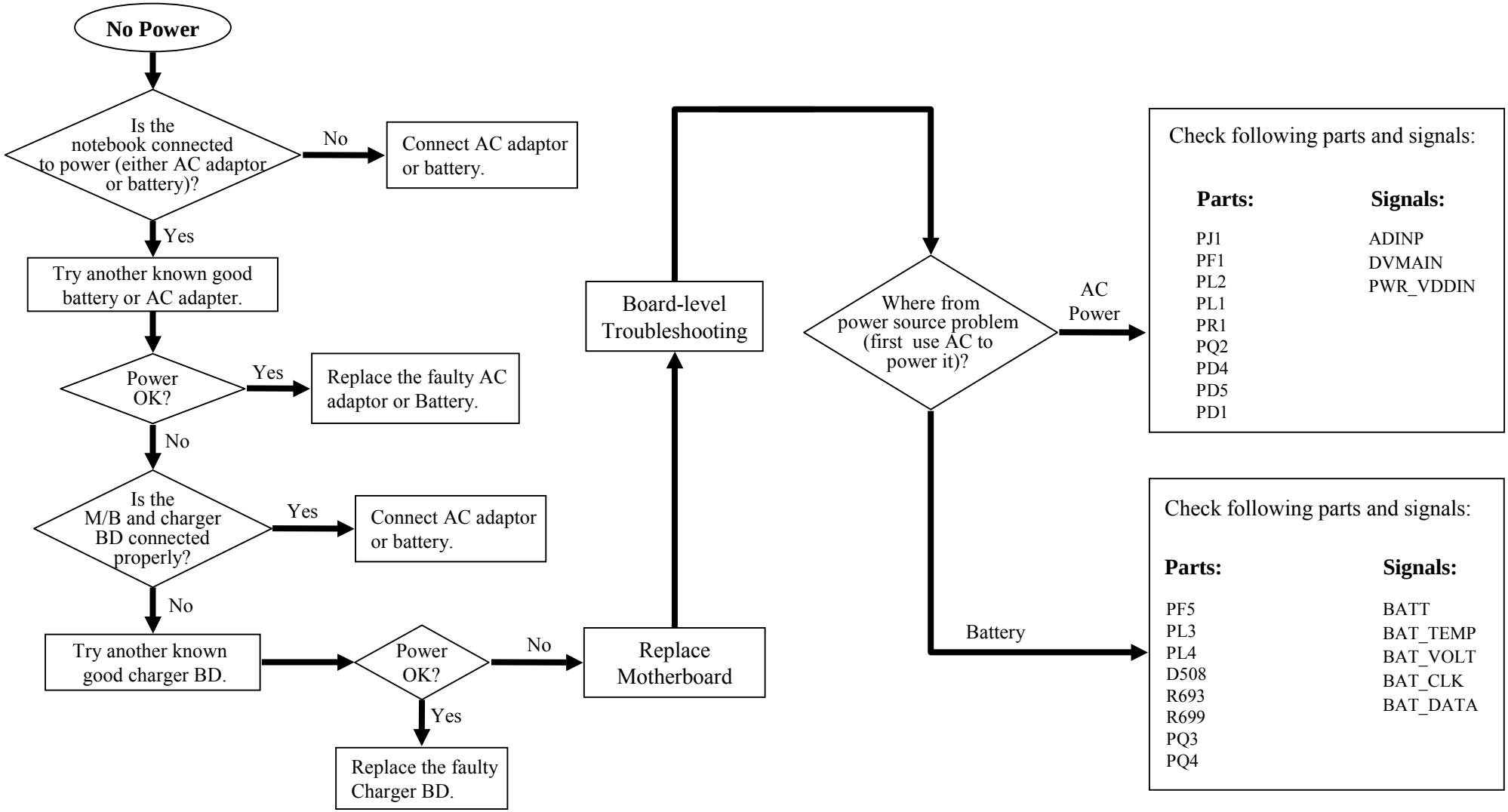
8. Trouble Shooting

- **8.1 No Power**
- **8.2 No Display**
- **8.3 VGA Controller Failure LCD No Display**
- **8.4 External Monitor No Display**
- **8.5 Memory Test Error**
- **8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error**
- **8.7 Hard Driver Test Error**
- **8.8 CD-ROM Driver Test Error**
- **8.9 USB Port Test Error**
- **8.10 Audio Failure**
- **8.11 LAN Test Error**
- **8.12 PC Card & 1394 Socket Failure**

8081 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

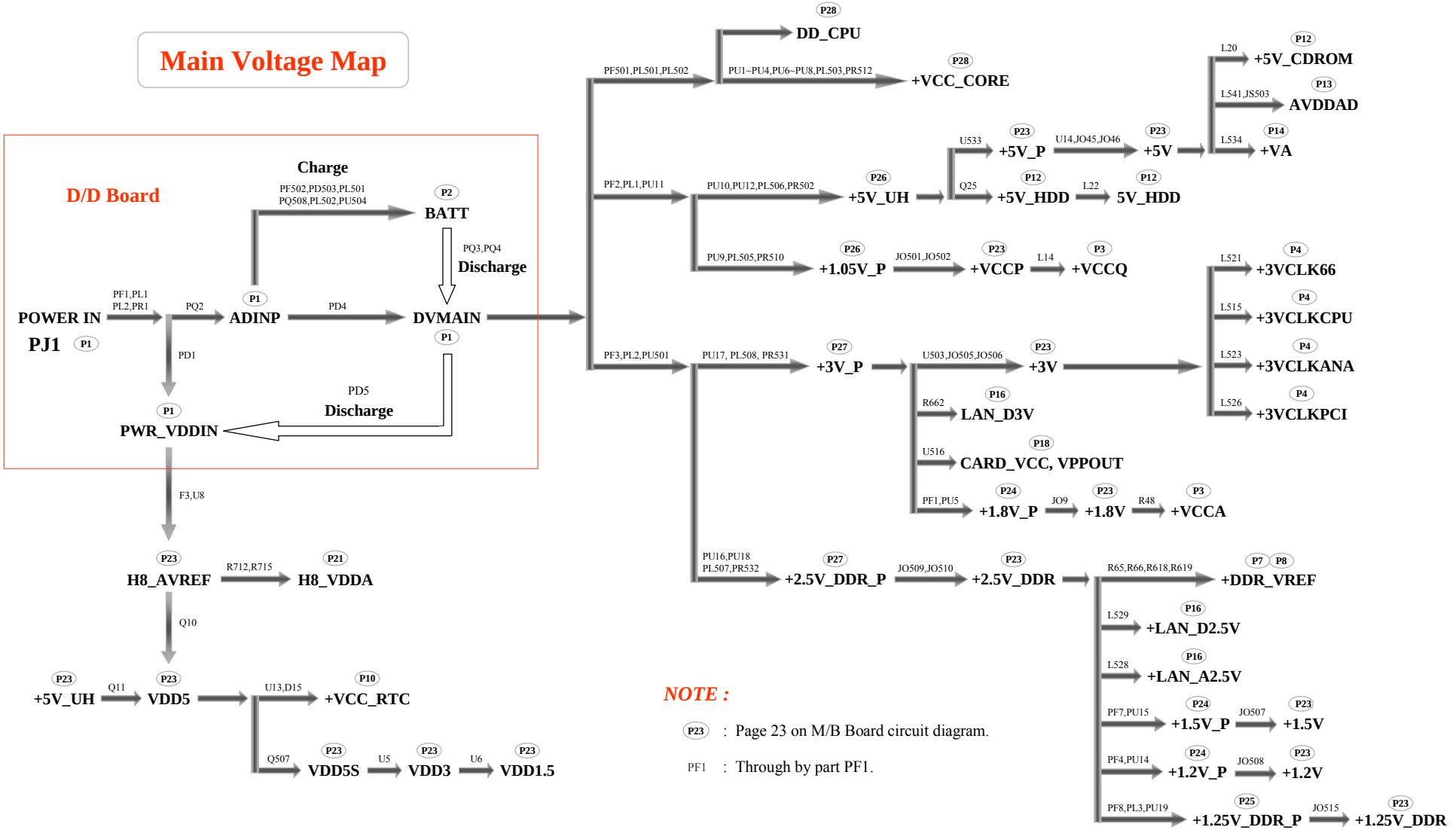


8081 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



NOTE :

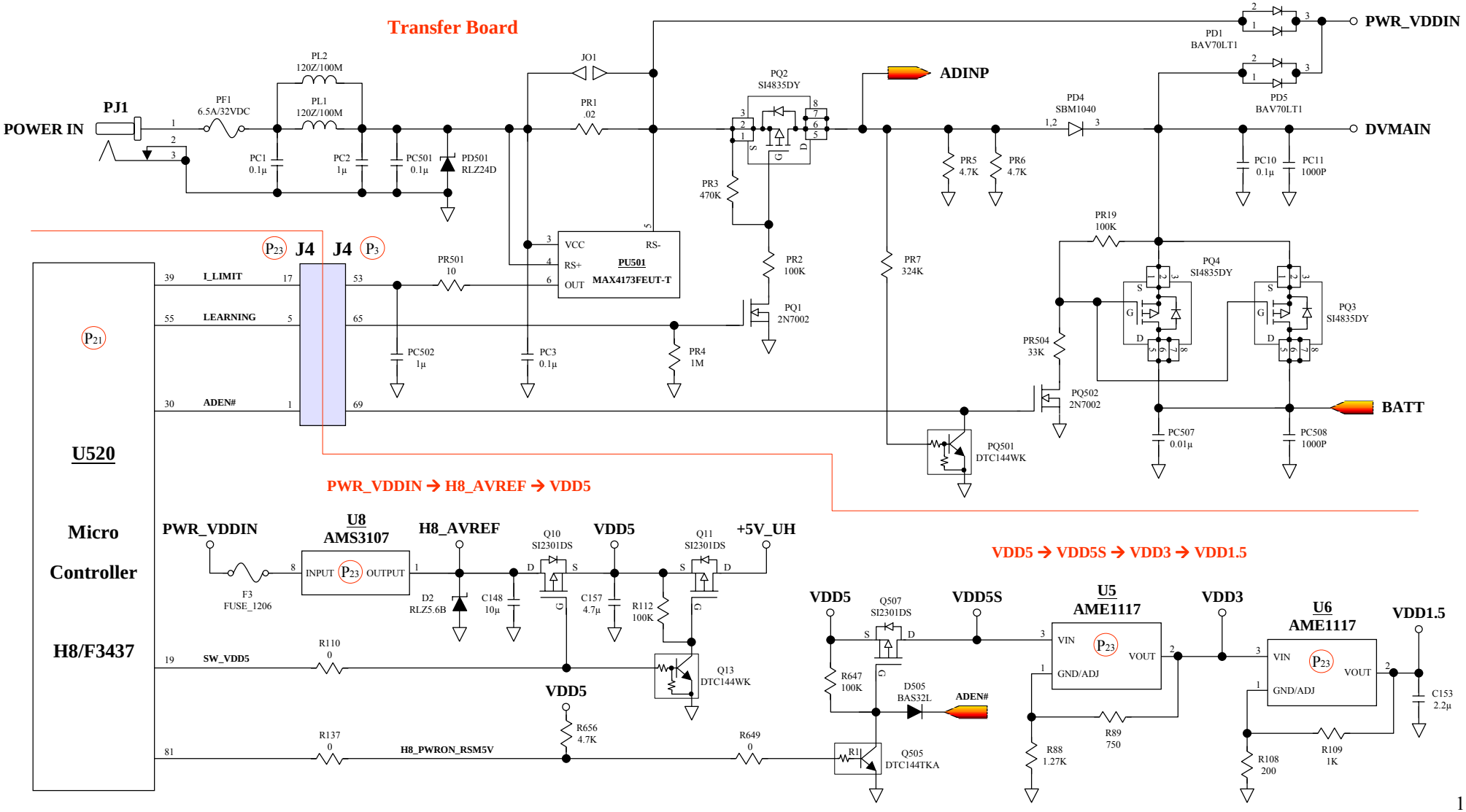
P23 : Page 23 on M/B Board circuit diagram.

PF1 : Through by part PF1.

8081 N/B Maintenance

8.1 No Power – ADINP

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

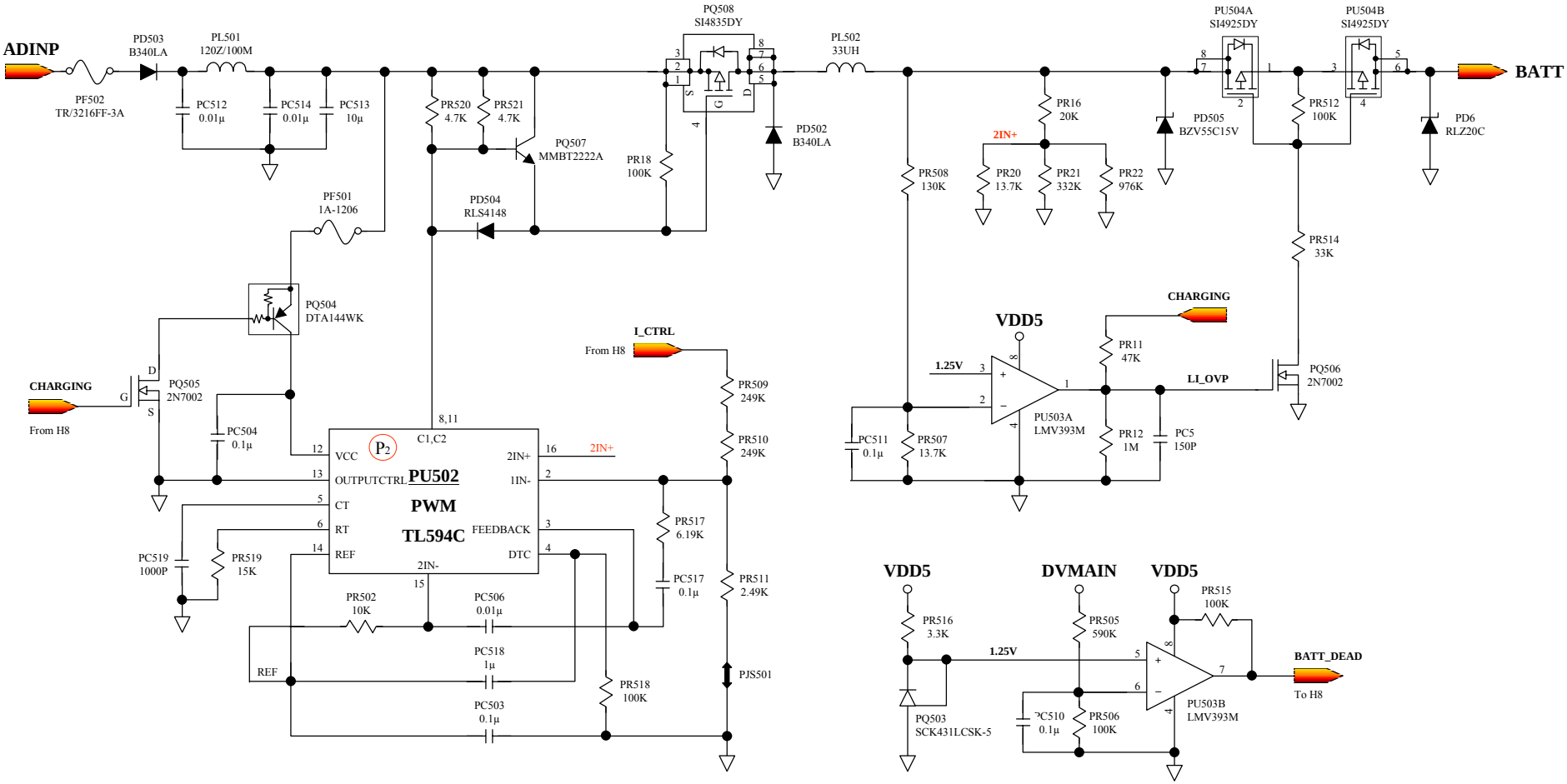


8081 N/B Maintenance

8.1 No Power – Charging

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

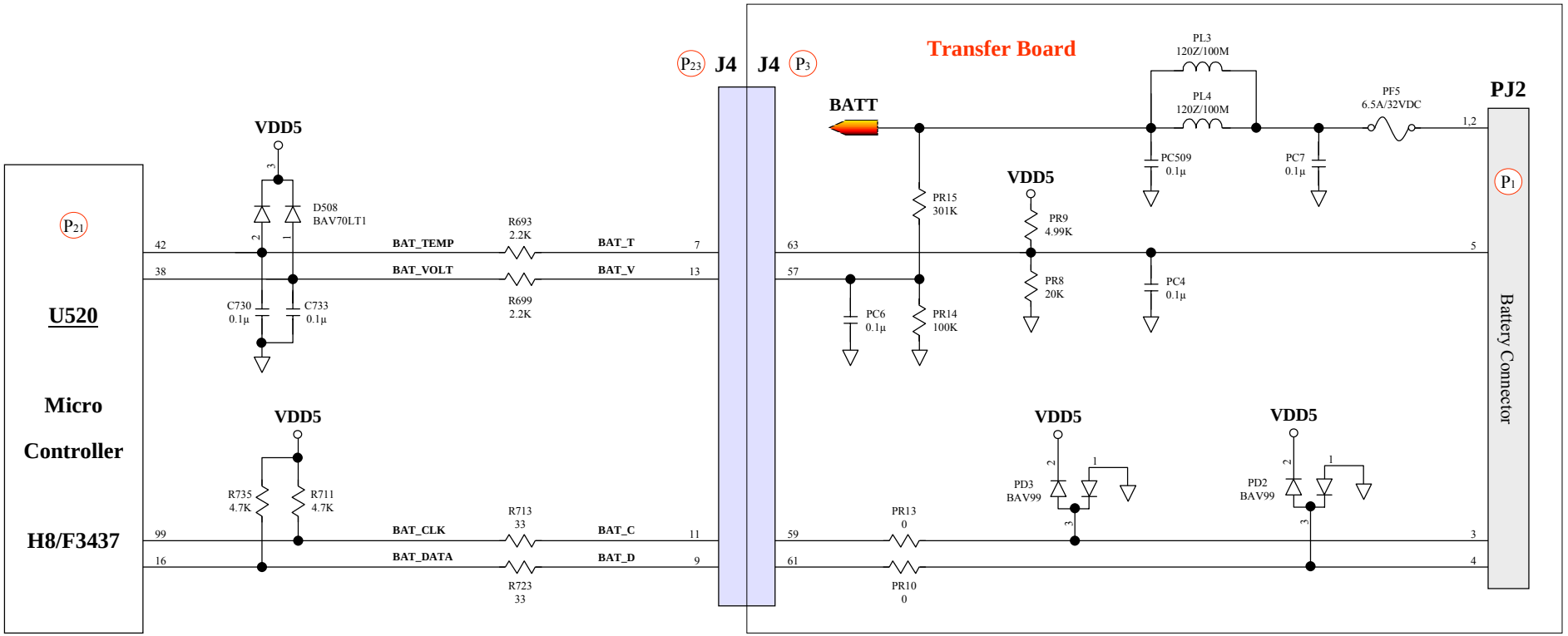
Transfer Board



8081 N/B Maintenance

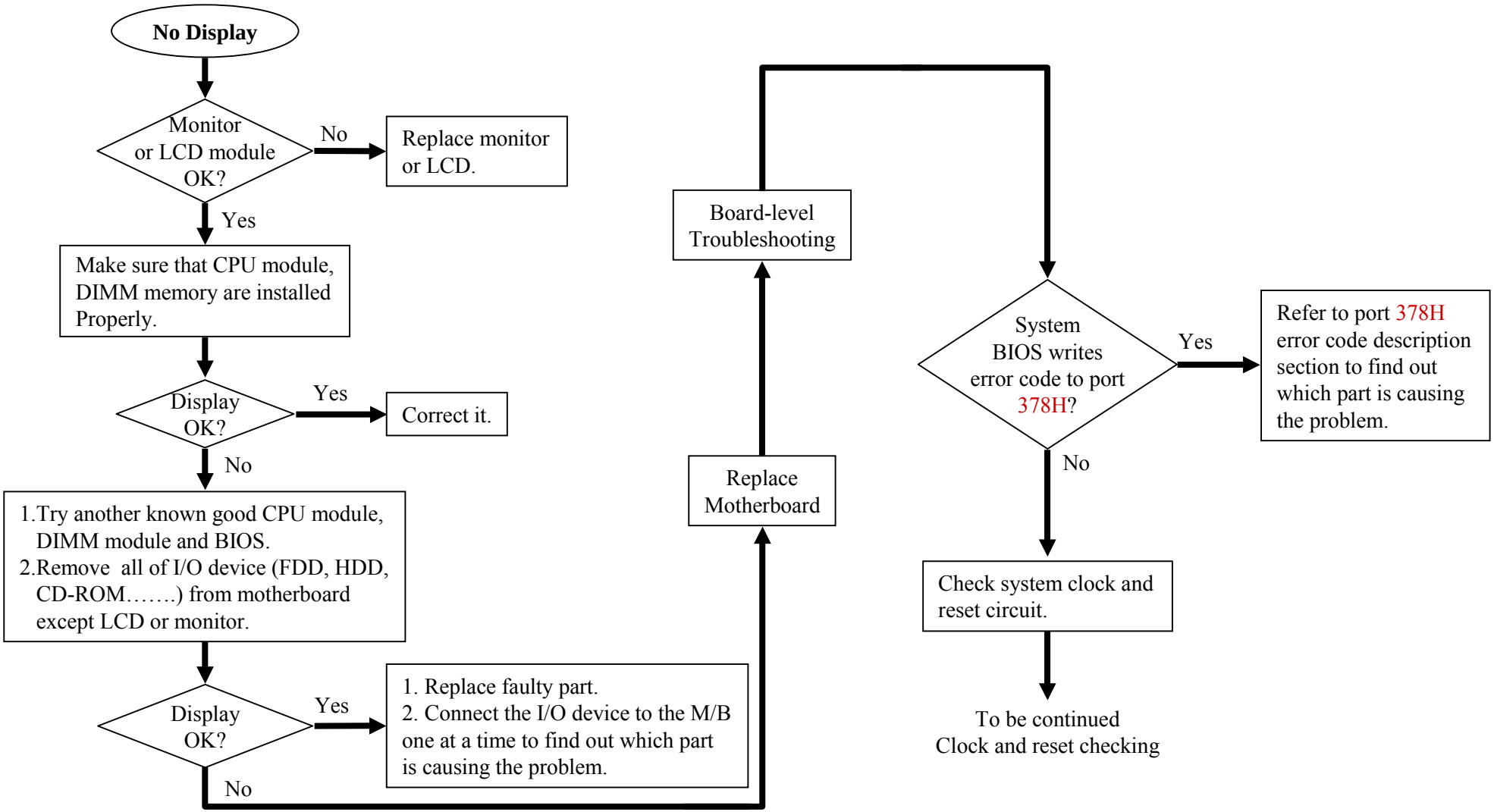
8.1 No Power – Discharge

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.2 No Display

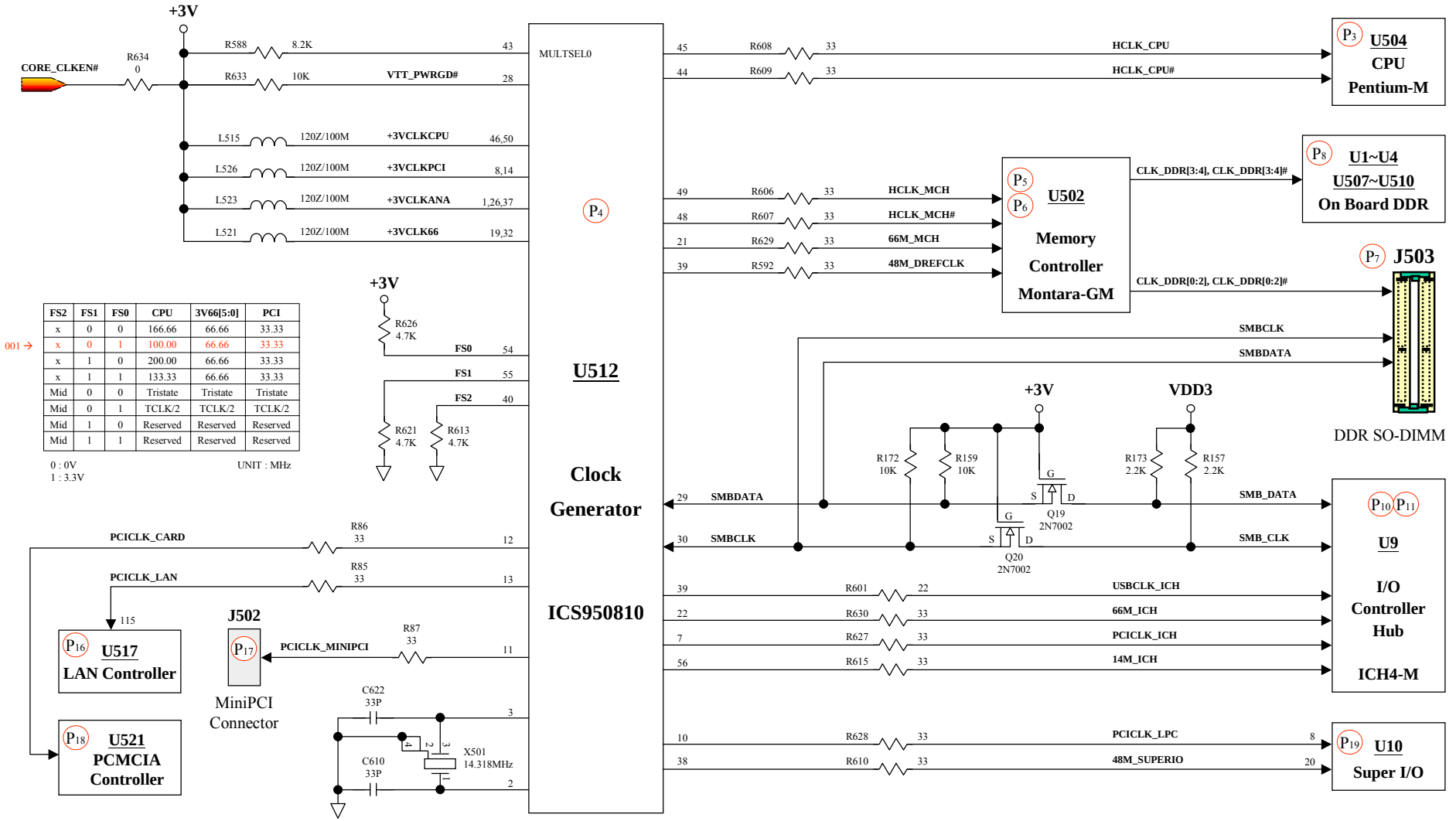
There is no display on both LCD and VGA monitor after power on.



8081 N/B Maintenance

8.2 No Display

****** System Clock Check ******

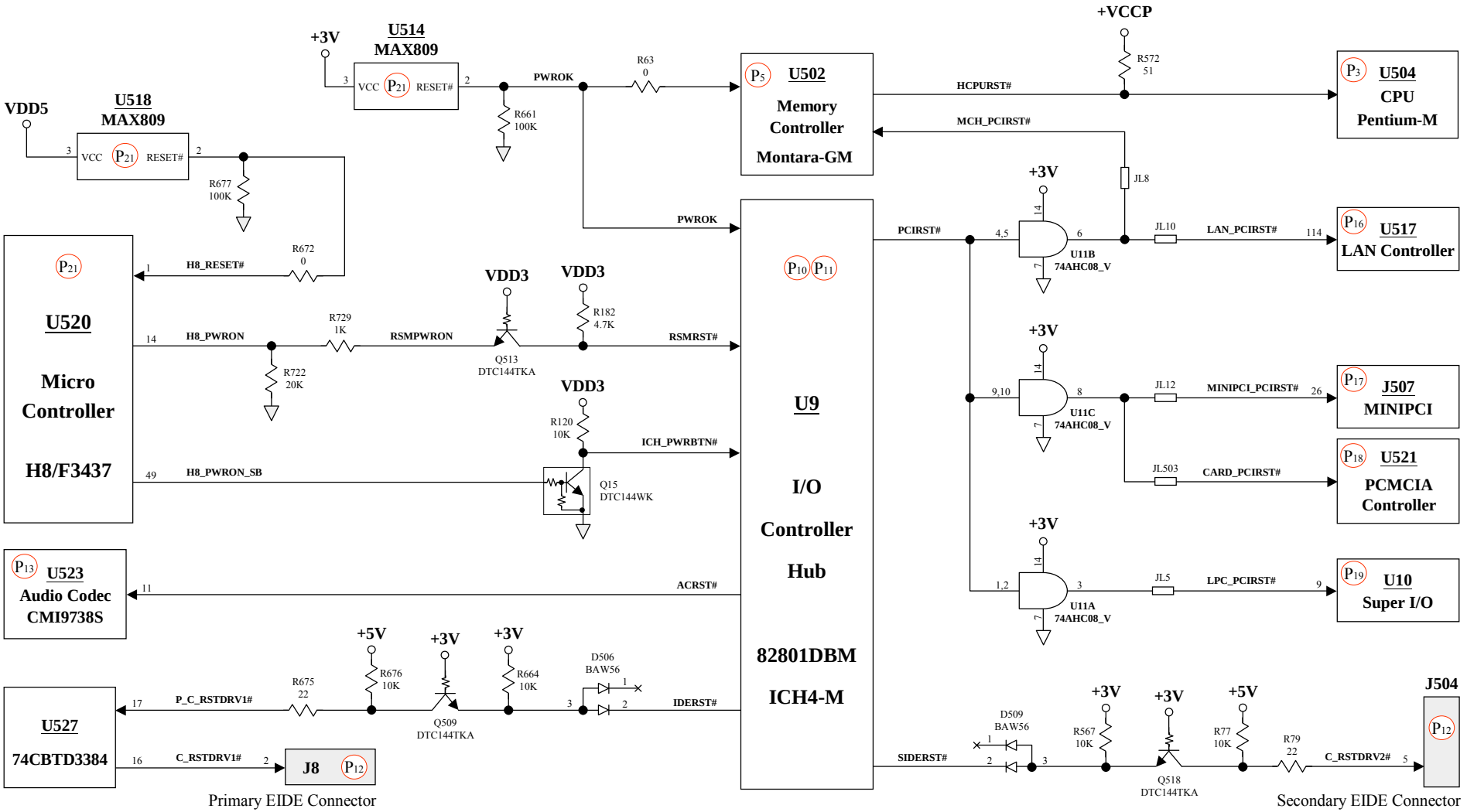


FS2	FS1	FS0	CPU	3V66[5:0]	PCI
x	0	0	166.66	66.66	33.33
x	0	1	100.00	66.66	33.33
x	1	0	200.00	66.66	33.33
x	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

8081 N/B Maintenance

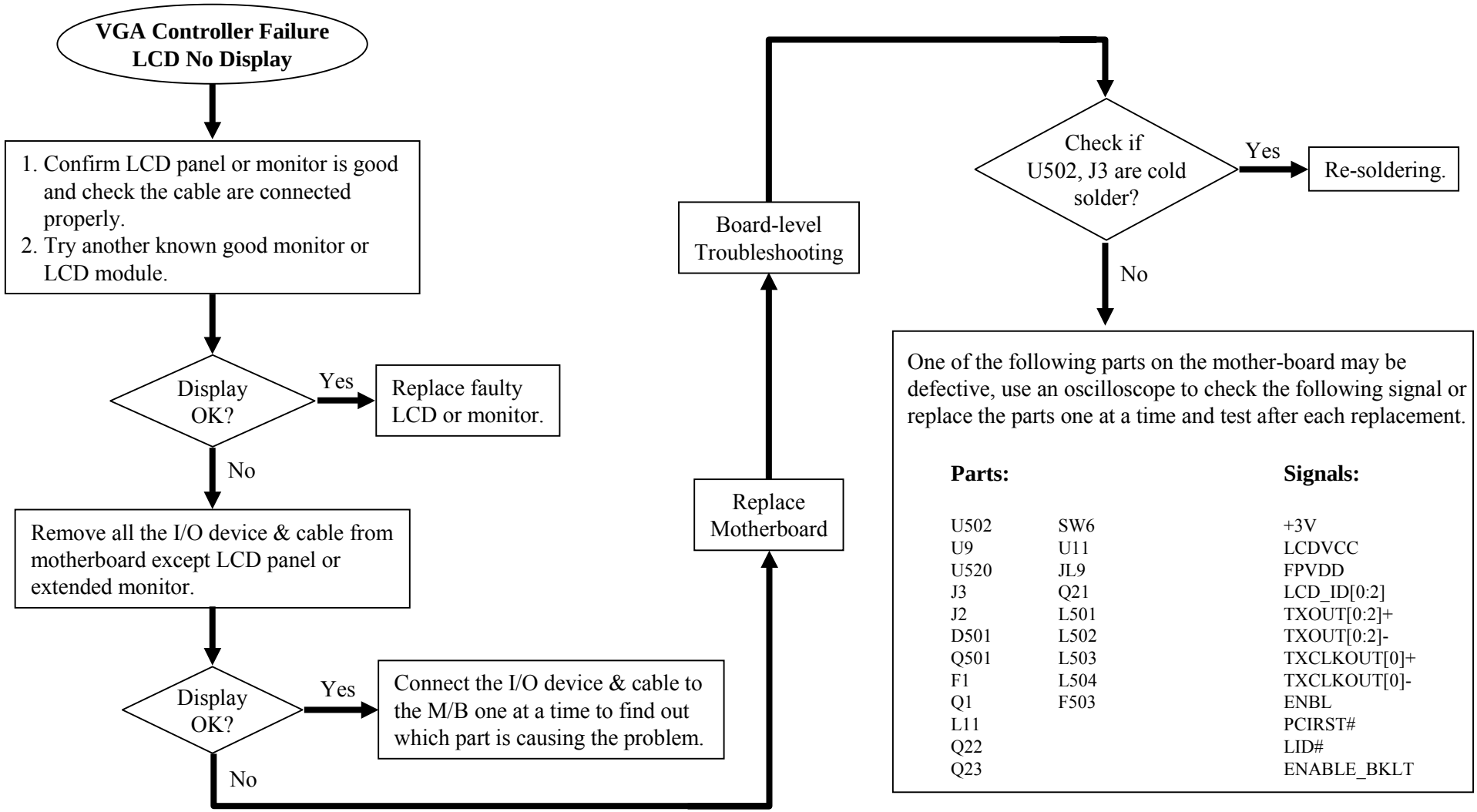
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

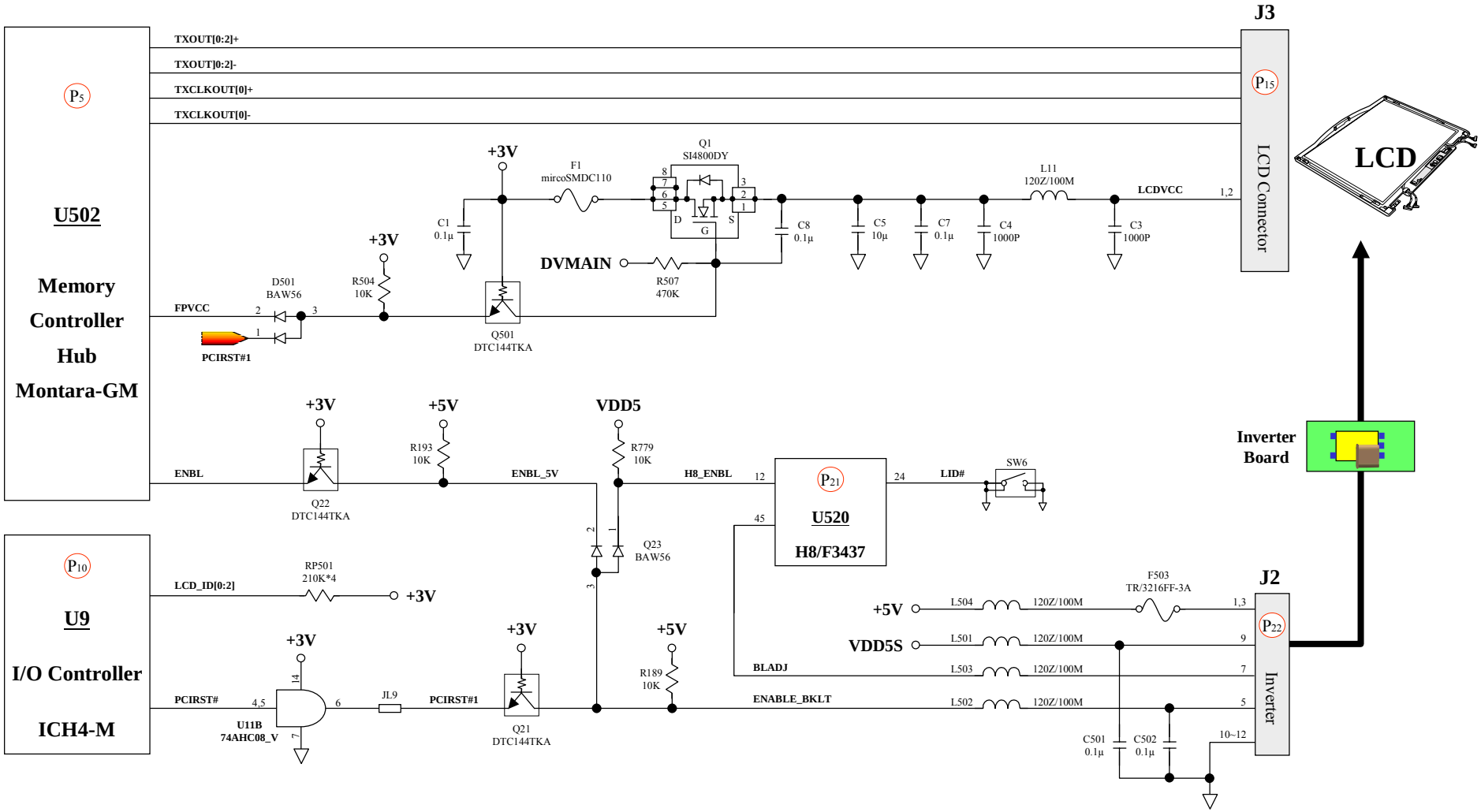
There is no display or picture abnormal on LCD although power-on-self-test is passed.



8081 N/B Maintenance

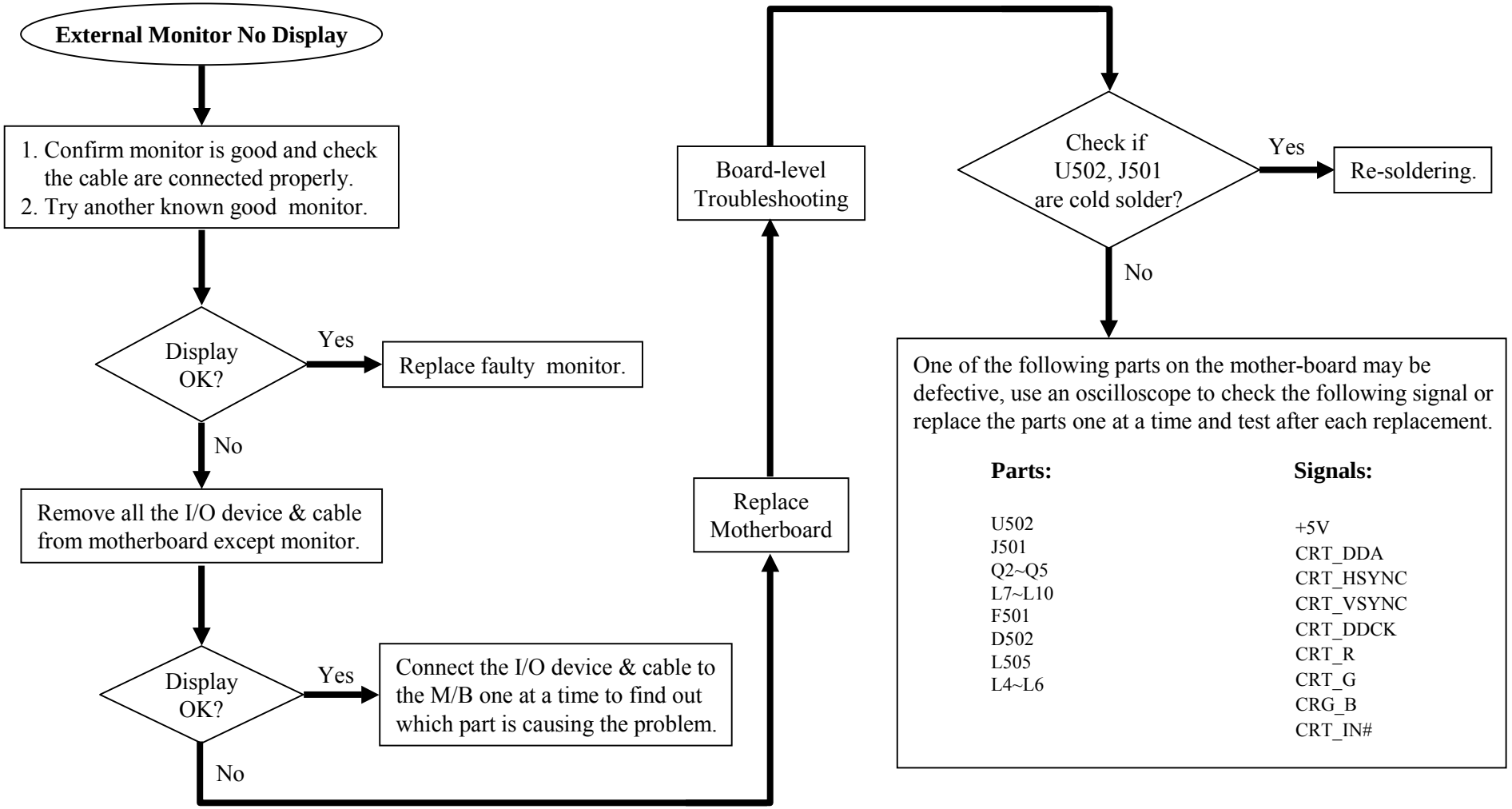
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



8.4 External Monitor No Display

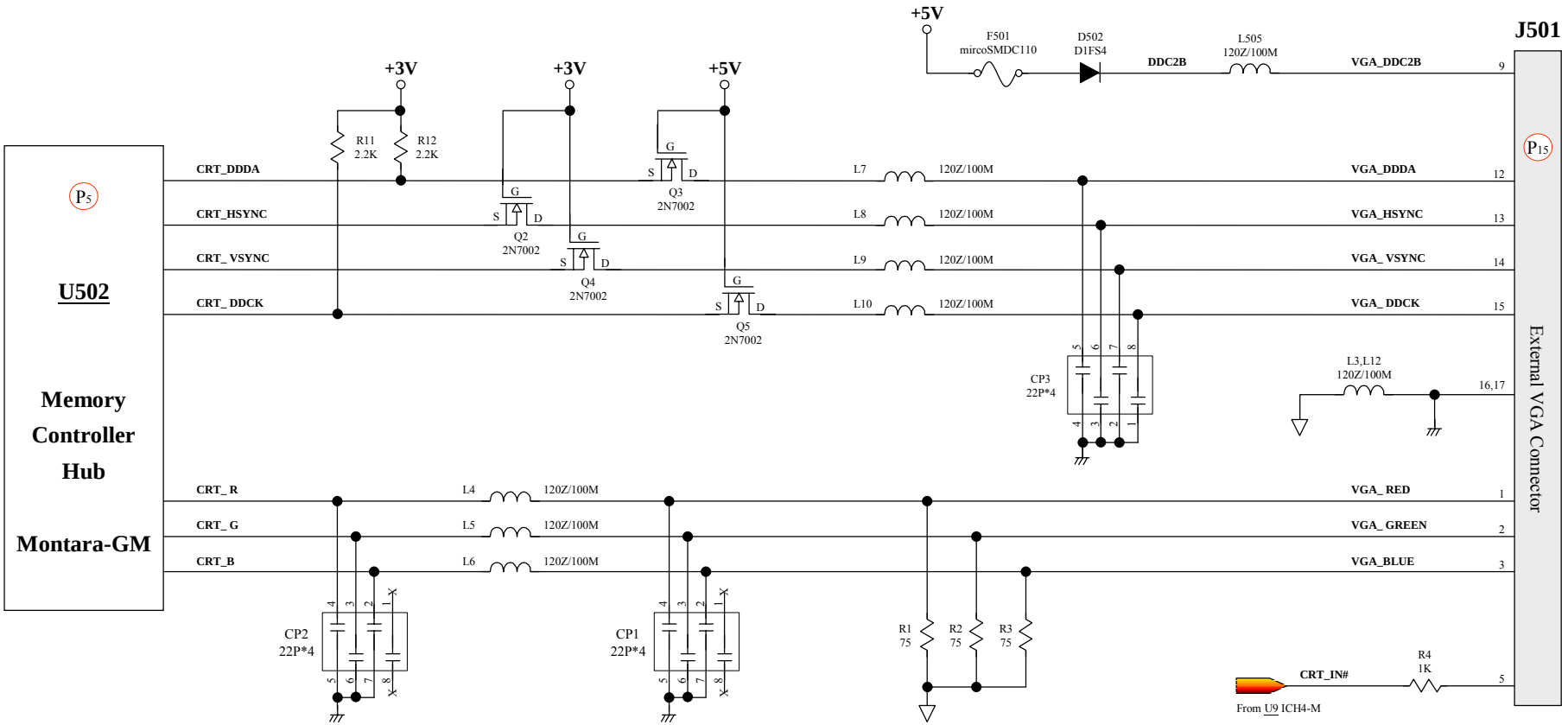
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8081 N/B Maintenance

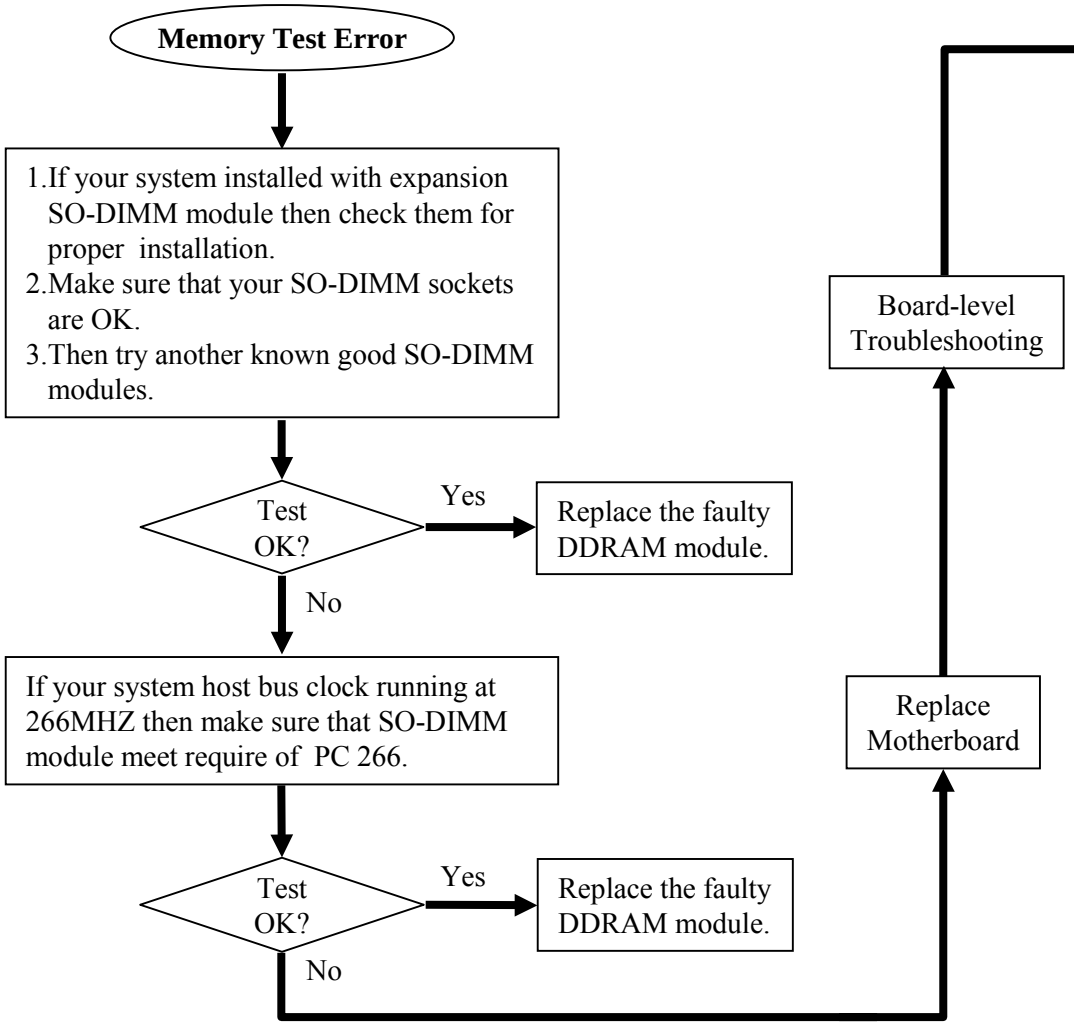
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

RP2~RP14
RP505~RP517
RP18~RP21
U502
U9
U512
U1~U4
U507~U510
J503
Q19
Q20
R606
R607
R629

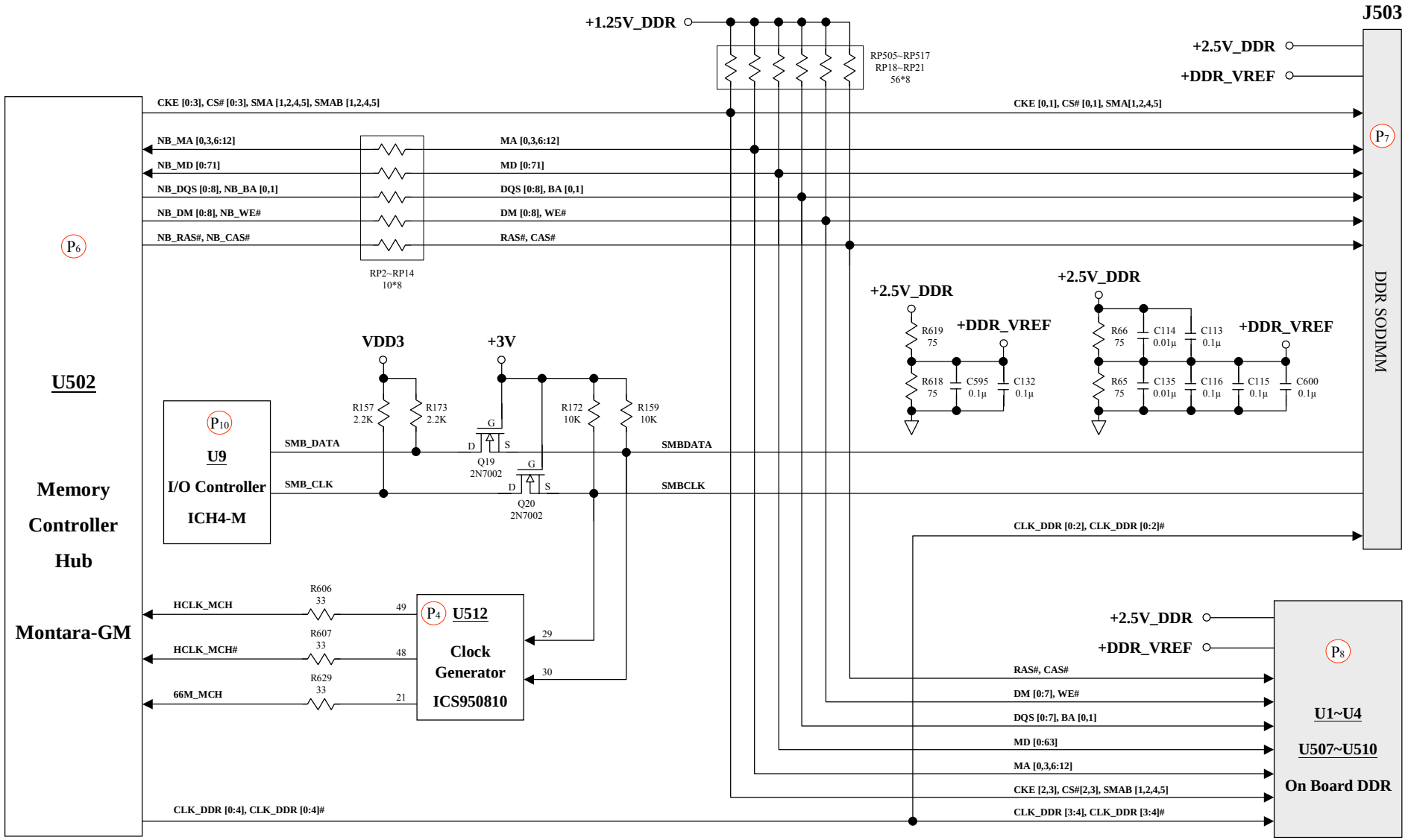
Signals:

+1.25V_DDR
+2.5V_DDR
+DDR_VREF
CKE [0:3]
CS# [0:3]
SMA [1,2,4,5]
SMAB [1,2,4,5]
NB_MA [0,3,6:12]
NB_MD [0:63]
NB_DQS [0:7]
NB_BA [0,1]
NB_CB [0:7]
NB_DM [0:8]
NB_RAS#
NB_CAS#
NB_WE#
SMB_DATA
SMB_CLK
HCLK_MCH
HCLK_MCH#
66M_MCH
CLK_DDR [0:4]
CLK_DDR [0:4]#

8081 N/B Maintenance

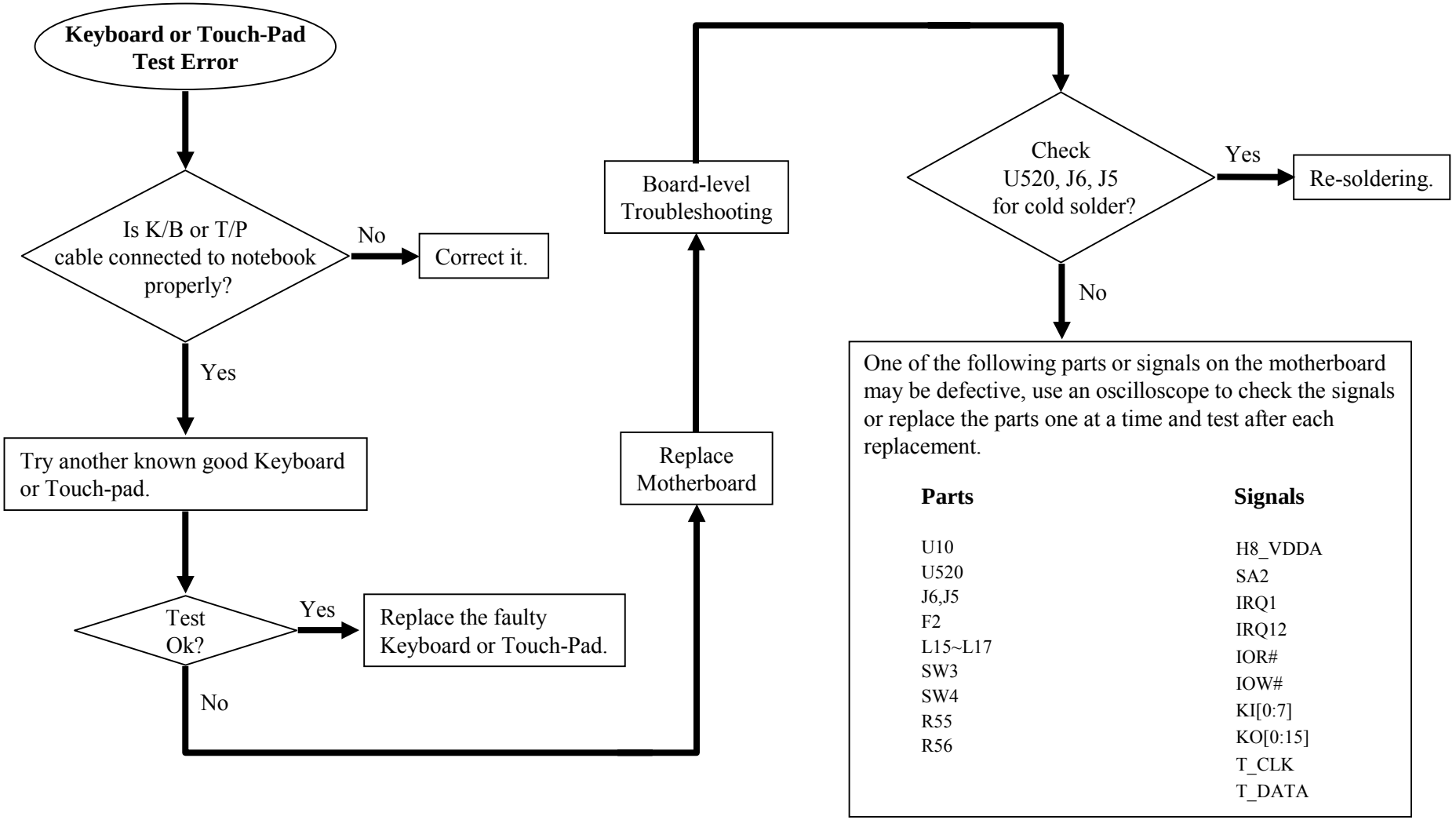
8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.



8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

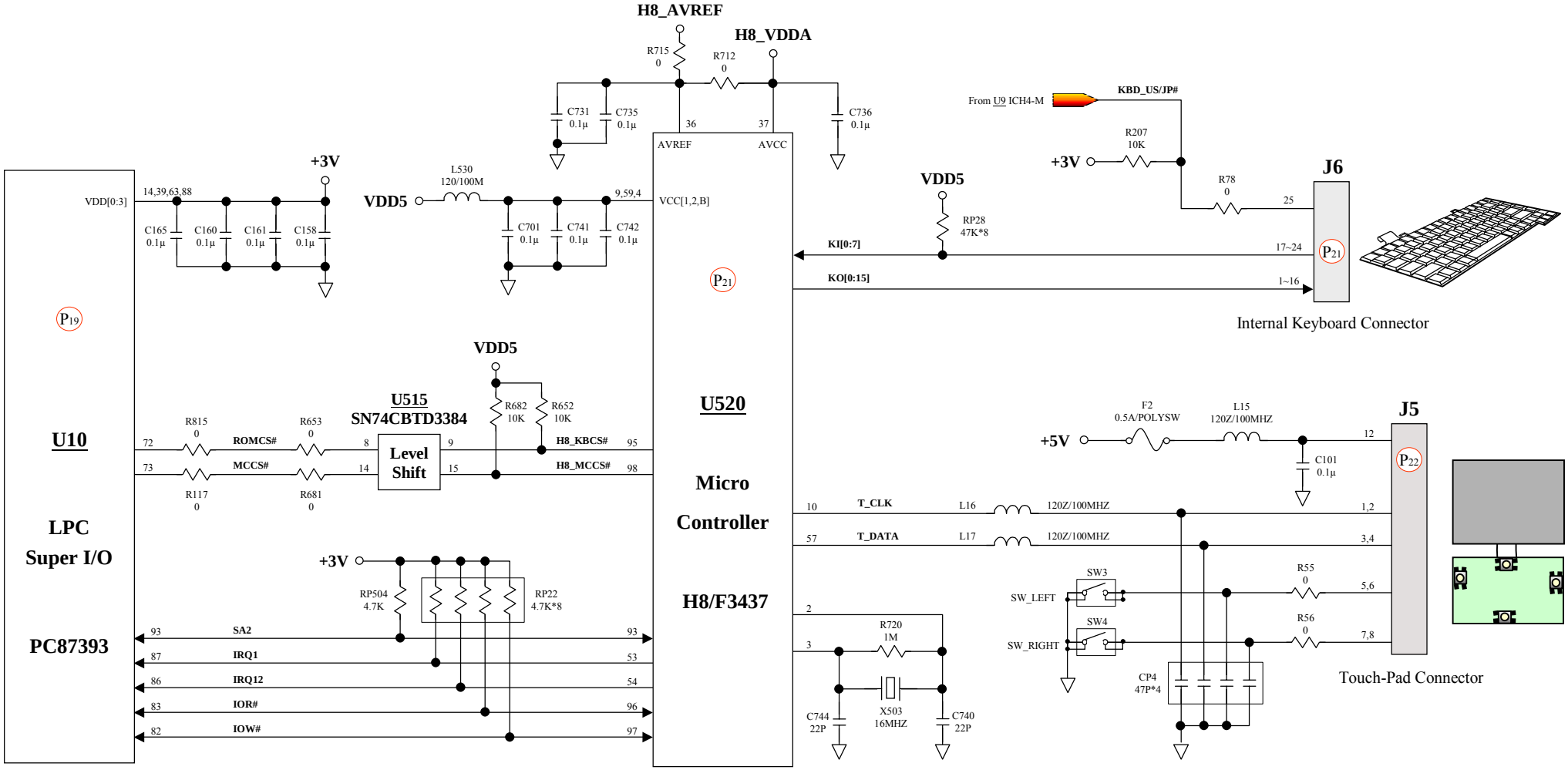
Error message of keyboard or touch-pad failure is shown or any key does not work.



8081 N/B Maintenance

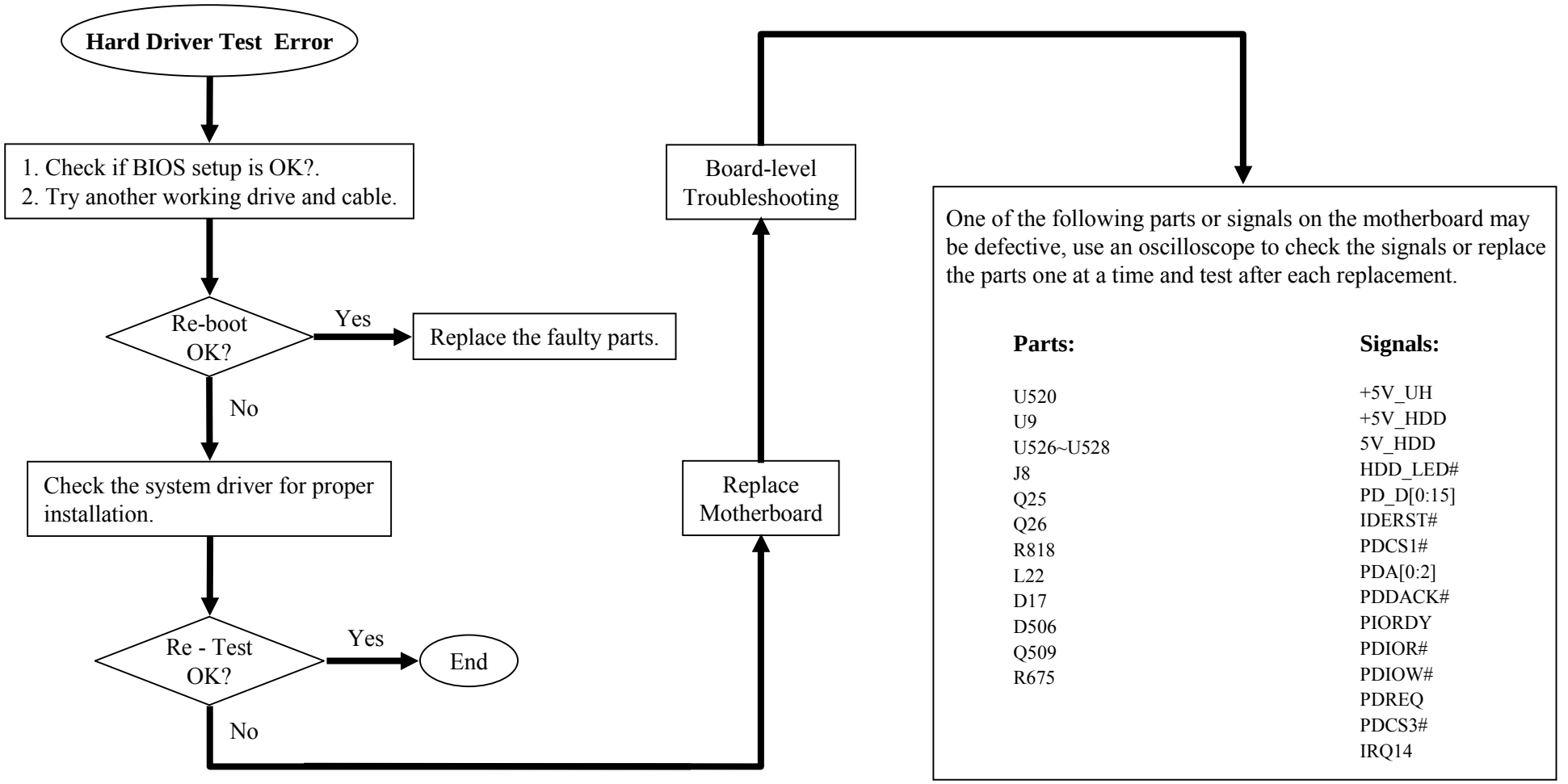
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Drive Test Error

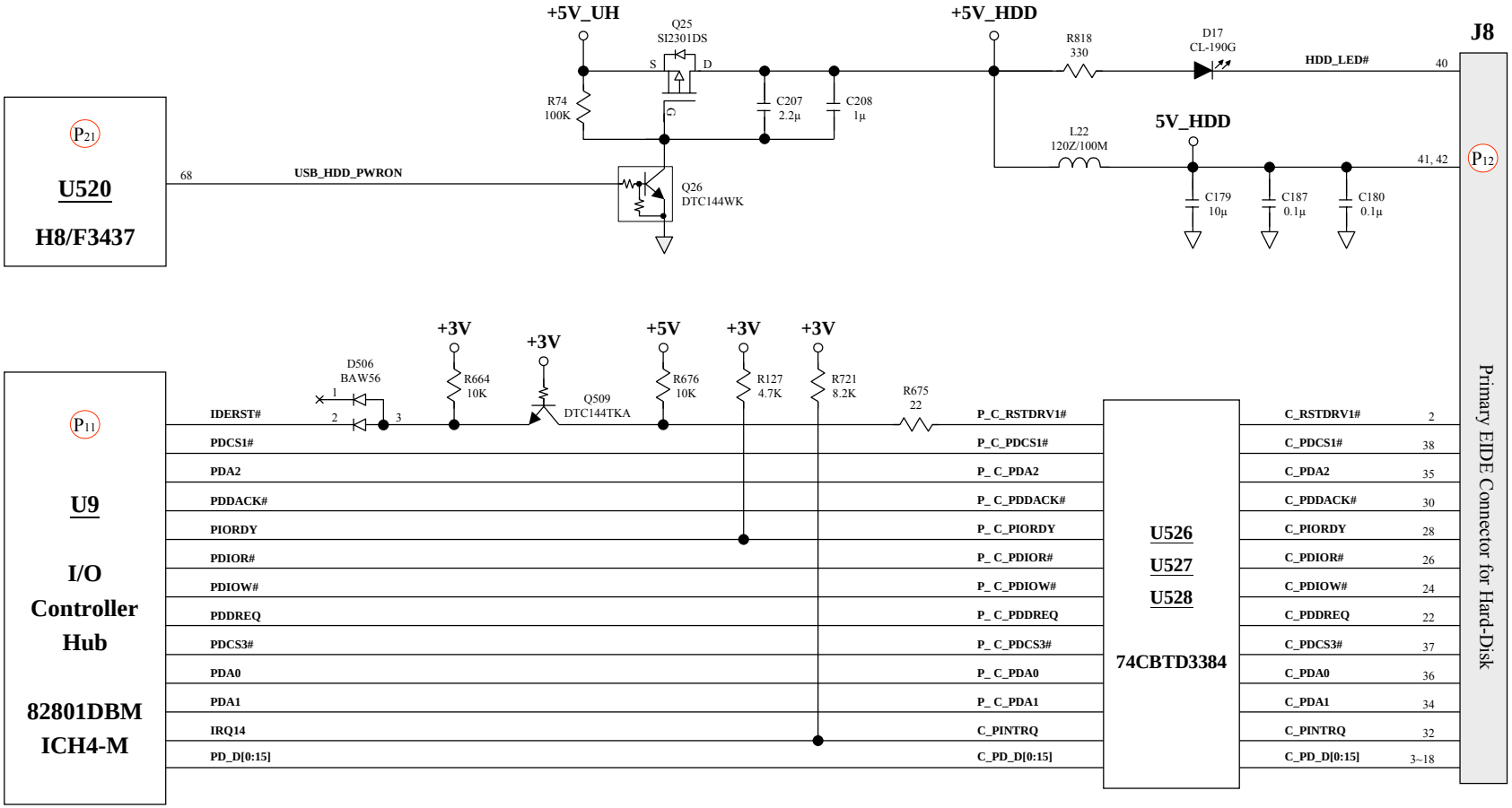
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8081 N/B Maintenance

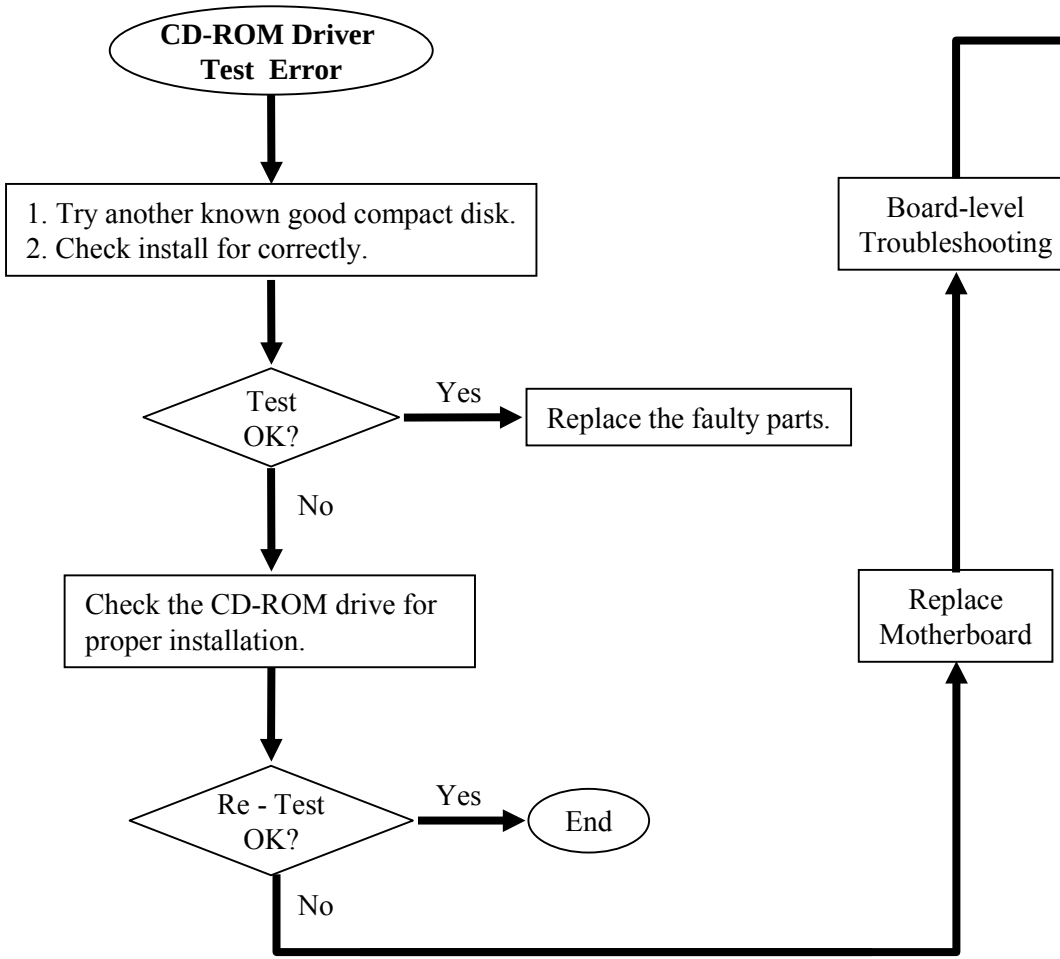
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



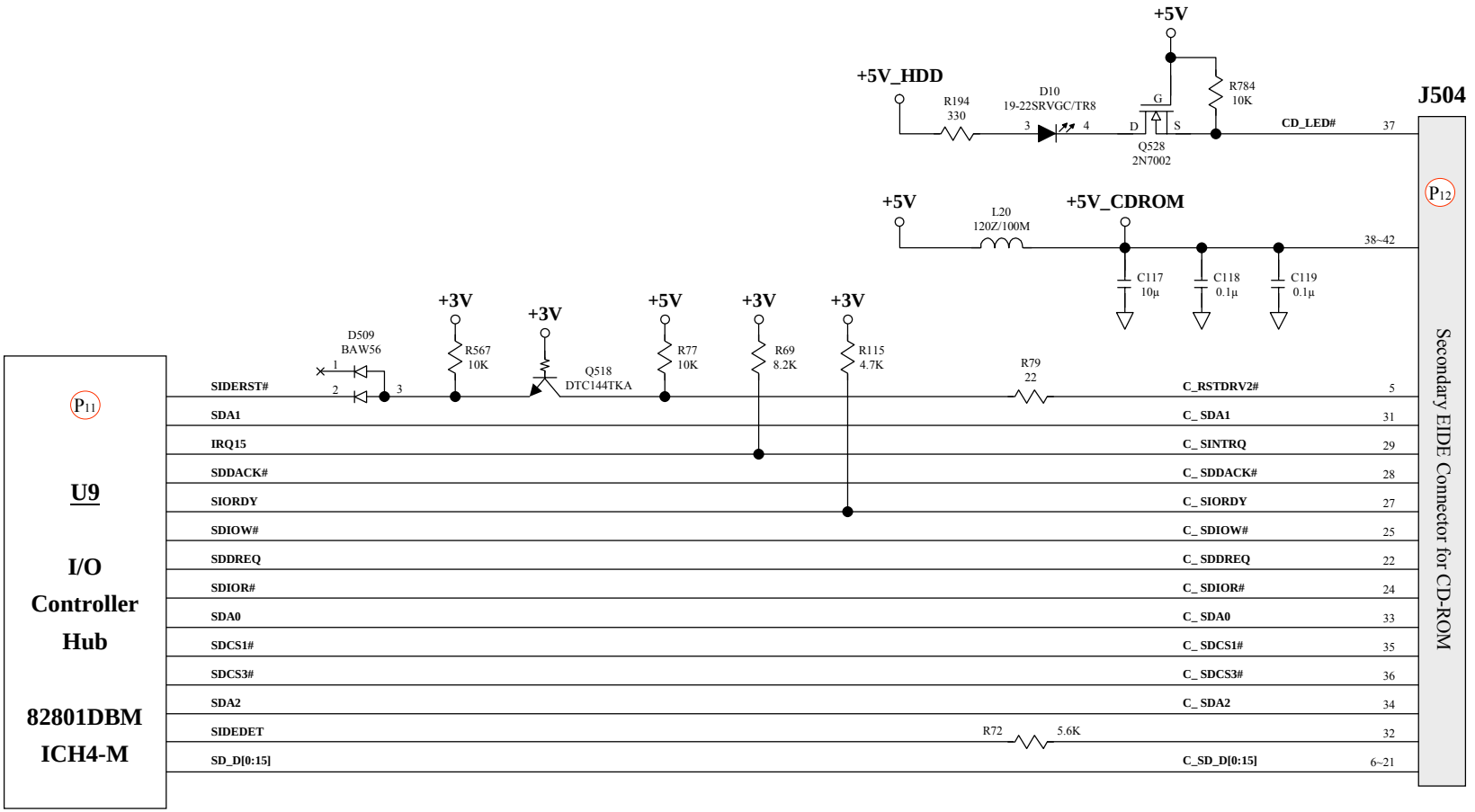
One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U9	+5V_CDROM
J504	CD_LED#
R194	SD_D]0:5]
D10	SIDERST#
Q528	SDA[0:2]
L20	IRQ15
D509	SDDACK#
Q518	SIORDY
R79	SDIOW#
R72	SDDREQ
	SDIOR#
	SDCS1#
	SDCS3#
	SIDEDET

8081 N/B Maintenance

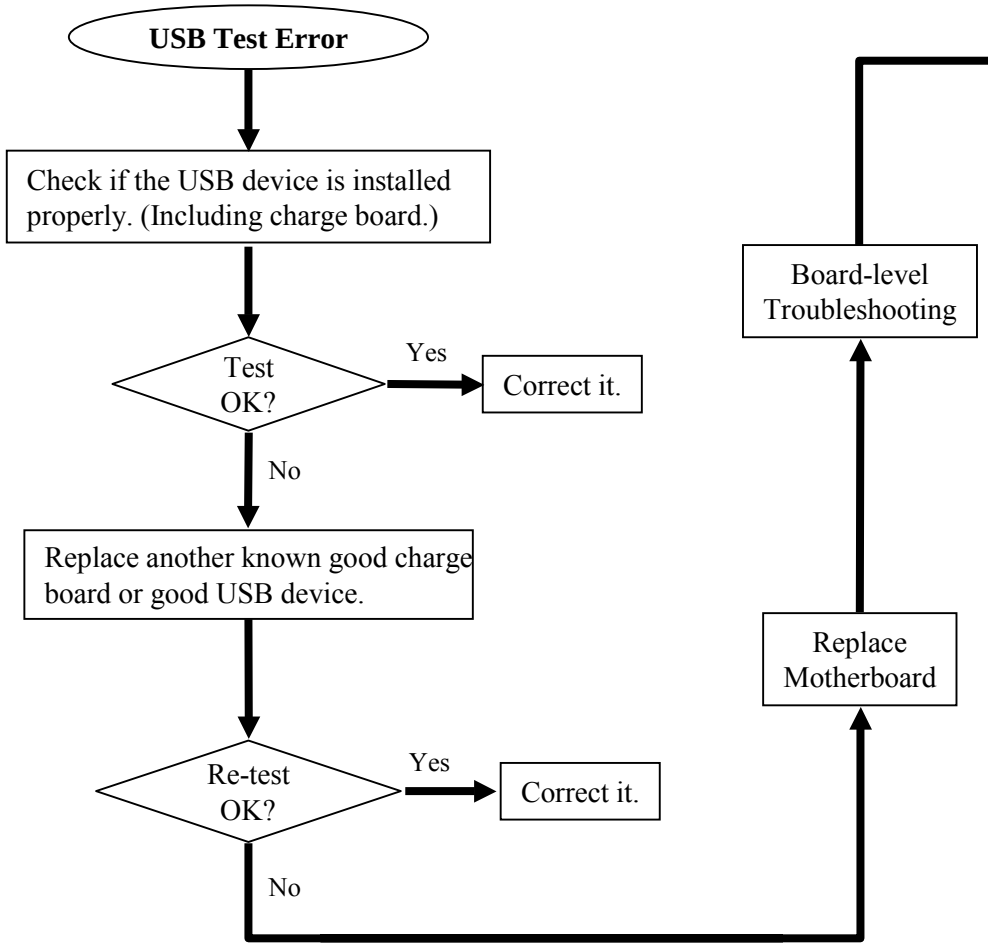
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error

An error occurs when a USB I/O device is installed.



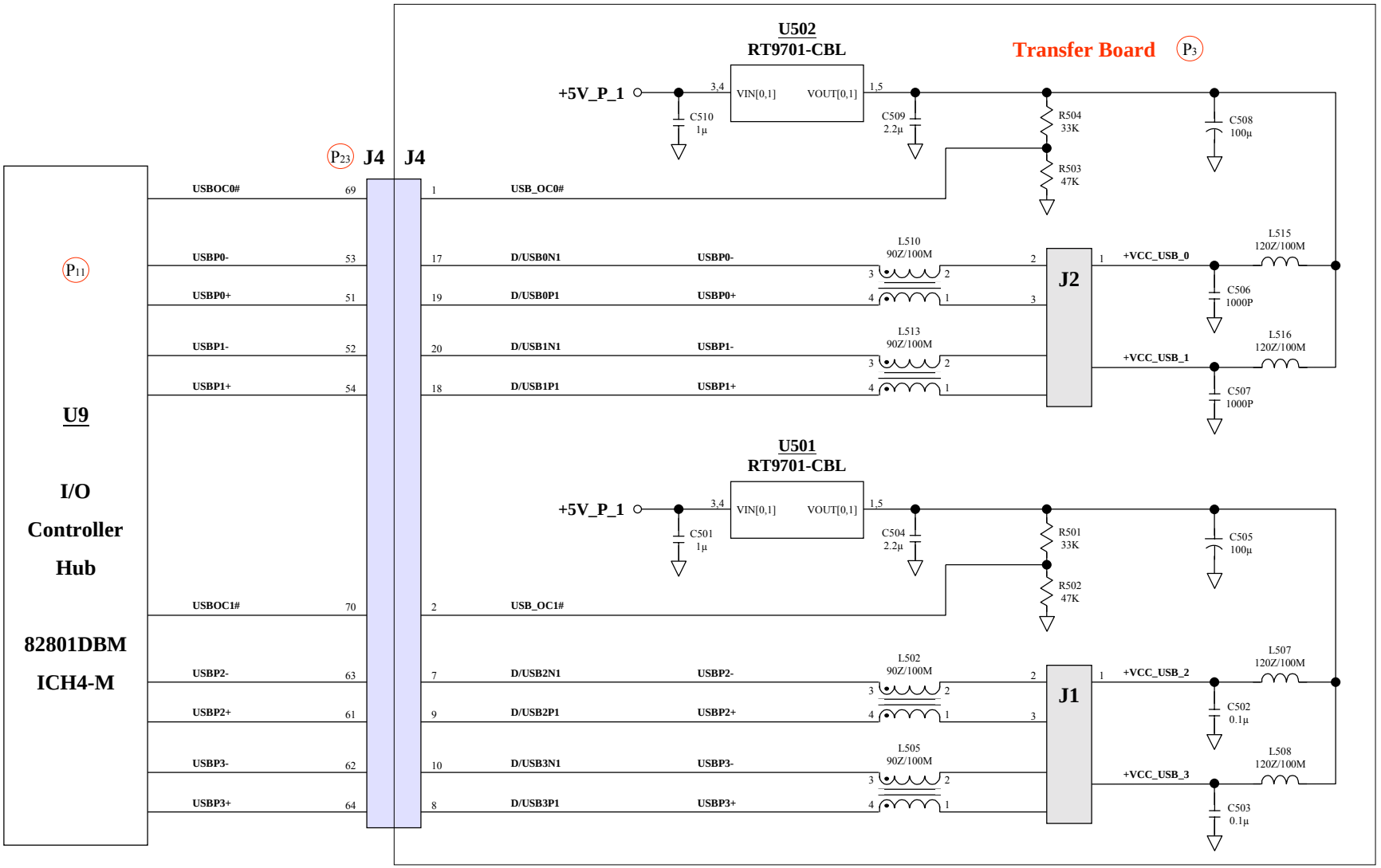
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
J4	+5V_P_1
U502	USBOC0#
L510	USBP[0:3]+
L513	USBP [0:3 -
L515	USBOC1#
L516	
J2	
U501	
L502	
L505	
L507	
L508	
J1	
M/B Board	
U9	
J4	

8081 N/B Maintenance

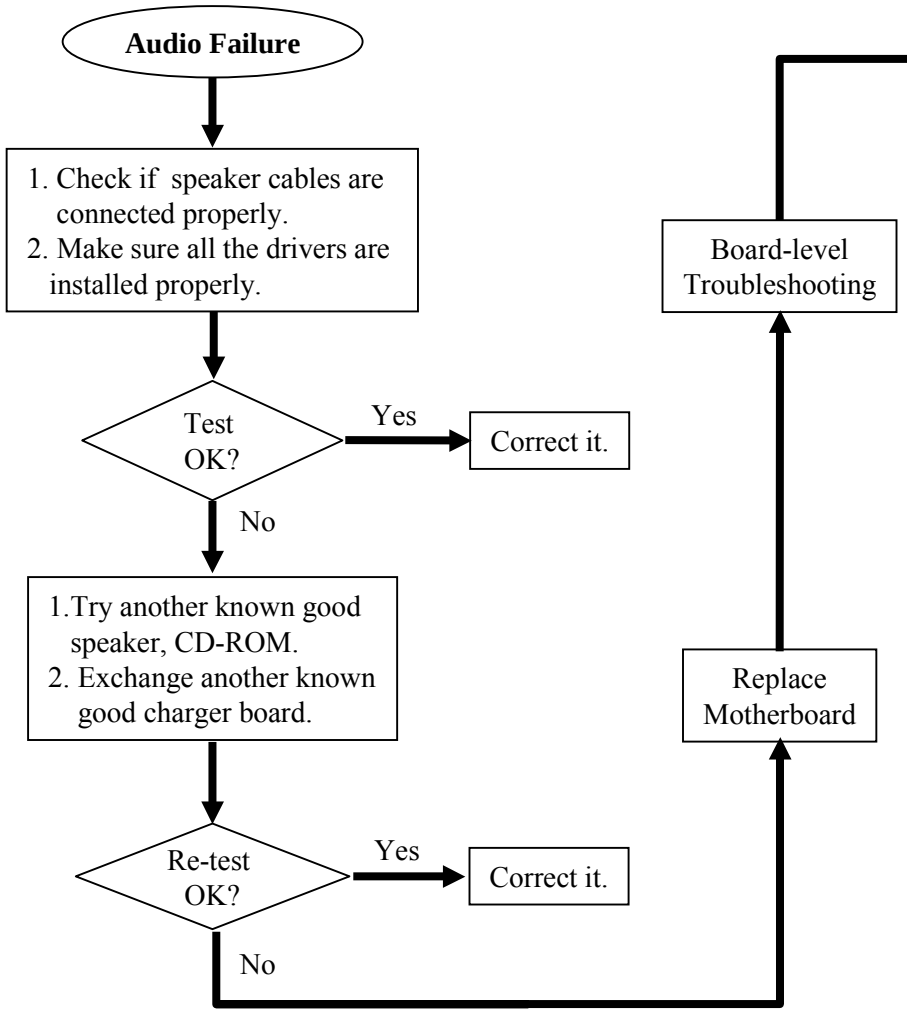
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



8.10 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U523	AOUT_R
U15	AOUT_L
J9	LINE_IN#
R775	SPK_OFF
R768	
L539	
L540	
R772	

2. If no sound cause of MIC, check the following parts & signals:

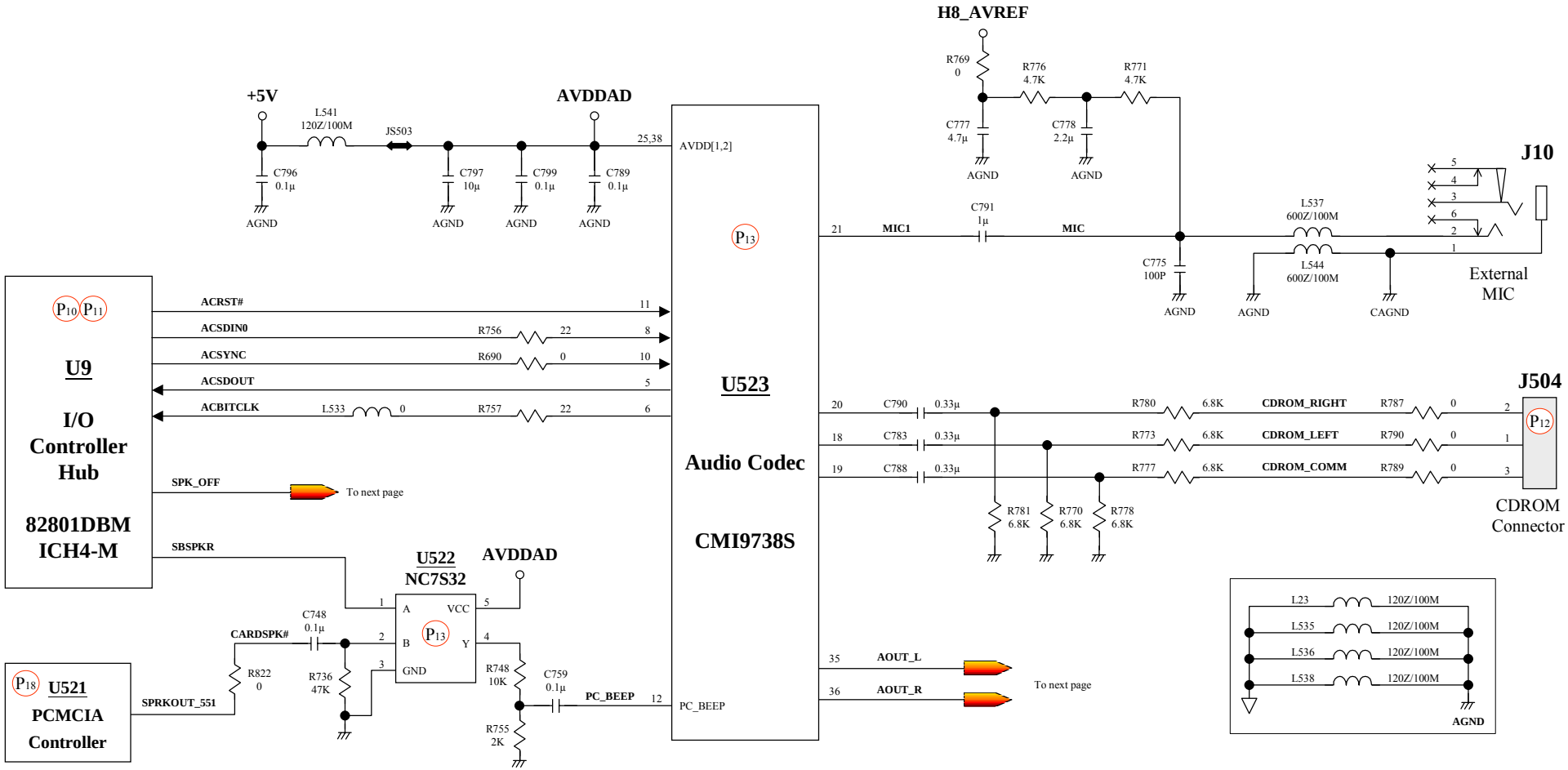
Parts:	Signals:
U9	H8_AVREF
U523	MIC1
J10	
L537	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U523	CDROM_LEFT
J504	CDROM_RIGHT
R787	CDROM_COMM
R790	
R789	

8.10 Audio Failure – Audio IN

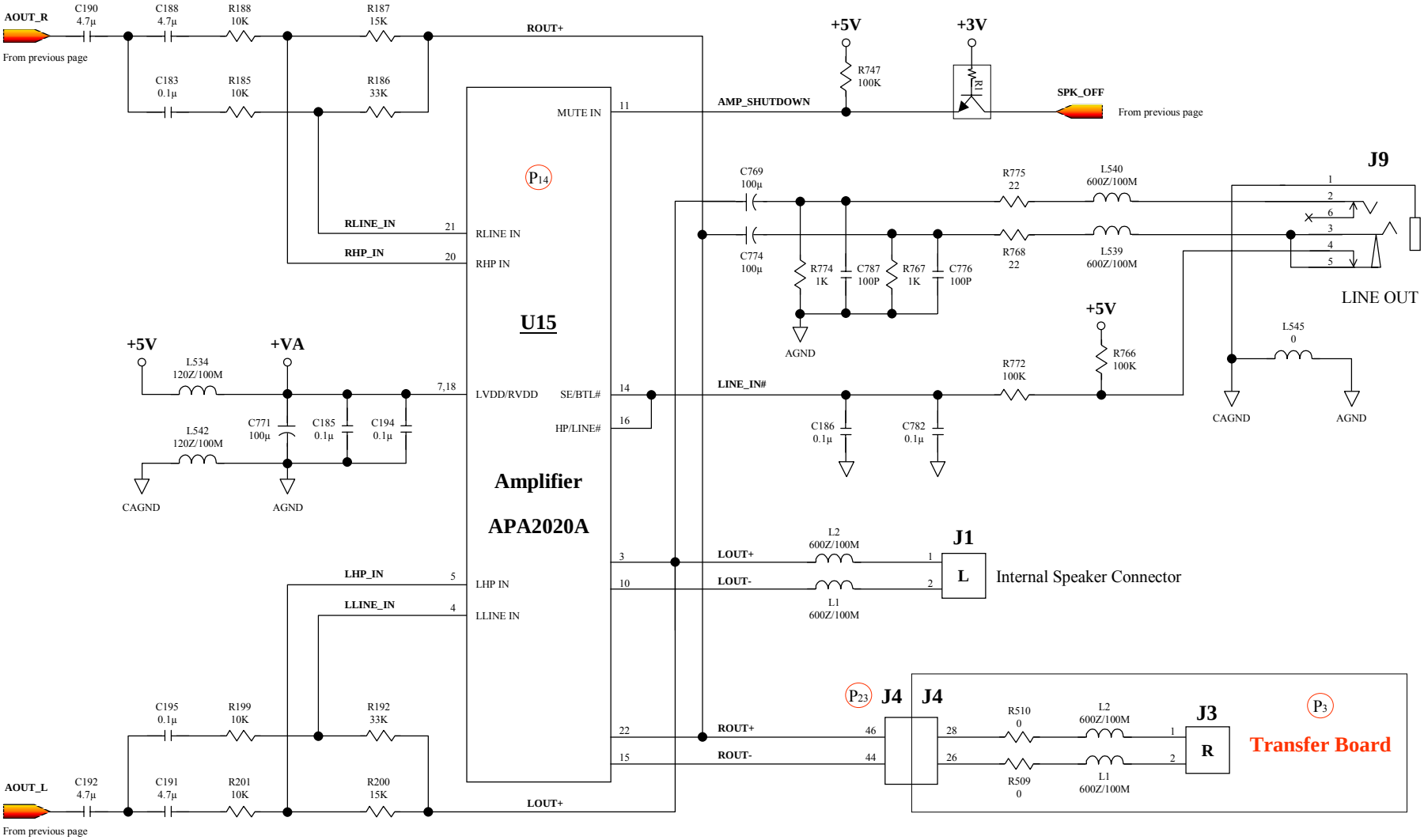
No sound from speaker after audio driver is installed.



8081 N/B Maintenance

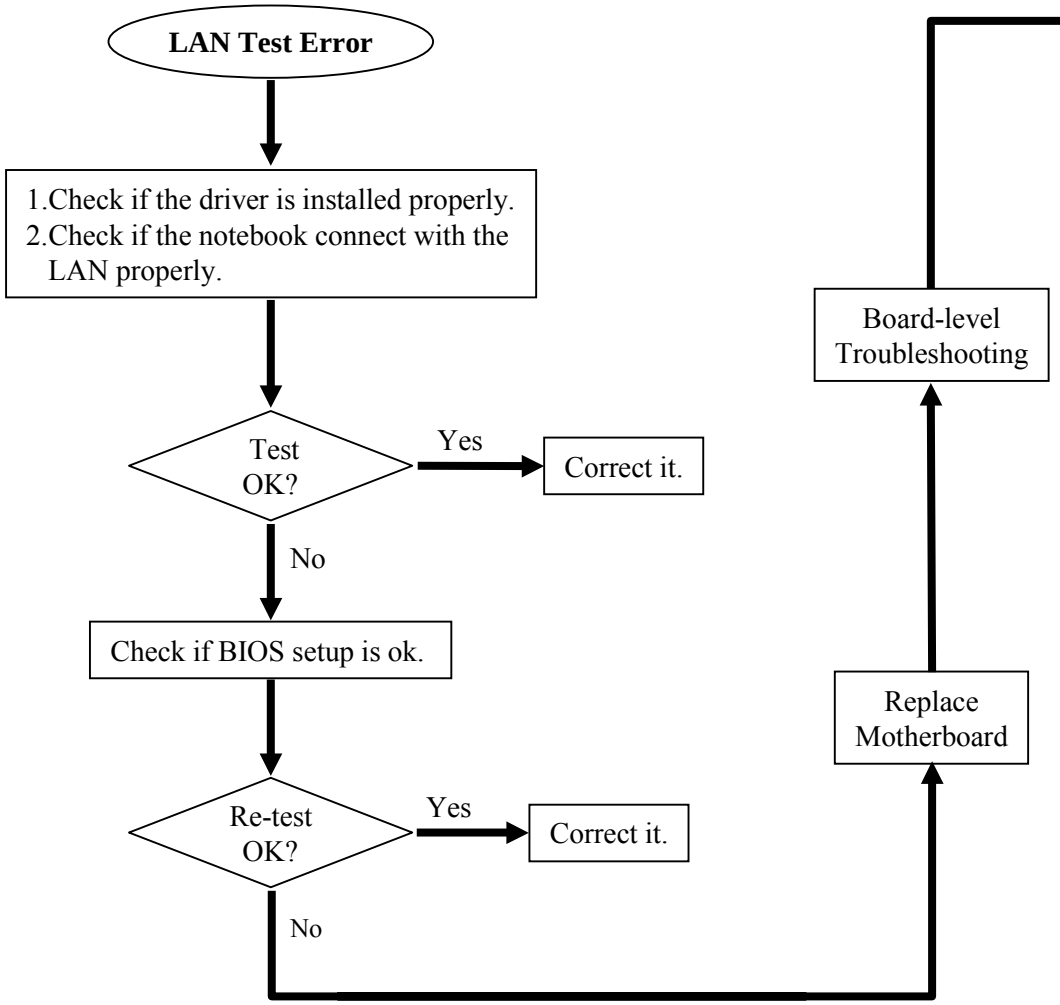
8.10 Audio Failure – Audio OUT

No sound from speaker after audio driver is installed.



8.11 LAN Test Error

An error occurs when a LAN device is installed.



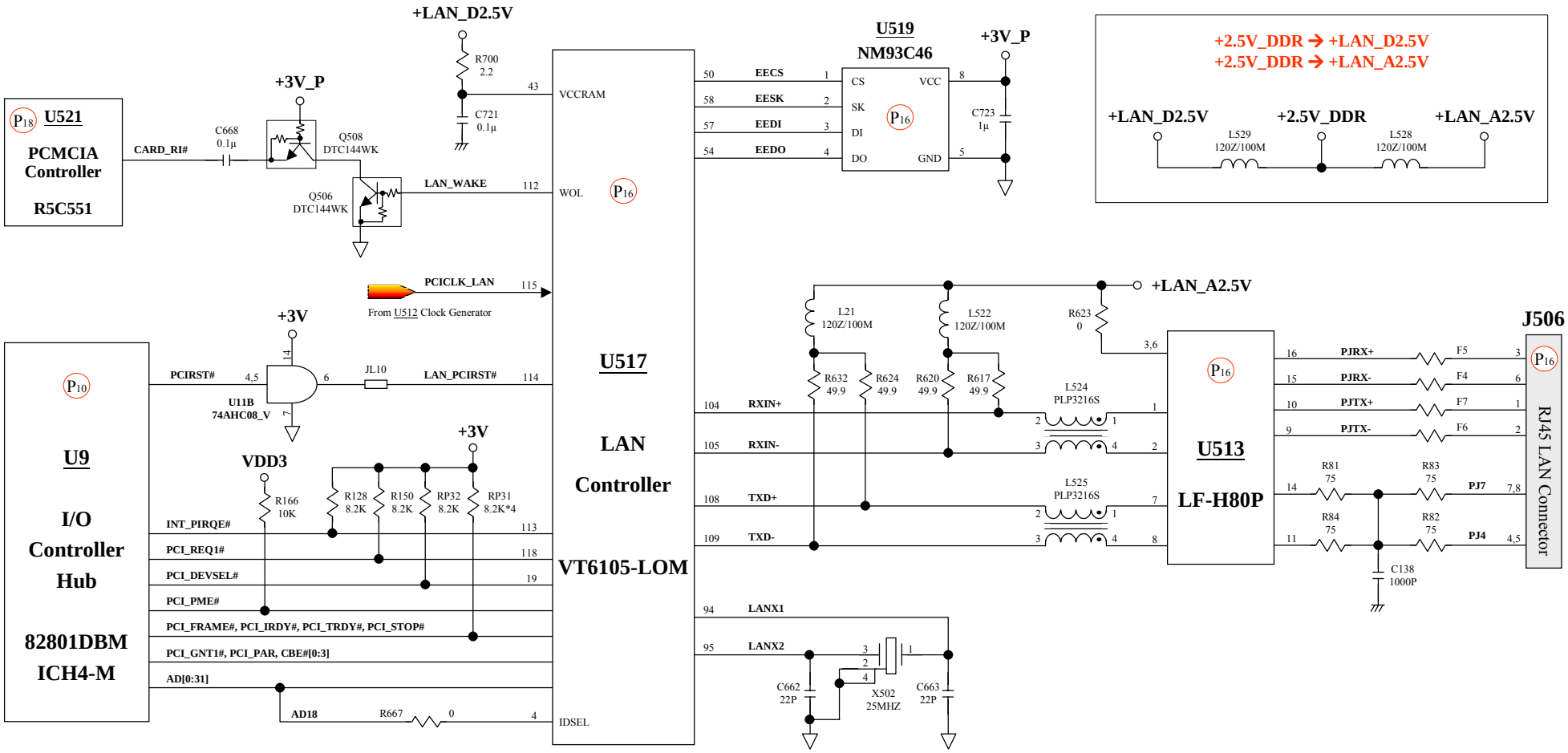
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U521	+LAN_A2.5V	PCI_GNT1#
U9	+LAN_D2.5V	PCI_PAR
U517	CARD_RI#	AD[0:31]
U513	PCICLK_LAN	CBE#]0:3]
U519	PCIRST#	RXIN+
J506	IN_PIRQE#	RXIN-
Q508	PCI_REQ1	TXD+
Q506	PCI_FRAME#	TXD-
U11	PCI_DEVSEL#	EECS
JL10	PCI_TRDY#	EESK
R667	PCI_IRDY#	EEDI
L524	PCI_PME#	EEDO
L525	PCI_STOP#	

8081 N/B Maintenance

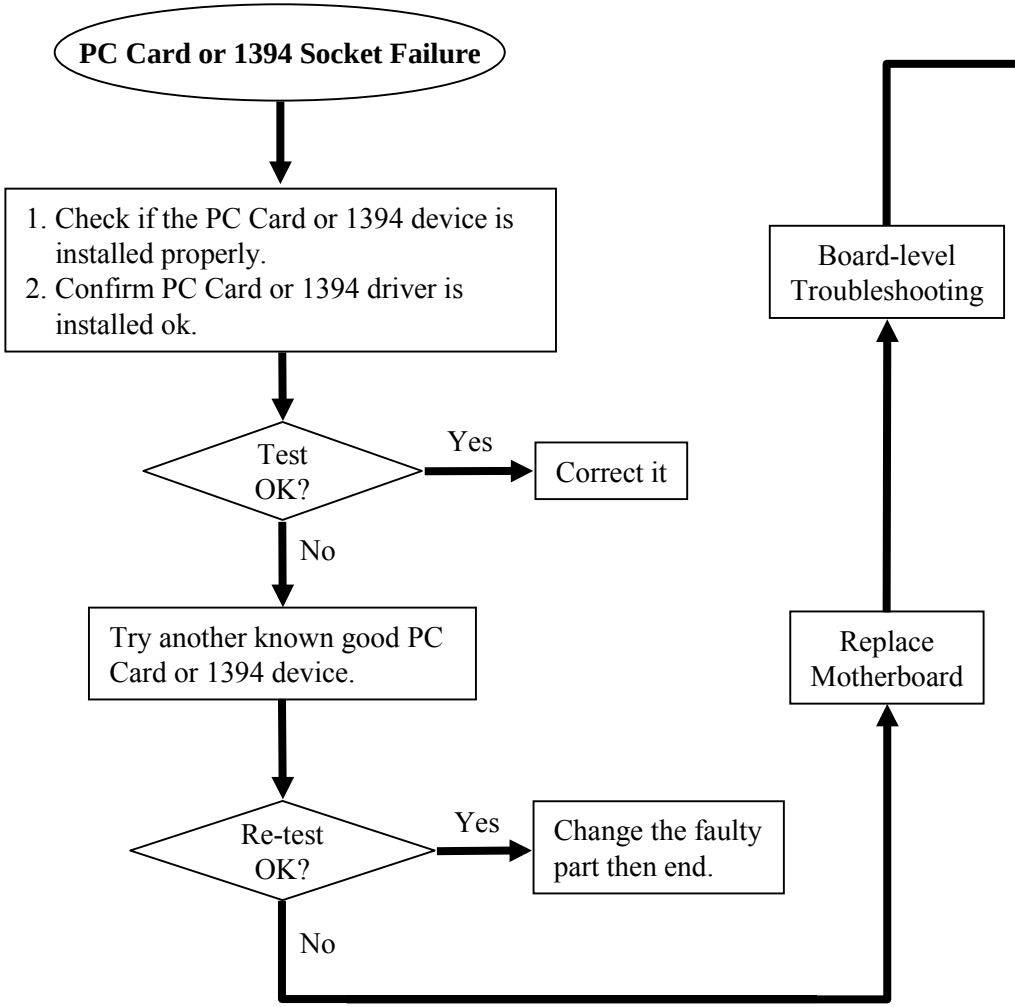
8.11 LAN Test Error

An error occurs when a LAN device is installed.



8.12 PC Card & 1394 Socket Failure

An error occurs when a PC card or 1394 device is installed.



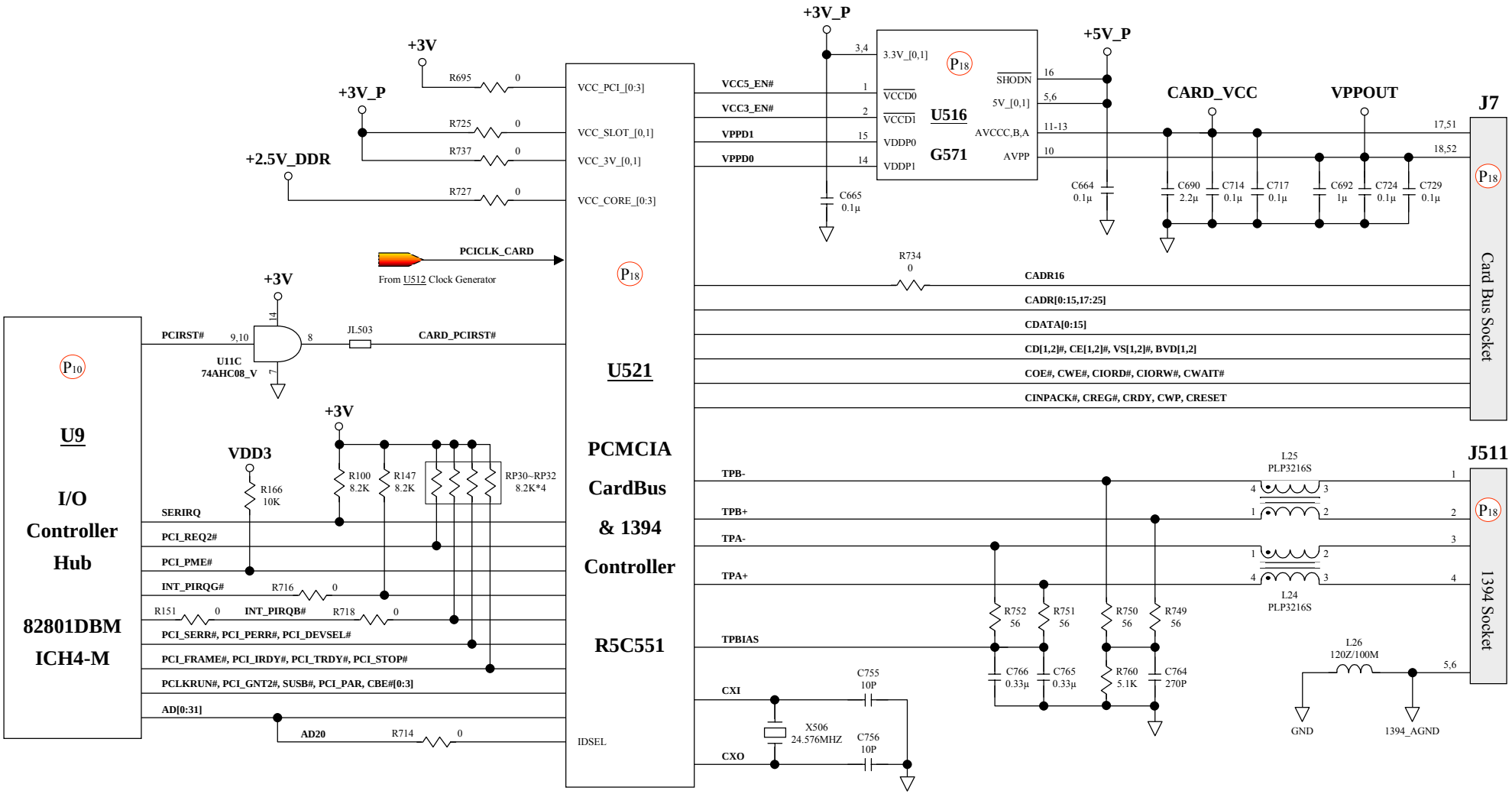
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U9	PCICLK_CARD	PIC_PAR
U521	PCIRST#	SERIRQ
U516	PCI_REQ2#	SUSB#
J7	PCI_SERR#	AD[0:31]
U11	PCI_PERR#	CBE#[0:3]
JL503	PCI_DEVSEL#	VCC5_EN#
R714	PCI_FRAME#	VCC3_EN#
R734	PCI_IRDY#	VPPD0
R151	PCI_TRDY#	VPPD1
R718	PCI_STOP#	TPB-
R716	PCLKRUN#	TPB+
L25	PCI_PME#	TPA-
L24	PCI_GNT2#	TPA+
J511		TPBIAS

8081 N/B Maintenance

8.12 PC Card & 1394 Socket Failure

An error occurs when a PC card or 1394 device is installed.



9. Spare Parts List - 1

Part Number	Description	Location(S)
442672600031	AC ADPT ASSY;19V,3.16A,DELTA,706	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667850001	AK;01-EN,BOX,8081	
541667850031	AK;EN,8081,UTILITY ONLY	
346678500006	AL-FOIL;LCD-LED,8081	
346678500007	AL-FOIL;T/P,8081	
421678500003	ANTENNA;LCD,MPT,8081	
441677370001	BATT ASSY;11.1V,4.0Ah,LI,BL3240	
441677370002	BATT ASSY;11.1V,4.0Ah,LI,CASE CL	
441677370003	BATT ASSY;11.1V,4.0Ah,LI,CORE PA	
338536010008	BATTERY;LI,3.6V/2.0AH,18650,SANY	
340678500015	BEZEL ASSY;COMBO,MKE,8081	
284505551001	BFM-SC,IC;R5C551,PCI-CARDBUS/139	U521
242670800113	BFM-WORLD MARK;WINXP,7521N	
221675340001	BOX;AK,8080	
342672200010	BRACKET;CD-ROM,8500	
342678500003	BRACKET;I/O,8081	
342676400008	BRACKET;L,LCD-QDI,APOLLON	
342676400009	BRACKET;R,LCD-QDI,APOLLON	
342678500004	BRACKET;VGA,8081	
342676400003	BRACKET-REAR,CDROM,APOLLON	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C10,C12,C14,C20,C22,C23,C24,C2
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C21,C6,C7

Part Number	Description	Location(S)
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R	C13
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C5
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C1,C2,C3
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C114,C135,C145,C147,C155,C156
272073103401	CAP;.01U ,CR,25V ,10%,0603,X7R,S	C7
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC23,PC37,PC56,PC57
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC506,PC507,PC512,PC514
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C4,C8
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	C162
272072104702	CAP;.1U ,16V,+80-20%,0603,Y5V,S	C113,C115,C116,C132,C563,C570
272073104501	CAP;.1U ,25V,+80-20%,0603,Y5V,S	PC1
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C1,C100,C101,C102,C103,C104,C
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C502,C503,PC1,PC11,PC3,PC4,PC
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C11,C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC517
272005104502	CAP;.1U ,CR,50V,20%,0805,Z5U,SM	PC16,PC38,PC6
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	C8
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC28,PC35,PC4,PC546,PC548
272072224402	CAP;.22U ,16V ,10%,0603,X7R,SMT	PC14
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C766,C783,C788,C790
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C124,C127,C129,C133,C138
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C199,C3,C4,C802,PC20,PC25,PC2
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C506,C507,PC10,PC508,PC519,PC
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C2,C775,C776,C787,PC30,PC32,P
272010101301	CAP;100P,2KV,5%,1206,NPO,SMT,onl	C14

9. Spare Parts List - 2

Part Number	Description	Location(S)
272991107502	CAP;100u,6.3V,20%,18m,SMT,MASTUS	C505,C508
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C699,C755,C756
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC511,PC532,PC560
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C10,C117,C12,C13,C14,C146,C14
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	PC19,PC43,PC44,PC536
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC503,PC504,PC505,PC506,PC5
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC513,PC522,PC523
272075121301	CAP;120P,CR,50V,5%,0603,NPO,SMT	C9
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	PC510,PC512,PC516
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC555
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C163,C164
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC13
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC502
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C159,C166,C171,C172,C176,C184
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C501,C510
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SM	C6
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC2
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC518
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C3
272001225401	CAP;2.2U ,CR,10V ,10%,0805,X5R,S	C5
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C139,C153,C178,C207,C585,C598
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C504,C509
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C666,C667,C690,C88
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C573,PC26
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C47,PC29,PC33,PC558

Part Number	Description	Location(S)
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC515,PC519,PC521,PC522,PC52
272431227527	CAP;220U,4V,+/-20%,H2.8,PT,NCC	PC539,PC541,PC543,PC544,PC54
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C662,C663,C740,C744
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	PC561,PC562
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C764
272075301302	CAP;300P,CR,50V,5%,0603,NPO,SMT	C10
272075330302	CAP;33P ,50V,5% ,0603,NPO,SMT	C610,C622
272011475501	CAP;4.7U ,10V,20%,1206,X5R,SMT	C12
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C174,C209,C558,C777
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C157,C188,C190,C191,C192
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	PC3
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	PC11
272431476502	CAP;47U ,6.3V,20%,SP-CAP,7343,S	C1
272030050301	CAP;5P,3KV,5%,1808,NPO,SMT,only	C13
221675350005	CARD BOARD;FRAME,PALLET,8080	
221675350004	CARD BOARD;TOP/BTM,PALLET,8080	
221600020252	CARTON;BATTERY,CAIMAN,PWR	
221675320002	CARTON;NON-BRAND,8080	
431678500001	CASE KIT;256M,8081	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
342665500010	CFM-SUYIN,S-STANDOFF,#4-40H4.8,N	
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L24,L25,L524,L525
273000500092	CHOKE COIL;2.2UH ,20%,16A,3.5MM	PL507
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5	L517
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L502,L505,L510,L513

9. Spare Parts List - 3

Part Number	Description	Location(S)
523467850017	COMBO ASSY;KME,UJDA750,8081	
291000000706	CON;BATTERY,7P,MA,2.5MM,R/A,C103	PJ2
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J501
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J5
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J508
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	J6
291000012411	CON;HDR,12P*1,1.25,ACES,SMT	CN1
331040050018	CON;HDR,BTB R/A,0.8MM,S-TECH1507	J504
291000017012	CON;HDR,FM,35P*2,1.27,H2.2,CEN,S	J4
291000012023	CON;HDR,MA,10P*2,1MM,H4.25,ST,SM	J3
291000021206	CON;HDR,MA,12P,1MM,ACES1212,SMT	J2
291000024421	CON;HDR,MA,22P*2,R/A,SUYIN,20038	J8
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J509
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J1,J505
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J3
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	CN2
291000277002	CON;HDR,MA,35P*2,1.27*1.27MM,CEN	J4
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S	J502
291000256827	CON;IC CARD,68P,0.635MM,62596-00	J7
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J511
291000000802	CON;MINI PCI SOCKET,0.8MM,H4.0,S	J507
291000811008	CON;PHONE JACK,2 IN 1,7.0MM,ALLT	J506
291000910601	CON;POWER JACK,6P,D=2.5,H=7,W=9.	PJ1
291000920605	CON;STEREO JACK,6P,W9.5,33184000	J10,J9
331000008033	CON;USB,FM,H15.64,R/A,4P*2,2522A	J1,J2

Part Number	Description	Location(S)
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C1034	CON1
441674800032	CONTACT PLATE ASSY;W4L27T0.15,S-	
441677310031	CONTACT PLATE ASSY;W4L27T0.15FUS	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200004	CONTACT PLATE;W4L63T0.15,1/4,T T	
340678500008	COVER ASSY,CPU,8081	
340678500006	COVER ASSY;HDD,8081	
340678500005	COVER ASSY;LCD,8081	
340678500007	COVER ASSY;MINI-PCI,8081	
340678500003	COVER ASSY;SPEAKER,8081	
340678500001	COVER ASSY;TOP,8081	
344678500021	COVER;BATTERY,8081	
344678500014	COVER;HINGE;L,8081	
344678500015	COVER;HINGE;R,8081	
344678500010	COVER;MDC,8081	
344678500012	COVER;REAR,L,8081	
344678500013	COVER;REAR,R,8081	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2,CP3
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP4
340676400025	CU FOIL ASSY;SOUTH BRIDGE,APOLLO	
323700000006	DDR SDRAM MODULE;256MB,16M*16*8,	
331660020003	DIMM SOCKET;DDR SODIMM 200P,AMP1	J503
288111544001	DIODE; 1SR-154-400 400V 1.0A	D1
288114148004	DIODE;1N4148WS,75V,200mW,SOD-323	D3

9. Spare Parts List - 4

Part Number	Description	Location(S)
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D2
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D505
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D4,D518,D6
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D15,D508
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	PD1,PD5
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100099001	DIODE;BAV99,70V,450MA,SOT-23	PD2,PD3
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D5,D501,D506,D509,PD4,PD506,
288105230004	DIODE;BZM55B3V6,ZENER,3.6V,5mA,M	D2
288105515001	DIODE;BZV55-C15,ZENER,5%,SOD-80,	PD7
288105520001	DIODE;BZV55-C20,ZENER,5%,SOD-80,	PD6
288105524003	DIODE;BZV55-C24,ZENER,5%,SOD-80,	PD501
288105524002	DIODE;BZV55-C2V4,ZENER,5%,SOD-80	PD2,PD3
288105533001	DIODE;BZV55-C3V3,ZENER,5%,SOD-80	PD6
288105543001	DIODE;BZV55-C4V3,ZENER,5%,SOD-80	PD5
288105556001	DIODE;BZV55-C5V6,ZENER,5%,SOD-80	PD1
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D502,PD501,PD504,PD55
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD502,PD503
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD502,PD503
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323	SD1
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D3
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	PD504
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D2,D503
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD1,ZD2

Part Number	Description	Location(S)
523408619050	DVD COMBO DRIVE;UJDA750KME-A,PUM	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C769,C771,C774
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC502,PC526,PC533
312272205051	EC;22U,20V,M,RA,D6.3,-55+105,OS-	PC9
227678500001	END CAP;LEFT,8081	
227678500002	END CAP;RIGHT,8081	
481678500002	F/W ASSY;KBD CTRL,8081	U520
481678500001	F/W ASSY;SYS/VGA BIOS,8081	U511
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA1
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L11,L15,L20,L22,L501,L504,L51
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L507,L508,L515,L516,PL1,PL2,P
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L10,L12,L13,L16,L17,L18,L19,L2
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L1
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L1,L2,L537,L539,L540,L542,L54
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L1,L2
422676400001	FFC;TOUCH PAD,APOLLON	
335152000085	FUSE; 128 DC-7A/50V 139℃only UC	F1
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F502
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F2
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,F501
295000010105	FUSE;1A,NORMAL,1206,SMT	F3,PF1,PF5
295000010105	FUSE;1A,NORMAL,1206,SMT	PF501
295000010153	FUSE;FAST,1A,32V,0603,SMT,THIN F	F5,F7
295000010103	FUSE;FAST,2A,32V,1206,SMT,CERAMI	PF6,PF7,PF8
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433	F1

9. Spare Parts List - 5

Part Number	Description	Location(S)
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	F503,PF4
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	PF502
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
295000010130	FUSE;NORMAL,4A/32VDC,3216,SMT	PF3
295000010009	FUSE;NORMAL,5A/32VDC,3216,SMT	PF2
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,PF2
345678500011	GASKET;1394,7*7*0.8,8081	
345676400013	GASKET;AUDIO,MB,APOLLON	
345678800004	GASKET;MODEM,20*5*3.5,8381	
345676400027	GASKET;PCMCIA-1,APOLLON	
345676400006	GASKET;PCMCIA-2,APOLLON	
345676400011	GASKET;PCMCIA-3,APOLLON	
345678500010	GASKET;USB,10*10*1.5,8081	
361200005001	GLUE;TOSHIBA 3941	
523467850002	HDD ASSY;30G,IC25N030ATMR04-0,HI	
523405320071	HDD DRIVE,30GB,2.5",IC25N030ATMR	
451678500001	HDD ME KIT;8081	
340678500018	HEATSINK ASSY;8081	
340676400015	HINGE,L,LCD,APOLLON	
340676400016	HINGE;R,LCD,APOLLON	
340676400018	HOLDER;PCMCIA FCI,APOLLON	
340678500002	HOUSING ASSY;CASE,8081	
340678500004	HOUSING ASSY;LCD,8081	
451678500091	HOUSING KIT,8081	

Part Number	Description	Location(S)
344678500022	HOUSING;BATTERY,8081	
291000616803	IC SOCKET;BANIAS m-FCBGA478P, MO	U504
324180786389	IC,CPU,BANIAS,1.6GHZ,MICRO-FCPGA	
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U11
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U20
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U7
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT2	U522
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U515,U526,U527,U528
284501021003	IC;ADM1021A,TEMPERATURE MTR,SSOP	U505
286300809014	IC;ADM809M, RESET CIRCUIT,4.38V,	U518
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	U13
284508807001	IC;AME8807AEHA,600mA,CMOS LDO,AM	PU5
286301117021	IC;AMS1117,VOL REGULATOR,1A,SOT-	U5,U6
286300317010	IC;AMS3107C, VOLTAGE REGULATOR,	U8
286302020001	IC;APA2020ARI,AUDIO AMP,2W,TSSOP	U15
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC4
284509738002	IC;CMI9738-S,AC97 CODEC,LQFP,48P	U523
283767180001	IC;DDR SDRAM,16M*16-133,TSOP,66P	U1,U2,U3,U4,U507,U508,U509,U
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U519
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC2
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U16
283450083002	IC;FLASH,512K*8-70,PLCC32,ST39SF	
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U9
286200571002	IC;G571,POWER INTERFACE SW,SSOP1	U516
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	

9. Spare Parts List - 6

Part Number	Description	Location(S)
284595081001	IC;ICS950810, CK408 CLOCK GEN, T	U512
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU503
284502996001	IC;LP2996,DDR,NS,PSOP8,SMT	PU19
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU11,PU501
286301907001	IC;MAX1907A,PWM CONTROLLER,40-QF	PU4
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU501
286300809012	IC;MAX809S,RESET CIRCUIT,2.9V,ON	U514
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC1
284500000050	IC;MONTARA-GM GMCH,MICRO-FCBGA,7	U502
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
284587393001	IC;PC87393,LPC SUPER I/O,TQFP,10	U10
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U501,U502
286387506001	IC;S-875061EUP VOLT DETECTOR S	IC3
286300338001	IC;SC338,FET CTRL,SC,MSOP-10	PU13
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ503
282074164002	IC;SN74LV164APWR,SIPO REGISTER,T	U21
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU502
284506105001	IC;VT6105LOM, PCI LAN CONTROLLER	U517
273000990089	INDUCTOR;10U,D104C,TOKO,10X10,H=	PL508
273000990050	INDUCTOR;10UH ,DS126C2,TOKO,SMT	PL506
273000990160	INDUCTOR;3.9UH,30%,DS104C2,SMT	PL505
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL502
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL503
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346678000001	INSULATOR;AL-FOIL,M/B-2,PUMA	

Part Number	Description	Location(S)
346678500002	INSULATOR;AL-FOIL,PCMCIA,8081	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346678000003	INSULATOR;D/D-BD,PUMA	
346677300005	INSULATOR;FIBER,93.5X15.5,T=0.25	
346677300006	INSULATOR;FIBER,UL94V-0,195x15,T	
346677300004	INSULATOR;FIBER,UL94V-0,35x15,T=	
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm	
346678500009	INSULATOR;INVERTER,8081	
346676400001	INSULATOR;M/B-1,APOLLON	
346676400003	INSULATOR;MINI-PCI,APOLLON	
346678500008	INSULATOR;SPK,8081	
531067850001	KBD OPTION;US,8081	
531017240176	KBD;86,US,3000160400,ZIPPY,8081	
451678500051	LABEL KIT;N-B,8081	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242678500001	LABEL;AGENCY-GLOBAL,8081	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242678500003	LABEL;BATT,11.1V/4.0AH,LI,SAN,80	

9. Spare Parts List - 7

Part Number	Description	Location(S)
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242669600005	LABEL;LOT NUMBER,RACE	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441678500031	LCD ASSY;14",XGA,QDI,141X1LH12,8	
451678500072	LCD ME KIT;TFT,QDI,XGA,14",8081	
413000020349	LCD;QD141X1LH12,TFT,XGA,14.1",QD	
294011200034	LED;GREEN,H.8,0603,19-21VGC/TR,S	LED3,LED4,LED5,LED6
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D17,D18,D19,D20,D510,D511,D5
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED1,LED2
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	D10
416267850001	LT PF;14",QDI,141X1LH12,256M,808	
526267850005	LTXNX;8081/4QDE/30J/1US1/L1D3A/X	
561567850001	MANUAL KIT;EN,8081,N-B	
561567850101	MANUAL;USER'S,EN,8081,N-B	
461677400001	PACKING KIT;DA-1A05-A;PWR	
461678500002	PACKING KIT;N-B,8081	
227678800003	PAD;LCD/KB,ANIT-STATIC,8381	
224670830002	PALLET;1250*1080*130,7521N	
221600050218	PARTITION;BATTERY,MARLIN,CAIMAN,	
221675350003	PARTITION;PALLET,8080	
221600050219	PARTITION;TOP/BTM,BATTERY,MARLIN	
412674500004	PCB ASSY;FAX MODEM 56K,MDC56S-I,	
412673400008	PCB ASSY;MINI-PCI,TYPE IIIB,INTE	

Part Number	Description	Location(S)
316677300001	PCB;PWA-APOLLON/BATT,BD,PWR	
316677400001	PCB;PWA-INVERTER BD (DA-1A05-A),	R0D
316678000002	PCB;PWA-PUMA/CHARGER BD	R02
316678000001	PCB;PWA-PUMA/MOTHER BD	R01
222678500001	PE BABBLE BAG;300mm*260mm,8081	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222668820003	PE BUBBLE BAG;160X270MM,ANTI-STA	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
222671620001	PE BUBBLE BAG;CD-ROM HOUSING,817	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100	L14,L23,L505,L515,L521,L523,L
345678500001	PLATE;T/P,COVER,8081	
341678500001	PLATE;T/P,GROUND,8081	
411678500006	PWA;PWA-8081,256M,MOTHER BD	
411678500008	PWA;PWA-8081,256M,MOTHER BD,SMT	
411678500007	PWA;PWA-8081,256M,MOTHER BD,T/U	
411677400001	PWA;PWA-INVERTER BD,DA-1A05-A,PW	
411677400002	PWA;PWA-INVERTER BD,SMT,DA-1A05-	
411678000005	PWA;PWA-PUMA,CHARGER BD,SMT	
411678000004	PWA;PWA-PUMA,CHARGER BD,T/U	
411677370001	PWA-PWA-8X81/BATT BD;LI,4.0Ah,2P	
411677370002	PWA-PWA-8X81/BATT BD;SMT,BL3240G	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR512

9. Spare Parts List - 8

Part Number	Description	Location(S)
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR532
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR510,PR522,PR531
271586026101	RES;.02 ,2W,1%,2512,SMT	PR1,PR513
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L545,R48,R662,R695,R727,R769
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R7
271071000002	RES;0 ,1/16W,5% ,0603,SMT	F4,F6,L527,L533,PR16,PR17,PR2
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR10,PR13,PR509,R1,R2,R3,R4,R
271044100101	RES;0.010,1.5W, 1%,2512,SMT;PWR	RM
271045507103	RES;0.050,1W, 1%,2512,SMT, only	RS1,RS2,RS3
271071127111	RES;1.27K,1/16W,1% ,0603,SMT	R88
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R521
271071196111	RES;1.96K,1/16W,1% ,0603,SMT	PR5
271002100301	RES;10 ,1/10W,5% ,0805,SMT	PR1,PR25,PR28,PR533,PR534
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR20,R126
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR501
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R5,R6
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R39,R51,R545,R547,R548
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R702
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R28,R29,R32,R33,R7,R8,R9
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R13,R15
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR14,PR506,PR518
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R23,R24,R25,R26,R30,R34
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR23,PR39,PR523,PR529,R112,R
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR18,PR19,PR2,PR512,PR515

Part Number	Description	Location(S)
271071103101	RES;10K ,1/16W,1% ,0603,SMT	R1,R10,R18
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR11,PR30,PR31,R754
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR502
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR525,PR536,PR9,R107,R120,R1
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R20,R21,R3
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R136,R138
271071121301	RES;120 ,1/16W,5% ,0603,SMT	R505,R686,R736
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR20,PR507
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R92
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR508
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R18
271071143212	RES;14.3K,1/16W,1%,0603,SMT	PR32
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R515,R541,R554,R556,R95,R96
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R571
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R2
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR26
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR519
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R187,R200
271071169211	RES;16.9K,1/16W,1% ,0603,SMT	R3
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR15
271071182213	RES;18.2,1/16W,1%,0603,SMT	R97
271071184101	RES;180K ,1/16W,1% ,0603,SMT	R6
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R180,R6
271071183301	RES;18K ,1/16W,5% ,0603,SMT	R186,R192
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R14

9. Spare Parts List - 9

Part Number	Description	Location(S)
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR3,PR521,R109,R532,R536
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R121,R16,R163,R183,R4,R5,R59,F
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR42,PR524,PR530,PR540,R7,R7
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR12,PR4
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R2,R4
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	R700
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R11,R12,R157,R173,R693,R699
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR511
271071274111	RES;2.74K,1/16W,1% ,0603,SMT	PR7
271071201101	RES;200 ,1/16W,1% ,0603,SMT	R108
271071201301	RES;200 ,1/16W,5% ,0603,SMT	PR13,PR22,R637
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR16
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R29
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR21,PR33,PR34
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR8
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R722
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R139,R142,R158,R601,R675,R709
271071220302	RES;22 ,1/16W,5% ,0603,SMT,INT	R9
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R23,R26,R28
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R748
271071237211	RES;23.7K,1/16W,1% ,0603,SMT	PR37
271071243011	RES;243 ,1/16W,1% ,0603,SMT	R546
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR510
271071274811	RES;27.4 ,1/16W,1% ,0603,SMT	R50,R523,R533,R542,R552,R570

Part Number	Description	Location(S)
271071283101	RES;28K ,1/16W,1% ,0603,SMT	PR6
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R22,R24
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R41
271071202301	RES;2K ,1/16W,5% ,0603,SMT	PC527,PC559,R755
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	PR516
271071301301	RES;300 ,1/16W,5% ,0603,SMT	R105
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R516,R538
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR18
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR15
271071303101	RES;30K ,1/16W,1% ,0603,SMT	R5
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR14
271071324012	RES;324K ,1/16W,1% ,0603,SMT	PR7
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R37,R510,R592,R606,R607,R608,I
271002331301	RES;330 ,1/10W,5% ,0805,SMT	FR1,FR2
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R21,R25,R27
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R194,R196,R197,R198,R746,R818
271071332311	RES;332K ,1/16W,1% ,0603,SMT	PR27,PR538
271071332311	RES;332K ,1/16W,1% ,0603,SMT	PR21
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR504,PR514,R501,R504
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R560
271071305301	RES;3M ,1/16W,5% ,0603,SMT	R12,R20
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR5,PR6
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R114,R115,R127,R161,R177,R182
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR520,PR521
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR12

9. Spare Parts List - 10

Part Number	Description	Location(S)
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR9
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R527
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR537
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR29,PR4,R179
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R8
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R507,R511
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR3
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R589
271071473101	RES;47K ,1/16W,1% ,0603,SMT	R19
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R135,R167,R174
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR11,R502,R503
271071487811	RES;48.7 ,1/16W,1% ,0603,SMT	R102
271071487011	RES;487 ,1/16W,1% ,0603,SMT,MUS	R91
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R35,R49,R544,R549,R597,R598,R
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR19,PR36
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R22
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	R760
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R72
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R54,R561,R573,R67,R68
271071511101	RES;510 ,1/16W,1% ,0603,SMT	PR513
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R52,R534,R535,R553
271071560101	RES;56 ,1/16W,1% ,0603,SMT	R749,R750,R751,R752
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R101,R577,R61,R638,R639,R93,R
271071594101	RES;590K ,1/16W,1% ,0603,SMT	PR505
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R646

Part Number	Description	Location(S)
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR517
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	PR10
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R770,R773,R777,R778,R780,R781
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R550,R551
271071604112	RES;604,1/16W,1% ,0603,SMT	R555,R557
271071649211	RES;64.9K,1/16W,1% ,0603,SMT	PR35
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R558
271071683101	RES;68K ,1/16W,1% ,0603,SMT	R4
271071732011	RES;732 ,1/16W,1% ,0603,SMT	R16
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R1,R2,R3,R618,R619,R65,R66,R81
271071751101	RES;750 ,1/16W,1% ,0603,SMT	R89
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R100,R128,R131,R140,R144,R146
271071825211	RES;82.5K,1/16W,1% ,0603,SMT	R11
271071953011	RES;953 ,1/16W,1% ,0603,SMT	R38
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR22
451678500031	ROM ME KIT;8081	
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP10,RP11,RP12,RP13,RP14,RP2
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP22,RP23,RP26,RP29,RP502,RP
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP24,RP28
271611560301	RP;56*4 ,8P ,1/16W,5% ,0612,SMT	RP18,RP19,RP20,RP511
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP21,RP505,RP506,RP507,RP508
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP25,RP30,RP31,RP32
345678500002	RUBBER;DOWN,LCD,8081	
345678500002	RUBBER;DOWN,LCD,8081	

9. Spare Parts List - 11

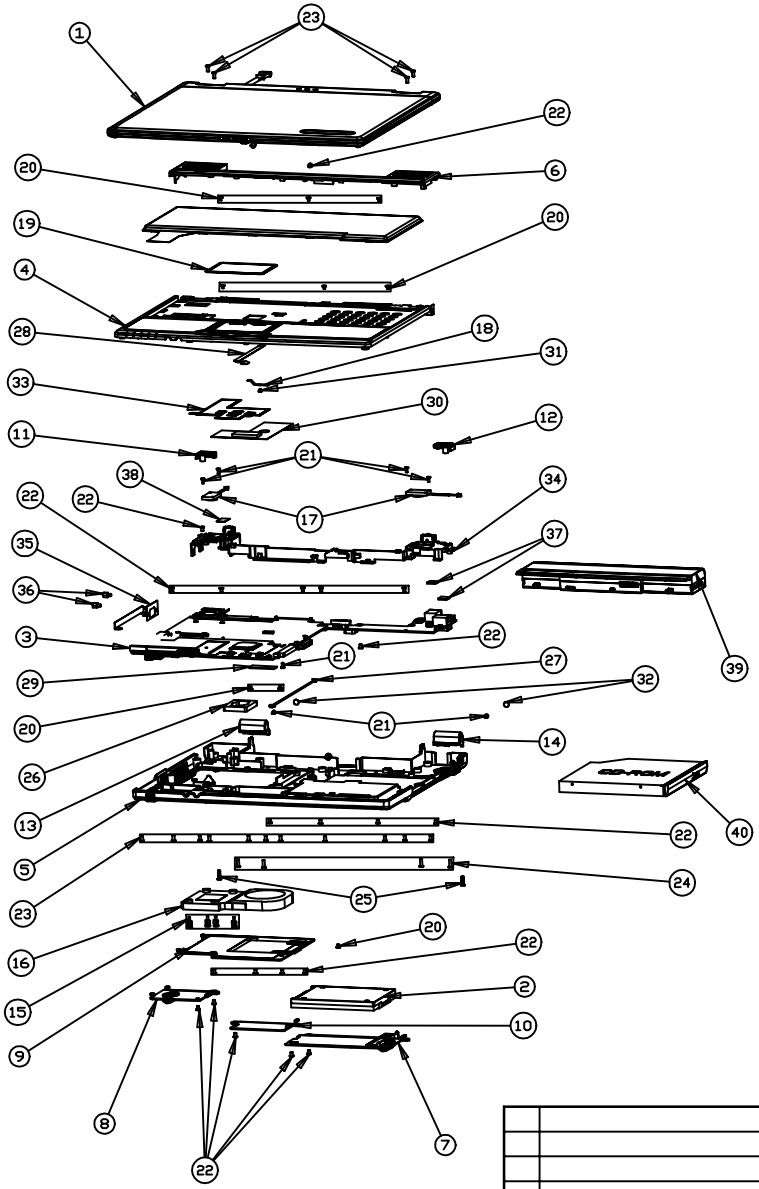
Part Number	Description	Location(S)
345677300002	RUBBER;SILICONE RUBBER,24X15.5,t	
345677300001	RUBBER;SILICONE RUBBER,T=1.5mm,D	
565167850001	S/W;CD ROM SYSTEM DRIVER,8081	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
340678500021	SHIELDING ASSY;HDD,8081	
333025000005	SHRINK TUBE;300V,125,I.D=2.5,T=0	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,t0.8,	
370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	
370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010301	SPC-SCREW;M2L3,NIB,K-HD,t0.8,NLK	
370103010303	SPC-SCREW;M3L3,NIB,K-HD(+)	

Part Number	Description	Location(S)
340676400009	SPEAKER ASSY,APOLLON	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
345676400025	SPONGE;COVER-SWITCH,MB,APOLLON	
345676400023	SPONGE;CPU-SOCKET,MB,APOLLON	
345676400008	SPONGE;D/D-B,APOLLON	
345676400016	SPONGE;RTC,APOLLON	
345676400016	SPONGE;RTC,APOLLON	
341678000001	SPRING-SCREW;HEATSINK,PUMA	
342674500002	STAND OFF;AM20-30,GP3	MTG501,MTG502
342676400015	STAND OFF;AM20-45,APOLLON	
342676400015	STAND OFF;AM20-45,APOLLON	MTG503
341678000002	STANDOFF;HEATSINK,PUMA	MTG12,MTG13,MTG14,MTG15
297040100007	SW;PUSH BUTTON,STS-043-A,5P,12V/	SW1,SW2,SW3,SW4,SW5
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	SW6
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
345676400032	THERMAL PAD;NORTH BRIDGE,APOLLON	
310111103013	THERMISTOR;10K,1%,RA,DISK,103AT-	
361400003038	THERMOSETTING BOND;80837,LOCTITE	
442164900021	TOUCHPAD MODULE;TM41PUC2311-2,DI	
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ2,PQ3,PQ4,PQ5,PQ501,P
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ502,PQ505,PQ506
288200301004	TRANS;3LN01S,N-MOSFET,SMCP	Q2,Q3
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU17,PU9
288200144008	TRANS;DTA144EKA,PNP,SMT	Q1

9. Spare Parts List - 12

Part Number	Description	Location(S)
288200144002	TRANS;DTA144WK,PNP,SMT	PQ504
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q12,Q14,Q16,Q17,Q18,Q21,Q22,(
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	Q13,Q15,Q26,Q503,Q506,Q508
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ501
288206676005	TRANS;FDS6676S,14.5A,30V,9mOHM,S	PU18,PU6,PU7,PU8
288206690003	TRANS;FDS6690S,N-MOS,.022OHM,SO8	PU10
288206694002	TRANS;FDS6694,N-MOSFET,SO8,SMT	PU1,PU2,PU3
288209412001	TRANS;FDS9412,N-MOS,.036OHM,SO8	PU12,PU14,PU15,PU16
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ507
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q504
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q1
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q10,Q11,Q25,Q502,Q507
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	U2
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	U14,U503,U533
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	Q1
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ2,PQ3,PQ4,PQ508
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU504
288208107001	TRANS;TPC8107,13A/30V,P-MOSFET,S	Q2,Q5
373101713502	T-SCREW;B.M1.7L3.5,HD04t0.25,0,B	
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	R73
422677300005	WIRE ;#20AWG,UL1007,L=140mm,RED;	CN1
422677300002	WIRE ;#20AWG,UL1007,L=230mm,BLAC	CN4
422677300004	WIRE ;#26AWG,UL1007,L=215mm,BLUE	CN3
422677300006	WIRE ;#26AWG,UL1007,L=290mm,YELL	CN2
421676400001	WIRE ASSY,MDC-MODEM,APOLLON	

Part Number	Description	Location(S)
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MO	
421676400003	WIRE ASSY;LCD 14,QDI,APOLLON	
273001050109	XFMR;CI8.5,16T/2600T(.21ψ),220m	T1
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U513
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X501
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X503
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X506
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X502
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X1
		P/N:526267850005



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
40					
39	441677370001	BATTERY ASSY;8081(Panasonic)	1	ASSY	
38	346678500008	INSULATOR;SPK,8081	1	PART	
37	345678500010	GASKET;USB,10*10*1.5,8081	2	PART	
36	342665500010	CFM-SUYIN,S-STANDOFF,#4-40H4.8,NIW,NLK	2	PART	
35	342678500004	BRACKET;VGA,8081	1	PART	
34	342678500003	BRACKET;I/O,8081	1	PART	
33	346678500007	AL-FOIL;T/P,8081	1	PART	
32	345678500002	RUBBER;DOWN,LCD,8081	2	PART	
31	370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	1	PART	TP-GN*1
30	340676400025	CU FOIL ASSY;SOUTH BRIDGE,APOLLON	1	ASSY	
29	345676400032	THERMAL PAD;NORTH BRIDGE,APOLLON	1	PART	
28	422676400001	FFC;TOUCH PAD,APOLLON	1	ASSY	
27	421676400001	WIRE ASSY,MDC-MODEM,APOLLON	1	ASSY	
26	345676400016	SPONGE;RTC,APOLLON	1	PART	
25	370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	2	PART	HOUSING-REARCOVER*2
24	370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	4	PART	HOUSING-SPKCOVER*4
23	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	15	PART	HOUSING-COVER*11 HINGE-ID*4
22	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	21	PART	MB-HOUSING*6 SPKCOVER-HOUSING*1 ALL-COVER*9 CD-ROM*2 HOUSING-ID*2 ID-MB*
21	370102010502	SPC-SCREW;M2L5,NIB,K-HD,t0.8,NLK	7	PART	SPEAKER*4 MB-DD*1 HINGE-COVER*2
20	370102010301	SPC-SCREW;M2L3,NIB,K-HD,t0.8,NLK	9	PART	TOP-HOUSING*4 KEYBOARD*3 MDC-MB*2
19	345678500001	PLATE;T/P,COVER,8081	1	PART	
18	341678500001	PLATE;T/P,GROUND,8081	1	PART	
17	340676400009	SPEAKER ASSY;APOLLON	2	ASSY	
16	340678500019	HEATSINK ASSY;MPT,8081	1	ASSY	
15	341678000001	SPRING-SCREW;HEATSINK,PUMA	4	PART	
14	344678500015	COVER;HINGE;R,8081	1	PART	
13	344678500014	COVER;HINGE;L,8081	1	PART	
12	344678500013	COVER;REAR,R,8081	1	PART	
11	344678500012	COVER;REAR,L,8081	1	PART	
10	344678500010	COVER;MDC,8081	1	PART	
9	340678500008	COVER ASSY,CPU,8081	1	ASSY	
8	340678500007	COVER ASSY;MINI-PCI,8081	1	ASSY	
7	340678500006	COVER ASSY;HDD,8081	1	ASSY	
6	340678500003	COVER ASSY;SPEAKER,8081	1	ASSY	
5	340678500002	HOUSING ASSY;CASE,8081	1	ASSY	
4	340678500001	COVER ASSY;TOP,8081	1	ASSY	
3	411678500006	PWA;PWA-8081,MOTHER BD	1	ASSY	
2	451678500001	HDD ME KIT;8081	1	ASSY	
1			1	ASSY	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± RANGE	Pla.	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	05-Jul-03	MATERIAL	SEE NOTES	TREATMENT	REMARK
UNIT	MM	SCALE	0.250	DRAWING NAME	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD R00A

MiTAC Technology Corp.

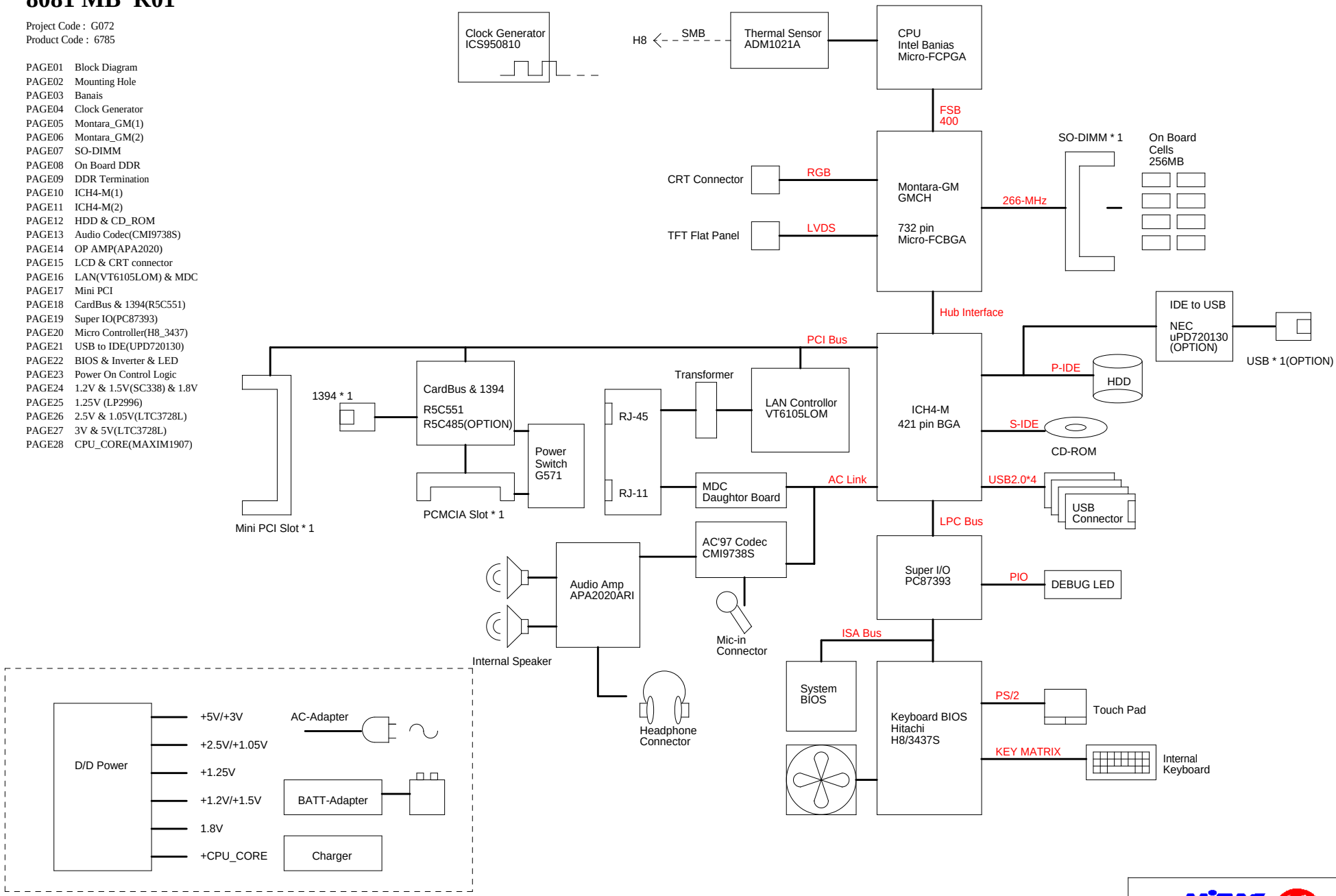
model name8081-ASSY-MAIN-ROBERT

file nameMAIN_ASSY_8081

8081 MB R01

Project Code : G072
Product Code : 6785

PAGE01 Block Diagram
PAGE02 Mounting Hole
PAGE03 Banais
PAGE04 Clock Generator
PAGE05 Montara_GM(1)
PAGE06 Montara_GM(2)
PAGE07 SO-DIMM
PAGE08 On Board DDR
PAGE09 DDR Termination
PAGE10 ICH4-M(1)
PAGE11 ICH4-M(2)
PAGE12 HDD & CD_ROM
PAGE13 Audio Codec(CMI9738S)
PAGE14 OP AMP(APA2020)
PAGE15 LCD & CRT connector
PAGE16 LAN(VT6105LOM) & MDC
PAGE17 Mini PCI
PAGE18 CardBus & 1394(R5C551)
PAGE19 Super IO(PC87393)
PAGE20 Micro Controller(H8_3437)
PAGE21 USB to IDE(UPD720130)
PAGE22 BIOS & Inverter & LED
PAGE23 Power On Control Logic
PAGE24 1.2V & 1.5V(SC338) & 1.8V
PAGE25 1.25V (LP2996)
PAGE26 2.5V & 1.05V(LTC3728L)
PAGE27 3V & 5V(LTC3728L)
PAGE28 CPU_CORE(MAXIM1907)



MiTAC

Title: **Block Diagram**

Size: C | Document Number: 411678500006 | Rev: 01

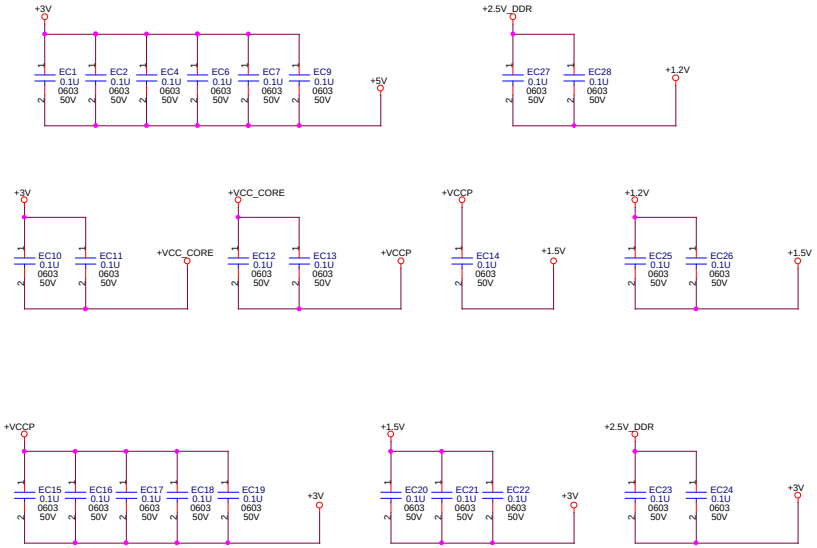
Date: Wednesday, June 11, 2003 | Sheet 1 of 28

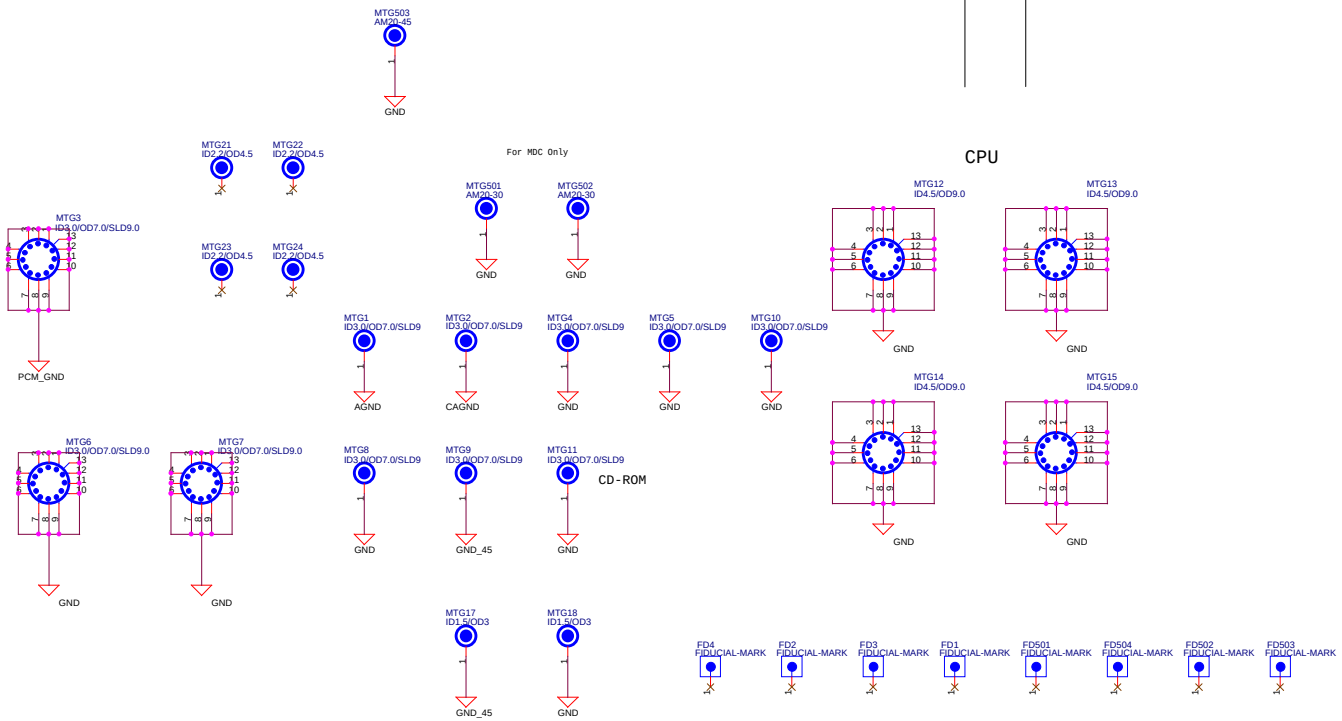
REV	Change detail	DATE	ECR No.
R00	Initail release (base on PUMA)	2003/05/02	
R01	1.Change PR4 ,PR29 and PR45 to 470 ohm for SUSB# signal quality. 2.LAN signal add fuse to protect LAN transformer. 3.Modify U533 control signal(SUSC# and 2 * 2N7002) for leakage current. 4.Remove R98 for leakage current and change pull high to +3V. 5.Change R202 and R217(M/B ID) pull high to +VDD3. 6.Change Q24 pin2 pull high to +EXT3V. 7.Change R777 and R778 to 6.8K for CD ROM audio noise. 8.Inverter input voltage add VMAIN option for future use. 9.Change Q517 to 2N7002 and rename Q33 for LED flash issue. 10.Change U522 power to +AVDDAD, C753 to AGND, R736 to AGND. 11.Change J10(MIC) pin6 to CAGND. 12.Reserve band pass tuning capacitor.(Page 13) 13.Add a resistor on CD LED# signal to prevent signal O.D. 14.Delete M/B to charger BD connector USB signal reserver resistors and connector origanl pin to GND. 15.Add a resistor(1M) and change R505 to 47K ohm and rename R507 for divided DVMAIN to tuen on LCDVCC MOS.(Reserved) 16.Reserve a regulator for audio +5V input. 17.Modify back light circuit. 18.Re-assign M/B to Charger BD pin. 19.Change R766 pull high to +VA. 20.Add R505 between CLK_DDR3/CLK_DDR3# and R686 between CLK_DDR4/CLK_DDR4#	2003/05/26	

VT6105LOM(LAN)
IDSEL: AD18
PCI REQ1#
PCI GNT1#
PCI INTE#

Mini PCI
IDSEL: AD17
PCI REQ3#
PCI GNT3#
PCI INTD# INTF#

R5C551
IDSEL: AD20
PCI REQ2#
PCI GNT2#
PCI INTB# INTG#





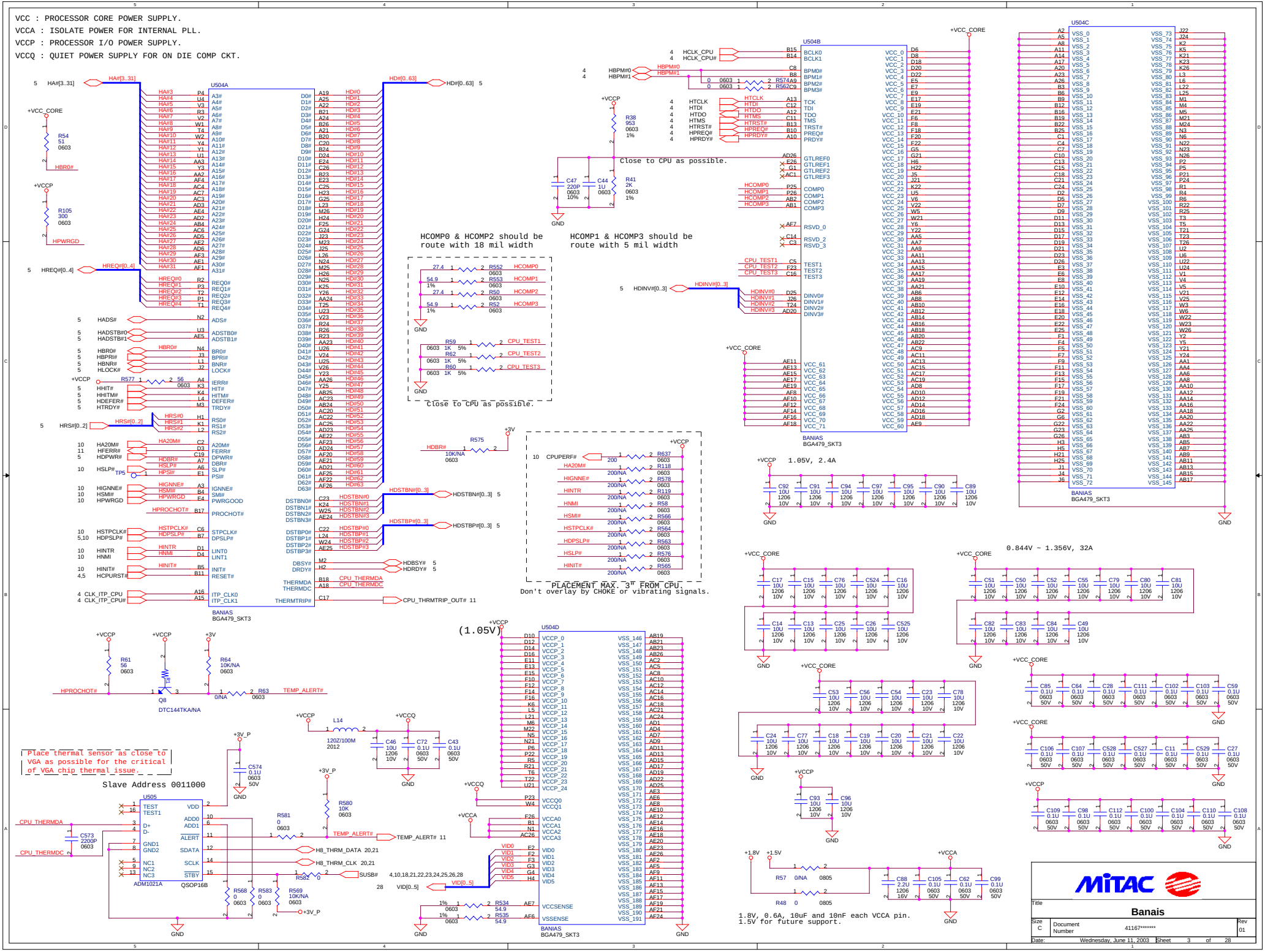
MiTAC

Title: **Mounting Hole**

Size	Document Number	Rev
C	41167*******	01

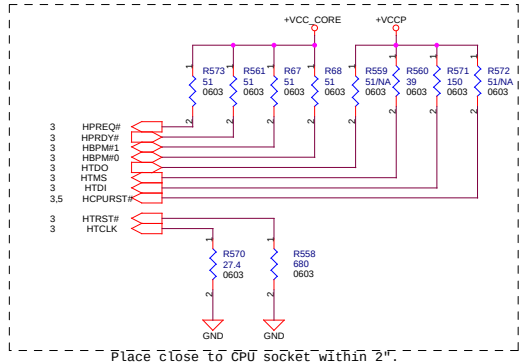
Date: Wednesday, June 11, 2003 Sheet 2 of 28

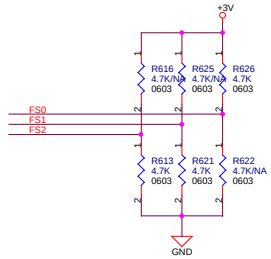
VCC : PROCESSOR CORE POWER SUPPLY.
VCCA : ISOLATE POWER FOR INTERNAL PLL.
VCCP : PROCESSOR I/O POWER SUPPLY.
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.



VID 5	4	3	2	1	0	VCC-Core
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

VID 5	4	3	2	1	0	VCC-Core
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700



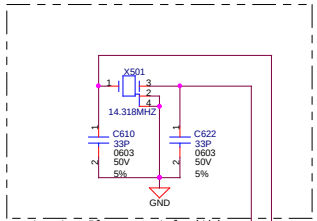


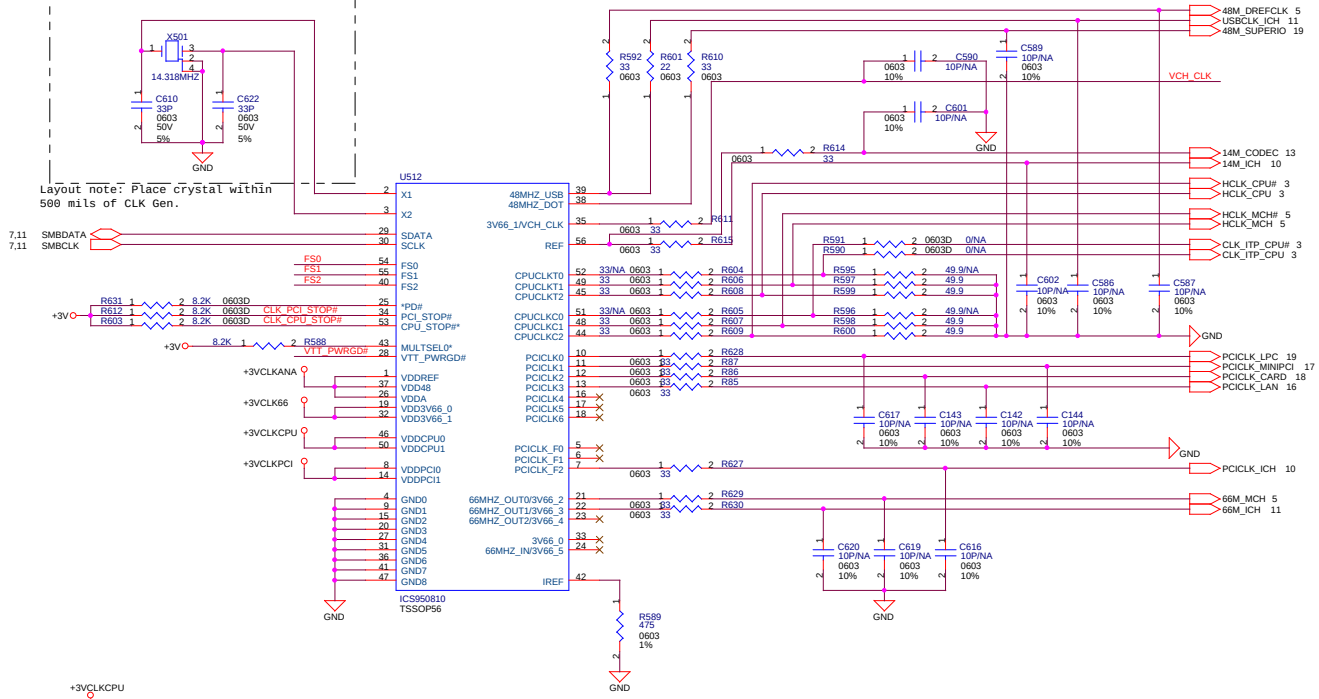
001

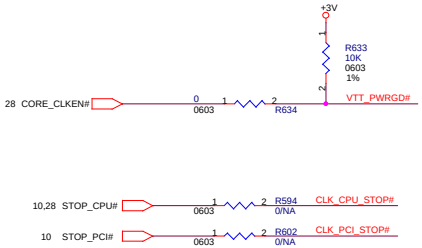
FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

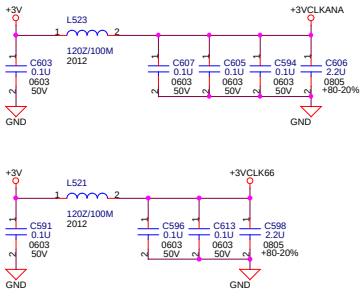
0:0V
1:3.3V

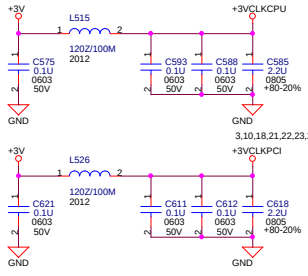
UNIT: MHz

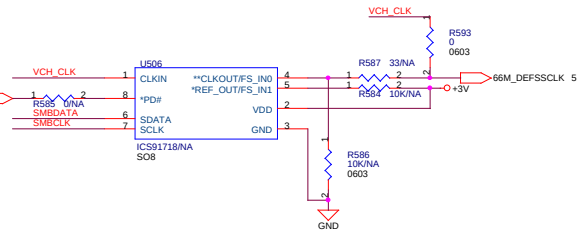










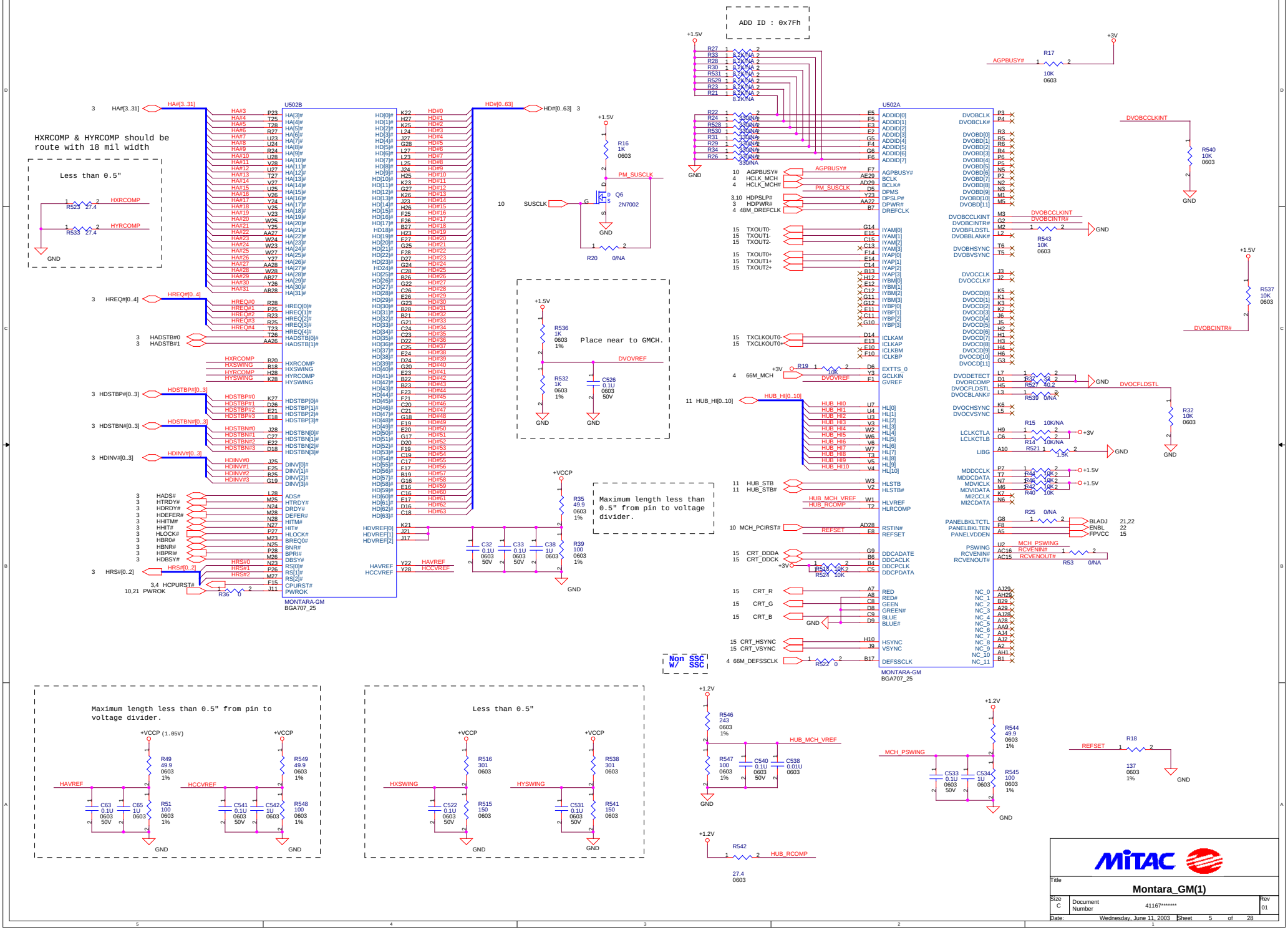


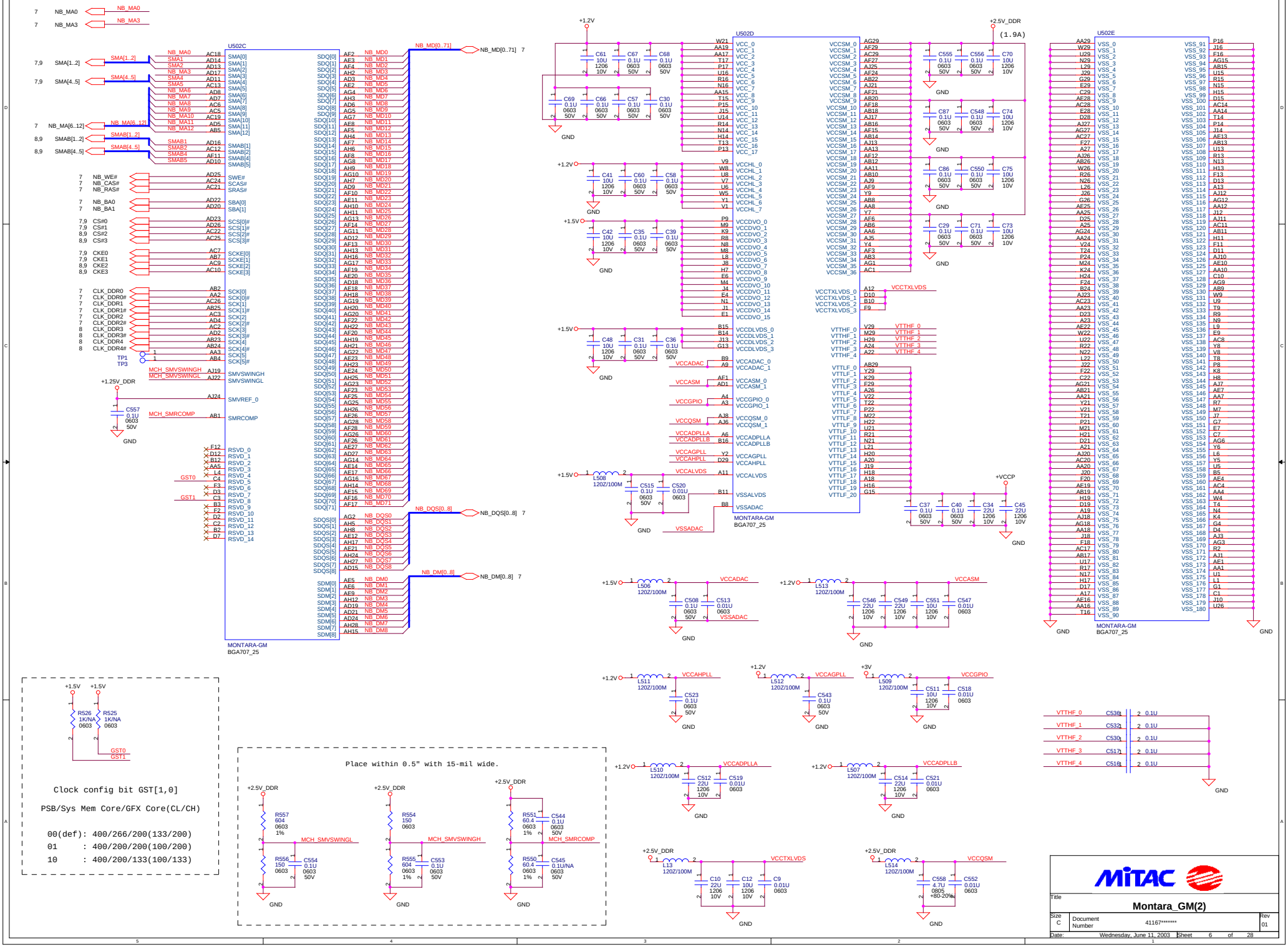
MiTAC

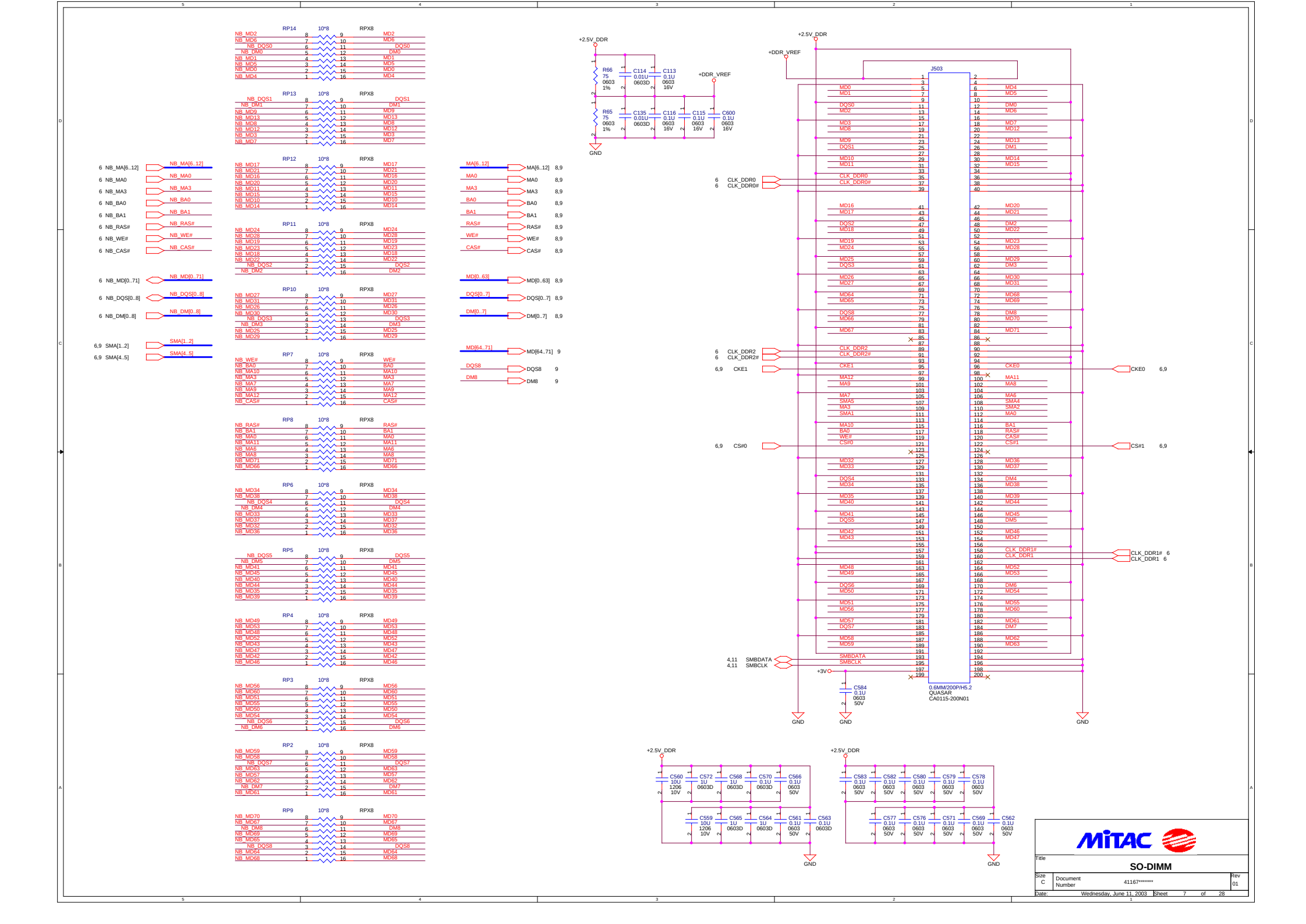
Title: Clock Generator

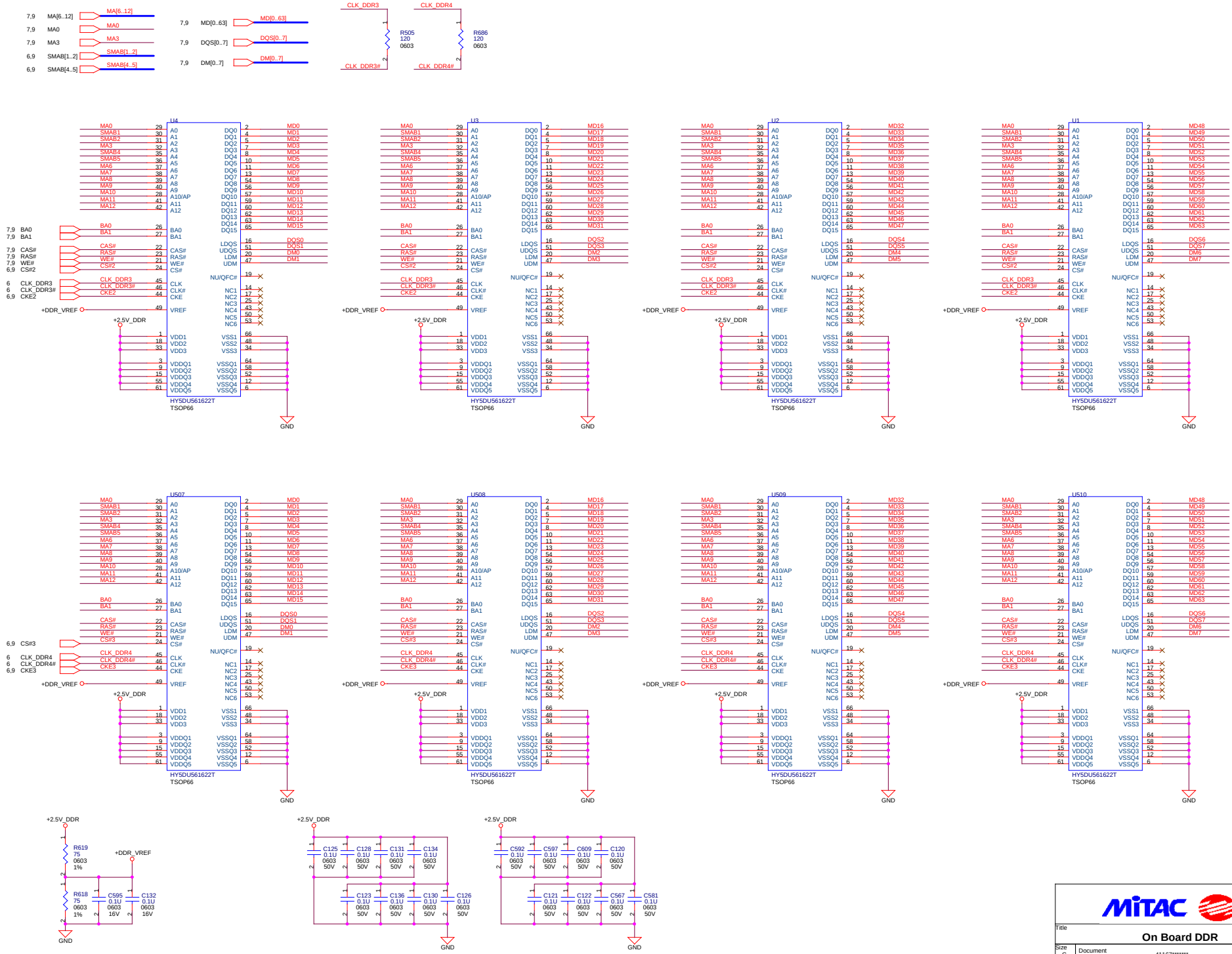
Size	Document Number	Rev
C	41167******	01

Date: Wednesday, June 11, 2003 Sheet 4 of 28


ADD ID : 0x7Fh
HXRCOMP & HYRCOMP should be route with 18 mil width
Less than 0.5"
Place near to GMCH.
Maximum length less than 0.5" from pin to voltage divider.
Maximum length less than 0.5" from pin to voltage divider.
Less than 0.5"
Non SSC
W/ SSC
U502B
MONTARA-GM
BGA707_25
U502A
MONTARA-GM
BGA707_25
Title
Montara_GM(1)
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 5 of 28


U502C
MONTARA-GM
BGA707_25
U502D
MONTARA-GM
BGA707_25
U502E
MONTARA-GM
BGA707_25
NB_MD[0..71]
NB_DQS[0..8]
NB_DM[0..8]
+1.2V
+1.5V
+2.5V_DDR
+1.25V_DDR
+VCCP
GND
Clock config bit GST[1,0]
PSB/Sys Mem Core/GFX Core(CL/CH)
00(def): 400/266/200(133/200)
01 : 400/200/200(100/200)
10 : 400/200/133(100/133)
Place within 0.5" with 15-mil wide.
Title
Montara_GM(2)
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 6 of 28


RP14 10*8 RPX8
NB_MD2 8 9 MD2
NB_MD6 7 10 MD6
NB_DQS0 6 11 DQS0
NB_DM0 5 12 DM0
NB_MD1 4 13 MD1
NB_MD5 3 14 MD5
NB_MD0 2 15 MD0
NB_MD4 1 16 MD4
RP13 10*8 RPX8
NB_DQS1 8 9 DQS1
NB_DM1 7 10 DM1
NB_MD9 6 11 MD9
NB_MD13 5 12 MD13
NB_MD8 4 13 MD8
NB_MD12 3 14 MD12
NB_MD3 2 15 MD3
NB_MD7 1 16 MD7
RP12 10*8 RPX8
NB_MD17 8 9 MD17
NB_MD21 7 10 MD21
NB_MD16 6 11 MD16
NB_MD20 5 12 MD20
NB_MD11 4 13 MD11
NB_MD15 3 14 MD15
NB_MD10 2 15 MD10
NB_MD14 1 16 MD14
RP11 10*8 RPX8
NB_MD24 8 9 MD24
NB_MD28 7 10 MD28
NB_MD19 6 11 MD19
NB_MD23 5 12 MD23
NB_MD18 4 13 MD18
NB_MD22 3 14 MD22
NB_DQS2 2 15 DQS2
NB_DM2 1 16 DM2
RP10 10*8 RPX8
NB_MD27 8 9 MD27
NB_MD31 7 10 MD31
NB_MD26 6 11 MD26
NB_MD30 5 12 MD30
NB_DQS3 4 13 DQS3
NB_DM3 3 14 DM3
NB_MD25 2 15 MD25
NB_MD29 1 16 MD29
RP7 10*8 RPX8
NB_WE# 8 9 WE#
NB_BA0 7 10 BA0
NB_MA10 6 11 MA10
NB_MA3 5 12 MA3
NB_MA7 4 13 MA7
NB_MA9 3 14 MA9
NB_MA12 2 15 MA12
NB_CAS# 1 16 CAS#
RP8 10*8 RPX8
NB_RAS# 8 9 RAS#
NB_BA1 7 10 BA1
NB_MA0 6 11 MA0
NB_MA11 5 12 MA11
NB_MA6 4 13 MA6
NB_MA8 3 14 MA8
NB_MD71 2 15 MD71
NB_MD66 1 16 MD66
RP6 10*8 RPX8
NB_MD34 8 9 MD34
NB_MD38 7 10 MD38
NB_DQS4 6 11 DQS4
NB_DM4 5 12 DM4
NB_MD33 4 13 MD33
NB_MD37 3 14 MD37
NB_MD32 2 15 MD32
NB_MD36 1 16 MD36
RP5 10*8 RPX8
NB_DQS5 8 9 DQS5
NB_DM5 7 10 DM5
NB_MD41 6 11 MD41
NB_MD45 5 12 MD45
NB_MD40 4 13 MD40
NB_MD44 3 14 MD44
NB_MD35 2 15 MD35
NB_MD39 1 16 MD39
RP4 10*8 RPX8
NB_MD49 8 9 MD49
NB_MD53 7 10 MD53
NB_MD48 6 11 MD48
NB_MD52 5 12 MD52
NB_MD43 4 13 MD43
NB_MD47 3 14 MD47
NB_MD42 2 15 MD42
NB_MD46 1 16 MD46
RP3 10*8 RPX8
NB_MD56 8 9 MD56
NB_MD60 7 10 MD60
NB_MD51 6 11 MD51
NB_MD55 5 12 MD55
NB_MD50 4 13 MD50
NB_MD54 3 14 MD54
NB_DQS6 2 15 DQS6
NB_DM6 1 16 DM6
RP2 10*8 RPX8
NB_MD59 8 9 MD59
NB_MD58 7 10 MD58
NB_DQS7 6 11 DQS7
NB_MD63 5 12 MD63
NB_MD57 4 13 MD57
NB_MD62 3 14 MD62
NB_DM7 2 15 DM7
NB_MD61 1 16 MD61
RP9 10*8 RPX8
NB_MD70 8 9 MD70
NB_MD67 7 10 MD67
NB_DM8 6 11 DM8
NB_MD69 5 12 MD69
NB_MD65 4 13 MD65
NB_DQS8 3 14 DQS8
NB_MD64 2 15 MD64
NB_MD68 1 16 MD68
6 NB_MA[6..12]
6 NB_MA0
6 NB_MA3
6 NB_BA0
6 NB_BA1
6 NB_RAS#
6 NB_WE#
6 NB_CAS#
6 NB_MD[0..71]
6 NB_DQS[0..8]
6 NB_DM[0..8]
6,9 SMA[1..2]
6,9 SMA[4..5]
MA[6..12] MA[6..12] 8,9
MA0 MA0 8,9
MA3 MA3 8,9
BA0 BA0 8,9
BA1 BA1 8,9
RAS# RAS# 8,9
WE# WE# 8,9
CAS# CAS# 8,9
MD[0..63] MD[0..63] 8,9
DQS[0..7] DQS[0..7] 8,9
DM[0..7] DM[0..7] 8,9
MD[64..71] MD[64..71] 9
DQS8 DQS8 9
DM8 DM8 9
+2.5V_DDR
R66 75 0603 1%
R65 75 0603 1%
C114 0.01U 0603D
C135 0.01U 0603D
C113 0.1U 0603 16V
C116 0.1U 0603 16V
C115 0.1U 0603 16V
C600 0.1U 0603 16V
+DDR_VREF
GND
+2.5V_DDR
+DDR_VREF
J503
MD0 MD1 MD2 MD3 MD8 MD9 MD10 MD11 MD16 MD17 MD18 MD19 MD24 MD25 MD26 MD27 MD64 MD65 MD66 MD67 MD32 MD33 MD34 MD35 MD40 MD41 MD42 MD43 MD48 MD49 MD50 MD51 MD56 MD57 MD58 MD59
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS8
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DM8
MD4 MD5 MD6 MD7 MD12 MD13 MD14 MD15 MD20 MD21 MD22 MD23 MD28 MD29 MD30 MD31 MD68 MD69 MD70 MD71 MD36 MD37 MD38 MD39 MD44 MD45 MD46 MD47 MD52 MD53 MD54 MD55 MD60 MD61 MD62 MD63
6 CLK_DDR0
6 CLK_DDR0#
6 CLK_DDR2
6 CLK_DDR2#
6,9 CKE1
CKE0 6,9
6,9 CS#0
CS#1 6,9
CLK_DDR1# 6
CLK_DDR1 6
4,11 SMBDATA
4,11 SMBCLK
+3V
C584 0.1U 0603 50V
0.6MM/200P/H5.2
QUASAR
CA0115-200N01
GND
+2.5V_DDR
C560 10U 1206 10V
C572 1U 0603D
C568 1U 0603D
C570 0.1U 0603D
C566 0.1U 0603 50V
C559 10U 1206 10V
C565 1U 0603D
C564 1U 0603D
C561 0.1U 0603 50V
C563 0.1U 0603D
C583 0.1U 0603 50V
C582 0.1U 0603 50V
C580 0.1U 0603 50V
C579 0.1U 0603 50V
C578 0.1U 0603 50V
C577 0.1U 0603 50V
C576 0.1U 0603 50V
C571 0.1U 0603 50V
C569 0.1U 0603 50V
C562 0.1U 0603 50V
GND
MiTAC
Title
SO-DIMM
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 7 of 28



MiTAC

Title: On Board DDR

Size	Document Number	Rev
C	41167*******	01

Date: Wednesday, June 11, 2003 Sheet 8 of 28

7,8 MD[0..63] — MD[0..63]
7,8 DQS[0..7] — DQS[0..7]
7,8 DM[0..7] — DM[0..7]
7 MD[64..71] — MD[64..71]
7 DQS8 — DQS8
7 DM8 — DM8

Data Signals - SDQ[63:0],DM[7:0],DQS[7:0]

Chip -> Rs -> So-DIMM0 -> So-DIMM1 -> Rt

Control Signals - CKE[3:0],CS#[3:0]

Chip -> So-DIMM0 -> So-DIMM1 -> Rt

Command Signals - MA[12:6,3,0],BA[1:0],RAS#,CAS#,WE#

1.Chip -> So-DIMM0 -> Rs -> So-DIMM1 -> Rt

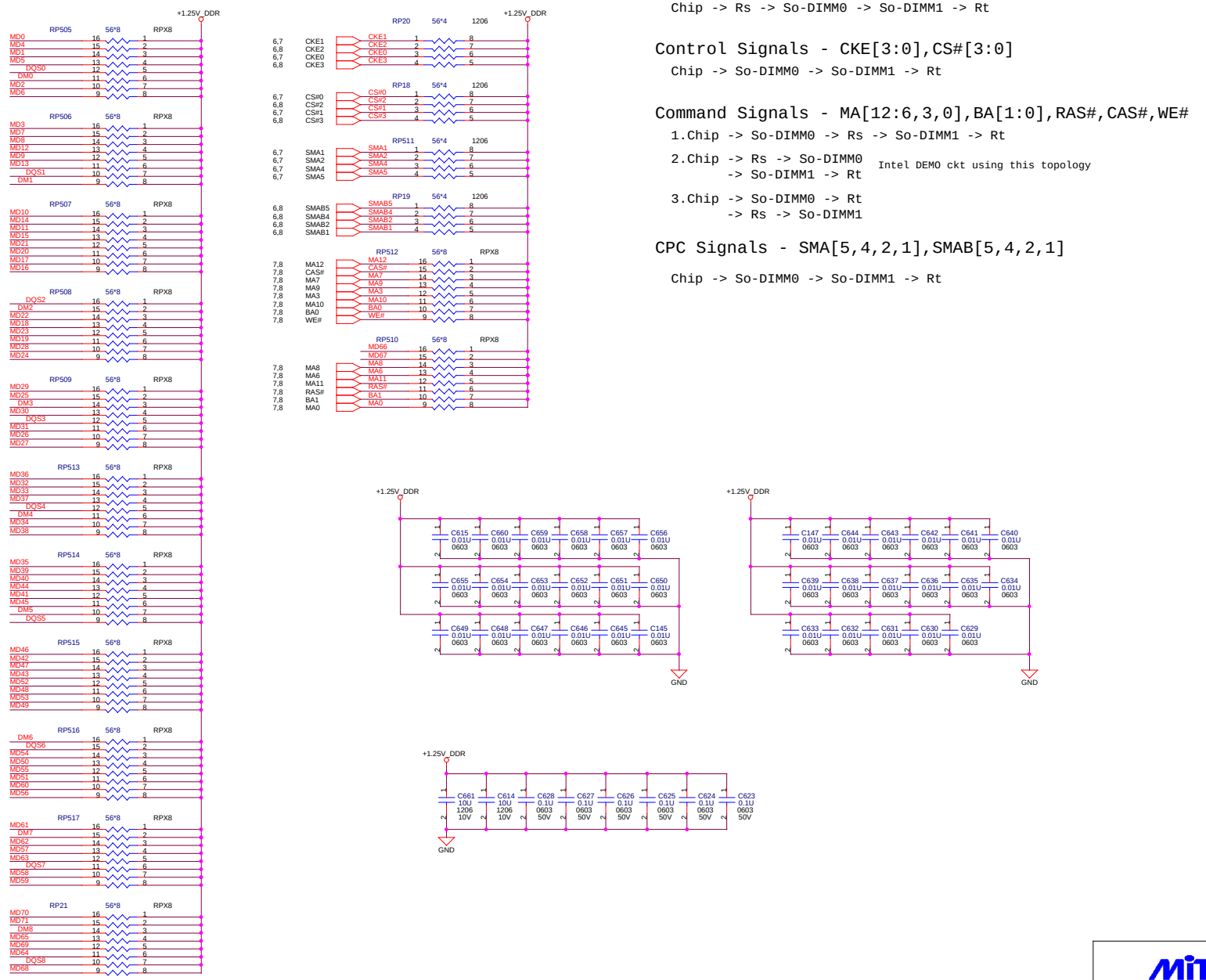
2.Chip -> Rs -> So-DIMM0
-> So-DIMM1 -> Rt

Intel DEMO ckt using this topology

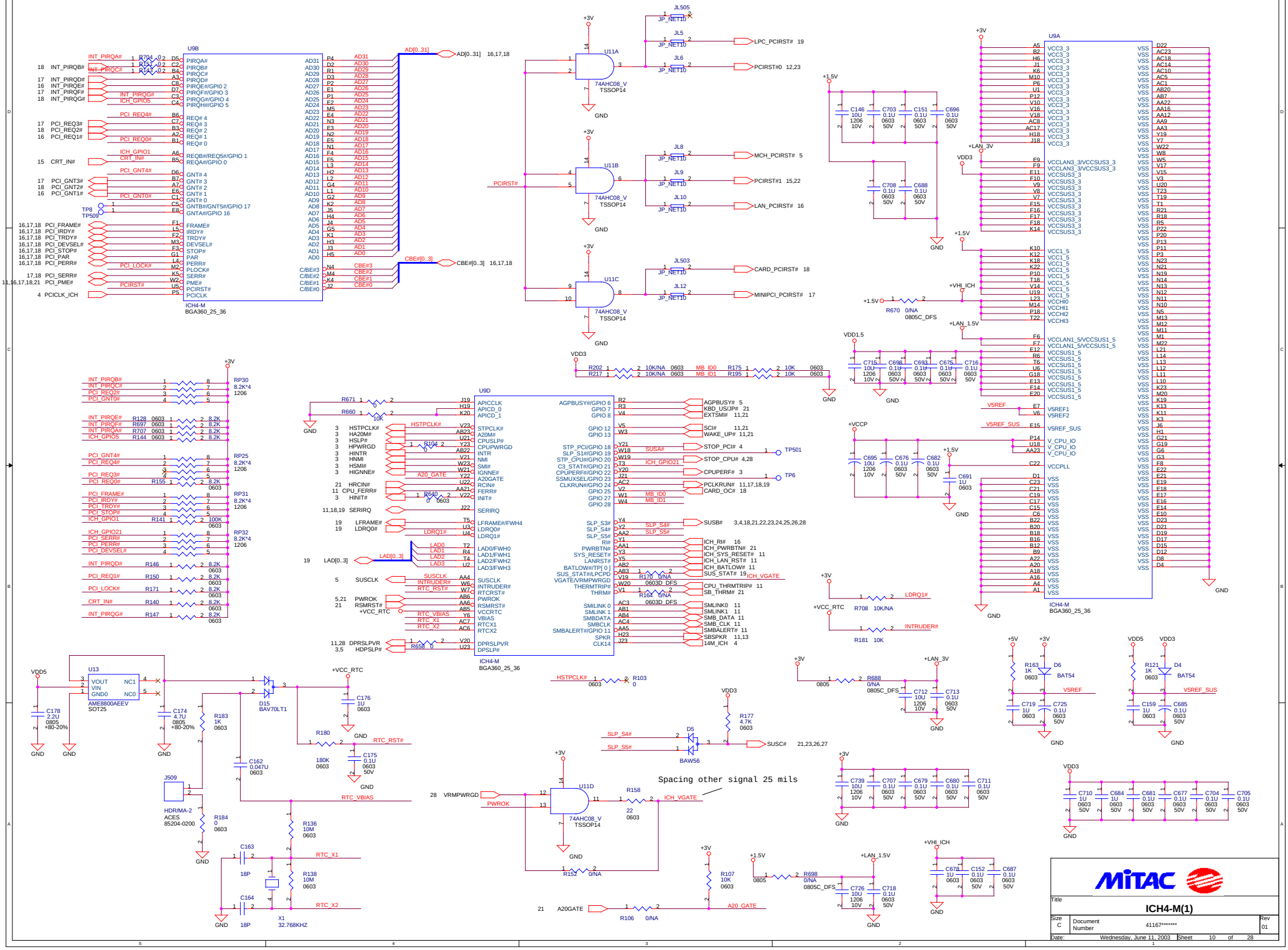
3.Chip -> So-DIMM0 -> Rt
-> Rs -> So-DIMM1

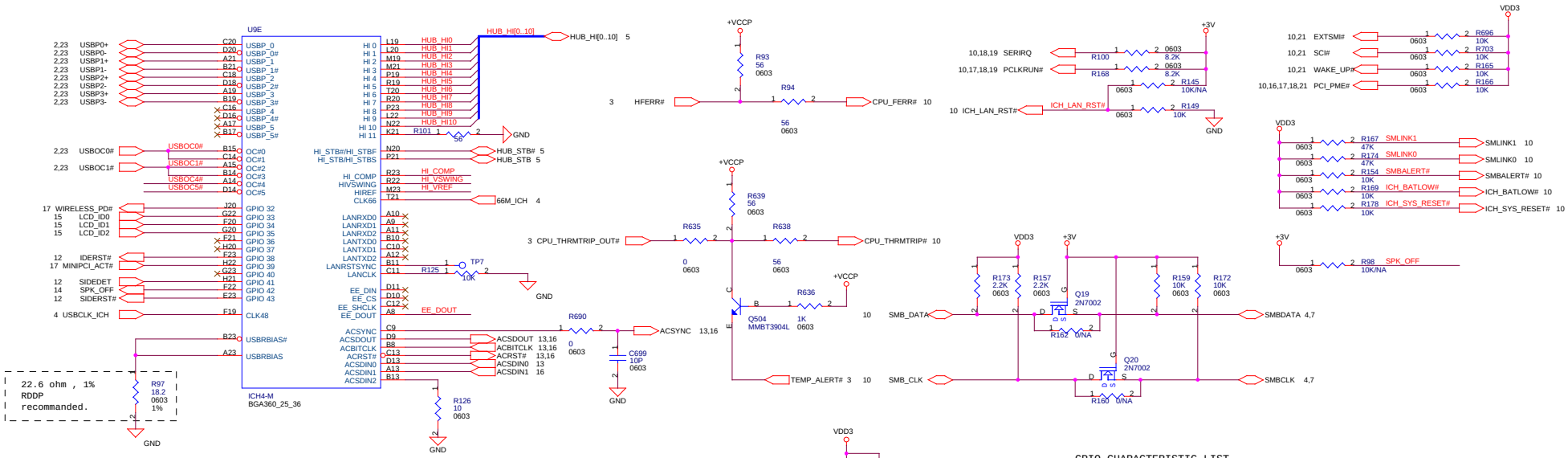
CPC Signals - SMA[5,4,2,1],SMAB[5,4,2,1]

Chip -> So-DIMM0 -> So-DIMM1 -> Rt

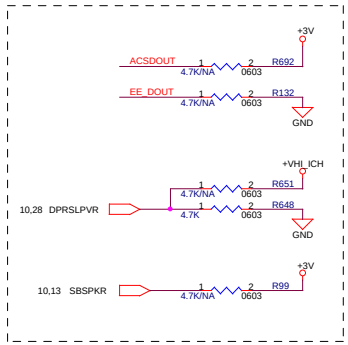


Title	DDR Termination		
Size C	Document Number 41167*******		Rev 01
Date: Wednesday, June 11, 2003	Sheet 9 of 28		


U9B
ICH4-M
BGA360_25_36
U11A
U11B
U11C
74AHC08_V
TSSOP14
U9A
U9D
U13
AME8800AEEV
SOT25
D15
BAV70LT1
J509
HDR/MA-2
ACES
85204-0200
X1
32.768KHZ
U11D
D5
BAW56
Spacing other signal 25 mils
Title
ICH4-M(1)
Size
C
Document Number
41167******
Rev
01
Date:
Wednesday, June 11, 2003
Sheet
10
of
28



STRAPPING



STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

GPIO CHARACTERISTIC LIST

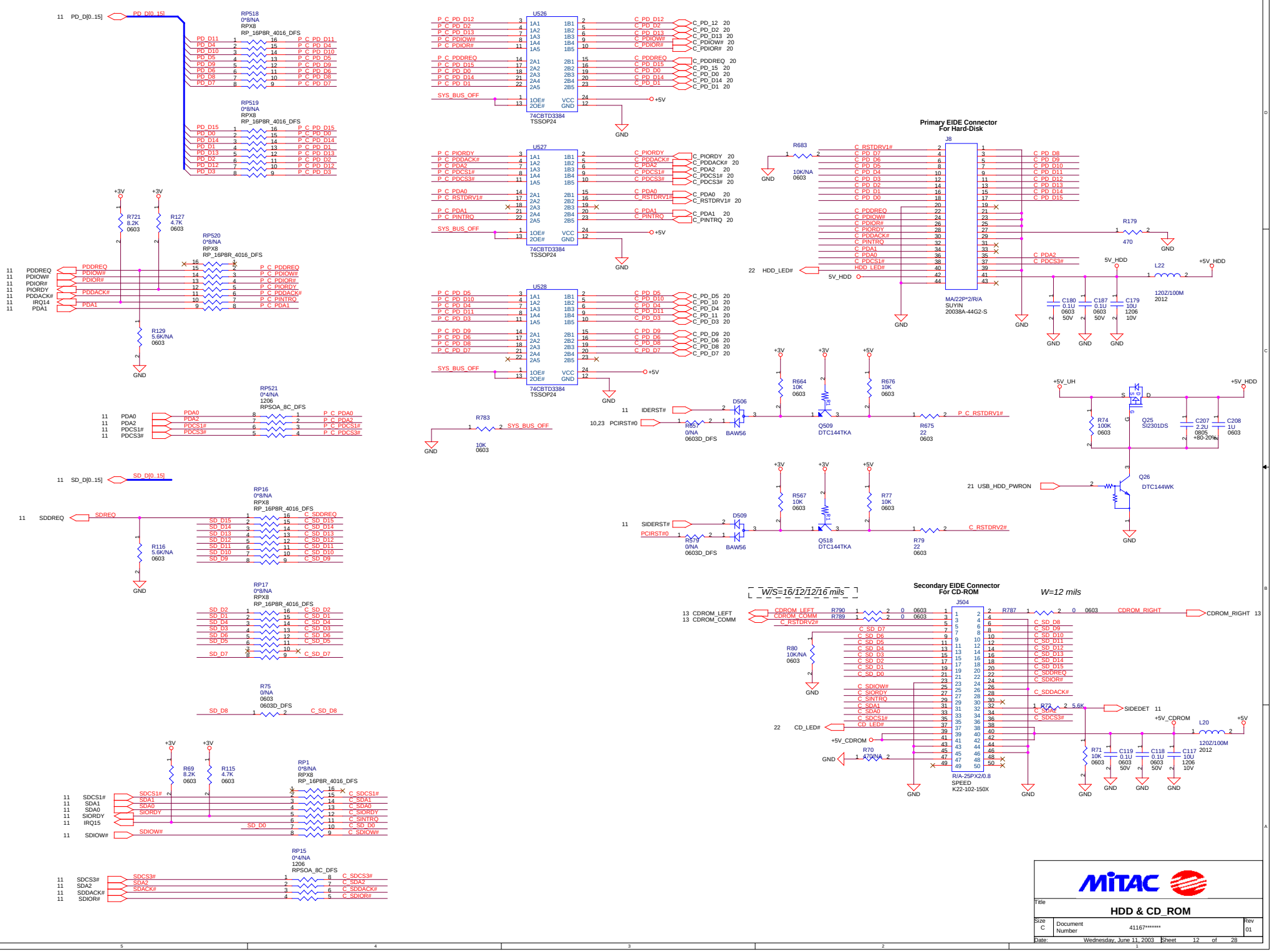
NAME	TYPE	POWER PLANE	CURRENT DEFINE
GPIO[0]	I	MAIN POWER WELL	CRT_IN#
GPIO[1]	I	MAIN POWER WELL	X
GPIO[2]	I	MAIN POWER WELL	INT_PIRQE#
GPIO[3]	I	MAIN POWER WELL	INT_PIRQF#
GPIO[4]	I	MAIN POWER WELL	INT_PIRQG#(Pull high only)
GPIO[5]	I	MAIN POWER WELL	X
GPIO[6]	I	MAIN POWER WELL	AGP_BUSY#
GPIO[7]	I	MAIN POWER WELL	KB_US/JP#
GPIO[8]	I	RESUME POWER WELL	EXTSMI#
GPIO[11]	I	RESUME POWER WELL	SMBALERT#(Pull high only)
GPIO[12]	I	RESUME POWER WELL	SCI#
GPIO[13]	I	RESUME POWER WELL	WAKE_UP#
GPIO[16]	O	MAIN POWER WELL	X
GPIO[17]	O	MAIN POWER WELL	X
GPIO[18]	O	MAIN POWER WELL	STOP_PCI#
GPIO[19]	O	MAIN POWER WELL	SUSA#
GPIO[20]	O	MAIN POWER WELL	STOP_CPU#
GPIO[21]	O	MAIN POWER WELL	X
GPIO[22]	OD	MAIN POWER WELL	CPUPERF#
GPIO[23]	O	MAIN POWER WELL	X
GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
GPIO[25]	I/O	RESUME POWER WELL	CARD_OC#
GPIO[27]	I/O	RESUME POWER WELL	MB_ID0
GPIO[28]	I/O	RESUME POWER WELL	MB_ID1
GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PD#
GPIO[33]	I/O	MAIN POWER WELL	LCDID0
GPIO[34]	I/O	MAIN POWER WELL	LCDID1
GPIO[35]	I/O	MAIN POWER WELL	LCDID2
GPIO[36]	I/O	MAIN POWER WELL	X
GPIO[37]	I/O	MAIN POWER WELL	X
GPIO[38]	I/O	MAIN POWER WELL	IDERST#
GPIO[39]	I/O	MAIN POWER WELL	MINIPCI_ACT#
GPIO[40]	I/O	MAIN POWER WELL	X
GPIO[41]	I/O	MAIN POWER WELL	SIDEDET
GPIO[42]	I/O	MAIN POWER WELL	SPK_OFF
GPIO[43]	I/O	MAIN POWER WELL	SIDERST#

MiTAC

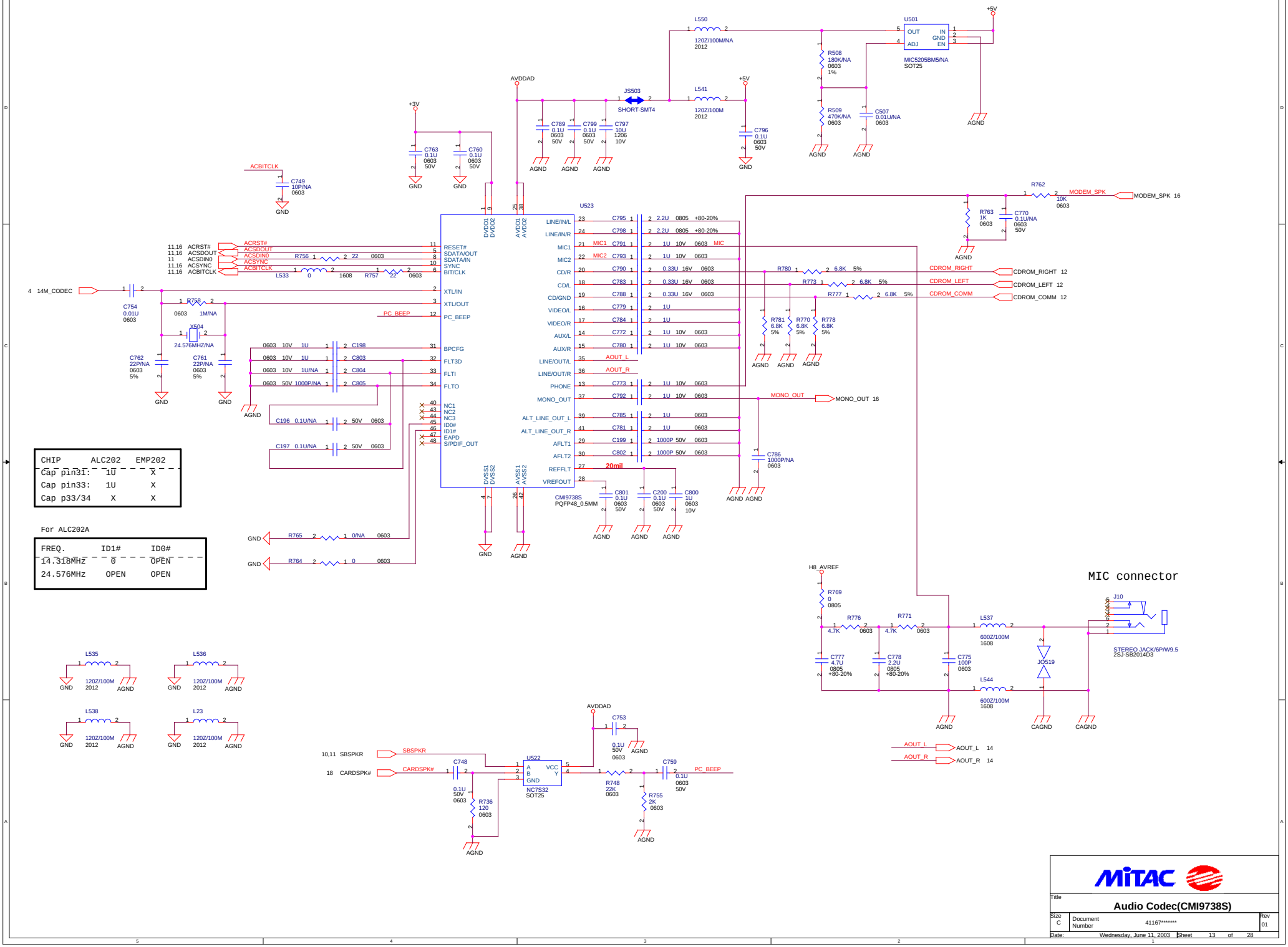
Title: ICH4-M(2)

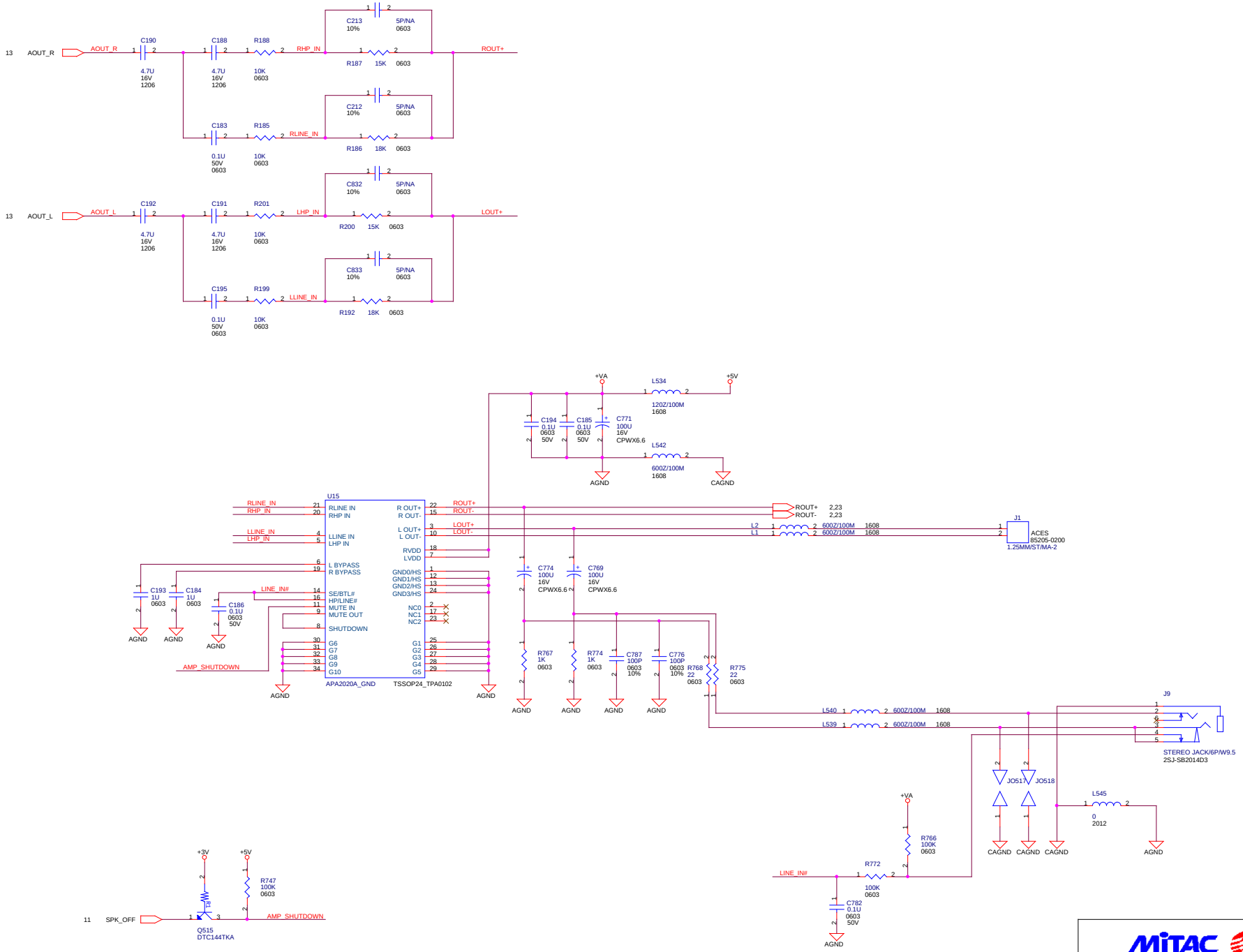
Size: C | Document Number: 41167****** | Rev: 01

Date: Wednesday, June 11, 2003 | Sheet 11 of 28



Primary EIDE Connector
For Hard-Disk
J8
MA/22P*2/R/A
SUYIN
20038A-44G2-S
Secondary EIDE Connector
For CD-ROM
J504
R/A-25PX2/0.8
SPEED
K22-102-150X
W/S=16/12/12/16 mils
W=12 mils
U526
U527
U528
74CBTD3384
TSSOP24
RP518
RP519
RP520
RP521
RP16
RP17
RP1
RP15
RP16P8R_4016_DFS
RPSOA_8C_DFS
Q509
DTC144TKA
Q518
DTC144TKA
Q25
SI2301DS
Q26
DTC144WK
D506
D509
BAW56
MITAC
Title
HDD & CD_ROM
Size
C
Document Number
41167*******
Rev
01
Date: Wednesday, June 11, 2003
Sheet 12 of 28

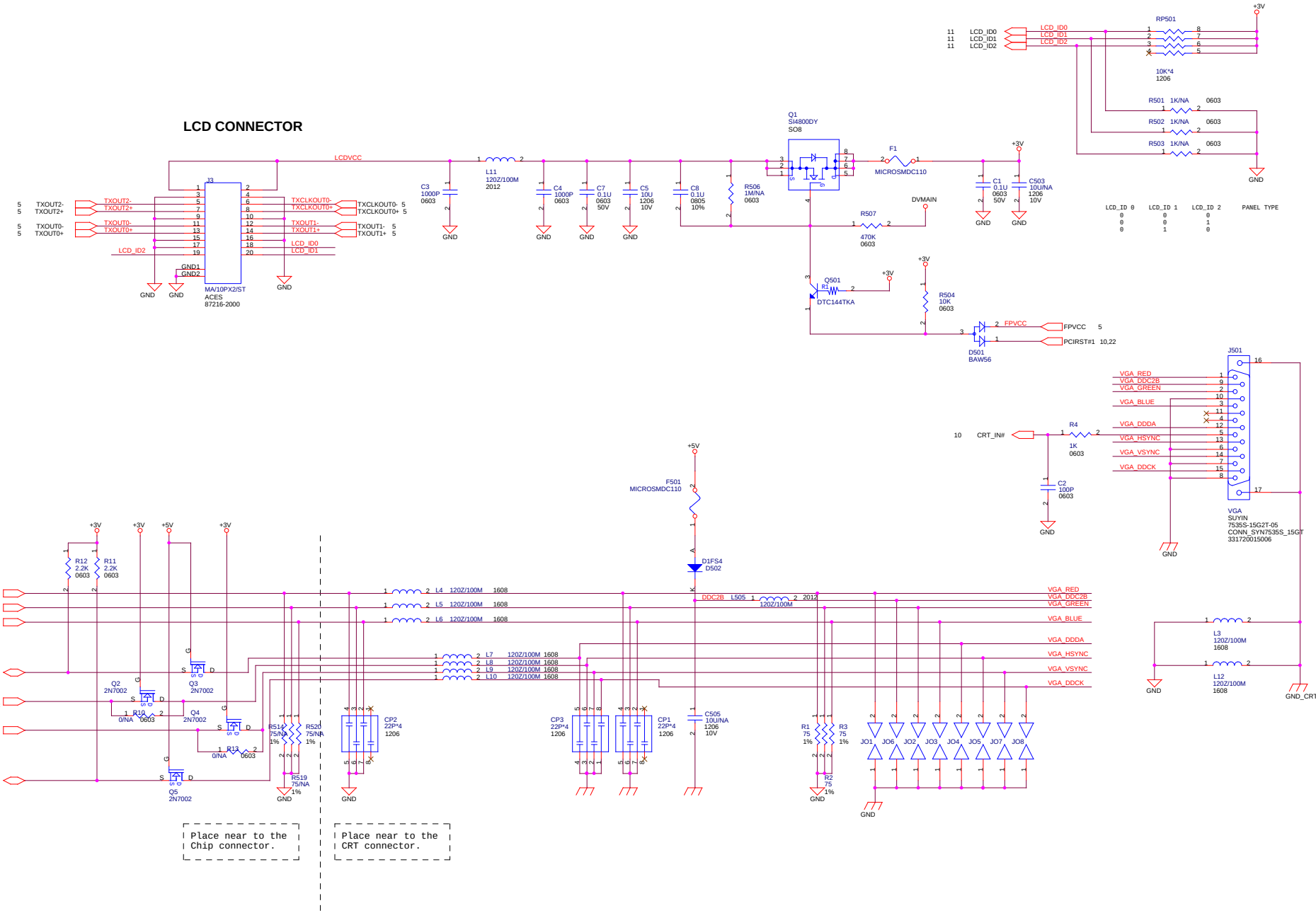

CHIP ALC202 EMP202
Cap pin31: 1U X
Cap pin33: 1U X
Cap p33/34 X X
For ALC202A
FREQ. ID1# ID0#
14.318MHz 0 OPEN
24.576MHz OPEN OPEN
U523
CMI9738S
PQFP48_0.5MM
U501
MIC5205BM5/NA
SOT25
U522
NC7S32
SOT25
MIC connector
J10
STEREO JACK/6P/W9.5
2SJ-SB2014D3
MiTAC
Title
Audio Codec(CMI9738S)
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 13 of 28



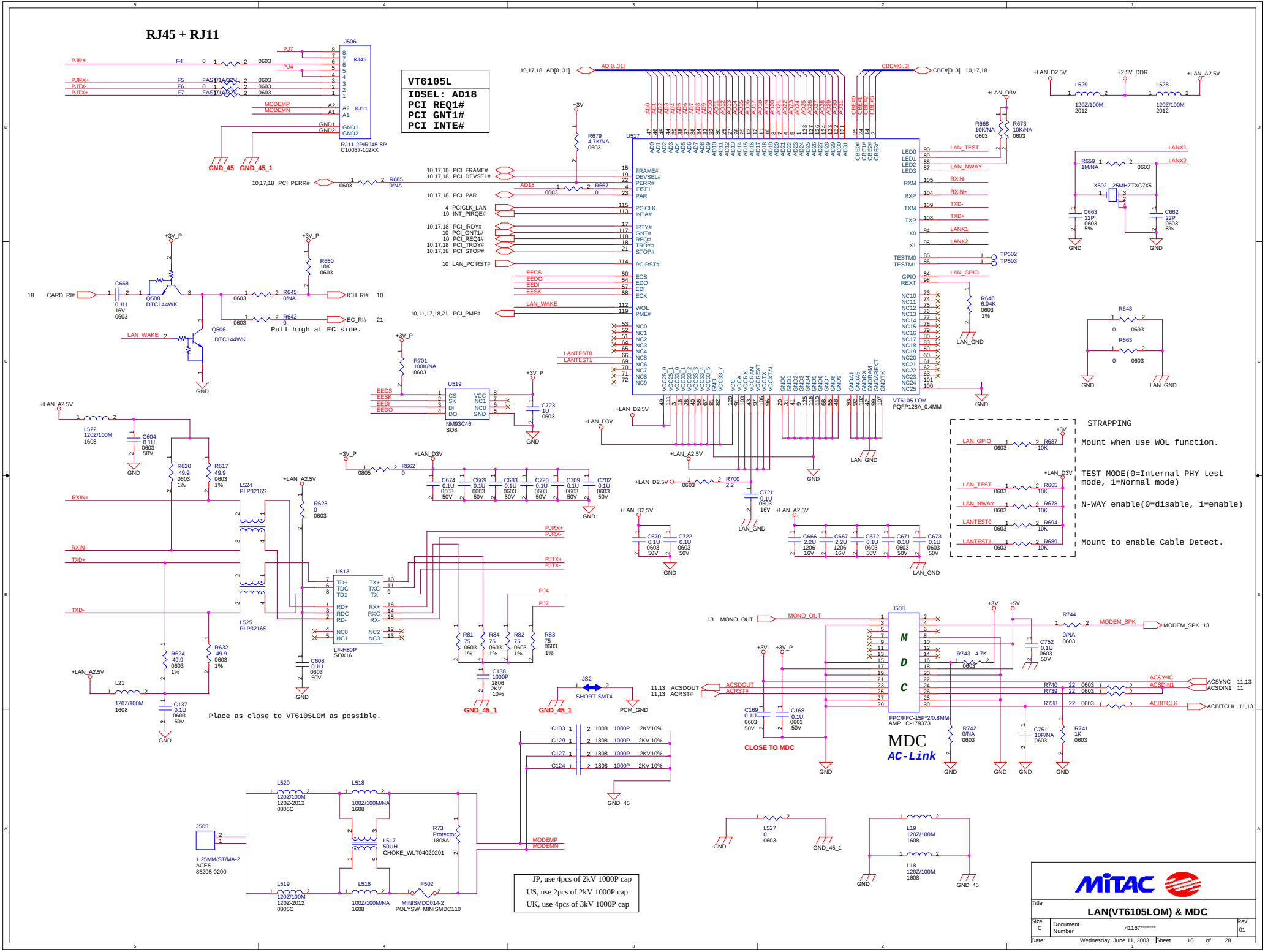
MiTAC

Title	OP AMP(APA2020)	
Size C	Document Number 41167******	Rev 01
Date: Wednesday, June 11, 2003	Sheet 14 of 28	

LCD CONNECTOR

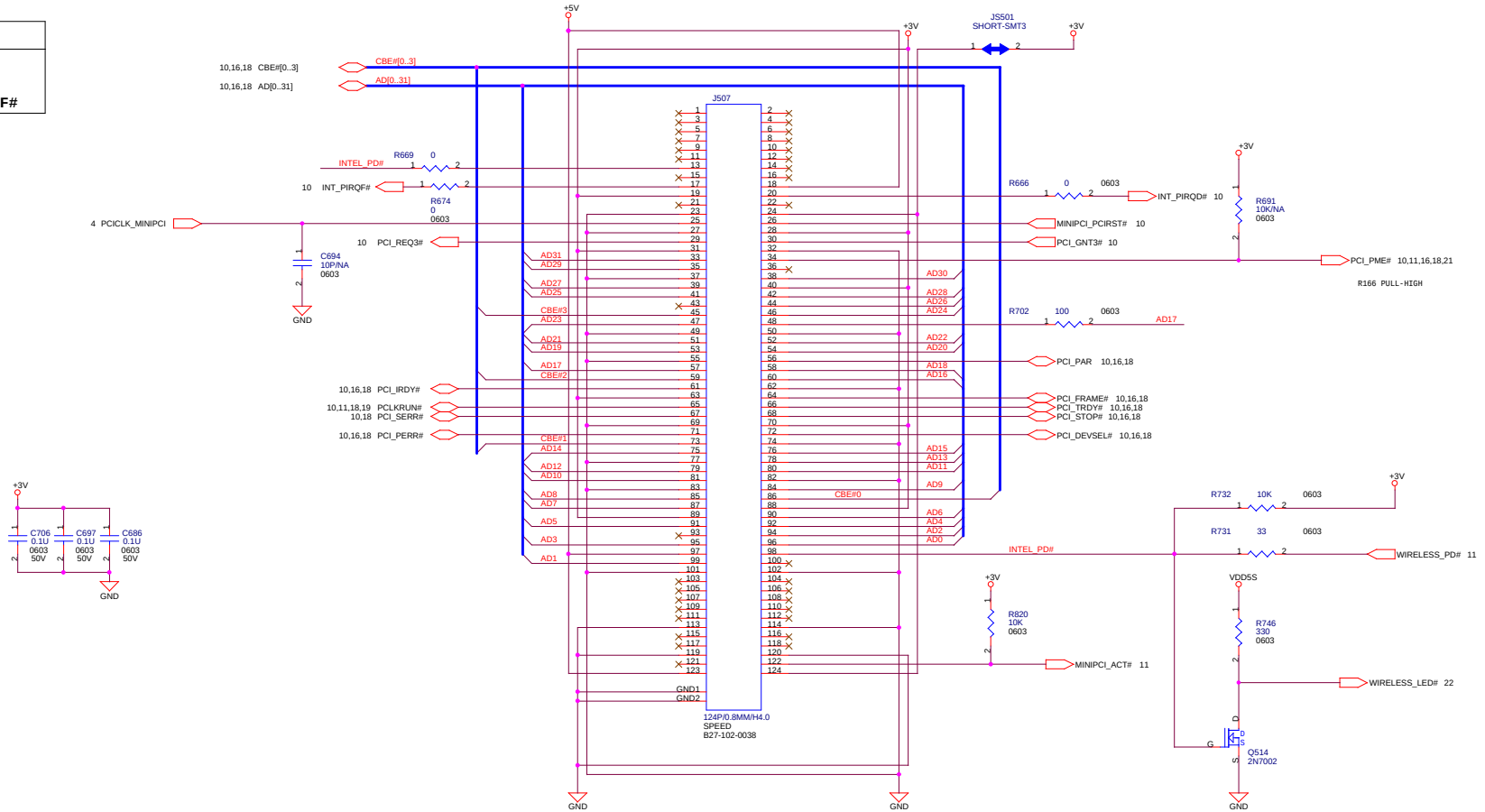


Title	LCD & CRT connector
Size	C
Document Number	41167******
Rev	01
Date:	Wednesday, June 11, 2003
Sheet	15 of 28

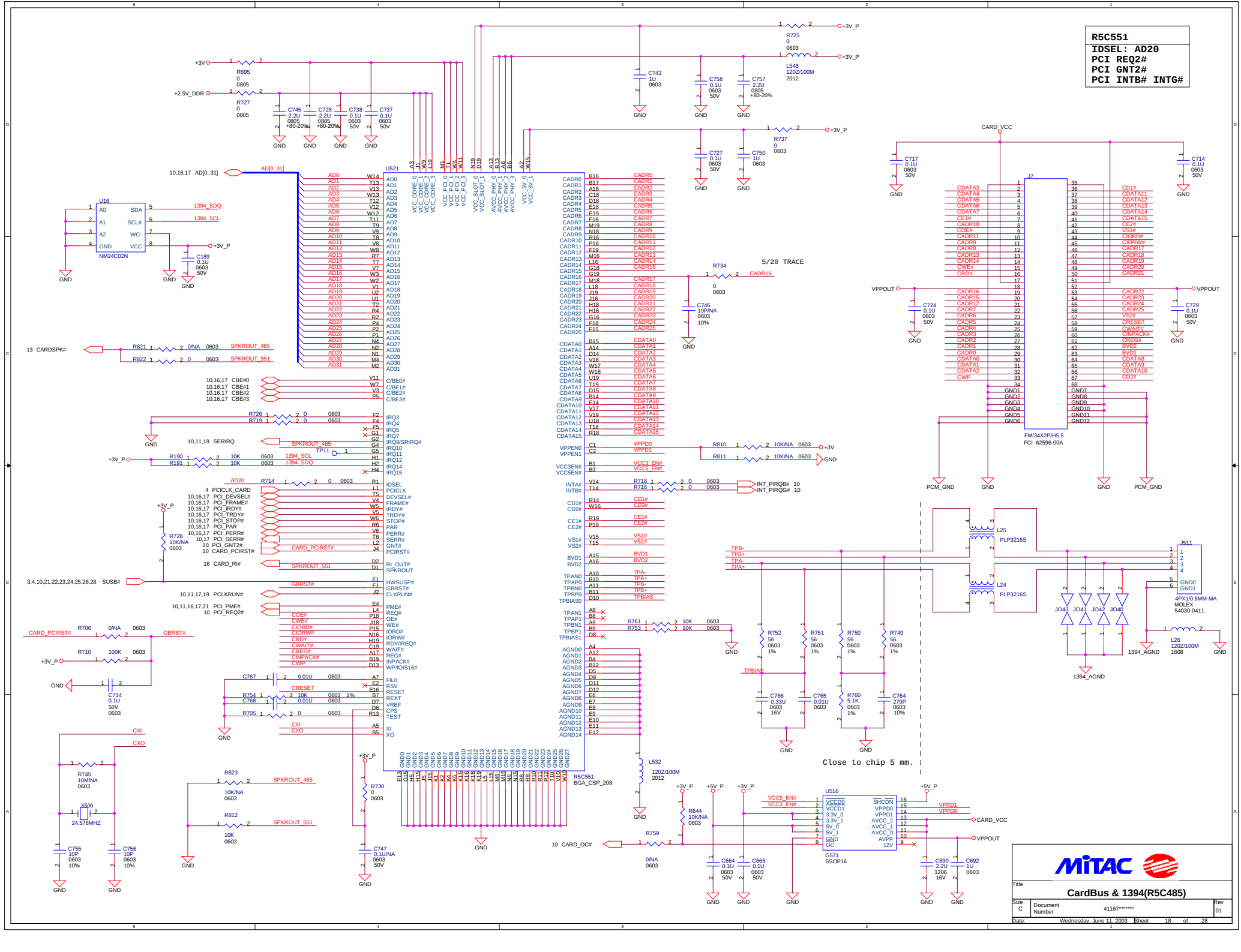

RJ45 + RJ11
VT6105L
IDSEL: AD18
PCI REQ1#
PCI GNT1#
PCI INTE#
J506
RJ11-2P/RJ45-8P
C10037-102XX
U517
VT6105-LOM
PQFP128A_0.4MM
U519
NM93C46
SO8
U513
LF-H80P
SOX16
J508
FPC/FFC-15P*2/0.8MM
AMP C-179373
MDC
AC-Link
CLOSE TO MDC
Pull high at EC side.
Place as close to VT6105LOM as possible.
STRAPPING
Mount when use WOL function.
TEST MODE(0=Internal PHY test mode, 1=Normal mode)
N-WAY enable(0=disable, 1=enable)
Mount to enable Cable Detect.
JP, use 4pcs of 2kV 1000P cap
US, use 2pcs of 2kV 1000P cap
UK, use 4pcs of 3kV 1000P cap
MiTAC
Title
LAN(VT6105LOM) & MDC
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 16 of 28

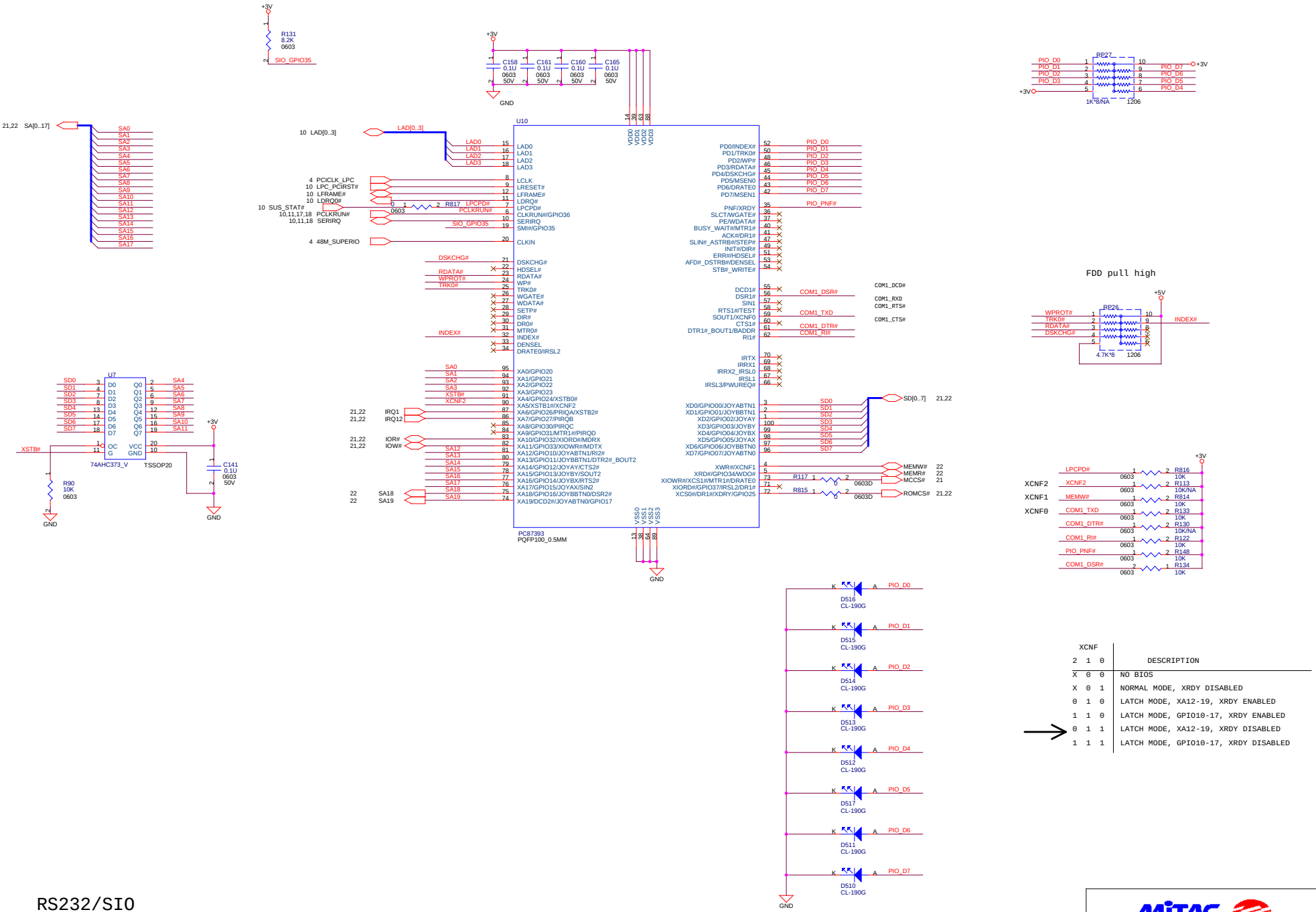
Mini PCI

IDSEL: AD17
PCI REQ3#
PCI GNT3#
PCI INTD# INTF#

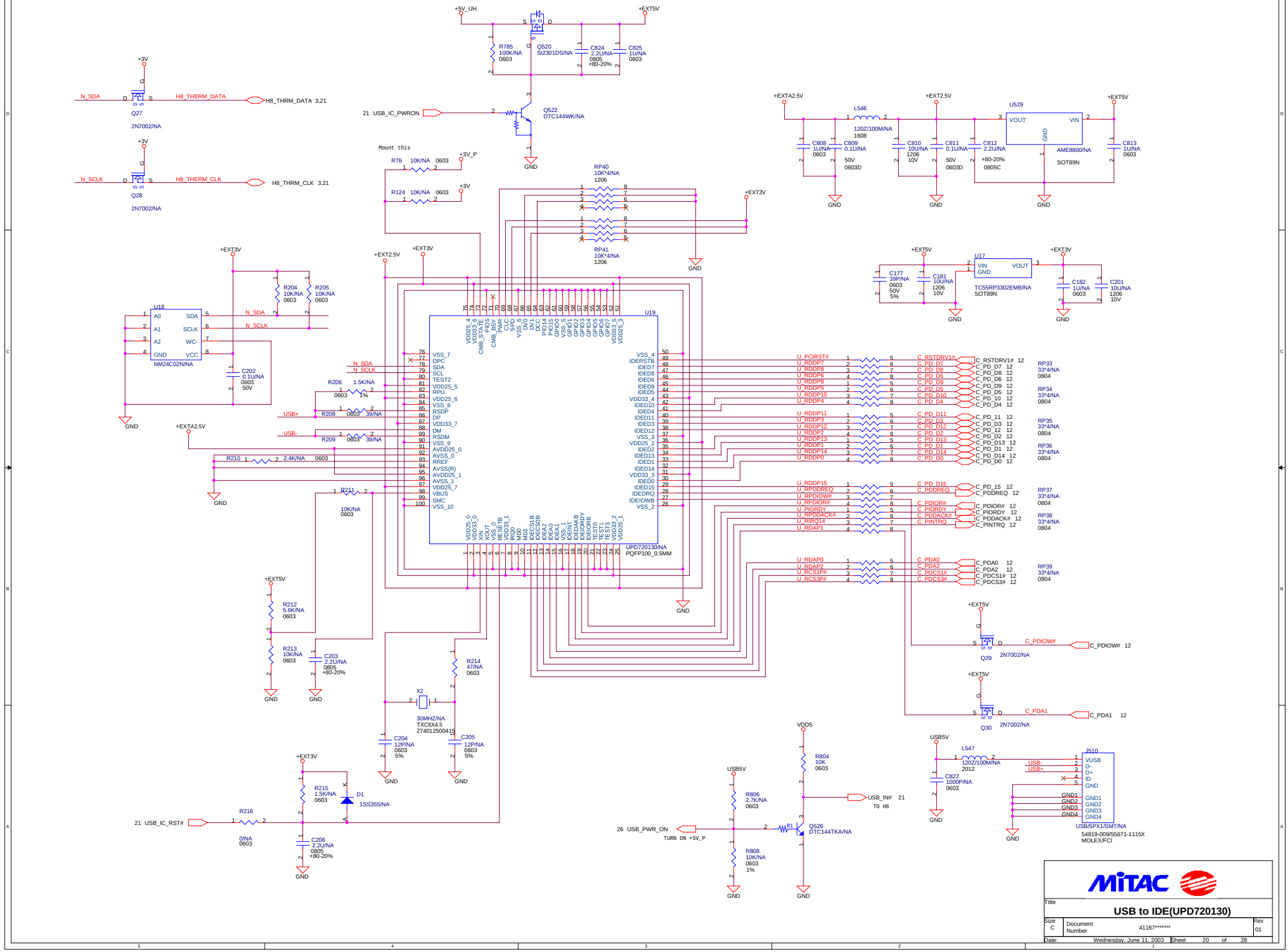


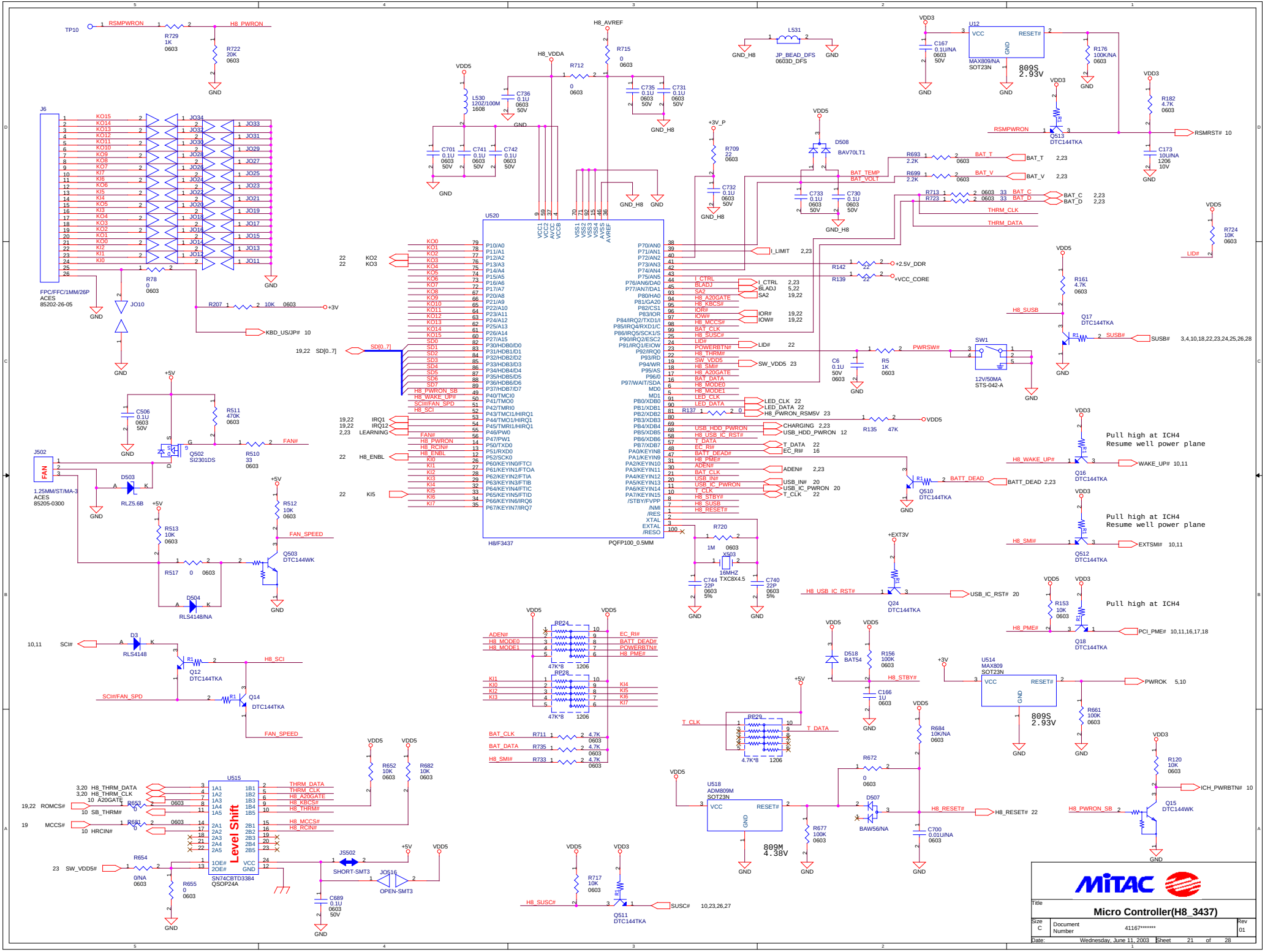
Title	Mini PCI		
Size C	Document Number 41167*******		Rev 01
Date: Wednesday, June 11, 2003	Sheet 17 of 28		


R5C551
IDSEL: AD20
PCI REQ2#
PCI GNT2#
PCI INTB# INTG#
U521
R5C551
BGA_CSP_208
U16
NM24C02N
J7
FM/34X2P/H5.5
FCI 62596-00A
U516
G571
SSOP16
5/20 TRACE
Close to chip 5 mm.
CardBus & 1394(R5C485)
MiTAC
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 18 of 28



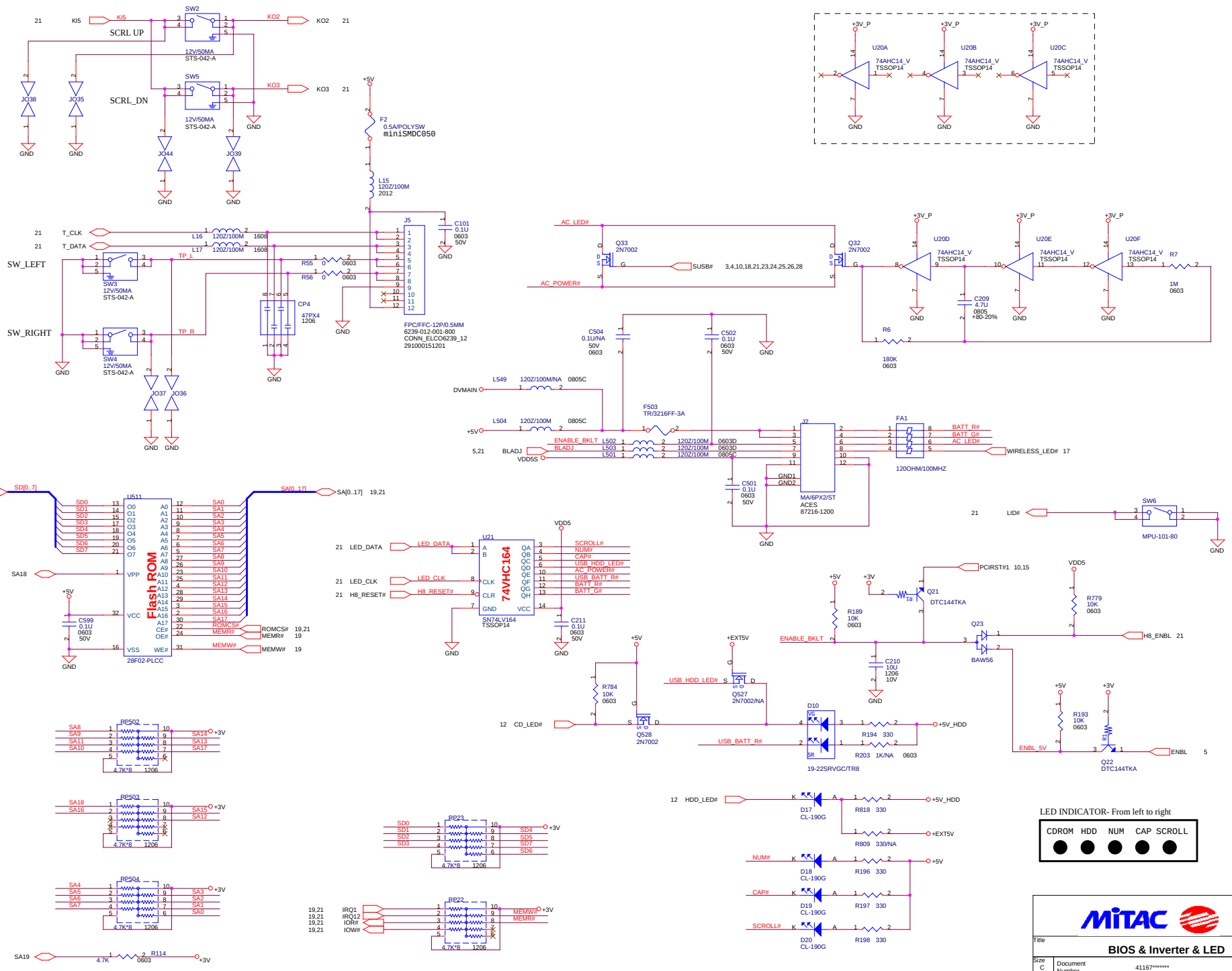
XCNF			DESCRIPTION
2	1	0	
X	0	0	NO BIOS
X	0	1	NORMAL MODE, XRDY DISABLED
0	1	0	LATCH MODE, XA12-19, XRDY ENABLED
1	1	0	LATCH MODE, GPIO10-17, XRDY ENABLED
0	1	1	LATCH MODE, XA12-19, XRDY DISABLED
1	1	1	LATCH MODE, GPIO10-17, XRDY DISABLED


+5V_UH
+EXT5V
R785 100K/NA 0603
Q520 SI2301DS/NA
C824 2.2U/NA 0805 +80-20%
C825 1U/NA 0603
21 USB_IC_PWRON
Q522 DTC144WK/NA
+3V
N_SDA
H8_THERM_DATA
H8_THRM_DATA 3,21
Q27
2N7002/NA
N_SCLK
H8_THERM_CLK
H8_THRM_CLK 3,21
Q28
2N7002/NA
Mount this
R76 10K/NA 0603
+3V_P
R124 10K/NA 0603
RP40 10K*4/NA 1206
RP41 10K*4/NA 1206
+EXT3V
GND
+EXTA2.5V
+EXT2.5V
L546 120Z/100M/NA 1608
C808 1U/NA 0603
C809 0.1U/NA 50V 0603D
C810 10U/NA 1206 10V
C811 0.1U/NA 50V 0603D
C812 2.2U/NA +80-20% 0805C
U529 AME8800/NA SOT89N
VOUT
VIN
GND
C813 1U/NA 0603
U17 TC55RP3302EMB/NA SOT89N
C177 39P/NA 0603 50V 5%
C181 10U/NA 1206 10V
C182 1U/NA 0603
C201 10U/NA 1206 10V
U18 NM24C02N/NA
A0
A1
A2
GND
SDA
SCLK
WC-
VCC
R204 10K/NA 0603
R205 10K/NA 0603
C202 0.1U/NA 0603 50V
U19
UPD720130/NA PQFP100_0.5MM
R206 1.5K/NA 0603 1%
R208 39/NA 0603
R209 39/NA 0603
USB+
USB-
R210 2.4K/NA 0603
R211 10K/NA 0603
R212 5.6K/NA 0603
R213 10K/NA 0603
C203 2.2U/NA 0805 +80-20%
R214 47/NA 0603
X2 30MHZ/NA TXC8X4.5 274012500415
C204 12P/NA 0603 5%
C205 12P/NA 0603 5%
R215 1.5K/NA 0603
D1 1SS355/NA
R216 0/NA 0603
21 USB_IC_RST#
C206 2.2U/NA 0805 +80-20%
U_PCIRST#
U_RDDP7
U_RDDP8
U_RDDP6
U_RDDP9
U_RDDP5
U_RDDP10
U_RDDP4
U_RDDP11
U_RDDP3
U_RDDP12
U_RDDP2
U_RDDP13
U_RDDP1
U_RDDP14
U_RDDP0
U_RDDP15
U_RPDDREQ
U_RPDIOW#
U_RPDIOR#
U_PIORDY
U_RPDDACK#
U_RIRQ14
U_RDAP1
U_RDAP0
U_RDAP2
U_RCS1P#
U_RCS3P#
C_RSTDRV1#
C_PD_D7
C_PD_D8
C_PD_D6
C_PD_D9
C_PD_D5
C_PD_D10
C_PD_D4
C_PD_D11
C_PD_D3
C_PD_D12
C_PD_D2
C_PD_D13
C_PD_D1
C_PD_D14
C_PD_D0
C_PD_D15
C_PDDREQ
C_PDIOR#
C_PIORDY
C_PDDACK#
C_PINTRQ
C_PDA0
C_PDA2
C_PDCS1#
C_PDCS3#
RP33 33*4/NA 0804
RP34 33*4/NA 0804
RP35 33*4/NA 0804
RP36 33*4/NA 0804
RP37 33*4/NA 0804
RP38 33*4/NA 0804
RP39 33*4/NA 0804
C_PDIOW#
C_PDA1
Q29 2N7002/NA
Q30 2N7002/NA
VDD5
USB5V
R804 10K 0603
R806 2.7K/NA 0603
R808 10K/NA 0603 1%
Q526 DTC144TKA/NA
USB_IN# 21
TO H8
26 USB_PWR_ON
TURN ON +5V_P
L547 120Z/100M/NA 2012
C822 1000P/NA 0603
J510
VUSB
D-
D+
ID
GND
GND1
GND2
GND3
GND4
USB/5PX1/SMT/NA
54819-009/55671-1115X
MOLEX/FCI
MiTAC
Title
USB to IDE(UPD720130)
Size C
Document Number 41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 20 of 28

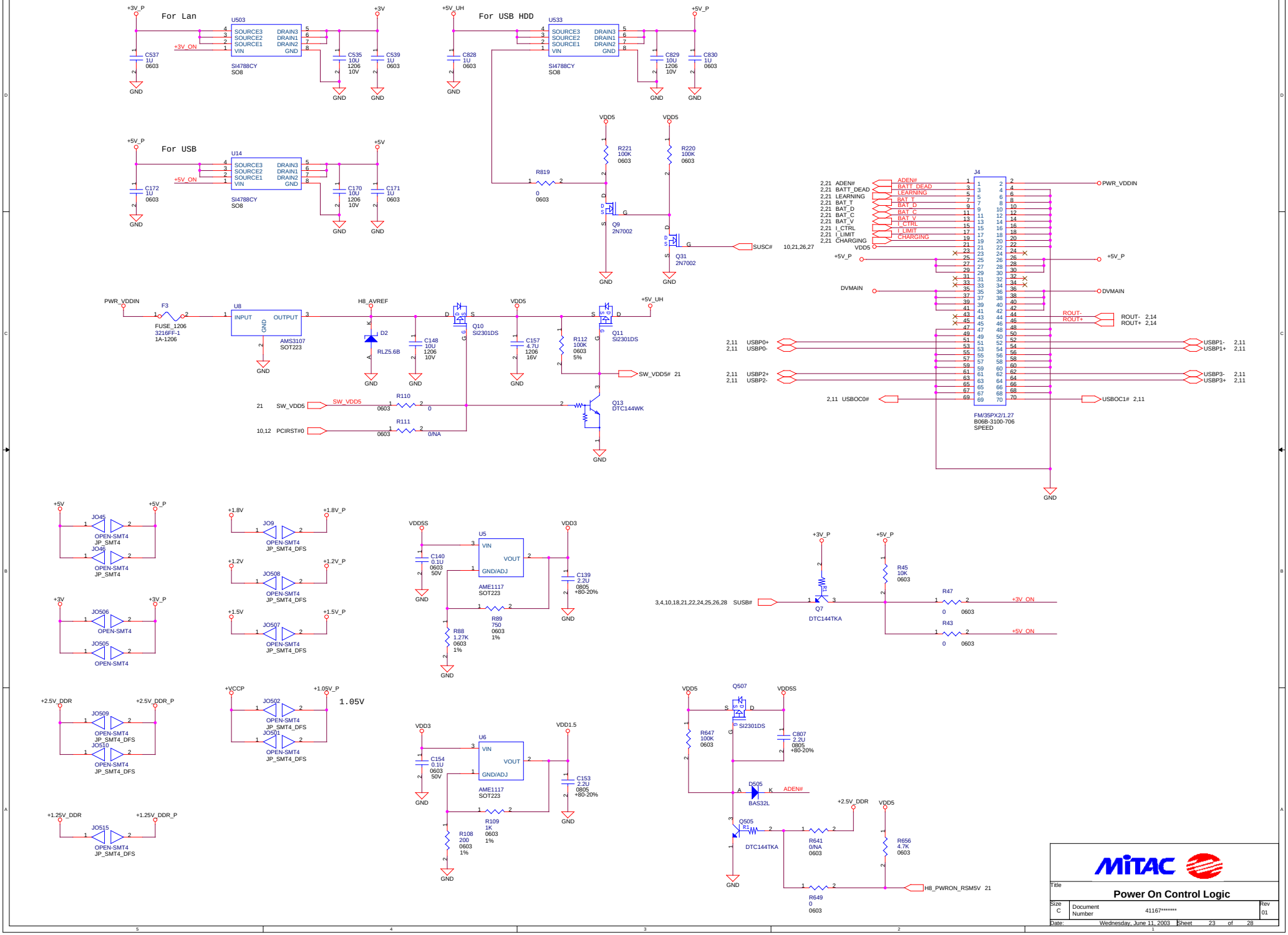


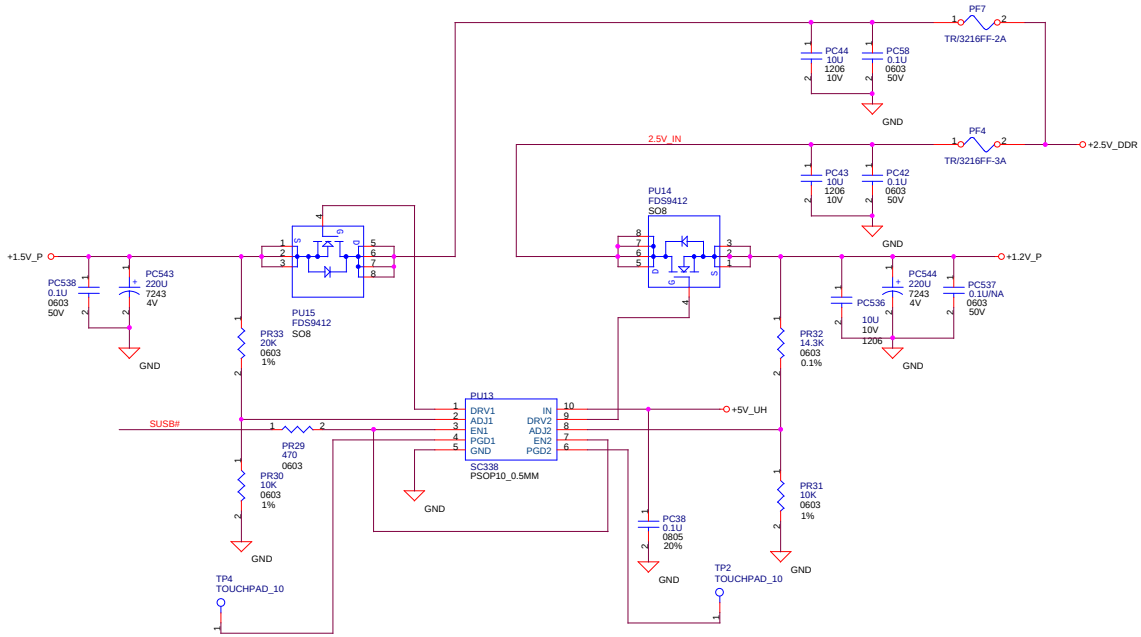
Title	Micro Controller(H8_3437)		
Size C	Document Number 41167*******		Rev 01
Date: Wednesday, June 11, 2003	Sheet 21 of 28		

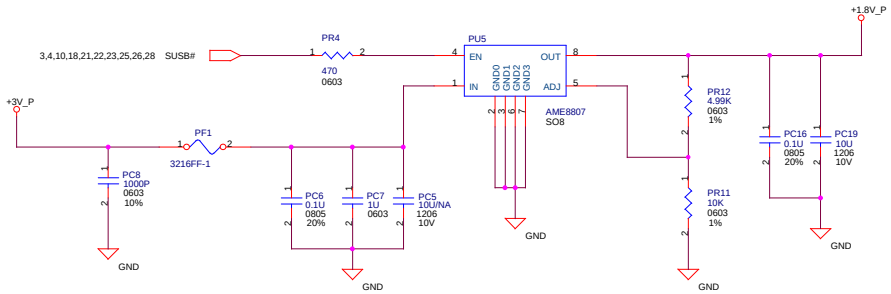
TOUCH_PAD



Title	BIOS & Inverter & LED
Size	C
Document Number	41167******
Rev	01
Date:	Wednesday, June 11, 2003
Sheet	22 of 28

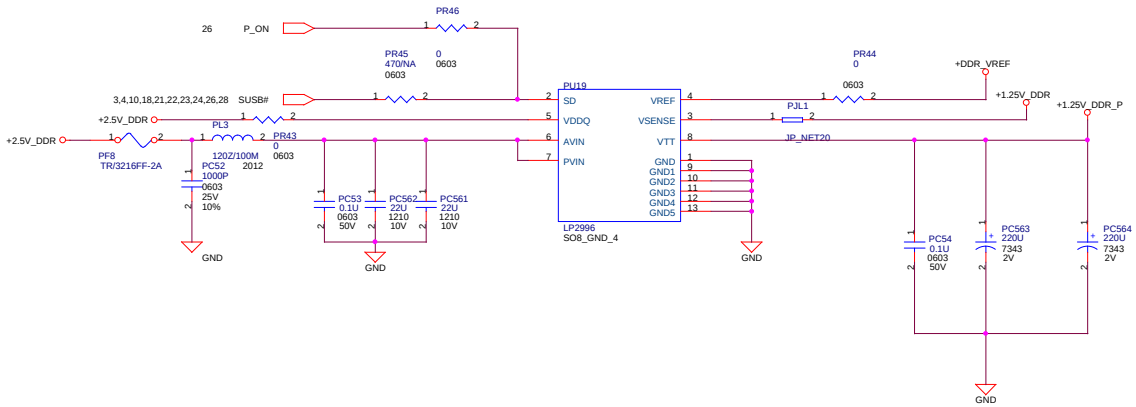

For Lan
For USB HDD
For USB
U503
U533
U14
SI4788CY
SO8
U8
AMS3107
SOT223
U5
U6
AME1117
SOT223
J4
FM/35PX2/1.27
B06B-3100-706
SPEED
Q9
2N7002
Q31
2N7002
Q10
SI2301DS
Q11
SI2301DS
Q13
DTC144WK
Q7
DTC144TKA
Q507
SI2301DS
Q505
DTC144TKA
D505
BAS32L
D2
RLZ5.6B
F3
FUSE_1206
3216FF-1
1A-1206
PWR_VDDIN
H8_AVREF
+5V_UH
SW_VDD5
PCIRST#0
SUSC#
SUSB#
ADEN#
BATT_DEAD
LEARNING
BAT_T
BAT_D
BAT_C
BAT_V
I_CTRL
I_LIMIT
CHARGING
DVMAIN
ROUT-
ROUT+
USBP0+
USBP0-
USBP1-
USBP1+
USBP2+
USBP2-
USBP3-
USBP3+
USBOC0#
USBOC1#
SW_VDD5#
+3V_ON
+5V_ON
+3V_P
+5V_P
+5V
+1.8V_P
+1.2V_P
+1.5V_P
+1.05V_P
+2.5V_DDR_P
+1.25V_DDR_P
+VCCP
1.05V
VDD5
VDD3
VDD1.5
VDD5S
GND
H8_PWRON_RSM5V
MiTAC
Title
Power On Control Logic
Size
C
Document Number
41167*******
Rev
01
Date:
Wednesday, June 11, 2003
Sheet
23
of
28





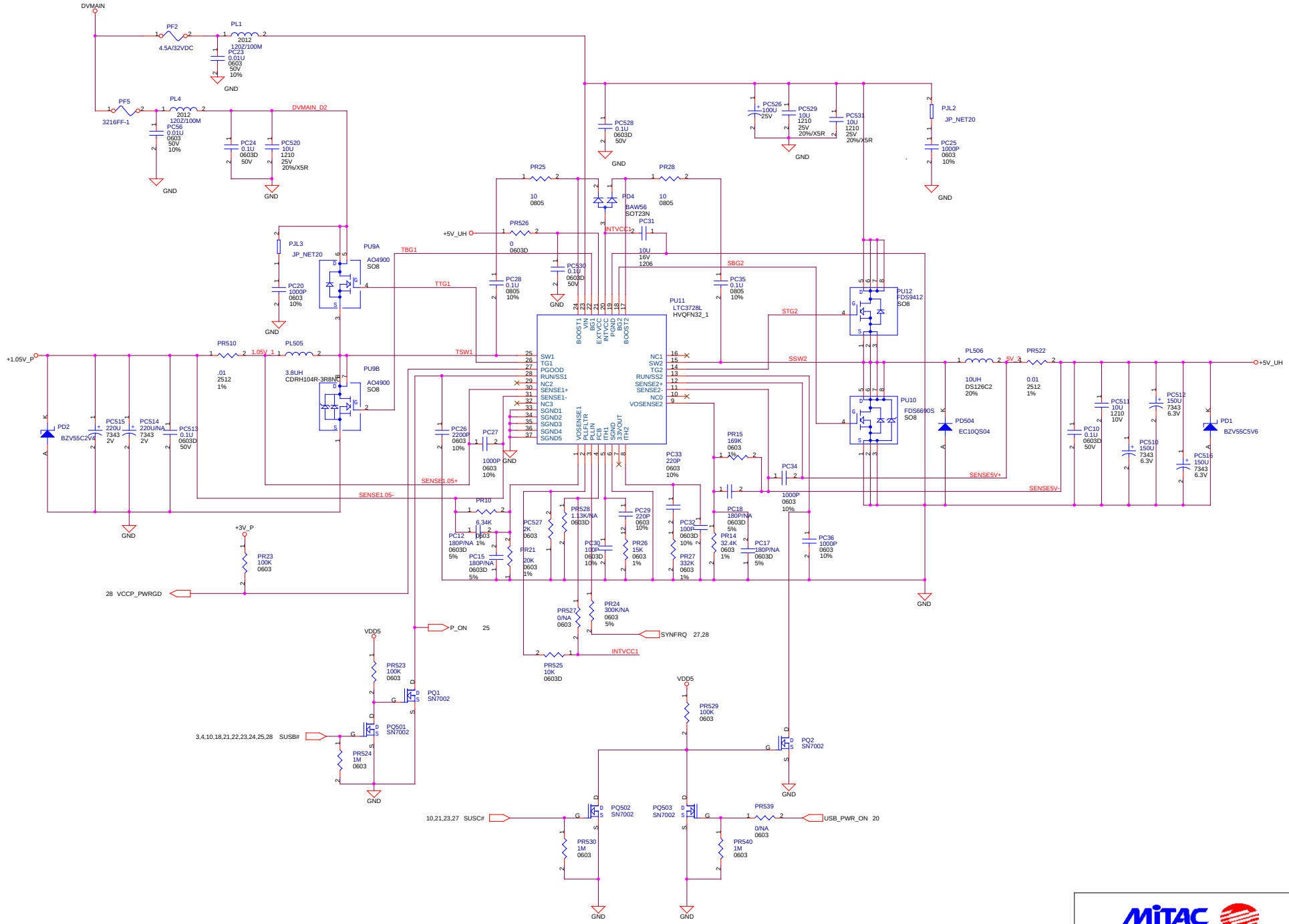
MiTAC

Title	1.2V & 1.5V(SC338) & 1.8V	
Size C	Document Number 41167******	Rev 01
Date: Wednesday, June 11, 2003	Sheet 24 of 28	



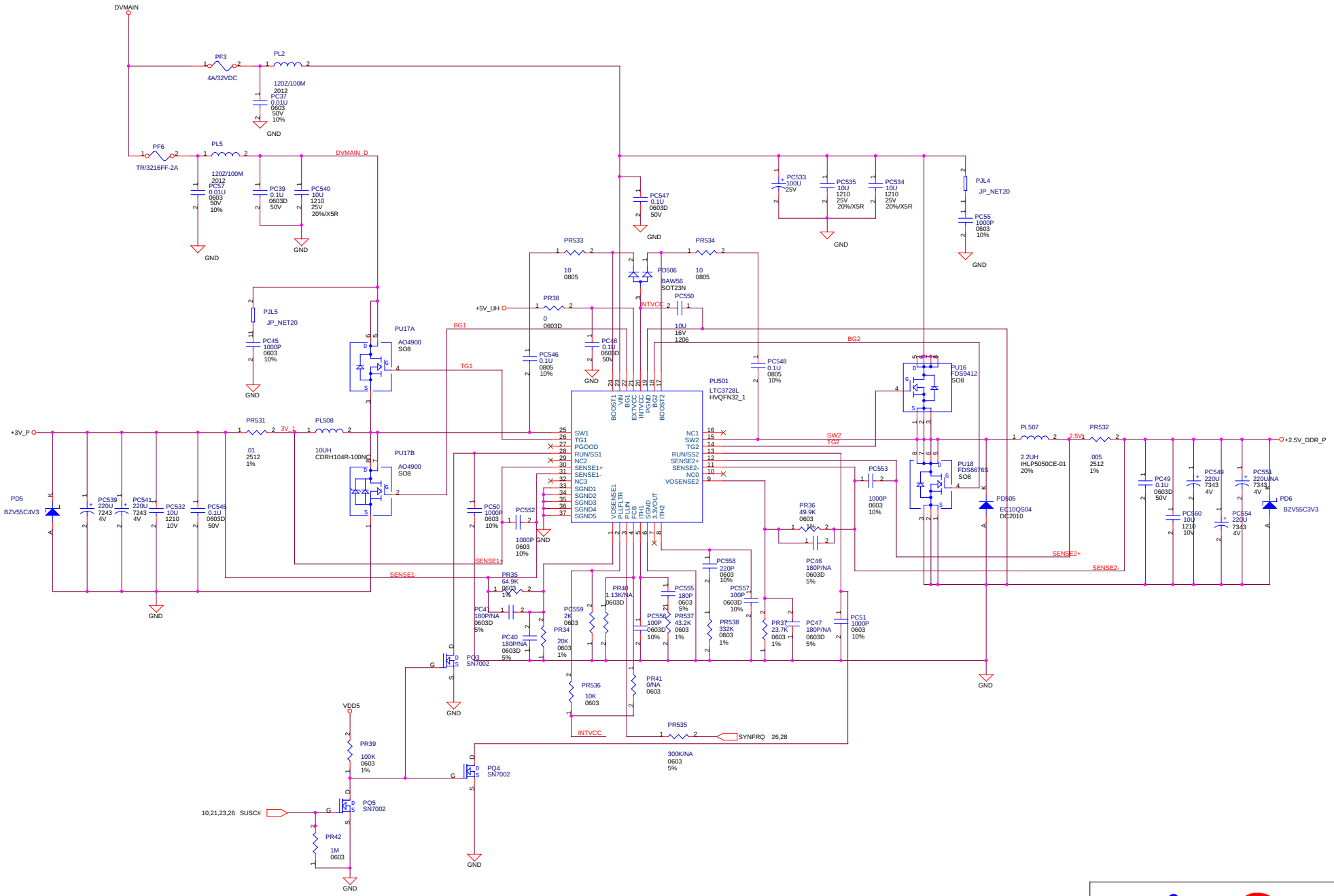
MiTAC

Title	1.25V (LP2996)	
Size C	Document Number 41167*******	Rev 01
Date: Wednesday, June 11, 2003	Sheet 25 of 28	

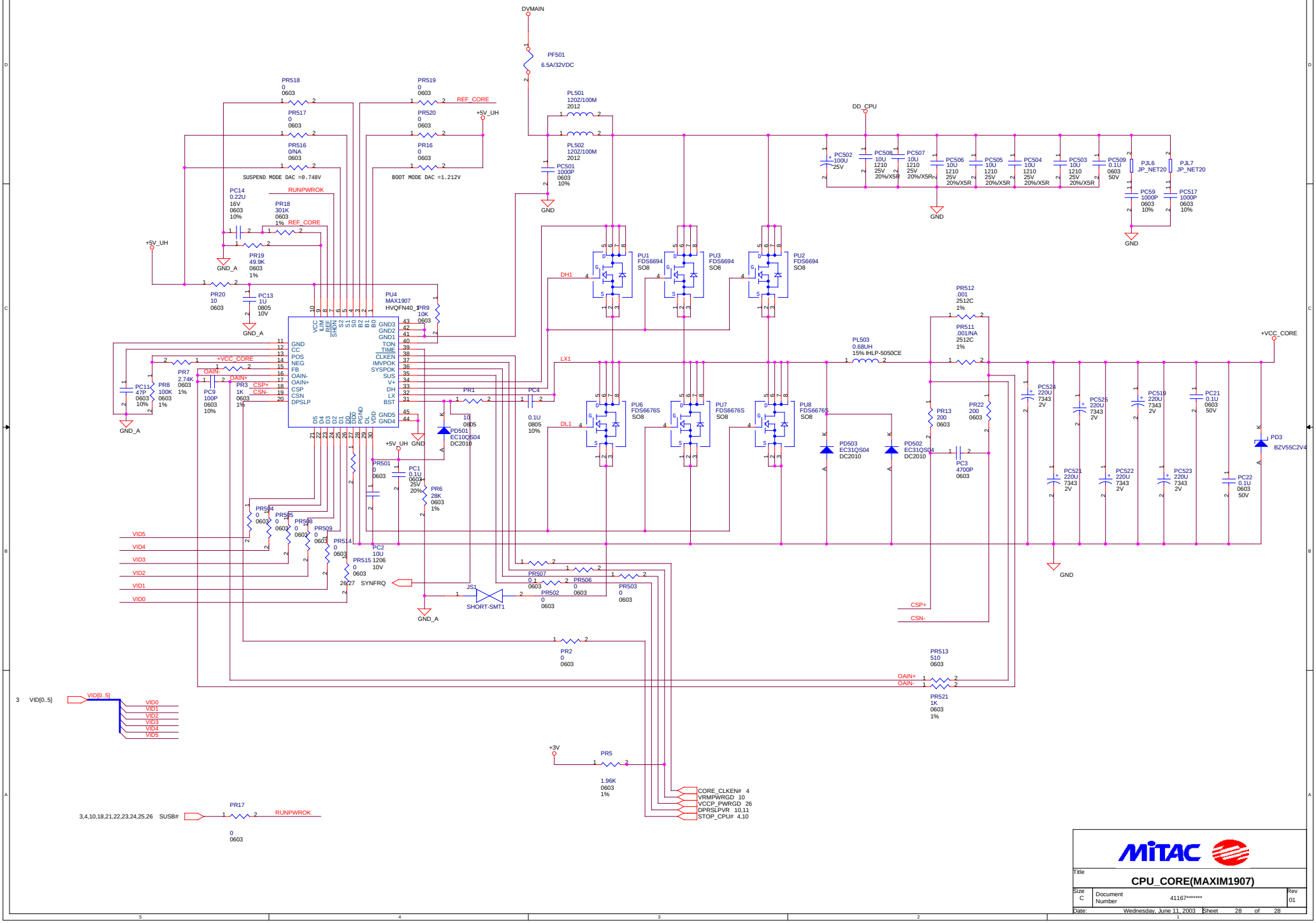


MiTAC

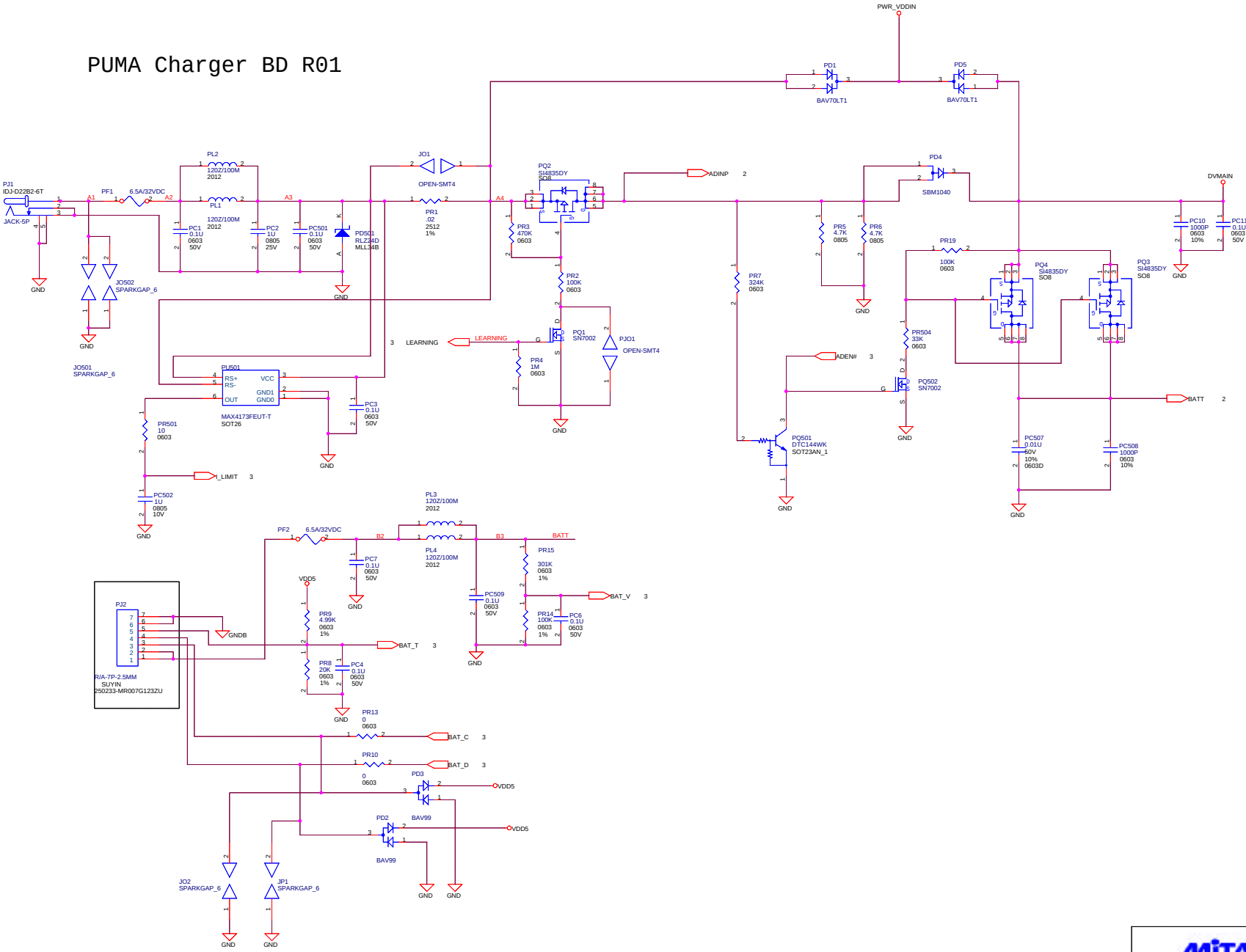
Title	5V & 1.05V(LTC3728L)	
Size C	Document Number 41167*******	Rev 01
Date: Wednesday, June 11, 2003	Sheet 26 of 28	



Title	3V & 2.5V(LTC3728L)	
Size C	Document Number 41167******	Rev 01
Date: Wednesday, June 11, 2003	Sheet 27 of 28	

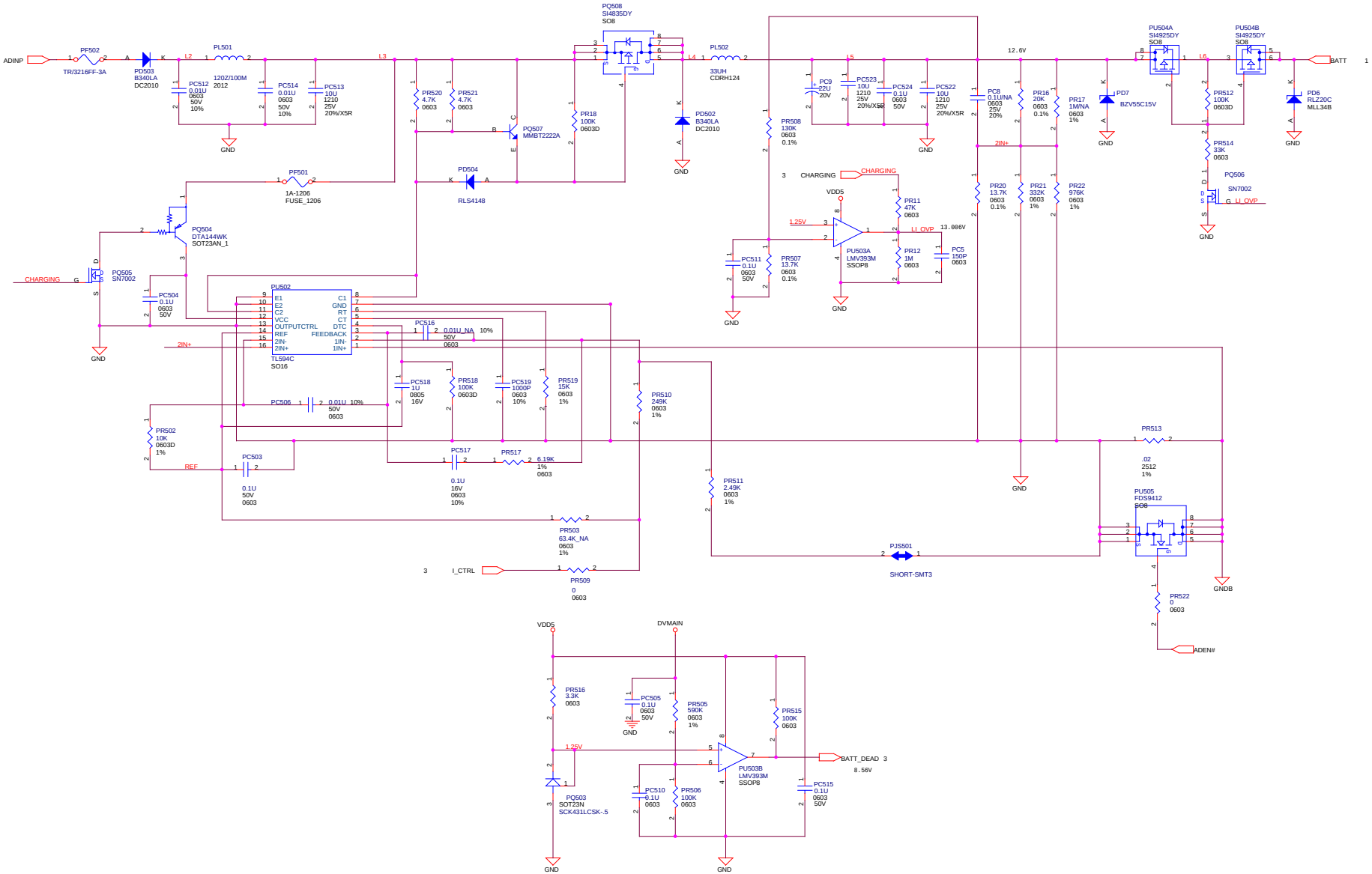

DVMAIN
PF501
6.5A/32VDC
PL501
120Z/100M
2012
PL502
120Z/100M
2012
PC501
1000P
0603
10%
GND
DD_CPU
PC502
100U
25V
PC508
10U
1210
25V
20%/X5R
PC507
10U
1210
25V
20%/X5R
PC506
10U
1210
25V
20%/X5R
PC505
10U
1210
25V
20%/X5R
PC504
10U
1210
25V
20%/X5R
PC503
10U
1210
25V
20%/X5R
PC509
0.1U
0603
50V
PJL6
JP_NET20
PJL7
JP_NET20
PC59
1000P
0603
10%
PC517
1000P
0603
10%
PR518
0
0603
PR519
0
0603
REF_CORE
PR517
0
0603
PR520
0
0603
+5V_UH
PR516
0/NA
0603
PR16
0
0603
SUSPEND MODE DAC =0.748V
BOOT MODE DAC =1.212V
PC14
0.22U
16V
0603
10%
RUNPWROK
PR18
301K
0603
1%
REF_CORE
+5V_UH
PR19
49.9K
0603
1%
GND_A
PR20
10
0603
PC13
1U
0805
10V
PU4
MAX1907
HVQFN40_1P
PR9
10K
0603
PU1
FDS6694
SO8
PU3
FDS6694
SO8
PU2
FDS6694
SO8
DH1
LX1
DL1
PR512
.001
2512C
1%
PR511
.001/NA
2512C
1%
PL503
0.68UH
15% IHLP-5050CE
+VCC_CORE
PR7
2.74K
0603
1%
PR8
100K
0603
1%
PC11
47P
0603
10%
PC9
100P
0603
10%
OAIN-
OAIN+
PR3
1K
0603
1%
CSP+
CSN-
PR1
10
0805
PC4
0.1U
0805
10%
PU6
FDS6676S
SO8
PU7
FDS6676S
SO8
PU8
FDS6676S
SO8
PD501
EC10QS04
DC2010
PD503
EC31QS04
DC2010
PD502
EC31QS04
DC2010
PR13
200
0603
PR22
200
0603
PC3
4700P
0603
PC528
220U
7343
2V
PC525
220U
7343
2V
PC519
220U
7343
2V
PC21
0.1U
0603
50V
PC521
220U
7343
2V
PC522
220U
7343
2V
PC523
220U
7343
2V
PC22
0.1U
0603
50V
PD3
BZV55C2V4
PR501
0
0603
PC1
0.1U
0603
25V
20%
PR6
28K
0603
1%
PC2
10U
1206
10V
PR504
0
0603
PR505
0
0603
PR508
0
0603
PR509
0
0603
PR514
0
0603
PR515
0
0603
26,27 SYNFRQ
PR507
0
0603
PR506
0
0603
PR503
0
0603
JS1
SHORT-SMT1
PR502
0
0603
GND_A
VID5
VID4
VID3
VID2
VID1
VID0
PR2
0
0603
PR513
510
0603
PR521
1K
0603
1%
3 VID[0..5]
VID[0..5]
+3V
PR5
1.96K
0603
1%
CORE_CLKEN# 4
VRMPWRGD 10
VCCP_PWRGD 26
DPRSLPVR 10,11
STOP_CPU# 4,10
3,4,10,18,21,22,23,24,25,26 SUSB#
PR17
0
0603
RUNPWROK
MiTAC
Title
CPU_CORE(MAXIM1907)
Size C
Document Number
41167*******
Rev 01
Date: Wednesday, June 11, 2003
Sheet 28 of 28

PUMA Charger BD R01

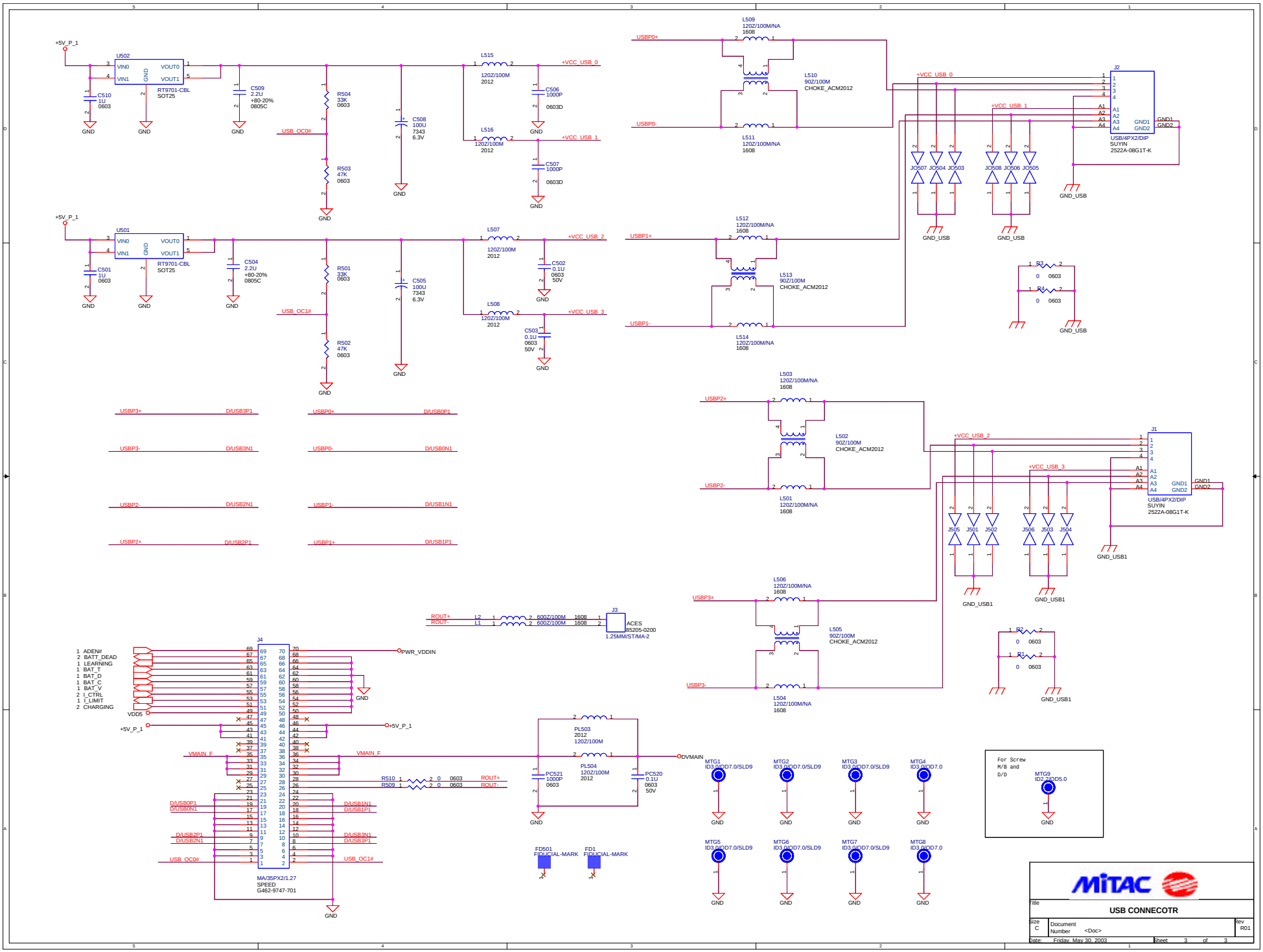


Title	ADINP & Discharge		
Size C	Document Number <Doc>		Rev R01
Date: Thursday, May 29, 2003		Sheet 1 of 3	

CHARGING



MiTAC		
Title	Charger	
Size C	Document Number <Doc>	Rev R01
Date: Friday, May 30, 2003	Sheet 2 of 3	


+5V_P_1
U502
VIN0
VIN1
VOUT0
VOUT1
GND
RT9701-CBL
SOT25
C510
1U
0603
C509
2.2U
+80-20%
0805C
R504
33K
0603
R503
47K
0603
C508
100U
7343
6.3V
USB_OC0#
L515
120Z/100M
2012
L516
120Z/100M
2012
C506
1000P
0603D
C507
1000P
0603D
+VCC_USB_0
+VCC_USB_1
U501
C501
1U
0603
C504
2.2U
+80-20%
0805C
R501
33K
0603
R502
47K
0603
C505
100U
7343
6.3V
USB_OC1#
L507
120Z/100M
2012
L508
120Z/100M
2012
C502
0.1U
0603
50V
C503
0.1U
0603
50V
+VCC_USB_2
+VCC_USB_3
USBP3+
USBP3-
USBP2-
USBP2+
USBP0+
USBP0-
USBP1-
USBP1+
D/USB3P1
D/USB3N1
D/USB2N1
D/USB2P1
D/USB0P1
D/USB0N1
D/USB1N1
D/USB1P1
L509
120Z/100M/NA
1608
L510
90Z/100M
CHOKE_ACM2012
L511
120Z/100M/NA
1608
L512
120Z/100M/NA
1608
L513
90Z/100M
CHOKE_ACM2012
L514
120Z/100M/NA
1608
L503
120Z/100M/NA
1608
L502
90Z/100M
CHOKE_ACM2012
L501
120Z/100M/NA
1608
L506
120Z/100M/NA
1608
L505
90Z/100M
CHOKE_ACM2012
L504
120Z/100M/NA
1608
J2
J1
USB/4PX2/DIP
SUYIN
2522A-08G1T-K
GND_USB
GND_USB1
JO507
JO504
JO503
JO508
JO506
JO505
J505
J501
J502
J506
J503
J504
R3
R4
R2
R1
0
0603
ROUT+
ROUT-
L2
L1
600Z/100M
1608
J3
ACES
85205-0200
1.25MM/ST/MA-2
J4
1 ADEN#
2 BATT_DEAD
1 LEARNING
1 BAT_T
1 BAT_D
1 BAT_C
1 BAT_V
2 I_CTRL
1 I_LIMIT
2 CHARGING
VDD5
PWR_VDDIN
VMAIN_F
R510
R509
PL503
2012
120Z/100M
PL504
120Z/100M
2012
PC521
1000P
0603
PC520
0.1U
0603
50V
DVMAIN
MA/35PX2/1.27
SPEED
G462-9747-701
FD501
FIDUCIAL-MARK
FD1
FIDUCIAL-MARK
MTG1
MTG2
MTG3
MTG4
MTG5
MTG6
MTG7
MTG8
ID3.0/OD7.0/SLD9
ID3.0/OD7.0
MTG9
ID2.2/OD5.0
For Screw
M/B and
D/D
MiTAC
Title
USB CONNECOTR
Size
C
Document
Number
<Doc>
Rev
R01
Date:
Friday, May 30, 2003
Sheet
3
of
3

Reference Material

❖ Intel Banias Pentium M Processor	Intel, INC
❖ Intel 82855GM Memory Controller Hub (GMCH)	Intel, INC
❖ Intel 82801DBM I/O Controller Hub Mobile (ICH4-M)	Intel, INC
❖ 8081 Hardware Engineering Specification	*Technology Corp.*/MiTAC

SERVICE MANUAL FOR 8081

Sponsoring Editor : Jesse Jan

Author : Sissel Diao

Assistant Editor : Janne Liu

Publisher : MiTAC International Corp.

Address : 1, R&D Road 2, Hsinchu Science-Based Industrial, Hsinchu, Taiwan, R.O.C.

Tel : 886-3-5779250 Fax : 886-3-5781245

First Edition : July. 2003

E-mail : Willy.Chen @ mic.com.tw

Web : http: //www.mitac.com http: //www.mitacservice.com