SERVICE MANUAL FOR

8599

BY: Star Meng

Repair Technology Research Department /EDVD

Jun.2004

MiTAC

8599 N/B Maintenance

Contents

1. Hardware Engineering Specification 4

1.1 Introduction 4
1.2 Hardware System 7
1.3 Electrical Characteristic 37
1.4 Appendix 1 : SiS963L GPIO Definition 42
1.5 Appendix 2 : Keyboard Controller Pins Definition 43
1.6 Appendix 3: Audio Performance 45

2. System View and Disassembly 46

2.1 System View 46
2.2 System Disassembly 49

3. Definition & Location of Connectors / Switches 69

3.1 Mother Board 69

4. Definition & Location of Major Components 72

4.1 Mother Board 72

5. Pin Description of Major Component 73

5.1 Inter Pentium 4 Processor mFC-PGA 478 Pins 73
5.2 SiS M661FX (IGUI Host Memory Controller) 78
5.3 SiS963L (MuTIOL®Media I/O South Bridge) 83

8599 N/B Maintenance

Contents

6. System Block Diagram 89

7. Maintenance Diagnostics 90

7.1 Introduction 90
7.2 Error Codes 91
7.3 Debug Tool 93

8. Trouble Shooting 94

8.1 No Power 96
8.2 Battery Can not Be Charged 99
8.3 No Display 101
8.4 LCD No Display or Picture Abnormal 105
8.5 External Monitor No Display or Color Abnormal 107
8.6 TV Test Error 109
8.7 Memory Test Error 111
8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error 113
8.9 Hard Driver Test Error 115
8.10 CD-ROM Driver Test Error 117
8.11 USB Port Test Error 119
8.12 PC Card Socket Test Error 123
8.13 Mini-PCI Socket Test Error 125
8.14 Audio Failure 127

Contents

8.15 LAN Test Error 130

9. Spare Parts List **132**

10. System Exploded Views **143**

11. Circuit Diagram **144**

12. Reference Material **172**

8599 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineer specification for 8599 portable notebook computer system.The 8599 notebook computer is a new mainstream high performance easy assembly notebook in the MiTAC notebook family.

1.1.2 System Overview (1)

Table 1. Hardware Specification

CPU	- Intel DT NW P4 2.4G,2.5G,2.53G,2.6G,2.66G,2.8G,3.06Ghz(p) w/z HT - Intel DT NW Celeron 2.0G~2.8G w/z - Intel DT Prescott Celeron 2.4G,2.53G,2.66G,2.8G,3.06G,3.2G w/z - Intel Northwood Mobile P4 2.40G,2.66G,2.80G,3.06G - Thermal ceiling 81.8W	- FSB 800/533 MHz - FSB 400MHz - FSB 533MHz
Core logic	- SiS M661FX + SiS963L	
L2 Cache	- 512KB OD for N/W DT & Mobile P4,128KB for N/W Celeron,256KB for Prescott Celeron	
System BIOS	-Insyde 256KB(P) Flash EPROM (Include System BIOS and VGA BIOS) -ACPI 1.0b;DMI 2.3.1 compliant -Plug & Play capability	

1.1.2 System Overview (2)

Continue to the previous page

Memory	- 0MB on board;Expandable up to 1024MB - Expandable with combination of optional 128MB/256MB/512MB memory - 184-pin DDR 266/333/400 DROM Memory Module x 2
ROM Drive	- 12.7mm Height - CD/DVD ROM Drive - Combo Drive - Super Combo Drive
HDD	- 2.5” 8.45/9.5 mm height:10/15/20/40GB - Support Ultra-DMA 66/100 function - User removable by latch,design reserve for screw fix
Ext.FDD	- Support External FDD w/z USB 1/F; 3.5” Format for 720KB/1.2MB/1.44MB
Display	- 15” XGA/TFT display; Resolution:1024x768
Video Controller	- SiS M661FX Int. w/64MB SMA
Keyboard	- 19mm key pitch/ 3.0mm key stroke/ 307mm length - Windows Logo Key x 1; Application Key x 1
Pointing Device	- Glide pad with 2x buttons and direction Scroll button
PCMCIA	- Type II x 1 without ZV - Cardbus Support
Indictor	- 3 LEDs for Power/battery/charge status (on display Housing/cover) - 1 LEDs for Radio wave status Power LED (BTO: Wireless LAN only) - 5 LEDs for HDD Access,ODD Access, Num lock, Cap lock and Scroll Lock

1.1.2 System Overview (3)

Continue to the previous page

Audio System	- Sound Blaster Pro compatible - Built-in mono microphone - AC97 2.2 Codec - 2X 2W Speakers
I/O Port	- USB port (2.0, backward compatible with USB 1.1) x 6 - RJ-11 port x 1 - RJ-45 port x 1 - DC input x 1 - VGA monitor port x 1 - Audio-out x 1 - Mic-in x 1 - S-Video TV-Out x 1 (NTSC/PAL)
Communication	- Built-in 56Kbps V.90 modem - Built-in 10/100 based-T LAN - One Mini-PCI slot and antenna reserved for wireless LAN
Battery	- 8 cell (2000mAH/3.7V) Li-ION smart battery
AC adapter	- Universal AC adapter 90W(P); Input: 100-240V,50/60hZ AC (support power on charge)
Dimensions	- 332x285x42 (max) (P)
Weight	- 3.5kg (P)

1.2 Hardware System

1.2.1 CPU Module

The Intel®Northwood DT Pentium®4 processor, Intel's most advanced, most powerful processor, is based on the new Intel®NetBurst™micro-architecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end users can truly appreciate and experience the performance. These applications include Internet audio and streaming video,image processing, video content creation, speech, 3D, CAD, games, multi-media, and multi-tasking user environments. The Intel Northwood DT Pentium 4processor delivers this world-class performance for consumer enthusiast and business professional DT users as well as for entry-level workstation users.

Highlights of the Northwood DT Pentium 4 Processor:

- Available at speeds ranging from2.26G/2.4G/2.5G/ 2.53G/2.66G/2.8G/3.06G Hz
- Featuring the new Intel NetBurst™micro-architecture
- Fully compatible with existing Intel Architecture-based software
- Internet Streaming SIMD Extensions 2
- Intel®MMX™media enhancement technology
- Memory cache ability up to 4 GB of addressable memory space and system memory scalability up to 64GB of physical memory
- Support for uni-processor designs
- Based upon Intel's 0.13 micron manufacturing process

8599 N/B Maintenance

Intel Pentium 4 Processor Product Feature:

The Intel NetBurst™micro-architecture delivers a number of new and innovative features including Hyper Pipelined Technology, 400 or 533 MHz System Bus, Execution Trace Cache, and Rapid Execution Engine as well as a number of enhanced features Advanced Transfer Cache, Advanced Dynamic Execution, Enhanced Floating-point and Multi-media Unit, and Streaming SIMD Extensions 2. Many of these new innovations and advances were made possible with improvements in processor technology, process technology, and circuit design that could not previously be implemented in high-volume, manufacturability solutions. The features and resulting benefits of the new micro-architecture are defined below.

- **Hyper Pipelined Technology**

  The hyper-pipelined technology of the NetBurst™micro-architecture doubles the pipeline depth compared to theP6 micro-architecture used on today's Pentium III processors. One of the key pipelines, the branch prediction / recovery pipeline, is implemented in 20 stages in the NetBurst™micro-architecture, compared to 10 stages in the P6 micro-architecture. This technology significantly increases the performance, frequency, and scalability of the processor.

- **400/533 MHz System Bus:**

  The Northwood DT Pentium 4 processor supports Intel's highest performance desktop system bus by delivering 3.2 or 4.3GBof data per second into and out of the processor. This is accomplished through a physical signaling scheme of quad pumping the data transfers over a100/133-MHz clocked system bus and a buffering scheme allowing for sustained 400/533-MHz data transfers. This compares to 1.06 GB/s delivered on the Pentium III processor's 133-MHz system bus.

8599 N/B Maintenance

- **Level 1 Execution Trace Cache:**

  In addition to the 8KB data cache, the Pentium 4 processor includes an Execution Trace Cache that stores up to12K decoded micro-ops in the order of program execution. This increases performance by removing the decoder from the main execution loop and makes more efficient usage of the cache storage space since instructions that are branched around are not stored. The result is a means to deliver a high volume of instructions to the processor's execution units and a reduction in the overall time required to recover from branches that have been mis-predicted.

- **Rapid Execution Engine:**

  Two Arithmetic Logic Units (ALUs) on the Pentium 4 processor are clocked at twice the core processor frequency. This allows basic integer instructions such as Add, Subtract, Logical AND,Logical OR, etc. to execute in half a clock cycle. For example, the Rapid Execution Engine on a 1.50 GHz Pentium 4 processor runs at 3 GHz.

- **512KB, Level 2 Advanced Transfer Cache:**

  The Level 2 Advanced Transfer Cache (ATC) is 512KB in size and delivers a much higher data throughput channel between the Level 2 cache and the processor core. The Advanced Transfer Cache consists of a 256-bit(32-byte) interface that transfers data on each core clock. As a result,the Northwood DT Pentium 4 processor 1.6 GHz can deliver a data transfer rate of 48 GB/s.This compares to a transfer rate of 16 GB/s on the Pentium III processor at 1 GHz. Features of the ATC include:

  - Non-Blocking, full speed, on-die Level 2 cache
  - 8-way set associativity

- 256-bit data bus to the level 2 cache
- Data clocked into and out of the cache every clock cycle

- **Advanced Dynamic Execution:**

The Advanced Dynamic Execution engine is a very deep, out-of-order speculative execution engine that keeps the execution units executing instructions. The Pentium 4 processor can also view 126 instructions in flight and handle up to 48 loads and 24 stores in the pipeline. It also includes an enhanced branch prediction algorithm that has the net effect of reducing the number of branch mis-predictions by about 33% over the P6 generation processor's branch prediction capability. It does this by implementing a 4KB branch target buffer that stores more detail on the history of past branches, as well as by implementing a more advanced branch prediction algorithm.

- **Enhanced Floating-Point and Multimedia Unit:**

The Pentium 4 processor expands the floating-point registers to a full 128-bit and adds an additional register for data movement which improves performance on both floating-point and multimedia applications..

- **Internet Streaming SIMD Extensions 2 (SSE2):**

With the introduction of SSE2, the NetBurst™micro-architecture now extends the SIMD capabilities that MMX technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase. They accelerate a broad range of applications, including video, speech,and image, photo processing, encryption, financial,engineering and scientific applications.

- **Features Used for Test and Performance / Thermal Monitoring:**

  - Built-in Self Test (BIST) provides single stuck-at fault coverage of the microcode and large logic arrays, as well as testing of the instruction cache, data cache, Translation Look aside Buffers (TLBs), and ROMs.
  - IEEE 1149.1 Standard Test Access Port and Boundary Scan mechanism enables testing of the Pentium 4 processor and system connections through a standard interface.
  - Internal performance counters can be used for performance monitoring and event counting.
  - Includes a new Thermal Monitor feature that allows motherboards to be cost effectively designed to expected application power usages rather than theoretical maximums.

1.2.2 SiS M661FX Graphics/Memory Controller

The SiSM661FX chipset features a SiS Real256E GPU, an AGP-8X port, and a Shared Memory Architecture DDR400 unified memory controller, supporting Intel Hyper Threading Technology Pentium 4 microprocessors series with FSB 800MHZ. The integrated Real256E GPU features a high performance 3D / 2D Graphics engine, a video accelerator, a MPEG1/II motion compensation decoder, and a video link(Muxed with AGP port) to support the TV-out & digital flat panel. The SiSM661FX, adopting the SMA, eliminates the need and thus the cost of the frame buffer memory by organizing the frame buffer,32MB or 64MB, in the system memory. The SiSM661FX, via the second-generation 1GB/s Multi-threaded I/O link, interconnects the SiS963 Media I/O that integrates one EHCI compliant USB2.0 host controller, 2 OHCI compliant USB 1.1 host controllers, dual ATA-133 IDE controllers, AC-97 V2.2 compliant audio controller, and the 10/100M bit Ethernet MAC controller with standard MII interface. Figure 1 illustrates a Pentium 4 PC system diagrams based on SiSM661FX and SiS963 chipsets.

8599 N/B Maintenance

The SiSM661FX Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Pentium 4 series processors with FSB 800MHz. The AGP interface supports the external AGP slot with AGP 4X/8X capability and Fast Write Transactions. The SiSM661FX incorporates the second generation 1GB/s MuTIOL1G interface, comprising the transaction layer, link layer, and physical layer, to bridge the SiS963 Media I/O. As seen in table 1, the SiSM661FX comprises two PCI devices sitting on the bus 0, and one PCI device on the Bus 1.The device 0 stands for the SiSM661FX entity with device ID 0661h, and IDSEL equal to AD11. The device 1 functions a virtual PCI to PCI bridge to connect the AGP device, with device ID equal to 0002h, and IDSEL equal to AD12. The device 0 in the bus 1 represents the integrated Real256E GPU, with device ID equal to 6330h. The integrated GUI device 6330h cannot work concurrently with an external AGP graphics device. When an external AGP device is installed in the system, the built-in GUI will be disabled. Figure 2 illustrates a graphic subsystem based on the integrated GUI in SiSM661FX.

The integrated Real256E GPU features a high performance 3D accelerator with 2 Pixel / 4 Texture, and a 128 bit 2D accelerator with 1T pipeline BITBLT engine. Two 12 bit DDR digital video links interfaced to SiS 301/2 Video Bridge is incorporated to expand the SiSM661FX functionality to support the secondary display, in addition to the default primary CRT display. The SiS301 Video Bridge features an NTSC/PAL video encoder with Macro Vision Ver. 7.1.L1 option for TV display, a TMDS transmitter with Bi-linear scaling capability to support up to UXGA TFT LCD panel, and an analog RGB port to support the secondary CRT. The primary CRT display and the extended secondary display, namely TV, TFT LCD, or 2'nd CRT, features the Dual Display Capability in the sense that both can generate the display in independent resolutions, color depths, and frame rates. Table 2 details the capability of the video overlay capability in SiSM661FX+SiS301/302 subsystem. In a summary, in the mirror mode, two separate H/W video overlay engines, and two separate subpicture engines work simultaneously to deliver high quality video overlay with subpicture in the respective display consoles simultaneously, say in the LCD, and CRT for the presentation application. However, in the dual display mode, only one H/W video overlay, and one subpicture engine can be enabled to overlay the video display and the subpicture in one display while the support of the second video overlay with subpicture in.

the second display can only be realized through software engine.

Two separate buses, the 64 bit Host-to-GUI bus, and the 128 bit IGUI-to-Memory Controller bus are devised to ensure concurrency of Host-to-GUI, and GUI-to-MC streaming. In the DDR-400 memory subsystem, the 128 bit IGUI-to-MC bus attains 3.2 GB/s, around 52% wider bandwidth than the AGP 8X one. The DDR-400 unified memory controller mainly comprises the Memory Arbiter, the M-data/M-Command Queues, and the Memory Interface. The Memory Arbiter arbitrates a plenty of memory access requests from the GUI or AGP controller, Host Controller, and the I/O bus masters based a default optimized priority list with the capability of dynamically prioritizing the I/O bus master requests to offer a privileged service to 1) the isochronous downstream transfer to guarantee the min. latency, & timely deliver, or 2) the PCI master downstream transfer to curb the latency within the max. tolerant period of 10us. Prior to the memory access requests pushed into the M-data queue, any command complaint to the paging mechanism is generated and pushed into the M-CMD queue. The M-data/M-CMD queue further orders and forwards these queuing requests to the Memory Interface in an effort to utilizing the memory bandwidth to its utmost by scheduling the command requests in the background when the data request streamlines in the foreground.

Features :

- **PC2001 Compliance**
- **High Performance Host Interface**

  - Supports Intel Pentium 4 processor family with data transfer rate
  - Supports Hyper-Threading Technology
  - Supports 12 outstanding transactions and out-of-order completion
  - Supports Quasi-synchronous/asynchronous Host-to-DRAM timing
  - Supports Master delivery System bus Interrupt

- Supports zero-wait state for contiguous CPU write data
- Supports 128K/256K/512K/1M/2M/4M/8M/16M TSEG SMRAM
- Supports Defer Function to maximize bus utilization
- Supports Dynamic Bus Inversion
- AGTL+ & AGTL compliant bus driver with auto compensation

- **64 Bit High Performance DDR400/DDR333/DDR266 Memory Controller**

- Supports DDR400/DDR333/DDR266 SDRAM
- Supports up to 2 un-buffered DIMM DDR400
- Supports up to 3 un-buffered DIMM DDR333
- Up to 1 GB per DIMM with maximum memory size up to 3 GB
- Supports 32Mb, 64Mb, 128Mb, 256Mb, 512Mb, 1Gb SDRAM technology with page size from 2KB up to 32 KB
- Supports up to 24 open pages
- Sustains DDR SDRAM CAS Latency at options of 2, 2.5, & 3 clocks
- Auto-compensation SSTL-2.5v driver optimizing for performance and stability
- Supports Suspend to DRAM function
- Programmable shared frame buffer size 32MB or 64MB for display memory
- 128KB SMRAM space re-mapping to A0000h, B0000h, or E0000h

- **Integrated A.G.P. Compliant Target/66MHz Host-to-PCI Bridge**

- Universal AGP v3.0 Compliant
- Support 1.5V AGP Interface Only

8599 N/B Maintenance

- Supports Graphic Window Size from 4MBytes to 512MBytes
- Supports Pipelined Process in CPU-to-A.G.P. Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance A.G.P. Controller Read/Write Performance
- Supports PCI-to-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to A.G.P. device
- Supports AGP 8X/4X Interface w/ Fast Write Transaction
- Supports Hardware Enforced Coherence Outside GART Range for A.G.P. Transaction
- Supports Data Bus Inversion and Calibration Cycle

- **High Throughput SiS MuTIOL® 1G Interconnecting to SiS963 MuTIOL 1G Media I/O**

  - Bi-directional 16 bit data bus
  - Perform 1GB/s bandwidth in 133MHz x 4 mode
  - Distributed arbitration strategy with long contiguous data streaming
  - Packet based, pipelining, and split transaction scheme

- **Dedicated Isochronous Response Queue**

  - Priority promotion for upstream Isochronous DMA memory read requests originated from real-time I/O device controllers, such as USB or audio/modem
  - Dedicated Isochronous response queue serving Isochronous downstream transfers responsive to the memory read requests originated from real-time I/O device controllers, such as USB or audio/modem. Offers privilege service to guarantee minimum latency & timely delivery

- **High Performance & High Quality 3D Graphics Accelerator**

  - Built-in a high performance 256-bit 3D engine

8599 N/B Maintenance

-- Built-in 32-bit floating point format VLIW triangle setup engine

-- Built-in 2 pixel rendering pipelines and 4 texture units

-- Built-in hardware stereo auto rendering engine

-- Supports Ultra-AGPIITM up to 2.7GB/s bandwidth

-- Up to 133 MHz 3D engine clock speed

-- Peak polygon rate: 11.6 M polygon/sec @ 1 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping

-- Peak fill rate: 333 M pixel/sec, 666 M texture/sec @ 10,000 pixel/polygon with Gouraud shaded and two bilinear textured, Z buffered and alpha blended

- Built-in a high quality 3D engine

-- Supports flat, and Gouraud shading

-- Supports high quality dithering

-- Supports Z-test, stencil test, Alpha-test, and scissors clipping test

-- Supports 16 ROPs

-- Supports Z-buffer, stencil buffer

-- Supports 16/24/32 bits integer Z buffer format and 32 bits floating point Z format

-- Supports 16/32 BPP render buffer format

-- Supports 1/2/4/8 stencil buffer format

-- Supports per-pixel texture perspective correction

-- Supports point-sampled, linear, bi-linear, and dual bi-linear texture filtering

-- Supports up to 2 pixels with 4 bi-linear texels within single cycles

-- Supports up to 2048x2048 texture size

-- Supports rectangle structure texture

-- Supports 16/24/32 bpp RGB/ARGB texture format
-- Supports DTX1, DTX2, DTX3 texture compression formats
-- Supports texture transparency, blending, wrapping, mirror, and clamping
-- Supports fogging, alpha blending
-- Supports vertex fogging and fog table
-- Supports specular lighting
-- Supports 2X/4X multi-sampling full scene anti-aliasing
-- Supports back face culling
-- Supports auto-stereo rendering

- **High Performance 2D Graphics Accelerator**

- Built-in hardware command queue
- Built-in Direct Draw Accelerator
- Built-in GDI 2000 Accelerator
- Built-in an 1T pipelined 128-bit BITBLT graphics engine with the following functions:
  -- 256 raster operations
  -- Rectangle fill
  -- Trapezoid fill
  -- Color expansion
  -- Enhanced color expansion
  -- Line-drawing with styled pattern
  -- NT fractional point line-drawing with styled pattern
  -- Multiple scan line

-- Built-in 256 bytes pattern registers
-- Built-in 8x8 mask registers
-- Rectangle clipping
-- Transparent BitBlt with source and destination keys (16 ROPs)
-- Gradient color fill
-- Anti-aliasing text drawing
-- Alpha blended Bitblt
-- YUV to RGB color transform Bitblt
-- Source data in command queue Bitbl
-- YUV420 to YUV422 format conversion Bitblt

- Supports memory-mapped, zero wait-state, burst engine write
- Built-in 64x64x2 bit-mapped mono hardware cursor
- Built-in 64x64x16 bit-mapped blended color hardware cursor
- Maximum 128MB frame buffer with linear addressing
- Built-in engine write-buffer with byte-merge
- Supports Ultra-AGPIITM 2.7GB/s for DDR333 and 3.2GB/s for DDR400 data read for all 2D Graphics engine functions
- Built-in source read-buffer to minimize engine wait-state
- Built-in destination read-buffer to minimize engine wait-state

Complete TV-OUT/Digital Flat Panel Solution

- Built-in secondary CRT controller to support independent display of secondary CRT, LCD and TV-out

8599 N/B Maintenance

- AGP signals multiplexed with two 165MHz dot clock 12-bit DDR digital video link connecting to SiS video bridge (SiS301, and SiS302) supporting
  - -- NTSC/PAL video output with max. resolution 1024x768x32@60NI
  - -- Digital LCD monitor with max. resolution 1600x1200x32@60NI
  - -- The secondary CRT with max. resolution 1600x1200x32@60NI
  - -- The Independent dual view support of the CRT+LCD, CRT+TV, LCD+TV combinations.

- **MPG-2/1 Video Decoder**

- MPEG-2 ISO/IEC 13818-2 MP@HL and MPEG-1 ISO/IEC 11172-2 standards compliant
- Built-in advanced hardware DVD acceleration logic
- Support AGP bus master/LFB-mode code fetching
- Half pixel resolution in motion compensation
- Supports up to 20 Mbit/sec bit rate decoding
- Support VCD, DVD and HDTV (all ATSC modes) decoding
- Direct DVD to TV playback

- **Video Accelerator**

- Supports video windows with overlay function
- Supports YUV-to-RGB color space conversion
- Supports bi-linear video interpolation with integer increments of 1/2048
- Supports graphics and video overlay function
  - -- Independent graphics and video formats

-- 16 color-key and/or chroma-key operations
-- Support YUV or RGB format chroma key
-- Rectangular video window mode
-- Video only mode
-- VCD, DVD and up to HDTV playback mode
-- Supports reading-back of current refresh scan line

- Supports tearing free double buffer flipping
- Supports RGB555, RGB565, YUV422, and YUV420 video playback format
- Supports filtered horizontal up and down scaling playback
- Supports de-interlaced function to improve field-display sources display quality
- Supports DVD sub-picture playback overlay
- Supports DVD playback auto-flipping
- Built-in video playback line buffers to support 1920x1080 video playback
- Supports DVD sub-picture playback overlay
- Built-in video line buffers and sub-picture buffers for DVD quality video
- Built-in independent Gamma correction RAM
- Supports DCI Drivers
- Supports Direct Draw Drivers

- **High Integration**

- Built-in CRT FIFOs to support ultra high resolution graphics modes and reduce CPU wait-state
- Built-in programmable 24-bit true-color RAMDAC up to 333 MHz pixel clock

-- Built-in reference voltage generator and monitor sense circuit
-- Supports downloadable 24 bits RAMDAC for gamma correction in high color and true color modes
-- Support programmable 4 levels DAC current ratio (700, 750, 800, 850 mv)
-- Support programmable pedestal level (0, 0.75mv)
-- Support programmable 4 levels slew rate control

- Built-in two clock generators for CRT, 2D, 3D and MPEG Engine
- Built-in TV Encoder Interface

- **Power Management**

- Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management
- Supports direct I/O command to force graphics controller into standby/suspend/off state
- Power down internal Gamma/Palette SRAM in direct color mode
- Supports PCI power management configuration registers for supporting ACPI power down controller
- Power down all internal macro cells such as SRAM, DAC, clock generator when power saving mode
- Supports clock stopping for video accelerator, 2D, 3D and MPEG decoder when disabled
- Supports auto clock throttling for 2D engine, 3D engine

1.2.3 SiS963L MuTIOL 1G Media I/O

The SiS963L MuTIOL 1G Media I/O integrates one Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the Ethernet MAC Controller w/ standard MII interface, two Universal Serial Bus 1.1 Host Controllers, the IDE Master/Slave controllers, and SiS MuTIOL 1G technology. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The high-speed host controller implements an EHCI compliant interface that provides 480Mb/s bandwidth for six USB 2.0 ports. The two USB1.1 host controllers implement an OHCI compliant interface and each USB1.1 host controller provides 12Mb/s bandwidth for three USB 1.1 ports. The totally six USB ports can be automatically routed to support a High-speed USB 2.0 device or Full- or Low-speed USB 1.1 device. Besides, each port can be optionally configured as the wake-up source. Legacy USB devices as well as over current detection are also implemented. The Integrated AC97 v2.2 compliance Audio Controller that features a 6-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated Fast Ethernet MAC Controller features an IEEE 802.3 and IEEE 802.3x compliant MAC with external LAN physical layer chip supporting full duplex 10 Base-T, 100 Base-T Ethernet, or with external Home networking physical layer chip supporting 1Mb/s & 10Mb/s Home networking. Additionally, 5 wake-up Frames, Magic Packet and link status changed wake-up function in G1/G2 states are supported. For storing Mac address, two schemes are provided: 1. Store in internal APC register or 2. Store in external EEPROM.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode 0,1,2,3,4, and Ultra DMA 33/66/100/133. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

8599 N/B Maintenance

SiS963L supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 8237A compatible DMA controllers, three 8254 compatible programmable 16-bit counters, hardwired keyboard controller and PS2 mouse interface, Real Time clock with 512B CMOS SRAM and two 8259A compatible Interrupt controllers. Besides, the I/O APIC managing up to 24 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 25 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the SiS963L supports Deeper Sleep power state for Intel Mobile processor. For AMD processor, the SiS963L use the CPUSTP# signal to reduce processor voltage during C3 and S1 state.

A high bandwidth and mature SiS MuTIOL 1G technology is incorporated to connect SiS MuTIOL 1G North Bridge and SiS963L MuTIOL1G Media I/O together. SiS MuTIOL 1G technology is developed into three layers, the Multi-threaded I/O Channels Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Channels layer, the Multi-threaded I/O Packet Layer in SiS963L to transfer data w/ 1GB/s bandwidth from/to Multi-threaded I/O Channels layer to/from SiS MuTIOL 1G North Bridge, and the Multi-threaded I/O Packet Layer in SiS MuTIOL 1G North Bridge to transfer data w/ 1GB/s from/to memory sub-system to/from the Multi-threaded I/O Packet Layer in SiS963L.

8599 N/B Maintenance

Features :

- **Meet PC2001 Requirements**
- **Support AMD Hammer CPU and HyperTransport Technology.**
- **Support Watchdog Timer Hardware Requirements for Microsoft Windows .NET Server**
- **High performance SiS MuTIOL 1G Technology Interconnecting SiS North bridge and South bridge chips**
  - Bi-directional 16-bit data bus
  - Perform 1GB/s bandwidth in 133MHz x 4 mode
  - Distributed arbitration strategy with long contiguous data streaming
  - Packet based, pipelining, and split transaction scheme
- **Integrated Multi-threaded I/O link ensures concurrency of upstream/down stream data transfer with1.2GB/s bandwidth**
- **Multiple DMA Bus Architecture**
  - Concurrent Servicing of all DMA Devices: Dual IDE Controllers, two USB 1.1 HC, One USB 2.0 HC, MAC Controller, Audio/Modem DMA Controller
  - Separate 32 Bit Input and Output Data Bus Scheme for each DMA Device
  - Advanced Performance Merits of Split & Pipelined Transaction and Concurrent
  - Execution among Multi-I/O Devices
  - Support isochronous request and continuous packet transmission

8599 N/B Maintenance

- **Integrated MuTIOL 1G to PCI Bridge**

  - PCI 2.2 Specification Compliance
  - Supports up to 6 PCI Masters
  - Two Prefetch cache Buffers support 2 delayed transactions
  - Each PCI request can be programmed at one of four level priority
  - Write Promotion Mechanism to Guarantee the 10 µs Time Limit of PCI Memory Write

- **Dual IDE Master/Slave Controller**

  - Integrated Multithreaded I/O Link Mastering with Read Pipelined Streaming
  - Dual Independent IDE Channels Each with 32 DW FIFO
  - Native and Compatibility Mode
  - PIO Mode 0, 1, 2, 3, 4 and Multiword DMA Mode 0, 1, 2
  - Ultra DMA 33/66/100/133
  - ATA/ATAPI 48-bit addressing compliance and support greater than 137Gbytes device.
  - Silicon Integrated Series Termination Resistors
  - Silicon Integrated IDE Bus pull up / down resistors
  - PCI 2.2 Specification Compliance
  - Bus master programming interface (SFF-8038i) specification compliance

- **Universal Serial Bus Host Controller**

  - Integrated Multithreaded IO Link Mastering
  - Two Independent OHCI USB 1.1 Host Controllers and One EHCI USB 2.0 Host Controller, support up to six ports

- Supports wake-up from S1-S3
- Legacy Keyboard/Mouse support
- Supports only one Debug port at port 0(first port), it is at USB 2.0 transfer rate.

- **Integrated Fast Ethernet MAC Controller**

- Multithread I/O link Mastering with Read/Write Concurrent transaction
- IEEE 802.3 and 802.3x Standard Compatible
- Supports Enhanced Software and Automatic Polling schemes to access PHY registers
- Supports full duplex 10base-T, 100base-Tx, 1 Mb/s & 10 Mb/s Home Networking
- Support ACPI v1.0b and PCI Power Management v1.1 Standard
- Support 5 Wake-up Frame, Magic Packet, and Link Status changed wake-up function at G1/G2 state
- Integrated 128-bit multicast hash table
- Support 2K bytes transmit and receive Data FIFO
- MAC address store scheme from external 4-pin EEPROM or Internal APC register

- **Integrated Audio Controller with AC97 Interface.**

- AC97 v2.2 compliance
- 6 Channels of AC97 speaker outputs and V.90 HSP-Modem
- 4 Separate SDATAIN pins supporting multiple Audio Codecs and one Modem Codec
- Supports Audio and Modem function with Multithreaded I/O link mastering
- Supports two Consumer Audio Digital interface: traditional Consumer Digital Audio Out and AC97 V2.2 Compliance Consumer Audio Digital Interface

- Supports VRA Mode for both AC97 Audio Link and Consumer Audio Digital Interface

- **Advanced Power Management**

  - Meets ACPI 1.0b Requirements
  - Meets APM 1.2 Requirements
  - ACPI Sleep States Include S1, S3, S4, S5
  - CPU Power States Include C0, C1, C2 C3, C4
  - Supports Intel Deeper Sleep Power State for Intel mobile processor.
  - Reduce AMD processor voltage during S1/C3 state
  - Power Button with Override only wake up by Power Button
  - RTC Day-of-Month, Month-of-Year Alarm
  - 24-bit Power Management Timer
  - LED Blinking in S0, S1 and S3 States
  - ACPI System Wake-up Events
  - ACPI S1 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-key and Mouse, RTC Alarm, Modem, Ring-In, LAN, PME#, AC'97 Wake-Up, USB Wake-Up, and 1394 Wake-up
  - ACPI S3 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-key and Mouse, RTC Alarm, Modem, Ring-In, GPIO7, LAN, PME#, AC'97 Wake-Up, USB Wake-Up, and 1394 Wake-up.
  - ACPI S4/S5 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-Key and Mouse, RTC Alarm, Modem, Ring-In, GPIO7, LAN, PME#, AC'97 Wake-Up, and P1394 Wake-up.
  - Software Watchdog Timer
  - PCI Bus Power Management Interface Spec. 1.1

8599 N/B Maintenance

- Support PCI CLKRUN and STP_PCI function (for Mobile only)
- Support RTC32KHz output from GPIO18 (for Mobile only)
- Integrated 32-bit Random Number Generator
- Support one GTL-level input signal used to instantly power off the system
- Support one GTL-level input signal used to assert SMI#/SCI#

- **Integrated DMA Controller**
  - Two 8237A Compatible DMA Controllers
  - 8/16- bit DMA Data Transfer

- **Integrated Interrupt Controller**
  - Two 8259A Compatible Interrupt Controllers for up to 15 interrupts
  - Programmable Level or Edge Triggered Interrupts
  - Support Serial Interrupt
  - Support 8 PCI interrupts for internal device
  - Support Message Interrupt Delivery Mode
  - Integrated I/O APIC in Serial Mode or FSB Interrupt Delivery Model for up to 24 Interrupts

- **Three 8254 Compatible Programmable 16-bit Counters**
  - System Timer Interrupt
  - Generate Refresh Request
  - Speaker Tone Output

8599 N/B Maintenance

- **Integrated Keyboard Controller**
  - Hardwired Logic Provides Instant Response
  - Supports PS/2 Mouse Interface
  - System Sleep and Power-Up by Hot-Key
  - KBC and PS2 Mouse Can Be Individually Disabled
- **Integrated High-Performance Event Timer**
  - Support three timers operating at 32- or 64-bit mode
- **Integrated PCI to LPC Bridge**
  - LPC 1.0 Compliance
  - Support Two Master/DMA devices
- **Integrated Real Time Clock (RTC) with 512B CMOS SRAM**
  - Supports ACPI Day-of-Month and Month-of-Year Alarm
- **Universal Serial Bus Host Controller**
- **NAND Tree for Ball Connectivity Testing**
- **371-Balls BGA Package**
- **1.8V Core with Mixed 1.5V, 1.8V, 2.65V and 3.3V I/O CMOS Technology**

1.2.4 Memory

- 64MB 400/33/266MHz DIMM DDR Memory expandable to 1024 MB (2 DDR slot)
- Support 184pin DDR DIMM Memory

Table 2. Memory Expansion Capacity

Slot1	Slot2	Slot3
256MB	0MB	256MB
256MB	256MB	512MB
512MB	0MB	512MB
512MB	256MB	768MB
512MB	512MB	1024MB

1.2.5 I/O Ports

- **Audio Ports**

  - Microphone In & Line Out
  - Built in 2 high quality internal speaker (2W)
  - Built in 1 mono microphone

RJ-11

- Connection to Modem Daughter Board Connector

Table 3. Modem Port

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	LINE +	I/O	Phone Line Positive
3	LINE -	I/O	Phone Line Negative
4	NC	-	No Connect

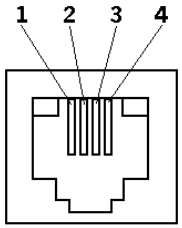


Figure 1 . Modem Connector

RJ-45

- Connection to On-Board NIC controller

Table 4. LAN Port

Pin	Signal Name	Direction	Description
1	TX+	Out	Transmit Data Ring
2	TX-	Out	Transmit Data Tip
3	RX+	IN	Receive Data Ring
4	TERM1	-	Internal termination resistor
5	TERM2	-	Internal termination resistor
6	RX	IN	Receive Data Tip
7	TERM3	-	Internal termination resistor
8	TERM4	-	Internal termination resistor

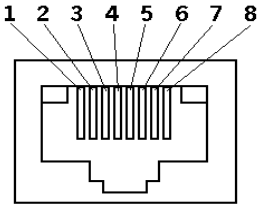


Figure 2 . LAN Connector

USB Ports

- Six industry standard USB 2.0 ports

Table 5. USB Port

Pin	Signal Name	Direction	Description
1	VCC	-	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	-	Ground

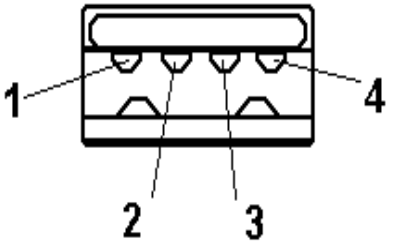


Figure 3 . USB Connector

7 Pins S-VIDEO Port for TV-Out

- Support up 1024*768 resolution
- Support PAL and NTSC system
- Support composite Output by a transfer cable(RCA)

Table 6. S-Video Port

Pin	Signal Name	Direction
1	GND	-
2	NC	-
3	GND	-
4	LUMA	O
5	NC	-
6	CRMA	O
7	COMP	O

CRT Ports

- Standard VGA compatible port
- DDC1 and DDC2B compliant (RCA)

Table 7. CRT Connector

PIN	SIGNAL	DESCRIPTION
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	Monitor Sense
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	Monitor Sense
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync control
14	VSYNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor

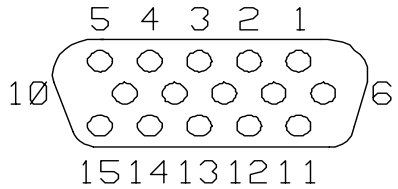


Figure 4 . CRT Connector

1.2.6 PC Card Slot

- One Type II/I slot supporting the 1997 PC Card standard,and including full R2 (16-bit) and 32-bit Cardbus data transfer
- TI PCI1410A (PCMCIA Controller) & TI TPS2211A (Power Switch)

1.2.7 Graphical Subsystem

- Integrate Real256E GPU +SIS301LV Video Bridge

1.2.8 Display

- Internal LCD Display is 15” TFT XGA panel
- External Video refresh rate of up to 85Hz supported

  - Vertical refresh frequencies to meet VESA requirements
  - Simultaneous video in specified video modes – switchable with hot key

1.2.9 LEDs Indiactor

- CDROM & HDD & NUM & CAP & SCROLL & WLAN
- AC & BAT & CHARGE

1.2.10 Read Only Memory (BIOS Flash)

- Fully compatible with industry standard software including Windows 2000 & Windows XP
- Fully supports APM V1.2 and latest ACPI specification
- 2Mb Flash BIOS
- Inside BIOS core

1.2.11 Power Management Features

- Local standby mode (Individual devices such as HDD, graphics controller,LCD etc..)
- CPU Idle mode (Including ACPI modes C1 and C2)
- Suspend mode (Including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant
- Fully ACPI V1.1 compliant
- Hibernate for Windows XP
- Thermal management
- Fully US EPA Energy Start compliant

1.2.12 Keyboard Controller

- Winboard W83L950D

1.2.13 Buttons

- Power on bin

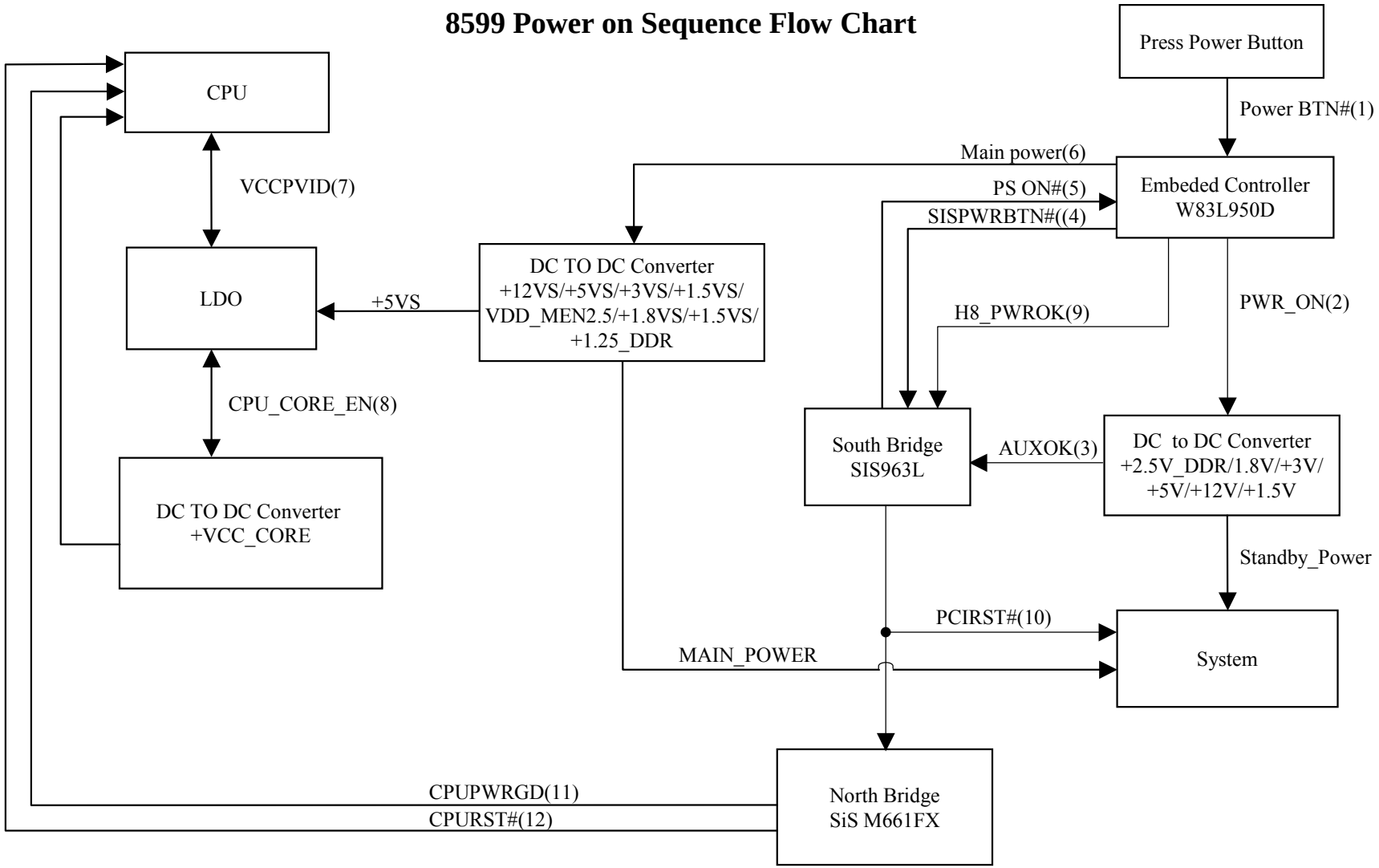
1.2.14 Modem

Table 8. Modem Daughter Board Connector

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MONO_OUT	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

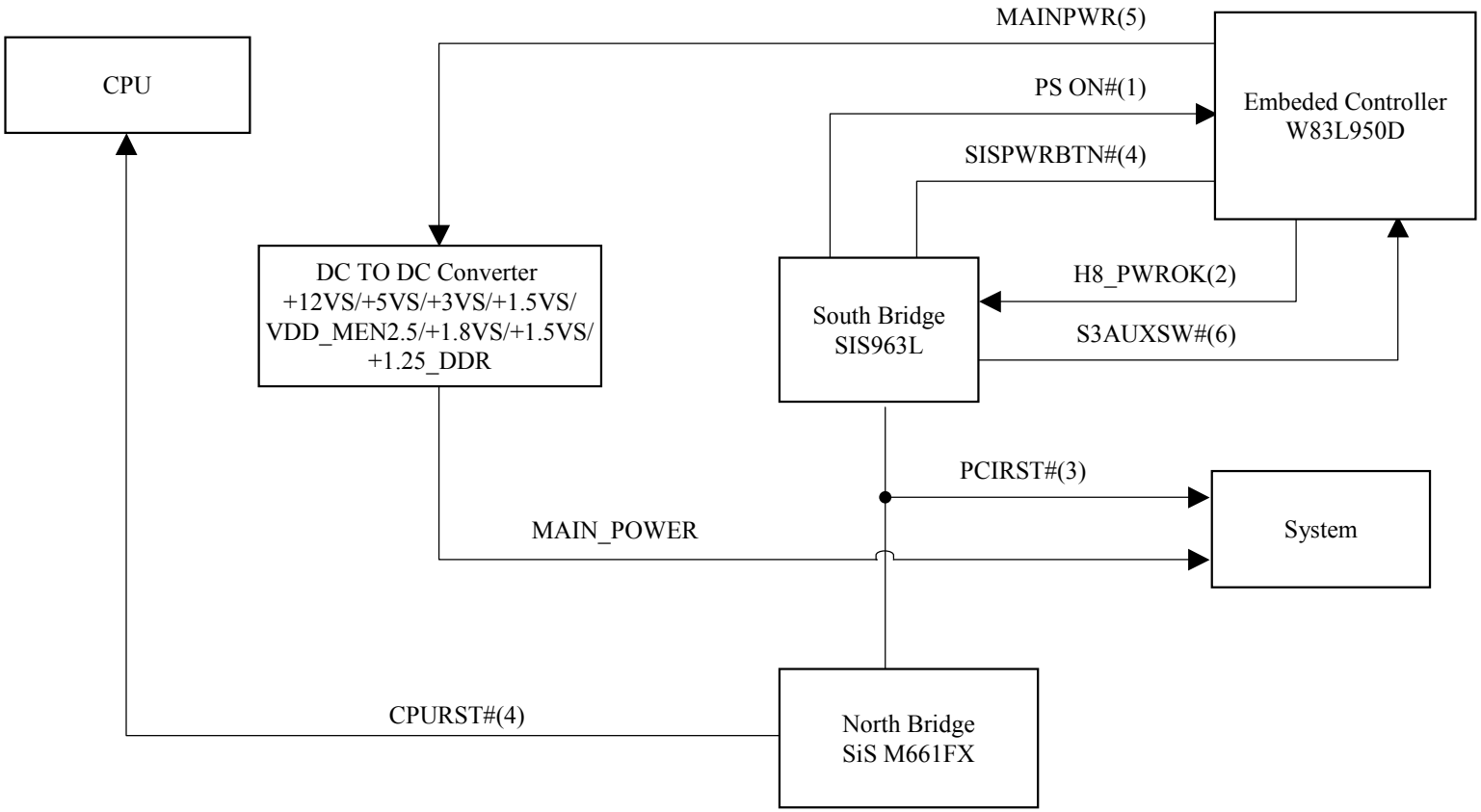
1.3 Electrical Characteristic

1.3.1 Power On Sequence



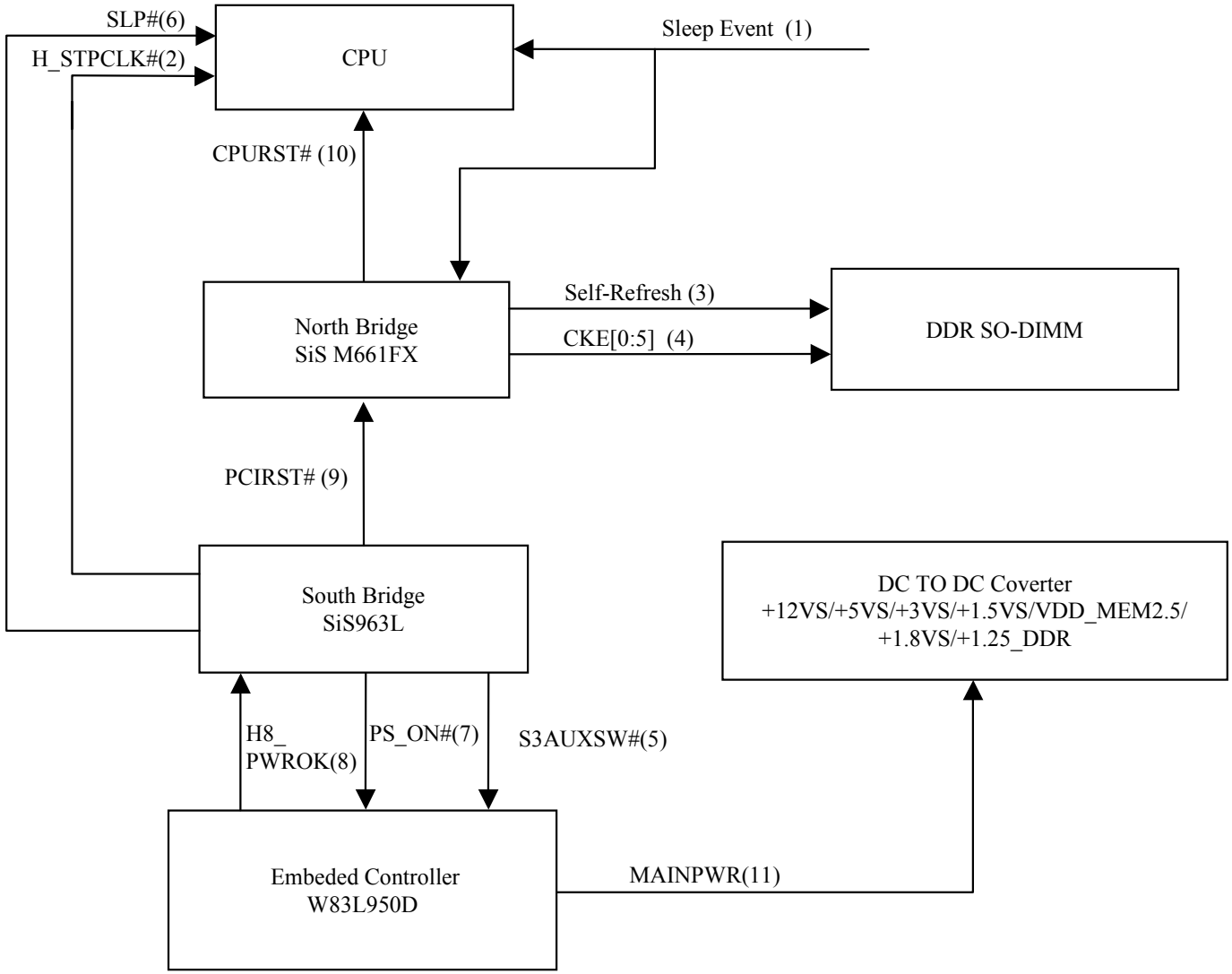
1.3.2 Power Off Sequence

8599 Power off Sequence Flow Chart



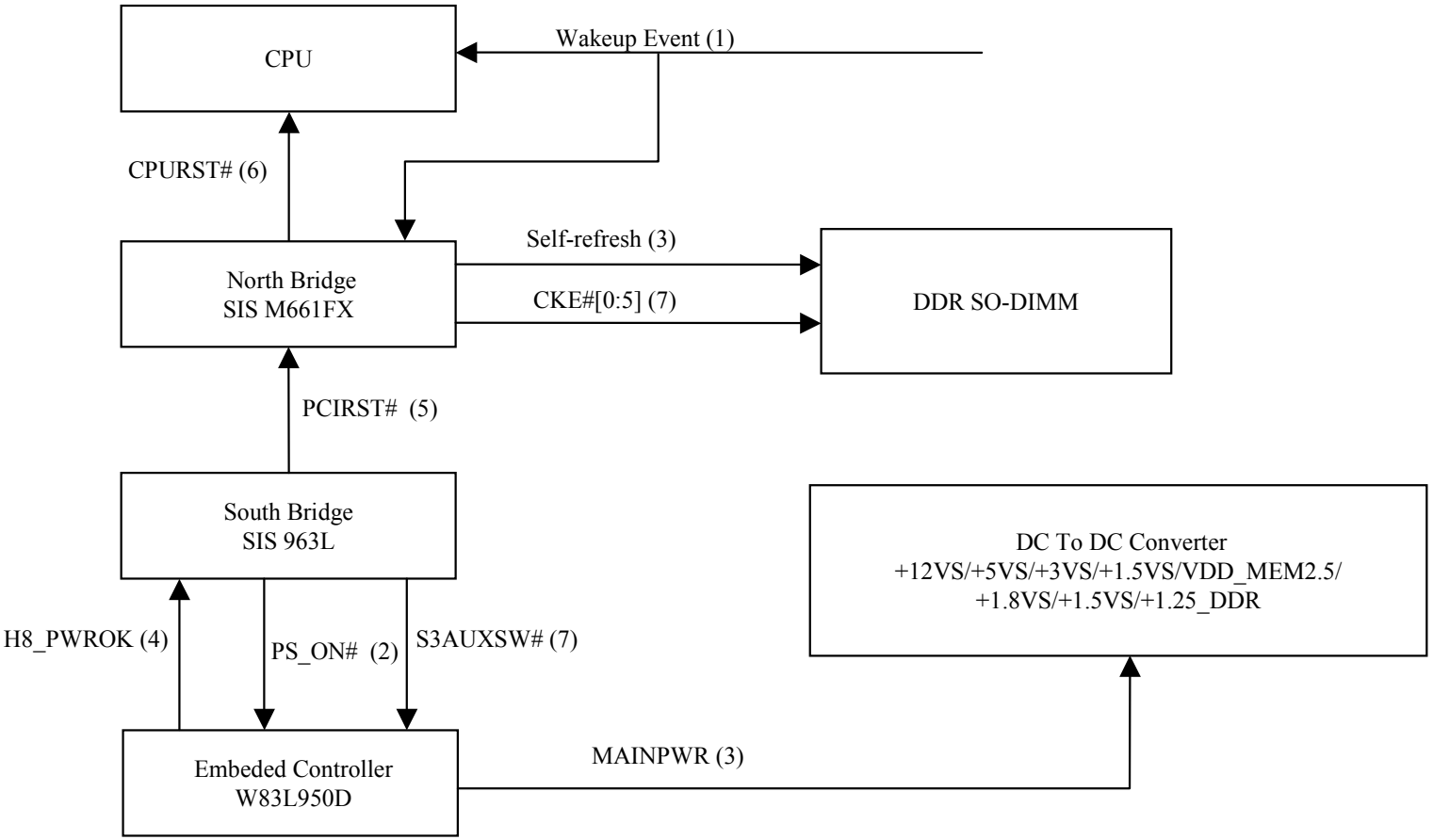
1.3.3 Suspend To RAM Sequence

8599 STR Sequence Flow Chart



1.3.4 Resume from Suspend To RAM Sequence

8599 Resume From STR Sequence Flow Chart



1.3.5 Power Consumption Of Suspend Mode

- Suspend to RAM < 40mA
- Suspend to Disk / Soft-Off /Mechanical Off < 1mA

1.4 Appendix 1: SiS963L GPIO Definitions

Pin Name	Pin Function	Signal Name	Type Define	Power Plan
GPIO0	GPIO	ENBKL_NAME	O	MAIN
GPIO1	GPIO	FLASH	O	MAIN
GPIO2	GPIO	SB_THRM#	I	MAIN
GPIO3	GPIO	EXTSMI#	I	MAIN
GPIO4	GPIO	CLKRUN#	I/O	MAIN
GPIO5	GPIO	MPCI_PD#	I	MAIN
GPIO6	GPIO	SPK_OFF#	O	MAIN
GPIO7	GPIO	GPWAK#	T/P	AUX
GPIO8	GPIO	WAKE_UP#	I	AUX
GPIO9	GPIO	SCI#	I	AUX
GPIO10	GPIO	CRT_IN#	I	AUX
GPIO11	GPIO	STP_PCI#	O	AUX
GPIO12	GPIO	CPU_STP#	O	AUX
GPIO13	GPIO	DPRSLPVR	O	AUX
GPIO14	GPIO	LCD_ID0	I	AUX
GPIO15	GPIO	GMUXSEL	T/P	AUX
GPIO16	GPO	CPUPERF#	O	AUX
GPIO17	GPO	N/A	T/P	AUX
GPIO18	GPO	N/A	T/P	AUX
GPIO19	GPIO	SMBCLK	I/O	AUX
GPIO20	GPIO	SMBDATA	I/O	AUX
GPIO21	GPI	GPIO21_EESK		AUX
GPIO22	GPI	GPIO22_EEDI		AUX
GPIO23	GPI	GPIO23_EEDO		AUX
GPIO24	GPI	GPIO24_EECS		AUX
APICD0			NC	MAIN(GTL LEVEL
APICD1			NC	MAIN(GTL LEVEL
APICCLK			NC	MAIN
OC5	GPI			AUX

1.5 Appendix 2: Keyboard Controller Pin Definitions (1)

Pin	Port	Signal Name	Type	Description
39~54	GP17~GP0	KO[0..15]	O	Keyboard Matrix
55~62	GP37~GP30	KI[7..0]	O	Keyboard Matrix
65~68	GP85~GP82	LAD[0..3]	I/O	LPC BUS
70	GP80	PCI_KBCLK	I	LPC CLK
69	GP81	SERIRQ	O	Serial IRQ
64	GP86	KBCLRST#	I	LPC Reset
63	GP87	LFRAME#	I/O	LPC FRAME
17	GP50	MAINPWR	O	We use this signal to control "VS" power on/off. HI:ON,LOW:OFF
15	GP52	SUSB#	I	STR Indicator signal
14	GP53	ADEN#	I	ADAPTOR IN
23	GP42	SW_+5VA	O	Switch +5VA
22	GP43	COVER_SW#	I	LCD Cover switch
19	GP46	SCI	O	Connect to South Bridge (SiS963L) to system configuration interrupt (ACPI mode)
3	GP76	BAT_DATA	I/O	SMBUS DATA for LM86 themal sensor & BATT THERMAL
2	GP77	BAT_CLK	I/O	SMBUS CLK for LM87 themal sensor & BATT THERMAL
27	GP40	FAN0	O	Control CPU FAN ON & Tum ON/OFF Duty
26	GP41	FAN1	O	Control System D/D FAN (Second FAN) ON & Tum ON/OFF Duty
13	GP54	FAN0_SPD0	I	Return FAN0 (CPU FAN) Speed
12	GP55	FAN0_SPD1	I	Return FAN0 (Second FAN) Speed
16	GP51	BATT_DEAD#	I	Indicated the battery capacity is not enough to power on system
18	GP47	PWRON	O	Control System Power ON/OFF
21	GP44	NUM#	O	Keyboard Number Lock indicator
20	GP45	CAP#	O	Keyboard CAPs Lock indicator
9	GP70	T_DATA	I/O	Conneter to touch Pad DATA
8	GP71	LEARNING#	I	Battery discharge control
7	GP72	SIS_PWRBTN#	O	Power Button Signal to SiS963L
6	GP73	T_CLK	I/O	Connect to Touch Pad clock

1.5 Appendix 2: Keyboard Controller Pin Definitions (2)

Continue to the previous page

Pin	Port	Signal Name	Type	Description
5	GP74	PWROK	O	System Power Good
4	GP75	PSON#_SB	I	System inter S4~S5,Positive Logic
38	GP20	SB_THRM#	O	TO SiS963L,Regustang the sysytem toenter power mangmentmode,Clock Throtting
37	GP21	WAKE_UP#	O	Connect to South Bridge (SiS963L) to wake up system
36	GP22	BATT_G#	O	The indicator when battery in charging
35	GP23	BATT_R#	O	The indicator when battery in charging
34	GP24	EXTSM#	O	Connect to South Bridge (SiS963L) to system management interrupt (Non-ACPI mode)
33	GP25	BATT_POWER#	O	The indicater when power supply from Battery
32	GP26	SCROLL#	O	Keyboard scroll lock indicator
31	GP27	AC_POWER#	O	The indicator when power supply from AC-Adapter
11	GP56	BLADJ	O	Back/Light Adijust Control
10	GP57	CHG_I	O	Supply current to Battery
1	GP60	PWRBTN#	I	Power Switch Signal to KBC
80	GP61	VRMPWRGD	I	CPU Power Good
79	GP62	+3V	I	
78	GP63	BAT_TEMP	I	Report Battery Thermal
77	GP64	BAT_VOLT	I	Report Battery Voltage
76	GP65	I_LIMIT	I	FOR BATTERY CHARGE I limit
75	GP66	I_CHG	I	Battery charge current
74	GP67	I_DISCHG	I	Battery discharge current
25	RESET#	RESET#	I	KBC Reset
28	XIN	XIN		
29	XOUT	XOUT		
72	VREF	+3VA		
71	VCC	+KBC_VDDA		

1.6 Appendix 3: Audio Performance

8599 meet all the following items

Table 9. Digital Playback (PC-D-A) for Line Output

Test Items	Mobile System
Full Scale Output Voltage	≧0.7Vrms (3.3V audio)
Sample Frequency Accuracy	≦0.1%
Frequency Response (44.1ks/sec)	20Hz～15kHz
Frequency Response (48ks/sec)	20Hz～15kHz
Dynamic Range (SNR)	≧70dBFSA
THD+N	≦-55dBFS
Cross-talk	≧50dB

Table 10. Analog Pass-through(A-A) for Microphone Input to Line Output

Test Items	Mobile System
Frequency Response	100Hz～12kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Table 11. Digital Recording(A-D-PC) for Microphone Input

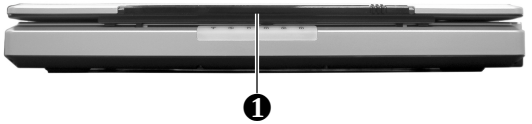
Test Items	Mobile System
Full Scale Input Voltage	≧100mVrms
Sample Frequency Accuracy	≦0.1%
Frequency Response(22.05ks/sec)	100Hz～8.8kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

2. System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Top Cover Latch

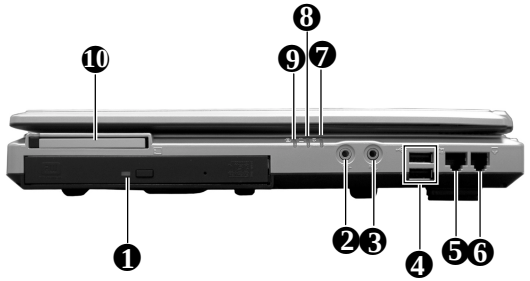


2.1.2 Left-side View

❶ Lock

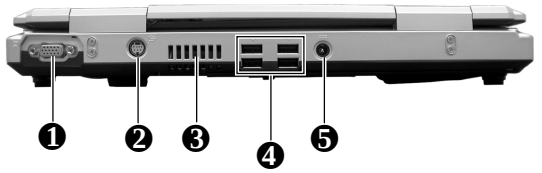
❷ Ventilation Openings

2.1.3 Right-side View



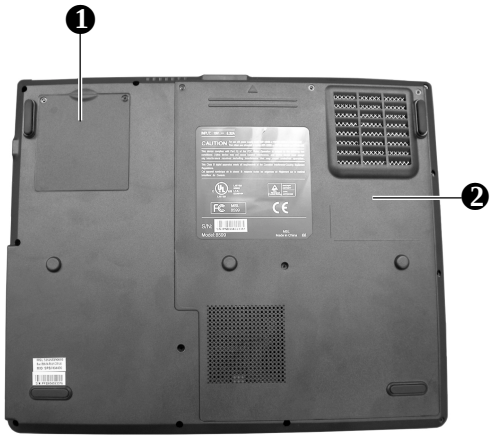
❶ CD/DVD driver
❷ Line out jack
❸ MIC in jack
❹ USB port *2
❺ RJ-45 connector
❻ RJ-11 connector
❼ AC Power Indicator
❽ Battery Power Indicator
❾ Battery Charge Indicator
❿ PC Card slot

2.1.4 Rear View



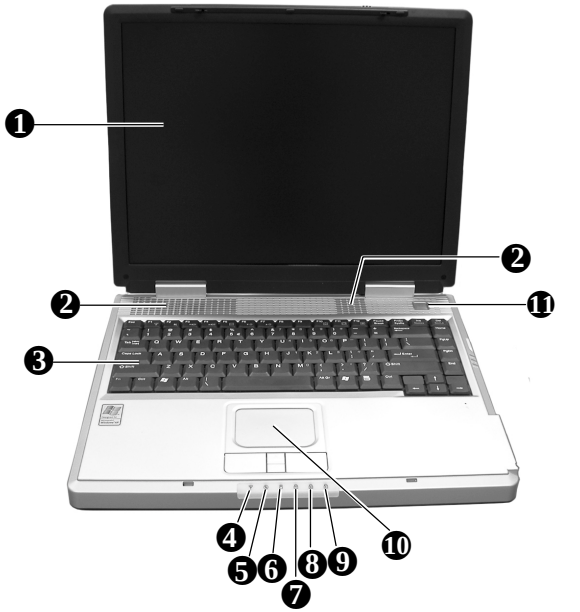
❶ VGA port
❷ S-Video output connector
❸ Ventilation Openings
❹ USB port *4
❺ Power connector

2.1.5 Bottom View



❶ Wireless Card cover
❷ CPU

2.1.6 Top-open View

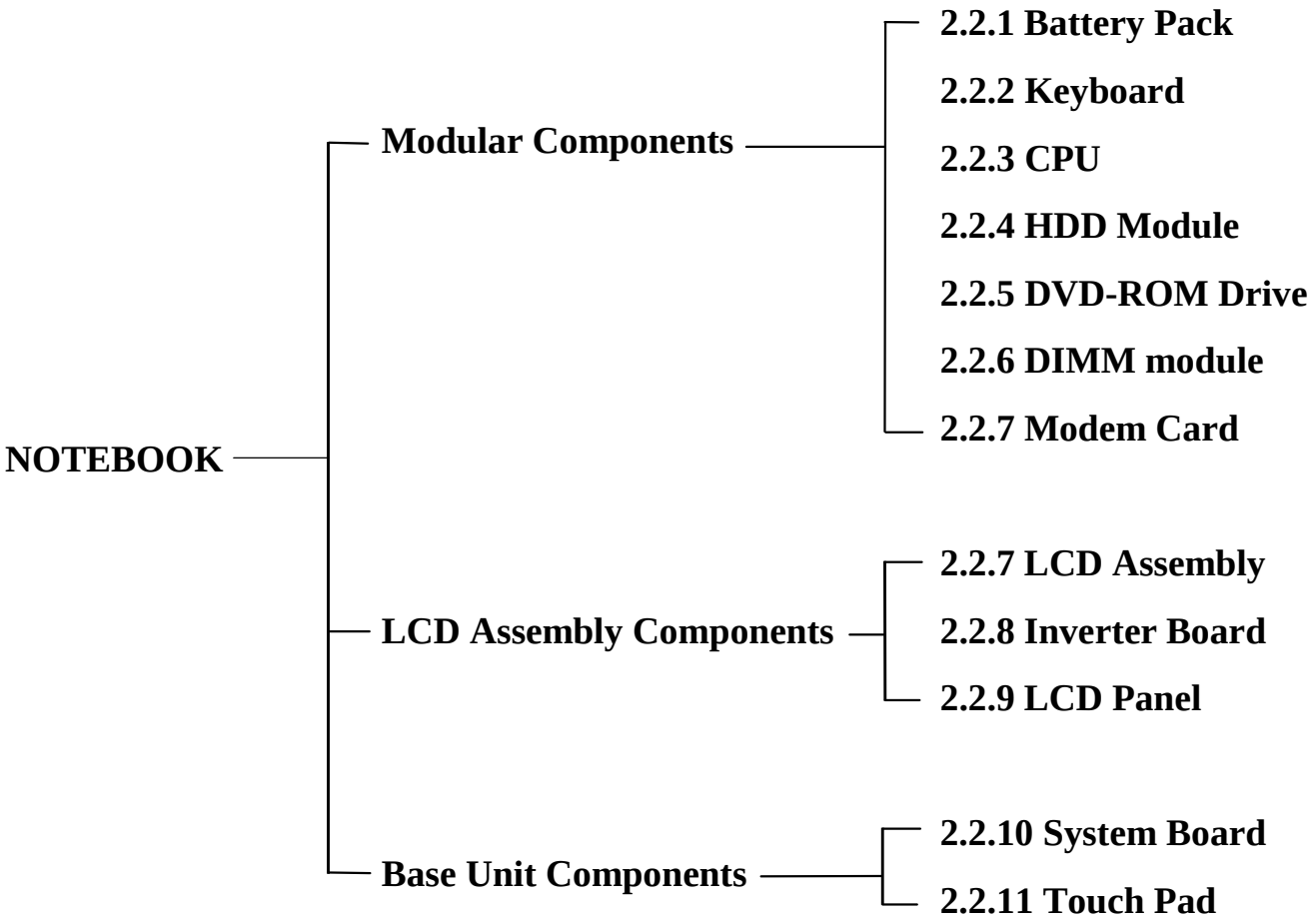


❶ LCD Screen
❷ Stereo set
❸ Keyboard
❹ Caps Lock
❺ Wireless Card Indicator
❻ CD/DVD-Rom Indicator
❼ HDD Indicator
❽ Num Lock
❾ Caps Lock
❿ Scroll Lock
⓫ Power Button

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Remove the four screws, then remove the CPU cover. (Figure 2-1)
3. Put up the battery pack, then free the battery pack. (Figure 2-2)

Figure 2-1 Remove the four screws

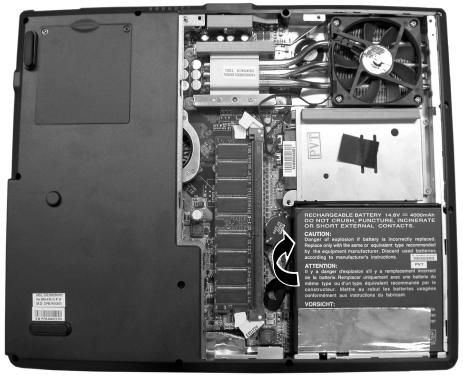


Figure 2-2 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Replace the CPU cover and secure the four screws.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Open the top cover.
3. Loosen the five latches locking the keyboard. (Figure 2-3)

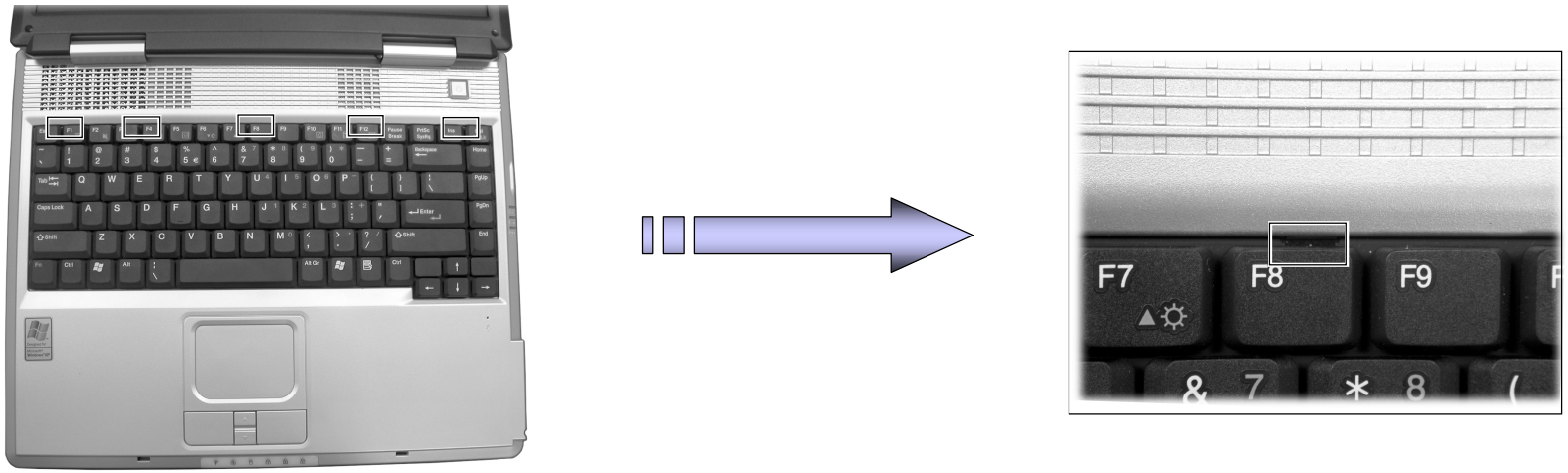


Figure 2-3 Loosen the five latches

4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-4)

Figure 2-4 Lift up the keyboard and disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back.
2. Replace the keyboard into place and fasten the five latches.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove five screws that secure the heatsink upon the CPU. (Figure 2-5)
3. Disconnect the fan's power cord from system board. (Figure 2-6)

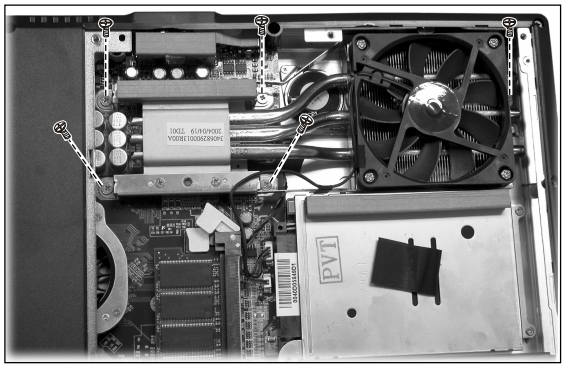


Figure 2-5 Remove five screws

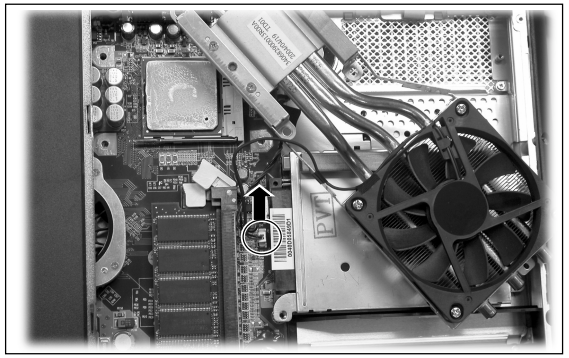


Figure 2-6 Disconnect the cable

4. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-7)

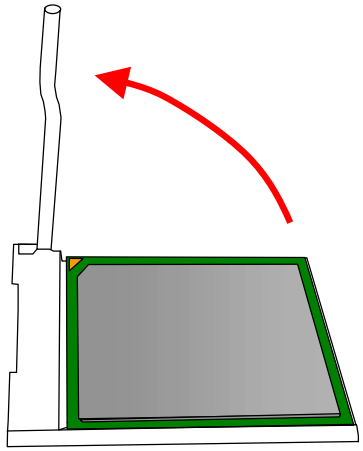


Figure 2-7 Free the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Reconnect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with five screws.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD module and slightly lift up HDD module. (Figure 2-8)
3. Remove four screws to separate the hard disk drive from the bracket, free the hard disk driver. (Figure 2-9)

Figure 2-8 Remove HDD module

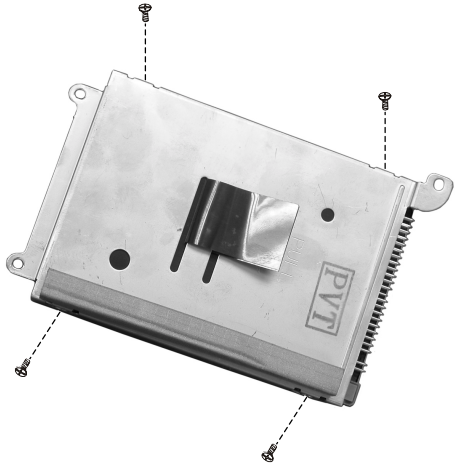


Figure 2-9 Free the HDD driver

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with two screws.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(❷). (Figure 2-10)

Figure 2-10 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 DIMM Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. To remove the memory module, pull the retaining clips outwards to the unlocked and lift the DIMM module up. (Figure 2-11)

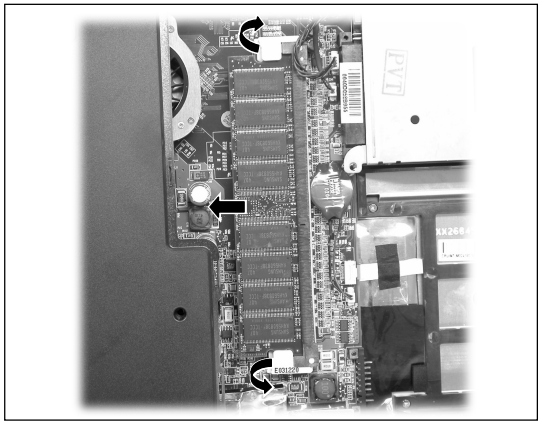


Figure 2-11 Remove the DIMM module

Reassembly

1. Replace DIMM module and lock it retaining clips.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Modem Card

Disassembly

1. Remove the battery, keyboard, CPU, hard disk driver, CD/DVD-ROM driver. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5 Disassembly)
2. Remove the four screws. (Figure 2-12)
3. Remove the eleven screws and put up the housing. (Figure 2-13)

Figure 2-12 Remove eleven screws

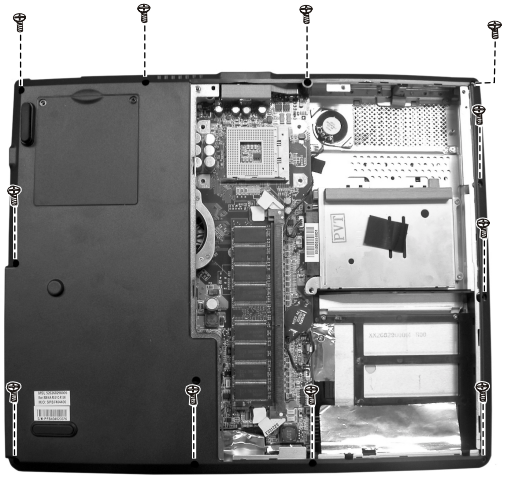


Figure 2-13 Free the housing

4. Remove three screws and free the bottom shielding. (Figure 2-14)
5. Disconnect the cable and remove the two screws. (Figure 2-15)

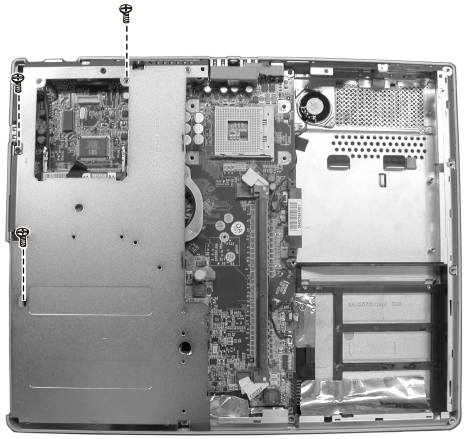


Figure 2-14 Free the bottom shielding

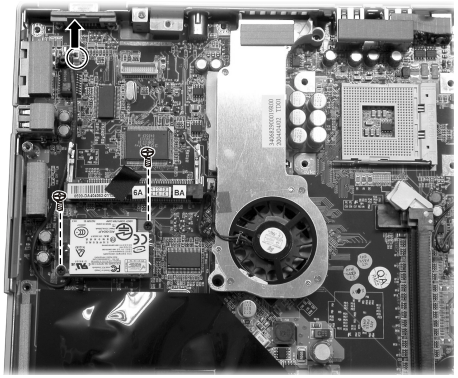


Figure 2-15 Free the Modem Card

Reassembly

1. Replace the modem card and secure two screws.
2. Reconnect the cable to the system board.
3. Replace the bottom shielding and secure the three screws.
4. Fit the top cover and the housing, then secure the fifteen screws.
5. Replace CD/DVD-ROM, HDD, CPU, keyboard and battery pack. (See sections 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.2.1 and 2.2.2 Disassembly)
2. Remove two hinge covers. (Figure 2-16)
3. Carefully put the notebook upside down. Remove the two screws fastening the wireless cover. (Figure 2-17)

Figure 2-16 Remove two hinge covers

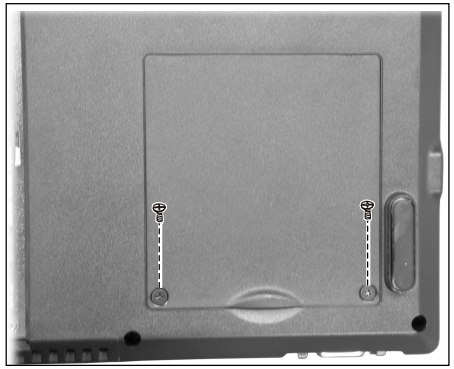


Figure 2-17 Remove the two screws

4. Disconnect the LCD cable from the system board and detach the antenna. (Figure 2-18)
5. Remove the four screws and put up the LCD assembly, then free the LCD assembly. (Figure 2-19)

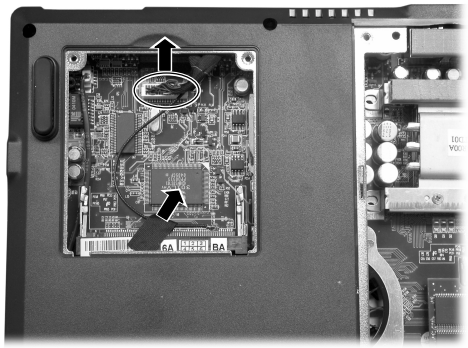


Figure 2-18 Disconnect the LCD cable

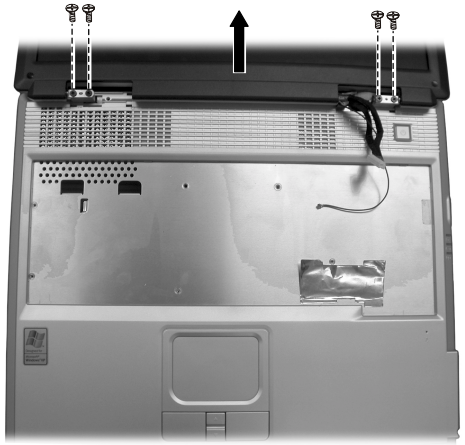


Figure 2-19 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws, then fit the antenna.
2. Reconnect the one cable to the system board, Then replace the wireless cover and secure two screws.
3. Replace the two hinge covers.
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.9 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove two screws and rubbers on the corners of the LCD panel. (Figure 2-20)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the one screw fastening the inverter board. (Figure 2-21)

Figure 2-20 Remove LCD cover

Figure 2-21 Remove the one screw

5. To remove the inverter board on the lower part of the LCD housing , disconnect two cables. (Figure 2-22)

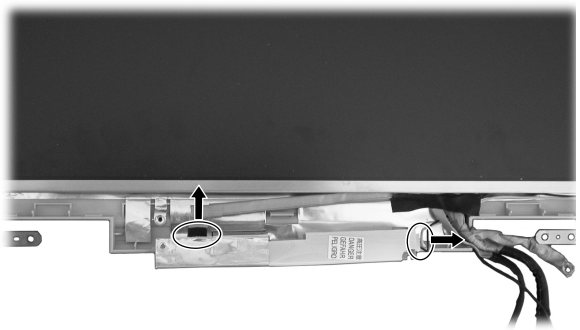


Figure 2-22 Remove the inverter board

Reassembly

1. Reconnect the two cables. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD cover and secure with two screws and rubbers.
3. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to sections 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer for two steps 2,3 of section 2.2.9 Disassembly)
3. Remove the eight screws fastening the LCD panel and detach the cable, Then lift it up. (Figure 2-23)
4. Remove the five screws fastening the LCD brackets. (Figure 2-24)

Figure 2-23 Remove the eight screws and detach the cable

Figure 2-24 Remove the five screws

5. Disconnect the cable and free the LCD panel. (Figure 2-25)

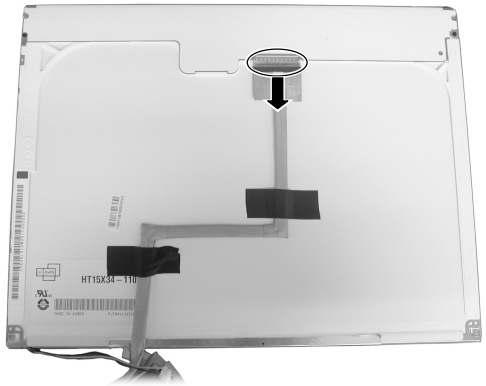


Figure 2-25 Free the LCD panel

Reassembly

1. Reconnect the cable, then replace the LCD brackets and secure with five screws.
2. Fit the LCD panel back into place and secure with eight screws, then reconnect the cable to the inverter board.
3. Replace the LCD cover and secure with two screws and rubbers. (Refer to section 2.2.9 Reassembly)
4. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
5. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DIMM module, modem card and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Disconnect the heatsink's cable from the system board and remove two screws fastening the heatsink. (Figure 2-26)
3. Disconnect the speaker's cable and the touch pad's cable from the system board.To free the system board, please remove one screw and four hex nuts that fastening the system board. (Figure 2-27)

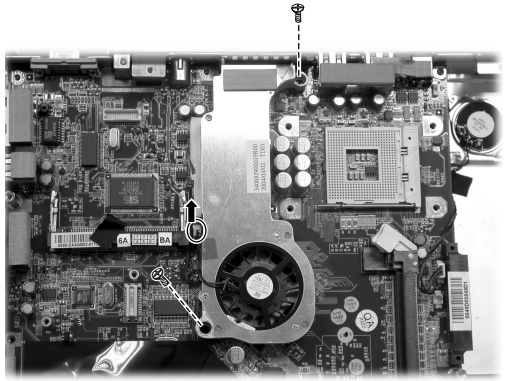


Figure 2-26 Free the heatsink

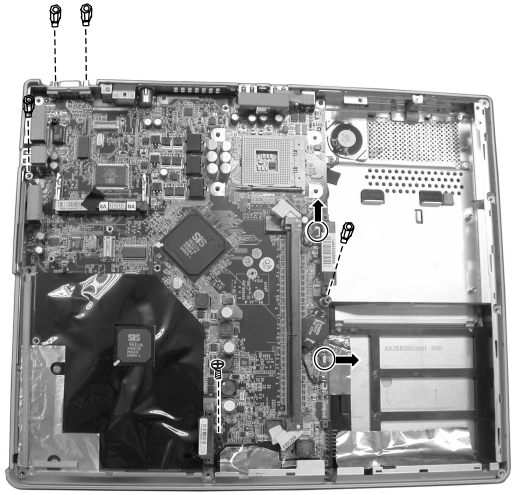


Figure 2-27 Free the system board

Reassembly

1. Replace the system board into the top cover and secure with one screw and four hex nuts.
2. Reconnect the touch pad's cable, the speaker's cable.
3. Replace the heatsink and secure the two screws, then reconnect the cable to the system board.
4. Replace the modem card. (See sections 2.2.7 reassembly)
5. Replace the LCD assembly, DIMM module, CD/DVD-ROM, HDD, CPU, keyboard and battery pack. (See sections 2.2.8, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.12 Touch Pad

Disassembly

1. Remove the system board. (See section 2.2.11 Disassembly)
2. Remove the two screws and disconnect the cable, then free the touch pad. (Figure 2-28)

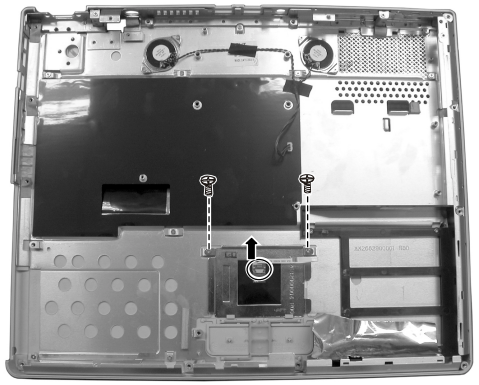


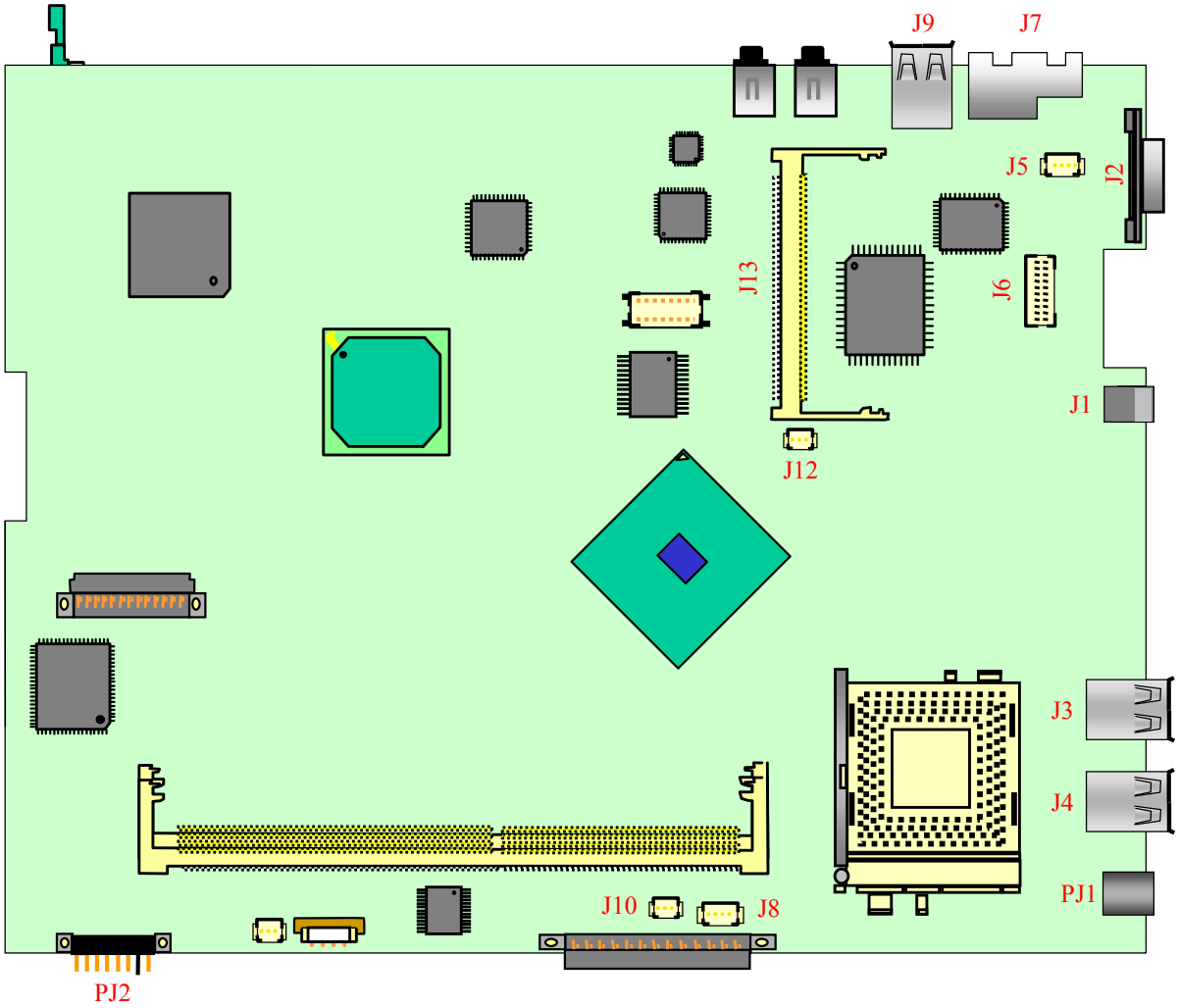
Figure 2-28 Free the touch pad

Reassembly

1. Replace the touch pad and reconnect the cable.
2. Replace the touch pad shielding and secure with two screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 1

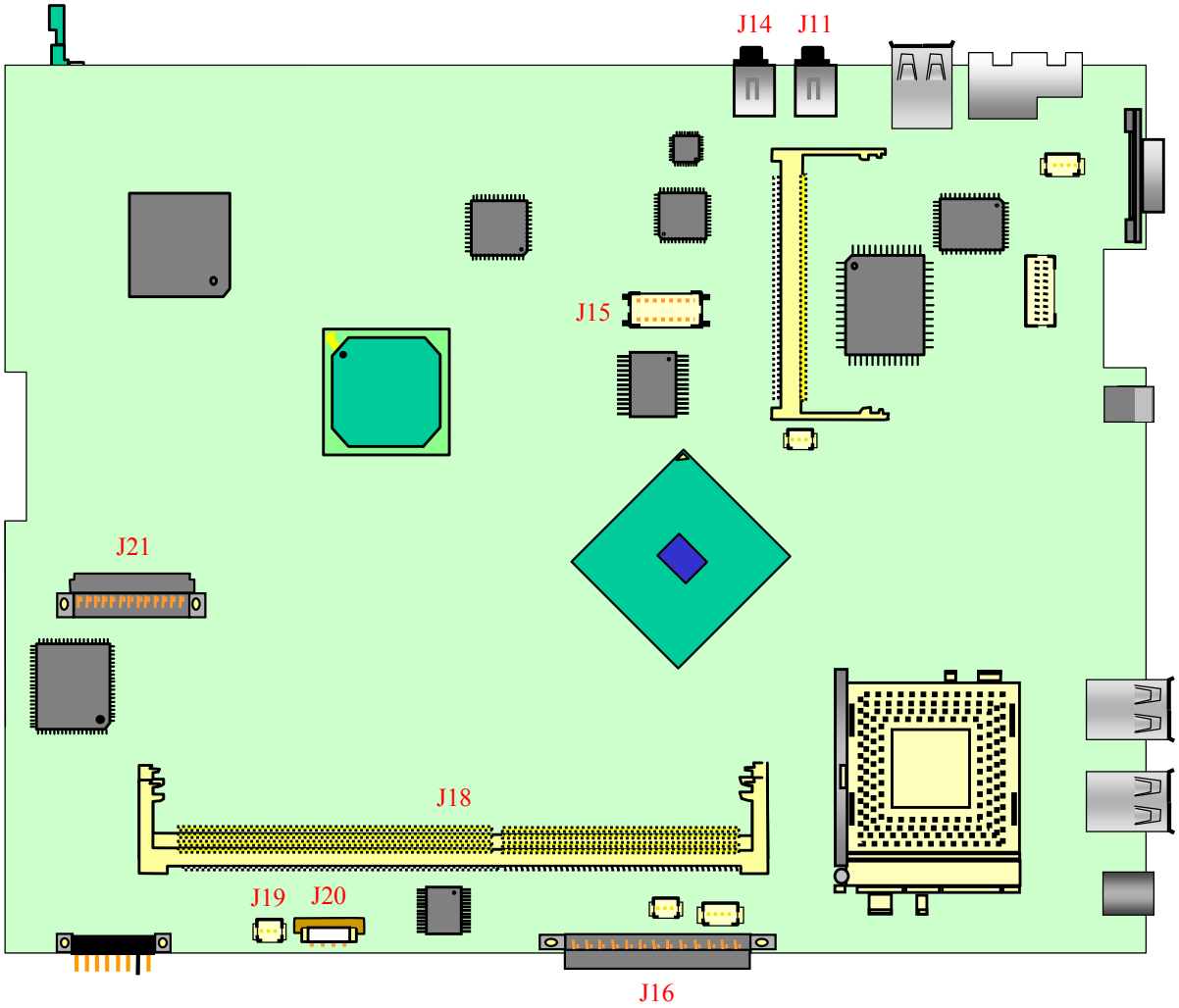


- PJ1 : AC Power Jack
- PJ2 : Battery Connector
- J1 : S-Video Port
- J2 : External VGA Connector
- J3, J4, J9 : USB Port Connector
- J5 : MDC Jump Wire Connector
- J6 : LCD Connector + Inverter
- J7 : RJ11 & RJ45 Connector
- J8 : Internal Left Speak Connector
- J10 : CPU Fan Connector
- J12 : NB Fan Connector
- J13 : Mini-PCI Socket

------ To next page ------

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 2

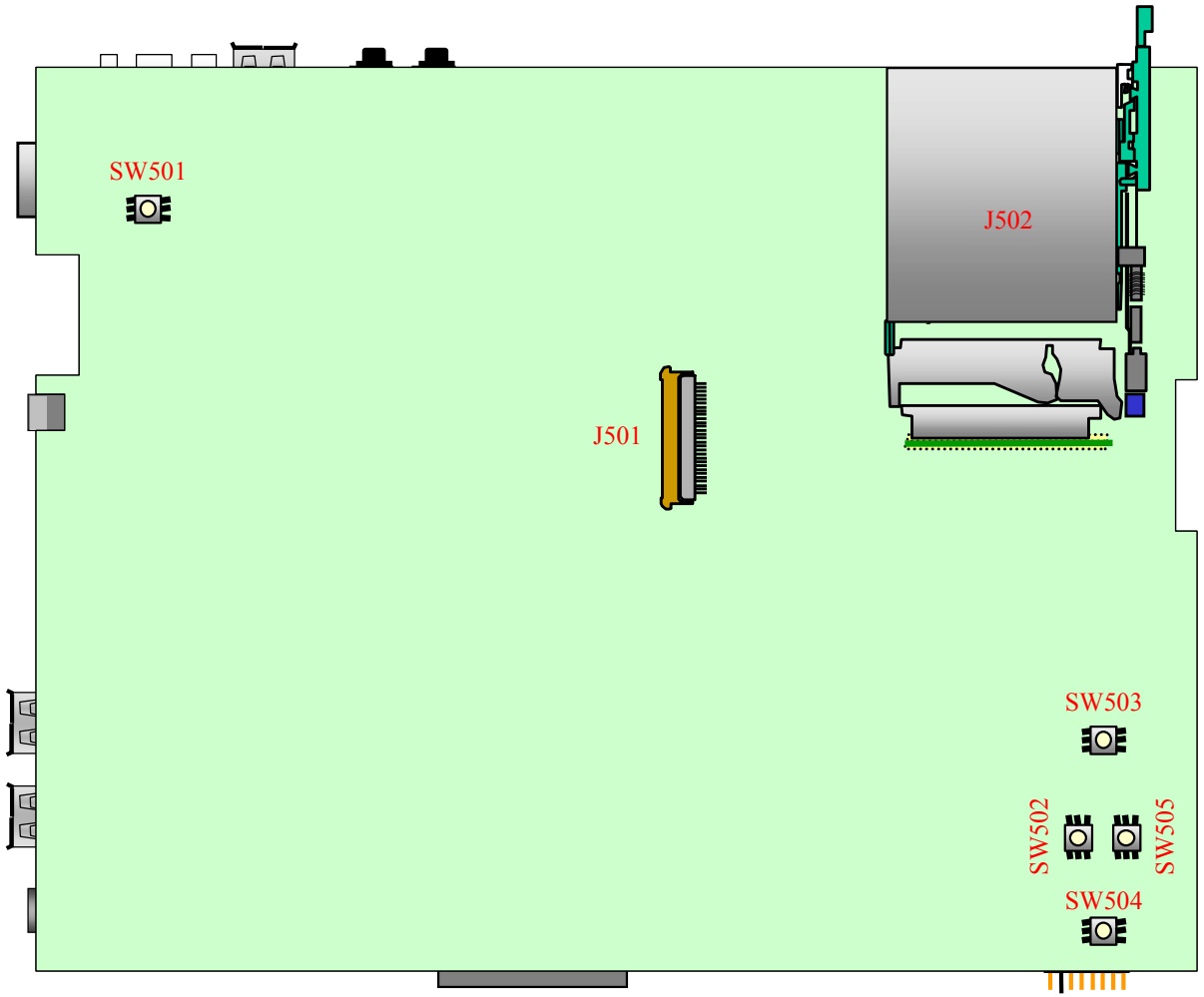


------ Continued to previous page ------

- J11 : MIC In Jack
- J14 : Line Out Jack
- J15 : MDC Board Connector
- J16 : Primary EIDE Connector
- J18 : Extend DDR SDRAM Socket
- J19 : RTC Battery Connector
- J20 : Touch-Pad Connector
- J21 : Secondary IDE Connector

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side B)

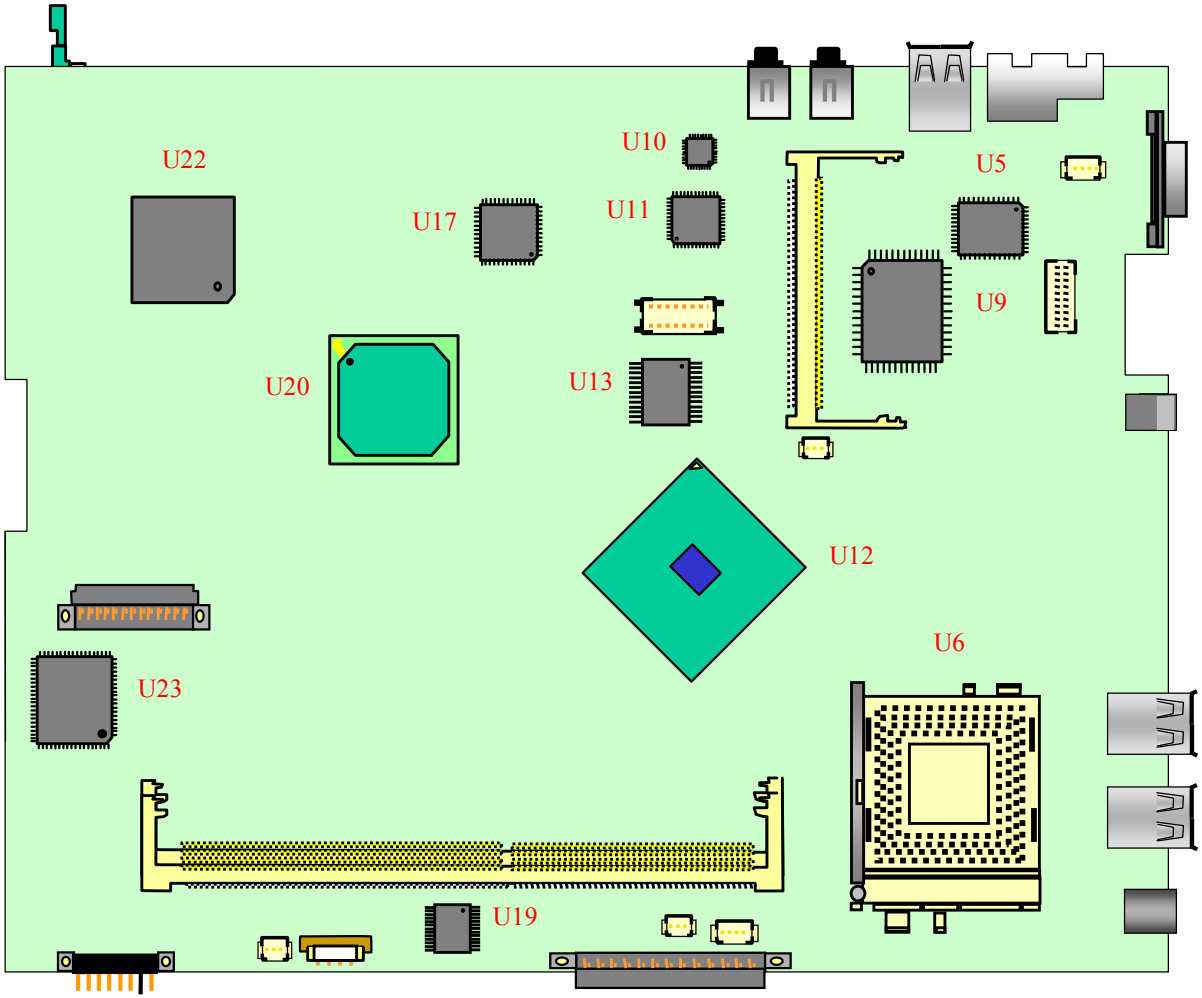


- J501 : Internal Keyboard Connector
- J502 : PCMCIA Card Socket

- SW501 : Power Button
- SW502 : Touch-Pad Up Button
- SW503 : Touch-Pad Right Button
- SW504 : Touch-Pad Left Button
- SW505 : Touch-Pad Down Button

4. Definition & Location of Major Components

4.1 Mother Board (Side A)



- U5 : ICS1883AF LAN Controller
- U6 : Intel P4 Process Socket
- U9 : TV/ LVDS Encoder (SiS301LV)
- U10 : GMT G1422 Amplifer
- U11 : VIA VI1616 Audio Codec
- U12 : SiS M661FX NB
- U13 : ICS952007 Clock Generator
- U17 : KBC (W83L950D)
- U19 : DDR Buffer Clock
- U20 : SiS963L SB
- U22 : Ti PCI1410A CardBus
- U23 : LPC BIOS ROM

5. Pin Descriptions of Major Components

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 1

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>AP[1:0]#</td><td>Input/ Output</td><td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines
<table>
<tr><th>Request Signals</th><th>subphase 1</th><th>subphase 2</th></tr>
<tr><td>A[35:24]#</td><td>AP0#</td><td>AP1#</td></tr>
<tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr>
<tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr>
</table>
</td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V CROSS .</td></tr>
<tr><td>BINIT#</td><td>Input/ Output</td><td>BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted
to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries.
If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</td></tr>
<tr><td>BNR#</td><td>Input/ Output</td><td>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/ Output</td><td>A[35:3]# (Address) define a 2 36 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals
must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/ Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/ Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB0#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB1#</td></tr>
</table>
</td></tr>
</table>

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 2

Name	Type	Description
HIT# **HITM#**	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signals does not have on-die termination. Refer to Section 2.5 fortermination requirements.**
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package. Refer to Section 2.5 for additional details and termination requirements.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

Name	Type	Description
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#	Output	FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 3

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 11 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 16, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 4

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. See Figure 12 and Table 16 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 5

Name	Type	Description
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow he guidelines for VCCA, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
VCCSENSE	Output	VCCSENSE is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSSSENSE	Output	VSSSENSE is an isolated low impedance connection to processor core Vss. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 SiS M661FX (IGUI Host Memory Controller) - 1

Host Bus Interface

Ball Name	Ball Attr	Description
CPUCLK CPUCLK#	I 0.71V – M	Host differential clock input.
CPURST#	O 0.9~1.8V – M	Host Bus Reset: CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
CPUPWRGD	O 0.9~1.8V – M	CPUPWRGD is used to inform CPU that main power is stable
ADS#	I/O 0.9~1.8V – M	Address Strobe : Address Strobe is driven by CPU or SiSM661FX to indicate the start of a CPU bus cycle.
HASTB[1:0]#	I/O 0.9~1.8V – M	Source synchronous address strobe used to latch HREQ[4:0]# & HA[31:3]# at both falling and rising edge. HREQ[4:0]# & HA[16:3]# are latched by HASTB0# HA[31:17]# are latched by HASTB1#
HREQ[4:0]#	I/O 0.9~1.8V – M	Request Command: HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
HA[31:3]#	I/O 0.9~1.8V – M	Host Address Bus
BREQ0#	O 0.9~1.8V – M	Symmetric Agent Bus Request: BREQ0# is driven by the symmetric agent to request for the bus.
BPRI#	O 0.9~1.8V – M	Priority Agent Bus Request: BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
BNR#	I/O 0.9~1.8V – M	Block Next Request: This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	I 0.9~1.8V – M	Host Lock : CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	I/O 0.9~1.8V – M	Keeping a Non-Modified Cache Line

Host Bus Interface (Continued)

Ball Name	Ball Attr	Description
HITM#	I/O 0.9~1.8V – M	Hits a Modified Cache Line: Hit Modified indicates the snoop cycle hits a modified line in the L1/L2 cache of CPU.
DEFER#	O 0.9~1.8V – M	Defer Transaction Completion: SiSM661FX will use this signal to indicate a retry or defer response to host bus.
RS[2:0]#	O 0.9~1.8V – M	Response Status: RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. RS[2:0]# Response 000 Idle State 001 Retry 010 Defer 011 Reserved 100 Reserved 101 No data 110 Implicit Write-back 111 Normal
HTRDY#	O 0.9~1.8V – M	Target Ready: During write cycles, response agent will drive TRDY# to indicate it is ready to accept data.
DRDY#	I/O 0.9~1.8V – M	Data Ready: DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O 0.9~1.8V – M	Data Bus Busy: Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
HD[63:0]#	I/O 0.9~1.8V – M	Host Data Bus
DBI[3:0]#	I/O 0.9~1.8V – M	Dynamic Bus Inversion: An active DBI# will invert it's corresponding data group signals. DBI0# is referenced by HD[15:0]# DBI1# is referenced by HD[31:16]# DBI2# is referenced by HD[47:32]# DBI3# is referenced by HD[63:48]#

5.2 SiS M661FX (IGUI Host Memory Controller) - 2

Host Bus Interface (Continued)

Ball Name	Ball Attr	Description
HDSTBP[3:0]#	I/O 0.9~1.8V – M	Source synchronous data strobe used to latch data at falling edge HD[15:0]#, DBI0# are latched by HDSTBP0# HD[31:16]#, DBI1# are latched by HDSTBP1# HD[47:32]#, DBI2# are latched by HDSTBP2# HD[63:48]#, DBI3# are latched by HDSTBP3#
HDSTBN[3:0]#	I/O 0.9~1.8V– M	Source synchronous data strobe used to latch data at falling edge HD[15:0]#, DBI0# are latched by HDSTBN0# HD[31:16]#, DBI1# are latched by HDSTBN1# HD[47:32]#, DBI2# are latched by HDSTBN2# HD[63:48]#, DBI3# are latched by HDSTBN3#
HCOMP_N	I M	GTL N-MOS Compensation Input
HCOMP_P	I M	GTL P- MOS Compensation Input
HVREF[4:0] HCOMPVREF_N	I M	AGTL+ I/O reference voltage

MuTIOL® 1G Interface

Pin Name	Pin Attr	Description
ZCLK	I 3.3V - M	SiS MuTIOL ? ?G clock
ZUREQ/ZDREQ	I/O 1.8V - M	SiS MuTIOL ? ?G Control pins
ZSTB[1:0]	I/O 1.8V - M	SiS MuTIOL ? ?G Strobe
ZSTB[1:0]#	I/O 1.8V - M	Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	Address/Data/DBI Pins
ZVREF	I M	SiS MuTIOL ? ?G Reference Voltage
ZCMP_N	I M	N-MOS Compensation Input
ZCMP_P	I M	P-MOS Compensation Input

DRAM Controller

Ball Name	Ball Attr	Description
DRAMTEST	I 2.5V - M	Test Clock Input
FWDSDCLKO	O 2.5V – M	SDRAM Forward Clock Output
MA[14:0]	O 2.5V - M	System Memory Address Bus
SRAS#	O 2.5V - M	SDRAM Row Address Strobe
SCAS#	O 2.5V - M	SDRAM Column Address Strobe
SWE#	O 2.5V - M	SDRAM Write Enable
CS[5:0]#	O 2.5V - M	SDRAM Chip Select CS[5:0]# multiplexed with DQS[5:0]
DQM#[7:0]	O 2.5V - M	SDRAM Input/Output Data Mask
DQS[7:0]	I/O 2.5V - M	2.5V - M DDR Data Strobe
MD[63:0]	I/O 2.5V - M	System Memory Data Bus
CKE[5:0]	O 2.5V – AUX	SDRAM Clock Enable
S3AUXSW#	O (open-drain) 2.5V - AUX	Aux power switch for ACPI-S3 state, low active.
DDRVREF[A:B]	I M	DDR I/O Reference Voltage
DDRCOMP_P	I M	P-MOS Compensation Input
DDRCOMP_N	I M	N-MOS Compensation Input

5.2 SiS M661FX (IGUI Host Memory Controller) - 3

AGP Interface

Ball Name	Ball Attr	Description
AGPCLK	I 3.3V – M	AGP Clock
AFRAME#	I/O 1.5V - M	AGP Frame#
AIRDY#	I/O 1.5V - M	AGP Initiator Ready
ATRDY#	I/O 1.5V - M	AGP Target Ready
ASTOP#	I/O 1.5V - M	AGP Stop#
ADEVSEL#	I/O 1.5V - M	AGP Device Select
ASERR#	I 1.5V - M	AGP System Error
AREQ#	I 1.5V - M	AGP Bus Request
AGNT#	O 1.5V - M	AGP Bus Grant
ADBI_LO	I/O 1.5V - M	DBI of AAD[15:0]
AAD[31:0]	I/O 1.5V - M	AGP Address/Data Bus
AC/BE[3:0]#	I/O 1.5V - M	AGP Command/Byte Enable
APAR	I/O 1.5V - M	AGP Parity
ST[2:0]	O 1.5V - M	AGP Status Bus
PIPE#	I 1.5V - M	AGP Pipeline Request in v2.0 DBI of AAD[31:16] in v3.0
SBA[7:0]	I/O 1.5V - M	Side Band Address
RBF#	I 1.5V - M	Read Buffer Full
WBF#	I 1.5V - M	Write Buffer Full

AGP Interface (Continued)

Ball Name	Ball Attr	Description
AD_STB[1:0]	I/O 1.5V - M	AD Bus Strobe
AD_STB[1:0]#	I/O 1.5V - M	AD Bus Strobe Compliment
SB_STB	I 1.5V - M	Side Band Strobe
SB_STB#	I 1.5V - M	Side Band Strobe Compliment
GC_DET#	I 1.5V - M	AGP v3.0 strap
AGPCOMP_P	I M	P-MOS Compensation Input
AGPCOMP_N	I M	N-MOS Compensation Input
AGPVREF	I M	AGP Reference Voltage

Stereo Glasses interface

Ball Name	Ball Attr	Description
CSYNC	O 3.3V - M	Reserved
RSYNC	O 3.3V - M	Reserved
LSYNC	O 3.3V - M	Reserved

5.2 SiS M661FX (IGUI Host Memory Controller) - 4

Digital Video Link Interface

Ball Name	Ball Attr	Description
VBCLK	I 1.8V - M	Channel B/A Clock Input VBCLK multiplexed with SBA0
VBHCLK	O 1.8V - M	VB Programming Interface Clock VBHCLK multiplexed with RBF#
VBCAD	I/O 1.8V - M	VB Programming Interface Data VBCAD multiplexed with AREQ#
VBCTL[1:0]	O 1.8V -M	VB Data Control VBCTL[1:0] multiplexed with AAD[29:28]
VGPIO[3:2]	I/O 1.8V - M	VB GPIO pins VGPIO[3:2] multiplexed with IPE#/WBF#
VBHSYNC	I/O 1.8V - M	Channel B H-Sync VBHSYNC multiplexed with AAD30
VBVSYNC	I/O 1.8V - M	Channel B V-Sync VBVSYNC multiplexed with AAD31
VBDE	I/O 1.8V - M	Channel B Data Valid VBDE multiplexed with AAD27
VBGCLK	I/O 1.8V - M	Channel B Clock Output. This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VBGCLK multiplexed with AD_STB1
VBGCLK#	I/O 1.8V - M	Channel B Differential Clock Output. (To support Chrontel). VBGCLK# multiplexed with AD_STB1#
VBD[11:0]	I/O 1.8V - M	Channel B Data VBD[11:0] multiplexed with AAD
VAHSYNC	I/O 1.8V - M	Channel A H-Sync VAHSYNC multiplexed with AAD18
VAVSYNC	I/O 1.8V - M	Channel A V-Sync VAVSYNC multiplexed with AAD17
VADE	I/O 1.8V - M	Channel A Data Valid VADE multiplexed with AAD16
VAGCLK	I/O 1.8V - M	Channel A Clock Output. This clock is used to trigger dual edge data 1.8V – M transfer. Perfect duty cycle is required. VAGCLK multiplexed with AD_STB0
VAGCLK#	I/O 1.8V - M	Channel A Differential Clock Output. (To support Chrontel). VAGCLK# multiplexed with AD_STB0#
VAD[11:0]	I/O 1.8V - M	Channel A Data VAD[11:0] multiplexed with AAD

Test Mode / Hardware Trap / Power Management

Ball Name	Ball Attr	Description
DLLEN#	I/O 3.3V/5V– M	Hardware Trap pin (refer to section 5)
TRAP2	I 3.3V/5V– AUX	Hardware Trap pin (refer to section 5)
TRAP[1:0]	I 3.3V/5V– M	Hardware Trap pins (refer to section 5)
ENTEST	I 3.3V/5V– M	Test Mode enable pin
TESTMODE[2:0]	I 3.3V/5V– M	Test Mode select pin Nand Tree Test: 100
AUXOK	I 3.3V – AUXI	Auxiliary Power OK : This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PCIRST#	I 3.3V – AUXI	PCI Bus Reset : PCIRST# is supplied from SiS963 MuTIOL ? ?G Media IO.
PWROK	I 3.3V – AUXI	Main Power OK : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

5.2 SiS M661FX (IGUI Host Memory Controller) - 5

VGA interface

Ball Name	Ball Attr	Description
VOSCI	I 3.3V - M	14.318MHzReference Clock Input
HSYNC	O 3.3V – M	Horizontal Sync
VSYNC	O 3.3V - M	Vertical Sync
INTA#	O 3.3V – M	Internal VGA Interrupt Pin
VGPIO[1:0]	I/O 3.3V/5V- M	Internal VGA GPIO pins
VCOMP	AI Analog - M	Compensation Pin
VRSET	AI Analog - M	Reference Resistor
VVBWN	AI Analog - M	Voltage Reference
ROUT	AO Analog - M	Red Signal Output
GOUT	AO Analog - M	Green Signal Output
BOUT	AO Analog - M	Blue Signal Output

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 1

Host Bus Interface

Name	Pin Attr	Description
FERR#	I 0.8V/2.65V -M	**Floating Point Error:** CPU will assert this signal upon a floating point error occurring.
IGNNE#	OD 0.8V/2.65V -M	**Ignore Numeric Error:** IGNNE# is asserted to inform CPU to ignore a numeric error.
NMI	OD 0.8V/2.65V -M	**Non-Maskable Interrupt:** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	OD 0.8V/2.65V -M	**Interrupt Request:** High-level voltage of this signal conveys to CPU that there is outstanding interrupt(s) needed to be serviced.
APICD1 / GPIOFF# APICD0 / THERM2#	I/OD I I/OD I 0.8V/2.65V -M	**APIC Data: APICD[1:0]** These two signals are used to send and receive APIC data. **GPIO OFF:** Turn off the system when input a low level signal. **Thermal 2:** Assert a SMI#/SCI# when input a low level signal.
CPUSLP#	OD 0.8V/2.65V -M	**CPU Sleep:** The CPUSLP# can be used to force CPU enter the Sleep state.
STPCLK#	OD 0.8V/2.65V -M	**Stop Clock:** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	OD 0.8V/2.65V -M	**System Management Interrupt:** SMI# will be asserted when a pre-defined power management event occurs.
INIT#	OD 0.8V/2.65V -M	**Initialization:** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium III platform it is active high. This signal requires an external pull-up resistor tied to VTT.
APICCK/ LDTREQ# / AGPBUSY#	I 2.5V/3.3V -M	**APIC Clock:** This signal is used to determine when valid data is being sent over the APCI bus. **LDTREQ# / AGPBUSY# (LDTREQ# for K8 use only)** When a low active signal inputs, it will wake up system from C3/S1.
A20M#	OD 0.8V/2.65V- M	**Address 20 Mask:** When A20M# is asserted, the CPU A20 signal will be forced to “0”

MuTIOL 1G Connect Interface

Name	Pin Attr	Description
ZCLK	I 3.3V - M	MuTIOL 1G I/O Connect Clock
ZUREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZDREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZSTB[1:0]	I/O 1.8V - M	MuTIOL 1G I/O Connect Strobe
ZSTB[1:0]#	I/O 1.8V - M	MuTIOL 1G Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	MuTIOL 1G Address/Data pins
ZVREF	I -M	MuTIOL 1G I/O reference voltage
ZCMP_N	I -M	MuTIOL 1G N-MOS Compensation Input
ZCMP_P	I -M	MuTIOL 1G P-MOS Compensation input

LPC Interface

Name	Pin Attr	Description
LAD[3:0]	I/O 3.3V/5V-M	**LPC Address/Data Bus:** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	I 3.3V/5V-M	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LDRQ1# (GPIO1)	I 3.3V/5V-M	**LPC DMA Request 1:** This pin is used by LPC device to request DMA cycle.
LFRAME#	O 3.3V -M	**LPC Frame:** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	I/O 3.3V/5V -M	**Serial IRQ:** This signal is used as the serial IRQ line signal.

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 2

PCI Interface

Name	Pin Attr	Description
PCICLK	I 3.3V/5V -M	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS963L. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O 3.3V/5V -M	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS963L is a PCI bus master and inputs when it is a PCI slave.
PLOCK#	I/O 3.3V/5V -M	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS963L considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
AD[31:0]	I/O 3.3V/5V -M	**PCI Address /Data Bus:** In address phase: 1.When the SiS963L is a PCI bus master, AD[31:0] are output signals. 2.When the SiS963L is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS963L is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS963L is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O 3.3V/5V -M	**Parity:** SiS963L drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
IRDY#	I/O 3.3V/5V -M	**Initiator Ready:** IRDY# is an output when the SiS963L is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS963L is a PCI slave, IRDY# is an input pin.

PCI Interface (Continued)

Name	Pin Attr	Description
FRAME#	I/O 3.3V/5V -M	**Frame#:**FRAME# is an output when the SiS963L is a PCI bus master. The SiS963L drives FRAME# to indicate the beginning and duration of an access. When the SiS963L is a PCI slave device, FRAME# is an input signal.
TRDY#	I/O 3.3V/5V -M	**Target Ready:** TRDY# is an output when the SiS963L is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS963L is a PCI master, it is an input pin.
STOP#	I/O 3.3V/5V -M	**Stop#:**STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	I/O 3.3V/5V -M	**Device Select:** As a PCI target, SiS963L asserts DEVSEL# by doing positive or subtractive decoding. SiS963L positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS963L is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PREQ[4:0]#	I 3.3V/5V -M	**PCI Bus Request:** PCI Bus Master Request Signals
PGNT[4:0]#	O 3.3V –M	**PCI Bus Grant:** PCI Bus Master Grant Signals
PREQ5# / **GPIO5**	I I/O 3.3V/5V- M	**PCI Bus Request:** PCI Bus Master Request Signal

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 3

PCI Interface (Continued)

Name	Pin Attr	Description
PGNT5# / GPIO6	O I/O 3.3V- M	**PCI Bus Grant:** PCI Bus Master Grant Signal
INT[A:D]#	I 3.3V/5V –M	**PCI interrupt A,B,C,D:** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	O 3.3V –M	**PCI Bus Reset:** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	I 3.3V/5V –M	**System Error:** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

Keyboard Controller Interface

Name	Pin Attr	Description
KBDAT (GPIO15)	I/OD 3.3V/5V -AUX	**Keyboard Dada:** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK (GPIO16)	I/OD 3.3V/5V -AUX	**Keyboard Clock:** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT (GPIO17)	I/OD 3.3V/5V -AUX	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal.
PMCLK (GPIO18)	I/OD 3.3V/5V -AUX	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal.

IDE Interface

Name	Pin Attr	Description
IDA[15:0]	I/O 3.3V/5V -M	Primary Channel Data Bus
IDB[15:0]	I/O 3.3V/5V -M	Secondary Channel Data Bus
IDECSA[1:0]#	O 3.3V -M	Primary Channel CS[1:0]
IDECSB[1:0]#	O 3.3V -M	Secondary Channel CS[1:0]
IIOR[A:B]#	O 3.3V -M	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	O 3.3V -M	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	I 3.3V/5V -M	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	O 3.3V -M	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	O 3.3V -M	Primary Channel Address [2:0]
IDSAB[2:0]	O 3.3V -M	Secondary Channel Address [2:0]
CBLID[A:B]	I 3.3V/5V -M	Primary/Secondary Ultra-66 Cable ID

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 4

Power Management Interface

Name	Pin Attr	Description
ACPILED	OD <=5V -AUX	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI# **(GPIO3)**	I I/O 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
PME#	I 3.3V/5V -AUX	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#.
PSON#	OD <=5V -AUX	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
AUXOK	I 3.3V -AUX	**Auxiliary Power OK:** This signal is supplied from the AUX power source. It is also used to reset the logic in AUX power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PWRBTN#	I 3.3V/5V -AUX	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
THERM# **(GPIO2)**	I 3.3V/5V -M	**Thermal Alarm:** When a low active signal inputs, it will assert a SMI#/SCI# event and assert CPU throttling.
EXTSMI# **(GPIO3)**	I 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
CLKRUN# **(GPIO4)**	I/O 3.3V/5V –M	**Clock Run: (for Mobile only)** Used by PCI and LPC peripherals to request the system PCI clock to re-start, or prevent PCI clock stopping. An external pull-up to the MAIN power is required.

Power Management Interface (Continued)

Name	Pin Attr	Description
GPWAK# **(GPIO7)**	I 3.3V/5V -AUX	**General Purpose Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
RING **(GPIO8)**	I 3.3V/5V -AUX	**Ring Indication:** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
AC_SDIN2, 3 **(GPIO9, 10)**	I 3.3V/5V -AUX	**AUDIO Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
STP_PCI# / **AGPSTOP#** **(GPIO11)**	O OD 3.3V/5V –AUX	**Stop PCI Clock: (for Mobile only)** Used to stop the system PCI clock. Used to support PCI CLKRUN# protocol. **AGP Clock Stop: (for Mobile only, if GPIO14 is used to be S3AUXSW#)** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state.
CPUSTP# **(GPIO12)**	OD 1.5V/5V -AUX	**CPU Clock Stop (for Mobile only):** For Intel Mobile processor, this signal can be used to stop the clock to the processor. This signal connected to the DPSLP# signal of Pentium 4 processor that can let the processor enter the Deep Sleep state as well (recommended). For AMD processor, this signal can be to reduce processor voltage during C3/S1 state.
DPRSLPVR **(GPIO13)**	O 3.3V/5V -AUX	**Deeper Sleep (for Mobile only):** Used to lower the voltage of VRM during CPU entered the deeper power saving mode. Because this signal will be at input mode after the Clear RTC operation, an external pulled down resistor is required for this signal. When this signal is high, the voltage regulator outputs the Deeper Sleep voltage. When this signal is low (default), the voltage regulator output the Normal voltage. DPRSLP# can be used to lower the Intel processor voltage during C3/S1 state.
AGPSTOP# / **S3AUXSW#** **(GPIO14)**	OD 3.3V/5V -AUX	**AGP Clock Stop (for Mobile only):** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state. **S3AUXSW#:(for SiS755 and SiSR658 use only)** The signal will keep low in S3 state.

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 5

Power Management Interface (Continued)

Name	Pin Attr	Description
VR_HILO# (GPIO15)	O 3.3V/5V -AUX	**Voltage Regulator HI / LO (for Mobile only):** This ping is used to select an appropriate VID for voltage regulator. A low level indicates the Battery Optimal mode. A high level indicates the Maximum Performance mode.
LO_HI# (GPIO16)	OD 1.5V/5V -AUX	**LO_HI# (for Mobile only):** This pin is connected to the processor. A high level indicates the Battery Optimal mode. A low level indicates the Maximum Performance mode.
VGATEM# (GPIO17)	OD 1.5V/5V -AUX	**VGATEM# (for Mobile only):** Output pin, it is used to mask the PWRGOOD of processor core voltage regulator.
RTC32KHZ (GPIO18)	O 3.3V/5V -AUX	**RTC32KHz output: (Mobile only)** Support RTC32KHz clock output in S0~S5.
THERM2# (APICD0)	I 0.8V/2.65V -M	**Thermal Alarm2: (GTL level)** When a low active signal inputs, it will assert a SMI#/SCI# event.
GPIOFF# (APICD1)	I 0.8V/2.65V -M	**GPIO OFF: (GTL level)** When a low level signal inputs, it will turn off the system. Then, the system can only be woken up again by PWRBTN#.

General Purpose I/O

Name	Pin Attr	Description
GPIO[6:0]	I/O 3.3V/5V -M	**GPIO:** Can be a General Purpose Input or Output.
GPIO[15:7]	I/O 3.3V/5V - AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[18:16]	O 3.3V/5V – AUX	**GPO:** Can be a General Purpose Output.
GPIO[20:19]	OD 3.3V/5V – AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[24:21]	I 3.3V/5V - AUX	**GPI:** Can be a General Purpose Input.

RTC Interface

Name	Pin Attr	Description
BATOK	I 3.3V -RTC	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	I 3.3V-RTC	**RTC 32.768 KHz Input:** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	O 3.3V -RTC	**RTC 32.768 KHz Output:** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an external oscillator is used.
PWROK	I 3.3V-RTC	**Main Power OK:** A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, PCIRST# will all be asserted until after PWROK goes high for 12 ms.

Hardware Trap Signals

Name	Pin Attr	Description
IPB_OUT0	O 3.3V -AUX	**IPB_OUTO:** Hardware Trap to select MuTIOL 1G clock PLL enable/disable
IPB_OUT1	O 3.3V – AUX	**IPB_OUT1:** Hardware Trap to select MuTIOL 1G operation mode

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 6

AC'97 Interface

Name	Pin Attr	Description
AC_BIT_CLK	I 3.3V/5V -M	**AC'97 Bit Clock:** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	O 3.3V -AUX	**AC'97 Reset:** Hardware reset signal for external Codecs.
AC_SDIN0	I 3.3V/5V -AUX	**AC'97 Serial Data Input :** Serial data input from primary Codec.
AC_SDIN1	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from secondary Codec. When Modem Codec is used, this pin dedicate to Modem Serial data input.
AC_SDIN[3:2] (GPIO[10:9])	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from third and forth Audio Codec.
AC_SDOUT	O 3.3V -M	**AC'97 Serial Data Output:** Serial data output to Codecs.
AC_SYNC	O 3.3V -M	**AC'97 Synchronization:** This is a 48KHz signal, which is used to synchronize the Codecs.

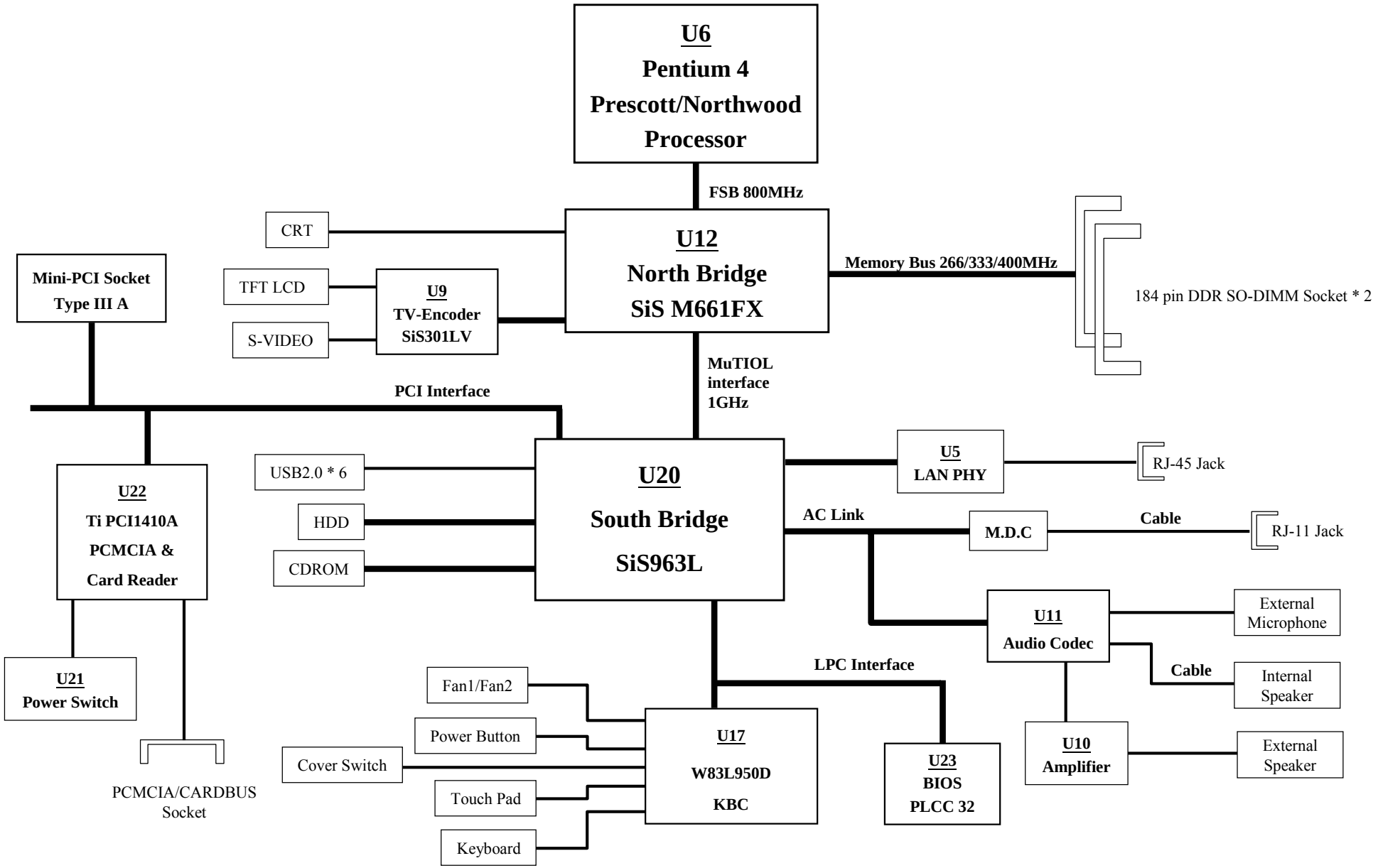
Legacy I/O and Miscellaneous Signals

Name	Pin Attr	Description
SPK	O 3.3V -M	**Speaker output:** The SPK is connected to the system speaker.
ENTEST	I 3.3V/5V -M	SiS963L Test Mode Enable Pin
OSCI	I 3.3V -M	14.318 MHz. Clock In

USB Interface

Name	Pin Attr	Description
OSC12MHI	I 3.3V/5V -AUX	**UTMI 12MHz Clock Input:** This pin provides the 12MHz clock signal input form external crystal or oscillator.
OSC12MHO	O 3.3V/5V -AUX	**UTMI 12Mhz Clock Output:** **This pin should be connected with the other end of the 12Mhz crystal or left unconnected if an external oscillator is used**
USBCLK48M	I 3.3V/5V -M	**USB 48 MHz clock input:** This signal provides the fundamental clock for the USB Controller.
OC[0:5]#	I/O 3.3V/5V - AUX	**USB Port 0-5 Overcurrent Detection:** OC[0:5]# are used to detect the overcurrent condition of USB Ports 0-5.
UV[3,0]+, UV[3,0]-	I/O 3.3V - AUX	**USB Port [3:**0] **Differentia**l: These differential pairs are used to transmit Data/Address /Command signals for ports 3 and 0. (USB controller 0)
UV[4,1]+, UV[4,1]-	I/O 3.3V - AUX	**USB Port [4:1] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 1. (USB controller 1)
UV[5,2]+, UV[5,2]-	I/O 3.3V - AUX	**USB Port [5,2] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 5 and 2. (USB controller 2)
USBREF	I 3.3V – AUX	**USB reference resistor inpu**t: A resistor should be connected to USBVSS from this pin for IO impedance calibration.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot.

7.2 Error Codes (1)

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes (2)

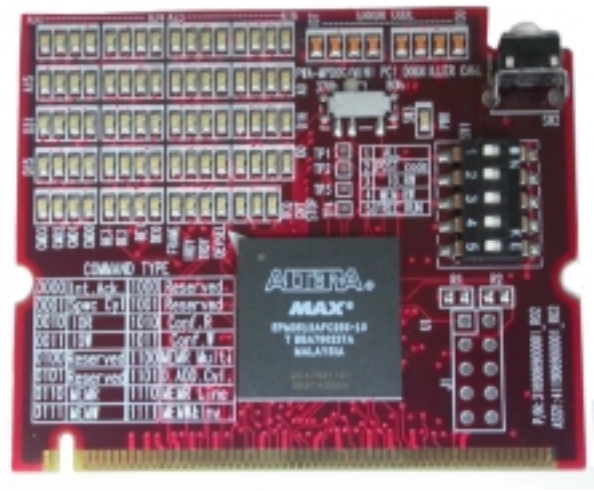
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville CPU init
52h	USB HC init

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 Battery Can not Be Charged
- 8.3 No Display (*2)
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 TV Test Error
- 8.7 Memory Test Error
- 8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.9 Hard Drive Test Error
- 8.10 CD-ROM Driver Test Error
- 8.11 USB Port Test Error
- 8.12 PC Card Socket Test Error
- 8.13 Mini-PCI Socket Test Error
- 8.14 Audio Failure
- 8.15 LAN Test Error

8599 N/B Maintenance

*1: No power definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No display definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

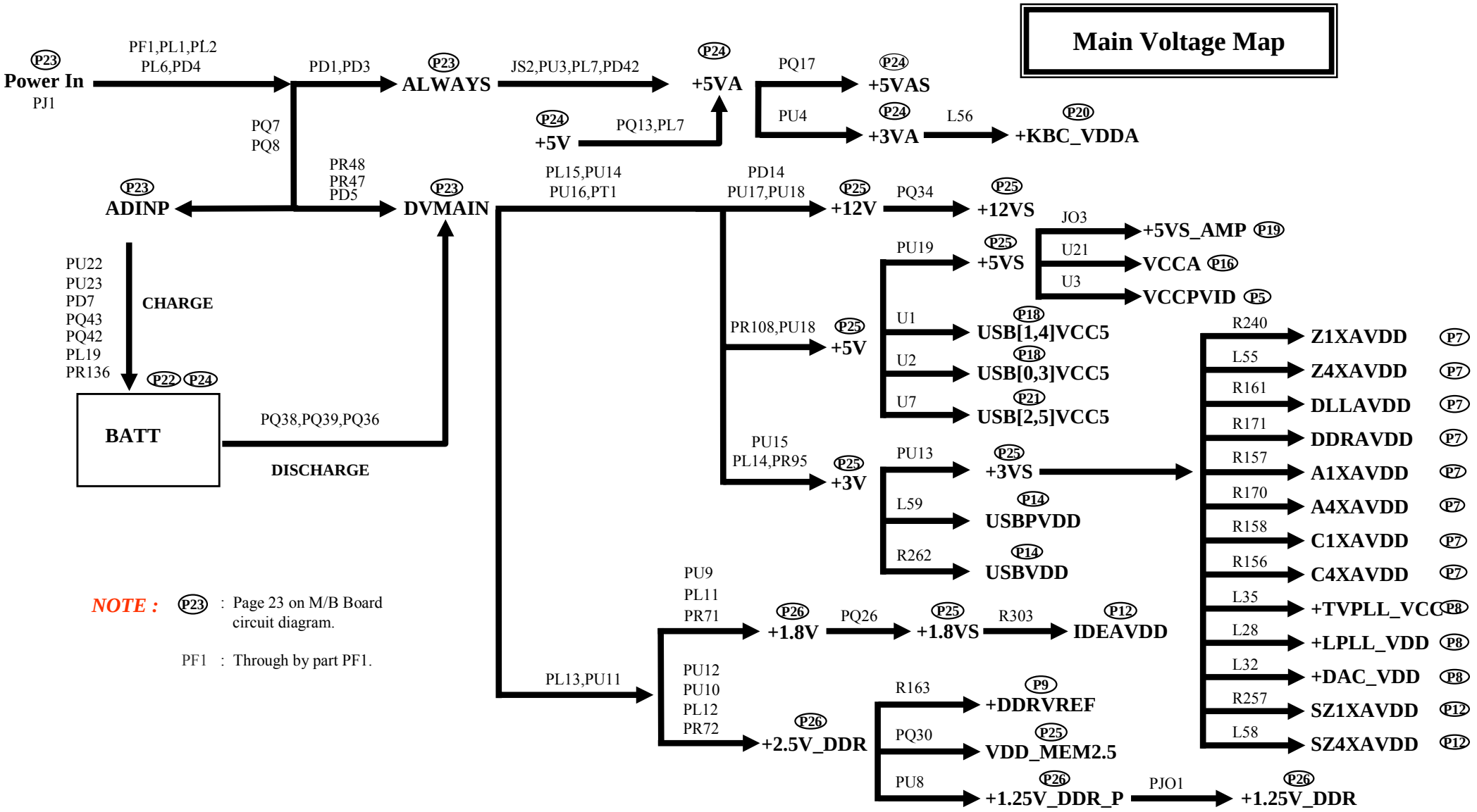
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8.1 No Power (1)

When power button is pressed ,nothing happens ,power indicator does not light up.

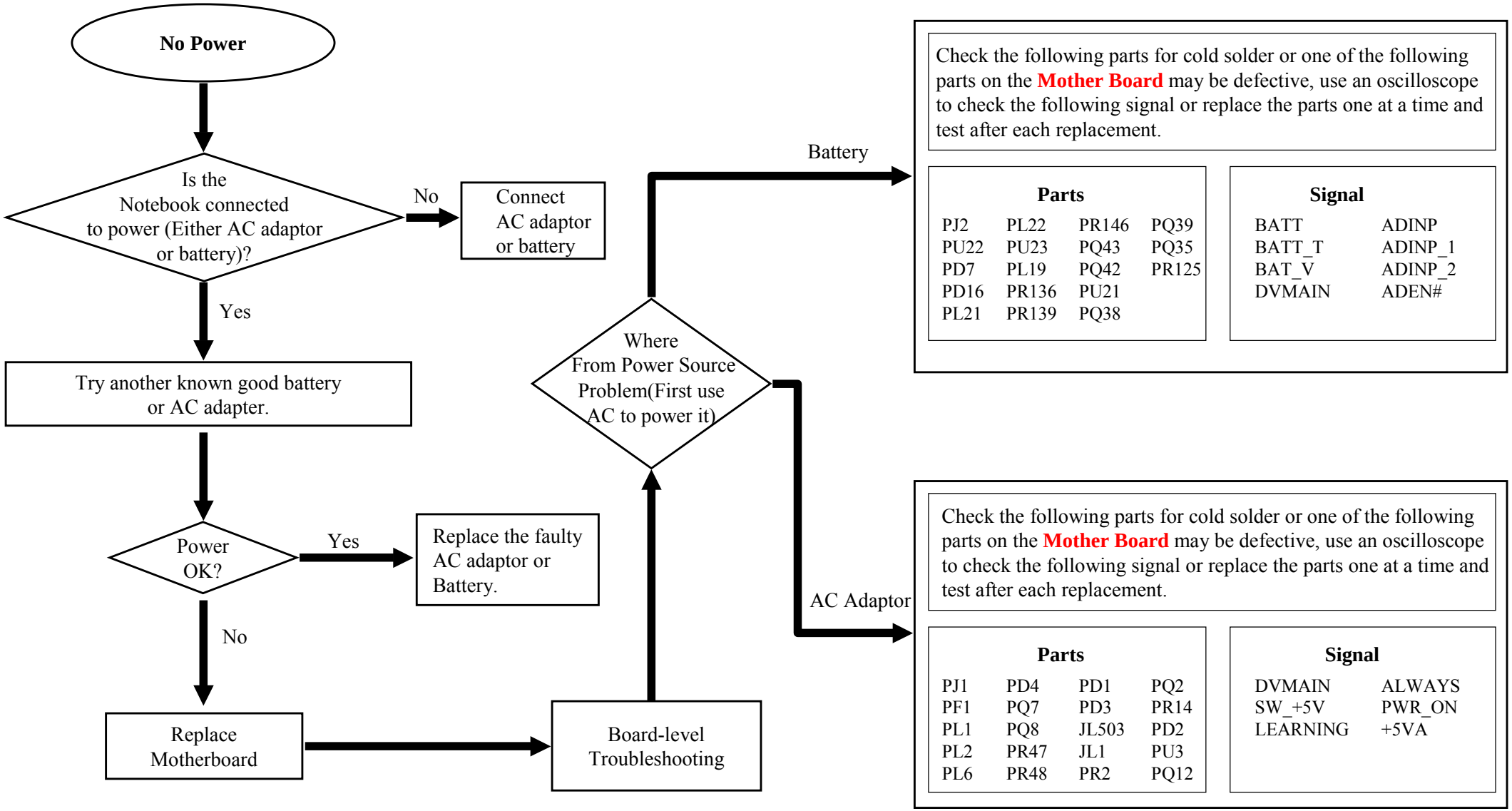


NOTE : P23 : Page 23 on M/B Board circuit diagram.

PF1 : Through by part PF1.

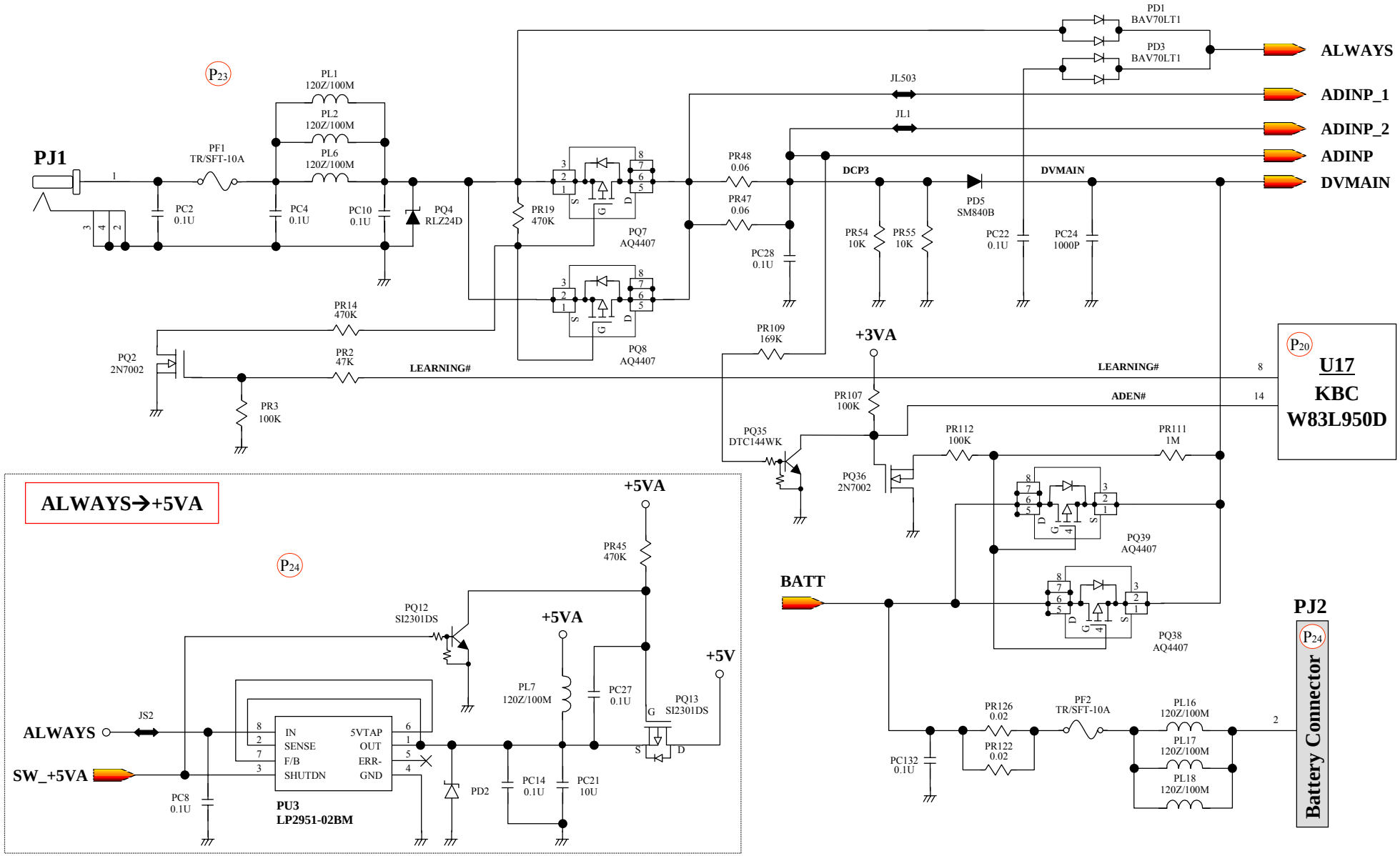
8.1 No Power (2)

When power button is pressed ,nothing happens ,power indicator does not light up.



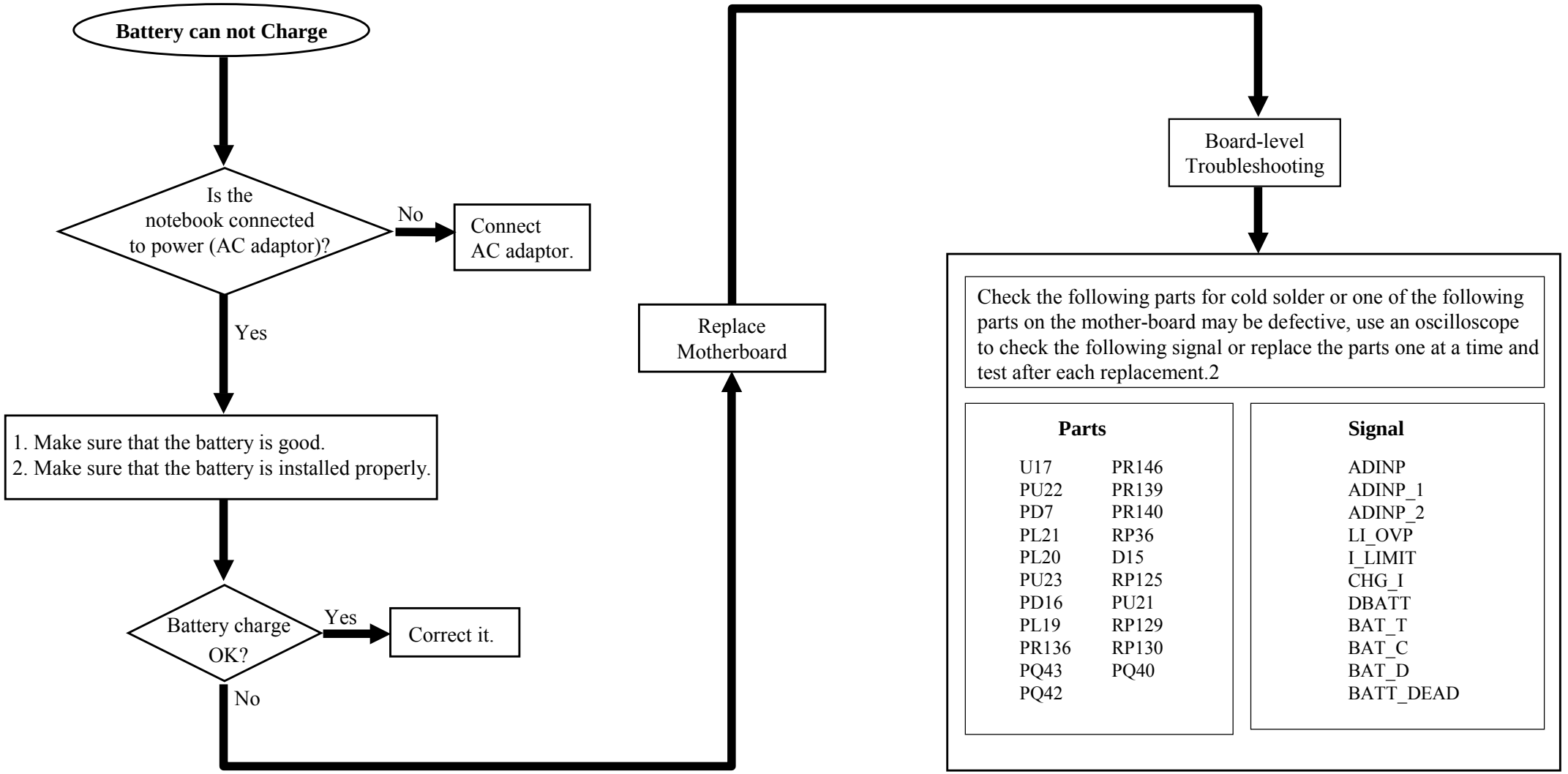
8.1 No Power (3)

When power button is pressed ,nothing happens ,power indicator does not light up.



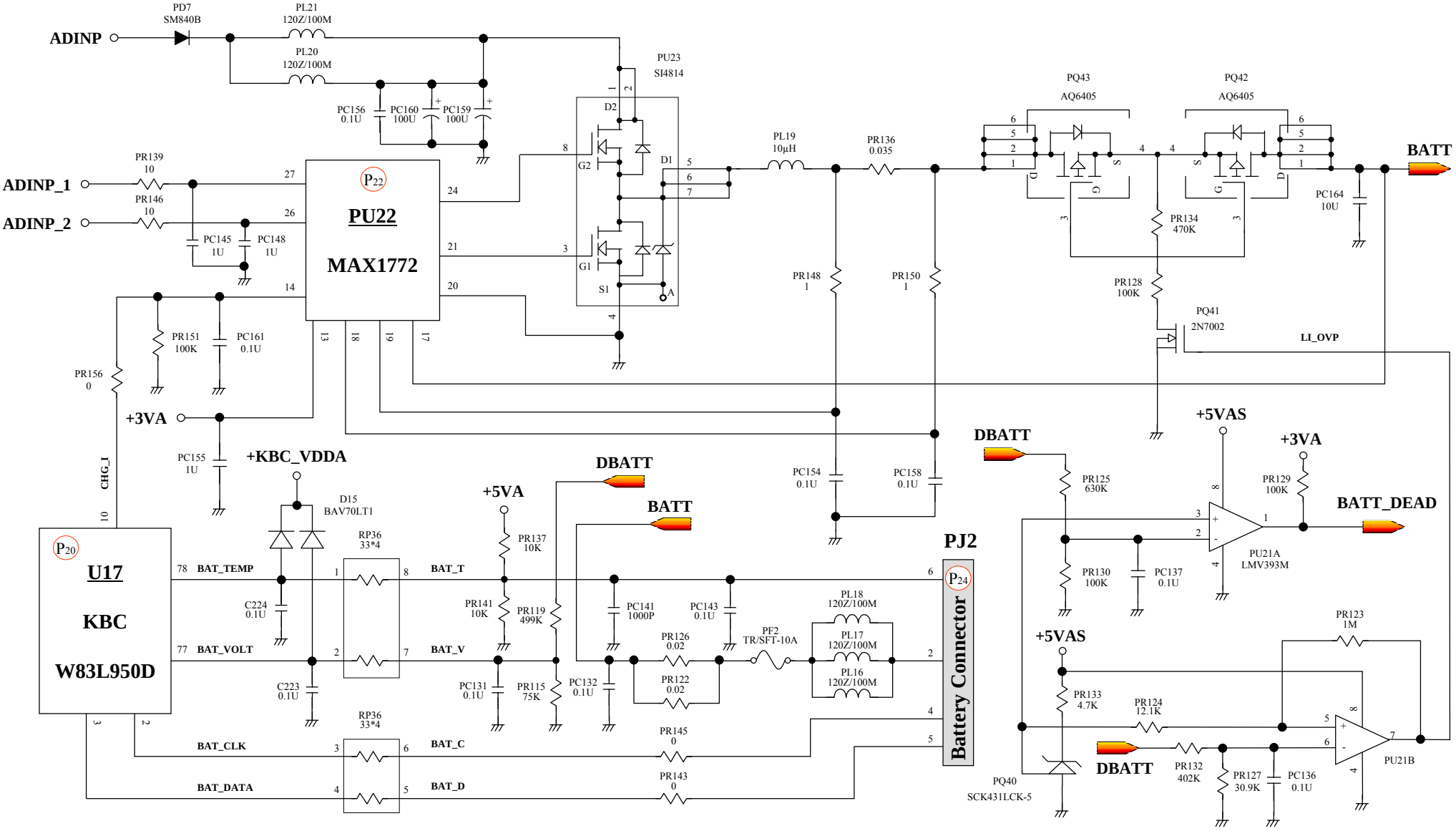
8.2 Battery Can not Be Charged (1)

When the battery is installed but the battery status indicate LED display abnormal.



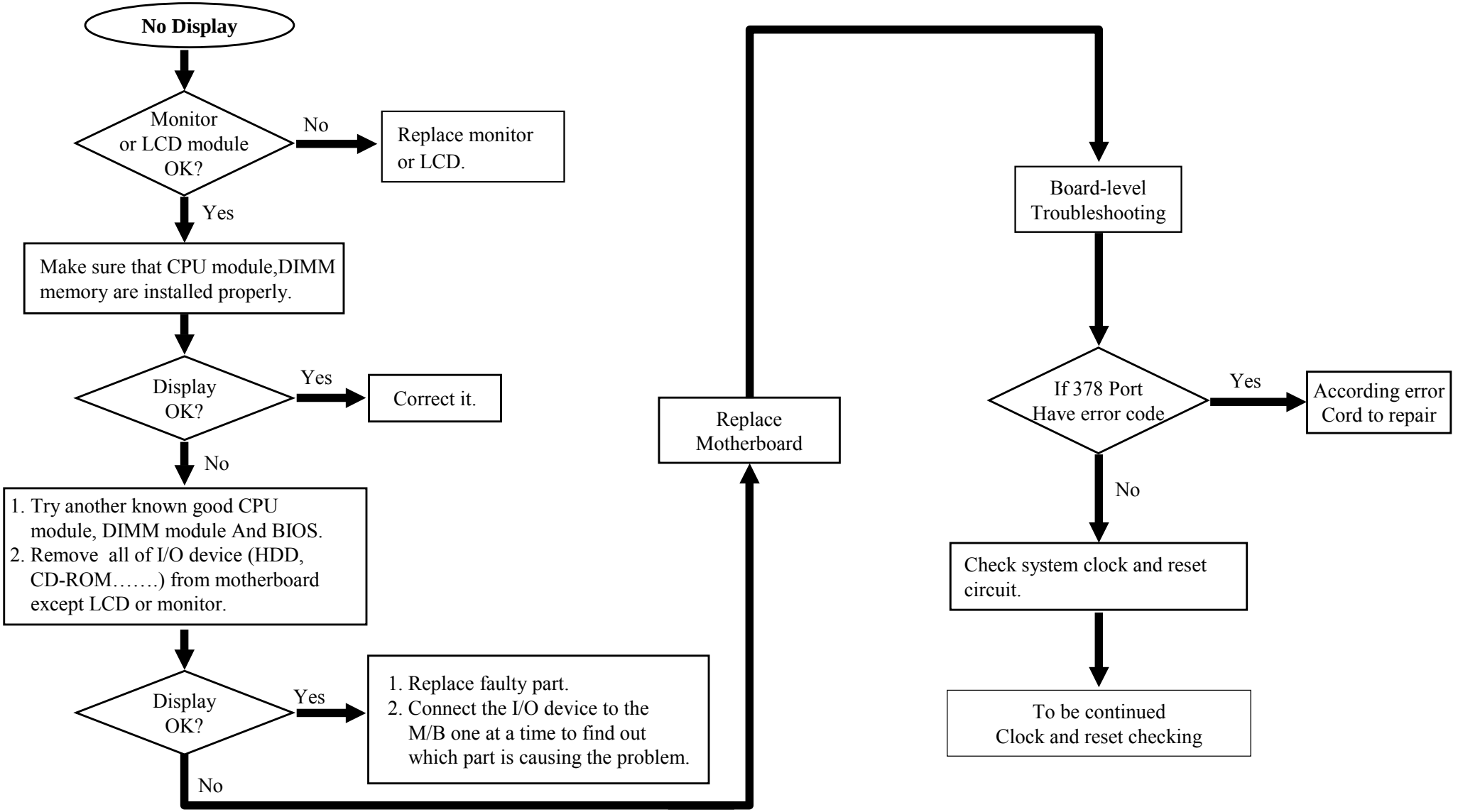
8.2 Battery Can not Be Charged (2)

When the battery is installed but the battery status indicate LED display abnormal.



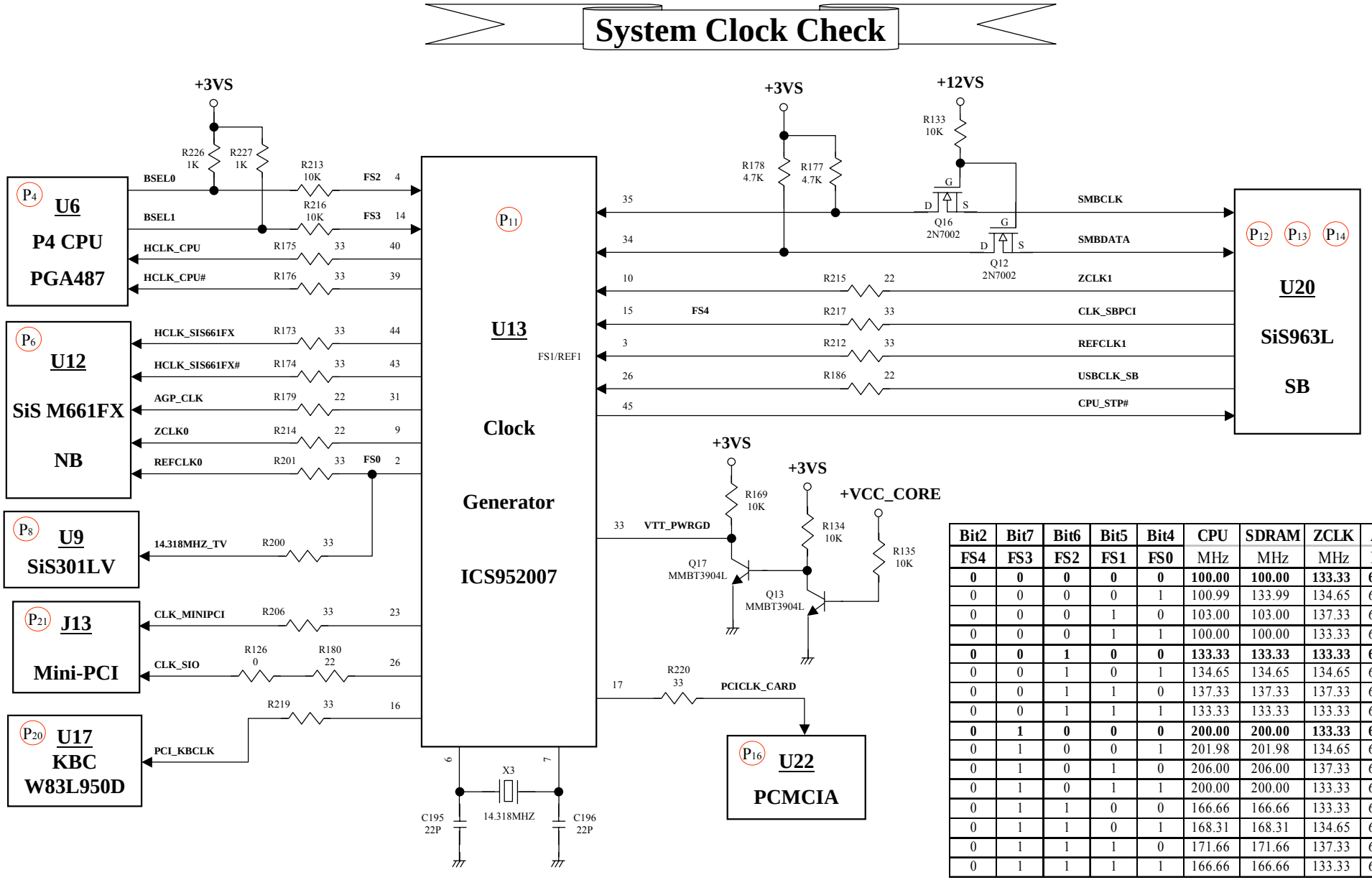
8.3 No Display (1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



8599 N/B Maintenance

8.3 No Display (2)

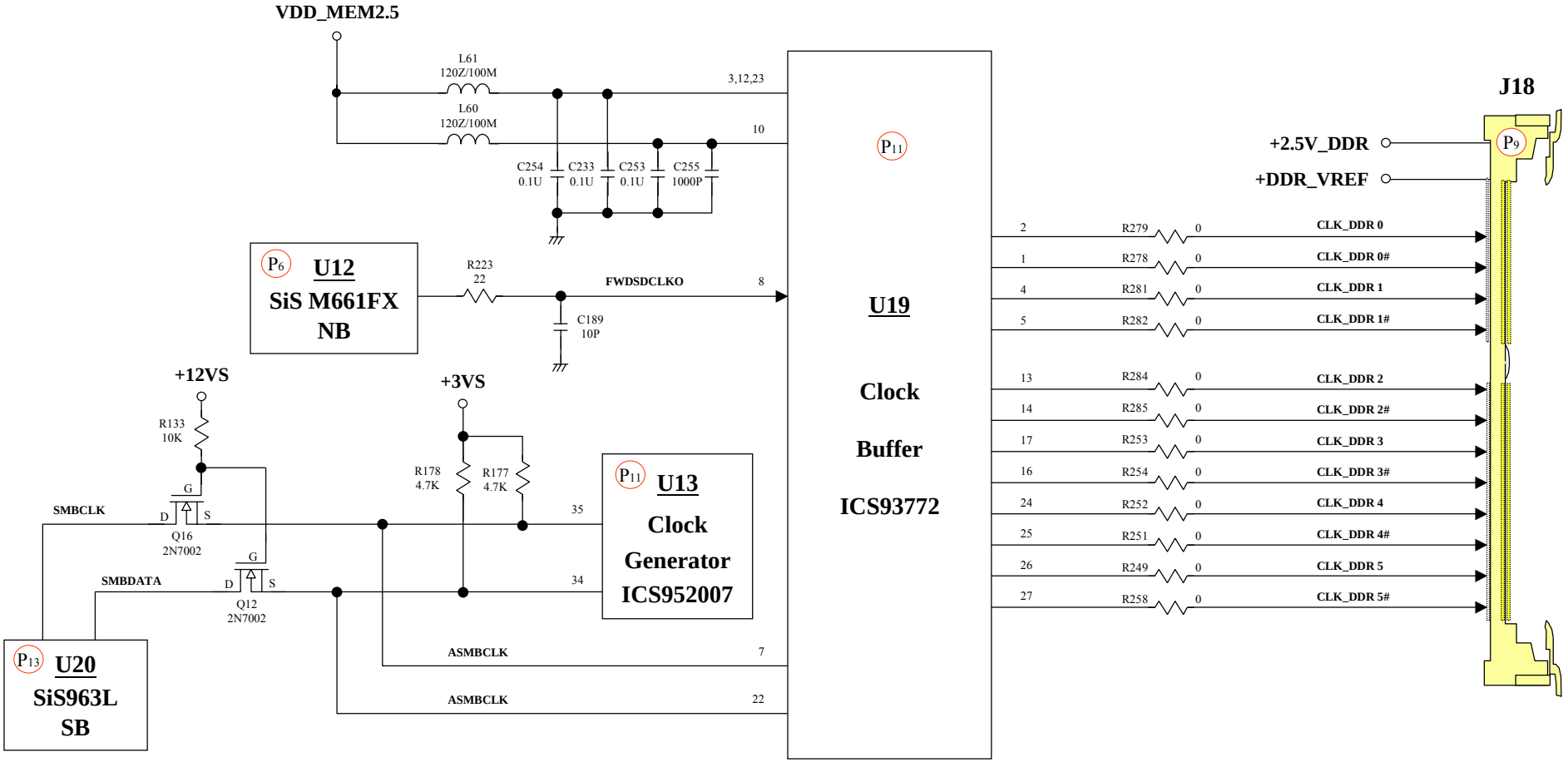


Bit2	Bit7	Bit6	Bit5	Bit4	CPU	SDRAM	ZCLK	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	**0**	**0**	**0**	**0**	**100.00**	**100.00**	**133.33**	**66.66**	**33.33**
0	0	0	0	1	100.99	133.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	66.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	**0**	**1**	**0**	**0**	**133.33**	**133.33**	**133.33**	**66.66**	**33.33**
0	0	1	0	1	134.65	134.65	134.65	67.32	33.66
0	0	1	1	0	137.33	137.33	137.33	68.66	34.33
0	0	1	1	1	133.33	133.33	133.33	66.67	33.33
0	**1**	**0**	**0**	**0**	**200.00**	**200.00**	**133.33**	**66.67**	**33.33**
0	1	0	0	1	201.98	201.98	134.65	67.33	33.66
0	1	0	1	0	206.00	206.00	137.33	68.67	34.33
0	1	0	1	1	200.00	200.00	133.33	66.67	33.33
0	1	1	0	0	166.66	166.66	133.33	66.66	33.33
0	1	1	0	1	168.31	168.31	134.65	67.32	33.66
0	1	1	1	0	171.66	171.66	137.33	68.66	34.33
0	1	1	1	1	166.66	166.66	133.33	66.66	33.33

8599 N/B Maintenance

8.3 No Display (3)

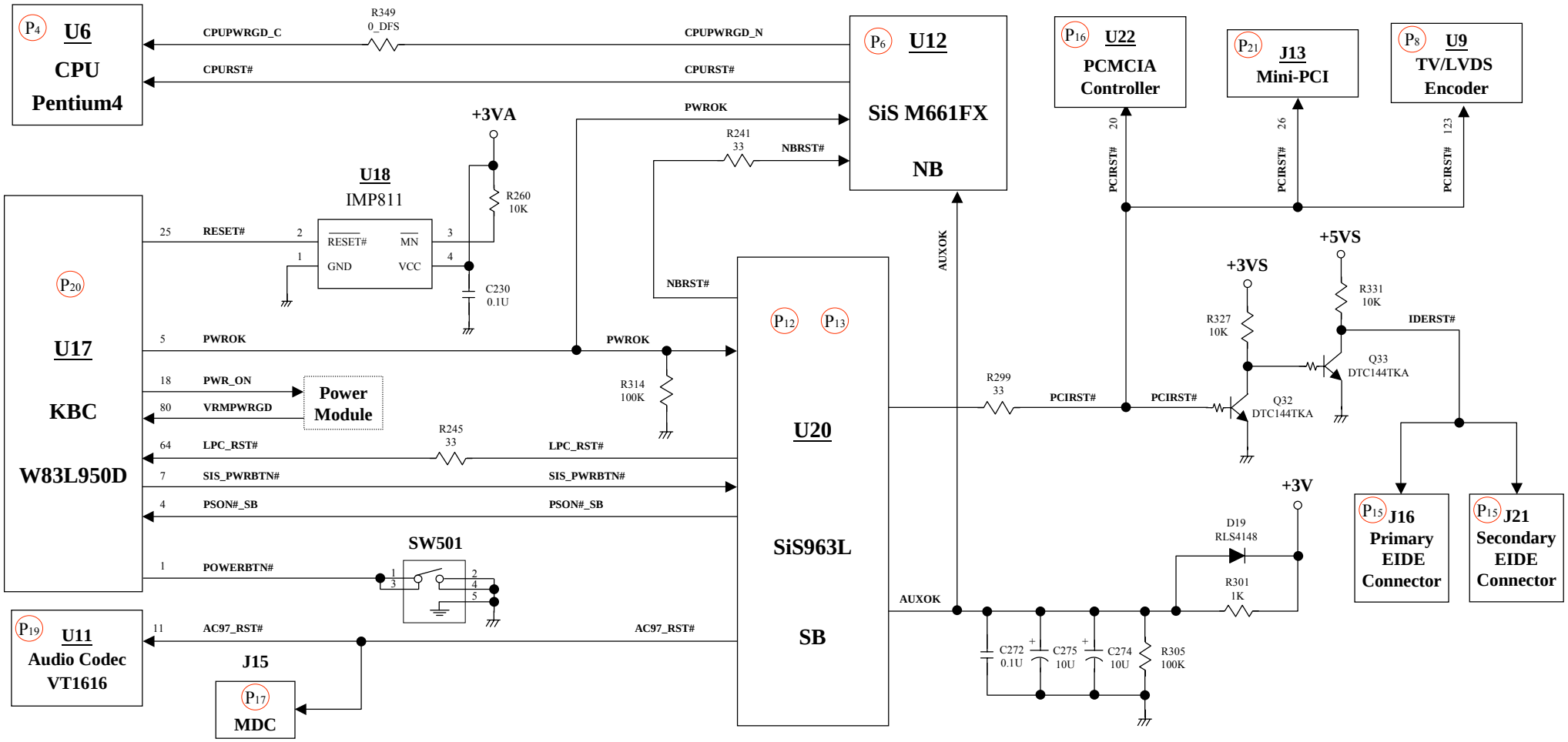
DDR Clock Check



8599 N/B Maintenance

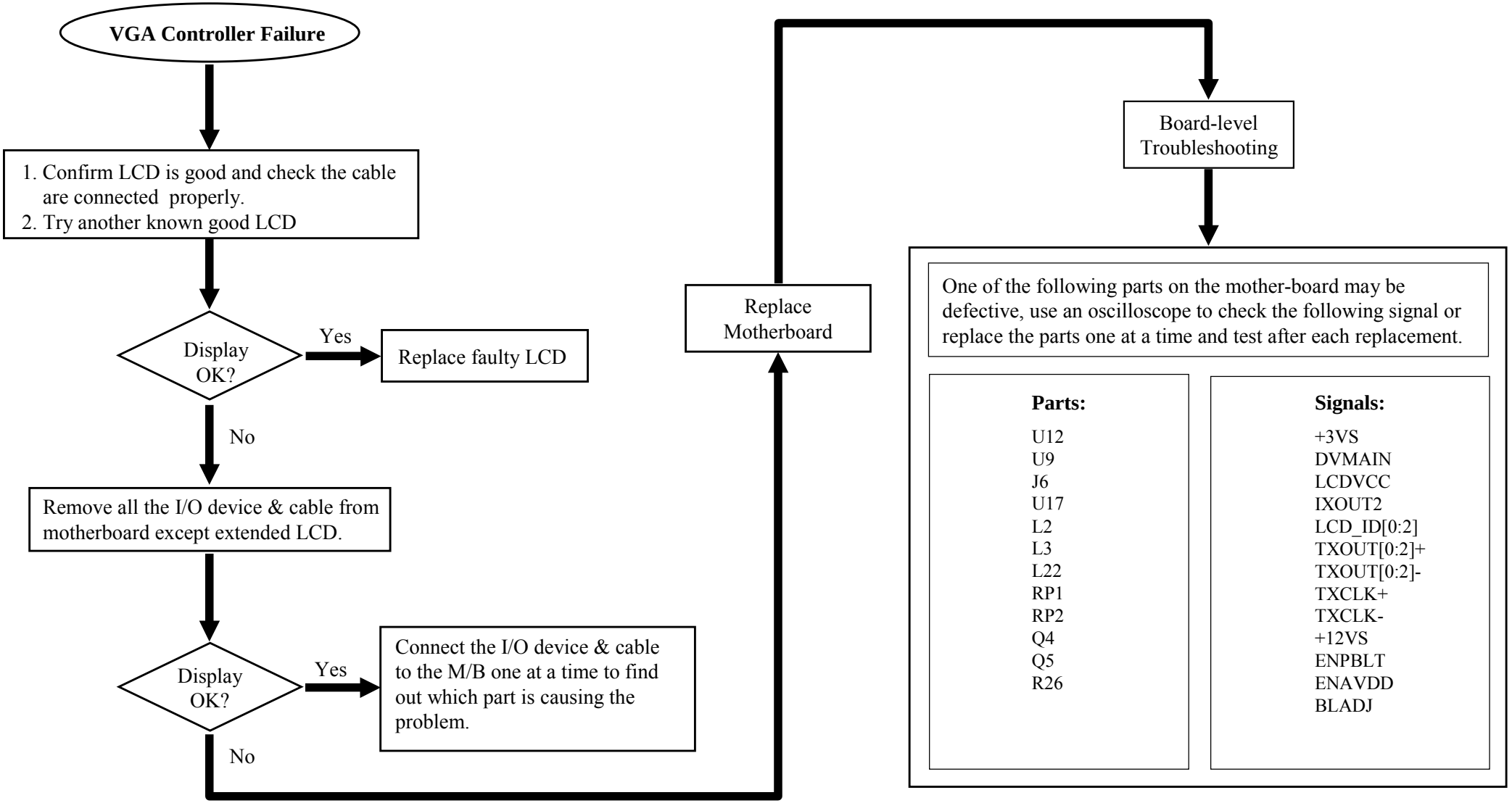
8.3 No Display (4)

System Reset Check



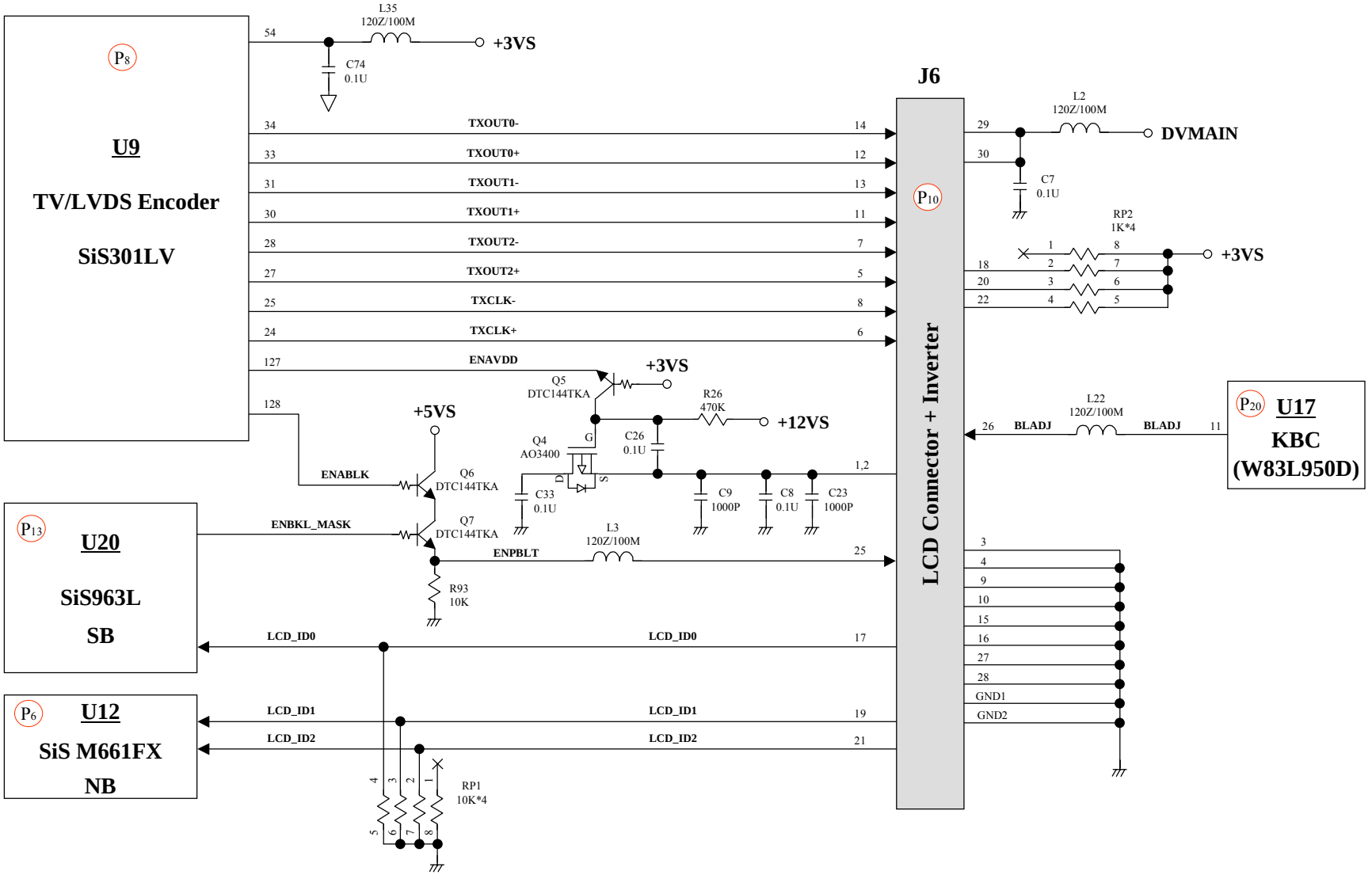
8.4 LCD No Display or Picture Abnormal (1)

There is no display or picture abnormal on LCD or monitor.



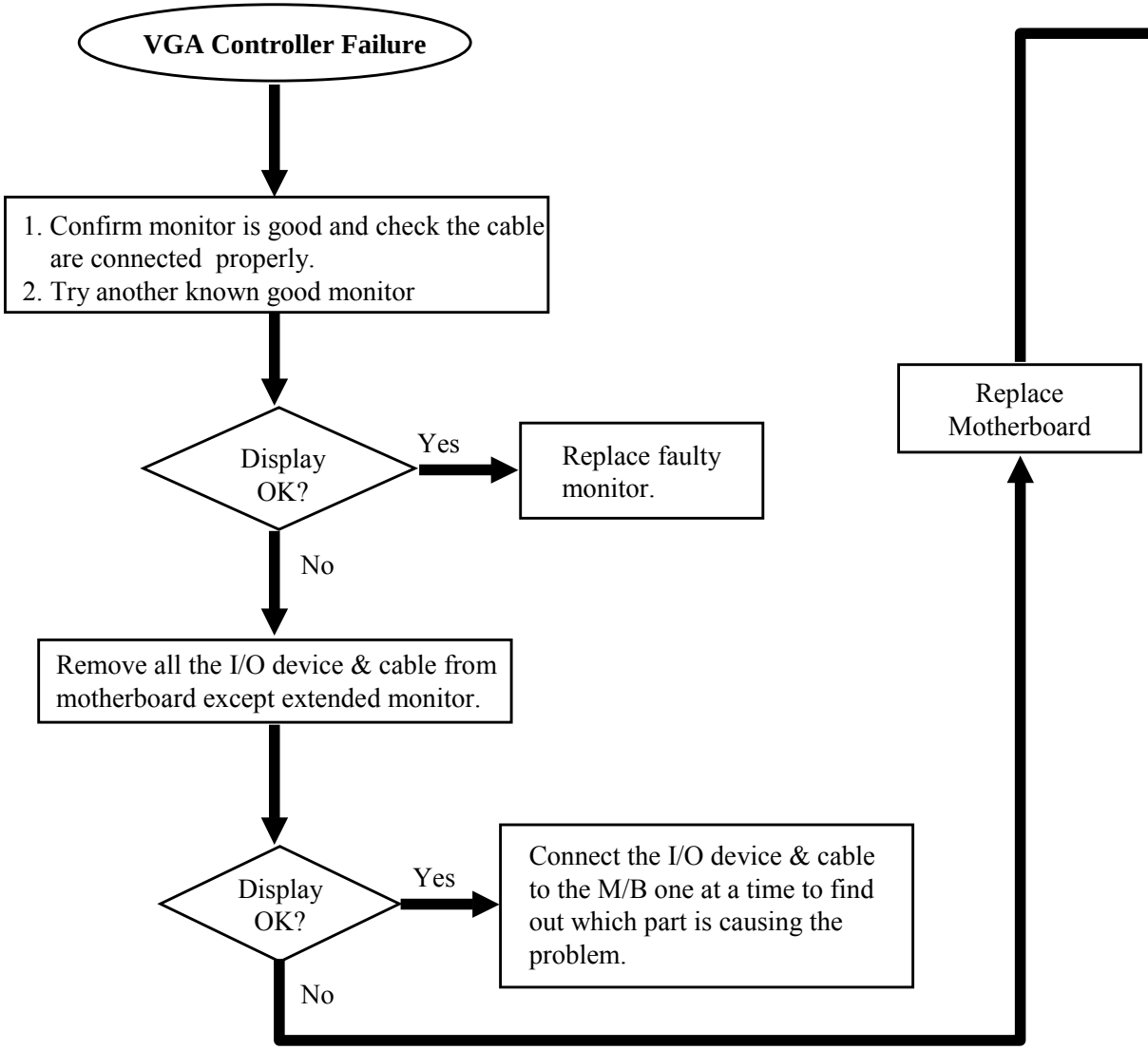
8.4 LCD No Display or Picture Abnormal (2)

There is no display or picture abnormal on LCD or monitor.



8.5 External Monitor No Display or Color Abnormal (1)

There is no display or picture abnormal on monitor.



Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

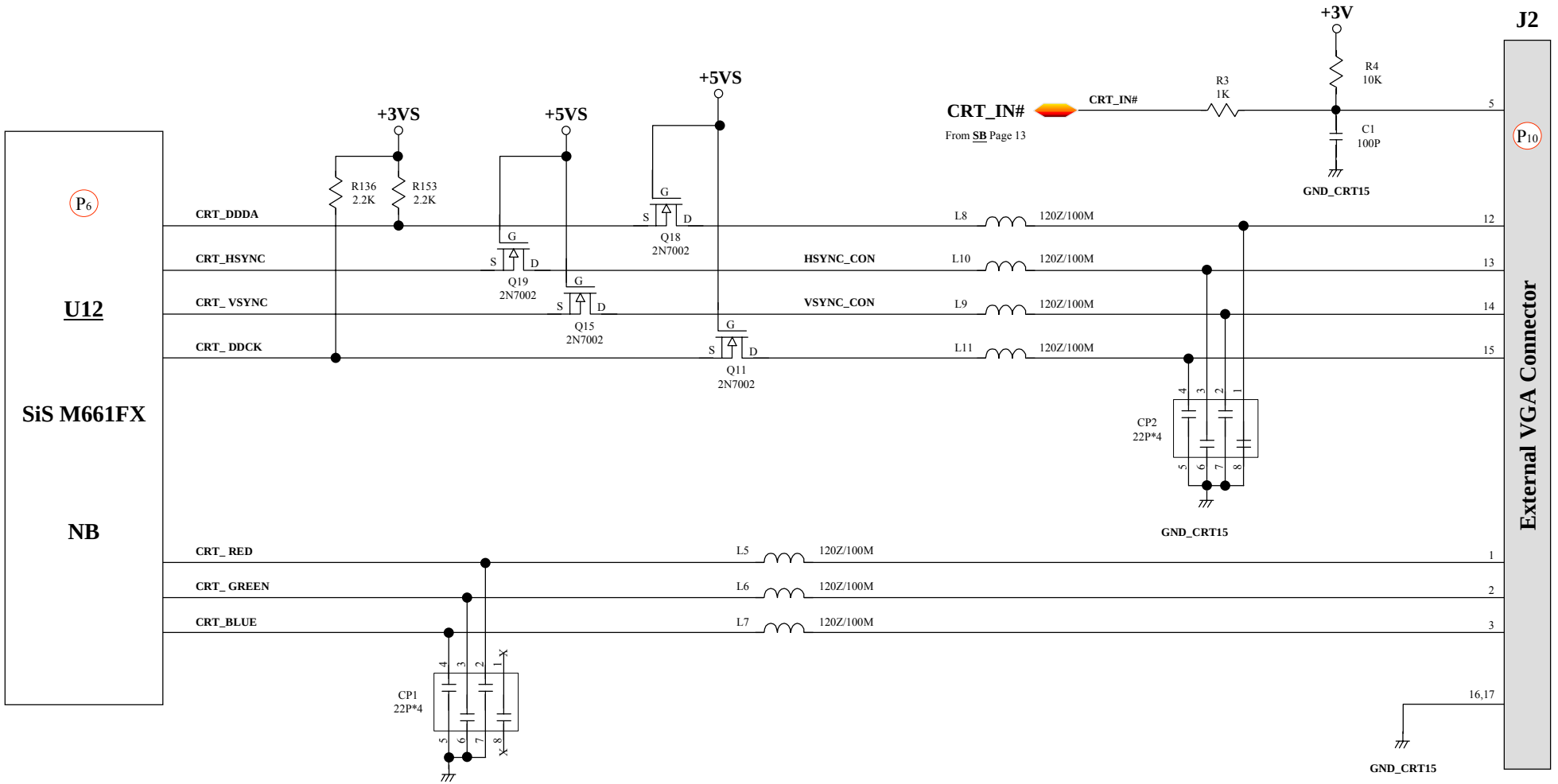
U12	L7
J2	L8
R153	L9
R136	L10
Q18	L11
Q19	R4
Q15	R3
Q11	JL501
L5	JL502
L6	

Signals:

+3VS
+5VS
+3V
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_DDDA
CRT_HSYNC
CRT_VSYNC
CRT_DDCK

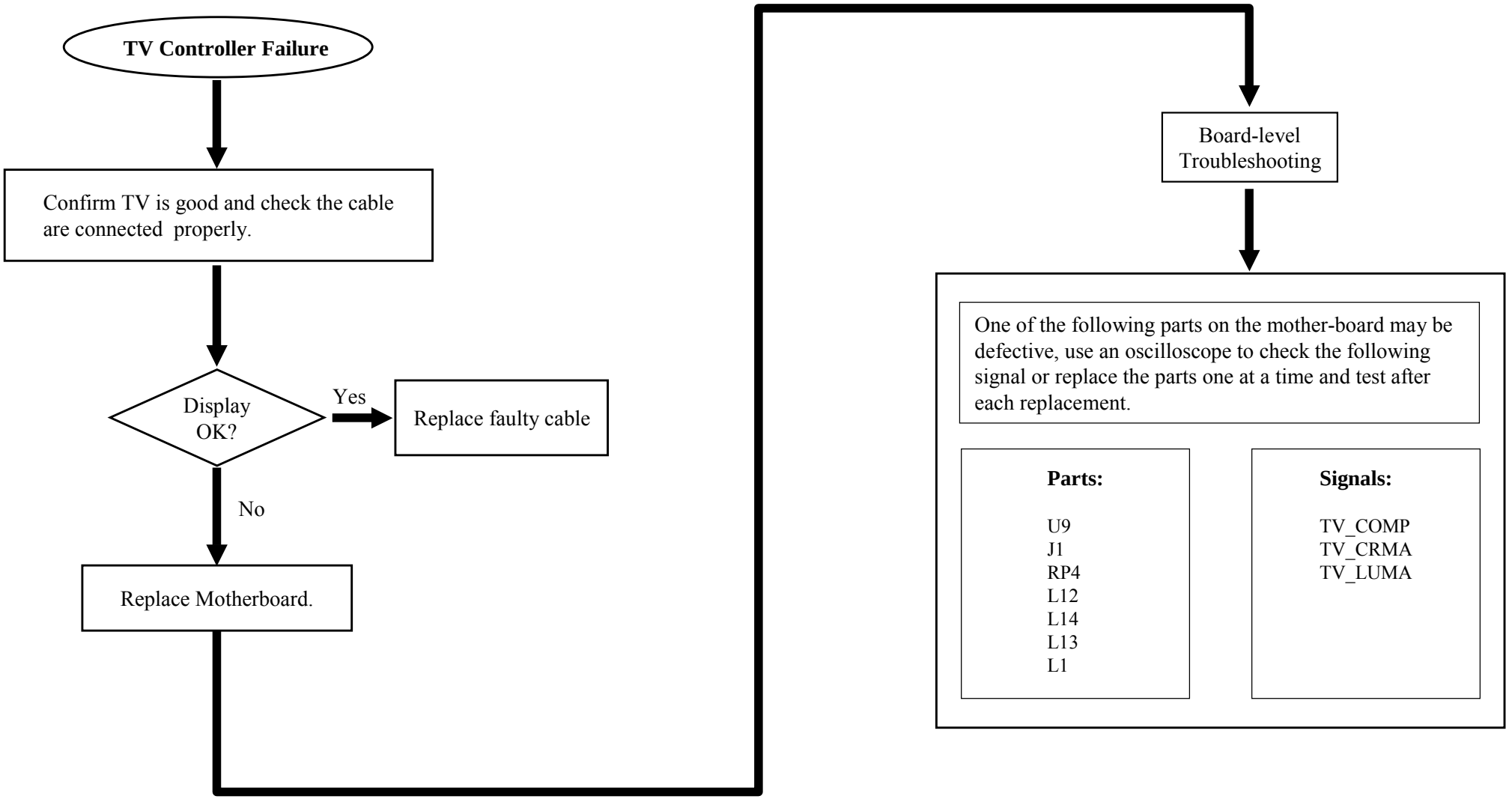
8.5 External Monitor No Display or Color Abnormal (2)

There is no display or picture abnormal on monitor.



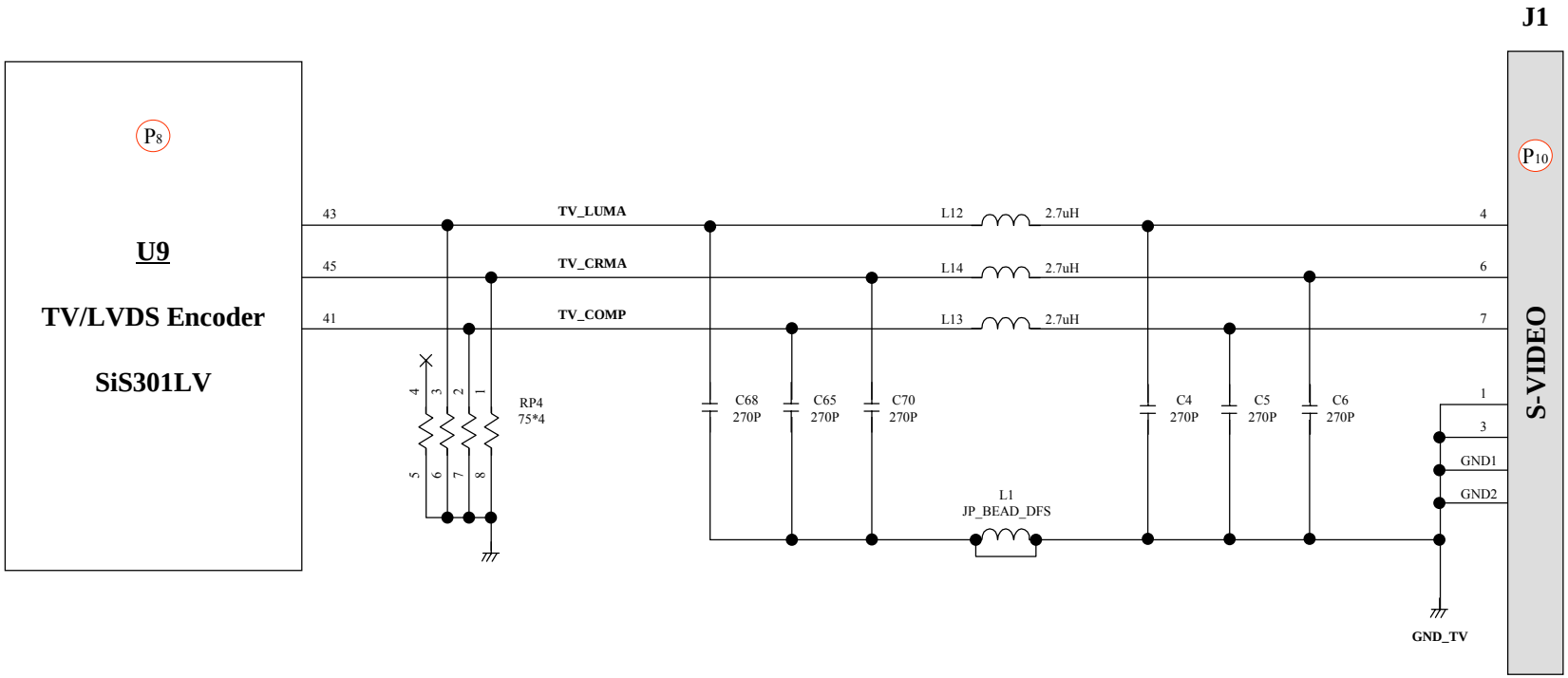
8.6 TV Test Error (1)

There is no display or picture abnormal on TV.



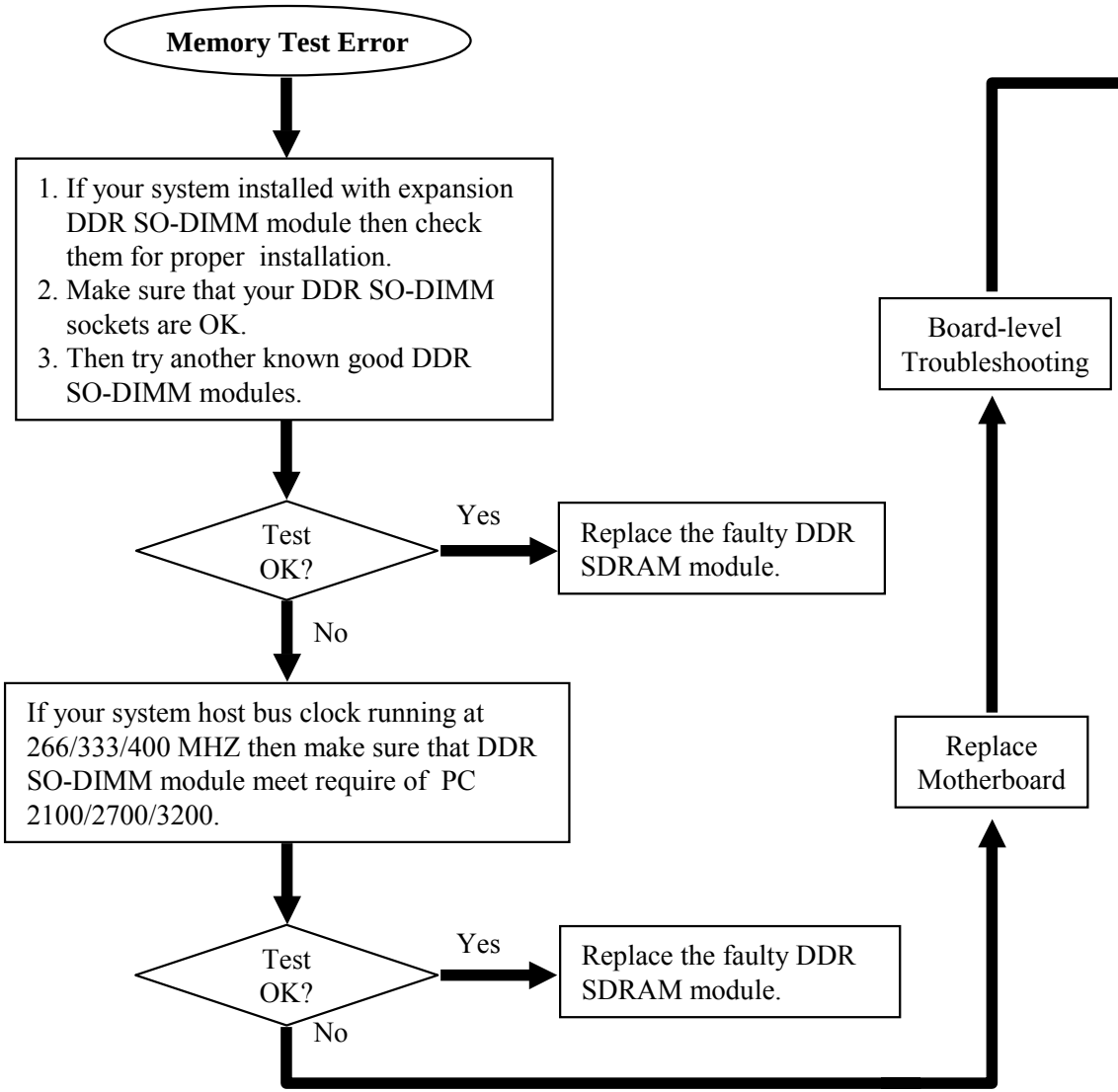
8.6 TV Test Error (2)

There is no display or picture abnormal on TV.



8.7 Memory Test Error (1)

Extend DDRAM is failure or system hangs up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

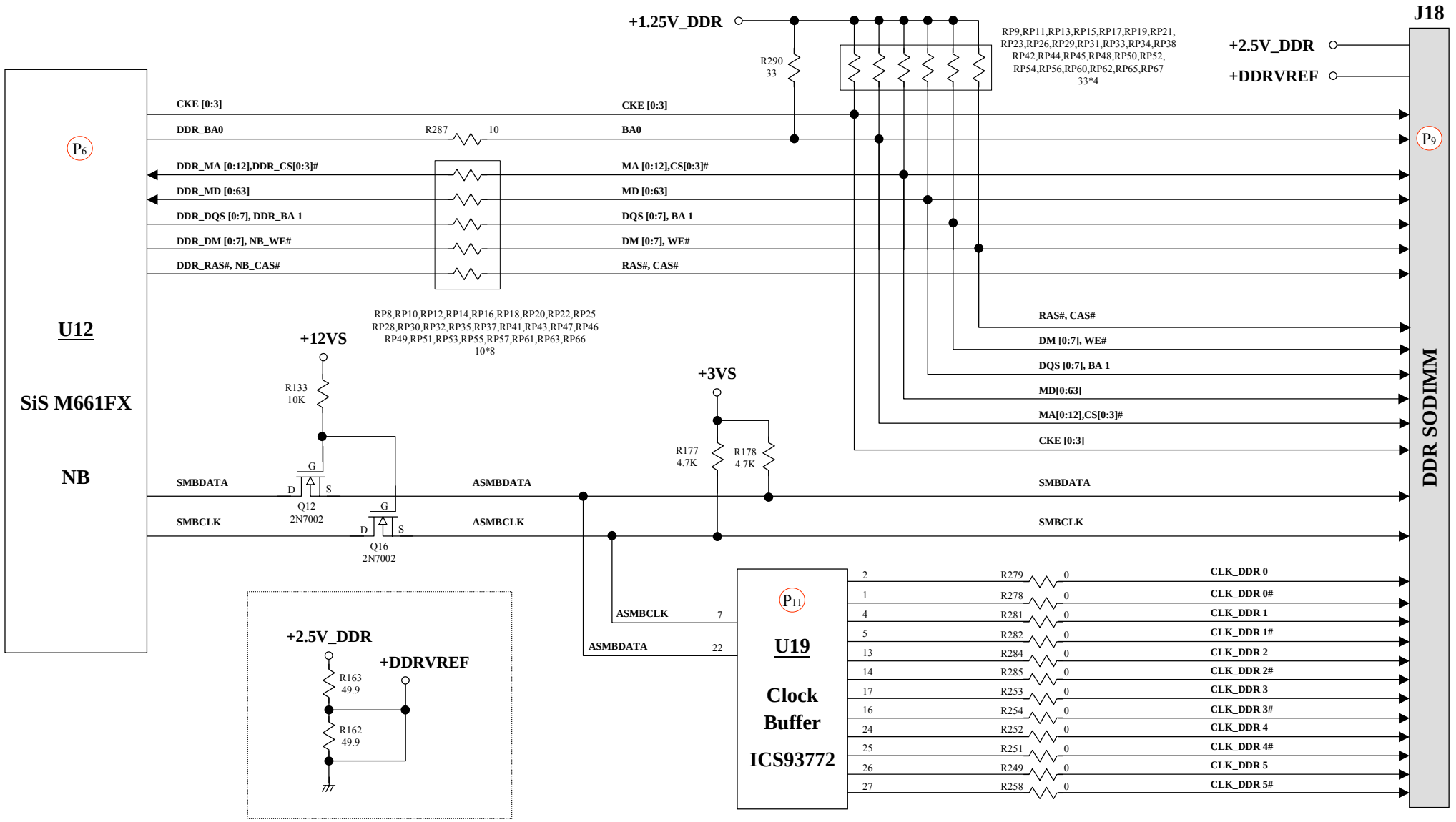
U12
U19
U13
J18
R287
R133
Q12
Q16
R251~R254
R49
R58

Signals:

+1.25V_DDR	DDR_RAS#
+2.5V_DDR	DDR_CAS#
+DDR_VREF	DDR_WE#
DDR_CKE [0:3]	SMBDATA
DDR_CS[0:3]#	SMBCLK
DDR_MA [0:12]	HCLK_SISM661FX
DDR_MD [0:63]	HCLK_SISM661FX#
DDR_DQS [0:7]	CLK_DDR [0:5]
DDR_BA [0,1]	CLK_DDR [0:5]#
DDR_DQM [0:7]	

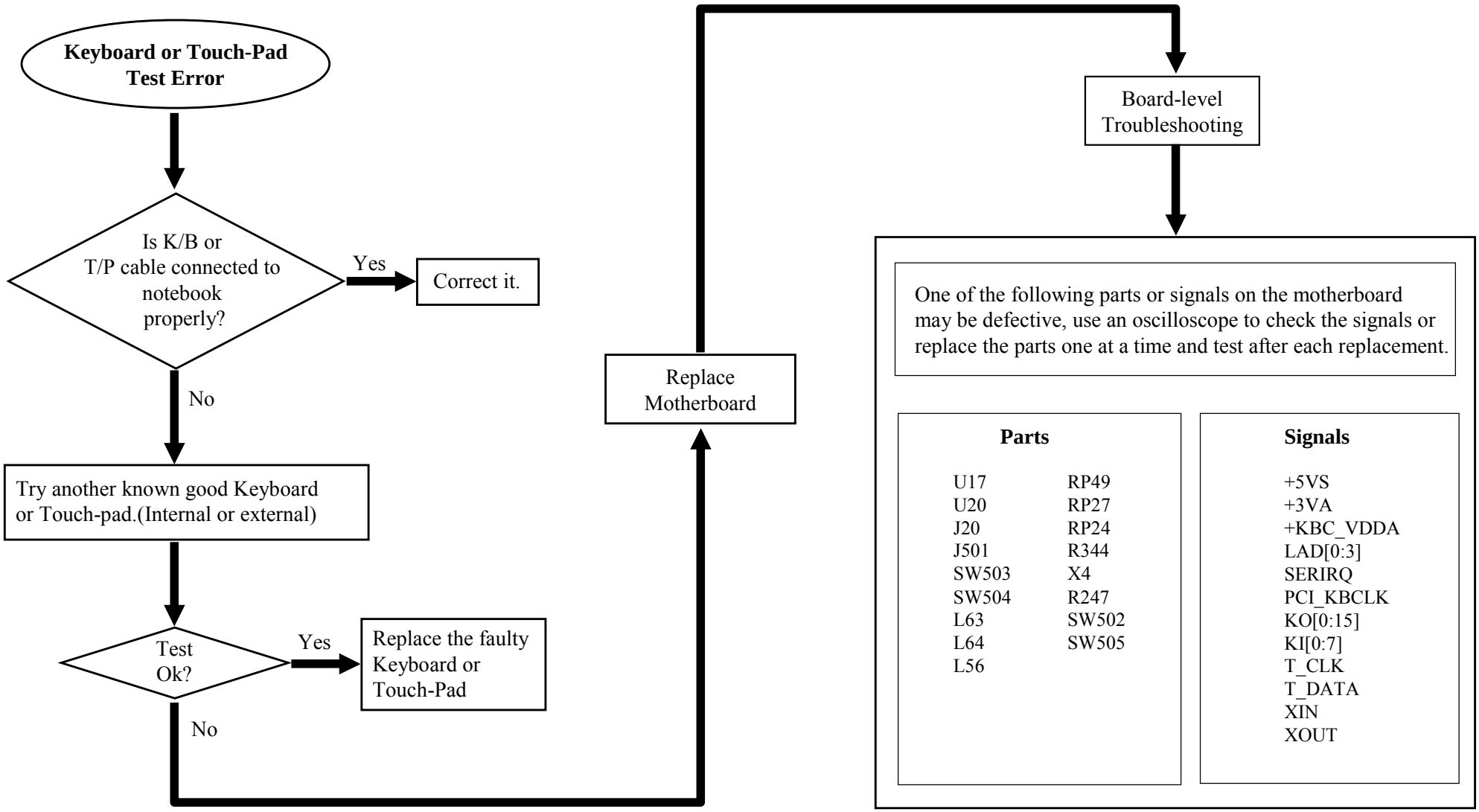
8.7 Memory Test Error (2)

Extend DDRAM is failure or system hangs up.



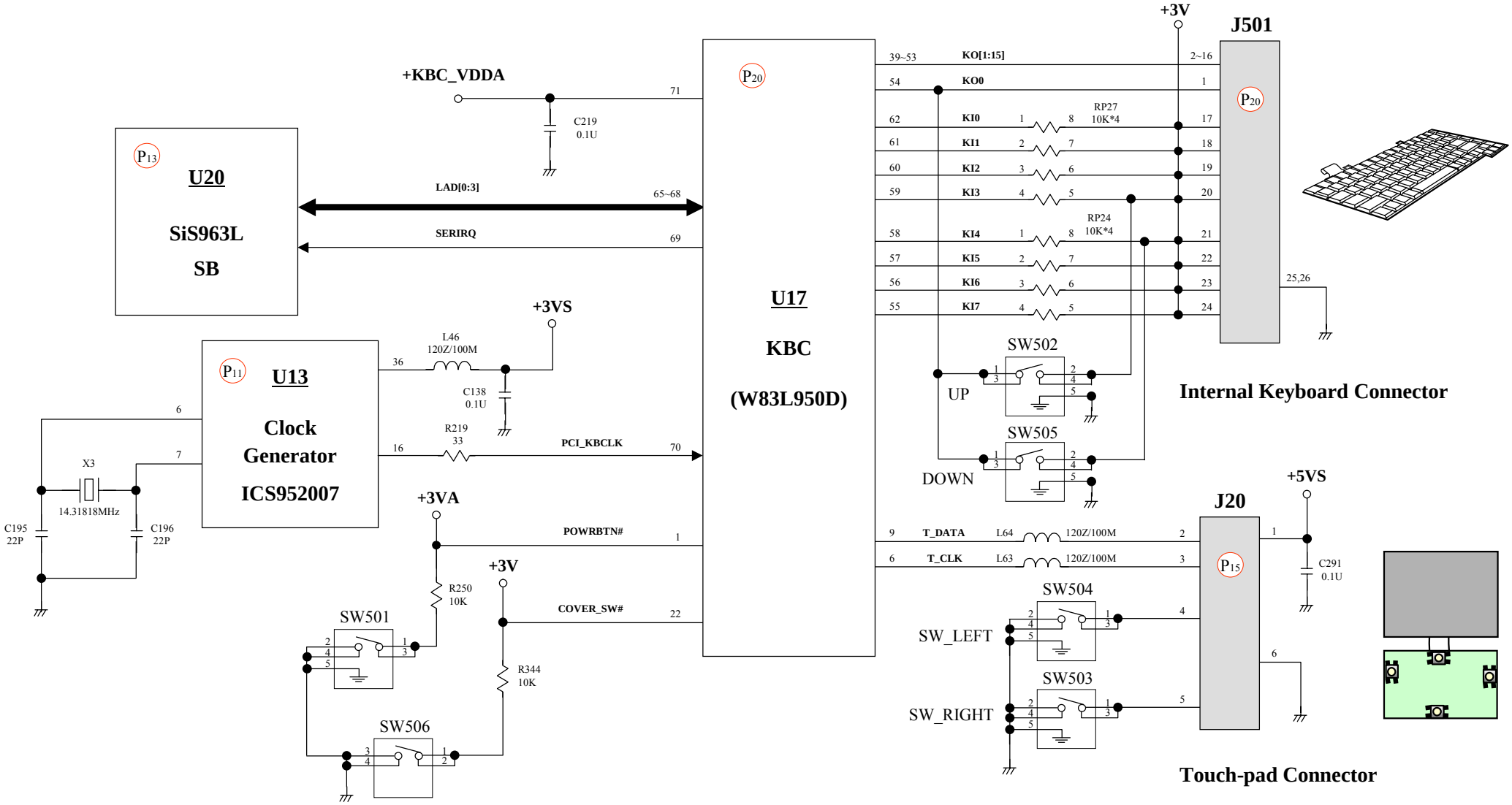
8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

Error message of keyboard or touch-pad failure is shown or any key does not work.



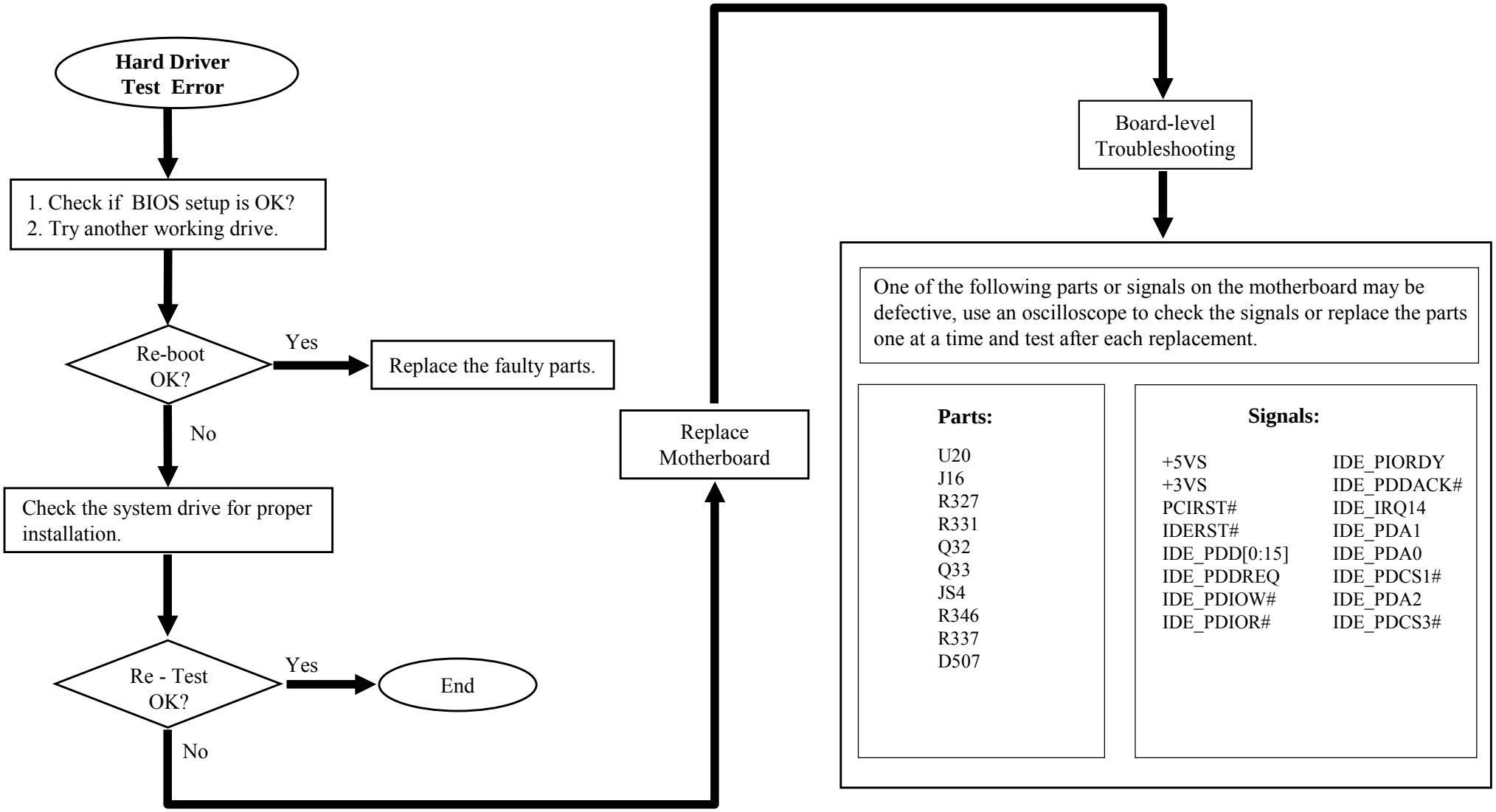
8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

Error message of keyboard or touch-pad failure is shown or any key does not work.



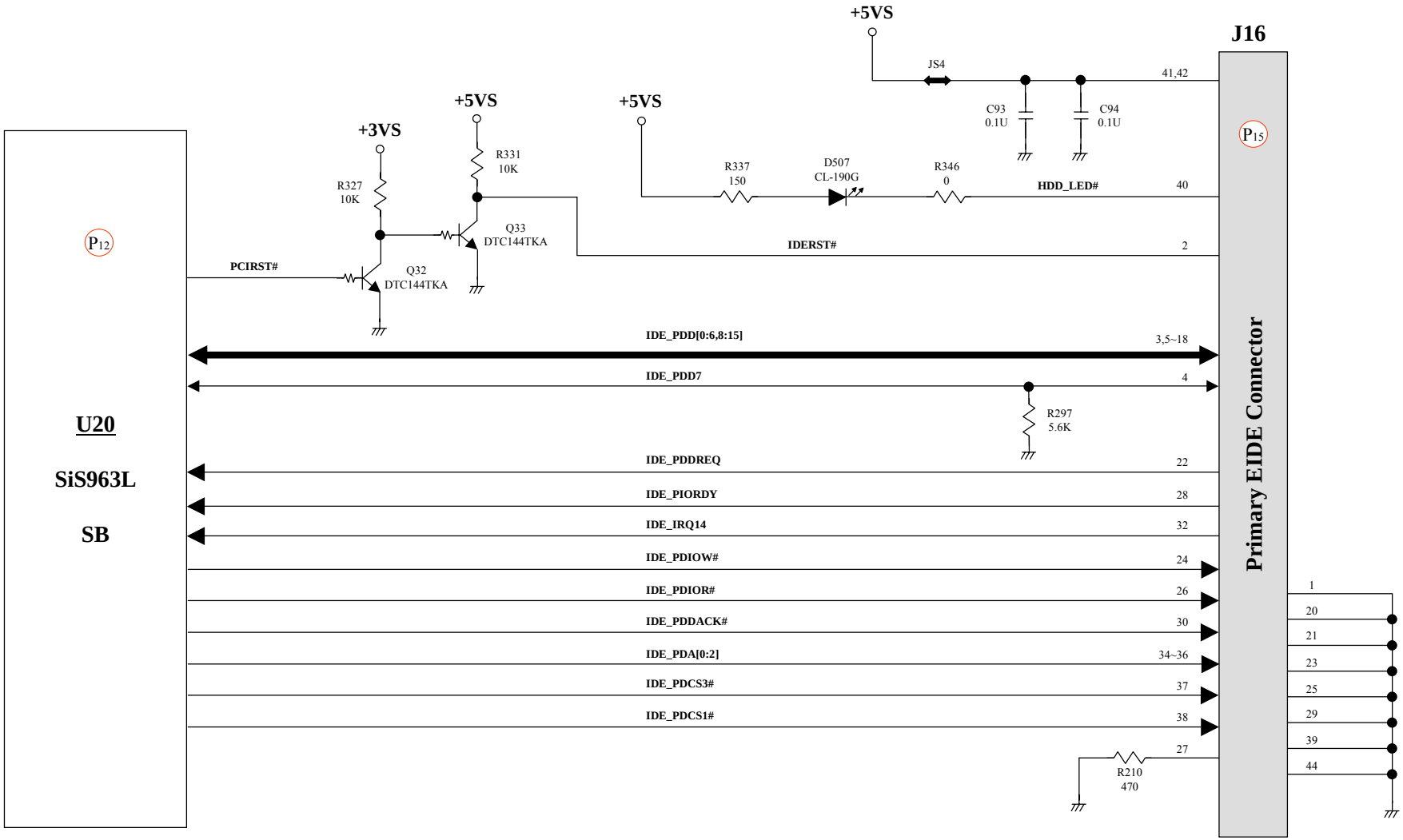
8.9 Hard Drive Test Error (1)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



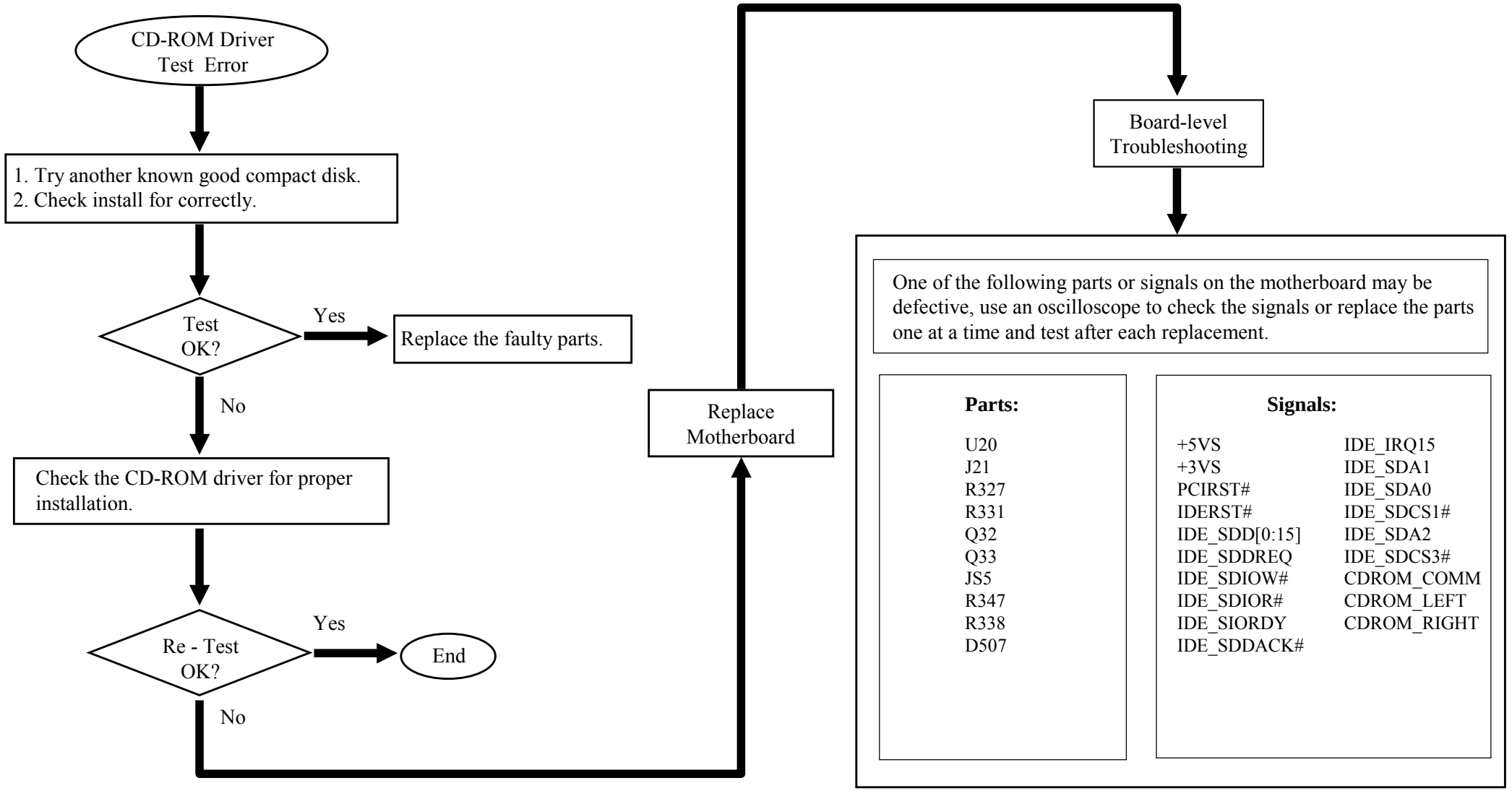
8.9 Hard Drive Test Error (2)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



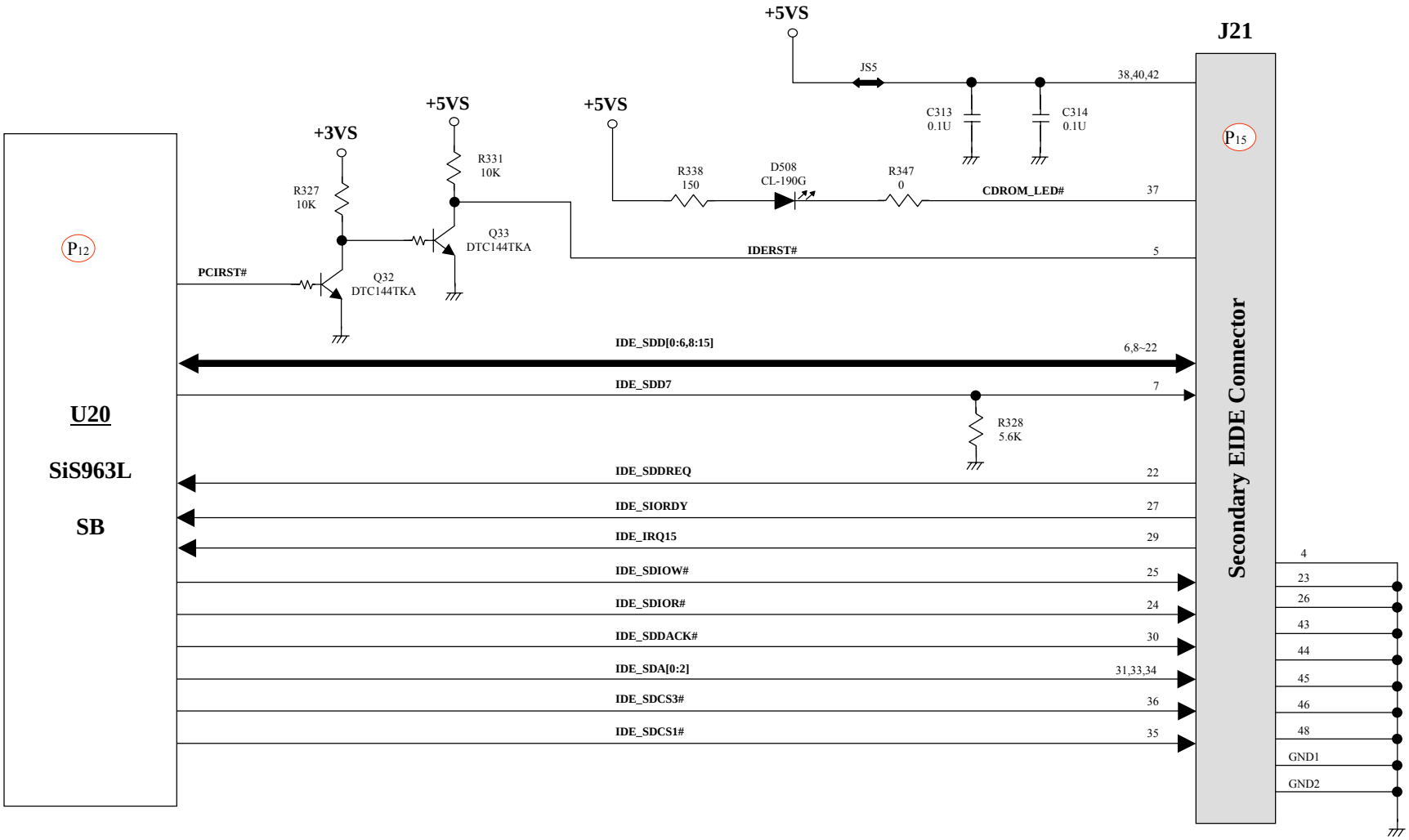
8.10 CD-ROM Drive Test Error (1)

An error message is shown when reading data from CD-ROM drive.



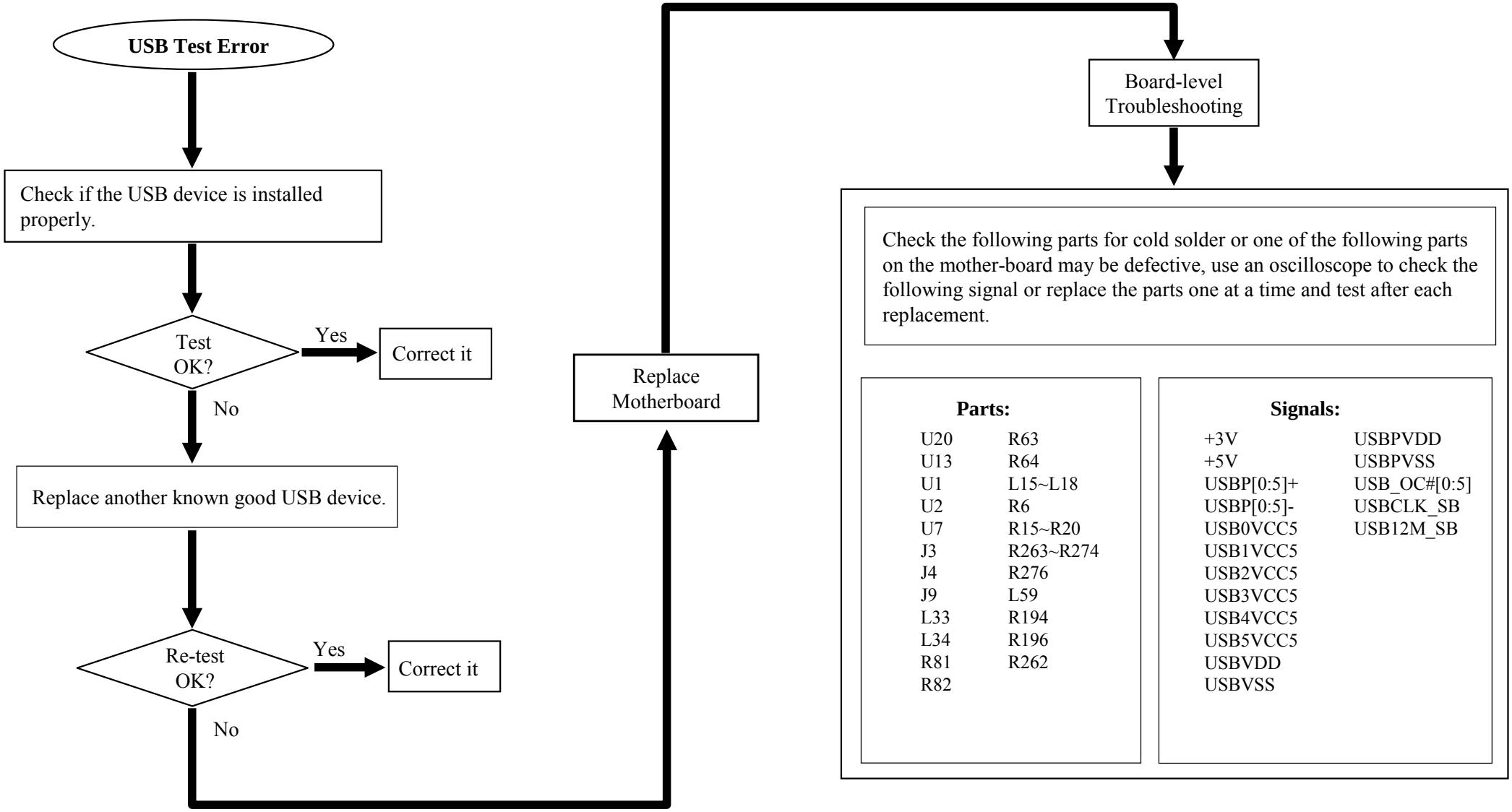
8.10 CD-ROM Drive Test Error (2)

An error message is shown when reading data from CD-ROM drive.



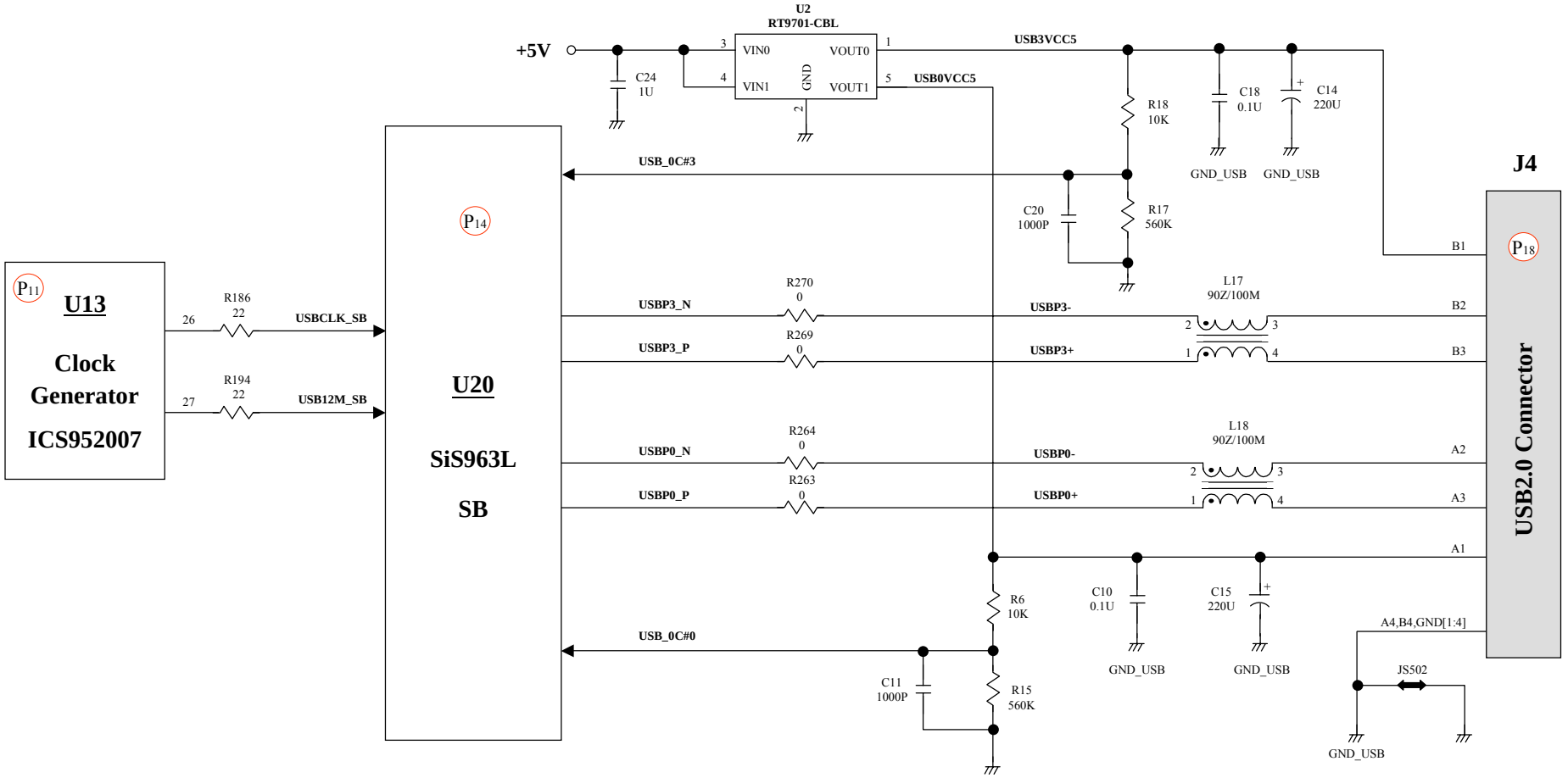
8.11 USB Port Test Error (1)

An error occurs when a USB I/O device is installed.



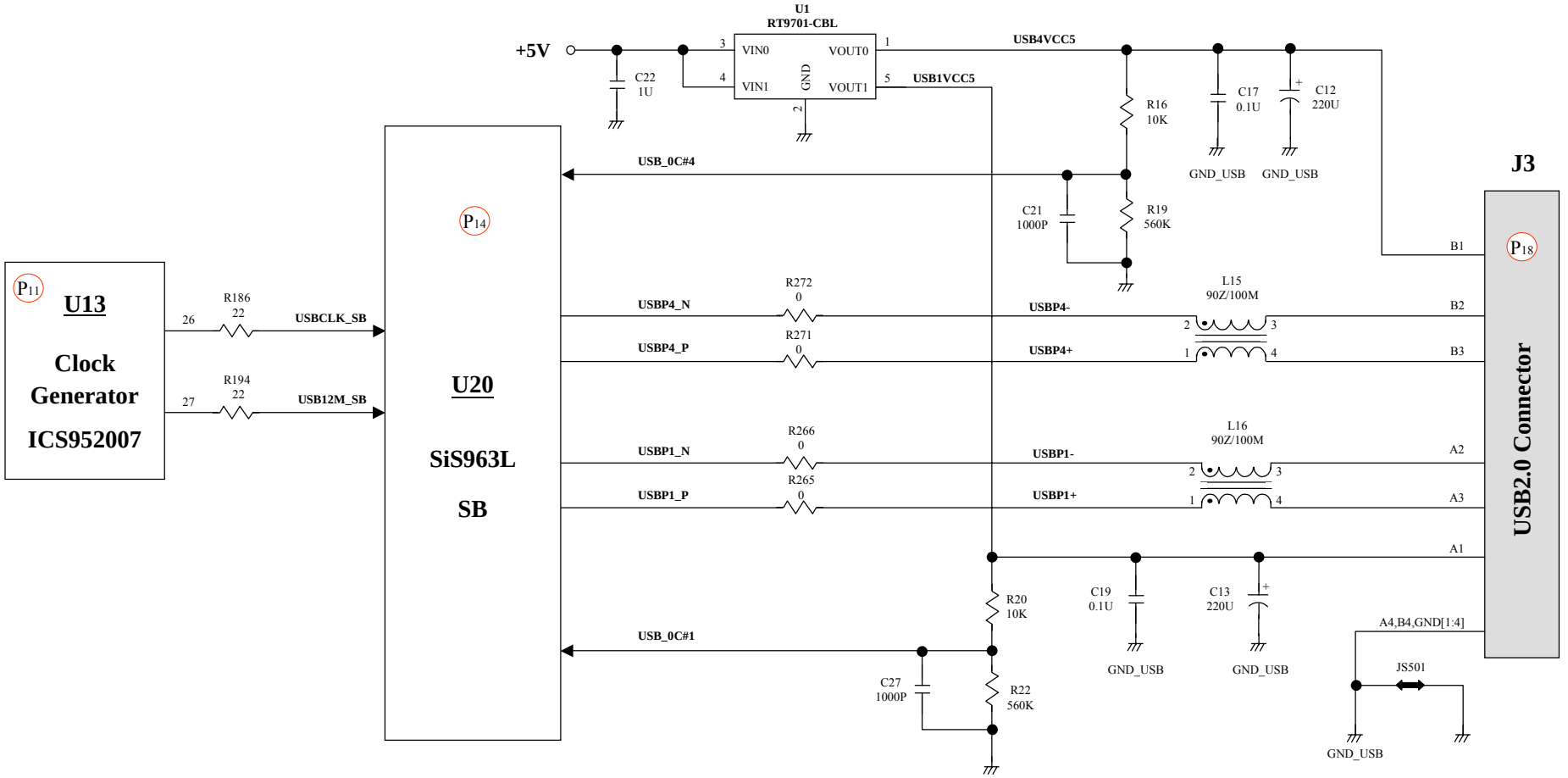
8.11 USB Port Test Error (2)

An error occurs when a USB I/O device is installed.



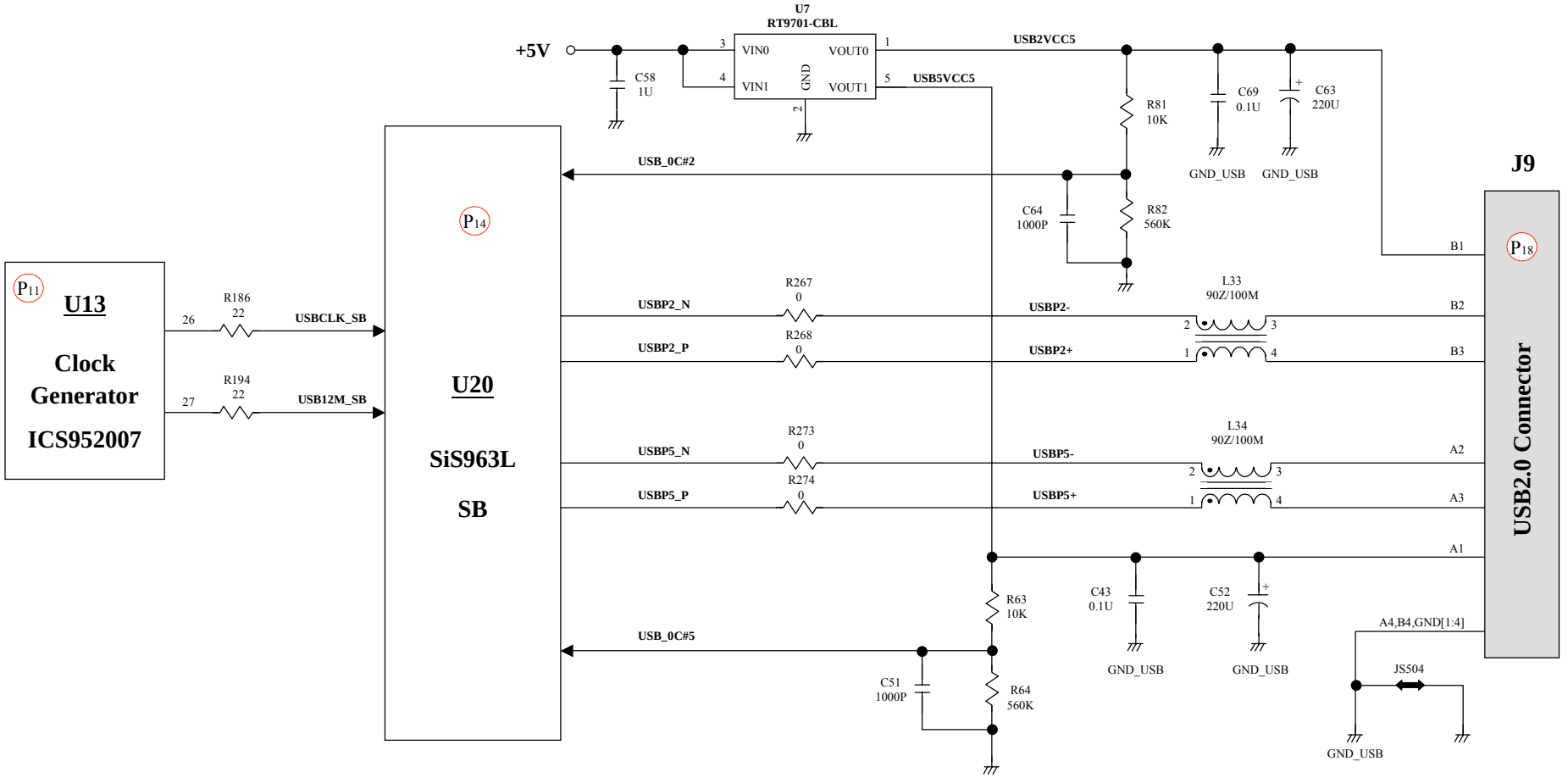
8.11 USB Port Test Error (3)

An error occurs when a USB I/O device is installed.



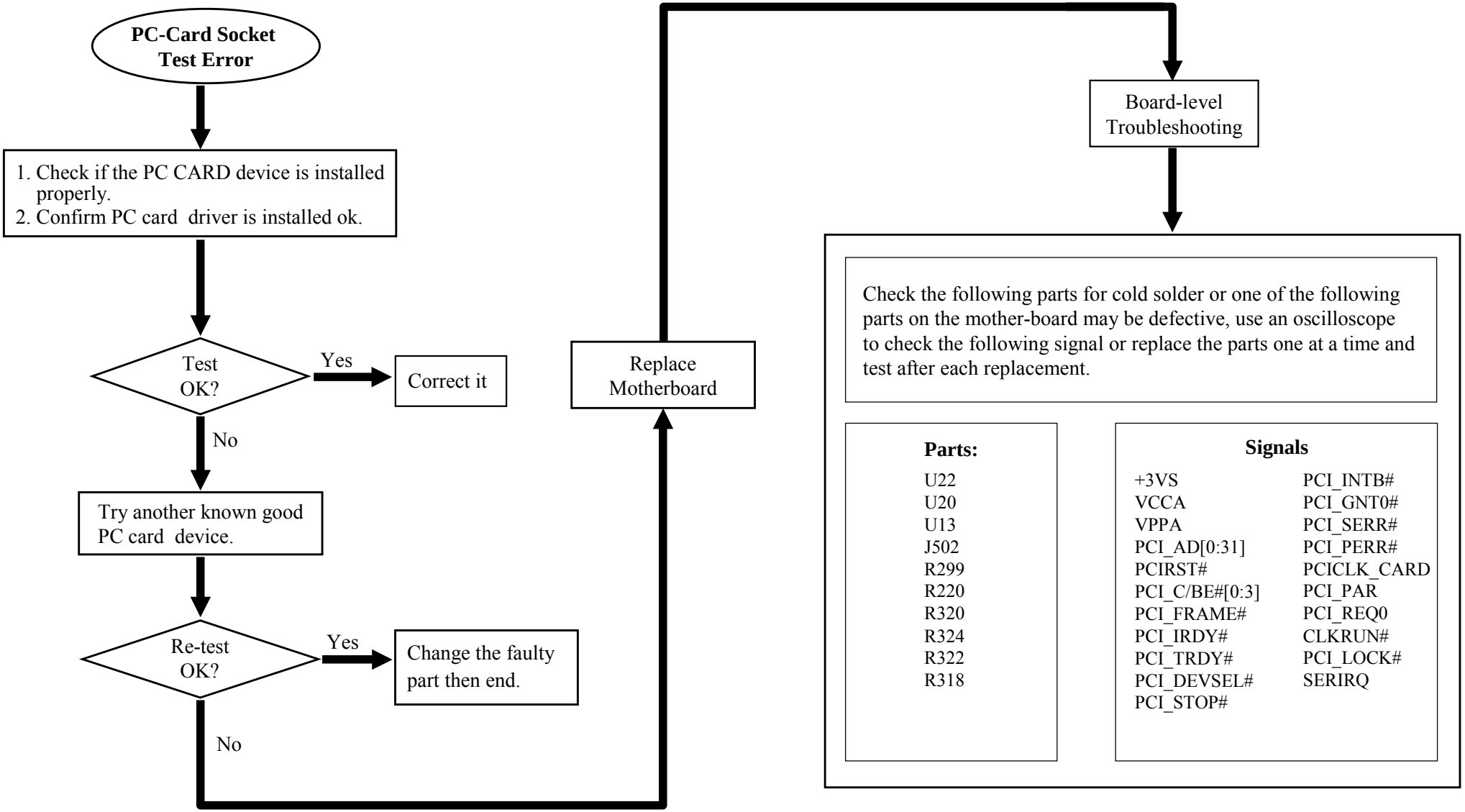
8.11 USB Port Test Error (4)

An error occurs when a USB I/O device is installed.



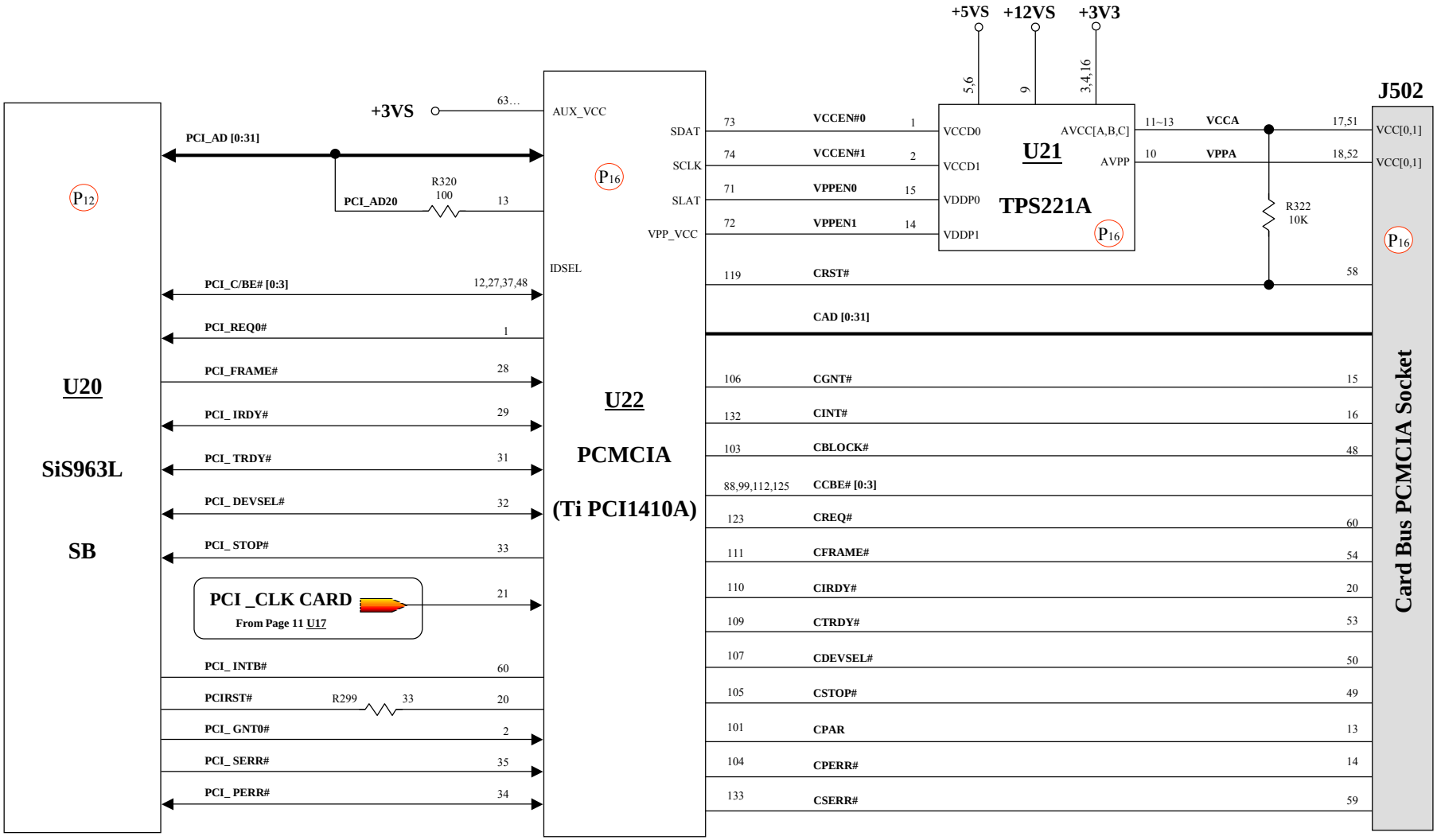
8.12 PC Card Socket Test Error (1)

An error occurs when a PC card device is installed.



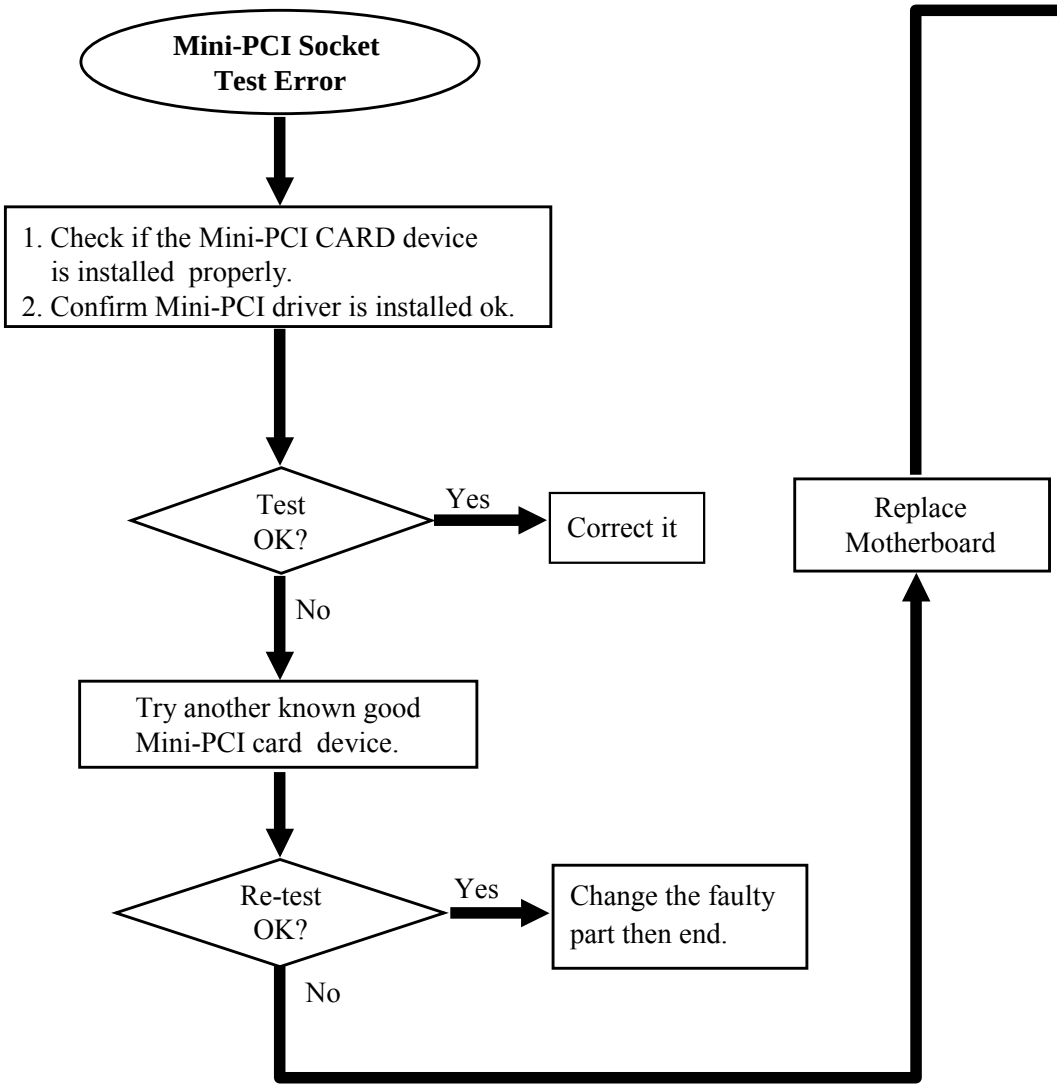
8.12 PC Card Socket Test Error (2)

An error occurs when a PC card device is installed.



8.13 Mini-PCI Socket Test Error (1)

An error occurs when a PC card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

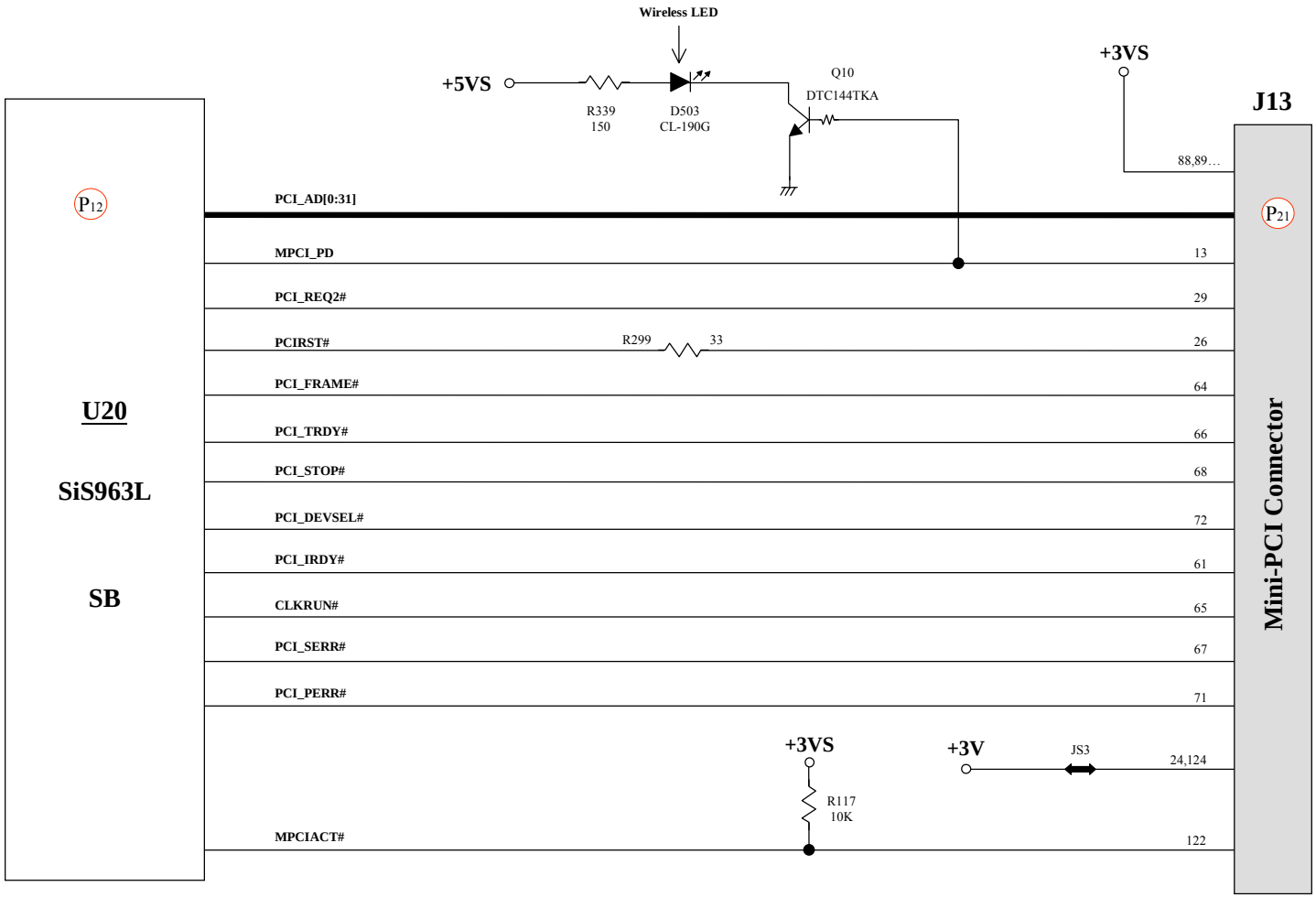
U20
J13
R339
D503
Q10
RP5
R120
R220
R299

Signals

+5VS
+3VS
PCI_AD[0:31]
LAD[0:3]
PCI_C/BE#[0:3]
MPCI_PD
PCI_INTC#
CLK_MINIPCI
PCI_REQ2#
PCI_IRDY#
CLKRUN#
PCI_SERR#
PCI_PERR#
PCI_INTD#
PCIRST#
PCI_GNT2#
PCI_PAR
PCI_FRAME#
PCI_TRDY#
PCI_STOP#
PCI_DEVSEL#

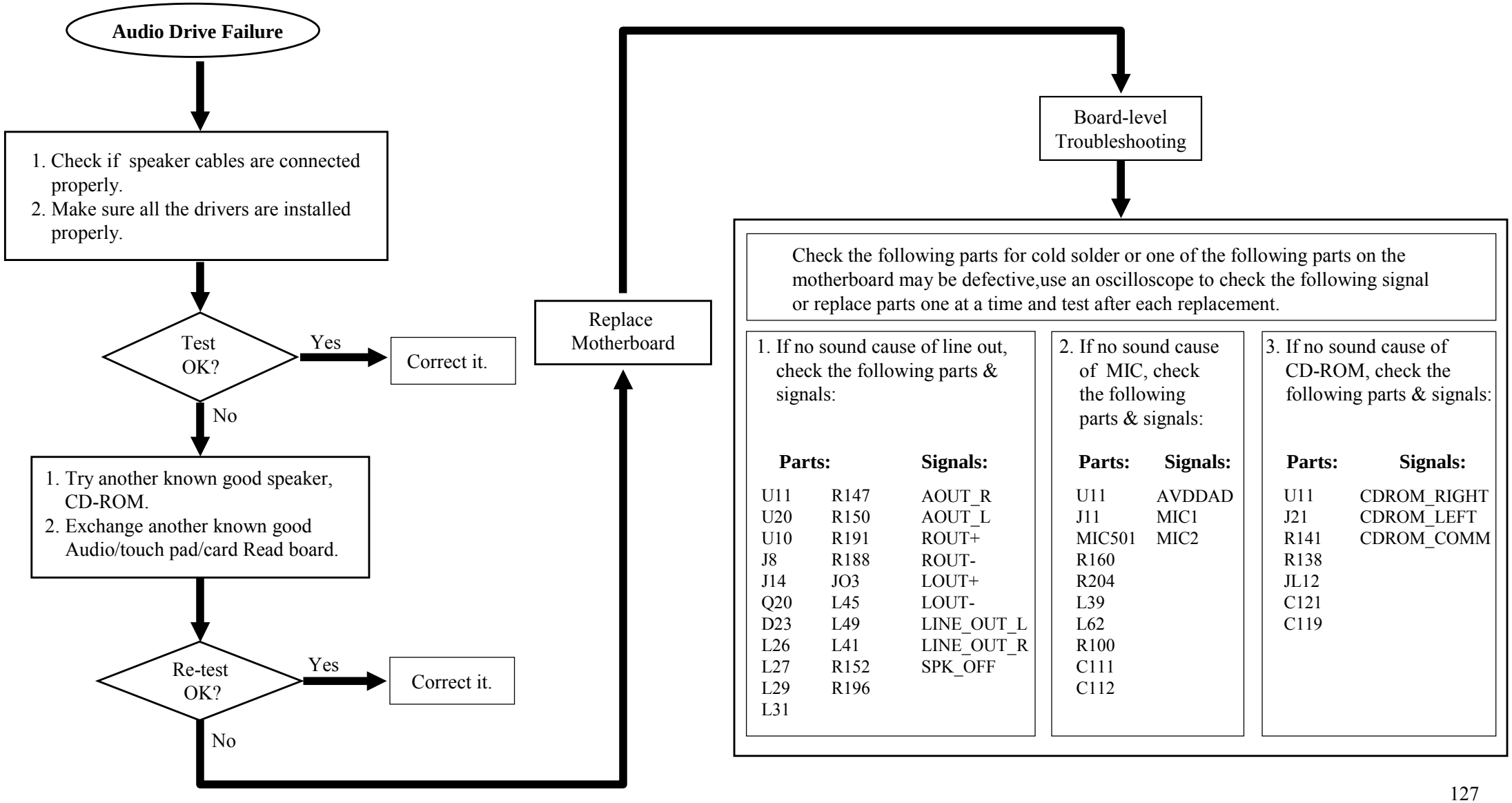
8.13 Mini-PCI Socket Test Error (2)

An error occurs when a PC card device is installed.



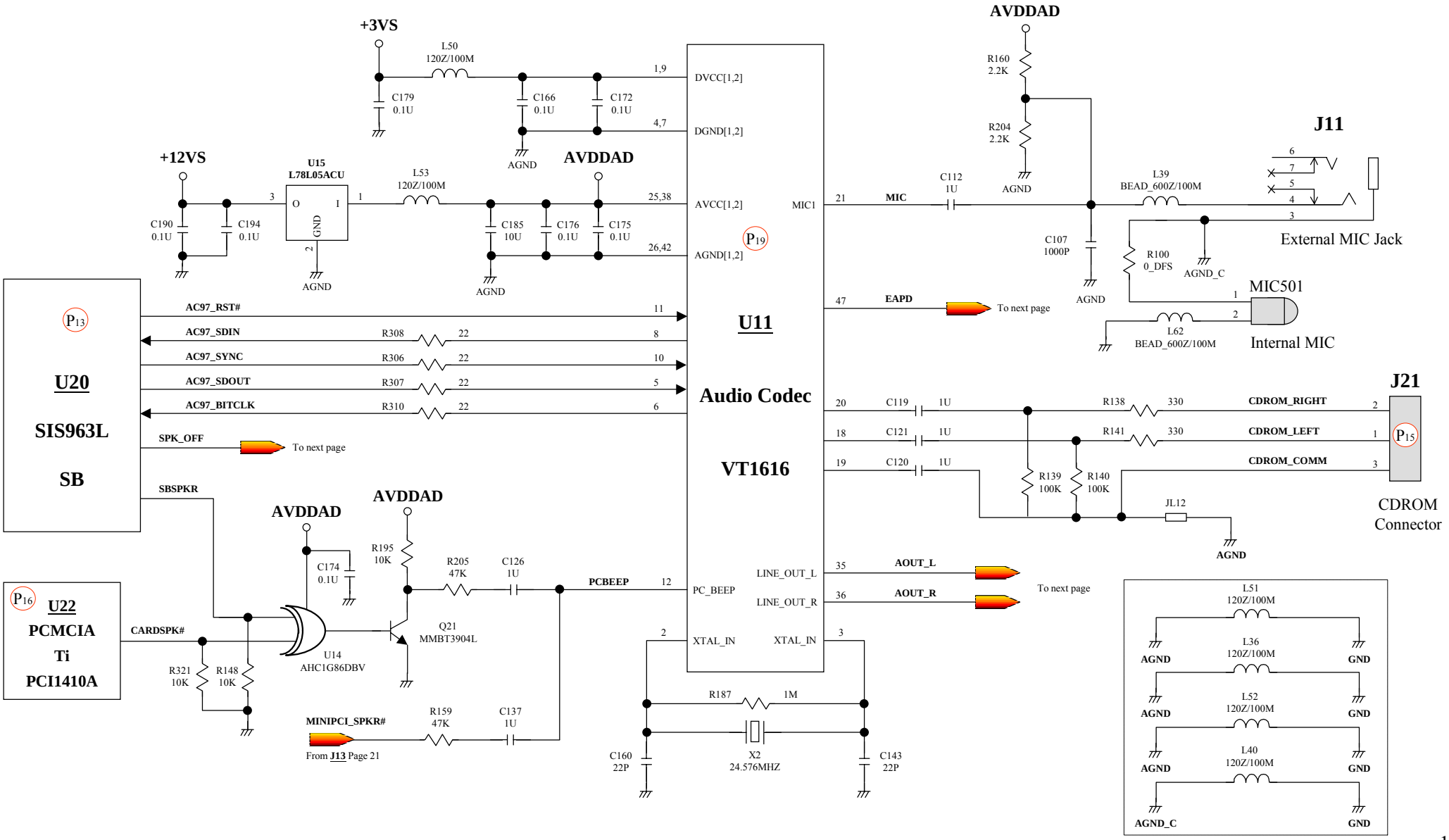
8.14 Audio Failure (1)

No sound from speaker after audio driver is installed.



8.14 Audio Failure (2) – Audio IN

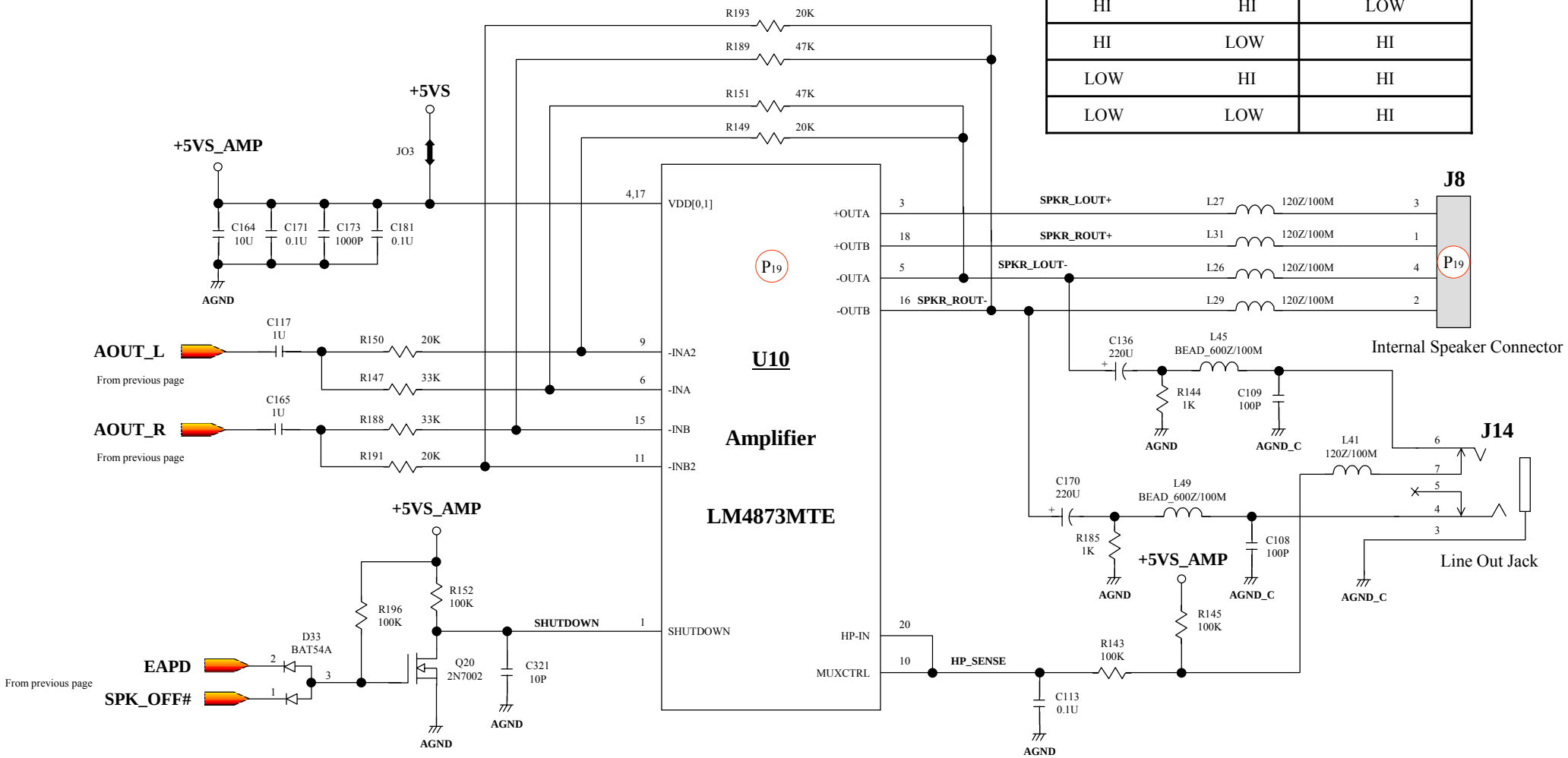
No sound from speaker after audio driver is installed.



8.14 Audio Failure (3) – Audio OUT

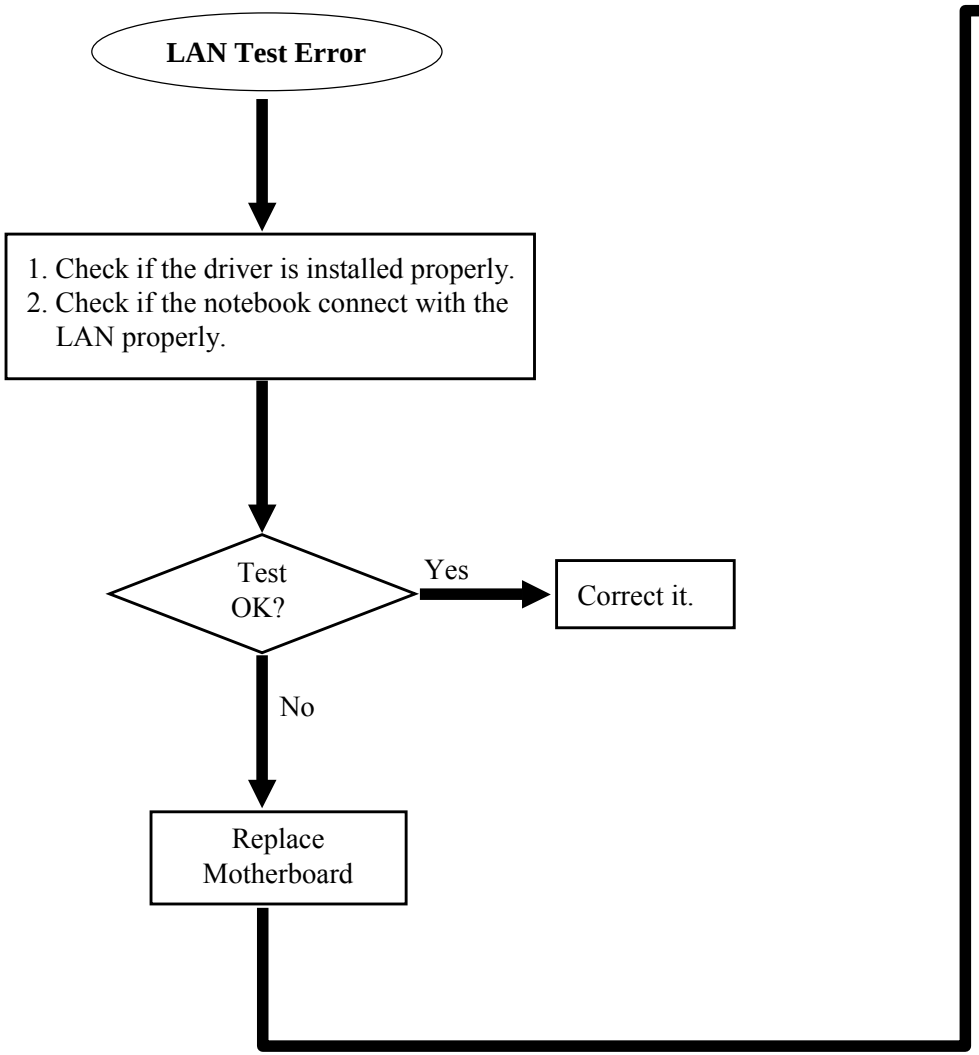
No sound from speaker after audio driver is installed.

SPK_OFF#	EAPD	SHUTDOWN
HI	HI	LOW
HI	LOW	HI
LOW	HI	HI
LOW	LOW	HI



8.15 LAN Test Error (1)

An error occurs when a LAN device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

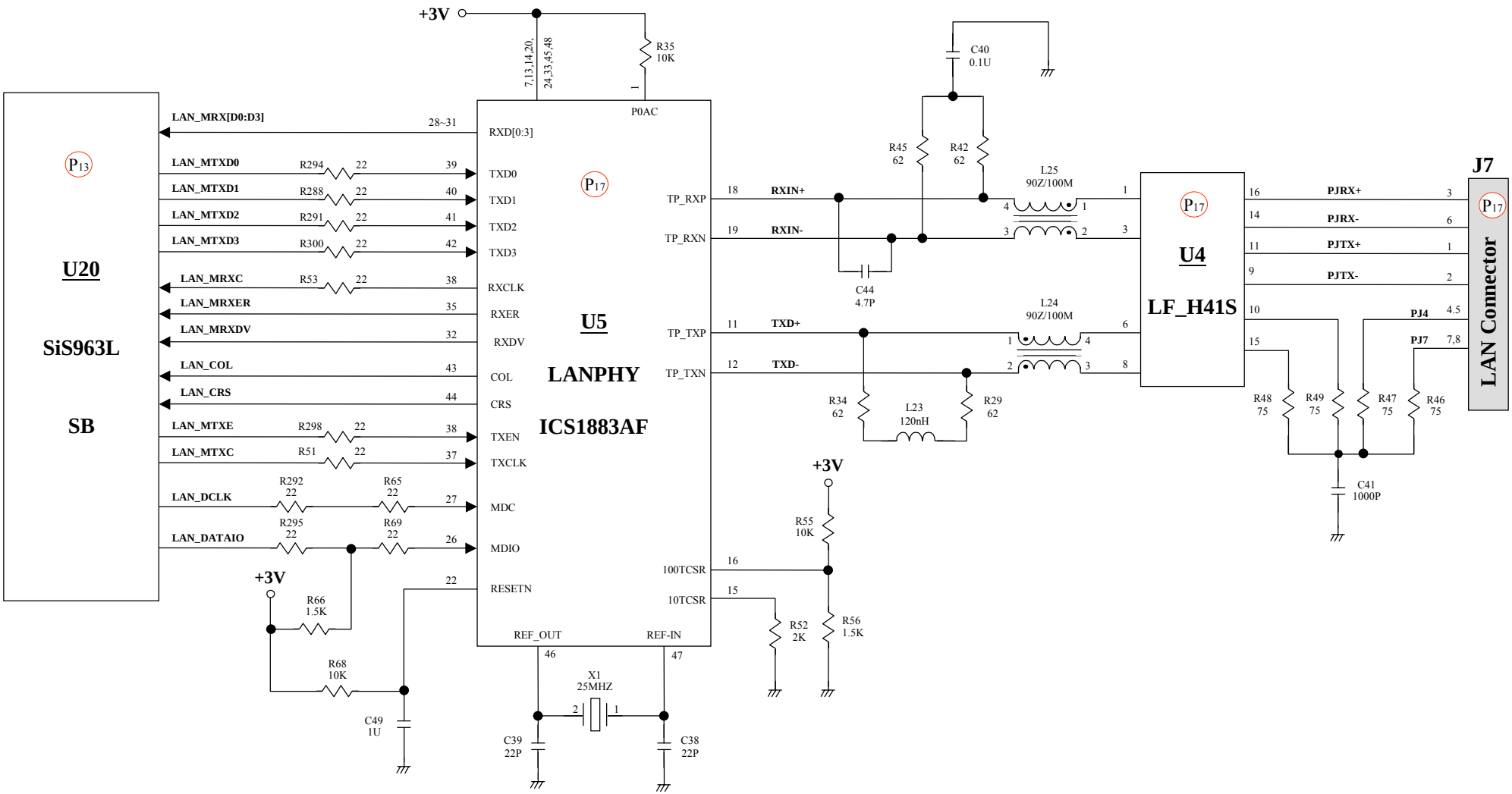
U20	R300
U5	R292
U4	R295
X1	L24
L19	L25
L23	R66
R298	R68
R294	R53
R288	R51
R291	R65
	R69

Signals

+3V	RXIN+
LAN_MRXD[0:3]	RXIN-
LAN_MRXDV	TXD+
LAN_MRXER	TXD-
LAN_MRXC	
LAN_MTXE	
LAN_MTXC	
LAN_DCLK	
LAN_DADAIO	
LAN_COL	
LAN_CRS	

8.15 LAN Test Error (2)

An error occurs when a LAN device is installed.



9. Spare Parts List

Spare Part List 1

Part Number	Description	Location(S)
221679920001	CARTON;NON-BRAND,8640C	
221679950001	PARTITION;IN CARTON,8640C	
221679950002	CARD BOARD;TOP/BTM,PALLET,8640C	
221679950003	CARD BOARD;FRAME,PALLET,8640C	
221679950004	PARTITION;PALLET,8640C	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222678500002	PE BUBBLE BAG;BATTERY,280*170,MS	
224670830002	PALLET;1250*1080*130,7521N	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225682900001	CONDUCTIVE TAPE;DC,M/B,8599	
227675400003	EPE PAD;K/B,8355	
227682900001	END CAP;R,8599	
227682900002	END CAP;L,8599	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	

Part Number	Description	Location(S)
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669600005	LABEL;LOT NUMBER,RACE	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242682900001	LABEL;AGENCY-GLOBAL,8599	
242682900005	LABEL;BATT 14.8V/4AH,LI,PANA,MSL	
271002103301	RES;10K ,1/10W,5% ,0805,SMT	PR114,PR54,PR55
271002104301	RES;100K ,1/10W,5% ,0805,SMT	PR110
271002331301	RES;330 ,1/10W,5% ,0805,SMT	FR3,FR4,R14,R15
271013102301	RES;1K ,1/4W ,5% ,1206,SMT	PR166,PR167
271013221301	RES;220 ,1/4W,5% ,1206,SMT	PR118,PR157,PR158,PR159
271044060301	RES;.006 ,1.5W,5% ,2512,SMT	
271044061101	RES;.06,2W,1%,2512,SMT,乾坤	
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR72
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR108,PR71
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR95
271045357101	RES;.035,1W,1%,2512,SMT	PR136
271046068101	RES;.006 ,1.5W ,1% ,2512,SMT;PWR	RM4
271046069101	RES;.06,2W,1%,2512,SMT	PR47,PR48
271061000002	RES;0 ,1/16W,0402,SMT	PC106,PC86,PR12,PR143,PR145,
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR52,PR59,PR63,R182,R199,R22

9. Spare Parts List

Spare Part List 2

Part Number	Description	Location(S)
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R120,R124,R130,R320,R325,R326
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PR105,PR92,R1,R144,R185,R2,R2
271061103102	RES;10K ,1/16W,1% ,0402,SMT	PR10,PR137,PR141,PR8,R146,R1
271061103501	RES;10K ,1/16W,5% ,0402,SMT	PR20,PR25,PR7,R117,R133,R134,
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR115,PR130
271061104501	RES;100K ,1/16W,5% ,0402,SMT	PR107,PR112,PR129,PR3,PR32,P
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR106,PR111,PR113,PR70,PR85,
271061121312	RES;12.1K,1/16W,1% ,0402,SMT	PR124
271061130111	RES;130 ,1/16W,1% ,0402,SMT	R131
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R110,R211,R224,R230,R232,R234
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R317
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R333,R56,R66
271061202102	RES;2K ,1/16W,1% ,0402,SMT	R52
271061203102	RES;20K ,1/16W,1% ,0402,SMT	PR102,PR34,PR76,PR81,PR96,R1
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R127,R128,R179,R180,R186,R194
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R136,R153,R160,R91,R92
271061243101	RES;24K ,1/16W,1% ,0402,SMT	R73
271061261211	RES;26.1K,1/16W,1%,0402,SMT	PR77
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R204
271061273501	RES;27K ,1/16W,5% ,0402,SMT	PR37
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R173,R174,R175,R176,R200,R201
271061333101	RES;33K ,1/16W,1% ,0402,SMT	R147,R188
271061402011	RES;40.2 ,1/16W,1% ,0402,SMT	R235,R236
271061471501	RES;470 ,1/16W,5% ,0402,SMT	PR1,R210
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R142,R155,R177,R178,R192,R246

Part Number	Description	Location(S)
271061473102	RES;47K ,1/16W,1% ,0402,SMT	R151,R189
271061473501	RES;47K ,1/16W,5% ,0402,SMT	PR131,PR2,R159,R315,R318
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR121,PR14,PR19,PR56,PR62,PR
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R168
271061475211	RES;4.75K,1/16W,1% ,0402,SMT	PR104,PR75
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R162,R163,R164,R165,R166,R167
271061512102	RES;5.1K ,1/16W,1% ,0402,SMT	PR38
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R297,R328
271061564101	RES;560K ,1/16W,1% ,0402,SMT	R15,R17,R19,R22,R64,R82
271061620101	RES;62 ,1/16W,1% ,0402,SMT	R103,R104,R105,R106,R107,R108
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R102
271061753101	RES;75,1/16W,1%,0402,SMT	R122,R46,R47,R48,R49
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR13,PR138,PR140,PR156,PR6
271071010301	RES;1 ,1/16W,5% ,0603,SMT	PR148,PR150
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR117,PR120,PR139,PR146,R21
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R13,R17,R18,R35,R36,R4
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR149,PR160,PR79,PR99
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,R37,R38
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R2,R3
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR128,PR142,PR151,PR153
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR123
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R16,R39
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R312

9. Spare Parts List

Spare Part List 3

Part Number	Description	Location(S)
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR103
271071125301	RES;1.2M ,1/16W,5% ,0603,SMT	PR29
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R14A
271071140101	RES;14 ,1/16W,1% ,0603,SMT	R132
271071147011	RES;147 ,1/16W,1% ,0603,SMT	R71
271071162211	RES;16.2K,1/16W,1% ,0603,SMT	PR42
271071169011	RES;169 ,1/16W,1% ,0603,SMT	R137,R54
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR109
271071182214	RES;18.2K,1/16W,1%,0603,SMT	PR147
271071183101	RES;18K ,1/16W,1% ,0603,SMT	PR144
271071201101	RES;200 ,1/16W,1% ,0603,SMT	R228,R231
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071221311	RES;221K ,1/16W,1% ,0603,SMT	PR154
271071223302	RES;22K ,1/16W,5% ,0603,SMT	PR30
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R41
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R119
271071274211	RES;27.4K,1/16W,1% ,0603,SMT	PR39
271071287111	RES;2.87K,1/16W,1% ,0603,SMT	PR40
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071309211	RES;30.9K,1/16W,1% ,0603,SMT	PR127
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR24,PR51,PR58,PR64
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR135
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R2
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R118
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR132

Part Number	Description	Location(S)
271071411102	RES;412,1/16W,1% ,0603,SMT	R283
271071422211	RES;42.2K,1/16W,1% ,0603,SMT	PR5
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071453211	RES;45.3K,1/16W,1% ,0603,SMT	PR83
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	PR133
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR134,PR31,PR45
271071475011	RES;475 ,1/16W,1% ,0603,SMT	PR33
271071475811	RES;47.5 ,1/16W,1% ,0603,SMT	PR41
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR119
271071549211	RES;54.9K,1/16W,1% ,0603,SMT	PR49
271071560101	RES;56 ,1/16W,1% ,0603,SMT	R233,R238,R259,R275
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R72
271071619011	RES;619 ,1/16W,1% ,0603,SMT	PR23,PR26,PR28
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR94
271071634311	RES;634K ,1/16W,1% ,0603,SMT	PR125
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071806111	RES;8.06K,1/16W,1% ,0603,SMT	PR101,PR78
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR27
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4,R5,R9
271586026101	RES;.02 ,2W,1%,2512,SMT	PR122,PR126
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP5
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP12,RP14,RP16,RP18,RP2
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP2

9. Spare Parts List

Spare Part List 4

Part Number	Description	Location(S)
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP24,RP27,RP3,RP39,RP40
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP13,RP15,RP17,RP19,RP2
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP4,RP7
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP58,RP59,RP6,RP64
272001106705	CAP;10U,10V,+80-20%,0805,Y5V,SMT	C146,C159,C164,C185,C320
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC29,PC46,PC61
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	PC38
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC145,PC148,PC19
272005104401	CAP;.1U ,CR,50V,10%,0805,X7R,IN	PC37,PC51,PC53
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C17,C18
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C129,C29,C302,C318,C319,C32,C
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C100,C225,C274,C275,C279,C346
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	C288
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,S	C14A,C14B
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030102301	CAP;100P,3KV,5%,1808,NPO,SMT ,PWR	C20
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C2,C3,C41
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC12,PC128,PC129,PC130,PC142
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C12,C17,C6
272072393401	CAP;.039U,CR,16V ,10%,0603,X7R,S	PC13
272072683404	CAP;.068U ,16V ,10%,0603,X7R,SMT	C16
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C9
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,S	C15A

Part Number	Description	Location(S)
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC151,PC153,PC32,PC45,PC60
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C11,C13,C3,C8
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C15,C16,C35,C37,C38,C39
272075103706	CAP; 0.1U CR 50V +80-20% 0603 Y	C28,C30,C31,C32,C33,C34
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	PC10,PC101,PC103,PC108,PC112
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,S	C281,C282
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SM	PC110,PC81
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC74
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C143,C160,C195,C196,C217,C221
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	PC11
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C5
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C29,C40,C41
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C36
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C19
272075479301	CAP;4.7P,50V,5%,0603,NPO,SMT	C44
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C501,C502,C503,C504,C505,C506
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C101,C110,C111,C112,C117,C118
272102153401	CAP;.015U ,CR,16V,10%,0402,X7R,S	PC89
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SM	C189,C229,C264,C266,C30,C31,C
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	C1,C108,C109,C57,PC109,PC116,
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C107,C11,C131,C150,C173,C20,C
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C183,C184,C191,C193,C228,C237
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C10,C102,C103,C104,C105,C106,
272105222301	CAP;220P ,50V ,5% ,0402,NPO,SMT	C35
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C67

9. Spare Parts List

Spare Part List 5

Part Number	Description	Location(S)
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C154,C157,C289,C316,C4,C5,C6,C
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC166
272431156501	CAP;150U,6.3V,TPE,20%,7343,SMT	PC165
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2
272990100301	CAP;10P,3000V,+- 5%,NPO,SMT	C19
272993106001	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	PC105,PC120,PC121,PC125,PC13
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L2,L22,L26
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L39,L45,L49,L62
273000130062	INDUCTOR;120nH,10%,0603,SMT	L23
273000130106	FERRITE CHIP;600OHM/100MHZ,.2A,1	
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL1,PL13,PL15,PL16,PL17,PL18
273000150106	INDUCTOR;4.7UH,10%,2012,30mA,SMT	L20,L21
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L15,L16,L17,L18,L24,L25,L33,L3
273000150326	INDUCTOR;4R7,2012,15mA;SMT,MAG.L	
273000500095	CHOCK COIL;0.5UH.1.0mOHM,25%,30A	PL10,PL8,PL9
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL14
273000500111	CHOCK COIL;3UH,14mOHM,7.5A,10039	PL11,PL12
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L19
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL19
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PT1
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U4
273001050127	XFMR;CI8.5,30T/2150T,300mH,SMT,o	T1
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U14
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC6

Part Number	Description	Location(S)
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U16
283467640002	IC;FLASH,256K*8, PLCC32, LPC, ST	
283468290001	IC;FLASH,256K*8,PLCC32,SST49LF02	
283468290002	IC;FLASH,256K*8,PLCC32,PM49FL002	
284500301004	IC;SIS301LV,TV ENCODER/LVDS,128P	U9
284500661001	IC;SISM661FX,N.B,BGA 839P	U12
284500781001	IC;G781,TEMPERATURE MTR,SO8	U8
284500963004	IC;SIS963L,S.B.,BGA 371P	U20
284501410007	IC;PCI1410A,PCI/CARDBUS,PQFP,144	U22
284501616002	IC;VT1616,6-CHANNEL CODEC WITH S	U11
284501883001	IC;ICS1883AF,LAN PHY,SMT,SSOP48	U5
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
284593772002	IC;ICS93772CF,DDR ZERO DELAY CLO	U19
284595200701	IC;ICS952007,CLOCK GEN,SSOP,48P	U13
286100358001	IC;LMV358M,DUAL AMP.,LOW VOLT.,S	PU2
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU21
286101422001	IC;G1422,AMPLIFIER,2W,TSSOP,20P,	U10
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ40
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC7
286301772001	IC;MAX1772,PWM,QSOP,28P	PU22
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U21
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	PU3
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU8
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU11,PU14

9. Spare Parts List

Spare Part List 6

Part Number	Description	Location(S)
286304377001	IC; MAX4377F,I-SENSEAMP ,MSOP8,S	PU20
286306207001	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PU5,PU6,PU7
286306247001	IC;ISL6247,PWM CONTROLLER,40-QFN	PU1
286307805019	IC;AZ78L05,VOL REGULATOR,SOT-89,	U15
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	PU4
286309181002	IC;RT9181, 150mA LDO with POG,SO	U3
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U1,U2,U7
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU17
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V	U18
286387506001	IC;S-875061EUP VOLT DETECTOR S	IC5
288100024004	DIODE;ZMD24,ZENER,24V,1W,5%,SMT	PD4
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD8
288100056003	DIODE;BAW56,70V,215mA,SOT-23	PD16
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD3,ZD4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD2
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,	
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD14
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-2	D33,PD11,PD13
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D15,PD1,PD3
288100840001	DIODE;SM840B,40V,8A,STD-202	PD5,PD7
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD12
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD10,PD6,PD9
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D19,D20,D21
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D3
288111544001	DIODE; 1SR-154-400 400V 1.0A	D4

Part Number	Description	Location(S)
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ12,PQ35
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ18,Q10,Q14,Q22,Q23,Q26,Q29
288200144008	TRANS;DTA144EKA,PNP,SMT	Q8
288200610001	TRANS;TP0610T,P-MOSFET,SOT-23	PQ9
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323	SD2
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	
288203400001	TRANS;AO3400,N-MOSFET,SOT-23	PQ26,PQ30,Q4
288203401001	TRANS;AO3401,P-MOSFET,SOT-23	PQ13,PQ17,PQ34
288203403001	TRANS;AO3403,P-MOSFET,SOT-23,ALP	Q8,Q9
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ6,Q13,Q17,Q21,Q31,Q34
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q30
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ38,PQ39,PQ7,PQ8
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q10,Q14
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0	PU10
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOI	PU13,PU19
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU16
288204814001	TRANS;SI4814,26.5mOHM,N_MOS ,SMT	PU15,PU23,PU9
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU18
288204892001	TRANS;SI4892DY,N-MOSFET,SO8	PU12
288205003004	TRANS;SUD50N03-11,N-MOS,TO252	PQ15,PQ16,PQ20,PQ21,PQ23,PQ
288206035005	TRANS;FDD6035AL,46A,30V,16mOHM,T	PQ14,PQ19,PQ22
288206405001	TRANS;AO6405,87mOHM ,P-MOS,SMT	PQ42,PQ43
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ1,PQ10,PQ11,PQ2,PQ27,PQ28
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000000708	CON;BATTERY,7P,FM,2.5MM,BTG-07AR	CON1

9. Spare Parts List

Spare Part List 7

Part Number	Description	Location(S)
291000001206	CON;MINI PCI SOCKET,P124,QTC,C10	
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	
291000010410	BFM-SC,CON;HDR,MA,4P*1,1.25MM,ST	
291000013016	CON;HDR,MA,15P*2,1MM,H4.25,ST,SM	J6
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000020222	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J10,J12,J19,J5
291000020415	CON;HDR,MA,4P*1,1.25MM,ST,SMT,38	J8
291000143011	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J15
291000150606	CON;FPC/FFC,6P,0.5MM,R/A,SMT	J20
291000150607	CON;FPC/FFC,6P,0.5MM,R/A,SMT,200	
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	
291000152614	CON;FPC/FFC,26P,1MM,H=2.0,R/A,SM	J501
291000611255	MINIPCI SOCKET;124P,0.8MM,H=9.2,	J13
291000614795	IC SOCKET;BGA-mPGA478B,478P,AMP	U6
291000616805	CON;PCMCIA CARD,68P,TAI-SOL,246-	J502
291000811001	CON;PHONE JACK,10P,R/A,RJ45,RJ11	J7
291000811011	CON;PHONE JACK,10P,R/A,RJ45,RJ11	
291000923002	CON;MDC,15P*2,.8MM,BD/BD,ST,SMT,	
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D501,D502,D503,D504,D505,D50
294011200200	LED;GREEN/RED,H0.8,W1.9,19-22SRV	D509
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF1,PF2
295000010154	FUSE;FAST,1.25A,63V,1206,SMT,043	F1
297030100015	SW;TOGGLE,SPST,5V/1mA,4P,SMT,TAI	SW506
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	
297040100027	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	

Part Number	Description	Location(S)
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW501,SW502,SW503,SW504,SW
310111103013	THERMISTOR;10K,1%,RA,DISK,103AT-	RT2
310111103025	THERMISTOR;10K,1%,RA,DISK,103AT-	
310111103031	THERMISTOR;10K,1%,150MM,BN35-3H1	
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC159,PC160,PC63,PC64
312272205359	EC;22U ,20V,20%,RA,D6.3*5,OS-CO	PC25,PC26,PC58
312272206101	EC;220U ,6.3V,M,6.3*5,-55+105',D	C12,C13,C136,C14,C15,C170,C52
312272206102	EC;220U ,10V,M,6.3*9,-55+105',DI	
312273361501	EC;330U ,6.3V ,RA,M,6.3*7,+105C	
312276806151	EC;680U ,6.3V,20%,D10,105'C,OS-C	PC127
312276806158	EC;680U,6.3V,20%,RA,10*10.5,105	
312278206151	EC;820U ,4V,+-20%,100*10.5,SP.OS	PC72,PC95
312278206161	EC;820U ,2.5V,+-20%,8X12.5,OS-CO	PC41,PC42,PC49,PC50,PC56,PC5
314100143505	XTAL;14.31818MHZ,30PPM,32PF,49S,	X3
314100143506	XTAL;14.31818MHZ,30PPM,32PF,AT49	
314100245504	XTAL;24.576MHZ,30PPM,16PF,49S,11	X2
314100250502	XTAL;25MHZ,30PPM,20PF,49S,11.5*3	X1,X6
314100327214	XTAL;32.768KHZ,12.5PF,20PPM,3*8,	X7
314149800402	XTAL;8MHZ,30PPM,HC-49/S,6B080002	X4
316678100001	PCB;PWA-INVERTER BD (DA-1A10-A);	R0C
316682900001	PCB;PWA-8599/M BD	R06
316682900003	PCB;PWA-8599/BATT ,PR AND GA BD	
323768290002	DDR SDRAM MODULE;256MB,184PIN,DD	
324180786744	IC;CPU,Celeron,2.8G,FSB 400,MICR	
331000000083	CON;HOLDER,PCMCIA,TAI-SOL,246-00	

9. Spare Parts List

Spare Part List 8

Part Number	Description	Location(S)
331000007038	CON;BAT,7P,2.5mm,OCT,tBTD-007001	PJ2
331000007044	CON;BAT,7P,2.5mm,ALLTOP,C10368	
331000008090	CON;USB,MA,ST,4P*2,SMT,020122MR0	
331000008091	CON;USB,MA,ST,4P*2,SMT,1-1470748	J3,J4,J9
331000050004	CON;CD-ROM,50P,0.8MM,H-10.4,R/A,	J21
331000050005	CON;CD-ROM,50P,0.8MM,H-10.4,R/A,	
331030044021	CON;HDR,FM,22P*2,2.0MM,SMT,C1783	J16
331030044023	CON;HDR,FM,22P*2,2.0MM,SMT,2001	
331650047804	IC SOCKET;BGA-PGA478B-SKT,MOLEX,	
331660018441	DIMM SOCKET;DOUBLE STACK DDR,202	J18
331678100001	CONNECTOR;7 PIN,1.25mm,SMT,ACES,	J1
331720015071	CON;D,FM,15P,2.29,R/A,SUYIN	J2
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J11
331840005014	CON;STEREO JACK,5P,R/A,28MF60-05	J14
331870007010	CON;MINI DIN,7P,R/A,W/GROUND,030	J1
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ1
332110020027	WIRE;#20,UL1007,50MM,BLACK,PRC	VL-VL
332110020097	WIRE;#20,UL1007,74MM,BLACK,YIYI;	
332110020175	WIRE;#20,UL1007,L=103MM,RED, PWR	CN10
332110026097	WIRE;#26,UL1007,55MM,BLACK,PRC	
332110026155	WIRE;26#,UL1061,L=115MM,YELLOW,	CN9
332110026156	WIRE;#26,UL1061,L=136.5MM,WHITE,	CN8
332810000197	PWR CORD;125V/7A,3P,BLACK,AMERIC	
333020000008	SHRINK TUBE;600V,125℃,Φ2.5mm,L	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0	

Part Number	Description	Location(S)
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
335152000085	FUSE; 128 DC-7A/50V 139℃only UC	F2
335152000094	FUSE;LR4-900,POLY SWITCH	
335152000100	FUSE; THERMAL,SF91E-1/94℃,10A/2	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,	MIC501
339115000059	MICROPHONE;-44dB+-3dB,D6.0*H5.0,	
339115000060	MICROPHONE; -62+/-3dB,60*27mm;HO	
340682900001	HOUSING ASSY;LCD,8599	
340682900002	COVER ASSY;LCD,8599	
340682900003	HINGE;R,8599	
340682900004	HINGE;L,8599	
340682900005	HINGE;R,SZS,8599	
340682900006	HINGE;L,SZS,8599	
340682900007	COVER ASSY;TOP,8599	
340682900009	BRACKET ASSY;TOUCH-PAD,8599	
340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHI	
340682900011	SPEAKER ASSY; 28*4.3,2W,VECO,859	
340682900013	HEATSINK ASSY;CPU,NORTHWOOD,MPT,	
340682900014	HEATSINK ASSY;CPU,NORTHWOOD,ALRO	
340682900015	HOUSING ASSY;BOTTOM,8599	
340682900016	SHIELDING ASSY;BOTTOM,8599	
340682900017	COVER ASSY;CPU,8599	
340682900018	COVER ASSY;MINIPCI,8599	

9. Spare Parts List

Spare Part List 9

Part Number	Description	Location(S)
340682900019	HAETSINK ASSY;SYSTEM,M/B,MPT,859	
340682900020	HAETSINK ASSY;SYSTEM,M/B,ALRO,85	
340682900021	SHIELDING ASSY;HDD,8599	
340682900023	COMBO BEZEL ASSY; QSI,SBW-242B,8	
341682900003	BRACKET;LCD,R,8599	
341682900004	BRACKET;LCD,L,8599	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GR	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342682900009	BRACKET;ROM,8599	
342682900010	CONTACT PLATE;W5L28T0.15MM,BATTE	
342682900011	CONTACT PLATE;W5L37.75T0.15MM,1/	
342682900012	CONTACT PLATE;W4L18.5T0.15MM,1/2	
342682900015	FINGER;EMI SMD FINGER,H=5.5,8599	
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	
344682900012	COVER;HINGE,8599	
344682900016	COVER;BATTERY,8599	
344682900017	HOUSING;BATTERY,8599	
345668900016	SPONGE;BIOS BATT,M722	
345675400023	RUBBER;DOWN LCD,8355	
345682900005	SPONGE;DUAL DDR,M/B,8599	
345682900006	SPONGE;SPSPEND SWITCH,M/B,8599	
345682900009	SPONGE;HINGE COVER,8599	
345682900013	INSULATOR;S-VIDEO,M/B,8599	
345684500004	RUBBER;SYSTEM HEATSINK,TARZAN	

Part Number	Description	Location(S)
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,	
346503100001	INSULATOR;BATT ASSY,THERMAL FUSE	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346673420003	MYLAR;15*10*0.8,8640P	
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm	
346678600005	INSULATOR;FIBER,UL94V-0,64X15,T=	
346682900005	INSULATOR;CARD BUS,8599	
346682900006	INSULATOR;SOUTH BRIDGE,8599	
346682900007	NYLON;BATTERY PULL,8599	
346682900009	AL-FOIL;T/P BRACKET,8599	
346682900010	AL-FOIL;T/P SWITCH,MB,8599	
346682900013	SPONGE;M/B,8599	
346682900014	INSULATOR;AL-FOIL,INVERTER,8599	
346684400001	INSULATOR;RIBRE,101*15*0.25MM,BA	
346684400002	INSULATOR;RIBRE,63*15*0.25MM,BAT	
347104030012	GASKET;1,04,030,012	
347104030030	GASKET;1,04,030,030	
347104045125	GASKET;1,04,045,125	
347105020090	GASKET;1,05,020,090	
347105060030	GASKET;1,05,060,030	
347105060060	GASKET;1,05,060,060	
347108010012	GASKET;1,08,010,012	
347108080090	GASKET;1,08,080,090	

9. Spare Parts List

Spare Part List 10

Part Number	Description	Location(S)
347108150024	GASKET;1,08,150,024	
347110020025	GASKET;1,10,020,025	
347110035035	GASKET;1,10,035,035	
347110040012	GASKET;1,10,040,012	
347110080025	GASKET;1,10,080,025	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003037	SOLDER CREAM;SH-6309,SHENMAO,63/	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	
371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	
371102610308	SCREW;M2.6L3,D3.5,t=0.5,K-HD,NIW	
371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	
371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
377102650901	S-STANDOFF;M2.6DP3.5H9L1.1,NIW	MTG2,MTG3
377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NY	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
411678100001	PWA;PWA-INVERTER BD,DA-1A10-A,PW	
411678100002	PWA;PWA-INVERTER BD,SMT,DA-1A10-	
411682900001	PWA;PWA-8599,MOTHER BD	
411682900002	PWA;PWA-8599,MOTHER BD,T/U	
411682900003	PWA;PWA-8599,MOTHER BD,SMT	
411684410001	PWA;PWA-BATT,PCB BD,LI,4.0Ah,2P4	
411684410002	PWA;PWA-BATT,BATT BD,SMT,BL-4240	
412678800001	PCB ASSY;FAX MODEM 56K,1456VQL4A	
413000020386	LCD;HSD150PX14-A,TFT15",XGA,HANN	
416268290011	LT PF;HANNSTAR,XGA,HSD150PX14-A,	
421311310001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421675400012	WIRE ASSY;BIOS,BATTERY,8355	
421676400001	WIRE ASSY,MDC-MODEM,APOLLON	
421682900004	WIRE ASSY;HSD150PX14-A,8599	
421682900007	WIRE ASSY;ANTENNA,8599	
421682900014	WIRE ASSY;HSD150PX14-A,GREATLAND	
422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,859	
422682900002	FFC ASSY;TOUCH-PAD,HONG-FU,8599	
422682900003	FFC ASSY;TOUCH-PAD,CEI,8599	
431682900001	CASE KIT;ID1,256KB 8599	
441682900010	LCD ASSY;HANNSTAR,XGA,HSD150PX14	
441684410001	BATT ASSY;14.8V,4.0Ah,LI,BL-424	
441684410002	BATT ASSY;14.8V,4.0Ah,LI,BL-424	

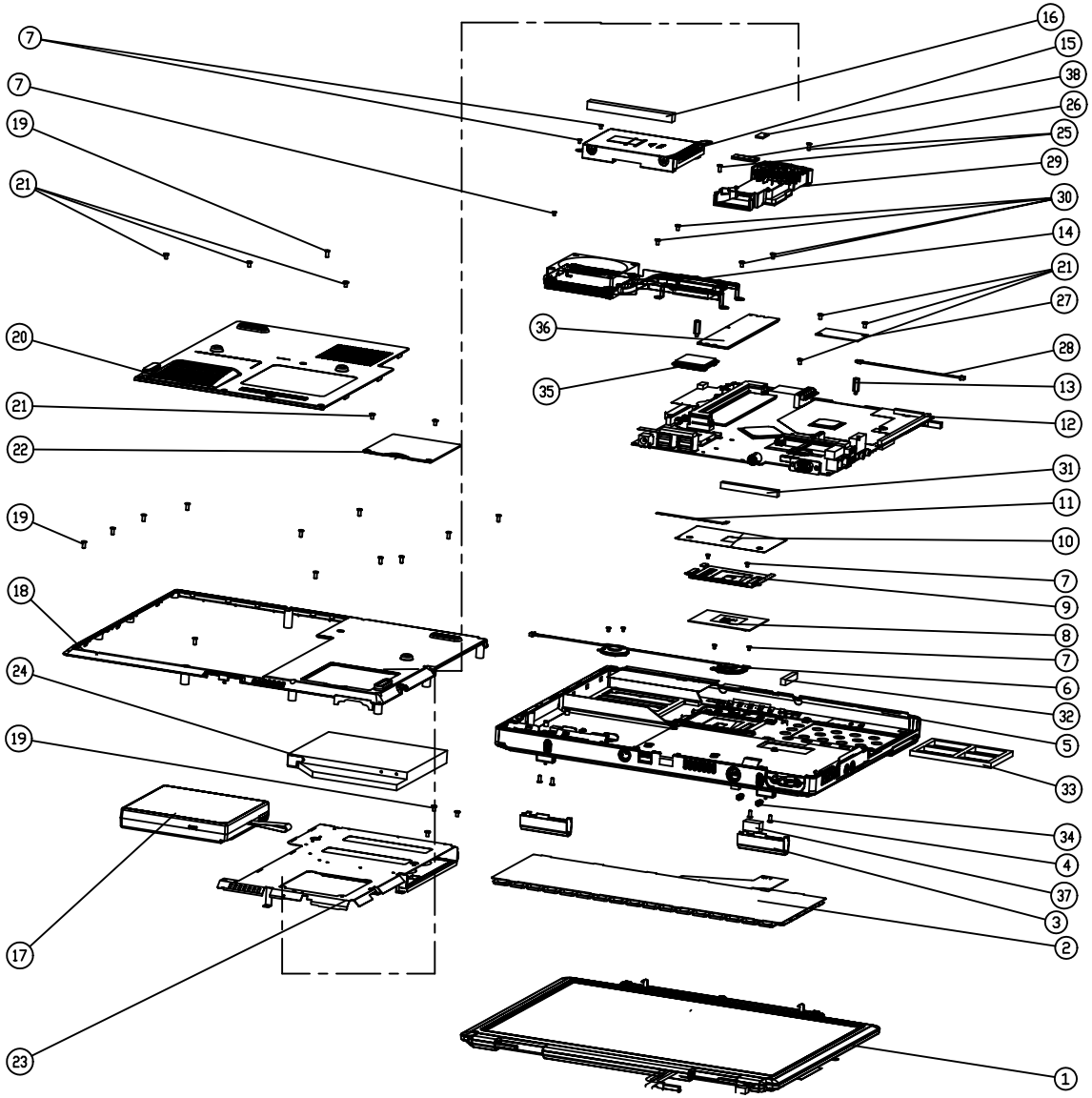
9. Spare Parts List

Spare Part List 11

Part Number	Description	Location(S)
441684410004	BATT ASSY;14.8V,4.0Ah,LI,CASE CL	
441684410005	BATT ASSY;14.8V,4.0Ah,LI,CORE PA	
441684410006	CONTACT PLATE ASSY;W5L45T0.13,FU	
441684410007	CONTACT PLATE ASSY;PTC,S-TUBE,BL	
441999900330	BATT ASSY OPTION;LI,8-CELL,ID1,8	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PU	
442682900021	AC ADPT ASSY;19V,6.32A,DELTA ADP	
451682900001	HDD ME KIT;8599	
451682900003	LCD ME KIT;15",XGA,Hannstar,8599	
451682900005	ROM ME KIT;8599	
451682900006	LABEL KIT;N-B,w/o Intel Inside L	
451682900007	HOUSING KIT;8599	
461677400001	PACKING KIT;DA-1A05-A;PWR	
461682900002	PACKING KIT;COMPACT,N-B,8599	
481682900001	F/W ASSY;SYS/VGA BIOS,8599	U23
481682900002	F/W ASSY;KBD CTRL,8599	U17
523402379051	HDD DRIVE;40GB,2.5",MHT2040AT,V4	
523430061010	DVD COMBO DRIVE;24X10X8X24,SBW-2	
523468290002	COMBO ASSY;SBW-242B,8599	
523468290005	HDD ASSY;FUJITSU,MHS2040AT,8599	
526268290006	LTXNX;8599/5RYB/40C/1UI9/A1D2A/X	
531010570032	KBD;88,UI,5035,BTC,8599	
561568290002	MANUAL;QSG,EN,8599	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	

Part Number	Description	Location(S)
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	

P/N:526268290006



SCALE 0.200

ITEM	PART NO	PART NAME	Q'TY	TYPE	MARK
38	345684500004	RUBBER;SYSTEM HEATSINK,TARZAN	1	part	
37	345682900009	SPONGE;HINGE COVER,8599	1	part	
36	323768290001	DDR SDRAM MODULE ;512MB,184PIN,DDR400,77.103736.464,APACER	1	part	OPTION
35	324180786587	IC;CPU,P4-NORTHWOOD,3.06G,FSB 533,MICRO_FCPGA,478P	1	part	OPTION
34	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	2	part	
33	344672300025	DUMMY CARD;PCMCIA,MANGUSTA	1	part	
32	347105060030	GASKET;1,05,060,030	1	part	
31	347105060060	GASKET;1,05,060,060	1	part	
30	370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,t0.8	4	part	
29	340682900019	HAETSINK ASSY;SYSTEM,M/B,MPT,8599	1	asm	OPTION
28	421676400001	WIRE ASSY,MDC-MODEM,APOLLON	1	asm	
27	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	asm	
26	347110020025	GASKET;1,10,020,025	1	part	
25	371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	2	part	
24	523468290001	DVD+RW ASSY;SDW-041,8599	1	asm	OPTION
23	340682900016	SHIELDING ASSY;BOTTOM,8599	1	asm	
22	340682900018	COVER ASSY;MINIPCI,8599	1	asm	
21	371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	8	part	
20	340682900017	COVER ASSY;CPU,8599	1	asm	
19	371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	16	part	
18	340682900015	HOUSING ASSY;BOTTOM,8599	1	asm	
17	441999900321	BATT ASSY OPTION;LI,8-CELL,8599	1	asm	OPTION
16	347108080090	GASKET;1,08,080,090	1	part	
15	523468290004	HDD ASSY;HITACHI,IC25N040ATMR04,8599	1	asm	OPTION
14	340682900013	HEATSINK ASSY;CPU,NORTHWOOD,MPT,8599	1	asm	OPTION
13	377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NYLOK	2	part	
12	411682900001	PWA;PWA-8599,MOTHER BD (A)	1	asm	OPTION
11	422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,8599	1	asm	OPTION
10	346682900009	AL-FOIL;T/P BRACKET,8599	1	part	
9	340682900009	BRACKET ASSY;TOUCH-PAD,8599	1	asm	
8	442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PUM1950	1	part	
7	371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,NIW	9	part	
6	340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHIUN,8599	1	asm	OPTION
5	340682900007	COVER ASSY;TOP,8599	1	asm	
4	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	part	
3	344682900012	COVER;HINGE,8599	2	part	
2	531020237940	KBD;88,UI,K080818G1,8599	1	part	OPTION
1	441682900002	LCD ASSY;15",XGA,SAMSUNG,8599	1	asm	OPTION

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± / RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	24-03-04	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.2	DRAWING NAME	LT PF;15",XGA,SAMSUNG,8599	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416268290001 R00

MiTAC Technology Corp.

model name8599_MAIN_ASSY

file name:DRW_8599_MAIN_ASSY

MODEL : 8599 Revision 06

Contexts

Title	Page
COVER SHEET & SCREW HOLE	1
System Block Diagram	2
Power Block Diagram	3
Prescott/Northwood (1/2)	4
Prescott/Northwood (2/2)	5
SIS M661FX(1/2)	6
SIS M661FX(2/2)	7
TV/LVDS ENCODER(SiS301LV)	8
DDR DIMMs	9
LCD&VGA Interface	10
Clock Generator/Buffer	11
SIS963L (1/3)	12
SIS963L (2/3)	13
SIS963L (3/3)	14
IDE Interface	15
PCMCIA (Ti PCI1410A)	16
LAN PHY (ICS1883AF) & MDC	17
USB 2.0 & Flash ROM	18
AUDIO CODEC	19
KBC (W83L950D)	20
MiNi-PCI & USB 2.0	21
Charge board	22
DC Connector	23
Battery Connector	24
+5V,+3V,+1.8V,+1.5V	25
+2.5V,1.25V,1.8VS	26
CPU_CORE1	27
CPU_CORE2	28
	29
	30
	31
	32
	33
	34

POWER STATES

STATE / SIGNAL	VOTAGE	POWER ON	STR	STD	MEC-OFF	REMARK
H8_SUSB	-	HIGH	LOW	LOW	LOW	
H8_SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
+VCC_CORE	+1.75V	O	X	X	X	
+12V	+12V	O	O	X	X	
+12VS	+12V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VS	+5V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3VS	+3.3V	O	X	X	X	
+2.5V_DDR	+2.5V	O	O	X	X	
+1.8V	+1.8V	O	O	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.25VS_DDR	+1.25V	O	X	X	X	
+5VA	+5V	O	O	O	O	
+3VA	+3.3V	O	O	O	O	
+3VAS	+3.3V	O	O	O	X	

IDSEL

IDSEL	CHIP
AD11	SiS 963
AD12	PCI to PCI Bridge
AD13	AC'97 Codec
AD14	USB
AD15	MII
AD20	Ti PCI1410A
AD21	MiniPCI

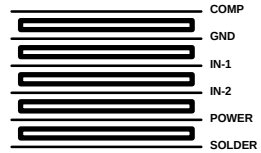
BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	Ti PCI1410
-REQ2/-GNT2	MINI PCI

PCIINT

PCIINT	CHIP
INTA#	SiS 301LV
INTB#	PCMCIA (PCI1410A)
INTC#	MINI PCI
INTD#	MINI PCI

Board Stackup-up



DRAW	DESIGN	CHECK	ISSUED

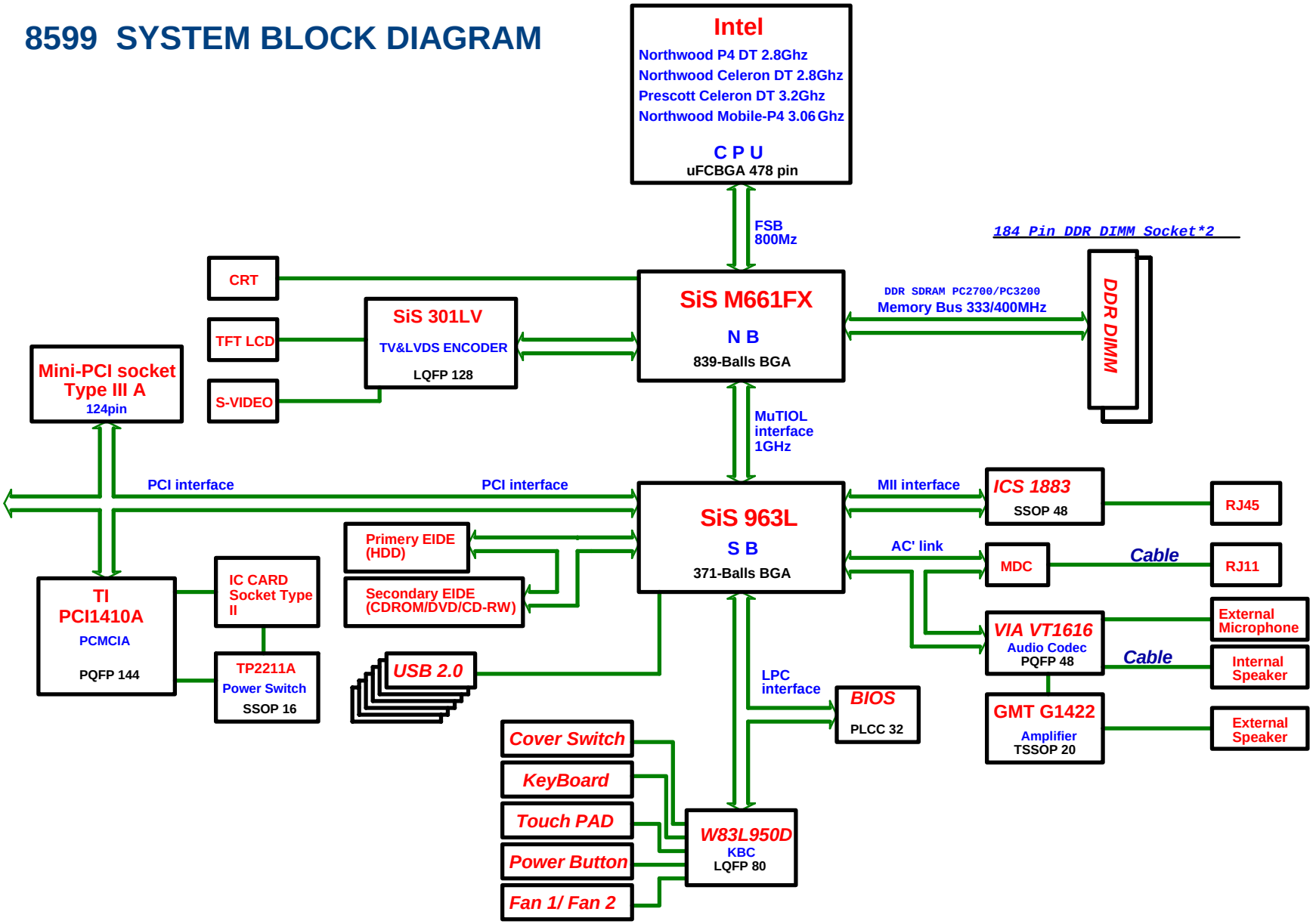
MiTAC

Title: COVER SHEET

Size | Document Number: 411682900001 | Rev: R06

Date: Monday, April 12, 2004 | Sheet 1 of 28

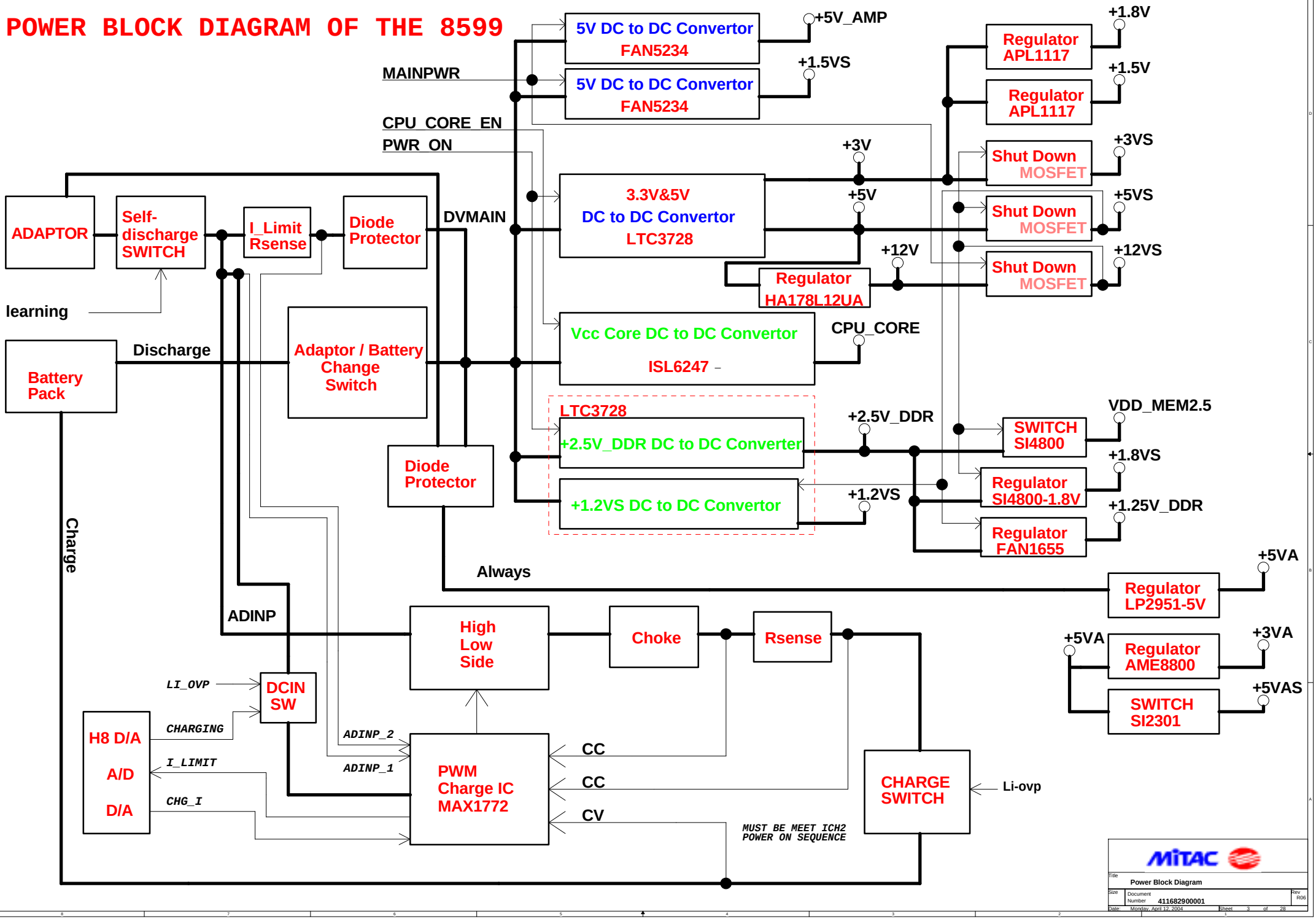
8599 SYSTEM BLOCK DIAGRAM



MiTAC

Title	SystemBlock DIAGRAM	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 2 of 28	

POWER BLOCK DIAGRAM OF THE 8599



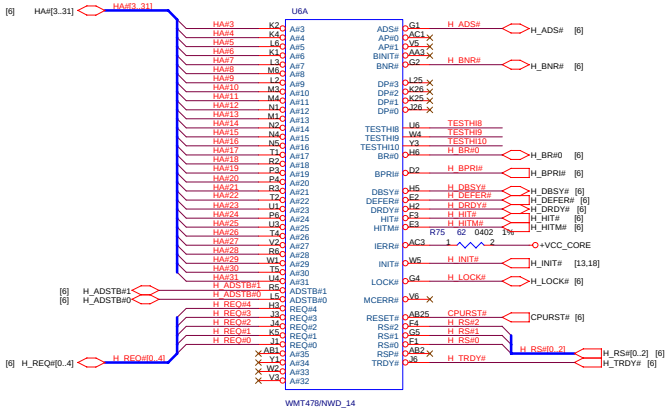
MiTAC

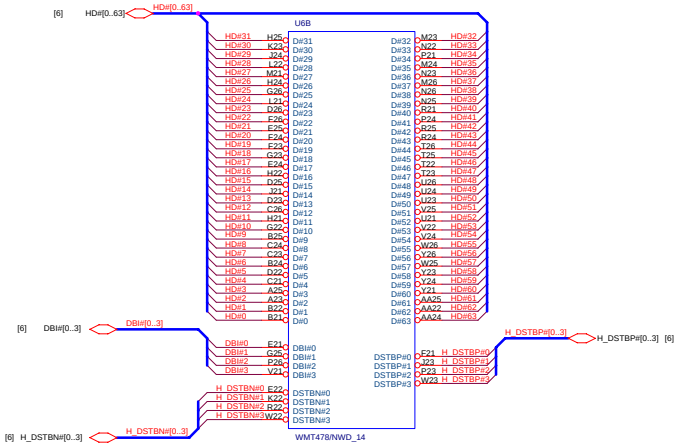
Title: Power Block Diagram

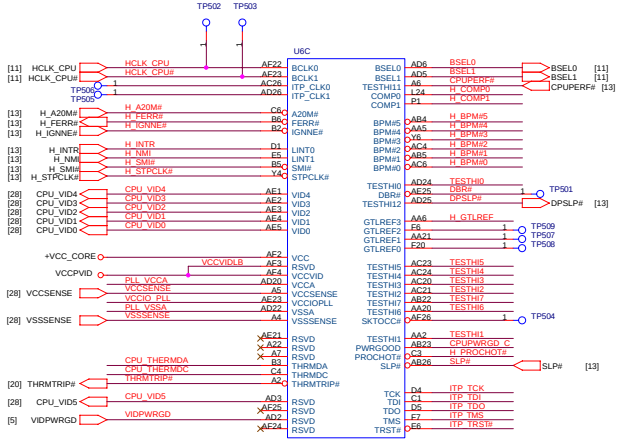
Size | Document Number: 411682900001 | Rev: R06

Date: Monday, April 12, 2004 | Sheet 3 of 28

Prescott/Northwood (1/2)





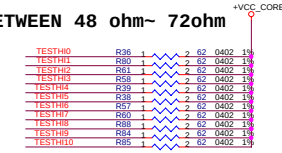


FSB SELECTION

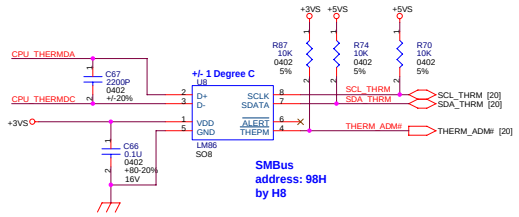
BSEL1	BSEL0	FUNCTION
0	0	100MHz
0	1	133MHz
1	0	200MHz
1	1	RESERVED

Mobile P4 533MHz impedance is 50 between 40~60 ohm.

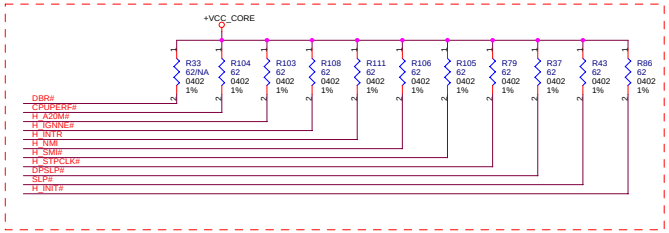
BETWEEN 48 ohm~ 72ohm

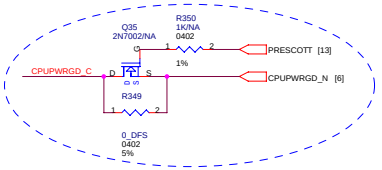


CPU Temperature Monitor

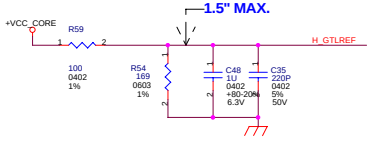


Placement : 3" (Maximum) From CPU

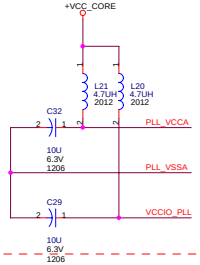




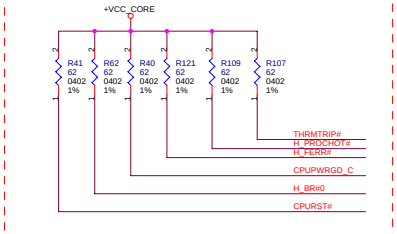
GTL Reference CKT



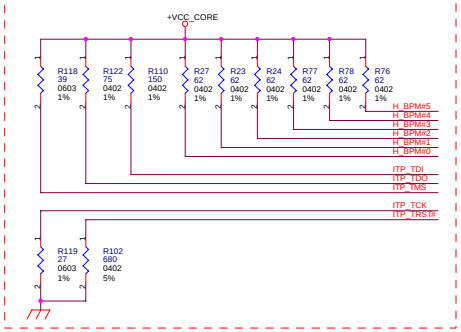
PLL SUPPLY FILTER



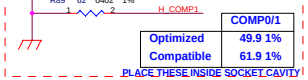
CPU SIGNAL TERMINATION



PLACE CLOSE TO CPU SOCKET



PRECISION FSB COMPENSATION RESISTORS



COMP0/1	
Optimized	49.9 1%
Compatible	61.9 1%

PLACE THESE INSIDE SOCKET CAVITY

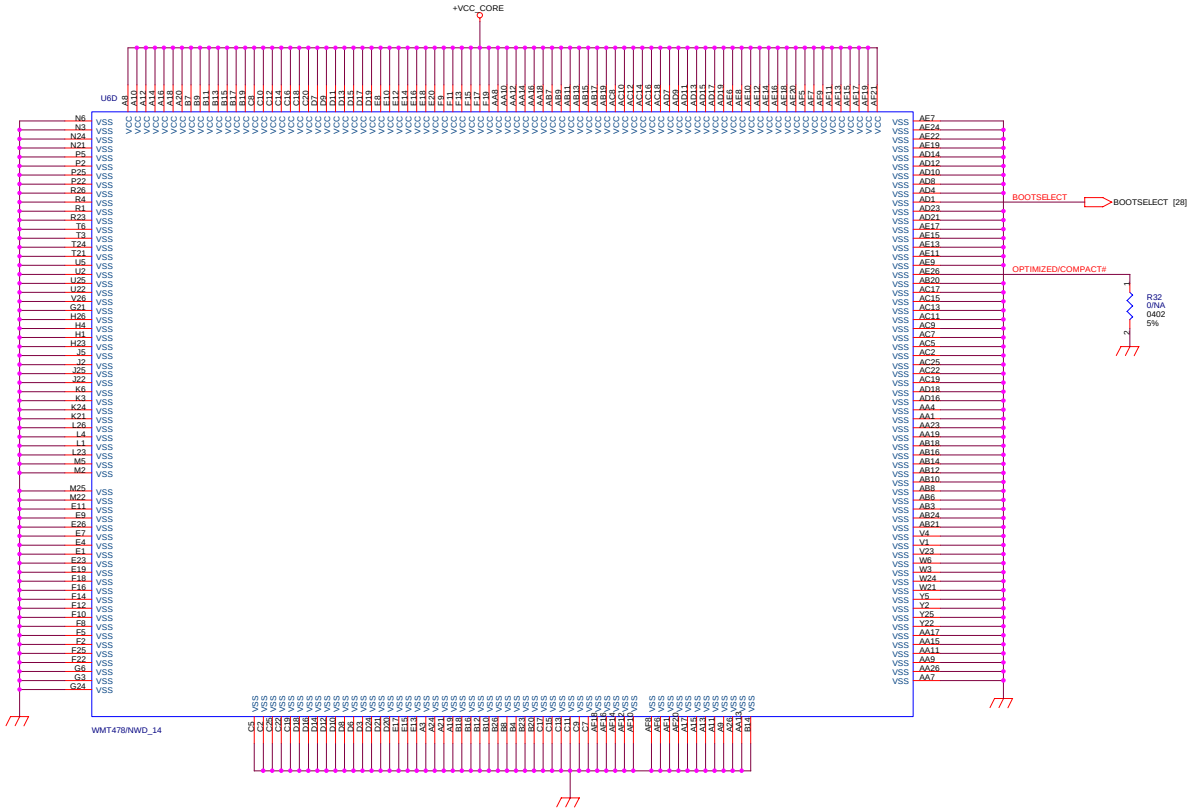
MiTAC

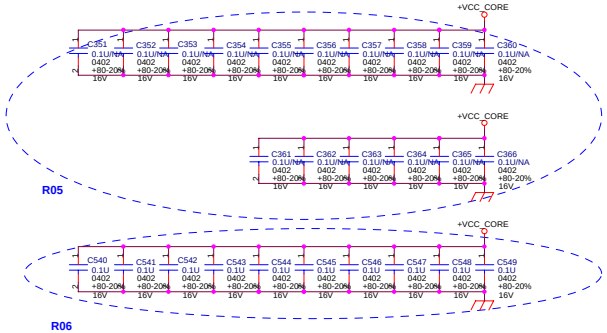
Title: Prescott/Northwood (1/2)

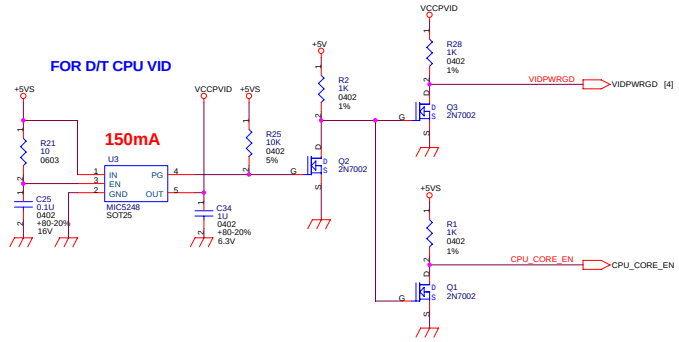
Size: | Document Number: 411682900001 | Rev: R06

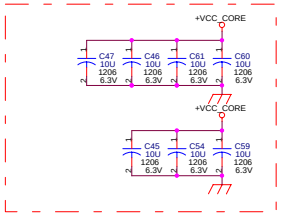
Date: Monday, April 12, 2004 | Sheet 4 of 28

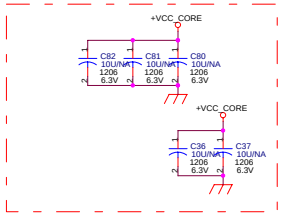
Prescott/Northwood (2/2)

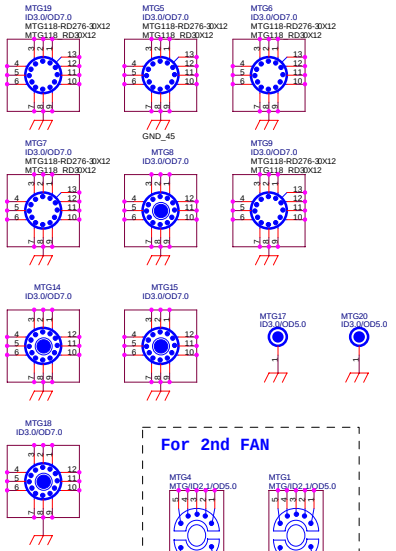


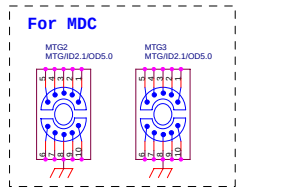


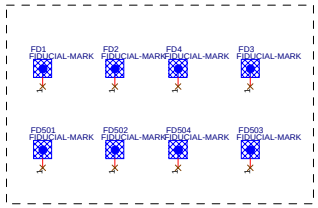








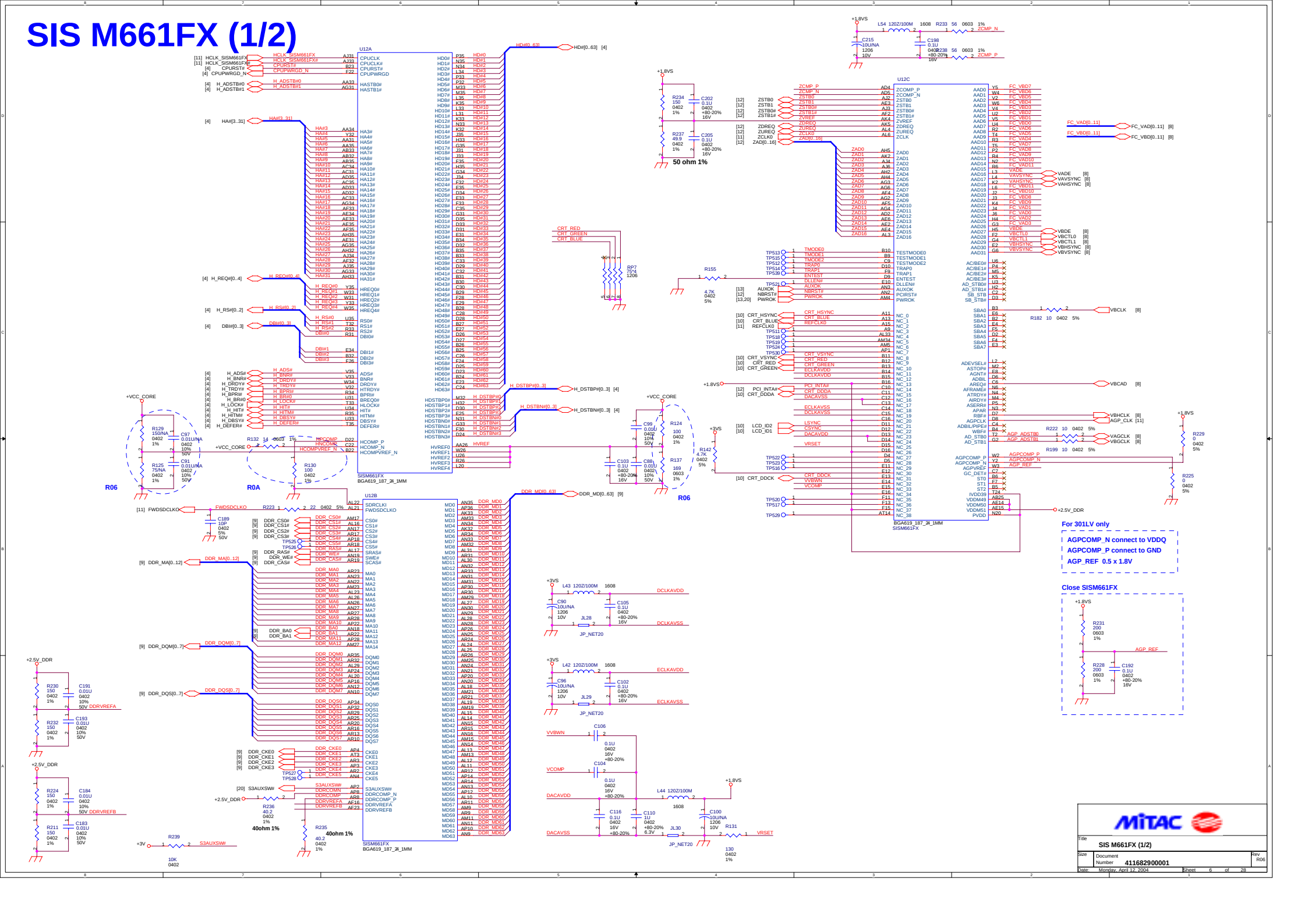




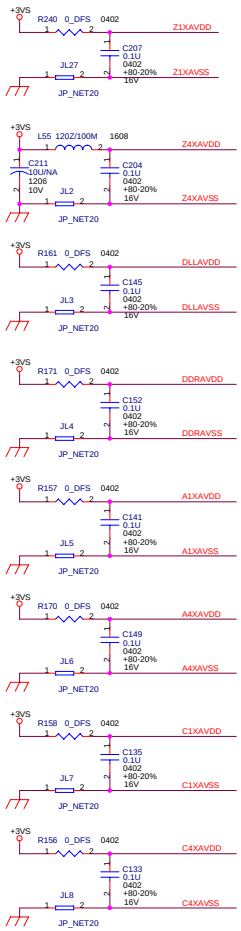
MiTAC

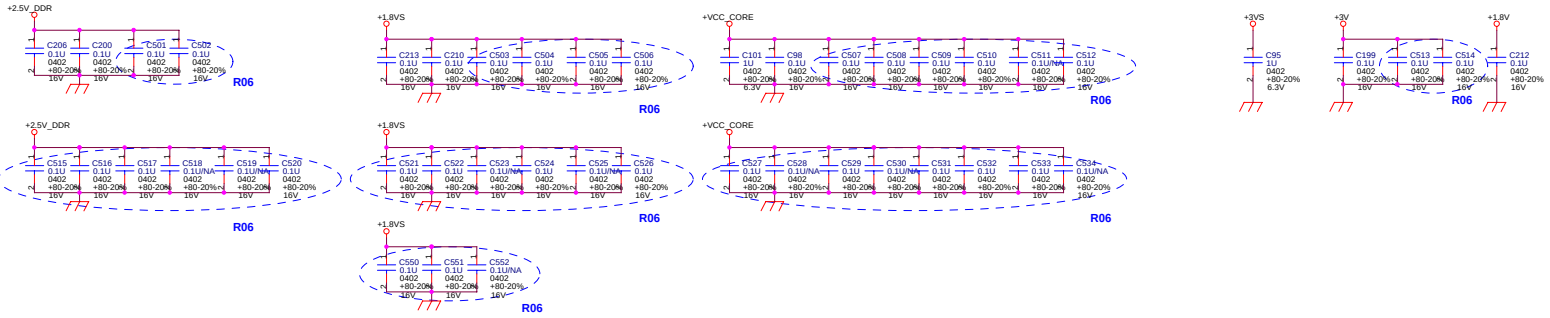
Title	Prescott/Northwood (2/2)
Size	Document Number 411682900001 Rev R06
Date: Monday, April 12, 2004	Sheet 5 of 28

SIS M661FX (1/2)



SIS M661FX (2/2)

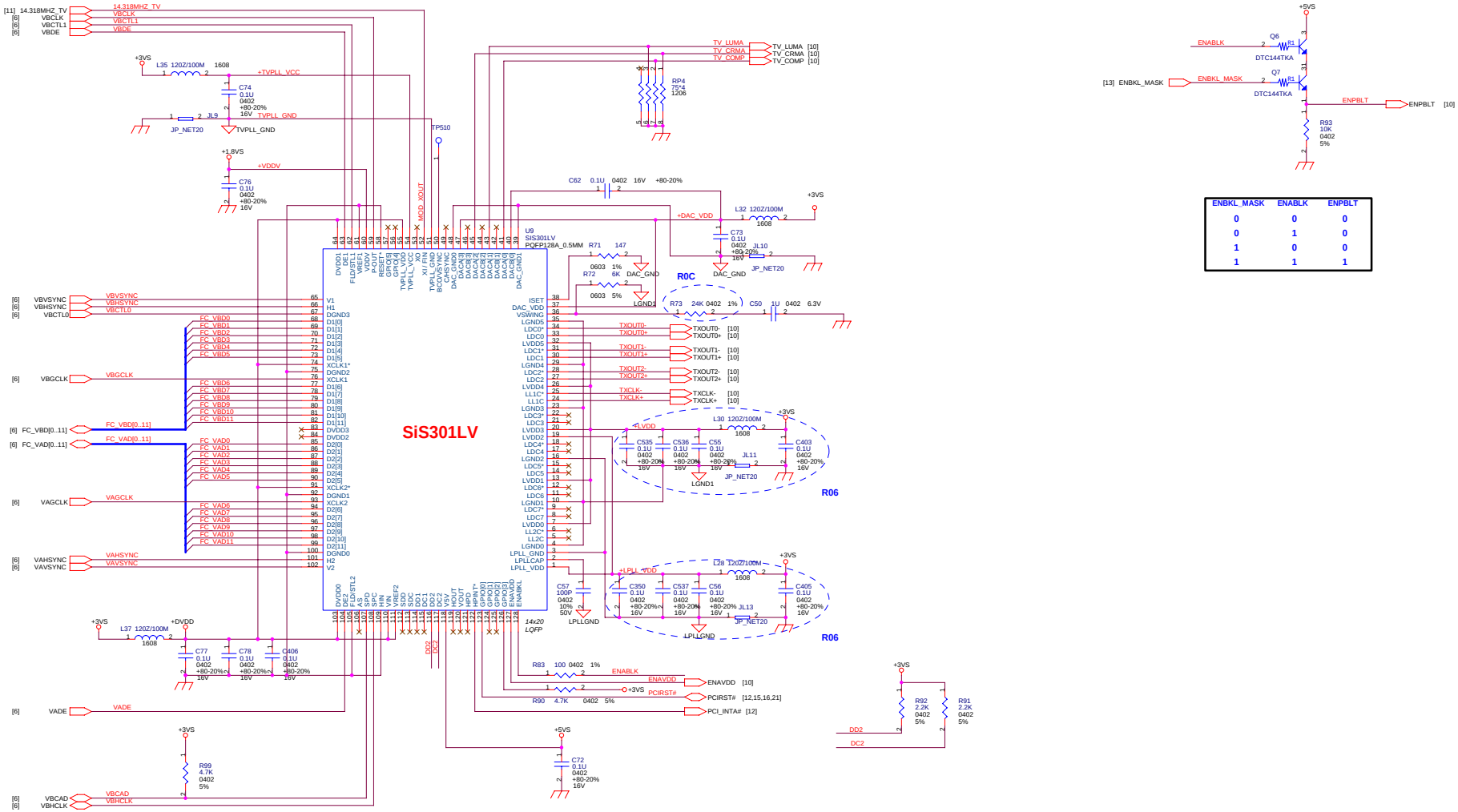




MiTAC

Title	SIS M661FX (2/2)	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 7 of 28	

TV/LVDS ENCODER (SIS301LV)



ENBKL_MASK	ENABLK	ENPBLT
0	0	0
0	1	0
1	0	0
1	1	1

Title	TV/LVDS ENCODER (SIS301LV)	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 8 of 28	

DDR DIMMs

SMBus address: A0h by BIOS

SMBus address: A2h by BIOS

Lower DIMM BANK0/1

Upper DIMM BANK2/3

PLACE CLOSE TO DDR socket

Difference	CLK	CKE	CS
Upper DIMM	CK0/0# ==> CLK_DDR3/3# CK1/1# ==> CLK_DDR4/4# CK2/2# ==> CLK_DDR5/5#	CKE0/1 ==> CKE2/3	CS0#/1# ==> CS2#/3#
Lower DIMM	CK0/0# ==> CLK_DDR0/0# CK1/1# ==> CLK_DDR1/1# CK2/2# ==> CLK_DDR2/2#	CKE0/1 ==> CKE0/1	CS0#/1# ==> CS0#/1#

THESE DECOUPLING CAPACITOR SHOULD BE PLACE WITHIN 150 Mils OF +1.25V THERMINATION R-PACKs

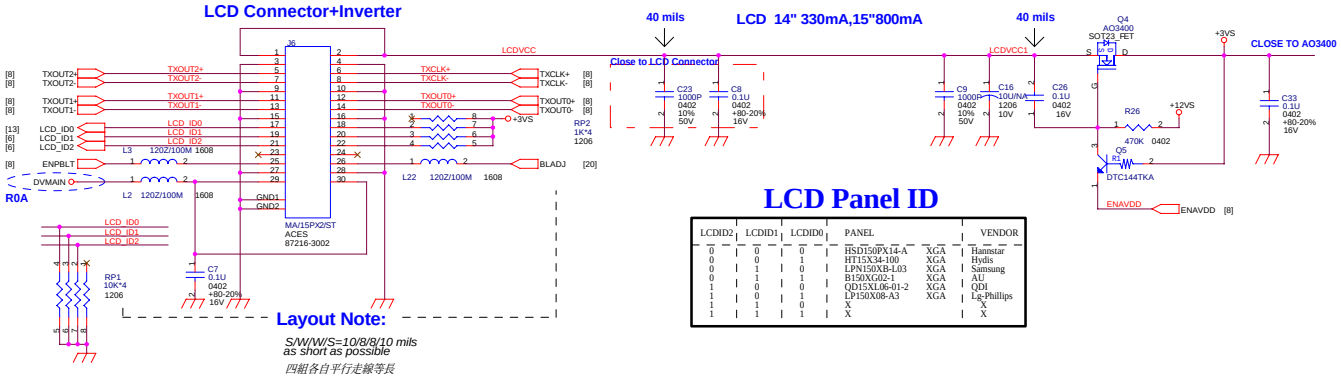
MiTAC

Title: DDR DIMMs

Size: Document Number 411682900001 Rev R06

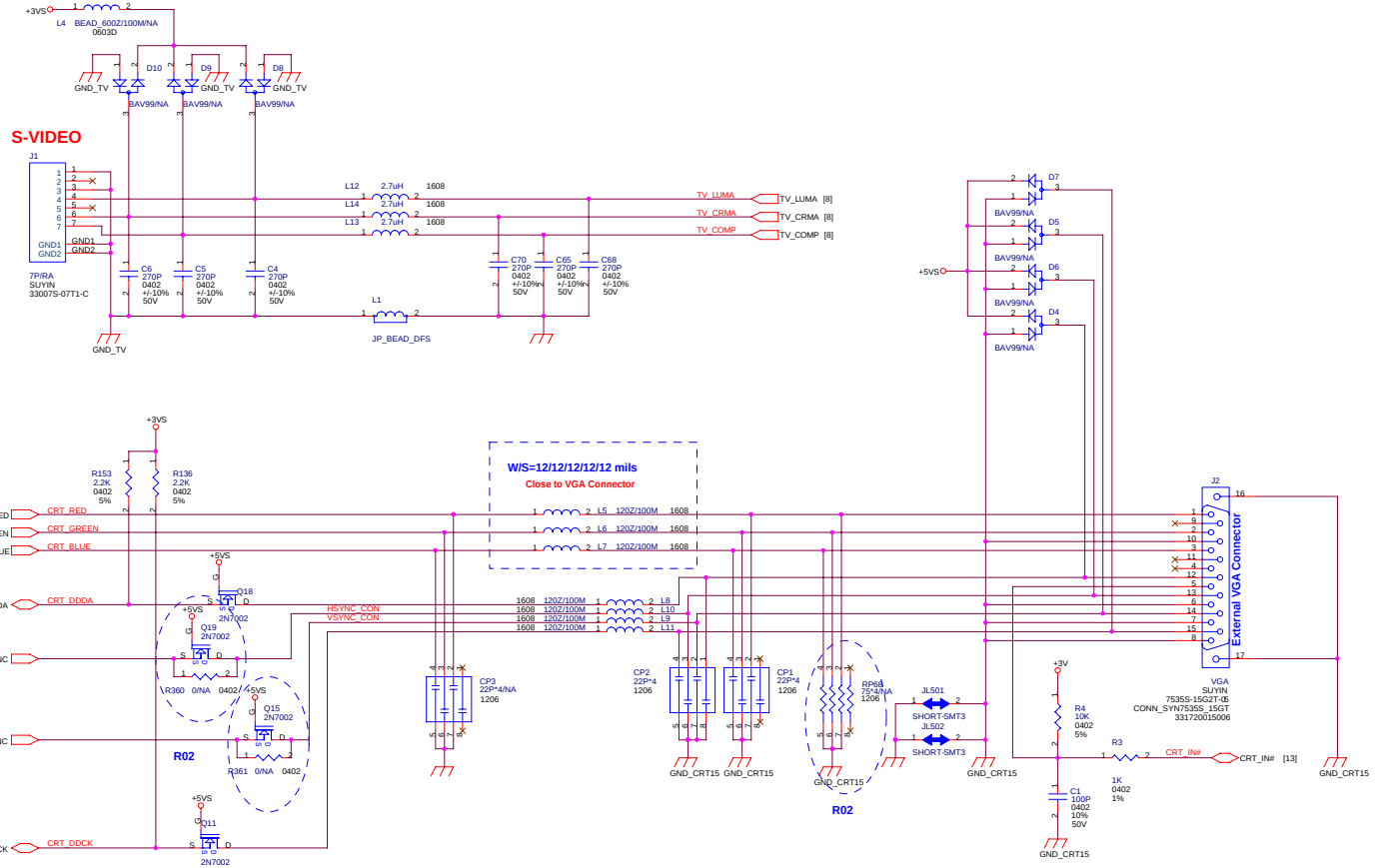
Date: Monday, April 12, 2004 Sheet 9 of 28

LCD / VGA Interface



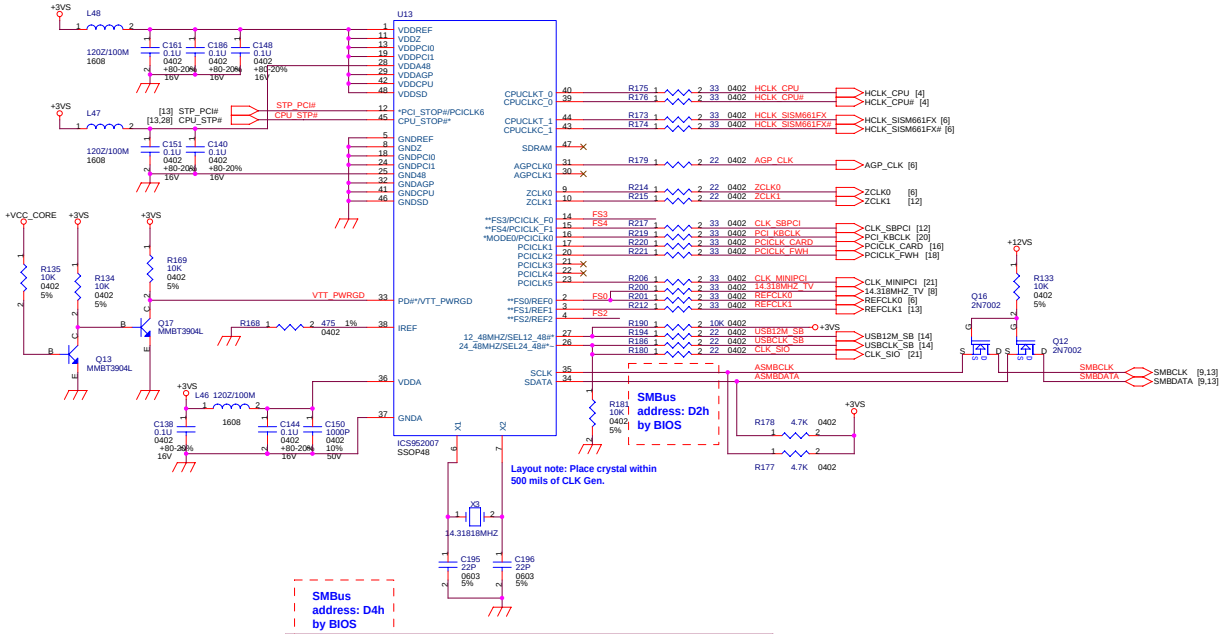
LCD Panel ID

LCDID2	LCDID1	LCDID0	PANEL	VENDOR
0	0	0	HSD150PX14-A XGA	Hannstar
0	0	1	HT15X34-100 XGA	Hydis
0	1	0	LPN150XB-L03 XGA	Samsung
0	1	1	B150XG02-1 XGA	AU
1	0	0	QD15XL06-01-2 XGA	QDI
1	0	1	LP150X08-A3 XGA	Lg-Phillips
1	1	0	X	X
1	1	1	X	X



Clock Generator/Buffer

* INTERNAL PULL UP RESISTOR
** INTERNAL PULL DOWN RESISTOR
~ THIS OUTPUT HAS 1.5X DRIVE STRENGTH



For ICS952011

Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	0	100.20	100.20	66.8	66.8	33.4
0	0	0	0	1	100.20	133.60	66.8	66.8	33.4
0	0	0	1	0	100.20	200.4	66.8	66.8	33.4
0	0	0	1	1	100.20	167.00	66.8	66.8	33.4
0	0	1	0	0	133.60	100.20	66.8	66.8	33.4
0	0	1	0	1	133.60	133.60	66.8	66.8	33.4
0	0	1	1	0	133.60	200.40	66.8	66.8	33.4
0	0	1	1	1	133.60	167.00	66.8	66.8	33.4
0	1	0	0	0	200.05	100.03	66.68	66.68	33.34
0	1	0	0	1	200.05	133.37	66.68	66.68	33.34
0	1	0	1	0	200.05	200.05	66.68	66.68	33.34
0	1	0	1	1	200.05	160.04	66.68	66.68	33.34
0	1	1	0	0	166.70	100.20	66.68	66.68	33.34
0	1	1	0	1	166.70	133.36	66.8	66.8	33.4
0	1	1	1	0	160.04	200.05	66.68	66.68	33.34
0	1	1	1	1	166.7	166.7	66.68	66.68	33.34
1	0	0	0	0	100.20	100.02	133.60	66.8	33.4
1	0	0	0	1	100.20	133.60	133.60	66.8	33.4
1	0	0	1	0	100.20	200.40	133.60	66.8	33.4
1	0	0	1	1	100.20	167.00	133.60	66.8	33.4
1	0	1	0	0	133.60	100.20	133.60	66.8	33.4
1	0	1	0	1	133.60	133.60	133.60	66.8	33.4
1	0	1	1	0	133.60	200.40	133.60	66.8	33.4
1	0	1	1	1	133.60	167.00	133.60	66.8	33.4
1	1	0	0	0	200.05	100.03	133.37	66.68	33.34
1	1	0	0	1	200.05	133.37	133.37	66.68	33.34
1	1	0	1	0	200.05	200.05	133.37	66.68	33.34
1	1	0	1	1	200.05	160.04	133.37	66.68	33.34
1	1	1	0	0	166.70	100.20	133.60	66.68	33.4
1	1	1	0	1	166.70	133.36	133.60	66.8	33.4
1	1	1	1	0	160.04	200.05	133.37	66.68	33.34
1	1	1	1	1	166.70	166.70	133.37	66.68	33.34

NON USE

BSEL1	BSEL0	FREQ
L	L	100MHz
L	H	133MHz
H	L	200MHz
H	H	RSVD

DEFAULT

For ICS952007

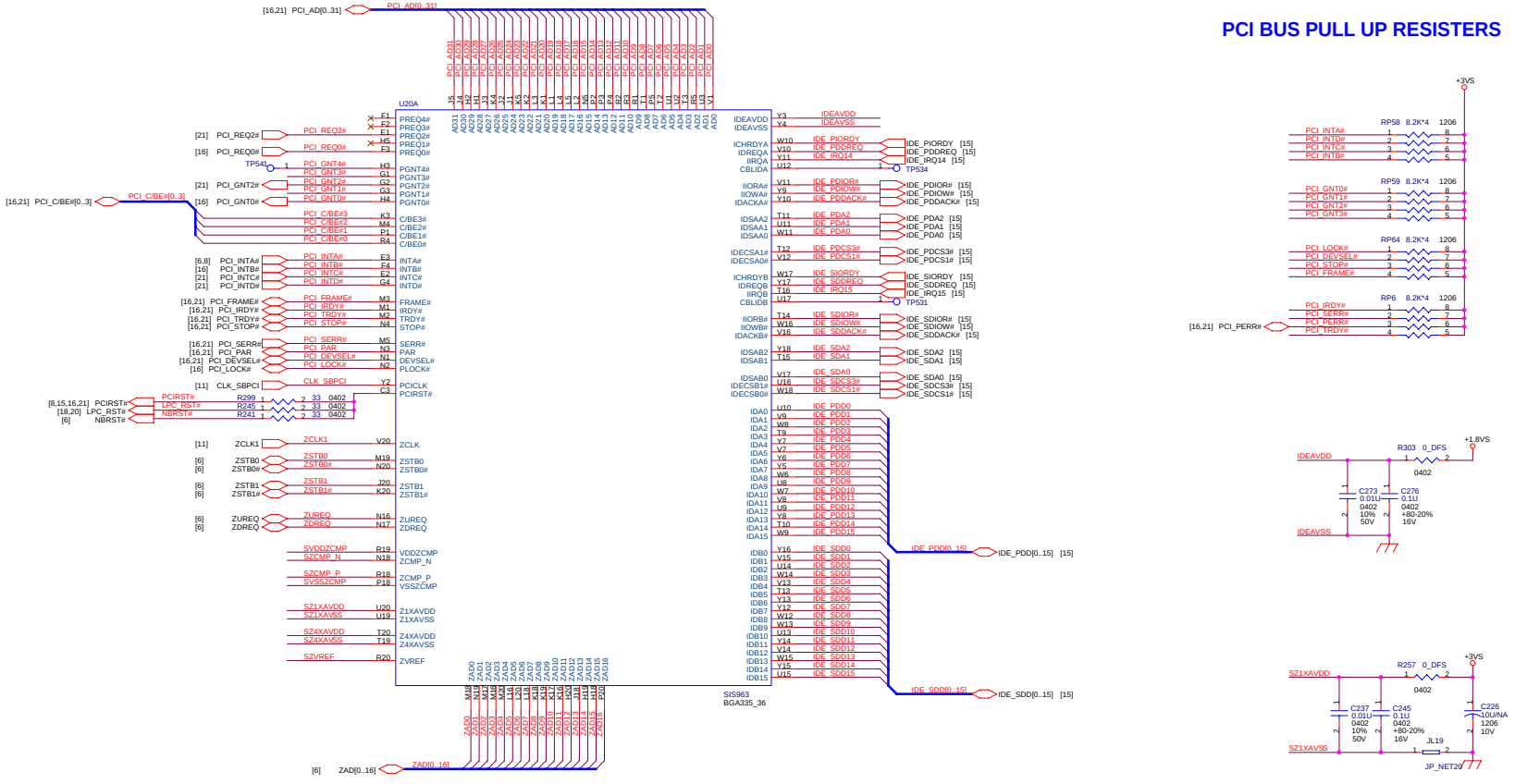
Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	0	100.00	100.00	133.33	66.66	33.33
0	0	0	0	1	100.00	133.00	133.00	66.67	33.33
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	0	1	0	0	133.33	133.33	133.33	66.66	33.33
0	0	1	0	1	133.00	133.00	133.00	67.33	33.00
0	0	1	1	0	137.33	137.33	137.33	68.66	34.33
0	0	1	1	1	133.33	133.33	133.33	66.67	33.33
0	1	0	0	0	200.00	200.00	133.33	66.67	33.33
0	1	0	0	1	201.00	201.00	134.00	67.33	33.00
0	1	0	1	0	206.00	206.00	137.33	68.67	34.33
0	1	0	1	1	200.00	200.00	133.33	66.67	33.33
0	1	1	0	0	200.00	150.00	133.33	66.66	33.33
0	1	1	0	1	199.01	199.01	134.00	67.33	33.00
0	1	1	1	0	171.66	171.66	137.33	68.66	34.33
0	1	1	1	1	166.66	166.66	133.33	66.66	33.33
1	0	0	0	0	100.20	100.02	133.60	66.79	33.40
1	0	0	0	1	105.00	105.00	140.00	69.99	35.00
1	0	0	1	0	107.00	107.00	142.66	71.33	35.66
1	0	0	1	1	110.00	110.00	146.66	73.33	36.66
1	0	1	0	0	133.60	133.60	133.60	66.79	33.40
1	0	1	0	1	140.00	140.00	140.00	69.99	35.00
1	0	1	1	0	142.66	142.66	142.66	71.33	35.66
1	0	1	1	1	146.66	146.66	146.66	73.33	36.66
1	1	0	0	0	200.40	200.40	133.60	66.79	33.40
1	1	0	0	1	210.00	210.00	140.00	69.99	35.00
1	1	0	1	0	214.00	214.00	142.66	71.33	35.66
1	1	0	1	1	220.00	220.00	146.66	73.33	36.66
1	1	1	0	0	166.99	166.99	133.60	66.79	33.40
1	1	1	0	1	174.99	174.99	140.00	69.99	35.00
1	1	1	1	0	178.33	178.33	142.66	71.33	35.66
1	1	1	1	1	183.33	183.33	146.66	73.33	36.66

NON USE

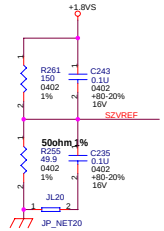
MiTAC

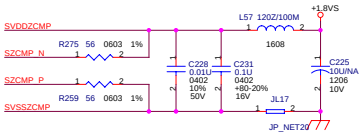
Title: Clock Generator/Buffer
Size: Document Number: 411682900001 Rev: R06
Date: Monday, April 12, 2004 Sheet 11 of 28

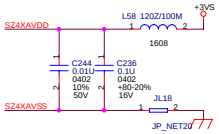
SIS963L (1/3)



PCI BUS PULL UP RESISTERS



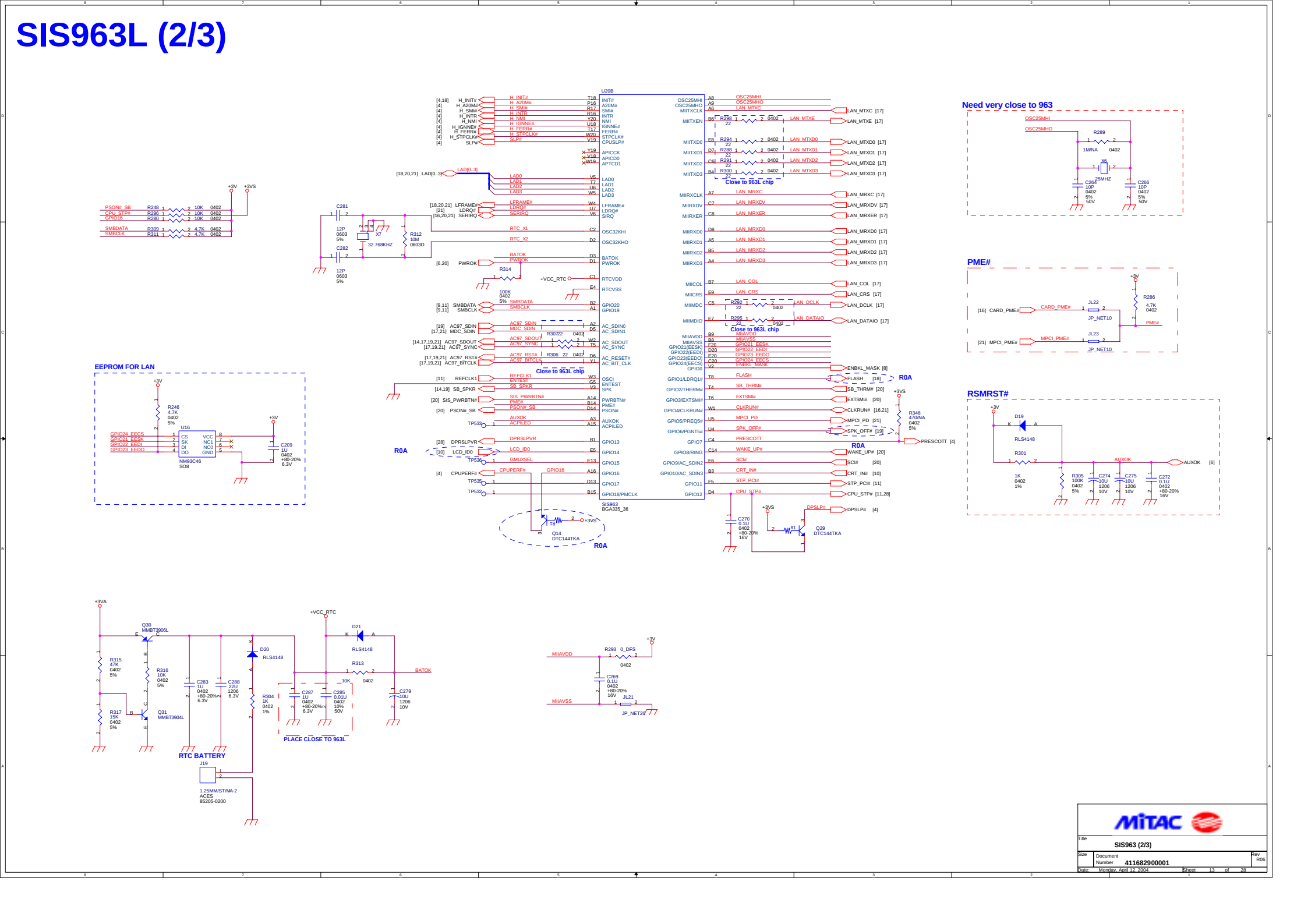




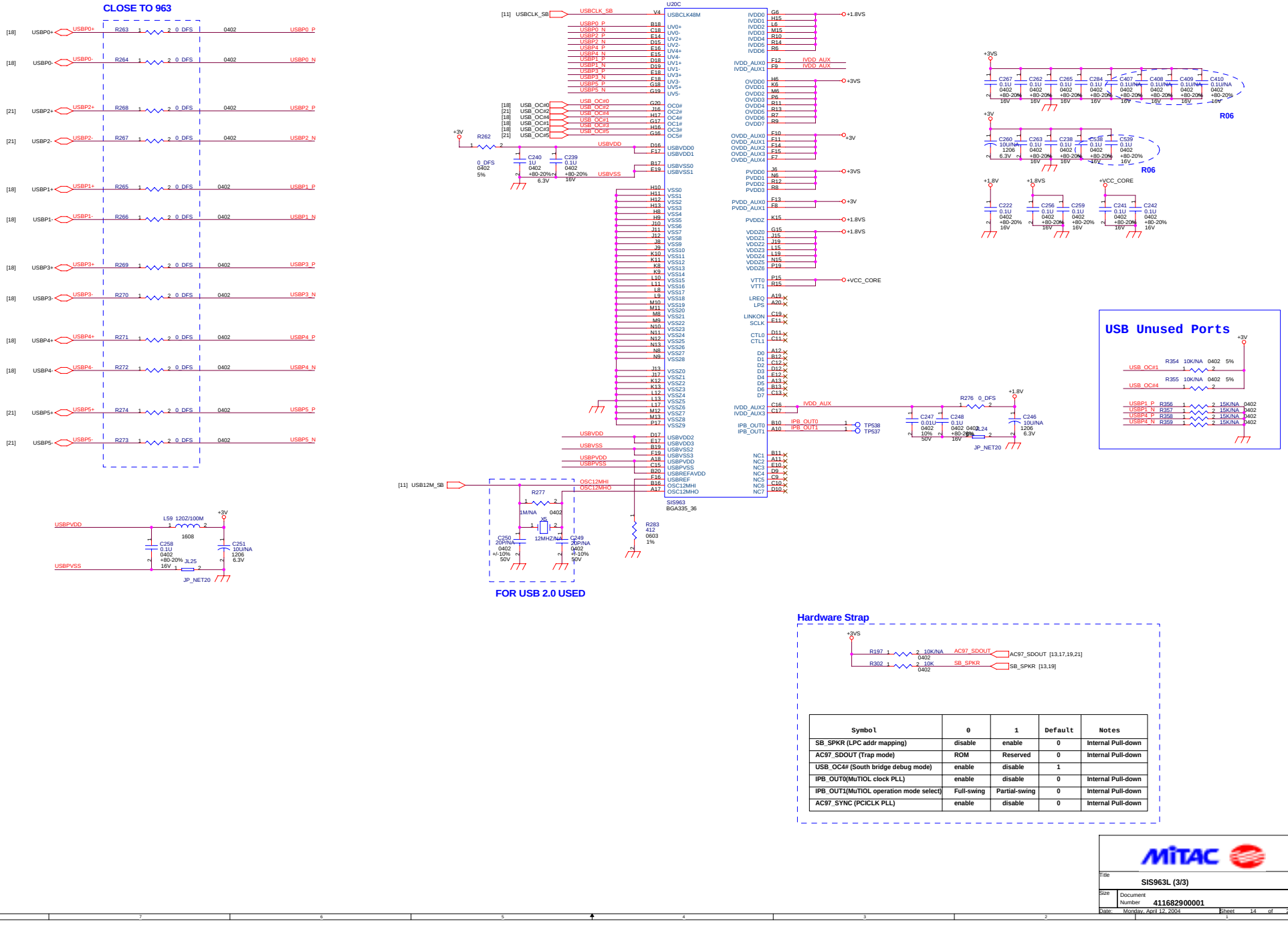
MiTAC

Title	SIS963 (1/3)	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 12 of 28	

SIS963L (2/3)


U20B
Close to 963L chip
EEPROM FOR LAN
NM93C46
SO8
RTC BATTERY
PLACE CLOSE TO 963L
Need very close to 963
PME#
RSMRST#
R0A
SIS963
BGA335_36
Title
SIS963 (2/3)
Document Number
411682900001
Rev
R06
Date: Monday, April 12, 2004
Sheet 13 of 28

SIS963L (3/3)



Symbol	0	1	Default	Notes
SB_SPKR (LPC addr mapping)	disable	enable	0	Internal Pull-down
AC97_SDOUT (Trap mode)	ROM	Reserved	0	Internal Pull-down
USB_OC4# (South bridge debug mode)	enable	disable	1	
IPB_OUT0(MuTIOL clock PLL)	enable	disable	0	Internal Pull-down
IPB_OUT1(MuTIOL operation mode select)	Full-swing	Partial-swing	0	Internal Pull-down
AC97_SYNC (PCICLK PLL)	enable	disable	0	Internal Pull-down

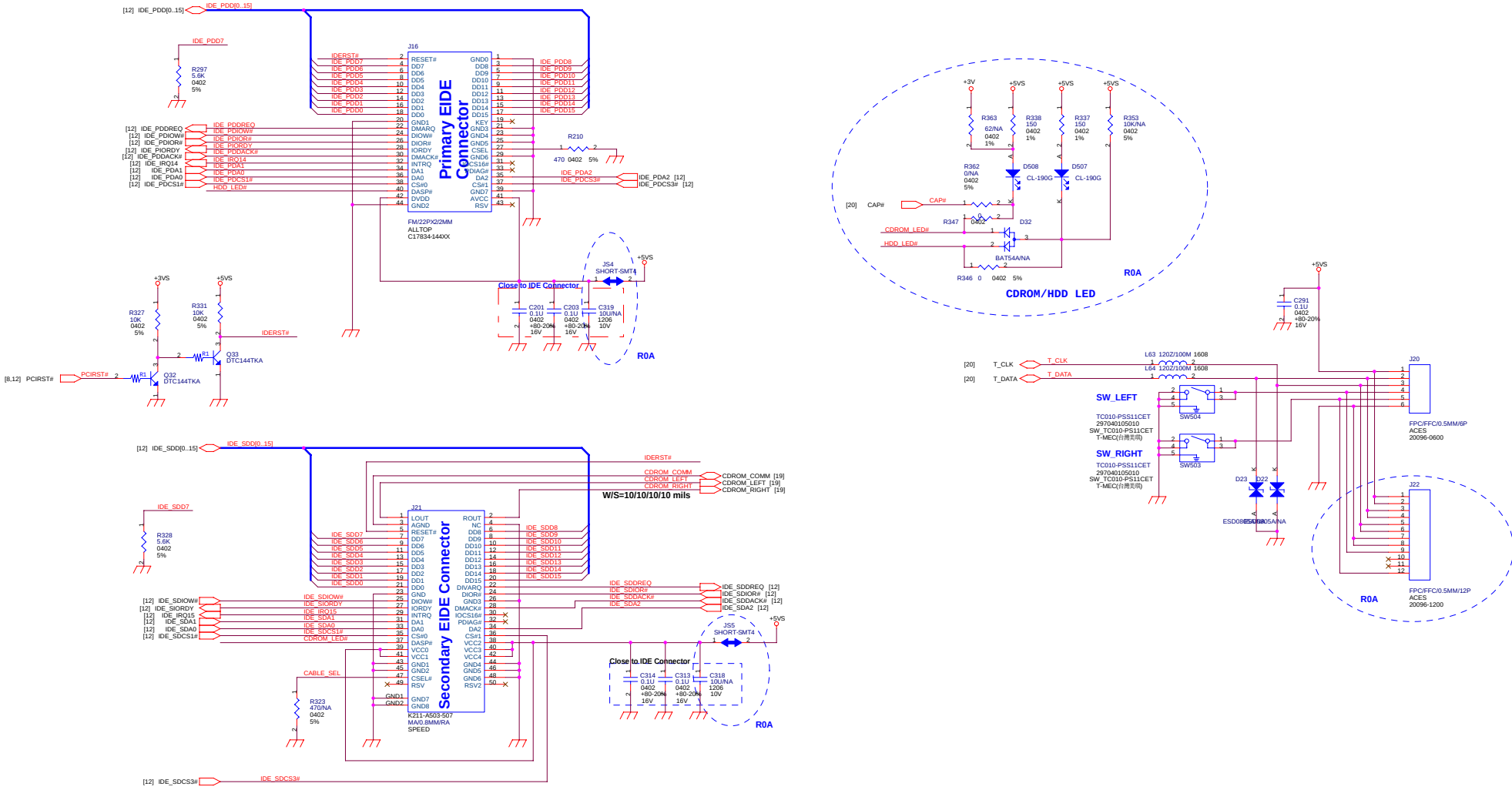
MiTAC

Title: SIS963L (3/3)

Size | Document Number: 411682900001 | Rev: R06

Date: Monday, April 12, 2004 | Sheet 14 of 28

IDE Interface



MiTAC

Title: IDE INTERFACE & IR

Size | Document Number: 411682900001 | Rev: R06

Date: Monday, April 12, 2004 | Sheet 15 of 28

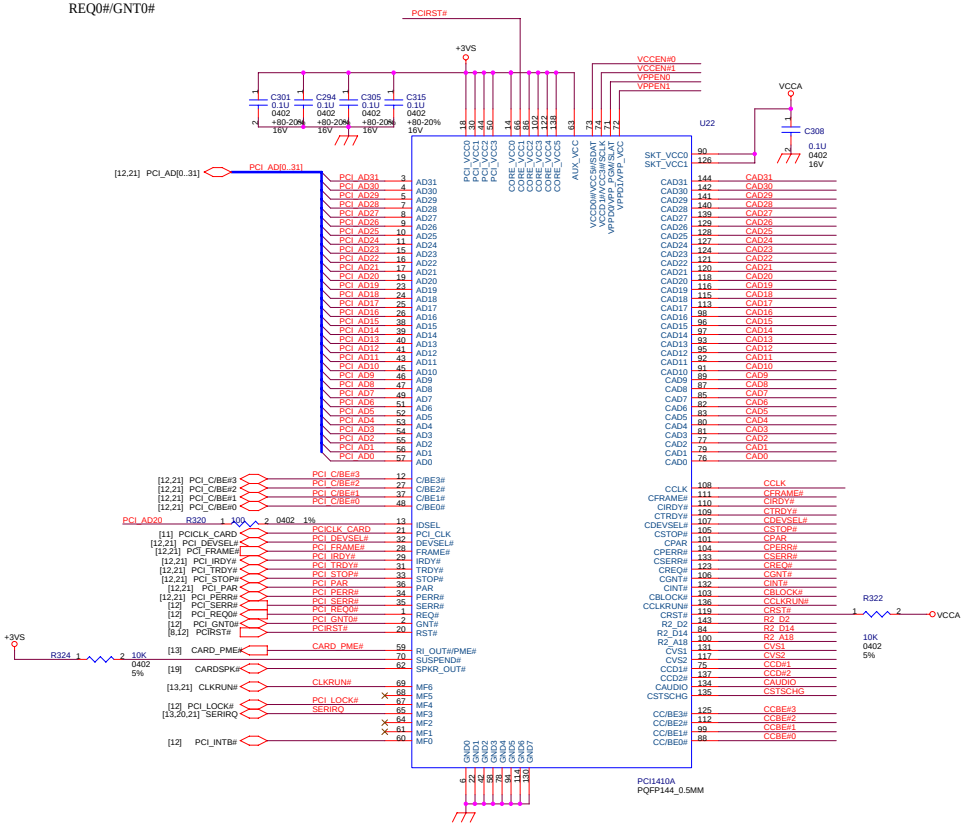
PCMCIA (Ti PCI1410A)

PCMCIA CONTROLLER & CARDBUS SCOKET

AD20

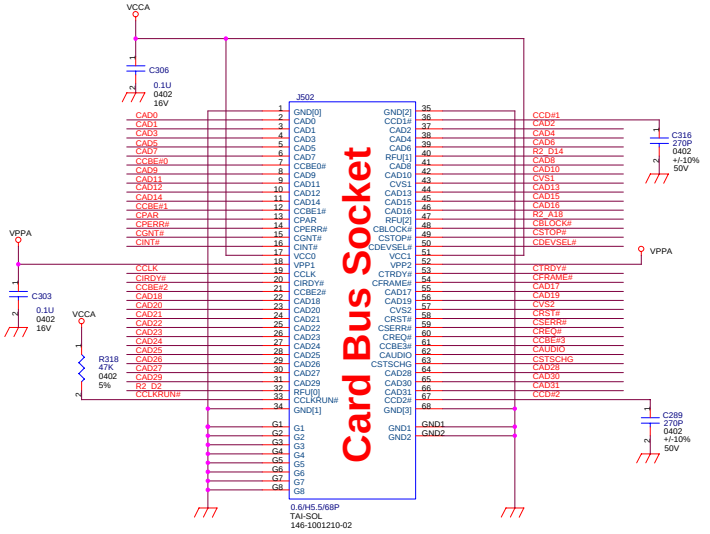
PCI_INTB#

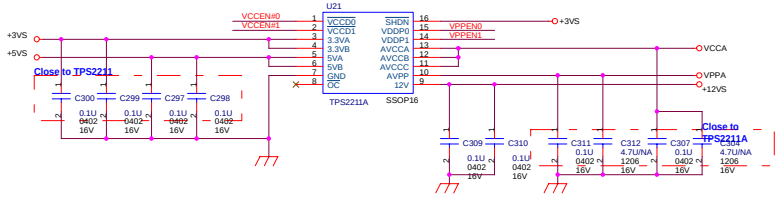
REQ0#/GNT0#



SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE





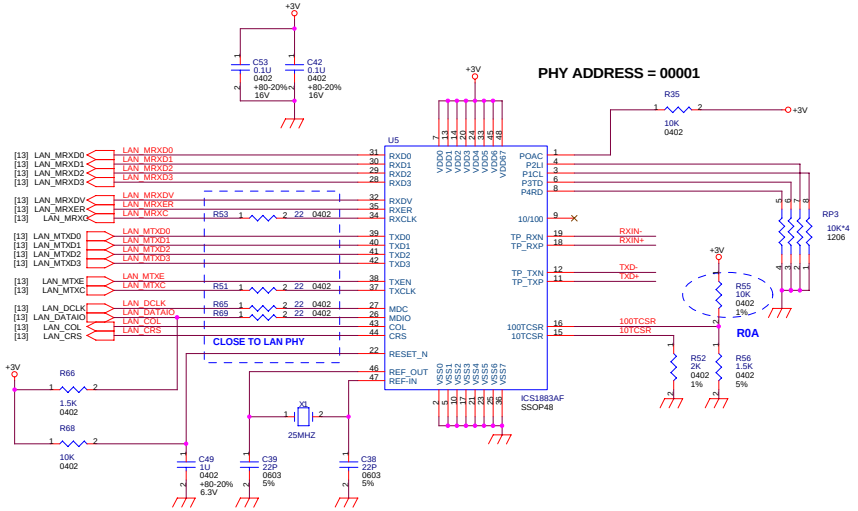
MiTAC

Title: PCMCIA (Ti PCI1410A)

Size: | Document Number: 411682900001 | Rev: R06

Date: Monday, April 12, 2004 | Sheet 16 of 28

LAN PHY (ICS1883AF) & MDC



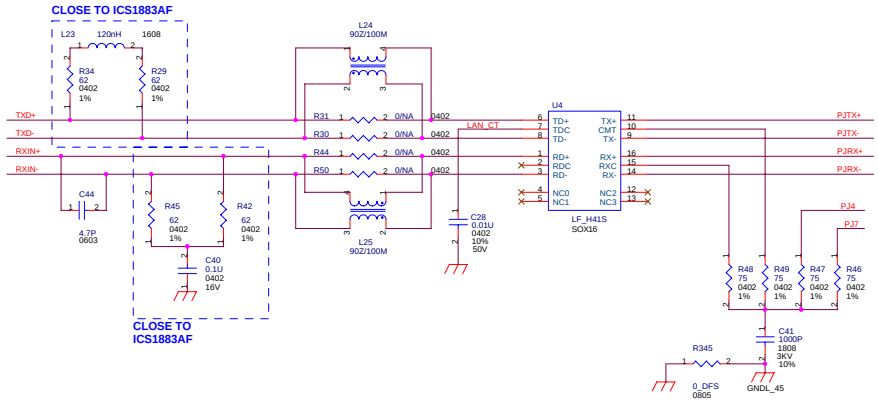
Layout Note:

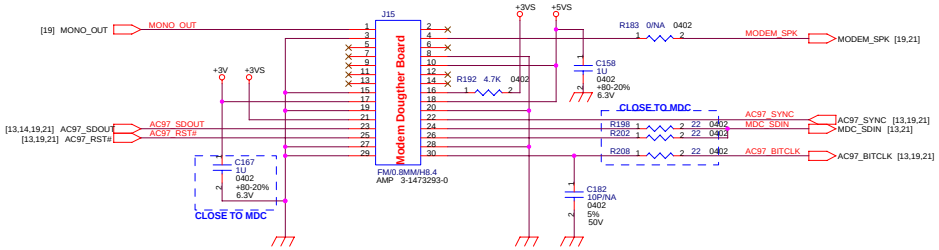
二組各自平行走線等長

二組中間須絕緣, EX: GND SHIELDING

S/W/W/S=10/8/8/10 mils

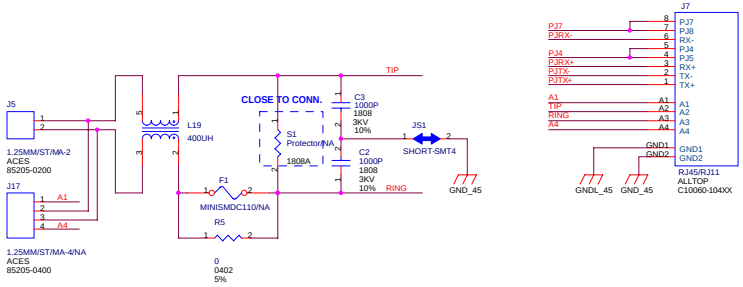
as short as possible





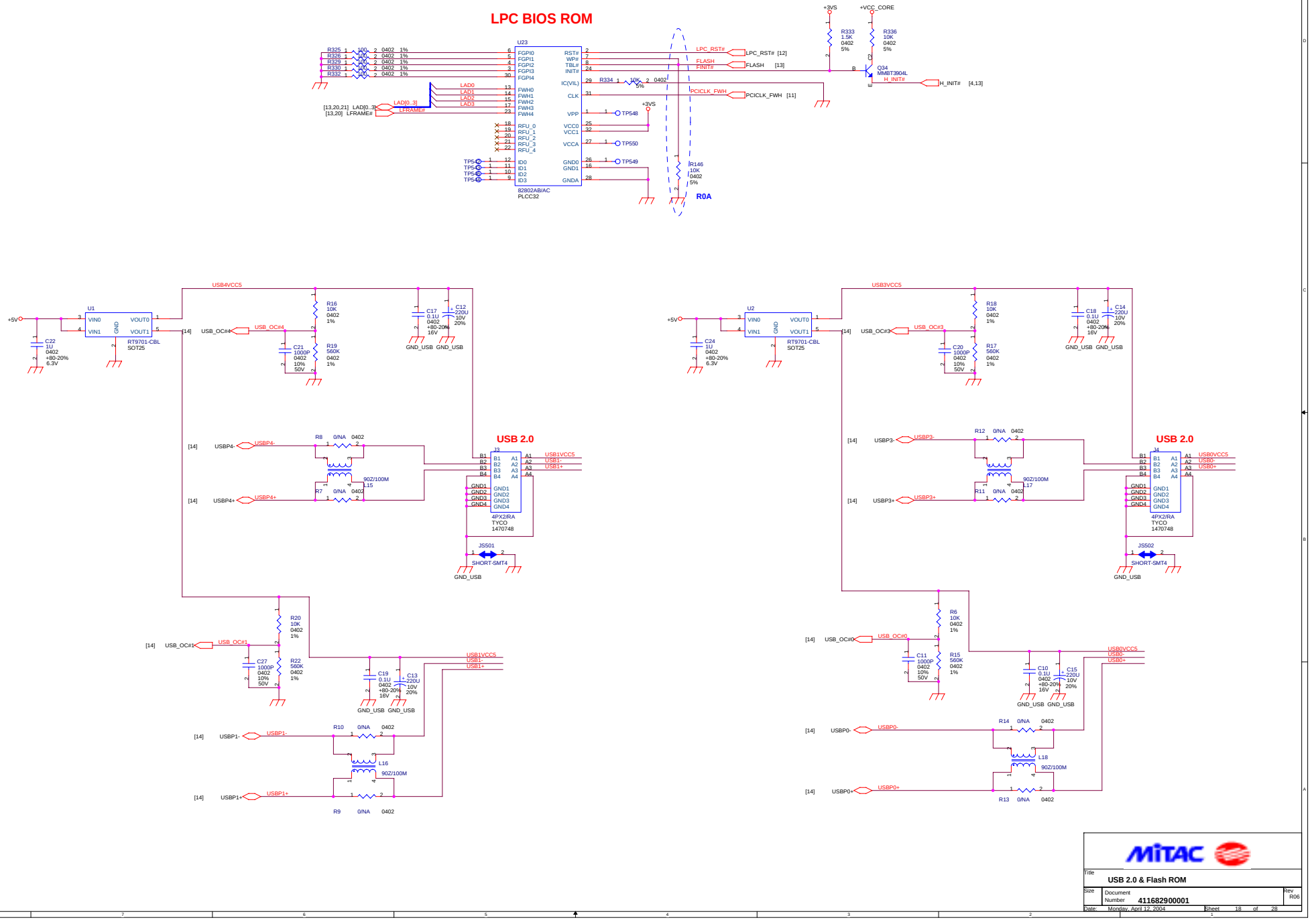
MDC HARDWARE STRAP

	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD

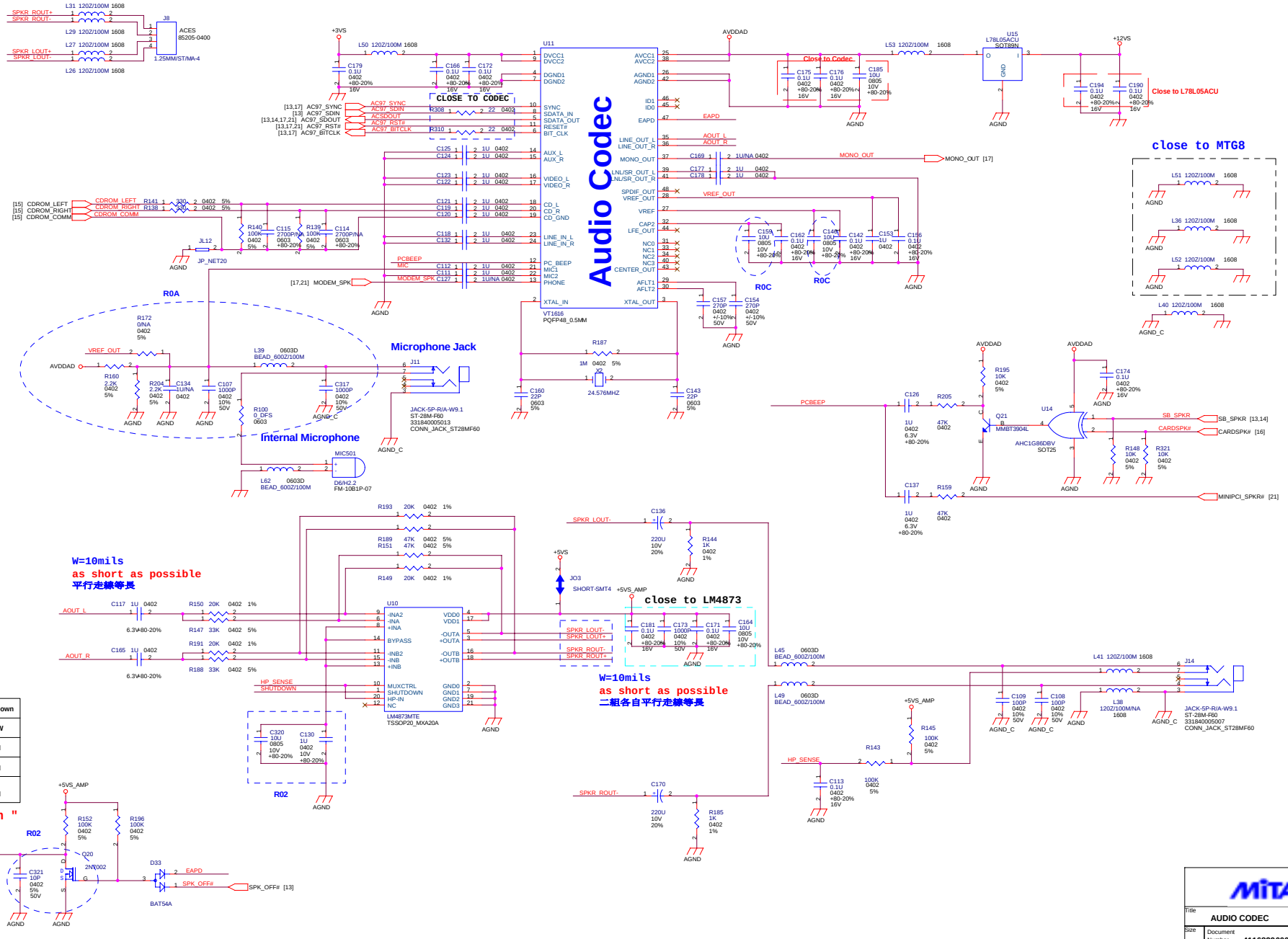


Title	LAN PHY (ICS1883AF) & MDC
Size	Document Number 411682900001 Rev R06
Date:	Monday, April 12, 2004 Sheet 17 of 28

USB 2.0 & Flash ROM



AUDIO CODEC



SPK_OFF#	EAPD	Shutdown
HI	HI	LOW
HI	LOW	HI
LOW	HI	HI
LOW	LOW	HI

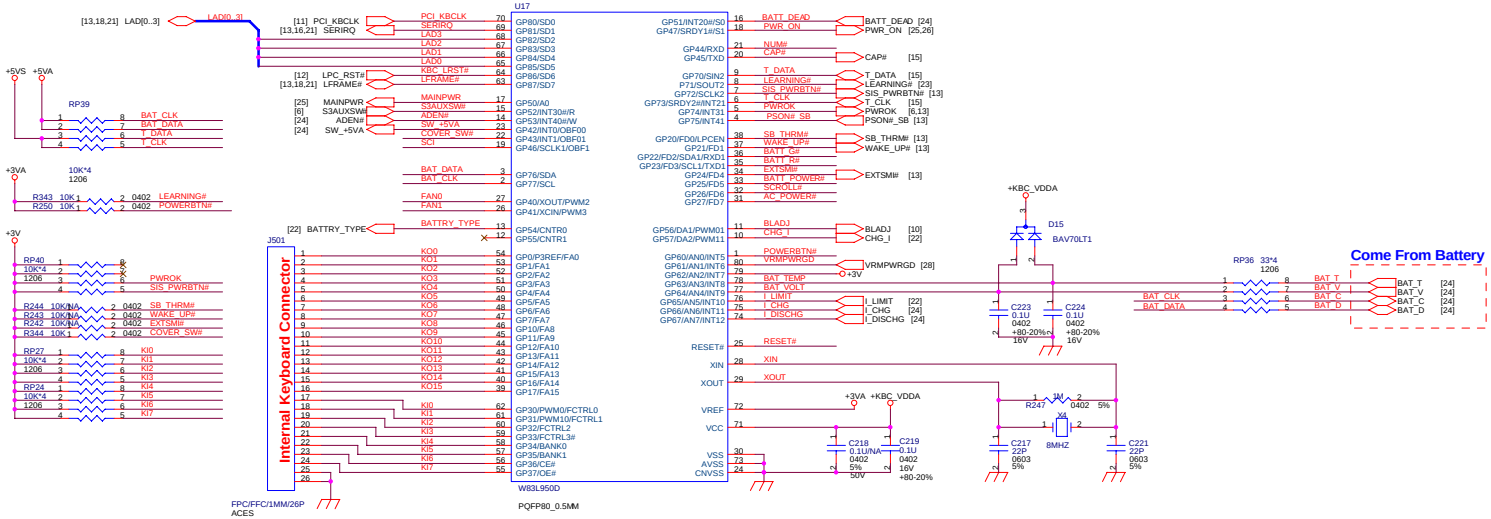
Title	AUDIO CODEC		
Size	Document Number	411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 19 of 28		

KBC (W83L950D)

+3VA — 30mil — +KBC_VDDA

L56 120Z/100M 1608

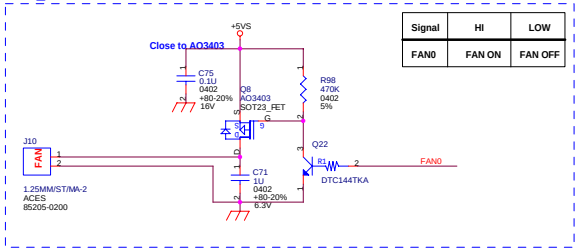
PSON#_SB	S3AUXSW#	STATUS
1->0	1	POWER ON
0->1	0	STR
0->1	1	STD/SOFT OFF
1->0	1	S3 Resume



CPU_FAN Control

Close to AO3403

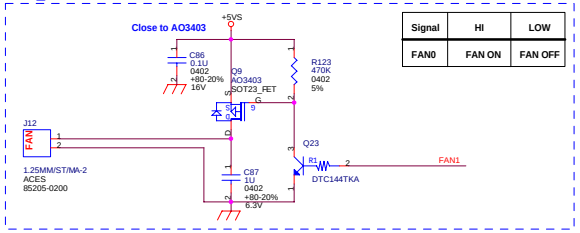
Signal	HI	LOW
FAN0	FAN ON	FAN OFF

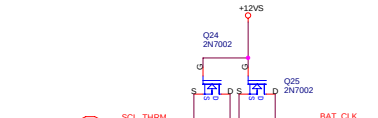


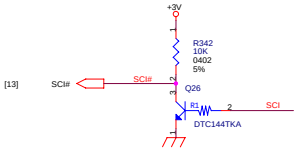
CPU_FAN Control

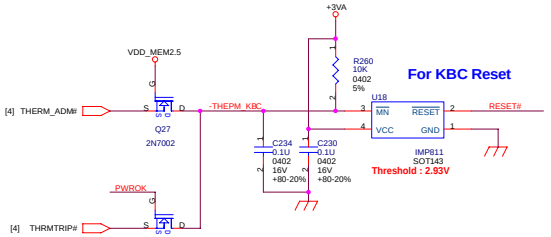
Close to AO3403

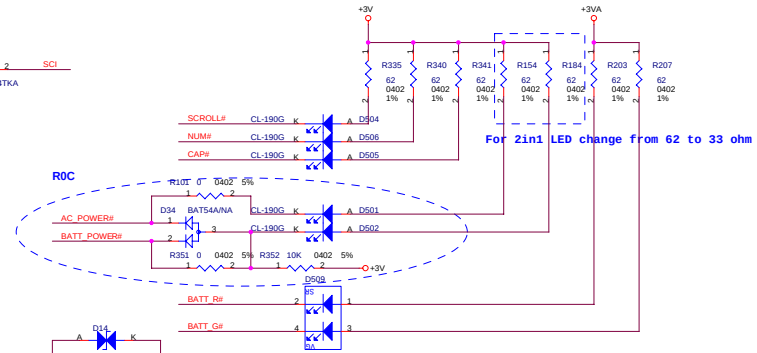
Signal	HI	LOW
FAN0	FAN ON	FAN OFF

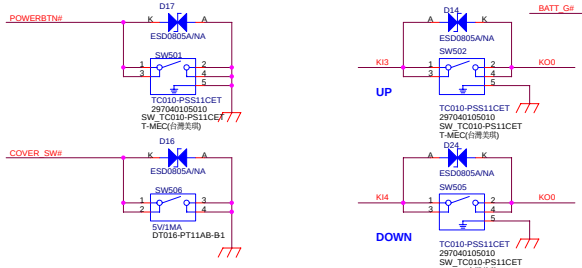






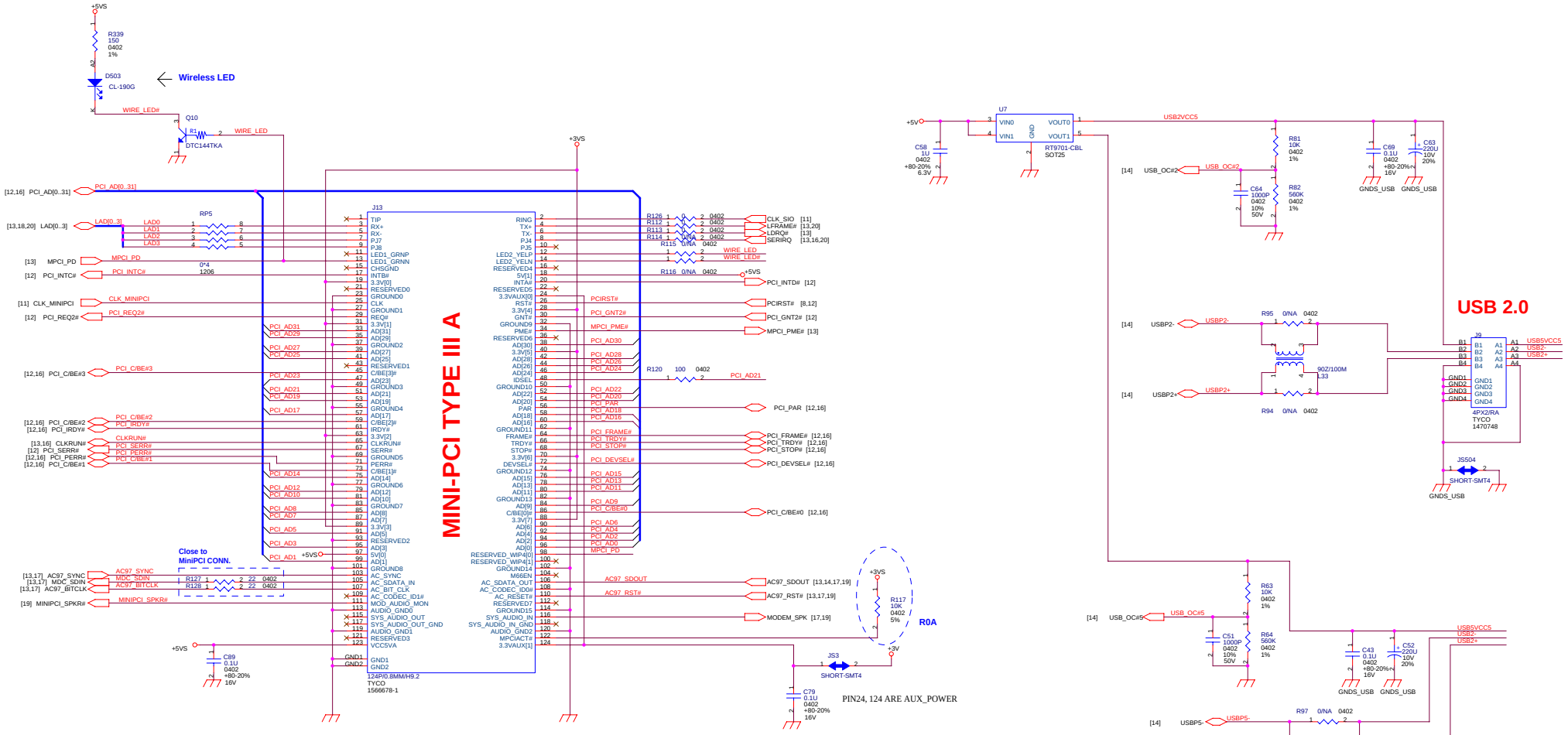






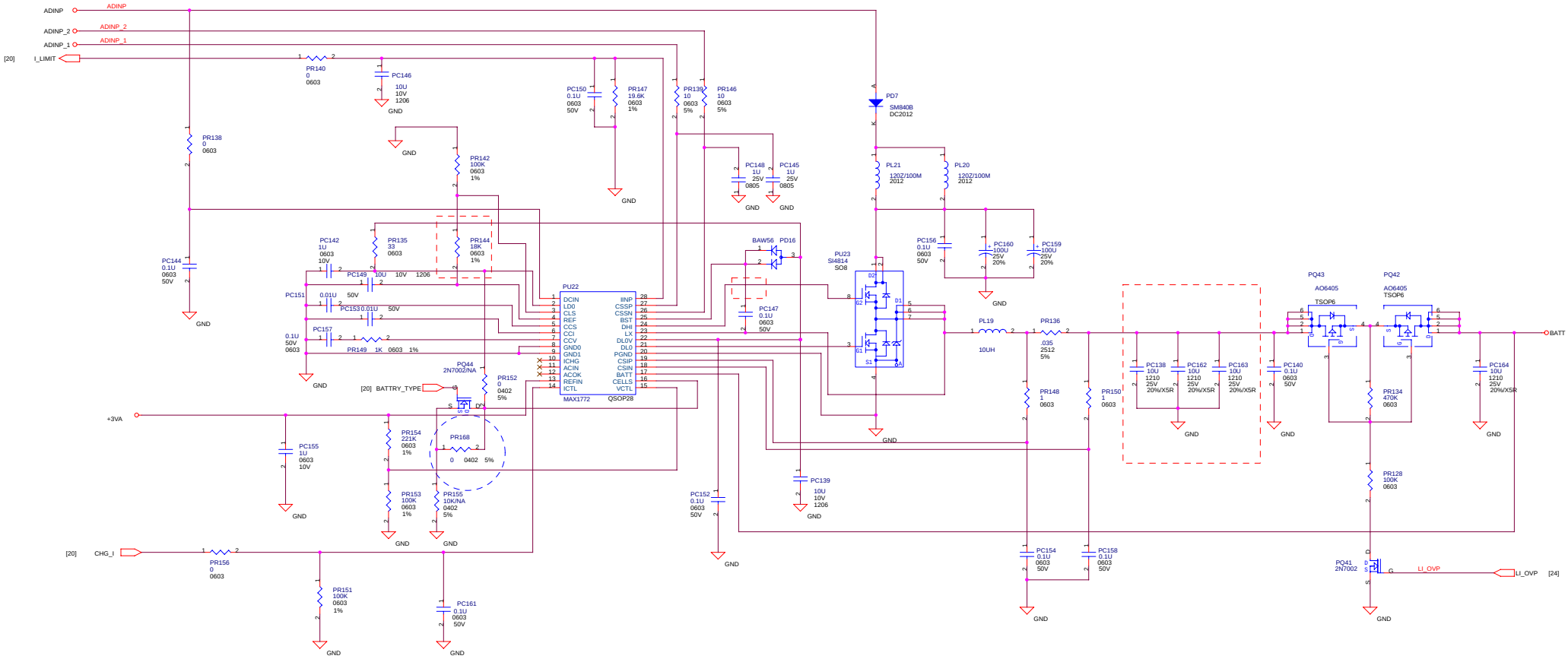
MiTAC	Title: KBC (W83L950D)		
	Size	Document Number: 411682900001	Rev: R06
	Date: Monday, April 12, 2004	Sheet 20 of 28	

Mini-PCI & USB 2.0



MINI-PCI

AD21
PCI_INTD# \ INTC#
REQ2#/GNT2#

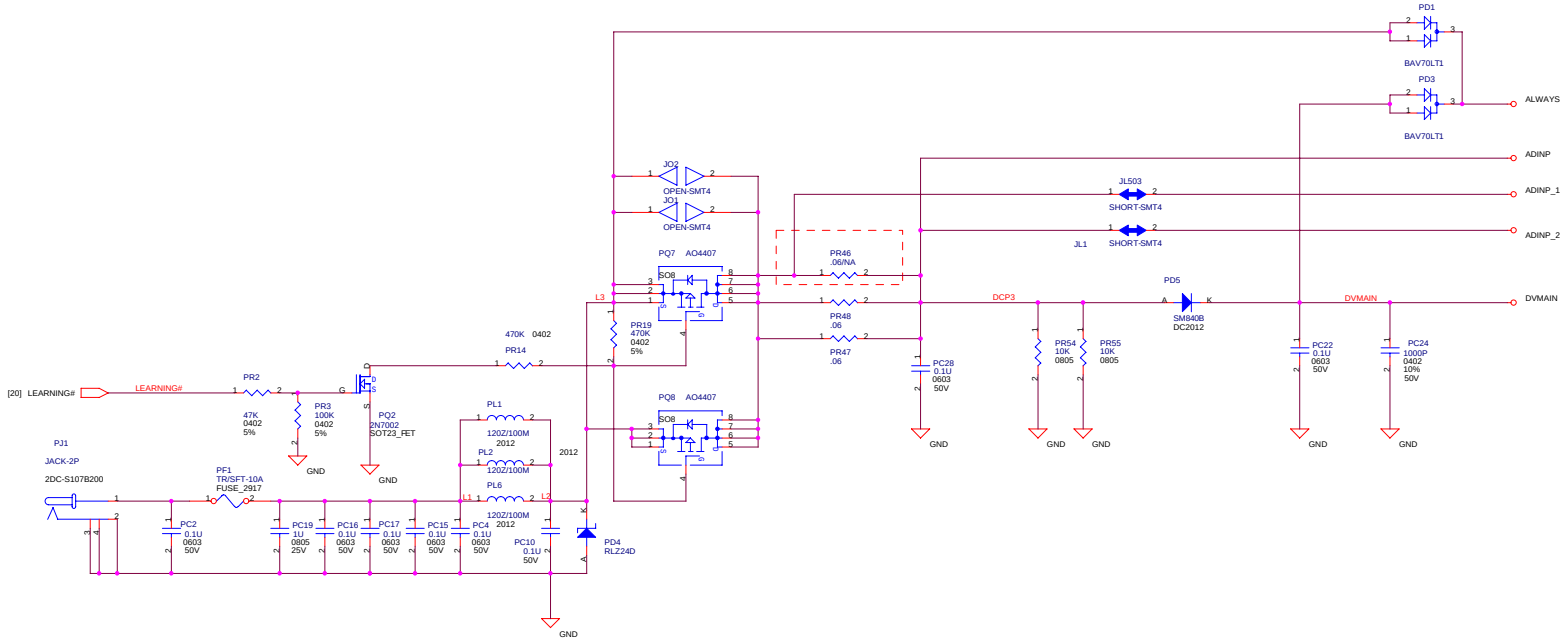


MiTAC

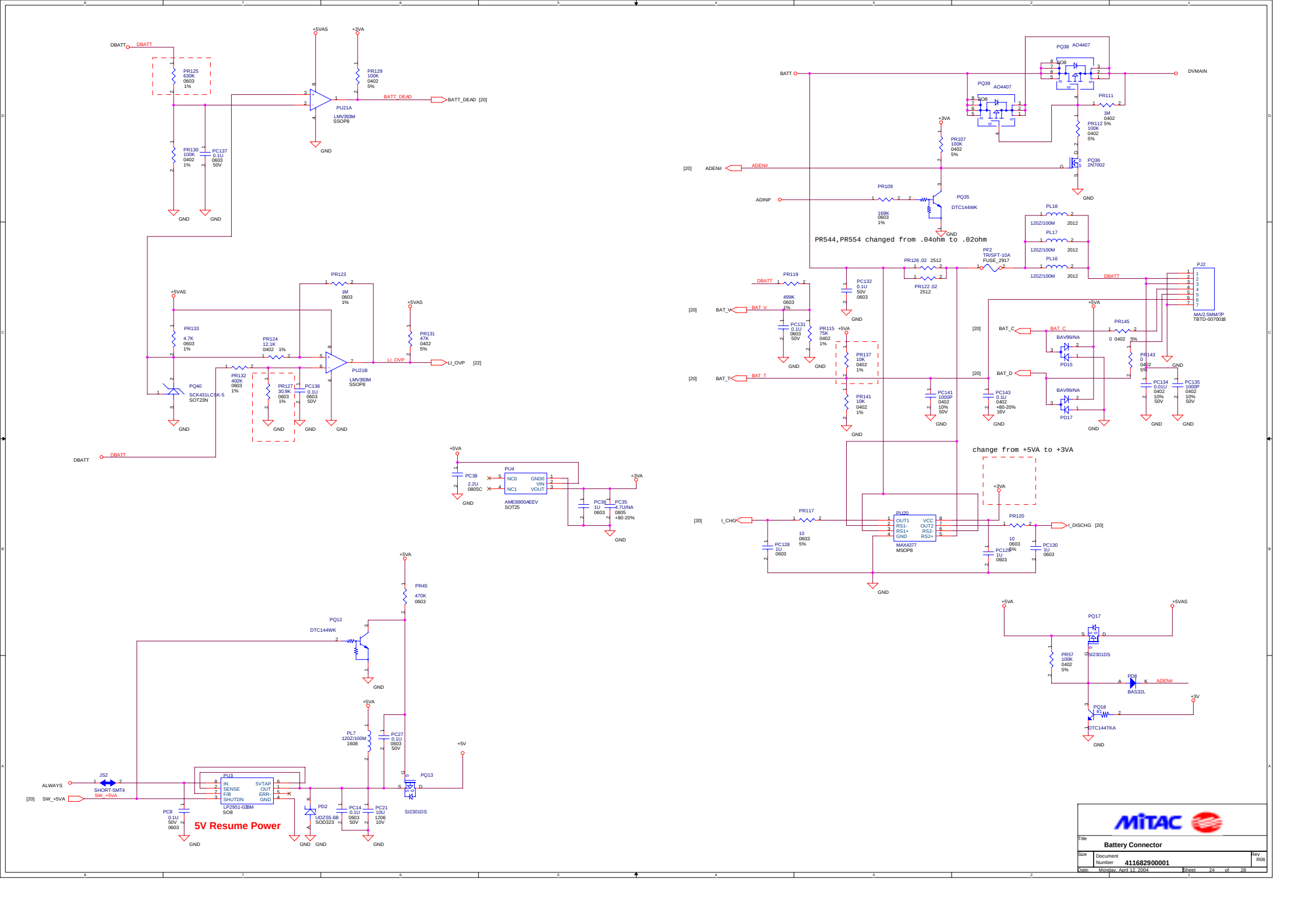
Title: DC-DC CONNECTOR ,CHARGER

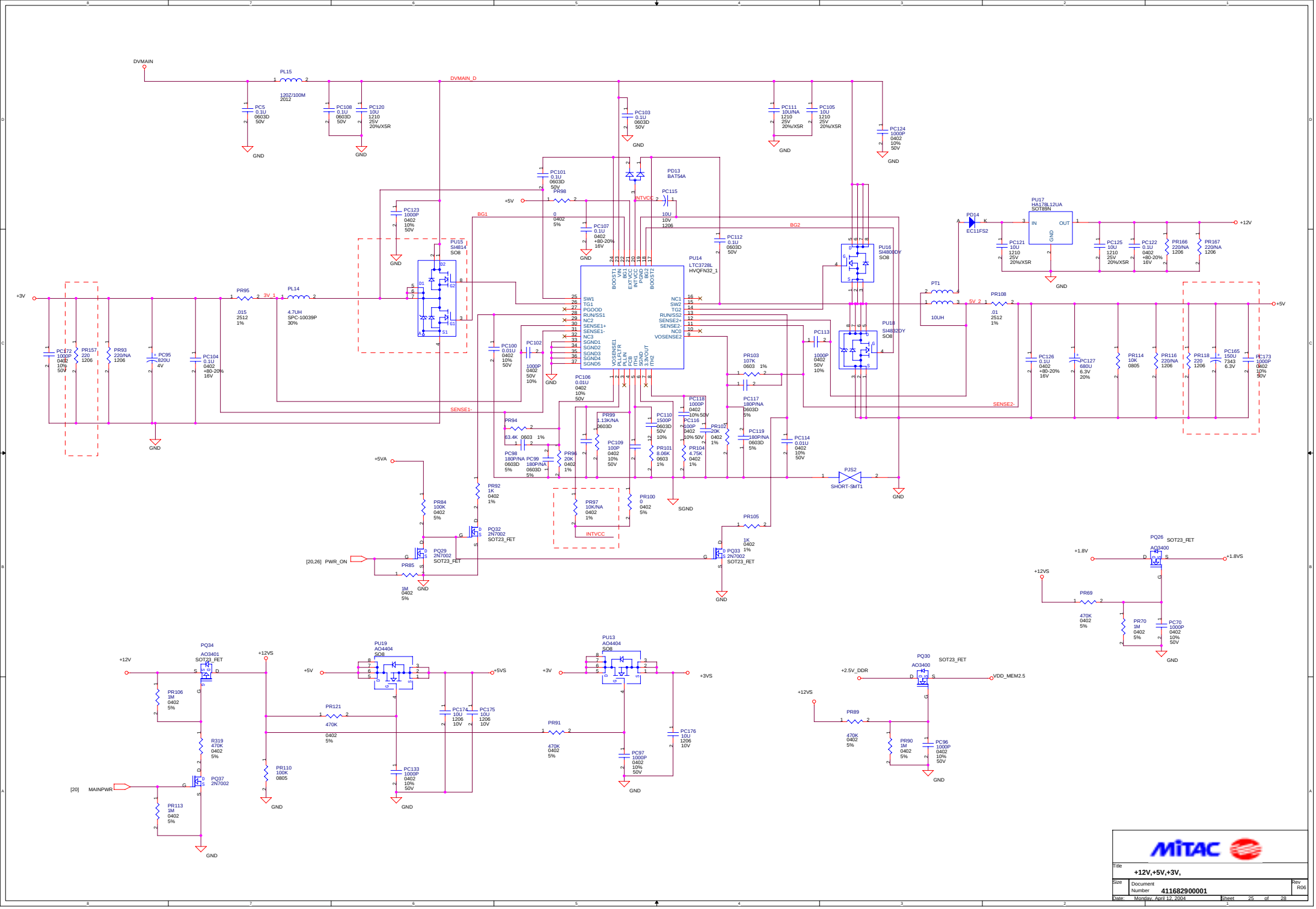
Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 22 of 28



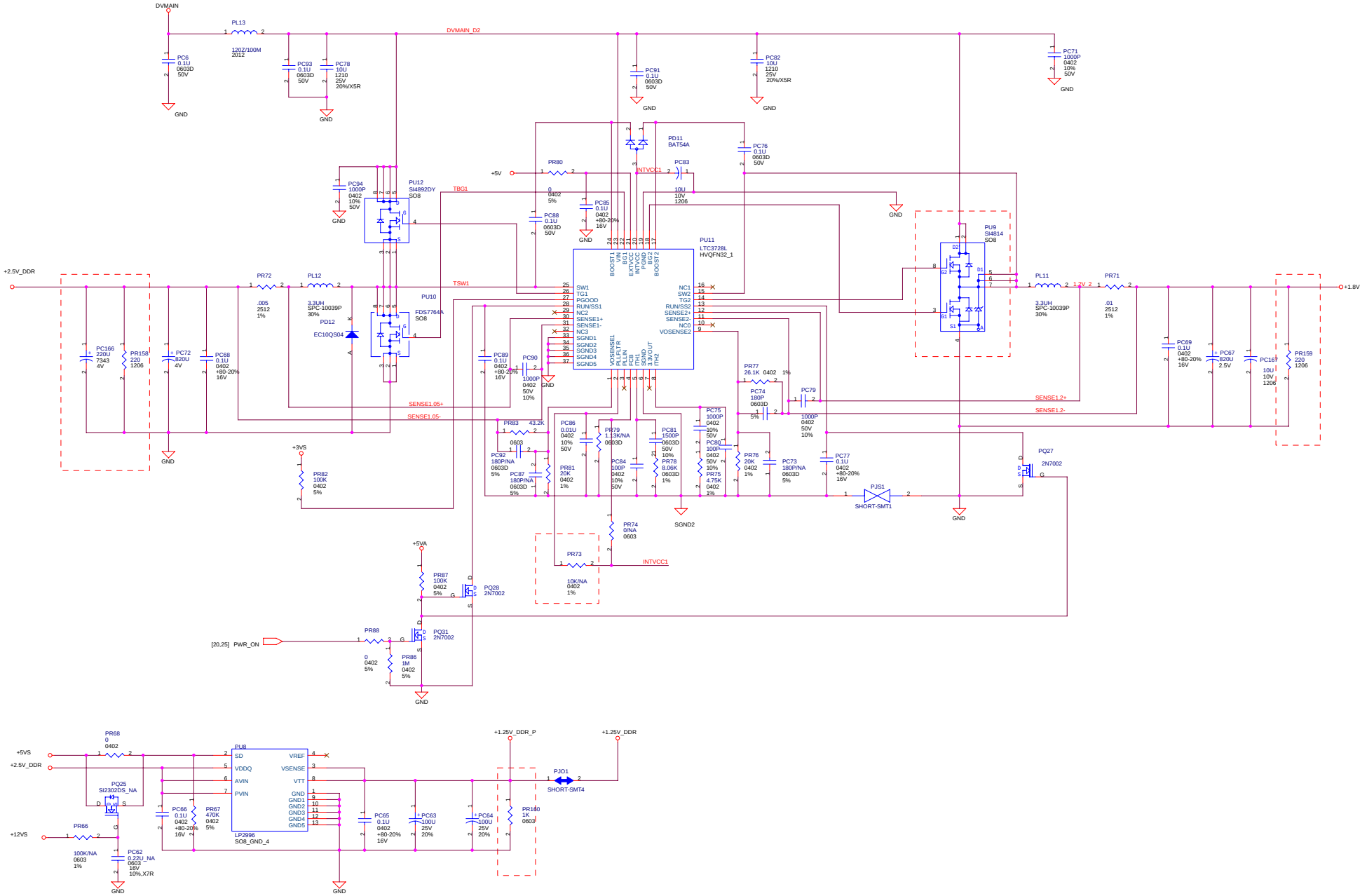
Title	DC Connector	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 23 of 28	


DBATT
PR125 630K 0603 1%
PR130 100K 0402 1%
PC137 0.1U 0603 50V
+5VAS
+3VA
PR129 100K 0402 5%
PU21A LMV393M SSOP8
BATT_DEAD
BATT_DEAD [20]
GND
PR123 1M 0603 1%
PR133 4.7K 0603 1%
PR124 12.1K 0402 1%
PR132 402K 0603 1%
PR127 30.9K 0603 1%
PC136 0.1U 0603 50V
PQ40 SCK431LCSK-5 SOT23N
PU21B LMV393M SSOP8
PR131 47K 0402 5%
LI_OVP
LI_OVP [22]
PU4 AME8800AEEV SOT25
PC38 2.2U 0805C
PC36 1U 0603
PC35 4.7U/NA 0805 +80-20%
+5V
PR45 470K 0603
PQ12 DTC144WK
PL7 120Z/100M 1608
PC27 0.1U 0603 50V
PQ13 SI2301DS
JS2 SHORT-SMT4
ALWAYS
[20] SW_+5VA
SW_+5VA
PU3 LP2951-02BM SO8
5VTAP OUT ERR GND
PC8 0.1U 50V 0603
PD2 UDZS5.6B SOD323
PC14 0.1U 0603 50V
PC21 10U 1206 10V
5V Resume Power
BATT
DVMAIN
PQ38 AO4407
PQ39 AO4407
PR111 1M 0402
PR112 100K 0402 5%
PR107 100K 0402 5%
PQ36 2N7002
ADEN#
[20] ADEN#
ADINP
PR109 169K 0603 1%
PQ35 DTC144WK
PR544,PR554 changed from .04ohm to .02ohm
PR126_02 2512
PR122_02 2512
PF2 TR/SFT-10A FUSE_2917
PL18 120Z/100M 2012
PL17 120Z/100M 2012
PL16 120Z/100M 2012
PJ2 MA/2.5MM/7P TBTD-007001B
PR119 499K 0603 1%
PC132 0.1U 50V 0603
PC131 0.1U 0603 50V
PR115 75K 0402 1%
BAT_V
[20] BAT_V
BAT_T
[20] BAT_T
PR137 10K 0402 1%
PR141 10K 0402 1%
PC141 1000P 0402 10% 50V
PC143 0.1U 0402 +80-20% 16V
BAT_C
[20] BAT_C
BAT_D
[20] BAT_D
BAV99/NA
PD15
PD17
PR145 0 0402 5%
PR143 0 0402 5%
PC134 0.01U 0402 10% 50V
PC135 1000P 0402 10% 50V
change from +5VA to +3VA
PR117 10 0603 5%
PU20 MAX4377 MSOP8
PR120 10 0603 5%
PC128 1U 0603
PC125 1U 0603
PC130 1U 0603
I_CHG
[20] I_CHG
I_DISCHG [20]
PQ17 SI2301DS
PR57 100K 0402 5%
PD8 BAS32L
PQ18 DTC144TKA
+3V
Title
Battery Connector
Size
Document Number 411682900001
Rev R06
Date: Monday, April 12, 2004
Sheet 24 of 28



MiTAC

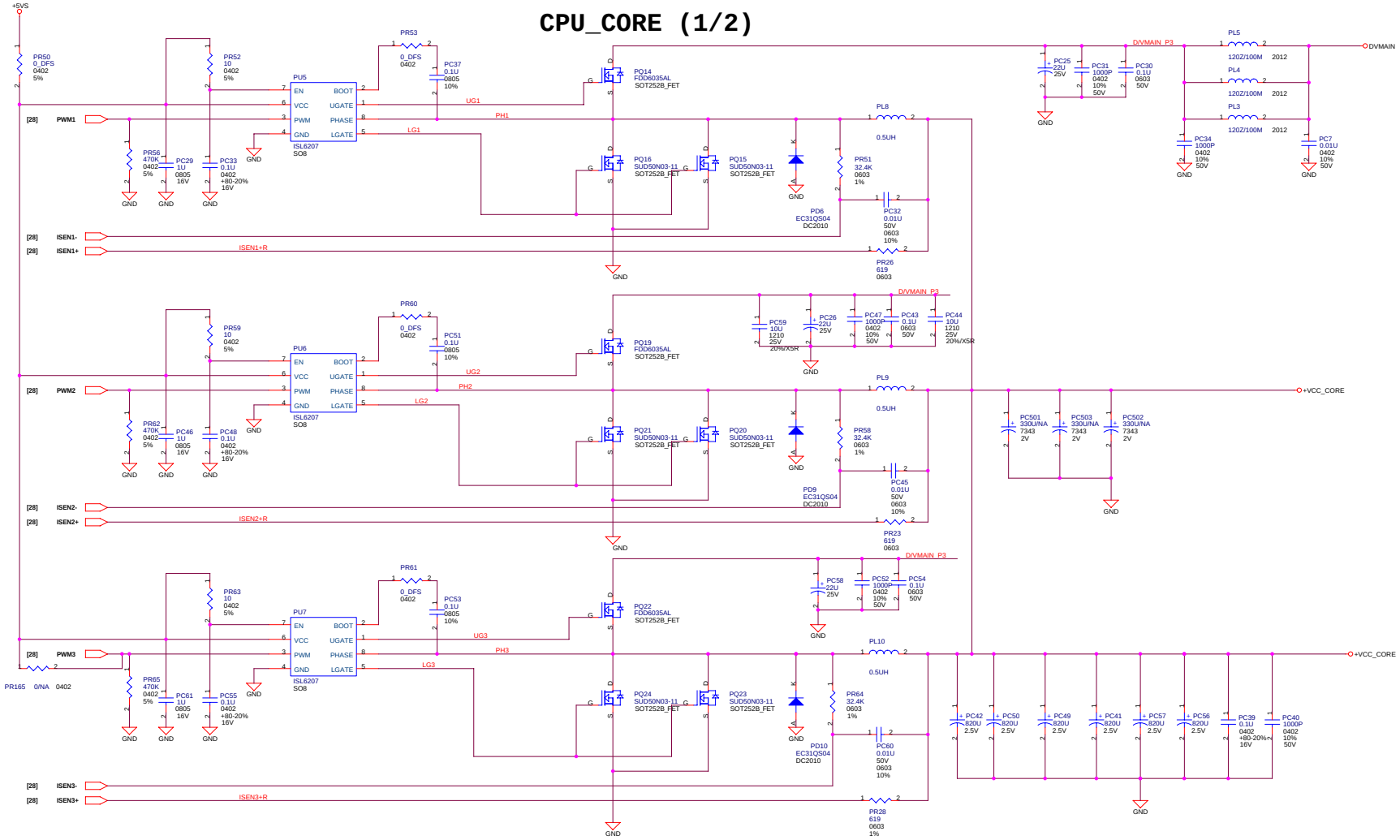
Title	+12V,+5V,+3V,
Size	Document Number 411682900001 Rev R06
Date: Monday, April 12, 2004	Sheet 25 of 28



MiTAC

Title	+2.5V,1.25V,1.8VS	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 26 of 28	

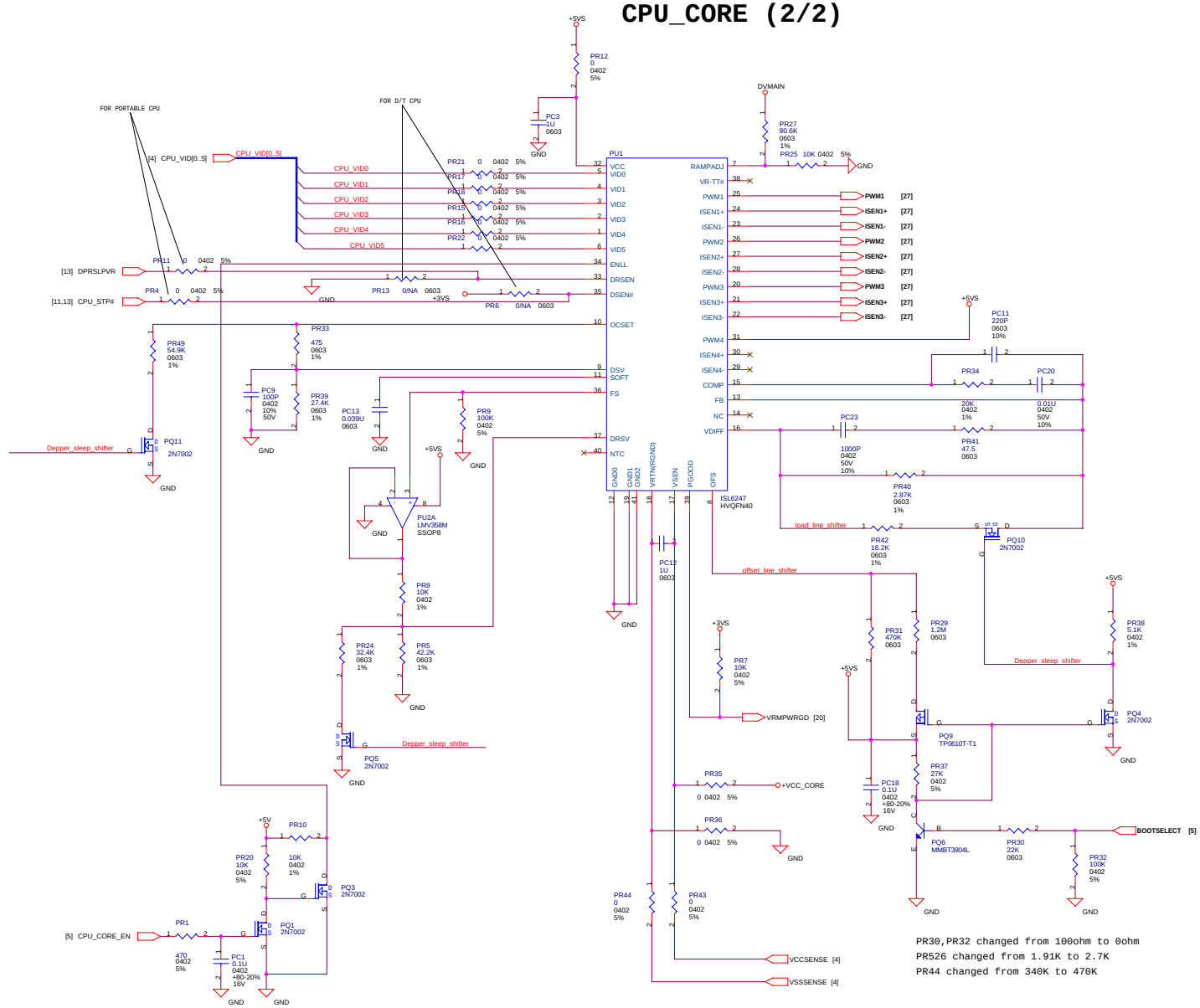
CPU_CORE (1/2)



MiTAC

Title	CPU_CORE1	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 27 of 28	

CPU_CORE (2/2)



PR30,PR32 changed from 100ohm to 0ohm
PR526 changed from 1.91K to 2.7K
PR44 changed from 340K to 470K

Title	CPU_CORE2	
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 28 of 28	

Reference Material

- Intel Pentium 4 Processor Specifications *Intel,INC*
- SiS M661FX (Host Memory Controller) *SiS,INC*
- SiS963L(MuTIOL®Media I/O South Bridge) *SiS,INC*
- Frequency Generator ICS952007 *ICS,INC*
- 8599 Hardware Engineering Specification *Technology.Corp./MiTAC*

SERVICE MANUAL FOR 8599

Sponsoring Editor : Jesse Jan

Author : Star Meng

Assistant Editor : Ping Xie

Publisher : MiTAC International Corp.

Address : 1, R&D Road 2, Hsinchu Science-Based Industrial, Hsinchu, Taiwan, R.O.C.

Tel : 886-3-5779250 Fax : 886-3-5781245

First Edition : Jun. 2004

E-mail : Willy.Chen @ mic.com.tw

Web : http: //www.mitac.com http: //www.mitacservice.com