SERVICE MANUAL FOR

8050QMA

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MiTAC

8050QMA N/B Maintenance

Contents

Contents

Contents

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8050QMA portable notebook computer system.

1.1.2 System Overview

The MiTAC 8050Q model is designed for Intel Dothan processor with 533MHz FSB with Micro-FCPGA package.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Battery Power indicator, Battery status indicator, HDD,CD-ROM, NUM LOCK, CAP LOCK, SCROLL LOCK, Wireless on/off Card Reader Accessing. It also equipped with LAN, 56K Fax MODEM, 4 USB port, S-Video and audio line in/out , external microphone function.

The memory subsystem supports DDR or DDR2 SDRAM channels (64-bits wide).

The 915PM MCH Host Memory Controller integrates a high performance host interface for Intel Dothan processor, a high performance PCI Express interface, a high performance memory controller and Direct Media Interface

(DMI) connecting with Intel ICH6-M.

The Intel ICH6-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, the SATA controller and Direct Media Interface technology.

The Realtek RTL8100CL is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI).

The VT6301S is a single chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a P2000. It implements the Link and PHY layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a P2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface. The VT6301S supports 100, 200 and 400 Mbit/sec transmission via an integrated 1-port PHY. The VT6301S services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The ENE CB712 CardBus/Media Reader controller functions as a single slot PCI to Cardbus bridge and also PCI interface MS/SD/MMC flash card reader. The CB712 provide one Cardbus slot and all reader interface may operate simultaneously.

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports and other functions needed in control system

configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	Intel® Pentium® M Processor (Dothan) 90nm, 2M L2, 533 MHz FSB Intel® Celeron® M processor, 90nm, 512K L2, 400 MHz FSB
Core logic	Intel 915PM + ICH6-M chipset
System BIOS	SST49LF004A
Memory	0MB DDR2-SDRAM on Board Expandable with combination of optional 128MB/256MB/512MB/1GB(P) memory Two 200-pin **DDR2 400/533** SDRAM Memory Module
VGA Control	Type I MXM Interface (max 25W) with 8 cells Vram Priority at launch: NV44M + 32MB discrete Vram + Turbo Memory
Clock Generator	ICS 954226
IEEE1394	VT6301S
LAN	RTL8100CL
PCMCIA + 4 IN 1 CARD	ENE CB712
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212
Modem	AC97 Link: MDC (Mobile Daughter Card) Askey: V1456VQL-P1(INT)

1.2.1 Intel Dothan Processors in Micro-FCBGA Package

Intel Dothan Processors with 479 pins Micro-FCBGA package.

It will be manufactured on Intel's advanced 90 nanometer process technology with copper interconnect. It's features include Intel Architecture with Dynamic Execution, On-die primary 32-kB instruction cache and 32-kB write-back data cache, on-die 2-MB second level cache with advanced Transfer Cache Architecture, Data Prefetch Logic, Streaming SIMD Extensions 2 (SSE2), 533-MHz FSB.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Clock Generator

System frequency synthesizer: ICS954226 is a CK410M Compliant clock synthesizer. It provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. It is driven with a 14.318MHz crystal and generates CPU outputs up to 400MHz. It provides the tight ppm accuracy required by Serial ATA and PCI-Express.

- Supports tight ppm accuracy clocks for Serial-ATA and SRC.
- Supports spread spectrum modulation, 0 to –0.5% down spread.
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning.
- Supports undriven differential CPU, SRC pair in PD# for power management.

1.2.3 The Mobile Intel 915PM Express Chipset

The Mobile Intel 915PM Express Chipset integras a memory controller hub (MCH) designed for use with the Dothan, Yonah and Intel Celeron M Processor. It is PCI Express based Graphics.

The 915PM MCH integrates a system memory DDR/DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR/DDR2) memory is supported; the buffers support DDR SSTL_2 and DDR2 SSTL_18 signaling interfaces. The memory controller interface is fully configurable through a set of control registers. It integras a high performance transition interface PCI Express Interface. PCI Express operates at a data rate of 2.5 for 8050QMA project. GB/s. This allows a maximum theoretical bandwidth of 40 GB/s each direction. The 915PM MCH integrates Direct media interface (DMI) chip-to-chip interconnect between the MCH and ICH6-M. DMI supports DMI x2 and DMI x4 configuration.

Features:

- **Processor/FSB Support**

8050QMA N/B Maintenance

- Intel® Dothan processor
- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ host bus addressing
- Supports system bus at 533MT/s (533 MHz) and 400MT/s (400 MHz)
- 2X Address, 4X data
- Host bus dynamic bus inversion HDINV support
- 12 deep, in-order queue

❖ **Memory System**

- Directly supports to two DDR or DDR2 SDRAM channels, 64-bts wide.
- Supports SO-DIMMs of the same type (e.g.,all DDR or all DDR2), not mixed.
- Maximum of two, double-sided unbuffered SO-DIMMs (4 rows populated)
- Minimum amount of memory supported is 128 MB (16 MB x 16-b x 4 devices x 1 rows = 128 MB) using 256-MB technology
- Maximum amount of memory supported is 2 GB using 1-GB technology.

- 256-MB, 512-MB and 1-GB technology using x8 and x16 devices.
- Three memory channel organizations are supported for DDR / DDR2 :
  - Single channel
  - Dual channel interleaved
  - Dual channel asymmetric
- Supports DDR 333 devices and DDR2 400 /533 devices
  - Supports on-die termination (ODT) for DDR2
- Supports Fast Chip Select mode
- Supports partial write to memory using Data Mask signal (DM)
- Supports high-density memory package for DDR or DDR2 type devices

❖ **PCI Express Interface**

- One x16 (16 lanes) PCI Express port intended for graphics attach
- Maximum theoretical realized bandwidth on interface of 4 GB/s in each direction simultaneously, for an average of 8 GB/s when x16
- Automatic discovery, negotiation and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)

- Supports only 1.5-V AGP electrics
- 32 deep AGP request queue
- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Direct Media Interface (DMI)
  - Chip-to-chip interconnect between the GMCH and ICH6-M
  - DMI x2 and DMI x4 configuration supported
  - Bit swapping is supported
  - Lane reversal is not supported

1.2.4 I/O Controller Hub : Intel ICH6-M

The ICH6 provides extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 1.0a-compliant
- PCI Local Bus Specification, Revision 2.3-compliant with support for 33 MHz PCI operations(supports up to seven Req/Gnt pairs)
- ACPI Power Management Logic Support
- Enhanced DMA controller, interrupt controller and timer functions

- Integrated Serial ATA host controller with independent DMA operation on two ports and AHCI support
- Integrated IDE controller supports Ultra ATA100/66/33
- USB host interface with support for three USB ports; three UHCI host controllers; one EHCI high-speed USB2.0 Host controller
- Integrated LAN controller
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I^2C devices
- Supports Audio Codec ’97, Revision 2.3 Specification (a.k.a.,AC ’97 Component Specification, Revision 2.3) which provides a link for Audio and Telephony codecs (up to 7 channels)
- Supports Intel High Definition Audio
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

1.2.5 CardBus: CB712

Features:

3.3V operation with 5V tolerant

LFBGA 169-ball package

Pin out Compatible with CB1410

- PCI Interface
  - Compliant with PCI Local Bus Specification Revision 2.3
  - Compliant with PCI Bus Power Management Interface Specification Revision 1.1
  - Compliant with PCI Mobile Design Guide Version 1.1
  - Compliant with Advanced Configuration and Power Interface Specification Revision 1.0
- CardBus Interface
  - Compliant with PC Card Standard 8.0
  - Support Standardized Zoomed Video Register Model
  - Support SPKROUT CAUDIO and RIOUT#
- Secure Digital Interface
  - Compliant with SD Host Controller Standard Specification Version 1.0
  - Support SD Suspend/Resume Functionality
  - Support DMA Mode to Minimize CPU Overhead
  - Support High Speed with the SD Clock Frequency Up to 50Mhz
  - Contain two 512-byte buffer to maximize the transfer speed
  - Support Traffic LED Light
  - Support Over Current Protection

8050QMA N/B Maintenance

- Memory Stick Interface
  - Compliant with Memory Stick PRO Format Specification Version 1.0
  - Support 4-bit Parallel Data Transfer Mode
  - Memory Stick Clock Frequency Up to 40Mhz
  - Support DMA Mode to Minimize CPU Overhead
  - Support Traffic LED Light
  - Support Over Current Protection
- Interrupt Configuration
  - Support Parallel PCI Interrupts
  - Support Parallel IRQ and Parallel PCI Interrupts
  - Support Serialized IRQ and Parallel PCI Interrupts
  - Support Serialized IRQ and PCI Interrupts
- Power Management Control Logic
  - Support CLKRUN# protocol
  - Support SUSPEND#
  - Support PCI PME# from D3, D2, D1 and D0
  - Support PCI PME# from D3cold
- Support Zoomed Video port

- Support parallel 4-wire power switch interface

1.2.6 AC'97 Audio System: Advance Logic, Inc, ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bitvolume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at

Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICH6 chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/

Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation,10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

8050QMA N/B Maintenance

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- Compliant with AC'97 2.3 specifications
  - 14.318MHz- 24.576MHz PLL to save crystal
  - 12.288MHz BITCLK input can be consumed
  - Integrated PCBEEP generator to save buzzer
  - Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP,PHONE-IN
- Two software selectable MIC inputs applications (software selectable)
- Boost preamplifier for MIC input 50mW/20 amplifier
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features

- Stereo MIC record for AEC/BF application
- Supports Power Off CD function
- Adjustable VREFOUT control Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification
- Power support: Digital: 3.3V; Analog: 3.3V/5V

1.2.7 MDC: Pctel Modem Daughter Card PCT2303W (Askey V1456VQL-P1)

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin

small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The

PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chip set is fully programmable to meet world-wide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

Features:

Virtual com port with a DTE throughout up to 460.8Kbps.

G3 Fax compatible

Auto dial and auto answer

Ring detection

❖ **Codec/DAA Features**

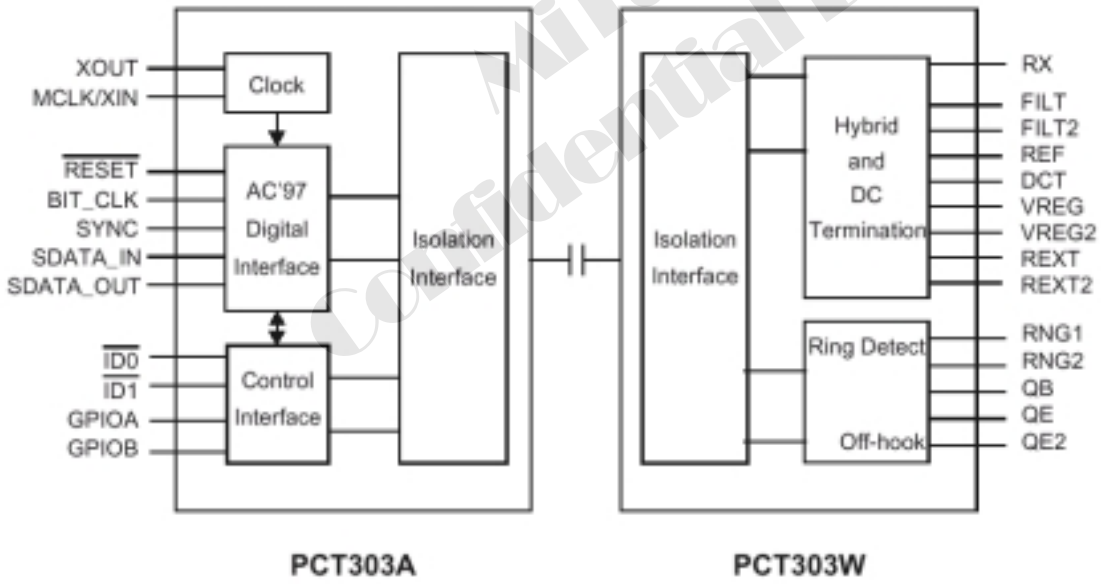
- AC97 2.1 compliant
- 86dB dynamic range TX/RX paths

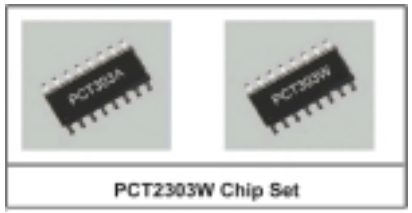
8050QMA N/B Maintenance

- 2-4-wire hybrid
- Integrated ring detector
- High voltage isolation of 4000V
- Support for “Caller ID”
- Compliant with FCC Part68, CTR21, Net4 and JATE
- Low power standby
- Low profile SOIC package 16 pins 10x3x1.55mm
- Low power consumption
- 10mA @ 3.3V operation
- 1mA @ 3.3V power down
- Integrated modem codec

Standard Features

- Data
  - ITU-T V.90 (56Kbps), V.34 (4.8Kbps TO 33.6 Kbps), V.32 bis (4.8Kbps to 14.4Kbps), V.22 bis (1.2 bps to 2.4 Kbps), V.21 and Bell 103 and 212A(300 to 1200 bps) modulation protocol
  - Data Compression ITU-T V.42bis MNP Class 5
  - Error Correction ITU-T V.42 LAPM MNP 2-4
- Fax
  - ITU-T V. 17, V.29, V.27ter, V.21, Channel 2, Group 3, EIA Class I





1.2.8 IEEE1394 VT6301S

1.2.8.1 Overview

The VT6301S IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a-2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface. The VT6301S supports 100, 200 and 400 Mbit/sec transmission via an integrated 1-port PHY. The VT6301S services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations. The VT6301S is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6301S is built into Microsoft Windows 98, Windows ME, Windows 2000 and Windows XP

1.2.8.2 Features

- 32 bit CRC generator and checker for receive and transmit data
- On-chip isochronous and asynchronous receive and transmit FIFOs for packets (2K for general receive plus 2K for isochronous transmit plus 2K for asynchronous transmit)
- 8 isochronous transmit contexts
- 4 isochronous receive contexts

- 3-deep physical post-write queue
- 2-deep physical response queue
- Dual buffer mode enhancements
- Skip Processing enhancements
- Block Read Request handling
- Ack_tardy processing

1.2.9 System Flash Memory (BIOS)

- Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets
- Flexible Erase Capability
  - Uniform 4 KByte Sectors
  - Uniform 16 KByte overlay blocks for SST49LF002A
  - Uniform 64 KByte overlay blocks for SST49LF004A
  - Top boot block protection
  - 16 KByte for SST49LF002A
  - 64 KByte for SST49LF004A

  - Chip-Erase for PP Mode

- Single 3.0-3.6V Read and Write Operations
- Superior Reliability
- Firmware Hub Hardware Interface Mode Supports Intel High Definition Audio
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block
  - Block Locking Register for all blocks
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection

1.2.10 Memory System

1.2.10.1 256MB, 512MB, 1GB (x64) 200-Pin DDR2 SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- VDD=+1.8V±0.1V, VDDQ=+1.8V±0.1V

8050QMA N/B Maintenance

- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS,DQS#) option
- Four-bit prefetch architecture
- Differential clock input (CK,CK#)
- Command entered on each rising CK edge
- DQS edge-aligned with data for Reads
- DQS center-aligned with data for Writes
- Duplicate output strobe (RDQS) option for x8 configuration
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable CAS Latency (CL) : 2,3,4 and 5
- Posted CAS additive latency (AL) : 0,1,2,3 and 4
- Write latency = Read latency – 1^{t}CK

- Programmable burst lengths : 4 or 8
- Read burst interrupt supported by another READ
- Write burst interrupt supported by another WRITE
- Adjustable data – output drive strength
- Concurrent auto precharge option is supported
- Auto Refresh (CBS) and Self Refresh Mode
- 64ms, 8,192-cycle refresh
- Off-chip drive (OCD) impedance calibration
- On-die termination (ODT)

1.2.11 LAN PHY: RTL8100C(L)

General

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power

Management (OSPM) to achieve the most efficient power management possible. The RTL8100C(L) does not support CardBus mode as the RTL8139C does. In addition to the ACPI feature, the RTL8100C(L) also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8100C(L) is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8100C(L) is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8100C(L) LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. The RTL8100C(L) also supports Analog Auto-Power-down, that is, the analog part of the RTL8100C(L) can be shut down temporarily according to user requirements or when the RTL8100C(L) is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8100C(L) will be negligible. The RTL8100C(L) also supports an auxiliary power auto-detect function and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

- 128 pin QFP/LQFP
- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation
- Supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller

    1. Compliant to PCI Revision 2.2

2. Supports PCI clock 16.75MHz-40MHz
3. Supports PCI target fast back-to-back transaction
4. Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8100C(L)'s operational registers
5. Supports PCI VPD (Vital Product Data)
6. Supports ACPI, PCI power management

- Supports 25MHz crystal or 25MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM.
- Compliant to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
- Includes a programmable, PCI burst size and early Tx/Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2Kbyte) independent receive and transmit FIFOs

- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter and VPD data
- Supports LED pins for various network activity indications
- Supports loop back capability
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)

1.2.12 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters.

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB
- Support 4 Timer (8 bit) signal with 3 prescalers

- Support 2 PWM channels, 2 D-A and 8 A-D converters
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.2.13 Hard Disk Drive

IDE HDD

The ICH6 IDE controller features one set of interface signals that can be enabled, tri-stated or driven low. The IDE interfaces of the ICH6 can support several types of data transfers:

- Programmed I/O (PIO): processor is in control of the data transfer
- 8237 style DMA: DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the ICH6. This protocol off loads the processor from moving data. This allows higher transfer rate of up to 16MB/s

8050QMA N/B Maintenance

- Ultra ATA/33/66/100: DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33/66/100 MB/s

1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Power down	Mini PCI power down
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F10	Battery Low Beep	On/Off Battery Low Beep
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power On/Off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode. Windows power management control panel set power button behavior.

You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None

2. Standby

3. Off

4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

1.3.4.1 Three LED Indicators at Front Side:

From left to right that indicate BATTERY POWER, BATTERY STATUS and AC POWER

-- AC POWER:

This LED lights green when the notebook was powered by AC power line, Flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by battery.

-- BATTERY POWER

This LED lights green when the notebook is being powered by Battery, and flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by AC adapter.

-- BATTERY STATUS:

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is

connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

AC POWER: This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to RAM no matter using AC power or Battery power. The LED is off when the notebook is off or powered by battery.

BATTERY POWER: This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1 second) when Battery is low. The LED is off when the notebook is off or powered by AC adaptor.

1.3.4.2 Seven LED Indicators:

System has seven status LED indicators at front side which to display system activity. From left to right that indicate HARD DISK, CD-ROM, NUM LOCK, CAPS LOCK, SCROLL LOCK, Wireless on/off, Card Reader Accessing Blue-Tooth.

1.3.5 Battery Status

1.3.5.1 Battery Warning

-- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.

-- Battery Warning: Capacity below 10%, Battery Capacity LED flashes , and system beeps per 2 seconds.

-- System will Suspend to HDD after 2 Minutes to protect users data.

1.3.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 11.5 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power On/Off Management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU and VGA temperature and PWM control fan speed. Fan speed is depended on CPU and VGA temperature. Higher CPU or VGA temperature faster Fan Speed.

1.3.7 CMOS Battery

CR2032 3V 220mAh lithium battery

When AC in or system main battery inside, CMOS battery will consume no power.

AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.

1.3.8 I/O Port

- One Power Supply Jack
- One External DVI-I Connector For DVI Display
- Supports four USB port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- One IEEE1394 port
- One TV-Out port
- Reserve 1 connector on board for USB 2.0 Device
- Headphone Out Jack.
- Microphone Input Jack.

- Line in Jack

1.3.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Power Management

The 8050MB system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full on Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.4.1.3 Standby Mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

-- CPU: Stop grant

-- LCD: backlight off

-- HDD: spin down

1.4.1.4 Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM

  -- CPU: off

  -- Intel 915GM: Partial off

  -- VGA: Suspend

  -- PCMCIA: Suspend

  -- Audio: off

  -- SDRAM: self refresh

- Suspend to HDD

  -- All devices are stopped clock and power-down

  -- System status is saved in HDD

-- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4.2.1 HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: Intel ICH6-M GPIO Definitions (1)

Pin name	Current Define		Power plane
GPIO0	PCI_REQ6#	I	MAIN
GPIO1	MINIPCI_ACT#	I	MAIN
GPIO2	PCI_INTE#	I	MAIN
GPIO3	PCI_INTF#	I	MAIN
GPIO4	PCI_INTG#	I	MAIN
GPIO5	PCI_INTH#	I	MAIN
GPIO6	PM_BMBUSY#	I	MAIN
GPIO9	X	I	RESUME
GPIO10	X	I	RESUME
GPIO11	SMBALERT#	I	RESUME
GPIO12	KBD_US/JP#	I	MAIN
GPIO13	WAKE_UP#	I	RESUME
GPIO14	X	I	RESUME
GPIO15	X	I	RESUME
GPIO16	SB_BY_ON#	O	MAIN
GPIO17	SCI#	I	MAIN
GPIO18	STOP_PCI#	O	MAIN
GPIO20	STOP_CPU#	O	MAIN
GPIO23	WIRELESS_PD#	O	MAIN
GPIO24	SPK_OFF	I/O	RESUME
GPIO25		I/O	RESUME
GPIO26	PANEL_ID0	I	MAIN
GPIO27	X	I/O	RESUME

1.5 Appendix 1: Intel ICH6-M GPIO Definitions (2)

Continue to previous page

Pin name	Current Define		Power plane
GPIO28	X	I/O	RESUME
GPIO29	PANEL_ID1	I	MAIN
GPIO30	PANEL_ID2	I	MAIN
GPIO31	PANEL_ID3	I	MAIN
GPIO32	PCLKRUN#	I/O	MAIN
GPIO33	MB_ID0	I/O	MAIN
GPIO34	MB_ID1	I/O	MAIN
GPIO40	MXM_DETECT#	I	MAIN
GPIO41	CRT_IN#	I	MAIN
GPIO48	X	O	MAIN
GPIO49	HPWRGD	OD O	MAIN

1.6 Appendix 2: W83L950D KBC Pins Definitions (1)

Port	Pin	Function	Implement
P0	0-7	Scan matrix	KO[0..7]
P1	0-7		KO[8..15]
P3	0-7		KI[0..7]
P2	0	LPC enable	H8_THRM#
	1	GPIO x1	H8_WAKE_UP#
	2	SMBUS1 or UART	BATT_G#
	3		BATT_R#
	4	GPIO x4	EXTSMI#
	5		CAP#
	6		NUM#
	7		SCROLL#
P4	0	Xcin/cout or PWM 2,3	H8_ENABKL
	1		CHARGING
	2	GPIO x2 (INT1)	LEARING
	3		H8_SUSB
	4	KBRST	H8_HRCIN#
	5	A20	A20GATE
	6	GPIO x2	H8_SCI
	7		H8_PWRON
P5	0	GPIO x1	SW_VDD3
	1	GPIO x3 (INT20,30,40)	H8_LIDSW#
	2		BATT_DEAD#
	3		H8_ADEN#
	4	GPIO x2	BATT_LED#
	5		KBC_PWRON_VDD3S
	6	D/A, PWM 2,3	BLADJ
	7		H8_I_CTR

1.6 Appendix 2: W83L950D KBC Pins Definitions (2)

Continue to previous page

Port	Pin	Function	Implement
P6	0	A/D (INT5-12)	PWRBTN#
	1		KBC_RI#
	2		AC_ POWER#
	3		BATT_V
	4		BATT_T
	5		H8_I_LIMIT
	6		H8_PROCHOT#
	7		+BC_CPUCORE
P7	0	PS/2 port x3	T_DATA
	1		H8_RSMRST
	2		ICH_PWRBTN
	3		T_CLK
	4		H8_PWRON_SUSB#
	5		SUSC#
	6	SMBUS	BAT_DATA
	7		BAT_CLK
P8	0	LPC interface	PCICLK_KBC
	1		SERIRQ
	2		LAD3
	3		LAD2
	4		LAD1
	5		LAD0
	6		KBC_PCIRST#
	7		LFRAME#

1.7 Appendix 3: 8050QMA Product Spec (1)

Item	Description
CPU	Intel® Pentium® M Processor (Dothan) 90nm, 2M L2, 533 MHz FSB Intel® Celeron® M processor, 90nm, 512K L2, 400 MHz FSB - CPU Thermal ceiling: 27W
Core logic	Intel 915PM + ICH6M - Dual Channel Memory Support - DDR2 400/533 Expandable to 2048MB(P)
System BIOS	Inside 512KB Flash EPROM Include System BIOS, VGA BIOS ACPI2.0; 2.31 compliants Boot from USB mass storage device
Memory	- 200-pin SO-DIMM DDR2 Memory Slot x2 - Support DDR2 400/533 - 0MB Memory onboard ; Expandable to 2.0GB(P)
VGA Controller	- Type I MXM Interface (max 25W) with 8 cells Vram - Priority at launch: NV44M + 32MB discrete Vram + Turbo Memory
ROM Drive	12.7mm Optical Drive - Combo Drive - DVD Dual - DVD Super Multi drive
HDD	One 2.5" 9.5 mm height HDD; - 5400/7200 RPM Serial PATA HDD - 40/60/80 GB Capacity
Display	15.4" Wide WXGA TFTLCD - Resolution: 1280 x 800
Keyboard	- Key pitch: 19mm, Key travel: 3.0mm - Windows Logo Key x 2 - W/z Hot Key Functions
Touch Pad	- Intelligence Glide pad without scroll button - 2 touch pad buttons

1.7 Appendix 3: 8050QMA Product Spec (2)

Continue to previous page

Item	Description
Audio/AV Function	- AC97, support S/PDIF output - 5.1 channel analog output - 2.1 channel system speaker. two full range speakers(1W*2 Front), one subwoofer(3W) - Build in microphone
Multi Card reader	- 4 in 1 Card Reader (SD/MMC/MS/MS Pro)
Indicator on board	- 3 LEDs for Power/Battery status (AC In status/Battery status/Reserved Power - System Status) (on inverter board) - 2 LEDs for HDD Access, ODD Access - 3 LEDs for Number lock, Caps lock, Scroll lock - 1 LED for Wireless on/off - 1 LED for Card Reader Accessing
PC CARD	1x Type II PCMCIA Interface without Zoom Video Support Support 3.3V, 5V device
I/O Ports	**I/O:** USB (support USB 1.1 and USB 2.0) port x 4 Reserve 1 connector on board for USB 2.0 Device RJ-11 port x 1 (4Pin) RJ-45 port x 1 DC input (2.5 * 5.5 * 11mm) x 1 IEEE1394 x 1(4 pin). Type III B MiniPCI x 1 (For wireless LAN) **Audio(Normal /5.1Analog output):** Line - out/SPDIF x 1 (5.1 mode: Front 2 channels) Mic - in x 1 (5.1 mode: LBF/Middle channels) Line - in x 1 (5.1 mode: Rear 2 channels) **Video** DVI- I x 1 TV-Out x 1 (7 Pin S-Video connector NTSC/PAL)

1.7 Appendix 3: 8050QMA Product Spec (3)

Continue to previous page

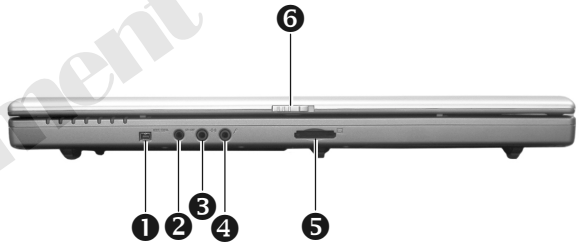
Item	Description
Communication	PCI 10/100 LAN MDC 56K, V.90 Modem 802.11g wireless LAN (Mini PCI optional) with built-in Antenna
Power Supply	6 cell Li-ion (2400mAH/3.7V) Battery pack Battery Life > 3HRs
AC adapter	Universal AC adapter 2 Pin 2.5*5.5*11 65W 19V DC output, Input: 100-240V, 50/60Hz AC
Dimensions	35mm x 250mm x 25 ~ 38mm(Max)(P)
Weight	2.8KG (TBD)
Manuals	EN, GR , Pan-EU
Accessories	AC Adapter, Power Cord, RJ-11 cable, (Option)
SAFETY LOCK	Security Lock hole (Kensington Lock)
Architecture	- Support PC2001 specifications; - WHQL-certified for Windows XP Professional/Home edition SP2
Sales Region	Europe USA
Agency	FCC, CE, CB,
Retailer Option Summary	CPU Memory Wireless Card HDD Battery ODD MDC

2. System View and Disassembly

2.1 System View

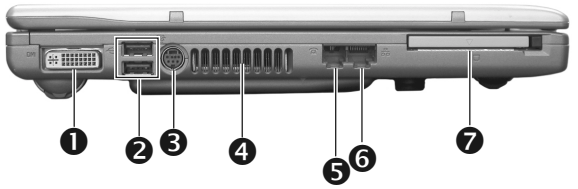
2.1.1 Front View

❶ 1394 Port
❷ Line Out Connector
❸ Line In Connector
❹ MIC In Connector
❺ MS/SD/MMC Card Slot
❻ Top Cover Latch



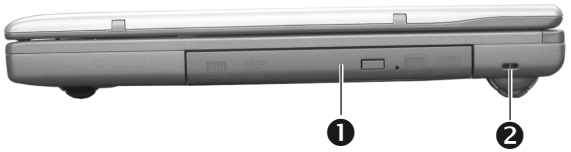
2.1.2 Left-side View

❶ DVI Port
❷ USB Ports *2
❸ S-Video Port
❹ Ventilation Openings
❺ RJ-11 Connector
❻ RJ-45 Connector
❼ PCMCIA Card Socket



2.1.3 Right-side View

❶ CD/DVD-ROM Drive
❷ Kensington Lock

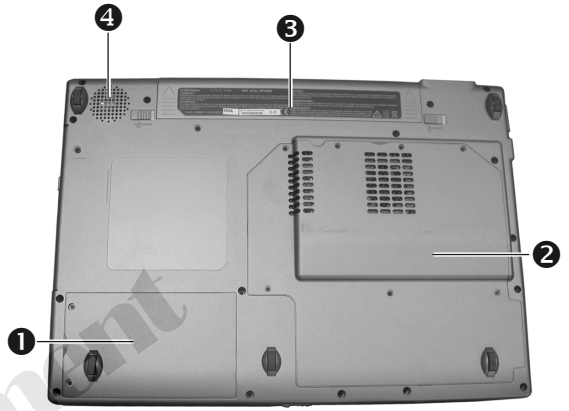


2.1.4 Rear View

❶ Lock
❷ AC Power Connector
❸ USB Ports *2

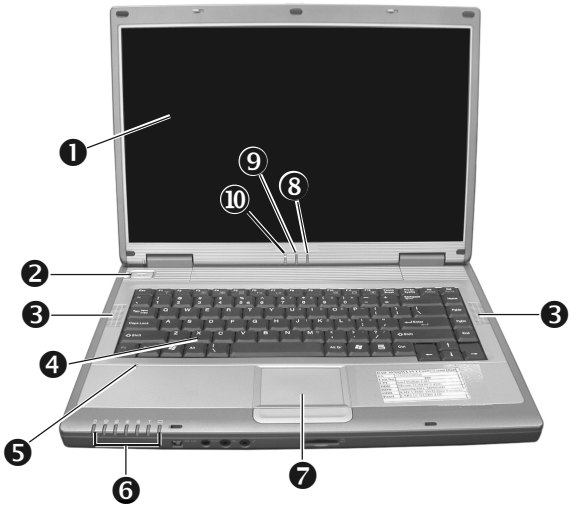
2.1.5 Bottom View

❶ Hard Disk Drive
❷ CPU
❸ Battery Park
❹ Stereo Speaker Set



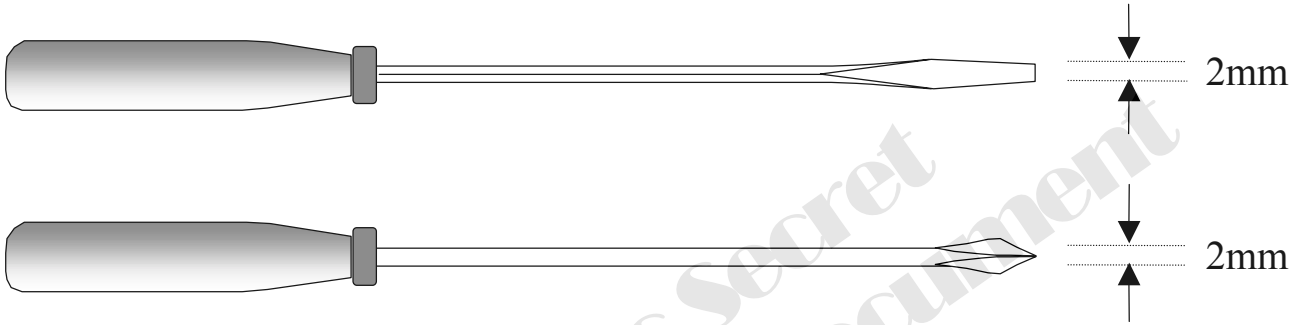
2.1.6 Top-open View

❶ LCD Screen
❷ Power Button
❸ Stereo Speaker Set
❹ Keyboard
❺ Internal MIC In
❻ Device LED Indicators
❼ Touch Pad
❽ AC Power Indicator
❾ Battery Charge Indicator
❿ Battery Power Indicator

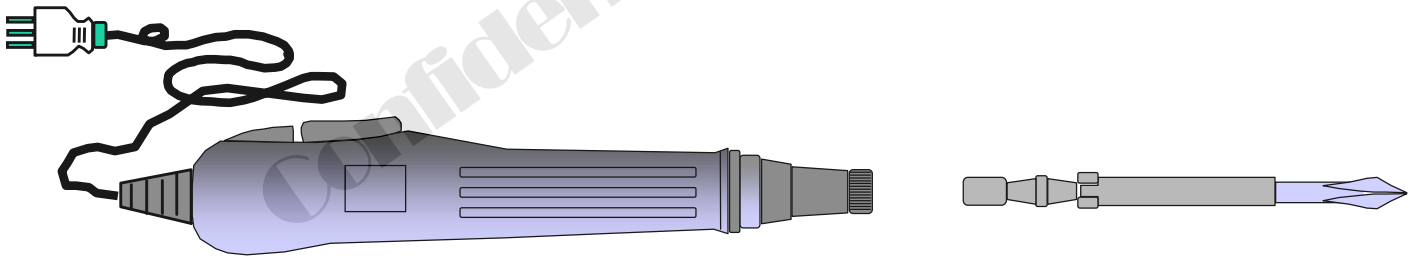


2.2 Tools Introduction

1. Minus screw driver with bit size 2mm for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

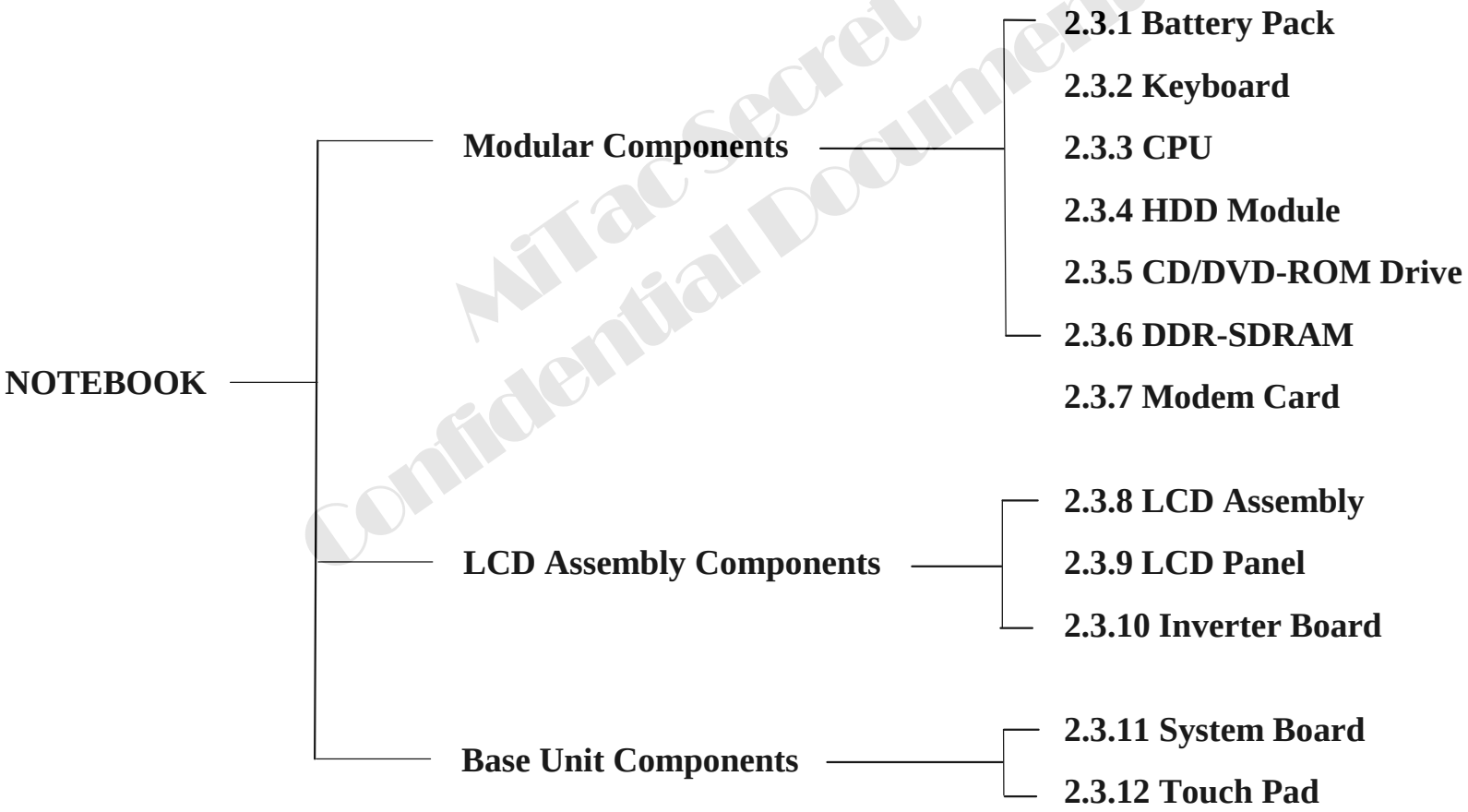
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

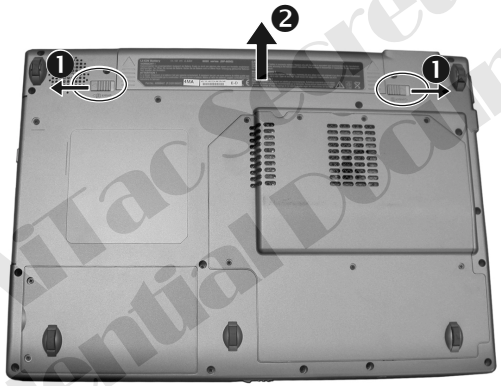


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" (🔒) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Open the top cover.
3. Loosen the five latches locking the keyboard. (Figure 2-2)

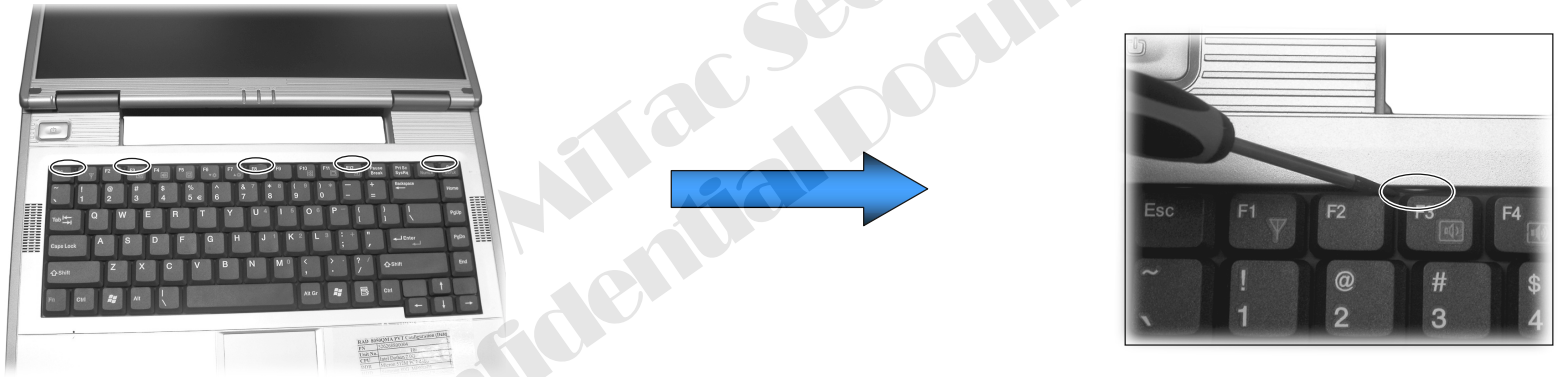


Figure 2-2 Loose the five latches

4. Slightly lift up the keyboard and disconnect the cable from the system board, then separate the keyboard. (Figure 2-3)

Figure 2-3 Free the keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard fasten the five latches.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Figure 2-4)
3. Remove the four spring screws and two screws that secure the heatsink upon the CPU and disconnect the fan's power cord from the system board. (Figure 2-5)

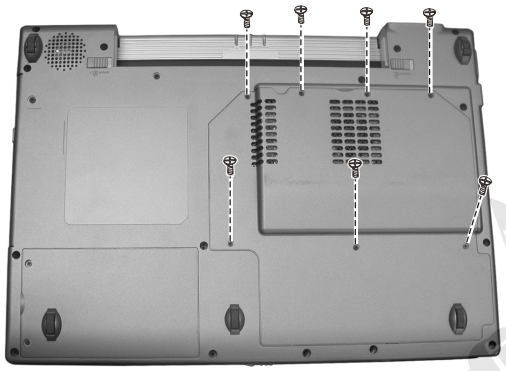


Figure 2-4 Remove the seven screws

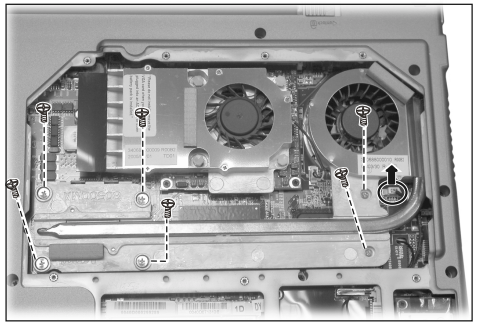


Figure 2-5 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver, upraise the CPU socket to unlock the CPU. (Figure 2-6)

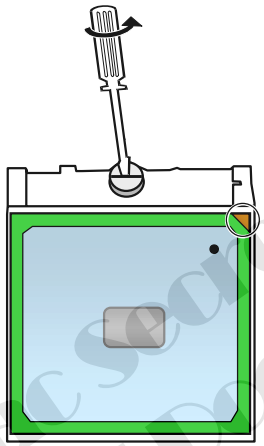


Figure 2-6 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU, then secure with four spring screws and two screws.
3. Replace the CPU cover and secure with seven screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-8)

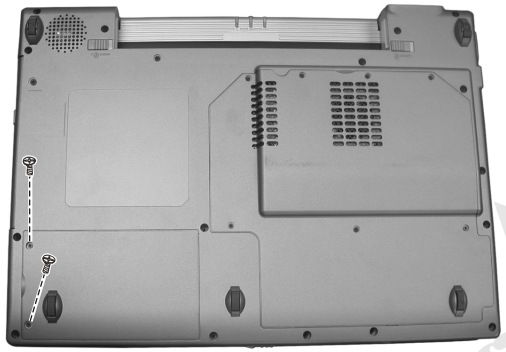


Figure 2-7 Remove the HDD compartment cover

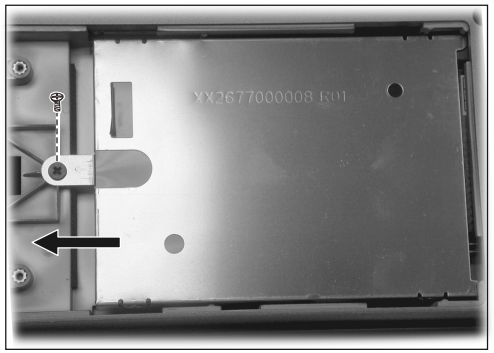


Figure 2-8 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-9)

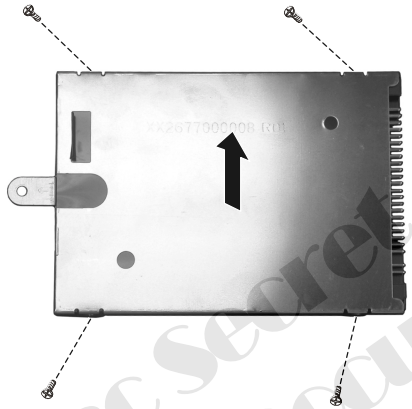


Figure 2-9 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the one screw fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷).

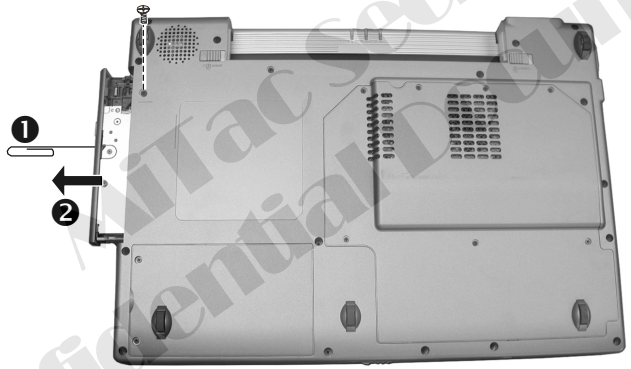


Figure 2-10 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.6 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to the step 2 of section 2.3.3 Disassembly)

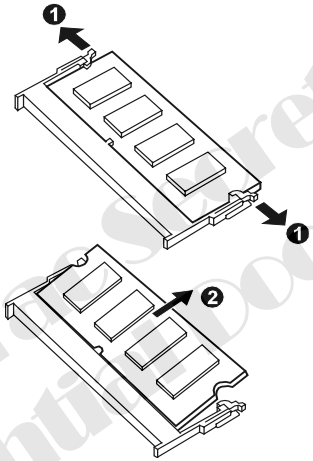


Figure 2-11 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-11)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with seven screws. (Refer to the step 3 of section 2.3.3 Reassembly)
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove seven screws fastening CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-12)
4. Lift up the modem card and disconnect the cord. (Figure 2-13)

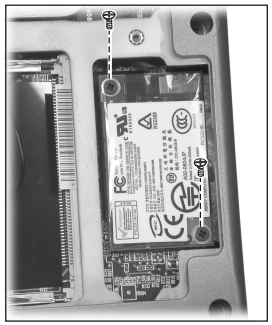


Figure 2-12 Remove two screws

Figure 2-13 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the CPU cover by seven screws. (Refer to step 3 of section 2.3.3 Reassembly).
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.8 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR and modem card. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.7 Disassembly)
2. Remove the eighteen screws fastening the housing and separate the antenna from the Mini PCI compartment. (Figure 2-14)
3. Disconnect the touch pad's cable from the system board and remove the two screws, then free the top cover. (Figure 2-15)

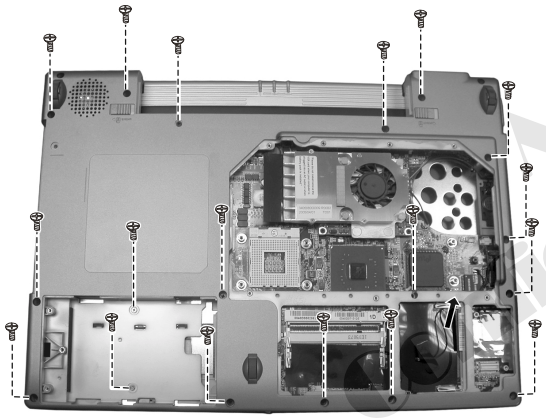


Figure 2-14 Remove the eighteen screws and separate the antenna

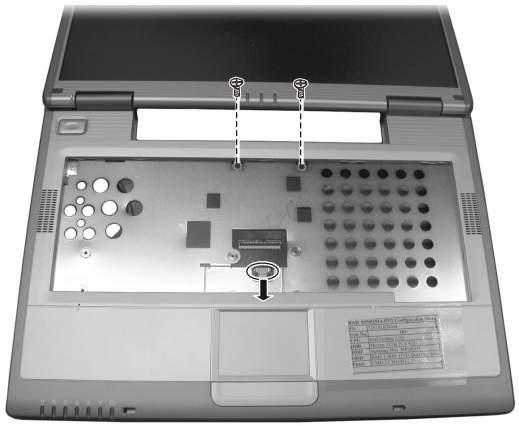


Figure 2-15 Free the top cover

4. Remove the seven screws and lift the top shielding up, then free the top shielding. (Figure 2-16)
5. Separate the antenna and disconnect the two cables from the system board. (Figure 2-17)

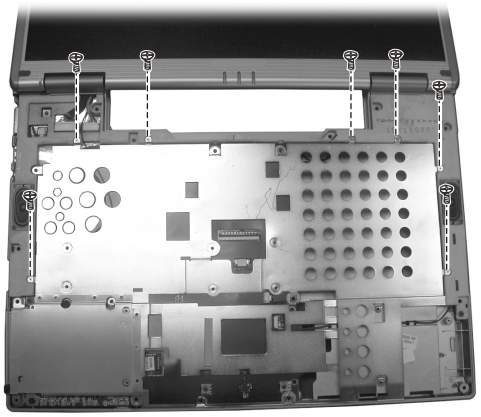


Figure 2-16 Remove the seven screws

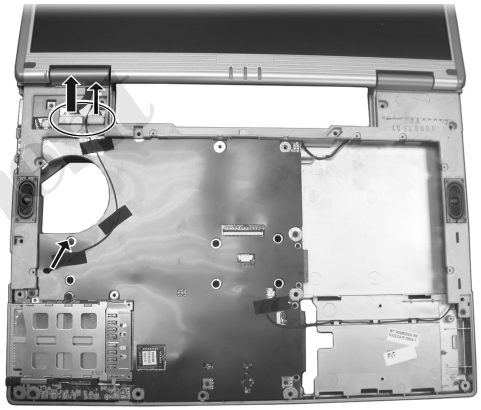


Figure 2-17 Disconnect the two cables and separate the antenna

6. Remove the two screws and lift the two hinge covers up, then free the two hinge covers. (Figure 2-18)
7. Remove the four screws, then free the LCD assembly. (Figure 2-19)

Figure 2-18 Free the two hinge covers

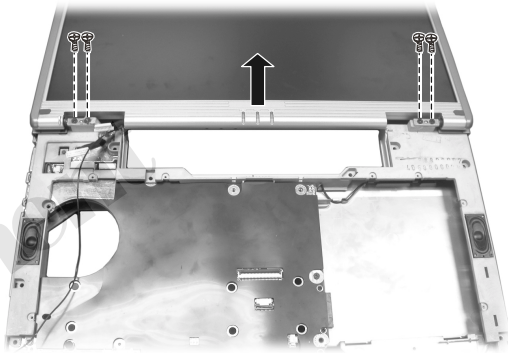


Figure 2-19 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna back into Mini PCI compartment.
3. Reconnect the two cables to the system board.
4. Replace the two hinge covers and secure with two screws.
5. Replace the top shielding and secure with seven screws.
6. Replace the top cover and secure with two screws, then reconnect the touch pad's cable into the system board.
7. Secure with eighteen screws fasten the housing.
8. Replace the modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.9 LCD Panel

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card and LCD assembly. (Refer to section 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-20)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the ten screws and disconnect the cable. (Figure 2-21)

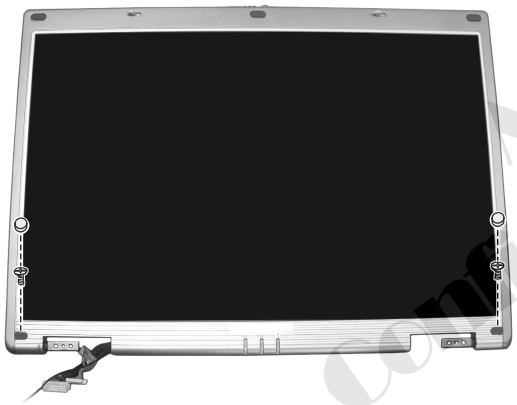


Figure 2-20 Remove LCD cover

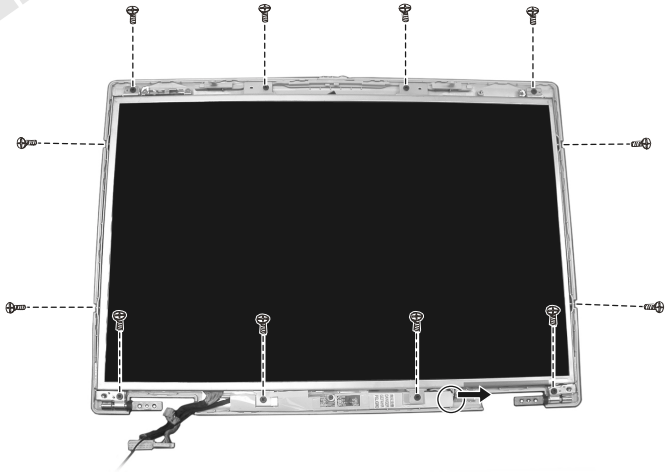


Figure 2-21 Remove the ten screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-22)
6. Disconnect the cable to free the LCD panel. (Figure 2-23)

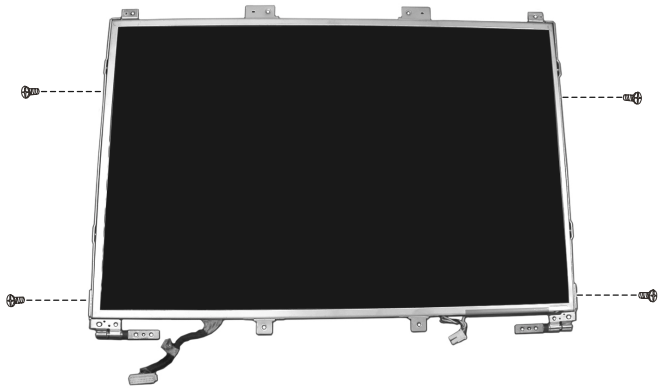


Figure 2-22 Remove the four screws

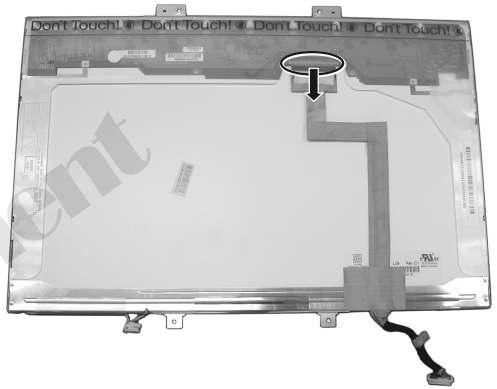


Figure 2-23 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing and secure with ten screws.
4. Reconnect one cable to inverter board.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.10 Inverter Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card, LCD assembly and LCD panel. (Refer to section 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7, 2.3.8 and 2.3.9 Disassembly)
2. Remove the one screw fastening the inverter board, then free the inverter board. (Figure 2-24)

Figure 2-24 Free the inverter board

Reassembly

1. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD panel, LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU keyboard and battery pack. (Refer to previous section reassembly)

2.3.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Remove the two screws fastening the housing. (Figure 2-25)
3. Remove the two screws fastening the housing. (Figure 2-26)

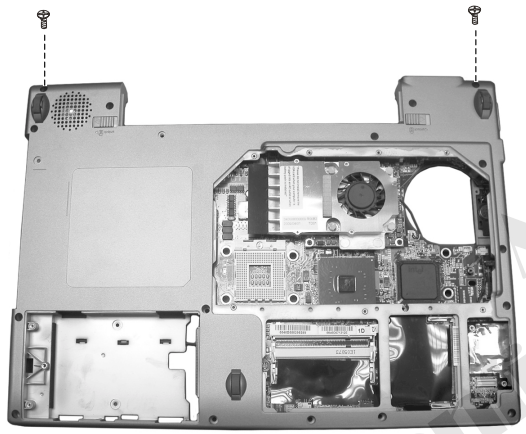


Figure 2-25 Remove the two screws

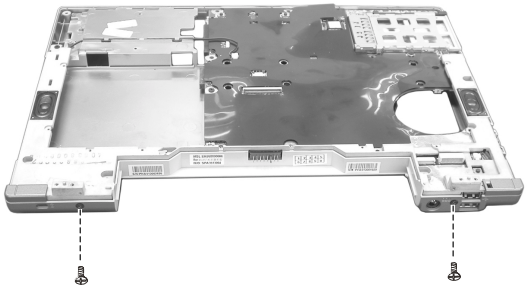


Figure 2-26 Remove the two screws

4. Disconnect the three speakers' cables from the system board and separate the (R&L) rear covers. (Figure 2-27)
5. Remove the four screws and lift the system board from the housing. (Figure 2-28)

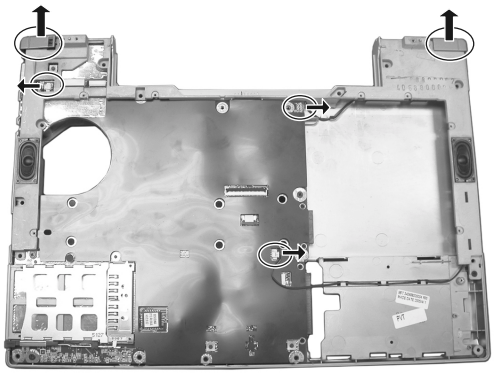


Figure 2-27 Disconnect the cables and separate the rear covers

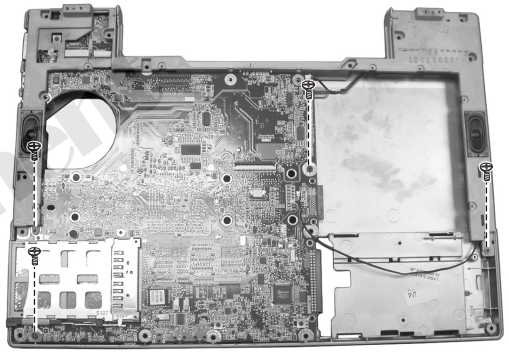


Figure 2-28 Remove the four screws

6. Remove the two screws and separate the I/O bracket from the system board, then free the system board. (Figure 2-29)

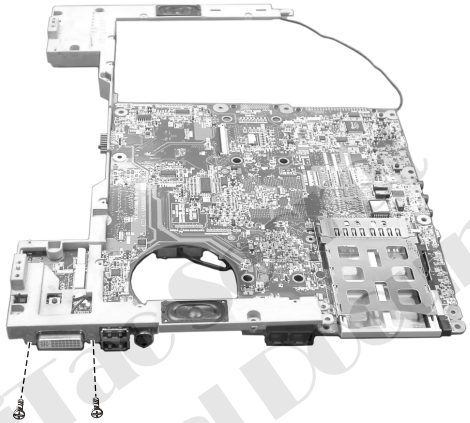


Figure 2-29 Free the system board

Reassembly

1. Fit the system board into the I/O bracket and secure with two screws.
2. Replace the system board into the housing and secure with four screws.
3. Reconnect the three speakers' cables into the system board and replace the (R&L) rear covers.
4. Secure with four screws fasten the housing.
5. Replace the LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to the section 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 Reassembly)

2.3.12 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR and modem card. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.7 Disassembly)
2. Remove the top cover. (Refer to the steps 1-3 of 2.3.8 section Disassembly)
3. Remove the four screws and lift the shielding, then free the touch pad. (Figure 2-30)

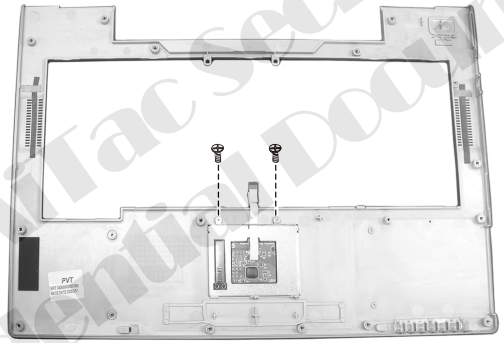


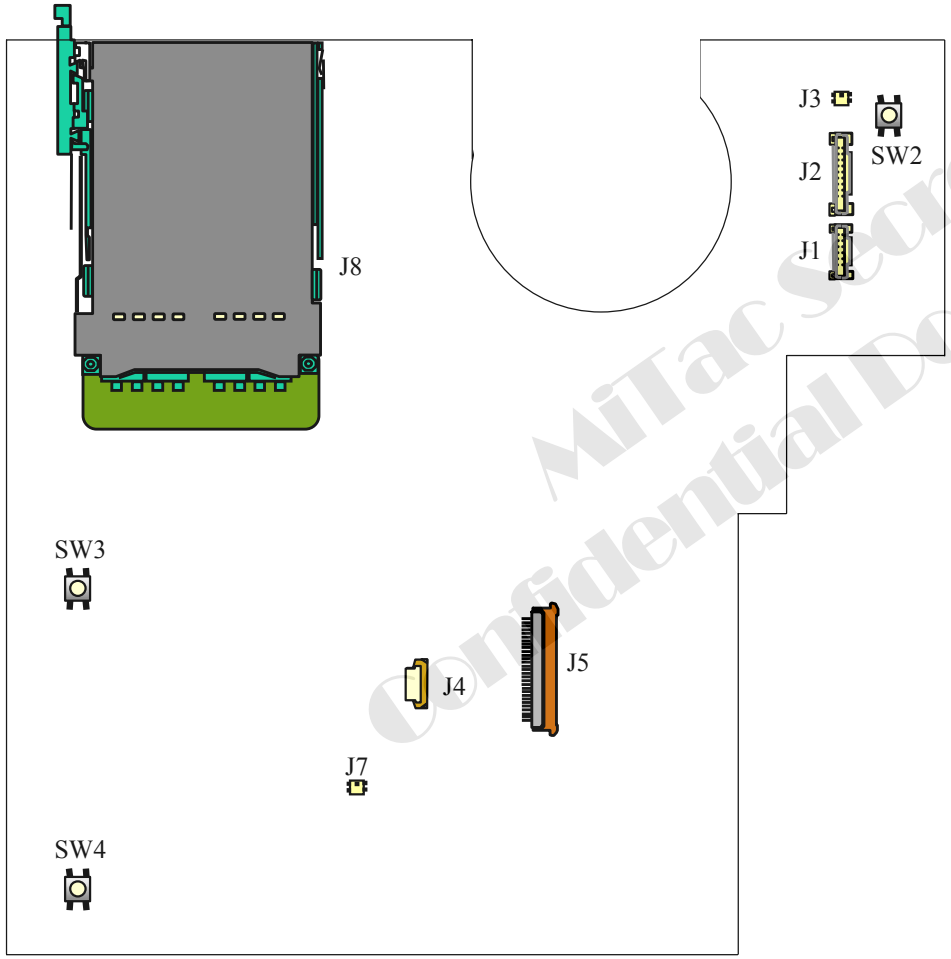
Figure 2-30 Free the touch pad

Reassembly

1. Replace the touch pad, then fit the shielding and secure with two screws.
2. Replace the top cover. (Refer to the step 6 of section 2.3.8 Disassembly)
3. Replace the modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (See sections 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A)

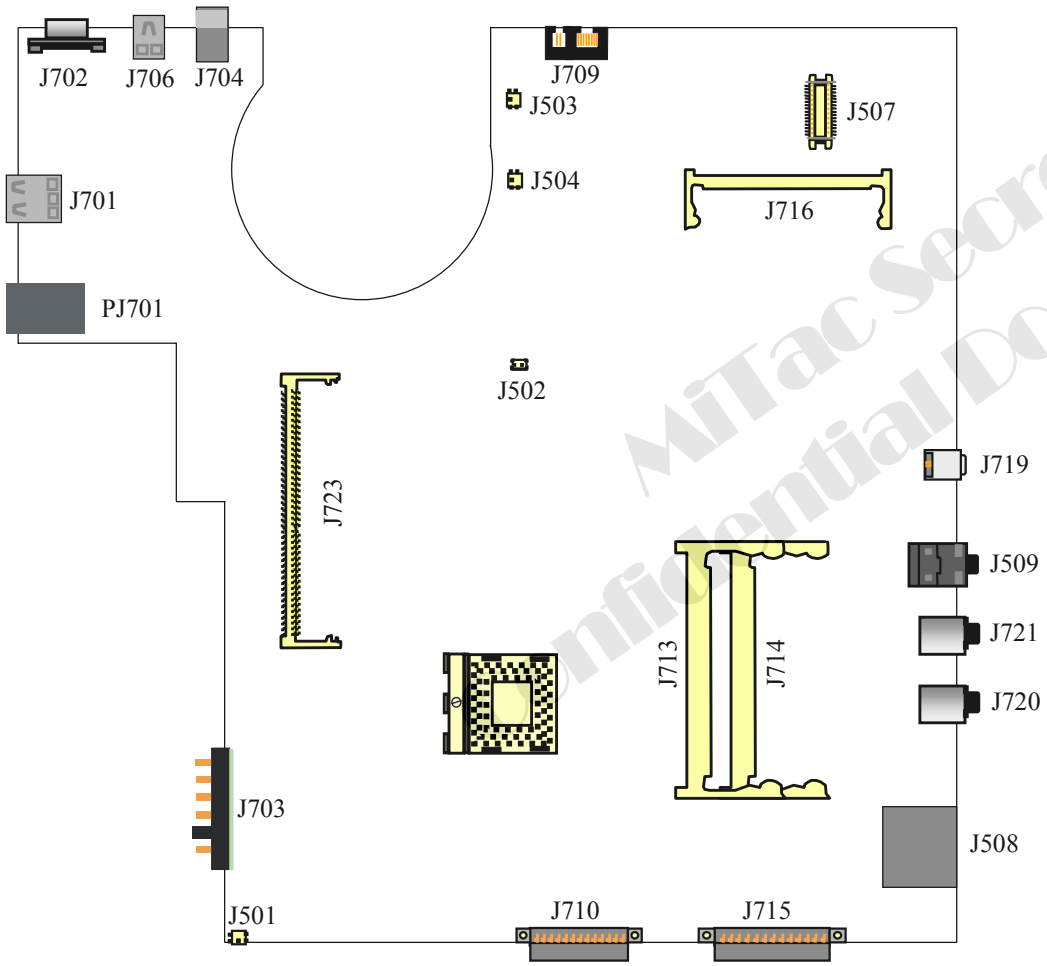


- J1 : Inverter Board Connector
- J2 : LCD Panel Connector
- J3 : Internal Left Speaker Connector
- J4 : Touch-pad Module Connector
- J5 : Internal Key-board Connector
- J7 : Internal Right Speaker Connector
- J8 : PCMCIA Card Connector

- SW2 : Power Button
- SW3 : Left Button Switch of Touch-pad
- SW4 : Right Button Switch of Touch-pad

3. Definition & Location of Connectors / Switches

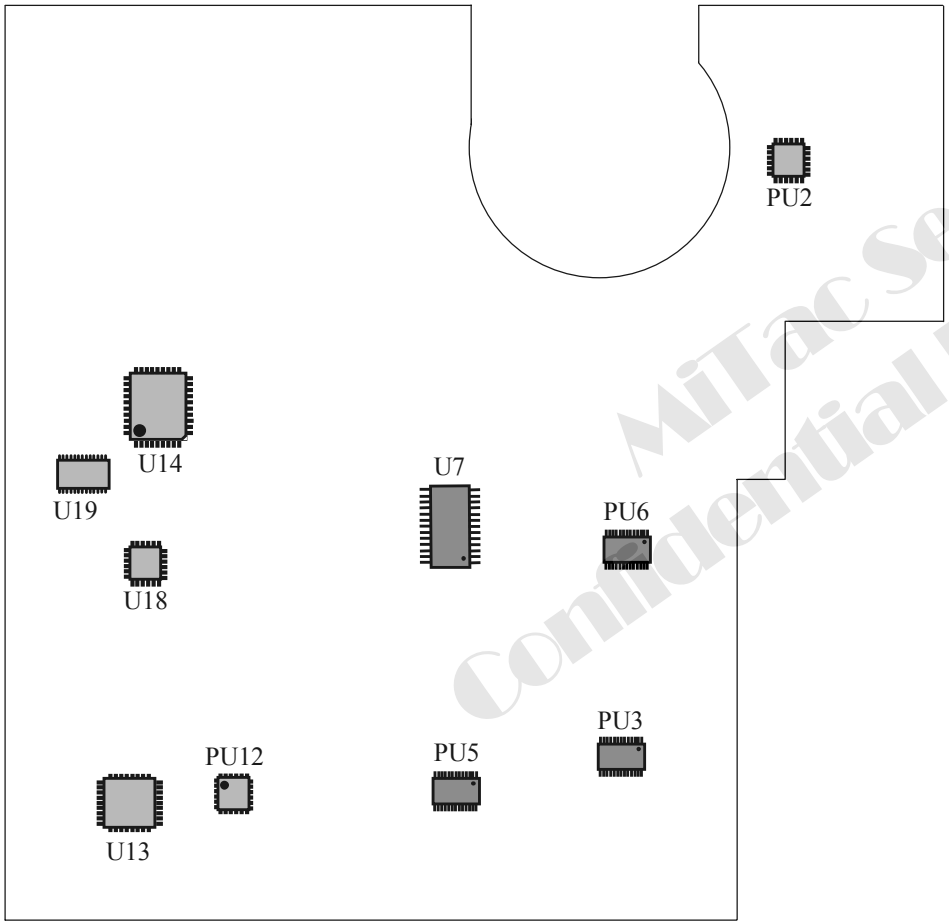
3.2 Mother Board (Side B)



- PJ701 : AC Adaptor Connector
- J701&J706 : USB Port Connector
- J702 : DVI Connector
- J703 : Battery Connector
- J704 : S-video Connector
- J709 : RJ45 & RJ11 Connector
- J710 : CD-ROM IDE Connector
- J713&J714 : DDR SO-DIMM Module Socket
- J715 : Hard Disk Driver Connector
- J716 : Mini-PCI Connector
- J723 : MXM_Connector
- J501 : Internal Subwoofer Speaker
- J502 : FAN Connector
- J504 : FAN Connector
- J508 : MS/SD/MMC Connector

4. Definition & Location of Major Components

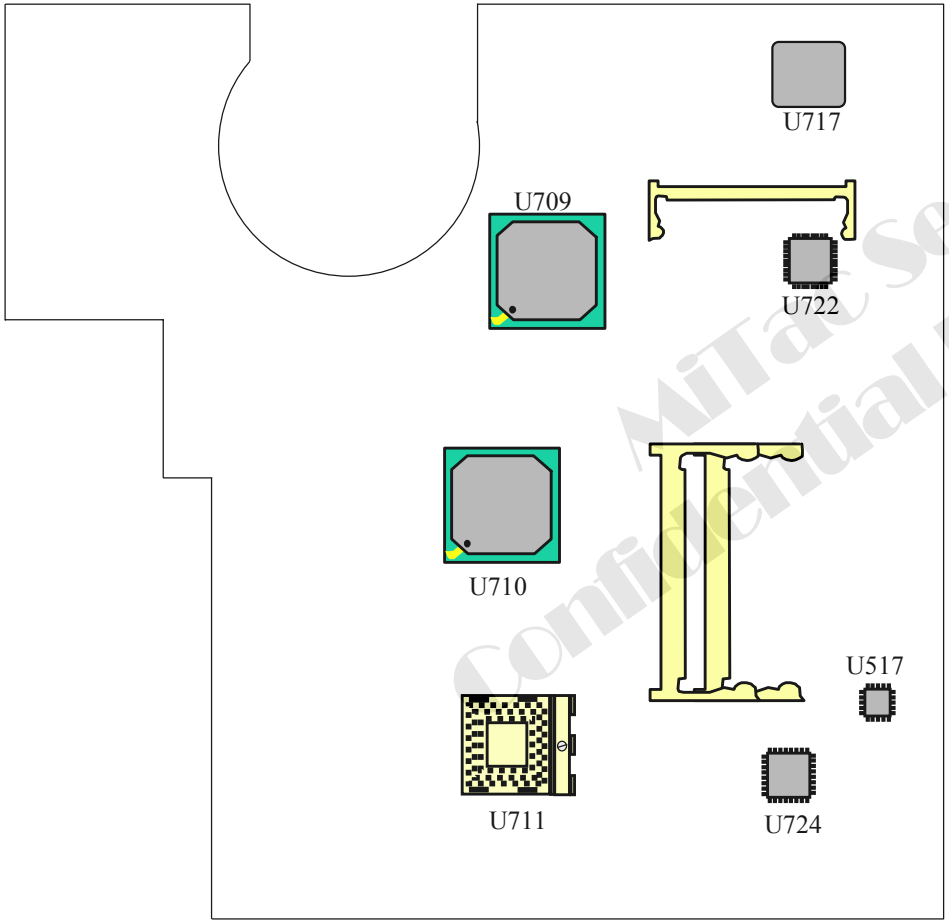
4.1 Mother Board (Side A)



- PU2 : +3VS/+5VS Voltage Generator
- PU3 : Charging Voltage Controller
- PU5 : CPU_Core Voltage Generator
- PU6 : +1.5VS/+1.05VS Voltage Generator
- PU12 : +1.8V_P/0.9VS_P Voltage Generate
- U7 : CLOCK SYNTHERIZER
- U13 : WINBOND KBC Controller
- U14 : SYSTEM BIOS
- U18 : SUBWOOFER AMP Controller
- U19 : AUDIO AMPLIFIER

4. Definition & Location of Major Components

4.2 Mother Board (Side B)



- U709 : Intel ICH6-M South Bridge
- U710 : Intel 915PM North Bridge
- U711 : Intel Dothan CPU
- U717 : LAN-RTL8100CL Controller
- U722 : IEEE1394 Controller
- U724 : Serial ATA Bridge 88SA8040
- U517 : Audio CODEC(ALC655)

5. Pin Descriptions of Major Components

5.1 Intel 915PM North Bridge(1)

Host Interface Signals

Signal Name	Type	Description
HADS#	I/O AGTL+	**Host Address Strobe:** The system bus owner asserts HADS# to indicate the first of two cycles of a request phase. The GMCH can also assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O AGTL+	**Host Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
HBPRI#	O AGTL+	**Host Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O AGTL+	**Host Bus Request 0#:** The GMCH pulls the processor bus HBREQ**0#** signal low during HCPURST#. The signal is sampled by the processor on the active-to-inactive transition of HCPURST#. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O AGTL+	**Host CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. HCPURS**T#** allows the processor to begin execution in a known state.
HDBSY#	I/O AGTL+	**Host Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O AGTL+	**Host Defer:** Signals that the GMCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O AGTL+	**Host Dynamic Bus Inversion:** Driven along with the HFD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINVF[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **HDINV# Data Bits** HDINV[3]# HD[63:48]# HDINV[2]# HD[47:32]# HDINV[1]# HD[31:16]# HDINV[0]# HD[15:0]#

Host Interface Signals (Continued)

Signal Name	Type	Description
HDRDY#	I/O AGTL+	**Host Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of DMI. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Host Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV[3:0]# at the 4x transfer rate. **Strobe Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, HDINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, HDINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, HDINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:00]#, HDINV[0]#
HHIT#	I/O AGTL+	**Host Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HHITM#	I/O AGTL+	**Host Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.

5.1 Intel 915PM North Bridge(2)

Host Interface Signals (Continued)

Signal Name	Type	Description
HLOCK#	I AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic, i.e. *PCI Express graphics access* to System Memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O AGTL+	**Host Response Status:** Indicates the type of response according to the following the table: **HRS[2:0]# Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by GMCH) 100 Hard Failure (not driven by GMCH) 101 No data response 110 Implicit Write back 111 Normal data response
HDPWR#	O AGTL+	**Host Data Power:** Used by GMCH to indicate that a data return cycle is pending within 2 HCLK cycles or more. CPU use's this signal during a read-cycle to activate the data input buffers in preparation for HDRDY# and the related data.
HCPUSLP#	O CMOS	**Host CPU Sleep:** When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts.

Host Interface Reference and Compensation

Signal Name	Type	Description
HVREF	I A	**Host Reference Voltage:** Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface.
HXRCOMP	I/O A	**Host X RCOMP:** Used to calibrate the Host AGTL+ I/O buffers. This signal is powered by the Host Interface termination rail (VCCP).
HXSCOMP	I/O A	**Host X SCOMP**: Slew Rate Compensation for the Host Interface
HXSWING	I A	**Host X Voltage Swing:** These signals provide reference voltages used by the HXRCOMP circuits.
HYRCOMP	I/O A	**Host Y RCOMP**: Used to calibrate the Host AGTL+ I/O buffers.
HYSCOMP	I/O A	**Host Y SCOMP:** Slew Rate Compensation for the Host Interface
HYSWING	I A	**Host Y Voltage Swing:** These signals provide reference voltages used by the HYRCOMP circuitry.

DMI

Signal Name	Type	Description
DMI_RXP[1:0] DMI_RXN[1:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[1:0] DMI_TXN[1:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

DMI x2 is supported for Intel 915GMS chipset

5.1 Intel 915PM North Bridge(3)

DDR / DDR2 SDRAM Channel A Interface

Signal Name	Type	Description
SA_DQ[63:0]	I/O SSTL1.8/2 2x	**Data Bus:** DDR / DDR2 Channel A data signal interface to the SDRAM data bus. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DM[7:0]	I/O SSTL1.8/2 2x	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]	I/O SSTL1.8 2x	**Data Strobes:** DDR: The rising and falling edges of SA_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_MA[13:0]	O SSTL1.8/2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_MA13 is for support of 1 Gb devices.
SA_BS[2:0]	O SSTL1.8/2	**Bank Selec**t: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_BS2 is for support for DDR2 only for 8 bank devices.

DDR / DDR2 SDRAM Channel A Interface (Continued)

Signal Name	Type	Description
SA_RAS#	O SSTL1.8/2	**RAS Control signa**l: Used with SA_CAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_CAS#	O SSTL1.8/2	**CAS Control signal:** Used with SA_RAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_WE#	O SSTL1.8/2	**Write Enable Control signal:** Used with SA_RAS# and SA_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_RCVENIN#	O SSTL1.8/2	**Clock Input:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENOUT#. Leave as No Connect.
SA_RCVENOUT#	O SSTL1.8/2	**Clock Output:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENIN#. Leave as No Connect.

PCI Express Based Graphics Interface Signals

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I PCIE	PCI Express Receive Differential Pair
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	PCI Express Transmit Differential Pair
EXP_ICOMPO	I A	PCI Express Output Current and Resistance Compensation
EXP_COMPI	I A	PCI Express Input Current Compensation

PCI Express Based Graphics is supported for Intel 915GM and Intel 915PM chipsets.

5.1 Intel 915PM North Bridge(4)

DDR / DDR2 SDRAM Channel B Interface

Signal Name	Type	Description
SB_DQ[63:0]	I/O SSTL1.8/2 2x	**Data Line**s: DDR / DDR2 Channel B data signal interface to the SDRAM data bus. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DM[7:0]	O SSTL1.8/2 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane. These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]	I/O SSTL1.8/2 2x	**Data Strobes:** DDR: The rising and falling edges of SB_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** (DDR2 only): DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_MA[13:0]	O SSTL1.8/2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: SB_MA13 is for support of 1 Gb devices.
SB_BS[2:0]	O SSTL1.8/2	**Bank Selec**t: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: SB_BS2 is for DDR2 support only.

DDR / DDR2 SDRAM Channel B Interface (Continued)

Signal Name	Type	Description
SB_RAS#	O SSTL1.8/2	**RAS Control signa**l: Used with SB_CAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_CAS#	O SSTL1.8/2	**CAS Control signal:** Used with SB_RAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_WE#	O SSTL1.8/2	**Write Enable Control signal:** Used with SB_RAS# and SB_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_RCVENIN#	I SSTL1.8/2	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOT**E: Signals do not exist in Intel 915GMS.
SB_RCVENOUT#	O SSTL1.8/2	**Clock Output:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOT**E: Signals do not exist in Intel 915GMS.

DMI

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[3:0] DMI_TXN[3:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

DMI x2 or x4 is supported for Intel 915GM, Intel 915PM and Intel 910GML chipsets.

5.1 Intel 915PM North Bridge(5)

DDR / DDR2 Common Signals

Signal Name	Type	Description
SM_CK[1:0], SM_CK[4:3]	O SSTL1.8/2	**SDRAM Differential Clock:** The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM. **SM_CK[0:1]** and its complement **SM_CK[1:0]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CK[4:3]** and its complement **SM_CK[4:3]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: **SM_CK2** and **SM_CK5** are reserved and not supported.
SM_CK[1:0]#, SM_CK[4:3]#	O SSTL1.8/2	**SDRAM Inverted Differential Clock:** These are the complementary Differential DDR2 Clock signals. **NOT**E: **SM_CK2#** and **SM_CK5#** are reserved and not supported.
SM_CS[3:0]#	O SSTL1.8/2	**Chip Select:** (1 per Rank): These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank **SM_CS[1:0]#** : Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CS[3:2]#** : Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SM_CKE[3:0]	O SSTL1.8/2	**Clock Enable:** (1 per Rank): SM_CKE[3:0] is used: .To initialize the SDRAMs during power-up .To power-down SDRAM ranks . To place all SDRAM ranks into and out of self-refresh during STR. SM_CKE[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A SM_CKE[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B

DDR / DDR2 Common Signals (Continued)

Signal Name	Type	Description
SM_ODT[3:0]	O SSTL1.8/2	**On Die Termination: Active Termination Contro**l. (DDR2 only) SM_ODT[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A *Signal Description* The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control **SM_CK[0:1]** and its complement **SM_CK[1:0]#** signal make a differential **SM_CK[4:3]** and its complement **SM_CK[4:3]#** signal make a differential **NOT**E: **SM_CK2** and **SM_CK5** are reserved and not supported. These are the complementary Differential DDR2 Clock signals. **NOT**E: **SM_CK2#** and **SM_CK5#** are reserved and not supported. These signals select particular SDRAM components during the active To place all SDRAM ranks into and out of self-refresh during STR. **On Die Termination: Active Termination Contro**l. (DDR2 only) SM_ODT[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B DDR: Leave as no connects. Not used for DDR devices. DDR2: On-die termination for DDR2 devices.

5.1 Intel 915PM North Bridge(6)

CRT DAC Signals

Signal Name	Type	Description
RED	O A	**RED Analog Video Output**: This signal is a CRT Analog video output from the internal color palette DAC.
RED#	O A	**RED# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
GREEN#	O A	**GREEN# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
REFSET	O A	**Resistor Set**: Set point resistor for the internal color palette DAC. A 256-Ω ± 1% resistor is required between REFSET and motherboard ground.
HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”.
VSYNC	O HVCMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync (polarity is programmable).

Analog TV-out Signals

Signal Name	Type	Description
TVDAC_A	O A	**TVDAC Channel A Output:** TVDAC_A supports the following: **Composite**: CVBS signal **Component**: Chrominance (Pb) analog signal
TVDAC_B	O A	**TVDAC Channel B Output:** TVDAC_B supports the following: **S-Video**: Luminance analog signal **Component**: Luminance (Y) analog signal
TVDAC_C	O A	**TVDAC Channel C Output:** TVDAC_C supports the following: **S-Video**: Chrominance analog signal **Component**: Chrominance (Pr) analog signal
TV_IRTNA	O A	**Current Return for TVDAC Channel A:** Connect to ground on board
TV_IRTNB	O A	**Current Return for TVDAC Channel B:** Connect to ground on board
TV_IRTNC	O A	**Current Return for TVDAC Channel C:** Connect to ground on board
TV_REFSET	O A	**TV Resistor set:** TV Reference Current uses an external resistor to set internal reference voltage levels. A 5-k §Ù ± 0.5% resistor is required between REFSET and motherboard ground.

5.1 Intel 915PM North Bridge(7)

Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
LCTLA_CLK	I/O COD	I2C Based control signal (Clock) for External SSC clock chip control –
LCTLB_DATA	I/O COD	I2C Based control signal (Data) for External SSC clock chip control –
DDCCLK	I/O COD	CRT DDC clock monitor control support
DDCDATA	I/O COD	CRT DDC Data monitor control support
LDDC_CLK	I/O COD	EDID support for flat panel display
LDDC_DATA	I/O COD	EDID support for flat panel display
SDVOCTRL_CLK	I/O COD	I2C Based control signal (Clock) for SDVO device
SDVOCTRL_DATA	I/O COD	I2C Based control signal (Data) for SDVO device

DDR SDRAM Reference and Compensation

Signal Name	Type	Description
SMRCOMPN	I/O A	**System Memory RCOMP** N: Buffer compensation This signal is powered by the System Memory rail (2.5 V for DDR, 1.8 V for DDR2).
SMRCOMPP	I/O A	**System Memory RCOMP** P: Buffer compensation This signal is powered by the System Memory rail
SMXSLEWIN	I A	**X Buffer Slew Rate Input control.**
SMXSLEWOUT	O A	**X Buffer Slew Rate Output control.**
SMYSLEWIN	I A	**Y Buffer Slew Rate Input control.**
SMYSLEWOUT	O A	**Y Buffer Slew Rate Output control.**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DQS, & RCVENIN#. Also used during ODT RCOMP.
SMOCDCOMP[1:0]	I A	**On-Die DRAM OCD driver compensation** OCD compensation

LVDS Signals

Signal Name	Type	Description
LDVS Channel A		
LADATAP[2:0]	I/O LVDS	Channel A differential data output - positive
LADATAN[2:0]	I/O LVDS	Channel A differential data output –negative
LACLKP	I/O LVDS	Channel A differential clock output – positive
LACLKN	I/O LVDS	Channel A differential clock output – negative
LDVS Channel B		
LBDATAP[2:0]	I/O LVDS	Channel B differential data output – positive **NOT**E: Signals do not exist in Intel 915GMS.
LBDATAN[2:0]	I/O LVDS	Channel B differential data output –negative **NOT**E: Signals do not exist in Intel 915GMS.
LBCLKP	I/O LVDS	Channel B differential clock output – positive **NOT**E: Signals do not exist in Intel 915GMS.
LBCLKN	I/O LVDS	Channel B differential clock output – negative **NOT**E: Signals do not exist in Intel 915GMS.
LFP Panel power and backlight control		
LVDD_EN	O HVCMOS	LVDS panel power enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.
LBKLT_EN	O HVCMOS	LVDS backlight enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
LBKLT_CRTL	O HVCMOS	Panel backlight brightness control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
LVDS Reference signals		
LIBG	I/O Ref	LVDS Reference Current. – 1.5 kΩ Pull down resistor needed
LVREFH	I Ref	Reserved. - No connect.
LVREFL	I Ref	Reserved. - No connect.
LVBG	O A	Reserve. - No connect

Note: LVDS Channel B interface is not supported and do not exist for Intel 915GMS

5.1 Intel 915PM North Bridge(8)

Serial DVO Interface.

Signal Name	Type	Description
SDVO B Interface		
SDVOB_CLKP	O PCIE	Serial Digital Video B Clock. Multiplexed with EXP_TXP_3.
SDVOB_CLKN	O PCIE	Serial Digital Video B Clock Complement. Multiplexed with EXP_TXN_3.
SDVOB_RED	O PCIE	Serial Digital Video B Red Data. Multiplexed with EXP_TXP_0.
SDVOB_RED#	O PCIE	Serial Digital Video B Red Data Complement. Multiplexed with EXP_TXN_0.
SDVOB_GREEN	O PCIE	Serial Digital Video B Green Data. Multiplexed with EXP_TXP_1.
SDVOB_GREEN#	O PCIE	Serial Digital Video B Green Data Complement. Multiplexed with EXP_TXN_1.
SDVOB_BLUE	O PCIE	Serial Digital Video B Blue Data. Multiplexed with EXP_TXP_2.
SDVOB_BLUE#	O PCIE	Serial Digital Video B Blue Data Complement. Multiplexed with EXP_TXN_2.
SDVO C Interface		
SDVOC_RED	O PCIE	Serial Digital Video C Red Data / SDVO B Alpha. Multiplexed with EXP_TXP_4. **NOT**E: Signals do not exist in Intel 915GMS..
SDVOC_RED#	O PCIE	Serial Digital Video C Red Complement / Alpha Complement. Multiplexed with EXP_TXN_4. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_GREEN	O PCIE	Serial Digital Video C Green. Multiplexed with EXP_TXP_5. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_GREEN#	O PCIE	Serial Digital Video C Green Complement. Multiplexed with EXP_TXN_5. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_BLUE	O PCIE	Serial Digital Video Channel C Blue. Multiplexed with EXP_TXP_6. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_BLUE#	O PCIE	Serial Digital Video C Blue Complement. Multiplexed with EXP_TXN_6. **NOT**E: Signals do not exist in Intel 915GMS.

Serial DVO Interface (Continued)

Signal Name	Type	Description
SDVO C Interface		
SDVOC_CLKP	O PCIE	Serial Digital Video C Clock. Multiplexed with EXP_TXP_7. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_CLKN	O PCIE	Serial Digital Video C Clock Complement. Multiplexed with EXP_TXN_7. **NOT**E: Signals do not exist in Intel 915GMS.
SDVO Common Signals		
SDVO_TVCLKIN	I PCIE	Serial Digital Video TVOUT Synchronization Clock. Multiplexed with EXP_RXP_0.
SDVO_TVCLKIN#	I PCIE	Serial Digital Video TV-out Synchronization Clock Complement. Multiplexed with EXP_RXN_0.
SDVO_FLDSTALL	I PCIE	Serial Digital Video Field Stall. Multiplexed with EXP_RXP_2.
SDVO_FLDSTALL#	I PCIE	Serial Digital Video Field Stall Complement. Multiplexed with EXP_RXN_2.
SDVOB_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_1.
SDVOB_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_1.
SDVOC_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_5.
SDVOC_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_5.

5.1 Intel 915PM North Bridge(9)

Reset and Miscellaneous Signals

Signal Name	Type	Description
RSTIN#	I HVCMOS	**Reset In**: When asserted this signal will asynchronously reset the GMCH logic. This signal is connected to the PLT_RST# output of the ICH6-M. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.
PWROK	I HVCMOS	**Power OK**: When asserted, PWROK is an indication to the GMCH that core power has been stable for at least 10 µs. This input buffer is 3.3-V tolerant.
H_BSEL [2:0] (CFG[2:0])	I HVCMOS	**Host Bus Speed Select:** At the deassertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus. External pull-ups are required.
CFG[17:3]	I AGTL+	**HW straps:** CFG [17:3] has internal pull up. **NOT**E: Not all CFG Balls are supported for Intel 915GMS.
CFG[20:18]	I HVCMOS	**HW straps:** CFG [20:18] has internal pull down **NOT**E: Not all CFG Balls are supported for Intel 915GMS.
BM_BUSY#	O HVCMOS	**GMCH Integrated Graphics Busy**: Indicates to the ICH that the integrated graphics engine within the MCH is busy and transitions to low power states should not be attempted until that is no longer the case.
THRMTRIP#	O COD	**GMCH Thermal Trip**: Assertion of THERMTRIP# (Thermal Trip) indicates the GMCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the GMCH core junction temperature. To protect GMCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the GMCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.
EXT_TS[1:0]#	I HVCMOS	**External Thermal Sensor Input**: If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling. **NOT**E: EXT_TS1# functionality is not supported in 915GMS. A pull up is required on this pin

PLL Signals

Signal Name	Type	Description
HCLKP	I Diff Clk	**Differential Host Clock In**: Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the GMCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low voltage differential signal and runs at ¼ the FSB data rate.
HCLKN	I Diff Clk	**Differential Host Clock Input Complement:**
GCLKP	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In**: These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
GCLKN	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In complement**
DREF_CLKP	I Diff Clk	**Display PLLA Differential Clock In** – Display PLL Differential Clock In, no SSC support –
DREF_CLKN	I Diff Clk	**Display PLLA Differential Clock In Complement** – Display PLL Differential Clock In Complement - no SSC support
DREF_SSCLKP	I Diff Clk	**Display PLLB Differential Clock In** – Optional Display PLL Differential Clock In for SSC support – **NOT**E: Differential Clock input for optional SSC support for LVDS display.
DREF_SSCLKN	I Diff Clk	**Display PLLB Differential Clock In complement** – Optional Display PLL Differential Clock In Complement for SSC support **NOT**E: Differential Clock input for optional SSC support for LVDS display.

Note: PLL interfaces signal group are supported the Mobile Intel 915GM/PM/GMS and Intel 910GML Express chipsets, unless otherwise noted.

5.1 Intel 915PM North Bridge(10)

Power and Ground

Interface	Ball Name	Description
Host	VTT (VCCP)	FSB power supply (1.05 V) - (VCCP)
DRAM	VCCA_SM	VCCASM is the Analog power supply for SM data buffers used for DLL & other logic (1.5 V)
	VCCSM	System memory power supply (DDR=2.5 V; DDR2=1.8 V)
PCI Express Based Graphics /DMI	VCC3G	PCI Express / DMI Analog power supply (1.5 V)
	VCCA_3GBG	PCI Express / DMI band gap power supply (2.5 V)
	VSSA_3GBG	PCI Express / DMI band gap ground
PLL Analog	VCCA_HPLL	Power supply for the Host VCO in the host/mem/core PLL (1.5 V)
	VCCA_MPLL	Power supply for the mem VCO in the host/mem/core PLL (1.5 V)
	VCCD_HMPLL	Power Supply for the digital dividers in the HMPLL (1.5 V)
	VCCA_3GPLL	Power supply for the 3GIO PLL (1.5 V)
	VCCA_DPLLA	Display A PLL power supply (1.5 V)
	VCCA_DPLLB	Display B PLL power supply (1.5 V)
High Voltage Interfaces	VCCHV	Power supply for the HV buffers (2.5 V)
CRT DAC	VCCA_CRTDAC	Analog power supply for the DAC (2.5 V)
	VSSA_CRTDAC	Analog ground for the DAC
	VCC_SYNC	Power supply for HSYNC/ VSYNC (2.5 V)
LVDS	VCCD_LVDS	Digital power supply (1.5 V)
	VCCTX_LVDS	Data/Clk Tx power supply (2.5 V)
	VCCA_LVDS	LVDS analog power supply (2.5 V)
	VSSALVDS	LVDS analog VSS

Power and Ground (Continued)

Interface	Ball Name	Description
TVDAC	VCCA_TVBG	TV DAC Band Gap Power (3.3 V)
	VSSA_TVBG	TV DAC Band Gap VSS
	VCCD_TVDAC	Dedicated Power Supply for TVDAC (1.5 V)
	VCCDQ_TVDAC	Power Supply for Digital Quiet TVDAC (1.5 V)
	VCCA_TVDACA	Power Supply for TV Out Channel A (3.3 V)
	VCCA_TVDACB	Power Supply for TV Out Channel B (3.3 V)
	VCCA_TVDACC	Power Supply for TV Out Channel C (3.3 V)
Core	VCC	Core VCC – (1.05 V or 1.5 V)
Ground	VSS	Ground
NCTF	**Non-Critical To Function power signals:** "NCTF" (Non-Critical To Function) have been designed into the package footprint to enhance the Solder Joint Reliability of our products by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, these balls may crack partially or completely, however, this will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as sacrificial stress absorbers. **NOT**E: Signals do not exist in Intel 915GMS.	
	VTT_NCTF	NCTF FSB power supply (1.05 V or 1.2 V)
	VCC_NCTF	NTCF Core VCC – (1.05 V or 1.5 V)
	VCCSM_NCTF	NTCF System memory power supply (DDR=2.5 V; DDR2=1.8 V)
	VSS_NCTF	NTCF Ground

5.2 Intel ICH6-M South Bridge(1)

PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data**: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® ICH6 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enable**s: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH6 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Selec**t: The ICH6 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH6 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH6 address or an address destined DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH6-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH6 until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH6 when the ICH6 is the target, and FRAME# is an output from the ICH6 when the ICH6 is the initiator. FRAME# remains tri-stated by the ICH6 until driven by an initiator.

PCI Interface Signals (Continued)

Name	Type	Description
IRDY#	I/O	**Initiator Read**y: IRDY# indicates the ICH6's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH6 has valid data present on AD[31:0]. During a read, it indicates the ICH6 is prepared to latch data. IRDY# is an input to the ICH6 when the ICH6 is the target and an output from the ICH6 when the ICH6 is an initiator. IRDY# remains tri-stated by the ICH6 until driven by an initiator.
TRDY#	I/O	**Target Read**y: TRDY# indicates the ICH6's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH6, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH6, as a target is prepared to latch data. TRDY# is an input to the ICH6 when the ICH6 is the initiator and an output from the ICH6 when the ICH6 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH6 until driven by a target.
STOP#	I/O	**Sto**p: STOP# indicates that the ICH6, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH6, as an initiator, to stop the current transaction. STOP# is an output when the ICH6 is a target and an input when the ICH6 is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH6 counts the number of one within the 36 bits plus PAR and the sum is always even. The ICH6 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH6 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH6 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH6 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH6 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH6 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH6 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH6 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

5.2 Intel ICH6-M South Bridge(2)

PCI Interface Signals (Continued)

Name	Type	Description
PERR#	I/O	**Parity Error**: An external PCI device drives PERR# when it receives data that has a parity error. The ICH6 drives PERR# when it detects a parity error. The ICH6 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[0:3]# **REQ[4]#** / GPI[40] **REQ[5]#** / GPI[1] **REQ[6]#** / GPI[0]	I	**PCI Request**s: The ICH6 supports up to 7 masters on the PCI bus. The REQ[4]#, REQ[5]#, and REQ[6]# pins can instead be used as a GPI.
GNT[0:3]# **GNT[4]#** / GPO[48] **GNT[5]#** / GPO[17]# **GNT[6]#** / GPO[16]#	O	**PCI Grant**s: The ICH6 supports up to 7 masters on the PCI bus. The GNT[4]# pin can instead be used as a GPO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[5]#/GPO[17] and GNT[6]#/GPO[17] both have an internal pull-up. **NOTE:** GNT[6] is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak, integrated pull-up resistor on the GNT[6] pin.
PCICLK	I	**PCI Clock**: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6). **NOTE:** PCIRST# is in the VccSus3_3 well.
PLOCK#	I/O	**PCI Lock**: This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH6 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	OD I/O	**System Error**: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH6 has the ability to generate an NMI, SMI#, or interrupt.
PME#	OD I	**PCI Power Management Event**: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH6 may drive PME# active due to an internal wake event. The ICH6 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

Serial ATA Interface Signals

Name	Type	Description
SATA[0]TXP **SATA[0]TXN**	O	**Serial ATA 0 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 0.
SATA[0]RXP **SATA[0]RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0.
SATA[1]TXP **SATA[1]TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1.
SATA[1]RXP **SATA[1]RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1.
SATA[2]TXP **SATA[2]TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2.
SATA[2]RXP **SATA[2]RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2.
SATA[3]TXP **SATA[3]TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3.
SATA[3]RXP **SATA[3]RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3.
SATARBIAS	O	**Serial ATA Resistor Bias:** These are analog connection points for an external resistor to ground.
SATARBIAS#	I	**Serial ATA Resistor Bias Complement:** These are analog connection points for an external resistor to ground.
SATA[0]GP / GPI[26]	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPI[26]. **NOTE:** All SATAxGP pins must be configured with the same function: as either SATAxGP pins or GPI pins.
SATA[1]GP / GPI[29]	I	**Serial ATA 1 General Purpose:** Same function as SATA[0]GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPI[29].
SATA[2]GP / GPI[30]	I	**Serial ATA 2 General Purpose:** Same function as SATA[0]GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPI[30].

5.2 Intel ICH6-M South Bridge(3)

Serial ATA Interface Signals (Continued)

Name	Type	Description
SATA[3]GP / GPI[31]	I	**Serial ATA 3 General Purpose:** Same function as SATA[0]GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPI[31].
SATALED#	OC O	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. **NOTE:** An internal pull-up is enabled only during PLTRST# assertion.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	OD I	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPI[5:2]	OD I	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the *Interrupt Steering* section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPI.
IDEIRQ	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drive.

LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** This signal is driven by the LAN Connect component. The frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** This clock is used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. IT runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller. Runs at 100 MHz. This clock is permitted to stop during S3 (or lower) states.
DMI_CLKP, DMI_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the Direct Media Interface. Runs at 100 MHz.

LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[0]# LDRQ[1]# / GPI[41]	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ[1]# may optionally be used as GPI.

5.2 Intel ICH6-M South Bridge(4)

IDE Interface Signals

Name	Type	Description
DCS1#	O	**IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	**IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DA[2:0]	O	**IDE Device Address:** These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DD[15:0]	I/O	**IDE Device Data:** These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDREQ	I	**IDE Device DMA Request:** This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on this signal.
DDACK#	O	**IDE Device DMA Acknowledge:** This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel ICH6 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
DIOR# / (DWSTB / RDMARDY#)	O	**DIOR# /** **Disk I/O Read (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the ICH6 on the de-assertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#) Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH6 drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH6 de-asserts RDMARDY# to pause burst data transfers.

IDE Interface Signals (Continued)

Name	Type	Description
DIOW# / (DSTOP)	O	**Disk I/O Write (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the de-assertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): ICH6 asserts this signal to terminate a burst.
IORDY / (DRSTB / WDMARDY#)	I	**I/O Channel Ready (PIO)**: This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ICH6 latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	OD I/O	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT#	OD I/O	**SMLink Alert:** Output of the integrated LAN and input to either the integrated ASF or an external management controller in order for the LAN's SMLINK slave to be serviced.

SM Bus Interface Signals

Name	Type	Description
SMBDATA	OD I/O	**SMBus Data:** External pull-up resistor is required.
SMBCLK	OD I/O	**SMBus Clock:** External pull-up resistor is required.
SMBALERT#/ GPI[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

5.2 Intel ICH6-M South Bridge(5)

USB Interface Signals

Name	Type	Description
USBP[0]P, USBP[0]N, USBP[1]P, USBP[1]N	I/O	**Universal Serial Bus Port [1:0] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[2]P, USBP[2]N, USBP[3]P, USBP[3]N	I/O	**Universal Serial Bus Port [3:2] Differentia**l: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[4]P, USBP[4]N, USBP[5]P, USBP[5]N	I/O	**Universal Serial Bus Port [5:4] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[6]P, USBP[6]N, USBP[7]P, USBP[7]N	I/O	**Universal Serial Bus Port [7:6] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
OC[3:0]# **OC[4]#** / GPI[9] **OC[5]#** / GPI[10] **OC[6]#** / GPI[14] **OC[7]#** / GPI[15]	I	**Overcurrent Indicator**s: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIs. **NOTE:** OC[7:0]# are not 5 V tolerant.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Cloc**k: This signal is the serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data I**n: This signal transfers data from the EEPROM to the Intel ® ICH6. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Ou**t: This signal transfers data from the ICH6 to the EEPROM.
EE_CS	O	**EEPROM Chip Selec**t: This is the chip select signal to the EEPROM.

Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.5 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device that in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. **2.** In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
TP[0]	I	**Test Point 0:** This signal must have an external pull-up to VccSus3_3.
TP[1]	O	**Test Point 1:** Route signal to a test point.
TP[2]	O	**Test Point 2:** Route signal to a test point.
TP[3]	I	**Test Point 3:** Route signal to a test point.
TP[4]	O	**Test Point 4:** Route signal to a test point.

5.2 Intel ICH6-M South Bridge(6)

Power Management Interface Signals

Name	Type	Description
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Rese**t: This pin forces an internal reset after being debounced. The ICH6 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller will be put into reset. This signal must be asserted for at least 10 ms after the resume well power (VccSus3_3 and VccSus1_5) is valid. When de-asserted, this signal is an indication that the resume well power is stable. **NOTE:** LAN_RST# must de-assert at some point to complete ICH6 power up sequencing.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wakeup.
MCH_SYNC#	I	**MCH SYNC:** This input is internally ANDed with the PWROK input. Connected to the ICH_SYNC# output of (G)MCH.
SUS_STAT# / LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH6 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
SUSCLK	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input.

Power Management Interface Signals (Continued)

Name	Type	Description
PLTRST#	O	**Platform Reset:** The ICH6 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, IDE, TPM, etc.). The ICH6 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH6 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH6 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	**Thermal Trip**: When low, this signal indicates that a thermal trip from the processor occurred, and the ICH6 will immediately transition to a S5 state. The ICH6 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control**: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power in order to use the ICH6's DRAM power-cycling feature. Refer to Chapter 5.14.10.2 for details.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH6 that core power has been stable for at least 99 ms and PCICLK has been stable for at least 1 mS. An exception to this rule is if the system is in S3 HOT , in which PWROK may or may notstay asserted even though PCICLK may be inactive. PWROK can be driven asynchronously. When PWROK is negated, the ICH6 asserts PLTRST#. **NOTE:** PWROK must de-assert for a minimum of three RTC clock periods in order for the ICH6 to fully reset the power and properly generate the PLTRST# output

5.2 Intel ICH6-M South Bridge(7)

Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUSLP#	O	**Processor Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel® ICH6 can optionally assert the CPUSLP# signal when going to the S1 state, and will always assert it when going to C3 or C4.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH6 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset ConfigurationRegisters:Offset 31FFh: bit 1). If FERR# is asserted, the ICH6 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH6 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Configuration Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the ICH6 for 16 PCI clocks to reset the processor. ICH6 can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH6 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.

Processor Interface Signals (Continued)

Name	Type	Description
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH6 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH6 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH6 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH6's other sources of INIT#. When the ICH6 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH6 will ignore RCIN# assertion during transitions to the S1, S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD / GPO[49]	OD O	**Processor Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the processor power is valid. This is an open- drain output signal (external pull-up resistor required) that represents a logical AND of the ICH6's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPO.

5.2 Intel ICH6-M South Bridge(8)

General Purpose I/O Signals 1,2

Name	Type	Tolerance	Power Well	Description
GPO[49]	OD O	V_CPU_IO	`Core	This signal is fixed as output only and can instead be used as CPUPWRGD.
GPO[48]	O	3.3 V	Core	This signal is fixed as output only and can instead be used as GNT4#.
GPIO[47:42]	N/A	N/A	N/A	This signal is not implemented.
GPI[41]	I	3.3 V	Core	This signal is fixed as input only and can be used instead as LDRQ1#.
GPI[40]	I	5 V	Core	This signal is fixed as input only and can be used instead as REQ4#.
GPIO[39:35]	N/A	N/A	N/A	This signal is not implemented.
GPIO[34:33]	I/O	3.3 V	Core	This signal can be input or output and is unmultiplexed
GPIO[32]	I/O	3.3 V	Core	This signal can be input or output.
GPI[31]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[3]GP.
GPI[30]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[2]GP.
GPI[29]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[1]GP.
GPIO[28:27]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed.
GPI[26]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[0]GP.
GPIO[25]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed. It is a strap for internal Vcc2_5 regulator. See Section 2.22.1.
GPIO[24]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed.
GPO[23]	O	3.3 V	Core	This signal is fixed as output only.
GPIO[22]	N/A	N/A	N/A	This signal is not Implemented
GPO[21]	O	3.3 V	Core	This signal is fixed as output only and is unmultiplexed
GPO[20]	O	3.3 V	Core	This signal is fixed as output only.
GPO[19]	O	3.3 V	Core	This signal is fixed as output only. **NOTE:** GPO[19] may be programmed to blink (controllable by GPO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 19)).

General Purpose I/O Signals 1,2 (Continued)

Name	Type	Tolerance	Power Well	Description
GPO[18]	O	3.3 V	Core	This signal is fixed as output only. **NOTE:** GPO[18] will blink by default immediately after reset (controllable by GPO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 18)).
GPO[17]	O	3.3 V	Core	This signal is fixed as output only and can be used instead as PCI GNT[5]#.
GPO[16]	O	3.3 V	Core	This signal is fixed as output only and can be used instead as PCI GNT[6]#.
GPI[15:14]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as OC[7:6]#
GPI[13]3	I	3.3 V	Resume	This signal is fixed as input only and is unmultiplexed.
GPI[12]3	I	3.3 V	Core	This signal is fixed as input only and is unmultiplexed.
GPI[11]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as SMBALERT#.
GPI[10:9]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as OC[5:4]#.
GPI[8]3	I	3.3 V	Resume	This signal is fixed as input only and is unmultiplexed.
GPI[7]3	I	3.3 V	Core	This signal is fixed as input only and is unmultiplexed.
GPI[6]3	I	3.3 V	Core	This signal is fixed as input only.
GPI[5:2]3	I	5 V	Core	This signal is fixed as input only and can be used instead as PIRQ[H:E]#.
GPI[1:0]3	I	5 V	Core	This signal is fixed as input only and can be used instead as PCI REQ[6:5]#.

NOTES:

1.All inputs are sticky. The status bit remains set as long as the input was asserted for two clocks.GPIs are sampled on PCI clocks in S0/S1. GPIs are sampled on RTC clocks in S3/S4/S5.

2.Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH6 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH6 driving a pin to a logic 1 to another device that is powered down.

3.GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.

5.2 Intel ICH6-M South Bridge(9)

AC '97/Intel ® High Definition Audio Link Signals

Name	Type	Description
ACZ_RST#	O	**AC '97/Intel ® High Definition Audio Reset:** Master hardware reset to external codec(s).
ACZ_SYNC	O	**AC '97/Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	**AC '97 Bit Clock Input:** 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note below). **Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel® High Definition Audio controller (the Intel ICH6). Thissignal has an integrated pull-down resistor so that ACZ_BIT_CLK does not float when an Intel High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.
ACZ_SDOUT	O	**AC '97/Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak integrated pull-down resistor on the ACZ_SDOUT pin.
ACZ_SDIN[2:0]	I	**AC '97/Intel High Definition Audio Serial Data In [2:0**]: Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel High Definition Audio. These signals have integrated pull-down resistors, which are always enabled.

NOTES:

1. Some signals have integrated pull-ups or pull-downs. Consult table in Section 3.1 for details.
2. Intel High Definition Audio mode is selected through D30:F1:40h, bit 0: AZ/AC97#. This bit selects the mode of the shared Intel High Definition Audio/AC '97 signals. When set to 0 AC '97 mode is selected. When set to 1 Intel High Definition Audio mode is selected. The bit defaults to 0 (AC '97 mode).

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** These signals are multiplexed with the LPC address signals.
FWH[4] / LFRAME#	O	**Firmware Hub Signals.** This signal is multiplexed with the LPC LFRAME# signal.

Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for core well I/O buffers (22 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for core well logic, group A (52 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for core well logic, group B (45 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc2_5	2.5V supply for internal logic (2 pins). This power may be shut off in S3, S4, S5 or G3 states. **NOTE:** This voltage may be generated internally (see Section 2.22.1 for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF	Reference for 5 V tolerance on core well inputs (2 pins). This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for resume well I/O buffers (20 pins). This power is not expected to be shut off unless the system is unplugged.
VccSus1_5	1.5 V supply for resume well logic (3 pin). This power is not expected to be shut off unless the system is unplugged. This voltage may be generated internally (see Section 2.22.1 for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF_Sus	Reference for 5 V tolerance on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well (1 pin). This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH6-based platform can be done by using a jumper on RTCRST# or GPI.
VccUSBPLL	1.5 V supply for core well logic (1 pin). This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. This signal must be powered even if USB not used.
VccDMIPLL	1.5 V supply for core well logic (1 pins). This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccSATAPLL	1.5 V supply for core well logic (1 pins). This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. This signal must be powered even if SATA not used.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor interface signals listed in Table 2-13.
Vss	Grounds (172 pins).

5.2 Intel ICH6-M South Bridge(10)

Functional Strap Definitions 1

Signal	Usage	When Sampled	Description
GNT[6]#/ GPO[16]	Top-Block Swa Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (ICH6 inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Configuration Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT6# being pulled down.
LINKALERT #	Reserved		This signal requires an external pull-up resistor.
SPKR	No Reboot	Rising Edge ofPWROK	The signal has a weak internal pull-down. If the signal is.sampled high, this indicates that the system is strapped to.the “No Reboot” mode (ICH6 will disable the TCO Timer. system reboot feature). The status of this strap is readable. via the NO REBOOT bit (Chipset Configuration. Registers:Offset 3410h:bit 5).
INTVRMEN	IntegratedVccSu 1_5VRM Enable/Disable	Always	This signal enables integrated VccSus1_5 VRM when.sampled high.
GPIO[25]	Integrated Vcc2_5 VRM Enable/ Disable	Rising Edge of RSMRST#	This signal enables integrated Vcc2_5 VRM when sampled low. This signal has a weak internal pull-up during RSMRST# and is disabled within 100 ms after RSMRST# de-asserts.
EE_CS	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
GNT[5]#/ GPO[17]	Boot BIOS Destination Selection	Rising Edge of PWROK	This signal has a weak internal pull-up. Allows for select memory ranges to be forwarded out the PCI Interface as opposed to the Firmware Hub. When sampled high, destination is LPC. Also controllable via Boot BIOS Destination bit (Chipset Configuration Registers:Offset 3410h:bit 3). **NOTE:** This functionality intended for debug/testing only.

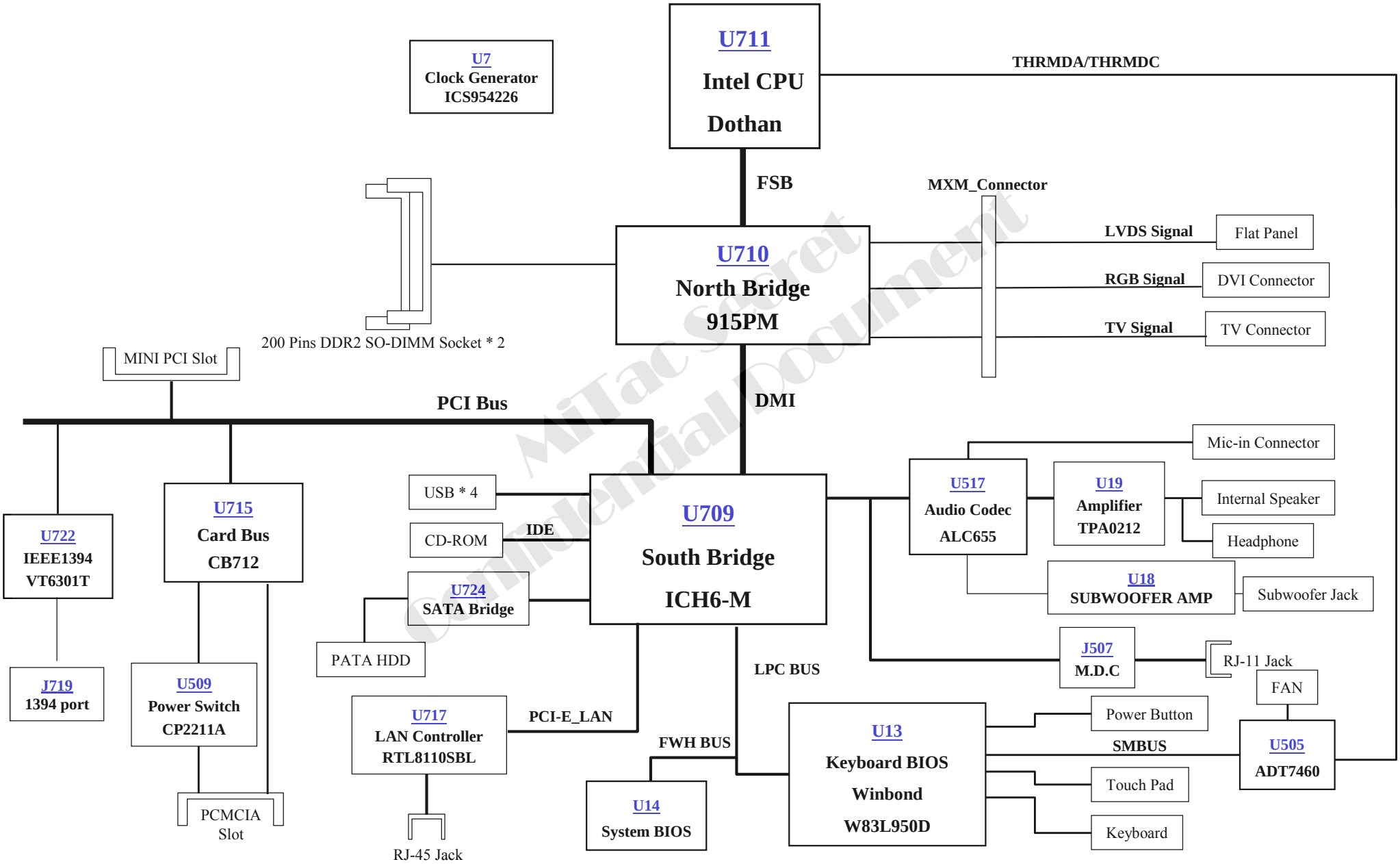
Functional Strap Definitions 1 (Continued)

Signal	Usage	When Sampled	Description
EE_DOUT	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
ACZ_SDOUT	XOR Chain Entrance / PCI Express* Port Configu-ration bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP[3] pulled low at rising edge of PWROK. See Chapter 24 for XOR Chain functionality information. When TP[3] not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Configuration Registers:Offset 224h). See Section 7.1.30 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Por Configu-ration bit 0	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Configuration Registers: Off set 224h). See Section 7.1.30 for details.
TP[1]	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
SATALED#	Reserved		This signal has a weak internal pull-up enabled only when PLTRST# is asserted. **NOTE:** This signal should not be pulled low.
REQ[4:1]#	XOR Chain Selection	Rising Edge of PWROK	See Chapter 24 for functionality information.
TP[3]	XOR Chain Entrance	Rising Edge of PWROK	See Chapter 24 for functionality information. This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low unless using XOR Chain testing.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

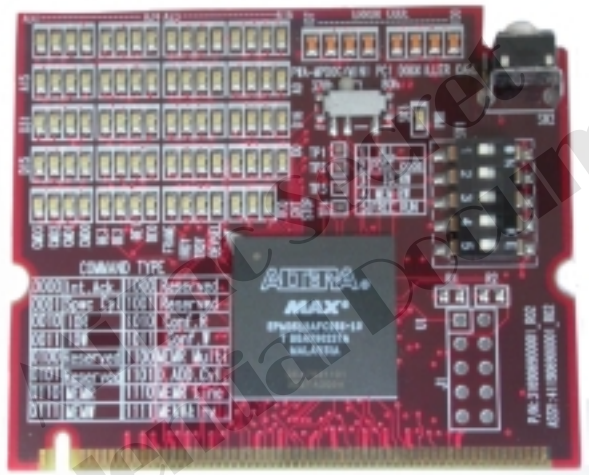
Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port-80H by the debug card plug at MINI PCI slot.

7.2 Maintenance Diagnostics

7.2.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-MPDOG/MINI PCI DOGKILLER CARD
Note: Order it from MIC/TSSC

7.3 Error Codes-1

Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
10h	Some Type of Lone Reset
11h	Turn off FAST A20 for Post
12h	Signal Power On Reset
13h	Initialize the Chipset
14h	Search for ISA Bus VGA Adapter
15h	Reset Counter / Timer 1
16h	User Register Config through CMOS
17h	Size Memory
18h	Dispatch to RAM Test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize Video Adapter(s)
1Ch	Initialize Video (6845Regs)
1Dh	Initialize Color Adapter
1Eh	Initialize Monochrome Adapter
1Fh	Test 8237A Page Registers

Code	POST Routine Description
20h	Test Keyboard
21h	Test Keyboard Controller
22h	Check if CMOS RAM valid
23h	Test Battery Fail & CMOS X-SUM
24h	Test the DMA Controller
25h	Initialize 8237A Controller
26h	Initialize Int Vectors
27h	RAM Quick Sizing
28h	Protected Mode Entered Safely
29h	RAM Test Completed
2Ah	Protected Mode Exit Successful
2Bh	Setup Shadow
2Ch	Going to Initialize Video
2Dh	Search for Monochrome Adapter
2Eh	Search for Color Adapter
2Fh	Sign on Messages Displayed

7.3 Error Codes-2

Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
30h	Special Init of Keyboard Controller
31h	Test if Keyboard Present
32h	Test Keyboard Interrupt
33h	Test Keyboard Command Byte
34h	Test, Blank and Count all RAM
35h	Protected Mode Entered Safely(2)
36h	RAM Test Complete
37h	Protected Mode Exit Successful
38h	Update Output Port
39h	Setup Cache Controller
3Ah	Test if 18.2Hz Periodic Working
3Bh	Test for RTC ticking
3Ch	Initialize the Hardware Vectors
3Dh	Search and Init the Mouse
3Eh	Update NUMLOCK status
3Fh	Special Init of COMM and LPT Ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the Floppies
42h	Initialize the Hard Disk
43h	Initialize Option ROMs
44h	OEM's Init of Power Management
45h	Update NUMLOCK Status
46h	Test for Coprocessor Installed
47h	OEM functions before Boot
48h	Dispatch to Operate System Boot
49h	Jump into Bootstrap Code

8. Trouble Shooting

- 8.1 No Power(*1)
- 8.2 No Display(*2)
- 8.3 VGA Controller Test Error LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Drive Test Error
- 8.8 CD-ROM Drive Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Test Error
- 8.11 LAN Test Error
- 8.12 PC Card Socket Test Error

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

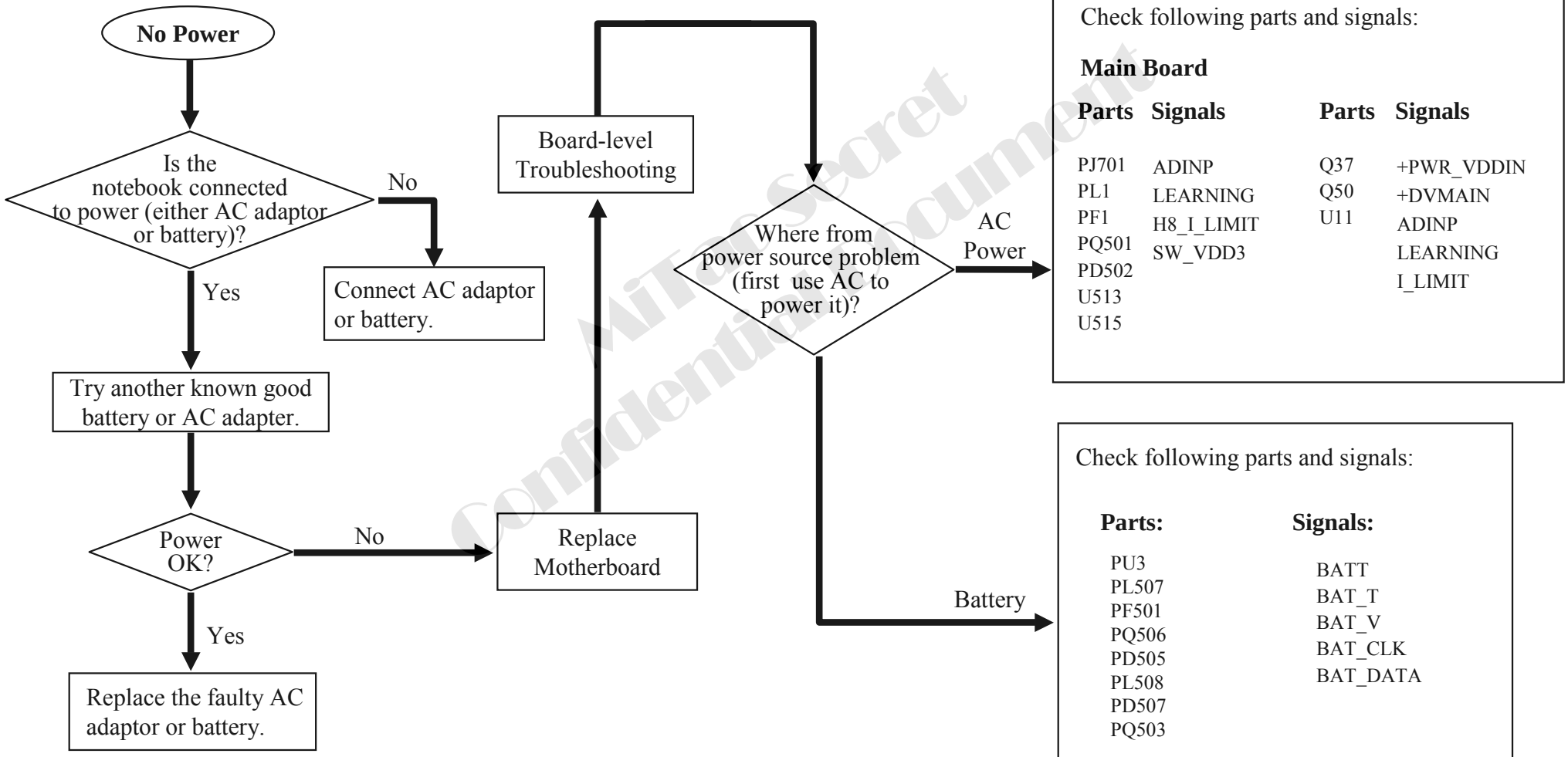
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8.1 No Power-1

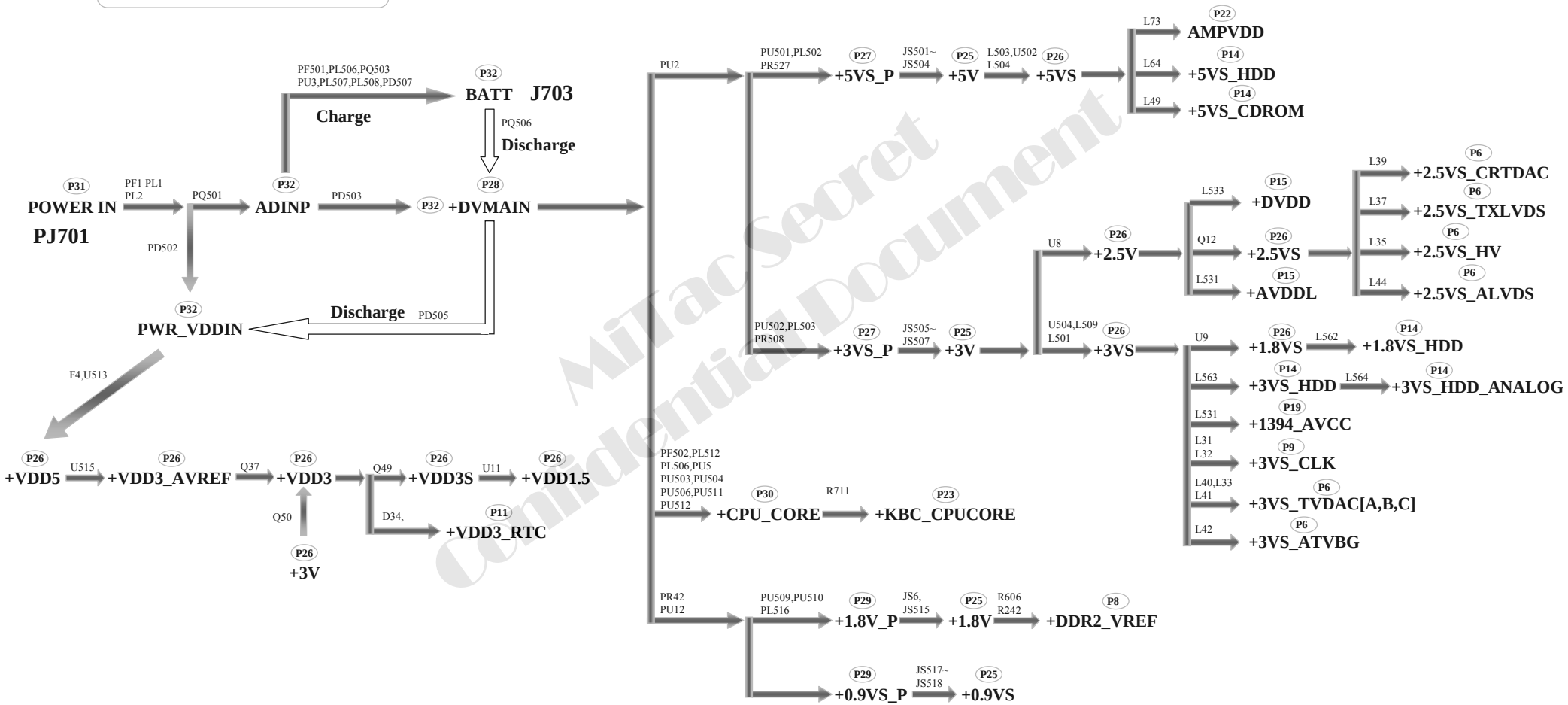
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-2

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

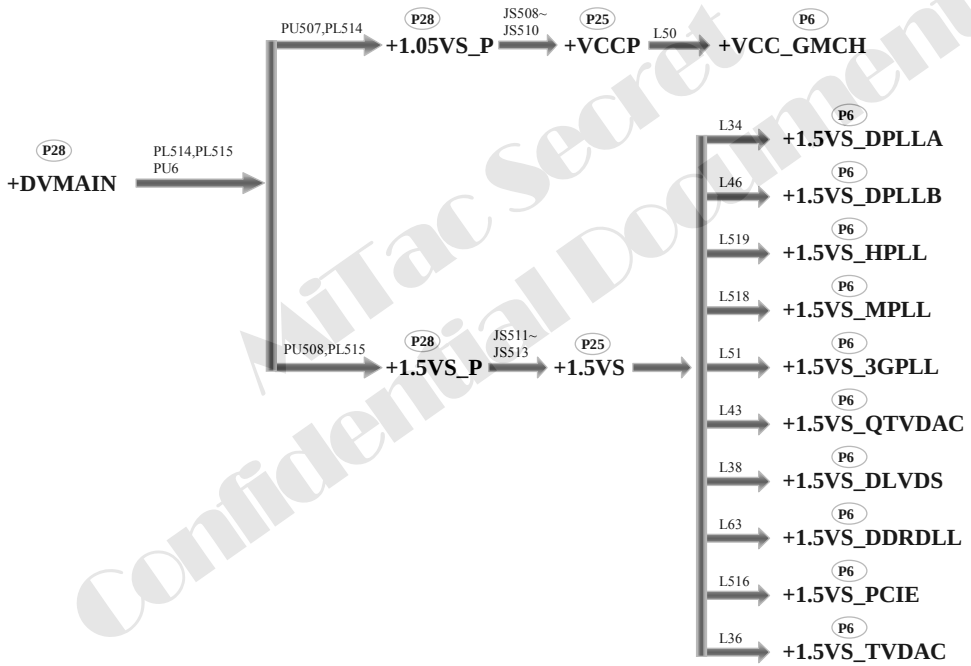
Main Voltage Map



8.1 No Power-3

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map

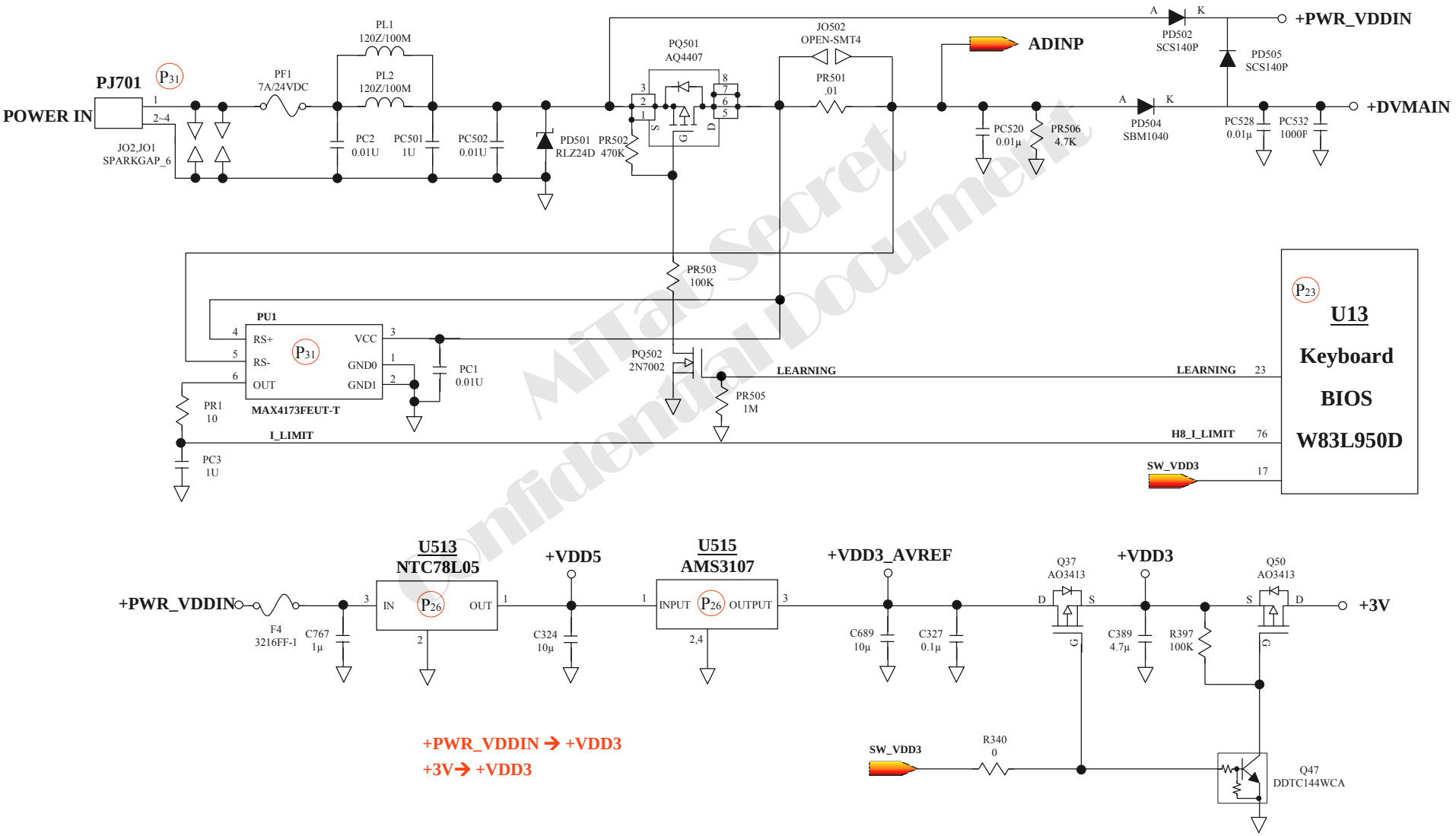


NOTE :

P25 : Page 25 on M/B Board circuit diagram.

8.1 No Power-4

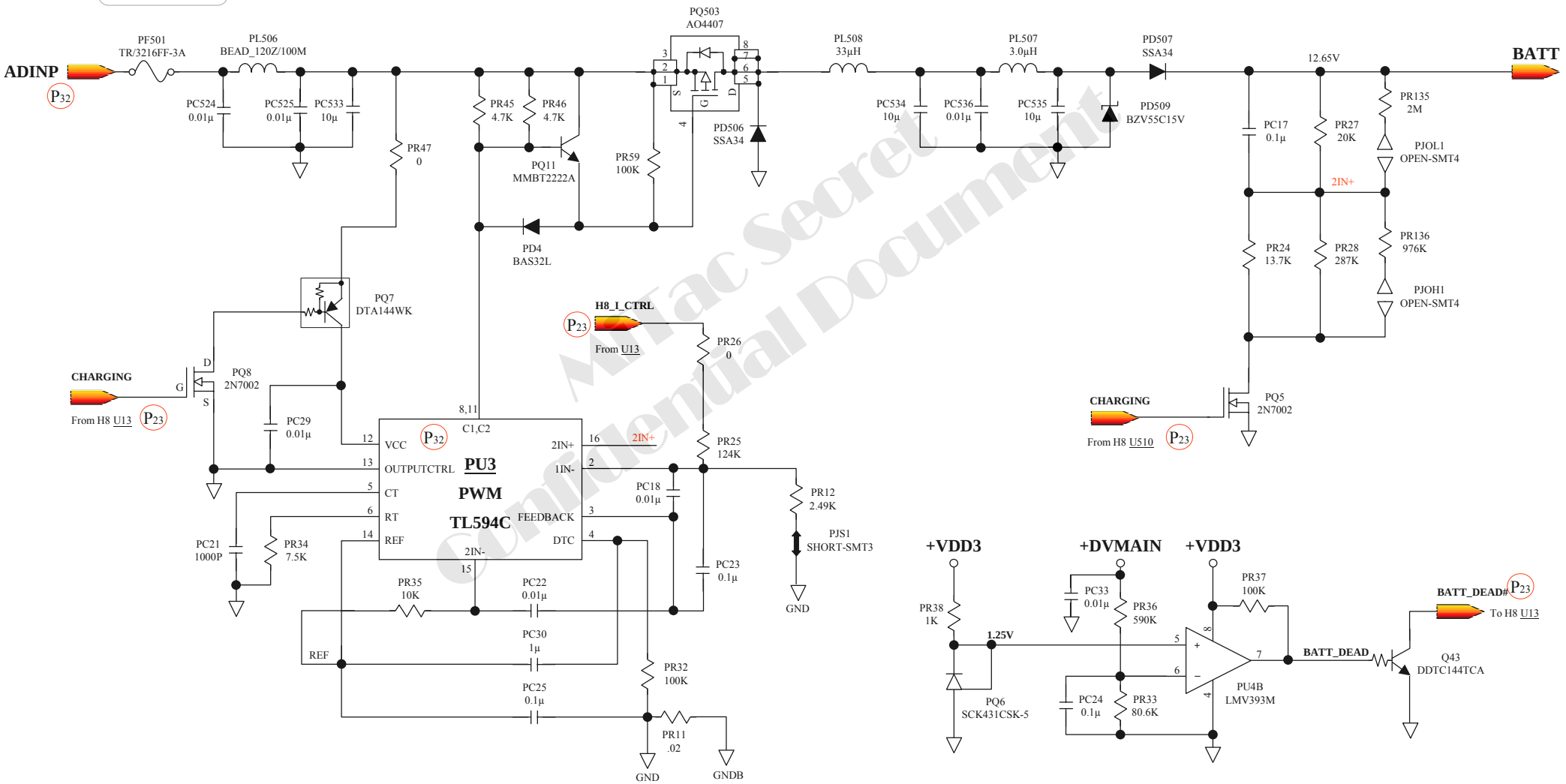
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-5

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

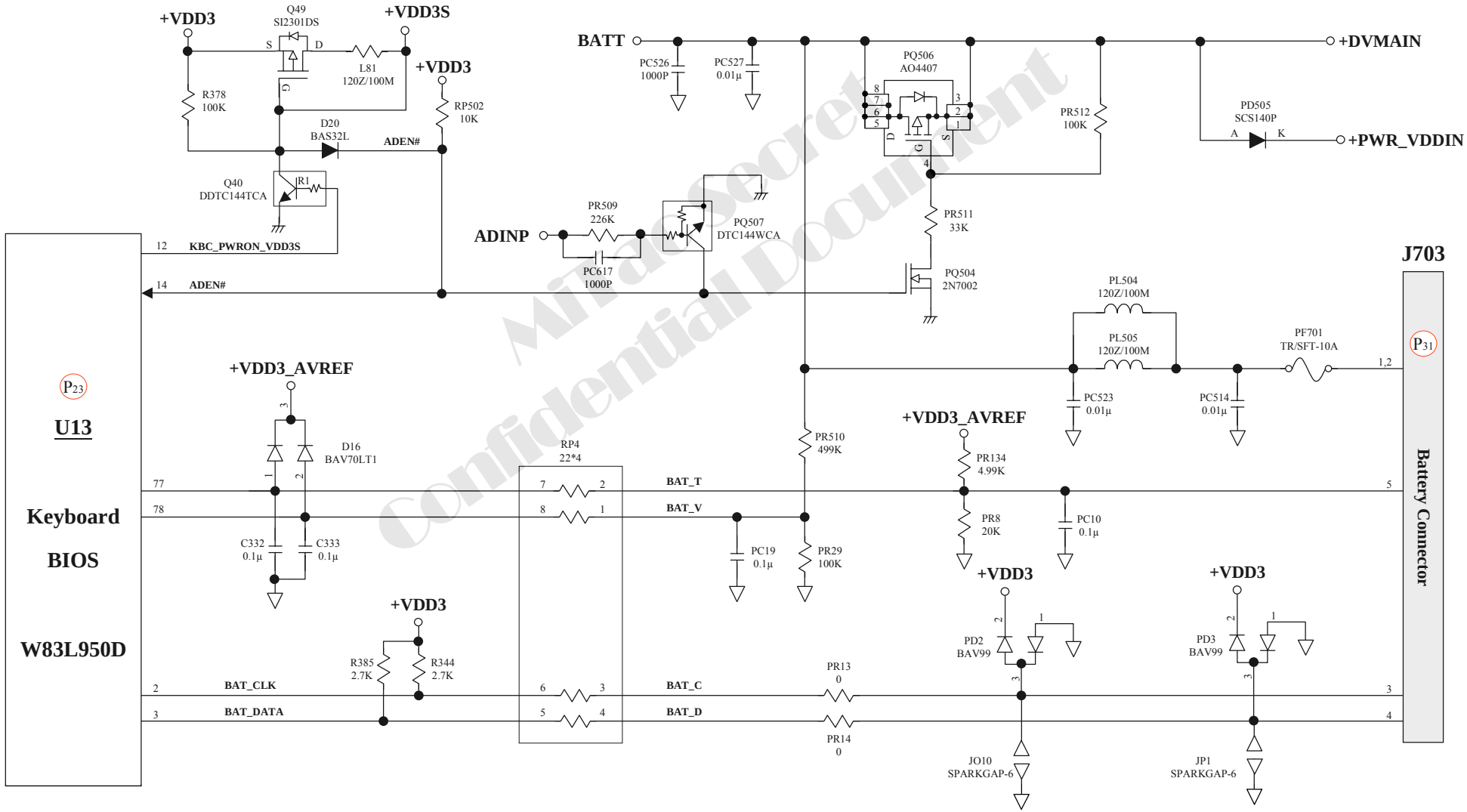
Charge



8.1 No Power-6

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

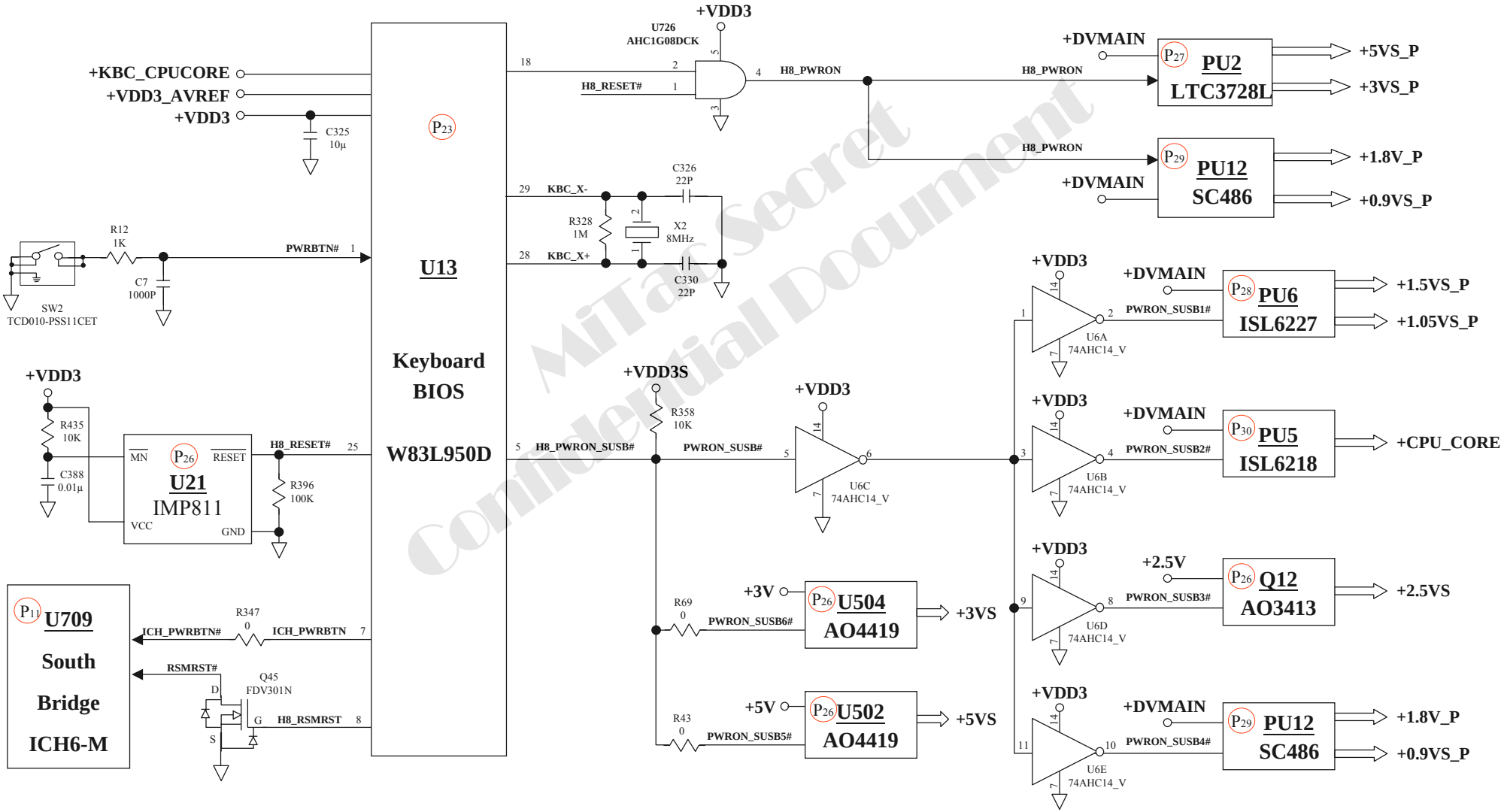
Discharge



8.1 No Power-7

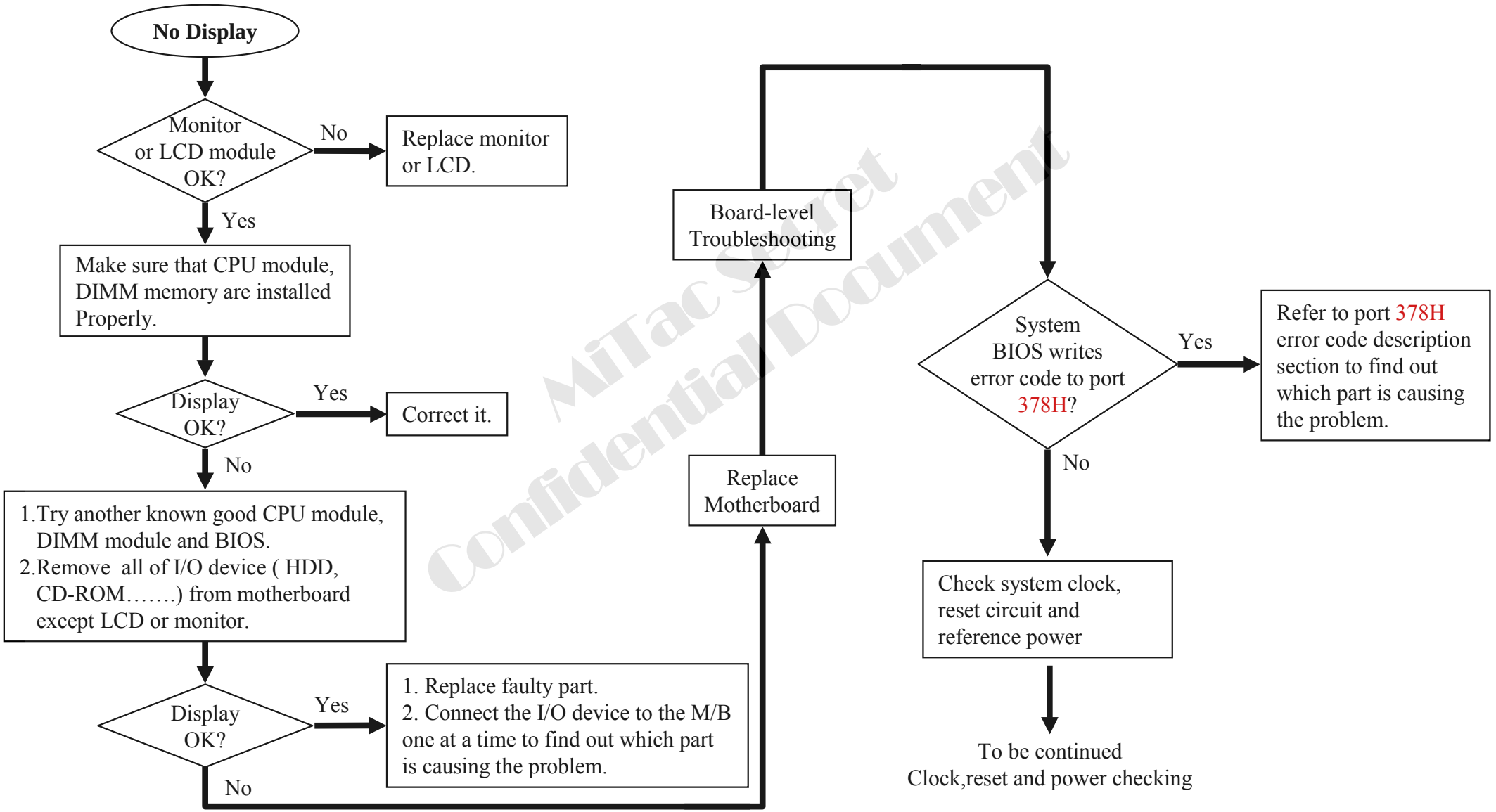
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Power Controller



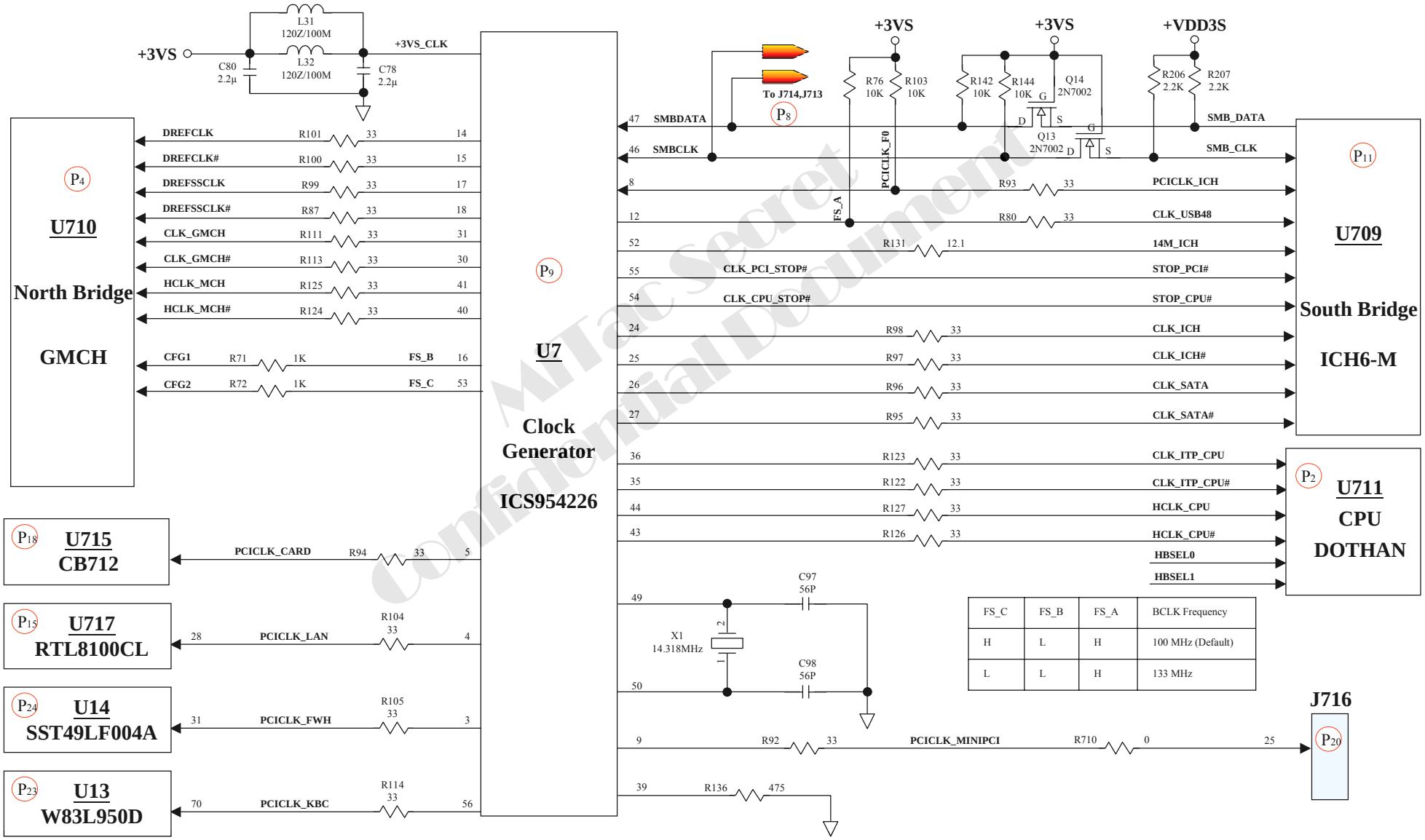
8.2 No Display-1

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



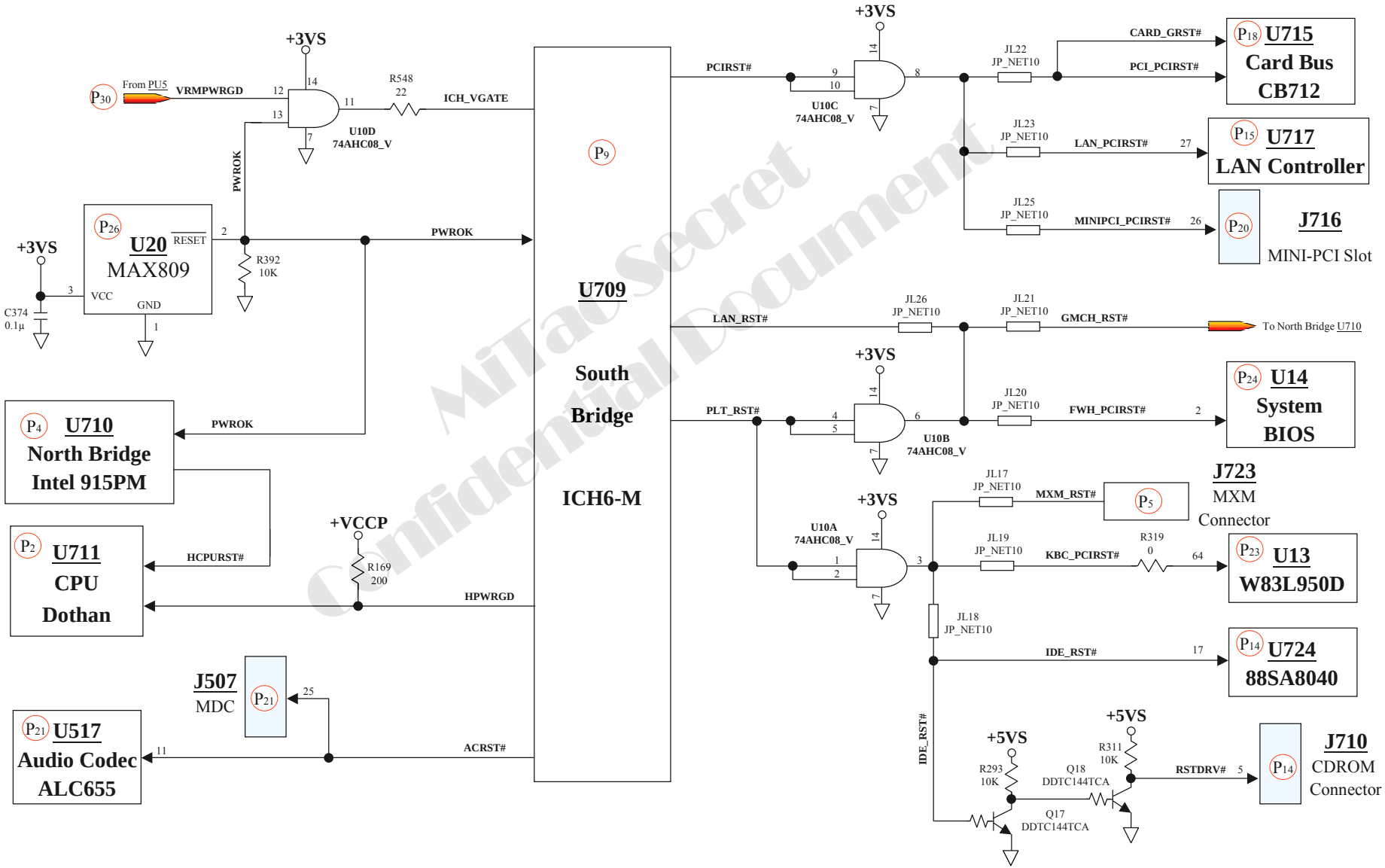
8.2 No Display-2

****** System Clock Check ******



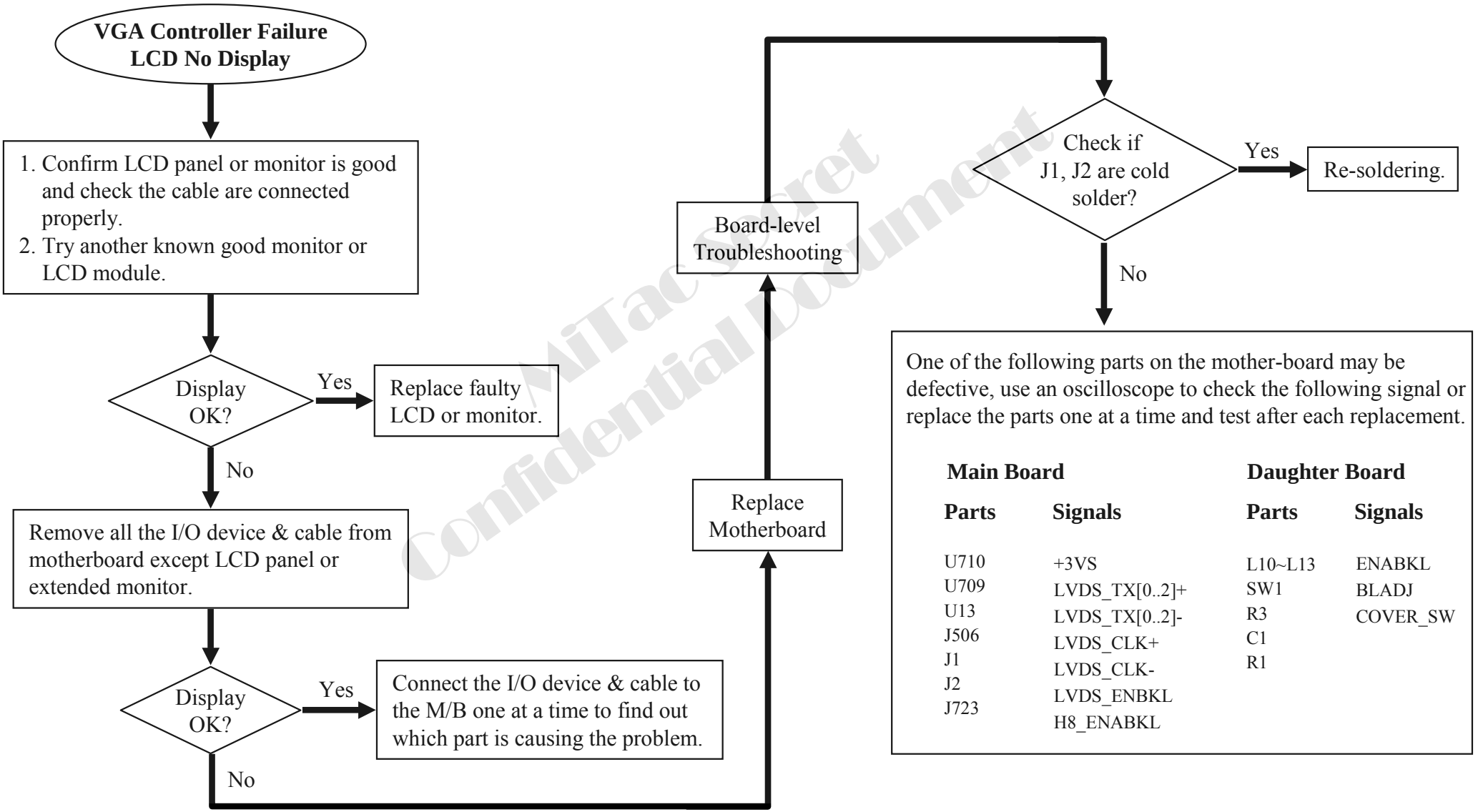
8.2 No Display-3

****** Power Good & Reset Circuit Check ******



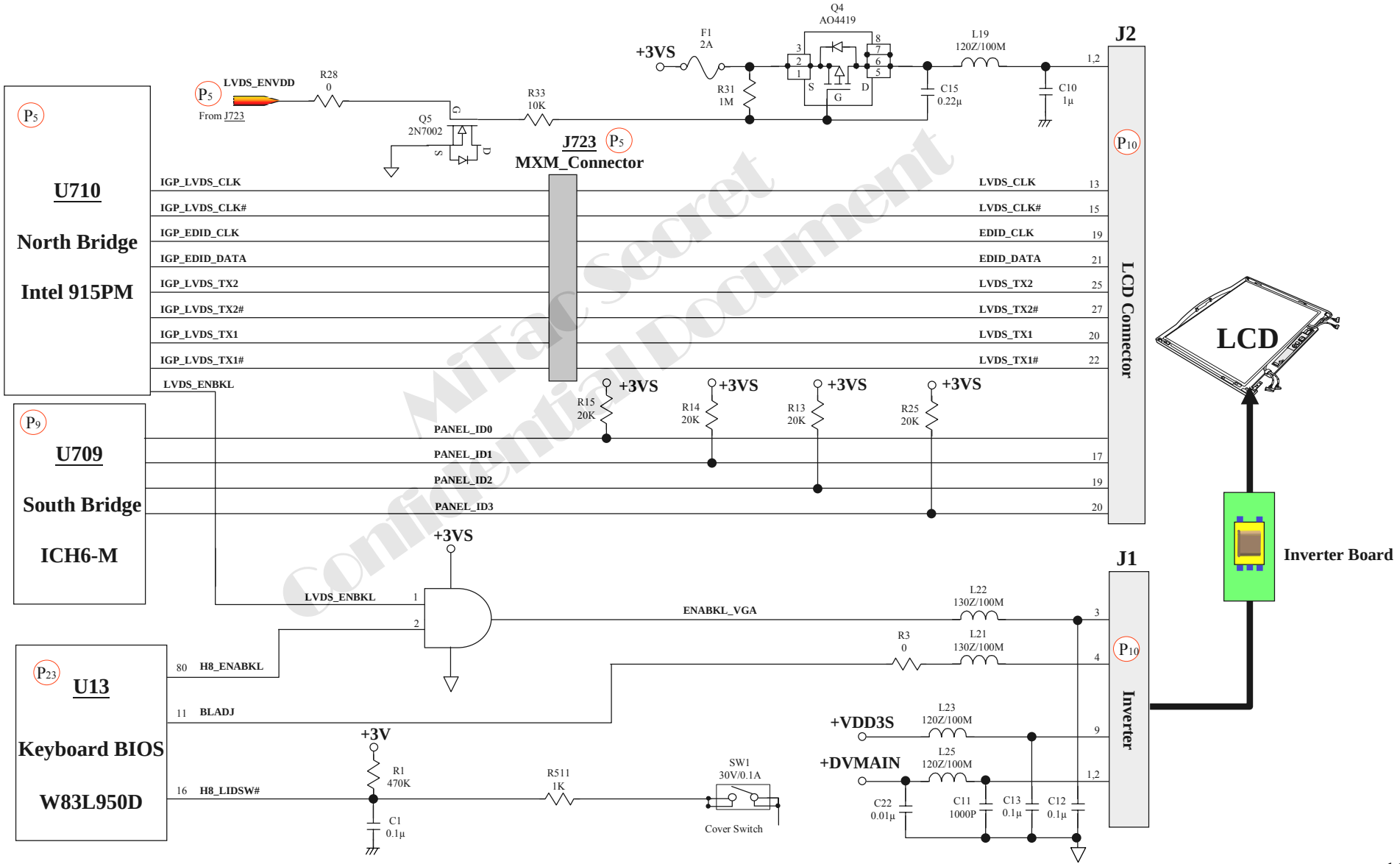
8.3 VGA Controller Test Error LCD No Display-1

There is no display or picture abnormal on LCD although power-on-self-test is passed.



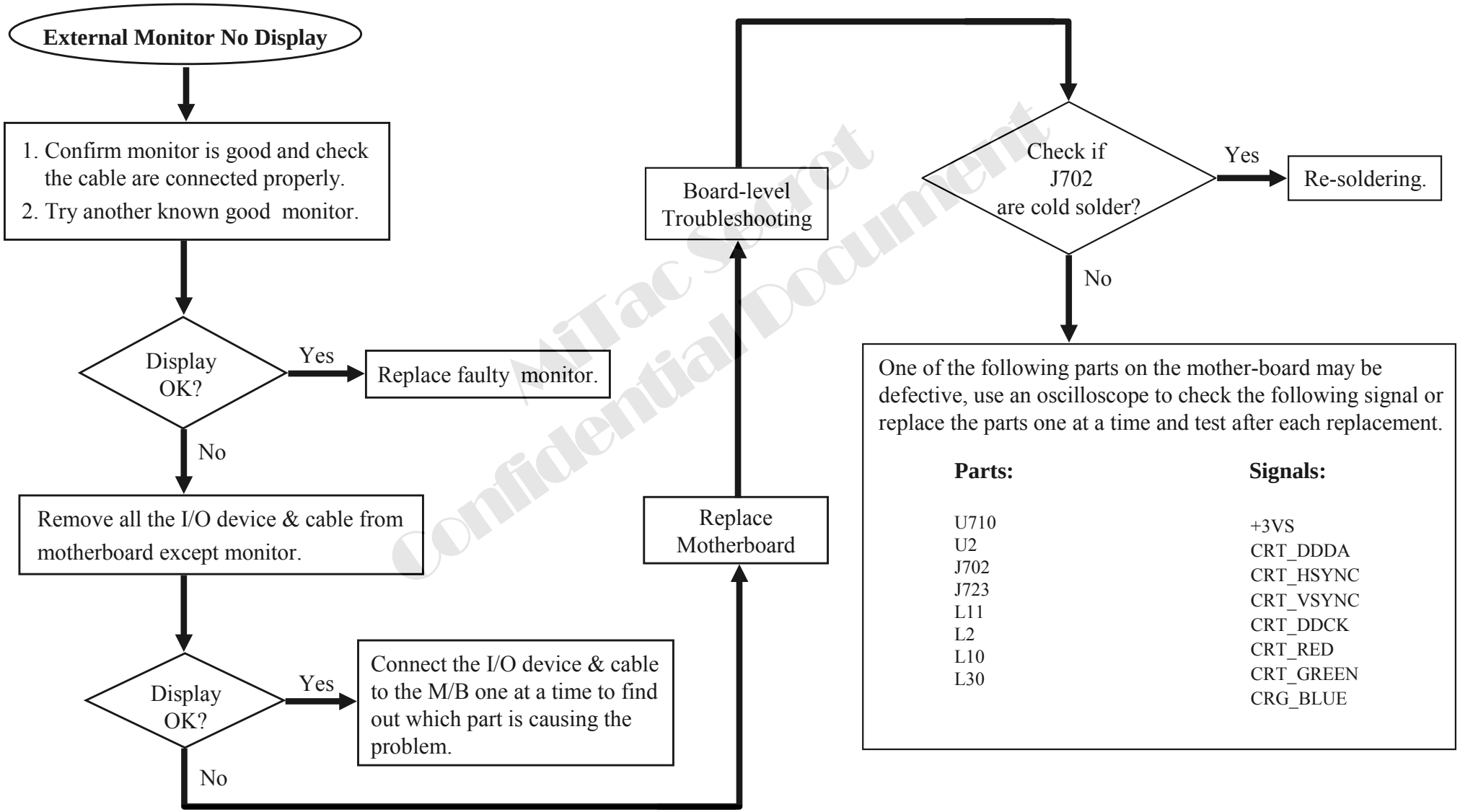
8.3 VGA Controller Test Error LCD No Display-2

There is no display or picture abnormal on LCD although power-on-self-test is passed.



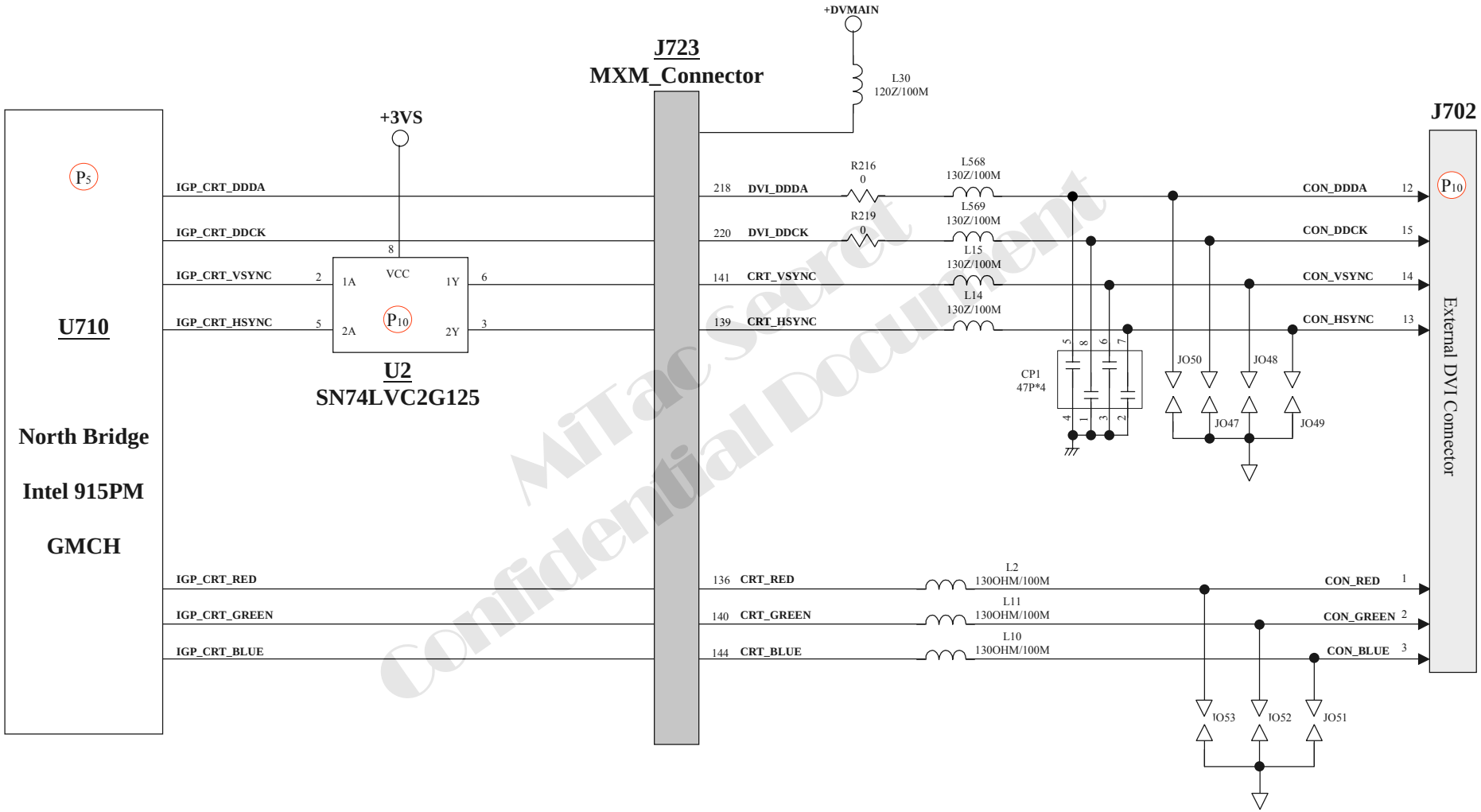
8.4 External Monitor No Display-1

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



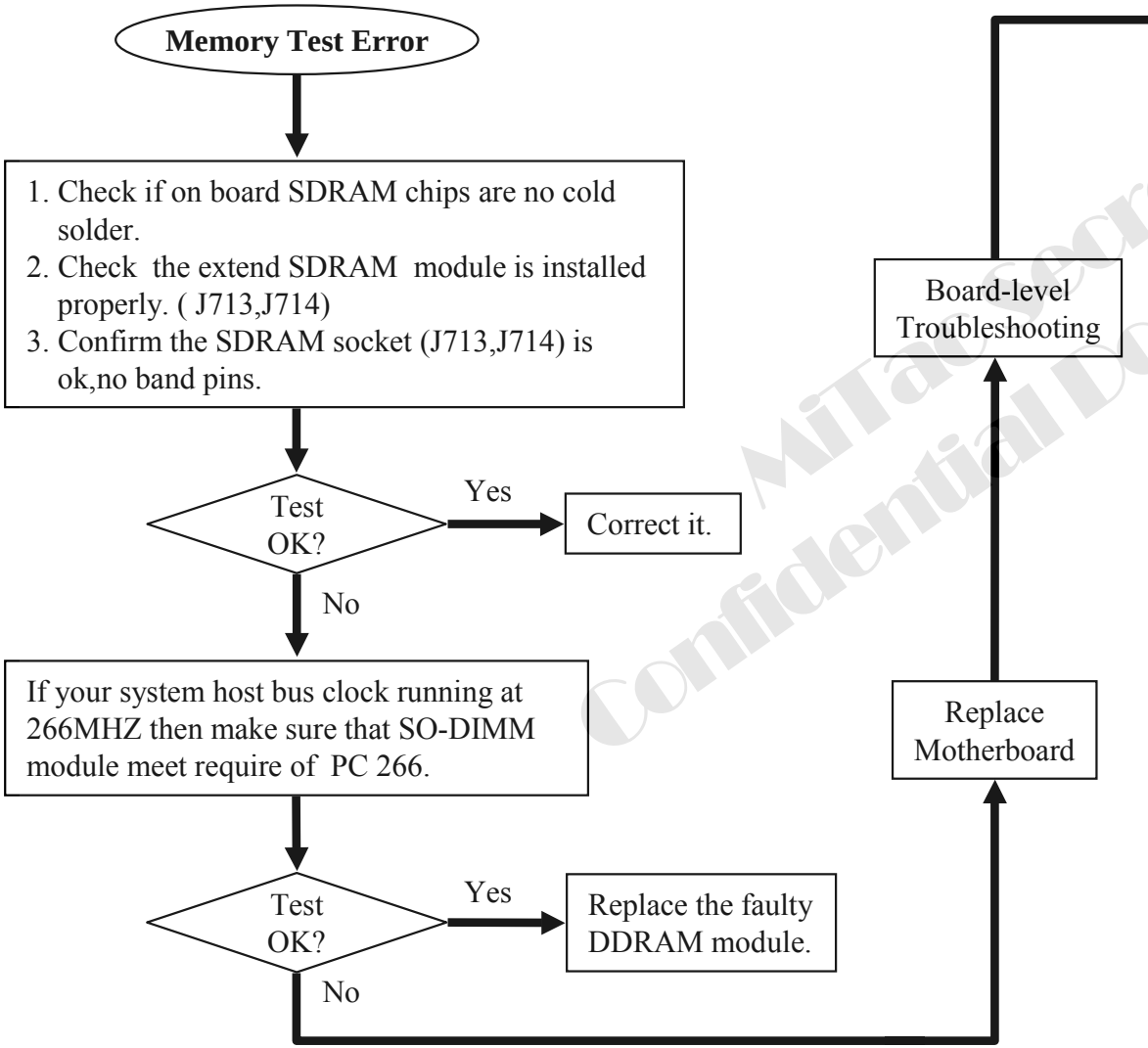
8.4 External Monitor No Display-2

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error-1

Extend DDRAM is failure or system hangs up.

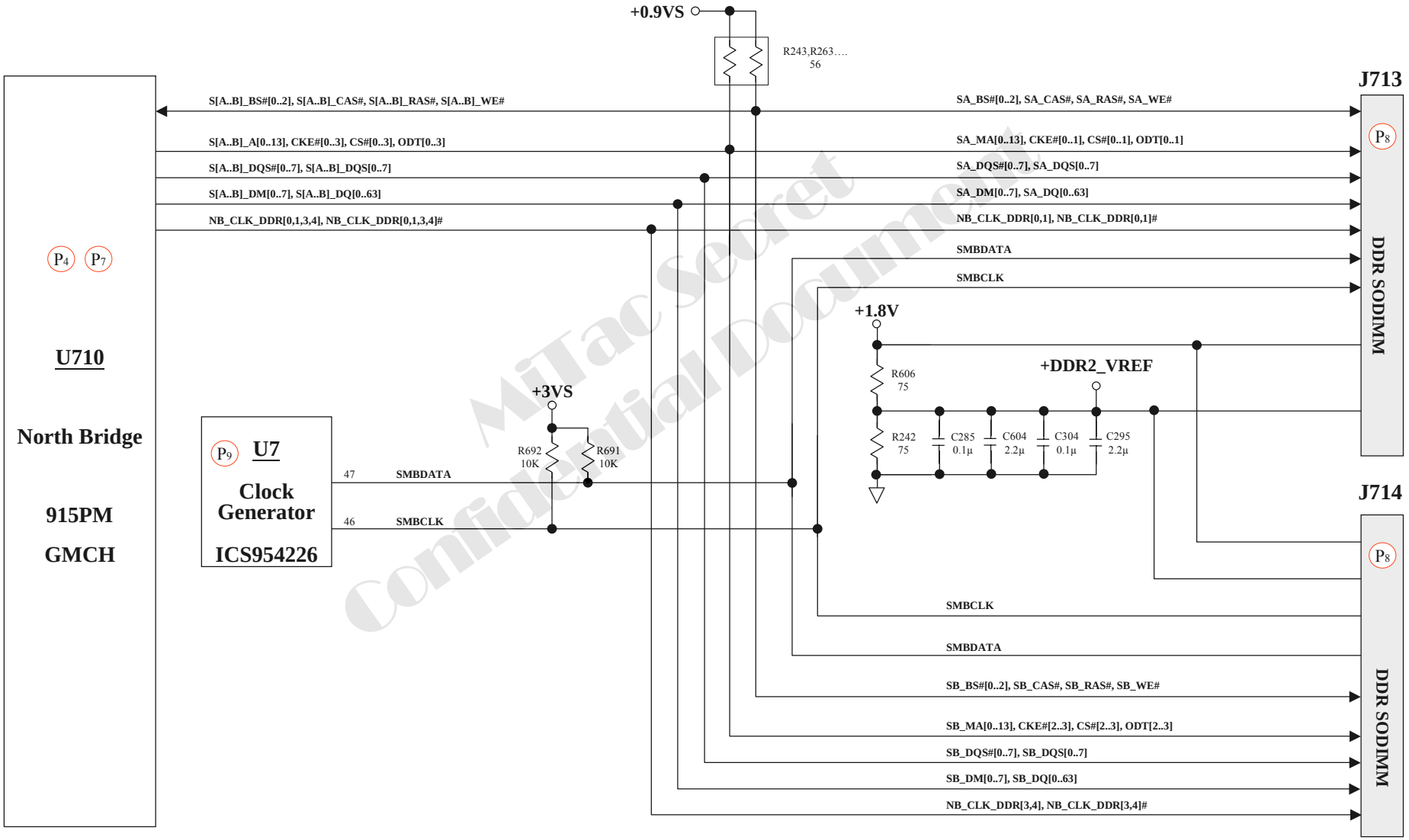


One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U710	+1.8V	SMBDATA
U7	+3VS	SMBCLK
J713	S[A..B]_MA[0..13]	NB_CLK _DDR[0,1,3,4]
J714	CKE#[0..3]	NB_CLK _DDR[0,1,3,4]#
R691	CS#[0..3]	
R692	ODT[0..3]	
R606	S[A..B]_BS#[0..2]	
R242	S[A..B]_CAS#	
C285	S[A..B]_RAS#	
C604	S[A..B]_WE#	
	S[A..B]_DQS#[0..7]	
	S[A..B]_DQS[0..7]	
	S[A..B]_DM[0..7]	
	S[A..B]_DQ[0..63]	

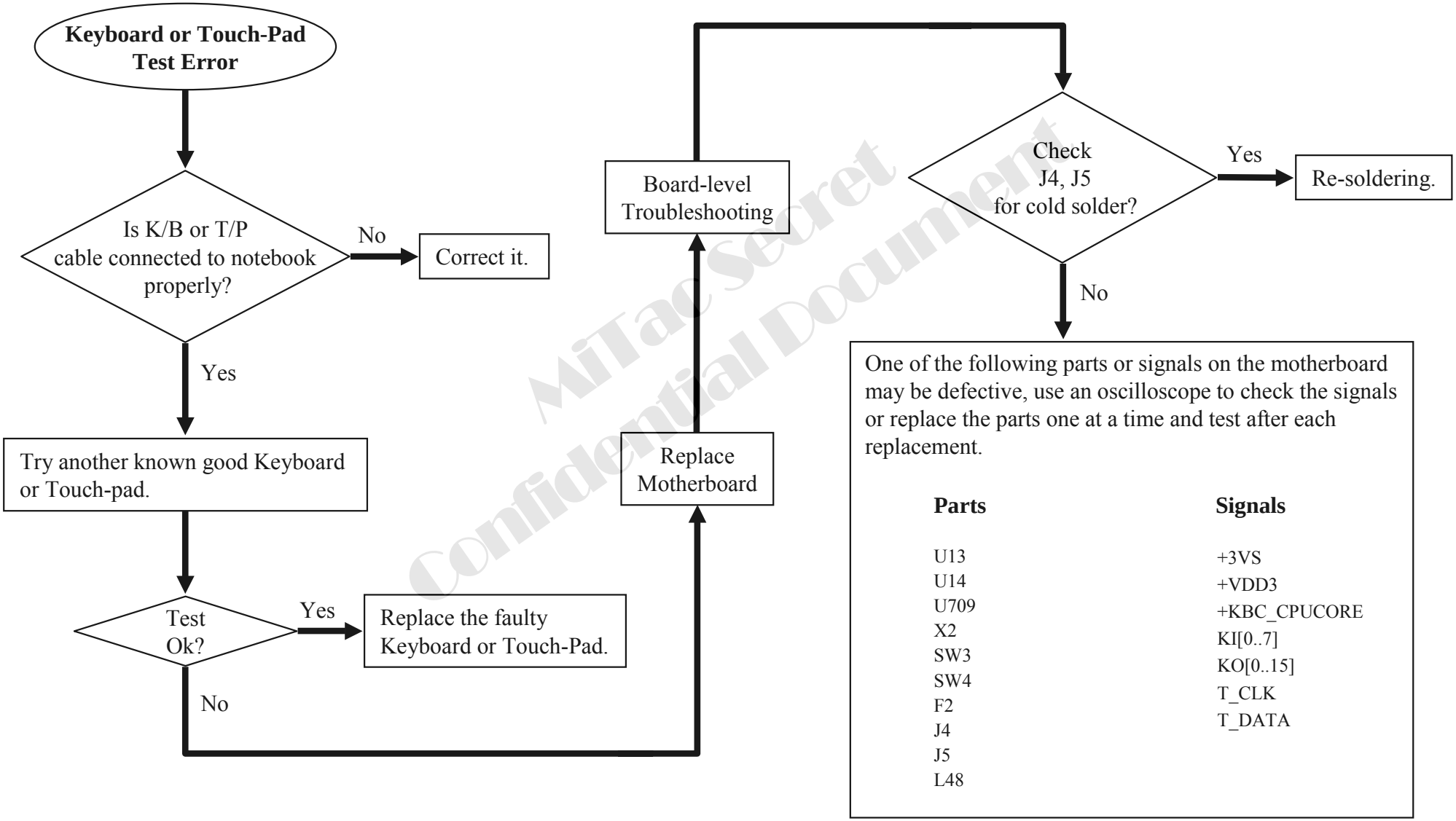
8.5 Memory Test Error-2

Extend DDRAM is failure or system hangs up.



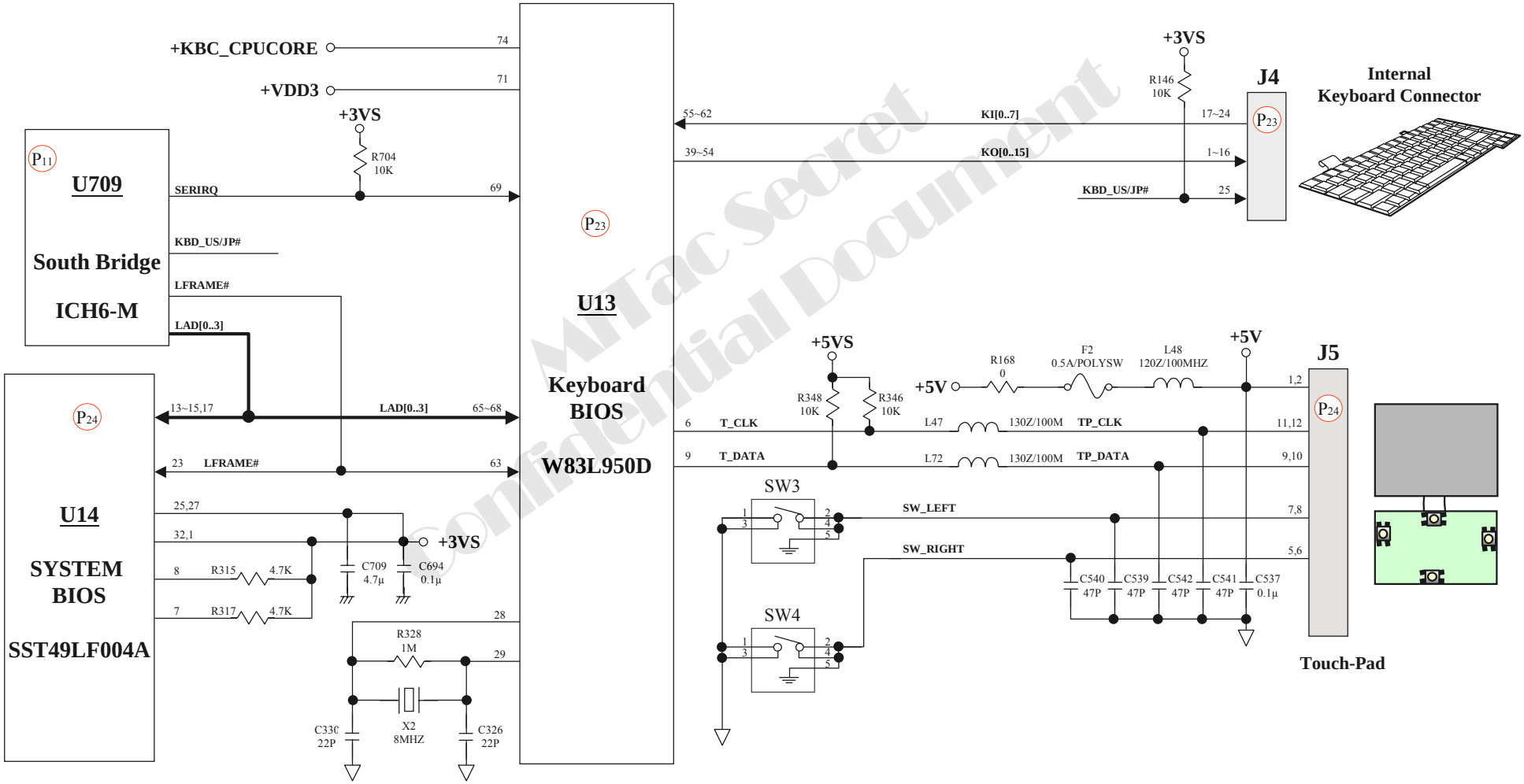
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-1

Error message of keyboard or touch-pad failure is shown or any key does not work.



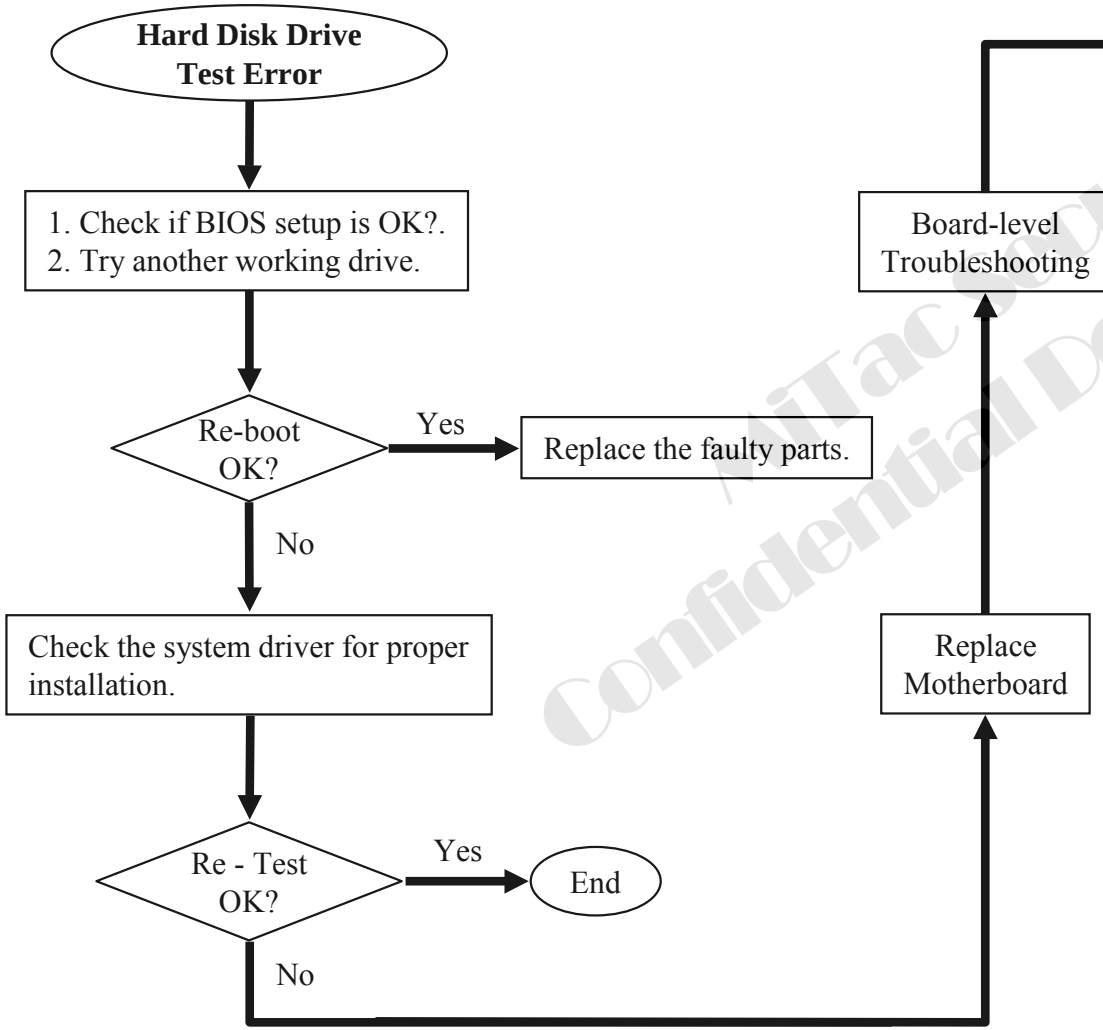
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-2

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Disk Drive Test Error-1

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.

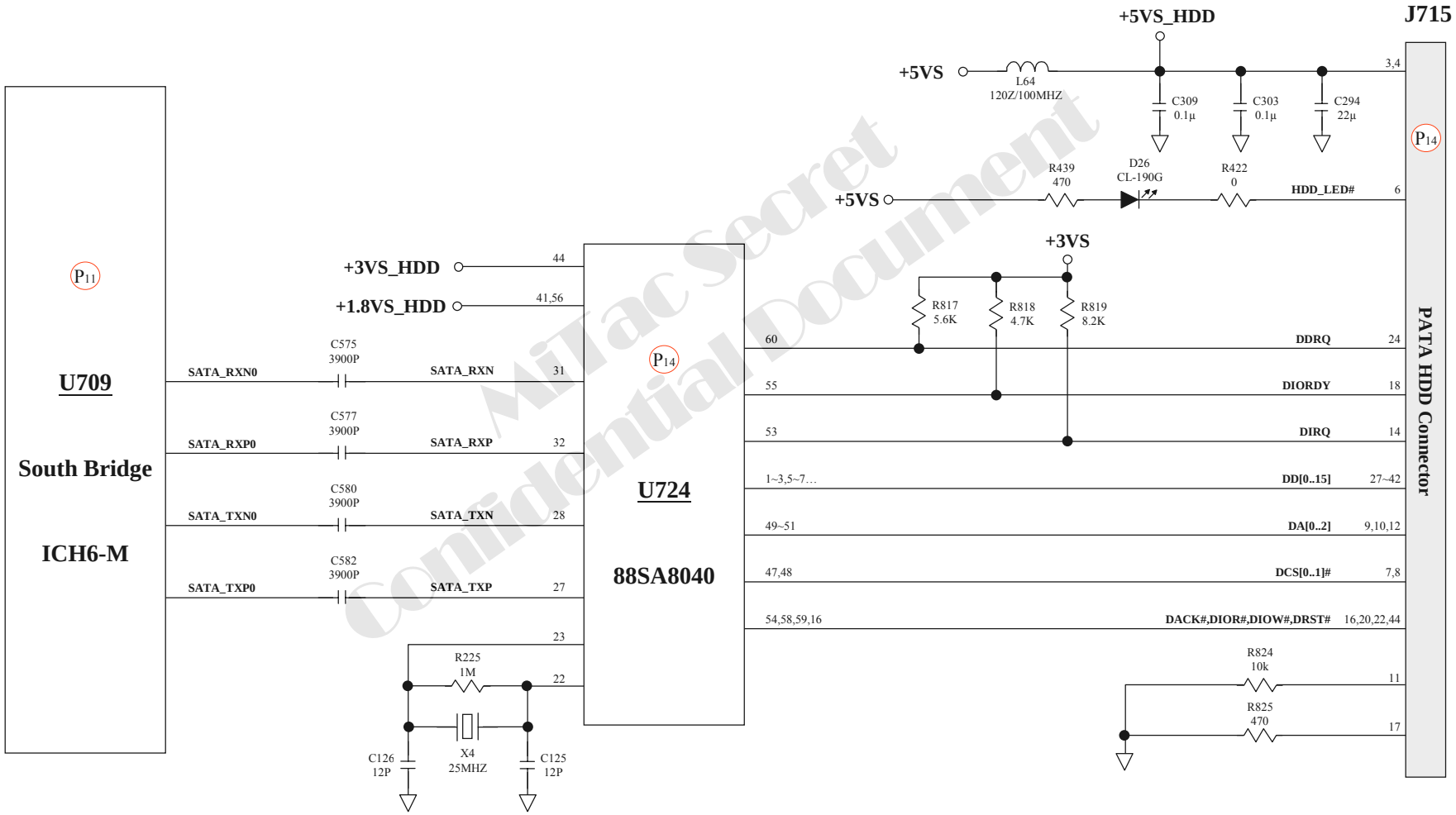


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U709	+5VS
U724	+5VS_HDD
J715	SATA_RXN0
X4	SATA_RXP0
L64	SATA_TXN0
D26	SATA_TXP0
C294	DDRQ
C303	DIORDY
C309	DIRQ
C575	DD[0..15]
C577	DA[0..2]
C580	DCS[0..1]#
C582	

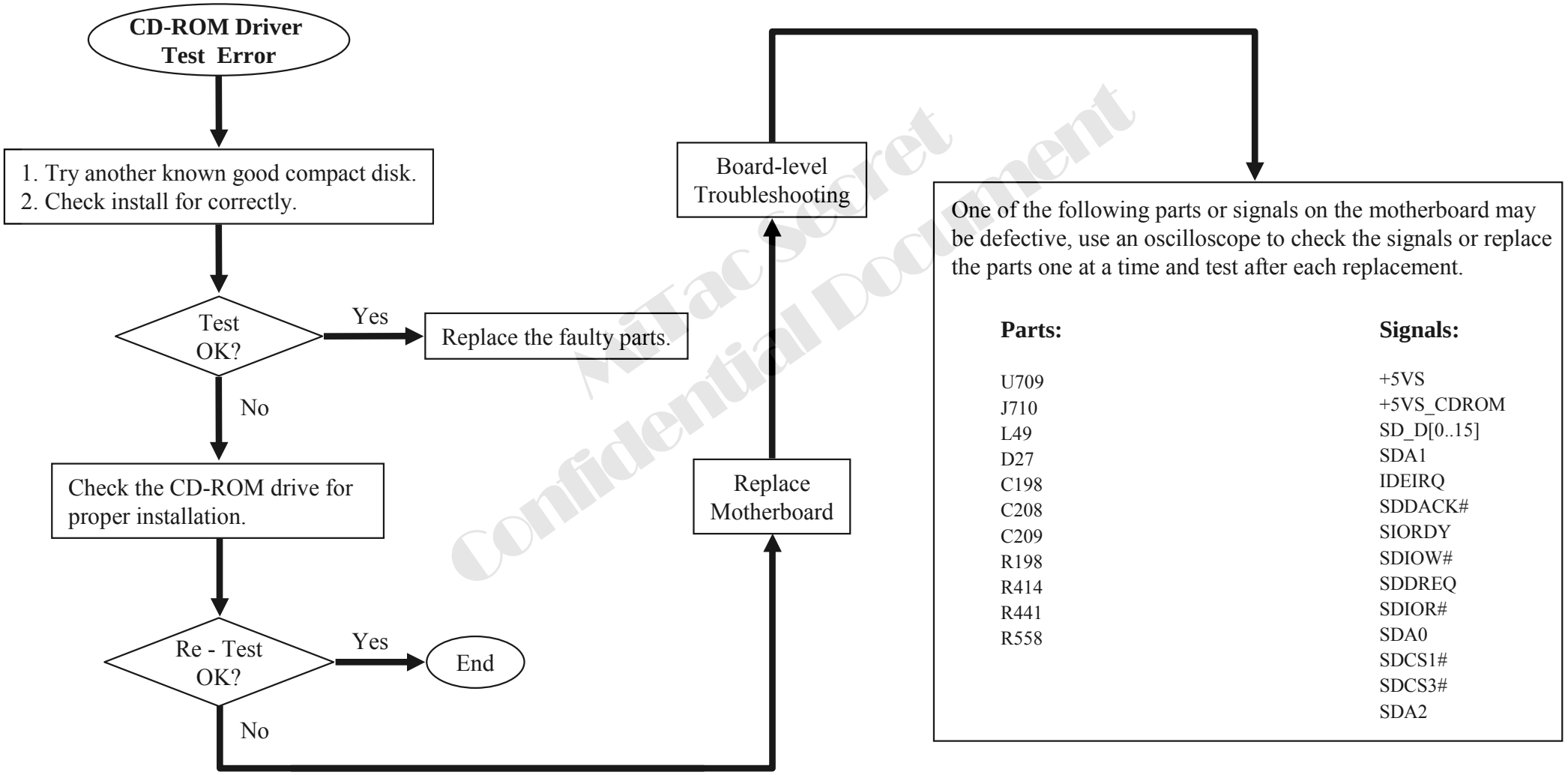
8.7 Hard Disk Drive Test Error-2

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



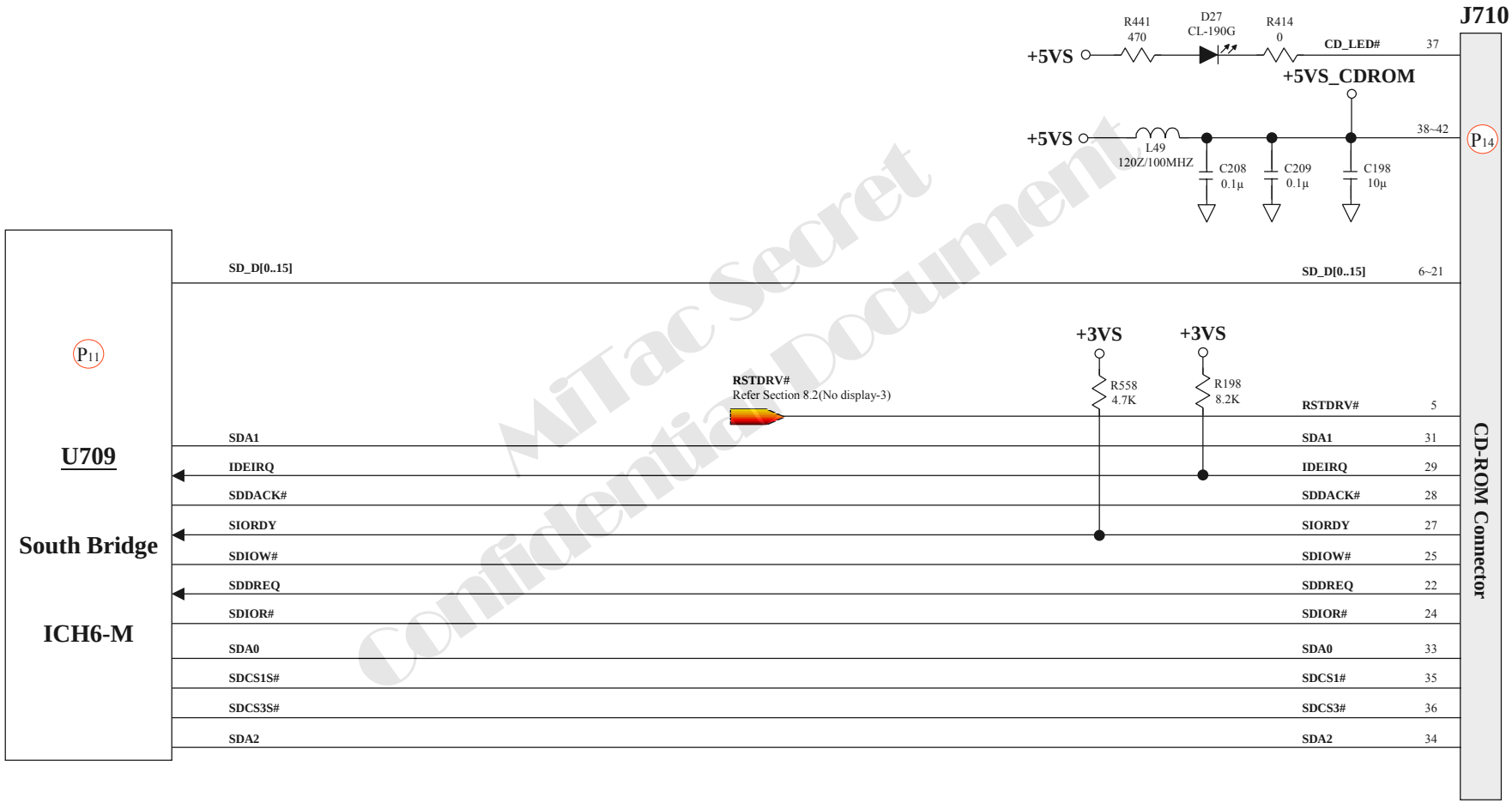
8.8 CD-ROM Drive Test Error-1

An error message is shown when reading data from CD-ROM drive.



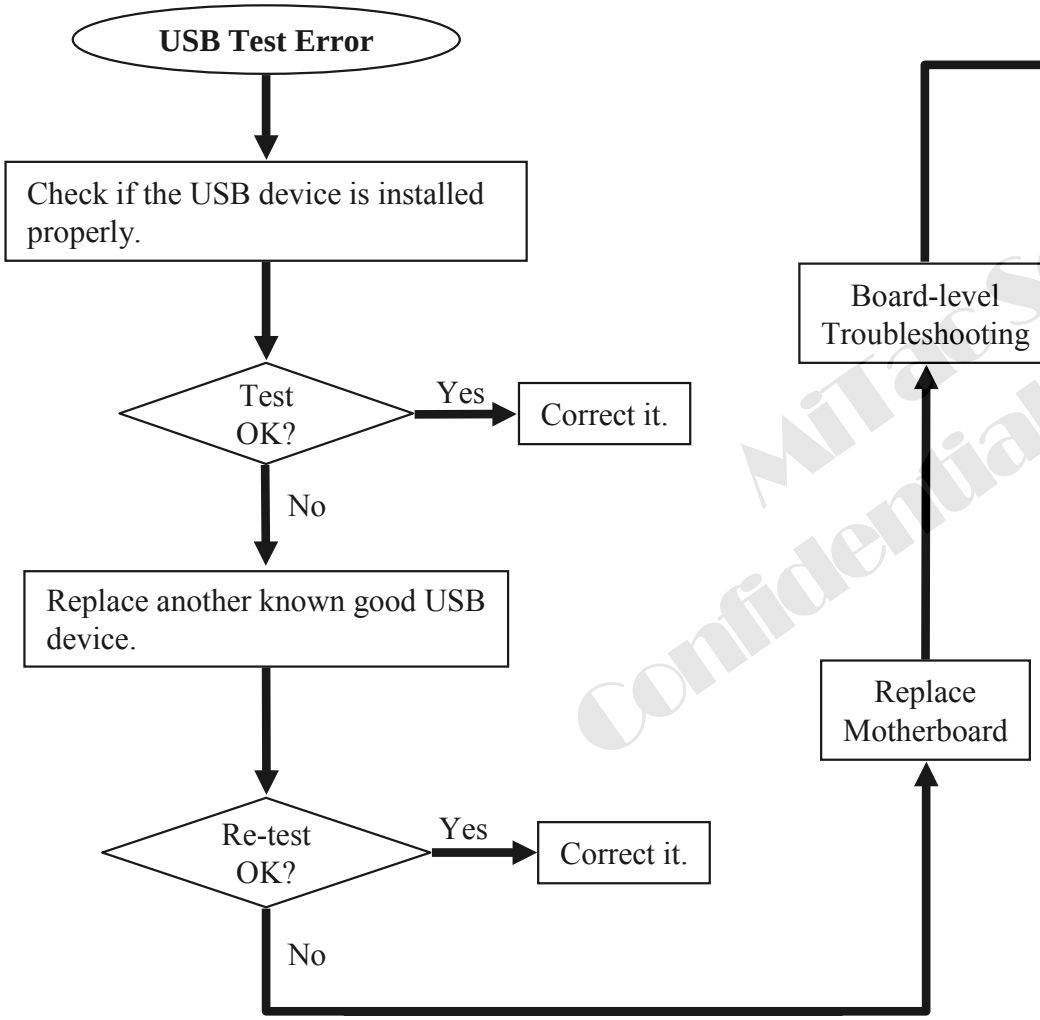
8.8 CD-ROM Drive Test Error-2

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error-1

An error occurs when a USB I/O device is installed.

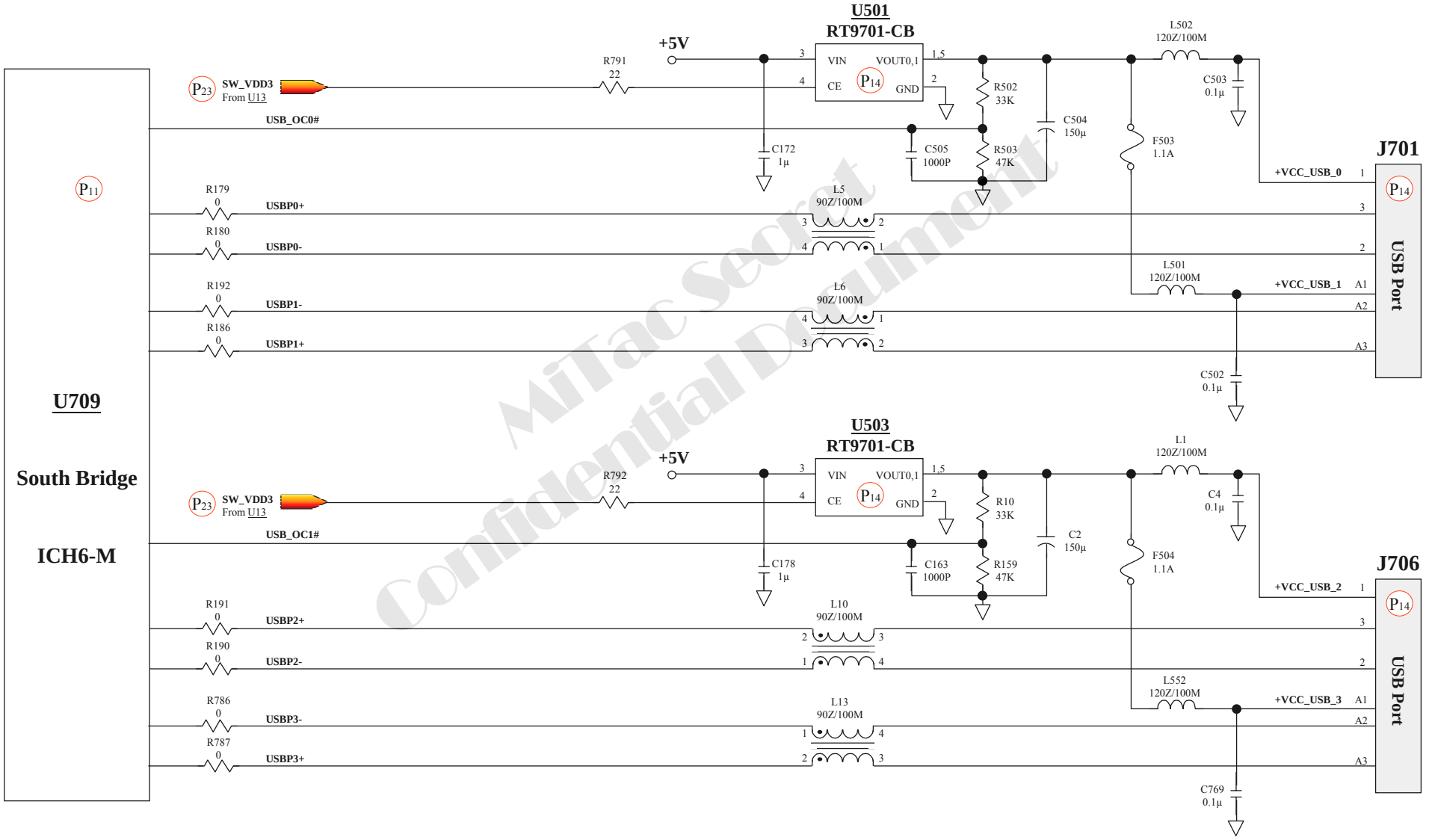


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U709	USB_OC0#
U501	USB_OC1#
U503	USBP[0..3]+
J701	USBP[0..3]-
J706	+VCC_USB_0
L5	+VCC_USB_1
L6	+VCC_USB_2
L10	+VCC_USB_3
L13	+5V
F503	SW_VDD3
F504	
C2	
C501	

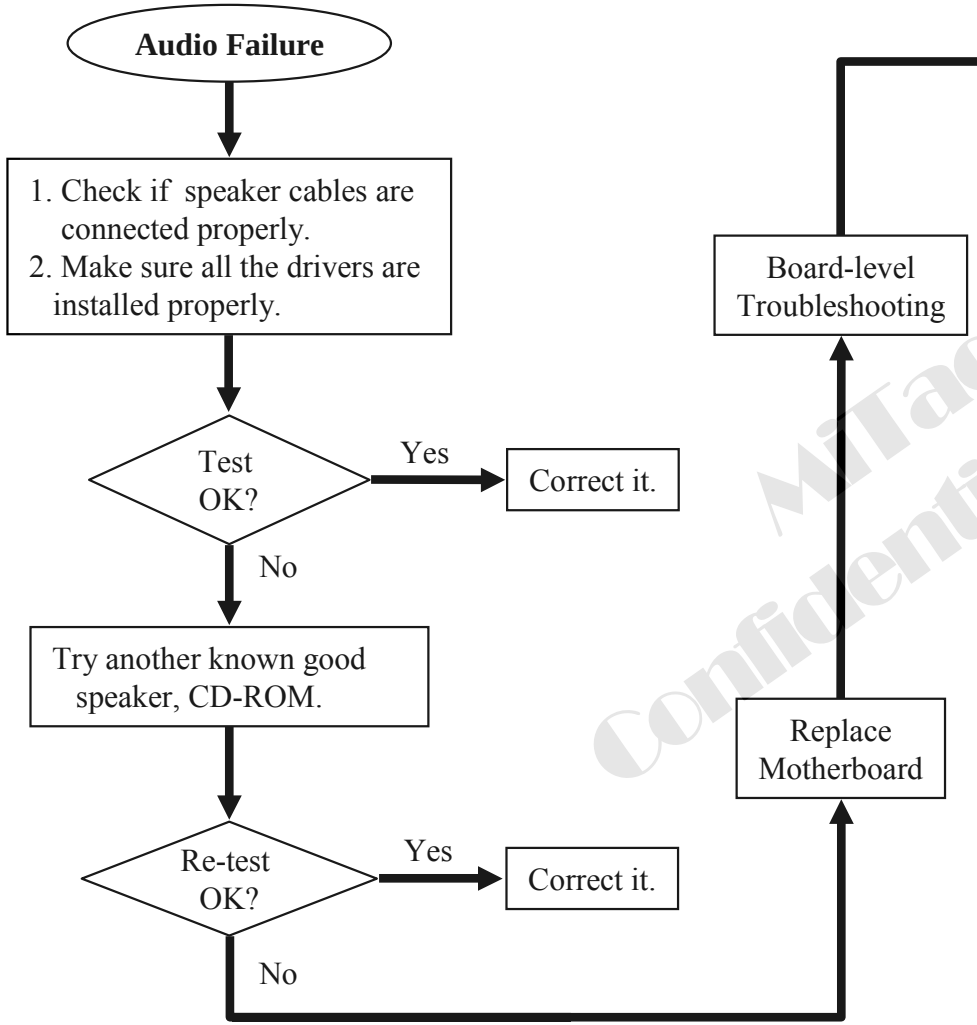
8.9 USB Test Error-2

An error occurs when a USB I/O device is installed.



8.10 Audio Test Error-1

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U517	AMP_RIGHT
U19	AMP_LEFT
U709	DEVICE_DECT
J509	DECT_HP#OPT
J7	SPDIFOUT
J3	SPK_OFF
L60	EAPD
L61	OPTIN#
Q48	
L20	
L18	
L73	
Q510	

2. If no sound cause of MIC, check the following parts & signals:

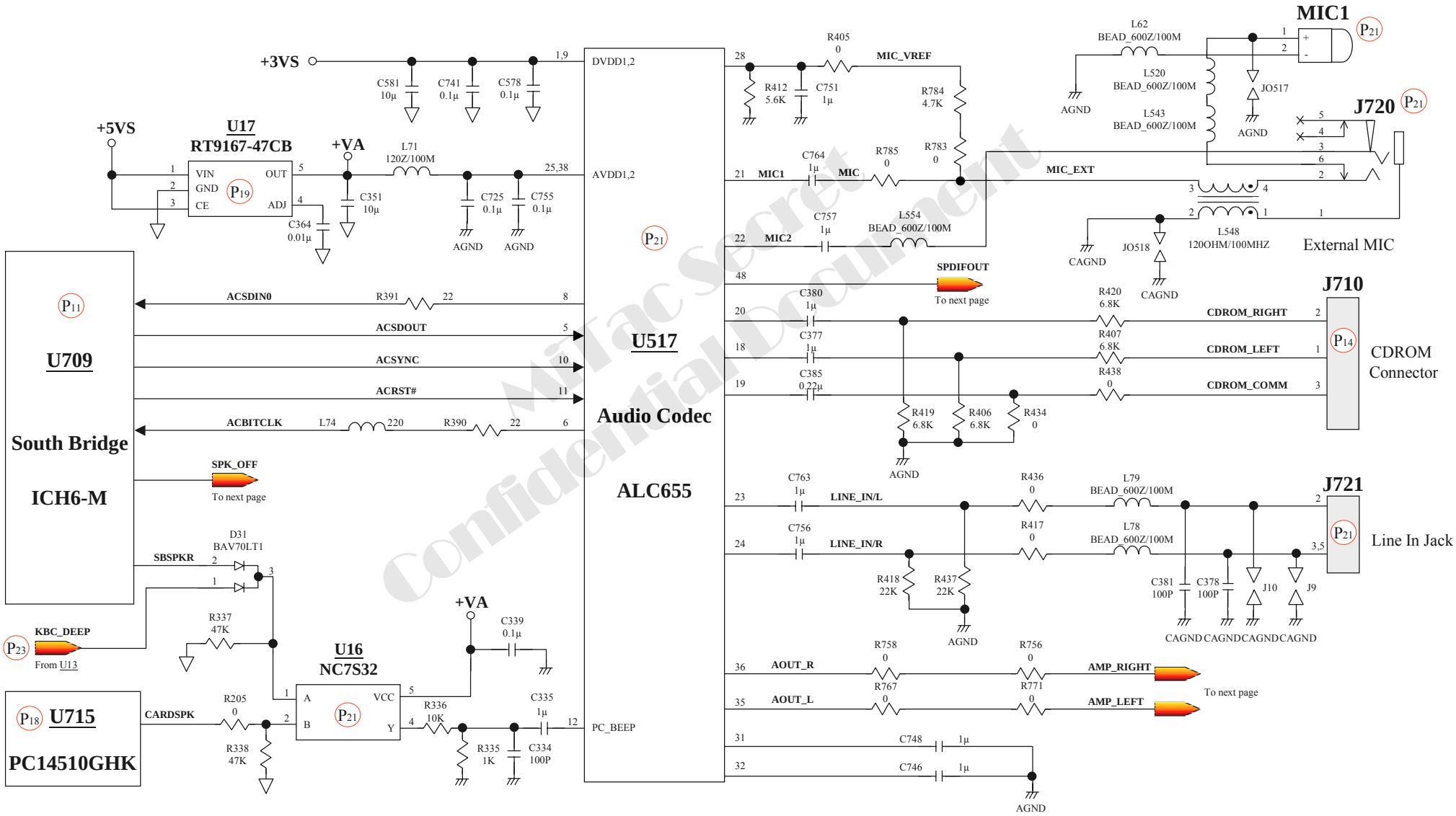
Parts:	Signals:
U517	+5VS
U709	+3VS
U16	+VA
U17	MIC_VREF
MIC1	MIC1
J720	MIC2
J721	MIC_EXT
L71	
L74	
D4	
L554	
L543	
L548	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U709	CDROM_LEFT
U517	CDROM_RIGHT
J710	CDROM_COMM
R420	
R407	
R438	
R419	
R406	
R434	

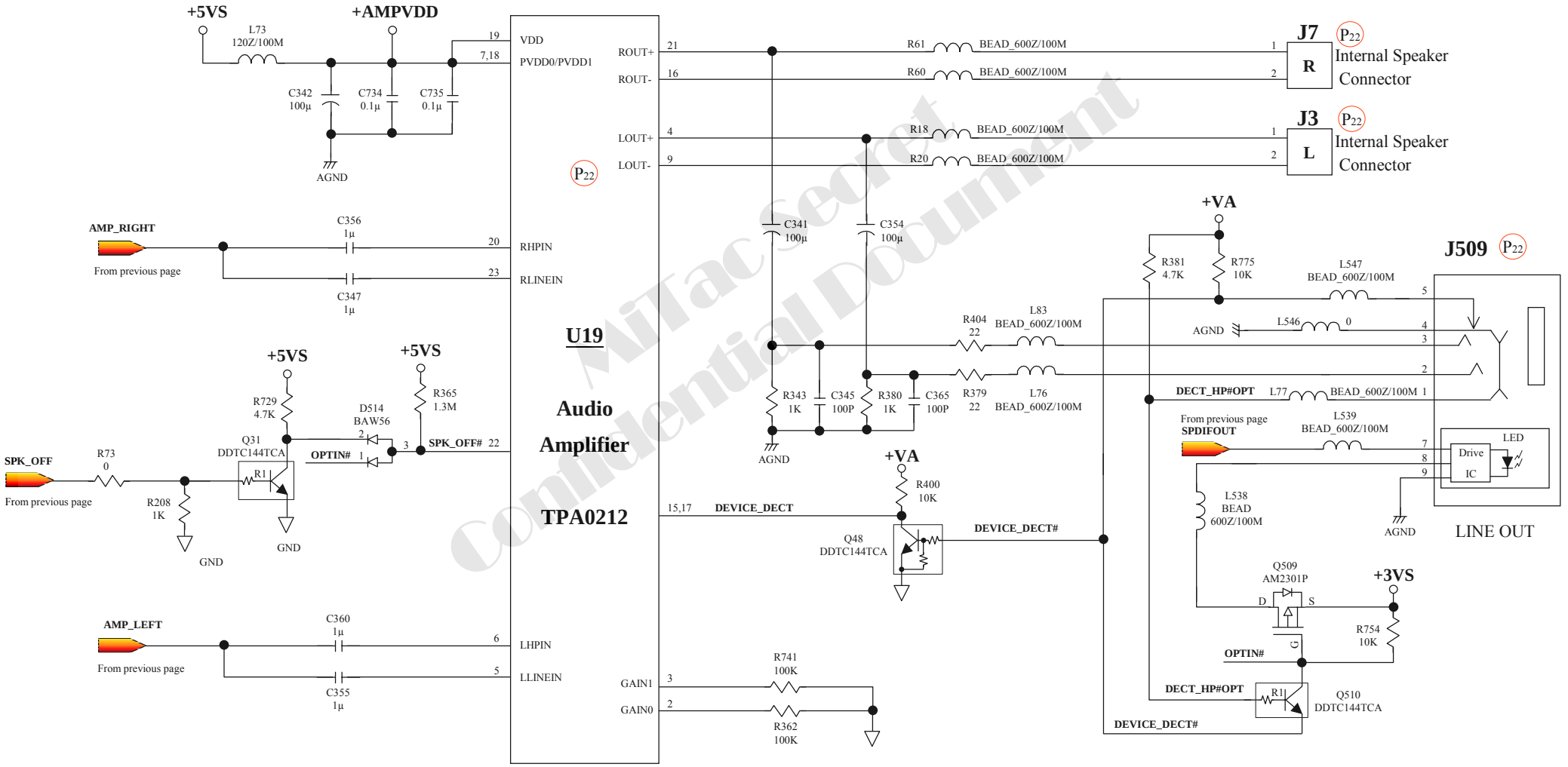
8.10 Audio Test Error-2 (Audio In)

No sound from speaker after audio driver is installed.



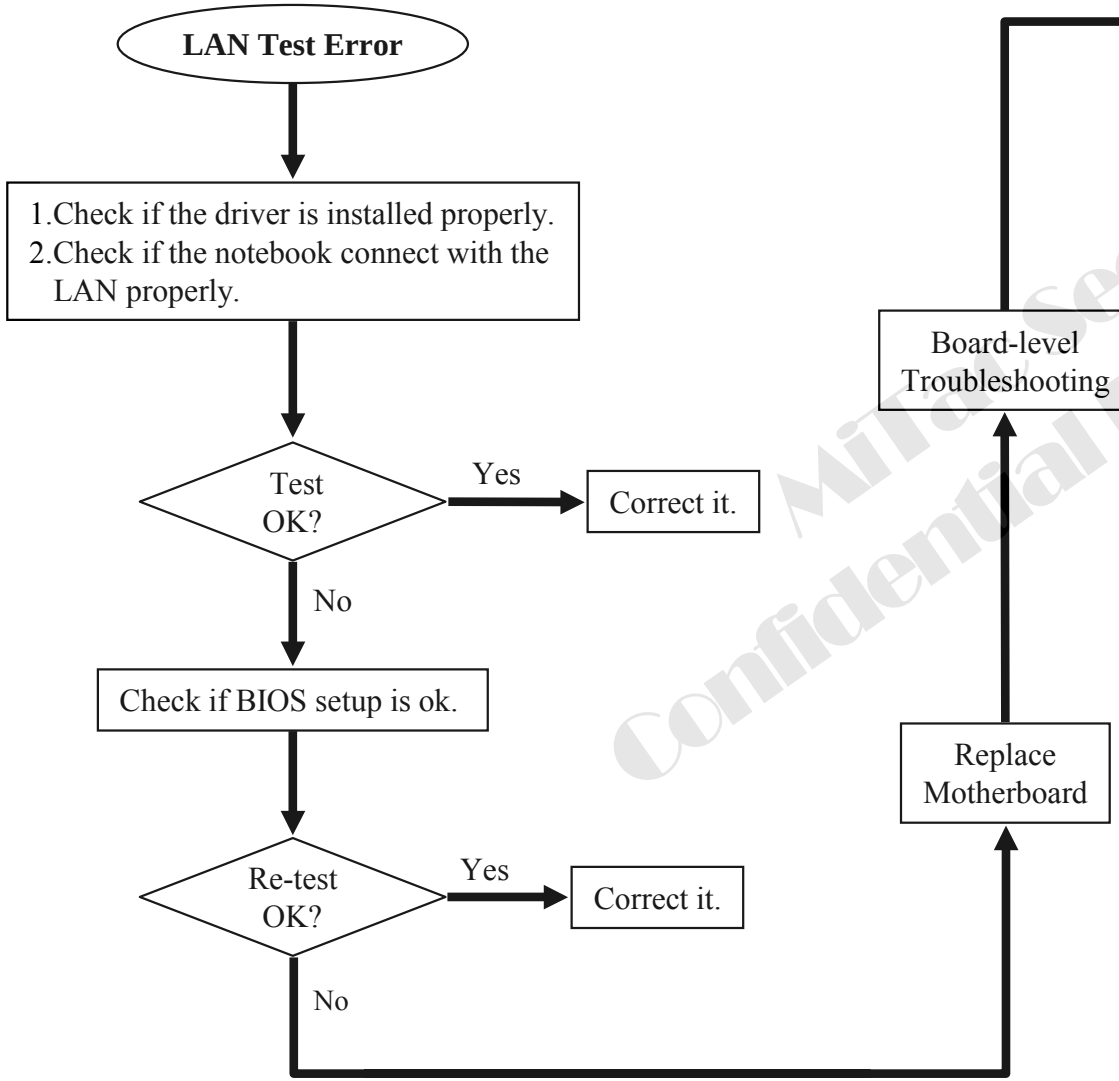
8.10 Audio Test Error-3 (Audio Out)

No sound from speaker after audio driver is installed.



8.11 LAN Test Error-1

An error occurs when a LAN device is installed.

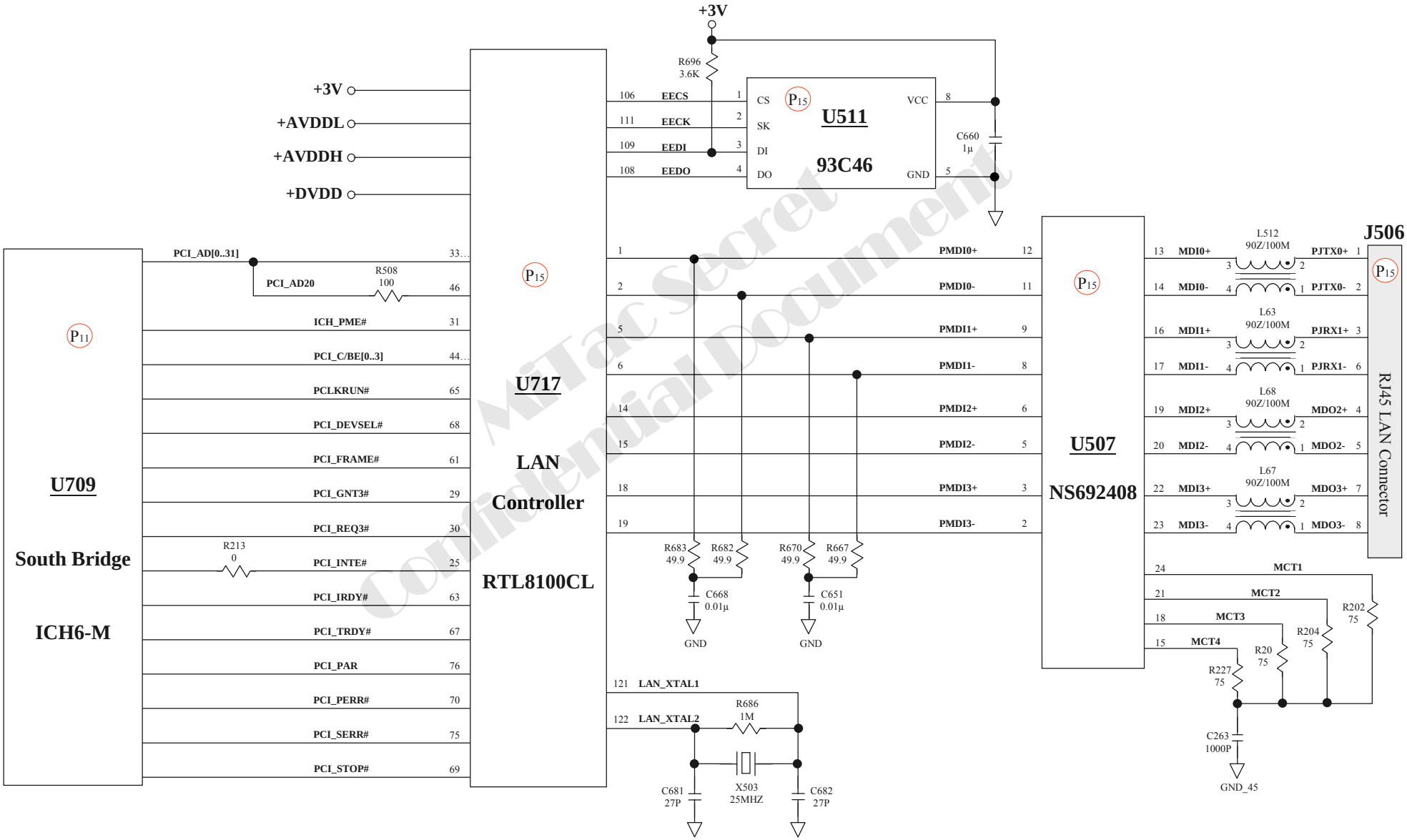


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U717	+3V
U709	ICH_PME#
U511	PCI_C/BE#[0..3]
J506	PCIKRUN#
U507	PCI_DEVESEL#
X503	PMDI[0..3]+
L508	PMDI[0..3]-
L510	EECS
L511	EECK
L512	EEDI
R682	EEDO
R683	PCI_SERR#
R667	
R670	

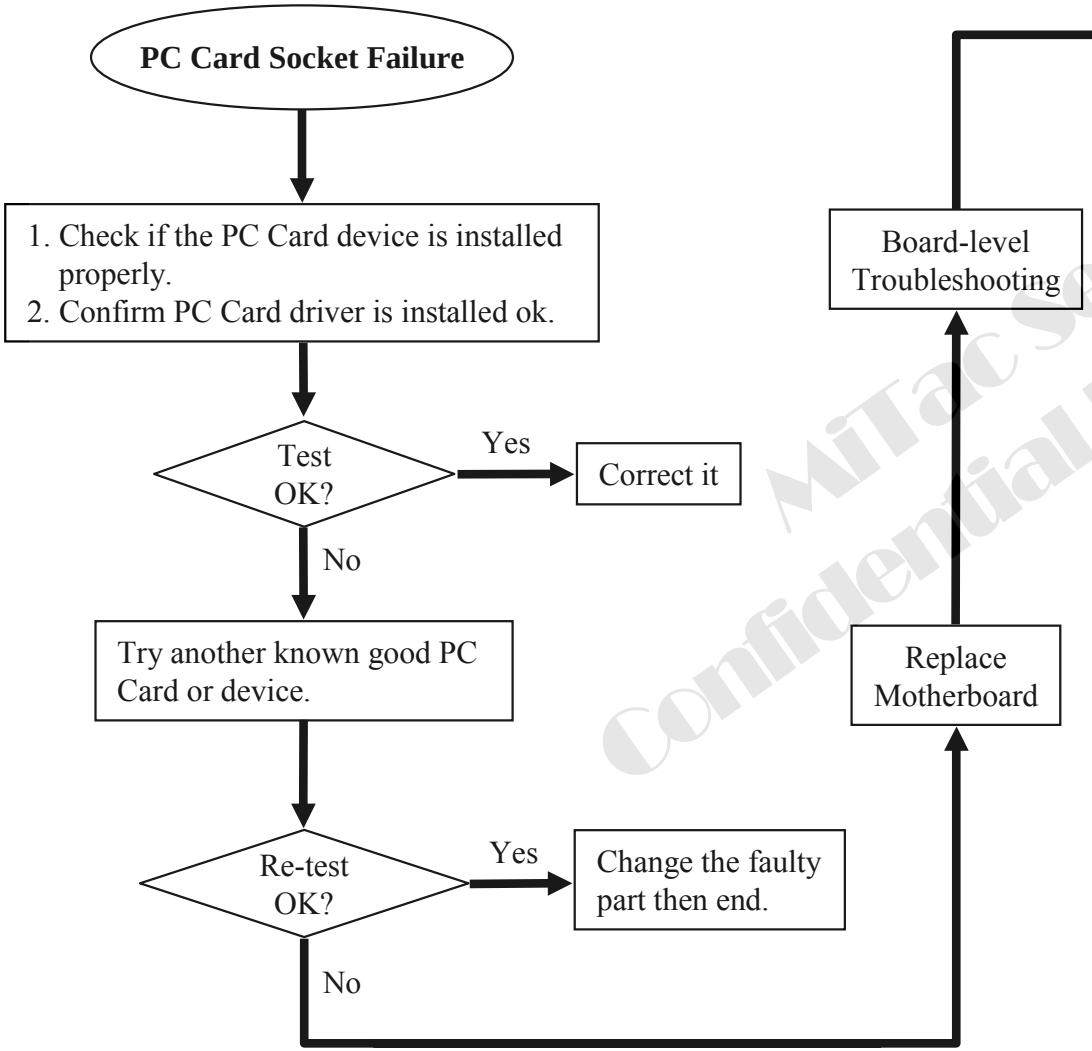
8.11 LAN Test Error-2

An error occurs when a LAN device is installed.



8.12 PC Card Socket Test Error-1

An error occurs when a PC card device is installed.

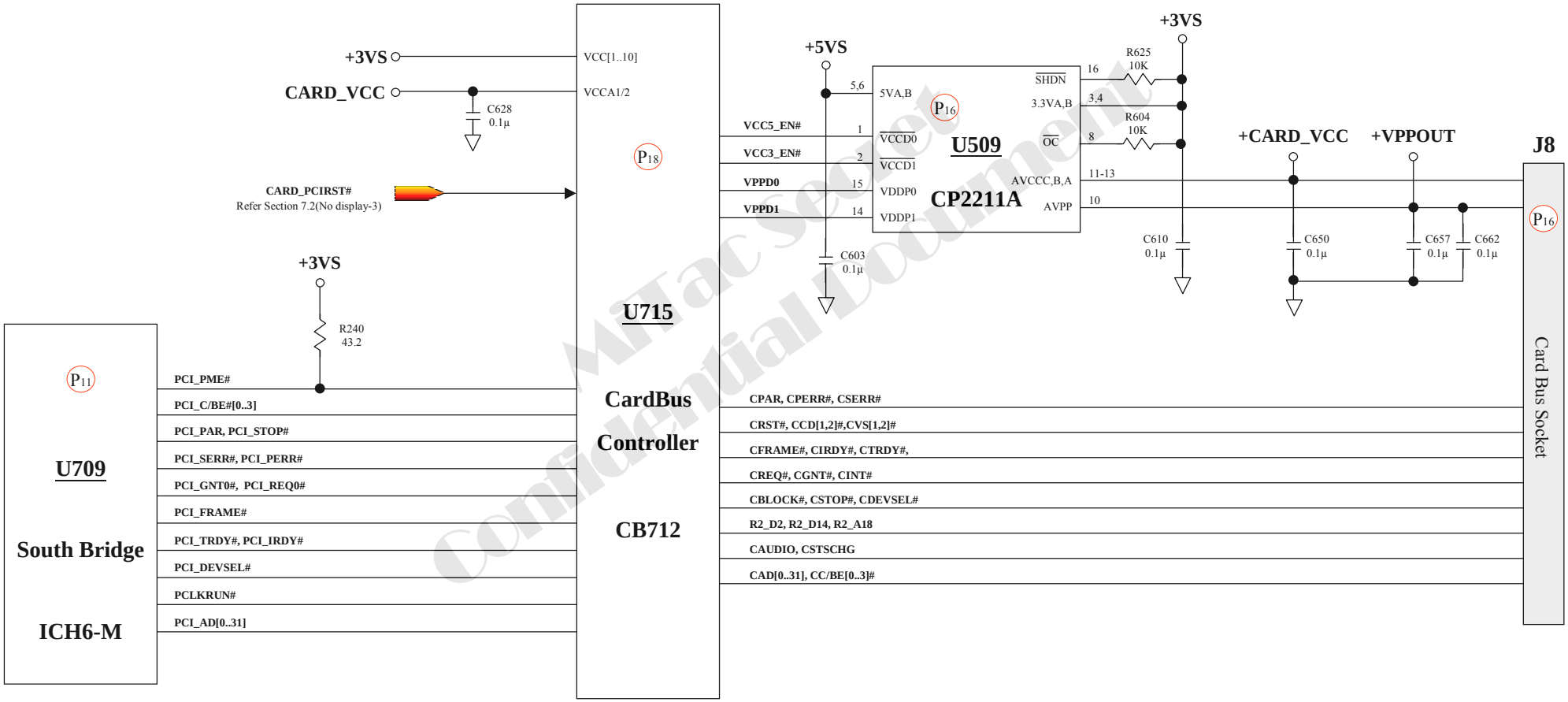


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals	
U715	PCI_REQ0#	PCI_PME#
U709	PCI_SERR#	PCI_GNT0#
U509	PCI_PERR#	PIC_PAR
J8	PCI_DEVSEL#	PCI_AD[0..31]
R625	PCI_FRAME#	PCI_C/BE#[0..3]
R604	PCI_IRDY#	VCC5_EN#
R240	PCI_TRDY#	VCC3_EN#
	PCI_STOP#	VPPD0
	PCLKRUN#	VPPD1

8.12 PC Card Socket Test Error-2

An error occurs when a PC card device is installed.



Reference Material

- Intel Pentium-M Processor — *Intel, INC*
- Intel 915PM North Bridge Data Sheet — *Intel, INC*
- Intel ICH6 South Bridge Data Sheet — *Intel, INC*
- System Explode View — *Technology.Corp./MiTAC*
- 8050QMA Hardware Engineering Specification — *Technology.Corp./MiTAC*

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