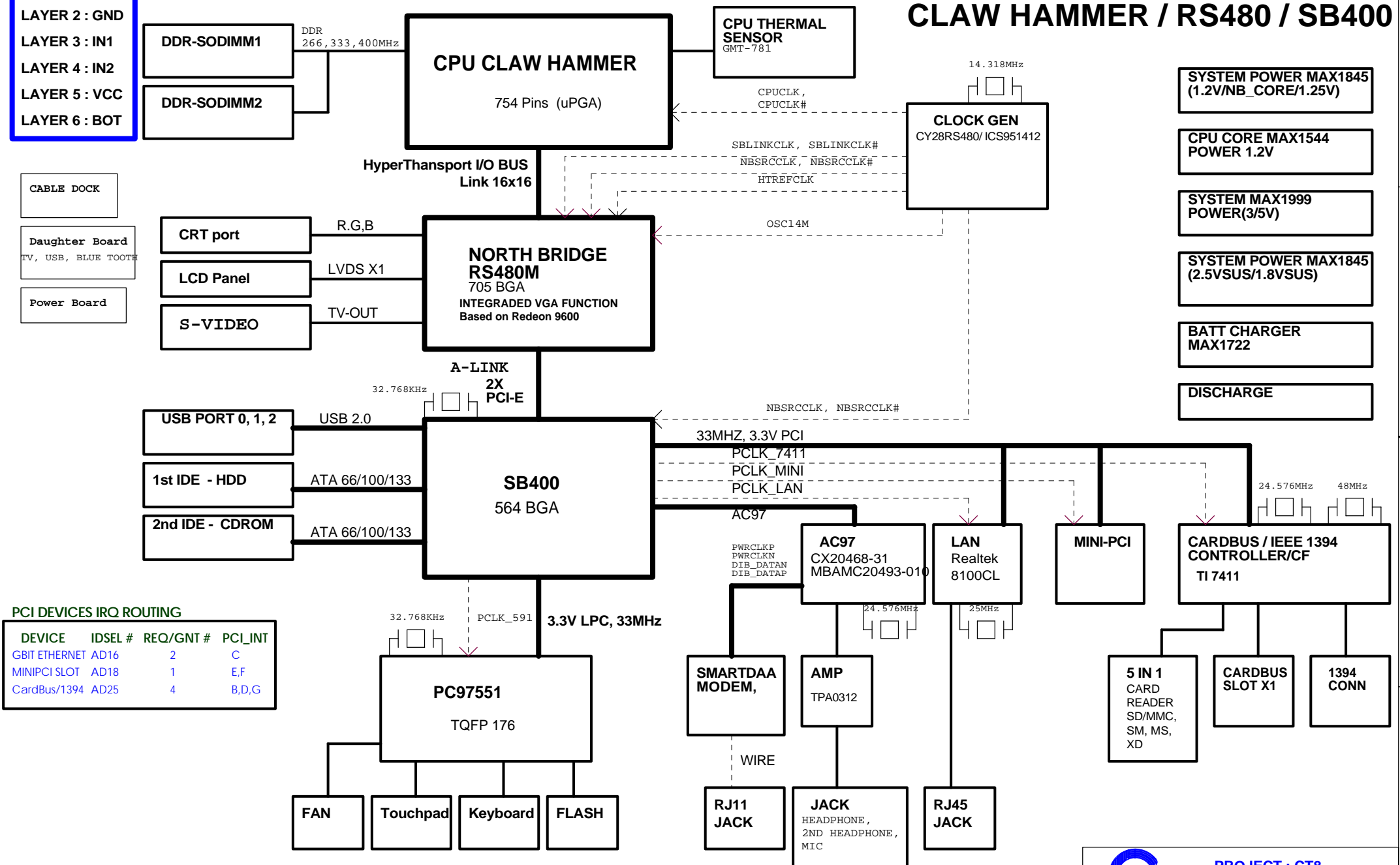


CT8 BLOCK DIAGRAM

CLAW HAMMER / RS480 / SB400

PCB STACK UP

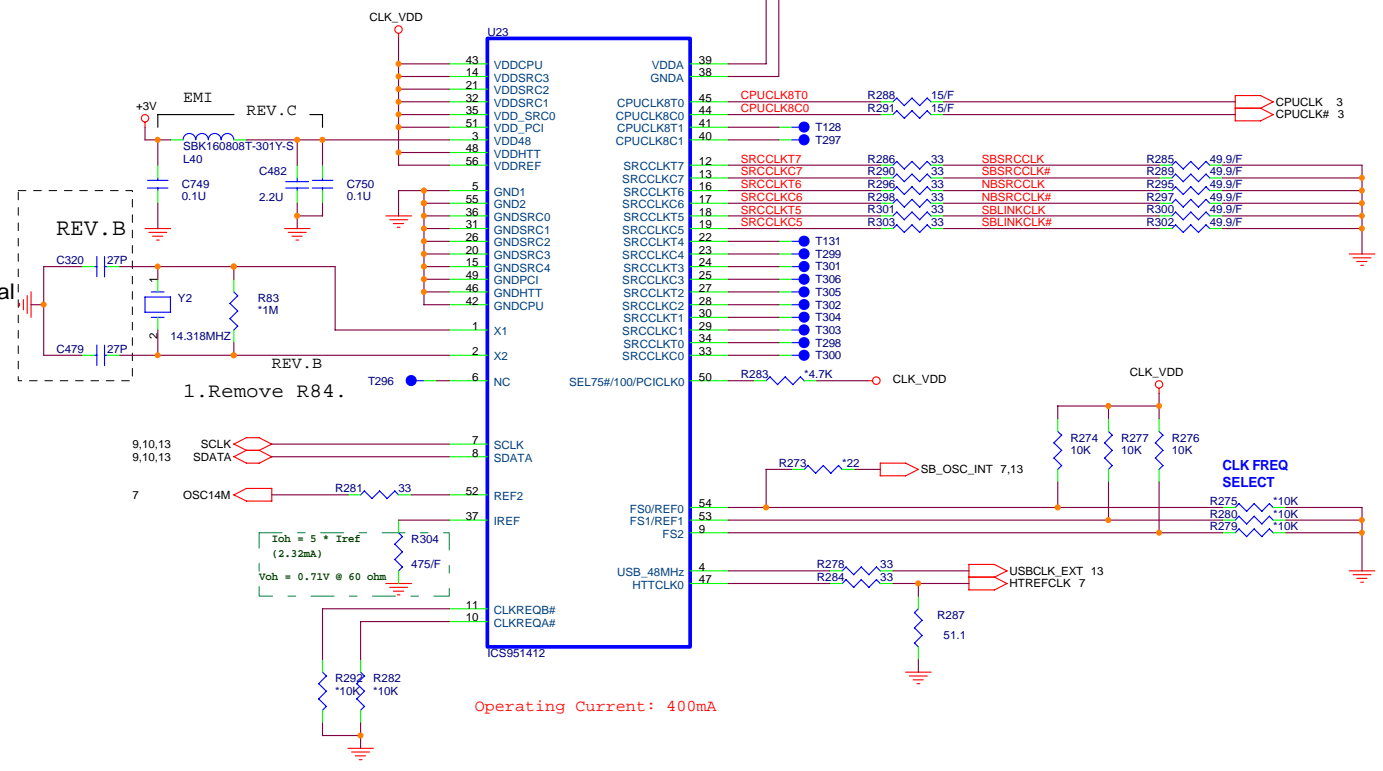
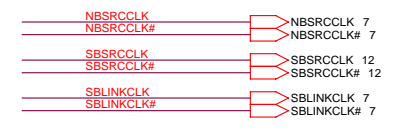
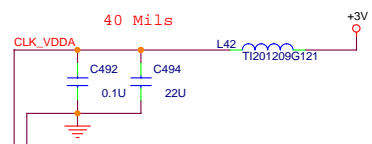
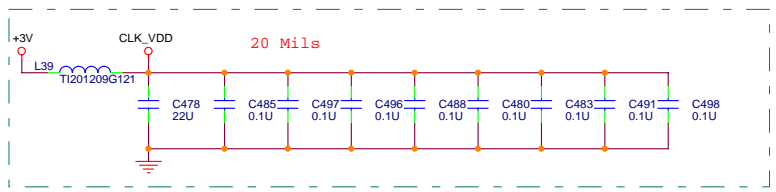
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



- SYSTEM POWER MAX1845 (1.2V/NB_CORE/1.25V)
- CPU CORE MAX1544 POWER 1.2V
- SYSTEM MAX1999 POWER(3/5V)
- SYSTEM POWER MAX1845 (2.5VSUS/1.8VSUS)
- BATT CHARGER MAX1722
- DISCHARGE

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET AD16		2	C
MINIPCI SLOT AD18		1	E,F
CardBus/1394 AD25		4	B,D,G



Parallel Resonance Crystal
Tolerance: 35ppm (max)
Load: 20pf

1. Remove R84.

Operating Current: 400mA

Layout Note:

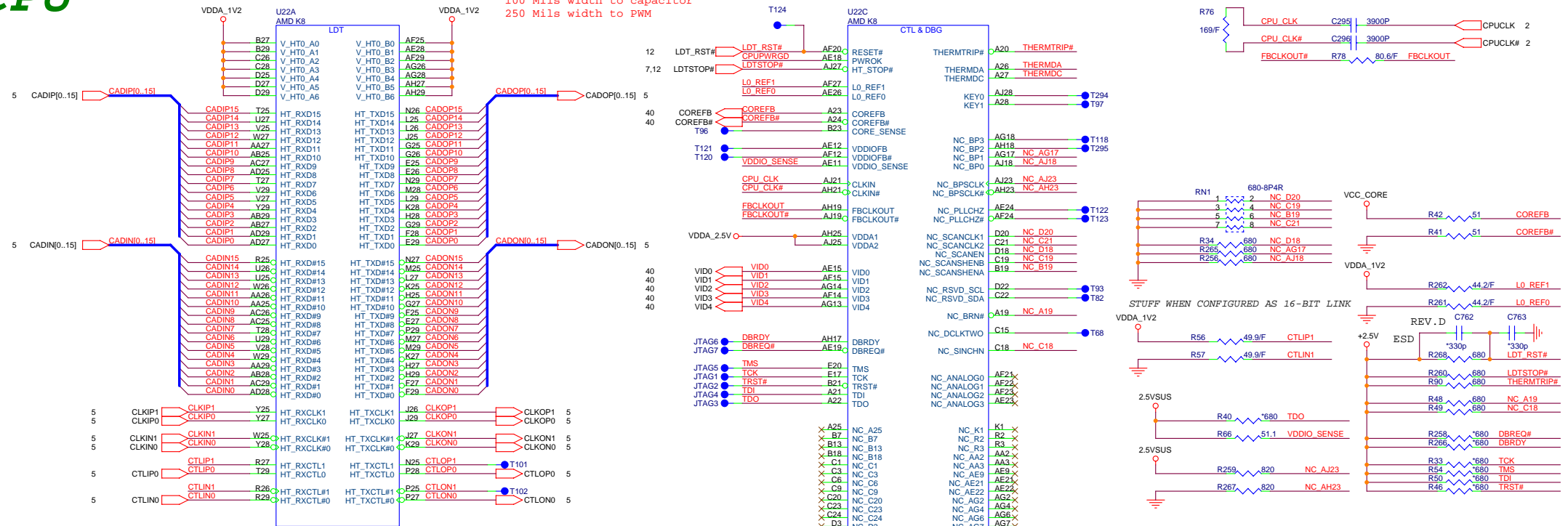
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CKG. AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

EXT CLK FREQUENCY SELECT TABLE(MHZ)

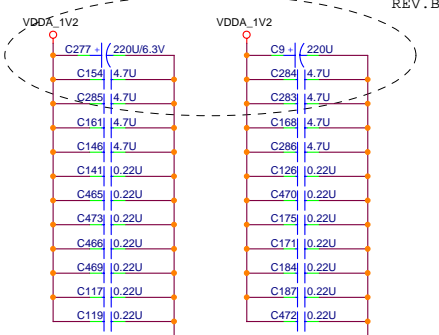
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation



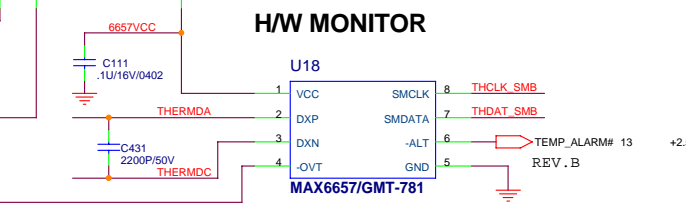
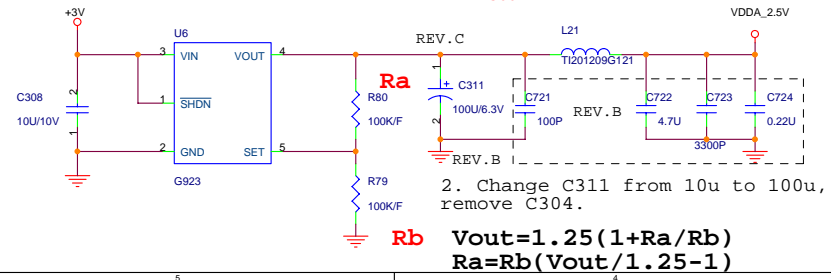
20 Mils width to pin
100 Mils width to capacitor
250 Mils width to PWM



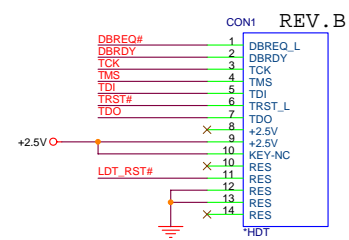
add c154,c283,c284,c285 4.7u
c9,c277 100u change to 220u

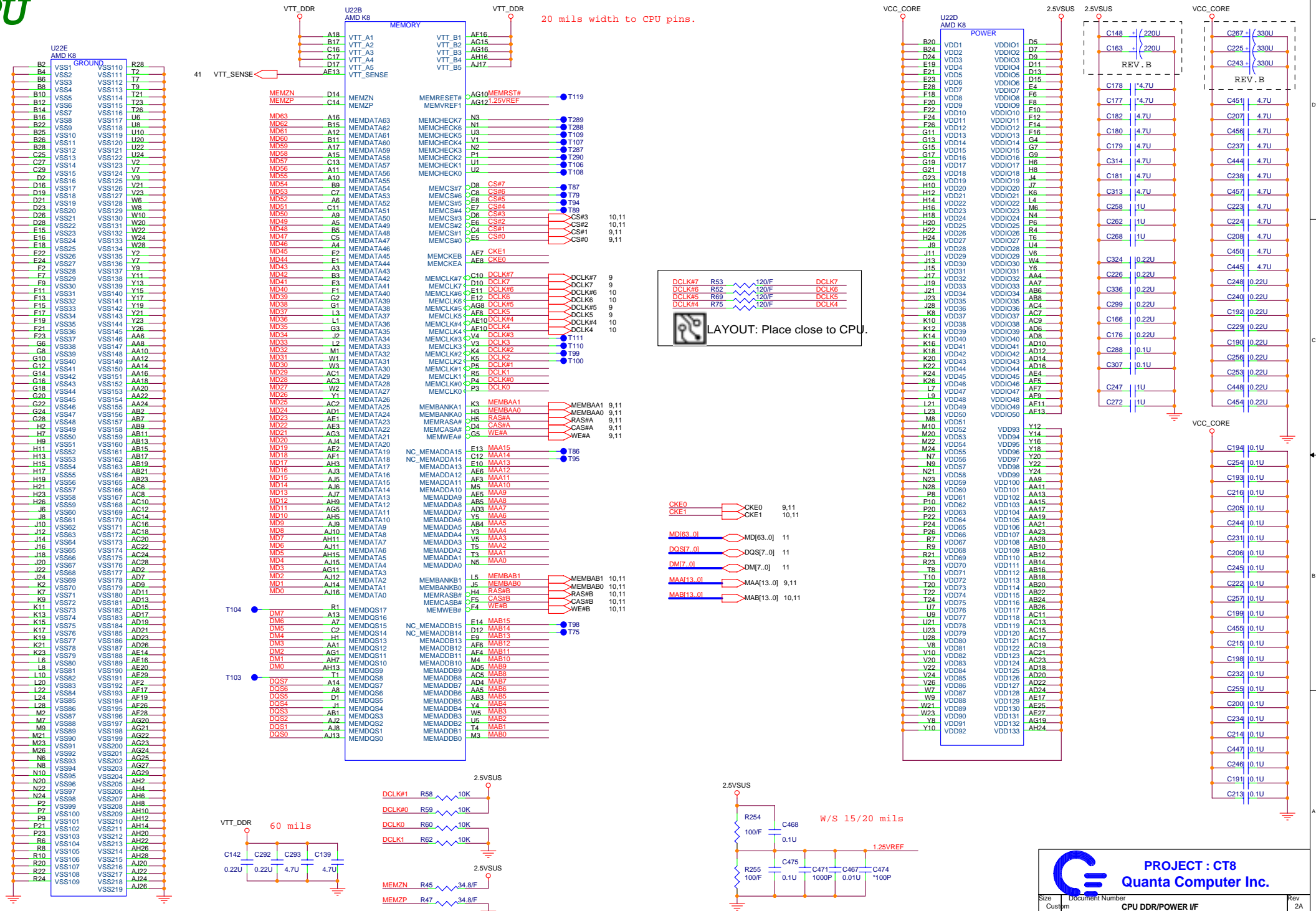


50 Mils, routing as 15 mils width if the distance from bead to cpu pin less than 1000 mils.



1. Remove R386,Q33, connect U18 pin 6 to TEMP_ALARM#.





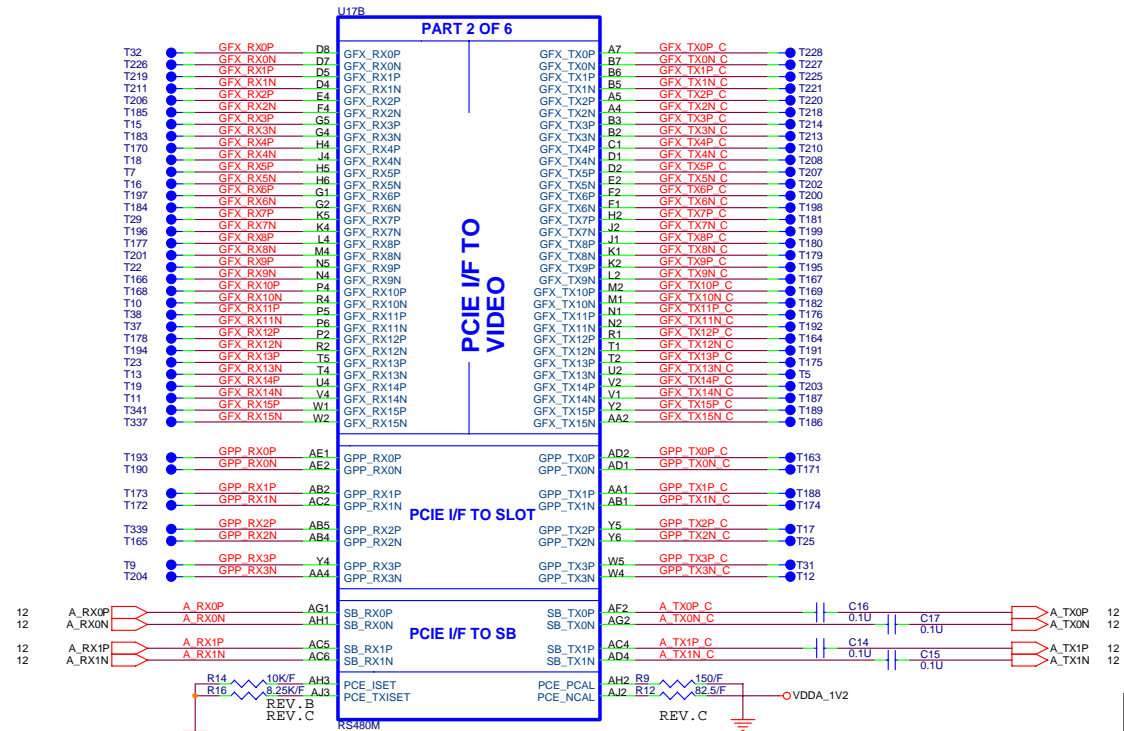
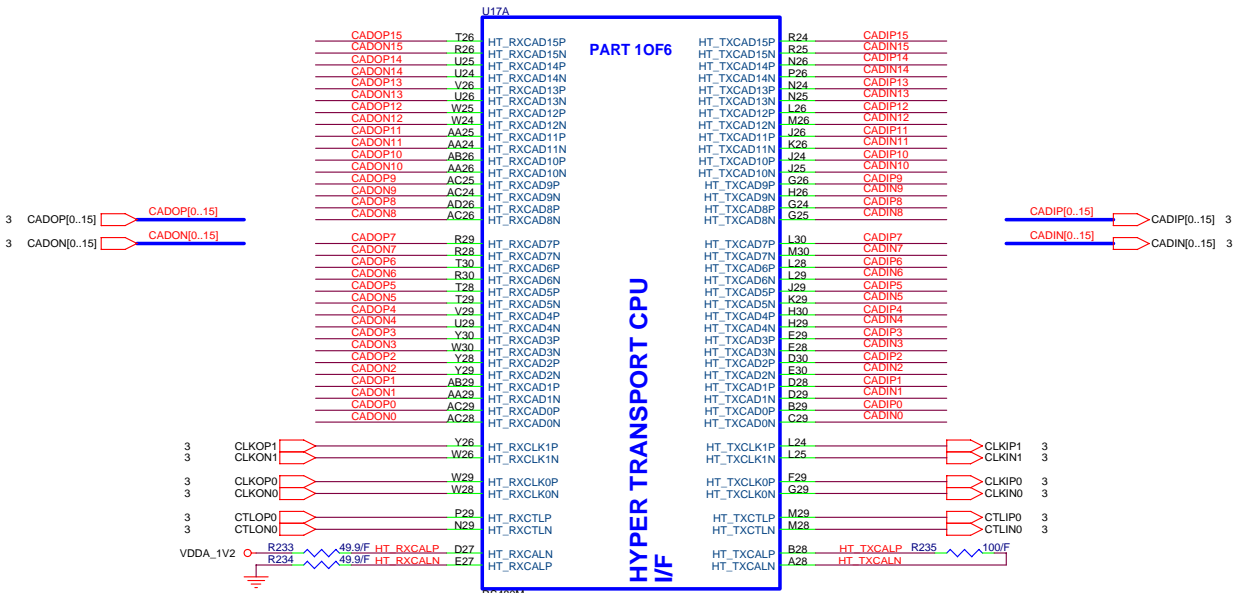
20 mils width to CPU pins.

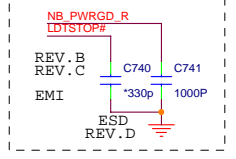
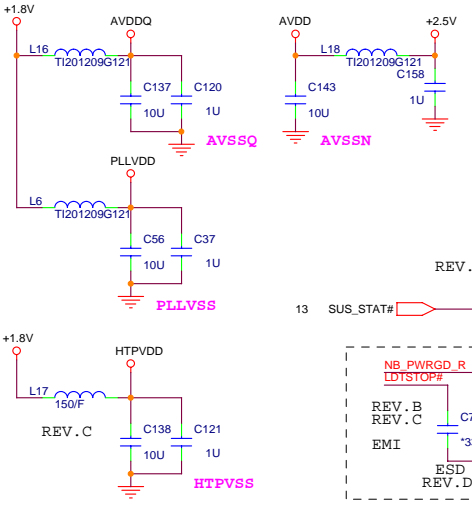
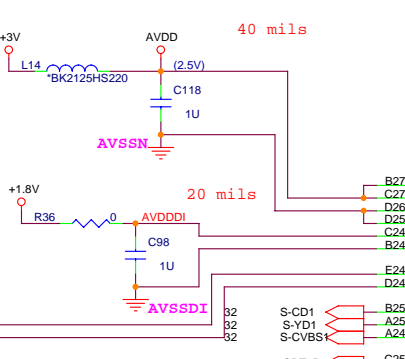
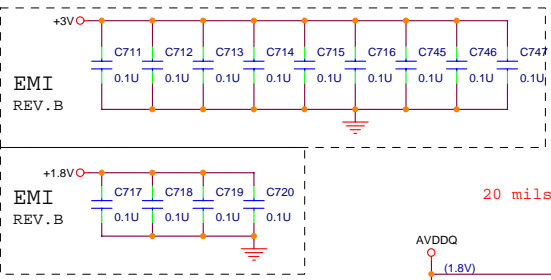
LAYOUT: Place close to CPU.

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU DDR/POWER I/F	2A

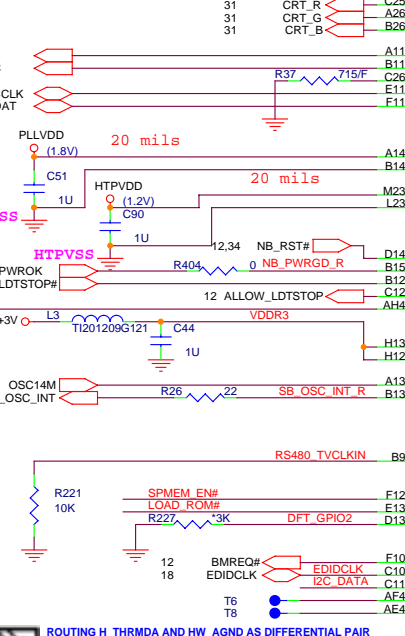
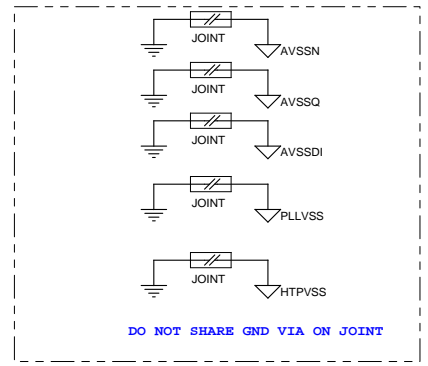
Date: Thursday, April 14, 2005 Sheet 4 of 42



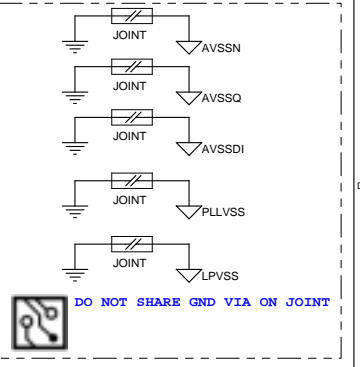
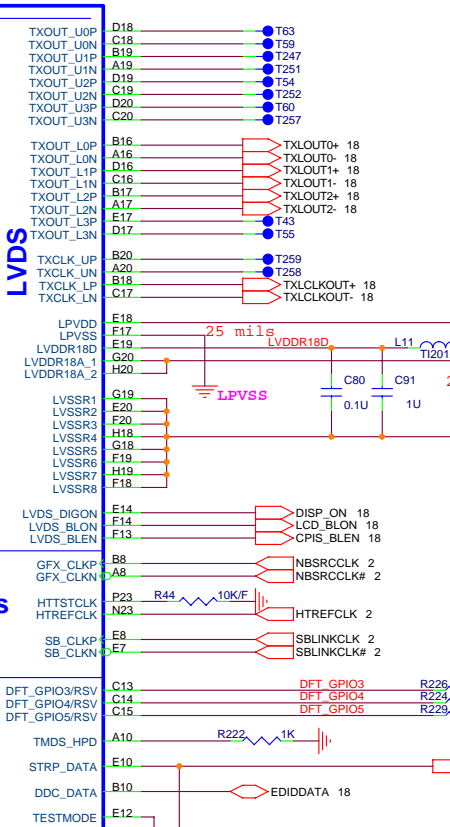
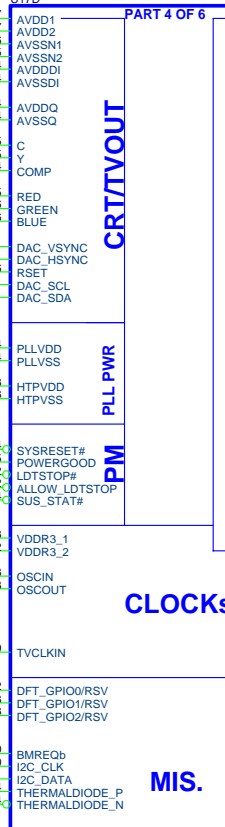


- AVDD DAC VDD (2.5V)
- AVDDDI DIGITAL VDD (1.8V)
- AVDDQ DAC2 BANDGAP REF (1.8V)
- PLLVD PLL VDD (1.8V)
- HTPVDD HT PLL VDD (1.8V)

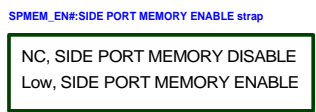
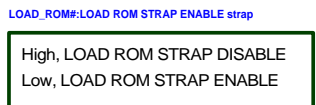
PUT AVDD, AVDDDI, AVDDQ, PLLVDD, HTPVDD DECOUPLING CAPS ON THE BOTTOM, CLOSE TO BALLS



ROUTING H_THRMCA AND HW_AGND AS DIFFERENTIAL PAIR

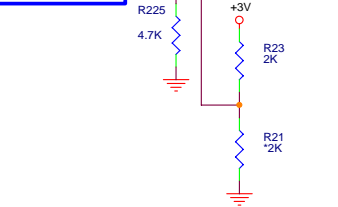


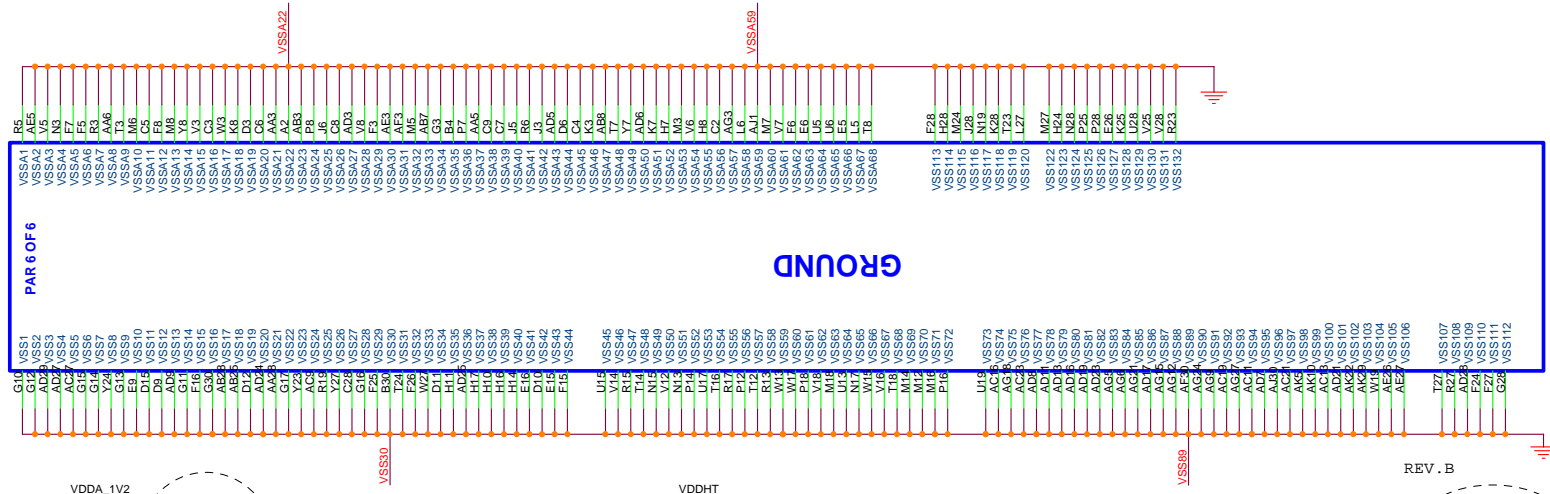
REV.B DEL Y1 AND U3 CIRCUIT.



LOAD_ROM#: LOAD ROM STRAP ENABLE strap
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

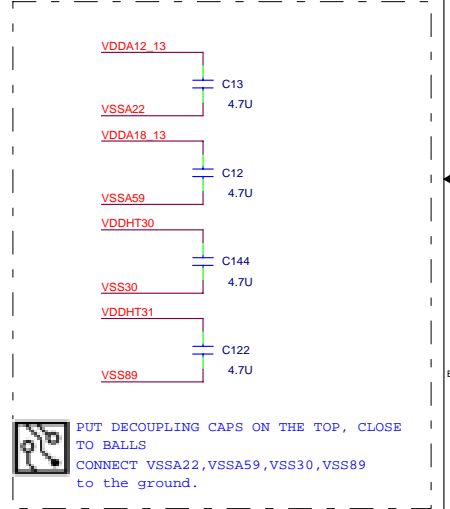
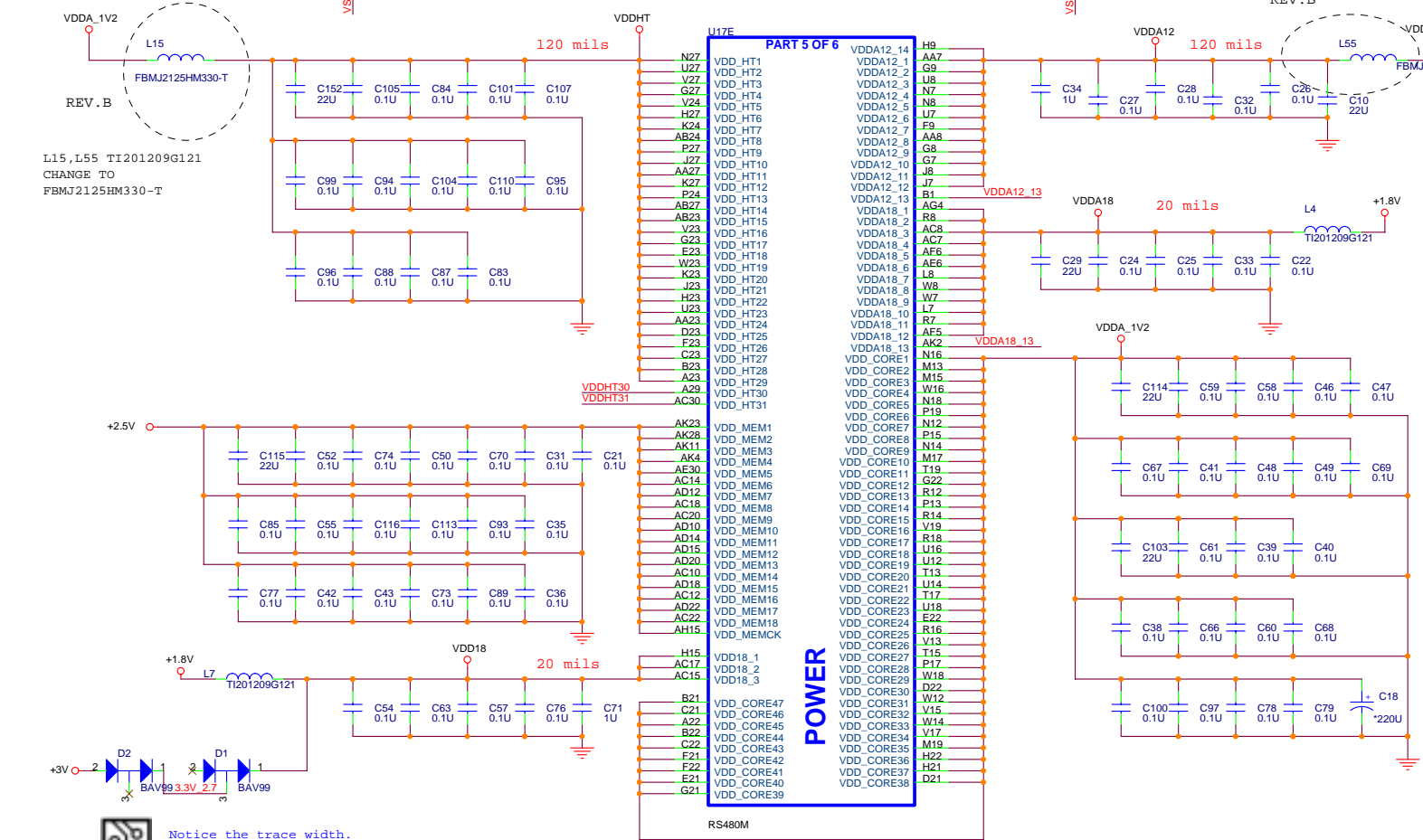
SPMEM_EN#: SIDE PORT MEMORY ENABLE strap
NC, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE





NB RS480 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	ON	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

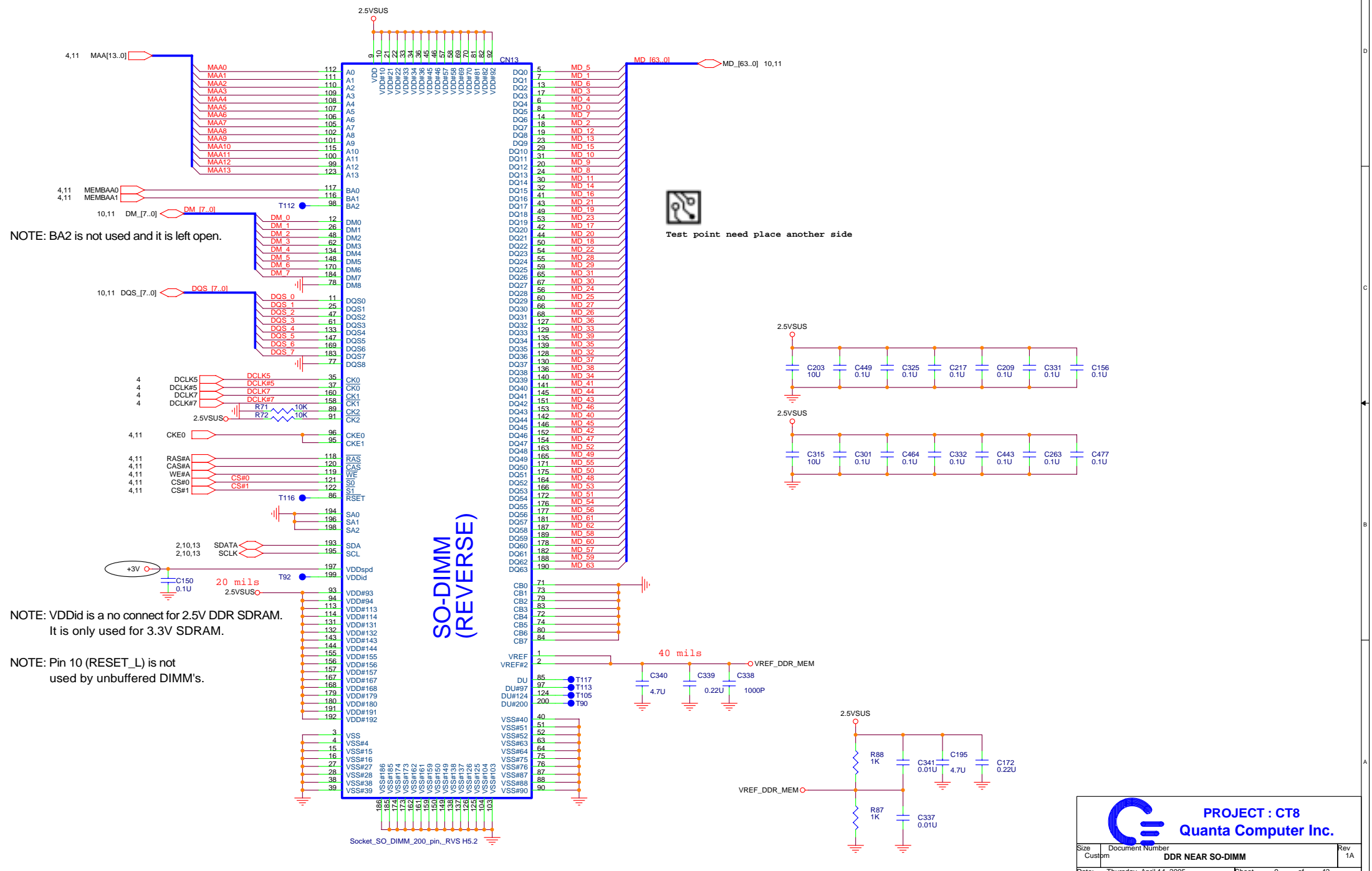


PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22, VSSA59, VSS30, VSS89 to the ground.

Notice the trace width.

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Size Custom	Document Number RS480M-POWER	Rev 2A
Date: Thursday, April 14, 2005		Sheet 8 of 42



NOTE: BA2 is not used and it is left open.

Test point need place another side

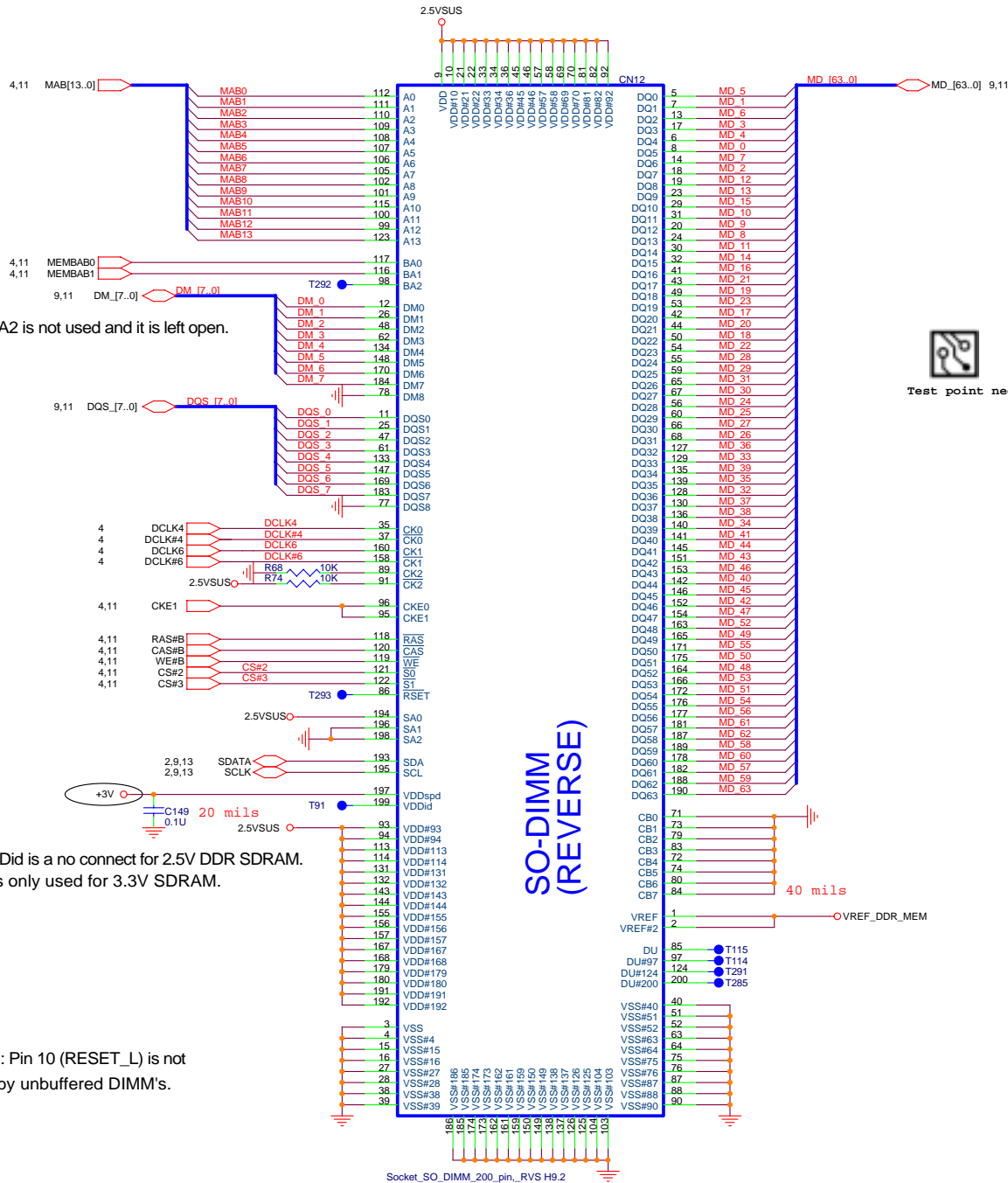
NOTE: VDDid is a no connect for 2.5V DDR SDRAM. It is only used for 3.3V SDRAM.

NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.

**SO-DIMM
(REVERSE)**

PROJECT : CT8
Quanta Computer Inc.

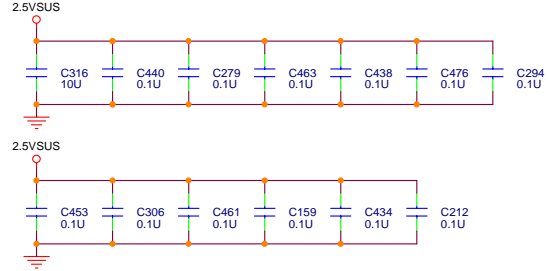
Size	Document Number	Rev
Custom	DDR NEAR SO-DIMM	1A
Date:	Thursday, April 14, 2005	Sheet 9 of 42



NOTE: BA2 is not used and it is left open.



Test point need place another side

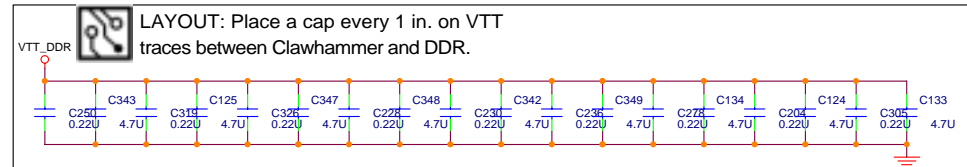
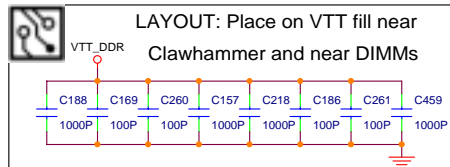
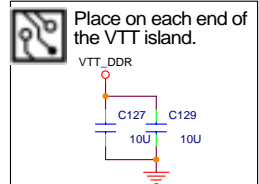
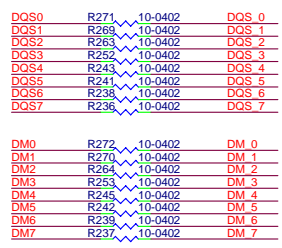
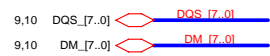
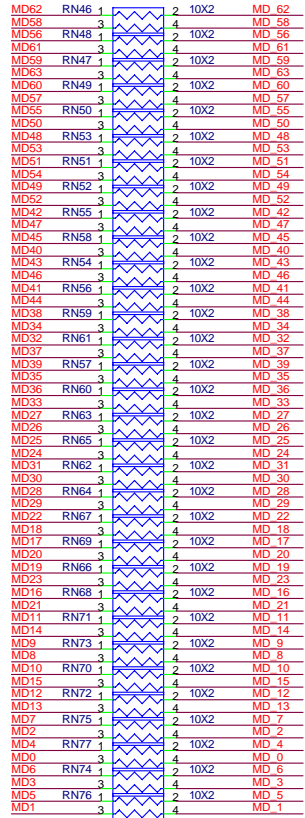
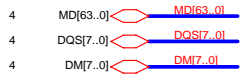


NOTE: VDDid is a no connect for 2.5V DDR SDRAM. It is only used for 3.3V SDRAM.

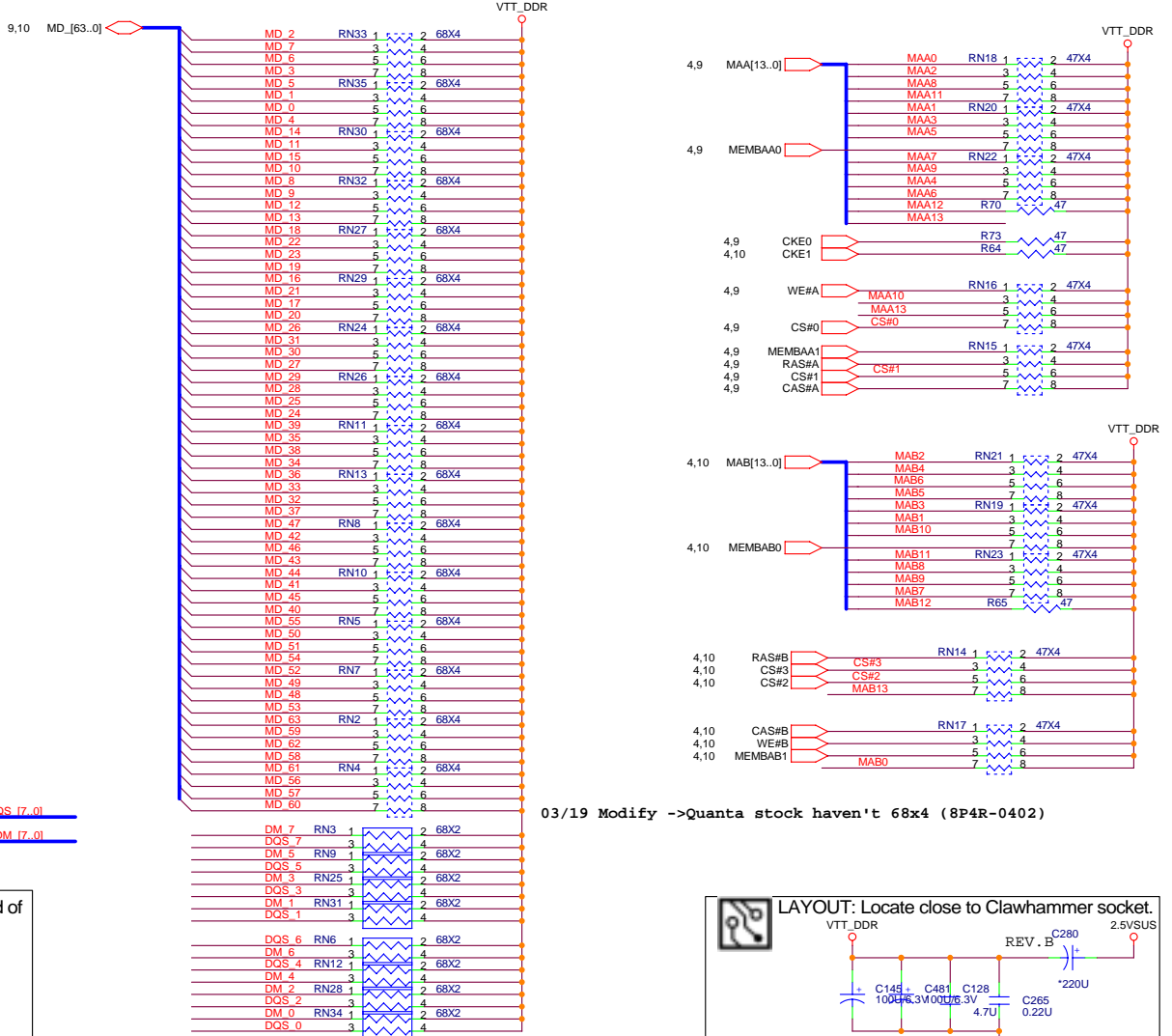
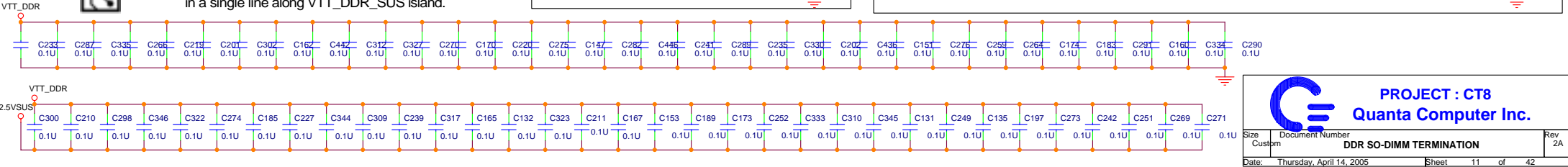
SO-DIMM (REVERSE)

NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.

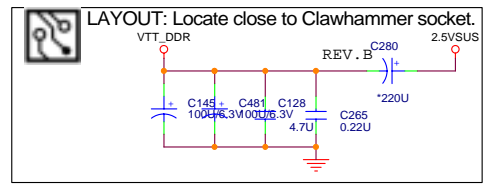
DDR



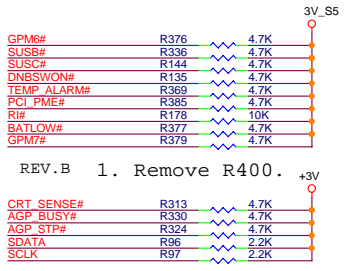
LAYOUT: Place alternating caps to GND and VDD_2.5V_SUS in a single line along VTT_DDR_SUS island.



03/19 Modify ->Quanta stock haven't 68x4 (8P4R-0402)



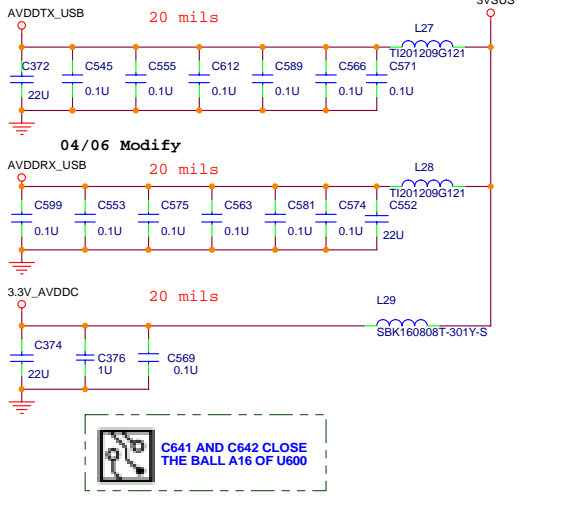
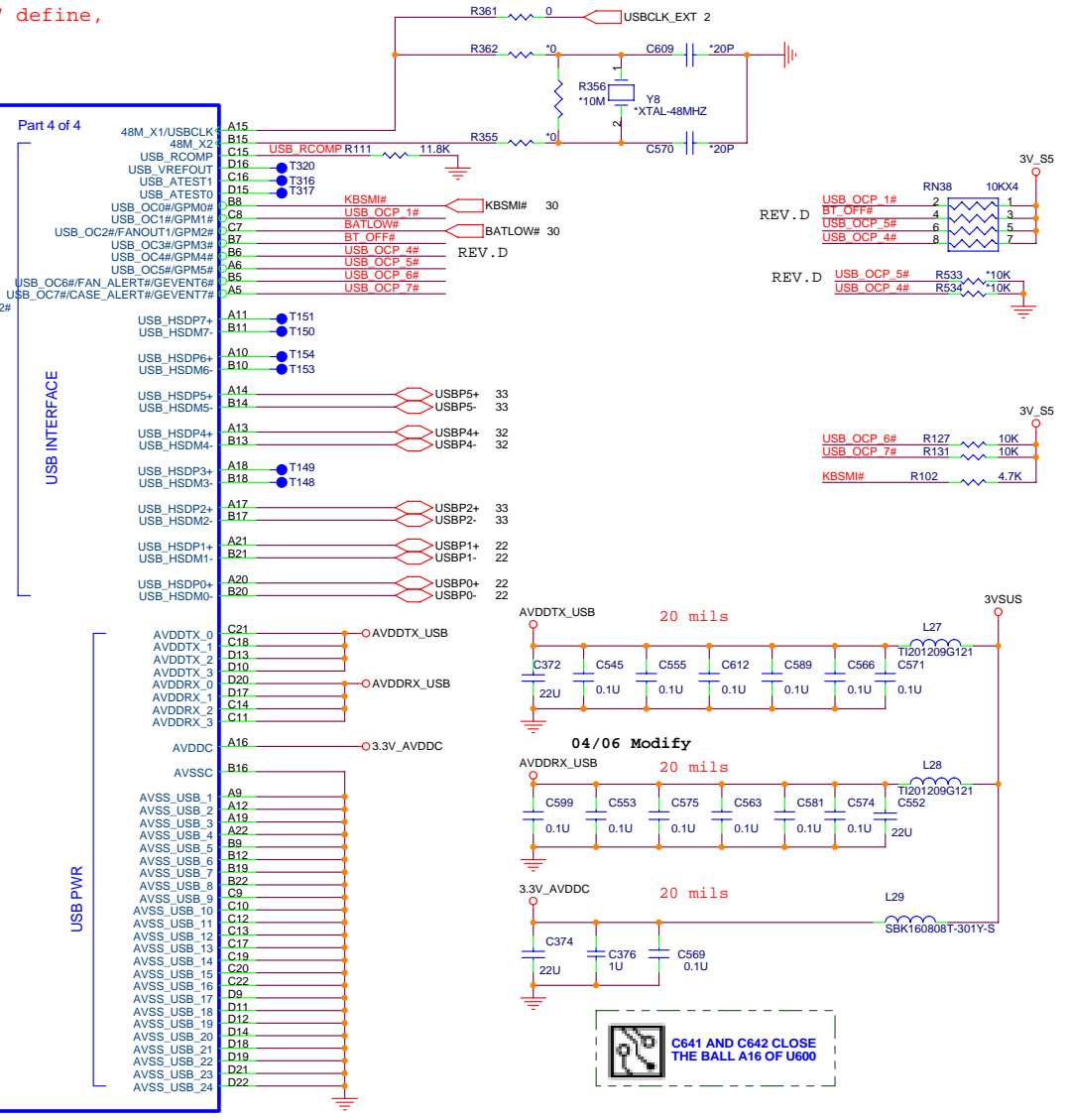
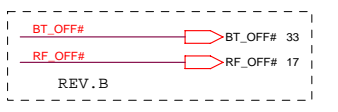
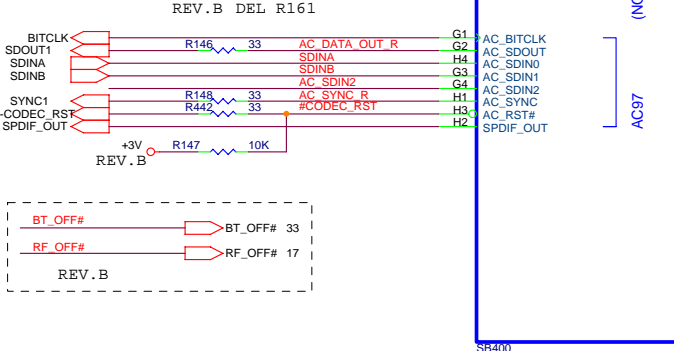
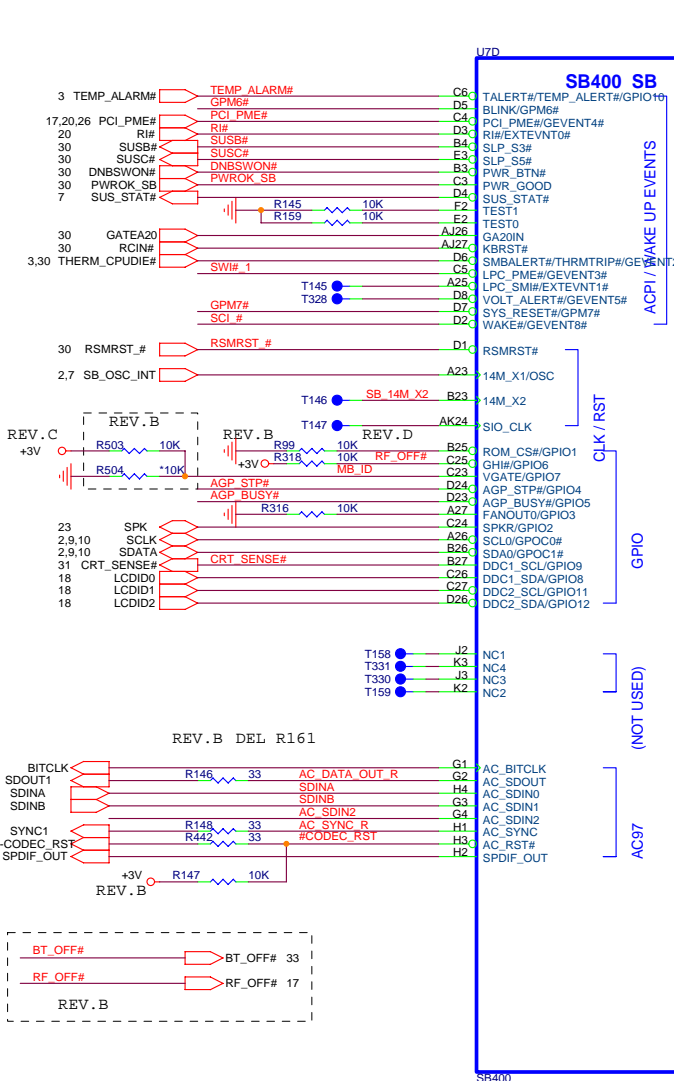
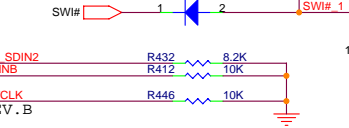
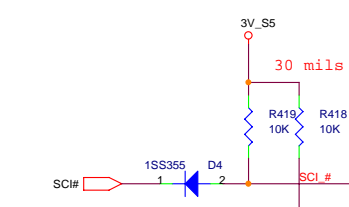
Please double check SB400 pin D5 & pin A27 define, because can't meet ATI library/symbols.

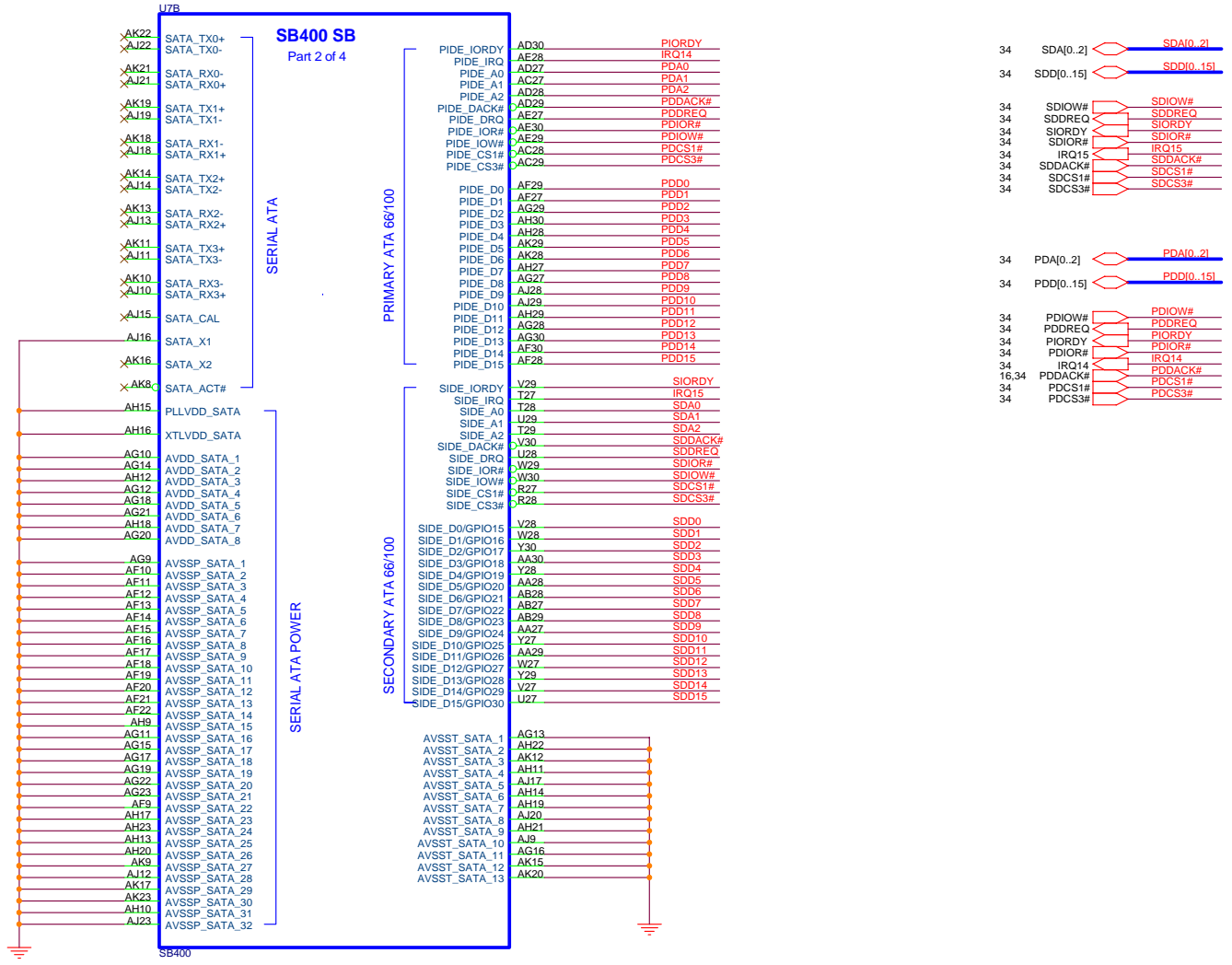


REV.B 1. Remove R400.



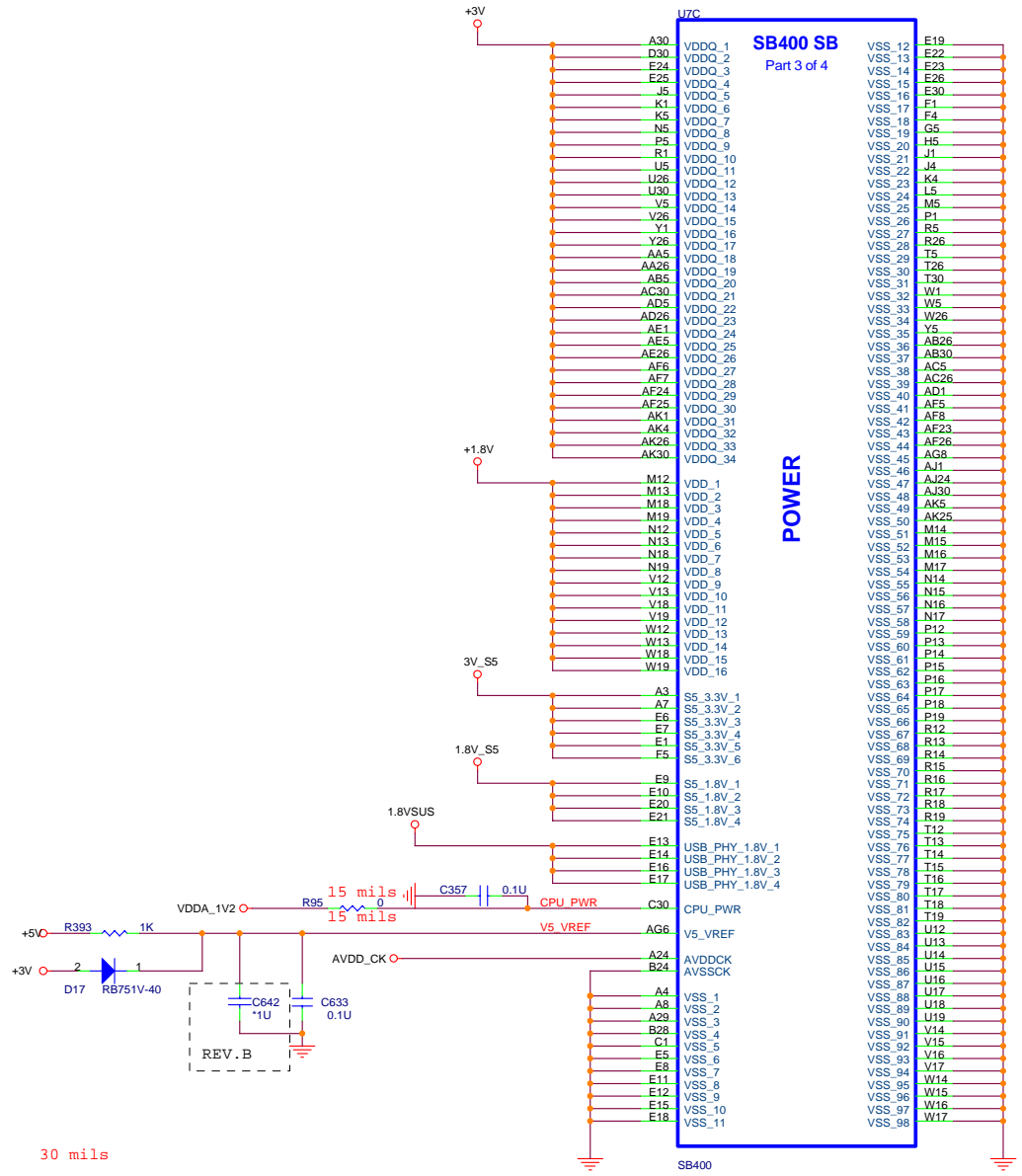
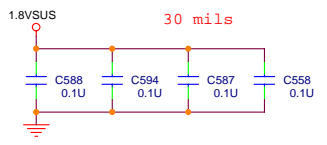
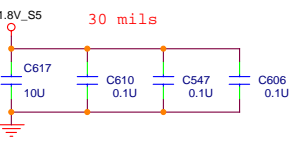
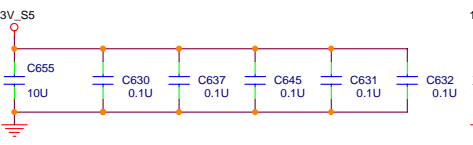
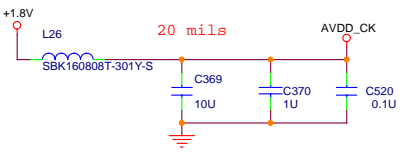
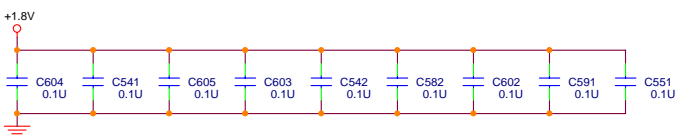
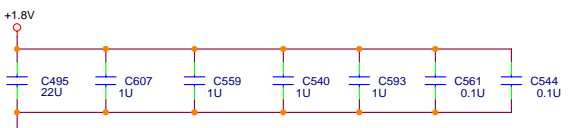
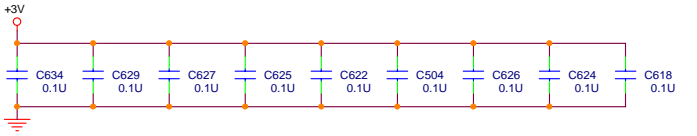
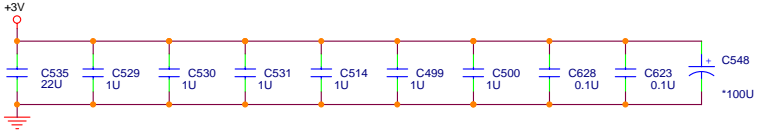
PWROK_SB is 33ms ~ 500ms after NB_PWRGD

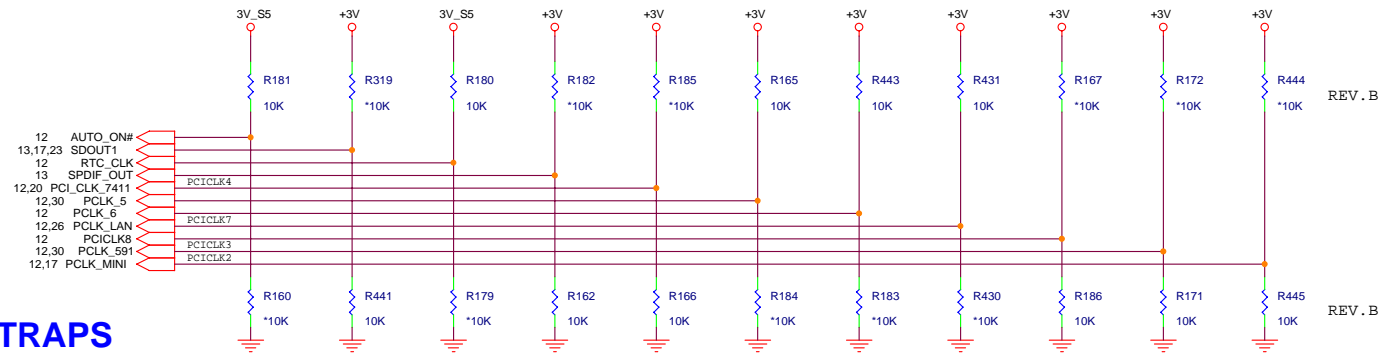






PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



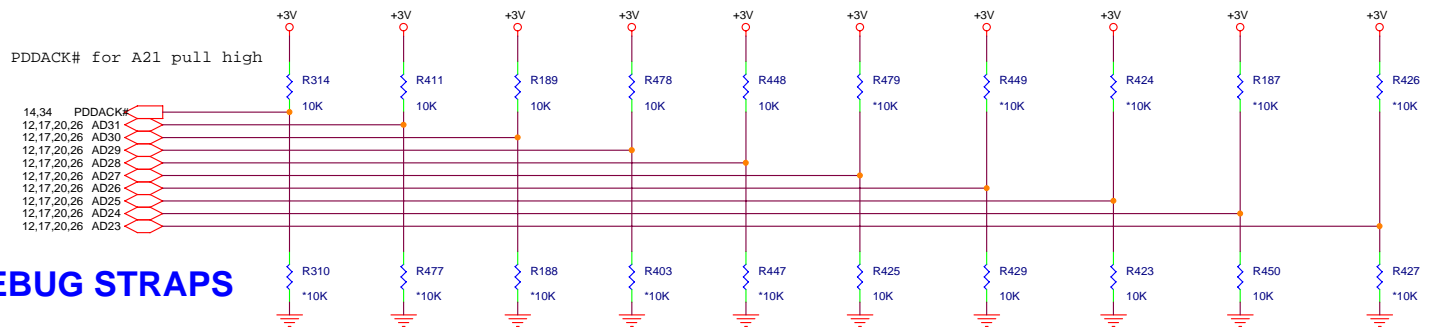


REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3
PULL HIGH	MANUAL PWR ON <i>DEFAULT</i>	USE DEBUG STRAPS	INTERNAL RTC <i>DEFAULT</i>	SIO 24MHz	48MHz OSC MODE <i>DEFAULT</i>	14MHz OSC MODE <i>DEFAULT</i>	CPU I/F = K8 <i>DEFAULT</i>	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM		USB PHY PWRDOWN DISABLE <i>DEFAULT</i>
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS <i>DEFAULT</i>	EXTERNAL RTC (NOT SUPPORTED W/ IT8712) <i>DEFAULT</i>	SIO 48MHz	48MHz XTAL MODE	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM		USB PHY PWRDOWN ENABLE

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

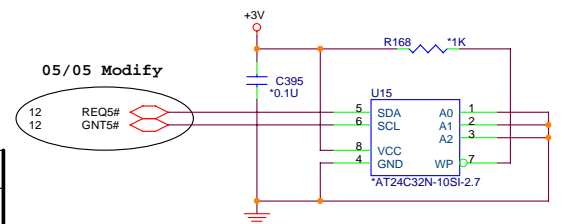
Need to check



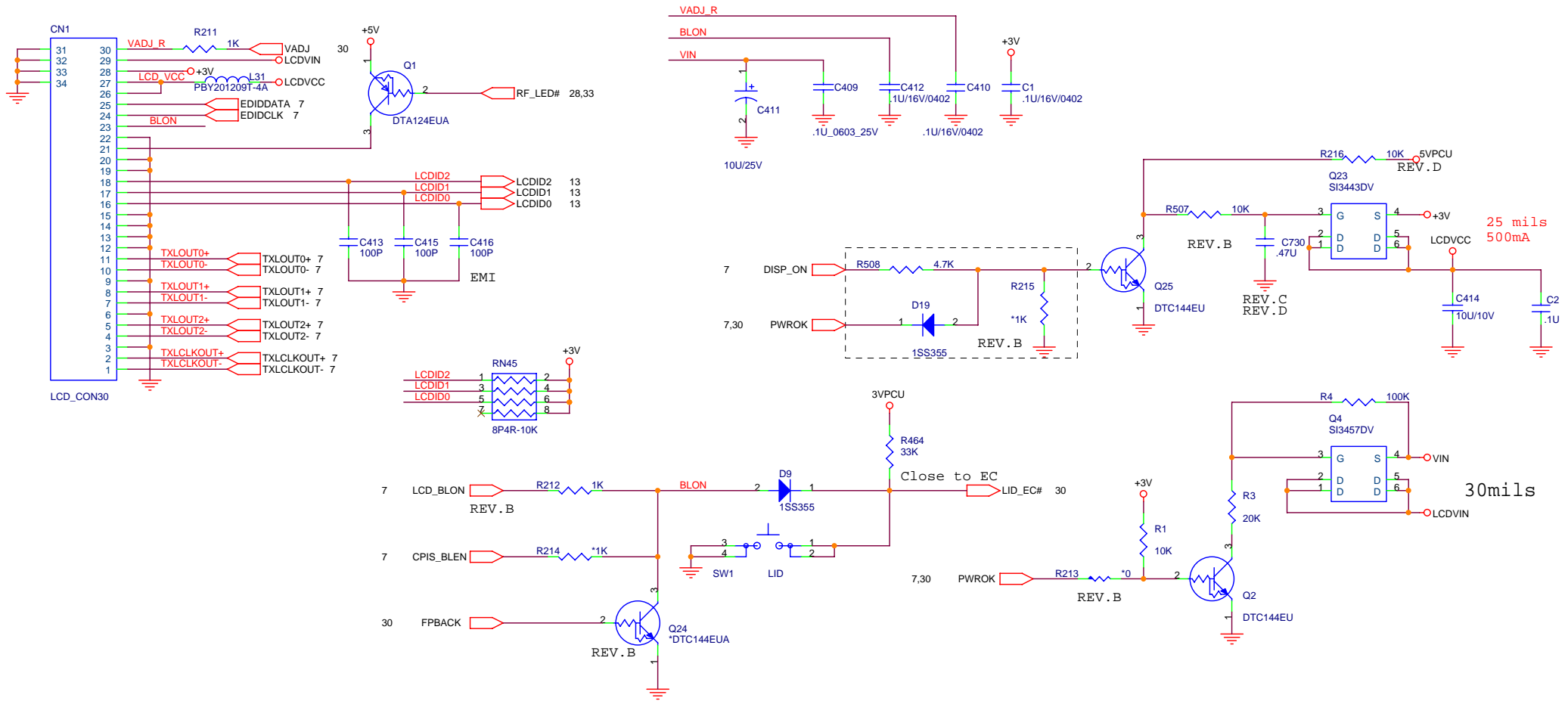
DEBUG STRAPS


	PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI <i>DEFAULT</i>	PLL CHARGE PUMP CTRL BIT 0 HI <i>DEFAULT</i>	PLL VCO CTRL BIT 1 HI <i>DEFAULT</i>	PLL VCO CTRL BIT 0 HI <i>DEFAULT</i>	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BY PASS USB PLL
PULL LOW	USE LONG RESET <i>DEFAULT</i>	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL <i>DEFAULT</i>	USE ACPI BCLK <i>DEFAULT</i>	USE IDE PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	USE USB PLL <i>DEFAULT</i>

Need to check



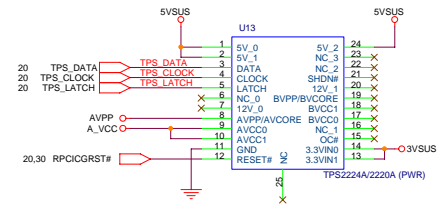
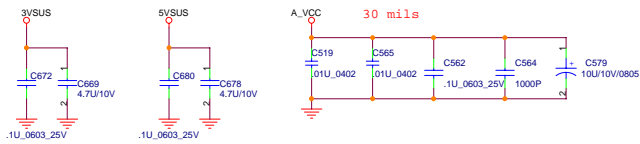
SB PCIE EEPROM STRAPS




PROJECT : CT8
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CardBus Connector



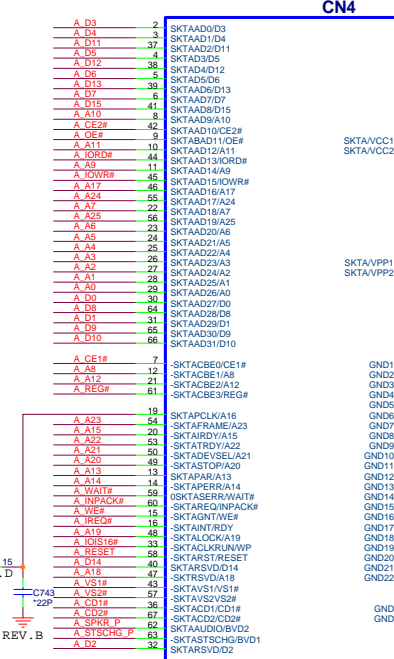
REV.B
REMOVE PCI1510 CIRCUIT AND PARTS.

U26-3	VCCB	D19	X
	VCCB	K19	X
B_CAD31/B_D10	B15	X	
B_CAD30/B_D9	A16	X	
B_CAD29/B_D11	B16	X	
B_CAD28/B_D8	A17	X	
B_CAD27/B_D0	C16	X	
B_CAD26/B_A0	D17	X	
B_CAD25/A1	C18	X	
B_CAD24/B_A2	D18	X	
B_CAD23/B_A3	E8	X	
B_CAD22/B_A4	F8	X	
B_CAD21/B_A5	G8	X	
B_CAD20/B_A6	H8	X	
B_CAD19/B_A25	H14	X	
B_CAD18/B_A7	H15	X	
B_CAD17/B_A24	G17	X	
B_CAD16/B_A17	K17	X	
B_CAD15/B_IOWR	K18	X	
B_CAD14/B_A8	L17	X	
B_CAD13/B_JORD	L18	X	
B_CAD12/B_A11	L19	X	
B_CAD11/B_OE	M17	X	
B_CAD10/B_CEE2	M18	X	
B_CAD9/B_A10	M19	X	
B_CAD8/B_D10	M14	X	
B_CAD7/B_D7	M15	X	
B_CAD6/B_D13	N15	X	
B_CAD5/B_D6	N16	X	
B_CAD4/B_D12	M13	X	
B_CAD3/B_D5	P15	X	
B_CAD2/B_D11	P16	X	
B_CAD1/B_D4	P17	X	
B_CAD0/B_D3	P18	X	
B_CCBE3/B_REG2	F15	X	
B_CCBE2/B_A12	G15	X	
B_CCBE1/B_A8	K14	X	
B_CCBE0/B_CET1	M14	X	
B_CPAR/B_A13	K13	X	
B_CFRAME/B_A23	G19	X	
B_CTRDY/B_A22	H13	X	
B_CIRDY/B_A16	J13	X	
B_CSTOP/B_A20	J17	X	
B_CDEVSL/B_A21	H19	X	
B_CBLOCK/B_A19	J19	X	
B_CSERRR/B_A14	J18	X	
B_CSERRR/B_WAIT	B18	X	
B_CREQA/B_INPACK	E18	X	
B_DGNT/B_WE	J15	X	
B_CSTSCHG/B_BVD1(STSCHG#)	F14	X	
B_CCLKRUN/B_WP(IOIS16)	A18	X	
B_CCLK/A16	H19	X	
B_CINT/B_READY(IREQ)	B19	X	
B_CRST/B_RESET	F17	X	
B_CAUDIO/B_BVD2(SPKR)	C17	X	
B_CCD1/B_CDI	N15	X	
B_CCD2/B_CDI	B17	X	
B_CVS1/B_VS1	C18	X	
B_CVS2/B_VS2	F19	X	
B_RSVD/B_D14	N17	X	
B_RSVD/B_D2	A15	X	
B_RSVD/B_A18	K15	X	

PCI7411GHK

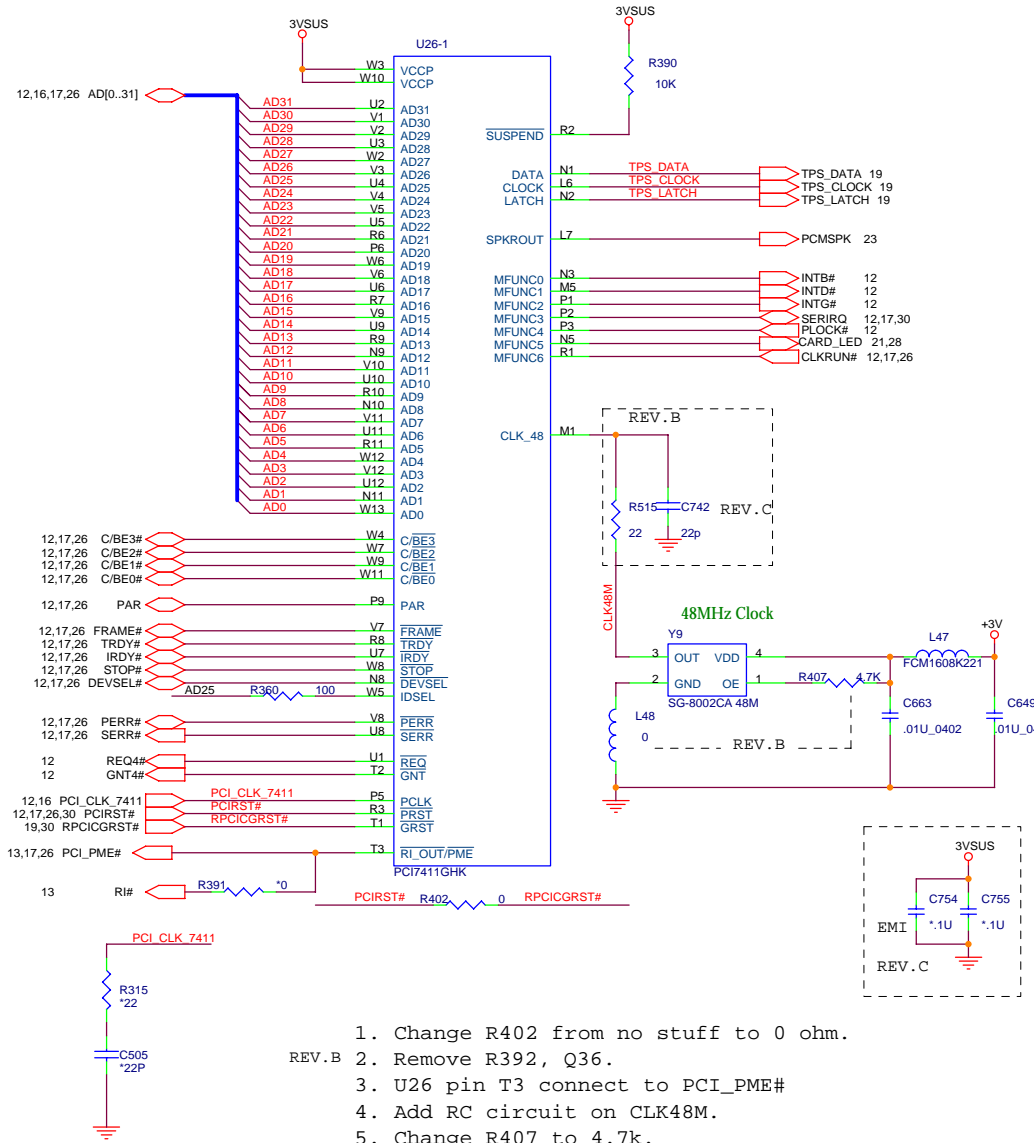
U26-2	VCCA	A5	X
	VCCA	A11	X
A_CAD31/A_D10	D1	A_D10	
A_CAD30/A_D9	D2	A_D1	
A_CAD29/A_D1	C2	A_D8	
A_CAD28/A_D8	B4	A_D0	
A_CAD27/A_D0	A4	A_A1	
A_CAD26/A_A0	E8	A_A2	
A_CAD25/A_A1	F8	A_A3	
A_CAD24/A_A2	G8	A_A4	
A_CAD23/A_A3	H8	A_A5	
A_CAD22/A_A4	C9	A_A6	
A_CAD21/A_A5	D9	A_A25	
A_CAD20/A_A6	E9	A_A24	
A_CAD19/A_A25	F9	A_A23	
A_CAD18/A_A7	A7	A_A24	
A_CAD17/A_A24	A10	A_A17	
A_CAD16/A_A17	A11	A_IOWR#	
A_CAD15/A_IOWR	G11	A_A9	
A_CAD14/A_A8	A_A7	A_IORD#	
A_CAD13/A_JORD	B11	A_A1	
A_CAD12/A_A11	C12	A_OE#	
A_CAD11/A_OE	A_A6	A_A25	
A_CAD10/A_CEE2	E12	A_D15	
A_CAD9/A_A10	F12	A_D13	
A_CAD8/A_D15	G12	A_D7	
A_CAD7/A_D7	A_A3	A_D5	
A_CAD6/A_D13	A_A4	A_D1	
A_CAD5/A_D6	A_A2	A_D0	
A_CAD4/A_D12	A_A0	A_D9	
A_CAD3/A_D5	A_A1	A_D8	
A_CAD2/A_D11	A_D0	A_D1	
A_CAD1/A_D4	A_D9	A_D10	
A_CAD0/A_D3	A_D10	A_D10	
A_CCBE3/A_REG2	C5	A_REG#	
A_CCBE2/A_A12	F9	A_A12	
A_CCBE1/A_A8	B10	A_A8	
A_CCBE0/A_CET1	C12	A_CET#	
A_CPAR/A_A13	G10	A_A13	
A_CFRAME/A_A23	C8	A_A23	
A_CTRDY/A_A22	A8	A_A22	
A_CIRDY/A_A16	B8	A_A15	
A_CSTOP/A_A20	A9	A_A20	
A_CDEVSL/A_A21	C9	A_A21	
A_CBLOCK/A_A19	E10	A_A19	
A_CSERRR/A_A14	F10	A_A14	
A_CSERRR/A_WAIT	B3	A_WAIT#	
A_CREQA_INPACK#	E7	A_INPACK#	
A_DGNT/A_WE	B8	A_WE#	
A_CSTSCHG/A_BVD1(STSCHG#)	C2	A_STSCHG_P	
A_CCLKRUN/A_WP(IOIS16)	E9	A_A16	
A_CCLK/A16	C4	A_IREQ#	
A_CINT/A_READY(IREQ)	A6	A_RESET	
A_CRST/A_RESET	A2	A_SPKR_P	
A_CAUDIO/A_BVD2(SPKR)	C15	A_CDI#	
A_CCD1/A_CDI	E6	A_CD2#	
A_CCD2/A_CDI	A3	A_VS1#	
A_CVS1/A_VS1	E8	A_VS2#	
A_CVS2/A_VS2	B13	A_D14	
A_RSVD/A_D14	D2	A_D2	
A_RSVD/A_D2	C10	A_A18	
A_RSVD/A_A18			

PCI7411GHK

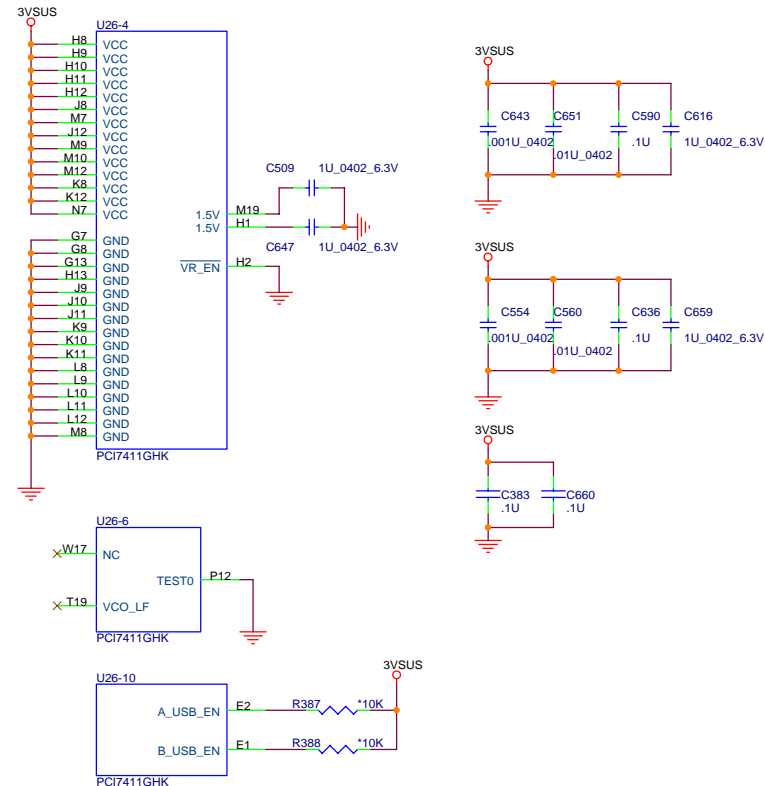


CARDBUS SLOT
FOX=WZ21131-G2

CardBus

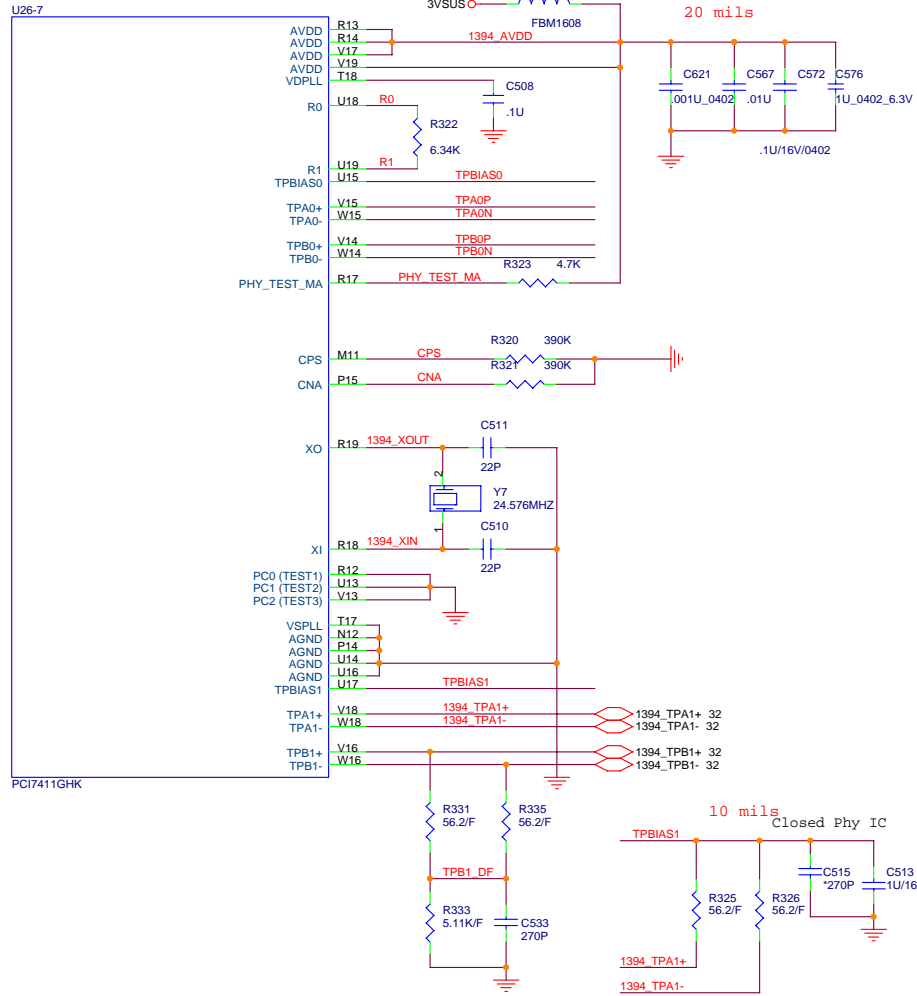


PCIXX21 Power Terminals

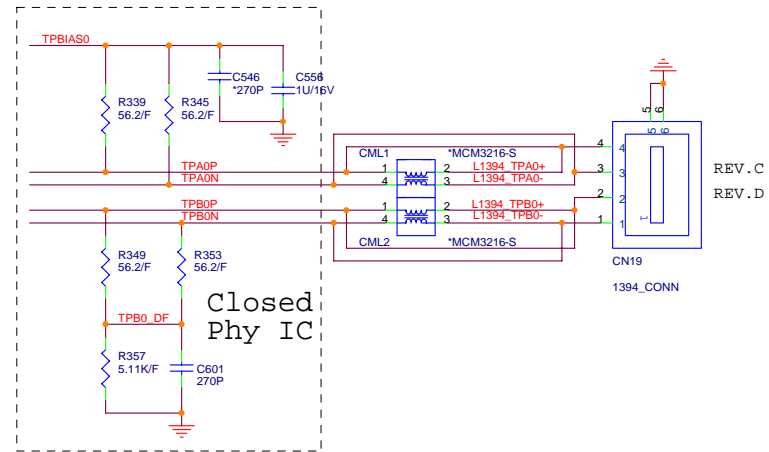


1. Change R402 from no stuff to 0 ohm.
- REV.B 2. Remove R392, Q36.
3. U26 pin T3 connect to PCI_PME#
4. Add RC circuit on CLK48M.
5. Change R407 to 4.7k.
6. Change L48 to 0 ohm.

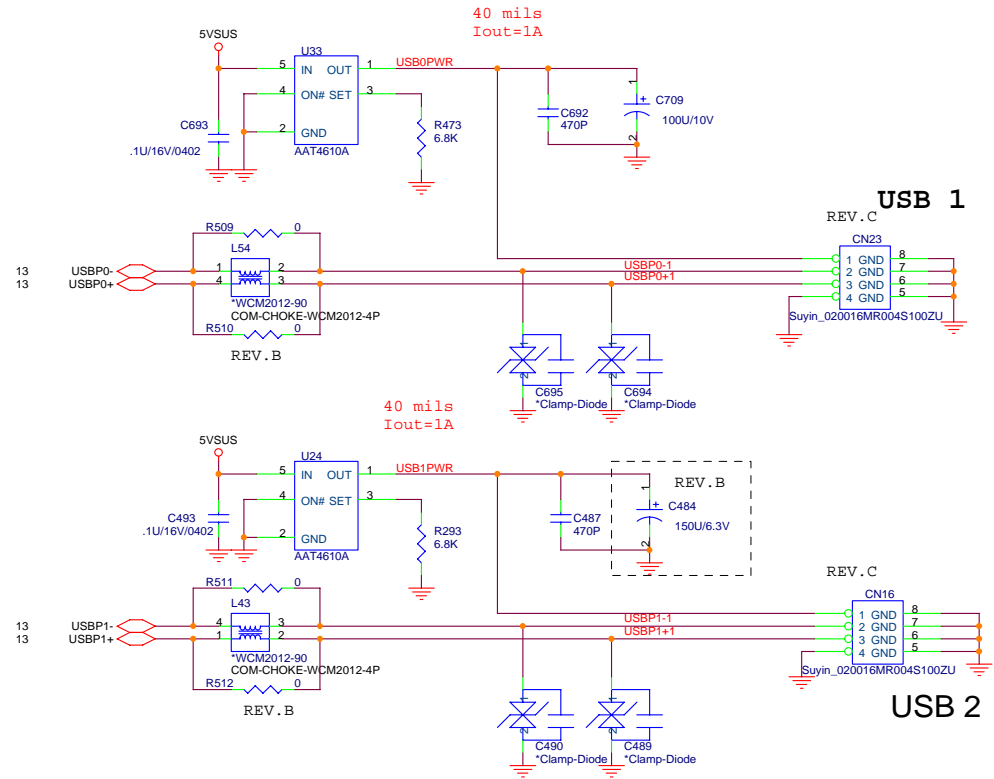
IEEE 1394a

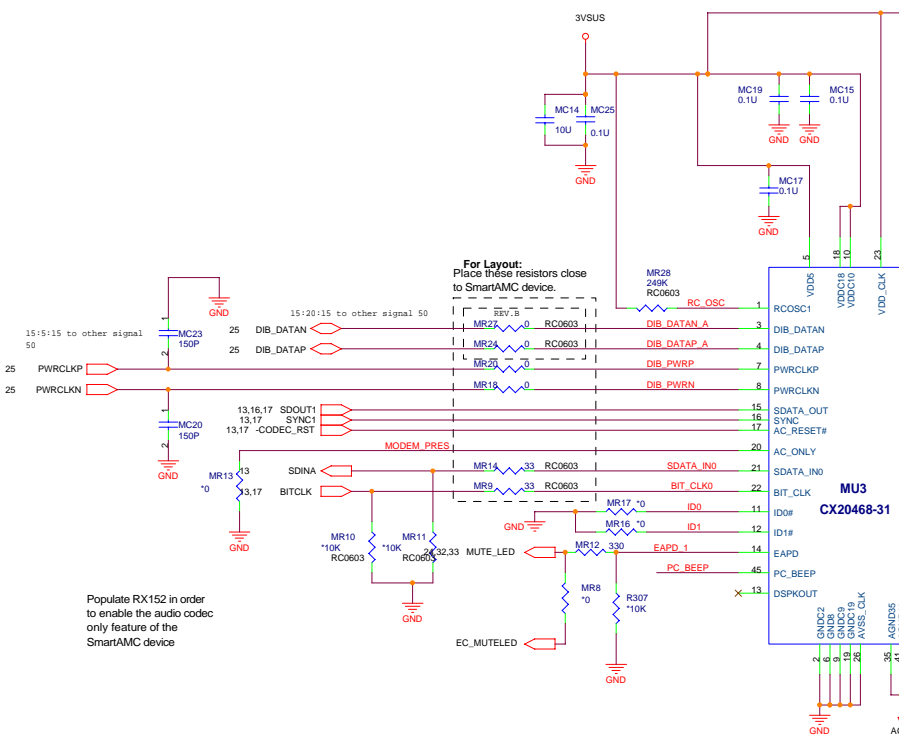


IEEE 1394 CONNECTOR



PCI7411GHK

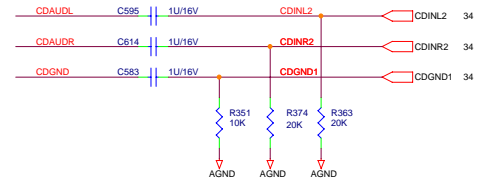




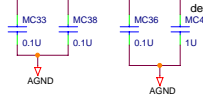
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

For Layout:
Place these resistors close to SmartAMC device.

FROM CD-ROM



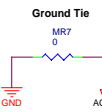
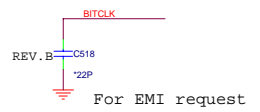
For Layout:
Place CX132, CX133, CX135, CX136 near SmartAMC device



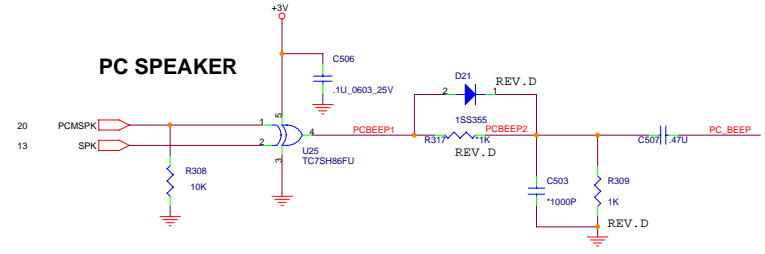
For Layout:

Place crystal and associated circuitry very near SmartAMC Device.

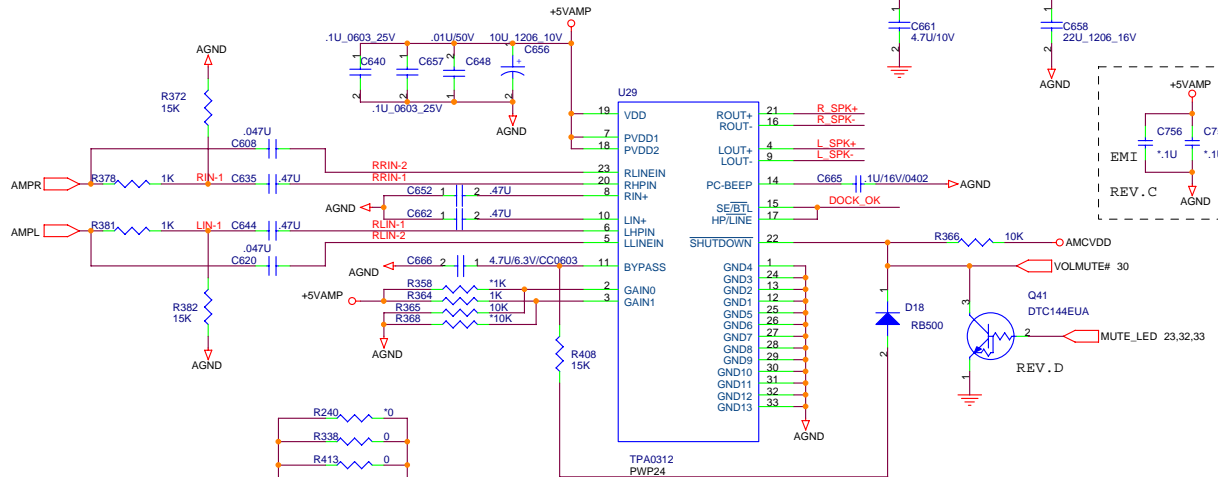
CX20468-21:	ADD R20, MR8 REMOVE MR12, R413, D24, MR30, MR31 REV:B SETTING
CX20468-31:	ADD MR12, R413, D24, MR30 REMOVE R20, MR31, MR8
CX20468-31 without software EQ:	ADD MR12, MR31, MR30 REMOVE R413, D24, MR8, R20



PC SPEAKER



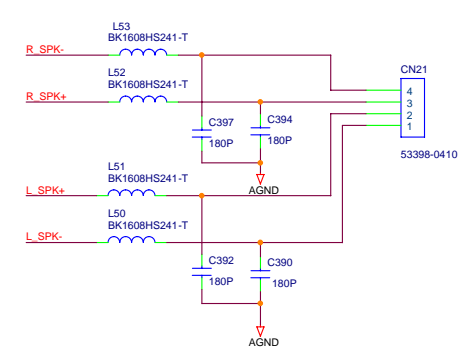
AUDIO AMPLIFIER



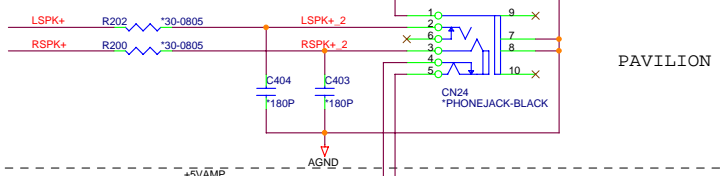
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV (inv)
0	0	6 dB	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT



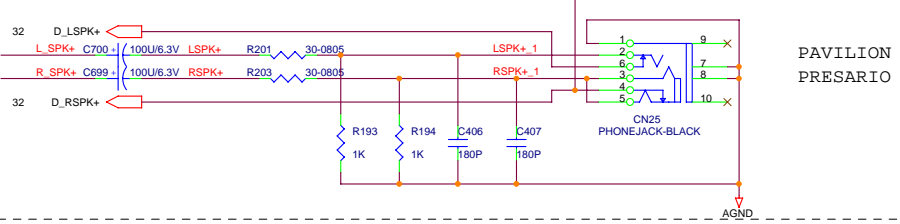
2ND HEADPHONE OUT



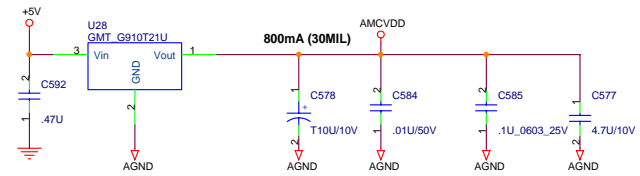
PAVILION

	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

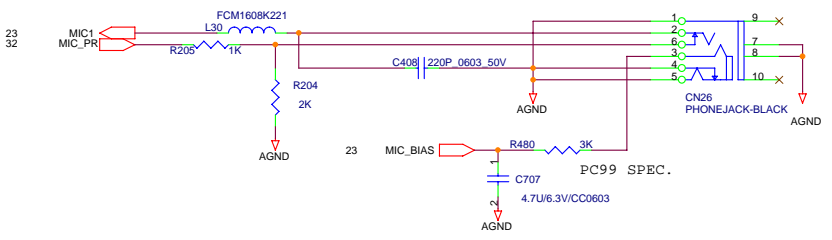
HEADPHONE OUT



PAVILION
PRESARIO



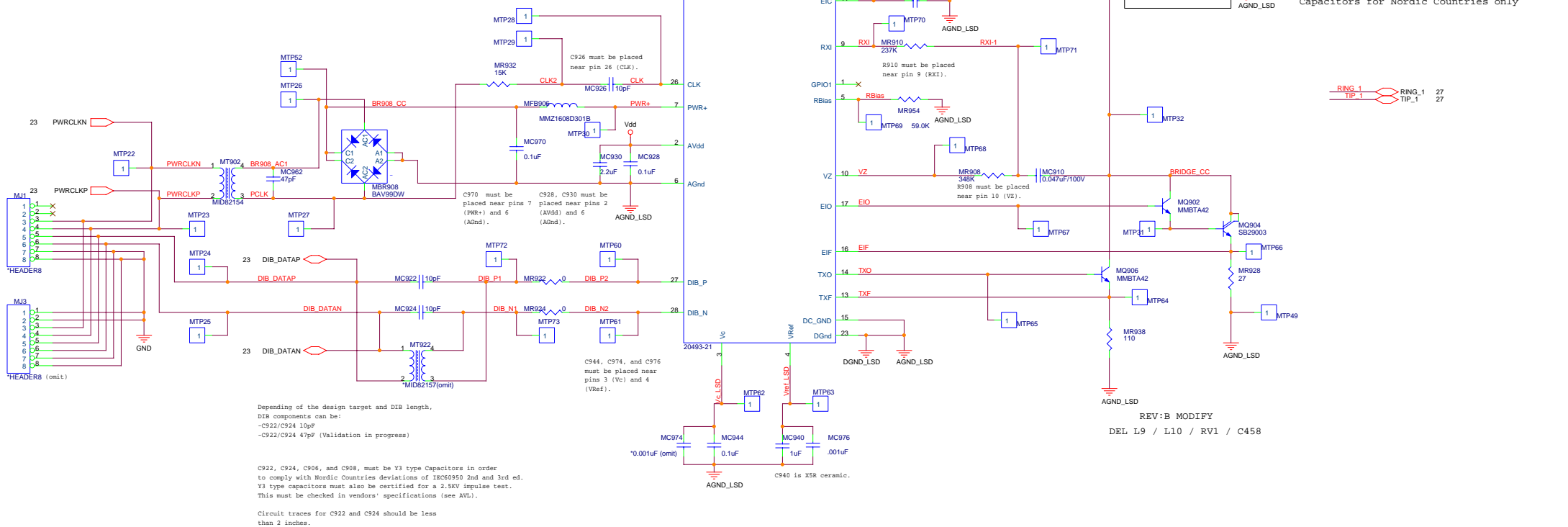
MICROPHONE



Revision History

REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators for MC986 from 3.3nF to 10nF, 100nF, +20%, V5V. By default, MC986 will be populated. Also, changed CX20493 revision from 11 to 21.	September 24, 2003
08	Changed MC986 from 3.3nF to 10nF, 100nF, +20%, V5V. By default, MC986 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

REV:B MODIFY FOR USE NEW MODEM MODULE



C906 and C908 must be Y3 type Capacitors for Nordic Countries only

Depending of the design target and DIB length, DIB components can be:
 -C922/C924 10pF
 -C922/C924 47pF (Validation in progress)

C922, C924, C906, and C908, must be Y3 type Capacitors in order to comply with Nordic Countries deviations of IEC60950 2nd and 3rd ed. Y3 type capacitors must also be certified for a 2.5KV impulse test. This must be checked in vendors' specifications (see AVL).

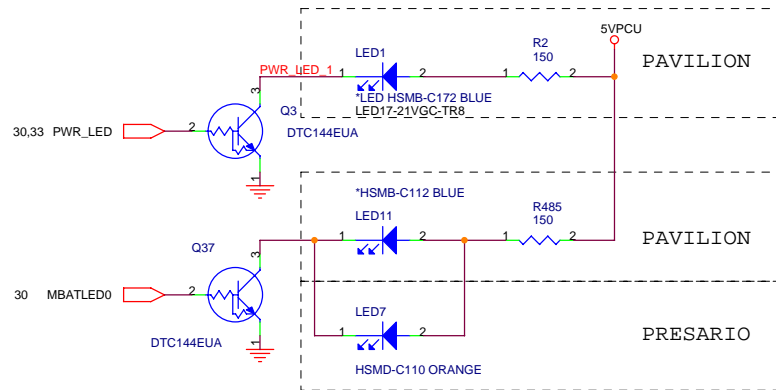
Circuit traces for C922 and C924 should be less than 2 inches.

C970 must be placed near pins 7 (PWR+) and 6 (AGnd).
 C928, C930 must be placed near pins 2 (AVdd) and 6 (AGnd).
 C944, C974, and C976 must be placed near pins 3 (Vc) and 4 (VRef).
 C940 is X5R ceramic.

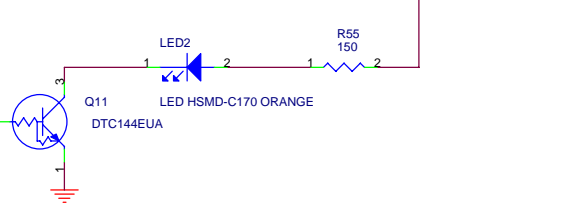
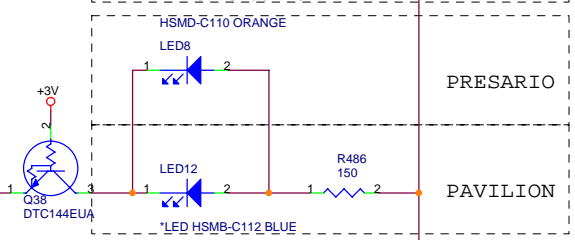
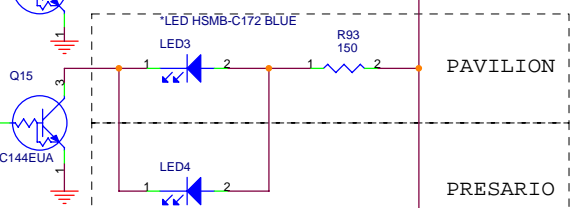
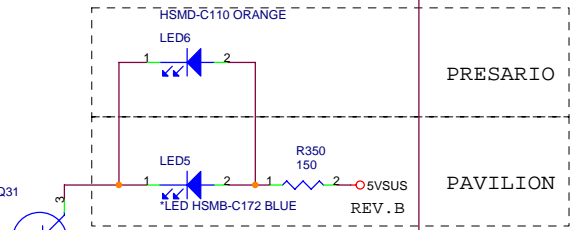
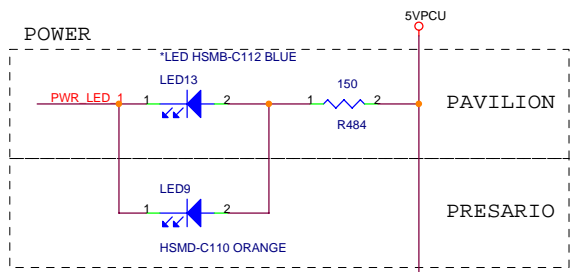
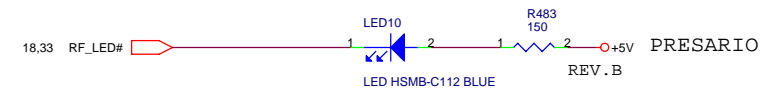
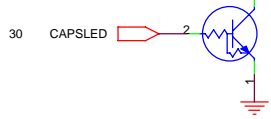
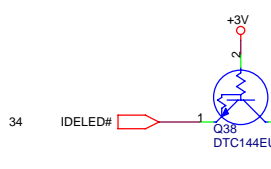
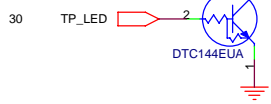
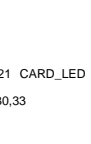
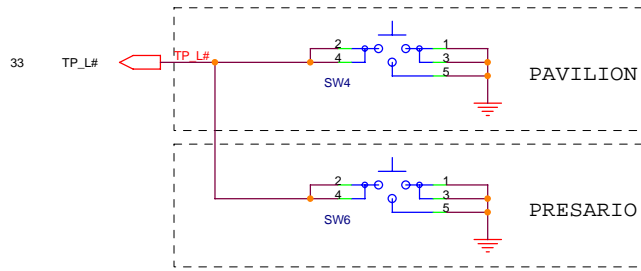
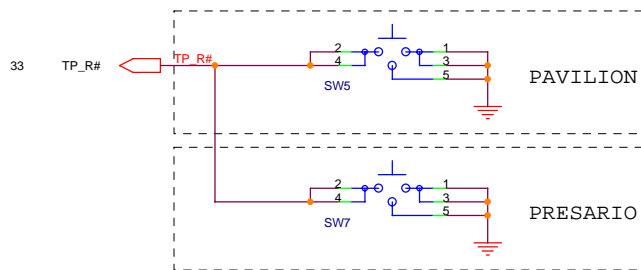
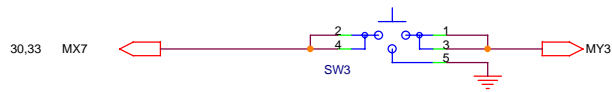
REV:B MODIFY
 DEL L9 / L10 / RV1 / C458

PROJECT : CT8
Quanta Computer Inc.

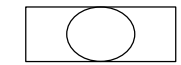
Size	Document Number	Rev
Custom	22--MODEM (DAA)	1A
Date: Thursday, April 14, 2005		Sheet 25 of 42



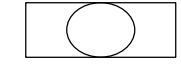
Touchpad control



LED HSMD-C170 ORANGE



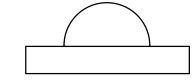
LED HSMB-C172 BLUE



LED HSMD-C110 ORANGE



LED HSMD-C112 BLUE

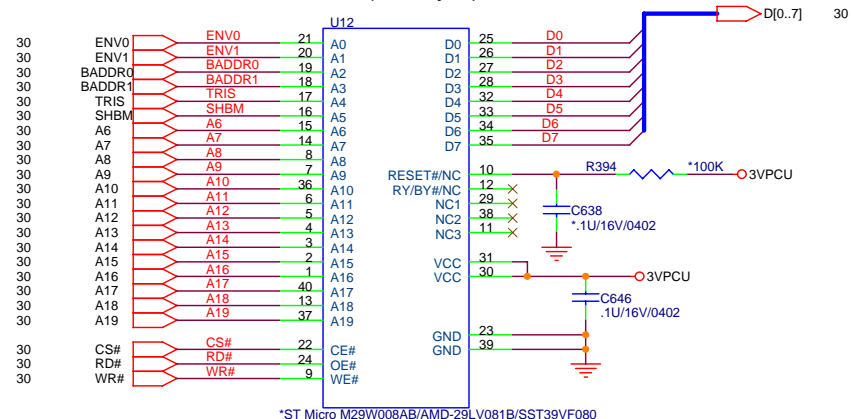


REV.B: LED7 AND LED8 SWAP

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom		2A
Date:	Thursday, April 14, 2005	Sheet 28 of 42

8Mbit (1M Byte), TSSOP40

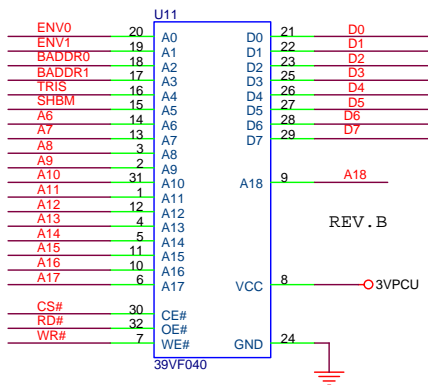


*ST Micro M29W008AB/AMD-29LV081B/SST39VF080

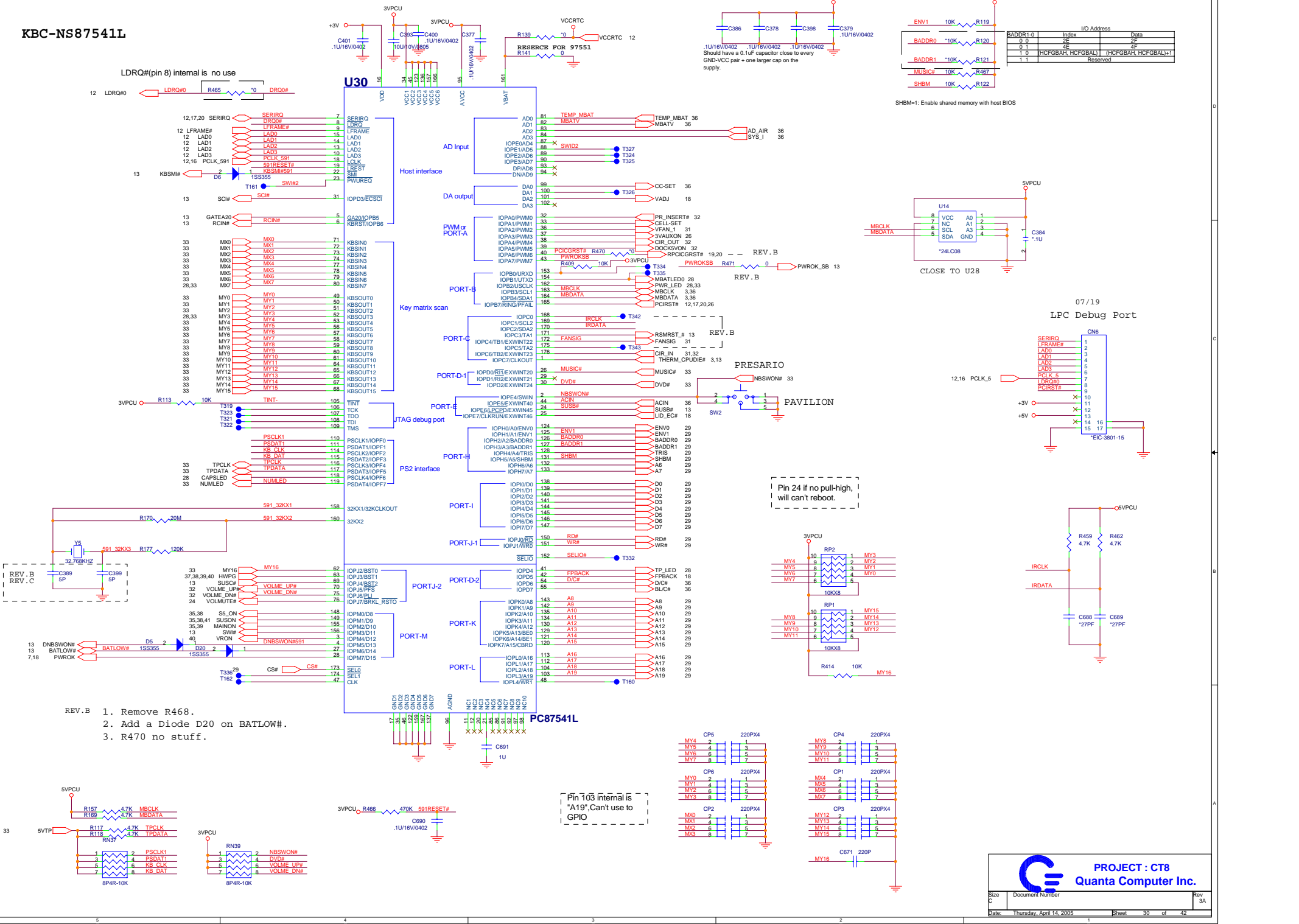
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100ms reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32



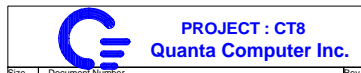
KBC-NS87541L

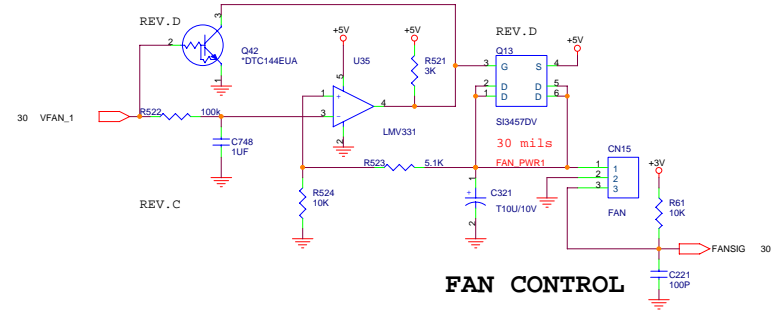
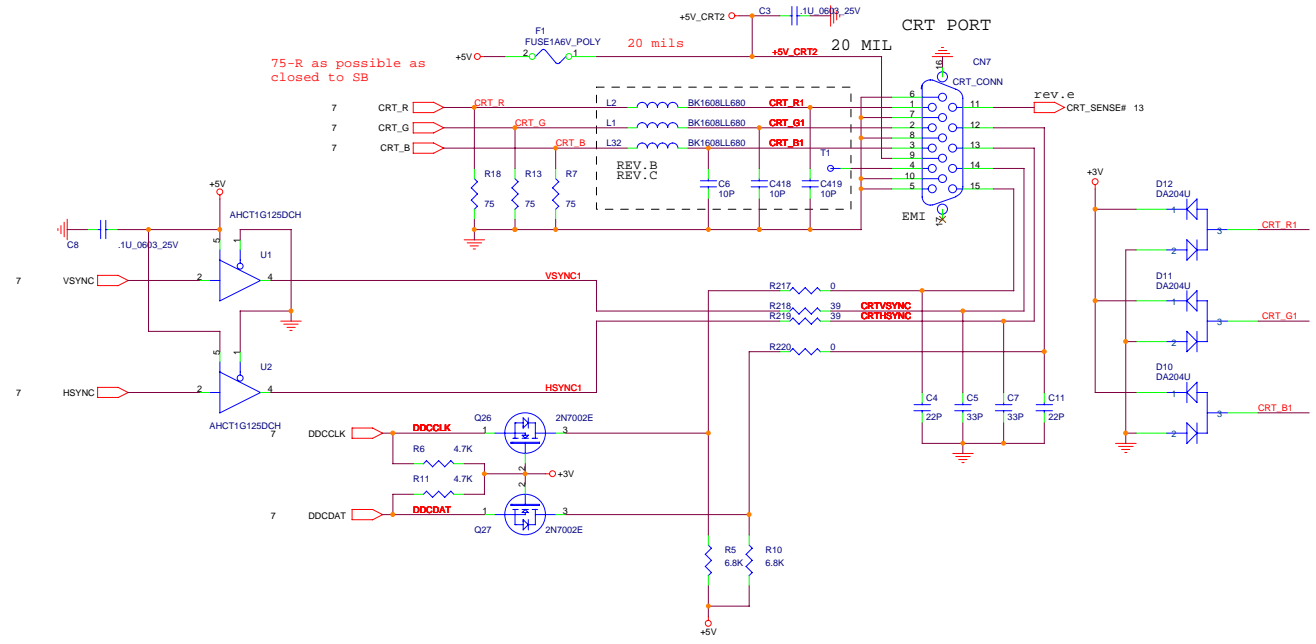
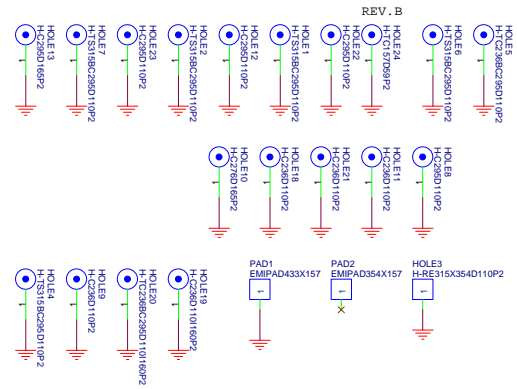
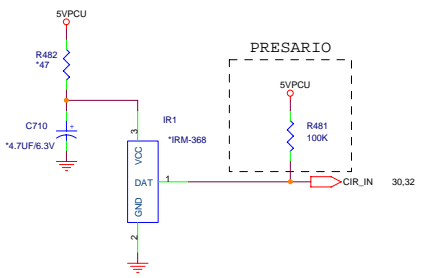


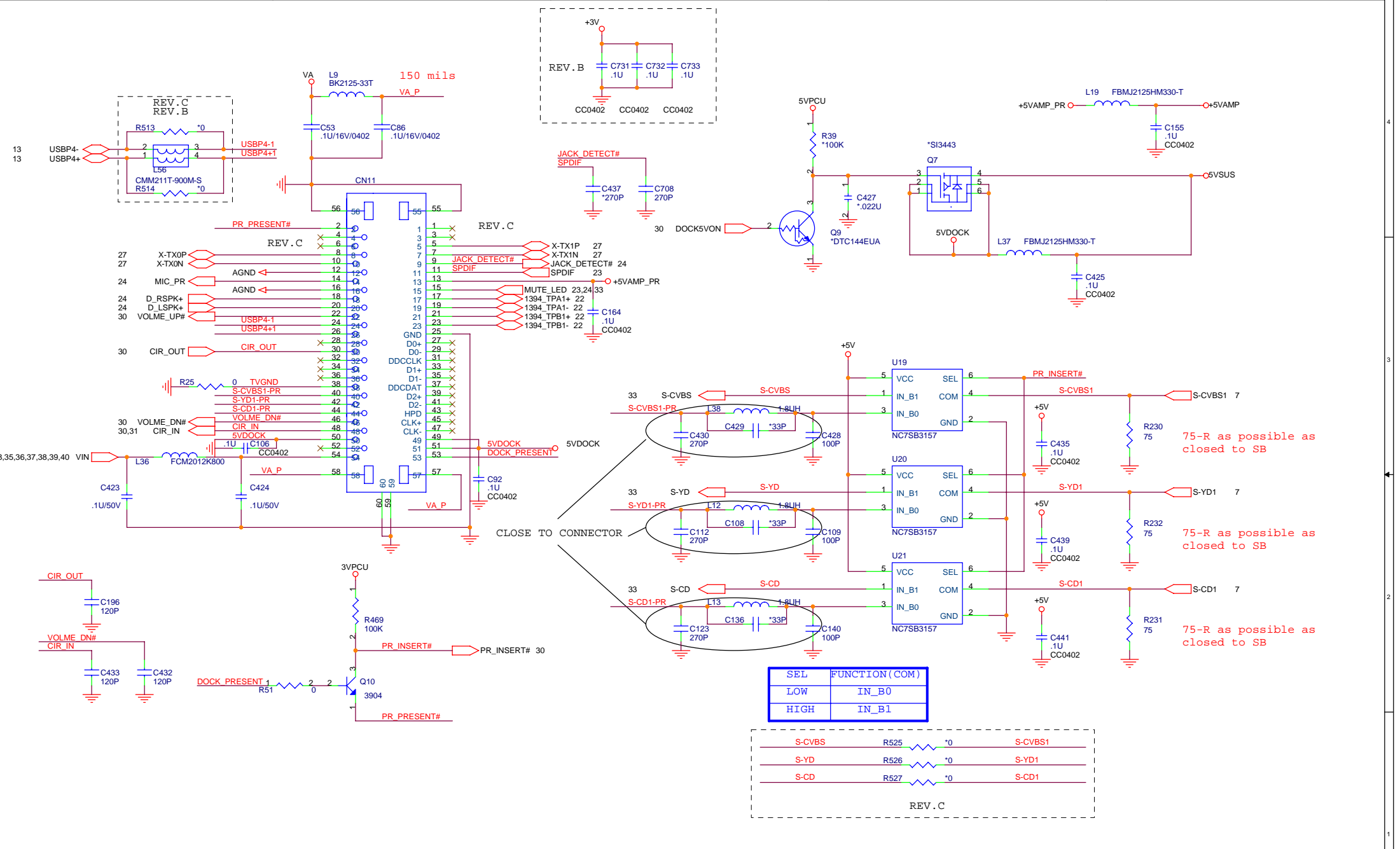
- REV. B
1. Remove R468.
 2. Add a Diode D20 on BATLOW#.
 3. R470 no stuff.

Pin 24 if no pull-high, will can't reboot.

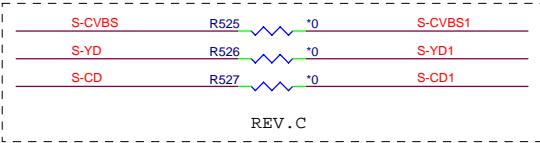
Pin 103 internal is "A19", Can't use to GPIO



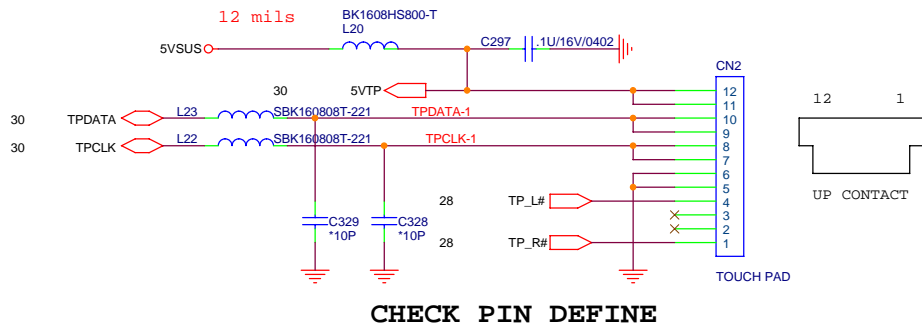




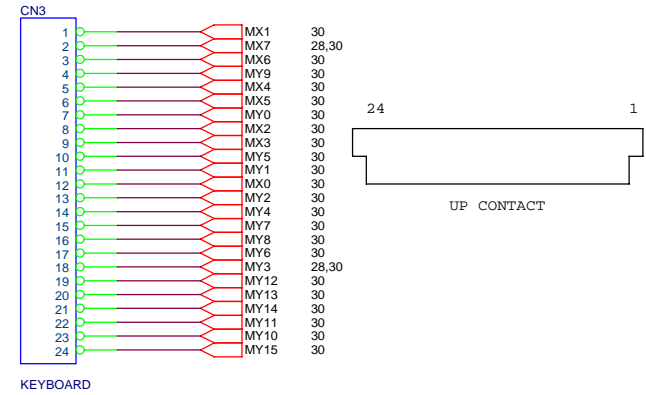
SEL	FUNCTION (COM)
LOW	IN_B0
HIGH	IN_B1



TOUCH PAD CONNECTOR



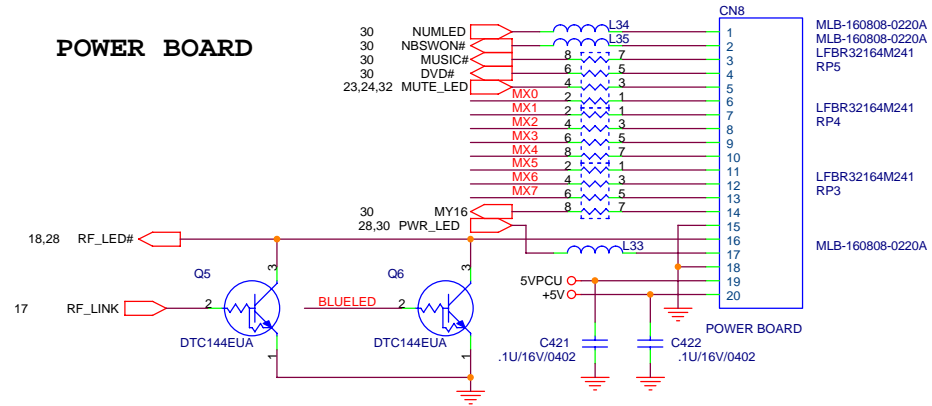
KEYBOARD CONNECTOR



AV BOARD

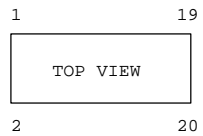
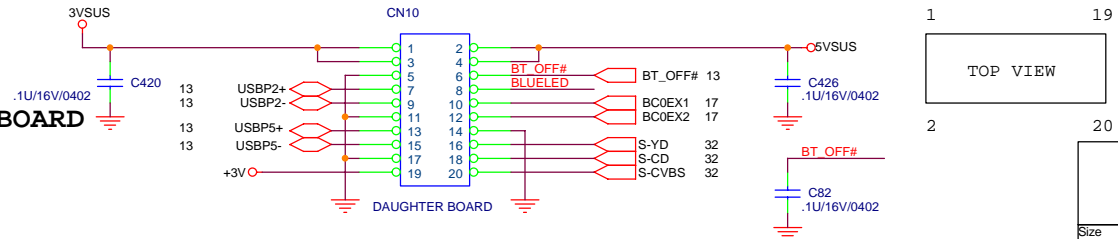
REV.B
DEL CN20, C681, C677, CC673

POWER BOARD



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARD	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD

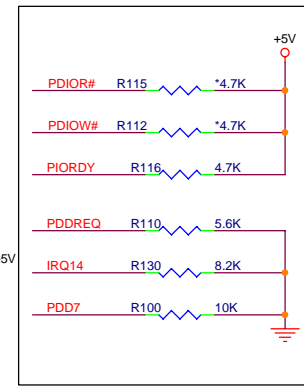
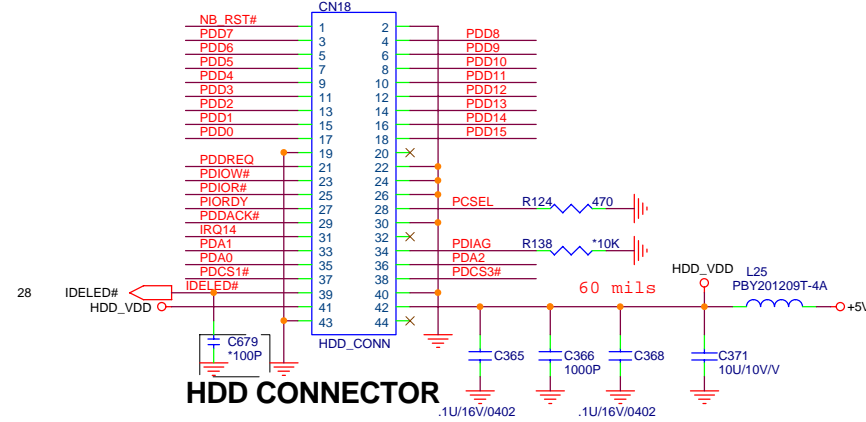
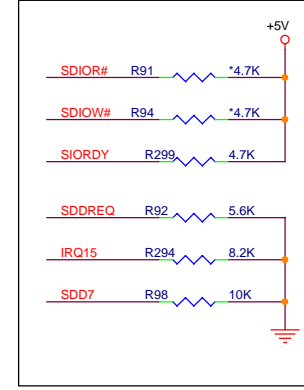
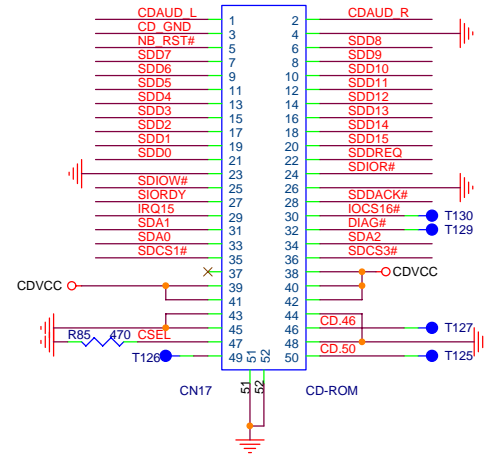
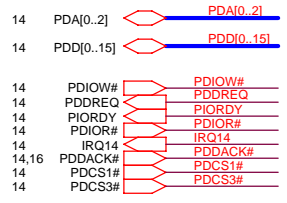
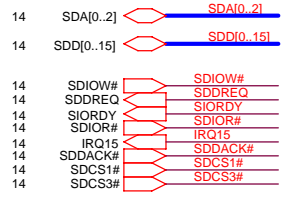
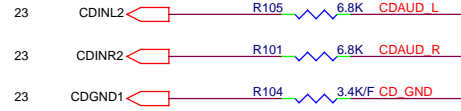
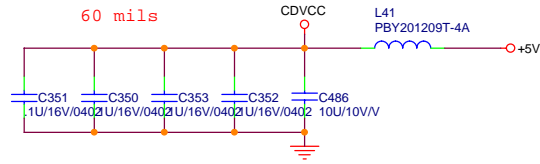



PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC	2A

Date: Thursday, April 14, 2005 Sheet 33 of 42

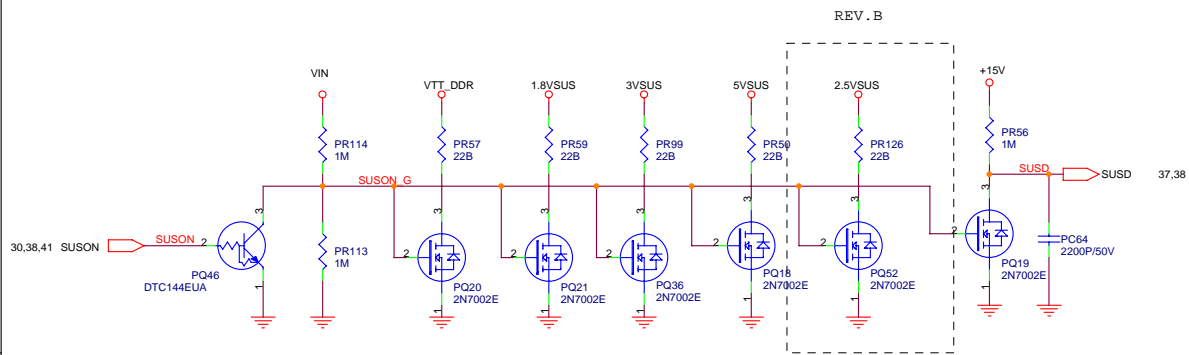
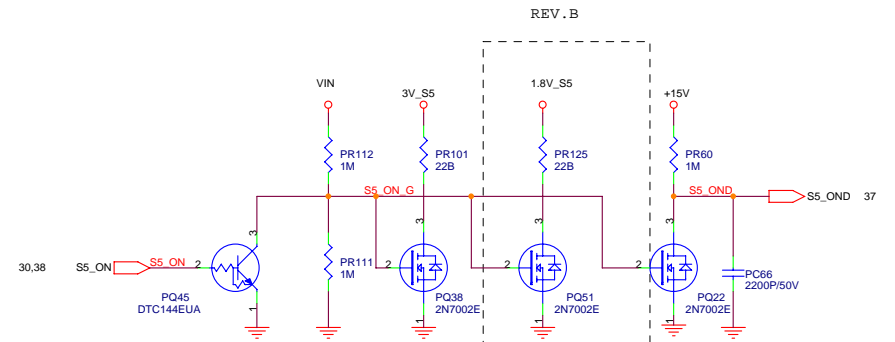
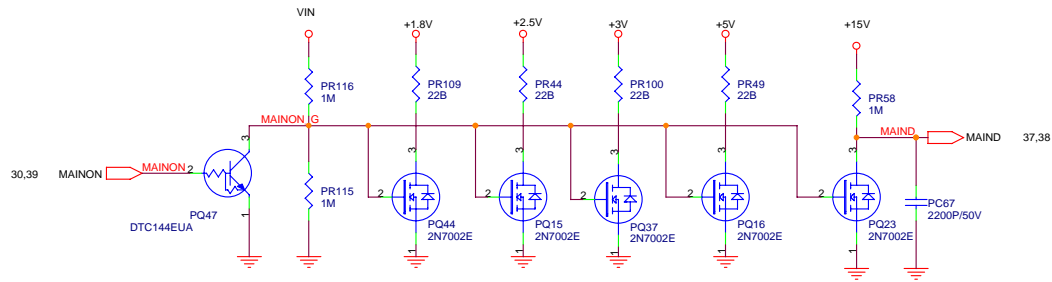
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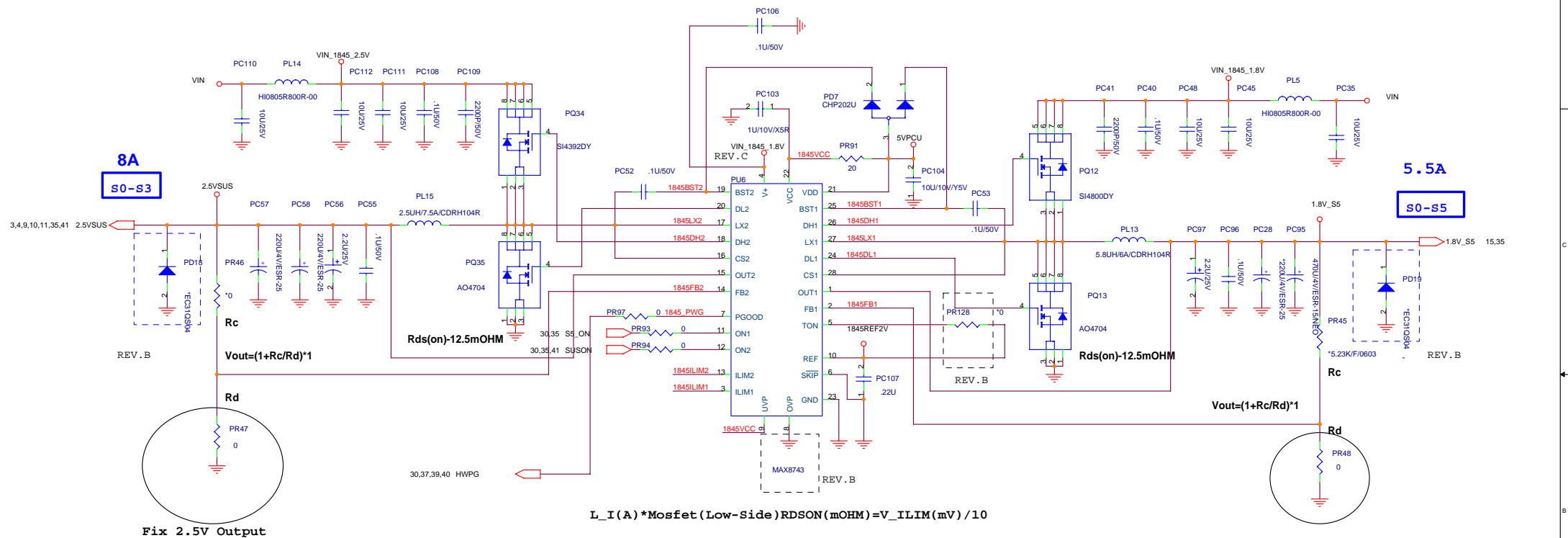




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Quanta Computer Inc.

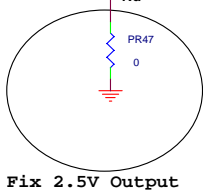
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Custom			
Date:	Thursday, April 14, 2005	Sheet	34 of 42



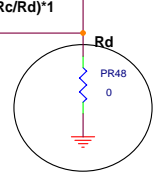


8A
S0-S3

5.5A
S0-S5

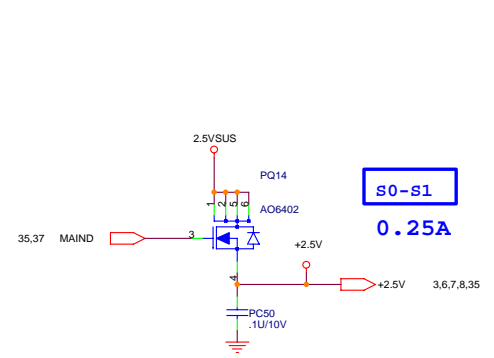


Fix 2.5V Output

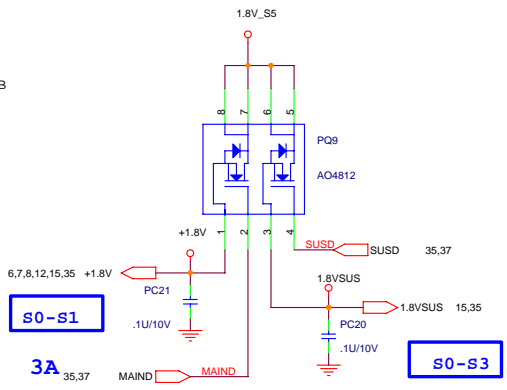


Fix 1.8V Output

$$L_I (A) * \text{Mosfet (Low-Side) RDSON (mOHM)} = V_ILIM (mV) / 10$$

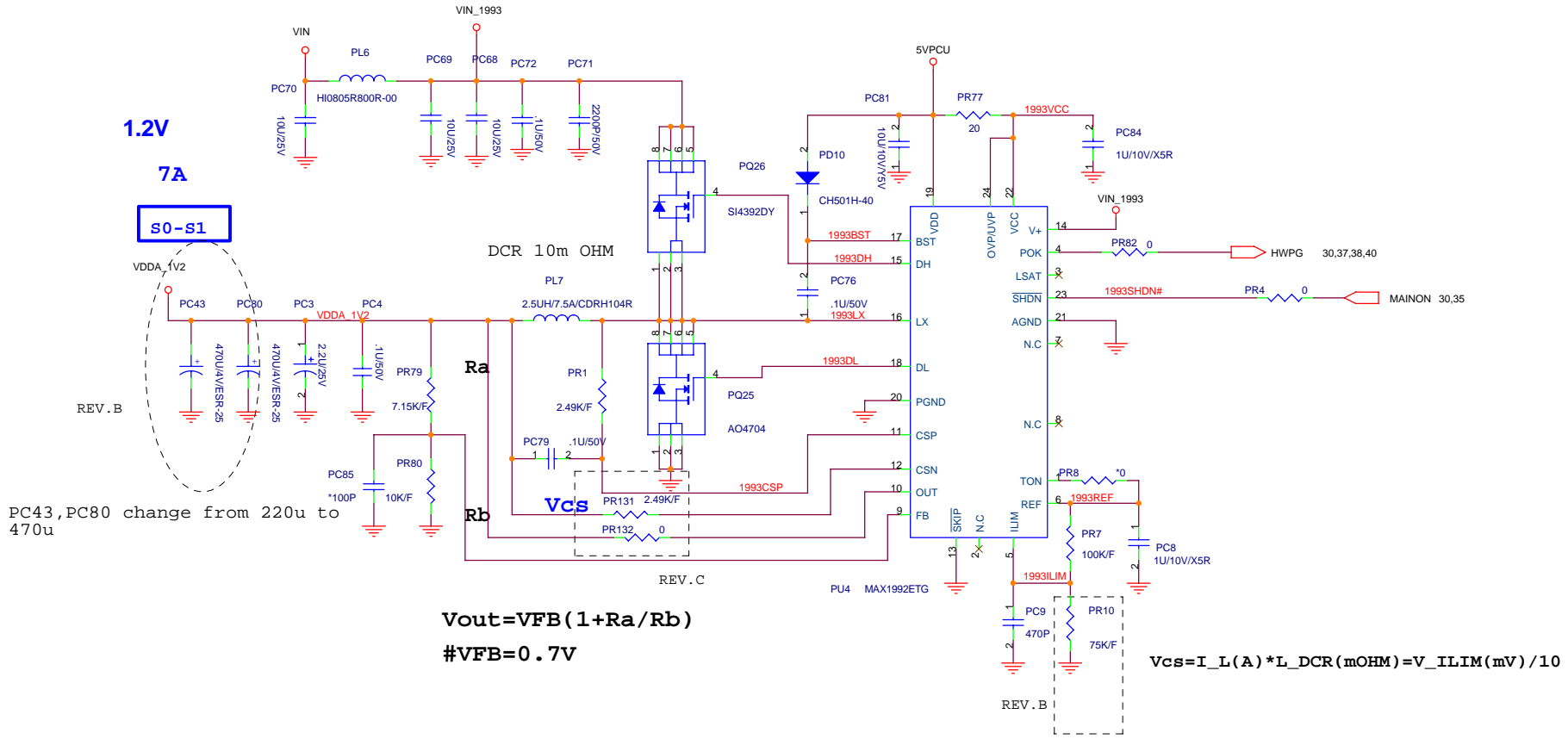


S0-S1
0.25A



S0-S1
3A

S0-S3
0.2A



1.2V

7A

S0-S1

REV. B

PC43,PC80 change from 220u to 470u

$$V_{out} = V_{FB} (1 + R_a / R_b)$$

$$\#V_{FB} = 0.7V$$

$$V_{cs} = I_L (A) * L_{DCR} (m\Omega) = V_{ILIM} (mV) / 10$$

MODEL	REV	CHANGE LIST		Model		CTS Mother Board
				Page	FROM TO	
CT8 M/B	1A	First Release				
	2A	PAGE 2 : 1. C330, C479 CHANGE VALUE FROM 33p TO 27p for meet 35ppm. 2. DEL R84 0ohm (don't need reserve).	PAGE22 : 1. C484 VALUE CHANGE FROM 100U TO 150U for USB power meet SPEC. 2. ADD R509, R510, R511, R512 FOR EMI.	1	1A	
		PAGE 3 : 1. ADD COM1 HPT CONNECTOR for AMD requirement. 2. ADD C721 100P, C722 4.7U, C723 3300P, C724 2.2U for high frequency decoupling. 3. Remove R386 Q33, connect U18 pin 6 to TEMP_ALARMH (no need level shift). 4. Change C311 from 10u to 100u and remove C304, that ensures VDD to VDDA power down sequence is met.	PAGE23 : 1. MCL3, MCL8 CHANGE VALUE FROM 33p TO 22p for tune clock range. 2. CHANGE MR24, MR27 FROM 1K TO 0ohm for Conexant requirement. 3. ADD SPDFIF 4. Del MR26 for meet PC99 SPEC. 5. Del C518 for tune BITCLK waveform.	2	3A	
PAGE 4 : 1. C148, C163 VALUE CHANGE FROM 330U TO 220U for Mechanic interference. 2. C225, C227 PART NUMBER CHANGE TO CH733LM812 for Mechanic interference. 3. R16 VALUE CHANGE FROM 10K TO 8.2K for ATI requirement.	PAGE26 : 1. ADD R502 15K pull low for tune ISOLATEB voltage. 2. R341 change 4.7K to 3.6K for REALTEK recommend. 3. Add C729 10u and C650 change value from 10u to 22u for REALTEK recommend. 4. Change C385 from 2200p to 3300p for tune 3VPCU drop level. 5. Add C736, C737, R438, C739 for EMI. 6. DEL R134 no need reserve, ADD Q40 for leakage current.	3	2A	3B		
2A	PAGE 5 : 1. R16 VALUE CHANGE FROM 10K TO 8.2K for ATI requirement.	PAGE27 : 1. U11 change package to TSSOP32 for Mechanic interference. 2. DEL R246, R249 for IG LAN.	4	3A	3B	
	PAGE 6 : 1. ADD C711-C720, C745-C747 0.1U FOR EMI 2. DEL R19 CHANGE R17 VALUE TO 4.7K FULL +1.8V for side-port memory is not used. 3. DEL R1 CIRCUI# because no need reserve is ATI requirement. 4. ADD C740, C741 FOR EMI.	PAGE28 : 1. R483 change signal from 5VPCU to +5V and R350 pull 5VSUS for leakage current. PAGE29 : 1. U11 change package to TSSOP32 for Mechanic interference. PAGE30 : 1. C389 8p, C399 5.6p change value to 15p for clock tolerance. 2. Del signal_BT_OFF#_RF_OFF# for HP implement guide. 3. ADD R471 and DEL R468, R470 for ATI power OK sequence. 4. Add D20 for EC leakage current.	5	2A		
2A	PAGE 7 : 1. ADD C711-C720, C745-C747 0.1U FOR EMI 2. DEL R19 CHANGE R17 VALUE TO 4.7K FULL +1.8V for side-port memory is not used. 3. DEL R1 CIRCUI# because no need reserve is ATI requirement. 4. ADD C740, C741 FOR EMI.	PAGE31 : 1. ADD HOLE24, AND D21 to C744 BOM NO STUFF for tune FAN clock. 2. CHANGE R464, L2, L32 TO BK1608LL680, C619, C419 TO 10P for CRT timing.	6	1A		
	PAGE 8 : 1. ADD L55 for VDDA_V2 frequency decoupling. 2. L15, L55 TH101209G121 CHANGE TO PBM12125HM330-T. 3. C290 VALUE CHANGE FROM 330U TO 220U for Mechanic interference.	PAGE32 : 1. ADD R513, R514 2, C731, C732, C733 FOR EMI. PAGE33 : 1. DEL CN26, C681, C677, C673 because no need AV function. PAGE35 : 1. ADD PR126, PR125, P051, P052 for 2.5VSUS and 1.8V_S5 discharge circuit. PAGE36 : 1. CHANGE PQ24 FROM SI4425 TO A04407, CHANGE PQ33 FROM A04411 TO A04407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add P053, PD17, PR127 PC144 for prevent AC discharge MOSFET damage when adapter over watt.	7	3A	3B	
2A	PAGE9 : 1. C290 VALUE CHANGE FROM 330U TO 220U for Mechanic interference. 2. Remove RTC charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function.	PAGE37 : 1. CHANGE PQ41 FROM A04704 TO A04702, CHANGE PR102 FROM 47.5K TO 80.6K, CHANGE PQ43 FROM SI4834 TO A04914 for Modify SVPCU OCP point.	8	2A		
	PAGE10 : 1. DEL R129, C391, C382, U9, D3, because no need reserve is ATI requirement. 2. Remove RTC charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function.	PAGE38 : 1. Change PWM IC from MAX1845 to MAX8743 to avoid negative voltage.Modify 2.5VSUS, 1.8V_S5 OCP point.	9	3A	3B	
2A	PAGE11 : 1. C290 VALUE CHANGE FROM 330U TO 220U for Mechanic interference.	PAGE39 : 1. CHANGE PR128 NO STUFF for adjust work frequency. 2. ADD PC80 change from 220u to 470u	10	1A		
	PAGE12 : 1. DEL R129, C391, C382, U9, D3, because no need reserve is ATI requirement. 2. Remove RTC charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function.	PAGE40 : 1. ADD PR124 15K, DEL PR70, PC2 for VR_ON signal add pull down resistor. 2. Change PR64 from 37.4k to 49.9k for update over current from 32A to 39A. PAGE41 : 1. Add R505, R506 and Change VSENSE from VTT_DDR to CPU_VTT_SENSE 2. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	11	2A	3B	
2A	PAGE13 : 1. CHANGE R99 for blue tooth on/off and R318 for wire less on/off function. 2. DEL R161 0ohm for BITCLK 3. ADD R503, R504 FOR F/F AND D/F. 4. CHANGE R147 PULL HIGH FROM 3V_S5 TO +3V for leakage current. and R446 contact to BITCLK because change net name.	PAGE42 : 1. Del R196, C402, no need reserve. 2. CHANGE R213 SIGNAL TO PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 3. Reserve R215 1K PULL DOWN 4. Add R507, R508, R509, D19 for ATI LCD back light bug.	12	3A	3B	
	PAGE14 : 1. Del C642 for meet IXP power on sequence. 2. Del R444 10K, Add R445 10K for ATI USB clock from outside. PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal.	PAGE43 : 1. ADD R516, R517, R518 for TI requirement. 2. Remove R397, D16, R489. 3. Add a Quick Switch U34 to isolate clock. 4. Change R501 to 0 ohm. 5. CN5 pin 35, 43 connect to the same net. 6. C725-C728 0.1U for power noise.	13	2A	3B	
2A	PAGE15 : 1. Del C642 for meet IXP power on sequence. 2. Del R444 10K, Add R445 10K for ATI USB clock from outside. PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal.	PAGE44 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	14	1A		
	PAGE16 : 1. Del R196, C402, no need reserve. 2. CHANGE R213 SIGNAL TO PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 3. Reserve R215 1K PULL DOWN 4. Add R507, R508, R509, D19 for ATI LCD back light bug.	PAGE45 : 1. Del 1G circuit, because no support 1G function.	15	3A	3B	
2A	PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal.	PAGE30 : 1. C89, C390 change value from 15p to 5p for frequency tolerance.	16	2A		
	PAGE18 : 1. Del R196, C402, no need reserve. 2. CHANGE R213 SIGNAL TO PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 3. Reserve R215 1K PULL DOWN 4. Add R507, R508, R509, D19 for ATI LCD back light bug.	PAGE31 : 1. Modify FAN circuit for diminish electronic magnetic noise. 2. Change L1, L2, L32 to BK1608LL680 for CRT waveform can meet SPEC.	17	3A	3B	
2A	PAGE19 : 1. DEL PCI1510 CIRCUI# AND PARTS. 2. ADD C743 for tune clock waveform. 3. R492 stuff for PCI reset timing. 4. Remove R392, Q36 and U26 pin T3 connect to PCI_PME# for PME timing. 5. Add R516, C742 circuit on CLK48M for tune clock waveform. 6. Change R197 to 4.7K for limit current. 7. Change L48 to 0 ohm for EMI. 8. ADD R494 47 ohm AND Q39 2N7002E for VCC_XD discharge. 9. CHANGE R487, R488, R490, R491, R492, R493, R495, R496, R497, R498, R499 VALUR FROM 0 TO 22 for signal waveform..	PAGE32 : 1. Del 1G signal. 2. Add R225, R526, R527 0ohm for option FF or DF TV. 3. Add common choke for USB.	18	3A	3B	
	PAGE20 : 1. Add D3 for meet SVTP SPEC. 2. Change C674, C675, C676, C683 value from 15p to 33p for EMI 3. C358, C359, C360, C361 change value from 0.1u to 0.01u for ATI PA_IXP400AC11. PAGE13 : 1. R503 change pull up source from 3VPCU to +3V for real power plane. PAGE17 : 1. CN22 pin15 pull down for customer request. PAGE18 : 1. Change C730 from 3300p to 0.1u for power drop. PAGE20 : 1. Add R529, R530 2.7K pull down for option FF and DF. 2. Reserve C754, C755 for EMI. 3. Change C742 to 22p for waveform quality. PAGE21 : 1. Add C758-C761 0.1u for bypass noise. 2. Change R501 from 3.3K to 0 for signal level. 3. Add R506, R511, U36 for signal driving. 4. Change R518, R519 to 2.2K for signal level. PAGE22 : 1. change CN19, CN23, CN16 footprint for new part. PAGE24 : 1. reserve C751, C752, C753, C756, C757 0.1u for EMI.	PAGE33 : 1. Change PC47 to 0.47U, PC37 to 0.047U for reduce Adapter in inrush current. 2. Del P049 for fix 3 CELL battery and cost down. 3. Change P053 for 2N7002K for ESD protect. 4. Add R130, P054 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm, PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate	19	2A	3B	
2A	PAGE21 : 1. Del C642 for meet IXP power on sequence. 2. Del R444 10K, Add R445 10K for ATI USB clock from outside. PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal.	PAGE34 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	20	3A	3B	
	PAGE22 : 1. Del R196, C402, no need reserve. 2. CHANGE R213 SIGNAL TO PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 3. Reserve R215 1K PULL DOWN 4. Add R507, R508, R509, D19 for ATI LCD back light bug.	PAGE35 : 1. ADD R516, R517, R518 for TI requirement. 2. Remove R397, D16, R489. 3. Add a Quick Switch U34 to isolate clock. 4. Change R501 to 0 ohm. 5. CN5 pin 35, 43 connect to the same net. 6. C725-C728 0.1U for power noise.	21	2A		
2A	PAGE23 : 1. ADD C721 100P, C722 4.7U, C723 3300P, C724 2.2U for high frequency decoupling. 3. Remove R386 Q33, connect U18 pin 6 to TEMP_ALARMH (no need level shift). 4. Change C311 from 10u to 100u and remove C304, that ensures VDD to VDDA power down sequence is met.	PAGE36 : 1. Change PC47 to 0.47U, PC37 to 0.047U for reduce Adapter in inrush current. 2. Del P049 for fix 3 CELL battery and cost down. 3. Change P053 for 2N7002K for ESD protect. 4. Add R130, P054 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm, PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate	22	3A	3B	
	PAGE24 : 1. C330, C479 CHANGE VALUE FROM 33p TO 27p for meet 35ppm. 2. DEL R84 0ohm (don't need reserve).	PAGE37 : 1. CHANGE PQ41 FROM A04704 TO A04702, CHANGE PR102 FROM 47.5K TO 80.6K, CHANGE PQ43 FROM SI4834 TO A04914 for Modify SVPCU OCP point.	23	2A		
2A	PAGE25 : 1. C148, C163 VALUE CHANGE FROM 330U TO 220U for Mechanic interference. 2. C225, C227 PART NUMBER CHANGE TO CH733LM812 for Mechanic interference. 3. R16 VALUE CHANGE FROM 10K TO 8.2K for ATI requirement.	PAGE38 : 1. Change PWM IC from MAX1845 to MAX8743 to avoid negative voltage.Modify 2.5VSUS, 1.8V_S5 OCP point.	24	3A	3B	
	PAGE26 : 1. ADD R502 15K pull low for tune ISOLATEB voltage. 2. R341 change 4.7K to 3.6K for REALTEK recommend. 3. Add C729 10u and C650 change value from 10u to 22u for REALTEK recommend. 4. Change C385 from 2200p to 3300p for tune 3VPCU drop level. 5. Add C736, C737, R438, C739 for EMI. 6. DEL R134 no need reserve, ADD Q40 for leakage current.	PAGE39 : 1. CHANGE PR128 NO STUFF for adjust work frequency. 2. ADD PC80 change from 220u to 470u	25	1A		
2A	PAGE27 : 1. U11 change package to TSSOP32 for Mechanic interference. 2. DEL R246, R249 for IG LAN.	PAGE40 : 1. ADD PR124 15K, DEL PR70, PC2 for VR_ON signal add pull down resistor. 2. Change PR64 from 37.4k to 49.9k for update over current from 32A to 39A. PAGE41 : 1. Add R505, R506 and Change VSENSE from VTT_DDR to CPU_VTT_SENSE 2. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	26	3A	3B	
	PAGE28 : 1. R483 change signal from 5VPCU to +5V and R350 pull 5VSUS for leakage current. PAGE29 : 1. U11 change package to TSSOP32 for Mechanic interference. PAGE30 : 1. C389 8p, C399 5.6p change value to 15p for clock tolerance. 2. Del signal_BT_OFF#_RF_OFF# for HP implement guide. 3. ADD R471 and DEL R468, R470 for ATI power OK sequence. 4. Add D20 for EC leakage current.	PAGE42 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	27	2A		
2A	PAGE29 : 1. U11 change package to TSSOP32 for Mechanic interference. PAGE30 : 1. C389 8p, C399 5.6p change value to 15p for clock tolerance. 2. Del signal_BT_OFF#_RF_OFF# for HP implement guide. 3. ADD R471 and DEL R468, R470 for ATI power OK sequence. 4. Add D20 for EC leakage current.	PAGE43 : 1. Del 1G circuit, because no support 1G function.	28	3A	3B	
	PAGE31 : 1. ADD HOLE24, AND D21 to C744 BOM NO STUFF for tune FAN clock. 2. CHANGE R464, L2, L32 TO BK1608LL680, C619, C419 TO 10P for CRT timing.	PAGE44 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	29	2A		
2A	PAGE32 : 1. ADD R513, R514 2, C731, C732, C733 FOR EMI. PAGE33 : 1. DEL CN26, C681, C677, C673 because no need AV function. PAGE35 : 1. ADD PR126, PR125, P051, P052 for 2.5VSUS and 1.8V_S5 discharge circuit. PAGE36 : 1. CHANGE PQ24 FROM SI4425 TO A04407, CHANGE PQ33 FROM A04411 TO A04407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add P053, PD17, PR127 PC144 for prevent AC discharge MOSFET damage when adapter over watt.	PAGE45 : 1. Del 1G circuit, because no support 1G function.	30	3A	3B	
	PAGE33 : 1. ADD R513, R514 2, C731, C732, C733 FOR EMI. PAGE35 : 1. ADD PR126, PR125, P051, P052 for 2.5VSUS and 1.8V_S5 discharge circuit. PAGE36 : 1. CHANGE PQ24 FROM SI4425 TO A04407, CHANGE PQ33 FROM A04411 TO A04407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add P053, PD17, PR127 PC144 for prevent AC discharge MOSFET damage when adapter over watt.	PAGE46 : 1. Del 1G signal. 2. Add R225, R526, R527 0ohm for option FF or DF TV. 3. Add common choke for USB.	31	2A		
2A	PAGE34 : 1. Change PC47 to 0.47U, PC37 to 0.047U for reduce Adapter in inrush current. 2. Del P049 for fix 3 CELL battery and cost down. 3. Change P053 for 2N7002K for ESD protect. 4. Add R130, P054 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm, PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate	PAGE47 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	32	3A	3B	
	PAGE35 : 1. ADD R516, R517, R518 for TI requirement. 2. Remove R397, D16, R489. 3. Add a Quick Switch U34 to isolate clock. 4. Change R501 to 0 ohm. 5. CN5 pin 35, 43 connect to the same net. 6. C725-C728 0.1U for power noise.	PAGE48 : 1. Del 1G signal. 2. Add R225, R526, R527 0ohm for option FF or DF TV. 3. Add common choke for USB.	33	2A		
2A	PAGE36 : 1. CHANGE PQ24 FROM SI4425 TO A04407, CHANGE PQ33 FROM A04411 TO A04407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add P053, PD17, PR127 PC144 for prevent AC discharge MOSFET damage when adapter over watt.	PAGE49 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	34	1A		
	PAGE37 : 1. CHANGE PQ41 FROM A04704 TO A04702, CHANGE PR102 FROM 47.5K TO 80.6K, CHANGE PQ43 FROM SI4834 TO A04914 for Modify SVPCU OCP point.	PAGE50 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	35	2A		
2A	PAGE38 : 1. Change PWM IC from MAX1845 to MAX8743 to avoid negative voltage.Modify 2.5VSUS, 1.8V_S5 OCP point.	PAGE51 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	36	3A	3B	
	PAGE39 : 1. CHANGE PR128 NO STUFF for adjust work frequency. 2. ADD PC80 change from 220u to 470u	PAGE52 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	37	2A		
2A	PAGE40 : 1. ADD PR124 15K, DEL PR70, PC2 for VR_ON signal add pull down resistor. 2. Change PR64 from 37.4k to 49.9k for update over current from 32A to 39A. PAGE41 : 1. Add R505, R506 and Change VSENSE from VTT_DDR to CPU_VTT_SENSE 2. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE53 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	38	3A	3B	
	PAGE41 : 1. Add R505, R506 and Change VSENSE from VTT_DDR to CPU_VTT_SENSE 2. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE54 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	39	2A		
2A	PAGE42 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	PAGE55 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	40	3A	3B	
	PAGE43 : 1. Del 1G circuit, because no support 1G function.	PAGE56 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	41	2A		
2A	PAGE44 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	PAGE57 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE45 : 1. Del 1G circuit, because no support 1G function.	PAGE58 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE46 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	PAGE59 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE47 : 1. Change PC47 to 0.47U, PC37 to 0.047U for reduce Adapter in inrush current. 2. Del P049 for fix 3 CELL battery and cost down. 3. Change P053 for 2N7002K for ESD protect. 4. Add R130, P054 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm, PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate					
2A	PAGE48 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop.	PAGE60 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE49 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm, PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate	PAGE61 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE50 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE62 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE51 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE63 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE52 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE64 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE53 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE65 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE54 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE66 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE55 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE67 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE56 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE68 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE57 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE69 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE58 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE70 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE59 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE71 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE60 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE72 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE61 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE73 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
2A	PAGE62 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE74 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				
	PAGE63 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.	PAGE75 : 1. Change PR52 to 33K, PR51 to 100k for timing. 3. PC61, PC62 no stuff.				