AT3 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1
PAG 13,14
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 13,14
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON
PAG 26

TV_OUT
CRT_OUT

CRT / S-VIDEO
PAG 25

LVDS(2 Channel)

Panel Connector
15" / 17" PAG 26

DMI LINK

NBSRCCLK, NBSRCCLK#

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

Option for 17" only

SATA - HDD
PAG 35
SATA2

SATA - HDD
PAG 32
SATA0 150MB

PATA- CD-ROM
PAG 32
PATA (66/100/133)

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0
5 | 0,1,2 | 3 | 4,6,7

Bluetooth PAG 35
USB2.0 I/O Ports X3 PAG 32
Camera X1 PAG 32
Mini PCI-E Card x1
Express Card x1
Cable Docking x1

PCI BUS / 33MHz
PCI-E
Azalia

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
(10/100/GagaLAN)
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

Realtek
ALC 268
PAG 29

Two-element microphone
PAG 29

Audio Jacks
(Phone/ MIC)
PAG 29

LPC

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

Keyboard Touch Pad PAG 36
CIR PAG 36
Capacitive Sense SW PAG 36

X-Bus

FAN PAG 38
Flash PAG 37
SPI PAG 37

AUDIO Amplifier
PAG 30

Jack to Speaker
PAG 30

MDC DAA
SI3080
PAG 31

MODEM RJ 11
PAG 33

SIM CARD
PAG 32

RJ45
PAG 33

IEEE1394
CONN
PAG 28

Memory CardReader
PAG 27

SYSTEM CHARGER(MAX8724)
PAG 41

SYSTEM POWER MAX8778
PAG 42

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR)
PAG 46

VCCP +1.5V AND GMCH 1.05V(MAX8717)
PAG 43

VGACORE(1.025V)MAX1992
PAG 45

CPU CORE MAX8771
PAG 44

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Thursday, January 11, 2007 Sheet 1 of 48

L42 BLM21PG600SN1D/08 120 ohms@100Mhz
C400 22U/10V/12 C464 .1U/10V/04 C436 .1U/10V/04 C441 .1U/10V/04 C446 .1U/10V/04 C429 .1U/10V/04
+CK_VDD_MAIN
SI-2 change

L43 BLM21PG600SN1D/08
VDDCPU
C447 22U/10V/12 C445 .1U/10V/04

L44 BLM21PG600SN1D/08 120 ohms@100Mhz
C479 22U/10V/12 C456 .1U/10V/04 C473 .1U/10V/04 C448 .1U/10V/04 C462 .1U/10V/04 C458 .1U/10V/04 C452 .1U/10V/04
+CK_VDD_MAIN2

CLK_3GPLLREQ# R321 10K/04
NEW-CARD_CLK_REQ# R322 10K/04

Y1 14.318MHZ
CG_XIN CG_XOUT
C431 27P/50V/04 C430 27P/50V/04
SI-1 modify (remove R256 --not need)
14.318MHz

internal have already build-in 33ohm damping resisteor

U16 CK505

+CK_VDD_MAIN	16	VDDPLL3	
	9	VDD48	
	2	VDDPCI	
	61	VDDREF	
	39	VDDSRC	
VDDCPU	55	VDDCPU	
+CK_VDD_MAIN2	12	VDD96I/O	
	20	VDDPLL3I/O	
	26	VDDSRCI/O	
	45	VDDSRCI/O	
	36	VDDSRCI/O	
	49	VDDCPU_IO	
	48	NC	
CG_XIN	60	X1	
CG_XOUT	59	X2	
CK_PWRGD	56	CK_PWRGD/PD#	
	57	FSLB/TEST_MODE	
13,14,39 CGCLK_SMB	64	SCLK	
13,14,39 CGDAT_SMB	63	SDATA	
	15	GND	
	19	GND	
	11	GND48	
	52	GNDCPU	
	8	GNDPCI	
	58	GNDREF	
	23	GNDSRC	
	29	GNDSRC	
	42	GNDSRC	

CPUCLKT0 CPUCLKC0	54	RHCLK_CPU	RP40 4 3 4P2R-S-0 CLK_CPU_BCLK 3
	53	RHCLK_CPU#	2 1 CLK_CPU_BCLK# 3
CPUCLKT1 CPUCLKC1	51	RHCLK_MCH	RP41 4 3 4P2R-S-0 CLK_MCH_BCLK 6
	50	RHCLK_MCH#	2 1 CLK_MCH_BCLK# 6
CPUT2_ITP/SRCT8	47	CPU_ITP	RP45 2 1 4P2R-S-0 CLK_CPU_ITP 3
CPUT2_ITP/SRCC8	46	CPU_ITP#	4 3 CLK_CPU_ITP# 3
DOTT_96/SRCT0	13	R_DOT96	RP64 4 3 4P2R-S-0 CLK_PCIE_MINI_C 39
DOTC_96/SRCC0	14	R_DOT96#	2 1 CLK_PCIE_MINI_C# 39
27MHz_Nonss/SRCCLK1/SE1	17	R_DREFSSCLK	RP42 2 1 4P2R-S-0 DREFCLK 7
27Mhz_ss/SRCCLC1/SE2	18	R_DREFSSCLK#	4 3 DREFCLK# 7
SRCCLKT2/SATACL	21	RSRC_SATA	RP43 2 1 4P2R-S-0 DREFSSCLK 7
SRCCLKC2/SATACL	22	RSRC_SATA#	4 3 DREFSSCLK# 7
SRCCLKT3/CR#_C	24	R_CLK_PCIE_VGA	RP46 2 1 4P2R-S-0 CLK_PCIE_SATA 21
SRCCLKC3/CR#_D	25	R_CLK_PCIE_VGA#	4 3 CLK_PCIE_SATA# 21
SRCCLKT4	27	RSRC1_LAN	RP48 2 1 4P2R-S-0 CLK_PCIE_VGA 20
SRCCLKC4	28	RSRC1_LAN#	4 3 CLK_PCIE_VGA# 20
PCI_STOP#	38	PM_STPPCI#	RP50 2 1 4P2R-S-0 CLK_PCIE_LAN 33
CPU_STOP#	37	PM_STPCPU#	4 3 CLK_PCIE_LAN# 33
SRCCLKT6	41	RSRC_ICH	PM_STPPCI# 23
SRCCLKC6	40	RSRC_ICH#	PM_STPCPU# 23
SRCCLKT7/CR#_F	44	CLK_PCIE_MINI	RP49 4 3 4P2R-S-0 CLK_PCIE_ICH 22
SRCCLKC7/CR#_E	43	CLK_PCIE_MINI_#	2 1 CLK_PCIE_ICH# 22
SRCCLKT9	30	RSRC_MCH	RP47 4 3 4P2R-S-0 CLK_PCIE_MINI 39
SRCCLKC9	31	RSRC_MCH#	2 1 CLK_PCIE_MINI# 39
SRCCLKT10	34	CLK_PCIE_NEW	RP52 2 1 4P2R-S-0 CLK_PCIE_3GPLL 7
SRCCLKC10	35	CLK_PCIE_NEW#	4 3 CLK_PCIE_3GPLL# 7
SRCCLKT11/CR#_H	33	NEW-CARD_CLK_REQ#	RP51 2 1 4P2R-S-0 CLK_PCIE_NEW_C 35
SRCCLKC11/CR#_G	32	CLK_3GPLLREQ#	4 3 CLK_PCIE_NEW_C# 35
PCICLK0/CR#_A	1	R_PCLK_KB3920	R_R324 475/F/03 NEW-CARD_CLK_REQ# NEW-CARD_CLK_REQ# 35
PCICLK1/CR#_B	3	R_PCLK_5C832	R323 475/F/03 CLK_3GPLLREQ# CLK_3GPLLREQ# 7
PCICLK2/TME	4	PCLK_MINI_LPC	R_PCLK_KB3920 R250 33/04 PCLK_LPC_KB3920 37,48
PCICLK3	5	PCI_ICH	R_PCLK_5C832 R260 33/04 PCI_CLK_5C832 28
PCICLK4/27_SELECT	6	FCTSEL1	PCLK_MINI_LPC R279 33/04 PCLK_LPC_DEBUG 39
			PCI_ICH T258
			FCTSEL1 R293 33/04 PCLK_MINI 40
PCI_F5/ITP_EN	7	ITP_EN	ITP_EN R285 33/04 PCLK_ICH 22
			R292 33/04 CLKUSB_48 23
USB_48MHZ/FSLA	10	FSA	FSA R295 4.7K/04 CLK_BSEL0
		FSC	FSC R257 4.7K/04 CLK_BSEL2
FSLC/TST_SL/REF	62		R266 33/04 14M_ICH 23

ICS9LPRS355AGLFT/CY28548ZXCT/RTM875T-606

SI-2 Add
SI-1 modify (add in UMA BOM)
SI-2 add -- reserve not need
SI-1 modify for S3 resume issue
form ICS FAE recommend(defaule is Hi)

Q16 2N7002E R288 10K/06 R308 10K/06 CGDAT_SMB
23,35 PDAT_SMB
R845 *100K/04
23 CK_PWG CLK_BSEL1 R298 4.7K/04 FSB
Q17 2N7002E CGCLK_SMB
23,35 PCLK_SMB

R259 10K/04 PCLK_MINI_LPC R269 *4.7K/04
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed

R287 *10K/04 FCTSEL1 R296 10K/04
0=UMA
1 = External VGA

Enable ITP
*10K/04 R283 ITP_EN 10K/04 R825

C416 *33P/50V/04 PCLK_LPC_KB3920
C421 *33P/50V/04 PCI_CLK_5C832
C442 *33P/50V/04 PCLK_ICH
C438 *33P/50V/04 PCLK_LPC_DEBUG
C432 *33P/50V/04 14M_ICH
for EMI

CPU Clock select

3 CPU_BSEL0 R309 0/04 CLK_BSEL0 R310 0/04 MCH_BSEL0 7
+1.05V R307 *56/04 R301 1K/04
3 CPU_BSEL1 R305 0/04 CLK_BSEL1 R299 0/04 MCH_BSEL1 7
R302 *0/04 +1.05V R303 1K/04
3 CPU_BSEL2 R277 0/04 CLK_BSEL2 R258 0/04 MCH_BSEL2 7
R264 *0/04 +1.05V R265 1K/04

<FAE>
1K to NB only when XDP is implement.No XDP can use 0 ohm

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

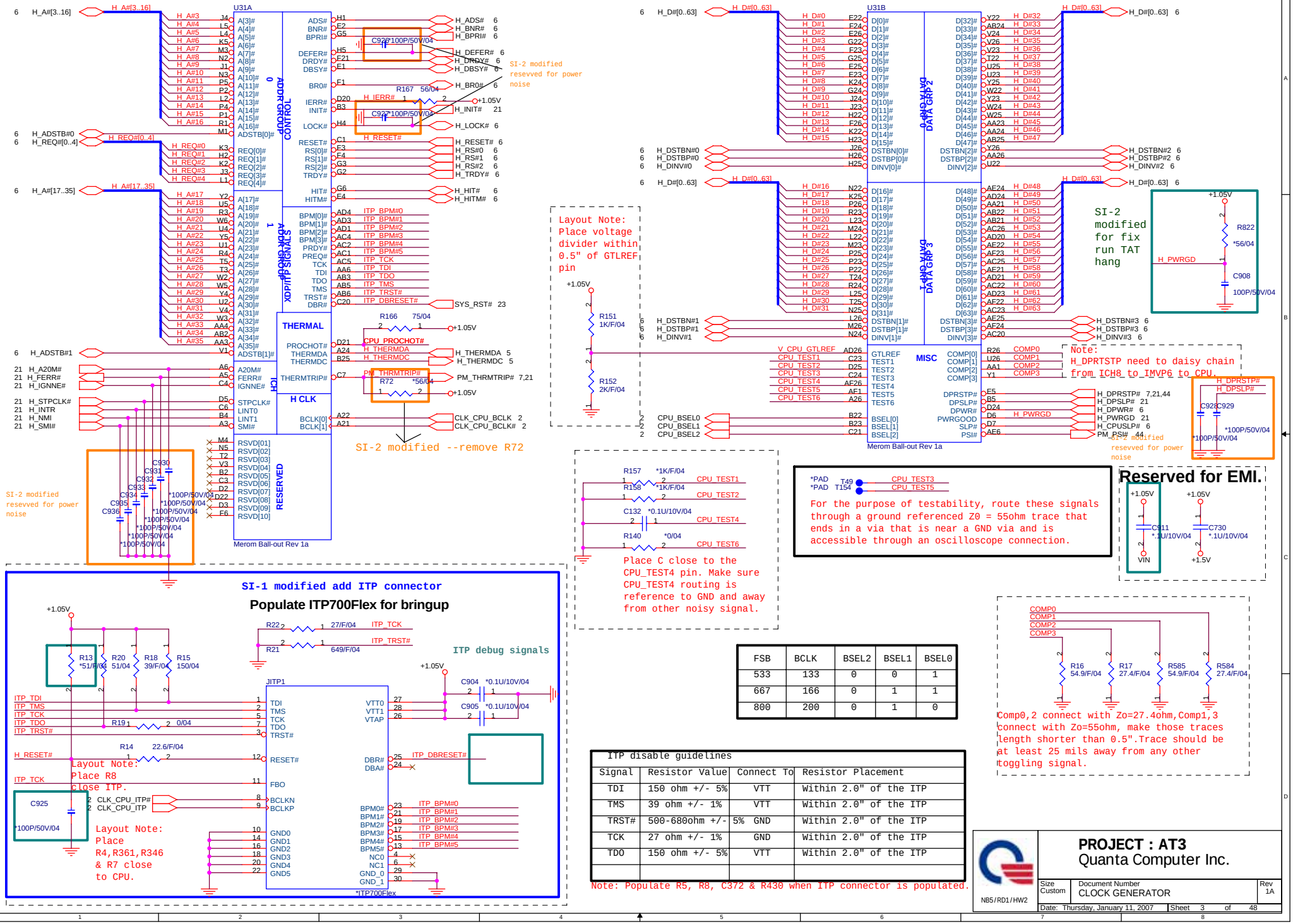
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Thursday, January 11, 2007 Sheet 2 of 48



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

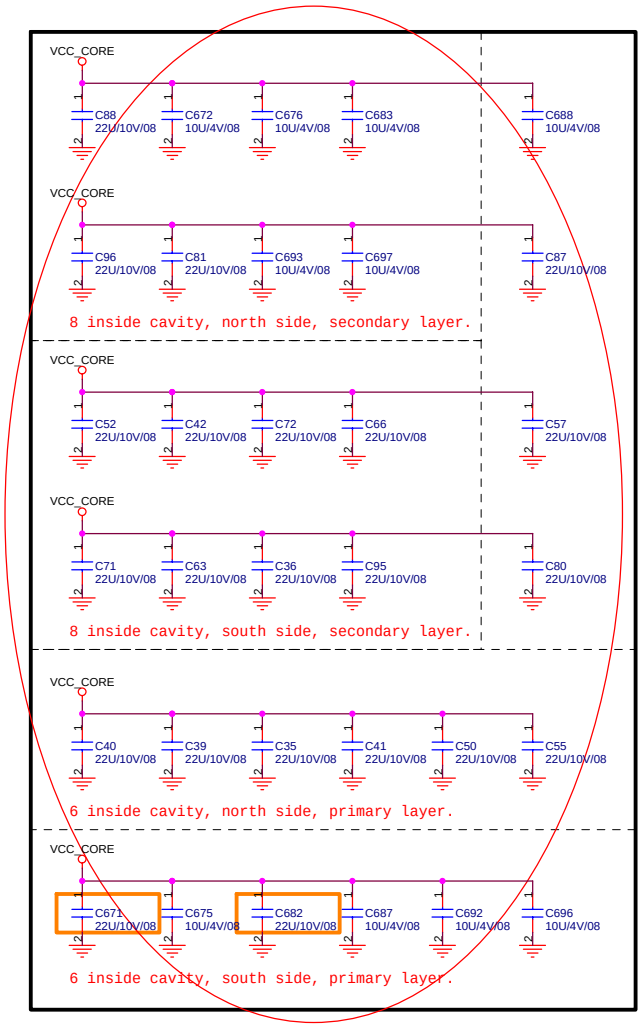
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

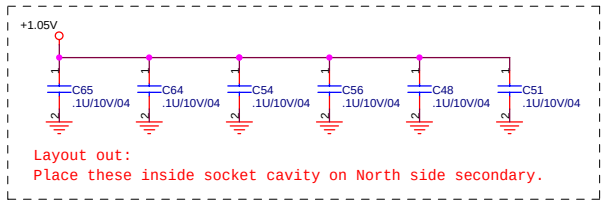
PROJECT : AT3
Quanta Computer Inc.

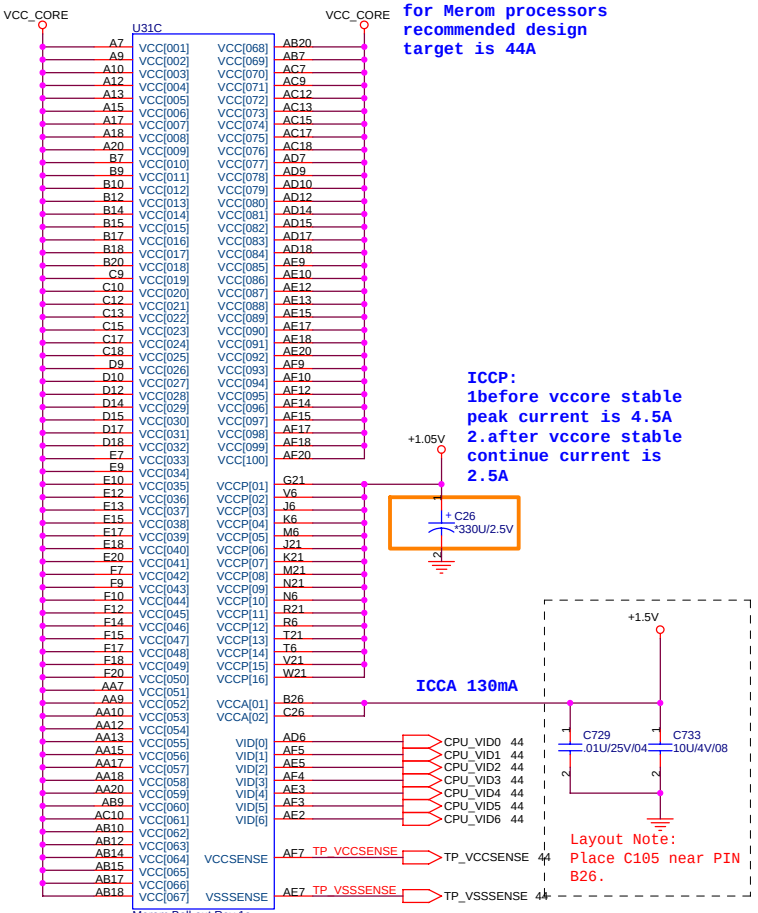
NB5/RD1/HW2

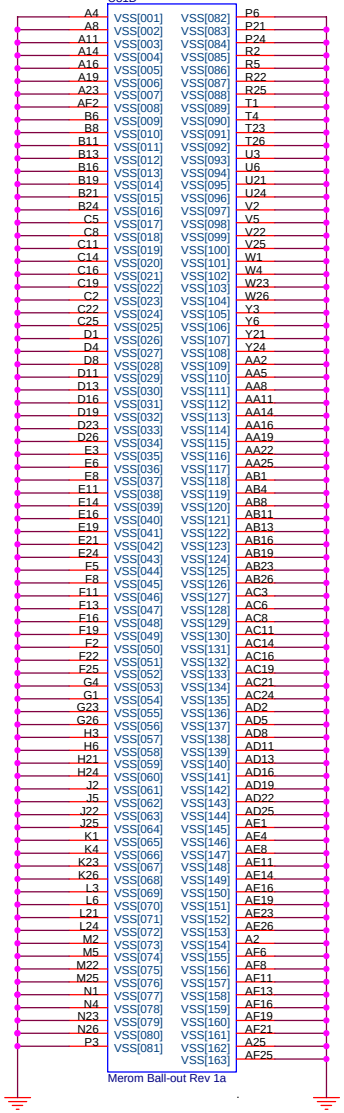
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Thursday, January 11, 2007 Sheet 3 of 48







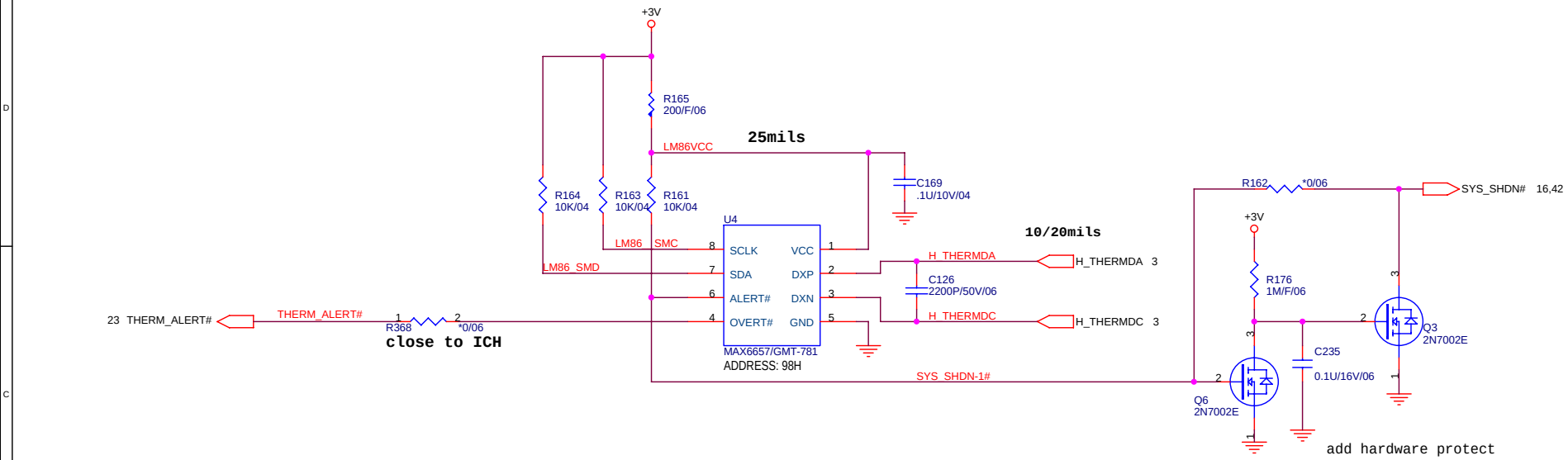


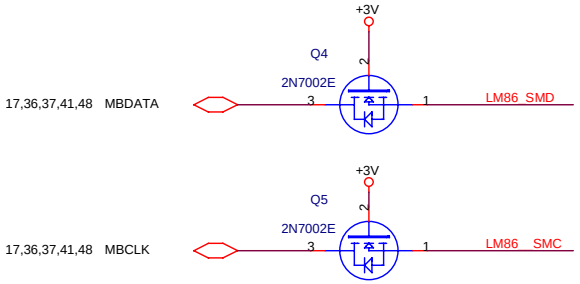
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom Processor (POWER)	1A

NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 4 of 48



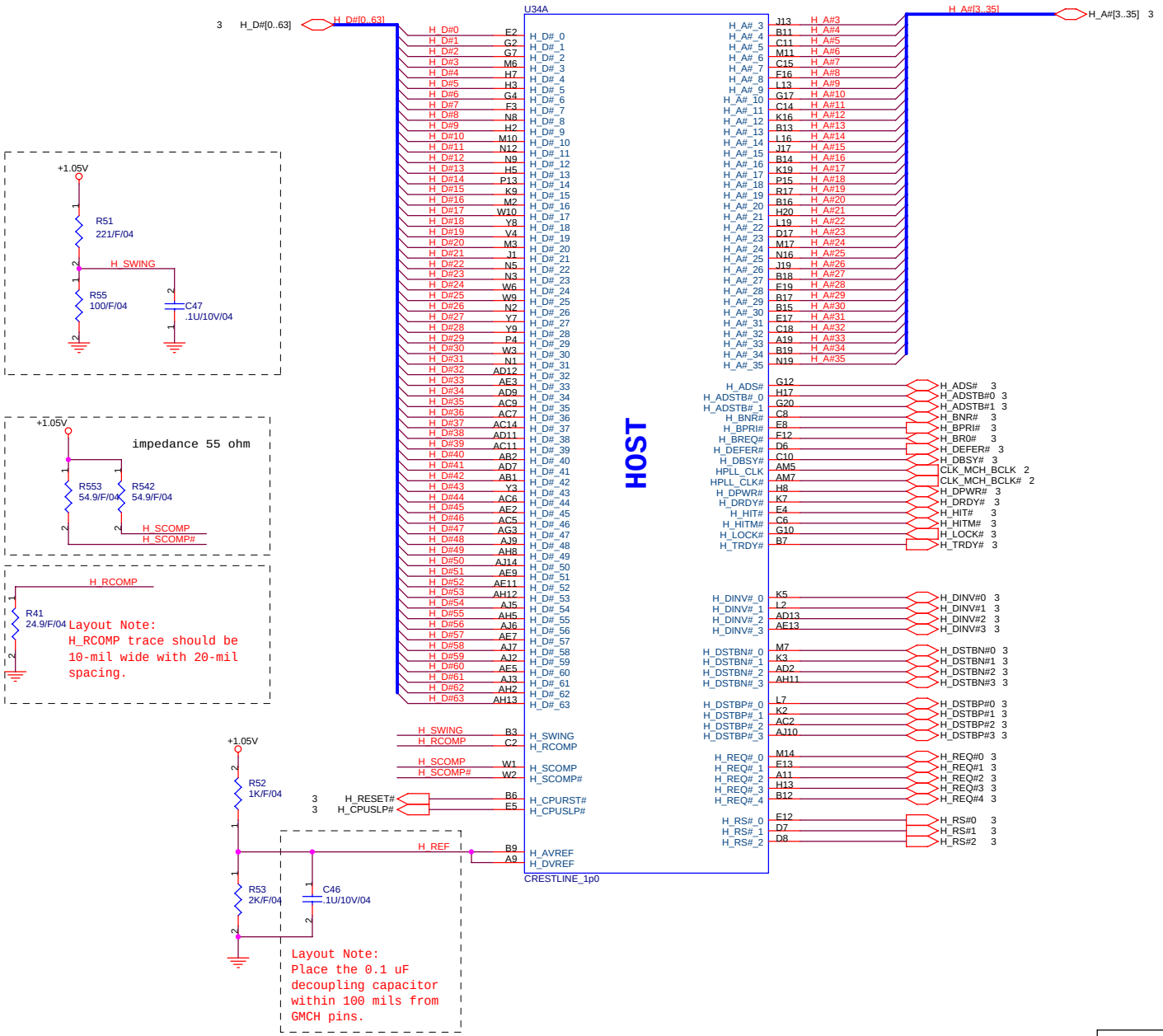


NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
B	THERMAL LM86	1A

Date: Thursday, January 11, 2007 Sheet 5 of 48

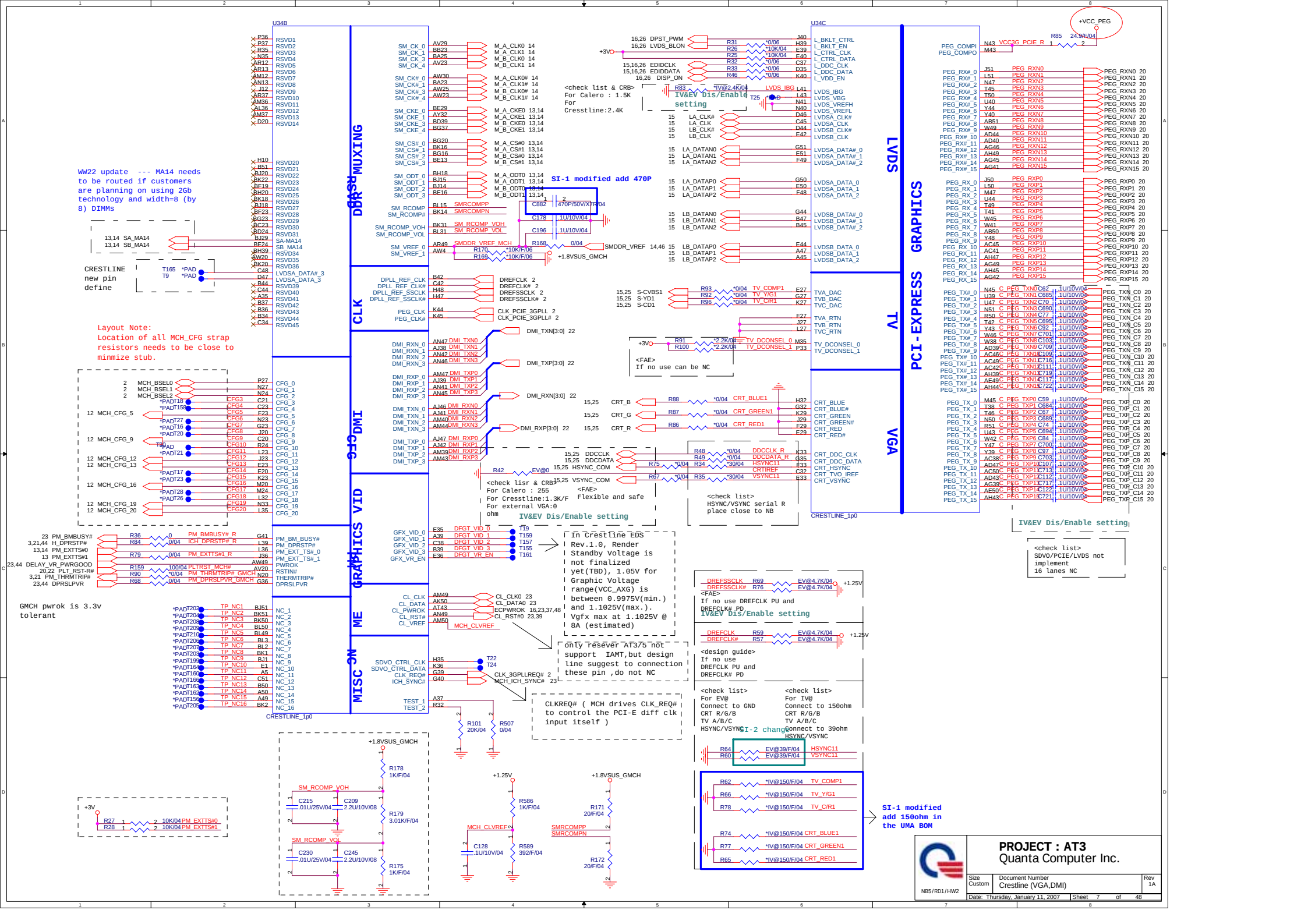


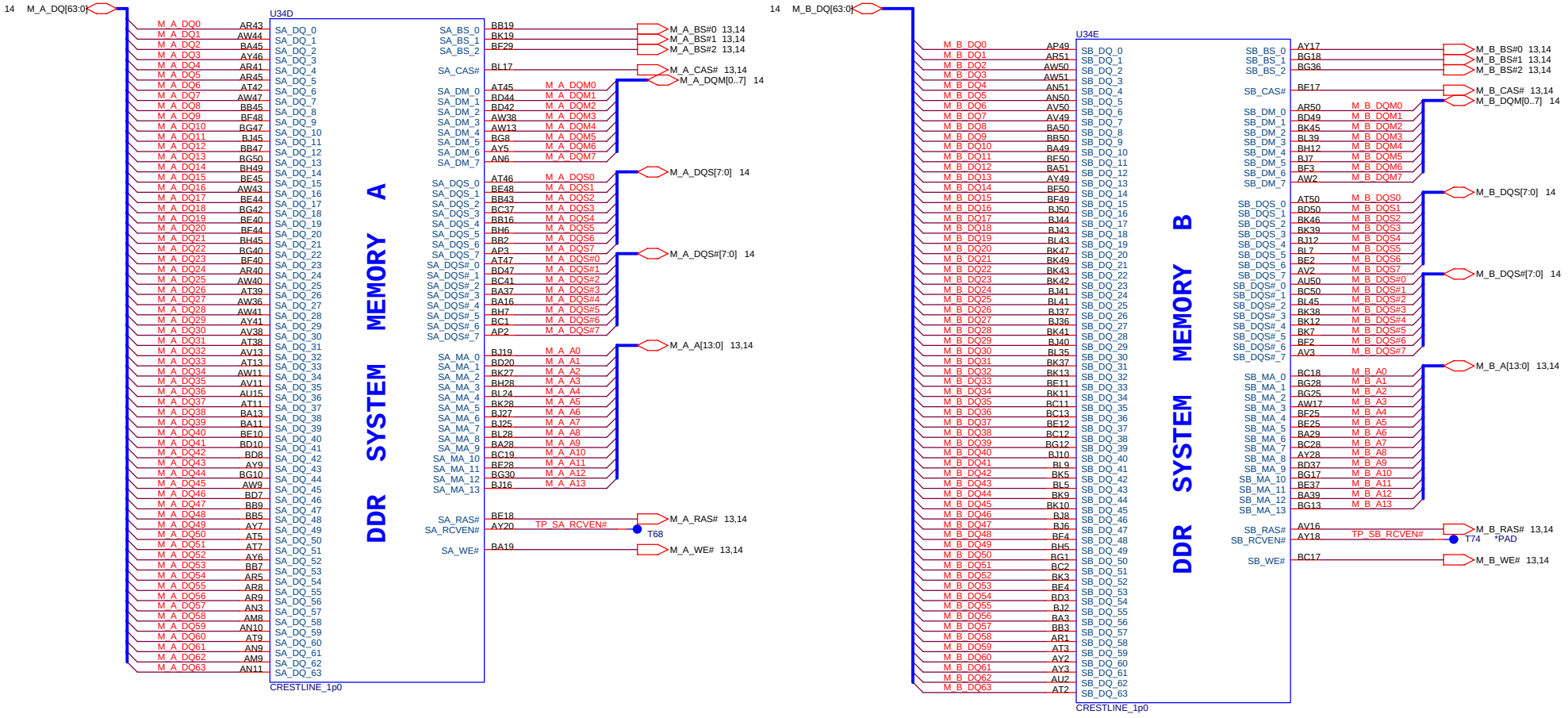
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (HOST)	1A

NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 6 of 48


U34B
U34C
DDR MUXING
CLK
DMI
GRAPHICS VID
ME
MISC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CRESTLINE_1p0
WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.
SI-1 modified add 470P
IV&EV Dis/Enable setting
GMCH pwrok is 3.3v tolerant
In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)
only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
SI-2 change
SI-1 modified add 150ohm in the UMA BOM
PROJECT : AT3
Quanta Computer Inc.
Crestline (VGA,DMI)
Document Number
Rev 1A
Date: Thursday, January 11, 2007
Sheet 7 of 48
NB5/RD1/HW2



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Thursday, January 11, 2007 Sheet 8 of 48

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

SI-1 modify (remove R73,R11 --not need)

SI-2 modified --remove ~~C91&C108~~

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

CRESTLINE_1p0

CRESTLINE_1p0

PROJECT :	AT3
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (VCC, NCTF) Rev: 1A
NB5/RD1/HW2	Date: Thursday, January 11, 2007 Sheet 9 of 48

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

IV&EV Dis/Enable setting

<FAE> INT VGA disable VCCSYNC connect to GND

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

SI-1 modify (NET name wrong)

FB_120ohm+-25%_100mHz _200mA_0.2ohm DC

0.1Caps should be placed 200 mils with in its pins.

Ivcca_PEG_BG supply current 100mA

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

+3V_VCC_HV

40 mil wide

Ivcc_PEG supply current 1.2A

SI-1 modified change

Ivcc_RX_DMI supply current 250mA

SI-2 modified for WW44 request

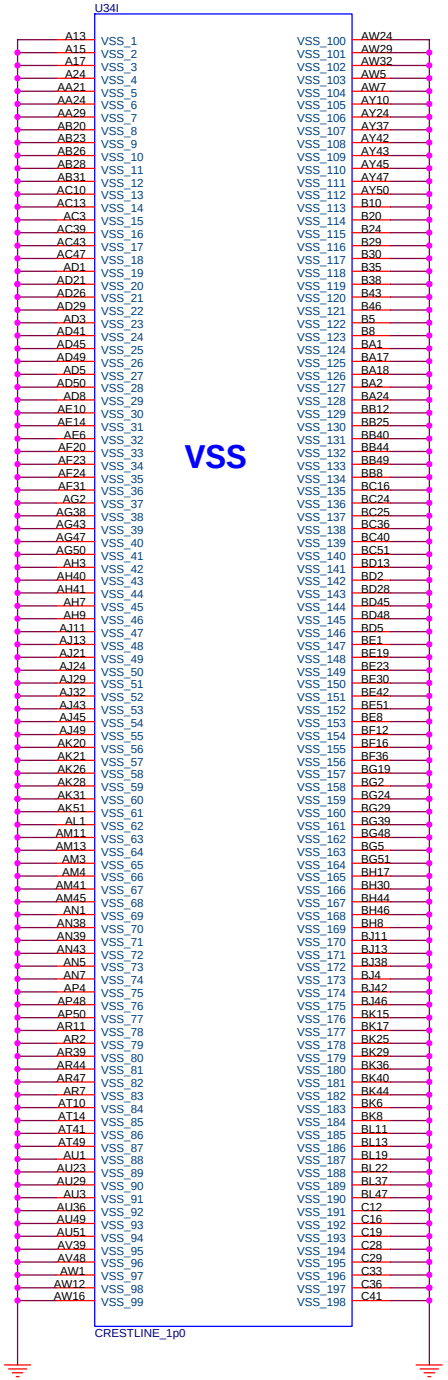
SI-2 add for UMA to fix TV-out noise

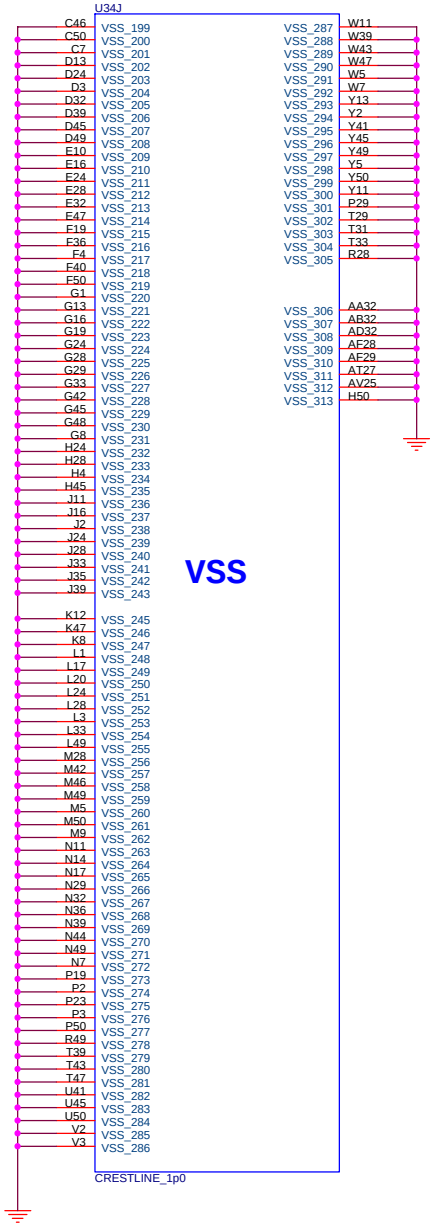
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

POWER

CRESTLINE_1p0

PROJECT :	AT3
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (POWER)
Rev: 1A	
Date: Thursday, January 11, 2007	Sheet 10 of 48
NB5/RD1/HW2	





NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom Document Number: Crestline (VSS)	Rev: 1A
	Date: Thursday, January 11, 2007	Sheet 11 of 48

Strap table

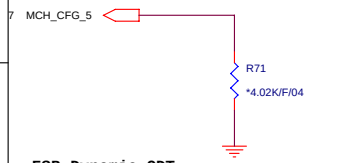
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

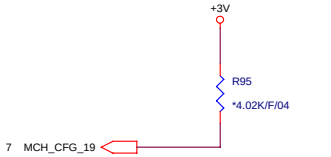
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

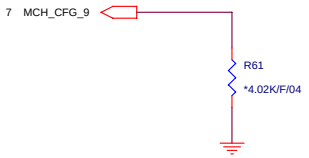


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

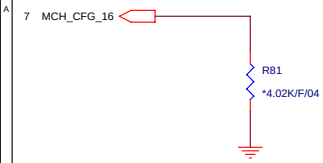


SDVO Present

Strap define at External DVI control page

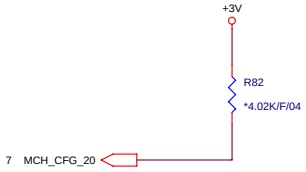
FSB Dynamic ODT

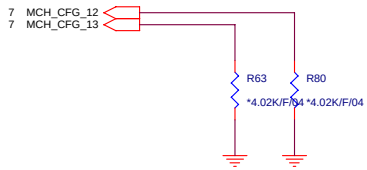
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

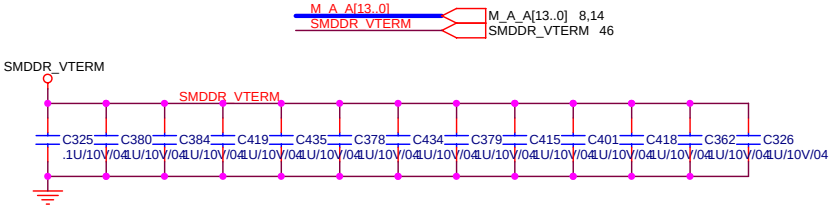
PROJECT : AT3
Quanta Computer Inc.

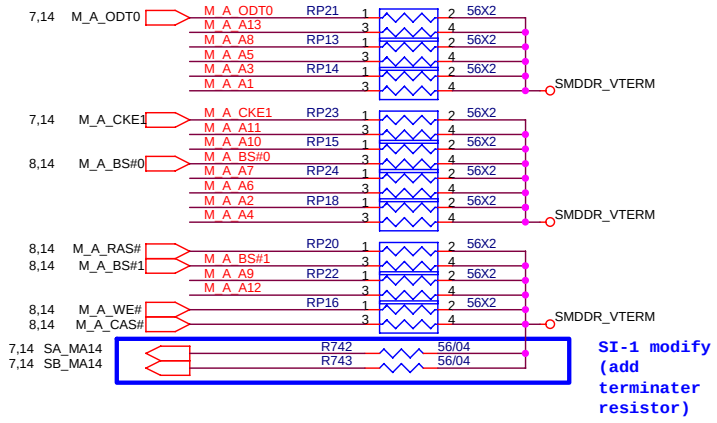
Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

Date: Thursday, January 11, 2007 Sheet 12 of 48

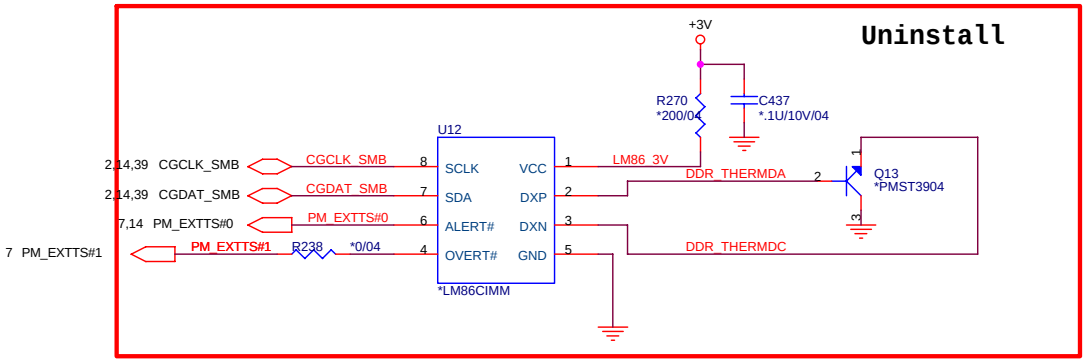
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

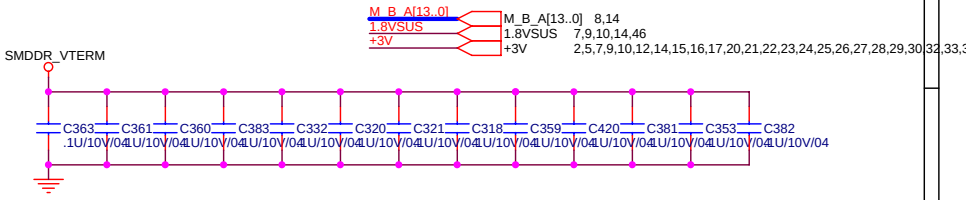




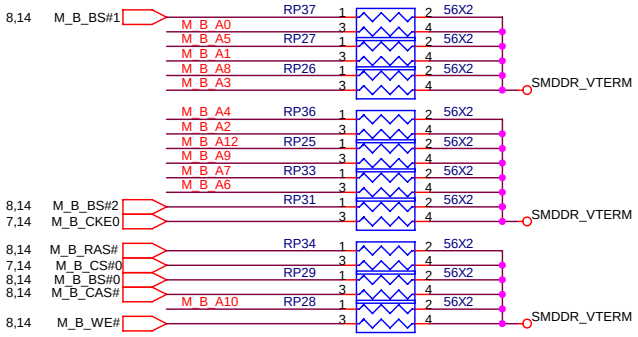
SI-1 modify (add terminater resistor)

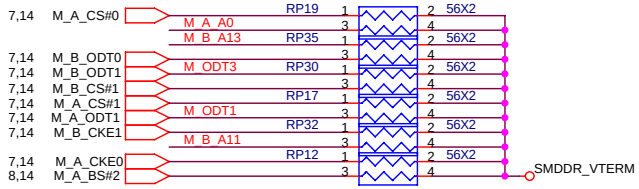


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: B	Document Number: DDRII RES.ARRAY	Rev: 1A
Date: Thursday, January 11, 2007	Sheet 13 of 48	

CGCLK_SMB
CGDAT_SMB
CGCLK_SMB 2,13,39
CGDAT_SMB 2,13,39

M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_CKE[0..1] 7,13
M_A_CS#[0..1] 7,13

M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_RAS# 8,13
M_A_CAS# 8,13
M_A_WE# 8,13

M_A_CLK0
M_A_CLK0# 7
M_A_CLK1 7
M_A_CLK1# 7
M_A_BS#[0..2] 8,13
M_A_ODT[0..1] 7,13

M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
M_A_DQM[0..7] 8
M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DQS#[0..7] 8
M_A_A[13..0] 8,13

M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_CKE[0..1] 7,13
M_B_CS#[0..1] 7,13

M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_RAS# 8,13
M_B_CAS# 8,13
M_B_WE# 8,13

M_B_CLK0
M_B_CLK0# 7
M_B_CLK1 7
M_B_CLK1# 7
M_B_BS#[0..2] 8,13
M_B_ODT[0..1] 7,13

M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]
M_B_DQM[0..7] 8
M_B_DQ[0..63] 8
M_B_DQS[0..7] 8
M_B_DQS#[0..7] 8
M_B_A[13..0] 8,13

+3V
1.8VSUS
+3V 2,5,7,9,10,12,13,15,16,17,20,21,22,23,24,25,26,27,28,29,30,32,33,35,36,37,38,39,40,42,47
1.8VSUS 7,9,10,46

PC2100 DDR2 SDRAM SO-DIMM (200P)

M_B_DQ1 5 / M_B_DQ4 7 / M_B_DQ2 17 / M_B_DQ3 19 / M_B_DQ5 4 / M_B_DQ0 6 / M_B_DQ7 14 / M_B_DQ6 16 / M_B_DQ13 23 / M_B_DQ12 25 / M_B_DQ10 35 / M_B_DQ11 37 / M_B_DQ8 20 / M_B_DQ9 22 / M_B_DQ15 36 / M_B_DQ14 38 / M_B_DQ21 43 / M_B_DQ17 45 / M_B_DQ19 55 / M_B_DQ23 57 / M_B_DQ20 44 / M_B_DQ16 46 / M_B_DQ18 56 / M_B_DQ22 58 / M_B_DQ28 61 / M_B_DQ29 63 / M_B_DQ27 73 / M_B_DQ26 75 / M_B_DQ24 62 / M_B_DQ25 64 / M_B_DQ31 74 / M_B_DQ30 76

M_B_A0 102 / M_B_A1 101 / M_B_A2 100 / M_B_A3 99 / M_B_A4 98 / M_B_A5 97 / M_B_A6 94 / M_B_A7 92 / M_B_A8 93 / M_B_A9 91 / M_B_A10 105 / M_B_A11 90 / M_B_A12 89

M_B_BS#0 107 / M_B_BS#1 106 / M_B_BS#2 85

M_B_CLK0 30 / M_B_CLK0# 32

M_B_CLK1 164 / M_B_CLK1# 166

CGCLK_SMB 197 / CGDAT_SMB 195 / DIM2_SA0 198 / DIM2_SA1 200

+3V 199

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 — DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 — DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DQS0 DQS0 DQS1 DQS1 DQS2 DQS2 DQS3 DQS3 DQS4 DQS4 DQS5 DQS5 DQS6 DQS6 DQS7 DQS7

BA0 BA1 NC/BA2 — CLK0 CLK0 — CLK1 CKL1

SCL SDA SA0 SA1 VDDSPD

CS0 CS1 RAS CAS WE CKE0 CKE1

M_B_DQ36 M_B_DQ33 M_B_DQ35 M_B_DQ39 M_B_DQ37 M_B_DQ32 M_B_DQ34 M_B_DQ38 M_B_DQ41 M_B_DQ46 M_B_DQ43 M_B_DQ45 M_B_DQ44 M_B_DQ47 M_B_DQ42 M_B_DQ55 M_B_DQ49 M_B_DQ51 M_B_DQ53 M_B_DQ48 M_B_DQ52 M_B_DQ50 M_B_DQ54 M_B_DQ61 M_B_DQ60 M_B_DQ58 M_B_DQ63 M_B_DQ56 M_B_DQ57 M_B_DQ62

M_B_DQM0 M_B_DQM1 M_B_DQM2 M_B_DQM3 M_B_DQM4 M_B_DQM5 M_B_DQM6 M_B_DQM7 M_B_DQS0# M_B_DQS1 M_B_DQS1# M_B_DQS2 M_B_DQS2# M_B_DQS3 M_B_DQS3# M_B_DQS4 M_B_DQS4# M_B_DQS5 M_B_DQS5# M_B_DQS6 M_B_DQS6# M_B_DQS7 M_B_DQS7#

M_B_CS#0 M_B_CS#1 M_B_RAS# M_B_CAS# M_B_WE# M_B_CKE0 M_B_CKE1

FOX=AS0A426-M2S-TR
CN26A

CKEA 0,1
H 9.2

DIM2_SA0 R267 10K/04 +3V
DIM2_SA1 R268 10K/04

SMbus address A4

M_A_DQ1 5 / M_A_DQ5 7 / M_A_DQ2 17 / M_A_DQ4 4 / M_A_DQ0 6 / M_A_DQ7 14 / M_A_DQ6 16 / M_A_DQ13 23 / M_A_DQ8 25 / M_A_DQ15 35 / M_A_DQ10 37 / M_A_DQ9 20 / M_A_DQ12 22 / M_A_DQ14 36 / M_A_DQ11 38 / M_A_DQ16 43 / M_A_DQ21 45 / M_A_DQ23 55 / M_A_DQ19 57 / M_A_DQ20 44 / M_A_DQ17 46 / M_A_DQ18 56 / M_A_DQ22 58 / M_A_DQ24 61 / M_A_DQ28 63 / M_A_DQ31 73 / M_A_DQ30 75 / M_A_DQ25 62 / M_A_DQ29 64 / M_A_DQ27 74 / M_A_DQ26 76

M_A_A0 102 / M_A_A1 101 / M_A_A2 100 / M_A_A3 99 / M_A_A4 98 / M_A_A5 97 / M_A_A6 94 / M_A_A7 92 / M_A_A8 93 / M_A_A9 91 / M_A_A10 105 / M_A_A11 90 / M_A_A12 89

M_A_BS#0 107 / M_A_BS#1 106 / M_A_BS#2 85

M_A_CLK0 30 / M_A_CLK0# 32

M_A_CLK1 164 / M_A_CLK1# 166

CGCLK_SMB 197 / CGDAT_SMB 195 / DIM1_SA0 198 / DIM1_SA1 200

+3V 199

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 — DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 — DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DQS0 DQS0 DQS1 DQS1 DQS2 DQS2 DQS3 DQS3 DQS4 DQS4 DQS5 DQS5 DQS6 DQS6 DQS7 DQS7

BA0 BA1 NC/BA2 — CLK0 CLK0 — CLK1 CKL1

SCL SDA SA0 SA1 VDDSPD

CS0 CS1 RAS CAS WE CKE0 CKE1

M_A_DQ32 M_A_DQ35 M_A_DQ37 M_A_DQ38 M_A_DQ33 M_A_DQ36 M_A_DQ39 M_A_DQ34 M_A_DQ40 M_A_DQ41 M_A_DQ46 M_A_DQ42 M_A_DQ45 M_A_DQ44 M_A_DQ43 M_A_DQ47 M_A_DQ52 M_A_DQ48 M_A_DQ55 M_A_DQ54 M_A_DQ53 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ56 M_A_DQ62 M_A_DQ58 M_A_DQ57 M_A_DQ61 M_A_DQ59 M_A_DQ63

M_A_DQM0 M_A_DQM1 M_A_DQM2 M_A_DQM3 M_A_DQM4 M_A_DQM5 M_A_DQM6 M_A_DQM7 M_A_DQS0# M_A_DQS1 M_A_DQS1# M_A_DQS2 M_A_DQS2# M_A_DQS3 M_A_DQS3# M_A_DQS4 M_A_DQS4# M_A_DQS5 M_A_DQS5# M_A_DQS6 M_A_DQS6# M_A_DQS7 M_A_DQS7#

M_A_CS#0 M_A_CS#1 M_A_RAS# M_A_CAS# M_A_WE# M_A_CKE0 M_A_CKE1

FOX=AS0A426-MAS-TR
CN24A

CKEB 0,1
H 5.2

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1

SMbus address A0

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM 1

VREF

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

1.8VSUS 81 / 1.8VSUS 82 / 1.8VSUS 87 / 1.8VSUS 88 / 1.8VSUS 95 / 1.8VSUS 96 / 1.8VSUS 103 / 1.8VSUS 104 / 1.8VSUS 111 / 1.8VSUS 112 / 1.8VSUS 117 / 1.8VSUS 118

M_B_ODT0 114 / M_B_ODT1 119

ODT0 ODT1

NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8

50 / 69 / 83 / 84 / 86 / 120 / 163

7,13 PM_EXTTS#0

SI-1 CHANGE

7,13 SB_MA14 — M_B_A13 116

VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58

162 165 168 171 172 177 178 183 184 187 190 193 196 201

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59

2 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 202

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26B

SMDDR_VREF_DIMM 1

VREF

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

1.8VSUS 81 / 1.8VSUS 82 / 1.8VSUS 87 / 1.8VSUS 88 / 1.8VSUS 95 / 1.8VSUS 96 / 1.8VSUS 103 / 1.8VSUS 104 / 1.8VSUS 111 / 1.8VSUS 112 / 1.8VSUS 117 / 1.8VSUS 118

M_A_ODT0 114 / M_A_ODT1 119

ODT0 ODT1

NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8

50 / 69 / 83 / 84 / 86 / 120 / 163

7,13 PM_EXTTS#0

SI-1 CHANGE

7,13 SA_MA14 — M_A_A13 116

VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58

162 165 168 171 172 177 178 183 184 187 190 193 196 201

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59

2 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 202

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
1 2
SMDDR_VREF_DIMM
R226 0/06
SMDDR_VREF 7,46
R227
1.8VSUS
R603 *10K/F/06
*10K/F/06

Place these Caps near So-Dimm1.

1.8VSUS

C773 2.2U/6.3V/06 C775 2.2U/6.3V/06 C785 2.2U/6.3V/06 C444 2.2U/6.3V/06 C764 2.2U/6.3V/06 C770 .1U/10V/04 C788 .1U/10V/04 C439 .1U/10V/04 C433 .1U/10V/04 C769 .1U/10V/04 C767 .1U/10V/04

SMDDR_VREF_DIMM
C772 .1U/10V/04 C768 2.2U/6.3V/06

+3V
C317 2.2U/6.3V/06 C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS

C774 2.2U/6.3V/06 C786 2.2U/6.3V/06 C784 2.2U/6.3V/06 C759 2.2U/6.3V/06 C760 .1U/10V/04 C776 .1U/10V/04 C789 .1U/10V/04 C787 .1U/10V/04 C443 .1U/10V/04 C765 .1U/10V/04 C766 .1U/10V/04

SMDDR_VREF_DIMM
C371 .1U/10V/04 C373 2.2U/6.3V/06

+3V
C372 2.2U/6.3V/06 C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A
Date: Thursday, January 11, 2007	Sheet 14 of 48	

YELLOW BLOCK is for G8X chip only

SI-2 change to bead

need add to 3v

YELLOW BLOCK is for G8X chip only

FOR G72M/G73M only

OPTION SIGNAL FROM NB FOR UMA VGA

OPTION SIGNAL FROM Nvidia to VGA

C34: PUN issue reserve
U54,C950,c949,R726,R727

Vout=1.25(1+Ra/Rb)

FOR IFPC VDD LEAKAGE CIRCUIT

SPREAD SPECTRUM

I2C ADDRESS: 0xD4H

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A

Date: Thursday, January 11, 2007 Sheet 15 of 48

NB5/RD1/HW2

15mil

U37E

MIOAD

MIOBD

THERMAL GPIO

ROM

U_GPU_G3

YELLOW BLOCK is for G8X chip only

GREEN BLOCK can remove if use G8X

GREEN BLOCK can remove if use G8X

MIOBD7 pull down and MIOB_DE pull up from nvidia HANK recommend

SI-2 MODIFIED

GFX_VID0
H : Low Voltage
L : Normal Voltage

VGACORECTL	G8XM
HI	1.0V
LO	1.1V

GPIO1 PULL DOWN strap can be remove from nvidia HANK recommend

SI-1 MOVE DISP_ON

SI-1 MOVE LVDS_BLON

SI-2 ADD for Nvidia requests

for HDMI function

ROM_TYPE(0:1) resister can be remove due to from nvidia HANK recommend need to reserve or cancel

PCI_DEVICE[3:0] Default are "0",can remove pull down resister from nvidia HANK recommend

PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN .

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

GPIO12	G8X
HI	AC MODE
LO	BAT MODE

SI-2 MODIFIED

FOR BATTERY MODE throttling FUNCTION

VGA THERMAIL CIRCUIT

Default are "0",can remove pull down resister from nvidia HANK recommend

PEX_PLL_EN	R563
3GIO_PADCFG_LUT_ADR0	MIOAD6 R556
3GIO_PADCFG_LUT_ADR1	MIOAD8 R108
3GIO_PADCFG_LUT_ADR2	MIOAD9 R107
3GIO_PADCFG_LUT_ADR3	3GIO_PADCFG3 R539

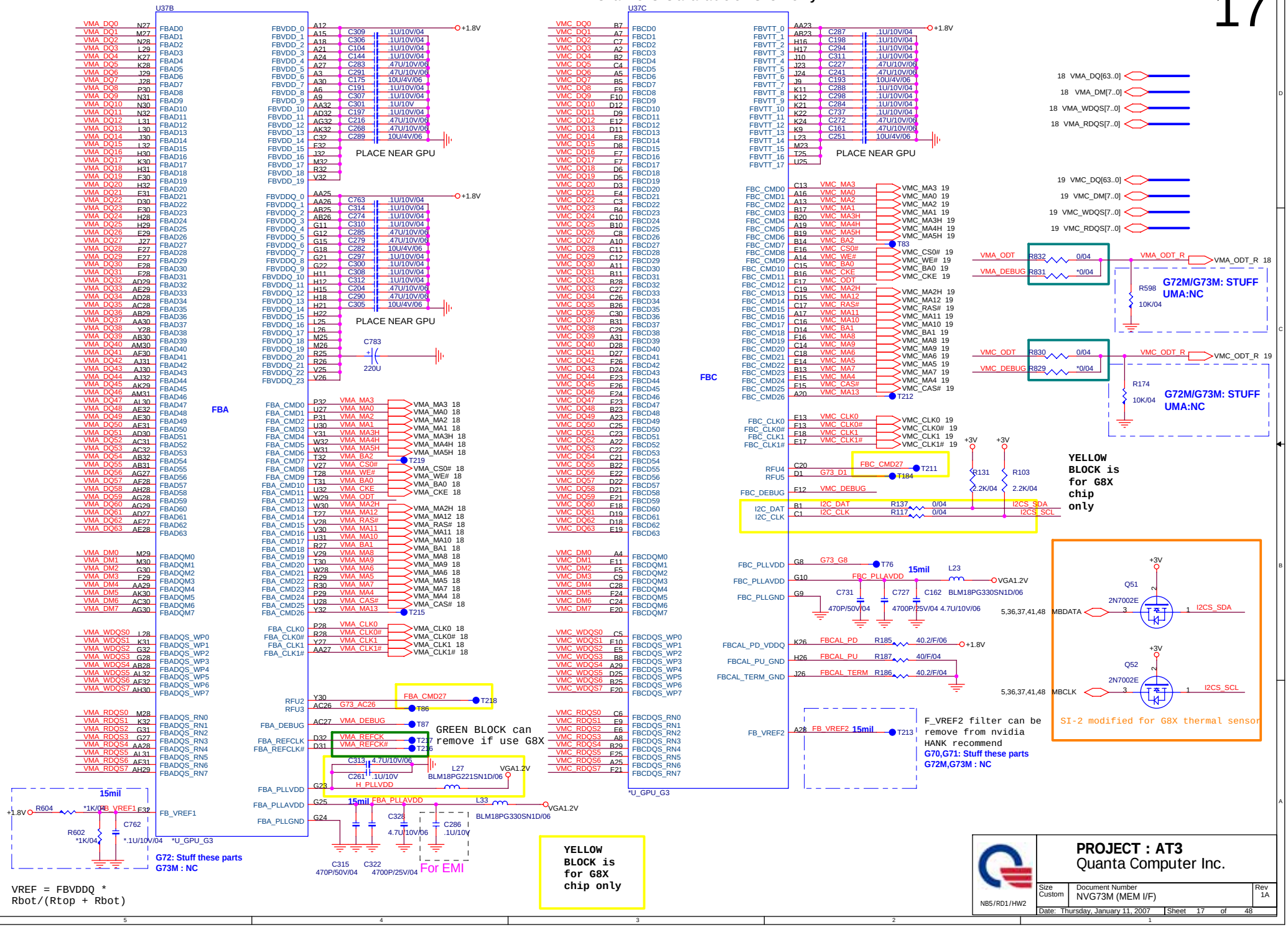
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (ROM/GPIO/STRAP)	1A

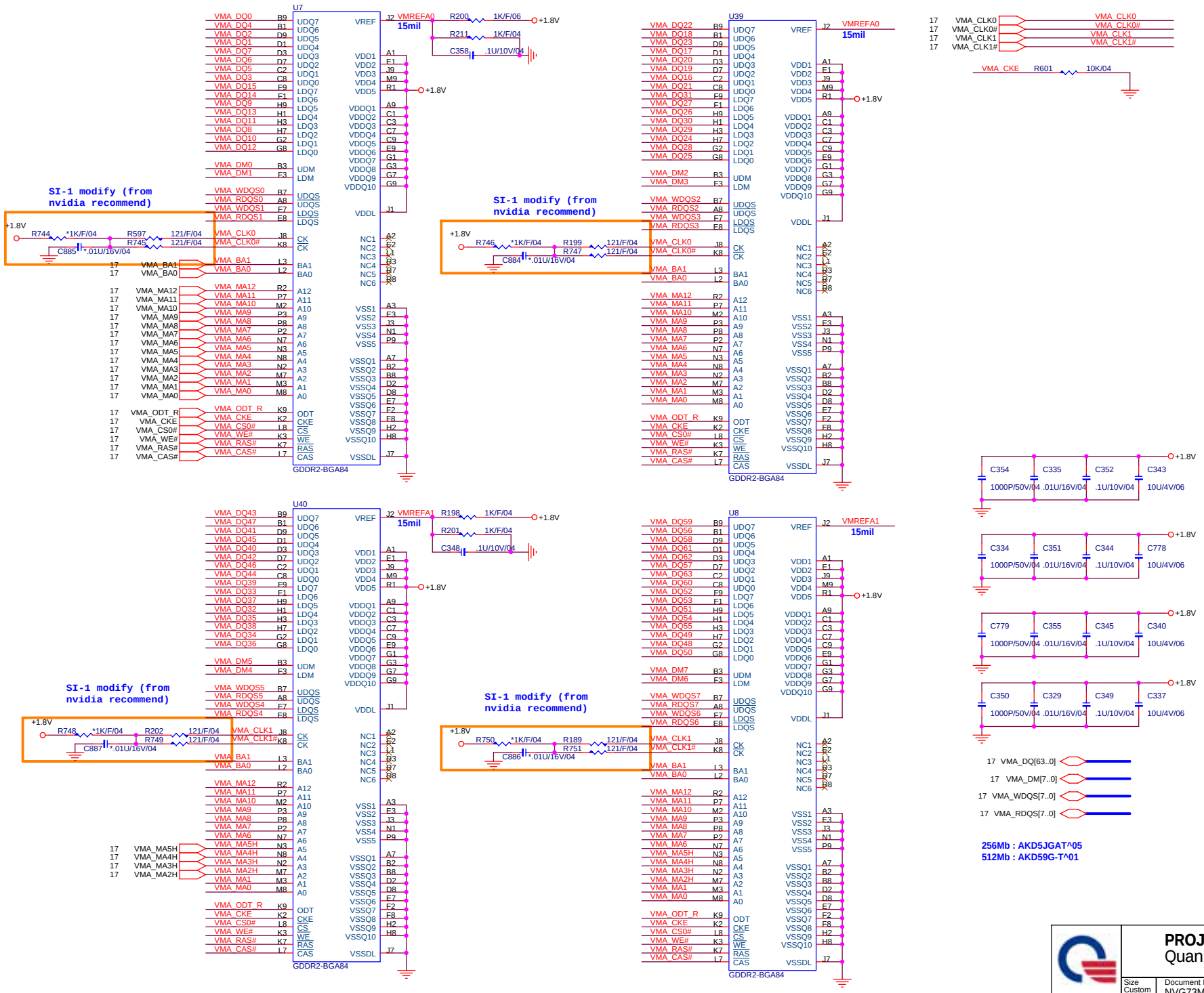
NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 16 of 48

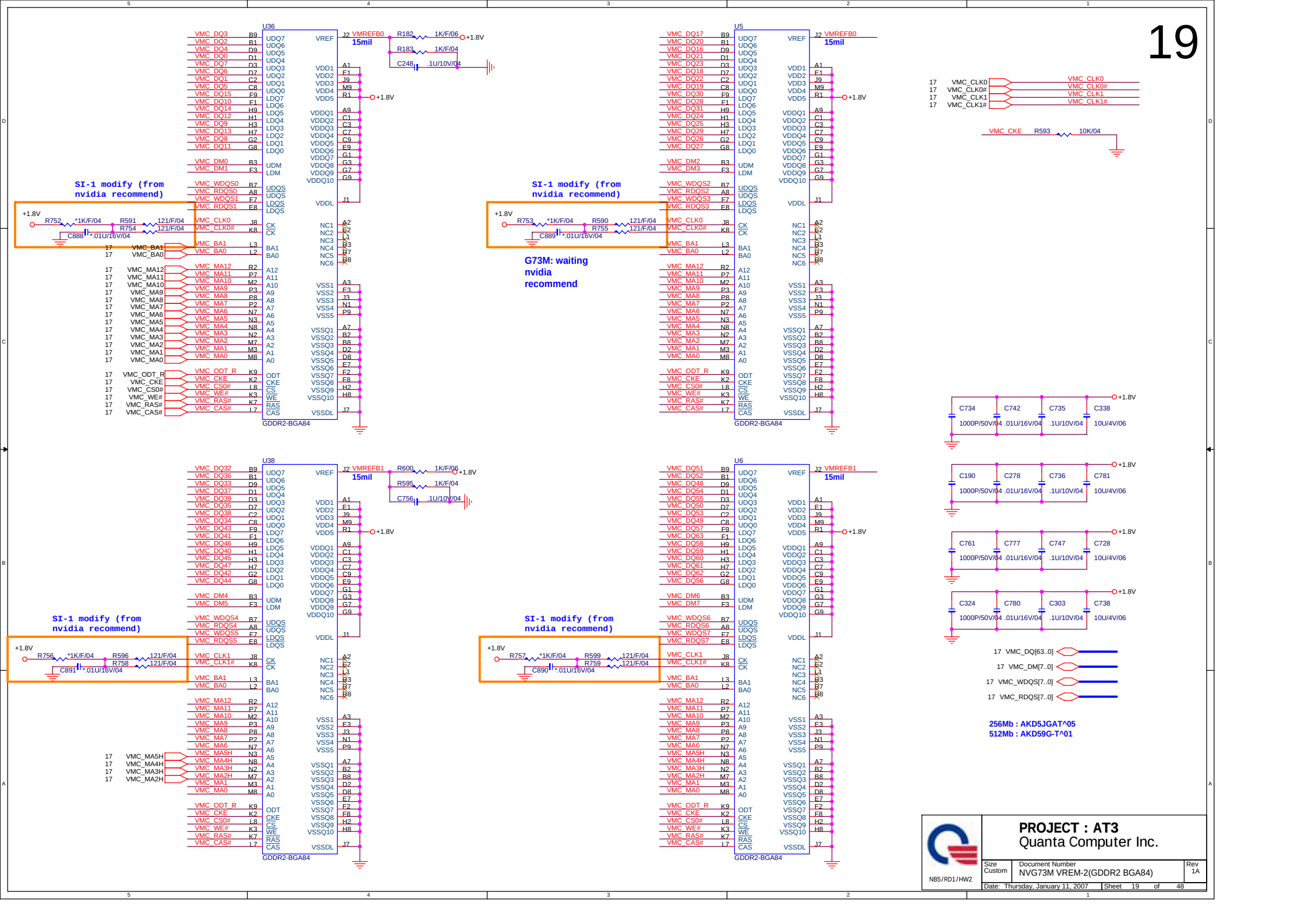
Channel C is available on G73M only



NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.	
Size: Custom	Document Number: NVG73M (MEM I/F)	Rev: 1A
Date: Thursday, January 11, 2007	Sheet 17 of 48	



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: NVG73M VRAN-1(GDDR2 BGA84)	Rev: 1A
Date: Thursday, January 11, 2007	Sheet 18 of 48	


U36
U5
U38
U6
GDDR2-BGA84
SI-1 modify (from nvidia recommend)
G73M: waiting nvidia recommend
15mil
VMREFB0
VMREFB1
+1.8V
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Document Number
NVG73M VREM-2(GDDR2 BGA84)
Size Custom
Rev 1A
Date: Thursday, January 11, 2007
Sheet 19 of 48

500mA

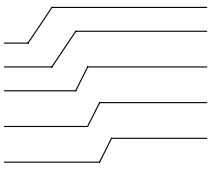
1500mA

180mA

20mA

G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---

power up sequence



For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.

SI-1 modify (change part number)

SI-2 modify for Nvidia requests del R823,R824

SI-1 DEL L22 Nvidia recommend

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (PCIE I/F)	1A

Date: Thursday, January 11, 2007 Sheet 20 of 48

NB5/RD1/HW2

RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

VCCRTC
3VPCU
C804 1U/16V/06
D41 CH500H-40
R638 20K/06
VCCRTC_2
D42 CH500H-40
R635 1K/06
R637 1M/F/06
C811 1U/16V/06
G2 *SHORT_ PAD1
C820 15P/50V/04
CLK_32KX1
Y6 32.768KHZ
R663 10M/06
C817 15P/50V/04
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
BT1 BAT_CONN
CN30 *CWY020-B0G1Z

SI-2-1 modified
(change to battery con)

20MIL 20MIL
5VPCU
R625 *1.2K/06
R628 *1K/06
Q42 *MMBT3904
R626 *4.7K/06
R629 *15K/06
add RTC Bat rechargeable circuit

+1.5V_PCIE
R334 24.9/F/04
GLAN_COMP_SB

U42A

RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS

RTC / LPC
LAN / GLAN
CPU
IHDA
SATA / IDE

ICH8M REV 1.0

FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15
DA0 DA1 DA2
DCS1# DCS3#
DIOR# DIOW# DDACK# IDEIRQ IORDY DDREQ

LAD0 LAD1 LAD2 LAD3 37,39,48
LFRAME# 37,39,48
LDRQ#0 LDRQ#1
GATEA20 37,48
H_A20M# 3
H_DPRSTP# H_DPSLP#
H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RCIN# 37,48
H_NMI 3
H_SMI# 3
H_STPCLK# 3
H_THERMTRIP_R
PDD[15:0] 32
PDA[2:0] 32
PDCS1# 32
PDCS3# 32
PDIOR# 32
PDIOW# 32
PDDACK# 32
IRQ14 32
PDIORDY 32
PDDREQ 32

+3V
R447 10K/06
R648 10K/06
RCIN#
GATEA20
+1.05V
R409 *56/F/06
R449 *56/F/06
R442 56/F/06
R439 0/06
H_DPRSTP# 3,7,44
H_DPSLP# 3
R415 0/F/06
H_FERR# 3
R432 0/F/06
H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RCIN# 37,48
R425 0/F/06
H_NMI 3
H_SMI# 3
H_STPCLK# 3
R406 24.9/F/06
PM_THRMTRIP# 3,7

SI-2 add for fix ESD issue
R849 56/04

Should be 2" close ICH7
C560 *SFI0603-050E101NP/06

ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDOUT
29 ACZ_SDIN0
31 ACZ_SDIN1
T255
T132

33 LAN_DISABLE#
+3V R691 10K/06
36 SATA_LED#
T143
SATA_LED#

32 SATA_RXN0
32 SATA_RXP0
32 SATA_TXN0
32 SATA_TXP0
C576 3900P/25V/04 SATA_RXN0_C
C577 3900P/25V/04 SATA_RXP0_C
C587 3900P/25V/04 SATA_TXN0_C
C590 3900P/25V/04 SATA_TXP0_C
CKL:1n ~ 20nF

SI-1 modified
T244 T243 T135 T136

35 SATA_RXN2
35 SATA_RXP2
35 SATA_TXN2
35 SATA_TXP2
C597 3900P/25V/04 SATA_RXN2_C
C600 3900P/25V/04 SATA_RXP2_C
C606 3900P/25V/04 SATA_TXN2_C
C609 3900P/25V/04 SATA_TXP2_C

2 CLK_PCIE_SATA#
2 CLK_PCIE_SATA

R655 24.9/F/06 SATA_BIAS
Place within 500 mils of ICH7
25mils/15mils

ACZ_SDOUT R654 33/04 ACZ_SDOUT_AUDIO 29
C814 *10P/50V/04
ACZ_SYNC R649 33/04 ACZ_SYNC_AUDIO 29
C816 *10P/50V/04
ACZ_BCLK R653 33/04 BIT_CLK_AUDIO 29
C813 *10P/50V/04
ACZ_RST# R646 33/04 ACZ_RST#_AUDIO 29

intel check list define to stuff 33ohm

ACZ_SDOUT R639 33/04 ACZ_SDOUT_AUDIO_MDC 31
C807 *10P/50V/04
ACZ_SYNC R640 33/04 ACZ_SYNC_AUDIO_MDC 31
C809 *10P/50V/04
ACZ_BCLK R643 33/04 BIT_CLK_AUDIO_MDC 31
C810 *10P/50V/04
ACZ_RST# R645 33/04 ACZ_RST#_AUDIO_MDC 31

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

VCCRTC R443 332K/F/06 ICH_INTVRMEN R417 *0
VCCRTC R444 332K/F/06 LAN100_SLP R414 *0
+3V R644 *1K/06 ACZ_SDOUT ICH_TP3 23 R428 *1K

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M HOST(1/4)	1A

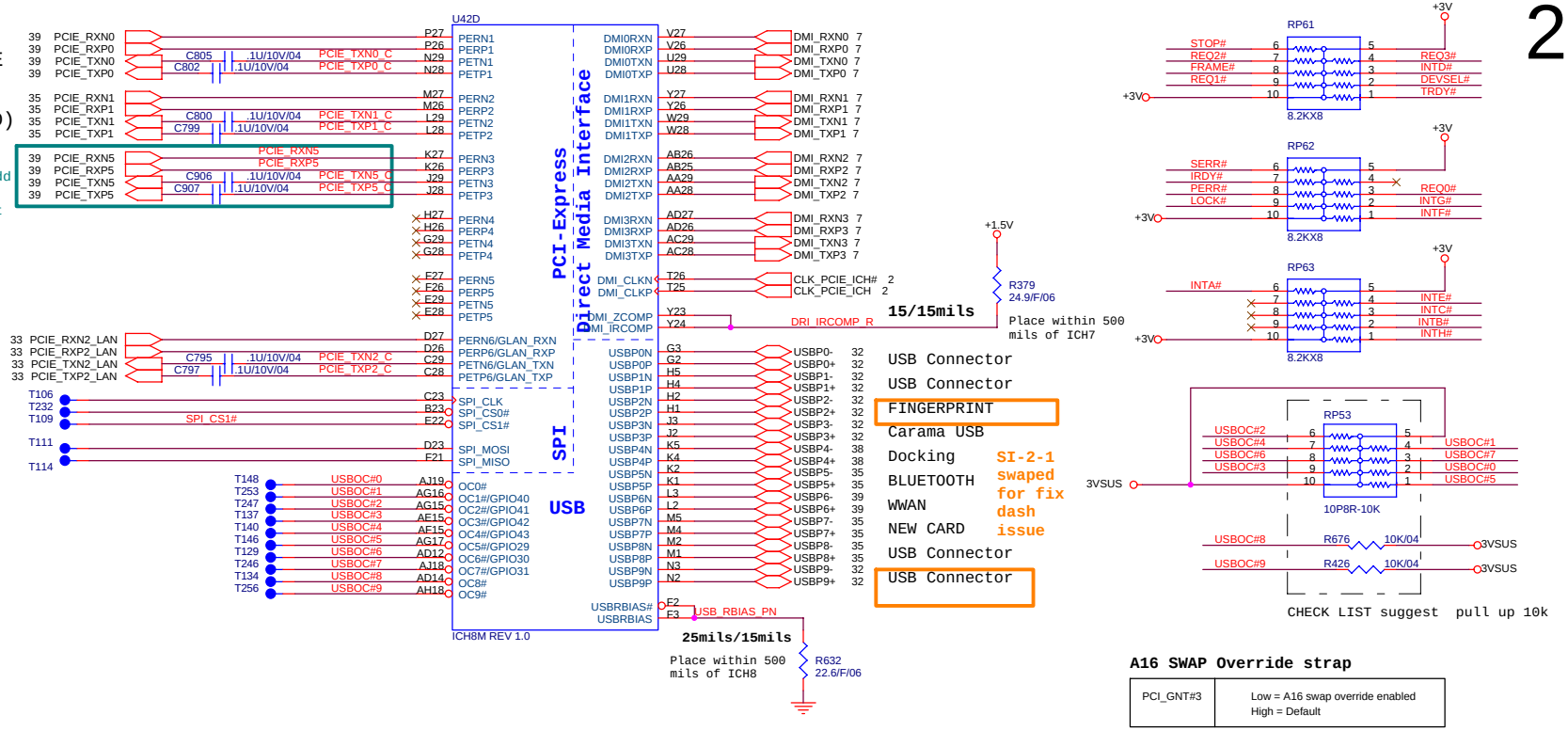
Date: Thursday, January 11, 2007 Sheet 21 of 48

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

SI-2 Add for support RBSON card

PCIE-LAN



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

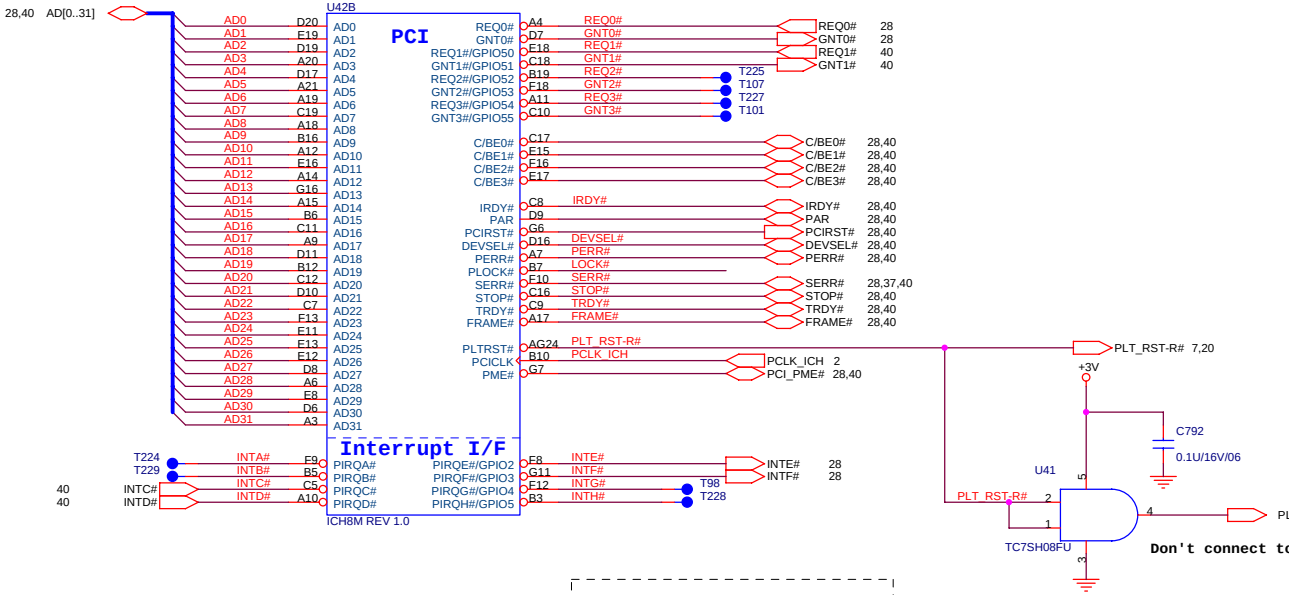
GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PCLK_ICH R328 *0 C484 *33P/50V

for EMI request

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

Date: Thursday, January 11, 2007 Sheet 22 of 48

SI-2 Add for fix re-boot fail

R833 2K/F/04

44 VR_PWRGD_CK410#

U26 NL17SZ14DFT2G

C608 .1U/16V/04

VR_PWRGD_CK410

R809 100K/04

SI-1 has modified it ,please measure BOM has add(intel checklist add)

PCLK_SMB R617 2.2K/06
PDAT_SMB R272 2.2K/06
PCIE_WAKE# R399 1K/06
PM_BATLOW#_R R387 8.2K/06

SMB_LINK_ALERT# R621 10K/06
SMLINK0 R619 10K/06
SMLINK1 R618 10K/06

RI# R624 8.2K/06
DNBSWON# R271 10K/06
SYS_RST#-1 R615 10K/06
SMB_ALERT# R273 10K/06

KBSMI#_R R281 10K/06

these pin if unused require 8.2k to 10k pull-up to +3v

SI-1 modified

SWI#_R R280 10K/06

CLKRUN# R433 8.2K/06
SERIRQ R656 8.2K/06
SCI#_R R662 10K/06

PM_RSMRST#_R R658 10K/06

SI-1 add

U42C ICH8M REV 1.0

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37

Clocks: CLK14, CLK48

SYS GPIO: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32

Power MGT: SUSCLK, SLP_S3#, SLP_S4#, SLP_S5#, S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#

GPIO: WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48

Controller Link: CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#

MISC: SPKR, MCH_SYNC#, TP3, MEM_LED/GPIO24, ME_EC_ALERT/GPIO10, EC_ME_ALERT/GPIO14, WOL_EN/GPIO9

2,35 PCLK_SMB
2,35 PDAT_SMB
PCLK_SMB R816 0/04
PDAT_SMB R817 0/04
SMB_LINK_ALERT#
SMLINK0
SMLINK1

RI#

SYS_RST# R614 0/04 SYS_RST#-1
PM_BMBUSY# R682 0/04
SMB_ALERT#

R450 *10K/F/06
R315 *10K/F/06
2 PM_STPPCI#
2 PM_STPCPU#
R402 0/F/06
R436 0/F/06
PM_STPPCI_ICH#
PM_STPCPU_ICH#

28,37,48 CLKRUN#
33,35,39 PCIE_WAKE#
28,37,40,48 SERIRQ
5 THERM_ALERT#
R364 8.2K/06
VR_PWRGD_CK410

37 KBSMI#
37 SCI#
37 SWI#
R405 0/04 KBSMI#_R
R386 0/04 SCI#_R
R611 0/04 SWI#_R

30 AMPBEEP_EN
26 LCD_BK
LCD_BK
BOARD_ID2

39 WAN_OFF#
39 RF_OFF#
36 BTLED
R687 0/04
R671 0/04
R420 0
R768 10K/04
R769 10K/04
R770 10K/04

SI-1 add

30 ACZ_SPKR
7 MCH_ICH_SYNC#
R427 0
MCH_ICH_SYNC#_R
21 ICH_TP3
R435 *10K

CLK14 14M_ICH 2
CLK48 CLKUSB_48 2
14M_ICH
CLKUSB_48

SUSCLK T108

SLP_S3# R616 100/F/06 SUSB# 37,48
SLP_S4# R326 100/F/06 SUSC# 37,48
SLP_S5# T130

S4_STATE#/GPIO26 T249 R677 *100K/04

PWROK ICH_PWROK

DPRSLPVR/GPIO16 R620 499/F DPRSLPVR DPRSLPVR 7,44

SI-2 change from 100ohm to 499 ohm check list -- series 500ohm to IMVP6+

BATLOW# R642 0/04 PM_BATLOW# 37
DNBSWON# DNBSWON# 37
PWRBTN# C819 .1U/16V/04
R665 *100/F/06
LAN_RST# PLTRST_LAN# R666 100/F/06 LAN_REST 33,37,48 PLTRST# 22,32,33,35,37,39
RSMRST# R659 100/F/06 RSMRST# RSMRST 37,48

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

CK_PWRGD E1 R623 0/04 CK_PWG 2
CLPWROK E3 R622 0/04 ECPWROK 7,16,37,48
SLP_M# AJ25 SUSM# T251

CL_CLK0 F23 CL_CLK0 7
CL_CLK1 AE18 ICH_CL_CLK1 39
CL_DATA0 F22 CL_DATA0 7
CL_DATA1 AF19 ICH_CL_DATA1 39
CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB
CL_RST# AJ23 CL_RST#0 7,39

MEM_LED/GPIO24 AJ27 R284 0/04 BT_OFF# 35
ME_EC_ALERT/GPIO10 AJ24 ME_SMC_ALERT# T250
EC_ME_ALERT/GPIO14 AE22 T141
WOL_EN/GPIO9 AG19 T144

R819 10K/04 3VSUS

SI-1 ADD (ww36 request)

3V_S5 R631 3.24K/F/06
R633 453/F/04
C798 .1U/10V/04

Controller Link 1 VREF for IAMT support only

+3V R338 3.24K/F/06
R344 453/F/04
C511 .1U/10V/04

Controller Link 0 VREF for IAMT support only

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R411 *10K

SI-2 Change

CRB STUFF 2K%1

3VSUS C818 .047U/10V/04

+3V R657 2K/F/04

7,44 DELAY_VR_PWRGOOD
7,16,37,48 ECPWROK
R661 100K/06

U43 TC7SH08FU

ICH_PWROK R667 10K/06

R660 *10K/06 BOARD_ID3 R760 10K/06
R652 *10K/06 BOARD_ID4 R761 10K/06

R692 *10K/06 BOARD_ID0 R693 10K/06
R688 *10K/06 BOARD_ID1 R448 10K/06
R690 *10K/06 BOARD_ID2 R689 10K/06

SI-1 modify (for board ID select)

Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15"PAV Discrete 965PM+G86MV+128M (0:1:0)	17" PAV Discrete 965PM+G86MV+128M (0:1:1)	17" PAV Discrete 965PM+G84MV+256M (1:0:0)	17" PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size: Custom | Document Number: ICH7-M GPIO(3/4) | Rev: 1A

Date: Thursday, January 11, 2007 | Sheet 23 of 48

1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
SI-2 modified (remove R374)
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

Can be connect to +3V_S5 or +1.5V_S5

Can be connect to +3V or +1.5V

U42E — ICH8M REV 1.0

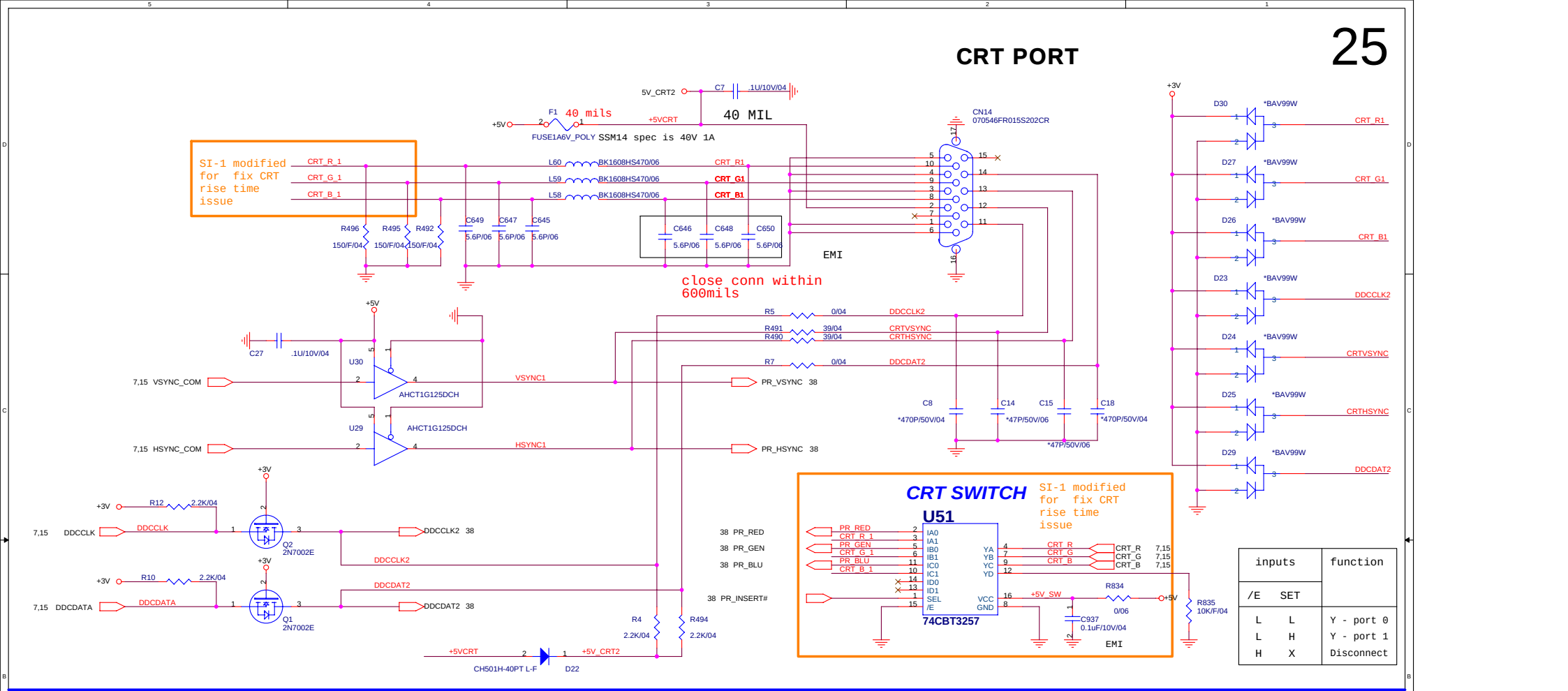
U42F — ICH8M REV 1.0

PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2

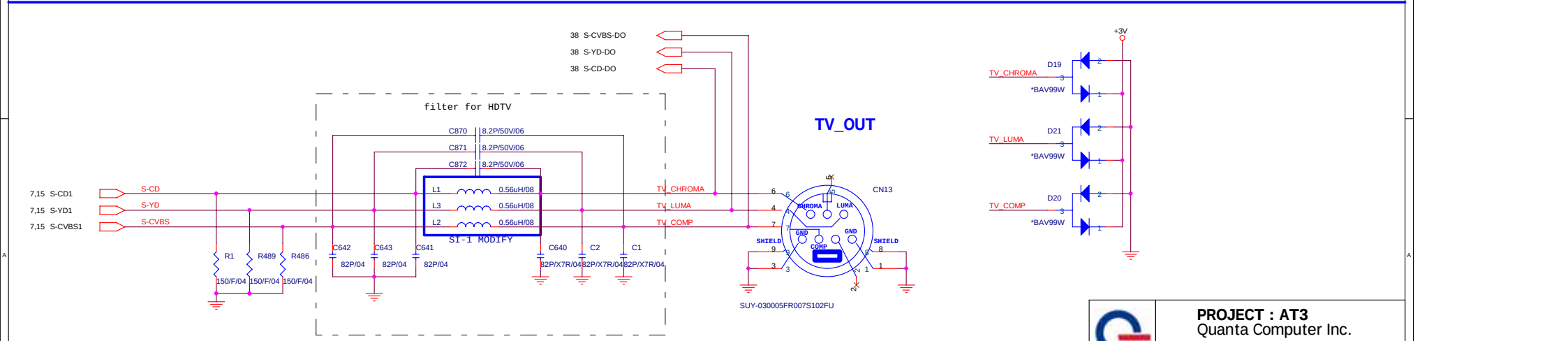
Size	Document Number	Rev
Custom	ICH7-M POWER(4/4)	1A

Date: Thursday, January 11, 2007 Sheet 24 of 48

CRT PORT



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

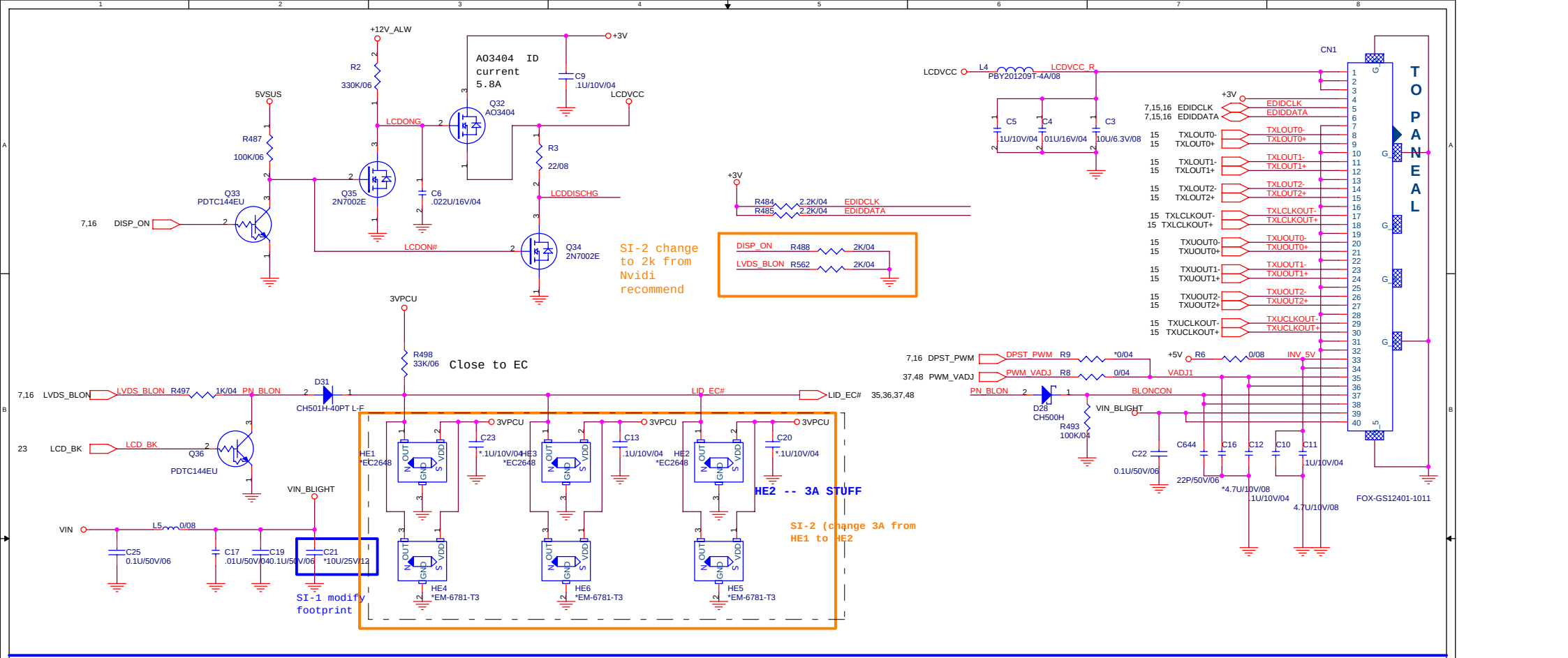


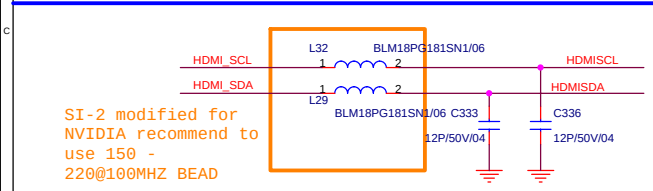
PROJECT : AT3
Quanta Computer Inc.

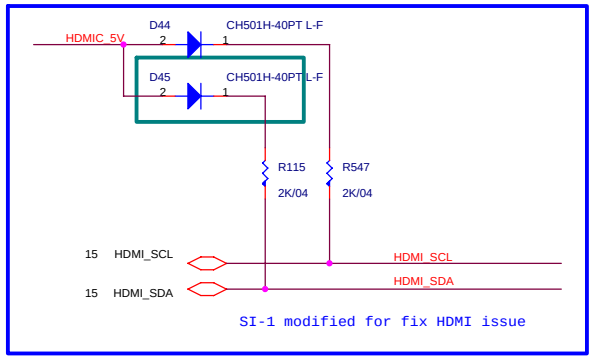
Size	Document Number	Rev
Custom	CRT/TV_OUT	1A

NB5/RD1/HW2

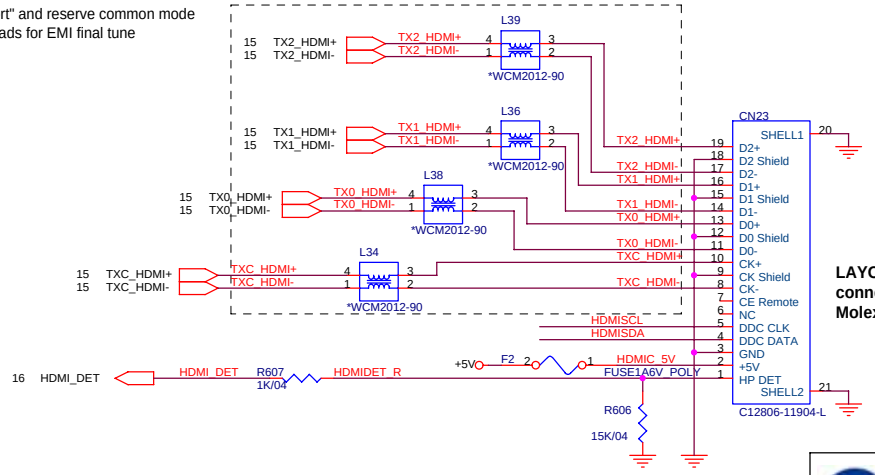
Date: Thursday, January 11, 2007 Sheet 25 of 48





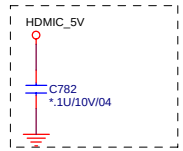


DB "short" and reserve common mode choke pads for EMI final tune



LAYOUT must support connectors from JAE, Molex and Acon.

HDMI PORT



for EMI request

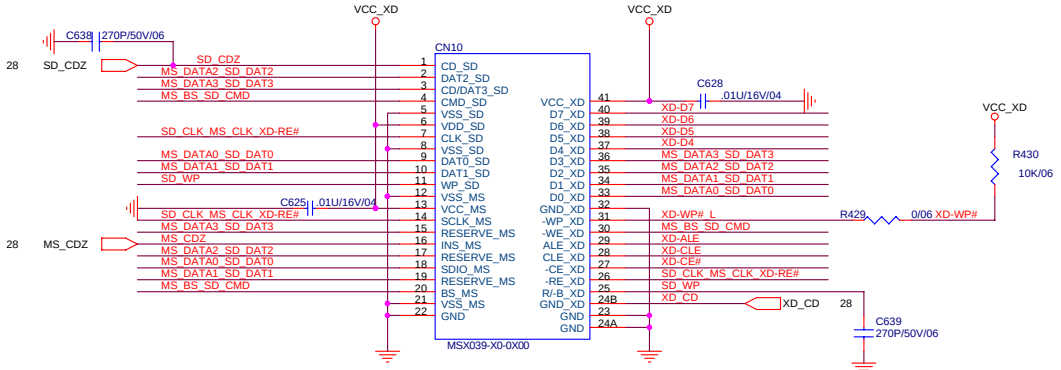
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/HDMI CONN	1A

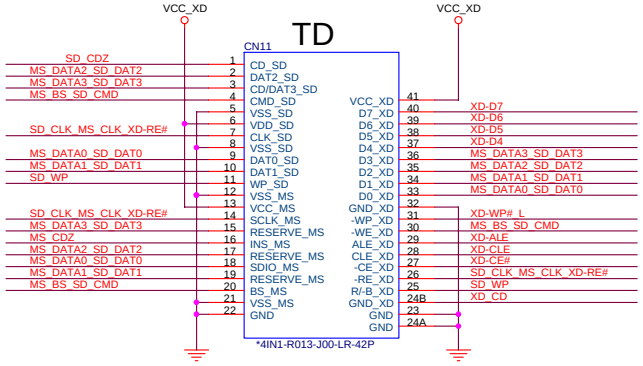
NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 26 of 48

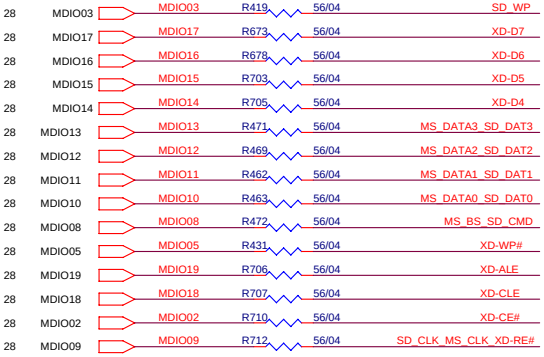
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

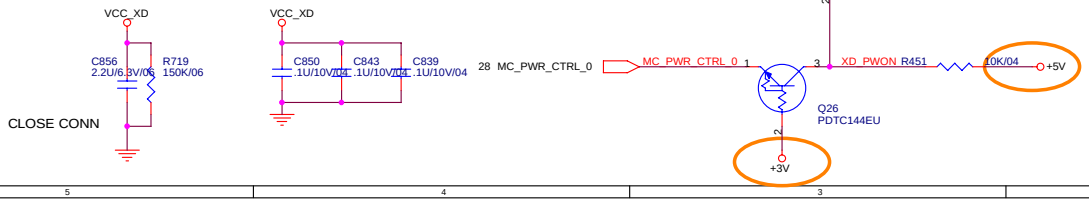


TD

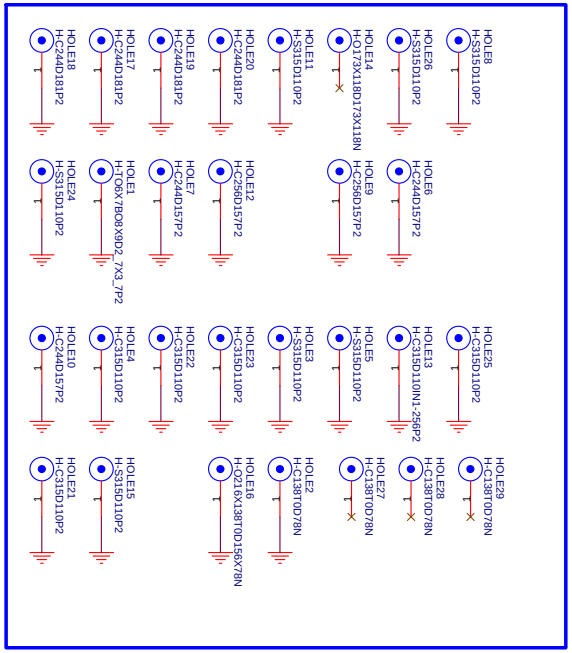


bom create 2'nd source

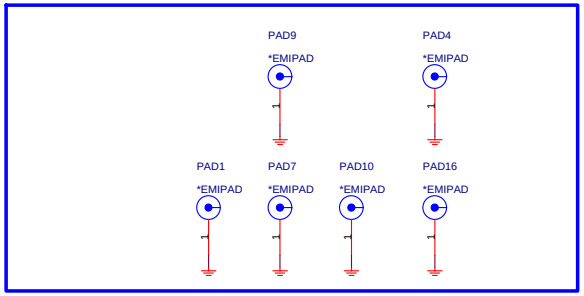


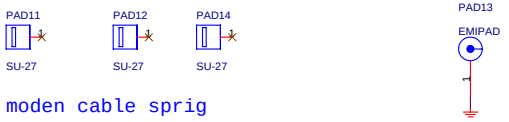


SCREW HOLE



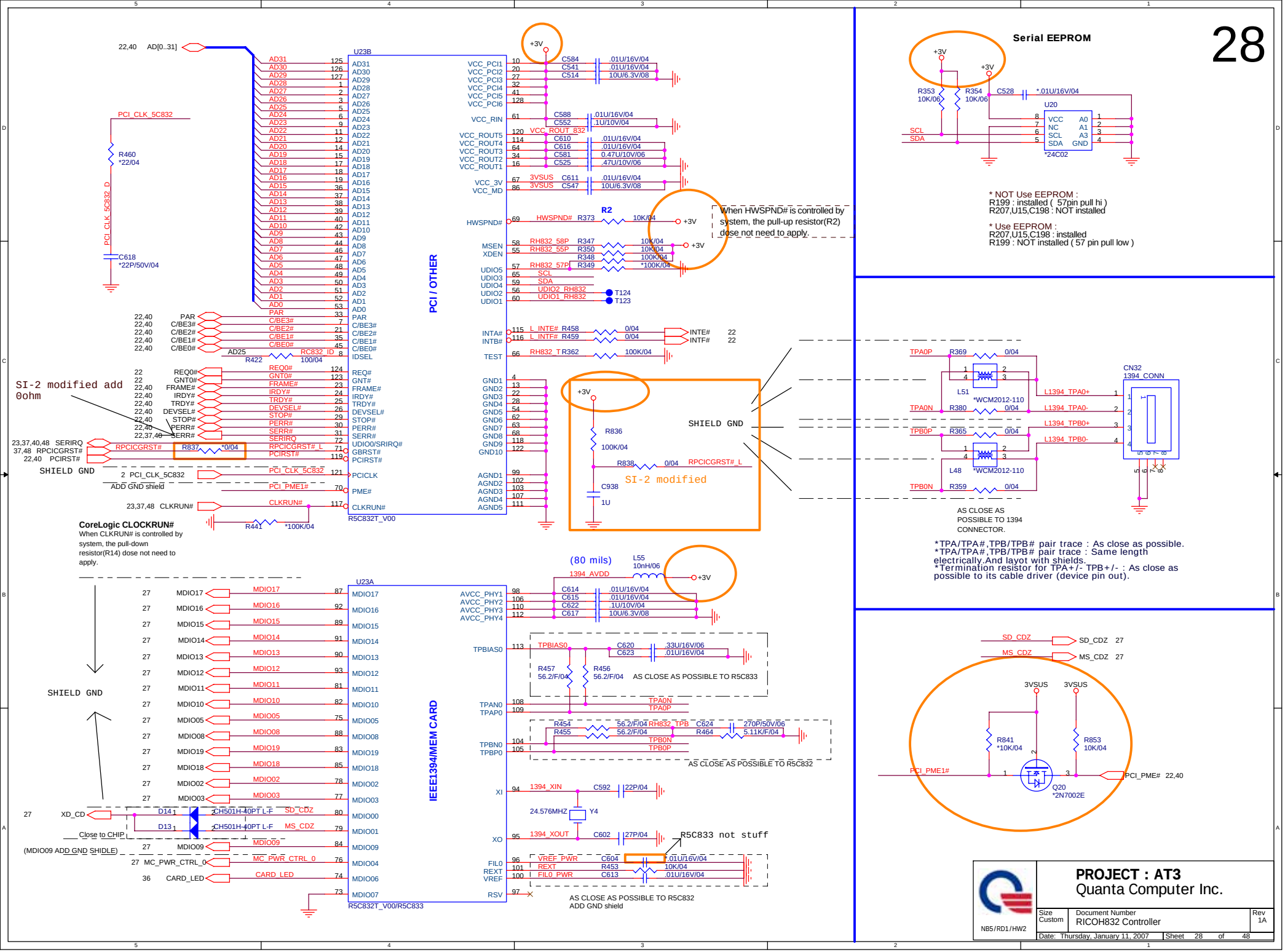
EMI PAD



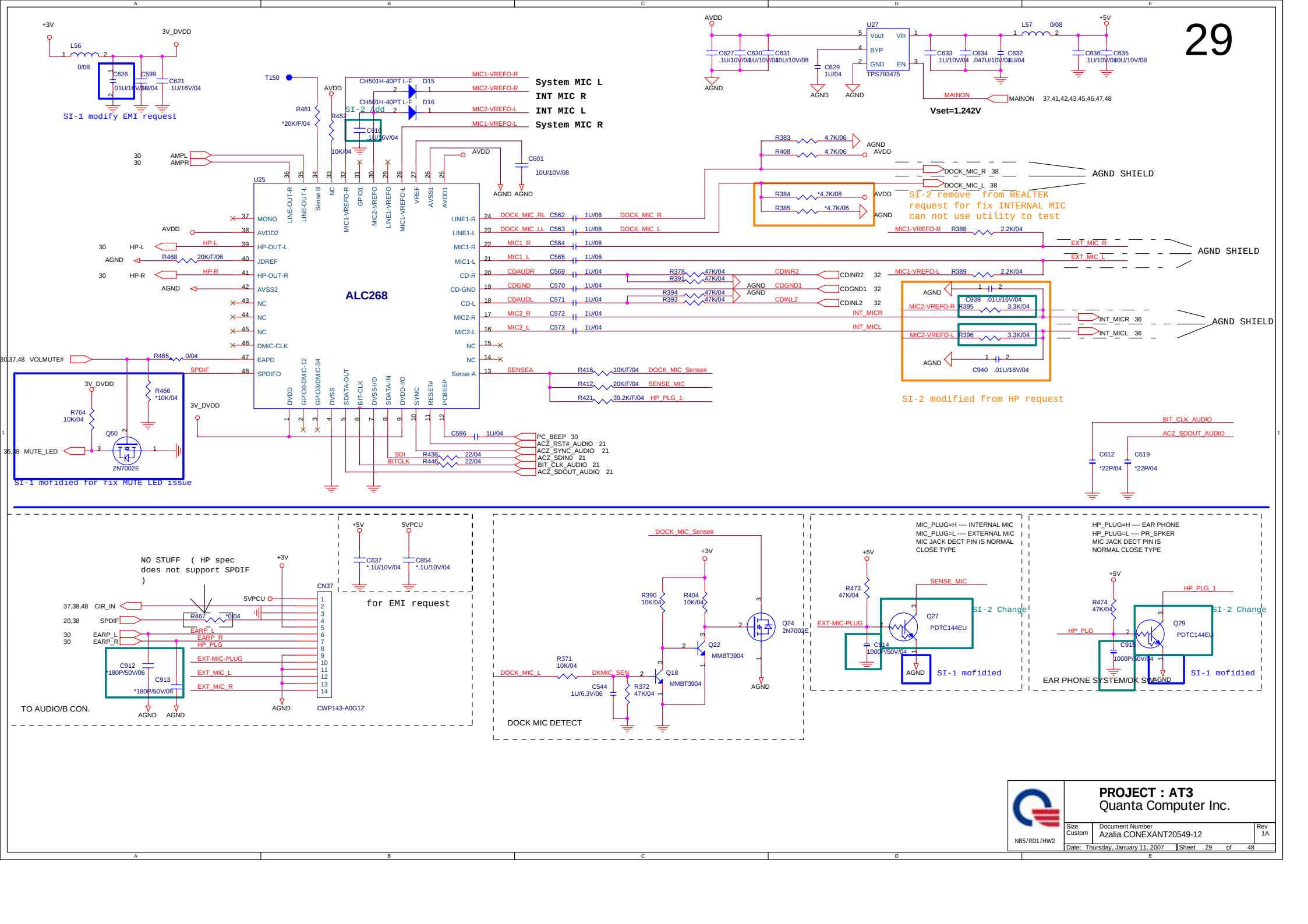


moden cable sprig

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size Custom	Document Number CARD READER/HOLE	Rev 1A
Date: Thursday, January 11, 2007	Sheet 27 of 48	



PROJECT : AT3		
Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom	Document Number: RICOH832 Controller
	Rev: 1A	
	Date: Thursday, January 11, 2007	Sheet 28 of 48


ALC268
SI-1 modify EMI request
SI-1 modified for fix MUTE LED issue
SI-2 Add
System MIC L
INT MIC R
INT MIC L
System MIC R
Vset=1.242V
SI-2 remove from REALTEK request for fix INTERNAL MIC can not use utility to test
AGND SHIELD
SI-2 modified from HP request
NO STUFF (HP spec does not support SPDIF)
for EMI request
TO AUDIO/B CON.
DOCK MIC DETECT
MIC_PLUG=H ---- INTERNAL MIC
MIC_PLUG=L ---- EXTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE
HP_PLUG=H ---- EAR PHONE
HP_PLUG=L ---- PR_SPKER
MIC JACK DECT PIN IS NORMAL CLOSE TYPE
SI-2 Change
SI-1 mofidied
EAR PHONE SYSTEM/DK SW
PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Azalia CONEXANT20549-12
Thursday, January 11, 2007

AUDIO AMPLIFIER

INT. SPEAKER

SI-2 remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

SI-1 ADD EMI request

EMI requests change footprint
SI-1 DEL EMI request

EMI requests change footprint
SI-1 DEL EMI request

EMI requests change footprint
SI-1 ADD EMI request

PCSPK BEEP

TO CODE

TO AMP

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

(AMP BEEP ENABLE AT SYSTEM BOOT)
H=ENABLE
L=DISABLE

LINE OUT Amplifier

LINE OUT Amplifier

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

SI-2 modified from HP recommend

QFN20-4X4-5-25P

PROJECT : AT3
Quanta Computer Inc.

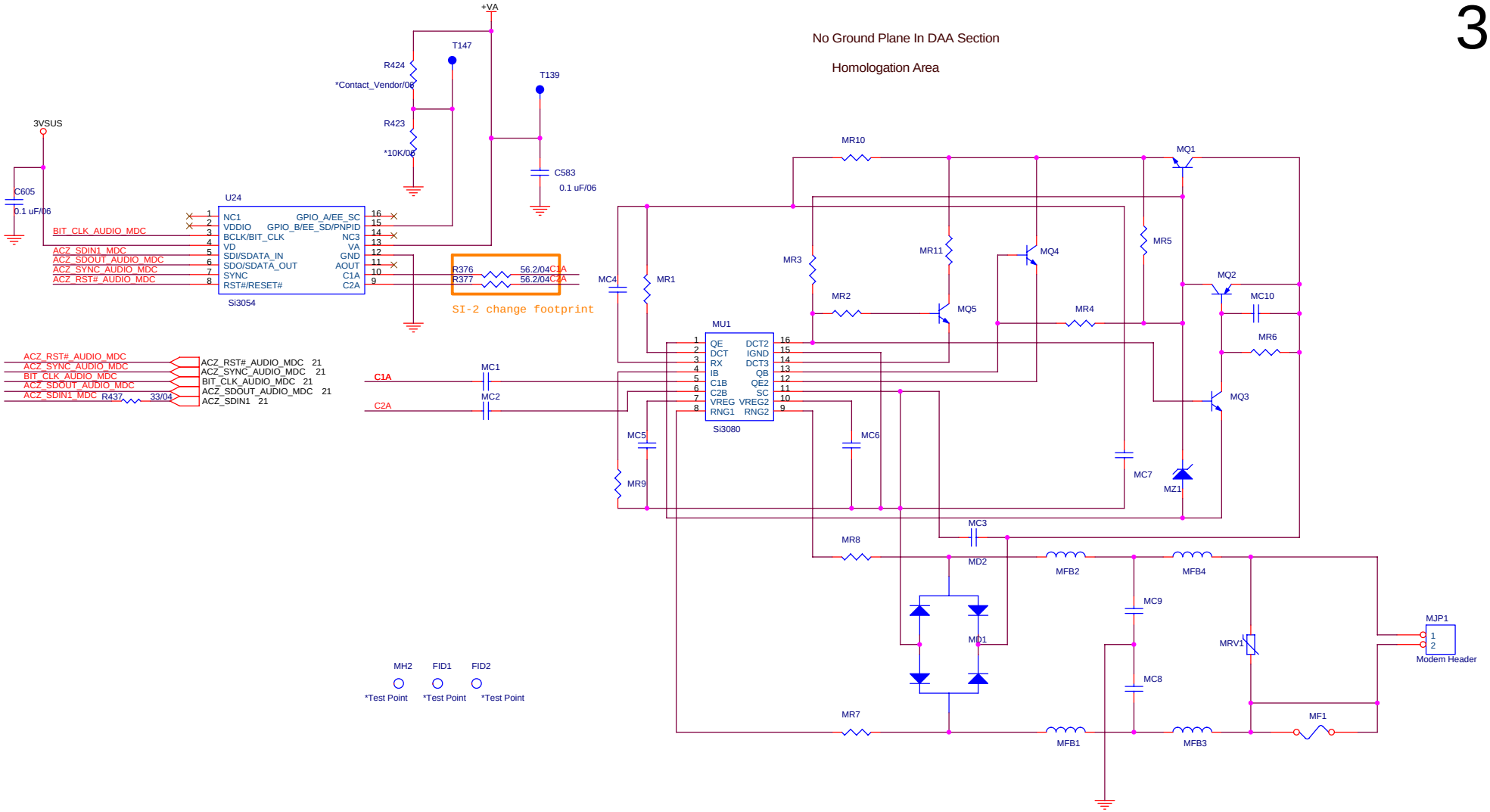
Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

Date: Thursday, January 11, 2007 Sheet 30 of 48

NB5/RD1/HW2

No Ground Plane In DAA Section

Homologation Area

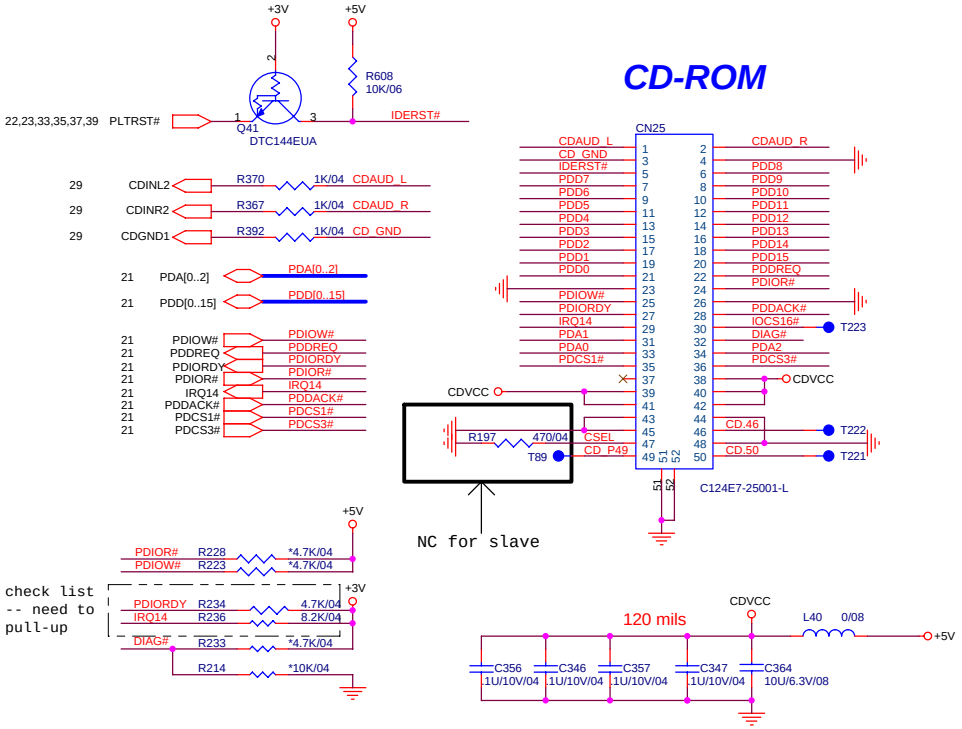


DESIGN SUBJECT TO CHANGE

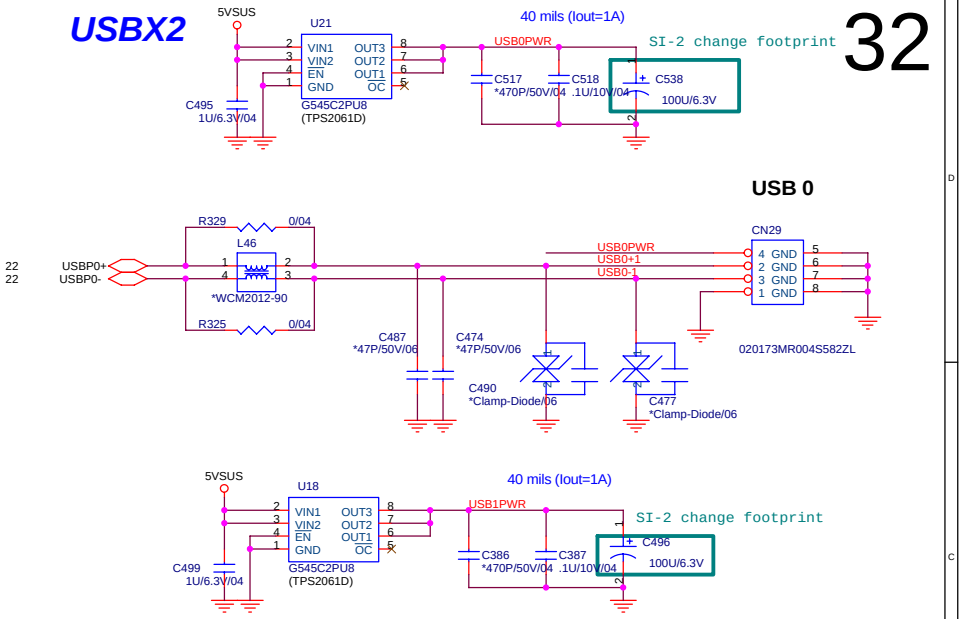
SILICON LABORATORIES CONFIDENTIAL

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: MODEM(DAA)	Rev: 1A
Date: Thursday, January 11, 2007	Sheet 31 of 48	

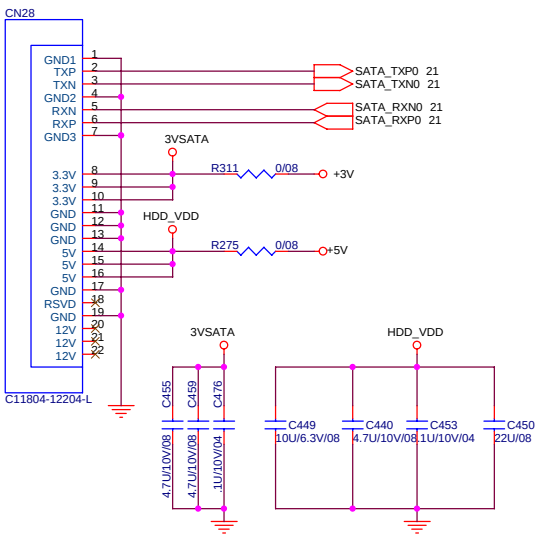
CD-ROM



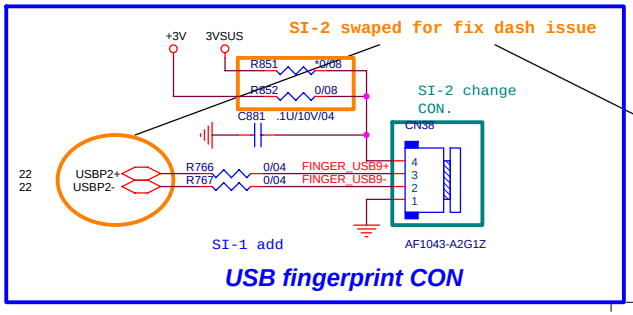
USBX2



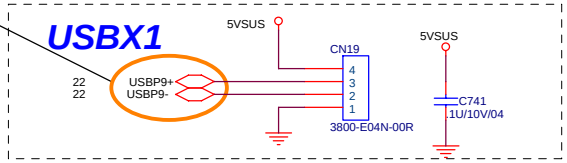
SATA_1 CONNECTOR



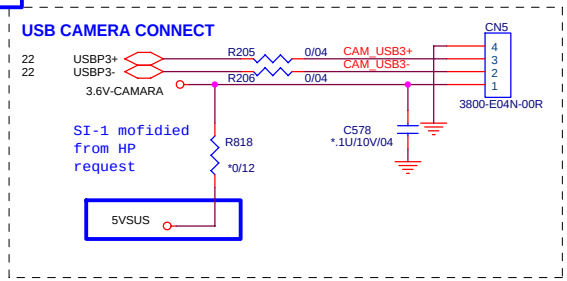
USB fingerprint CON

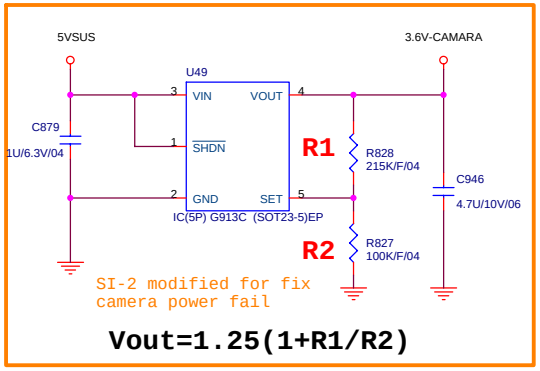


USBX1



USB CAMERA CONNECT





PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A

Date: Thursday, January 11, 2007 Sheet 32 of 48

NB5/RD1/HW2

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix
10/100 LAN LED issue

R345 0/04

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

U19 RTL8111B/8111C/8101E

for 93C56 used. NC if 93C46 is used.

U22 93C46-3GR

R407 *10K/04

R381 3.6K/06

R356 1K/04

R355 15K/04

R358 *0/F/06

ISOLATEB

LAN_DISABLE# 21

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

BLOCK A is only for RTL8101E application.

Block A

R320 *49.9/F/06

R319 *49.9/F/06

R318 *49.9/F/06

R317 *49.9/F/06

C461 *.01U/16V/04

C460 *.01U/16V/04

PCIE_WAKE#

LAN_REST

PCIE_TXP2_LAN

PCIE_TXN2_LAN

PCIE_RXN2_LAN_L

PCIE_RXP2_LAN_L

CLK_PCIE_LAN#

CLK_PCIE_LAN

R335 *0/04

R333 0/04

C513 .1U/10V/04

C509 .1U/10V/04

PCIE_RXN2_LAN 22

PCIE_RXP2_LAN 22

CLK_PCIE_LAN# 2

CLK_PCIE_LAN 2

LAN-AGND

RJ45

CN21

C877 *.1U/10V/04

C878 *.1U/10V/04

R154 150/04

R180 150/04

LAN_YLED

LAN_YLED#

LAN_GLED

LAN_GLED#

CN2 3800N-E002-NNN

C100F9-110A4-L

C746 470P/3KV-1808

C745 470P/3KV-1808

CHASSIS GND

SI-1 modified to fix giga LAN LED issue

Remove R70 for 8111B and 8111C

R316 *0/04

R339 0/04

R351 0/04

U14 NS892403/2404

NS892403:GIGABIT

NS892405:10/100

close U6

C398 1000P/3KV

LAN_GLINK10#

LAN_GLINK100#

LAN_GLINK1000#

LAN_TX#

D36 D35 D37 D4

CH501H-40PT L-F

C732 *.1U/10V/04

C256 *.1U/10V/04

C755 1U/10V/04

C754 .01U/16V/04

C127 1U/10V/04

C133 .01U/16V/04

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size Custom | Document Number RTL8111B/8111C/8101E | Rev 1A

Date: Thursday, January 11, 2007 | Sheet 33 of 48

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

LANVCC
1.2W
364mA

LANVCC_L L47 0/08

all component place near lan power mosfet

C539 22U/6.3V/08
C540 .1U/10V/04

LANVCC

C515 .1U/10V/04 C531 .1U/10V/04 C535 .1U/10V/04 C485 .1U/10V/04

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

LAN_A3.3

L45 0/08

C480 .1U/10V/04 C505 .1U/10V/04

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

LANVCC

33 CTRL18

MMJT9435T1 Q19

Only For 8111B application

L52 0/08

LAN_A1.8

C472 .1U/10V/04 C470 .1U/10V/04 C471 .1U/10V/04 C469 .1U/10V/04

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

C561 22U/08 C567 .1U/10V/04

L54 *0/08

C568 22U/08

Only For 8101E application

LAN_E1.8

R361 0/12

C497 .1U/10V/04 C498 .1U/10V/04

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

LAN-AGND

Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

LANVCC

33 CTRL15

MMJT9435T1 Q21

Only For 8111B application

L53 *0/08

C546 22U/08

C586 22U/08 C585 .1U/10V/04

Only For 8101E application

LAN_D1.5

C530 .1U/10V/04 C534 .1U/10V/04 C519 .1U/10V/04 C520 .1U/10V/04 C527 .1U/10V/04 C526 .1U/10V/04 C532 .1U/10V/04 C492 .1U/10V/04 C533 .1U/10V/04 C478 .1U/10V/04

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

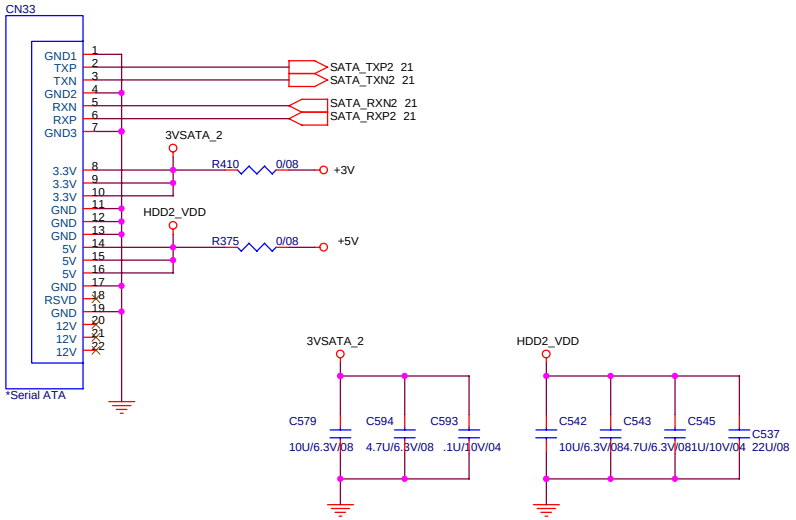
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

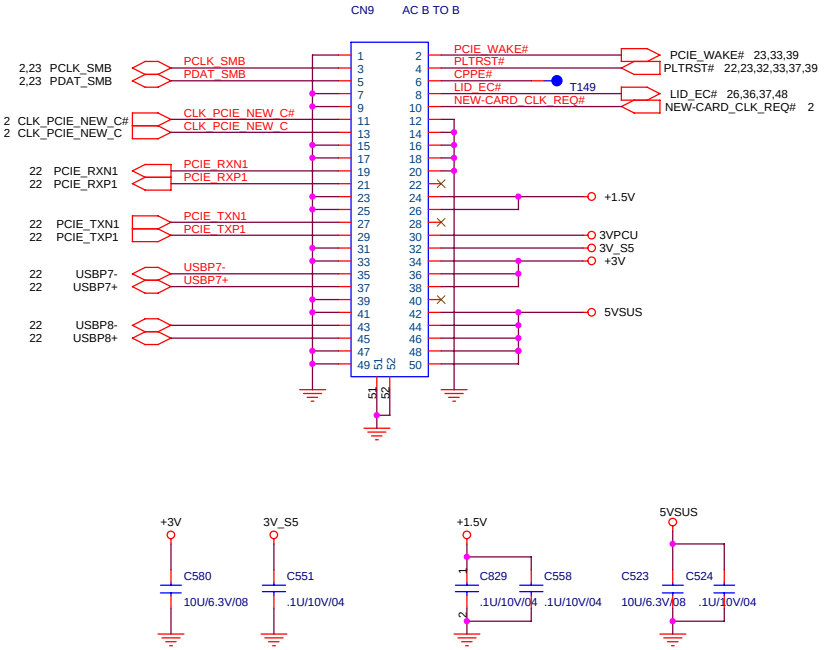
NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 34 of 48

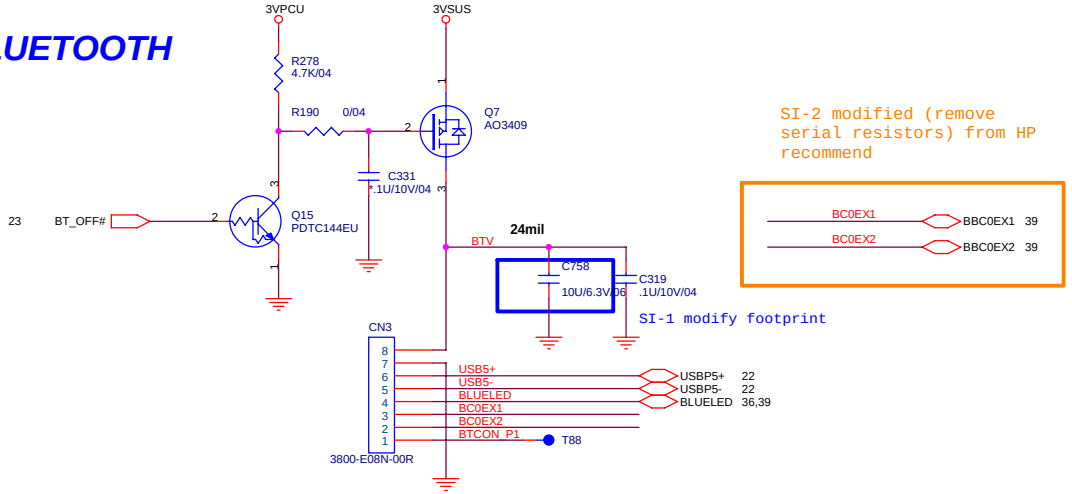
SATA_2 CONNECTOR
For 17"W Second HDD



NEWCARD



BLUETOOTH



SI-2 modified (remove serial resistors) from HP recommend

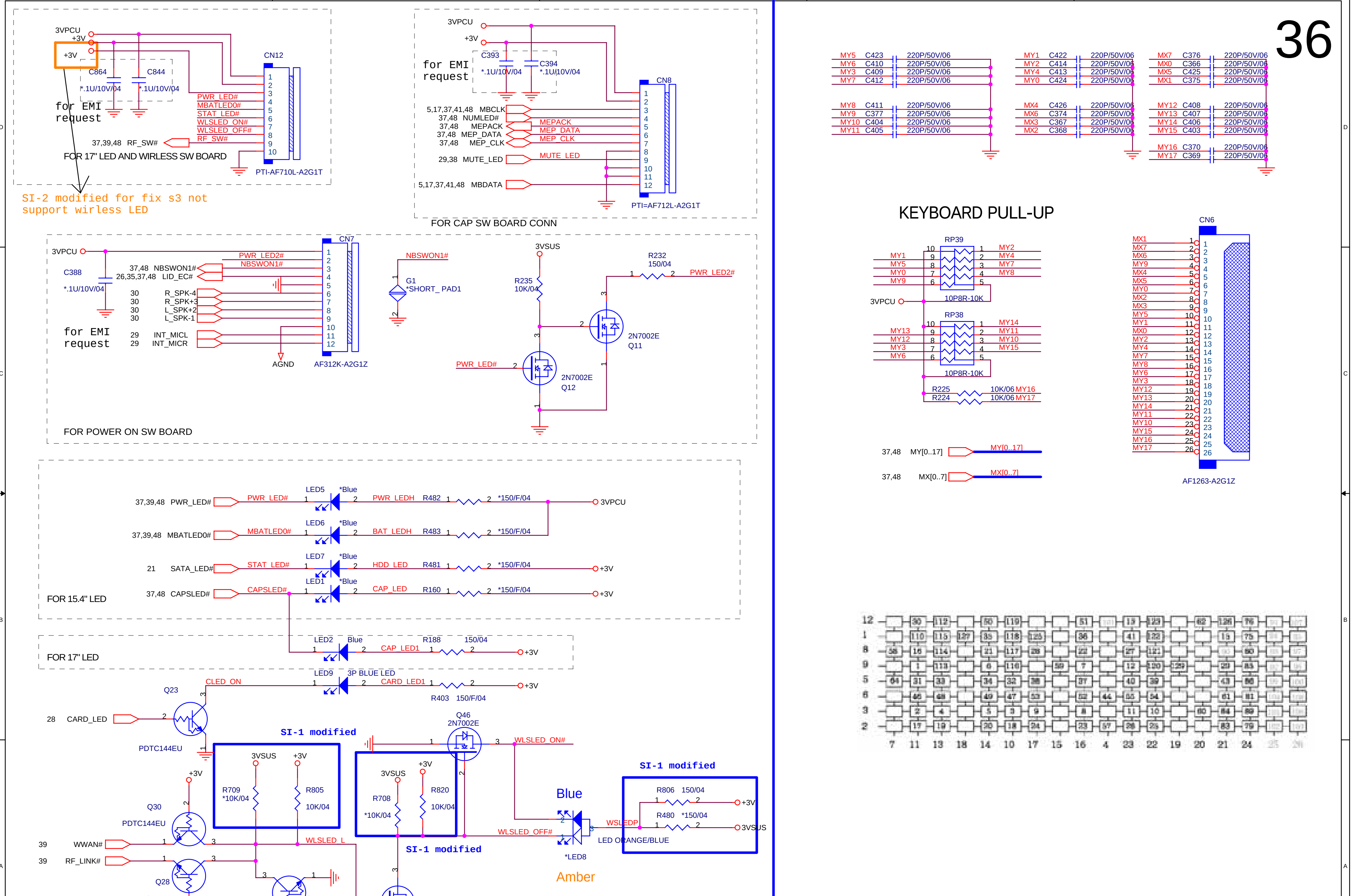
SI-1 modify footprint

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	1A

NB5/RD1/HW2

Date: Thursday, January 11, 2007 Sheet 35 of 48



FOR 17" LED AND WIRELESS SW BOARD
CN12
PTI-AF710L-A2G1T
3VPCU
+3V
C864
C844
*.1U/10V/04
for EMI request
PWR_LED#
MBATLED0#
STAT_LED#
WLSLED_ON#
WLSLED_OFF#
RF_SW#
37,39,48 RF_SW#
SI-2 modified for fix s3 not support wirless LED
FOR CAP SW BOARD CONN
CN8
PTI=AF712L-A2G1T
C393
C394
5,17,37,41,48 MBCLK
37,48 NUMLED#
37,48 MEPACK
37,48 MEP_DATA
37,48 MEP_CLK
29,38 MUTE_LED
5,17,37,41,48 MBDATA
MEPACK
MEP_DATA
MEP_CLK
MUTE_LED
FOR POWER ON SW BOARD
CN7
AF312K-A2G1Z
C388
37,48 NBSWON1#
26,35,37,48 LID_EC#
30 R_SPK-
30 R_SPK+
30 L_SPK+
30 L_SPK-
29 INT_MICL
29 INT_MICR
AGND
PWR_LED2#
NBSWON1#
G1
*SHORT_PAD1
3VSUS
R235
10K/04
R232
150/04
2N7002E
Q11
Q12
KEYBOARD PULL-UP
RP39
RP38
10P8R-10K
R225
R224
10K/06
CN6
AF1263-A2G1Z
37,48 MY[0..17]
37,48 MX[0..7]
220P/50V/06
FOR 15.4" LED
LED5
LED6
LED7
LED1
*Blue
37,39,48 PWR_LED#
37,39,48 MBATLED0#
21 SATA_LED#
37,48 CAPSLED#
PWR_LEDH
BAT_LEDH
HDD_LED
CAP_LED
R482
R483
R481
R160
*150/F/04
FOR 17" LED
LED2
Blue
CAP_LED1
R188
150/04
LED9
3P BLUE LED
CARD_LED1
R403 150/F/04
Q23
CLED_ON
28 CARD_LED
PDTC144EU
SI-1 modified
R709
*10K/04
R805
10K/04
R708
R820
Q46
2N7002E
WLSLED_ON#
WLSLED_OFF#
WLSLED_L
Blue
Amber
*LED8
LED ORANGE/BLUE
WSLEDP
R806 150/04
R480 *150/04
Q30
Q28
Q44
Q45
Q31
39 WWAN#
39 RF_LINK#
35,39 BLUELED
R476 150/04
23 BTLED
FOR WIRLESS LED

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

Date: Thursday, January 11, 2007 Sheet 36 of 48

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

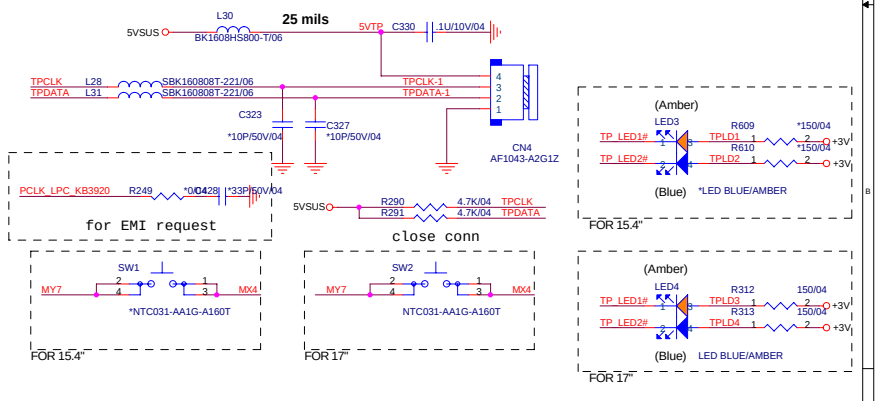
All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

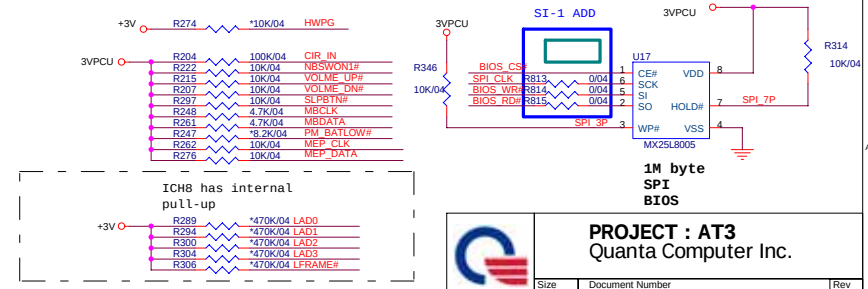
SELECT KBC TPYE

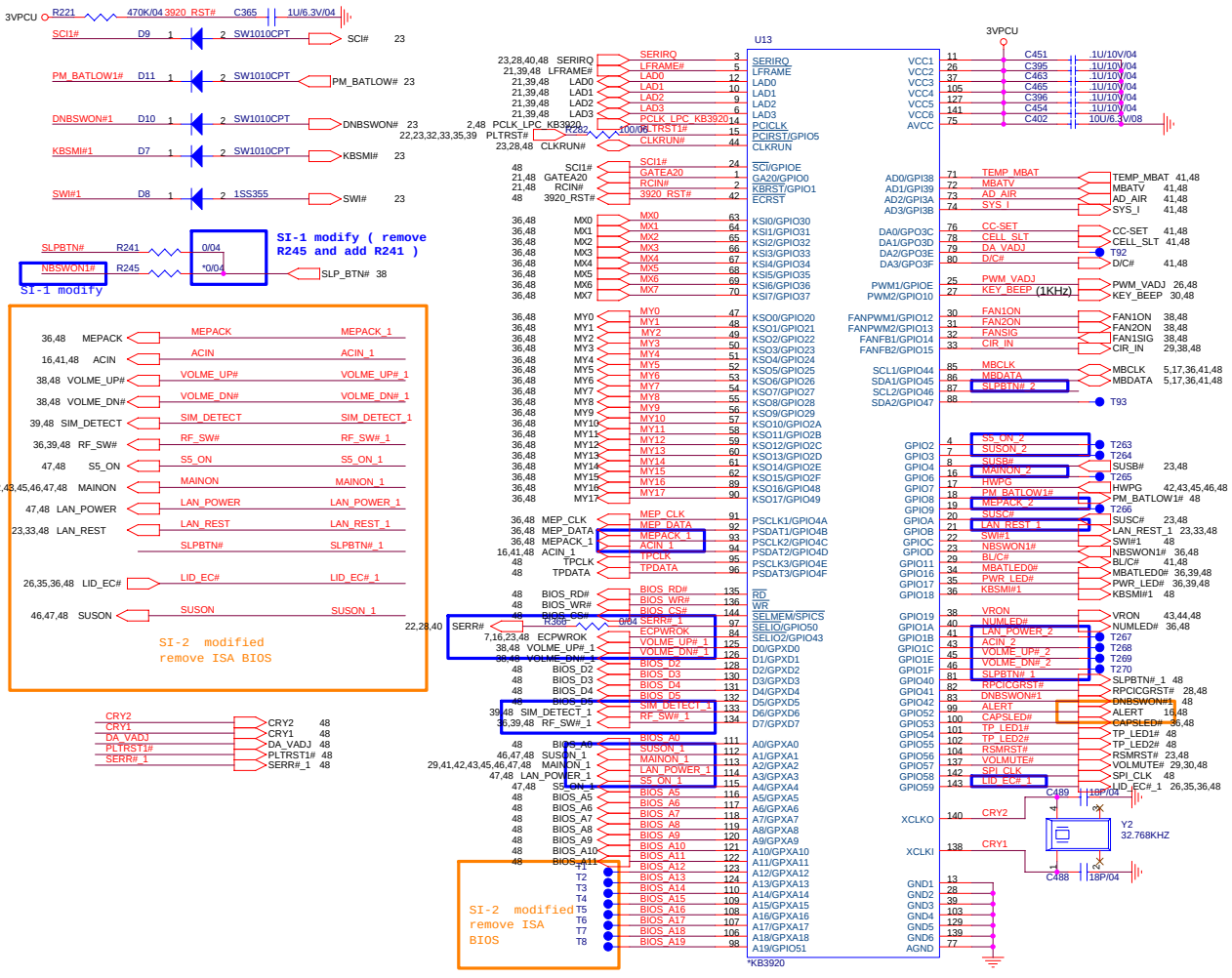
PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR

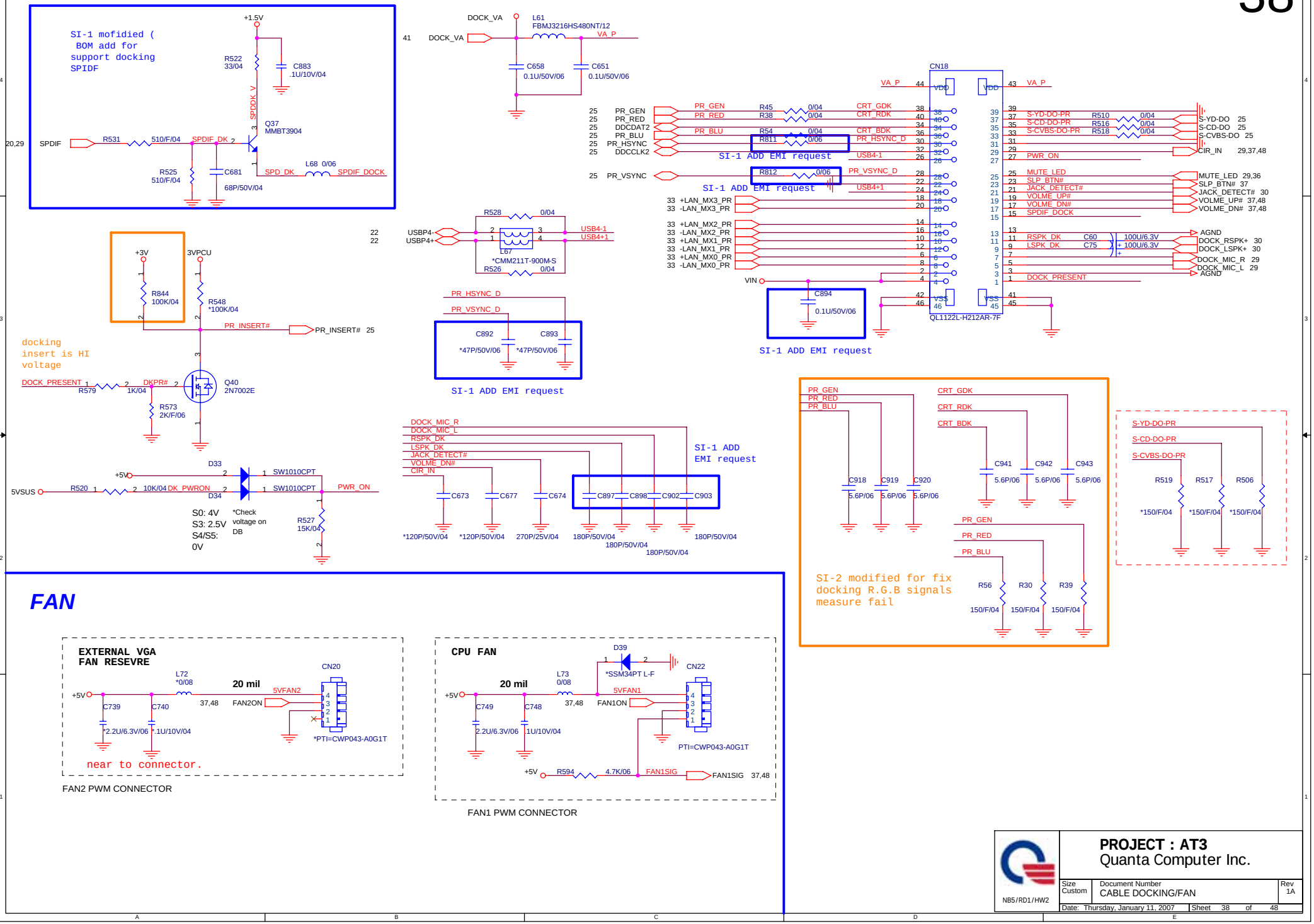






CABLE DOCK

support 6A 200mils
CX000480005



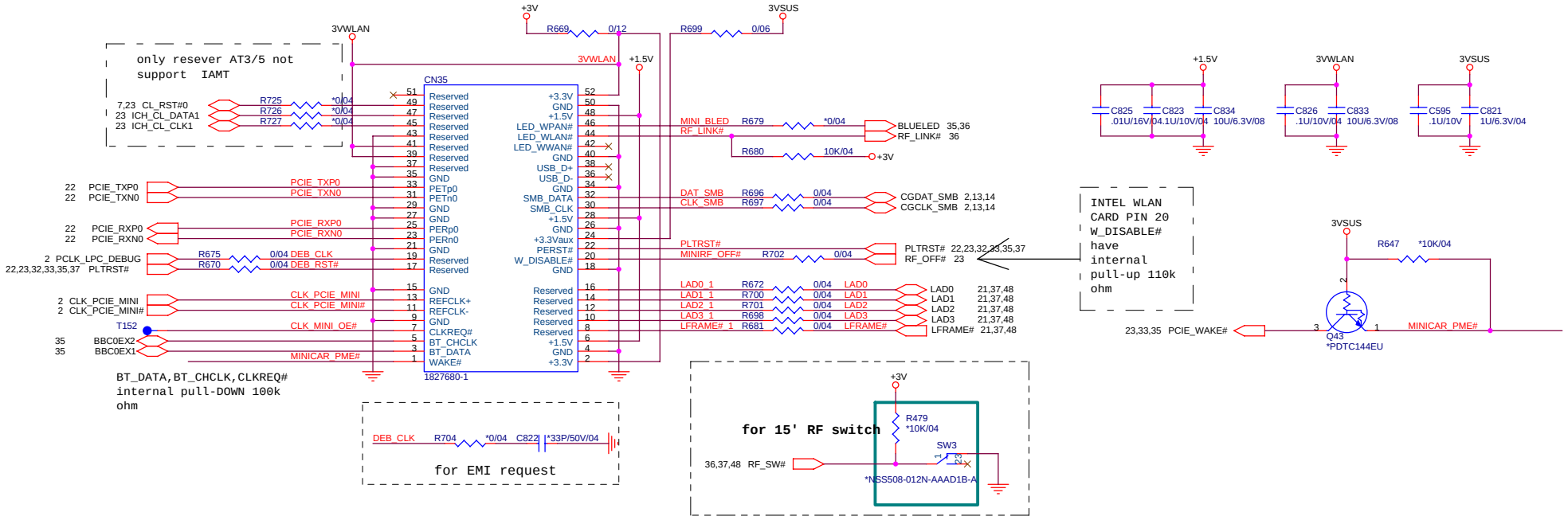
FAN

FAN2 PWM CONNECTOR

FAN1 PWM CONNECTOR

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: CABLE DOCKING/FAN	Rev: 1A
Date: Thursday, January 11, 2007	Sheet 38 of 48	

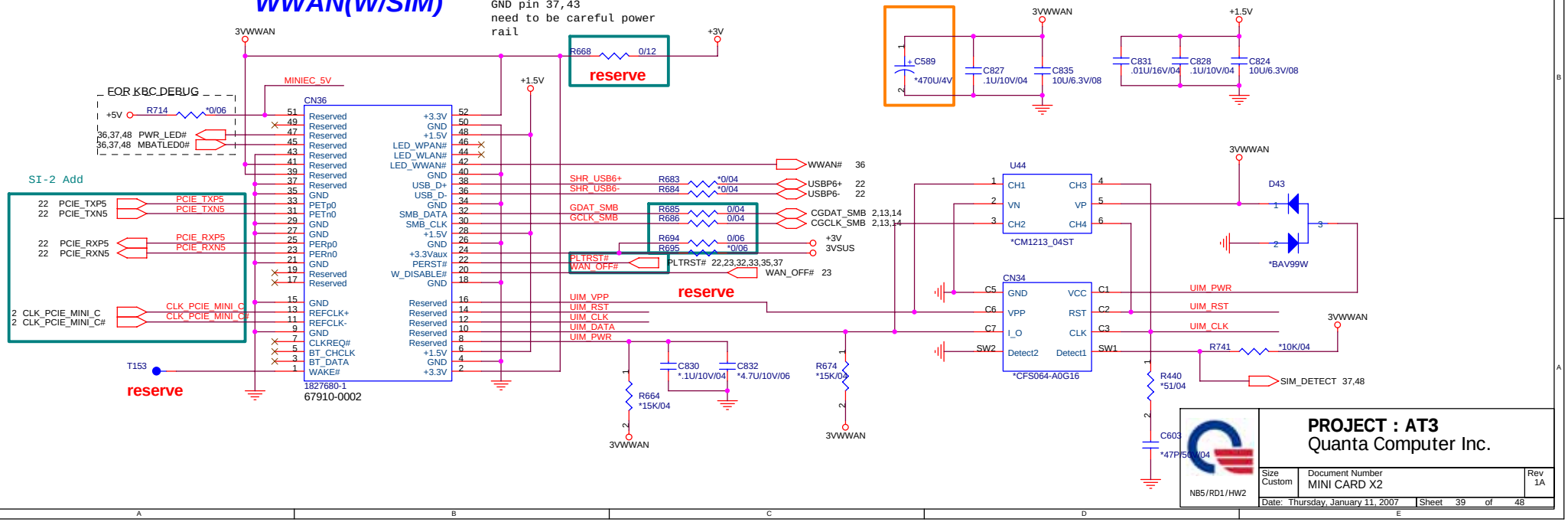
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

SI-2 modified
(BOM remove C589
)



PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI CARD X2	1A

NB5/RD1/HW2

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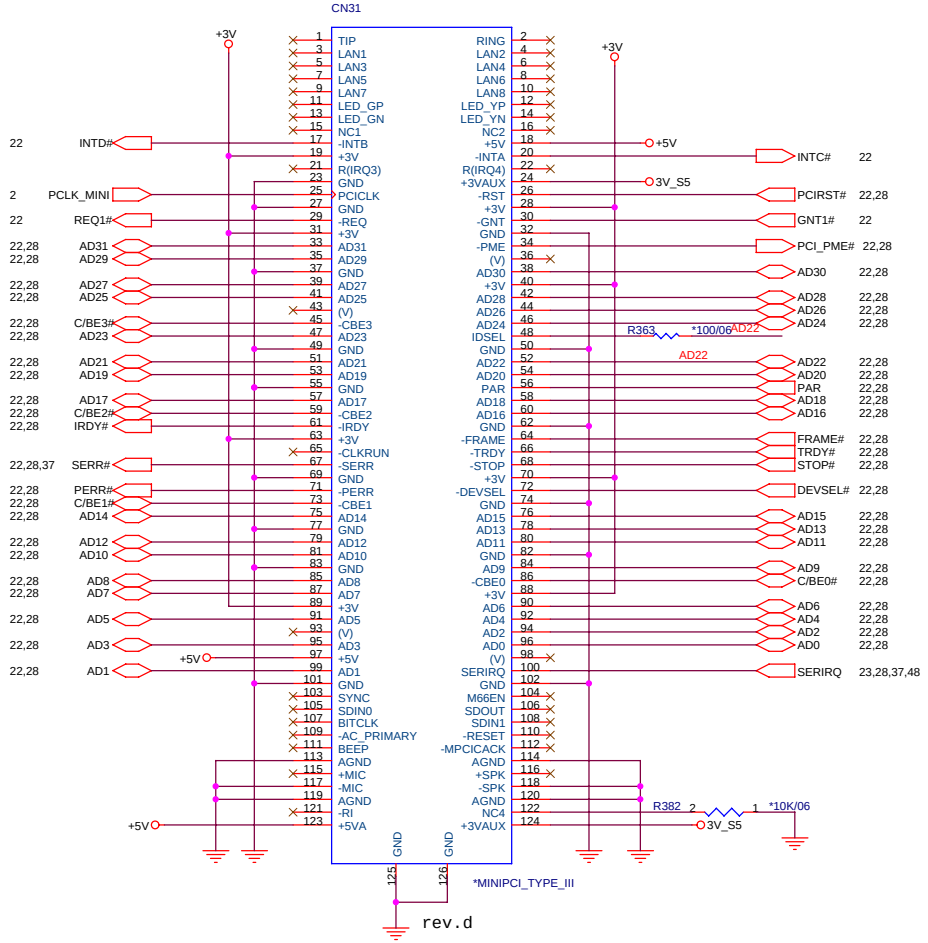
MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



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Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI TYPE III SLOT
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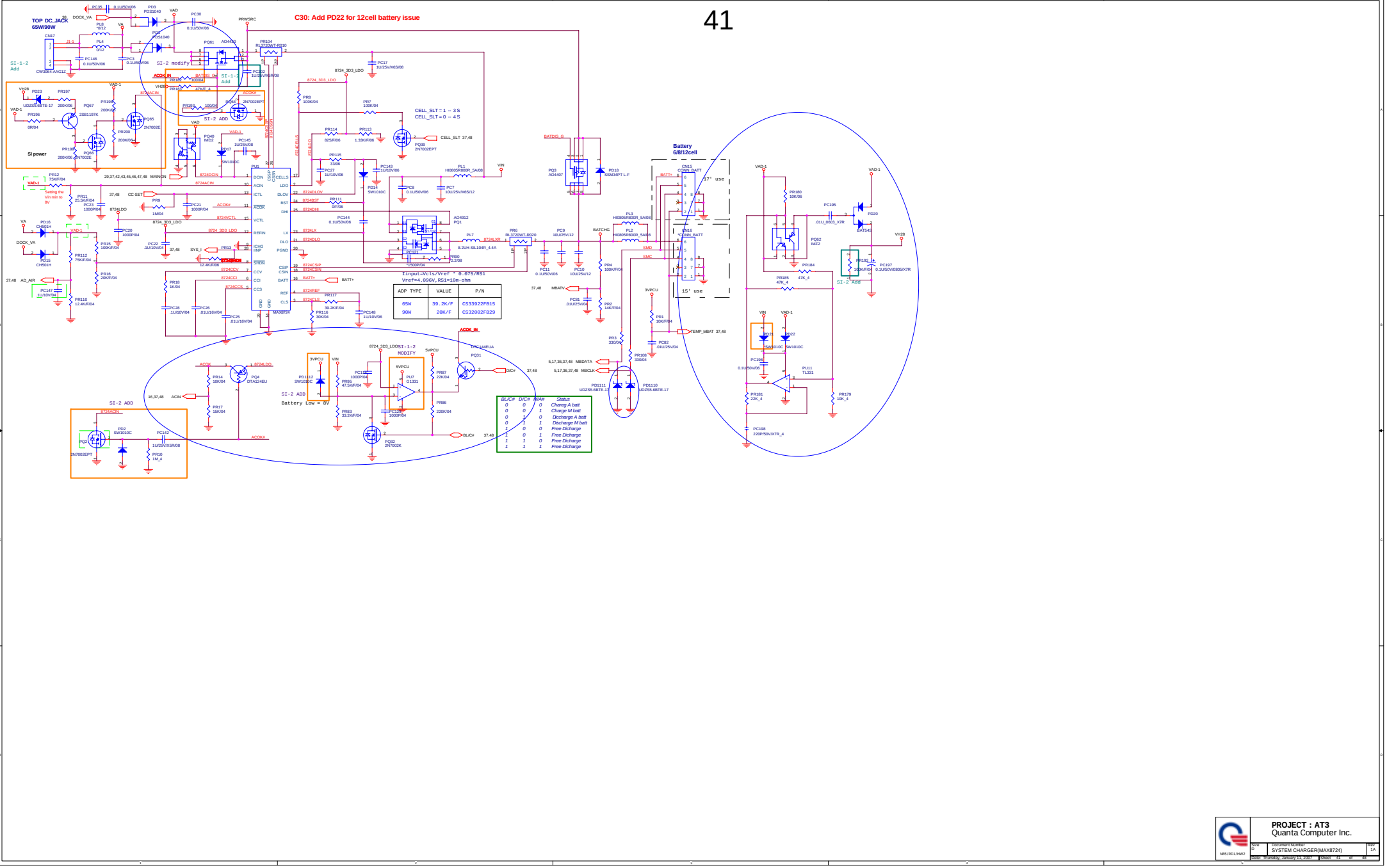
C30: Add PD22 for 12cell battery issue
TOP DC_JACK
65W/90W
SI-1-2 Add
SI-2 modify
SI-2 ADD
SI power
Battery 6/8/12cell
17' use
15' use
CELL_SLT = 1 ~ 3 S
CELL_SLT = 0 ~ 4 S
Iinput=Vcls/Vref * 8.875/RS1
Vref=4.096V,RS1=10m-ohm
ADP TYPE | VALUE | P/N
65W | 39.2K/F | CS33922FB15
90W | 20K/F | CS32002FB29
Battery Low = 8V
BL/C# D/C# 90A# Status
0 0 0 Charg A batt
0 0 1 Charge M batt
0 1 0 Discharge A batt
0 1 1 Discharge M batt
1 0 0 Free Dicharge
1 0 1 Free Dicharge
1 1 0 Free Dicharge
1 1 1 Free Dicharge
MAX8724
PROJECT : AT3
Quanta Computer Inc.
NB5/R01/HW2
SYSTEM CHARGER(MAX8724)
Thursday, January 11, 2007

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

Rds(on) 15m ohm

Max Power Consumption 1.6W

For G73 Only

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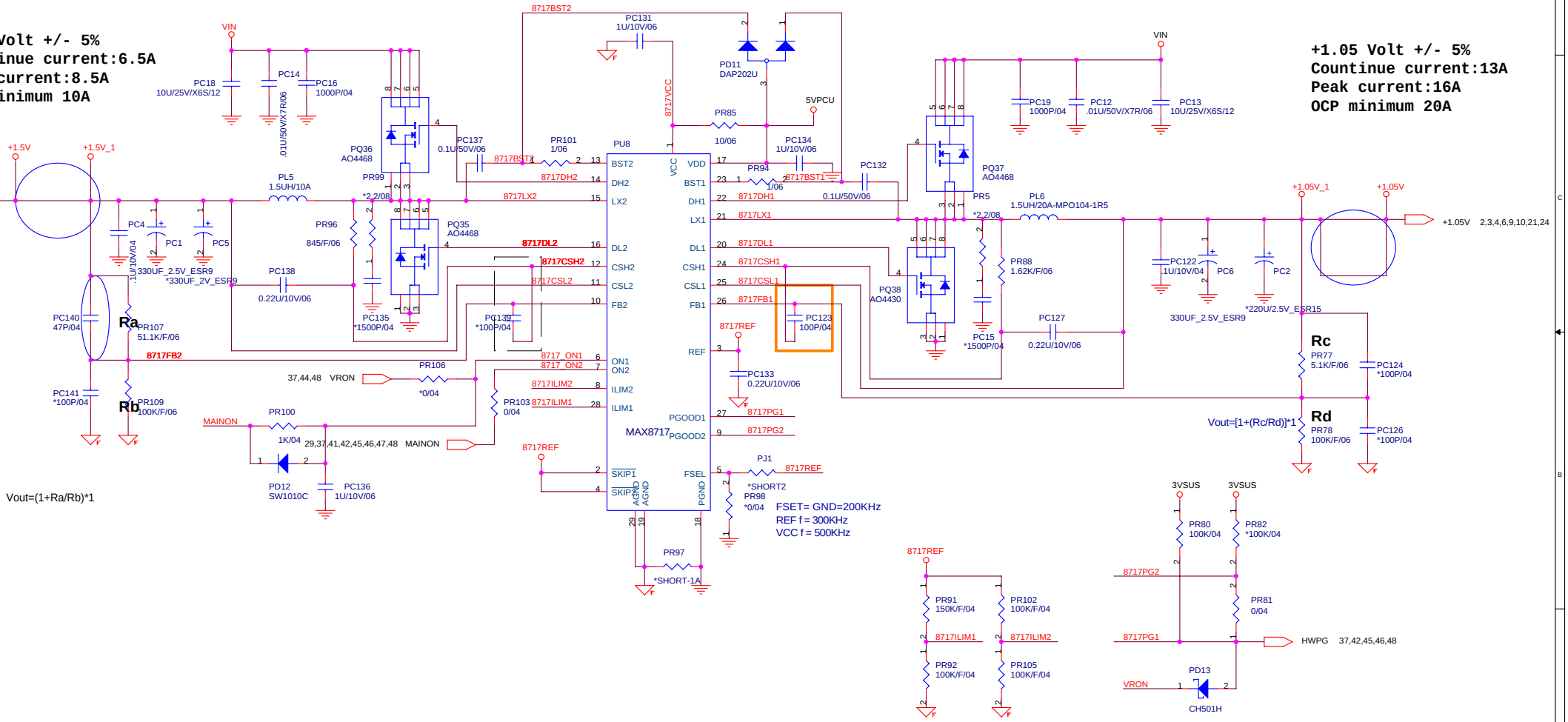
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.		
	Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
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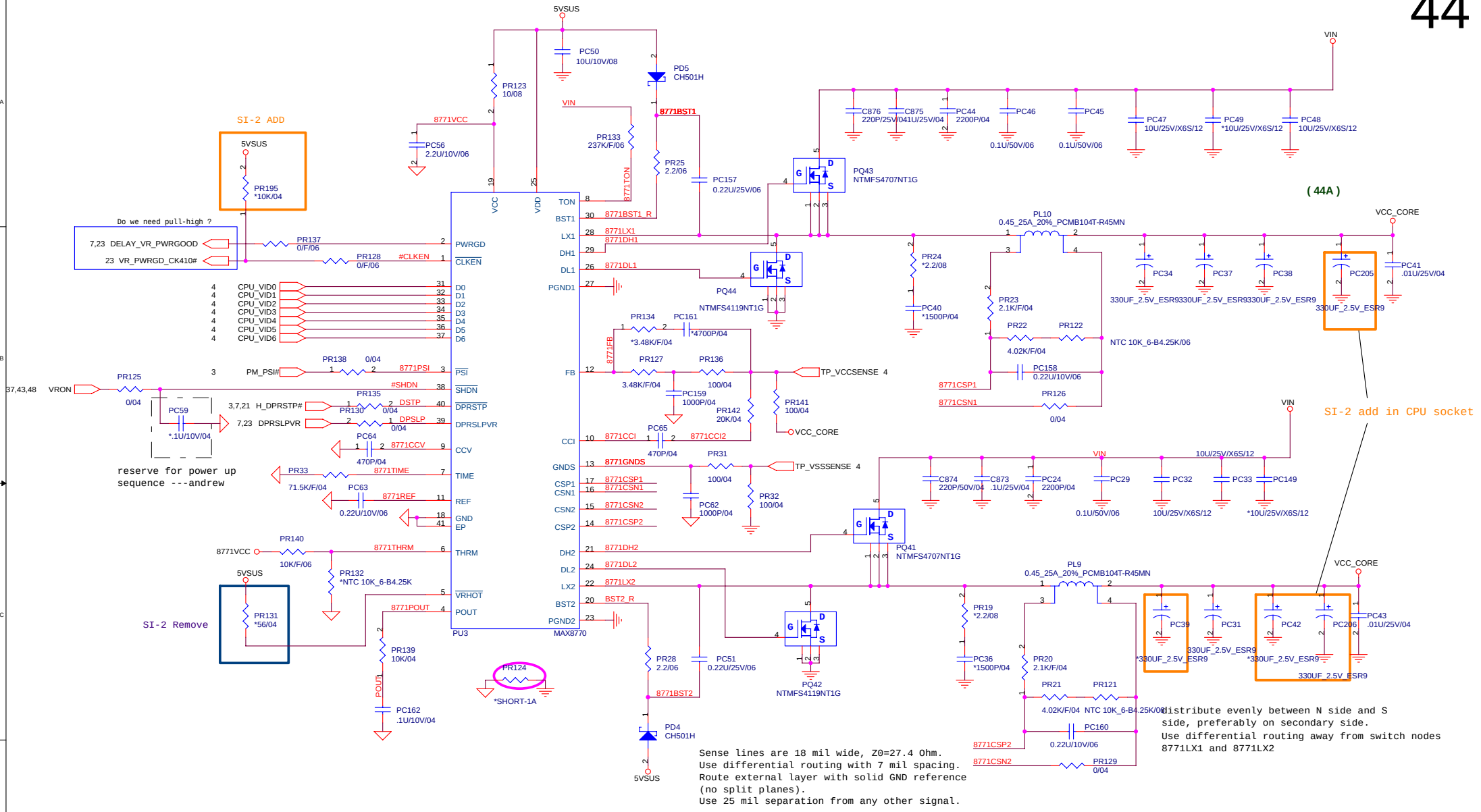

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size Custom	Document Number CPU_CORE(MAX8771)	Rev 1A
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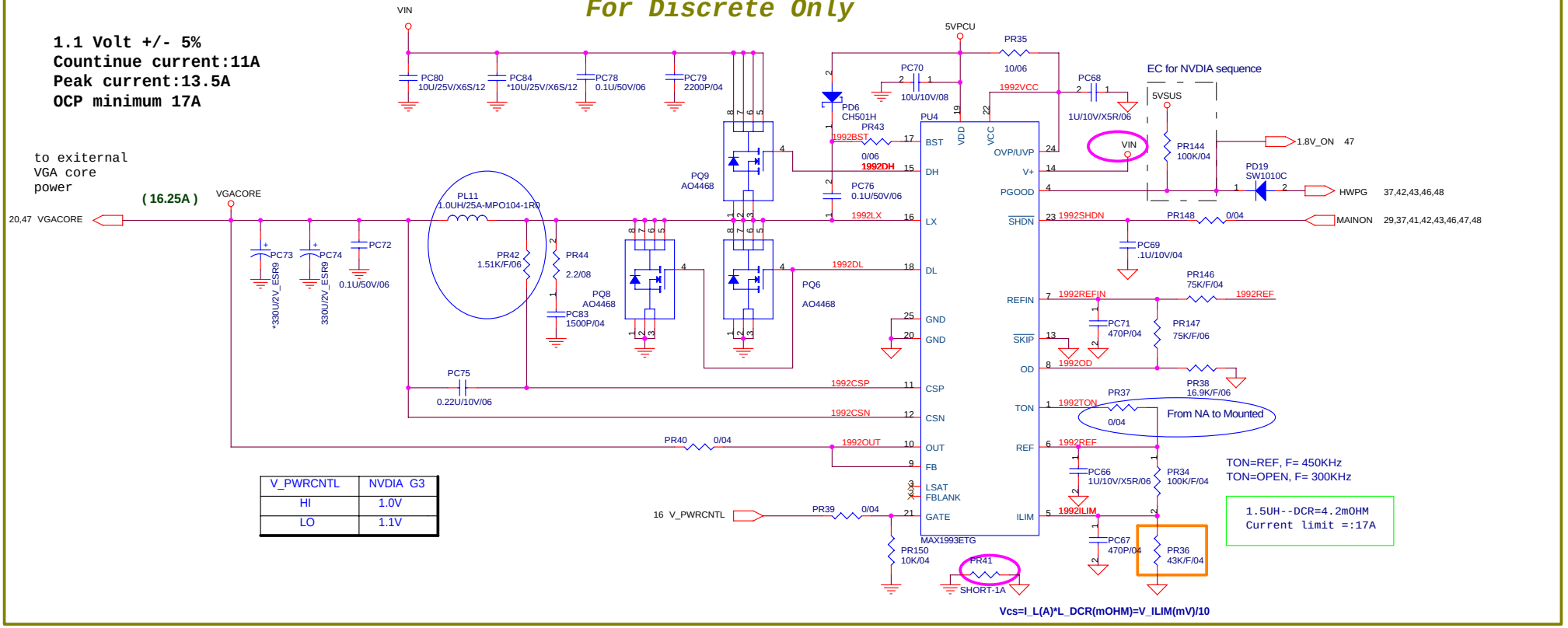
For Discrete Only

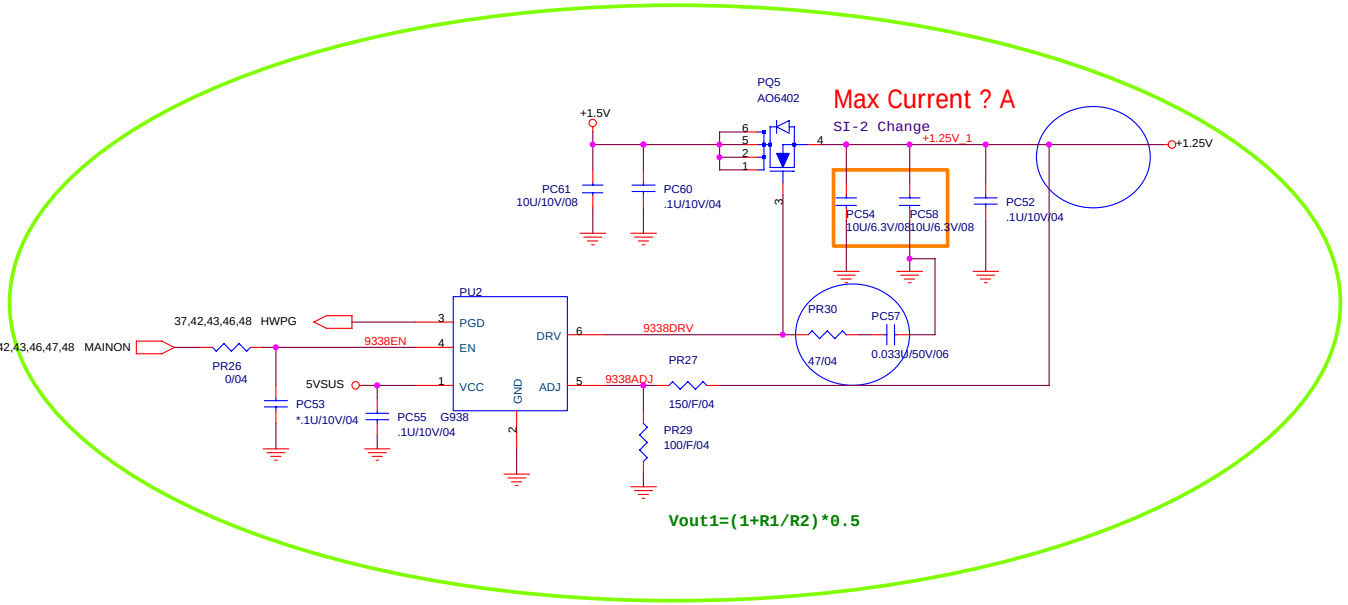
1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

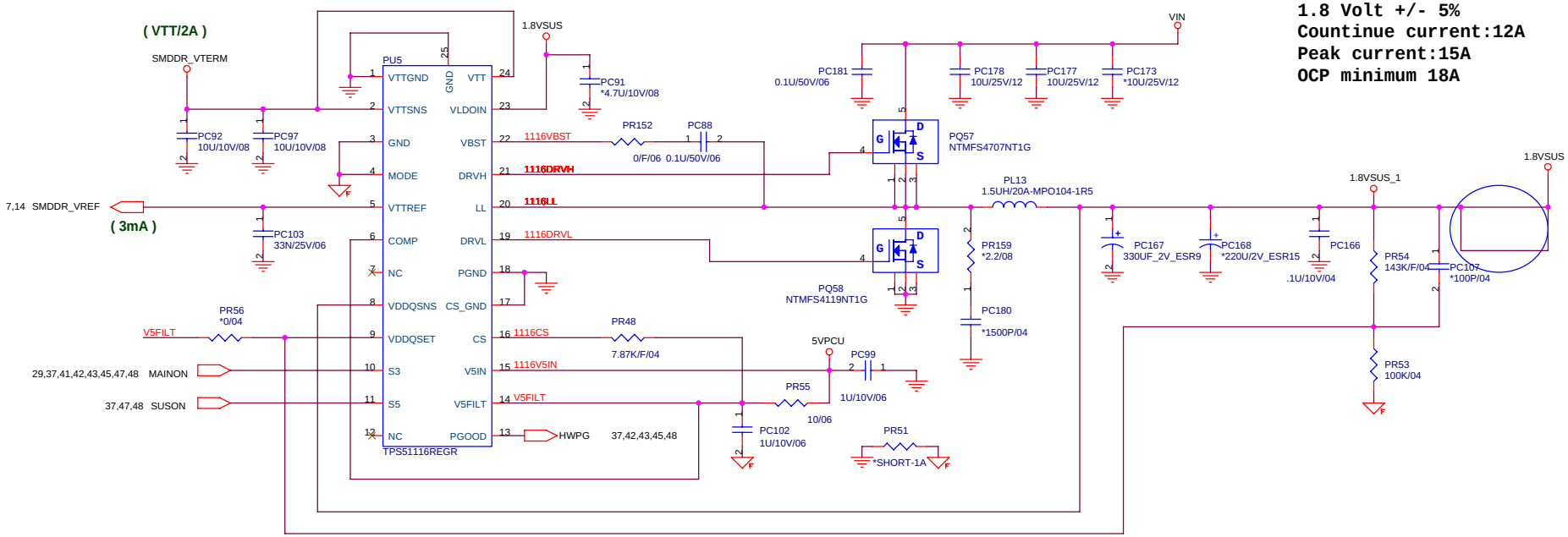
to exiternal
VGA core
power

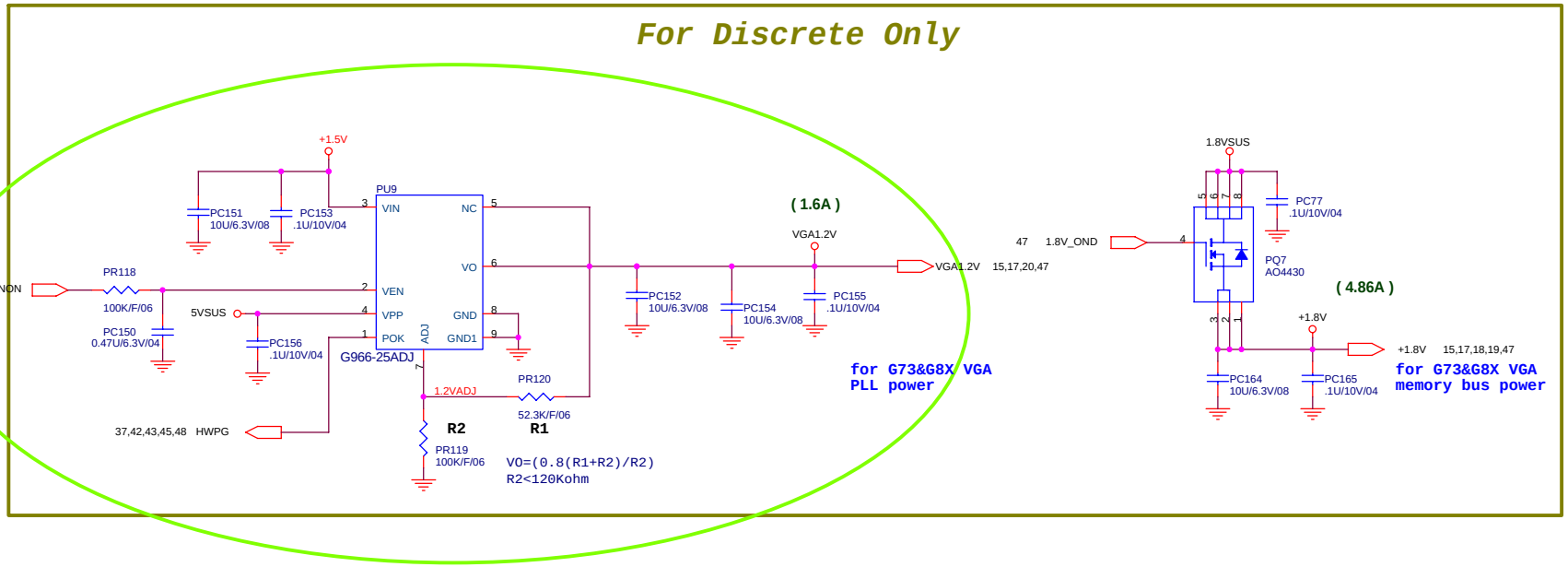
(16.25A)



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V







PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	1A

NB5/RD1/HW2

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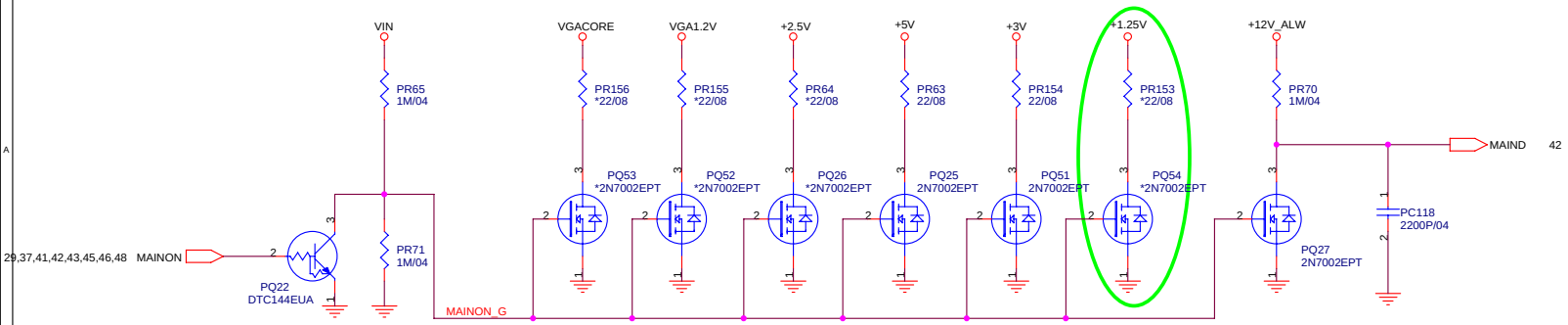
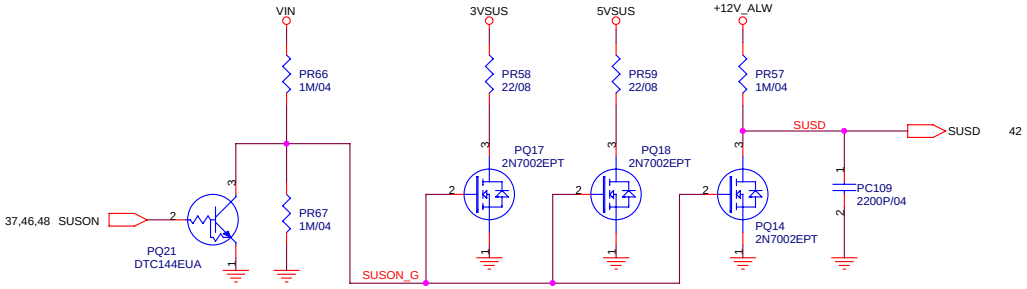
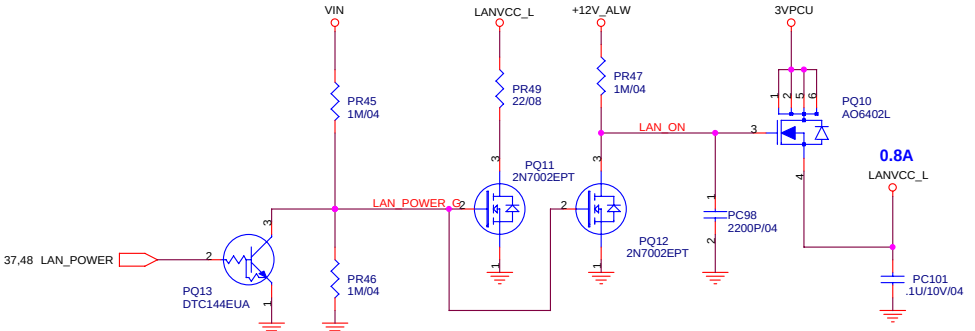
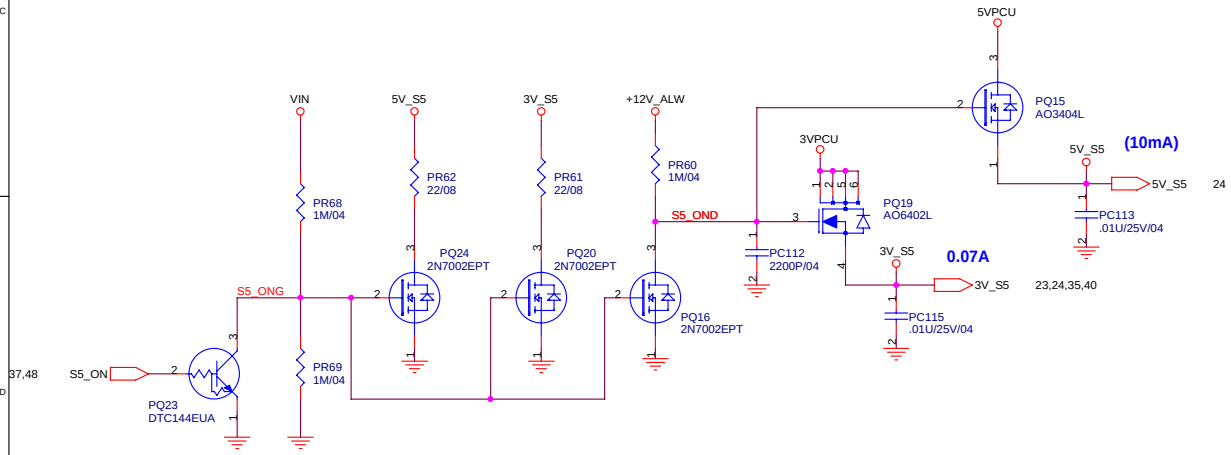
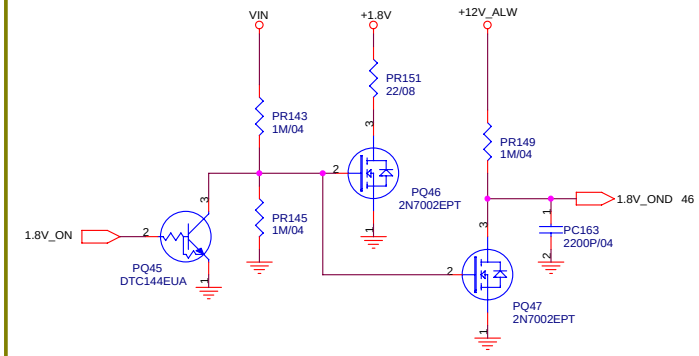








For Discrete Only



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	1A

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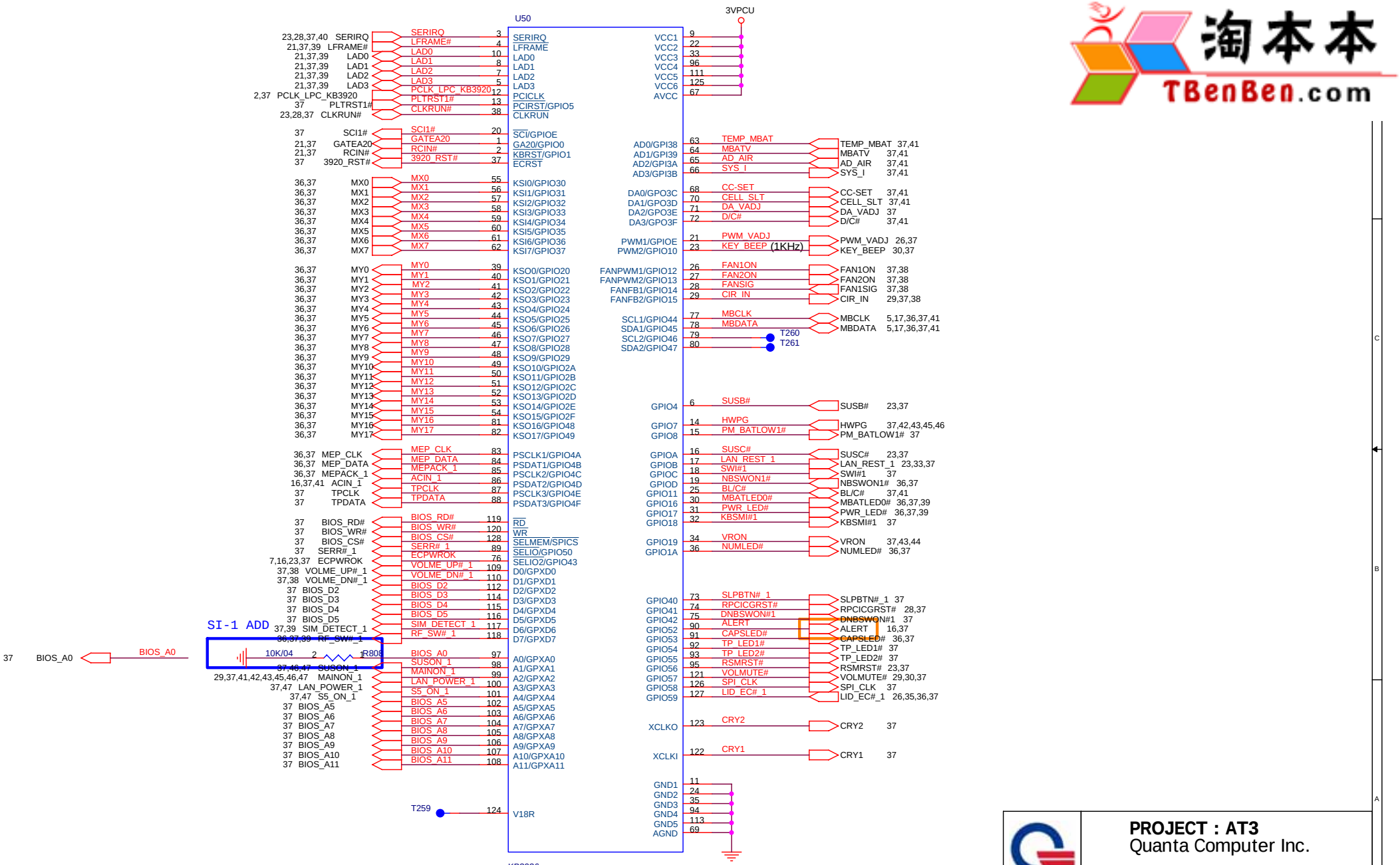

PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: B	Document Number: KB3926
Rev: 1A	
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