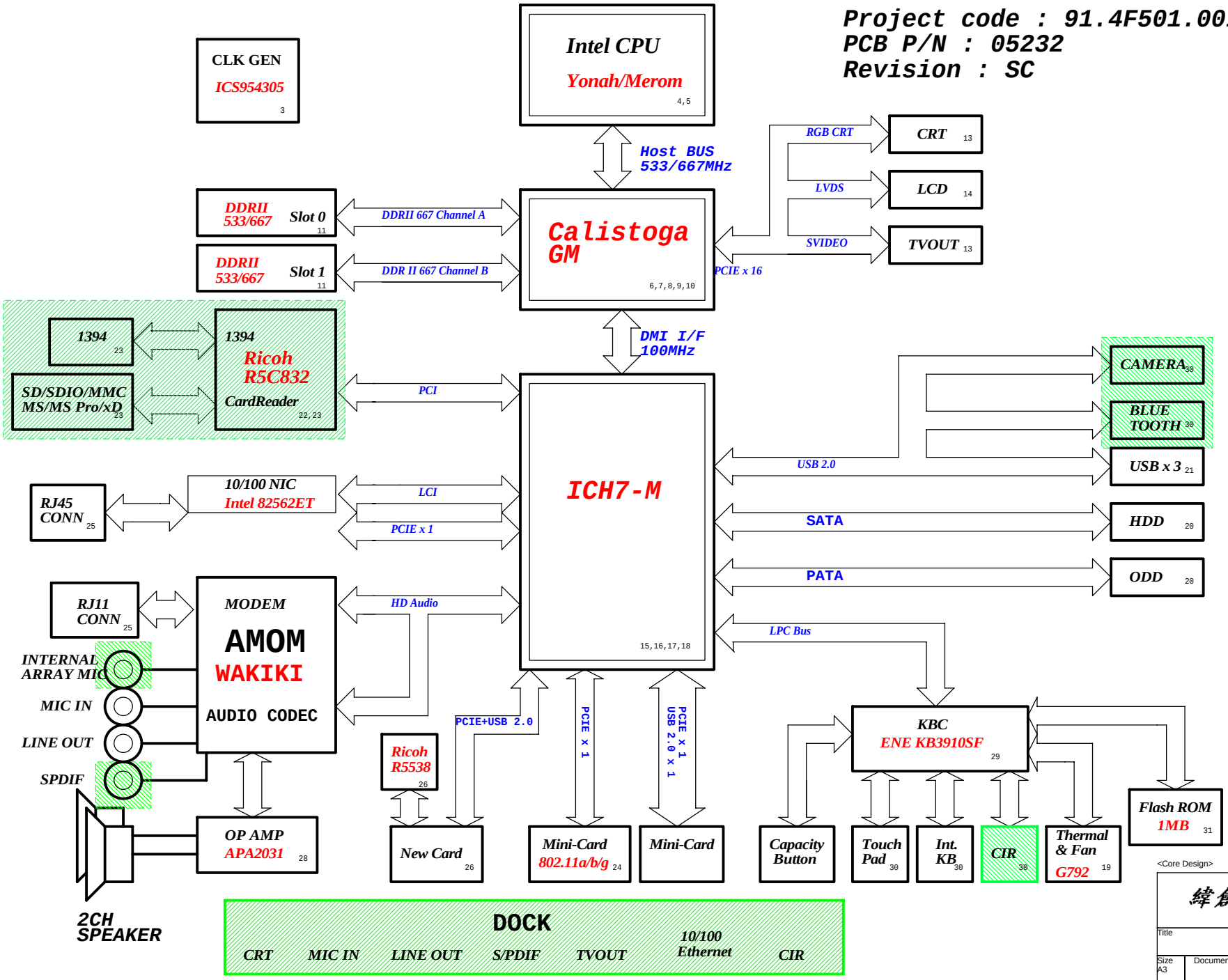
Akita Block Diagram

Project code : 91.4F501.001
PCB P/N : 05232
Revision : SC



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Akita | Rev: SC
Date: Thursday, December 01, 2005 | Sheet 1 of 39

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

125CV Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

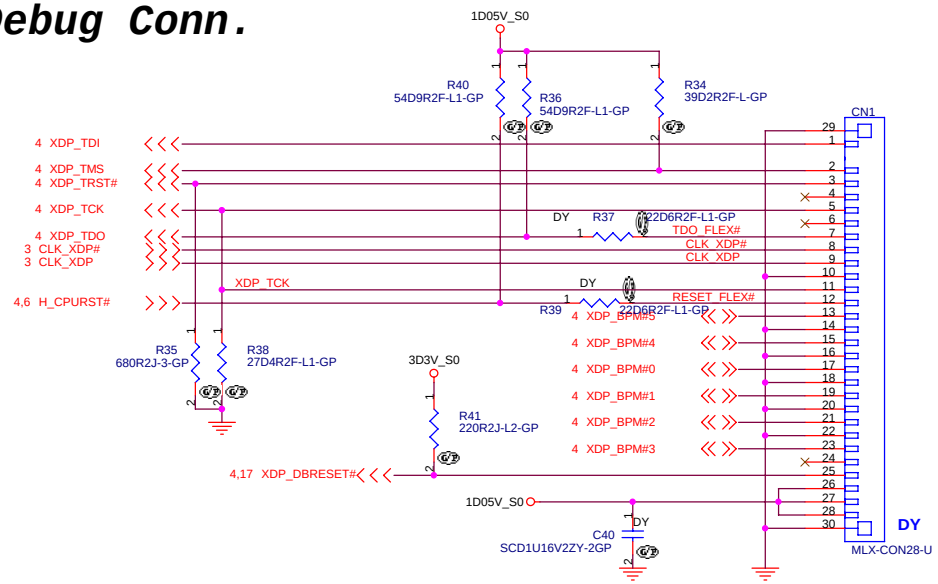
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

11.18.2004: mini card not ready

ITP Debug Conn.



<Core Design>

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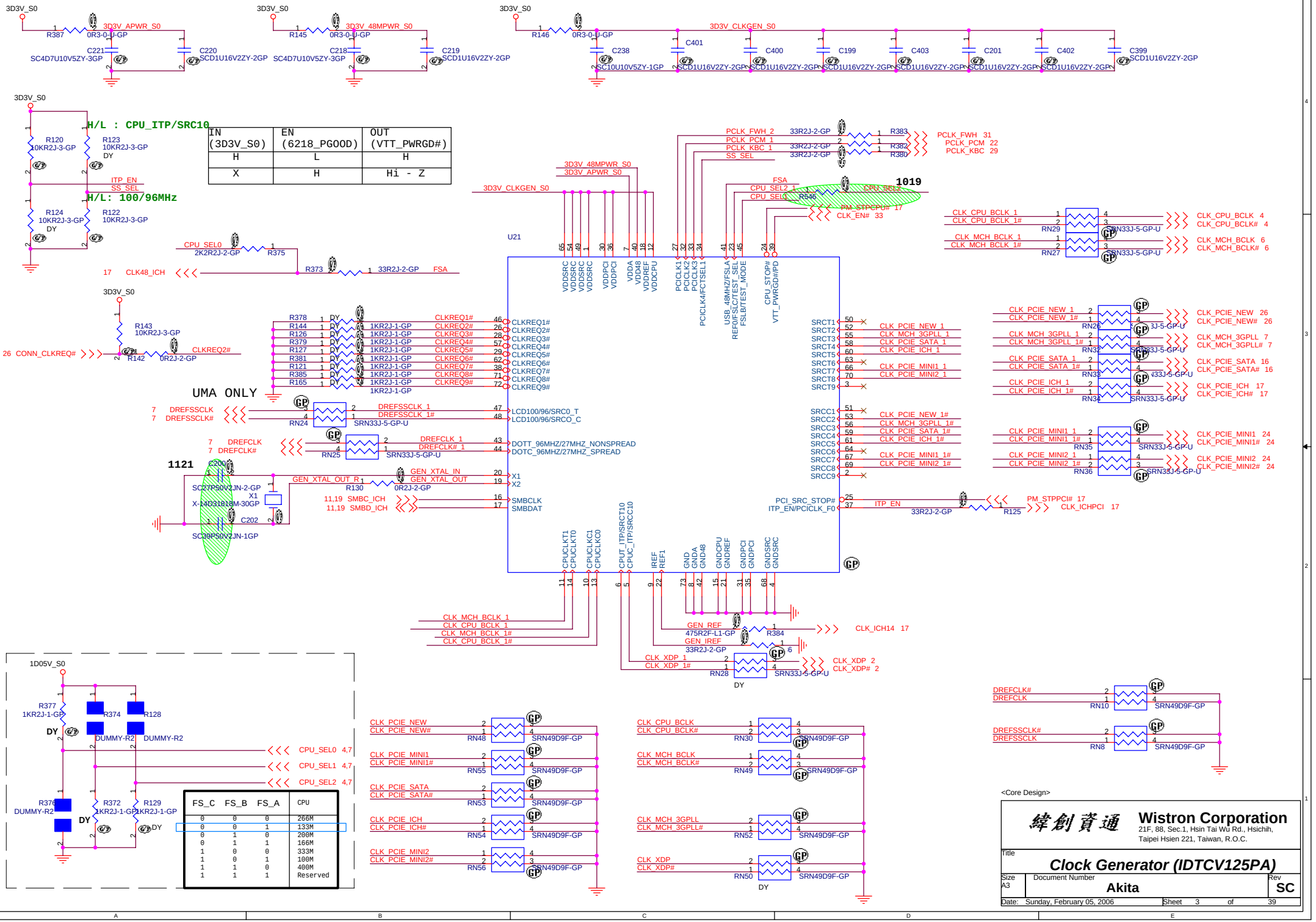
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A3 | Document Number: Akita | Rev: SC

Date: Sunday, February 05, 2006 | Sheet 2 of 39



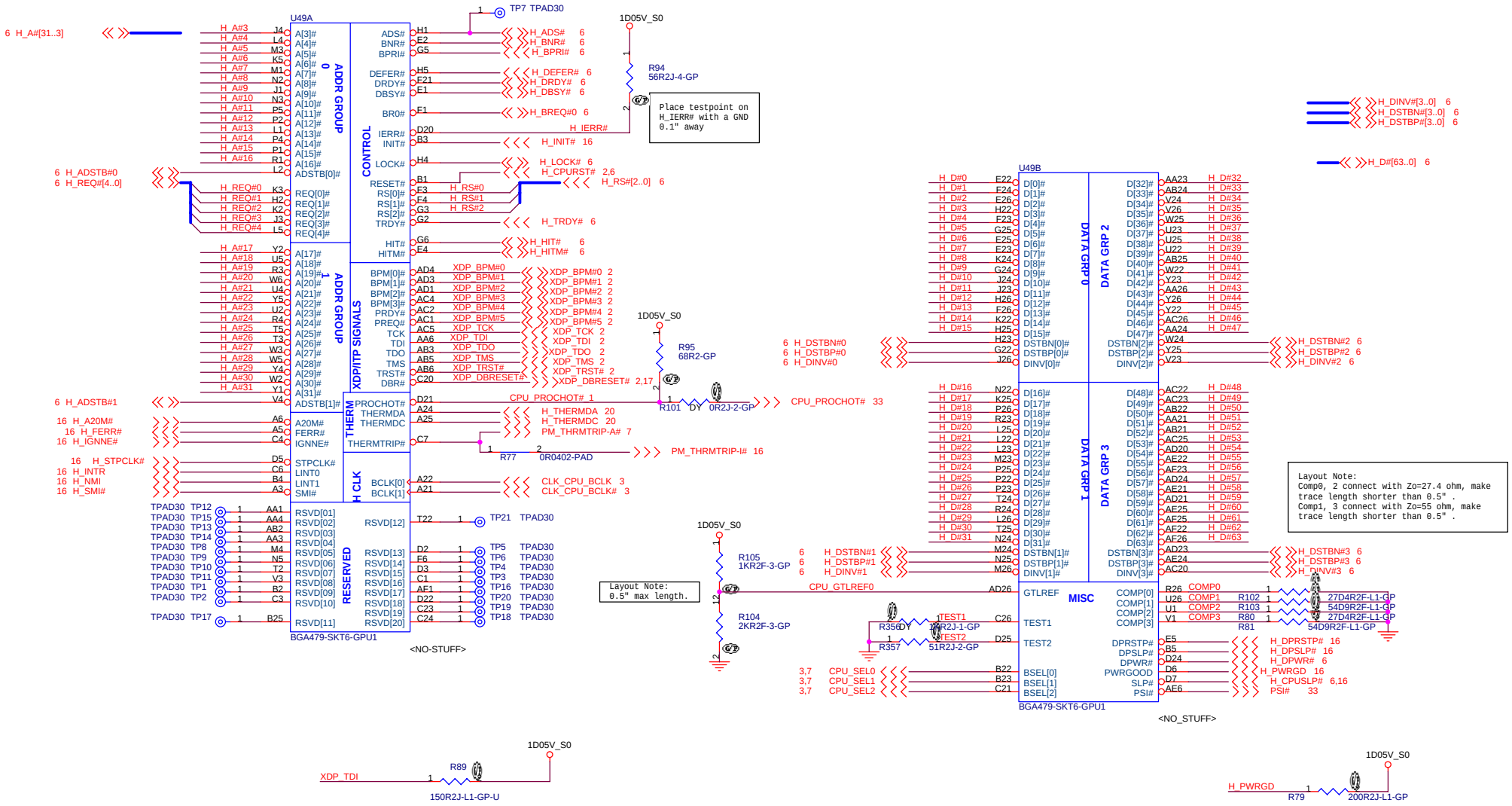
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator (IDTCV125PA)**

Size: A3 | Document Number: **Akita** | Rev: **SC**

Date: Sunday, February 05, 2006 | Sheet 3 of 39



<Core Design>

Wistron Corporation
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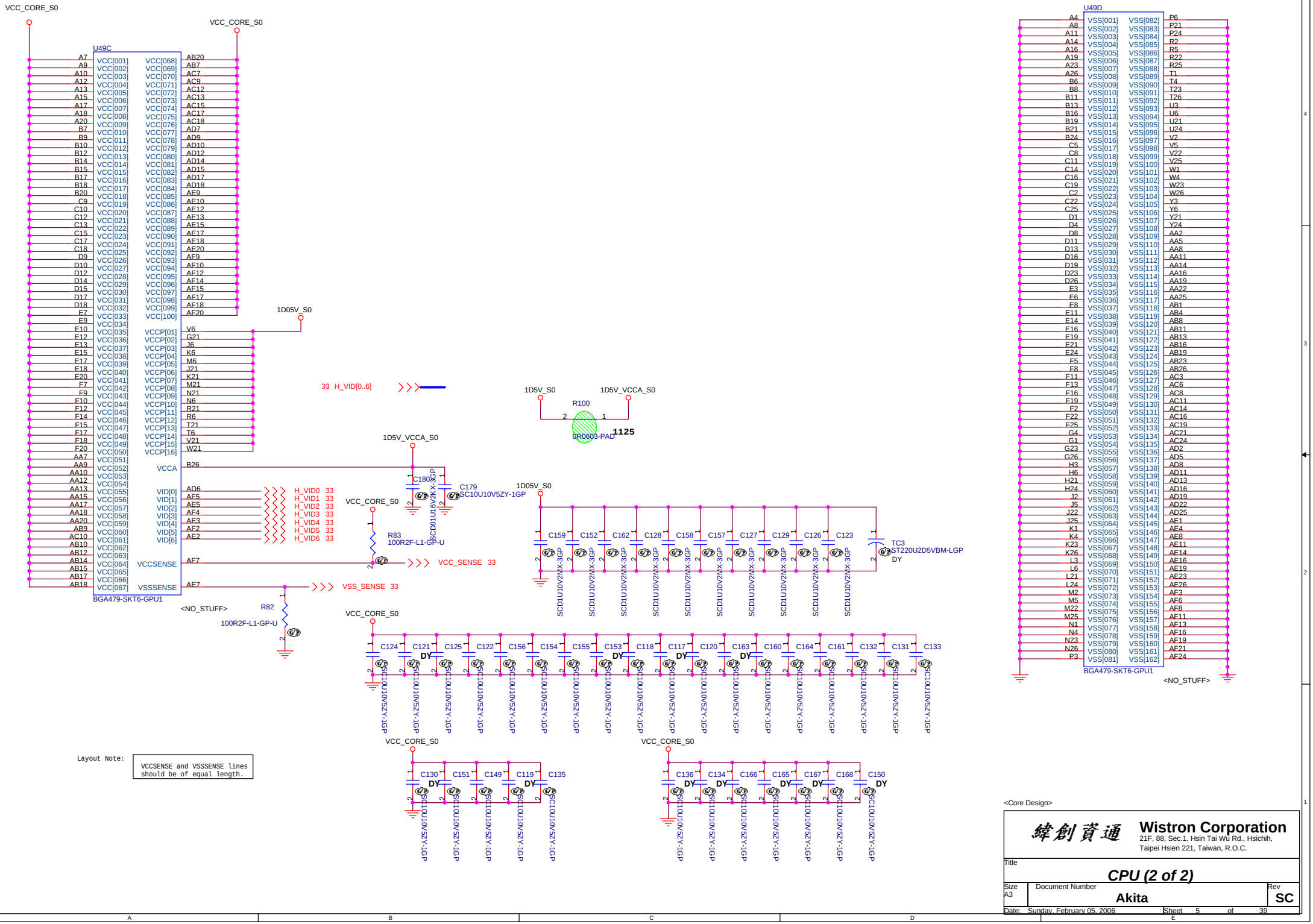
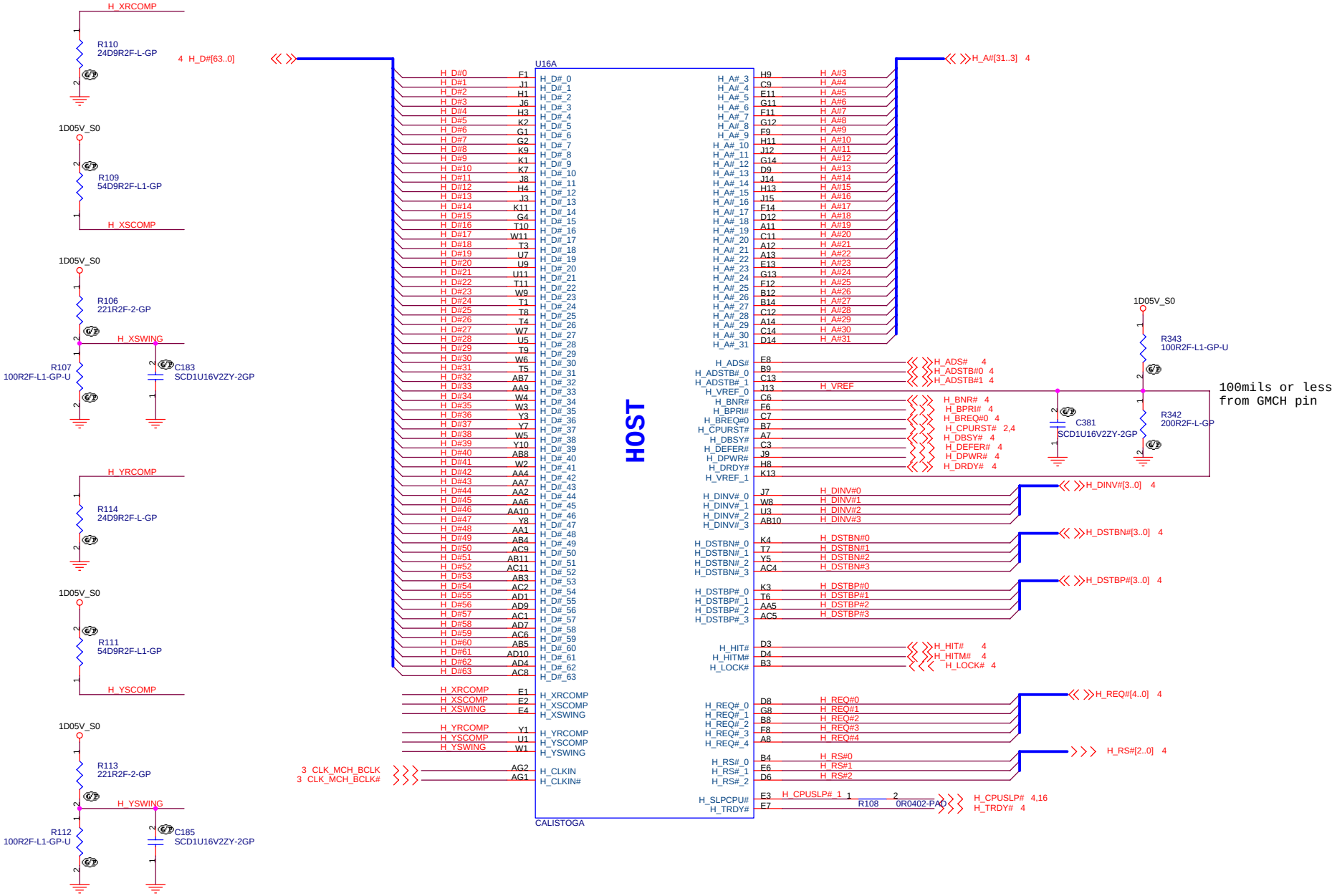
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (1 of 2)**

Size: A3 | Document Number: **Akita** | Rev: **SC**

Date: Sunday, February 05, 2006 | Sheet 4 of 39


VCC_CORE_S0
U49C
BGA479-SKT6-GPU1
1D05V_S0
33 H_VID[0..6]
1D05V_VCCA_S0
R100
0R0603-PAD
1125
C180
C179
SC10U10V5ZY-1GP
R83
100R2F-L1-GP-U
VCC_SENSE 33
VSS_SENSE 33
R82
100R2F-L1-GP-U
<NO_STUFF>
TC3
ST220U2D5VBM-LGP
DY
U49D
BGA479-SKT6-GPU1
<NO_STUFF>
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size A3
Document Number
Akita
Rev SC
Date: Sunday, February 05, 2006
Sheet 5 of 39



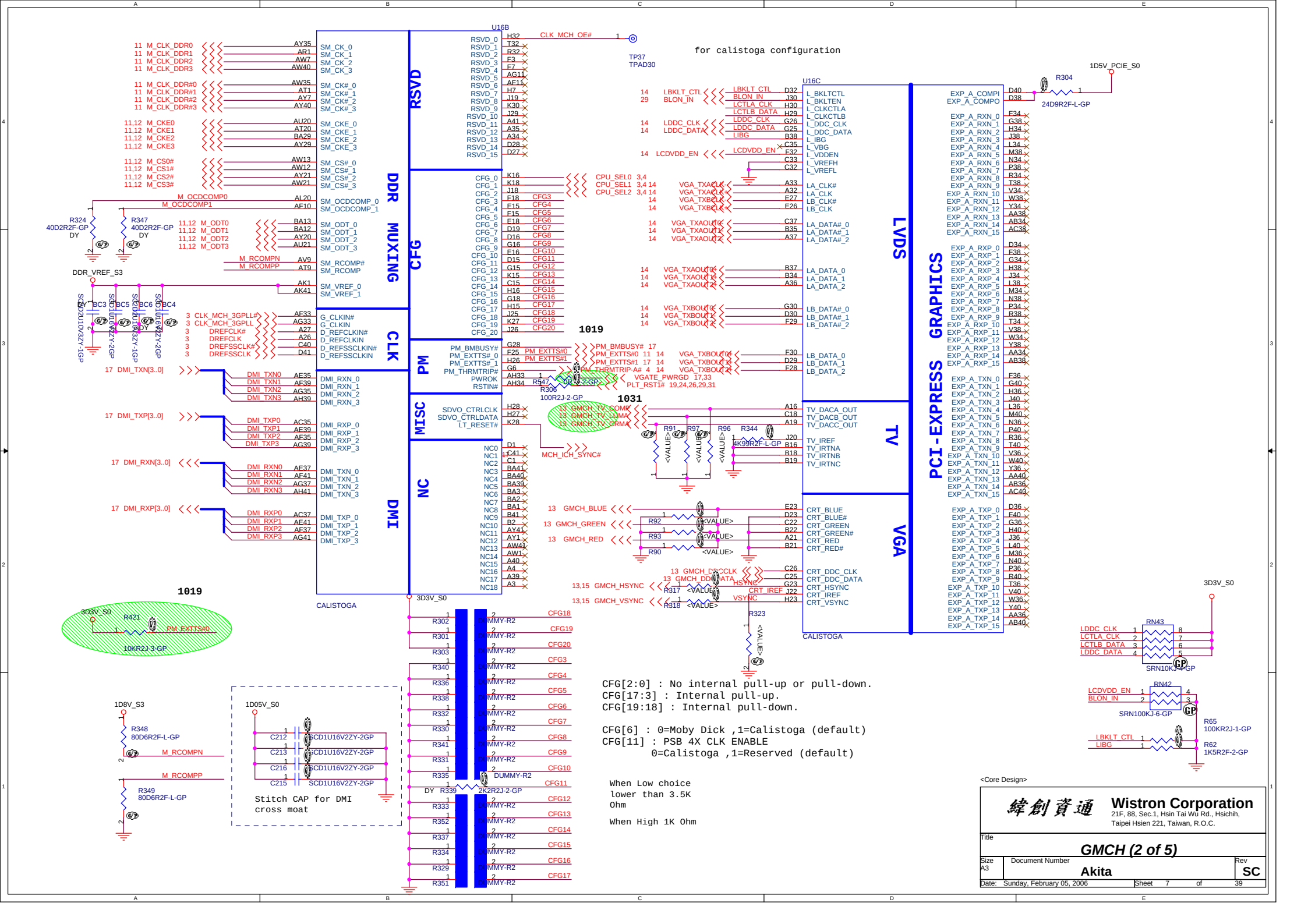
<Core Design>

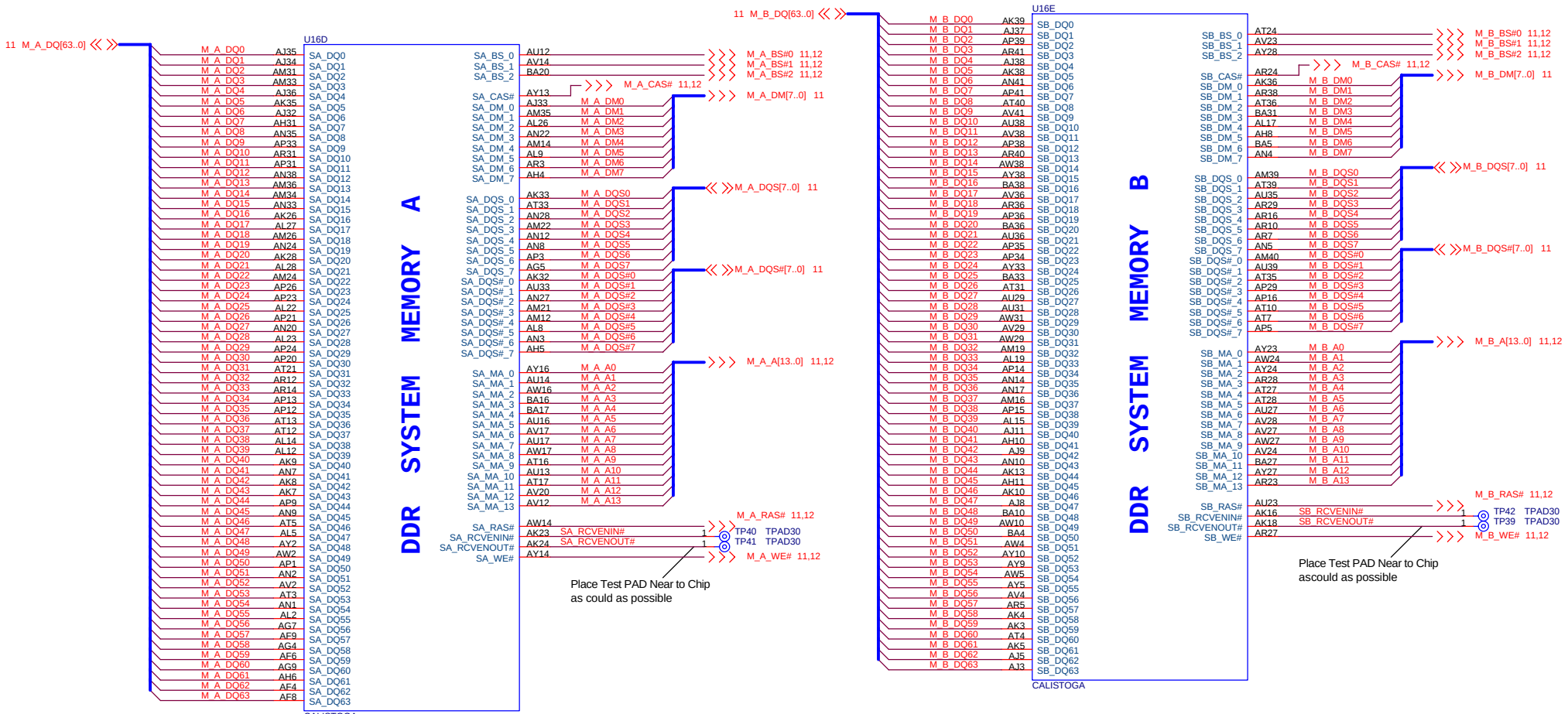
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	Akita	SC

Date: Sunday, February 05, 2006 Sheet 6 of 39


for calistoga configuration
DDR MUXING
CFG
CLK
PM
MISC
NC
DMI
RSVD
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
U16B
U16C
1019
1031
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)
When Low choice
lower than 3.5K
Ohm
When High 1K Ohm
Stitch CAP for DMI
cross moat
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number
Akita
Rev SC
Date: Sunday, February 05, 2006
Sheet 7 of 39



<Core Design>

緯創資通 **Wistron Corporation**
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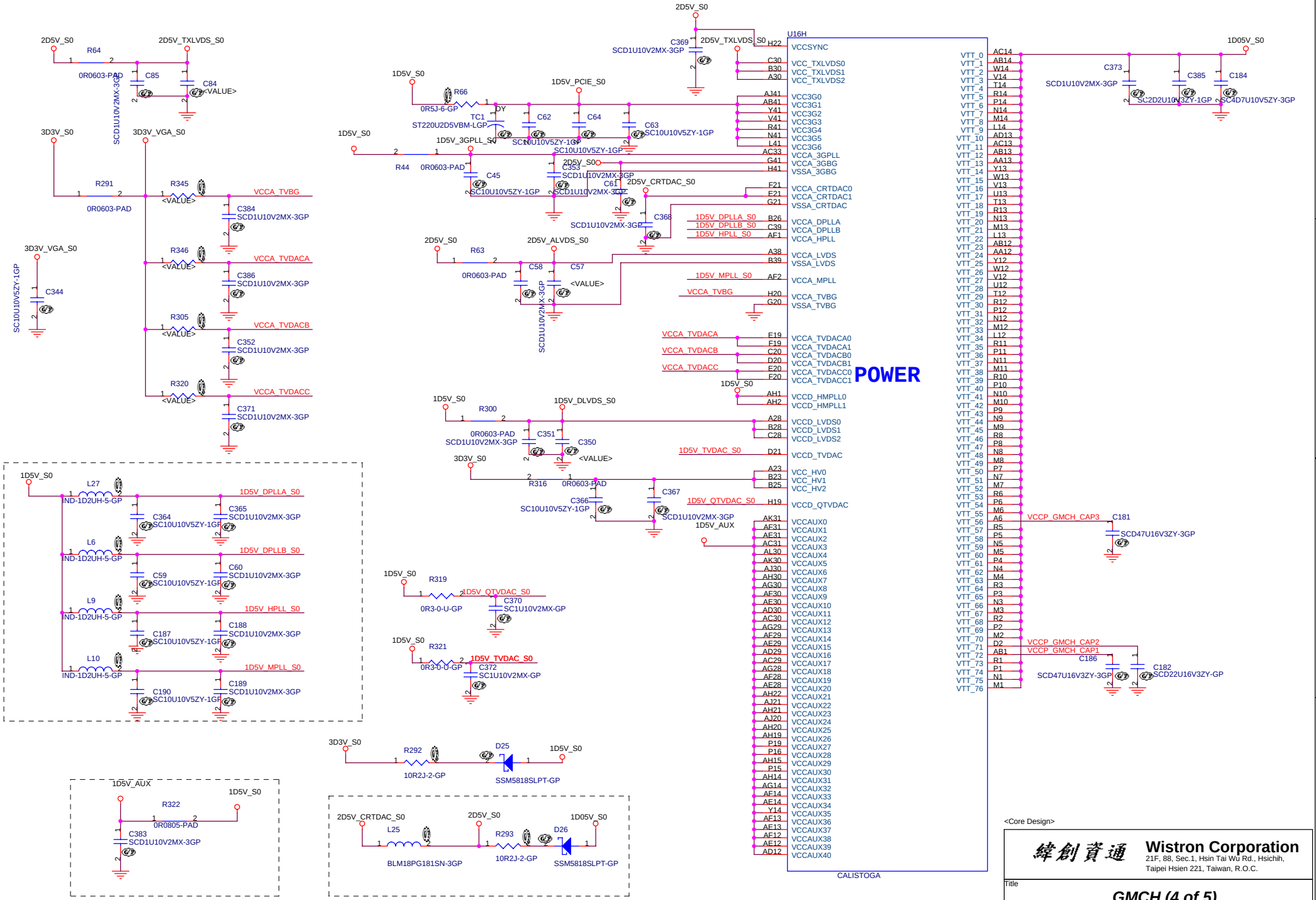
Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
A3	Akita	SC

Date: Sunday, February 05, 2006 Sheet 8 of 39



<Core Design>

Wistron Corporation
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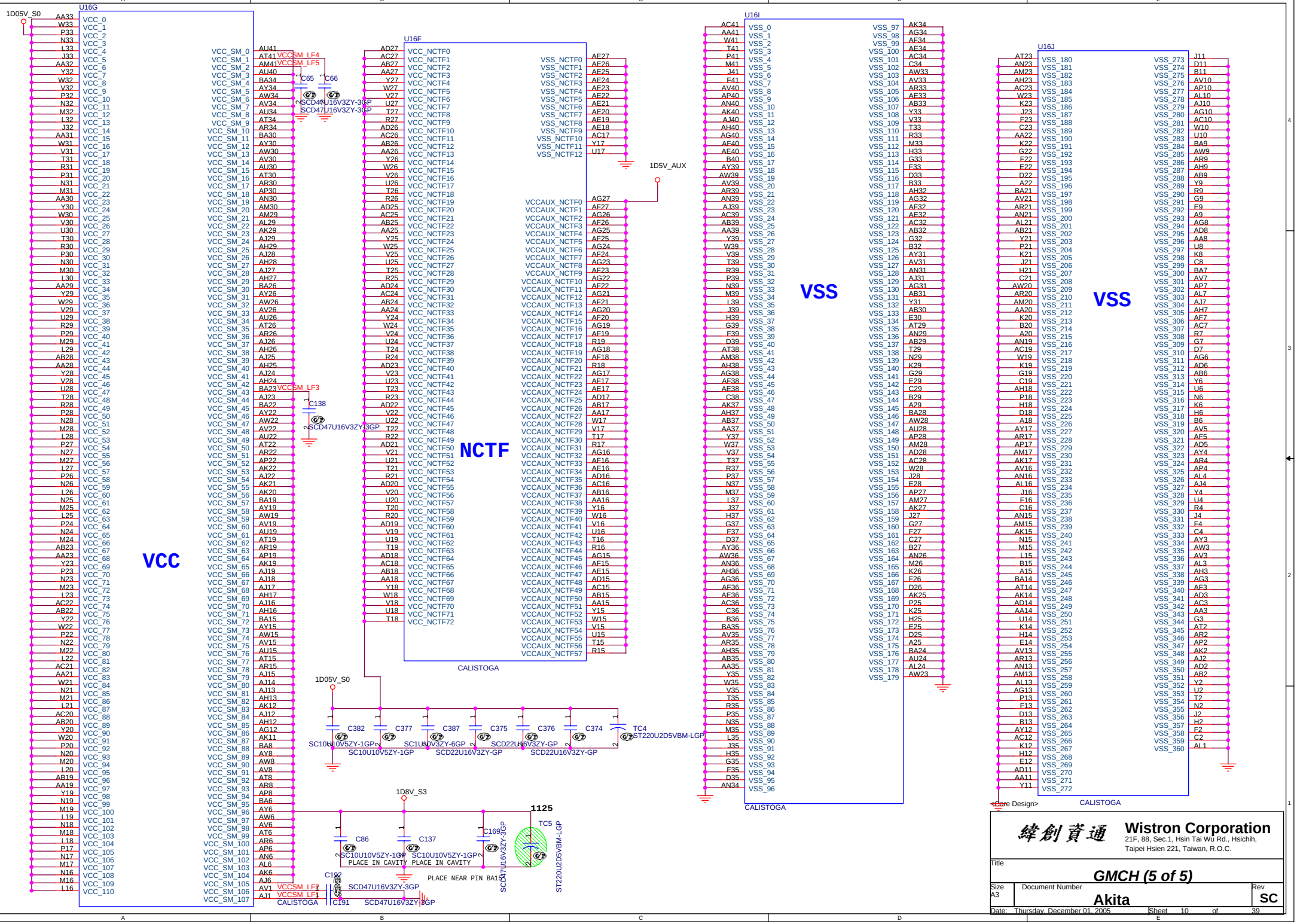
Title: ***GMCH (4 of 5)***

Size	Document Number	Rev
A3	Akita	SC

Date: Saturday, February 04, 2006 Sheet 9 of 39



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GMCH (5 of 5)
Size	A3
Document Number	Akita
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Date	Thursday, December 01, 2005
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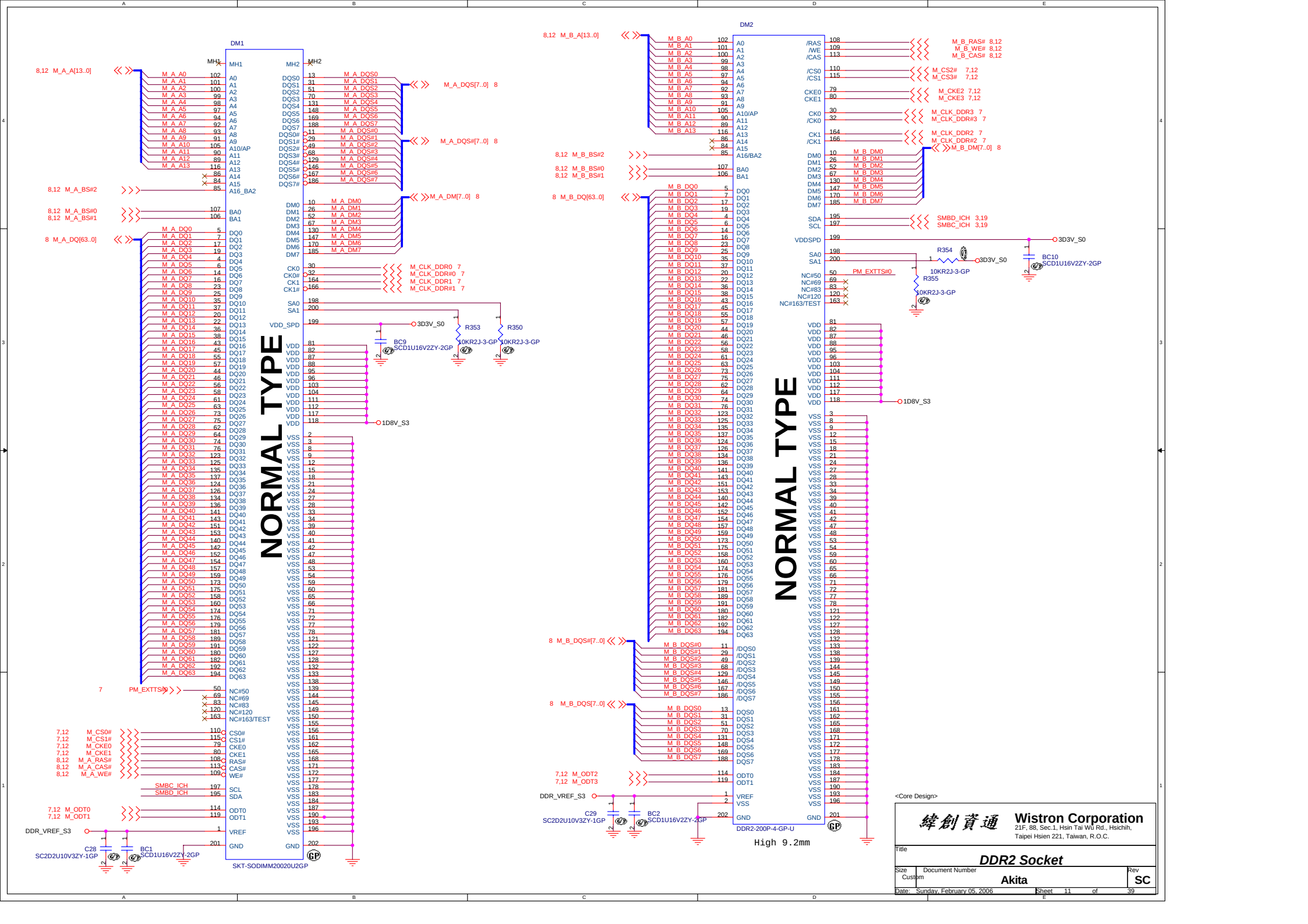
DM1
DM2
NORMAL TYPE
NORMAL TYPE
SKT-SODIMM20020U2GP
DDR2-200P-4-GP-U
High 9.2mm
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
Akita
Rev
SC
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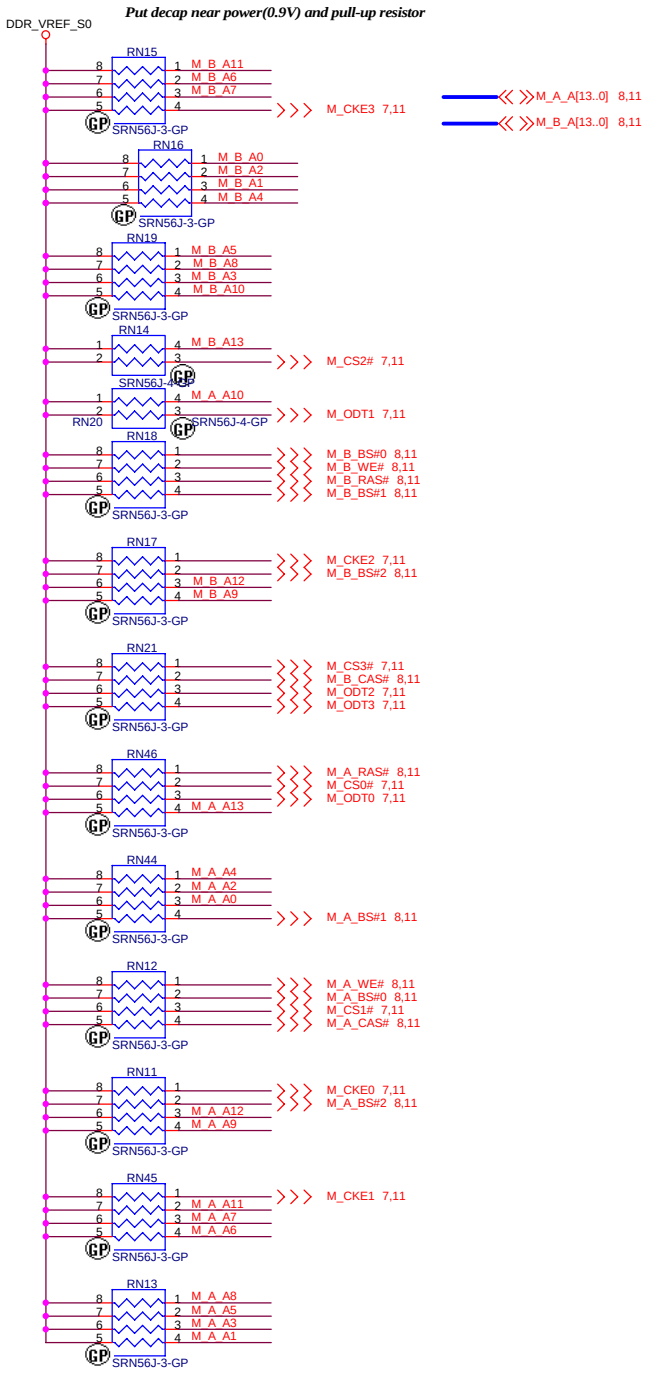
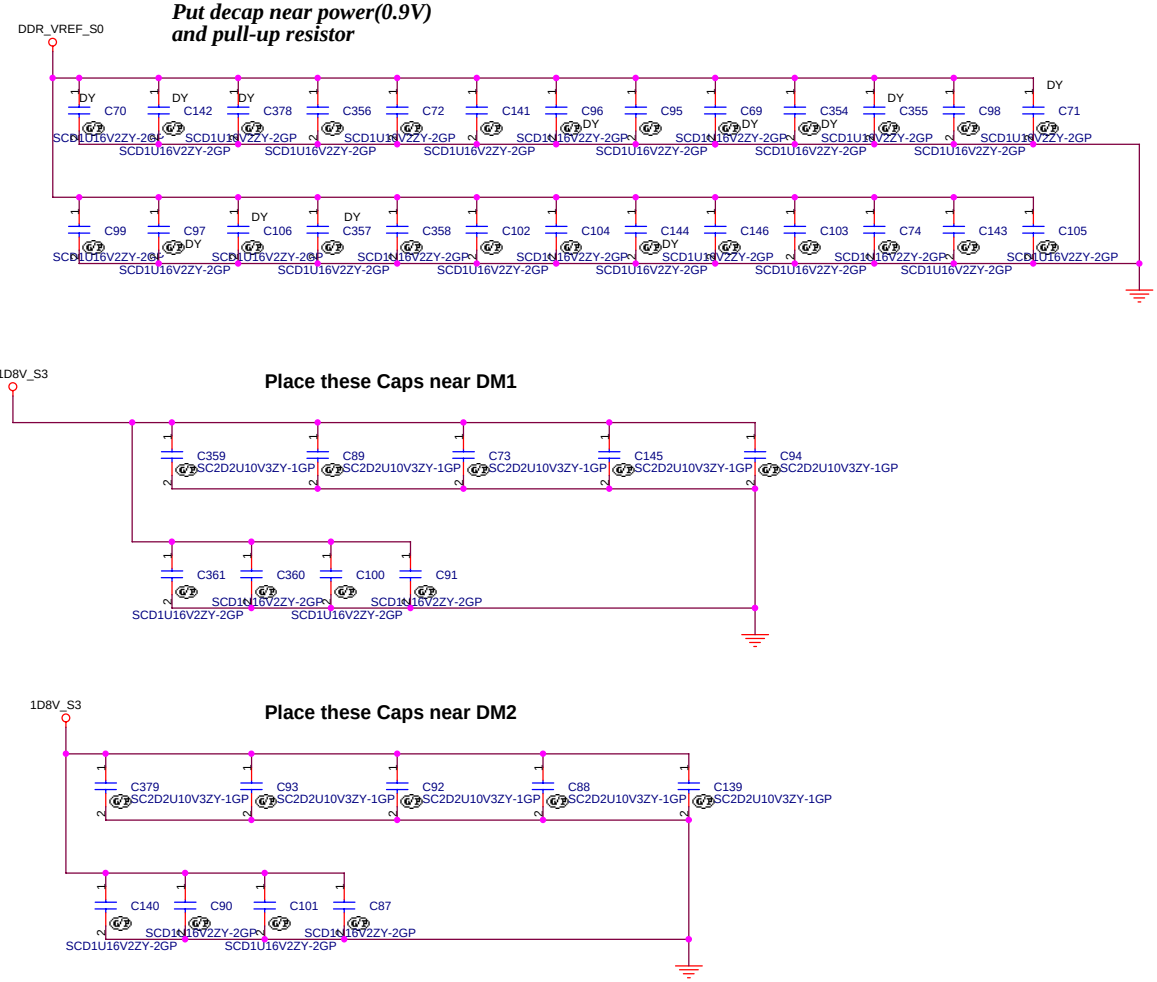
PARALLEL TERMINATION



Decoupling Capacitor



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

7 GMCH_RED
7 GMCH_GREEN
7 GMCH_BLUE

1122

BLM18BB470SN1-GP (L2, L3, L1)

R5 150R2F-1-GP
R4 150R2F-1-GP
R3 150R2F-1-GP
C14 SC22P50V2JN-4GP
C15 SC22P50V2JN-4GP
C11 SC22P50V2JN-4GP
C12 SC2P50V2CN-GP
C13 SC2P50V2CN-GP
C9 SC2P50V2CN-GP

CRT_R → CRT_R 15
CRT_G → CRT_G 15
CRT_B → CRT_B 15

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0
C10 SCD01U16V2KX-3GP
F1 FUSE-1D1A6V-8GP
5V_S0
D3 CH751H-40PT-1GP
1124
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U
CRT_R
CRT_G
CRT_B
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON
C7 SC33P50V2JN-3GP
C6 SC33P50V2JN-3GP
C8 SC22P50V2JN-4GP
C1 SC22P50V2JN-4GP

D10 BAV99-7-F-GP
D9 BAV99-7-F-GP
DDC_DATA_CON
DDC_CLK_CON
5V_CRT1_S0

1124
U2 PACDN009MR-GP-U
GMCH_HSYNC
GMCH_VSYNC
CRT_R
CRT_G
CRT_B

5V_S0
C21 SCD1U16V2ZY-2GP
PR_INSERT 15

7,15 GMCH_HSYNC
7,15 GMCH_VSYNC
U5A TSAHCT125PW-GP
U5B TSAHCT125PW-GP
HSYNC_5
VSYNC_5
RN4 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP
U1 2N7002DW-7F-GP
7 GMCH_DDCDATA
DDC_DATA_CON
DDC_DATA_CON 15
15 DDC_CLK_CON
DDC_CLK_CON
GMCH_DDCCLK 7
RN6 SRN0J-6-GP
DY

5V @ ext. CRT side

TV OUT CONN

connector

7 GMCH_TV_CRMA
L18 BLM18BB151SN-1GP
C328 SC10P50V2JN-4GP
C324 SC10P50V2JN-4GP
R272 150R2F-1-GP
TV_CRMA 15

7 GMCH_TV_COMP
L20 BLM18BB151SN-1GP
C326 SC10P50V2JN-4GP
C327 SC10P50V2JN-4GP
R271 150R2F-1-GP
TV_COMP 15

7 GMCH_TV_LUMA
L19 BLM18BB151SN-1GP
C329 SC10P50V2JN-4GP
C325 SC10P50V2JN-4GP
R270 150R2F-1-GP
TV_LUMA 15

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP
TV_LUMA
TV_CRMA
TV_COMP
LUMA
CRMA
COMP
NC#2
NC#5
GND

D2 BAV99-7-F-GP
C3 SCD1U16V2ZY-2GP
D1 BAV99-7-F-GP
C2 SCD1U16V2ZY-2GP
D4 BAV99-7-F-GP
C4 SCD1U16V2ZY-2GP

<Core Design>

緯創資通 Wistron Corporation
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Title: CRT/TV Connector
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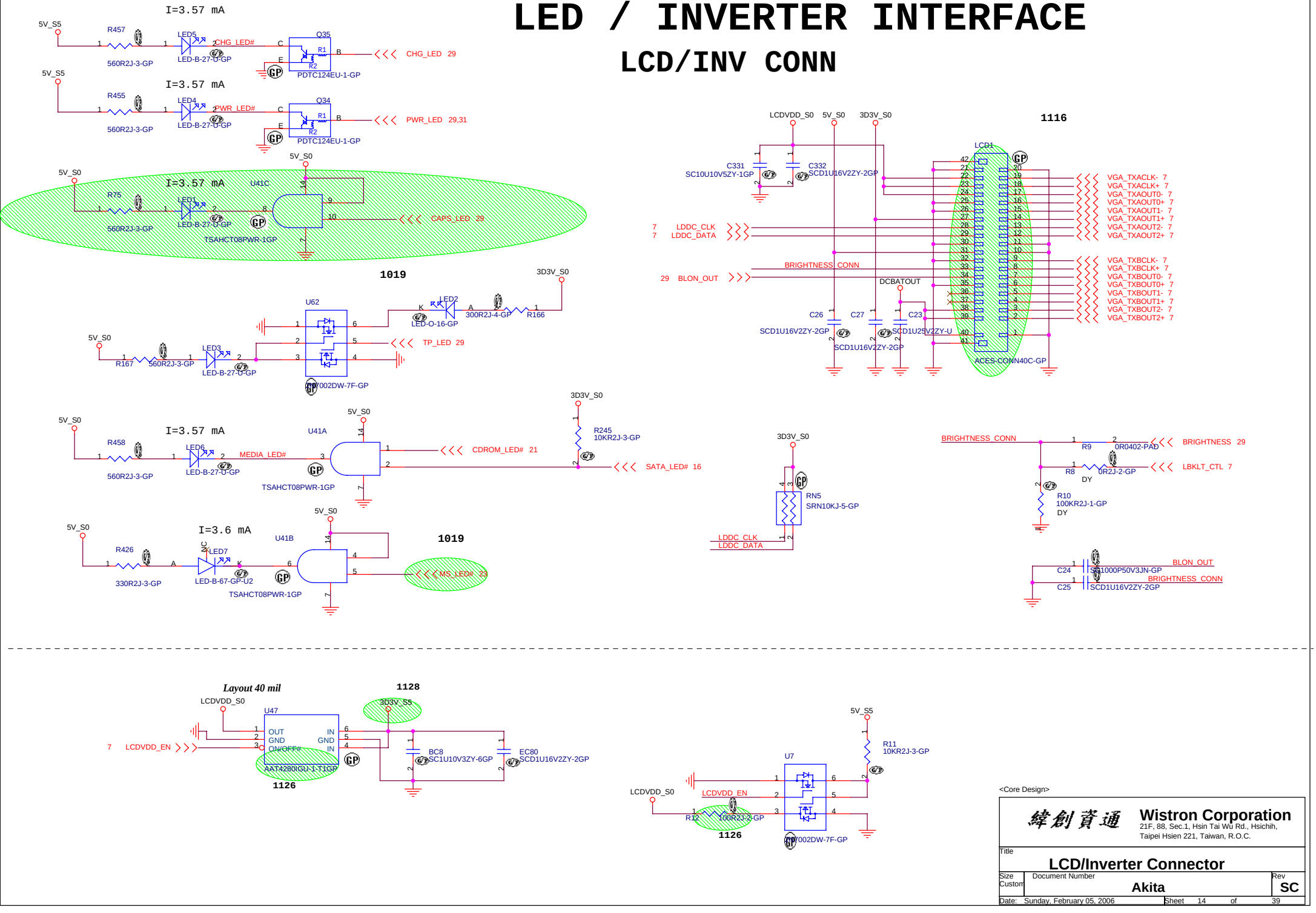
LED / INVERTER INTERFACE

LCD/INV CONN



<Core Design>

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Title: **LCD/Inverter Connector**

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Custom	Akita	SC

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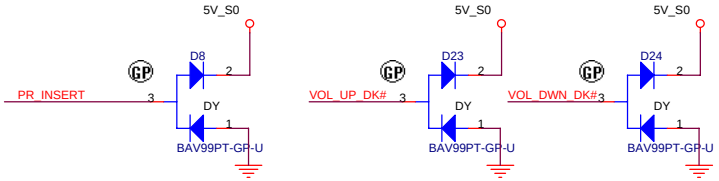
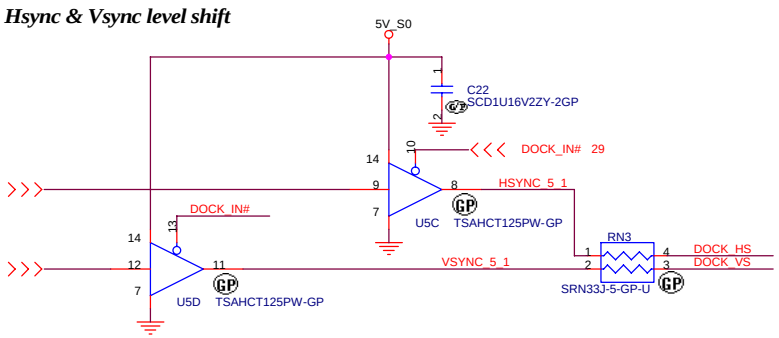
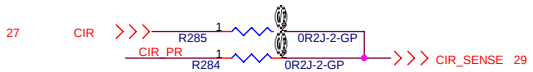
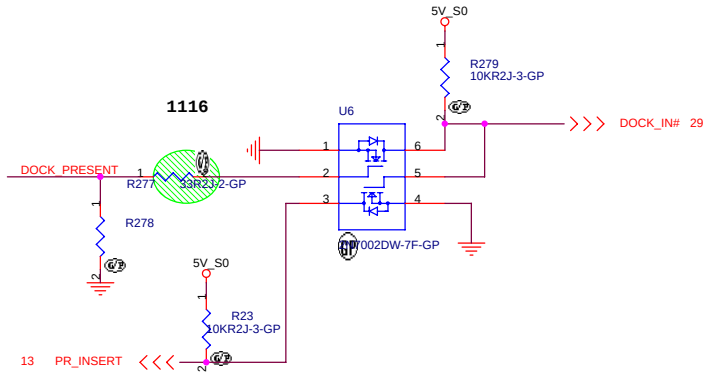
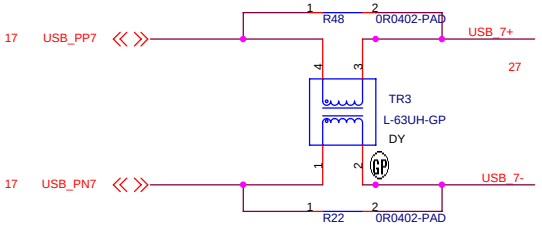
Docking Connector

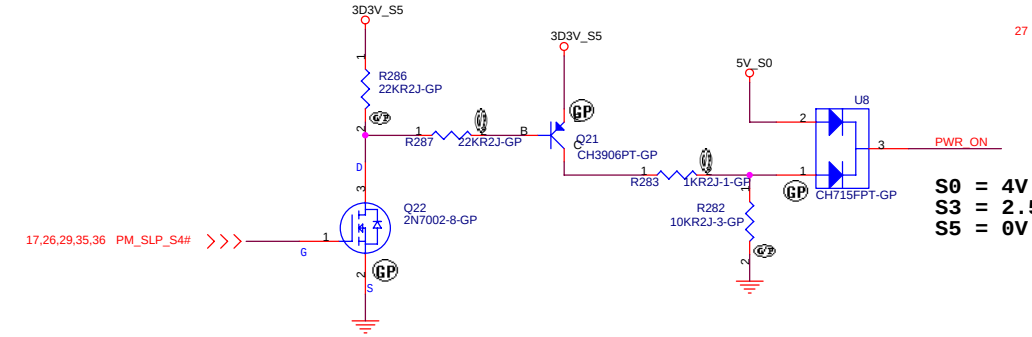




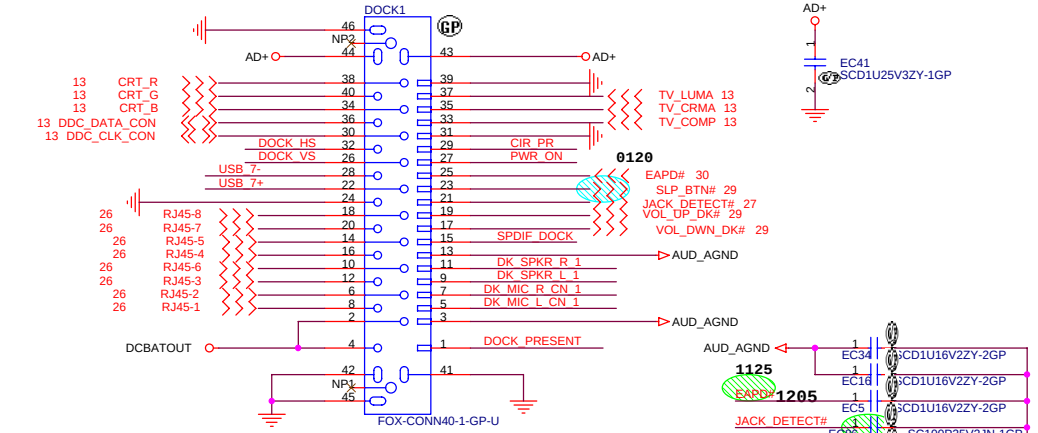


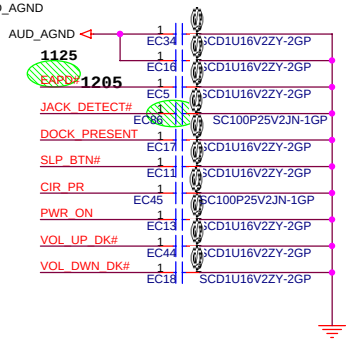


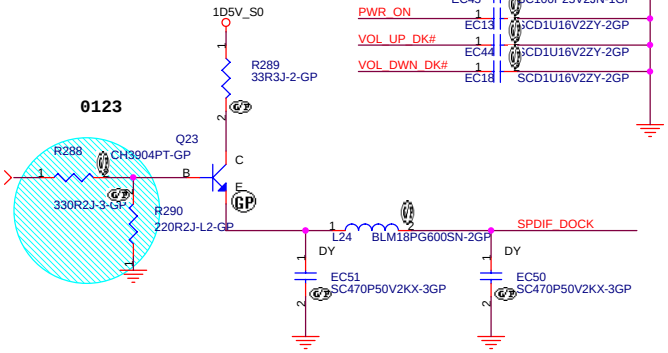


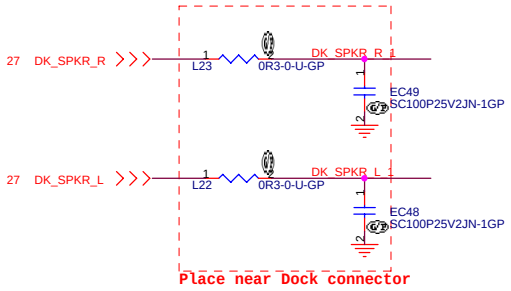


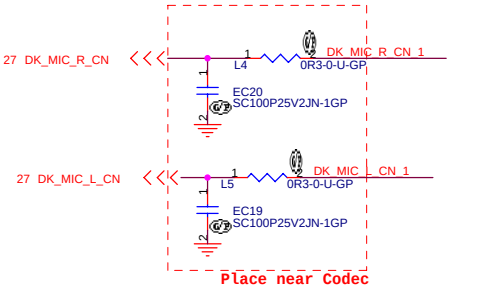
S0 = 4V
S3 = 2.5V
S5 = 0V











<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

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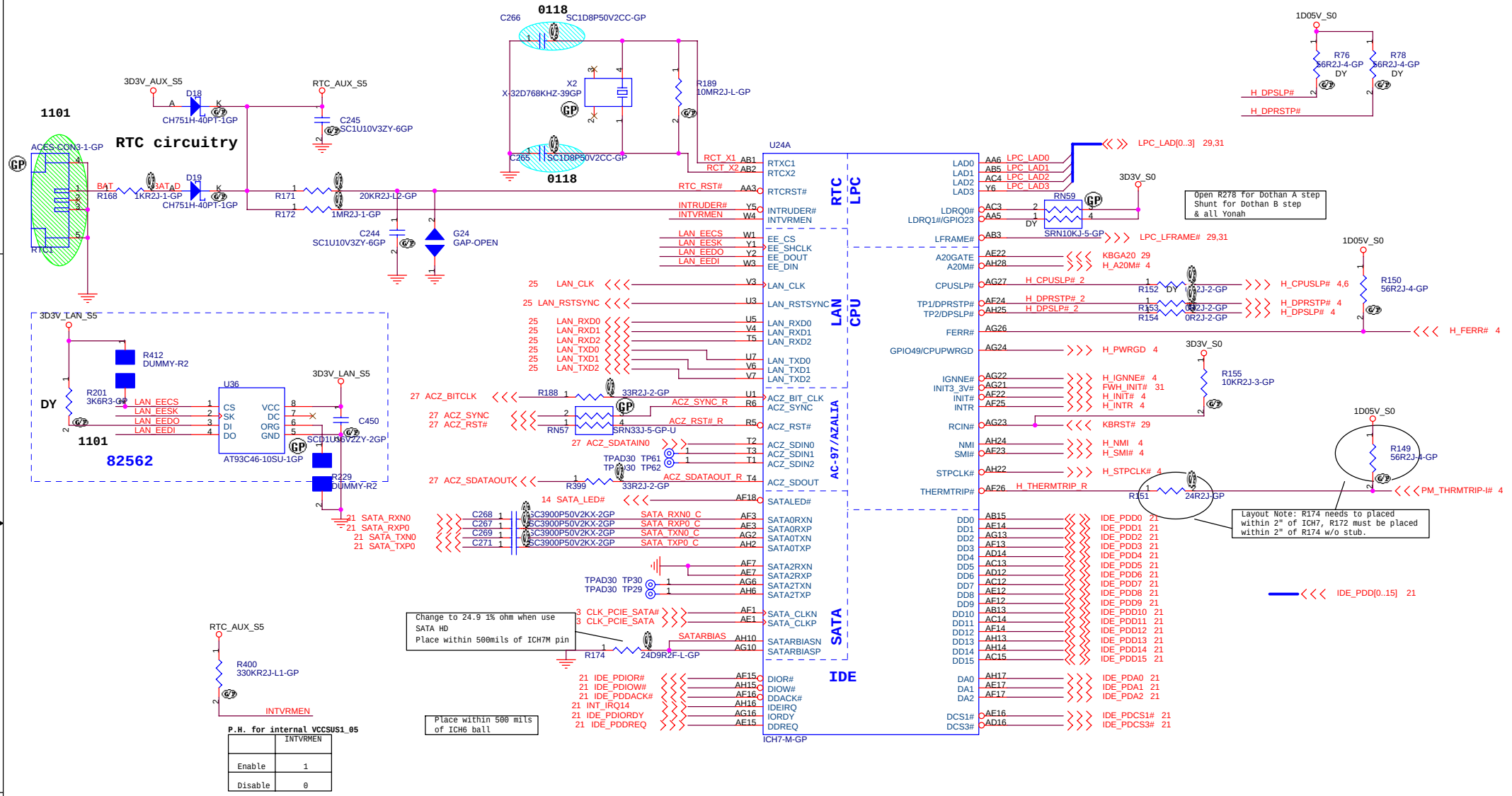
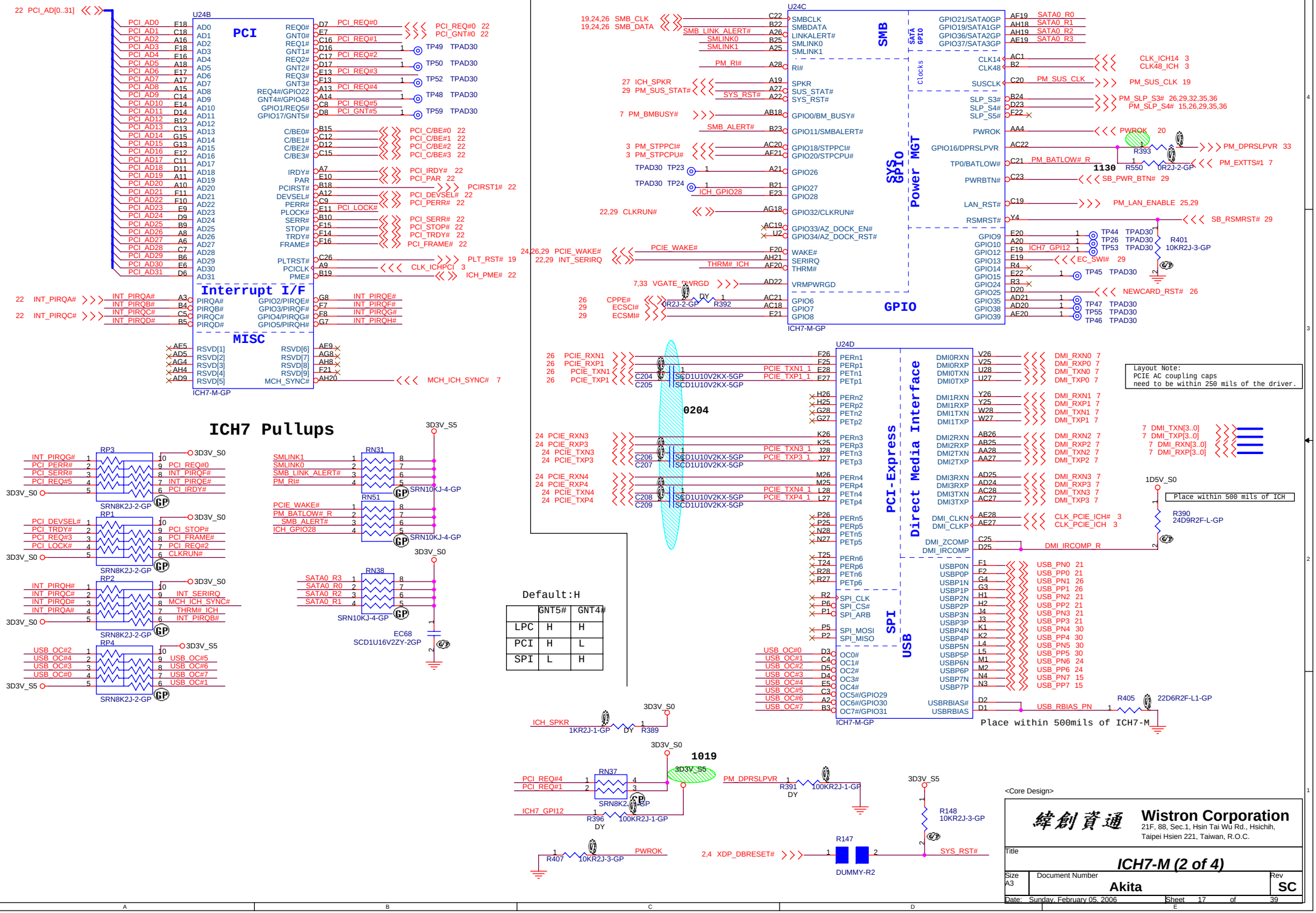
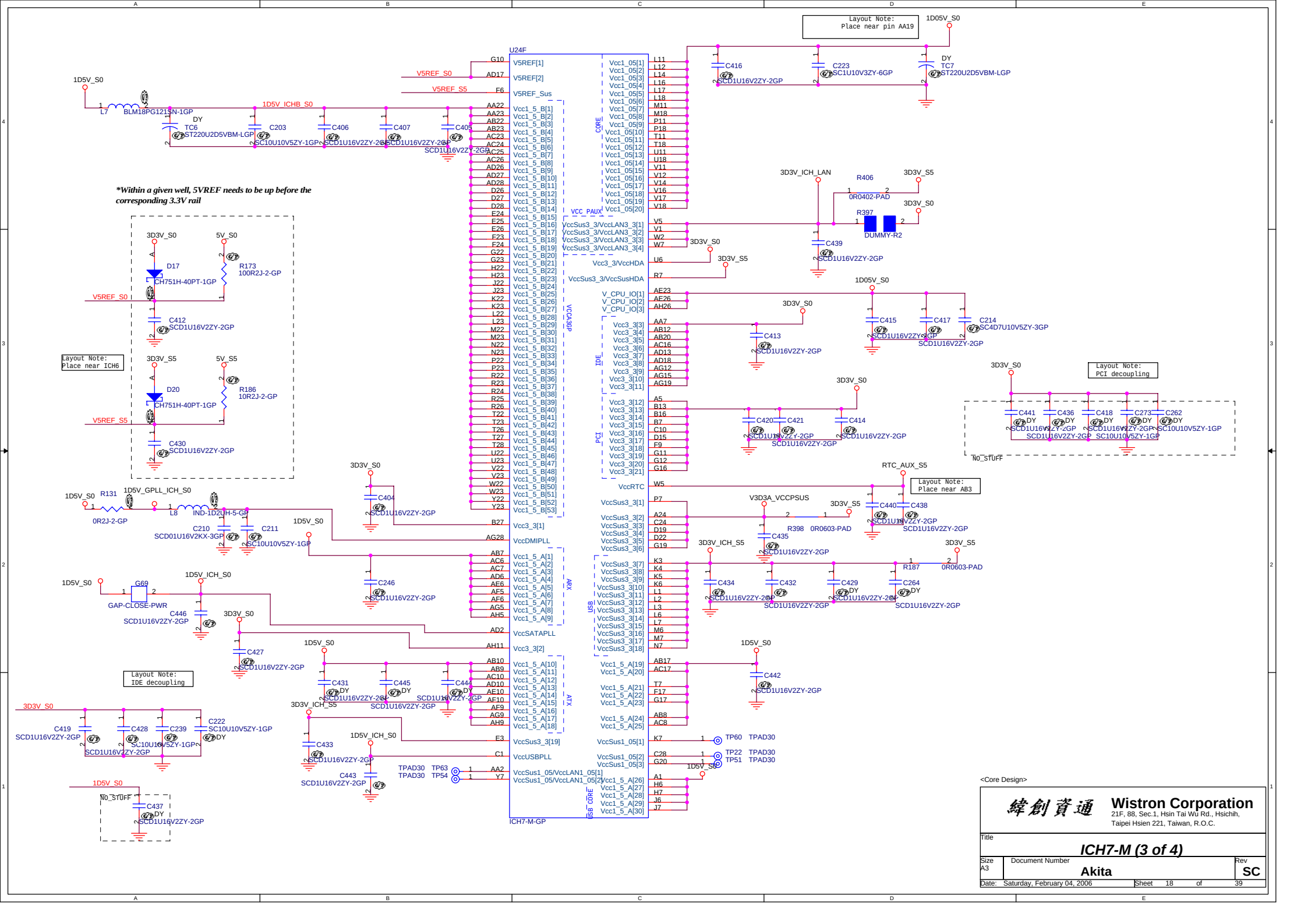
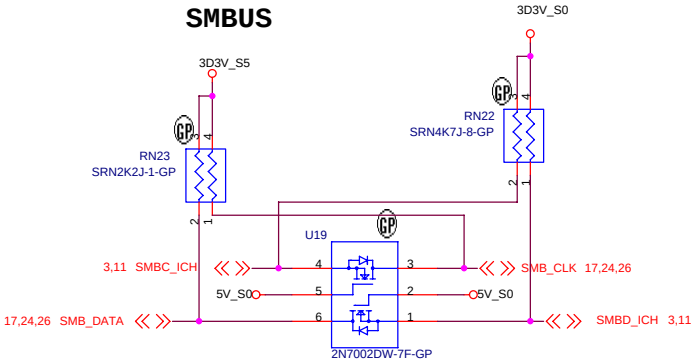

RTC circuitry
1101
ACES-CON3-1-GP
RTC1
BAT
R168
1KR2J-1-GP
3ATAD
D18
D19
CH751H-40PT-1GP
3D3V_AUX_S5
RTC_AUX_S5
C245
SC1U10V3ZY-6GP
R171
R172
20KR2J-L2-GP
1MR2J-1-GP
C244
SC1U10V3ZY-6GP
G24
GAP-OPEN
0118
C266
SC1D8P50V2CC-GP
X2
X-32D768KHZ-39GP
C265
R189
10MR2J-L-GP
RCT_X1
RCT_X2
RTC_RST#
INTRUDER#
INTVRMEN
U24A
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
ICH7-M-GP
LAN_EECS
LAN_EESK
LAN_EEDO
LAN_EEDI
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
ACZ_SDATAOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
LPC_LAD[0..3] 29,31
LPC_LFRAME# 29,31
KBGA20 29
H_A20M# 4
H_CPUSLP# 2
H_DPRSTP# 2
H_DPSLP# 2
H_FERR# 4
H_PWRGD 4
H_IGNNE# 4
FWH_INIT# 31
H_INIT# 4
H_INTR 4
KBRST# 29
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
PM_THRMTRIP-I# 4
IDE_PDD[0..15] 21
3D3V_LAN_S5
R412
DUMMY-R2
R201
3K6R3-GP
DY
U36
AT93C46-10SU-1GP
82562
C450
SCD1U16VZZY-2GP
R229
DUMMY-R2
R188
33R2J-2-GP
RN57
SRN33J-5-GP-U
R399
TPAD30 TP61
TPAD30 TP62
TPAD30 TP30
TPAD30 TP29
C268
C267
C269
C271
SC3900P50V2KX-2GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
R174
24D9R2F-L-GP
SATARBIAS
CLK_PCIE_SATA#
CLK_PCIE_SATA
R400
330KR2J-L1-GP
INTVRMEN
R59
SRN10KJ-5-GP
R155
10KR2J-3-GP
R76
56R2J-4-GP
R78
56R2J-4-GP
R150
56R2J-4-GP
R149
56R2J-4-GP
R152
R153
R154
0R2J-2-GP
R151
24R2J-GP
1D05V_S0
3D3V_S0
H_DPSLP#
H_DPRSTP#
Open R278 for Dothan A step
Shunt for Dothan B step
& all Yonah
Change to 24.9 1% ohm when use
SATA HD
Place within 500mils of ICH7M pin
Place within 500 mils
of ICH6 ball
Layout Note: R174 needs to placed
within 2" of ICH7, R172 must be placed
within 2" of R174 w/o stub.
Placement Note:
Diatance between the ICH-6 M and cap on the "P" signal
should be identical distance between the ICH-6 M and cap
on the "N" signal for same pair.
P.H. for internal VCCSUS1_05
INTVRMEN
Enable 1
Disable 0
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (1 of 4)
Size A3
Document Number
Akita
Rev SC
Date: Sunday, February 05, 2006
Sheet 16 of 39


U24B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U24C
SMB
SYS GPIO
Power MGT
GPIO
ICH7-M-GP
U24D
PCI-Express
Direct Media Interface
SPI
USB
ICH7-M-GP
ICH7 Pullups
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
0204
1019
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500mils of ICH7-M
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number
Akita
Rev SC
Date: Sunday, February 05, 2006
Sheet 17 of 39

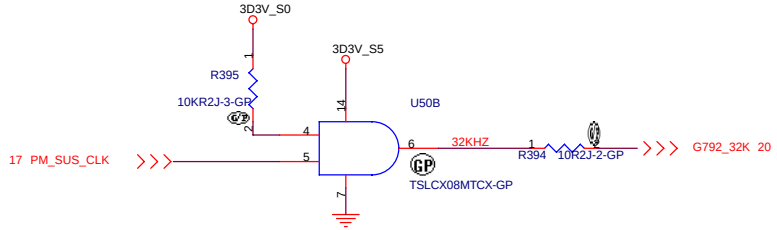

U24F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near AB3
No_STUFF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
Akita
Rev SC
Date: Saturday, February 04, 2006
Sheet 18 of 39

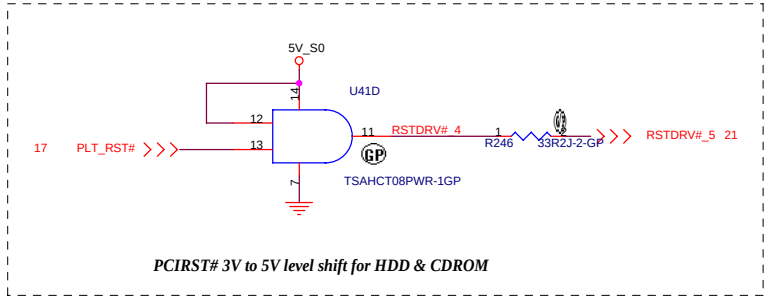
SMBUS



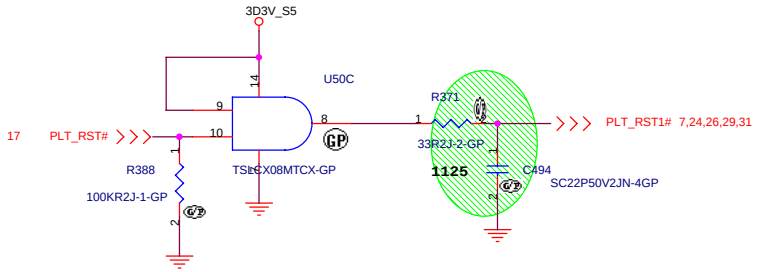
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

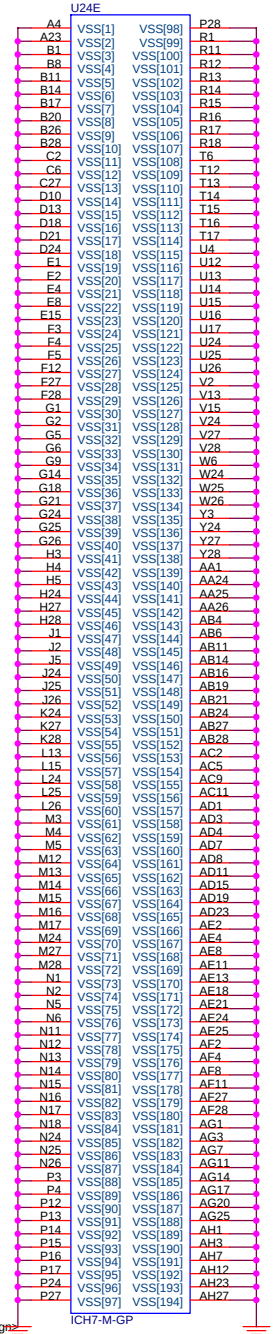
32K suspend clock output





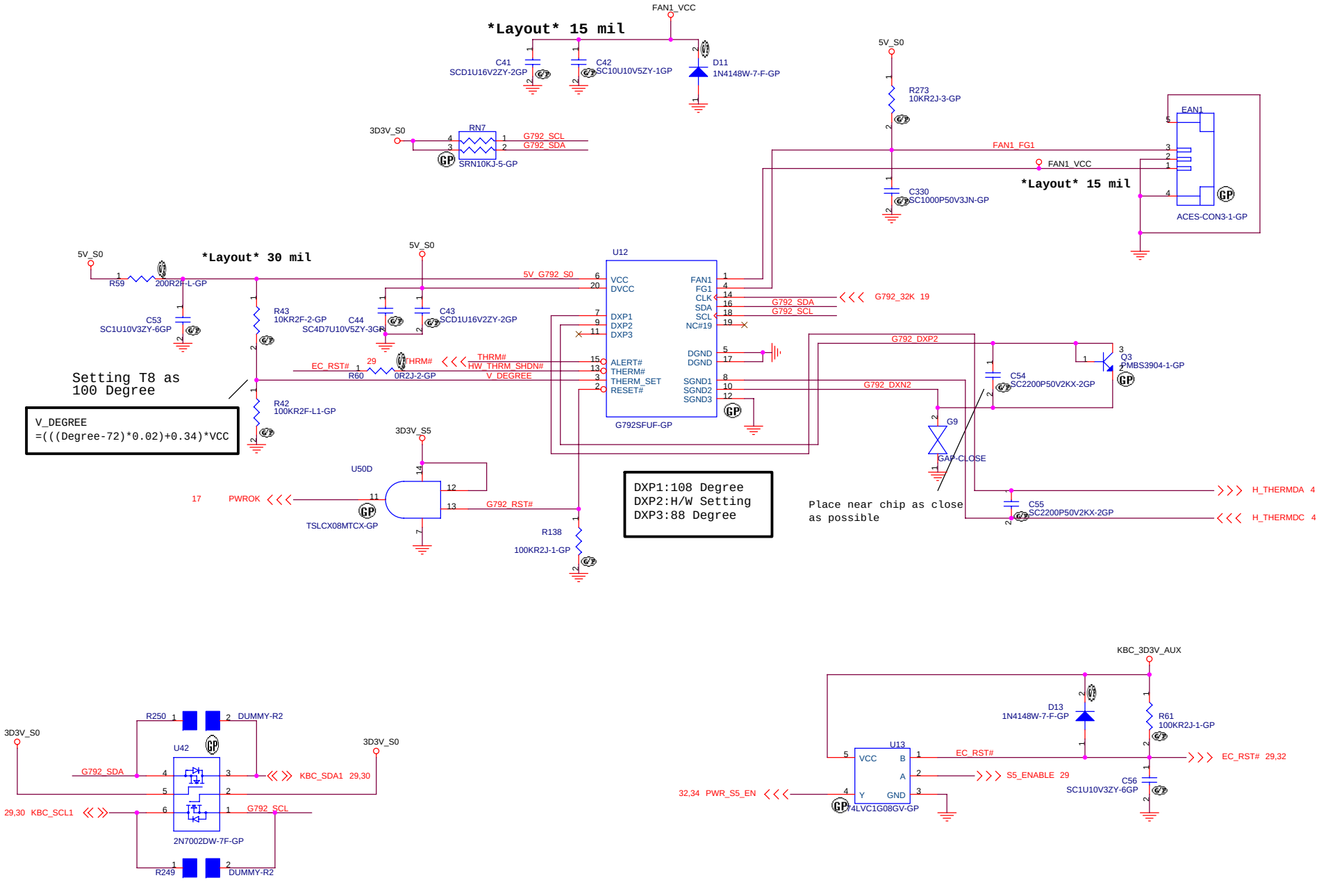
PCIRST# 3V to 5V level shift for HDD & CDROM





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ICH7-M (4 of 4)*		
Size: A3	Document Number: Akita	Rev: SC
Date: Sunday, February 05, 2006	Sheet 19 of 39	



<Core Design>

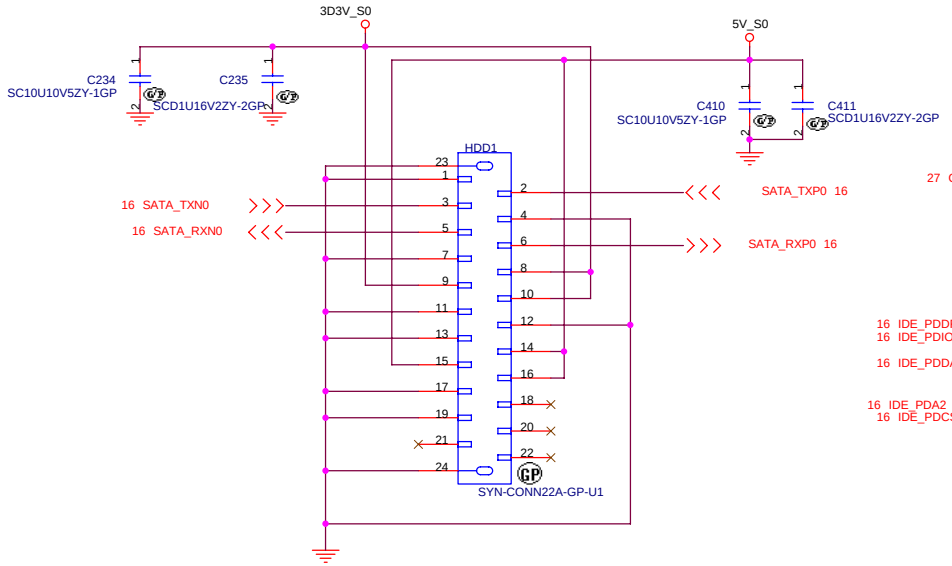
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

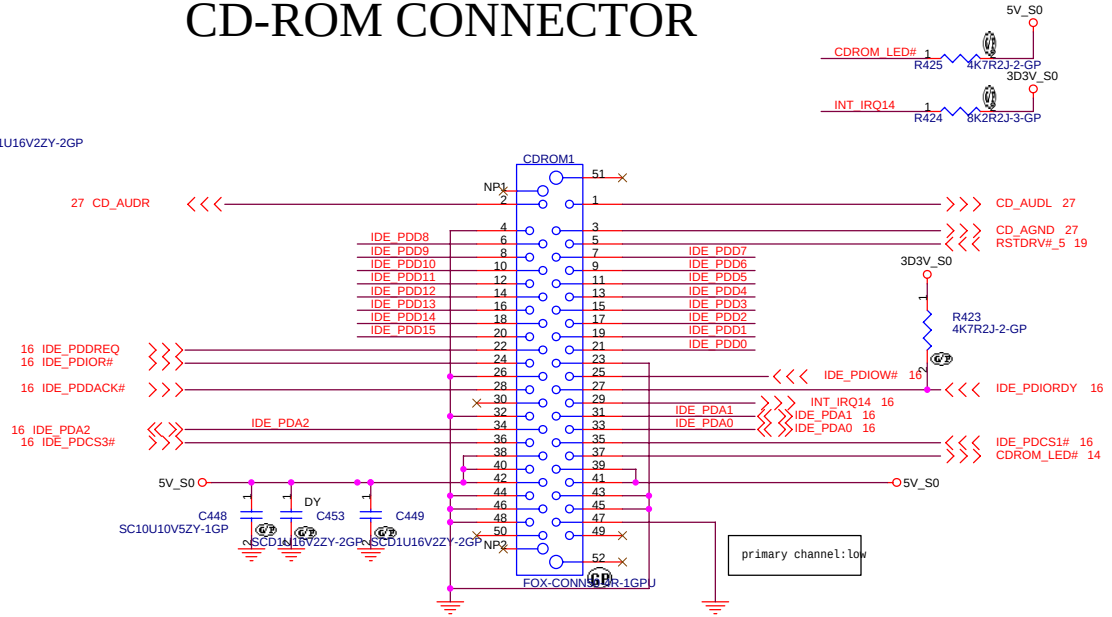
Size	Document Number	Rev
Custom	**Akita**	**SC**

Date: Sunday, February 05, 2006 Sheet 20 of 39

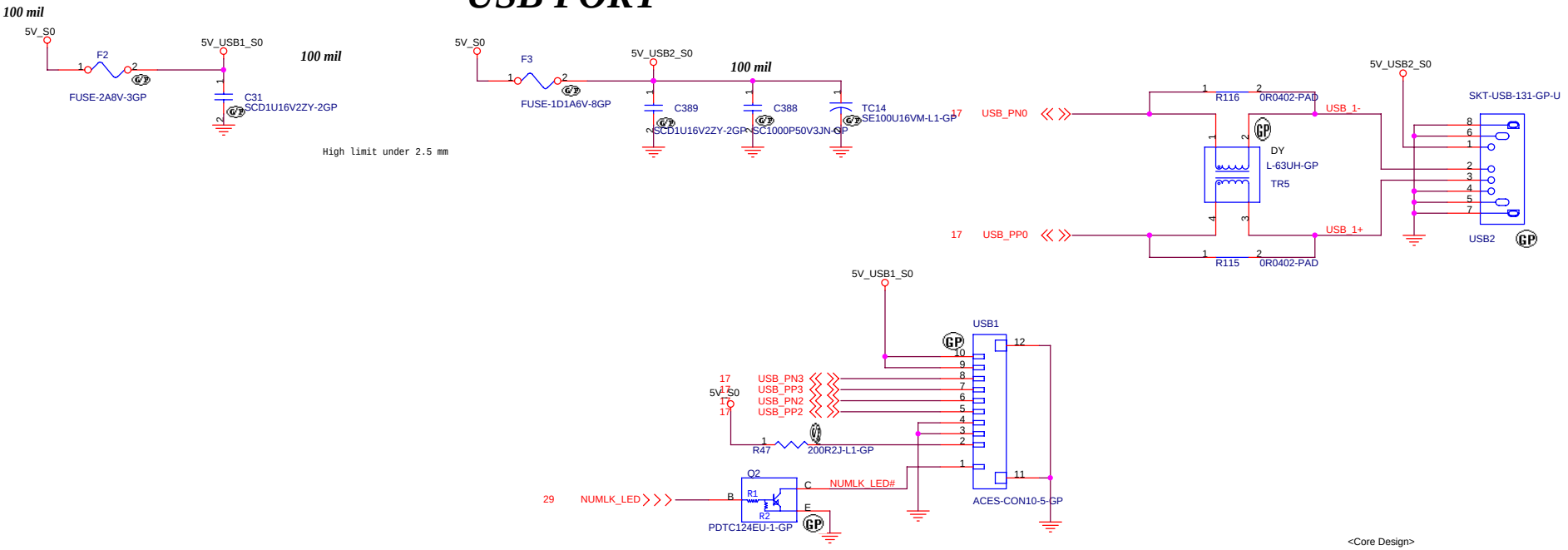
SATA HD Connector



CD-ROM CONNECTOR

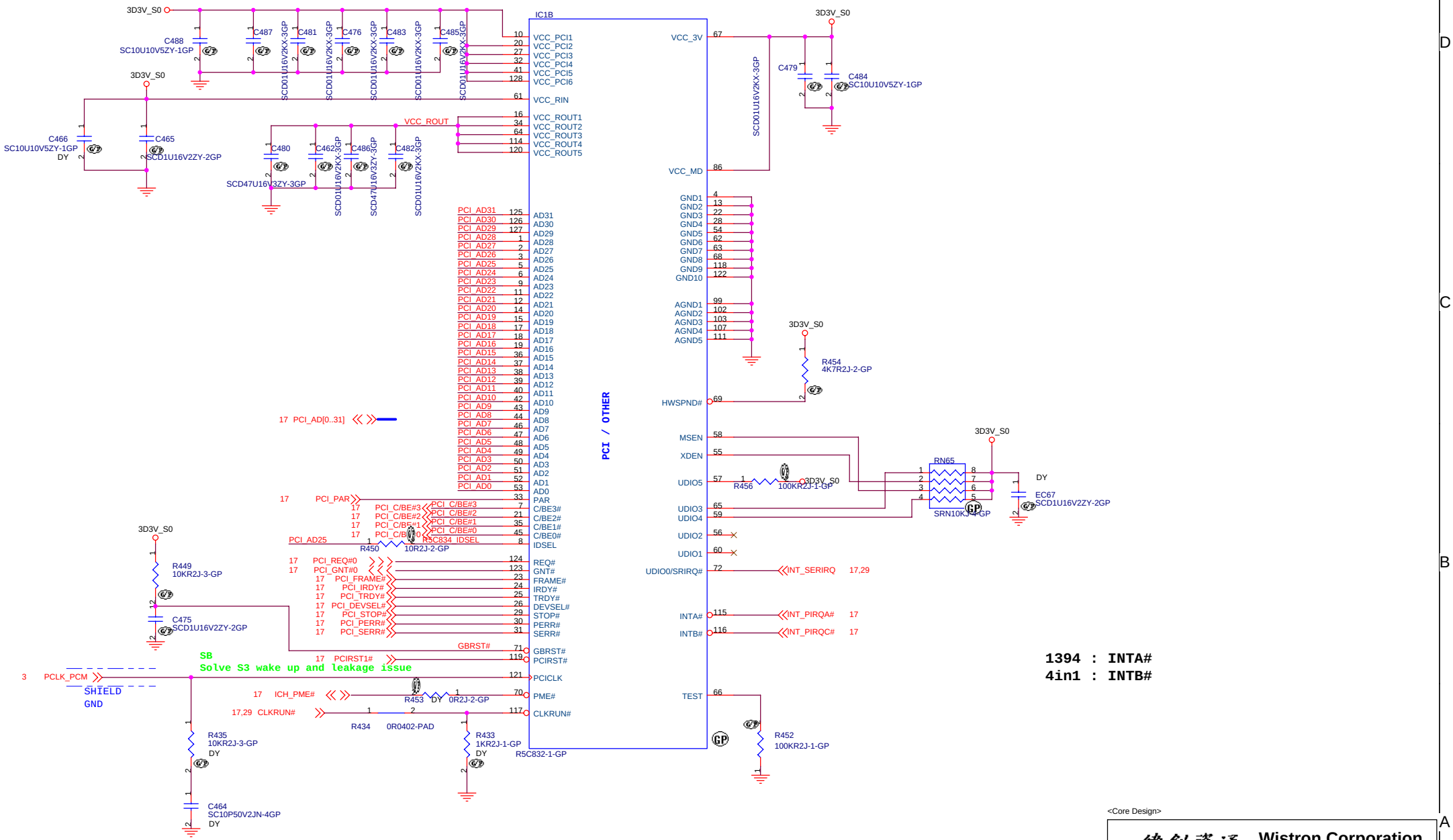


USB PORT



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HD/CDROM***
Size A3	Document Number **Akita** Rev **SC**
Date: Sunday, February 05, 2006	Sheet 21 of 39



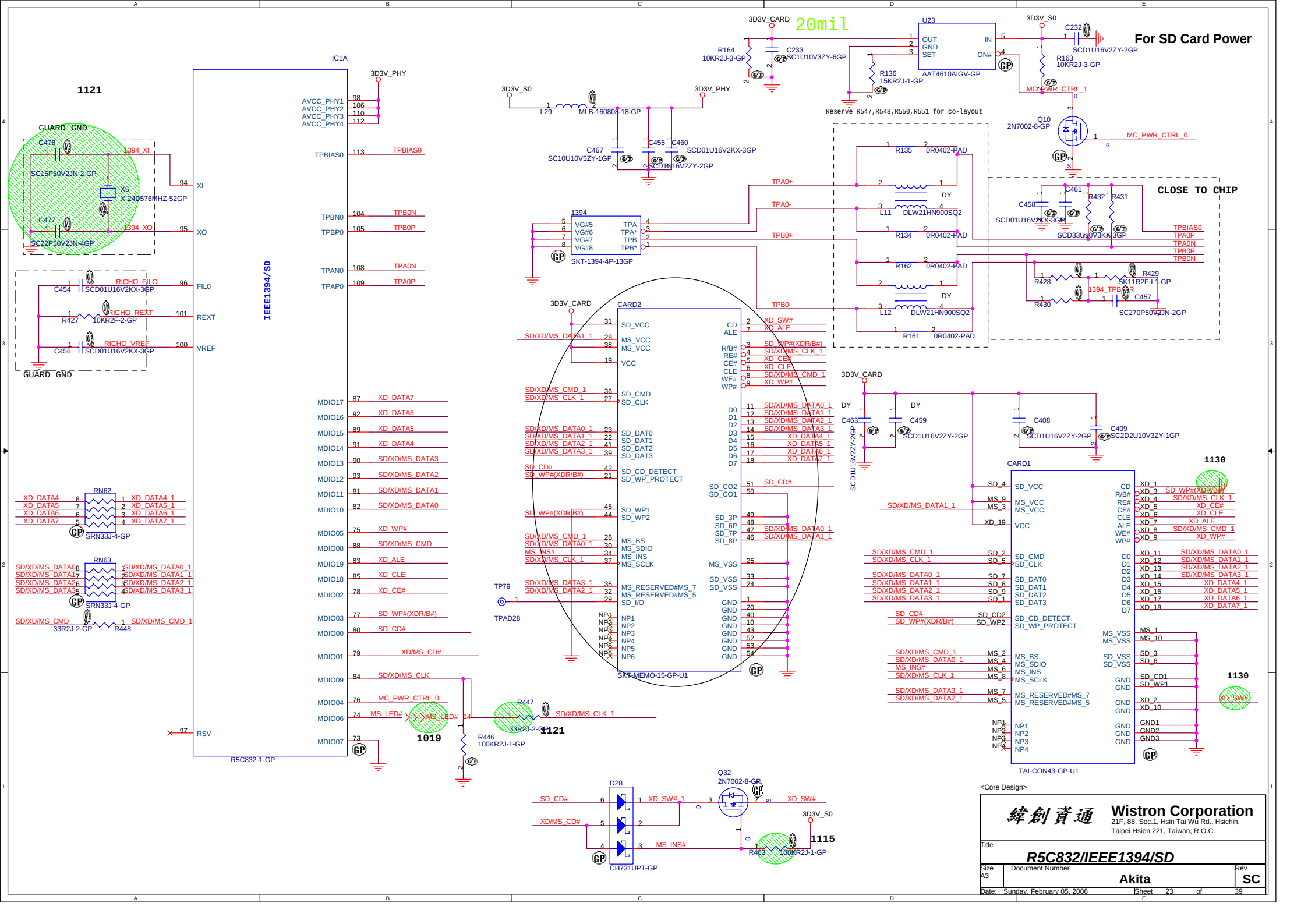
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C832/PCI***

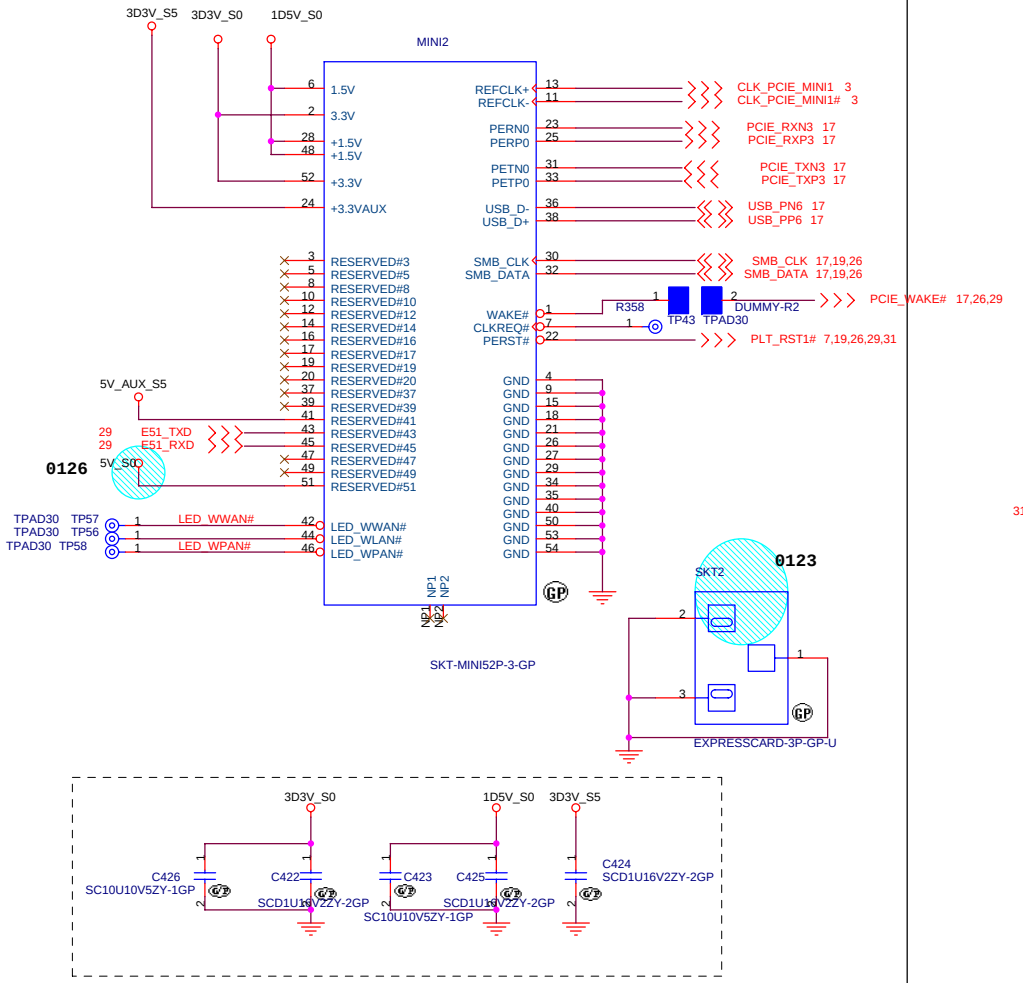
Size: A3 | Document Number: **Akita** | Rev: **SC**

Date: Sunday, February 05, 2006 | Sheet 22 of 39

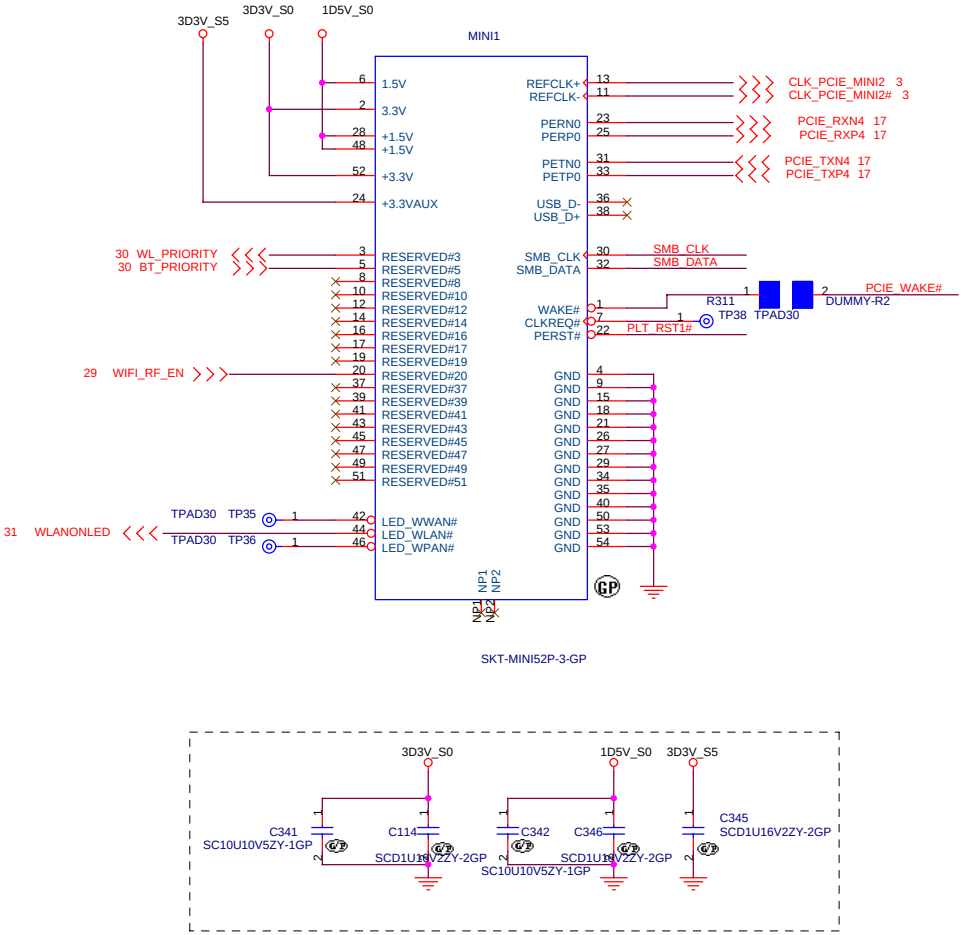

For SD Card Power
CLOSE TO CHIP
IC1A
IEEE1394/SD
R5C832-1-GP
CARD2
SKT-MEMO-15-GP-U1
CARD1
TAI-CON43-GP-U1
SKT-1394-4P-13GP
AAT4610AIGV-GP
CH731UPT-GP
Reserve R547,R548,R550,R551 for co-layout
20mil
1121
1019
1115
1130
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Akita
SC
Sunday, February 05, 2006
23
39

Mini Card Connector

Mini Card Connector 1

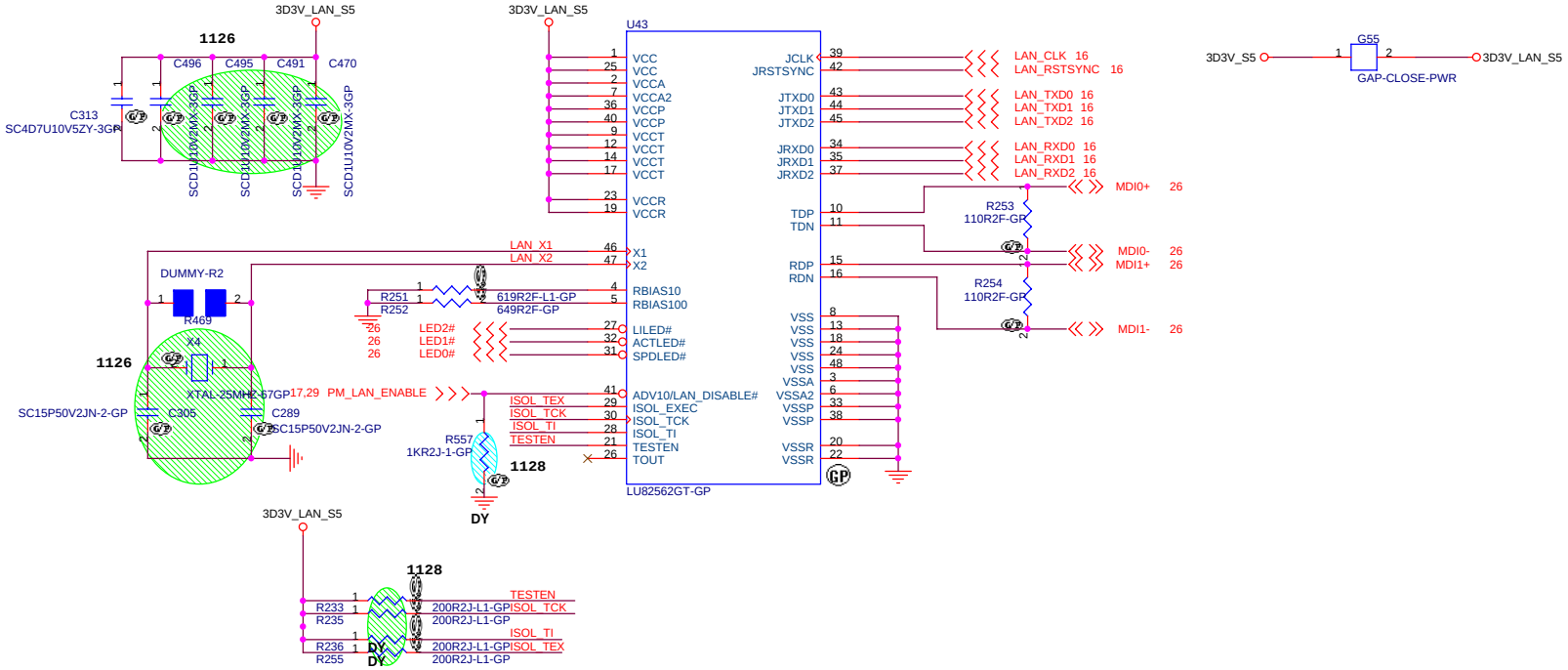


Mini Card Connector 2



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD CONN .***
Size: A3	Document Number: **Akita** — Rev: **SC**
Date: Sunday, February 05, 2006	Sheet 24 of 39



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN TEKOA***

Size	Document Number	Rev
A3	**Akita**	**SC**

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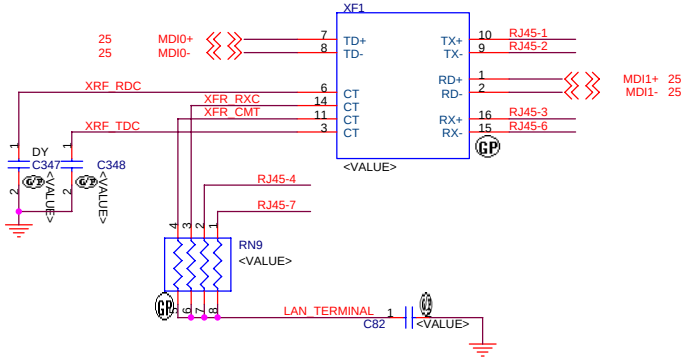
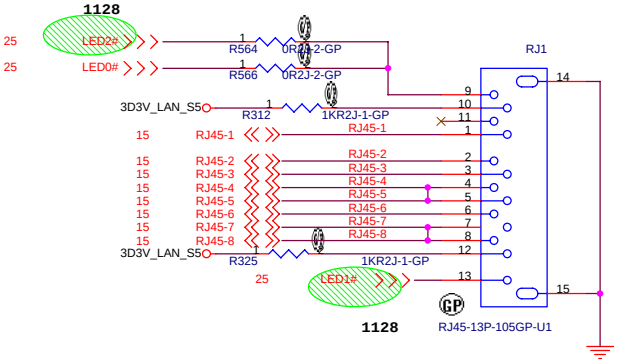
10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps

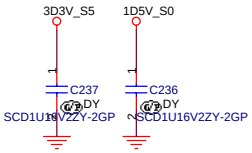


Green : Link up
Blinking : TX/RX activity

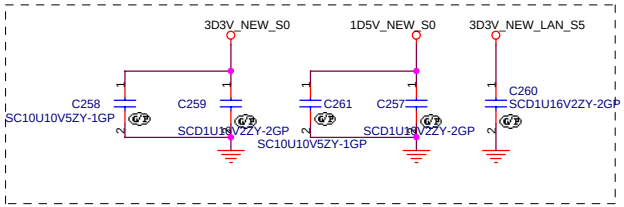
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

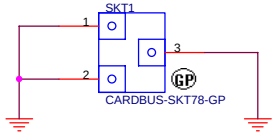
NEWCARD Connector

Place them Near to Chip

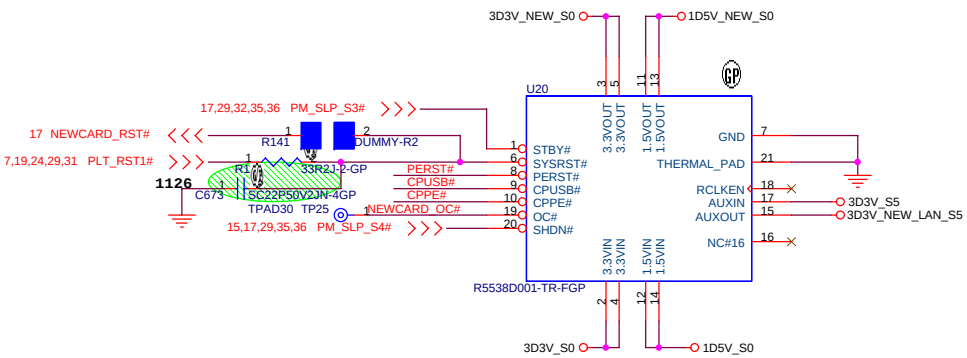


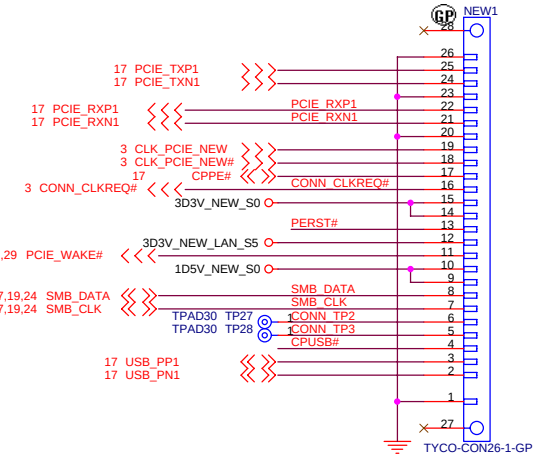
Place them Near to Connector





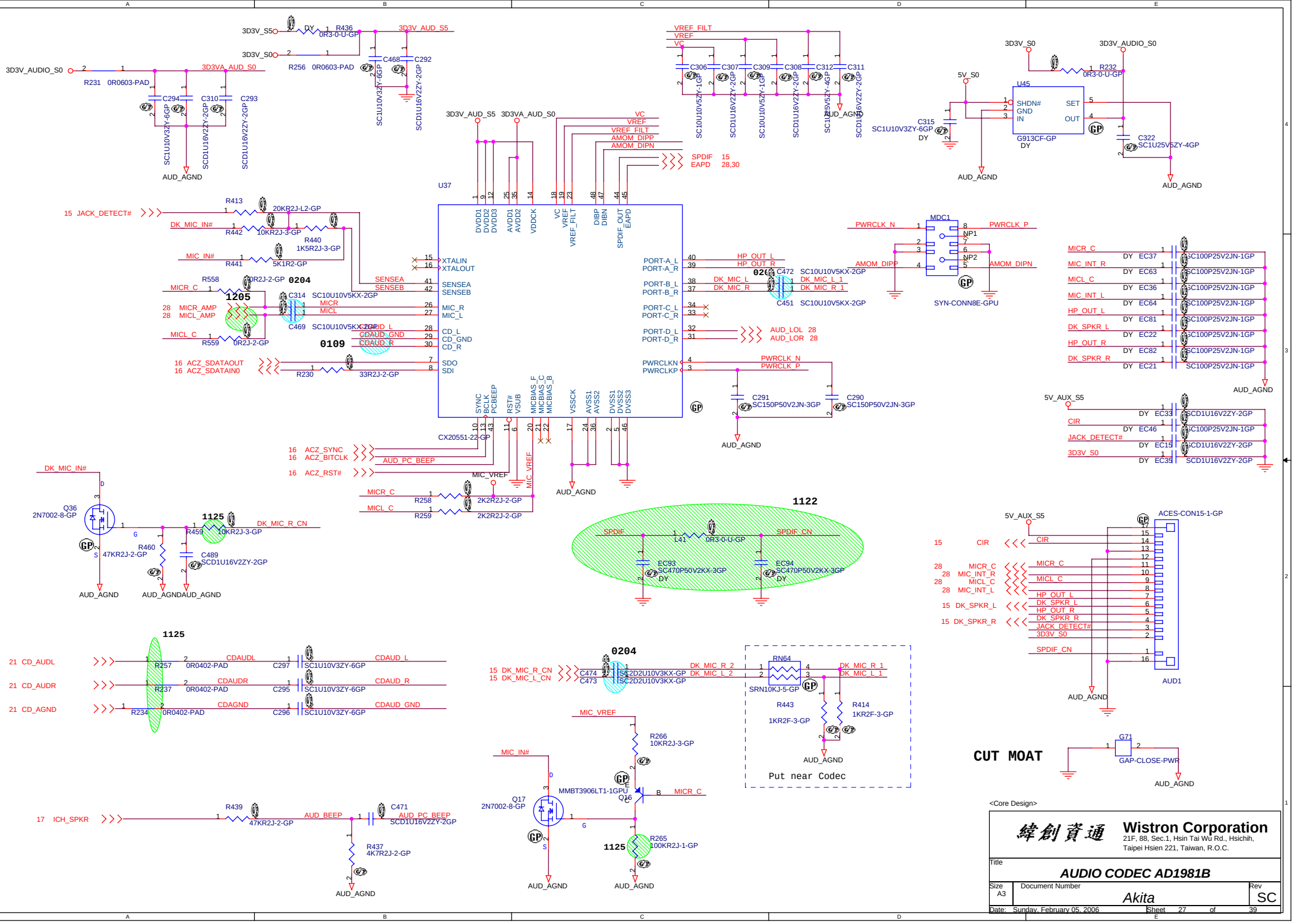
For Newcard socket





<Core Design>

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***New Card***		
Size: A3	Document Number: **Akita**	Rev: **SC**
Date: Sunday, February 05, 2006	Sheet 26 of 39	



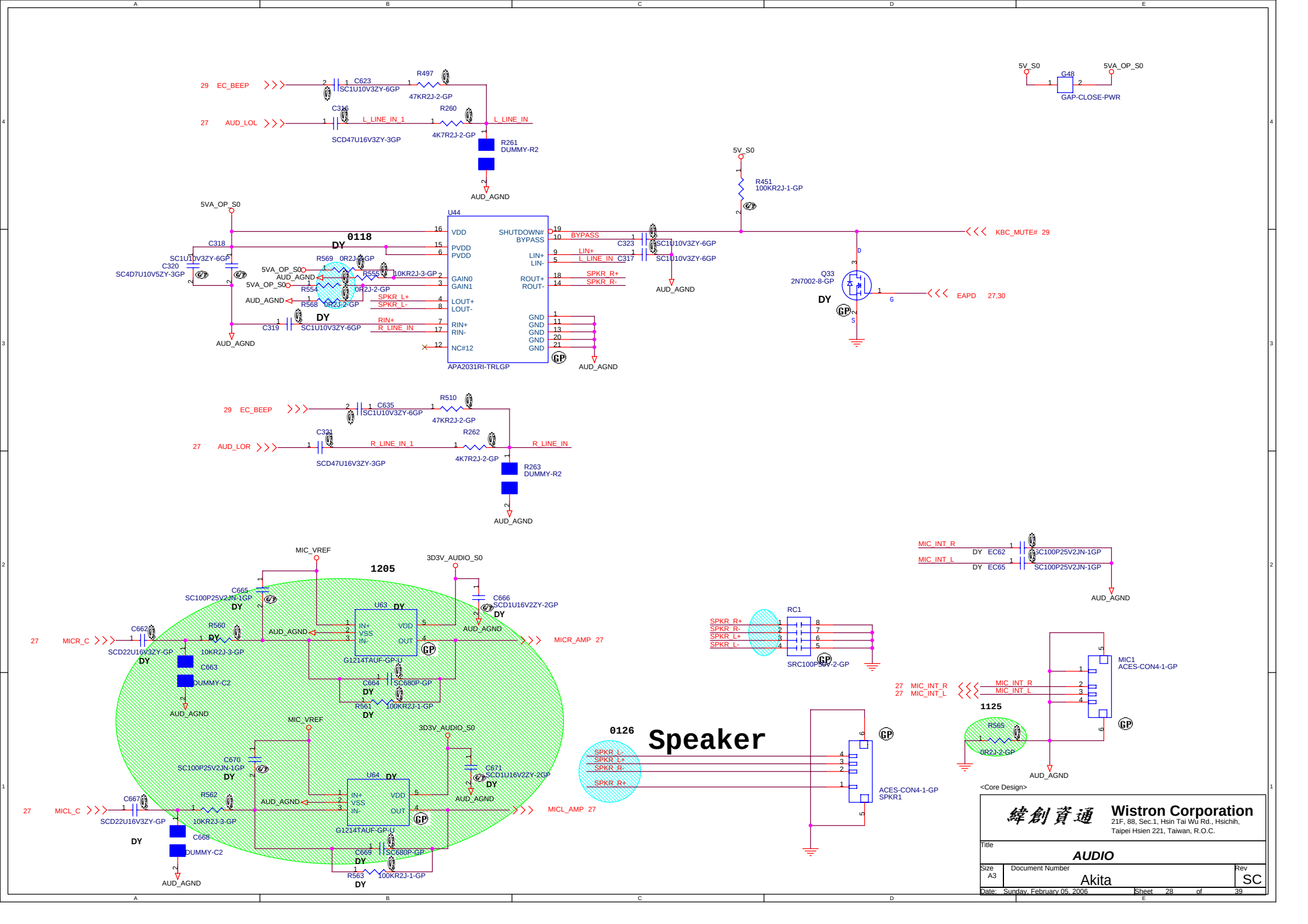
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO CODEC AD1981B***

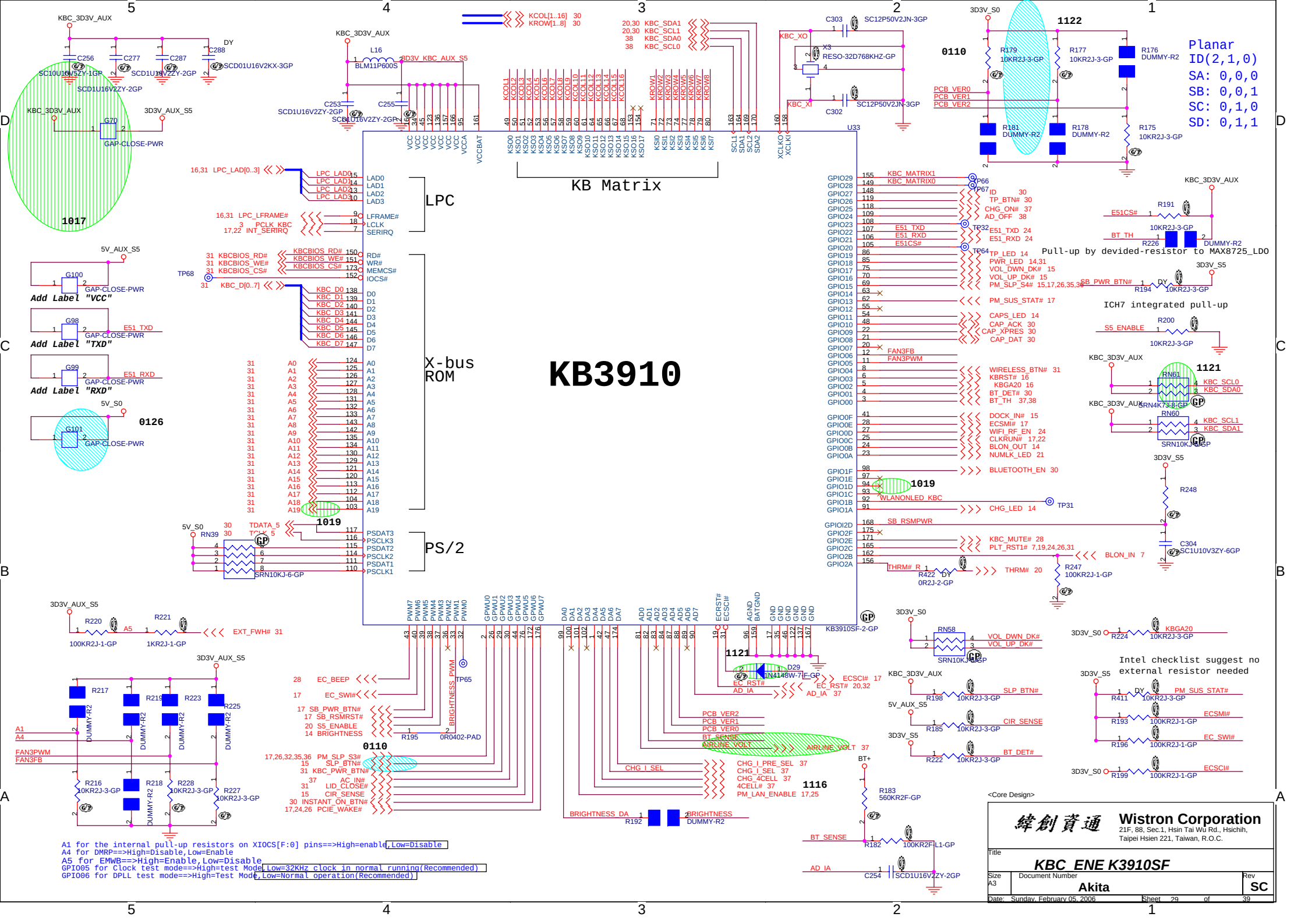
Size	Document Number	Rev
A3	*Akita*	SC

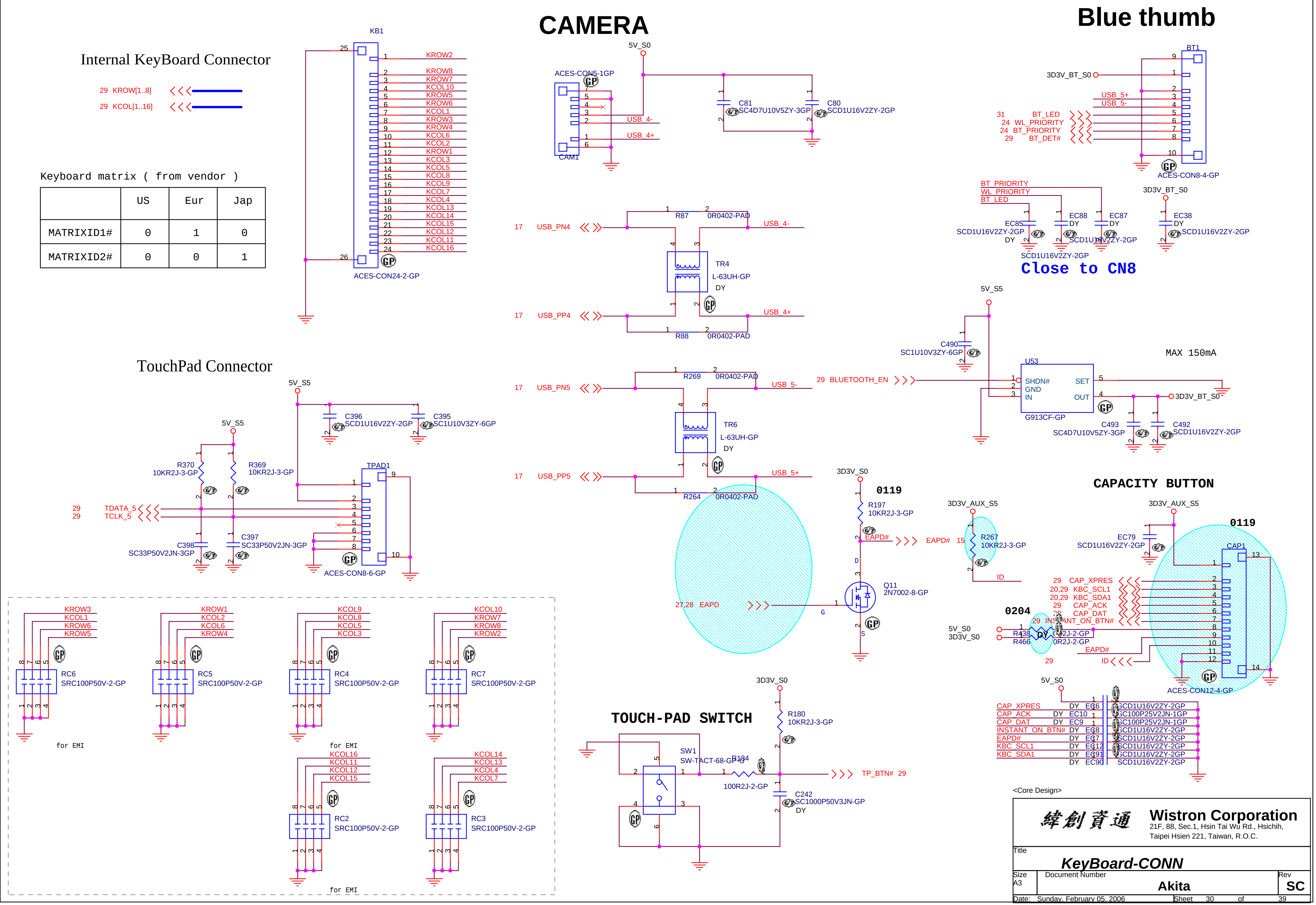
Date: Sunday, February 05, 2006 Sheet 27 of 39



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AUDIO***	
Size A3	Document Number Akita	Rev SC
Date: Sunday, February 05, 2006	Sheet 28 of 39	


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
KB3910SF-2-GP
U33
Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Akita
Date: Sunday, February 05, 2006
Sheet 29 of 39



CAMERA
Blue thumb
Internal KeyBoard Connector
29 KROW[1..8]
29 KCOL[1..16]
KB1
ACES-CON24-2-GP
KROW2 KROW8 KROW7 KCOL10 KROW5 KROW6 KCOL1 KROW3 KROW4 KCOL6 KCOL2 KROW1 KCOL3 KCOL5 KCOL8 KCOL9 KCOL7 KCOL4 KCOL13 KCOL14 KCOL15 KCOL12 KCOL11 KCOL16
Keyboard matrix (from vendor)
TouchPad Connector
TPAD1
ACES-CON8-6-GP
29 TDATA_5
29 TCLK_5
R370 10KR2J-3-GP
R369 10KR2J-3-GP
C396 SCD1U16V2ZY-2GP
C395 SC1U10V3ZY-6GP
C398 SC33P50V2JN-3GP
C397 SC33P50V2JN-3GP
5V_S5
5V_S0
ACES-CON5-1GP
CAM1
USB_4-
USB_4+
C81 SC4D7U10V5ZY-3GP
C80 SCD1U16V2ZY-2GP
17 USB_PN4
17 USB_PP4
R87 0R0402-PAD
R88 0R0402-PAD
TR4 L-63UH-GP DY
17 USB_PN5
17 USB_PP5
R269 0R0402-PAD
R264 0R0402-PAD
TR6 L-63UH-GP DY
USB_5-
USB_5+
BT1
ACES-CON8-4-GP
3D3V_BT_S0
31 BT_LED
24 WL_PRIORITY
24 BT_PRIORITY
29 BT_DET#
EC85 SCD1U16V2ZY-2GP DY
EC88 DY
EC87 DY
EC38 DY SCD1U16V2ZY-2GP
Close to CN8
MAX 150mA
C490 SC1U10V3ZY-6GP
U53 G913CF-GP
SHDN# GND IN SET OUT
29 BLUETOOTH_EN
C493 SC4D7U10V5ZY-3GP
C492 SCD1U16V2ZY-2GP
3D3V_S0
0119
R197 10KR2J-3-GP
EAPD#
EAPD# 15
Q11 2N7002-8-GP
27,28 EAPD
3D3V_AUX_S5
R267 10KR2J-3-GP
ID
CAPACITY BUTTON
EC79 SCD1U16V2ZY-2GP
CAP1
ACES-CON12-4-GP
29 CAP_XPRES
20,29 KBC_SCL1
20,29 KBC_SDA1
29 CAP_ACK
29 CAP_DAT
29 INSTANT_ON_BTN#
0204
R438 R466 0R2J-2-GP DY
EAPD#
29 ID
CAP_XPRES CAP_ACK CAP_DAT INSTANT_ON_BTN# EAPD# KBC_SCL1 KBC_SDA1
EC6 EC10 EC9 EC8 EC7 EC12 EC91 EC90
SCD1U16V2ZY-2GP SC100P25V2JN-1GP
TOUCH-PAD SWITCH
SW1 SW-TACT-68-GP-U
R184 100R2J-2-GP
R180 10KR2J-3-GP
C242 SC1000P50V3JN-GP DY
TP_BTN# 29
RC6 SRC100P50V-2-GP
RC5 SRC100P50V-2-GP
RC4 SRC100P50V-2-GP
RC7 SRC100P50V-2-GP
RC2 SRC100P50V-2-GP
RC3 SRC100P50V-2-GP
for EMI
<Core Design>

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

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Title: KeyBoard-CONN

Size: A3 | Document Number: Akita | Rev: SC

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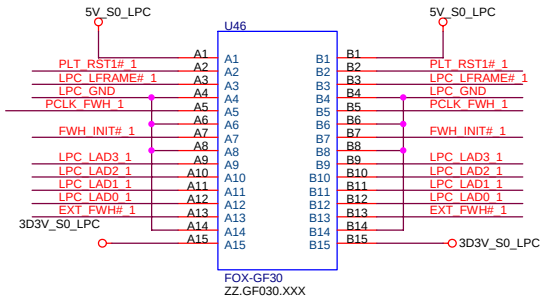
GOLDEN FINGER FOR DEBUG BOARD

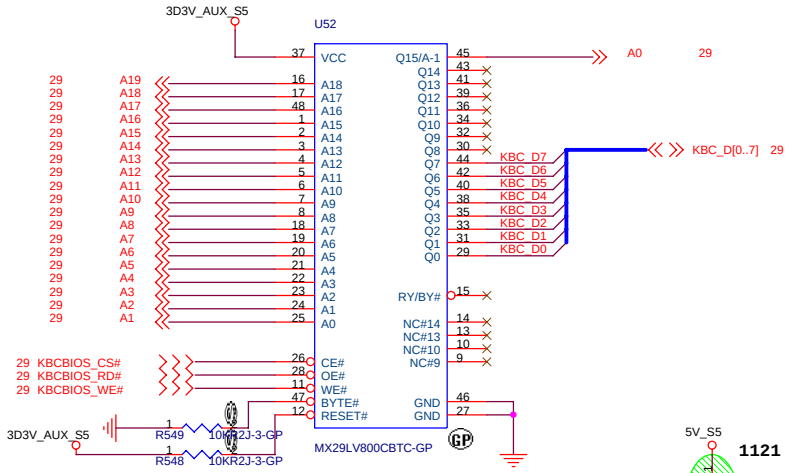


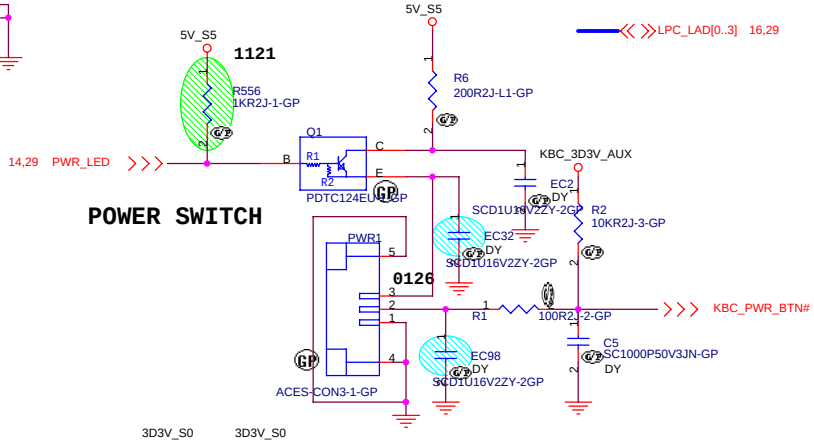
TOP VIEW

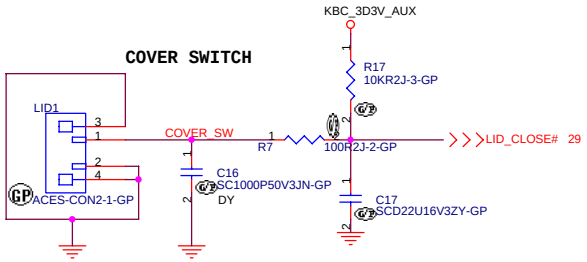
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

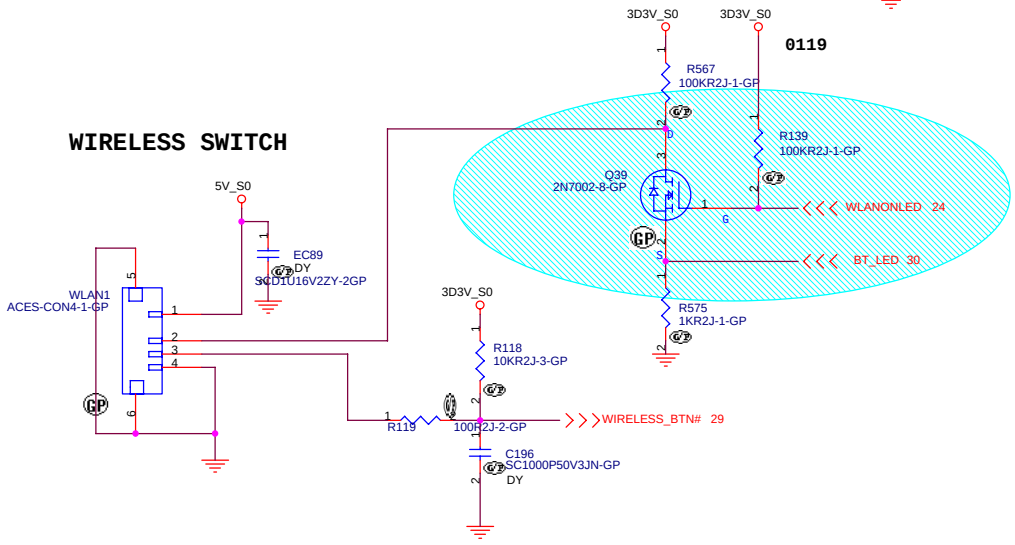
(BOTTOM VIEW)

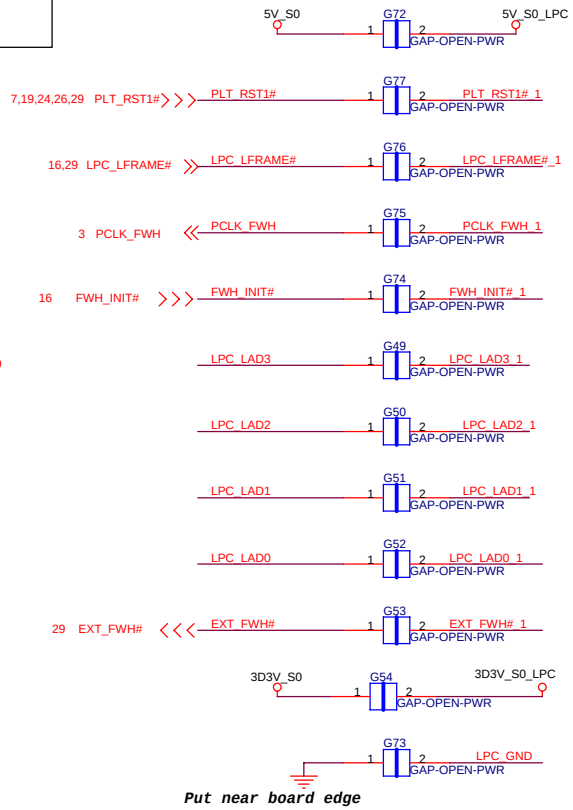
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46











<Core Design>

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Title: ***FWH and Debug***

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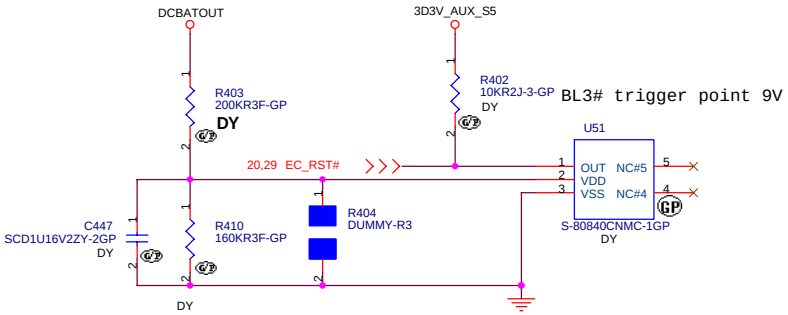
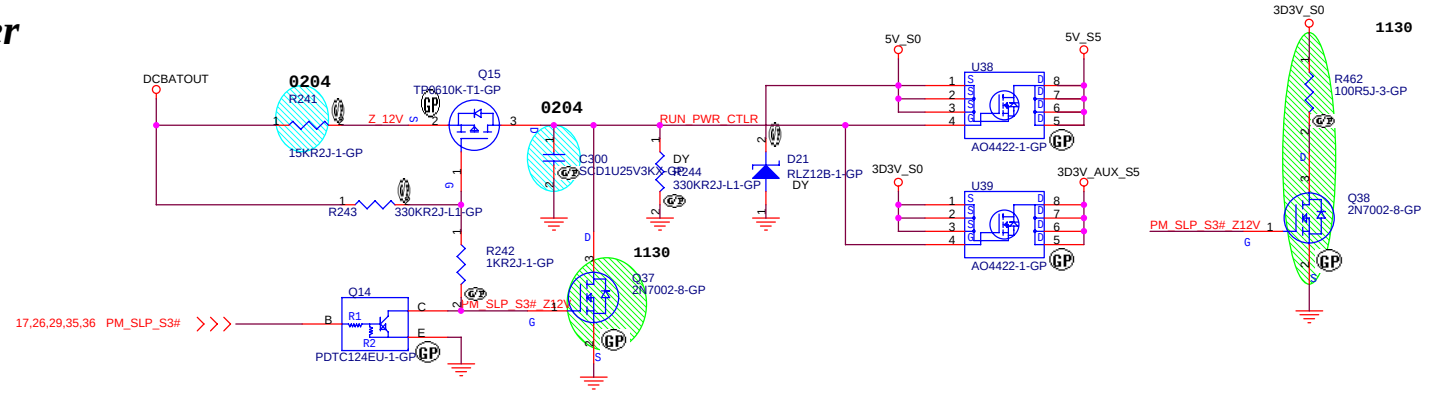
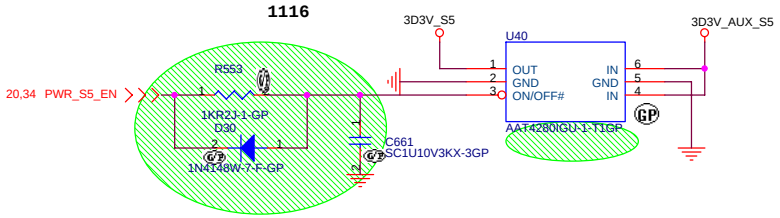


Run Power





<Core Design>

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Title: ***PWRPLANE&RESETLOGIC***

Size: A3 | Document Number: Akita | Rev: SC

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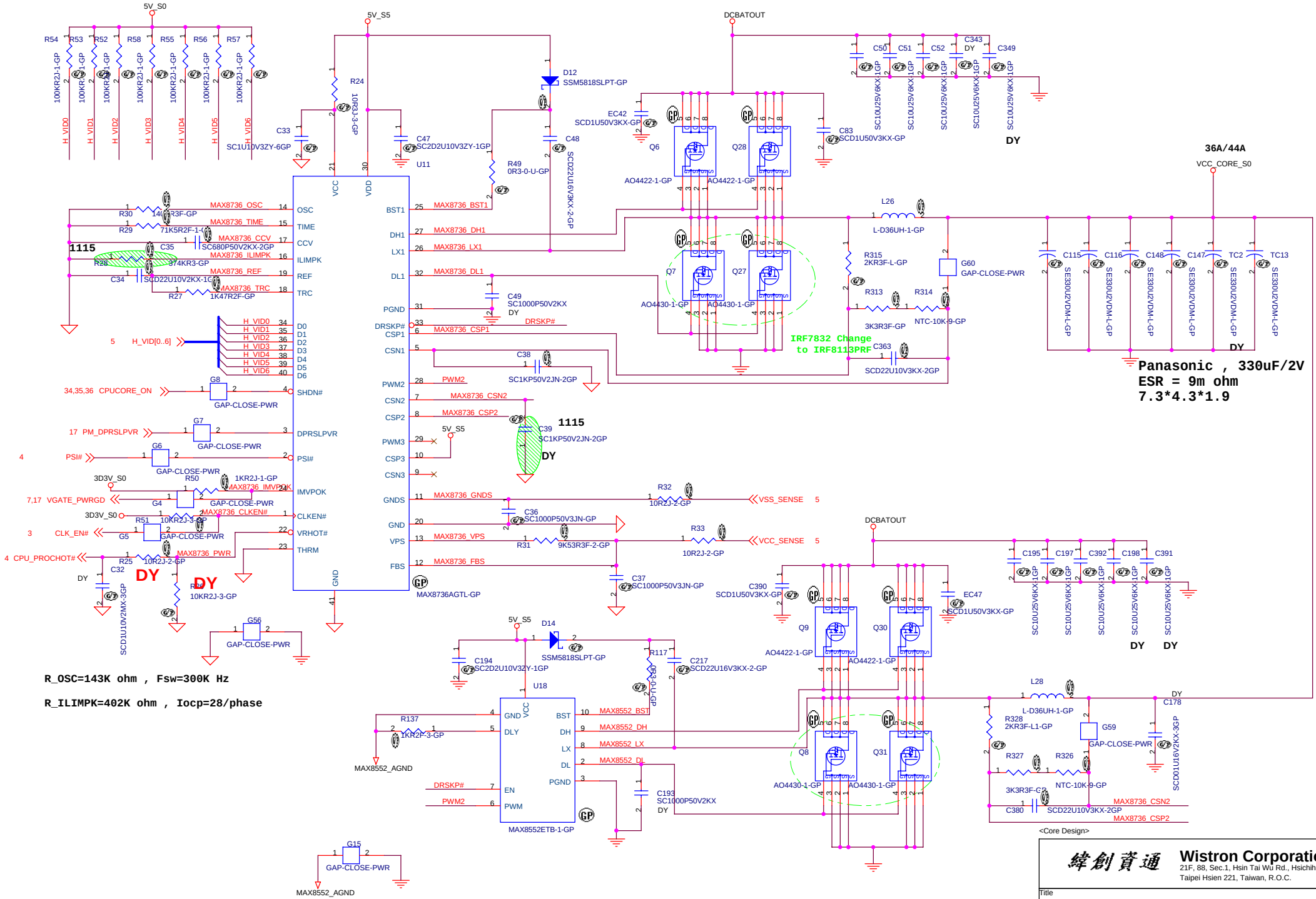

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Title: **DC-DC VCCCPUCORE**

Size	Document Number	Rev
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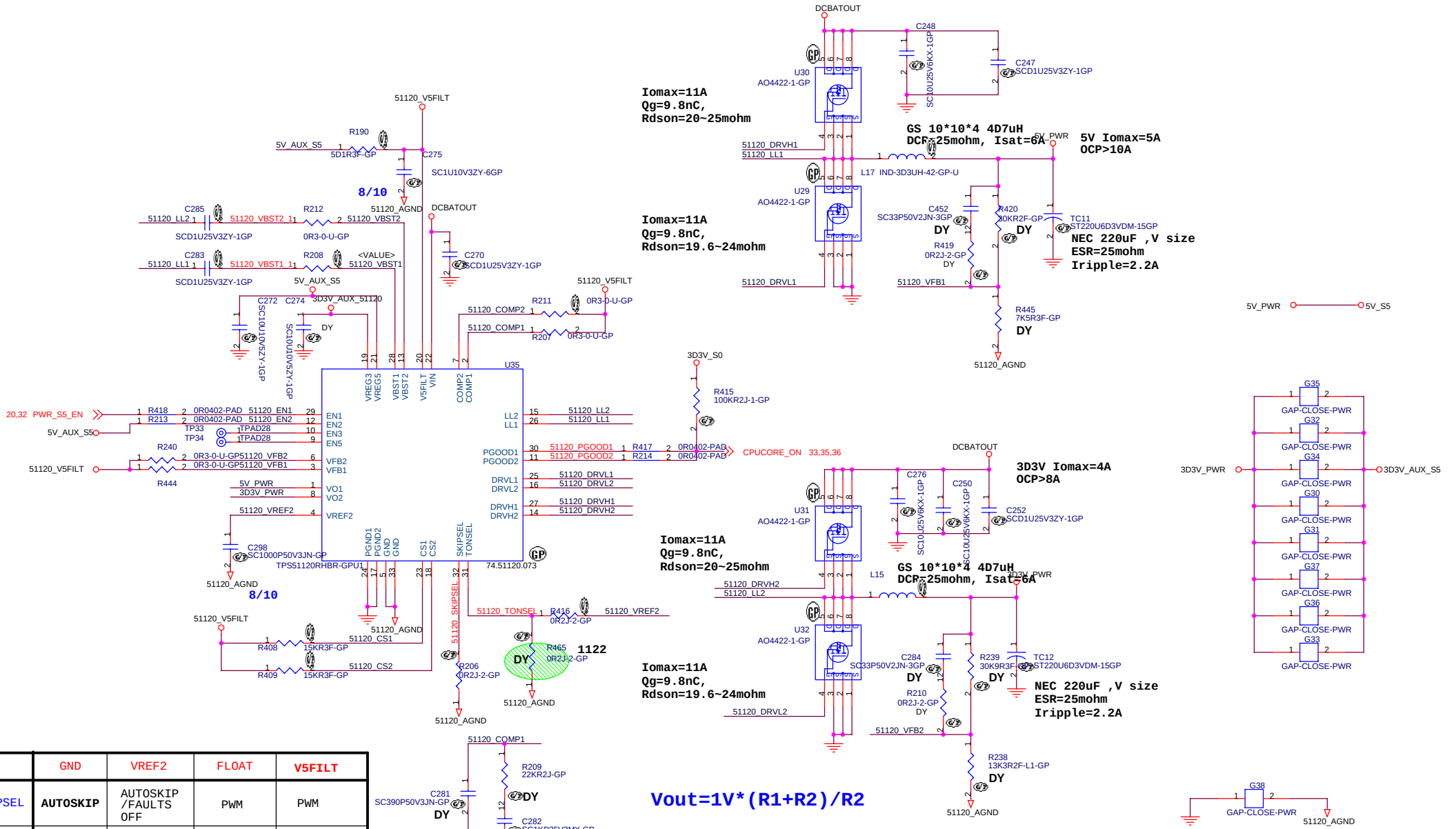
<Core Design>



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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Title: 5V_S5/3D3V_S5

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Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/7A
OCP>=14A

1D8V_S3 1D8V_PWR

G63 G62 G66 G65 G64 G67 G61 G68 — GAP-CLOSE-PWR

1D05V_PWR 1D05V_S0

G23 G20 G19 G18 G22 G21 G16 G17 — GAP-CLOSE-PWR

5V_S5

DCBATOUT

C229 SCD1U10V2MX-3GP
C228 SC1U10V3ZY-6GP
C243 SCD1U10V2MX-3GP
C231 SC1U25V5ZY-4GP

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R157 10R3J-3-GP

D16 BAW56-7-F-GP

MAX8743_BST2

MAX8743_VCC

C251 SC10U25V6KX-1GP
EC73 SCD1U25V3ZY-1GP

U27 AO4422-1-GP

8/18

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

R158 0R3-0-U-GP
C241 SCD1U25V3ZY-1GP

R360 100KR2F-L1-GP
C226 SC1U10V3ZY-6GP
R359 90K9R3F-GP
R365 100KR2F-L1-GP
R366 90K9R3F-GP
R156 0R3-0-U-GP
C227 SCD1U25V3ZY-1GP

MAX8743_ILIM2

U22 MAX8743EEI-1-GP

UVP VCC VDD V+ ILIM2 BST2 DH2 LX2 DL2 CS2 OUT2 FB2 ON2 PGOOD OVP GND ILIM1 BST1 DH1 LX1 DL1 CS1 OUT1 FB1 ON1 TON REF SKIP#

MAX8743_BST1
MAX8743_BST1R
MAX8743_ILIM1
MAX8743_BST2R
MAX8743_DH1
MAX8743_LX1
MAX8743_DL1
MAX8743_DH2
MAX8743_LX2
MAX8743_DL2
MAX8743_ON1
MAX8743_ON2
MAX8743_TON
MAX8743_PGOOD
MAX8743_VREF
MAX8743_FB1
MAX8743_FB2

L14

TC9 SE220U2D5VDM-3GP
C225 SCD1U25V3ZY-1GP
DY

Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

R169 8K2R3F-GP

U28 FDS6690DS-GP

8/18

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

0204
C393 SC1U10V3ZY-6GP
DY C394 SCD1U25V3ZY-1GP
74.08743.A79

Voutsetting=1.820V

R170 10KR3F-L-GP

5V_S5

MAX8743_VREF
R363 DUMMY-R2
DY R362 0R2J-2-GP
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R361 DUMMY-R2

15,17,26,29,36 PM_SLP_S4# R368 0R2J-2-GP MAX8743_ON1
17,26,29,32,36 PM_SLP_S3# R367 0R2J-2-GP MAX8743_ON2

0205
PM_SLP_S3# R268 220KR2J-L2-GP
DY R160 220KR2J-L2-GP
PM_SLP_S4#
MAX8743_SKIP#

C230 SC1000P50V3JN-GP DY
R159 0R2J-2-GP

DCBATOUT

EC76 SCD1U25V3ZY-1GP
C249 SC10U25V6KX-1GP
C240 SC10U25V6KX-1GP

U26 AO4422-1-GP

8/18

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

U25 FDS6690DS-GP

L13

TC8 SE220U2VDM-8GP
DY C224 SCD1U25V3ZY-1GP

Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

R132 5K11R3F-1-GP
R133 100KR3F-GP

Voutsetting=1.0511V

Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

R364 0R0402-PAD CPUCORE_ON 33,34,36

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

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Title: *1D8V_S3/1D5V_S0*

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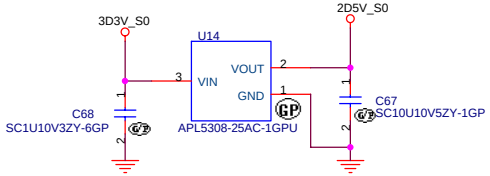
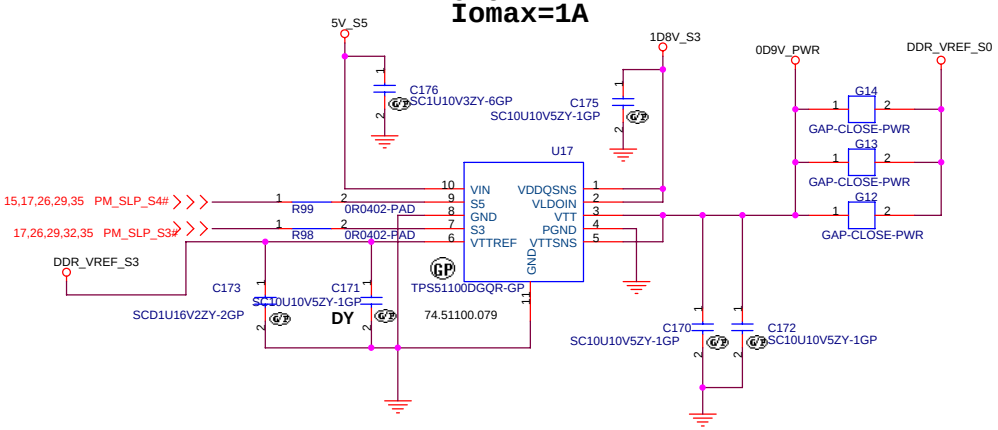
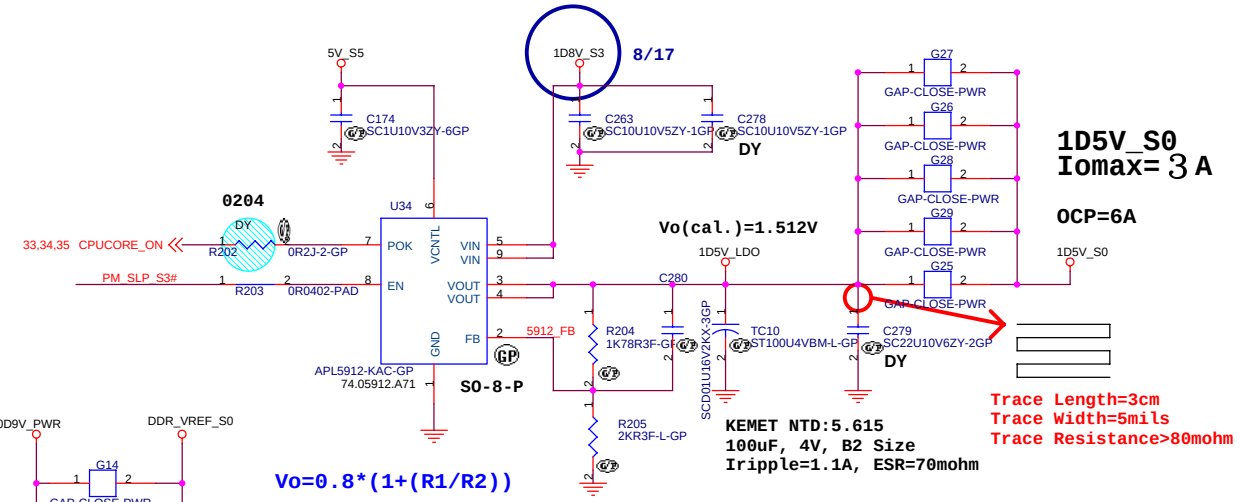
2D5V_S0
Iomax=300mA



0D9V
Iomax=1A





1D5V_S0
Iomax= 3 A

OCP=6A

Vo=0.8*(1+(R1/R2))

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Title	***0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO***
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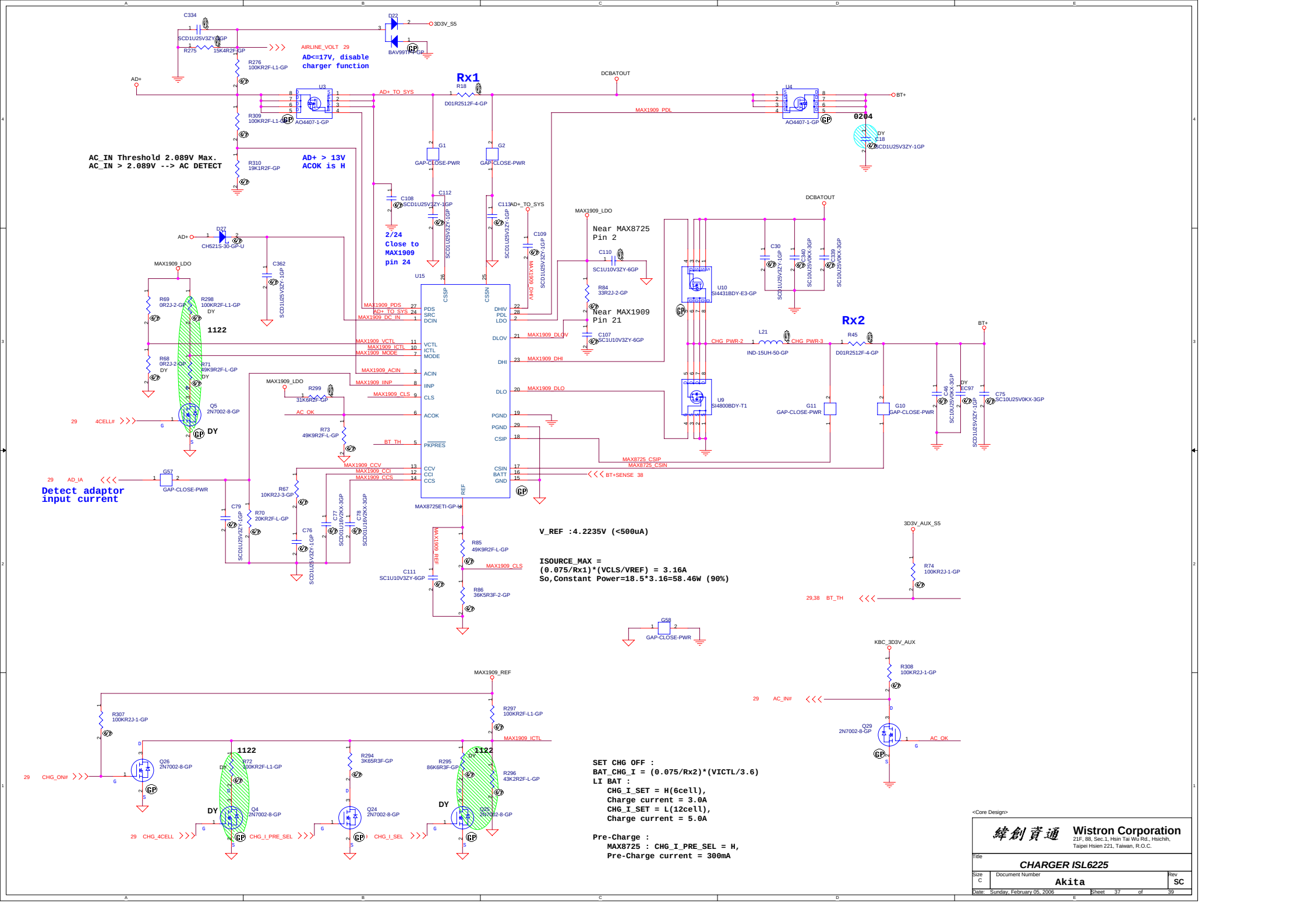

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Title: CHARGER ISL6225

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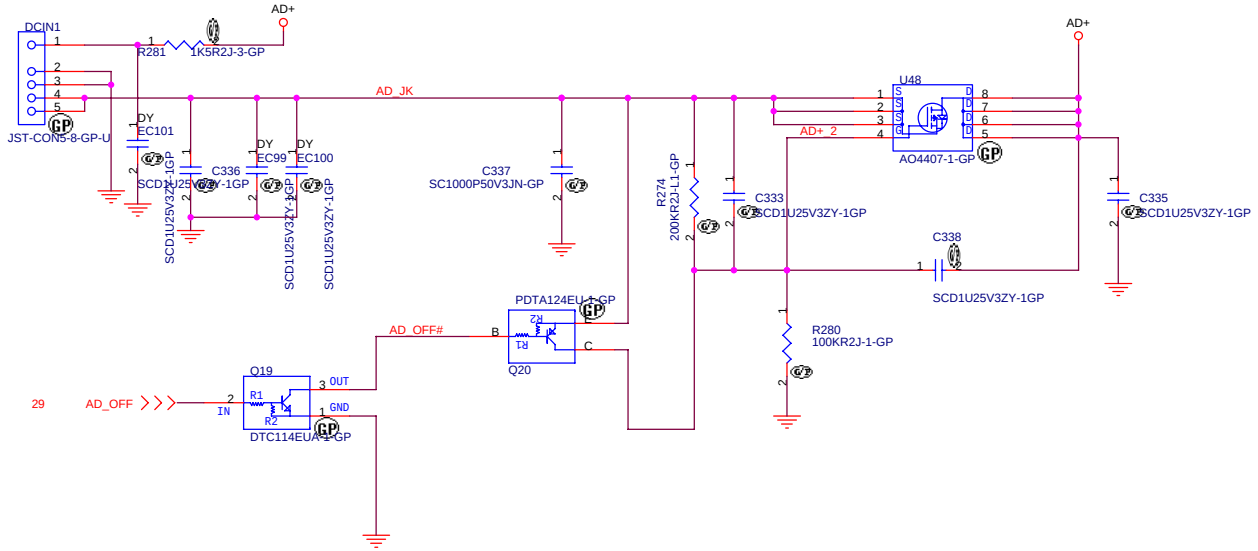
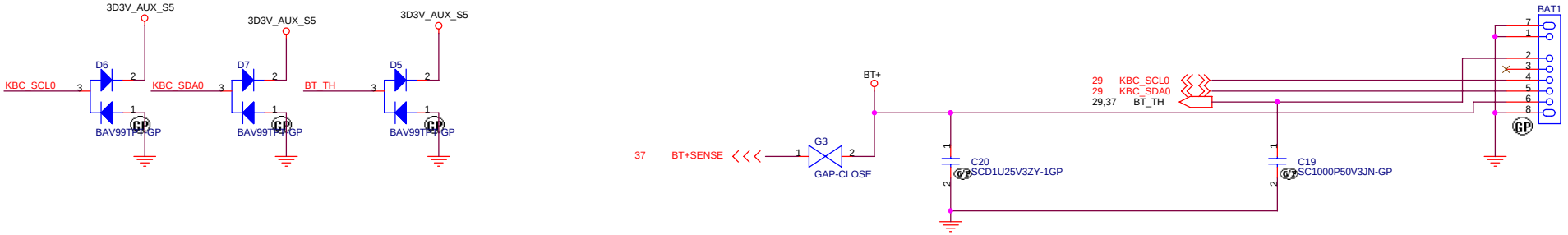
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Title: **AD/BATT CONN**

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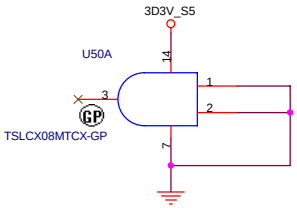

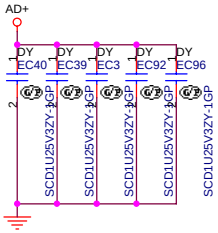

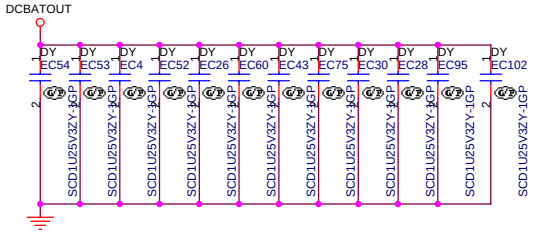

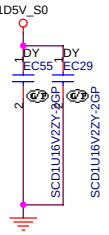

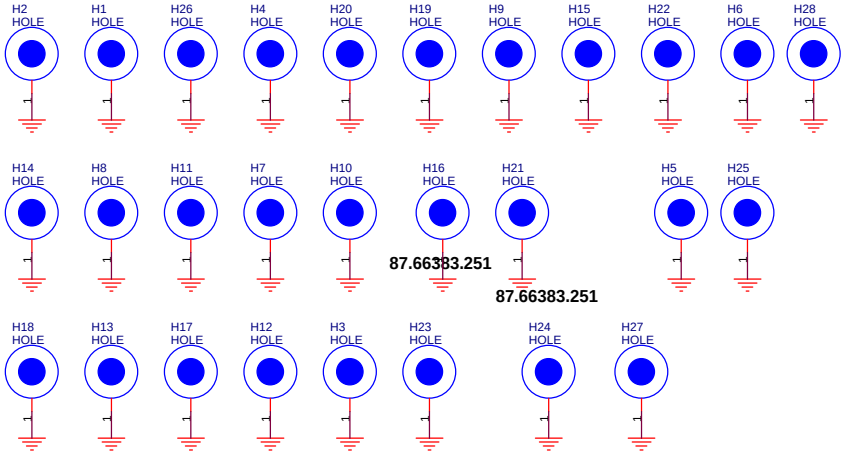

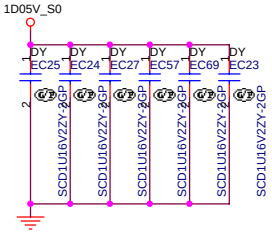

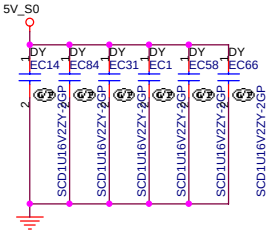

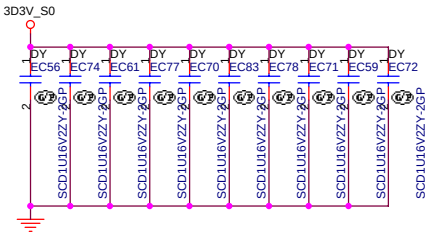

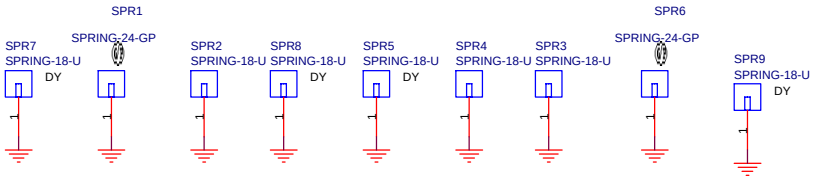

<Core Design>

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Title: ***MISC***

Size: A3 | Document Number: **Akita** | Rev: **SC**

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