Hardware Functional Overview
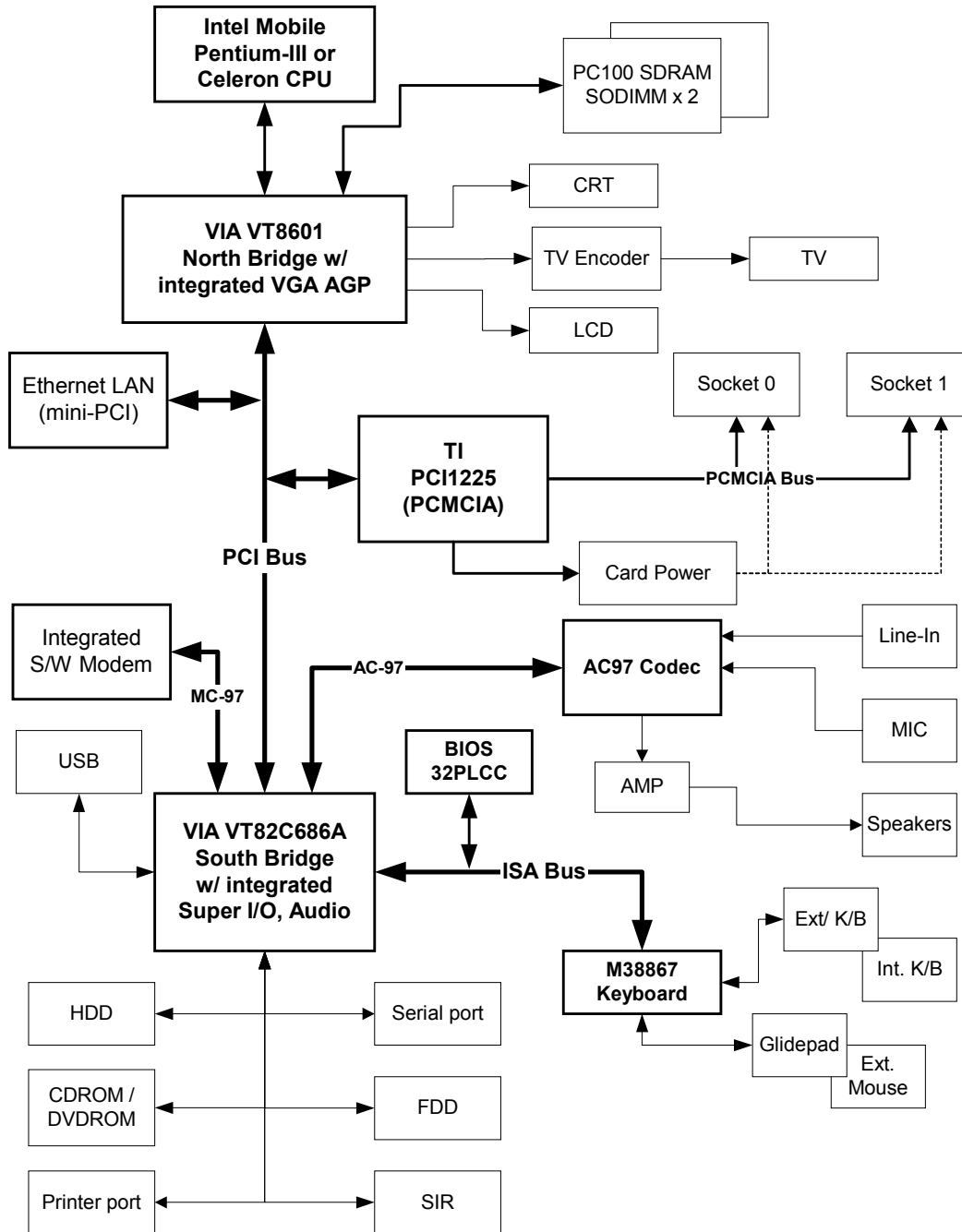
4.1 Overview

The FIC A440 Series consist of several major functions and subsystems (see Figure 4-1) including:

- System Processor – implemented on the motherboard using Intel Pentium-III or Mobile Celeron with Socket 370 FC-PGA packaging at 100MHz system bus speed.

- System North Bridge Core Logic – implemented on the motherboard using the VIA ProMedia VT8601 chipset which integrates the following:
    - Trident CyberBladei1 AGP 3D Graphics Accelerator
    - Advanced System Memory Controller

- System South Bridge Core Logic – implemented on the motherboard using the VIA VT82686A PCI-to-ISA chipset which integrates the following:
    - Enhanced IDE Interface for HDD, CD-ROM, and IDE Device Bay
    - SoundBlaster/DirectSound AC97 Digital Audio Controller
    - USB Interface for the external USB port
    - Super I/O

- Clock Frequency Generator – implemented on the motherboard using the ICWork W156 clock generator chip.

- Cache Memory Subsystem – implemented on-die on the Intel Mobile CPU.

- Video Subsystem – integrated on the VIA VT8601 North Bridge chip using Trident CyberBladei1 and on the LCD Panel for supporting the LCD and CRT.

- PCMCIA Subsystem – implemented on the motherboard using the Texas Instrument (TI) 1225 PCMCIA controller chip.

- Audio Subsystem – integrated on the VIA South Bridge chip.

- Keyboard and Pointing Device Subsystem – implemented on the AIO board, the Keyboard assembly, and the Glidepad assembly.

- I/O Subsystem – integrated on the VIA South Bridge chip.

- LAN and Modem Feature Card – implemented on the motherboard via the mini-PCI bus module socket.

- Port Bar – implemented on the motherboard and the Port Bar assembly.

- Power Subsystem – implemented on the DC-DC board, LCD Inverter Board, Battery Pack, and AC adapter.

- Micro-P Subsystem – implemented on the motherboard using PIC 16C62A.

Hardware Functional Overview

4.2   System Hardware Block Diagram

```
┌──────────────────┐                              ┌──────────────────┐
│  Intel Mobile    │                              │  PC100 SDRAM     │
│  Pentium-III or  │──────────────────────────────│  SODIMM x 2      │
│  Celeron CPU     │                              └──────────────────┘
└──────────────────┘

┌──────────────────┐         ┌──────────┐
│  VIA VT8601      │─────────│   CRT    │
│  North Bridge w/ │         └──────────┘
│  integrated      │         ┌────────────┐      ┌──────────┐
│  VGA AGP         │─────────│ TV Encoder │──────│    TV    │
└──────────────────┘         └────────────┘      └──────────┘
                             ┌──────────┐
                             │   LCD    │
                             └──────────┘

┌──────────────────┐                    ┌──────────┐   ┌──────────┐
│  Ethernet LAN    │                    │ Socket 0 │   │ Socket 1 │
│  (mini-PCI)      │                    └──────────┘   └──────────┘
└──────────────────┘

                   ┌──────────────┐
                   │     TI       │
                   │   PCI1225    │────────── PCMCIA Bus
                   │   (PCMCIA)   │
                   └──────────────┘
     PCI Bus                          ┌────────────┐
                                      │ Card Power │
                                      └────────────┘

┌──────────────┐                      ┌──────────────┐      ┌──────────┐
│ Integrated   │                      │ AC97 Codec   │──────│ Line-In  │
│ S/W Modem    │        AC-97         └──────────────┘      └──────────┘
└──────────────┘                                            ┌──────────┐
        MC-97                                               │   MIC    │
┌──────────┐   ┌──────────────────┐  ┌──────────┐           └──────────┘
│   USB    │   │ VIA VT82C686A    │  │  BIOS    │
└──────────┘   │ South Bridge     │  │ 32PLCC   │  ┌────────┐
               │ w/ integrated    │  └──────────┘  │  AMP   │
               │ Super I/O, Audio │                └────────┘  ┌──────────┐
               └──────────────────┘      ISA Bus               │ Speakers │
                                                               └──────────┘
┌──────────┐         ┌─────────────┐     ┌──────────────┐   ┌──────────┐
│   HDD    │         │ Serial port │     │   M38867     │   │ Ext/ K/B │
└──────────┘         └─────────────┘     │   Keyboard   │   └──────────┘
┌──────────┐         ┌─────────────┐     └──────────────┘   ┌──────────┐
│ CDROM /  │         │     FDD     │                        │ Int. K/B │
│ DVDROM   │         └─────────────┘      ┌──────────┐      └──────────┘
└──────────┘                              │ Glidepad │  ┌──────────┐
┌──────────────┐     ┌─────────────┐      └──────────┘  │  Ext.    │
│ Printer port │     │     SIR     │                    │  Mouse   │
└──────────────┘     └─────────────┘                    └──────────┘
```

Hardware Functional Overview

4.3   Chipset Summary

The notebook consists of following major chipsets:

Controller Chip	Vendor	Description
Processor	Intel	Socket 370 Pentium III at 650 – 850MHz
		Socket 370 Celeron at 500 – 667MHz
Core Logic	VIA	ProMedia VT8601 (North Bridge)
		ProMedia VT82C686A (South Bridge)
Video Controller	Trident	CyberBladei1 (Integrated in North Bridge)
PCMCIA Controller	TI	TI-1225 CardBus
Supper I/O Controller	VIA	(Integrated in South Bridge)
Audio Codec	WM	WM9701A (AC97 1.03) / WM9703 (AC97 2.1)
Audio Amplifier	TI	TDA0102
Keyboard Controller	Mitsubishi	M38867
PMU Controller	MicroChip	PIC16C62B (SSOP)
ROM BIOS	Winbond	W29C040P, Boot Block Structure
Clock Generator	IC Work	W156
Temperature Sensor	VIA	(embedded in South Bridge chip)
LVDS		THC63LVDM63A
LAN	Intel	82559 (10/100Mbs Fast Ethernet)
Modem	PCTEL	MC-97 S/W Modem (integrated in South Bridge)

4.4   System Processor (CPU)

The FIC A440 runs on Intel Mobile Pentium-III based on Socket 370 FCPGA packaging. It supports CPU with up to 850 MHz clock speed rating. The processor operates in conjunction with the RAM and ROM memory and the system control logic (e.g. VIA VT8601) to process software instructions (BIOS, Windows, and Applications).

4.4.1   Intel Mobile Pentium-III Features

Using Intel's advanced 0.18 micron process technology, the Intel mobile Pentium III processor is offered at speeds of 400MHz, 450MHz, and 500MHz while still offering lower power for long battery life. Other performance advancements include the addition of new Internet Streaming SIMD instructions, an advanced transfer cache architecture, and a processor system bus speed of 100MHz.

Intel Mobile Pentium III processor featuring Intel SpeedStep technology is the next dramatic step towards achieving near desktop performance. This exciting new processor has two performance modes and allows real-time dynamic switching of the voltage and frequency between the modes. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system.

There are two performance modes offered, Maximum Performance and Battery Optimized Performance. Maximum Performance mode provides near desktop performance and runs at 600 or 650MHz. Battery Optimized Performance mode provides the best balance between performance and battery life and operates at a lower frequency of 500MHz.

Hardware Functional Overview

The integrated L2 cache is designed to help improve performance, and it complements the system bus by providing critical data faster and reducing total system power consumption. The mobile Pentium III processor's 64-bit wide Gunning Transceiver Logic (GTL+) system bus provides a glue-less, point-to-point interface for an I/O bridge/memory controller, and is compatible with the 440BX AGPset, 440ZX-M AGPset, and the 440MX Chipset.

Features summary of the Mobile Pentium-III CPU:

- Processor core/bus speeds
  - Single frequency at 1.60V: 450/100 MHz and 500/100 MHz
  - Single frequency at 1.35V: 400/100 MHz and 500/100 MHz
  - Featuring Intel SpeedStep technology: 600/100 MHz and 650/100 MHz (Maximum Performance Mode at 1.60V) and 500/100 MHz (Battery Optimized Performance Mode at 1.35V)
- Supports the Intel Architecture with Dynamic Execution
- On-die primary (L1) 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level L2 cache (256-Kbyte)
- Integrated GTL+ termination
  6-bit data bus, 100-MHz operation
- Integrated math co-processor
- Intel Processor Serial Number
- Fully compatible with previous Intel microprocessors
  - Binary compatible with all applications
  - Support for MMX technology
  - Support for Streaming SIMD Extensions enhances floating point, video, sound, and 3-D application performance
- Power Management Features
  - Quick Start for low power, low exit latency clock "throttling"
  - Deep Sleep mode provide low power dissipation
- On-die thermal diode

4.4.2 Intel Mobile Celeron Features

The Intel Celeron processor is designed for uni-processor based Value PC and is binary compatible with previous generation Intel architecture processors. The Intel Celeron processor provides good performance for applications running on advanced operating systems such as Windows 95/98, Windows NT, and UNIX. This is achieved by integrating the best attributes of Intel processors – the dynamic execution performance of the P6 micro-architecture plus the capabilities of MMX technology – bringing a balanced level of performance to the Value PC market segment.

Features summary of the Mobile Celeron CPU:

- Available up to 700 MHz core frequencies with 128 KB level-two cache (on die)
- Intel's latest Celeron processors in the FC-PGA package are manufactured using the advanced 0.18 micron technology.
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Dynamic execution microarchitecture.
- Operates on a 66 MHz, transaction-oriented system bus.
- Specifically designed for uni-processor based Value PC systems, with the capabilities of MMX technology.

- Power Management Capabilities
- Optimized for 32-bit applications running on advanced 32-bit operating systems.
- Uses Flip-Chip Pin Grid Array (FC-PGA) Package. The FC-PGA uses the same 370-pin zero insertion force socket (PGA370) as the PPGA. Thermal solutions are attached directly to the back of the processor core package without the use of a thermal plate or heat speader.
- Integrated high performance 32 KB instruction and data, nonblocking, level-one cache: separate 16 KB instruction and 16 KB data caches.
- Integrated thermal diode.

4.5   System Core Logic

The system core logic function of the notebook is implemented on the CPU module and motherboard using the VIA Apollo ProMedia VT8601 North Bridge chip and the VIA VT82C686A South Bridge chip.

4.5.1   Apollo ProMedia Features

The VIA VT8601 Apollo ProMedia – System Media Accelerated North Bridge (SMA) – is a high performance, cost-effective and energy efficient solution for the implementation of Integrated 2D / 3D Graphics – PCI – ISA desktop and notebook personal computer systems from 66MHz to 133MHz based on 64-bit Intel Pentium II, Pentium III, and Celeron processors.

Summary Features of the VT8601:

- Supports Intel Celeron, Pentium III and VIA Cyrix III processors
- 66 / 100 / 133 MHz Front Side Bus (FSB) settings
- Integrated Trident Blade3D AGP 2X graphics core
- Support for PC133 SDRAM as well as PC66/100 SDRAM and Virtual Channel memory
- Integrated AC-97, MC-97 Audio/Modem
- Integrated 10/100 Base-T Ethernet controller
- Integrated Super I/O and IOAPIC
- Support for ATA 33/66/100
- Support for CRT, LCD or TV display
- 4 USB ports, UHCI compliant
- Integrated hardware monitoring
- Advanced mobile power management features
- 510 BGA VT8601 North Bridge

The VT8601 functions and capabilities include:

- General
  - 510 BGA Package
  - 2.5V core with 3.3V CMOS I/O
  - Supports GTL+ I/O buffer Host interface
  - Supports separately powered 5.0V tolerant interface to PCI bus and Video interface
  - 2.5V, 0.25um, high speed / low power CMOS process
  - PC98/99 compatible using VIA VT82C686A (352-pin BGA) south bridge chip for Desktop and Mobile applications

- 66 / 100 / 133MHz CPU Front Side Bus (FSB) Operation
- High Integration
  - Single chip implementation for 64-bit Slot-1 and Socket-370 CPUs, 64-bit system memory, 32-bit PCI with integrated 2D / 3D GUI accelerator
  - Apollo ProMedia Chipset: VT8601 system controller and VT82C686A PCI to ISA bridge
  - Chipset includes dual UltraDMA-33/66 EIDE, AC-97 link, 4 USB ports, integrated Super-I/O, hardware monitoring, keyboard/mouse interfaces, and RTC/CMOS
- High Performance CPU Interface
  - Supports Slot-1 Intel Pentium II / Pentium III and Socket 370 Celeron processors
  - 66 / 100 / 133 MHz CPU Front Side Bus (FSB)
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Five outstanding transactions (four In-Order Queue (IOQ) plus one input latch)
  - Supports WC (Write Combining) cycles
  - Dynamic deferred transaction support
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism
- Internal Accelerated Graphics Port (AGP) Controller
  - AGP v1.0 compliant
  - Pipelined split-transaction long-burst transfers up to 533 MB/sec
  - Eight level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (128 bytes)
  - Sixteen level (quadwords) write data FIFO (64 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
  - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support
- Concurrent PCI Bus Controller
  - PCI Bus is synchronous / pseudo-synchronous to host CPU bus
  - 33 MHz operation on the primary PCI bus
  - Supports up to five PCI masters
  - Concurrent multiple PCI master transactions
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132MB/sec
  - Six levels (double-words) of CPU to PCI posted write buffers
  - Enhanced PCI command optimization
  - Delay transaction from PCI master reading DRAM
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs
- Advanced High Performance DRAM Controller
  - DRAM interface synchronous or pseudo-synchronous with CPU FSB speed of 66 / 100 / 133 MHz
  - Concurrent CPU, AGP, and PCI access
  - Supports FP, EDO, SDRAM and VCM-SDRAM memory types
  - 64-bit data width only
  - 3.3V DRAM interface with 5V-tolerant inputs
- General Graphics Capabilities
  - 64-bit Single Cycle 2D/3D Graphics Engine

- Supports 2 to 8 MB of Frame Buffer
- Real Time DVD MPEG-2 and AC-3 Playback
- Video Processor
- I^2C Serial Interface
- Integrated 24-bit 230MHz True Color DAC
- Extended Screen Resolutions up to 1600x1200
- Extended Text Modes 80 or 132 columns by 25/30/43/60 rows
- DirectX 6 and OpenGL ICD API
- Graphics Performance
  - Sustained 1M polygon/second and 100M pixel/second
  - 30fps DVD playback of 9.8Mbps MPEG-2 video with 30% headroom
  - Host Based AC-3 decode at only 8% utilization
- High Performance rCAD3D Accelerator
  - 32-entry command queue, 32 entry data queue
  - 4Kbyte texture cache with over 90% hit rates
  - Pipelined Single Cycle Setup/Texturing/Rendering Engines
  - DirectDraw acceleration
  - Multiple buffering and page flipping
- DVD
  - Hardware Assisted MPEG-2 Architecture for DVD with AC-3
  - Simultaneous motion compensation and front-end processing
  - Supports full DVD 1.0, VCD 2.0 and CD-Karaoke
  - Microsoft DirectShow 3.0 native support, backward compatible with MCI
  - No additional frame buffer requirements
- Video Processor
  - On-chip Color Space Converter (CSC)
  - Dual frame buffer apertures for independent memory access for graphics and video
  - Horizontal/vertical interpolation with edge recovery
  - Video Module Interface (VMI) to MPEG and video decoder
  - Overlay differing video and graphic color depths
  - Display two simultaneous video streams from both internal AGP and VMI
- Flat Panel Interfaces
  - 85MHz Flat Panel interface supports 1024x768 panels
  - Support TFT, STN & DSTN panel technologies
  - Allows external LVDS or TMDS transmitter for advanced panel interfaces
- Power Management Support
  - Dynamic power down of SDRAM (CKE)
  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - Suspend-to-DRAM and Self-Refresh operation
  - EDO self-refresh and SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- Testability
  - Build-in NAND-tree pin scan test capability

Hardware Functional Overview

4.5.2   VT82C686A Features

The VT82C686A PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high-integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI/ISA system.

The VT82C686A functions and capabilities include:

- Inter-operable with VIA and other Host-to-PCI Bridges
  - Combine with VT8601 for a complete 66 / 100 / 133 MHz Socket 370 or Slot-1 system with integrated 2D / 3D graphics (Apollo ProMedia)
  - Inter-operable with Intel or other Host-to-PCI bridges for a complete PC99 compliant PCI / AGP / ISA system
- PCI to ISA Bridge
  - Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated USB Controller with root hub and four function ports
  - Integrated UltraDMA-33/66 master mode EIDE controller with enhanced PCI bus commands
  - PCI-2.2 compliant with delay transaction and remote power management
  - Distributed DMA support for ISA legacy DMA across the PCI bus
  - Fast reset and Gate A20 operation
  - Flash EPROM, 4Mb EPROM and combined BIOS support
  - Supports positive and subtractive decoding
- UltraDMA-33 / 66 Master Mode PCI EIDE Controller
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
  - Support ATAPI compliant devices including DVD devices
  - Support PC native and ATA compatibility modes
  - Complete software driver support
- Integrated Super IO Controller
  - Supports 2 serial ports, IR port, parallel port, and floppy disk controller functions
  - Two UARTs for Complete Serial Ports
  - Infrared-IrDA (HPSIR) and ASK (Amplitude Shift Keyed) IR port multiplexed on COM2
  - Multi-mode parallel port
  - Floppy Disk Controller
- SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller
  - Dual full-duplex Direct Sound channels between system memory and AC97 link
  - PCI master interface with scatter / gather and bursting capability
  - 32 byte FIFO of each direct sound channel
  - Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors
  - Loopback capability for re-directing mixed audio streams into USB and 1394 speakers
  - Hardware SoundBlaster Pro for Windows DOS box and real-mode DOS legacy compatibility

- Hardware assisted FM synthesis for legacy compatibility
- Direct two game ports and one MIDI port interface
- Complete software driver support for Windows-95/98/2000 and Windows NT
- Voltage, Temperature, Fan Speed Monitor and Controller
  - Five positive voltage (one internal), three temperature (one internal) and two fan-speed monitoring
  - Programmable control, status, monitor and alarm for flexible desktop management
  - Automatic clock throttling with integrated temperature sensing
  - Internal core VCC voltage sensing
  - Flexible external voltage sensing arrangement (any positive supply and battery)
- Universal Serial Bus Controller
  - USB v1.1 and Intel Universal HCI v1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Root hub and four function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- System Management Bus Interface
  - Host interface for processor communications
  - Slave interface for external SMBus masters
- Sophisticated PC99-Compatible Mobile Power Management
  - Supports both ACPI and legacy APM power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enabled (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types
  - Multiple suspend power plane controls and suspend status indicators
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - Up to 12 general purpose input ports and 23 output ports
  - One programmable chip select and one microcontroller chip select
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm on either external or any combination of three internal temperature sensing circuits
  - Hot docking support
  - I/O pad leakage control
- Plug and Play Controller
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, audio, soundblaster, MIDI
  - Steerable DMA channels for integrated floppy, parallel, and soundblaster pro controllers
  - One additional steerable interrupt channel for on-board plug and play devices

- Microsoft Windows 98, Windows NT, Windows 95 and plug and play BIOS compliant
- Integrated I/O APIC (Advanced Peripheral Interrupt Controller) (CG Silicon)
- Built-in NAND-tree pin scan test capability
- 0.35um, 3.3V, low power CMOS process
- Single chip 27x27 mm, 352 pin BGA

4.6 Clock Frequency Generator

The notebook utilizes the ICWORK chip to supply the system clock needed to run the computer. The following are the available clock frequencies:

- System clock:
  - Clock generator support:
    - 66/100 MHz for Pentium IIII Mobile CPU
  - 30/33 MHz for PCI device bus clock use
  - 48 MHz for VT82C686A
  - 14.318 MHz for VT82C686A refresh use
- 14.318 MHz XTAL for ICWORK use
- 32.768 KHz XTAL for RTC real time clock
- 8.0 MHz XTAL for K/B controller use
- 14.318 MHz OSC for sound blaster use

4.7 Cache Memory

The primary (L1) and secondary (L2) level cache are integrated on the CPU. By incorporating the cache on-die (meaning it is combined with the CPU into one component), Intel eliminates the need for separate components. The 256KB on-die L2 cache provides three (3X) times faster processor access, resulting in significant improvements in performance. Likewise, an integrated cache means a reduction of connections resulting in increased reliability.

4.8 System Memory

The memory subsystem, implemented on the motherboard, includes System and Video memory. The VIA VT8601 System Controller chip provides primary control for the system memory.

4.8.1 System Memory

The notebook offers two (2) 64-bit SODIMM (Small Outline Dual Inline Memory Module) sockets for main memory configuration. The memory sockets accept any standard 144-pin SODIMM modules at 16MB, 32MB, 64MB, and 128MB sizes. Memory modules are 3.3V SDRAM type.

4.8.2 Video Memory

The video memory (frame buffer) of the notebook is shared from the system main memory using Shared Memory Architecture (SMA) design of the integrated VGA controller. The frame buffer size can be set to either 4MB or 8MB from the CMOS Setup program. With 4MB, the notebook can support display resolutions of up to 1024x768 at 16M color (TFT LCD). The default frame buffer size is 8MB.

4.9   System BIOS

The notebook utilizes the Phoenix BIOS 4.0 Release 6.0 (Basic I/O System) that contains both the main system BIOS and the VGA BIOS with Shadow BIOS capability. It utilizes Flash EPROM BIOS that allows instant erasing and programming without replacing the EPROM chip.

The BIOS is stored in a 32-pin PLCC package FLASH ROM 29EE020 120ns with 4Mbit size and is mounted into the motherboard. While posting the system, the Shadow RAM will be enabled and the ROM will be disabled.

4.10   Video Subsystem

The video subsystem, integrated inside the North Bridge chip and the LCD panel, controls the display output to both the LCD Panel screen and to the external VGA port.

4.10.1 Video Chip Controller

The video subsystem utilizes the Trident CyberBladei1 VGA controller integrated inside the North Bridge chip. CyberBladei1's notebook graphics controller core incorporates high performance 2D and 3D graphics engine, video accelerator, DVD playback, video capture and TV output capabilities. It also eliminates the need for an external frame buffer by taking advantage of the Shared Memory Architecture (SMA). For more information of the VGA function, refer to the System Core Logic section of this chapter.

4.10.2 Video Clock

ICWORK provides 14.318 MHz input to generate VGA internal slate machine, MCLK, and DCLK. The VT82C686A chip also provides 32.768 KHz O/P for video RAM refresh.

4.11   I/O Subsystem

The I/O (Input/Output) Subsystem of the notebook is integrated inside the South Bridge chip VT82C686A on the motherboard. Refer to the System Core Logic section of this chapter.

4.12   PCMCIA Controller

The PCMCIA controller of the notebook is implemented on the motherboard using the TI PCI1225 PC Card Controller. The TI PCI1225 is a high-performance PCI-to-PC Card controller that supports two independent card sockets compliant with the 1997 PC Card Standard. The PCI1225 provides a rich features set that makes it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1997 PC Card Standard retains the 16-bit PC Card specification defined in PCMCIA Release 2.2 and defines the new 32-bit PC Card (CardBus), capable of full 32-bit data transfers at 33MHz. The PCI-1225 supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5V or 3.3V, as required.

Feature Summary of the PCI1225:

- PCI Bus Power Management Interface Specification 1.0 Compliant
- ACPI 1.0 Compliant
- Packaged in 208-pin low-profile QFP (PDV) or GHK High Density BGA
- PCI Local Bus Specification Revision 2.2 Compliant

- 1997 PC Card Standard Compliant
- PC99 Compliant
- 3.3V Core Logic with Universal PCI Interfaces Compatible with 3.3V and 5V PCI Signaling Environments
- Mix and Match 5V/3.3V 16-bit PC Cards and 3.3V CardBus Cards
- Supports Two PC Card or CardBus Slots with hot insertion and removal
- Uses serial interface to TI TPS2202/2206 Dual-Slot PC Card Power Switch
- Supports Burst Transfers to Maximize Data Throughput on the PCI Bus and CardBus Bus
- Supports Parallel PCI Interrupts, Parallel ISA IRQ and Parallel PCI Interrupts, Serial ISA IRQ with Parallel PCI Interrupts, and Serial ISA IRQ and PCI Interrupts
- Serial EEPROM Interface for Loading Subsystem ID and Subsystem Vendor ID
- Pipelined Architecture allows greater than 130-MBps throughput from CardBus-to-PCI and from PCI-to-CardBus
- Supports up to Five General-Purpose I/Os
- Programmable Output Select for CLKRUN
- Multifunction PCI Device with separate configuration space for each socket
- Five PCI Memory Windows and Two I/O Windows available for each R2 socket
- Two I/O Windows and Two Memory Windows available to each CardBus socket
- Exchange Card Architecture (ExCA) Compatible Registers are mapped in memory and I/O Space
- Intel 82365Sl-DF Register Compatible
- Supports Distributed DMA (DDMA) and PC/PCI DMA
- Supports 16-bit DMA on both PC Card sockets
- Supports Ring Indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN
- LED Activity Pins
- Supports PCI Bus Lock (LOCK)
- Advanced Submicron, Low-Power CMOS Technology

4.13 Audio Subsystem

The audio subsystem is integrated inside the South Bridge chip on the motherboard. Refer to the System Core Logic section of this chapter.

An internal two-way mini speaker and microphone provide the notebook with mobile sound generation and recording capabilities. In addition, a set of 3.5mm bayonet socket (1/8" minijack) connectors allow for external microphone, line inputs, and headphone outputs.

4.14 Keyboard and Pointing Device

The Keyboard Subsystem of the notebook is implemented on the Motherboard and Keyboard Assembly using the Mitsubishi 38867M8 keyboard controller chip and the Phoenix MultiKey/M3886L keyboard controller firmware. This chip controls the internal built-in keyboard, the built-in touchpad pointing device, as well as the external PS/2 keyboard and mouse port. The keyboard controller allows simultaneous use of both the internal and external keyboard and PS/2 mouse.

The A440 Series membrane keyboard is an 86-key IBM 101-key enhanced compatible keyboard with standard characters and 12 function keys including an embedded numeric keypad. See Chapter 1 for more information.

The pointing device subsystem consists of the built-in ALPS Touchpad pointing device

module on the system top cover assembly and a pre-programmed Mitsubishi 38867M8 micro-controller that interfaces the mouse device to the Motherboard. The touchpad module is connected to audio board through a 6-pin FPC cable. An external PS/2 port also supports the use of an external PS/2 compatible mouse where the system automatically detects on system power up and runs both internal and external mouse simultaneously.

The ALPS Touchpad, a pointing device for personal computers, detects the position of a finger over a touch-sensitive area. To move the cursor, the user lightly slides a finger over the smooth sensor area. To 'click', the user gently taps on the surface.

The ultra-thin module is the thinnest PCB based touchpad available today. It is a capacitive sensor - the finger is detected by measuring its effect on an array of capacitive lines integrated into the PC board. The pad senses both the finger's position and its contact area (X, Y, and Z). The area of contact is a measure of applied pressure. One side of the module PC board is the sensor surface; electronic components are mounted on the other side. The sensitive area is protected by a layer of smooth and durable mylar.

The ALPS touchpad communicates with the host via a standard PS/2 mouse or trackball interface. It is fully compatible with the standard Microsoft mouse driver. The module connector includes the PS/2 signal pins, power supply pins and two connections for external button switches.

The ALPS Touchpad includes a special "edge-motion" feature that allows the user to extend a drag operation when the finger reaches the edge of the sensor pad. The cursor continues to coast in the indicated direction when the finger is held against the edge.

4.15 Disk Drives Subsystem

The disk drives subsystem, implemented on the Motherboard and on the associated internal hard disk drive assembly and device bay, provides disk storage for all system software and user files.

The notebook is equipped with high capacity hard disk drive ranging from 6.0GB to 18GB using Enhanced IDE controller with LBA (Logical Block Addressing) and Ultra DMA mode support.

The VT82C686A controller chip provides the Primary IDE controller for the internal hard disk, and the Secondary Master for the CD-ROM.

The floppy disk drive supports standard 3.5-inch 720KB and 1.44MB mini-diskettes while adding support for 1.2MB (Mode 3) mini-diskettes for Japanese market.

The notebook uses the TEAC 24X-speed IDE CD-ROM Drive that reads digital data stored on CD-ROM at 24 times faster rotational speed. The CD-ROM drive supports CD-DA transfer over ATAPI function that the host system can read CD audio data. The drive also supports Photo-CD Multi-session disc compatibility and Multimedia PC-3 specification compatibility.

4.16 Power Subsystem

The Power Subsystem consists of the following major sections:

4.16.1 AC Power Adapter

The computer is equipped with a 50W universal AC power adapter that converts AC voltage (100 to 240VAC, 47 to 63Hz) into DC voltage used to operate the notebook and charge the batteries.

4.16.2 Internal Battery Pack

The computer utilizes Nickel Metal Hydride (NiMH) or Lithium-Ion (Li-Ion) that provides DC power for the notebook and real time clock battery on the motherboard when the AC Adapter is not connected to the computer.

The normal charging time for the Li-Ion battery is around 2.5 hours when computer is turn off while it should take around 8 hours when the computer is running. Running time of battery is around 2 to 2.5 hours.

4.16.3 DC-DC Module of Motherboard

The DC-DC module receives approximately 12VDC from the battery pack and uses this input voltage to generate multiple regulated output voltages to provide power for all internal notebook board assemblies.

4.16.4 LCD Inverter Board Assembly

The LCD Inverter Board Assembly is located in the LCD Panel Assembly. It converts the +12VDC input directly from the Battery Pack into a high voltage AC output used to light the CCFT (Cold-Cathode Fluorescent Tube).

4.17 Micro-P Subsystem (PIC-16C62A)

The micro controller PIC16C62A acts as a supplement for the power management control. It supports many functions via the SMBus interface.

The system communicates with the PIC16C62A via the SMBus interface. The SMBus host (M38867) should be first initialized before starting the transaction. The following is the procedure for system communication with PIC16C62A:

1. Enable SMBus interface by writing 01h to SmbHstCfg register.
2. Get SMBus I/O port base address by reading from SmbBA register.
3. Clear SMBus status by writing 1Eh to SmbHstSts register.
4. Write the PIC16C62A slave address to SmbHstAdd register.
   − Send command to PIC16C62A -- Slave address is 04h.
   − Read data from PIC16C62A -- Slave address is 05h.
5. Write the desired command to SmbHstCmd register.
6. Write the desired parameters to SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to send command to PIC16C62A.
7. Wait for SMBus interrupt occurred by monitoring SmbHstSts register INTR bit.
8. Get the desired data by reading from SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to read data from PIC16C62A.

Features Summary of the Micro-P:

- 5 channels 8-bit analog to digital converter
- Timer0: 8-bit tuner/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module
- Synchronous Serial port (SSP) with SPI and I^2C
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Brown-out detection circuitry for Brown-out Reset (BOR)
- 2K bytes program memory
- 128 bytes data memory
- 22 I/O pin
- 8 interrupt sources