Chapter 3

Software Functional Overview

3.1 Overview

The A440 is an IBM PC/AT compatible Notebook PC that supports the Socket 370 Intel Mobile Pentium III or Celeron processor family. The following are the major features that A440 supports:

- Microsoft PC99 and ACPI logo approval
- Offer 800x600 SVGA display with 12.1" LCD panel
- Offer 1024x768 XGA display with 13.3"/14.1" LCD panel
- Support ACPI 1.0 (or above)
- Support PCI 2.1 (or above)
- Support AGP 2.0
- Support SMBIOS 2.1 (or above)
- Support 100MHz CPU front side bus
- Support a proprietary Port Replicator

3.2 Summary of the BIOS Specification

Below is the summary of the BIOS software specification:

Controller Chip	Description
BIOS Feature	▪ Boot Block / Crisis Rescue ▪ APM 1.2 Compliance ▪ Support PCI 2.1 (or above) Spec ▪ Support Windows 95, Windows NT4.0, Windows 98, and Windows 2000 ▪ Support Flash function for new BIOS update ▪ Support 3-Mode FDD ▪ Support ACPI 1.0 (or above) Spec ▪ Support SMBIOS 2.1 (or above) Spec ▪ Support AGP 2.0 ▪ Support boot from FDD, HDD and CDROM Drive ▪ Support maximum 4 different keyboards on same BIOS
CPU	Auto detect the CPU type and speed for the Socket 370 or Slot 1 based system
DRAM	▪ Auto sizing and detection ▪ Support PC-100 SDRAM
Cache	▪ Level 2 SRAM auto sizing and detection ▪ Always enable CPU L1 and L2 cache
Shadow	Always enable VGA and System BIOS shadow
Display	▪ System auto detects LCD or CRT presence on boot and lid closed ▪ Support Panning while LCD in a display resolution greater than supported ▪ Support Microsoft Direct 3D

Controller Chip	Description
Hard Disk	▪ Enhanced IDE spec ▪ Support auto IDE detection ▪ Support LBA mode for larger capacity HDD ▪ Support Ultra DMA 33 ▪ Support Fast PIO mode 1-4 transfer ▪ Support 32-bit PIO transfer ▪ Support Multi-Sector transfer
Multi Boot	Allow the user to select boot from FDD, LS120, HDD and CD-ROM
Plug and Play	Support PnP Run Time Service and conflict-free allocation of resource during POST
Smart Battery	Support BIOS interface to pass battery information to the application via SMBus
Keyboard Controller	Support Fn hot keys, one Win95 hot keys, built-in Glide Pad and external PS/2 mouse/keyboard
PCMCIA	Compliant with PCMCIA 2.1 specification
Port Replicator	I/O port replicator duplicates the following ports ▪ Video port ▪ Printer port ▪ COM1 port ▪ PS/2 Mouse & Standard Keyboard port ▪ USB Port ▪ DC In Jack
Power Management Support (APM Mode)	The power management is compliant with APM 1.2 specification and supports the following power state: ▪ Full-On Mode ▪ Doze Mode (This mode is transparent to user) ▪ Stand-By (POS) Mode ▪ Suspend to RAM (STR) Mode ▪ Suspend to Disk (STD) Mode ▪ Soft-Off Mode (SOff)
Power Management Support (ACPI Mode)	The power management is compliant with ACPI 1.0 specification and supports the following power state: ▪ S0 (Full-On) Mode ▪ S3 (STR) Mode ▪ S4 (STD) Mode ▪ S5 (Soft-Off) Mode

3.3 Subsystem Software Functions

This section provides introduction on the software functions of the notebook subsystems and BIOS related function.

3.3.1 Key Chipset Summary

Following are the main chipsets used in the notebook:

Controller Chip	Vendor	Description
Processor	Intel	Socket 370 Pentium III at 650 – 850MHz Socket 370 Celeron at 500 – 667MHz
Core Logic	VIA	ProMedia VT8601 (North Bridge) ProMedia VT82C686A (South Bridge)
Video Controller	Trident	Trident 8400 (Integrated in North Bridge)
PCMCIA Controller	TI	TI-1225 CardBus
Supper I/O Controller	VIA	(Integrated in South Bridge)
Audio Codec	WM	WM9701A (AC97 1.03) / WM9703 (AC97 2.1)
Audio Amplifier	TI	TDA0102
Keyboard Controller	Mitsubishi	M38867
PMU Controller	MicroChip	PIC16C62B (SSOP)
ROM BIOS	Winbond	W29C040P, Boot Block Structure
Clock Generator	IC Work	W156
Temperature Sensor	VIA	(embedded in South Bridge chip)
LVDS		THC63LVDM63A
LAN	Intel	82559 (10/100Mbs Fast Ethernet)
Modem	Lucent	Mars3 (PCI Bus S/W Modem)

3.3.2 System Memory

The system memory consists of PC100 SDRAM memory on 64-bit bus and the module size options are 16/32/64/128MB. PC100 SDRAM synchronizes itself with the CPU bus speed so if the CPU is set at 100MHz-bus speed, the memory speed is also running at 100MHz. The BIOS will automatically detect the amount of memory in the system and configure CMOS accordingly during the POST (Power-On Self Test) process. This is done in a way that requires no user interaction.

DRAM Combination Configuration:

Slot #1	Slot #2	Total Size
32MB	NIL	32MB
32MB	32MB	64MB
32MB	64MB	96MB
32MB	128MB	160MB
64MB	NIL	64MB
64MB	32MB	96MB
64MB	64MB	128MB
64MB	128MB	192MB
128MB	NIL	128MB

Slot #1	Slot #2	Total Size
128MB	32MB	160MB
128MB	64MB	192MB
128MB	128MB	256MB
NIL	32MB	32MB
NIL	64MB	64MB
NIL	128MB	128MB

3.3.3 Video

The Video subsystem uses 4 or 8MB of "Shared Memory" from the System Main Memory. The system supports true ZV port, Microsoft Direct 3D, simultaneous display, monitor sense for auto display on boot and VESA Super VGA function call.

Supported Video Mode

The following is all the display modes supported by the Trident 8400 in LCD only, CRT only, and simultaneous mode. The VGA BIOS will allow mode sets of resolutions greater than the panel size but only show as much mode display as will fit on the panel.

Supported standard VGA modes:

Mode	Pixel Resolution	Colors	Dot Clock	Horizontal Freq.	Vertical Freq.
0, 1	320*400	16	27.175 MHz	31.5 KHz	70 Hz
0*, 1*	320*350	16	25.175 MHz	21.85 KHz	60 Hz
0+, 1+	360*400	16	28.322 MHz	31.5 KHz	70 Hz
2, 3	640*200	16	25.175 MHz	31.5 KHz	70 Hz
2*, 3*	640*350	16	25.175 MHz	21.85 KHz	60 Hz
2+, 3+	720*400	16	28.322 MHz	31.5 KHz	70 Hz
4, 5	320*200	4	25.175 MHz	31.5 KHz	70 Hz
6	640*200	2	25.175 MHz	31.5 KHz	70 Hz
7	720*400	Mono	28.322 MHz	31.5 KHz	70 Hz
D	320*200	16	25.175 MHz	31.5 KHz	70 Hz
E	640*200	16	25.175 MHz	31.5 KHz	70 Hz
F	640*350	Mono	25.175 MHz	31.5 KHz	70 Hz
10	640*350	16	25.175 MHz	31.5 KHz	70 Hz
11	640*480	2	25.175 MHz	31.5 KHz	60 Hz
12	640*480	16	25.175 MHz	31.5 KHz	60 Hz
13	320*200	256	25.175 MHz	31.5 KHz	70 Hz

"*" - Needs to be assign numbers of scan line before setting VGA mode.

"+" - Means default mode.

Supported extended video modes:

VESA Mode	Pixel Resolution	Colors	Dot Clock	Horizontal Freq.	Vertical Freq.
100	640*400	256	25.175 MHz	31.5 KHz	70 Hz
101	640*480	256	25.175 MHz	31.5 KHz	60 Hz
			31.5 MHz	37.5 KHz	75 Hz
			36.0 MHz	43.3 KHz	85 Hz
103	800*600	256	40.0 MHz	37.8 KHz	60 Hz
			49.5 MHz	46.9 KHz	75 Hz
			56.25 MHz	53.7 KHz	85 Hz
105	1024*768	256	65.0 MHz	48.3 KHz	60 Hz
			75.359 MHz	56.746 KHz	75 Hz
			78.75 MHz	60.0 KHz	85 Hz
10D	320*200	32K	25.175 MHz	31.5 KHz	70 Hz
10E	320*200	64K	25.175 MHz	31.5 KHz	70 Hz
110	640*480	32K	25.175 MHz	31.5 KHz	60 Hz
			31.5 MHz	37.5 KHz	75 Hz
			36.0 MHz	43.3 KHz	85 Hz
111	640*480	64K	25.175 MHz	31.5 KHz	60 Hz
			31.5 MHz	37.5 KHz	75 Hz
			36.0 MHz	43.3 KHz	85 Hz
112	640*480	16M	25.175 MHz	31.5 KHz	60 Hz
			31.5 MHz	37.5 KHz	75 Hz
			36.0 MHz	43.3 KHz	85 Hz
113	800*600	32K	40.0 MHz	37.8 KHz	60 Hz
			49.5 MHz	46.9 KHz	75 Hz
			56.25 MHz	53.7 KHz	85 Hz
114	800*600	64K	40.0 MHz	37.8 KHz	60 Hz
			49.5 MHz	46.9 KHz	75 Hz
			56.25 MHz	53.7 KHz	85 Hz
115	800*600	16M	40.0 MHz	37.8 KHz	60 Hz
			49.5 MHz	46.9 KHz	75 Hz
			56.25 MHz	53.7 KHz	85 Hz
116	1024*768	32K	65.0 MHz	48.3 KHz	60 Hz
			75.359 MHz	56.746 KHz	75 Hz
			78.75 MHz	60.0 KHz	85 Hz
117	1024*768	64K	65.0 MHz	48.3 KHz	60 Hz
			75.359 MHz	56.746 KHz	75 Hz
			78.75 MHz	60.0 KHz	85 Hz
120	320*240	256	25.212 MHz	31.5 KHz	60 Hz
121	320*240	64K	25.212 MHz	31.5 KHz	60 Hz
122	400*300	256	40.091 MHz	37.965 KHz	60 Hz
123	400*300	64K	40.091 MHz	37.965 KHz	60 Hz
124	512*384	256	65.028 MHz	48.384 KHz	60 Hz
125	512*384	64K	65.028 MHz	48.384 KHz	60 Hz

Panel Type Initialization

The VGA BIOS will issue an INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPI pins before the VGA chip initializes, and pass this information to VGA BIOS through INT 15 Function 5F00h.

LCD Panel ID pin Definition:

GPI Pins			Panel Type
GPI [18]	GPI [10]	GPI [9]	
0	0	0	Reserved
0	0	1	Type 5
0	1	0	Reserved
0	1	1	Type 2
1	0	0	Type 3
1	0	1	Type 4
1	1	0	Type 1
1	1	1	Type 0

Supported LCD panel: Panel Type	Display Size	Panel Description
Type 0	1024*768	14.1” TFT LG
Type 1	1024*768	14.1” TFT Hitachi
Type 2	1024*768	13.1” TFT Acer
Type 3	800*600	12.1” TFT Sanyo
Type 4	1024*768	14.1” TFT CPT
Type 5	800*600	12.1” DSTN Panasonic

3.3.4 Enhanced IDE

The system BIOS can support 4 IDE devices on two controllers up to 12GB in capacity. The BIOS supports Ultra DMA 33 and automatic configuration of drives using both the LBA and CHS large drive re-mapping method. In addition to supporting standard drives through an auto-configuration process that does NOT require user involvement or confirmation. The system should automatically do this at POST time in a way that is transparent to the user. If a drive is connected to the bus, the drive should be automatically recognized, configured and available for use under MS-DOS.

Ultra DMA

Ultra DMA/33 is a new physical protocol used to transfer data between an Ultra DMA/33 capable IDE controller and one or more Ultra DMA/33 capable IDE devices. It utilizes the standard Bus Master IDE functionality and interface to initiate and control the transfer. Ultra DMA/33 utilizes a “source-synchronous” signaling protocol to transfer data at rates up to 33 Mbytes/sec.

3.3.5 Audio

The audio subsystem will support the requirements identified by the AC’97 specification.

Both software and hardware will control the volume level for the internal audio subsystem. In addition to the volume control, the user will be able to mute the sound to completely cut off the volume using both software and hardware.

3.3.6 Super I/O

The Super I/O controller is embedded inside the VIA VT82C686A South Bridge chip. This controller contains 16550A or FIFO Enabled UART, ECP/Standard/Bi-directional Parallel Port meeting the 1284 specification.

3.3.7 PCMCIA

The PCMCIA controller chip of the notebook provides the following features:

- PCI Power Management Compliant
- ACPI 1.0 Compliant
- Supports Two PC Card or CardBus Slots with Hot Insertion and Removal
- Supports Serialized IRQ with PCI Interrupts
- System Interrupts can be Programmed as PCI-style or ISA IRQ-style
- Supports Zoom Video with internal Dual-Buffering (Top Slot)
- Support for 3.3v, 5v and 12v (flash programming) cards.

3.3.8 LED Indicator

The table below lists down the functions of the Status LED indicator:

Indicator	Function Description
IDE accessing LED❶	This LED will turn on while accessing the IDE Device.
FDD accessing LED❶	This LED will turn on while accessing the FDD Device.
Battery Charging LED	Turn on (Green) – Battery is under charging mode Turn off – Battery full charged or no battery
Caps Lock LED❶	This LED will turn on when the function of Caps Lock is active.
Scroll Lock LED❶	This LED will turn on when the function of Scroll Lock is active.
Num Lock LED❶	This LED will turn on when the function of Num Lock is active.
Power Status LED	Green – System is powered on. Green Blinking- System is entered suspend mode. Amber – Battery Low.

❶ - LED will be turned off during Suspend mode.

3.3.9 Hot Keys Definition

All Hot keys must be active at all times under all operation systems.

Hot Keys by Internal Keyboard

Hot Key	Function	Handler
Fn + F3	Toggle Display (LCD/CRT/Simul)	BIOS Handler
Fn + F4	Standby (STR)	BIOS Handler
Fn + F5	Display Stretch	BIOS Handler
Fn + F6	System Speaker On/Off	BIOS Handler
Fn + F8	Brightness Increase	Controlled by M38867
Fn + F9	Brightness Decrease	Controlled by M38867
Fn + F10	Contrast Increase	Controlled by M38867
Fn + F11	Contrast Decrease	Controlled by M38867
Fn + Power Button	Save to Disk	BIOS Handler
Internet Button	Internet Explorer Browser function	Controlled by Driver
Email Button	Internet email function	Controlled by Driver

ⓘ The system will issue a beep to inform user when Fn + F4 and Fn + Power Button hot-keys are pressed.

ⓘ The scale parameters of the brightness and contrast will be saved in CMOS before SoftOff.

Hot Keys by External Keyboard

The following hot keys should be accessible via an external keyboard:

External Keyboard	Function	Handler
Ctrl + Alt + F3	Toggle Display (LCD/CRT/Simul)	BIOS Handler
Ctrl + Alt + F4	Standby (STR)	BIOS Handler
Ctrl + Alt + F5	Display Stretch	BIOS Handler
Ctrl + Alt + F6	System Speaker On/Off	BIOS Handler

3.3.10 Port Replicator (Docking Station)

The Port Bar duplicates the following ports from the notebook:

- VGA port
- Serial port
- Printer port
- PS/2 port For Keyboard
- PS/2 port For Mouse
- USB Port
- DC In Jack

3.3.11 Plug & Play

The BIOS supports the Plug and Play Specification 1.0A. This section describes the device management.

The system board devices and its resources are as follows:

Device	Connect Type	Resources			
		I/O	IRQ	DMA	Memory
DMA Controller	Static	00~0F, 81~8F	-	4	-
Interrupt Controller	Static	20~21, A0~A1	2	-	-
System Timer	Static	40~43	0	-	-
RTC	Static	70~71	8	-	-
ISA Bus	Static	-	-	-	-
System Speaker	Static	61	-	-	-
System Board	Static	-	-	-	E0000~FFFFF
PnP Mother Board	Static	80	-	-	-
Keyboard Controller	Static	60, 64	1	-	-
Math Coprocessor	Static	F0~FF	13	-	-
PS/2 Mouse	Enable / Disable	-	12	-	-
Video Controller	Static	3B0~3BB, 3C0~3DF	5	-	A0000~BFFFF, C0000~C9FFF, FE800000~FEBFFFFF
Serial Port	Static	3F8~3FF	4	-	-
ECP, Parallel port	Static	378~37F, 778~77F	7	1	-
FDC	Static	3F0~3F5, 3F7	6	2	-
Dual IDE Controller	Static	170~177, 1F0~1F7, 3F6	14, 15	-	-
CardBus Controller	Static	3E0~3E1	10	-	08000000~08001FFF
FAX/Modem	Static	1050~1057, 1400~14FF	5	-	64000000~640000FF
LAN	Static	1080~10FF	5	-	08003000~080033FF
SIR	Static	2F8-2FF, 108~10F	3	0	-
USB Host Controller	Static	EF80~EF9F	5	-	-
Audio Controller	Static		5		

3.3.12 PCI Device

The table below summarizes the IDSEL Pin Allocation:

IDSEL Pin	PCI Device		
	Device Number	Function Number	Device Name
AD11	Device 00	Function 0	VT8601 Host to PCI bridge.
AD12	Device 01	Function 0	VT8601 PCI to PCI bridge.
AD17	Device 06	Function 0	MODEM / LAN
		Function 0	VT82C686A – PCI to ISA bridge
		Function 1	VT82C686A – IDE interface
		Function 2	VT82C686A – USB Port 0-1 Interface
AD18	Device 07	Function 3	VT82C686A – USB Port 2-3 Interface.
		Function 4	VT82C686A – PMU and SMBus interface
		Function 5	VT82C686A – AC97 Audio Interface.
		Function 6	VT82C686A – AC97 Modem Interface.
AD21	Device 0A	Function 0	Card Bus Socket A
		Function 1	Card Bus Socket B

The table below summarizes the INT Pin Allocation:

INT Pin	PCI Device
INTA	CardBus
INTB	LAN/Modem
INTC	VGA/Audio
INTD	USB

The table below summarizes the PCI bus master Allocation:

REQ# Pin	PCI Device
REQ 0	CardBus
REQ 1	VGA
REQ 2	Audio
REQ 3	LAN/Modem

3.3.13 SMBus Devices

The SMBus is a two-wire interface through which the system can communicate with power-related chips. The BIOS should initialize the SMBus devices during POST.

SMBus Device	Host/Slave	Address	BIOS Need to Initialize
VIA VT82C686A	Both Host and Slave	10h	Enable SMBus interface and SMBus interrupt
PIC16C62 – Micro P	Both Host and Slave	04h	No need
IMISC671 – Clock Synthesizer	Slave	D2h	Program the desired clock frequency (Pin23 output 24MHz, Pin22 output 48MHz)
BQ 2040 – Smart Battery	Both Host and Slave	16h	No need

3.3.14 Resource Allocation

This section summarizes the resource allocation of the notebook computer.

I/O Map

Hex Address	Device
000 – 01F	8237-1
020 – 021	8259-1
022	VIA VT82C686A
040 – 05F	8254
060 – 06F	Keyboard Controller
070 – 07F	RTC & NMI Mask
080 – 08F	DMA Page Registers
092	System Control Port
0A0 – 0A1	8259-2
0C0 – 0DF	8237-2
0F0 – 0FF	Math Coprocessor
170 – 177	Secondary IDE Controller
1F0 – 1F7	Primary IDE Controller
200 – 20F	Game Port
220 – 22F	Sound Blaster
279	PnP configuration – Address port
2F8 – 2FF	FIR
330 – 333	MIDI
370 – 371	Sound chip control port
378 – 37A	Parallel Port
388 – 38B	FM Synthesizer
398 – 399	Super I/O Chip
3B0 – 3DF	Video Controller
3E0 – 3E1	PCMCIA Controller
3E8 – 3EF	Fax/Modem

Hex Address	Device
3F0 – 3F7	Floppy Disk Controller
3F8 – 3FF	Serial Port 1
530 – 537	Windows Sound System
778 – 77B	ECP port
A79	PnP configuration – Write data port
CF8 – CFC	PCI BUS configuration register

ISA DMA Map

DMA Channel	Device
DMA 0	Unused
DMA 1	ECP
DMA 2	Floppy Disk
DMA 3	Audio
DMA 4	[Cascade]
DMA 5	Unused
DMA 6	Unused
DMA 7	Unused

Memory Map

Address Range	Length	Description
00000 ~ 9F7FFh	638KB	Base Memory
9F800 ~ 9FFFFh	2 KB	Extended BIOS Data Area
A0000 ~ BFFFFh	128 KB	Video Memory
C0000 ~ C9FFFh	40 KB	Video ROM
CA000 ~ DFFFFh	88 KB	Unused
E0000 ~ FFFFFh	128 KB	System ROM BIOS

IRQ Map

IRQ#	Description
IRQ 0	System Timer
IRQ 1	Keyboard
IRQ 2	[Cascade]
IRQ 3	SIR
IRQ 4	Serial Port
IRQ 5	Audio / VGA / USB / (LAN/MODEM)
IRQ 6	Floppy Disk Drive
IRQ 7	Parallel Port
IRQ 8	RTC Alarm
IRQ 9	Reserved for PCMCIA card
IRQ10	Cardbus
IRQ11	Reserved for PCMCIA card
IRQ12	PS/2 Mouse

IRQ#	Description
IRQ13	FPU
IRQ14	Hard Disk Drive
IRQ15	CDROM or DVD

3.3.15 GPIO Pin Assignment

The GPI and GPO pins connected to system devices. The BIOS can get device status and control the device via the GPI and GPO pins.

PMU and GPIO Signal Description

Pin Name	Signal Name	Description	Components
GPI [0]	LS120IN#	LS120 module inside.	VT82C686A
GPI [1]	PSCI#	System control interrupt for ACPI events	VT82C686A ← M38867
GPI [2]	PWRBTN#	Power button release check	VT82C686A
GPI [3]	PWSCI#	System control interrupt for wake-up events	VT82C686A ← M38867
GPI [4]	IRQ 6	Assign to IRQ 6.	VT82C686A
GPI [5]	PME#	PME#	VT82C686A
GPI [6]	CLRTC#	Clear RTC	VT82C686A
GPI [7]	RING#	Ring indicate	VT82C686A
GPI [8]	NC		
GPI [9]	LCDID0	LCD Panel ID Pin 0	VT82C686A
GPI [10]	LCDID1	LCD Panel ID Pin 1	VT82C686A
GPI [11]	NC		
GPI [12]	NC		
GPI [13]	NC		
GPI [14]	NC		
GPI [15]	NC		
GPI [16]	KBID0	Keyboard type data 0	VT82C686A
GPI [17]	KBID1	Keyboard type data 1	VT82C686A
GPI [18]	LCDID 2	LCD Panel ID Pin 2	VT82C686A
GPI [19]	BATT_CHG	Battery Charge LED Indicator	VT82C686A
GPI [20]	CDIN#	CDROM module inside	VT82C686A
GPI [21]	DVDIN#	DVD module inside	VT82C686A
GPI [22]	NC		
GPI [23]	NC		

Pin Name	Signal Name	Description	Components
GPO [0]	NC		
GPO [1]	NC		
GPO [2]	STR#	Suspend to ram.	VT82C686A → PIC
GPO [3]	SUSSTAT1#	Suspend status 1	VT82C686A
GPO [4]	CPUSTP#	CPU stop clock	VT82C686A
GPO [5]	PCISTP#	PCI stop clock	VT82C686A
GPO [6]	NC		
GPO [7]	NC		
GPO [8]	DRAMEN#	Select SO0DIMM Dram socket I2C Bus A or B.	VT82C686A
GPO [9]	NC		
GPO [10]	NC		
GPO [11]	L2ZZNC	Power down L2 Cache	VT82C686A
GPO [12]	PORT80CS#	Read/Write Port 80H	VT82C686A
GPO [13]	MCCS#	ACPI chip select	VT82C686A
GPO [14]	IRTX#	SIR	VT82C686A
GPO [15]	IRRX#	SIR	VT82C686A
GPO [16]	HDDREST#	HDD reset.	VT82C686A
GPO [17]	CDROMReset#	CDROM reset.	VT82C686A
GPO [18]	NC		
GPO [19]	SERIRQ	Serial interrupt request	VT82C686A
GPO [20]	FANON#	Power on FAN.	VT82C686A
GPO [21]	PDCOM#	Power down COM	VT82C686A
GPO [22]	PDAMP#	Power down audio amplifier	VT82C686A
GPO [23]	STANDBY#	Inform to PIC the system is in Standby mode	VT82C686A → PIC
EXTSMI#	EXTSMI#	External SMI signal	VT82C686A ← M38867
RSMRST#	RSMRST#	Reset internal suspend logic(resume reset)	VT82C686A ← PIC
PWRBTN#	PWRBTN#	Power button for VT82C686A	VT82C686A ← PIC

Pin Name	Signal Name	Description	Components
SDA	SMBCLK	SM bus clock	M 38867 → PIC
SCL	SMBDATA	SM bus data	M 38867 → PIC
P40	KBCEXTSMI#	Keyboard SMI#	M38867
P54	BATLOW#	Battery low signal	M38867 ← PIC
P55	LID#	LCD lid closing	M38867
P56	CONADJ#	Panel contrast vary	M38867
P57	BACKADJ#	Panel backlight brightness vary	M38867
P60	IDA#	Battery Inside.	M38867
P62	WAKEUP#	SM bus Alert	M38867,PIC
P64	ACIN#	Adapter plug-in detect	M38867, PIC
P66	PME#		M38867
MCLR	PICRESET#	Reset PIC16C62	PIC
RA5	PWRON	Enable system power	PIC
RA1	LEDBATL#	Battery low led indicate	PIC
RB0	PWRSW#	Power switch for PIC	PIC
RA4	RSTGATE	Reset gate for wakeup inhibit reset	PIC
RB2	VEEENA	Enable panel form PIC	PIC
RB3	LEDSUSP#	Suspend led indicate	PIC

3.4 Power Management

This section provides the Power Management software function of the notebook.

3.4.1 General Requirements

The BIOS meet the following general Power Management requirements:

- Compliant with APM 1.2 Specification
- Full APM Support for Windows 95 Fuel Gauge and Power Management functionality
- Support for Suspend-to-RAM and Suspend-to-Disk mode
- Support for Resume on Modem Ring while in STR Mode. This is controlled by a CMOS Setup option
- Power Management must be OS independent
- Power Management must support Resume-on-Time

3.4.2 Power Management Mode Definitions

A particular implementation of system power management may use some or all of the depicted states. A brief description of the state's characteristics is:

Full-On Mode

The system state where no devices are power managed and the system can respond to applications with maximum performance.

Doze Mode

The CPU clock is slow down and all other devices are still full on. (Similar to IDLE mode – Transparent to user)

Stand By (POS) Mode

A suspend state where all motherboard components are still powered-on except for the system clock generator device. The PCI and CPU buses are driven to the inactive idle state. The system memory is powered and refreshed by the memory bridge, and the graphics frame buffer is powered and refreshed by the graphic chip. The system provides a 32KHz clock (SUSCLK) in this suspend mode to support refresh of these memory subsystems. Only an enabled "resume event" can bring the system out of the powered-on suspend (POS) state. The Banister also provides a resume timer that allows the system to resume after a programmed time has elapsed.

Suspend to RAM (STR) Mode

A suspend state where all motherboard components are powered-off. The CPU and PCI busses are powered off. All devices connected to the CPU and PCI busses must either be powered-off or isolate their bus interfaces. The system memory is powered and refreshed by the memory bridge, and the graphics frame buffer is powered and refreshed by the graphics chip. The system provides a 32 KHz clock (SUSCLK) in this suspend mode to support refresh of these memory subsystems. Only an enabled "resume event" can bring the platform out of the Suspend-to-RAM (STR) state.

Suspend to Disk (STD) Mode:

A suspend state where the context of the entire system is saved to disk, all motherboard components are powered-off, and all clocks are stopped. Any enabled "resume event", such as

Power Button or RTC, can bring the platform out of the Suspend-to-disk (STD) state.

Soft Off (SOFF) Mode

This is the same as suspend to disk except the context of memory is not saved. The system will resume from Soft Off as if a hard reset had occurred.

Mechanical Off (MOFF) Mode

All power except the RTC has been removed from the system.

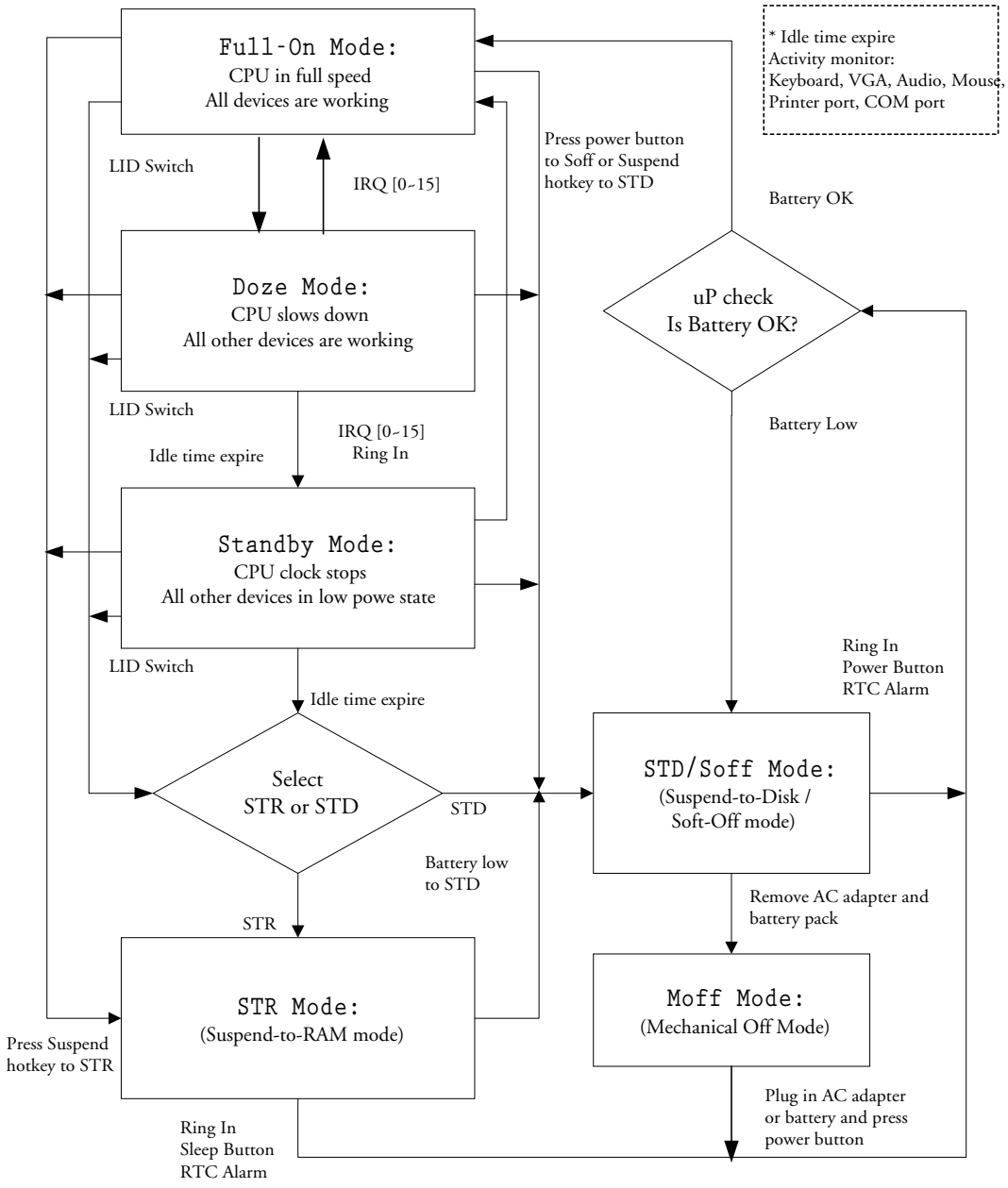
3.4.3 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
B+	Nil	IMM, (9V~20V)
5VALWAYS	Nil	PIC 16C62A
3VALWAYS	Nil	RTC I/F, Internal modem ring
RTCVCC	Nil	RTC
+12V	PWRON	PCMACIA card
+5V	PWRON	M38867, MAX 3243, PCMCIA Slot (5V VCC)
+3V	PWRON	VGA, Video RAM, PCMCIA chip, PCMCIA Slot (3V), DRAM
+3VS	SUSB#	Audio, Clock Generator, FIR (IMI651 SCLK), TAG RAM, PCI interface, Super-IO
+5VS	SUSB#	HDD, CD-ROM, USB, Internal K/B, Glide Pad, External P/S2 Mouse, FDD, Audio AMP, BIOS ROM

3.4.4 Power Management Mode Transition Flow Chart



3.4.5 PMU Mode Transition Event

The following table summarizes the entry events and wake-up events of each power management mode:

Power State	Entry Event	Wake up Event
Doze	Doze Time out	Predefined Memory I/O range access Ring Indicator Keystroke (Internal, external or USB keyboard) Mouse movement IRQ 1-15
STR	Suspend Time out Lid close Sleep button STR hotkey pressed.	Sleep Button Ring Indicator Schedule Alarm Battery Low Lid Open
STD	Suspend Time out Battery Low Fn + Sleep Button	Sleep Button Schedule Alarm
Soft Off	Sleep button Execute Win95 shutdown command	Sleep Button Schedule Alarm

3.4.6 Device Power Control Methodology

Power State of Local Devices Table

This section illustrates the power control status of each key device/component of the system under each power management mode.

State / Component	Doze	Stand By	STR	STD/SOff
CPU	Stop Grant	Stop Clock	Power Off	Power Off
VT8601	ON	Stop Clock	Power Off (except Vcc)	Power Off
VT82C686A	ON	ON	Power Off (except SUSVcc, RTCVcc)	Power Off (except SUSVcc, RTCVcc)
DRAM	ON	Self Refresh	Self Refresh	Power Off
L2 CACHE	ON	Power down	Power Off	Power Off
CDROM	ON	Power down	Power Off	Power Off
HDD	ON	Power down	Power Off	Power Off
FDD	ON	Power down	Power Off	Power Off
KBC	ON	ON	Power down	Power Off
PIC 16C62A	ON	ON	Power down	Power down
VGA	ON	Power down	Power down	Power Off
PCMCIA	ON	Power down	Power down	Power Off
Sound	ON	Power down	Power Off	Power Off

State / Component	Doze	Stand By	STR	STD/Soff
LCD Backlight	ON	Power down	Power Off	Power Off
Serial (UART1)	ON	Power down	Power down	Power Off
LAN	ON	Power down	Power down	Power Off
Modem	ON	Power down	Power down	Power down
Parallel	ON	Power down	Power Off	Power Off

Device Power Control Methodology During Stand by Mode

This section illustrates the control methodology of each device/component and its details under Stand by mode.

Device	Power Down Controlled by	Description
CPU	Hardware	Controlled by SUS_STAT1# pin
VT8601	Hardware	Controlled by SUS_STAT1# pin
VGA Chip	Software	Enter PCI PM D3 state
PCMCIA Controller	Software	Enter PCI PM D3 state
KBC	Working	
FDD	Software	FDD support power down command
HDD	Software	HDD support power down command
CD-ROM	Software	CD-ROM support power down command
Audio AMP	Software	Controlled by GPO[22] pin
Modem	Software	Enter PCI PM D3hot state
LAN	Software	Enter PCI PM D3hot state
LCD Backlight	Hardware	Controlled by VGA chip (FPBACK pin)
Clock Synthesizer	Hardware	Controlled by CPUSTP# and PCISTP# pin
PIC 16C62A	Working	
MAX3243 (RS232 Transceiver)	Software	Controlled by GPO[21] pin
L2 CACHE	Software	Controlled by GPO[3] pin

Device Power Control Methodology During Suspend to RAM Mode

This section illustrates the control methodology of each device/component and its details under Suspend to RAM mode.

Device	Power Down Controlled by	Description
VT8601	Hardware	Controlled by SUS_STAT1# pin
Super I/O	Hardware	Power off
VGA Chip	Software	Controlled by VT8501
HDD	Hardware	Power off
CD-ROM	Hardware	Power off.
PCMCIA Controller	Hardware	Controlled by PCI Bus.
Modem	Software	Power off

Device	Power Down Controlled by	Description
LAN	Hardware	See H/W Spec
FDD	Hardware	Power off
Audio AMP	Hardware	Power off
LCD Backlight	Hardware	Power off
Clock Synthesizer	Hardware	Power off
KBC	Software	Controlled by M38867 power down command
MAX3243 (RS232 transceiver)	Hardware	Controlled by GPO [21] Pin
L2 CACHE	Hardware	Power off
PIC 16C62A	Software	Controlled by PIC 16C62A power down command

Device Power Control Methodology During Suspend to Disk Mode

This section illustrates the control methodology of each device/component and its details under Suspend to Disk mode.

Device	Power Down Controlled by	Description
VT8501	Hardware	Power off
Super I/O	Hardware	Power off
VGA Chip	Hardware	Power off
HDD	Hardware	Power off
CD-ROM	Hardware	Power off
PCMCIA Controller	Hardware	Power off
Modem	Hardware	Supply ring power
LAN	Hardware	Power off
FDD	Hardware	Power off
Audio AMP	Hardware	Power off
LCD Backlight	Hardware	Power off
Clock Synthesizer	Hardware	Power off
KBC	Hardware	Power off
MAX3243 (RS232 transceiver)	Hardware	Power off
L2 CACHE	Hardware	Power off
PIC 16C62A	Software	Controlled by PIC 16C62A power down command

3.4.7 Power / Sleep Button

The Power / Sleep Button can work as Power Button or Suspend Button where the working mode is selected by CMOS setup menu.

Working Mode	Power State					
	OFF	Full on	Doze	Stand by	STR	STD
Power on/off	Power on	Power off	Power off	Power off	Full on	Full on
Sleep	Power on	STR/STD*	STR/STD	STR/STD	Full on	Full on

If you cannot resume properly from Suspend by pressing the Sleep button, try to press it and hold for over 4 seconds, the system will force to power off.

The mode of STR/STD can be selected via CMOS setup.

3.4.8 Lid Switch (Cover Switch)

The Lid Switch will be recognized only when Lid Switch continuously closed for more than 1 second. The system may have different action upon the LCD panel is closed or opened.

Display Mode	Power State	Lid Close	Lid Open
LCD	Full on	STR	Resume
	STR	No active	Resume
	STD	No active	No active
CRT	Full on	No active	No active
	STR	No active	Resume
	STD	No active	No active
Both	Full on	CRT	Both
	STR	No active	Resume
	STD	No active	No active

3.4.9 Power Management Mode Transition

To / From	Full-On	Stand by	Suspend to RAM	Suspend to disk	Off
Full-On	-	Yes	Yes	Yes	Yes
Stand by	Yes	-	Yes	Yes	Yes
Suspend to RAM	Yes	No	-	Yes	-
Suspend to Disk	Yes	No	No	-	-
Soft Off	Yes	No	No	No	-

Transition to Suspend to RAM

- Timer expires
- Lid Switch pressed down (LCD only)

Transition to Suspend to Disk

- Timer expires
- Critical Battery (always Suspend to Disk)

Transition to Soft Off

- Power Switch (When system is not in STR or STD mode)

Resume from Suspend to RAM

- Power Switch
- Modem Ring (SETUP “Resume From Modem Ring: [Enabled]”)
- RTC alarm

Resume from Suspend to Disk

- Power Switch
- Modem Ring (SETUP ”Resume From Modem Ring: [Enabled]“)
- RTC alarm

Resume from Off

- Power Switch

3.5 ACPI

This section provides the ACPI software function of the notebook.

3.5.1 General Requirements

The BIOS must meet the following general Power Management requirements:

- Refers to the portion of the firmware that is compatible with the ACPI specifications.
- Support for Suspend-to-RAM (S3 state) and Suspend-to-Disk mode (S4 state).
- Support the Wake up event from Modem Ring in S3~S4 state. This is enabled by a CMOS Setup option.
- Support the Wake up event from RTC Time/Date alarm in S3~S4 state. This is enabled by a CMOS Setup option.
- Power Management must not substantially affect or degrade system performance.
- Power Management must be OS independent

3.5.2 System Power Plane

Power Group	Power Control Pin	Controlled Devices
B+	Nil	IMM, (9V~12V)
+12V	PWRON	Inverter, AC97 codec, PCMCIA card
+3V	PWRON	VGA, PCMCIA, PCMCIA Slot 3V, DRAM, North Cluster (DRAM I/F), MAX32443
+3VS	SUSB#	Flash ROM, Audio, Clock Generator, TAG RAM
+5V	PWRON	PCMCIA Slot 5V VCC, M38867
+5VS	SUSB#	Super I/O, HDD, CD-ROM, USB, LPT Port, K/B, Glide Pad, Ext. PS/2 Mouse, IR, FDD, Audio AMP
+3V Always	Nil	UP (PIC16C62), Internal modem ring

3.5.3 Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user. Following is a list of the system states:

G0/S0 - Working

In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

G1 - Sleeping

A state where the computer consumes a small amount of power, user mode threads are not being executed, and the system appear to be off (from an end user's perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are saved by the hardware, while the rest by the system software. It is not safe to disassemble the machine in this state.

G2/S5 - Soft Off

This is a state where the computer consumes a minimal amount of power. No user mode or system mode code is running. This state requires a large latency in order to return to the Working state. The system's context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

G3 – Mechanical Off:

This state is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

3.5.4 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state and transition, refer to the ACPI specification.

S1 Sleeping State (Doze mode)

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system contexts.

S2 Sleeping State (Standby mode)

The S2 sleeping state is a low wake-up latency sleeping state. This state is similar to the S1 sleeping state except the CPU and system cache context is lost (the OS is responsible for maintaining the caches and CPU context). Control starts from the processor's reset vector after the wake-up event.

S3 Sleeping State (STR mode)

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake-up event.

S4 Sleeping State (STD mode)

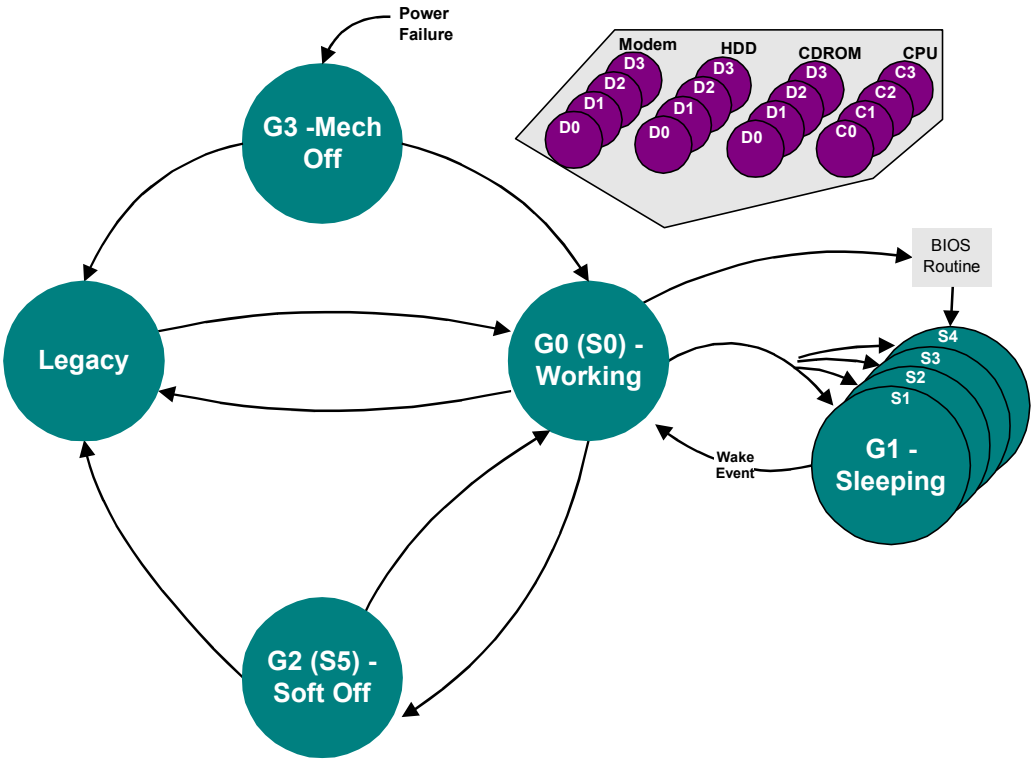
The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

S5 Soft Off State

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the "SOFF" off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state. This is to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

3.5.5 Power States

From a user-visible level, the system can be thought of as being one of the states in the following diagram:



3.5.6 Power States transition event

The following table summarizes the entry events and wake-up events of each power:

Power State	Entry Event	Wake up Event
S1	OSPM* control	Predefined Mem/IO range access Ring Indicator Keystroke IRQ1-15 SMI# / ACPI SCI# / USB
S2	OSPM control	Predefined Mem/IO range access Battery Warning Battery Low Ring Indicator Keystroke (Int., Ex. And USB keyboard) Mouse movement Schedule Alarm SMI# / ACPI SCI# / USB

Power State	Entry Event	Wake up Event
S3	OSPM control, Sleep Button, Lid Close	Sleep button Ring Indicator Schedule Alarm Lid Open PME# Battery Low
S4	OSPM control,	Sleep Button Ring Indicator Schedule Alarm
S5	OSPM control, Power Button	

ⓘ OSPM: OS-directed Power Management

3.5.7 Lid Switch

ⓘ The function of the Lid Switch (Lid Cover) follows the ACPI Power Management Control Settings under Windows.

3.5.8 Power/Sleep Button

ⓘ The function of the Power/Sleep Button follows the ACPI Power Management Control Settings under Windows.

3.5.9 Device Power Management

ⓘ Please refer to the 3.4.8 Device Power Management for APM mode.

3.6 Battery Management

The A440 supports both Li-Ion and Ni-MH Battery Pack. There is only one battery pack activating at one time.

3.6.1 Battery-Powered Mode

This mode assumes that the mobile system is powered only from the battery. The purpose of this is to maximize battery life.

3.6.2 AC-Powered Mode

In this mode it is assumed that the mobile system is powered from an external AC/DC source. The purpose of this state is to maximize performance subject to thermal constraints.

3.6.3 Battery Sub-system

- The charger will stop charge the battery when the following condition is detected.
  - The temperature of the system is too high

  - The battery voltage is too high
- Battery Life → average 2.5 Hours.
- Battery reading methodology is through M38867 SMBus.

ⓘ Note that the battery life is dependent on different configuration running. E.g. with CD-ROM battery life is shorter, document keyin only battery life is longer, PMU disable battery life is short, PMU enable battery life is longer.

3.6.4 Battery Low

When the battery voltage is approaching to the Low level (8%), the M38867 will generate a battery low SMI. The system will do the following action.

- The Power Indicator will become amber.
- The system will issue Warning beep.

ⓘ Under Windows 98, the battery low level is set at 10%.

3.6.5 Battery Low-Low

When the battery voltage is approaching to the Low-Low level (3%), the M38867 will generate a battery low-low SMI. The system will do the following action.

- The Power Indicator will keep amber.
- The system will enter Suspend To Disk mode even the power management is disabled. The function of power-on or Resume will be inhibited until the Battery Low-Low condition is removed.

ⓘ Under Windows 98, the battery critical level is set at 3%.

3.6.6 AC Adapter

When plug in the AC adapter, the system will do the following action:

- The charger will charge the Main Battery, if remaining capacity is not full.
- The Battery Charging Indicator will turn on if the battery is in changing mode.
- The power management function will be disabled, if the Setup item of “Power Management” is set to “Battery Only”.
- The “Battery Warning” and “Battery Low” condition will be removed.

3.7 PIC16C62A – uP

The micro controller PIC16C62A acts as a supplement for power management control. It supports many functions via SMBus interface.

3.7.1 System Communication with PIC16C62A

The system communicates with PIC16C62A via SMBus interface. The SMBus host (M38867) should be firstly initialized before starting the transaction. The following is the procedure for system communication with PIC16C62A:

1. Enable SMBus interface by writing 01h to SmbHstCfg register.

2. Get SMBus I/O port base address by reading from SmbBA register.

3. Clear SMBus status by writing 1Eh to SmbHstSts register.

4. Write the PIC16C62 slave address to SmbHstAdd register.
   - Send command to PIC16C62A -- Slave address is 04h.
   - Read data from PIC16C62A -- Slave address is 05h.

5. Write the desired command to SmbHstCmd register.

6. Write the desired parameters to SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to send command to PIC16C62A.

7. Wait for SMBus interrupt to occur, by monitoring SmbHstSts register INTR bit.

8. Get the desired data by reading from SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to read data from PIC16C62A.

3.7.2 PIC16C62 Command List

The micro controller PIC16C62 (called micro-P or uP) acts as a supplement for power management control. It supports the following functions via SMBus command:

Command/Data	Access	Unit	Function Description
0x00			Reserved
0x01	read	word	Read PIC software version
0x02	read	byte	Read LCD contrast level (DAC)
0x03	read	byte	Read LCD brightness level (DAC)
0x04	read	word byte0 byte1	Read primary battery DQ_NAC NACH NACL
0x05	read	word byte0 byte1	Read 1st battery DQ_LMD&NACH DQ_LMD DQ_NACH
0x06	read	byte	Read primary battery DQ_FLGS1
0x07	read	byte	Read primary battery DQ_TMPGG
0x08	read	byte	Read primary battery DQ_FLGS2

Command/Data	Access	Unit	Function Description
0x09	read	byte	Read primary battery DQ_PPD
0x0A	read	byte	Read primary battery DQ_PPU
0x0B	read	byte	Read primary battery DQ_VSB 2014
0x0C	read	byte	Read primary battery DQ_VTS 2014
0x0D	read	word byte0 byte1	Read secondary battery DQ_NAC NACH NACL
0x0E	read	byte byte0 byte1	Read 2nd battery DQ_LMD&NACH DQ_LMD DQ_NACH
0x0F	read	byte	Read secondary battery DQ_FLGS1
0x10	read	byte	Read secondary battery DQ_TMPGG
0x11	read	byte	Read secondary battery DQ_FLGS2
0x12	read	byte	Read secondary battery DQ_PPD
0x13	read	byte	Read secondary battery DQ_PPU
0x14	read	byte	Read secondary battery DQ_VSB
0x15	read	byte	Read secondary battery DQ_VTS
0x16	read	word byte0 byte1	Read battery chemistry characteristic Primary battery 0x00:non-battery 0x02:Li-ION 0x03:Ni-MH Secondary battery 0x00:non-battery 0x02:Li-ION 0x03:Ni-MH
0x17	read	word byte0 byte1	Read primary battery NACL1, NACL2 at interval of 20s NACL2 NACL1
0x18	read	word byte0 byte1	Read secondary battery NACL1, NACL2 at interval of 20s NACL2 NACL1
0x19	read	word byte0 byte1	Read LCD contrast/brightness Brightness Contrast
0x1A	reserved		
0x1B	reserved		
0x1C	reserved		
0x1D	reserved		
0x1E	reserved		
0x1F	reserved		
0x20	write	byte	System command

Command/Data	Access	Unit	Function Description
0x20/00			NOP
0x20/01			System suspend request
0x20/02			System resume from suspend
0x20/03			Mask PICSMI, BAT_L, BAT_LL
0x20/04			Enable PICSMI, BAT_L, BAT_LL
0x20/05			Blinking battery low LED
0x20/06			Un-blinking battery low LED
0x20/07			AC adapter plugged in
0x20/08			AC adapter plugged out
0x20/09			System power off
0x20/0A			Used in SMB system
0x20/0B			Used in DQ battery system
0x20/0C			Sound single set alarm beep
0x20/0D			Un-sound alarm beep
0x20/0E			Blinking battery low LED & Sound single alarm beep
0x20/0F			Un-blinking battery low LED & Un-sound single alarm beep
0x20/10			Sound alarm beep twice per minute
0x20/11			Un-sound alarm beep twice per minute
0x20/12			Blinking battery low LED & Sound alarm beep twice per minute
0x20/13			Un-blinking battery low LED & Un-sound alarm beep twice per minute
0x20/14			Enable LCM VEENA
0x20/15			Disable LCM VEENA
0x20/16			System resume from suspend & Issue a low pulse 100mS
0x20/17			Set suspend LED ON
0x20/18			Set suspend LED OFF
0x20/19			Stop PWM1 & PWM2 function
0x20/1A			Resume PWM1 & PWM2 function
0x20/1B			Mask modem ring-in resume
0x20/1C			Enable modem ring-in resume
0x21	write	byte	Set LCD contrast level
0x22	write	byte	Set LCD contrast maximum value
0x23	write	byte	Set LCD contrast minimum value
0x24	write	word byte0 byte1	Set LCD adjust scale Contrast scale Brightness scale
0x25	write	byte	Set LCD brightness level
0x26	write	byte	Set LCD brightness maximum value
0x27	write	byte	Set LCD brightness minimum value

Command/Data	Access	Unit	Function Description
0x28	write	word byte0 byte1	First power on set LCD contrast, brightness level & for POST reset BAT_L, BAT_LL signal & LED Contrast Brightness
0x29	reserved		
0x2A	write	word byte0 byte1	Write data to primary battery BQ2010 command | 0x80 (set bit7) i.e. 83H:write NACH 84H:write BATID 85H:write LMD 8CH:write VTS 2014 only Data
0x2B	write	word byte0 byte1	Write data to secondary battery BQ2010 command | 0x80 (set bit7) i.e. 83H:write NACH 84H:write BATID 85H:write LMD 8CH:write VTS 2014 only Data

3.8 Miscellaneous

3.8.1 Security

The user may enter up to eight standard text characters for a password. The password includes two levels. The higher priority is the Supervisor Password. The lower priority is the User Password. The Supervisor Password can access all the system resource. Also, the User Password may not access the floppy disk when the Supervisor Password protects it.

When the security function is enabled, the system will request the user to enter password during the following situation:

- Power On → The system will prompt the user to enter the password before booting the OS. If the user key in the wrong password three times, then the system will halt.

- Resume → The system will prompt the user to enter password while resuming from STR or STD mode. If the user keys in the wrong password for three times, the system will not resume and should return to Suspend mode.

- Entering CMOS Setup → The system will prompt the user to enter the password before entering the CMOS Setup. If the user keys in the wrong password for three times, then the system will halt.

3.9 CMOS Setup Utility

The Setup utility is used to configure the system. The Setup contains the information regarding the hardware for boot purpose. The changed settings will take effect after the system rebooted. Refer to Chapter 1 on running BIOS Setup Program for more detailed information.