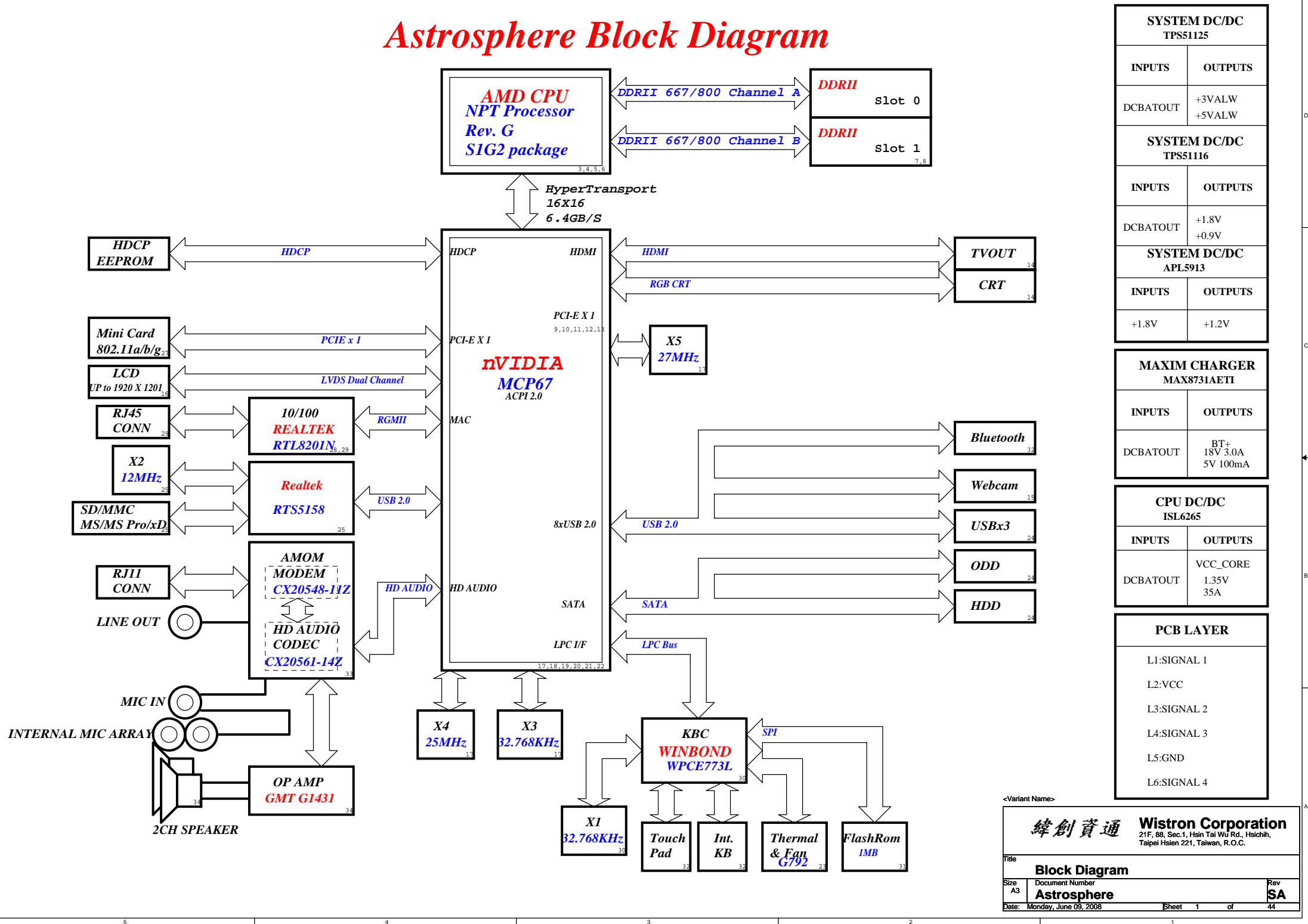


# Astrosphere Block Diagram



SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
DCBATOUT	+3VALW +5VALW

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+1.8V +0.9V

SYSTEM DC/DC APL5913	
INPUTS	OUTPUTS
+1.8V	+1.2V

MAXIM CHARGER MAX8731AETI	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC ISL6265	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 1.35V 35A

PCB LAYER	
L1:	SIGNAL 1
L2:	VCC
L3:	SIGNAL 2
L4:	SIGNAL 3
L5:	GND
L6:	SIGNAL 4

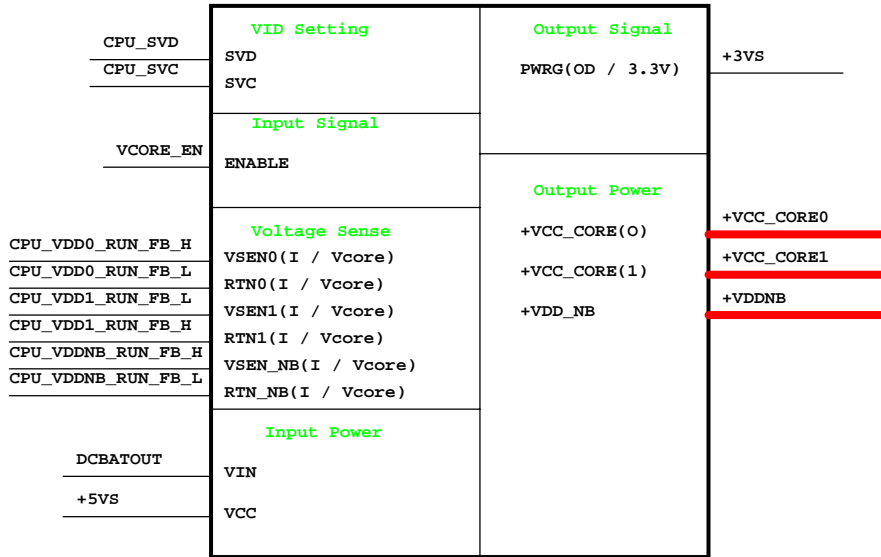
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

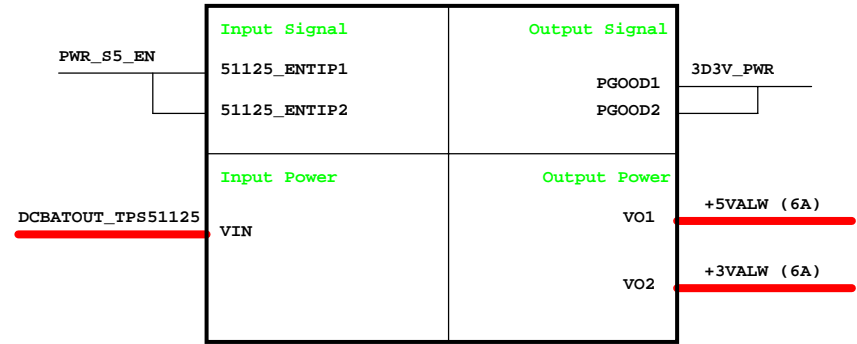
Title: **Block Diagram**

Size: A3	Document Number: <b>Astrosphere</b>	Rev: SA
Date: Monday, June 09, 2008	Sheet: 1 of 44	

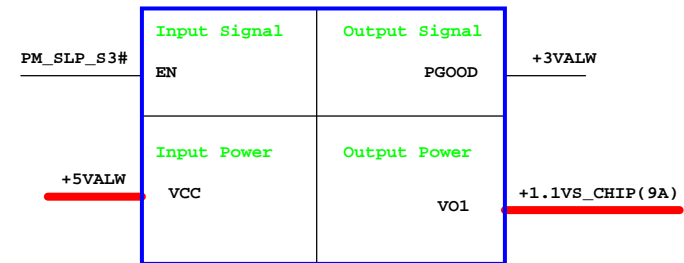
**CPU\_CORE**  
**ISL6265**



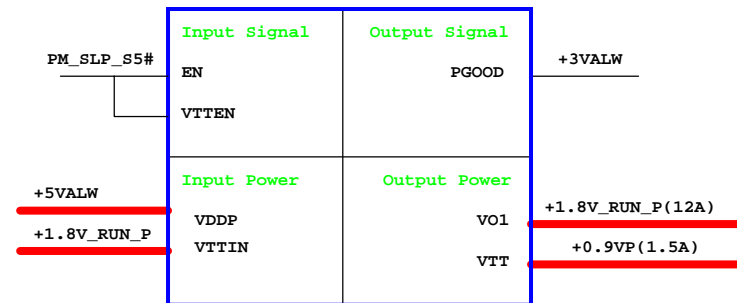
**5V/3.3V**  
**TI TPS51125**



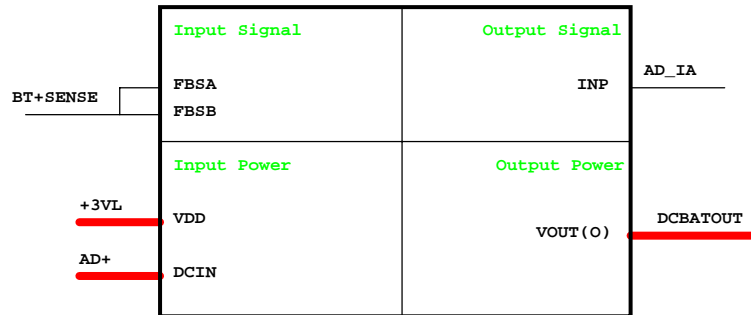
**+1.1VS\_CHIP**  
**SC412A**



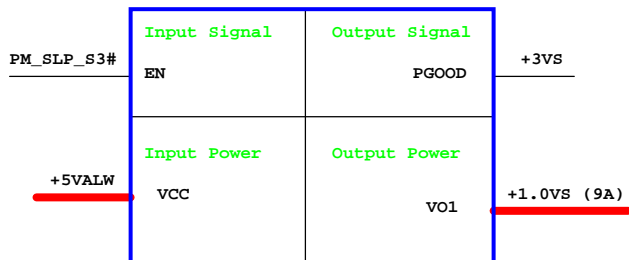
**+1.8V/ +0.9VP**  
**TPS51116**



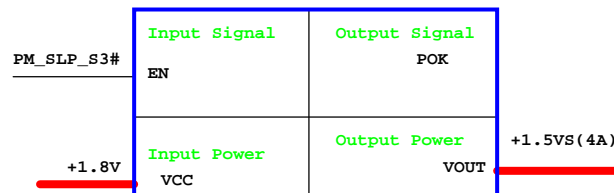
**Charger**  
**MAX8731A**



**+1.0VS** SC471A

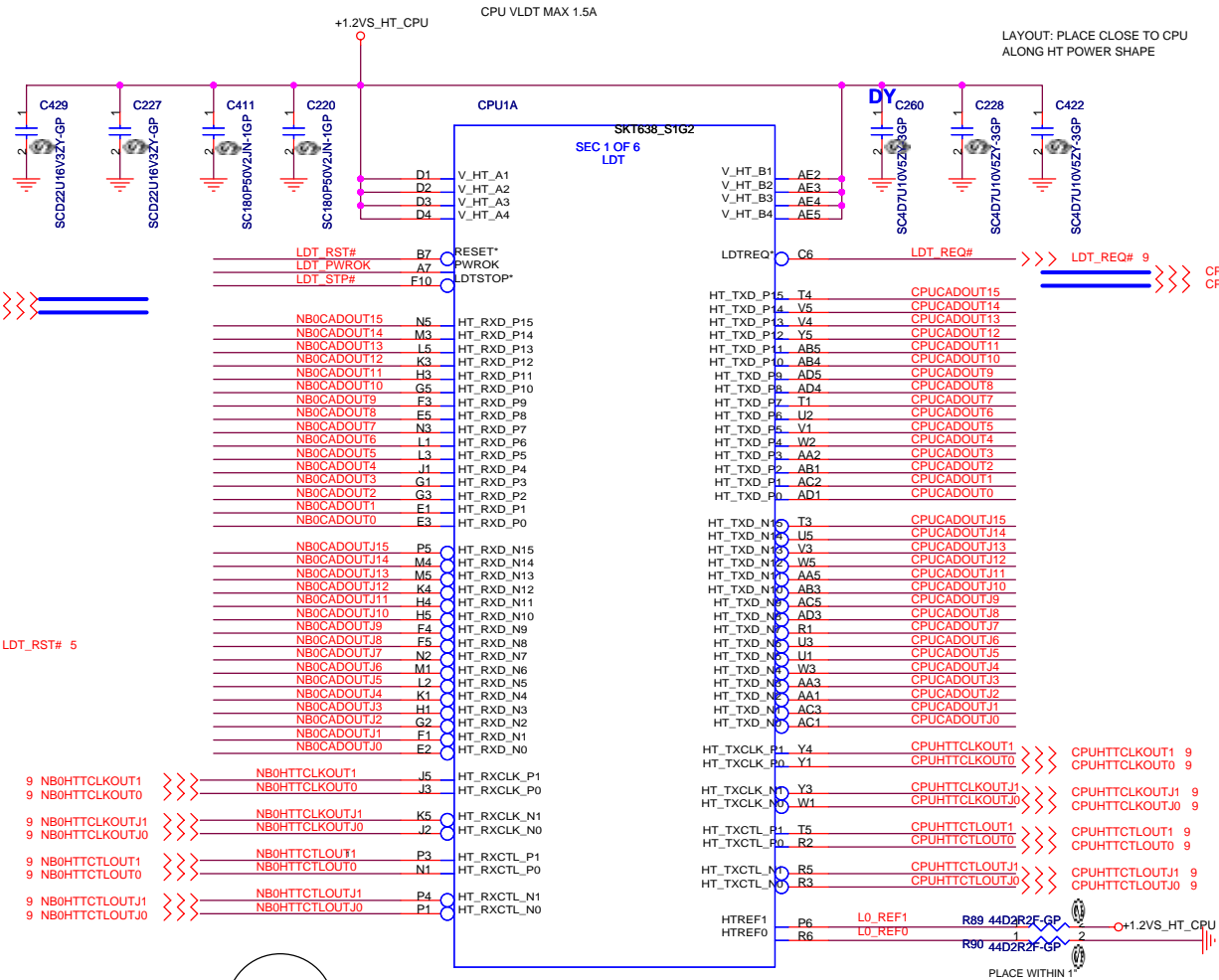


**+1.5V\_VS**  
**APL5913**

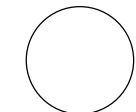
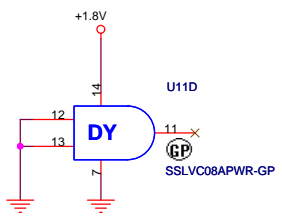
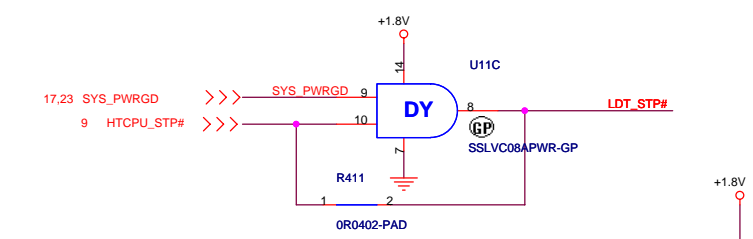
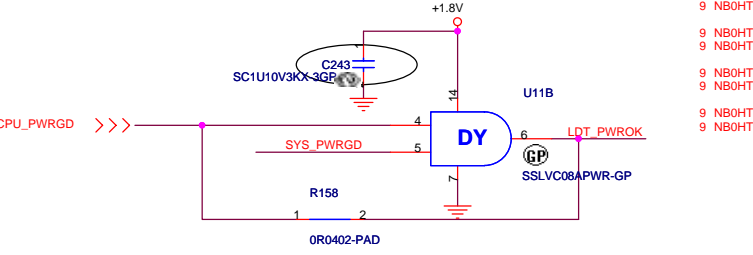
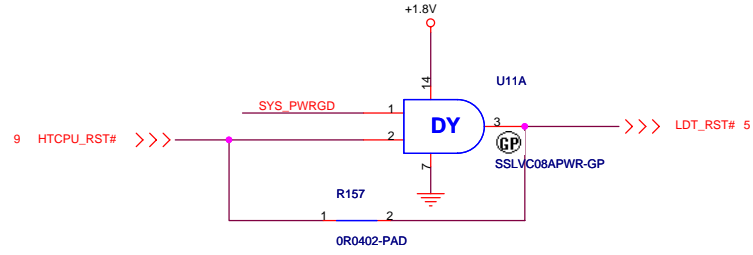
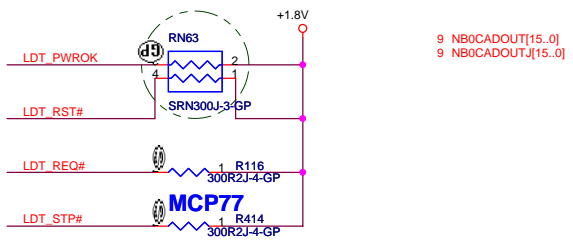


<Variant Name>

LAYOUT: PLACE CLOSE TO CPU  
ALONG HT POWER SHAPE



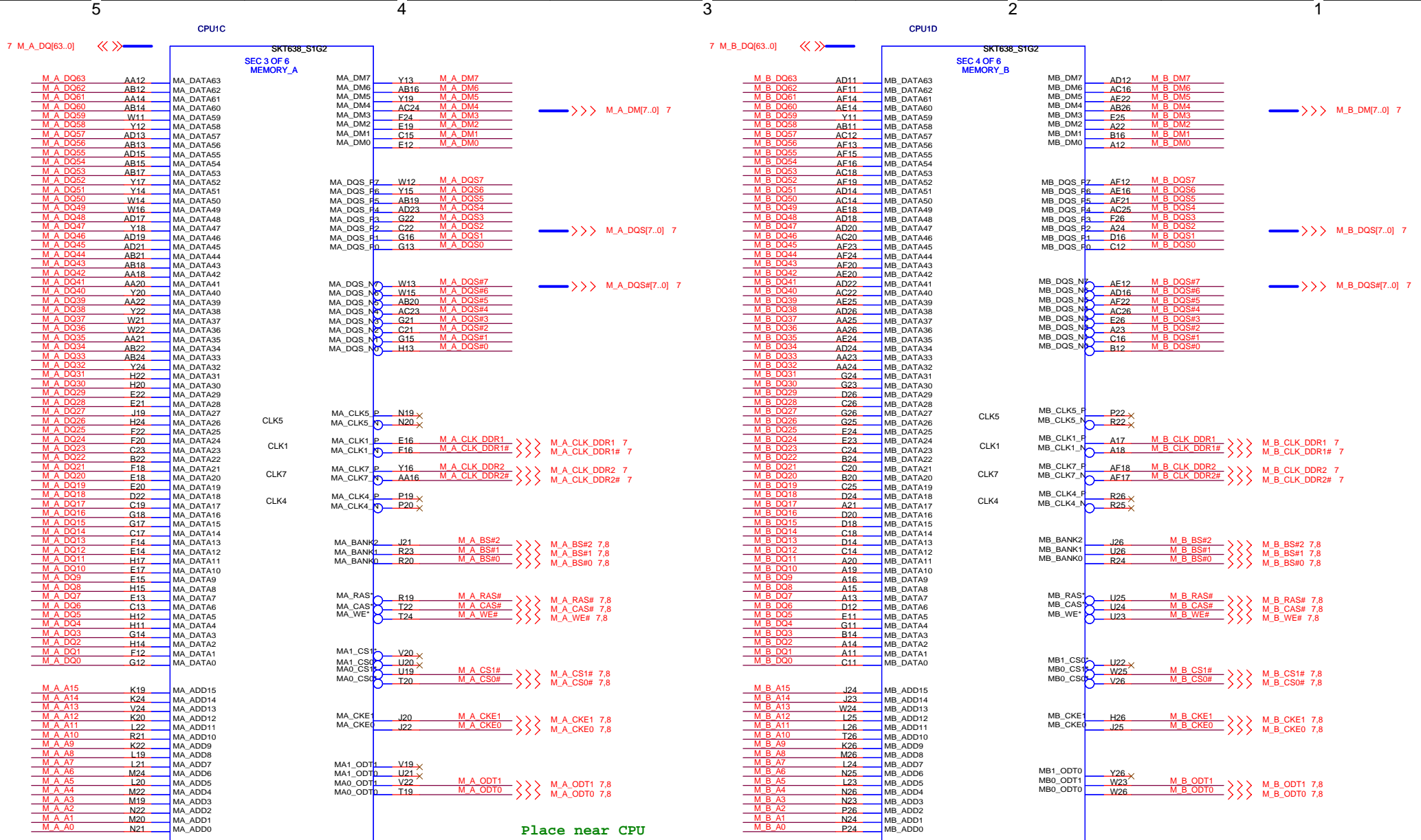
PV 0408



<Variant Name>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsish Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

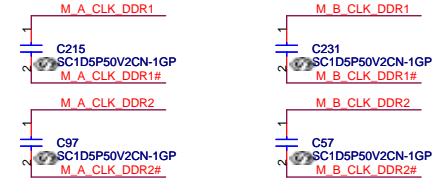
Title		
<b>CPU(1/4) HT</b>		
Size	Document Number	Rev
A3	<b>Astrosphere</b>	<b>SA</b>
Date:	Monday, June 09, 2008	Sheet 3 of 44



Place near CPU

>>> M\_A\_A[15..0] 7.8

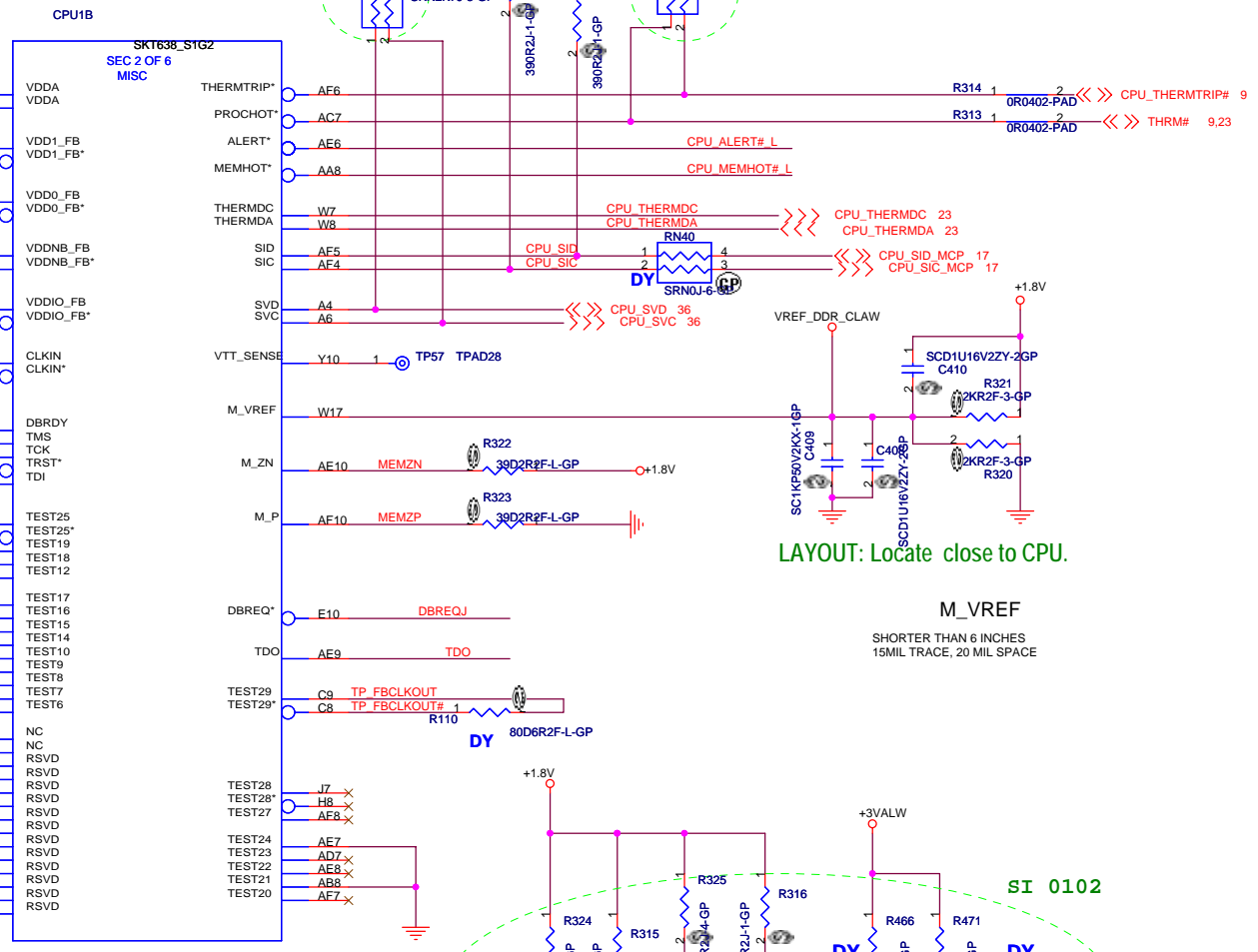
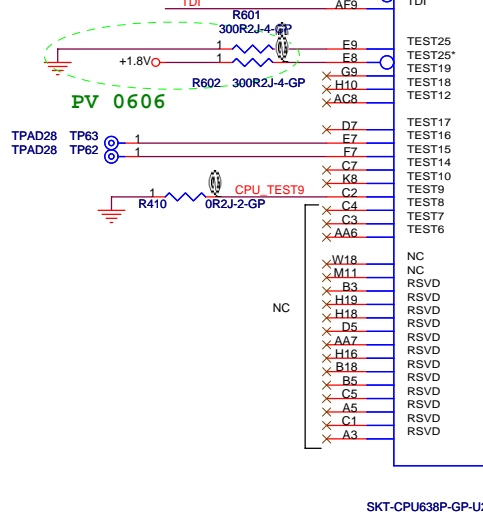
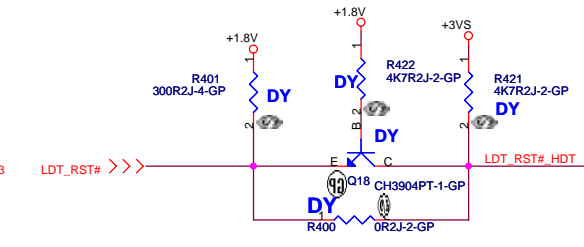
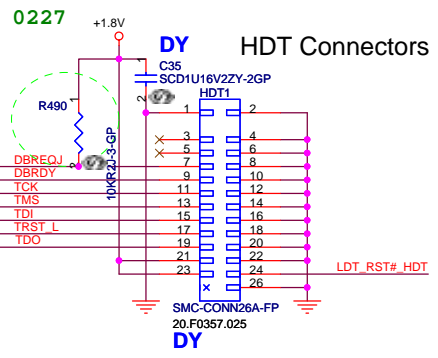
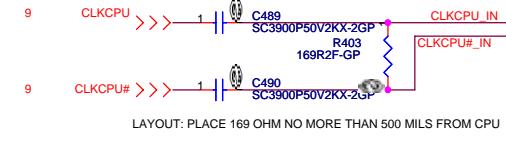
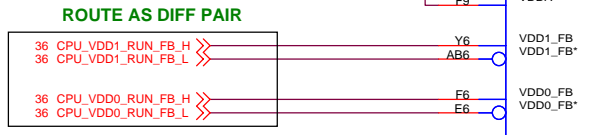
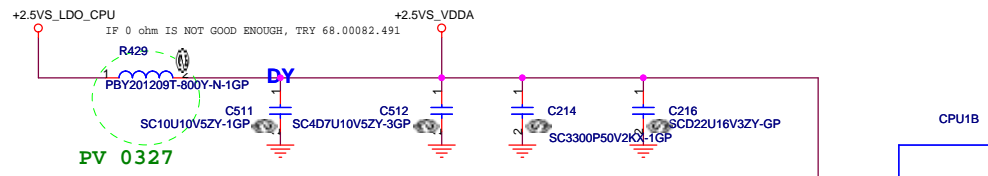
>>> M\_B\_A[15..0] 7.8



MAX NECKDOWN TO & FROM CAPS IS 500MILS  
TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS

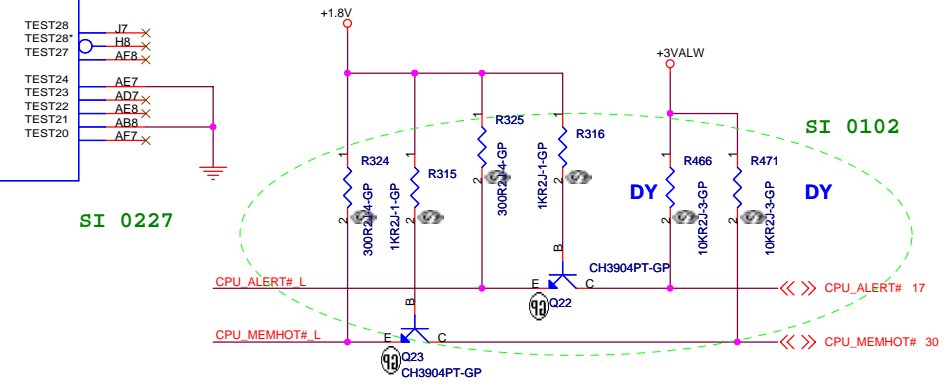
<-Variant Name-

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>CPU(2/4) DDR II</b>			
File	Document Number		Rev
Size	Astrosphere		SA
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LAYOUT: Locate close to CPU.

M\_VREF  
 SHORTER THAN 6 INCHES  
 15MIL TRACE, 20 MIL SPACE



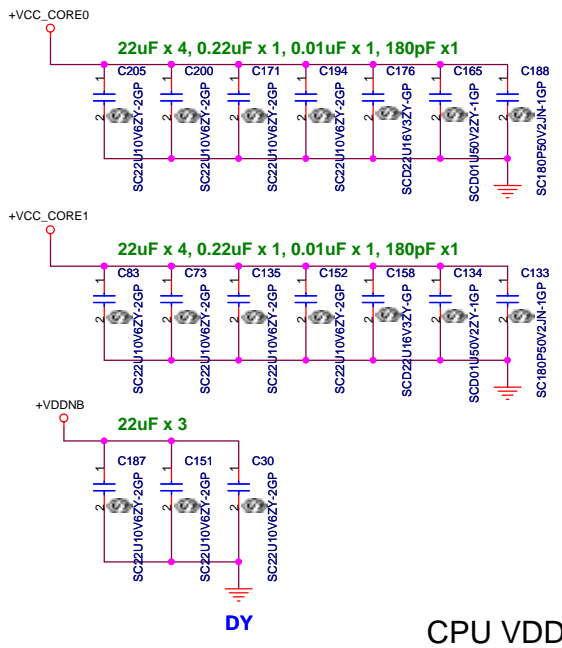
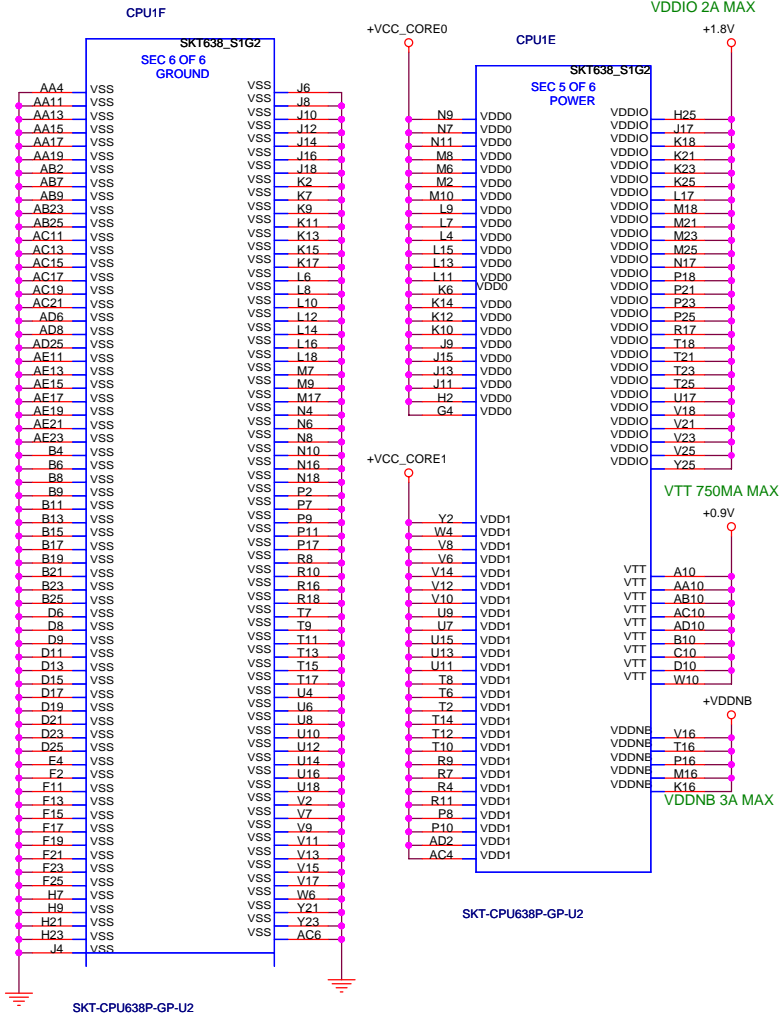
<-Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(3/4) CONTROL**

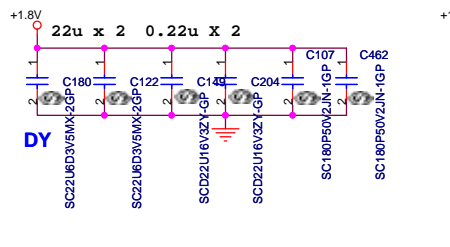
Size: A3 Document Number: **Astrosphere** Rev: SA

Date: Monday, June 09, 2008 Sheet 5 of 44

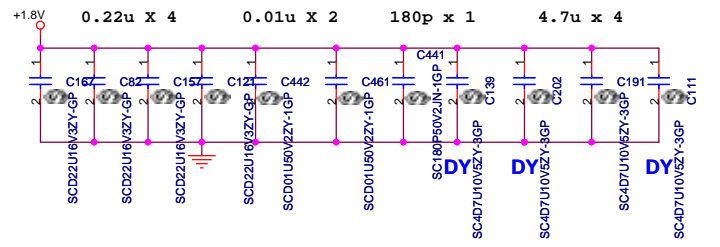


**CPU VDDIO**

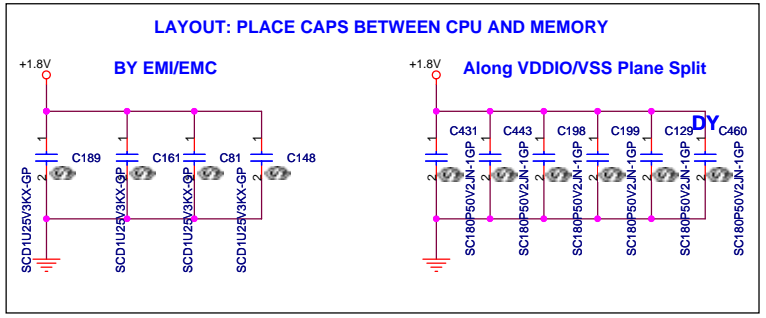
LAYOUT: PLACE UNDER CPU ON BACK



LAYOUT: PLACE CLOSE TO CPU BETWEEN CPU AND MEMORY

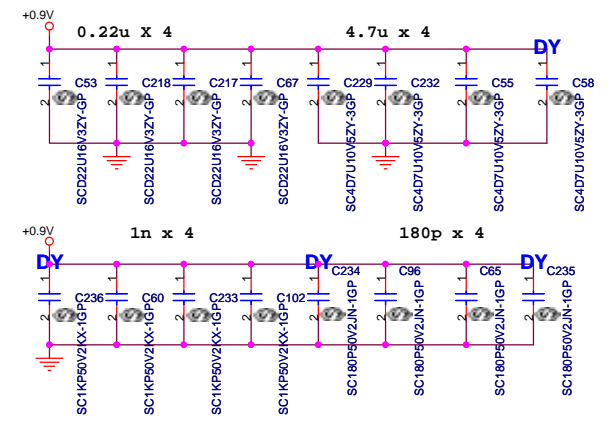


LAYOUT: PLACE CAPS BETWEEN CPU AND MEMORY



**CPU MEMORY VTT**

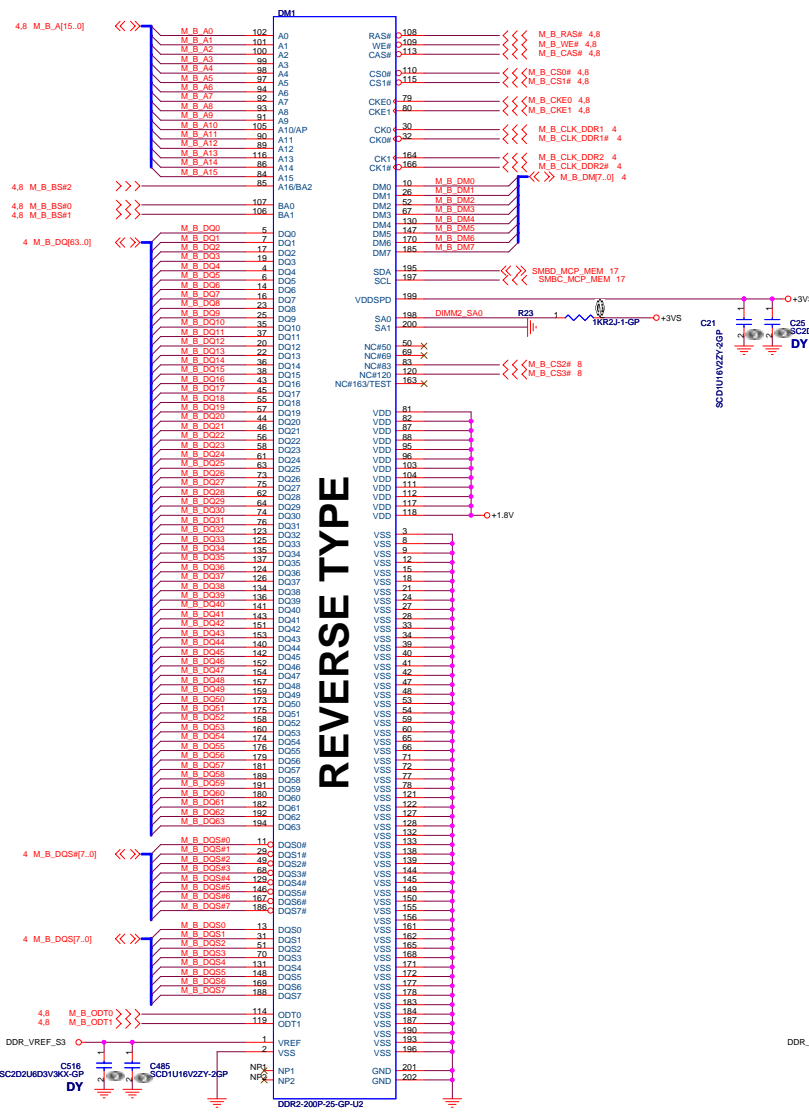
LAYOUT: PLACE CLOSE TO CPU BETWEEN CPU AND MEMORY



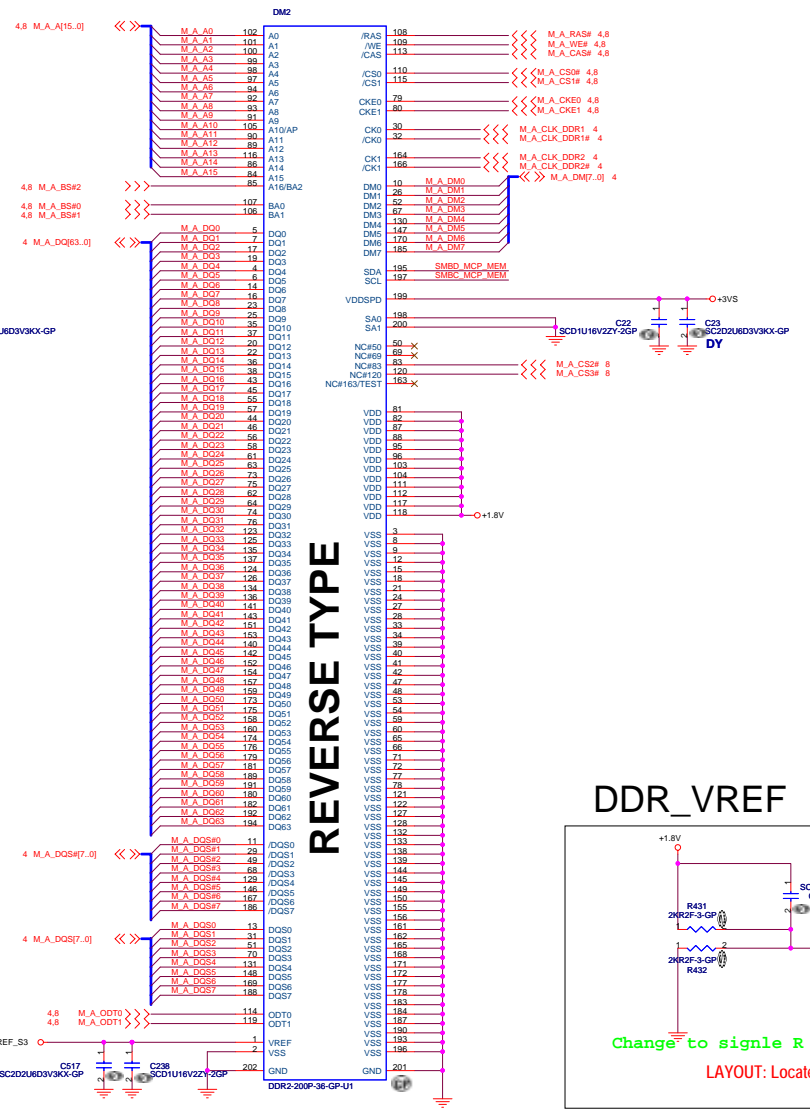
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**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

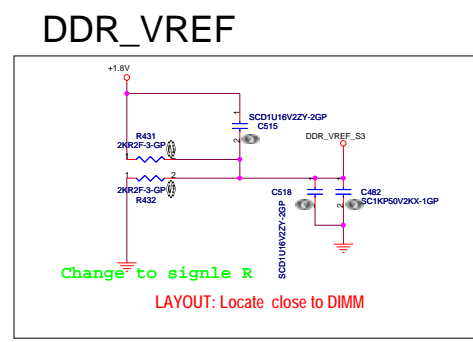
Title <b>CPU(4/4) POWER</b>		
Size A3	Document Number <b>Astrosphere</b>	Rev <b>SA</b>
Date: Monday, June 09, 2008	Sheet 6	of 44



Hi 9.2 mm **DM1 use 62.10017.B51**



Low 5.2 mm **DM2 use 62.10017.E11**

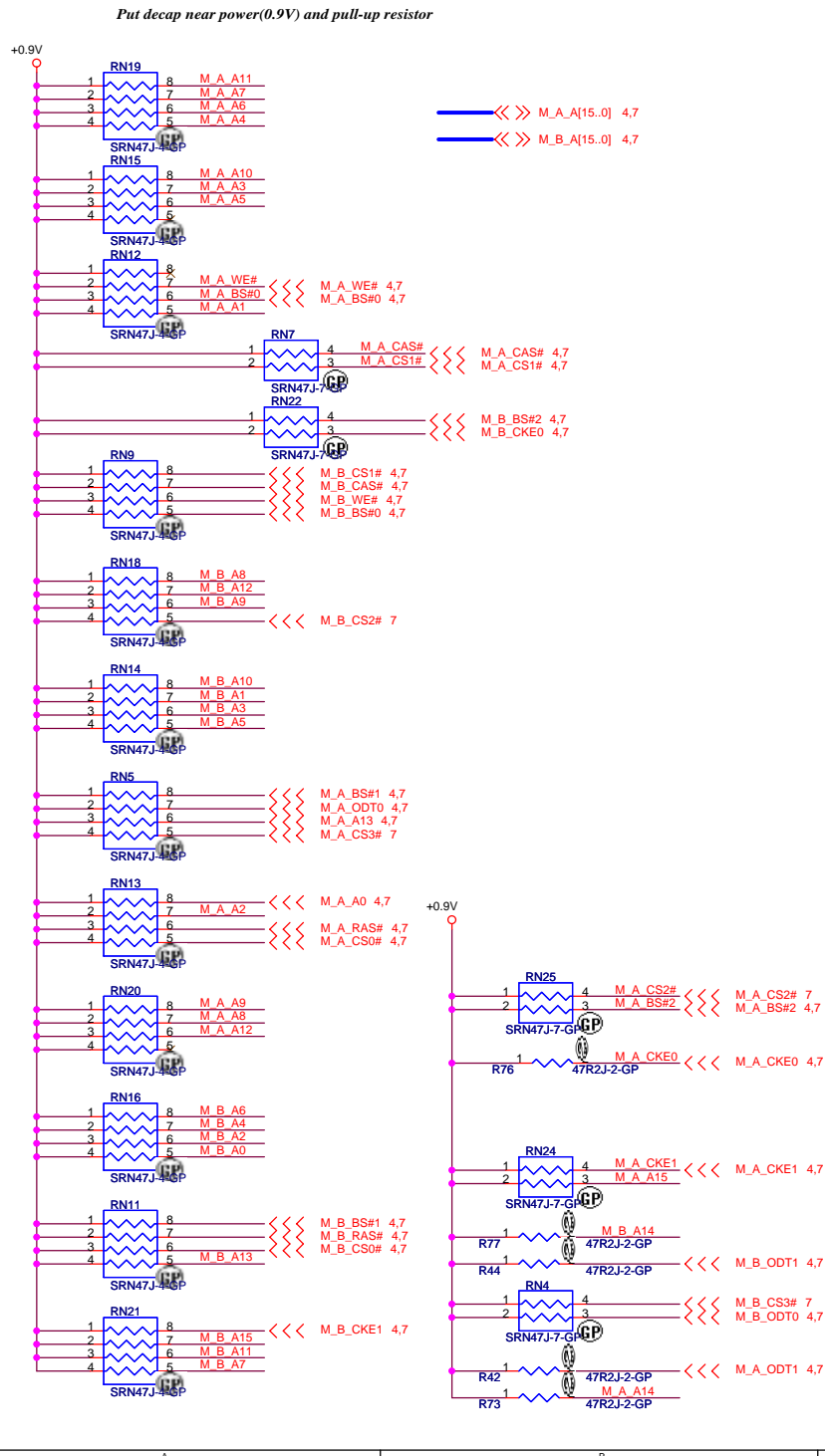


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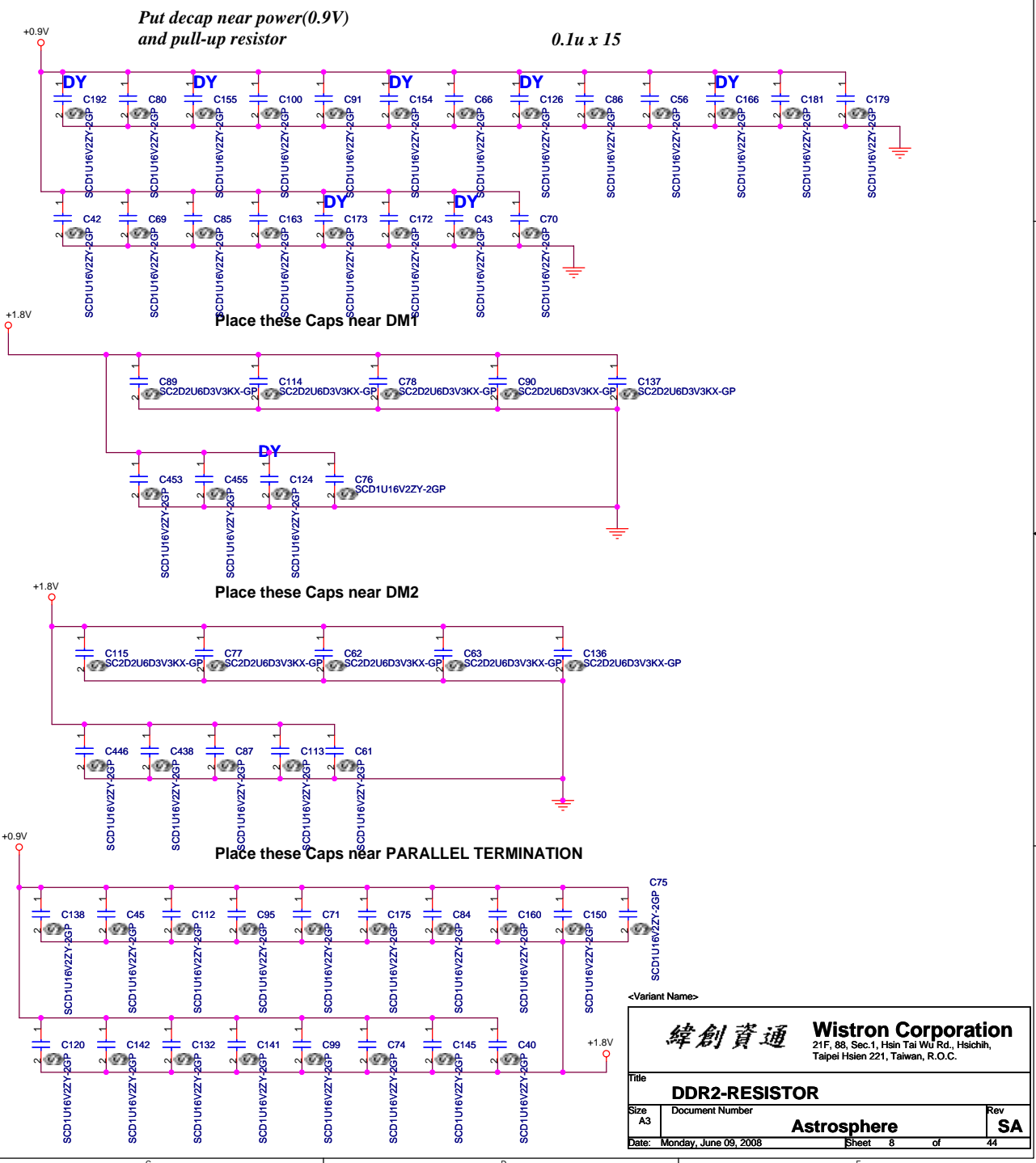
**REVERSE TYPE**



# PARALLEL TERMINATION



# Decoupling Capacitor



<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	<b>DDR2-RESISTOR</b>		
Size	Document Number	<b>Astrosphere</b>	
Date:	Monday, June 09, 2008	Sheet	8 of 44
Rev	<b>SA</b>		



CPUCADOUT[15..0] 3  
 CPUCADOUTJ[15..0] 3

3 NB0CADOUT[15..0] <<<<  
 3 NB0CADOUTJ[15..0] <<<<

U48A 1 OF 8

CPUCADOUT0	AE16	HT_MCP_RXD0_P	HT_MCP_TXD0_P	AK27	NB0CADOUT0
CPUCADOUTJ0	AG18	HT_MCP_RXD0_N	HT_MCP_TXD0_N	CAJ27	NB0CADOUTJ0
CPUCADOUT1	AH16	HT_MCP_RXD1_P	HT_MCP_TXD1_P	AK26	NB0CADOUT1
CPUCADOUTJ1	AJ18	HT_MCP_RXD1_N	HT_MCP_TXD1_N	CAJ26	NB0CADOUTJ1
CPUCADOUT2	AJ15	HT_MCP_RXD2_P	HT_MCP_TXD2_P	AK25	NB0CADOUT2
CPUCADOUTJ2	AK15	HT_MCP_RXD2_N	HT_MCP_TXD2_N	CAJ25	NB0CADOUTJ2
CPUCADOUT3	AK18	HT_MCP_RXD3_P	HT_MCP_TXD3_P	AL24	NB0CADOUT3
CPUCADOUTJ3	AL18	HT_MCP_RXD3_N	HT_MCP_TXD3_N	CAJ24	NB0CADOUTJ3
CPUCADOUT4	AG17	HT_MCP_RXD4_P	HT_MCP_TXD4_P	AK22	NB0CADOUT4
CPUCADOUTJ4	AF17	HT_MCP_RXD4_N	HT_MCP_TXD4_N	CAJ22	NB0CADOUTJ4
CPUCADOUT5	AL17	HT_MCP_RXD5_P	HT_MCP_TXD5_P	AK21	NB0CADOUT5
CPUCADOUTJ5	AK17	HT_MCP_RXD5_N	HT_MCP_TXD5_N	CAJ21	NB0CADOUTJ5
CPUCADOUT6	AL18	HT_MCP_RXD6_P	HT_MCP_TXD6_P	AH21	NB0CADOUT6
CPUCADOUTJ6	AJ18	HT_MCP_RXD6_N	HT_MCP_TXD6_N	CAJ21	NB0CADOUTJ6
CPUCADOUT7	AK19	HT_MCP_RXD7_P	HT_MCP_TXD7_P	AM20	NB0CADOUT7
CPUCADOUTJ7	AD14	HT_MCP_RXD7_N	HT_MCP_TXD7_N	AG27	NB0CADOUT8
CPUCADOUT8	AD14	HT_MCP_RXD8_P	HT_MCP_TXD8_P	AH27	NB0CADOUT8
CPUCADOUTJ8	AE14	HT_MCP_RXD8_N	HT_MCP_TXD8_N	AF25	NB0CADOUT9
CPUCADOUT9	AF14	HT_MCP_RXD9_P	HT_MCP_TXD9_P	AG25	NB0CADOUT9
CPUCADOUTJ9	AG14	HT_MCP_RXD9_N	HT_MCP_TXD9_N	AH25	NB0CADOUT10
CPUCADOUT10	AH14	HT_MCP_RXD10_P	HT_MCP_TXD10_P	AJ25	NB0CADOUT10
CPUCADOUTJ10	AL14	HT_MCP_RXD10_N	HT_MCP_TXD10_N	AE23	NB0CADOUT11
CPUCADOUT11	AL13	HT_MCP_RXD11_P	HT_MCP_TXD11_P	AE23	NB0CADOUT11
CPUCADOUTJ11	AK13	HT_MCP_RXD11_N	HT_MCP_TXD11_N	AD21	NB0CADOUT12
CPUCADOUT12	AC15	HT_MCP_RXD12_P	HT_MCP_TXD12_P	AE21	NB0CADOUT12
CPUCADOUTJ12	AD15	HT_MCP_RXD12_N	HT_MCP_TXD12_N	AF21	NB0CADOUT13
CPUCADOUT13	AD18	HT_MCP_RXD13_P	HT_MCP_TXD13_P	AG21	NB0CADOUT13
CPUCADOUTJ13	AE18	HT_MCP_RXD13_N	HT_MCP_TXD13_N	AC20	NB0CADOUT14
CPUCADOUT14	AE17	HT_MCP_RXD14_P	HT_MCP_TXD14_P	AD20	NB0CADOUT14
CPUCADOUTJ14	AD17	HT_MCP_RXD14_N	HT_MCP_TXD14_N	AE19	NB0CADOUT15
CPUCADOUT15	AB17	HT_MCP_RXD15_P	HT_MCP_TXD15_P	AE19	NB0CADOUT15
CPUCADOUTJ15	AC17	HT_MCP_RXD15_N	HT_MCP_TXD15_N	AE19	NB0CADOUT15

HT

3 CPUHTTCLKOUT0 >>> CPUHTTCLKOUT0 AJ17 HT\_MCP\_RX\_CLK0\_P  
 3 CPUHTTCLKOUTJ0 >>> CPUHTTCLKOUTJ0 AH17 HT\_MCP\_RX\_CLK0\_N  
 3 CPUHTTCLKOUT1 >>> CPUHTTCLKOUT1 AL14 HT\_MCP\_RX\_CLK1\_P  
 3 CPUHTTCLKOUTJ1 >>> CPUHTTCLKOUTJ1 AK14 HT\_MCP\_RX\_CLK1\_N

3 CPUHTTCTLOUT0 >>> CPUHTTCTLOUT0 AH19 HT\_MCP\_RXCTL0\_P  
 3 CPUHTTCTLOUTJ0 >>> CPUHTTCTLOUTJ0 AG19 HT\_MCP\_RXCTL0\_N  
 3 CPUHTTCTLOUT1 >>> CPUHTTCTLOUT1 AC18 RESERVED#AC18  
 3 CPUHTTCTLOUTJ1 >>> CPUHTTCTLOUTJ1 AD18 RESERVED#AD18

5 CPU\_THERMTRIP# >>> THERMTRIP#/GPIO\_58 AC13  
 5 THRM# >>> PROCHOT#/GPIO\_20 AB13

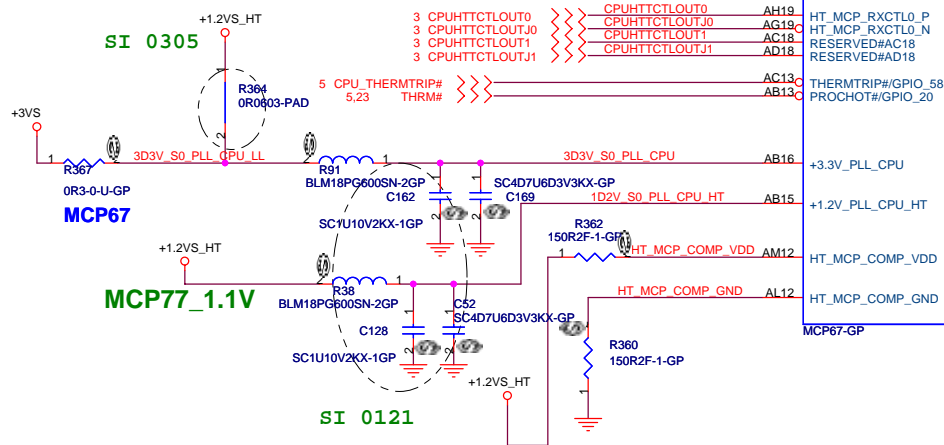
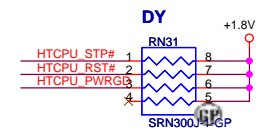
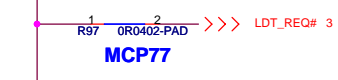
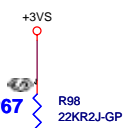
HT\_MCP\_TX\_CLK0\_P >>> NB0HTTCLKOUT0 AK23 NB0HTTCLKOUT0  
 HT\_MCP\_TX\_CLK0\_N >>> NB0HTTCLKOUTJ0 AJ23 NB0HTTCLKOUTJ0  
 HT\_MCP\_TX\_CLK1\_P >>> NB0HTTCLKOUT1 AG23 NB0HTTCLKOUT1  
 HT\_MCP\_TX\_CLK1\_N >>> NB0HTTCLKOUTJ1 AH23 NB0HTTCLKOUTJ1

HT\_MCP\_TXCTL0\_P >>> NB0HTTCTLOUT0 AK20 NB0HTTCTLOUT0  
 HT\_MCP\_TXCTL0\_N >>> NB0HTTCTLOUTJ0 AJ20 NB0HTTCTLOUTJ0  
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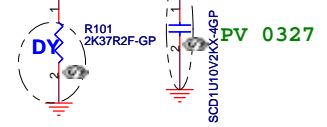
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 HT\_MCP\_STOP# >>> HT\_CPU\_STOP# CAB20 HT\_CPU\_STOP#  
 HT\_MCP\_RST# >>> HT\_CPU\_RST# AC21 HT\_CPU\_RST#  
 HT\_MCP\_PWRGD >>> HT\_CPU\_PWRGD L AD22 HT\_CPU\_PWRGD L

CLKOUT\_200MHZ\_P >>> CLKCPU\_C51 AL28 CLKCPU\_C51  
 CLKOUT\_200MHZ\_N >>> CLKCPU# C51 AM28 CLKCPU# C51

CLKOUT\_25MHZ >>> TPAD28 AK28 CLKOUT\_25MHZ  
 CPU\_SBVREF >>> MCP\_CPU\_SBVREF AG28 MCP\_CPU\_SBVREF  
 CLK200\_TERM\_GND >>> TPAD28 AJ28 CLK200\_TERM\_GND



SI 0313



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(1/8) HT CPU**

Size: A3 Document Number: **SA** Rev: **SA**

Date: Monday, June 09, 2008 Sheet: 9 of 44

D

D

C

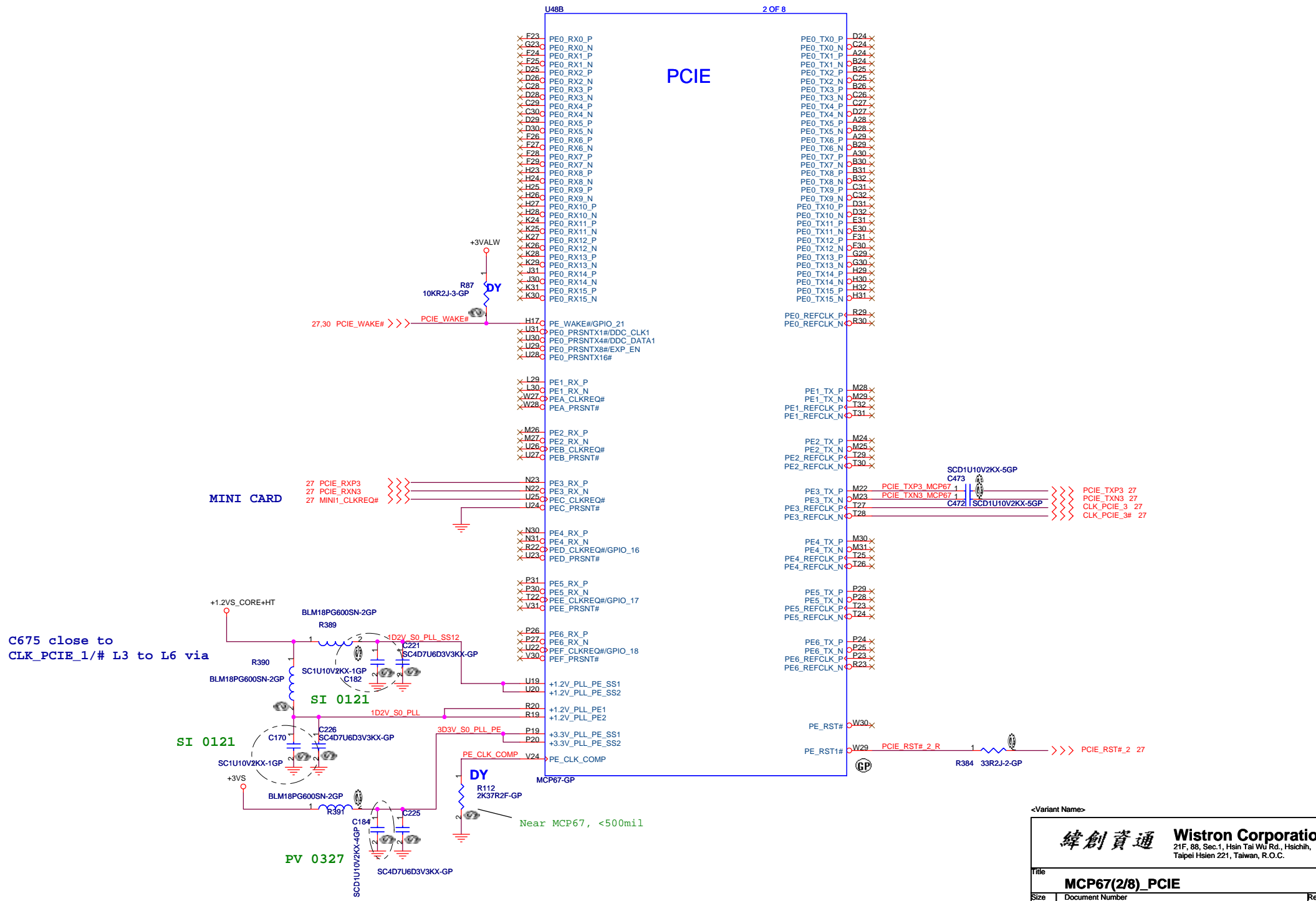
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B

B

A

A

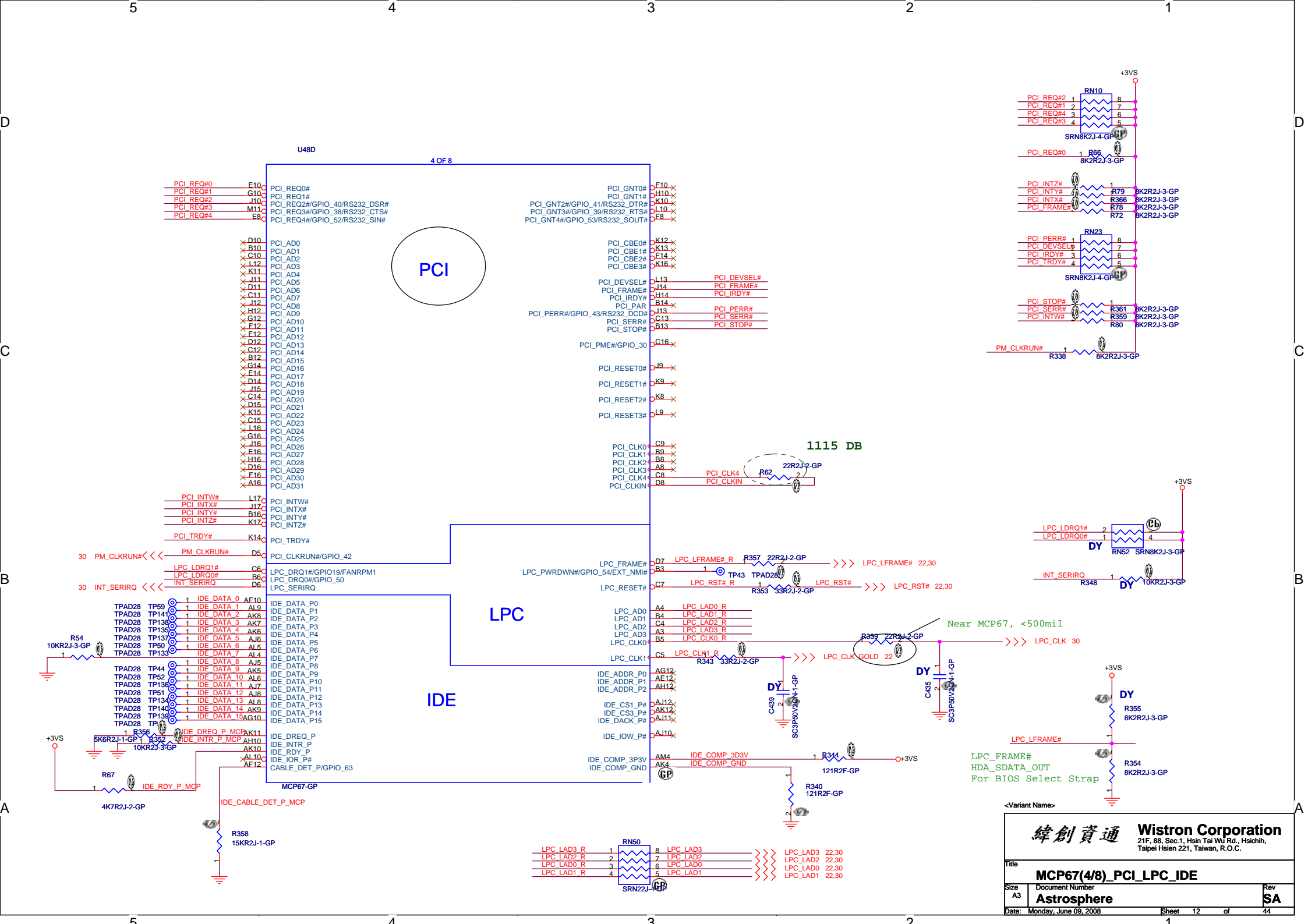


<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title <b>MCP67(2/8)_PCIE</b>		
Size A3	Document Number <b>Astrosphere</b>	Rev <b>SA</b>
Date: Monday, June 09, 2008	Sheet 10	of 44





PCI\_REQ#0 F10C  
 PCI\_REQ#1 G10C  
 PCI\_REQ#2 J10C  
 PCI\_REQ#3 M11C  
 PCI\_REQ#4 E8C

>D10 PCI\_AD0  
 >B10 PCI\_AD1  
 >C10 PCI\_AD2  
 >L12 PCI\_AD3  
 >K11 PCI\_AD4  
 >J11 PCI\_AD5  
 >C11 PCI\_AD6  
 >C11 PCI\_AD7  
 >J12 PCI\_AD8  
 >H12 PCI\_AD9  
 >G12 PCI\_AD10  
 >F12 PCI\_AD11  
 >E12 PCI\_AD12  
 >D12 PCI\_AD13  
 >C12 PCI\_AD14  
 >B12 PCI\_AD15  
 >G14 PCI\_AD16  
 >E14 PCI\_AD17  
 >D14 PCI\_AD18  
 >J15 PCI\_AD19  
 >G14 PCI\_AD20  
 >D15 PCI\_AD21  
 >K15 PCI\_AD22  
 >C15 PCI\_AD23  
 >L16 PCI\_AD24  
 >G16 PCI\_AD25  
 >I16 PCI\_AD26  
 >E16 PCI\_AD27  
 >H16 PCI\_AD28  
 >D16 PCI\_AD29  
 >F16 PCI\_AD30  
 >A16 PCI\_AD31

PCI\_INTW# L17C  
 PCI\_INTX# J17C  
 PCI\_INTY# B16C  
 PCI\_INTZ# K17C

PCI\_TRDY# K14C  
 PM\_CLKRUN# D5C

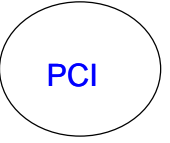
LPC\_LDRQ1# C6C  
 LPC\_LDRQ0# B6C  
 INT\_SERIRQ D6C

TPAD28 TP59 1 IDE\_DATA\_0 AE10  
 TPAD28 TP141 1 IDE\_DATA\_1 AL9  
 TPAD28 TP138 1 IDE\_DATA\_2 AK9  
 TPAD28 TP135 1 IDE\_DATA\_3 AK7  
 TPAD28 TP137 1 IDE\_DATA\_4 AK6  
 TPAD28 TP50 1 IDE\_DATA\_5 AL5  
 TPAD28 TP133 1 IDE\_DATA\_6 AL4  
 TPAD28 TP44 1 IDE\_DATA\_7 AL4  
 TPAD28 TP52 1 IDE\_DATA\_8 AJ5  
 TPAD28 TP136 1 IDE\_DATA\_9 AK5  
 TPAD28 TP137 1 IDE\_DATA\_10 AL6  
 TPAD28 TP136 1 IDE\_DATA\_11 AJ7  
 TPAD28 TP51 1 IDE\_DATA\_12 AL5  
 TPAD28 TP134 1 IDE\_DATA\_13 AL5  
 TPAD28 TP140 1 IDE\_DATA\_14 AK9  
 TPAD28 TP139 1 IDE\_DATA\_15 AG10  
 TPAD28 TP139 1 IDE\_DATA\_15 AG10

IDE\_DREQ\_P MCPAK11  
 IDE\_INTR\_P MCP AH10  
 IDE\_INTR\_P MCP AH10  
 IDE\_RDY\_P AL10  
 IDE\_IOR\_P# AE12

IDE\_RDY\_P MCP  
 IDE\_CABLE\_DET\_P MCP

R358 15KR2J-1-GP



PCI\_GNT0# E10  
 PCI\_GNT1# H10  
 PCI\_GNT2#/GPIO\_41/RS232\_DTR# K10  
 PCI\_GNT3#/GPIO\_39/RS232\_RTS# L10  
 PCI\_GNT4#/GPIO\_53/RS232\_SOUT# F8

PCI\_CBE0# OK12  
 PCI\_CBE1# OK13  
 PCI\_CBE2# E14  
 PCI\_CBE3# OK16

PCI\_DEVSEL# L13  
 PCI\_FRAME# J14  
 PCI\_IRDY# B14

PCI\_PERR#/GPIO\_43/RS232\_DDM# J13  
 PCI\_SERR# C13  
 PCI\_STOP# B13

PCI\_PME#/GPIO\_30 C16

PCI\_RESET0# J9  
 PCI\_RESET1# K9  
 PCI\_RESET2# K8  
 PCI\_RESET3# L9

PCI\_CLK0# C9  
 PCI\_CLK1# B8  
 PCI\_CLK2# B8  
 PCI\_CLK3# A8  
 PCI\_CLK4# C8  
 PCI\_CLKIN# D8

LPC\_FRAME# D7  
 LPC\_PWRDWN#/GPIO\_54/EXT\_NMI# B3  
 LPC\_RESET# C7

LPC\_AD0 A4  
 LPC\_AD1 B4  
 LPC\_AD2 C4  
 LPC\_AD3 A3  
 LPC\_AD4 B5

LPC\_AD5 A4  
 LPC\_AD6 B4  
 LPC\_AD7 C4  
 LPC\_AD8 A3  
 LPC\_AD9 B5

LPC\_AD10 A4  
 LPC\_AD11 B4  
 LPC\_AD12 C4  
 LPC\_AD13 A3  
 LPC\_AD14 B5

LPC\_AD15 A4  
 LPC\_AD16 B4  
 LPC\_AD17 C4  
 LPC\_AD18 A3  
 LPC\_AD19 B5

LPC\_AD20 A4  
 LPC\_AD21 B4  
 LPC\_AD22 C4  
 LPC\_AD23 A3  
 LPC\_AD24 B5

LPC\_AD25 A4  
 LPC\_AD26 B4  
 LPC\_AD27 C4  
 LPC\_AD28 A3  
 LPC\_AD29 B5

LPC\_AD30 A4  
 LPC\_AD31 B4

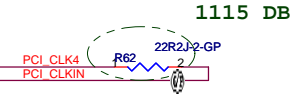
IDE\_COMP\_3P3V AM4  
 IDE\_COMP\_GND AK4

LPC\_LAD3 R RN50  
 LPC\_LAD2 R 2  
 LPC\_LAD0 R 3  
 LPC\_LAD1 R 4

LPC\_LAD3 22.30  
 LPC\_LAD2 22.30  
 LPC\_LAD0 22.30  
 LPC\_LAD1 22.30

PCI\_DEVSEL# L13  
 PCI\_FRAME# J14  
 PCI\_IRDY# B14

PCI\_PERR# J13  
 PCI\_SERR# C13  
 PCI\_STOP# B13



LPC\_LFRAME# R R357 22R2J-2-GP >>> LPC\_LFRAME# 22.30  
 LPC\_RST# R TP43 TPAD28 R353 33R2J-2-GP >>> LPC\_RST# 22.30

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

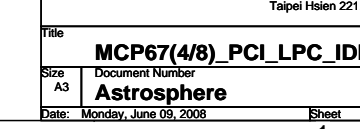
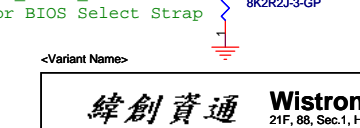
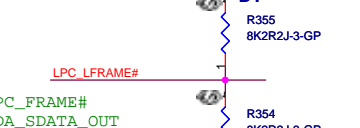
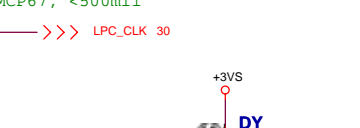
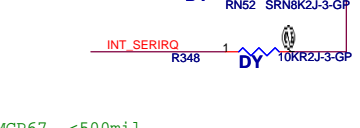
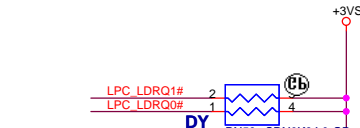
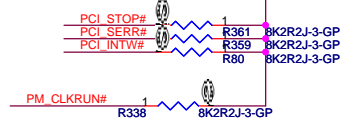
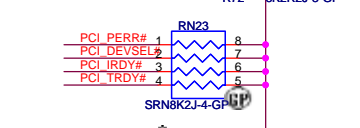
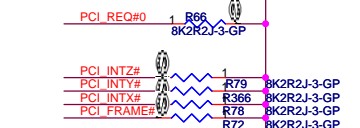
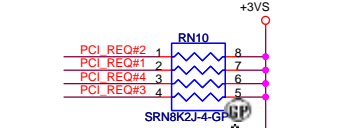
LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22

LPC\_CLK# R R343 33R2J-2-GP >>> LPC\_CLK# GOLD 22



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsien 221, Taiwan, R.O.C.

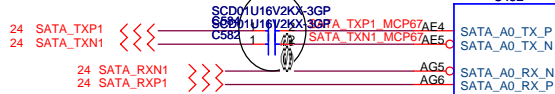
Title: **MCP67(4/8)\_PCI\_LPC\_IDE**

Size: A3 Document Number: **Astrosphere** Rev: SA

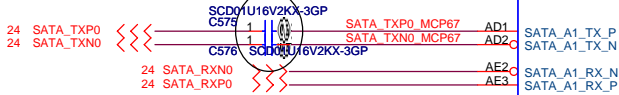
Date: Monday, June 09, 2008 Sheet: 12 of 44

If no 1394  
Port 0 for NVidia Win-debug

place near MCP67



place near MCP67



U48E 5 OF 8

SATA

USB

Single USB

CARD READER

Bluetooth

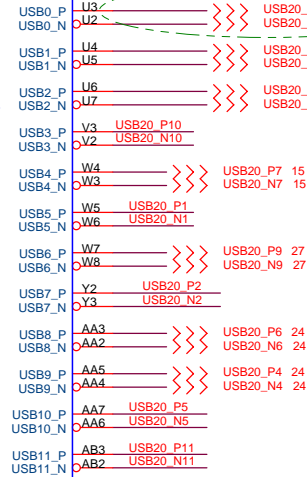
Camera

MINI CARD

USB2

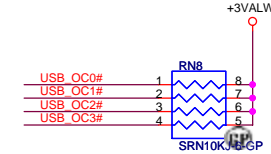
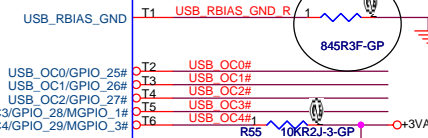
USB1

HDA



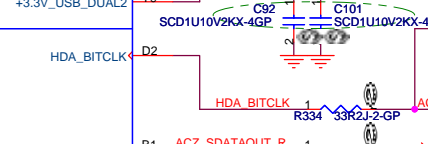
SI 0317

Only MCP77  
1.1K on MCP67



PV 0327

Check this NEW\_OC#

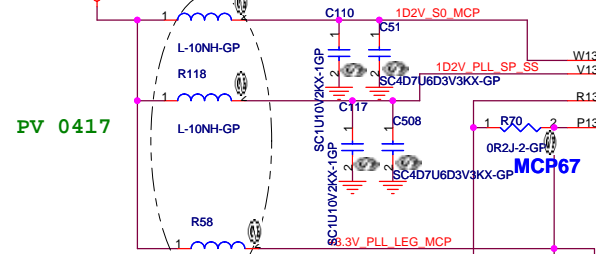


SI 1217

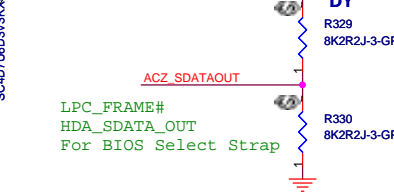
MCP77\_ 1.1V



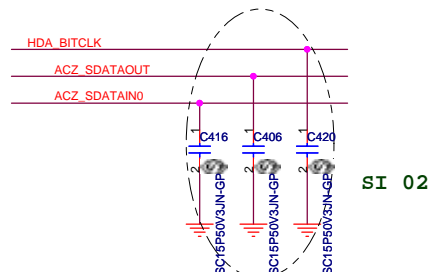
PV 0417



SI 0303



SI 0227



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

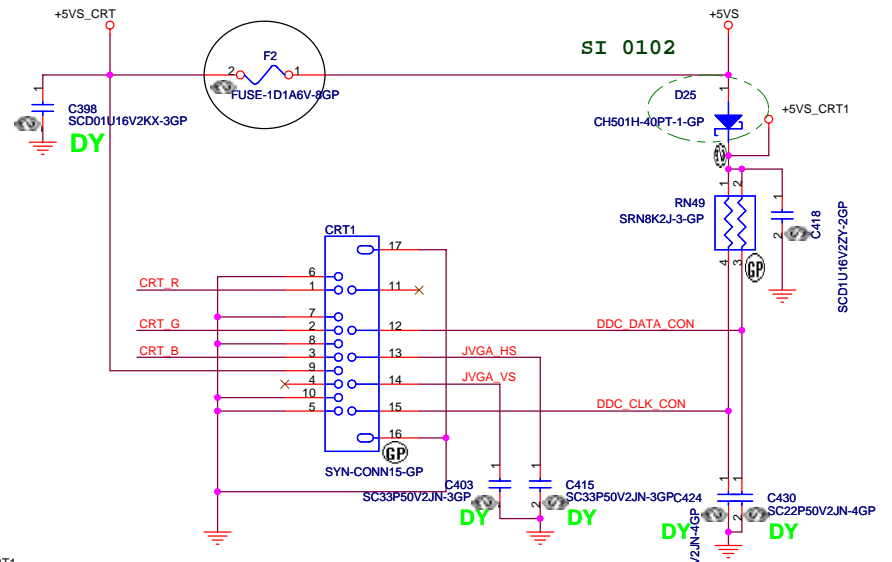
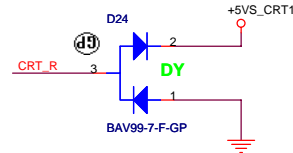
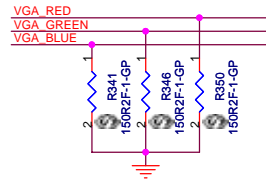
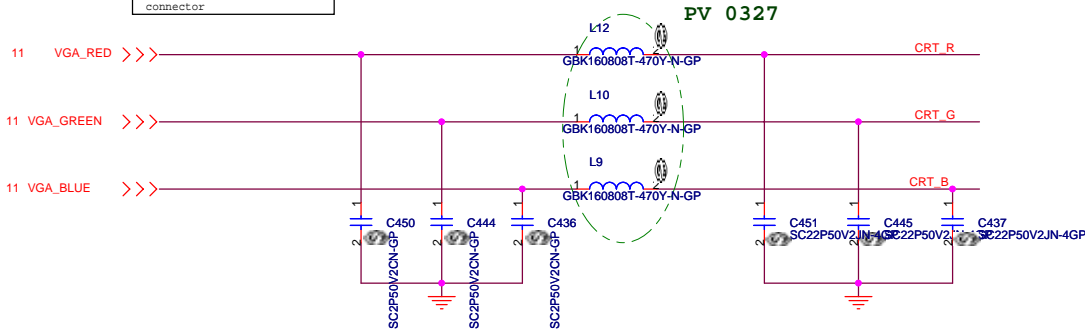
Title  
**MCP67(5/8)\_SATA\_USB\_HDA**

Size A3 Document Number  
**Atmosphere** Rev SA

Date: Monday, June 09, 2008 Sheet 13 of 44

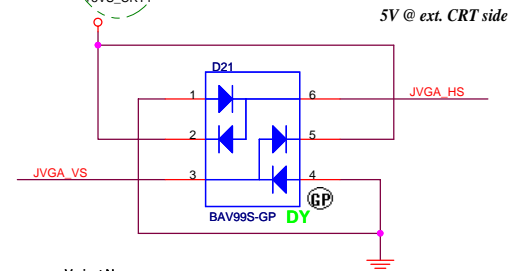
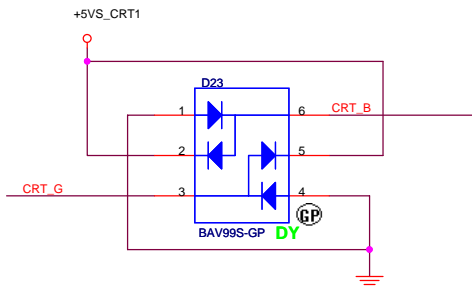
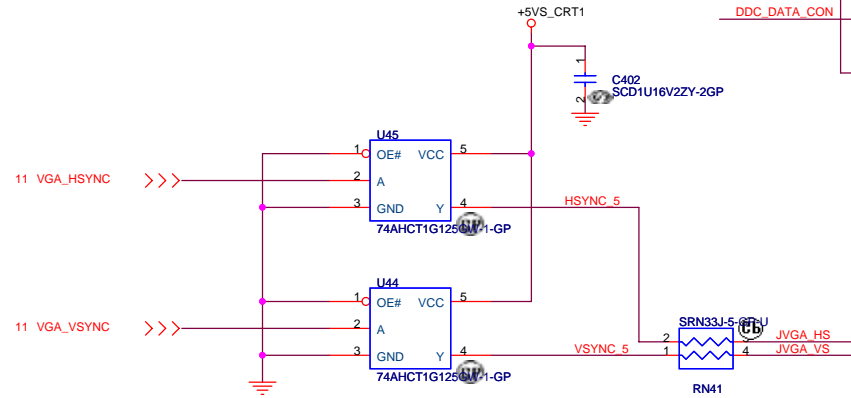
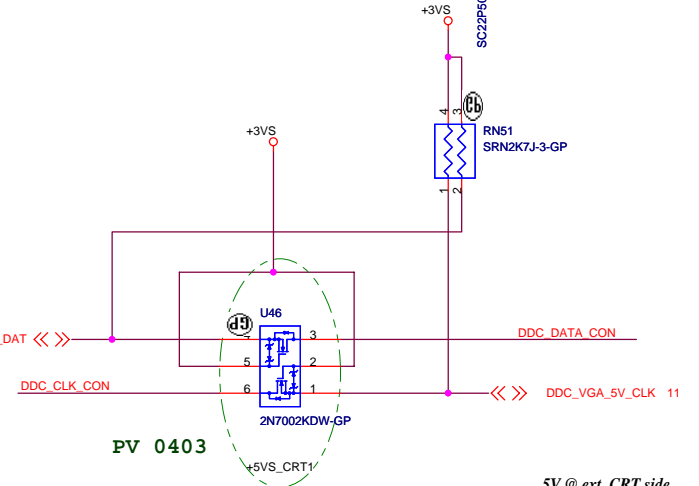
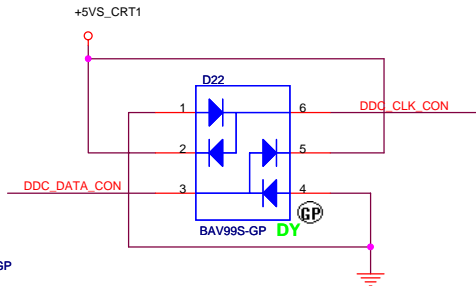
# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector



**Layout Note:**

\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV CONNECTOR**

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Date: Monday, June 09, 2008	<b>Astrosphere</b>	<b>SA</b>
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<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title **Board to board conn/ Docking**

Size A3	Document Number <b>Astrosphere</b>	Rev <b>SA</b>
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A

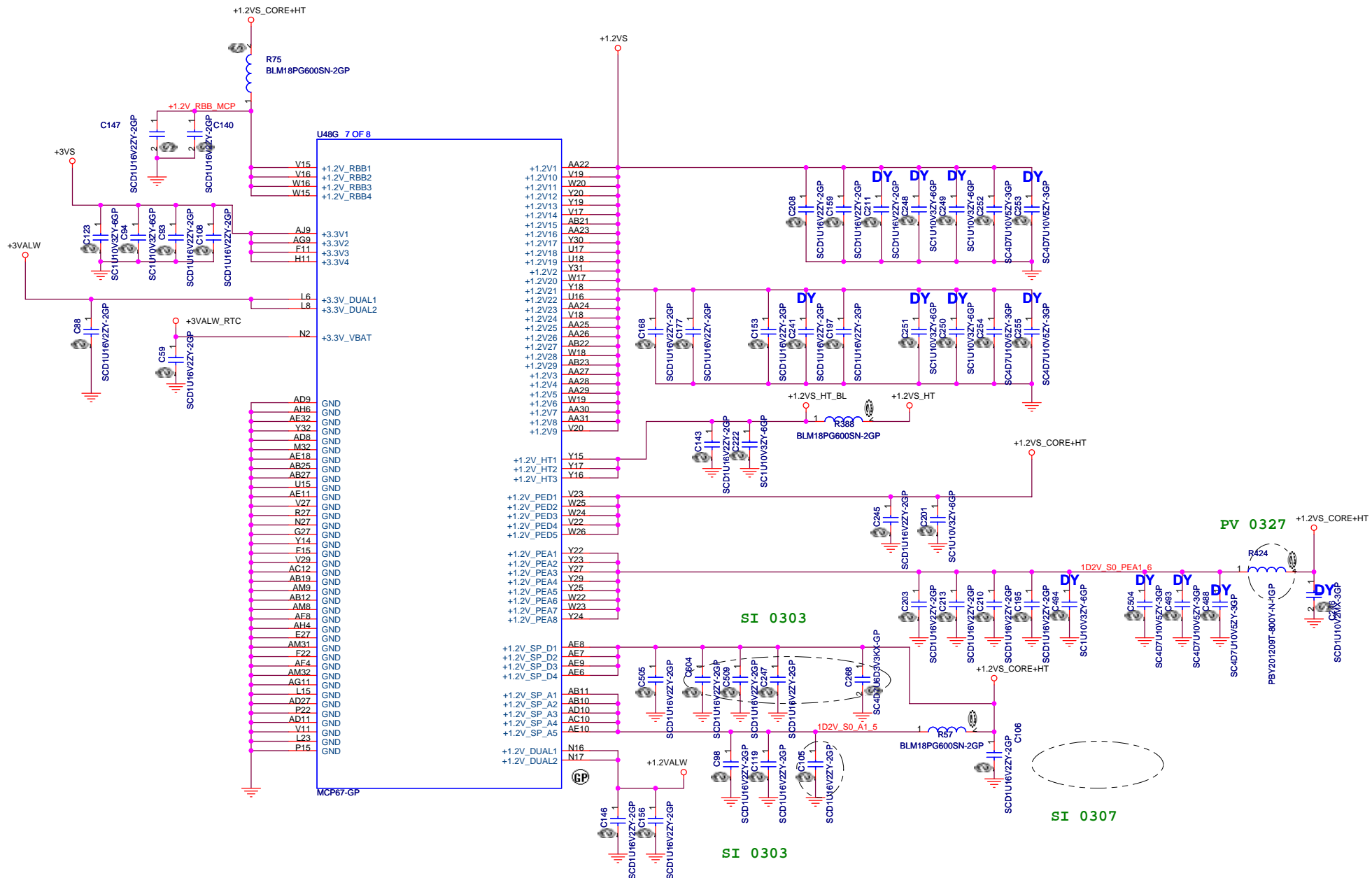
B

C

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E





<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

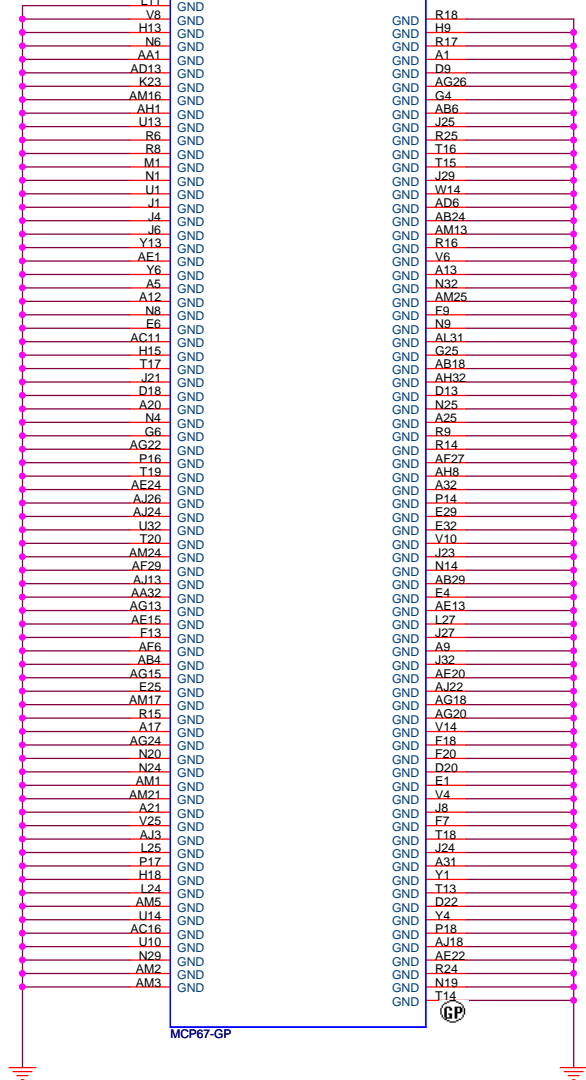
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Size: A3 Document Number: **Astrosphere** Rev: SA

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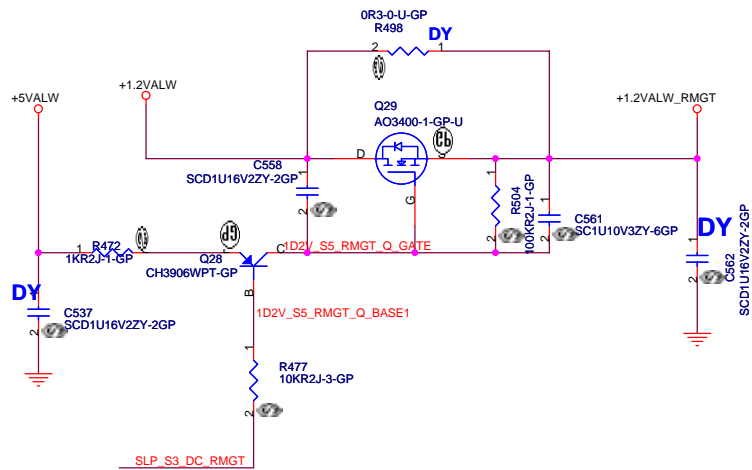
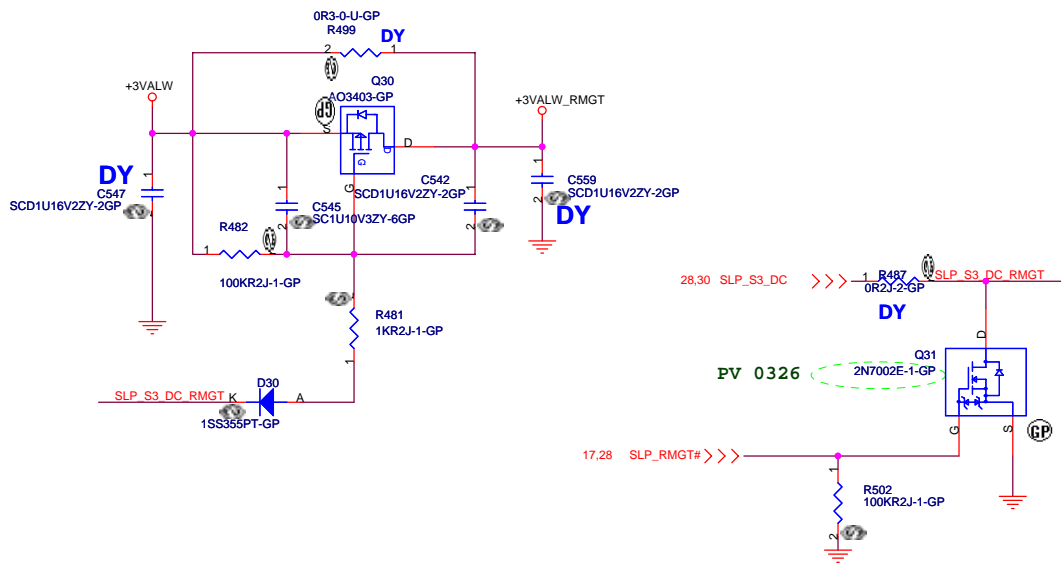
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<del>AC6</del>	RESERVED#AC6	RESERVED#AB8	<del>AB8</del>
<del>AC8</del>	RESERVED#AC8	RESERVED#V9	<del>V9</del>
<del>AA8</del>	RESERVED#AA8	RESERVED#W11	<del>W11</del>
<del>AD3</del>	RESERVED#AD3	RESERVED#W10	<del>W10</del>
<del>AD4</del>	RESERVED#AD4	RESERVED#W9	<del>W9</del>
<del>AA9</del>	RESERVED#AA9	RESERVED#Y11	<del>Y11</del>
<del>AC5</del>	RESERVED#AC5	RESERVED#Y10	<del>Y10</del>
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		RESERVED#AA10	<del>AA10</del>



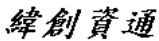
<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>MCP67(8/8)_GND</b>			
Size	Document Number	Date:	Rev
A3	<b>Astrosphere</b>	Monday, June 09, 2008	<b>SA</b>
		Sheet	of
		19	44

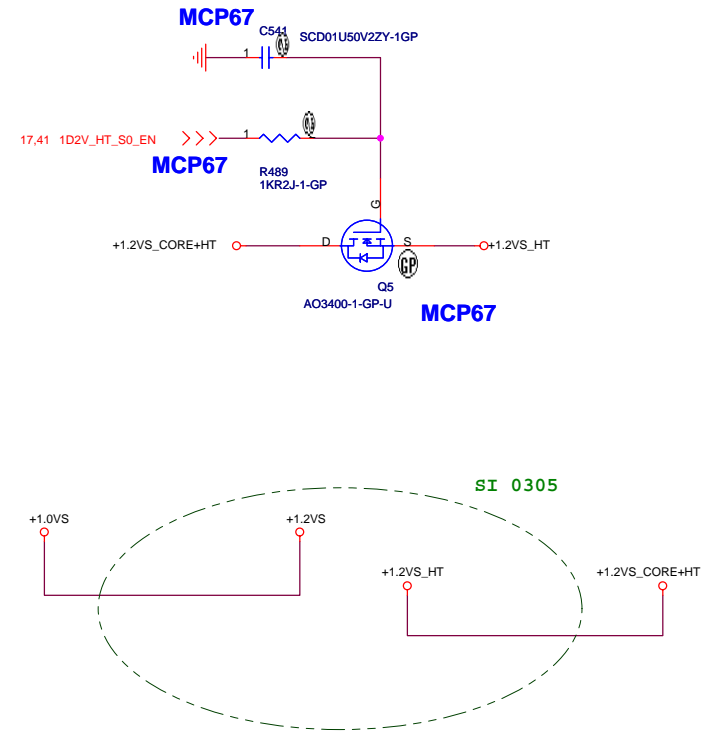




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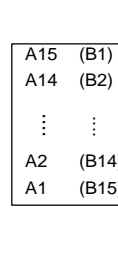
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Title	
Size A3	Document Number <b>Astrosphere</b>
Date: Monday, June 09, 2008	Rev <b>SA</b>
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MCP67



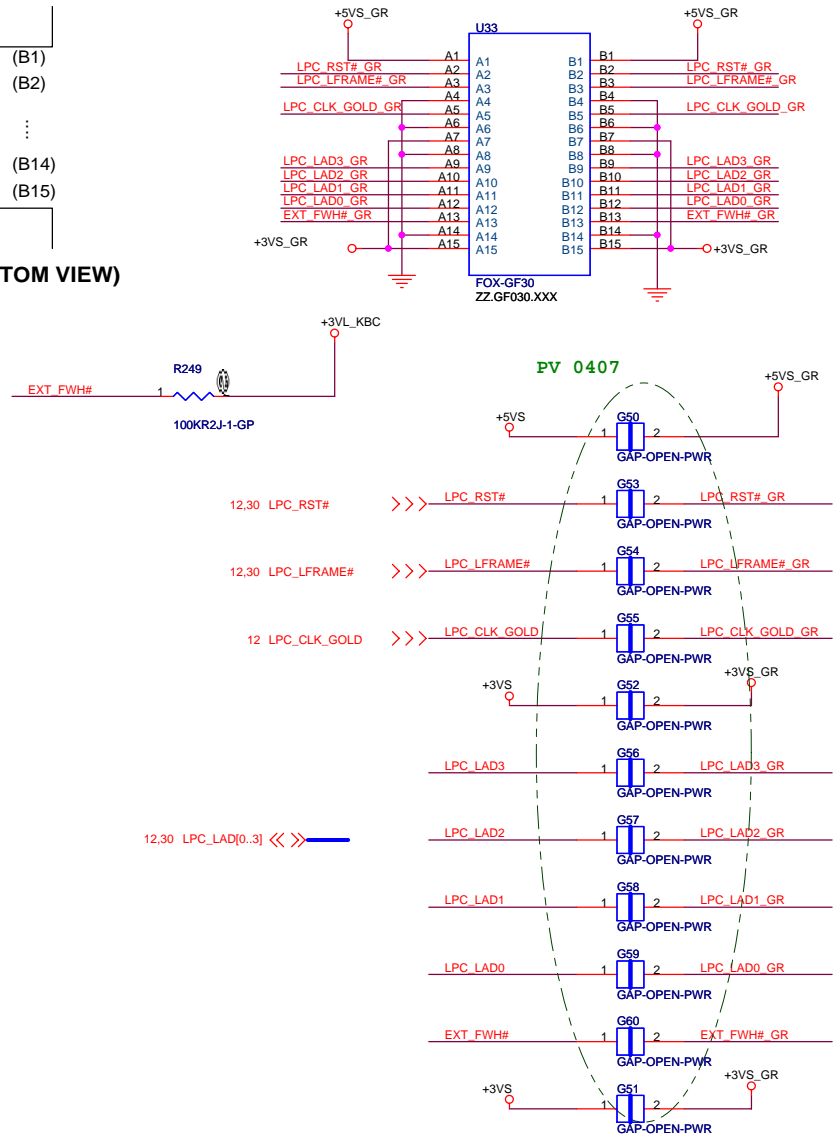
MCP77

TOP VIEW



(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

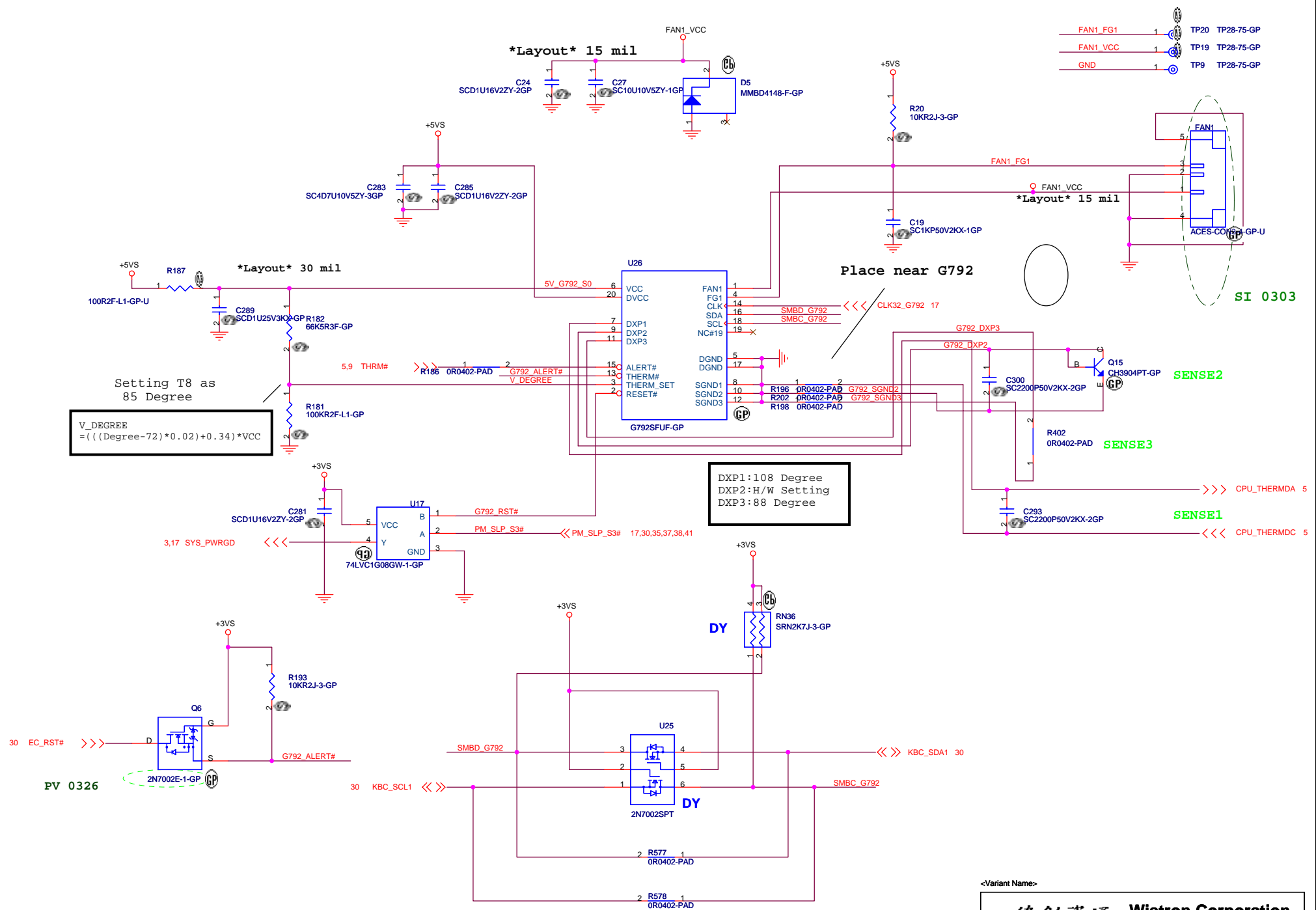


Put near board edge

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>POWER PATH</b>			
Size	Document Number	Rev	
A3		<b>SA</b>	
Date: Monday, June 09, 2008		Sheet	22 of 44





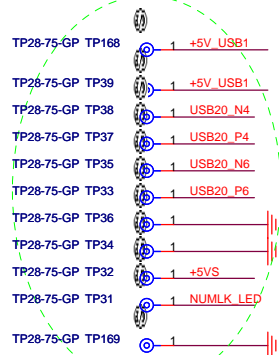
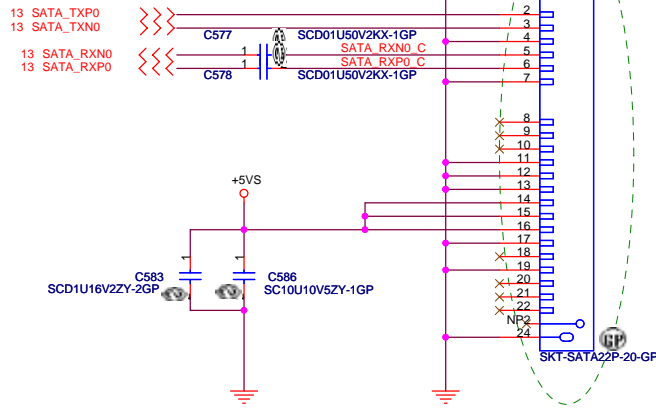
Setting T8 as 85 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

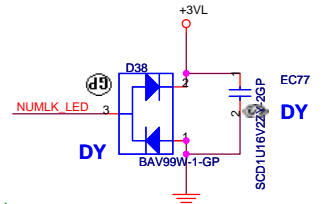
DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

# SATA HD Connector

PV 0407

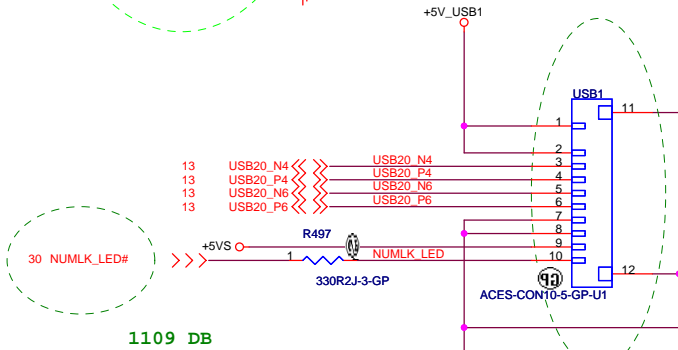
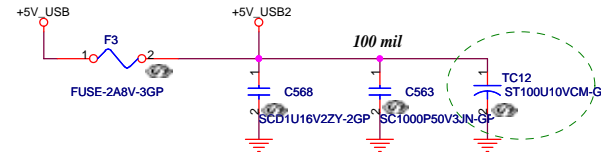


1115 DB  
Close to USB1



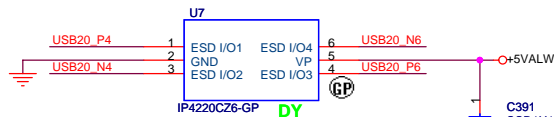
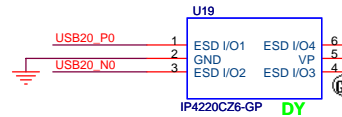
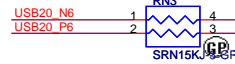
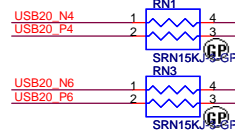
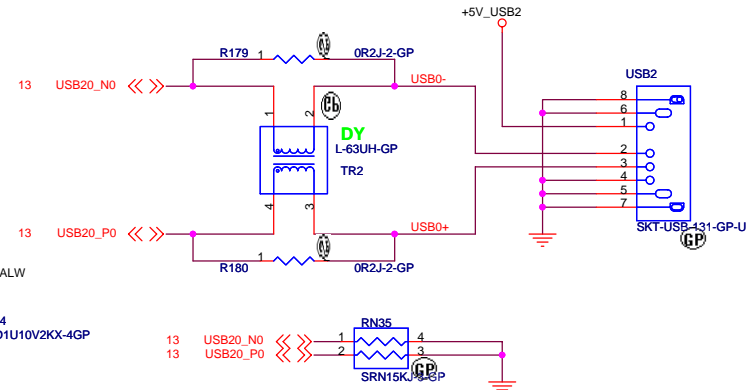
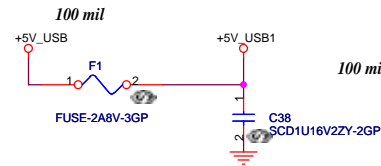
# USB PORT

SI 0102

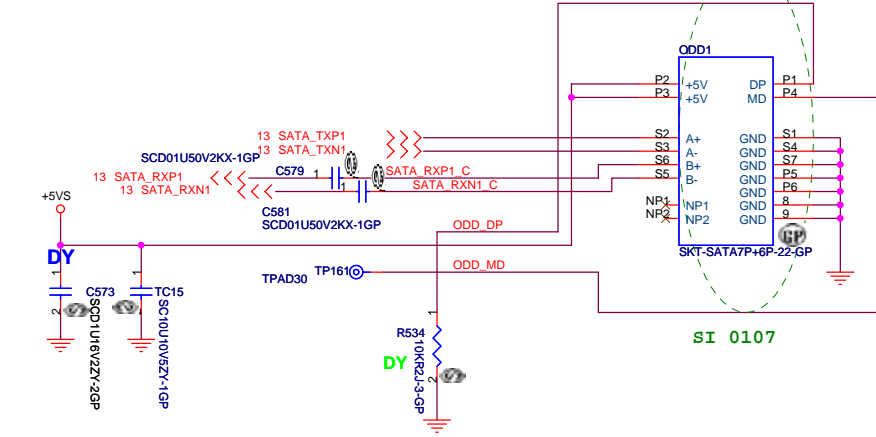


1109 DB

1112 DB



# ODD Connector



SI 0107

<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HD/CDROM	
Size	Document Number	Rev
A3	Astrosphere	SA
Date:	Monday, June 09, 2008	Sheet 24 of 44



A

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<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**R5C832/IEEE1394/SD**

Size  
A3

Document Number

**Astrosphere**

Rev

**SA**

Date: Monday, June 09, 2008

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A

B

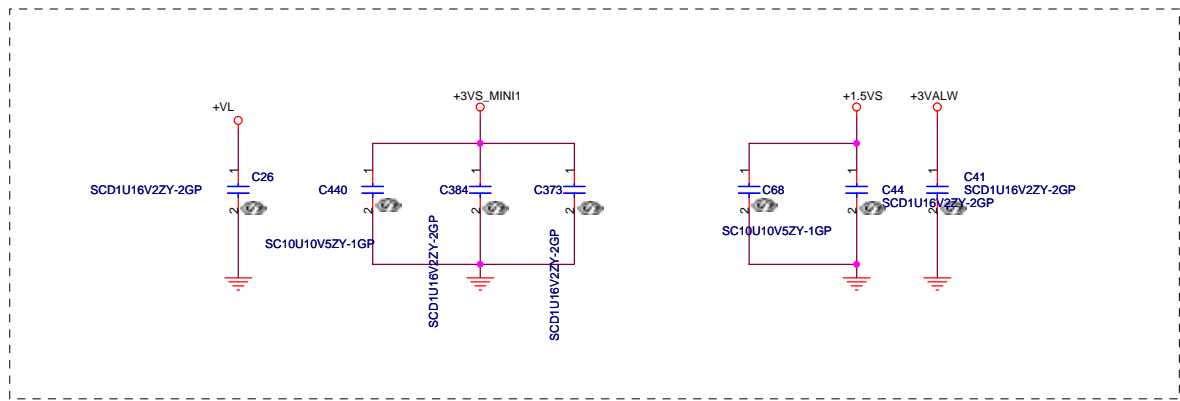
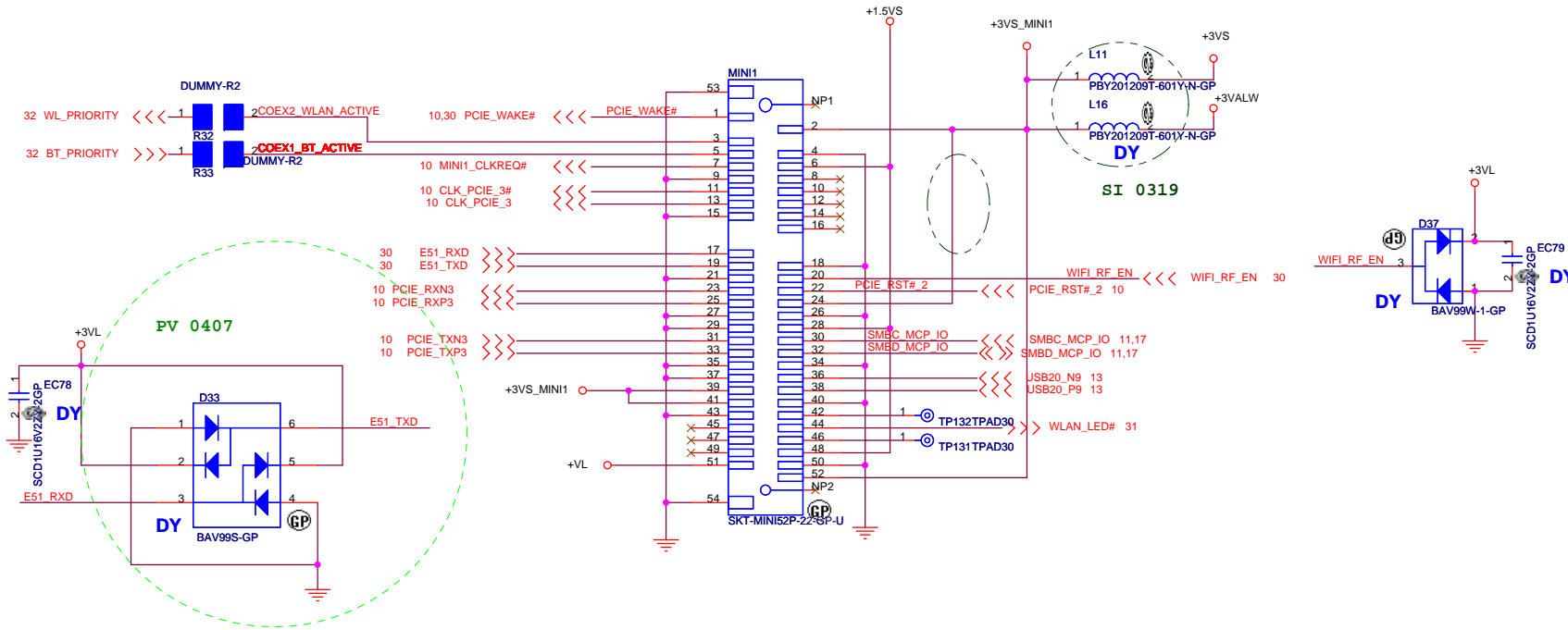
C

D

E

# Mini Card Connector 1

Wireless Card



<Variant Name>

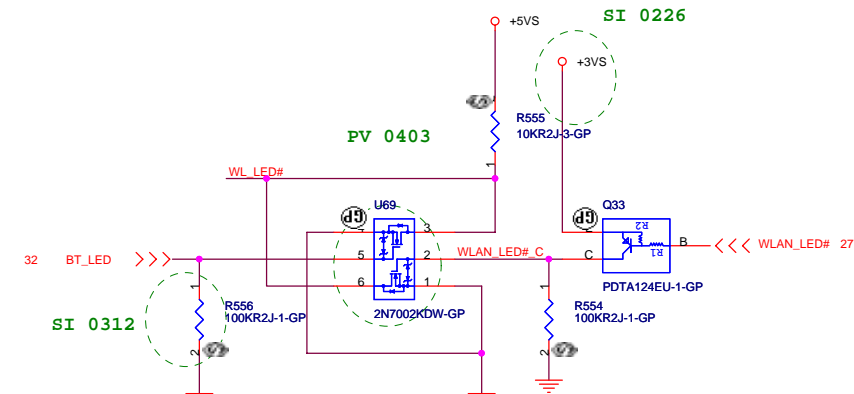
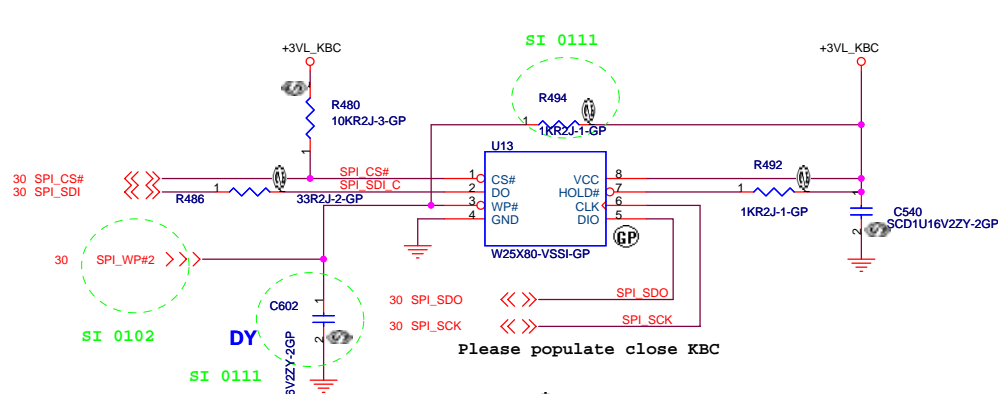
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<b>MINI CARD CONN .</b>	
Title	Rev
Size A3	SA
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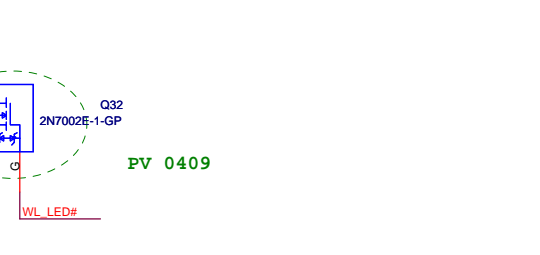
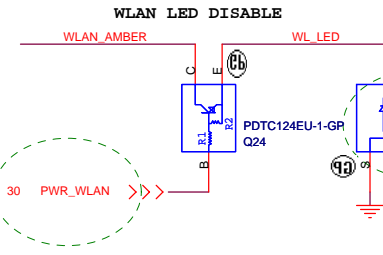
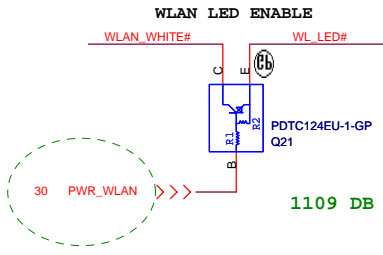




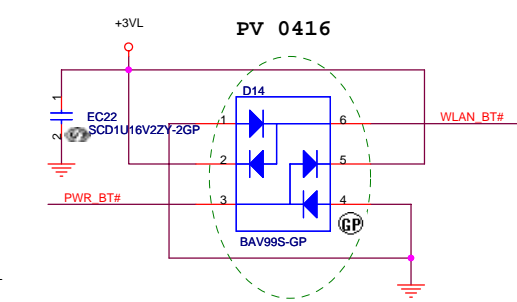
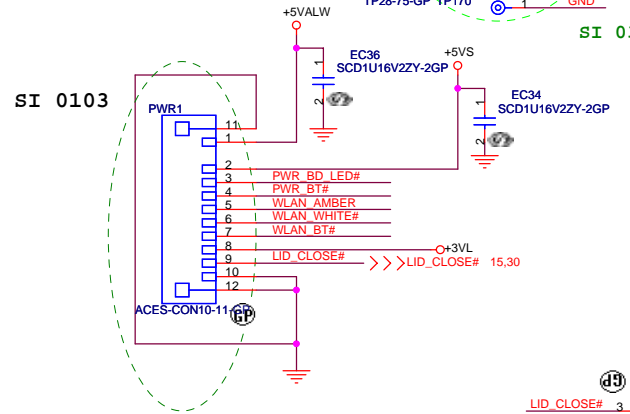




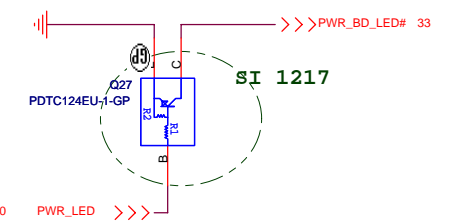
- TP28-75-GP TP26 <--> +5VALW
- TP28-75-GP TP22 <--> +5VS
- TP28-75-GP TP29 <--> PWR\_BD\_LED#
- TP28-75-GP TP24 <--> PWR\_BT#
- TP28-75-GP TP30 <--> WLAN\_AMBER
- TP28-75-GP TP28 <--> WLAN\_WHITE#
- TP28-75-GP TP27 <--> WLAN\_BT#
- TP28-75-GP TP23 <--> LID\_CLOSE#
- TP28-75-GP TP25 <--> +3VL
- TP28-75-GP TP21 <--> GND
- TP28-75-GP TP170 <--> GND



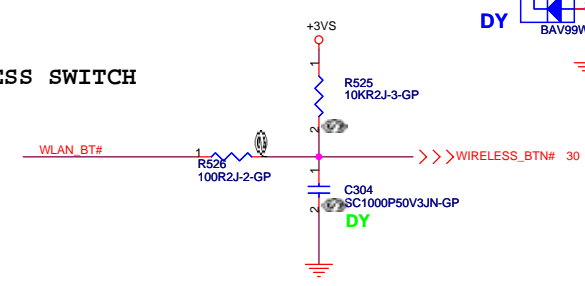
1113 DB  
Close to PWR1



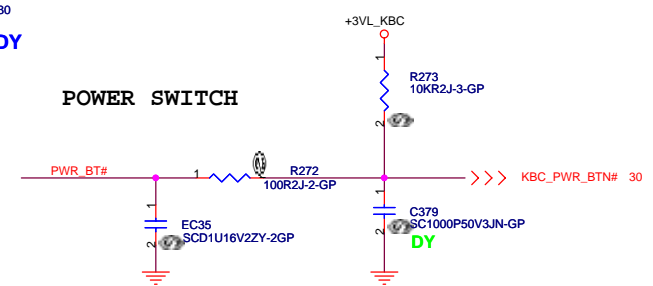
1112 DB



WIRELESS SWITCH



POWER SWITCH



<Variant Name>

**緯創資通 Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **FLASH and Debug**

Size: A3  
Date: Monday, June 09, 2008

Document Number: **Astrosphere**

Rev: **SA**

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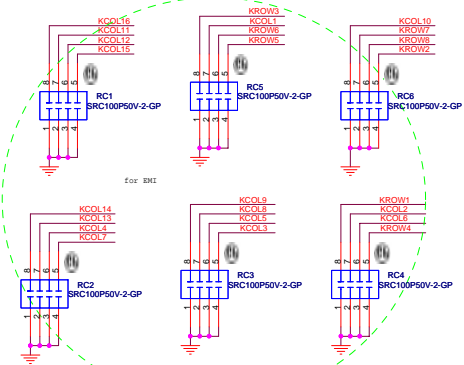
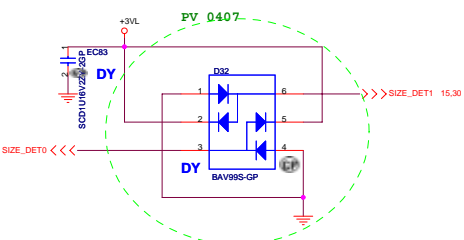
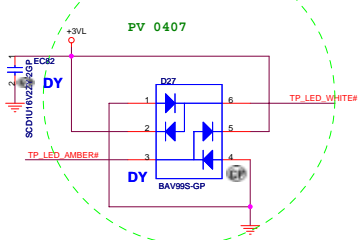
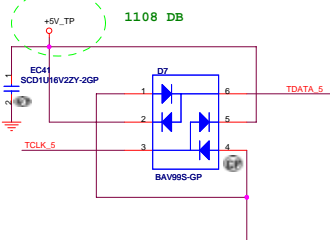
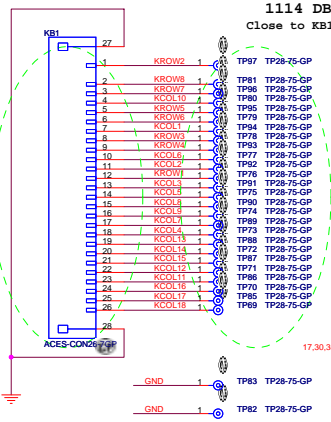
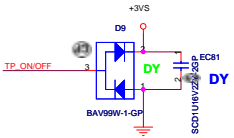
# Internal Keyboard Connector

30 KROW[1..8] <<<< <<<< <<<< <<<<  
 30 KCOL[1..18] <<<< <<<< <<<< <<<<

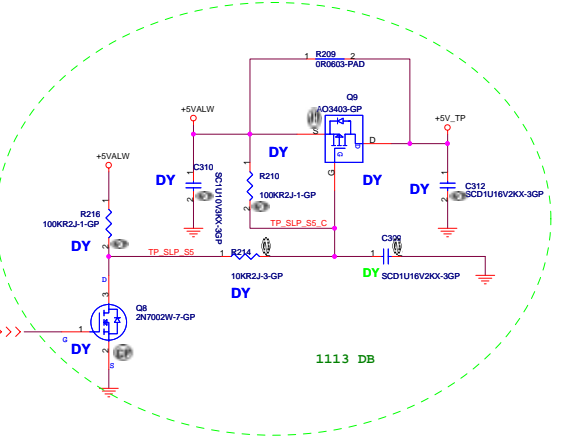
Keyboard matrix ( from vendor )

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

SI 0310

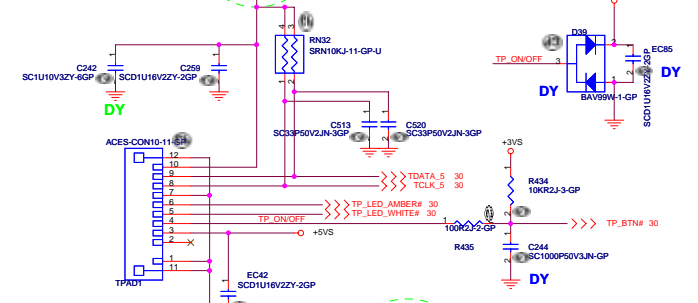


1114 DB  
Close to KB1

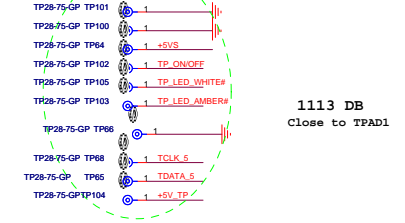


1108 DB

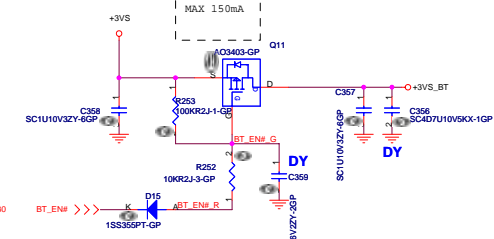
TouchPad Connector



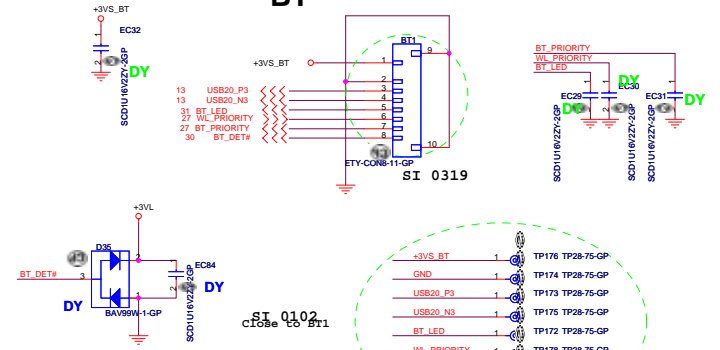
SI 0103



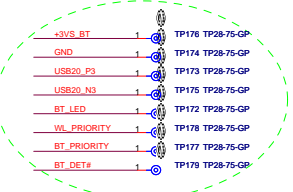
1113 DB  
Close to TPAD1



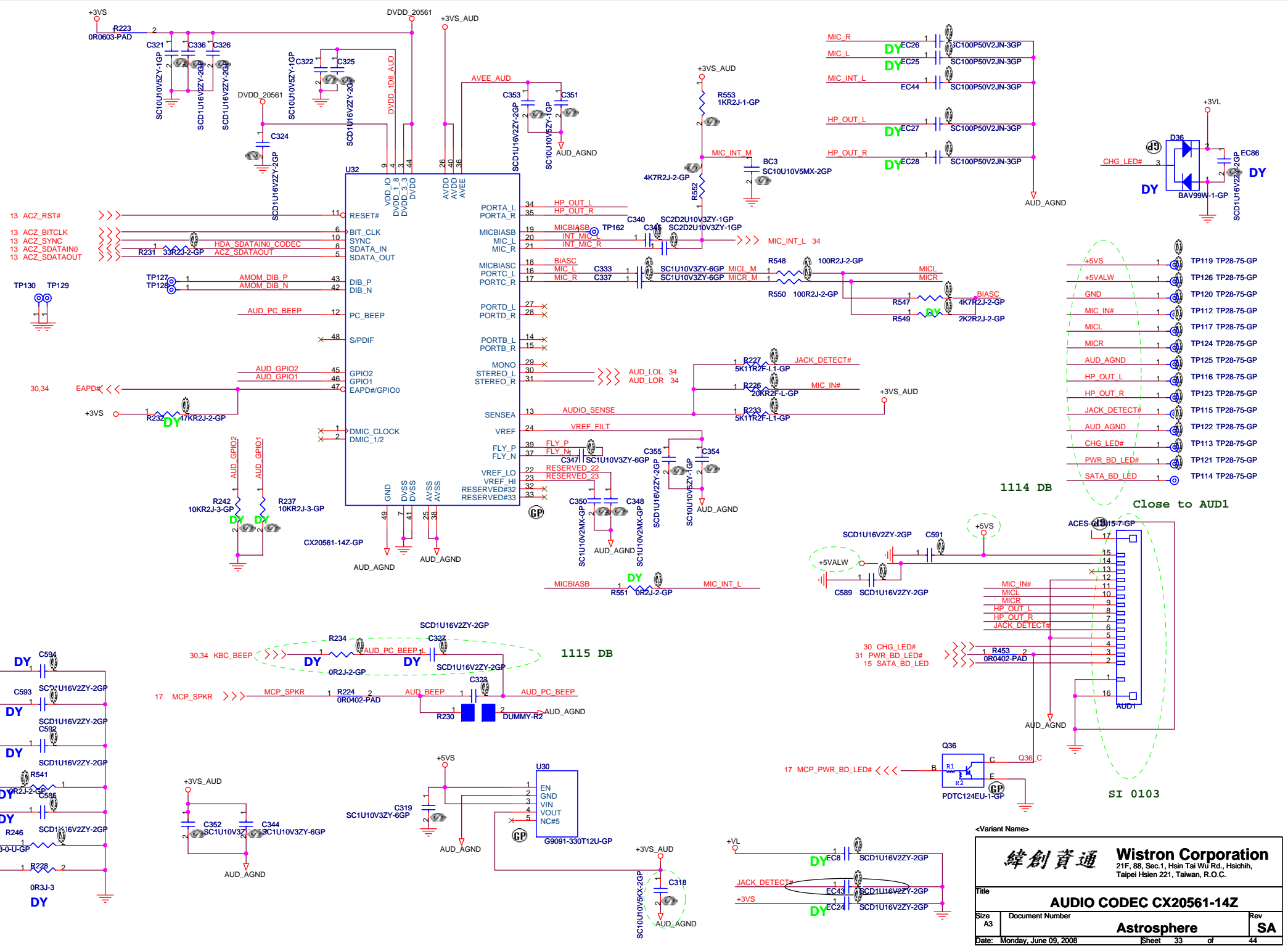
BT



SI 0102  
Close to BT1



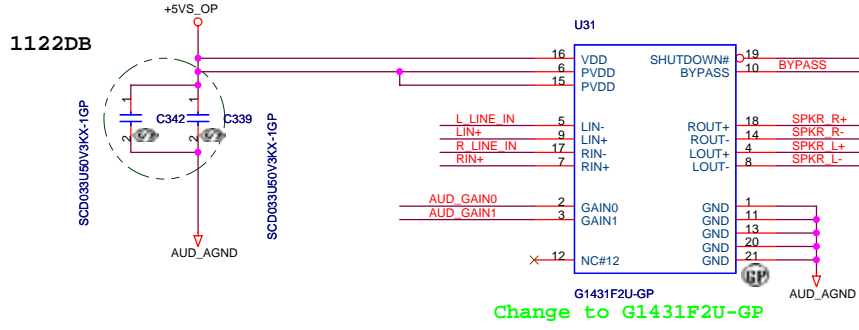
<-Variant Name>



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 Taipei Hsien 221, Taiwan, R.O.C.

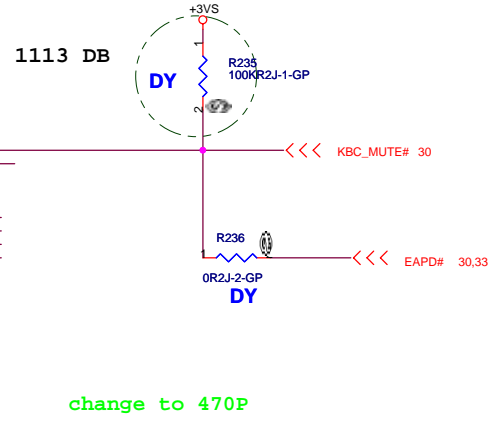
**AUDIO CODEC CX20561-14Z**

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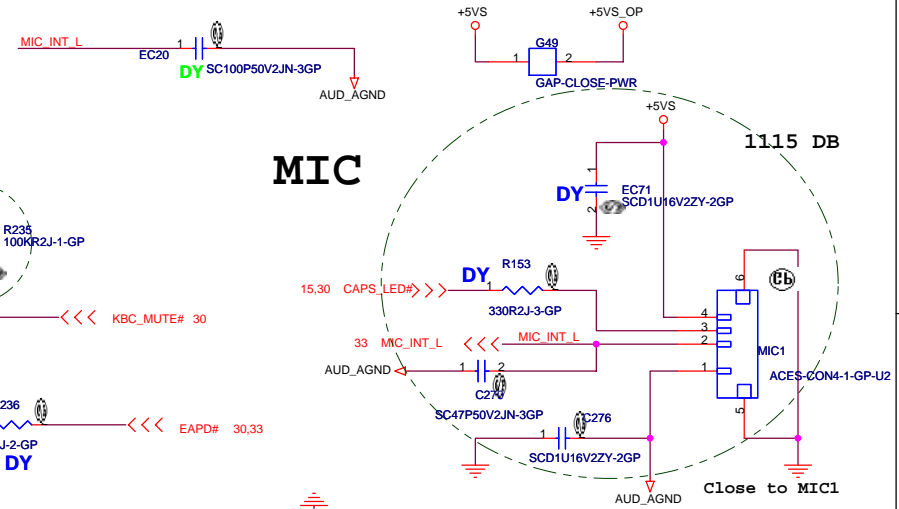
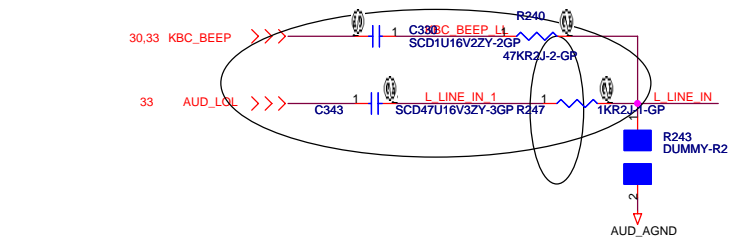
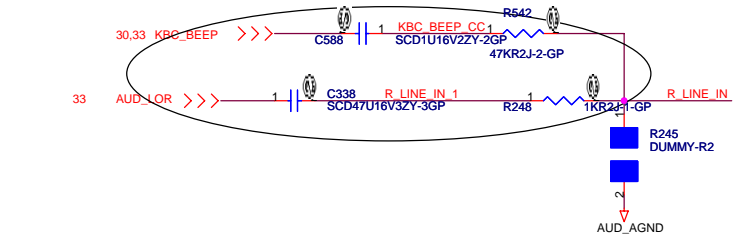
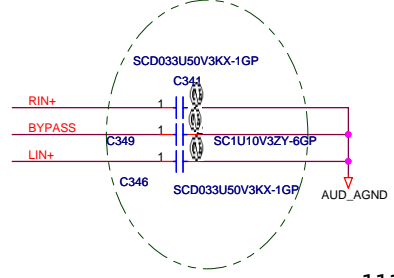


GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

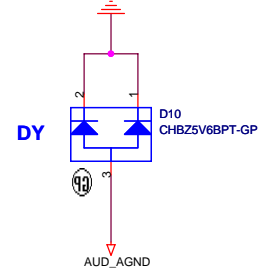
Set to 15.6dB



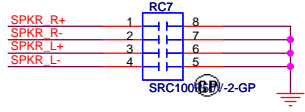
change to 470P



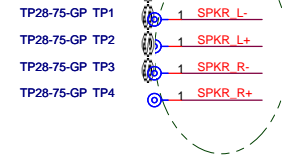
### MIC



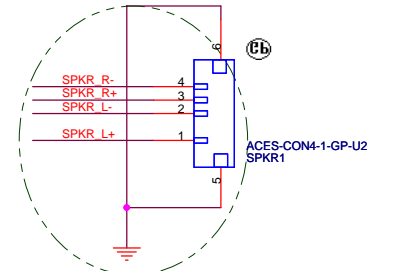
### Speaker



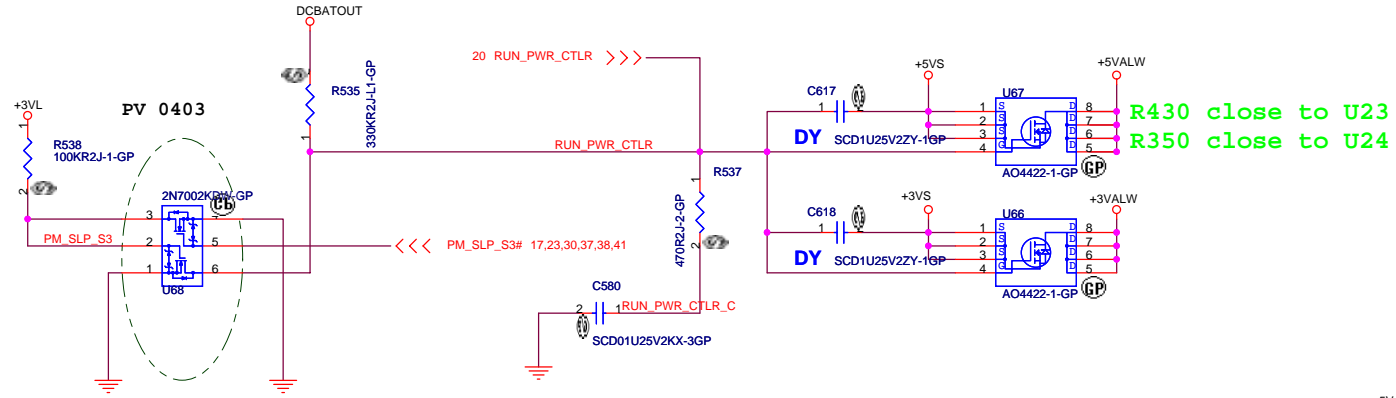
1113 DB



Close to SPKR1

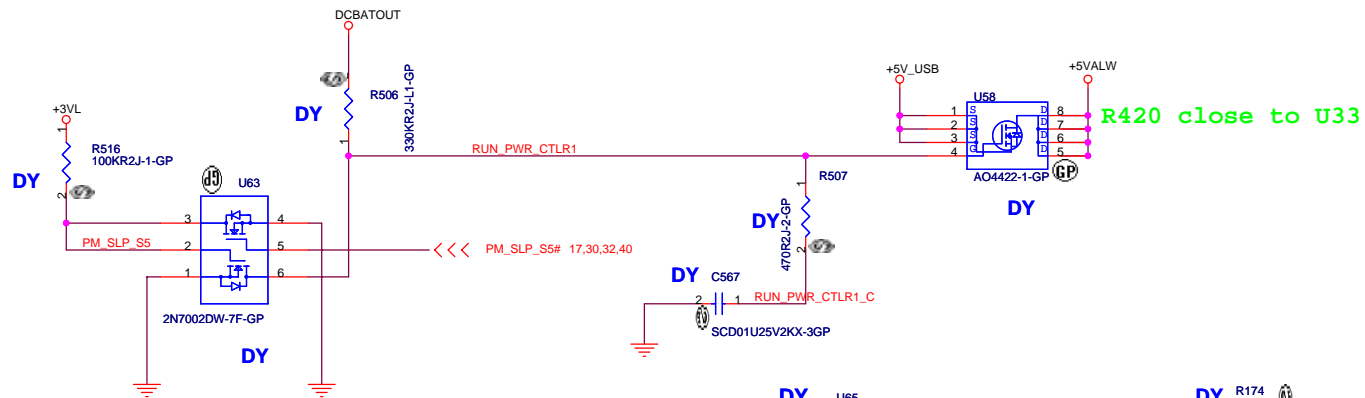


# Run Power



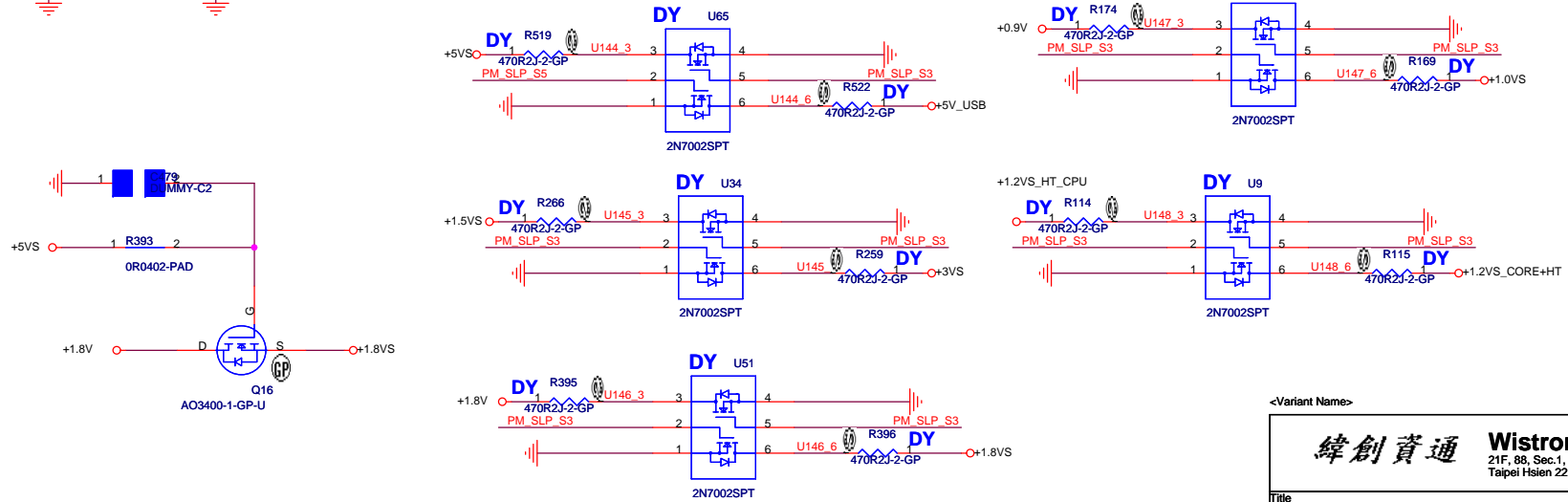
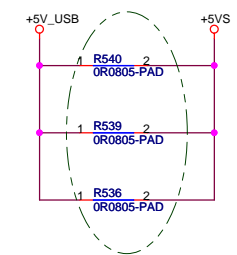
R430 close to U23  
R350 close to U24

# Run Power



R420 close to U33

## PV 0327



<Variant Name>

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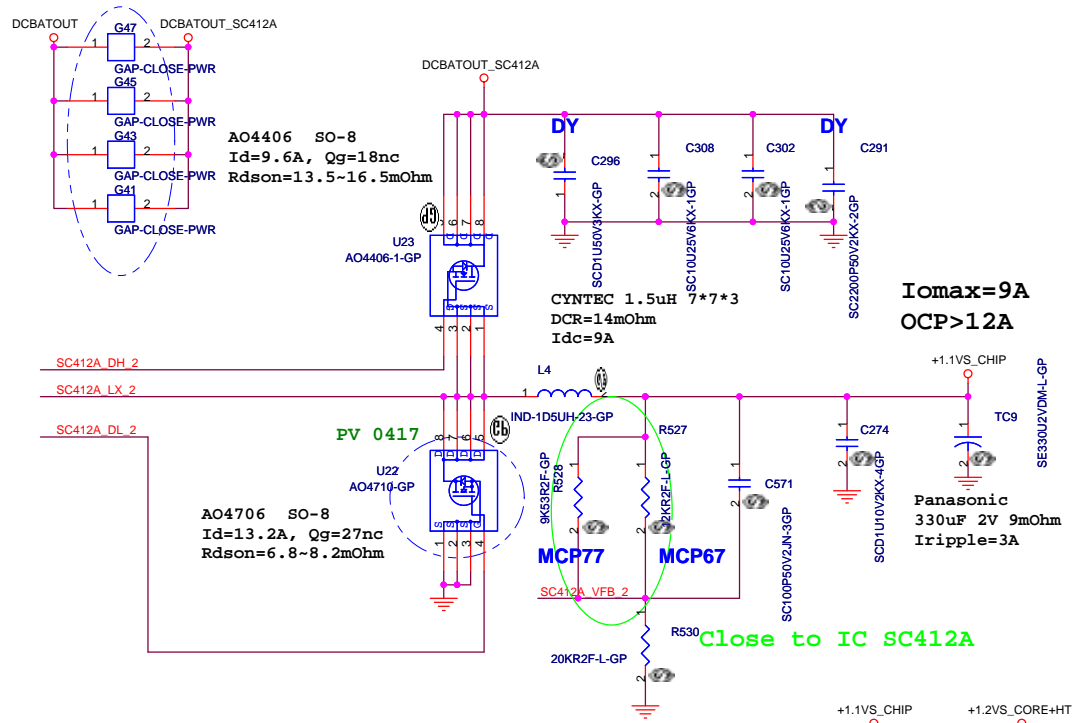
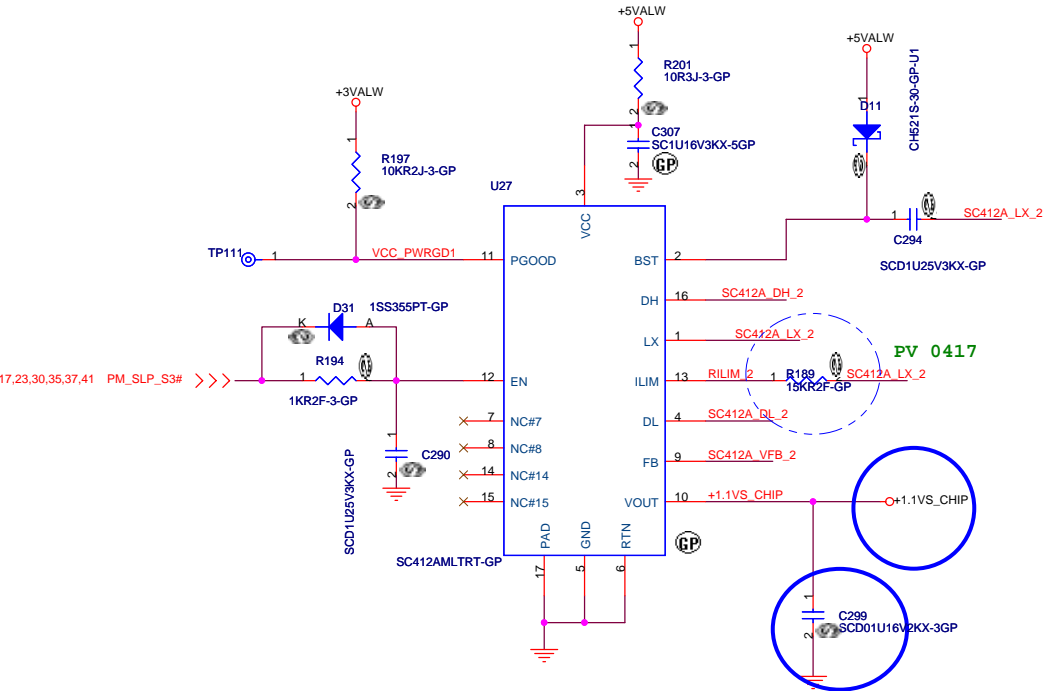
Title: **PWRPLANE&RESETLOGIC**

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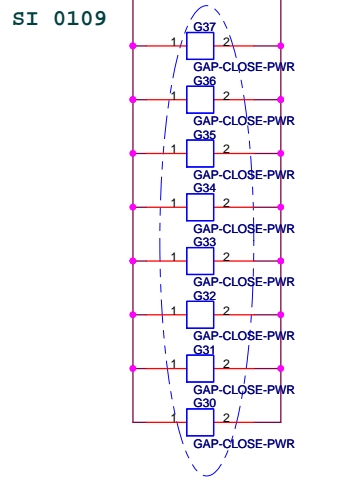




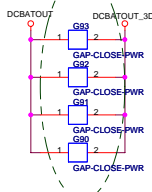




**MCP67: 1.2V (R425/R426) = (12K/20K)**  
**MCP77: 1.1V (R425/R426) = (9.53K/20K)**



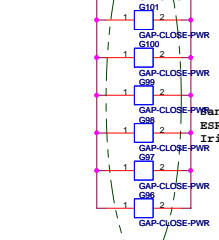
SI 0109



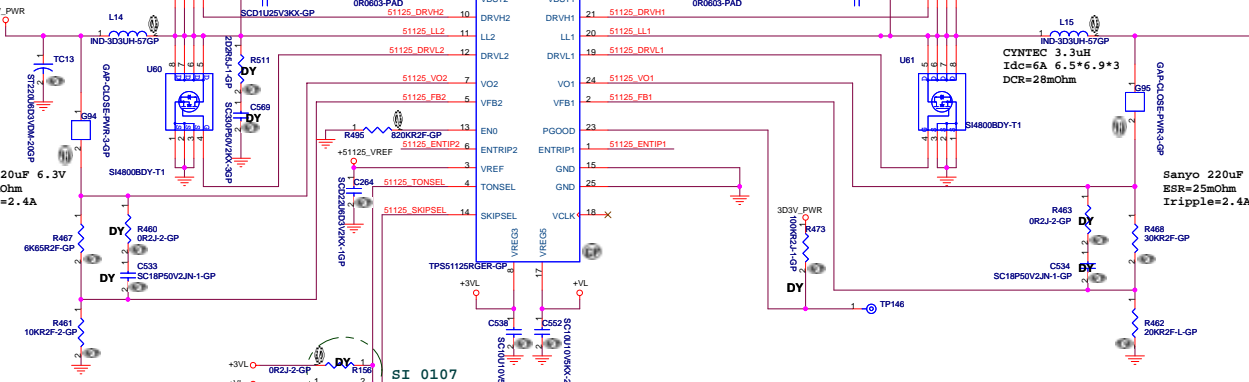
3.3V  
Design Current =6A  
OCP >8 A

SI4800, SO-8  
Id=9A, Qg=8.7-13nC  
Rdaon=23-30mchm

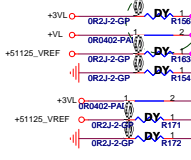
SI 0109



Sanyo 220uF 6.3V  
ESR=25mOhm  
Irripple=2.4A

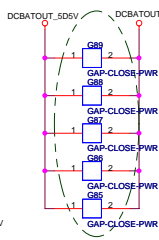


SI 0107



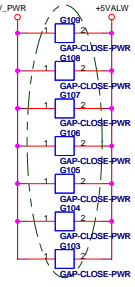
	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1	245k/CH1	300k/CH1	365k/CH1
	250k/CH2	305k/CH2	375k/CH2	460k/CH2

SI 0109

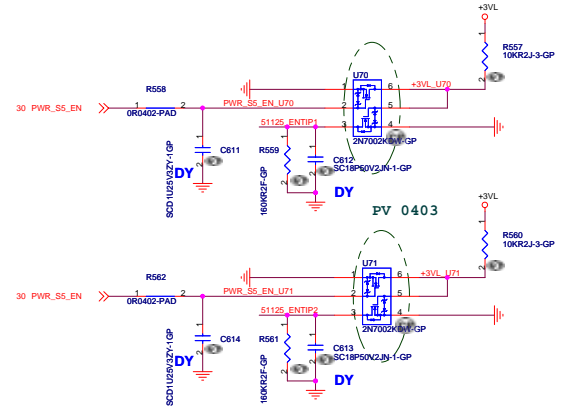


5V  
Design Current =6A  
OCP design >8A

SI 0109

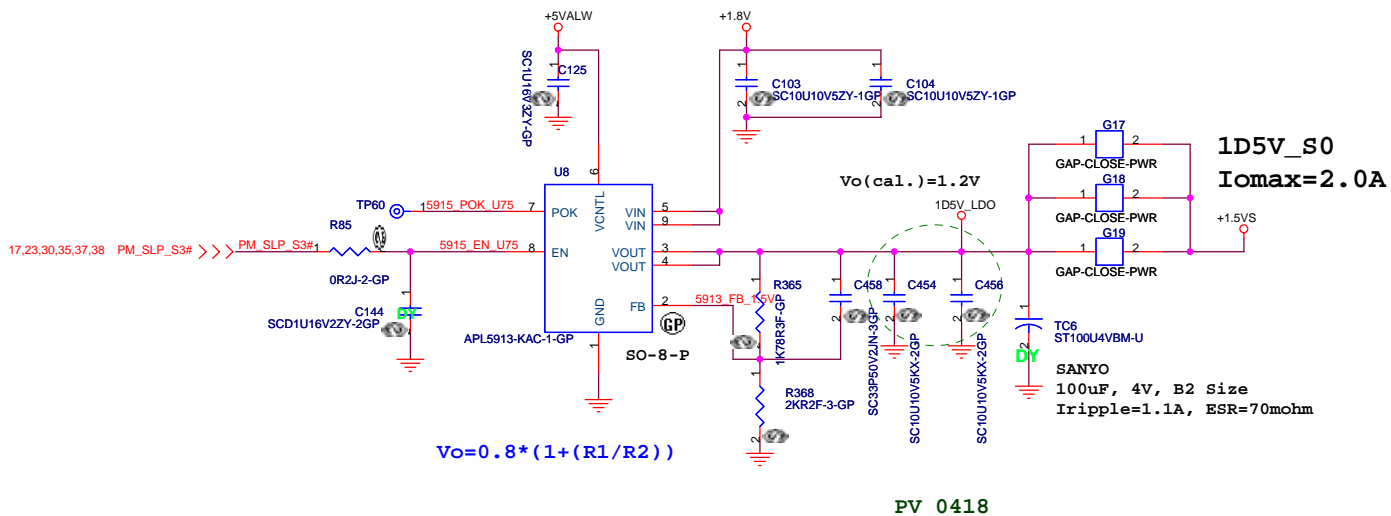
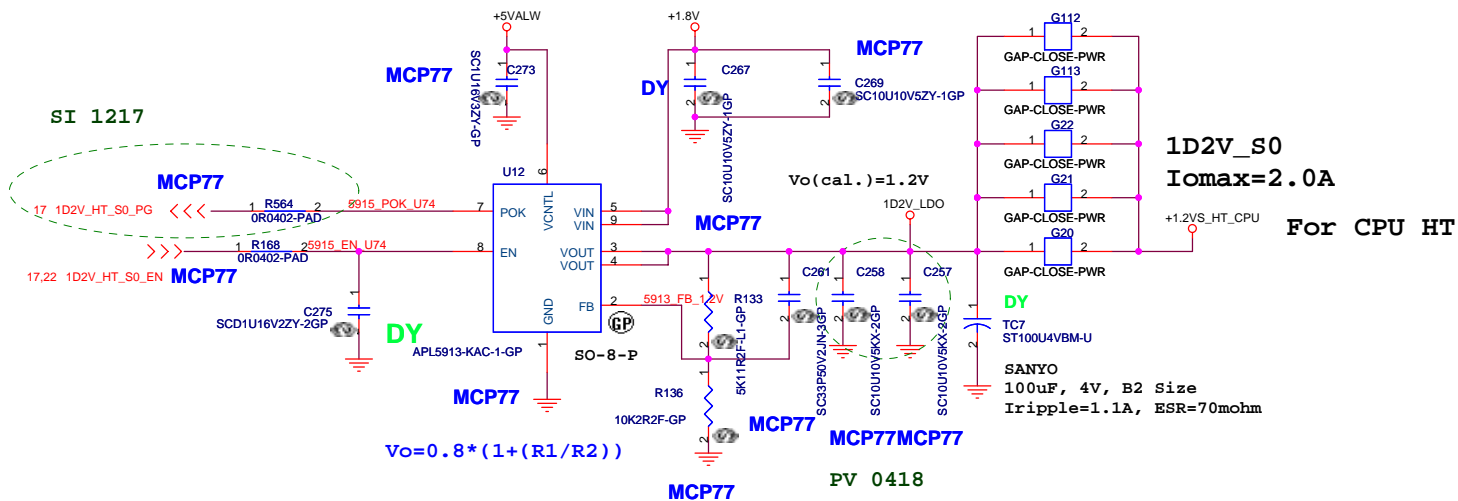
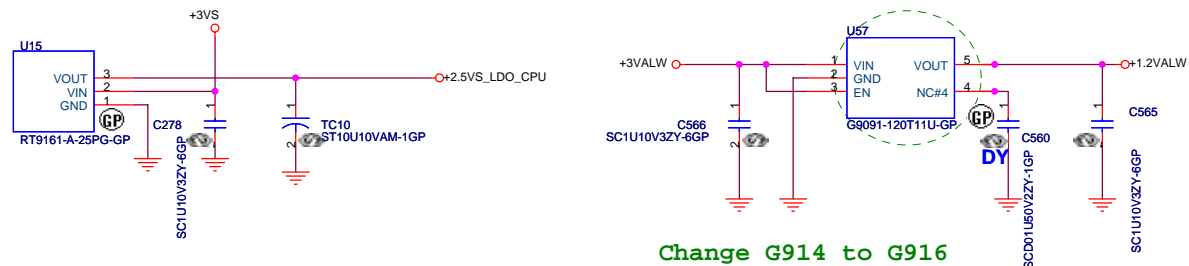


Sanyo 220uF 6.3V  
ESR=25mOhm  
Irripple=2.4A



«Core Design»



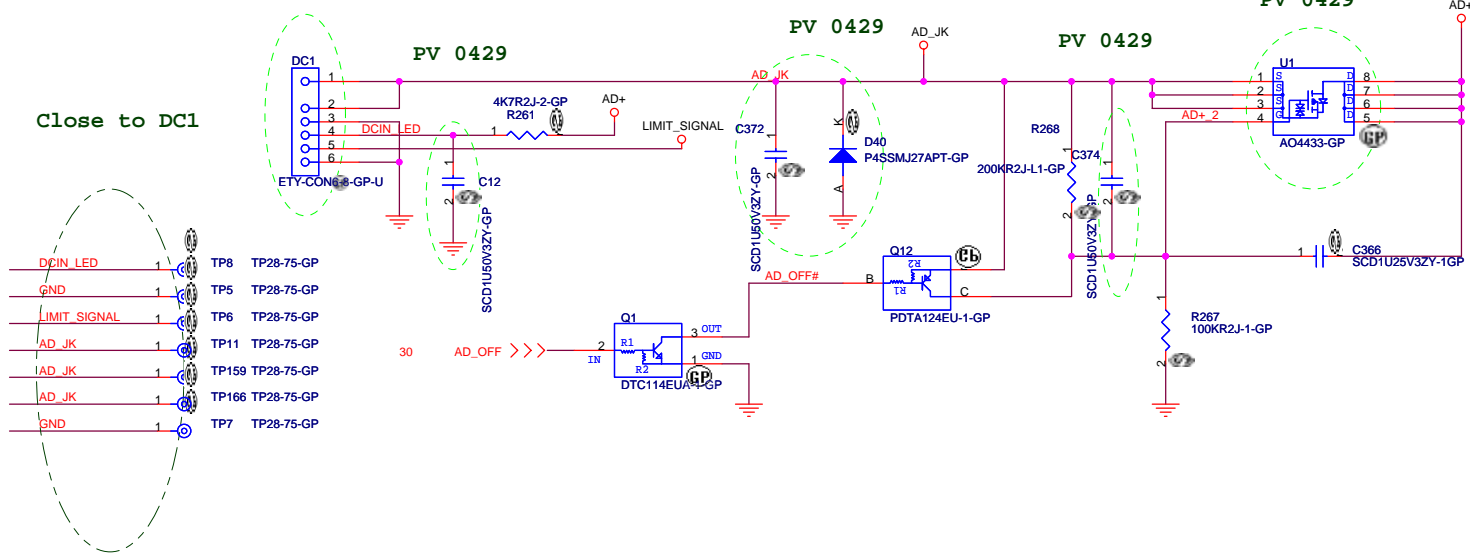




# Adaptor in to generate DCBATOUT

SI 0218

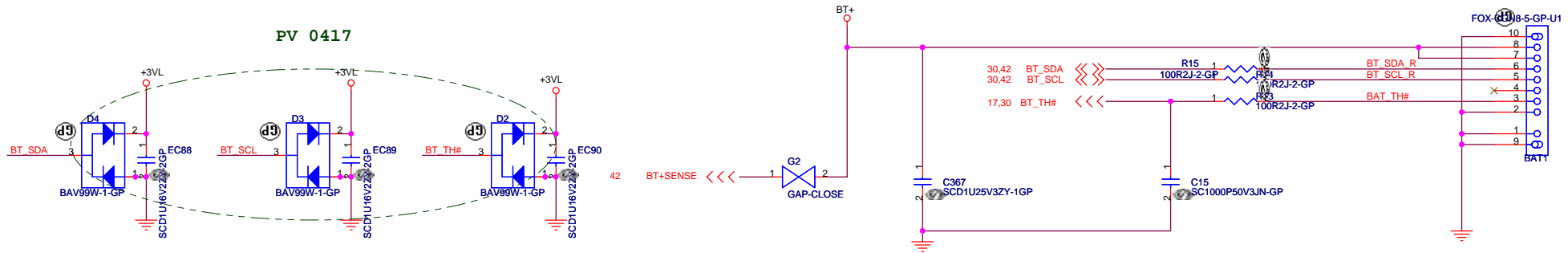
Close to DC1



DCIN_LED	1	TP8	TP28-75-GP
GND	1	TP5	TP28-75-GP
LIMIT_SIGNAL	1	TP6	TP28-75-GP
AD_JK	1	TP11	TP28-75-GP
AD_JK	1	TP159	TP28-75-GP
AD_JK	1	TP166	TP28-75-GP
GND	1	TP7	TP28-75-GP

# BATTERY CONNECTOR

PV 0417



SI 0306

BT+	1	TP171	TP28-75-GP
BT+	1	TP16	TP28-75-GP
BT+	1	TP15	TP28-75-GP
GND	1	TP12	TP28-75-GP
GND	1	TP13	TP28-75-GP
BT_SDA_R	1	TP18	TP28-75-GP
BT_SCL_R	1	TP14	TP28-75-GP
BAT_TH#	1	TP17	TP28-75-GP
GND	1	TP10	TP28-75-GP

Close to BAT1

<Core Design>

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<b>AD/BATT CONN</b>		
Size A3	Document Number	Rev SA
<b>Astrosphere</b>		
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