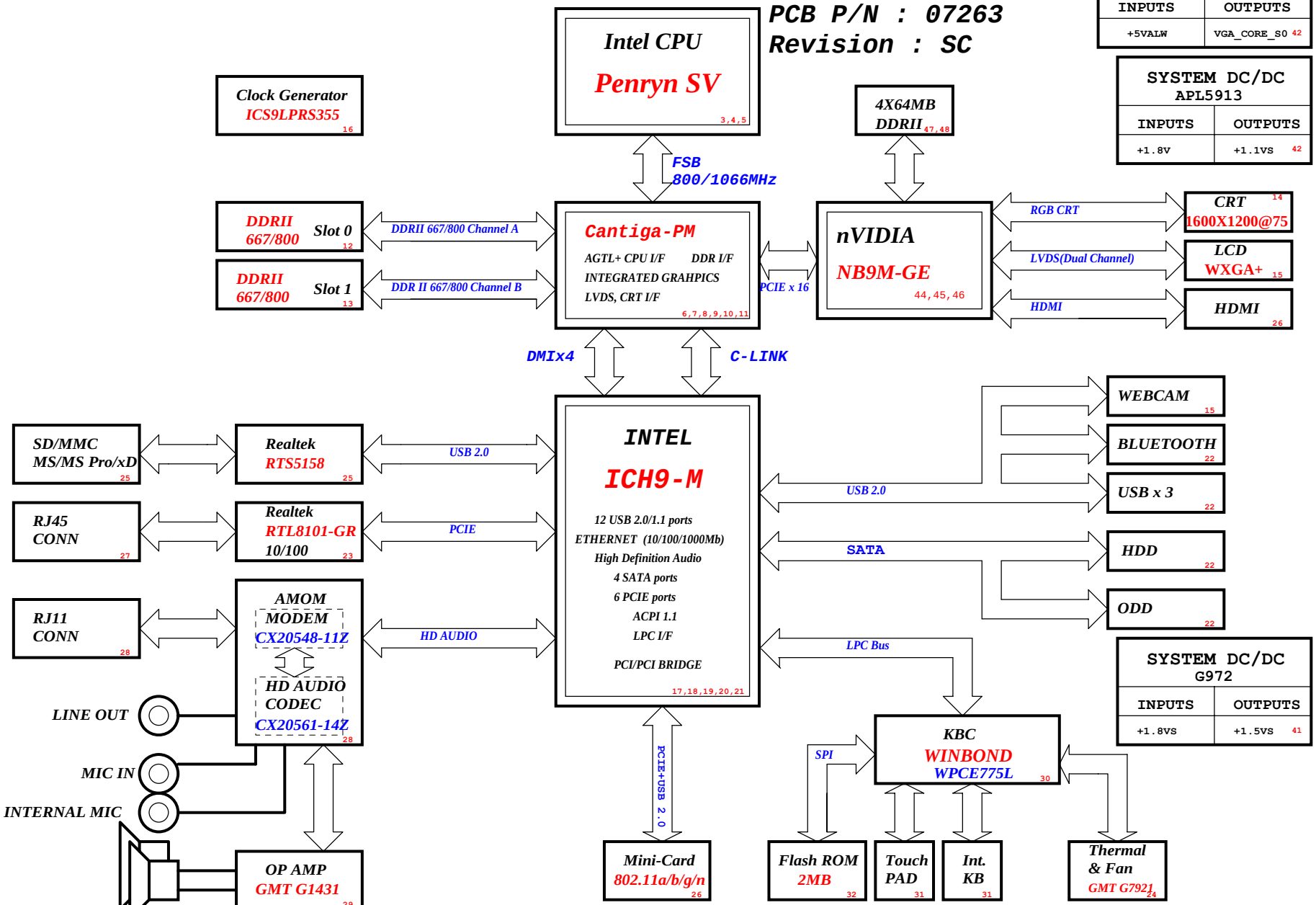
VITAS Block Diagram

Project code : 91.4I501.001
PCB P/N : 07263
Revision : SC



VGA DC/DC SC421A	
INPUTS	OUTPUTS
+5VALW	VGA_CORE_S0 42

SYSTEM DC/DC APL5913	
INPUTS	OUTPUTS
+1.8V	+1.1VS 42

SYSTEM DC/DC G972	
INPUTS	OUTPUTS
+1.8VS	+1.5VS 41

SYSTEM DC/DC TPA51125	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 38

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 36

CPU DC/DC ISL6260CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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Title: **Block Diagram**

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

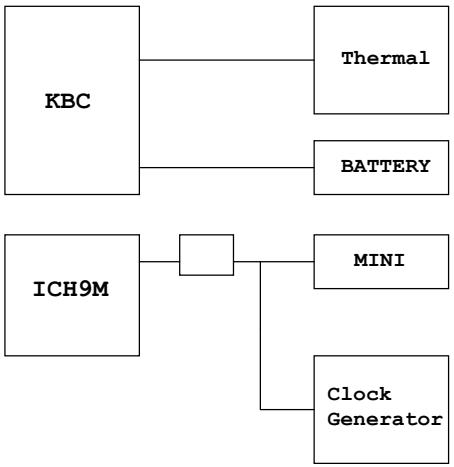
PCIE Routing page 19

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Reserve for ITP, when install ITP connector, install R338.

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Connect to V Core

4/23 Houston

PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)

ITP Connector

Reserve for ITP

Place R310 with in 200ps (~1") to CPU

U65A 1 OF 4

BGA479-SKT6-GPU6

62.10079.001

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Title: CPU (1 of 2)

Size: | Document Number: VITAS | Rev: SA

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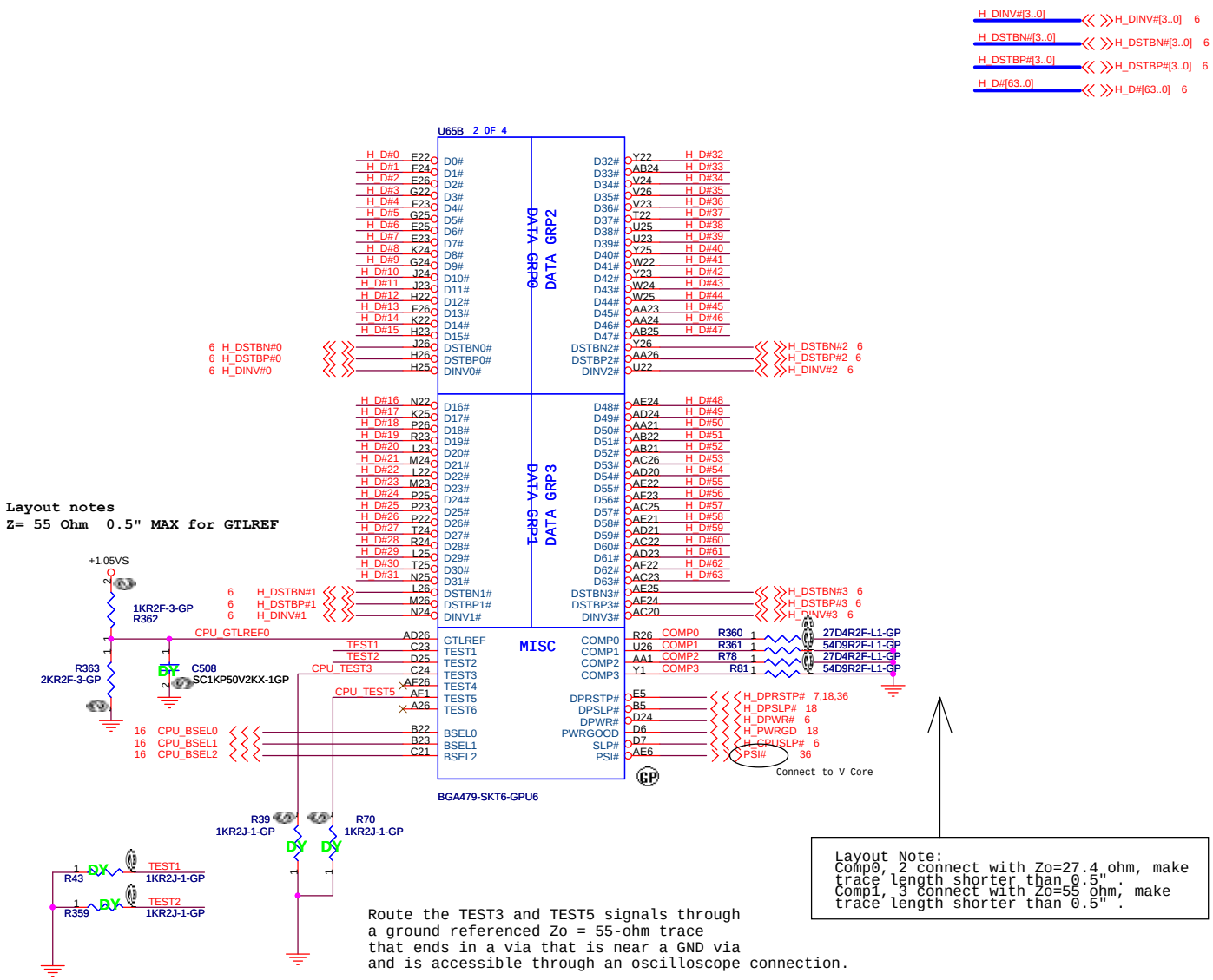

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Title: ***CPU (3 of 2)***

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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

0128 DB

0429 PV

U65C 3 0F 4

BGA479-SKT6-GPU6

U65D 4 0F 4

BGA479-SKT6-GPU6

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

NCTF PIN

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Title: CPU (3 of 3)

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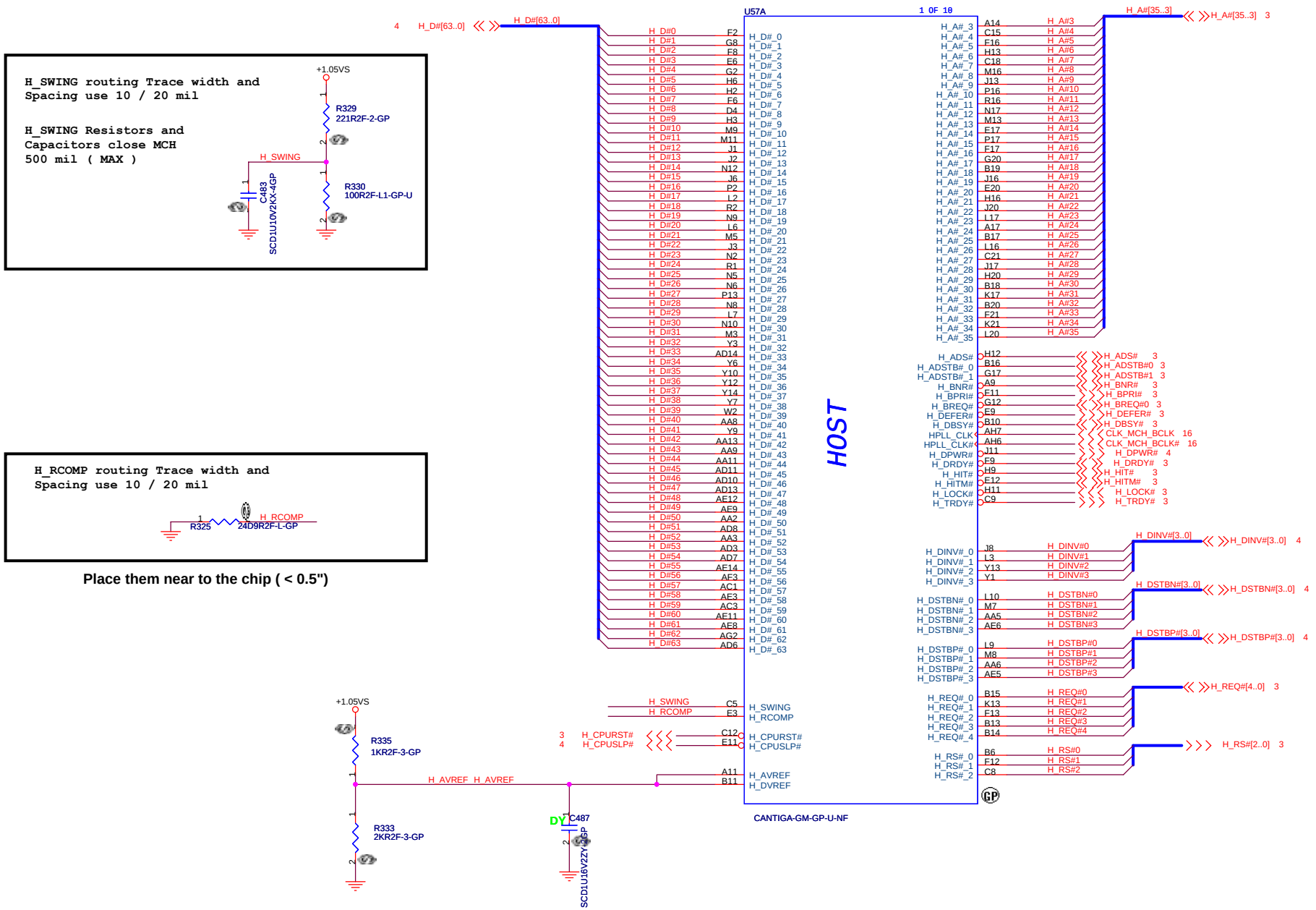

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Title: Cantiga (1 of 6)

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Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

U57B — 2 OF 10

RESERVED#M36 RESERVED#N36 RESERVED#R33 RESERVED#T33 RESERVED#AH9 RESERVED#AH10 RESERVED#AH12 RESERVED#AH13 RESERVED#K12 RESERVED#AL34 RESERVED#AK34 RESERVED#AN35 RESERVED#AM35 RESERVED#T24

RESERVED#B31 RESERVED#B2 RESERVED#M1

RESERVED#AY21

RESERVED#BG23 RESERVED#BF23 RESERVED#BH18 RESERVED#BF18

RSVD

SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 — M_CLK_DDR0 12, M_CLK_DDR1 12, M_CLK_DDR2 13, M_CLK_DDR3 13

SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 — M_CLK_DDR#0 12, M_CLK_DDR#1 12, M_CLK_DDR#2 13, M_CLK_DDR#3 13

SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 — M_CKE0 12, M_CKE1 12, M_CKE2 13, M_CKE3 13

SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 — M_CS0# 12, M_CS1# 12, M_CS2# 13, M_CS3# 13

SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 — M_ODT0 12, M_ODT1 12, M_ODT2 13, M_ODT3 13

SM_RCOMP — M_RCOMPP
SM_RCOMP# — M_RCOMPN
SM_RCOMP_VOH — SM_RCOMP_VOH
SM_RCOMP_VOL — SM_RCOMP_VOL

DDR CLK/ CONTROL/COMPENSATION

SM_VREF — DDR_VREF_S3
SM_PWROK
SM_REXT — SM_REXT — R343 499R2F-2-GP
SM_DRAMRST#

+1.8V — R50 1KR2F-3-GP DY — R48 1KR2F-3-GP DY

Use DDR3 need enable

DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# — 1218

PEG_CLK PEG_CLK# — CLK_MCH_3GPLL 16, CLK_MCH_3GPLL# 16

CLK

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 — DMI_TXN0 19, DMI_TXN1 19, DMI_TXN2 19, DMI_TXN3 19

DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 — DMI_TXP0 19, DMI_TXP1 19, DMI_TXP2 19, DMI_TXP3 19

DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 — DMI_RXN0 19, DMI_RXN1 19, DMI_RXN2 19, DMI_RXN3 19

DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 — DMI_RXP0 19, DMI_RXP1 19, DMI_RXP2 19, DMI_RXP3 19

DMI

FSB setting

3,16 MCH_CLKSEL0
3,16 MCH_CLKSEL1
3,16 MCH_CLKSEL2

CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

CFG

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4

GFX_VR_EN

GRAPHICS VID

PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

PM

CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF — CL_CLK0 19, CL_DATA0 19, M_PWROK 19, CL_RST#0 19

ME

DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# — ICH_SDVO_CLK, ICH_SDVO_DATA, MCH_CLK_REQ# 16, MCH_ICH_SYNC# 19

TSATN# — TSATN#

1015 DB — TP54 TP55 — 1113 DB

DDPC/SDVO for HDMI used

HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC — TP168 TP53 TP51 TP52 TP167

1218

HDA

NC/#BG48 NC/#BF48 NC/#BD48 NC/#BC48 NC/#BH47 NC/#BG47 NC/#BE47 NC/#BH46 NC/#BF46 NC/#BG45 NC/#BH44 NC/#BH43 NC/#BH6 NC/#BH5 NC/#BG4 NC/#BH3 NC/#BF3 NC/#BH2 NC/#BG2 NC/#BE2 NC/#BG1 NC/#BF1 NC/#BD1 NC/#BC1 NC/#F1 NC/#A47

NC

MISC

CANTIGA-GM-GP-U-NF

R351 80D6R2F-L-GP — M_RCOMPP
R348 80D6R2F-L-GP — M_RCOMPN

+3VS — RN6 SRN10KJ-5-GP — PM_EXTTS#0 PM_EXTTS#1

CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG16 CFG18 CFG19 CFG20

R31 2K21R2F-GP CFG18
R26 2K21R2F-GP CFG11
R32 4K02R2F-GP CFG19
DY

1011 DB

R33 4K02R2F-GP CFG20
R28 2K21R2F-GP CFG6
R354 2K21R2F-GP CFG5
R29 2K21R2F-GP CFG7
R347 2K21R2F-GP CFG8
R349 4K02R2F-GP CFG9
R23 2K21R2F-GP CFG12
R24 2K21R2F-GP CFG13
R22 2K21R2F-GP CFG16
R352 2K21R2F-GP CFG10

19 PM_SYNC#
4,18,36 H_DPRSTP#
12 PM_EXTTS#0
13 PM_EXTTS#1
19,33 PM_PWROK
17,23,26,27,30,44 PLT_RST#
3,18 PM_THRMTRIP-A#
19,36 PM_DPRSLPVR
Connect to V Core

R44 0R0402-PAD
R20 100R2-2-GP
C41 SC100P50V2JN-3GP DY

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

1113 DB

Please Close GMCH
R522 10KR2J-3-GP
R340 56R2J-4-GP
TSATN#_KBC — TSATN#_KBC 30
Q7 MMBT3904WT1G-GP
Please Close to U22
1218

+1.05VS — R37 1KR2F-3-GP — CL_VREF ~= 0.35V
C82 SCD1U10V2KX-4GP
R38 499R2F-2-GP
1107 DB

U57C — 3 OF 10

L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK
L_CTRL_DATA L_DDC_CLK L_DDC_DATA
L_VDD_EN LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK
LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3
LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3
LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3
LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3

LVDS

TVA_DAC TVB_DAC TVC_DAC TV_RTN
TV_DCONSEL_0 TV_DCONSEL_1

TV

CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN
CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_TVO_IREF CRT_VSYNC

VGA

CANTIGA-GM-GP-U-NF

PEG_COMPI PEG_COMPO — R40 49D9R2F-GP — +VCC_PEG — PEG_CMP

PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15 — PEG_RXN0 44 … PEG_RXN15 44

PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15 — PEG_RXP0 44 … PEG_RXP15 44

PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15 — TXN0 … TXN15 — C803 … C581 — SCD1U10V2KX-5GP — PEG_TXN0 44 … PEG_TXN15 44

PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15 — TXP0 … TXP15 — C804 … C582 — SCD1U10V2KX-5GP — PEG_TXP0 44 … PEG_TXP15 44

PCI-EXPRESS GRAPHICS

R367 1KR2F-3-GP — +1.8V
R364 3K01R2F-3-GP — C516 SCD01U16V2KX-3GP — SM_RCOMP_VOH — C512 SC2D2U6D3V3MX-1-GP
R355 1KR2F-3-GP — C501 SCD01U16V2KX-3GP — SM_RCOMP_VOL — C502 SC2D2U6D3V3MX-1-GP

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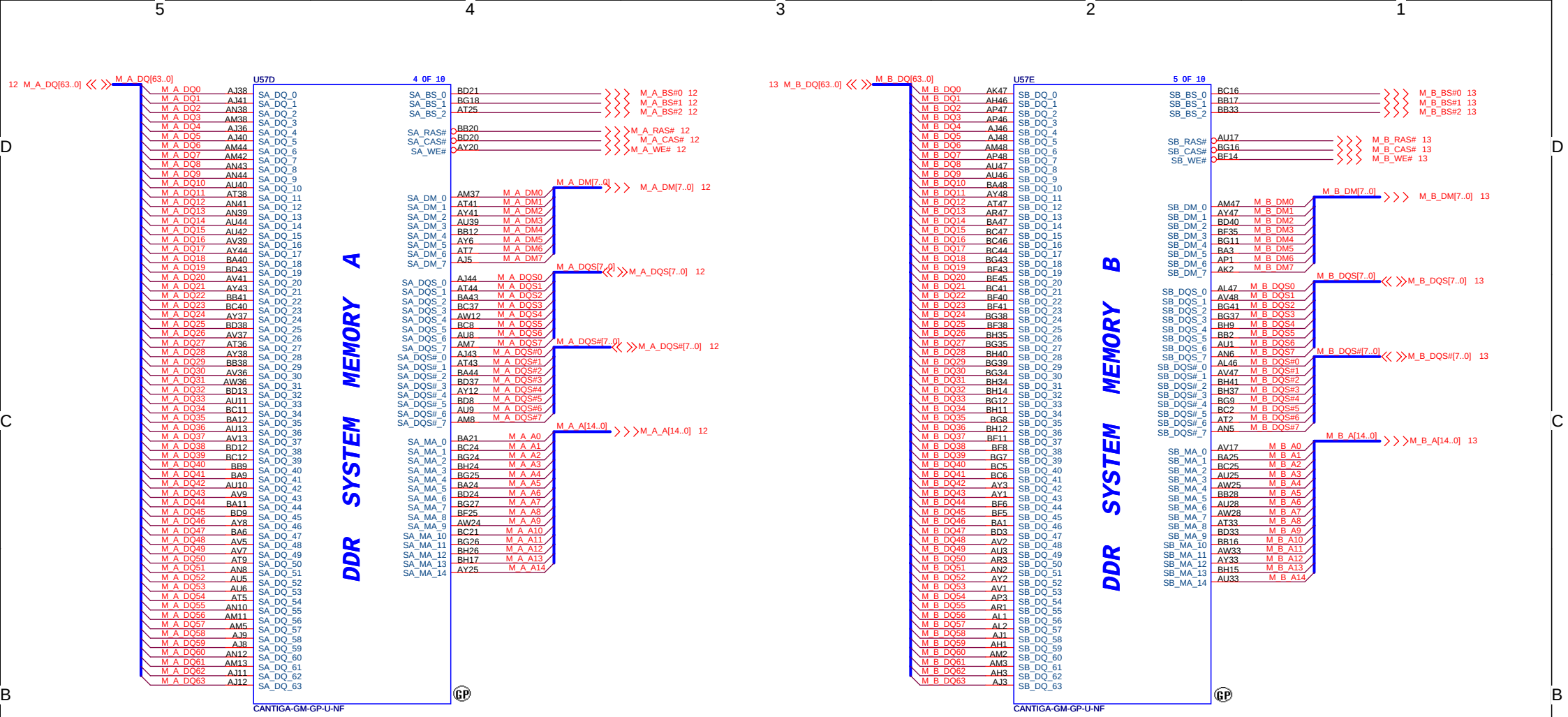

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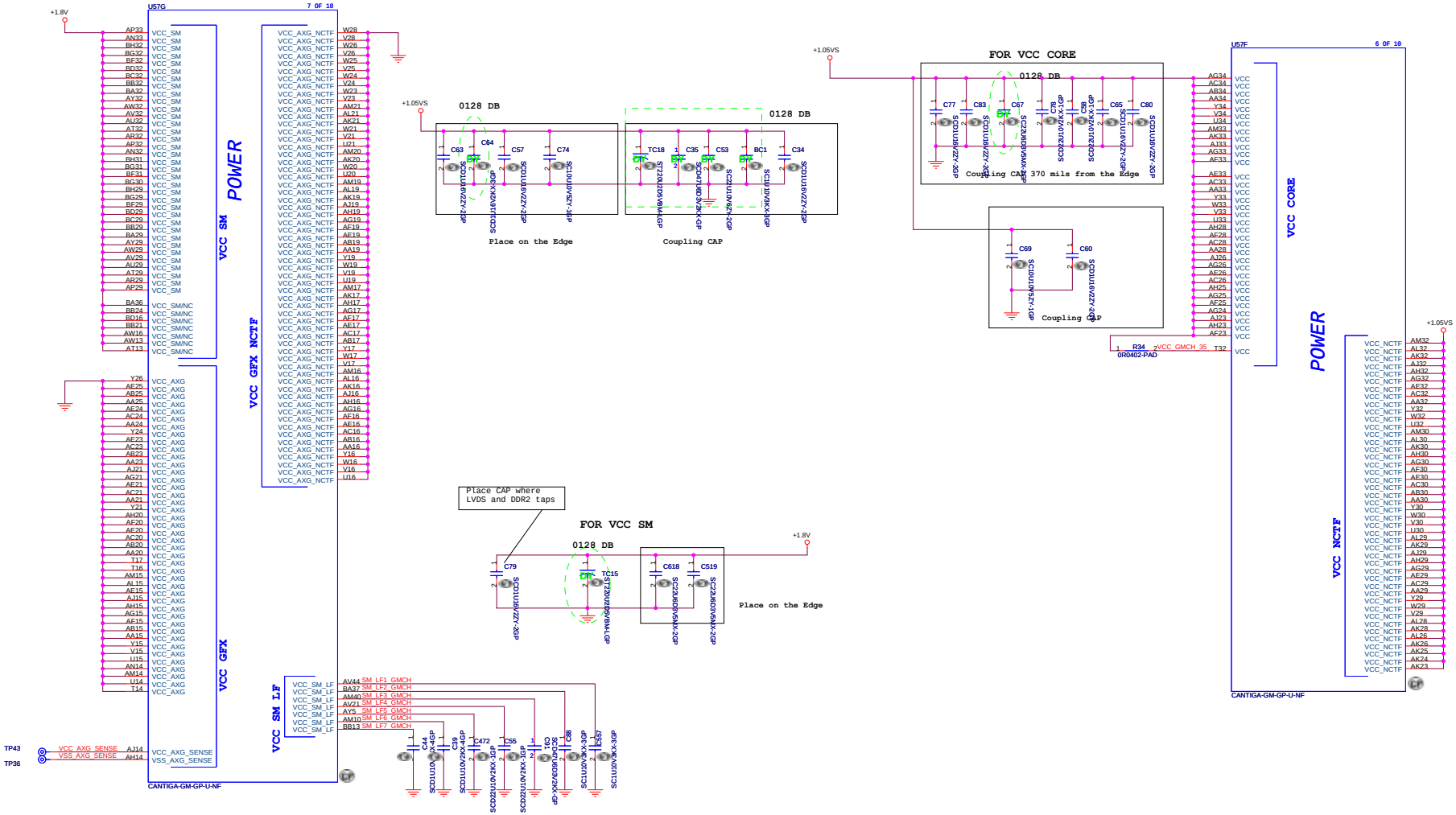

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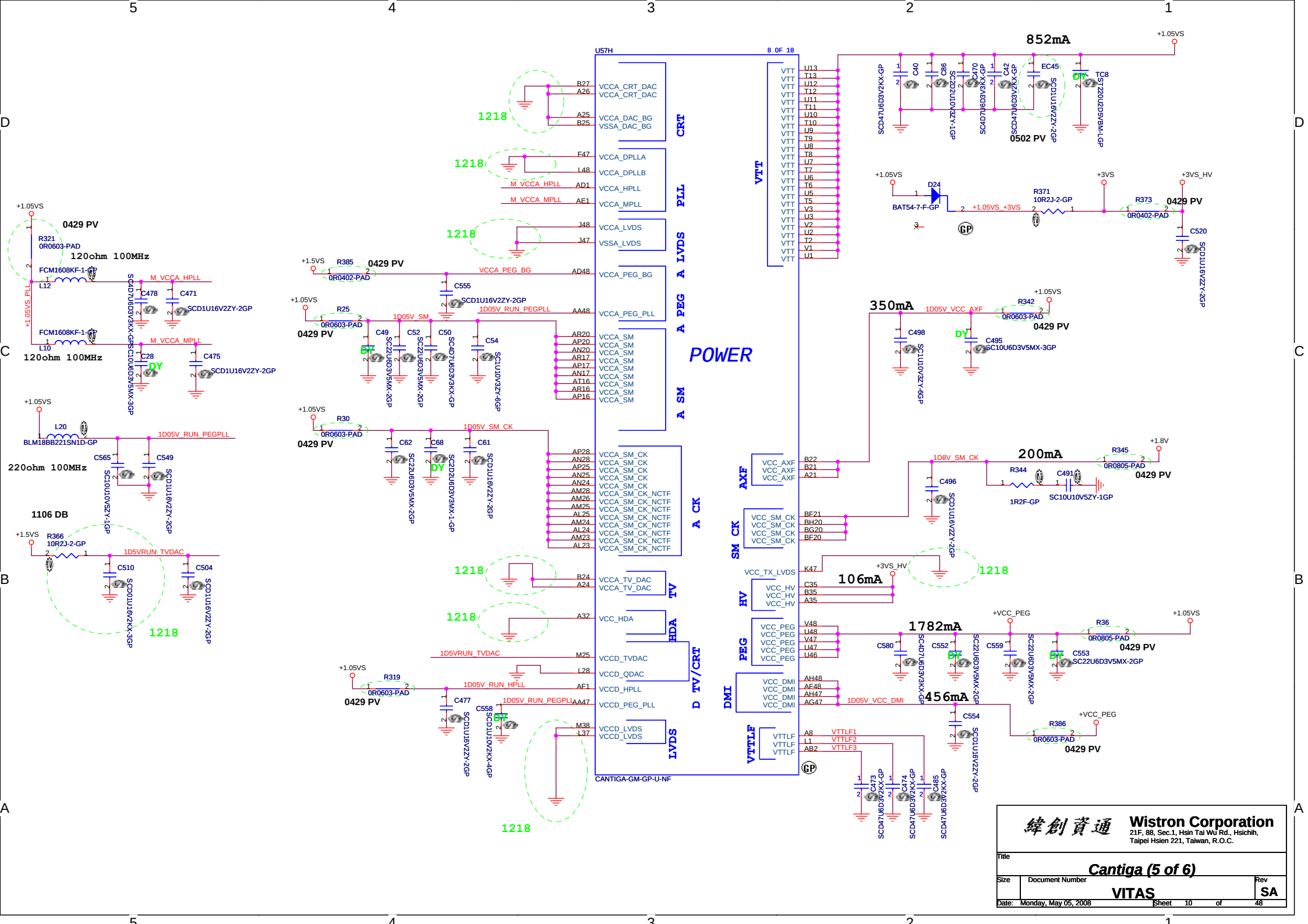
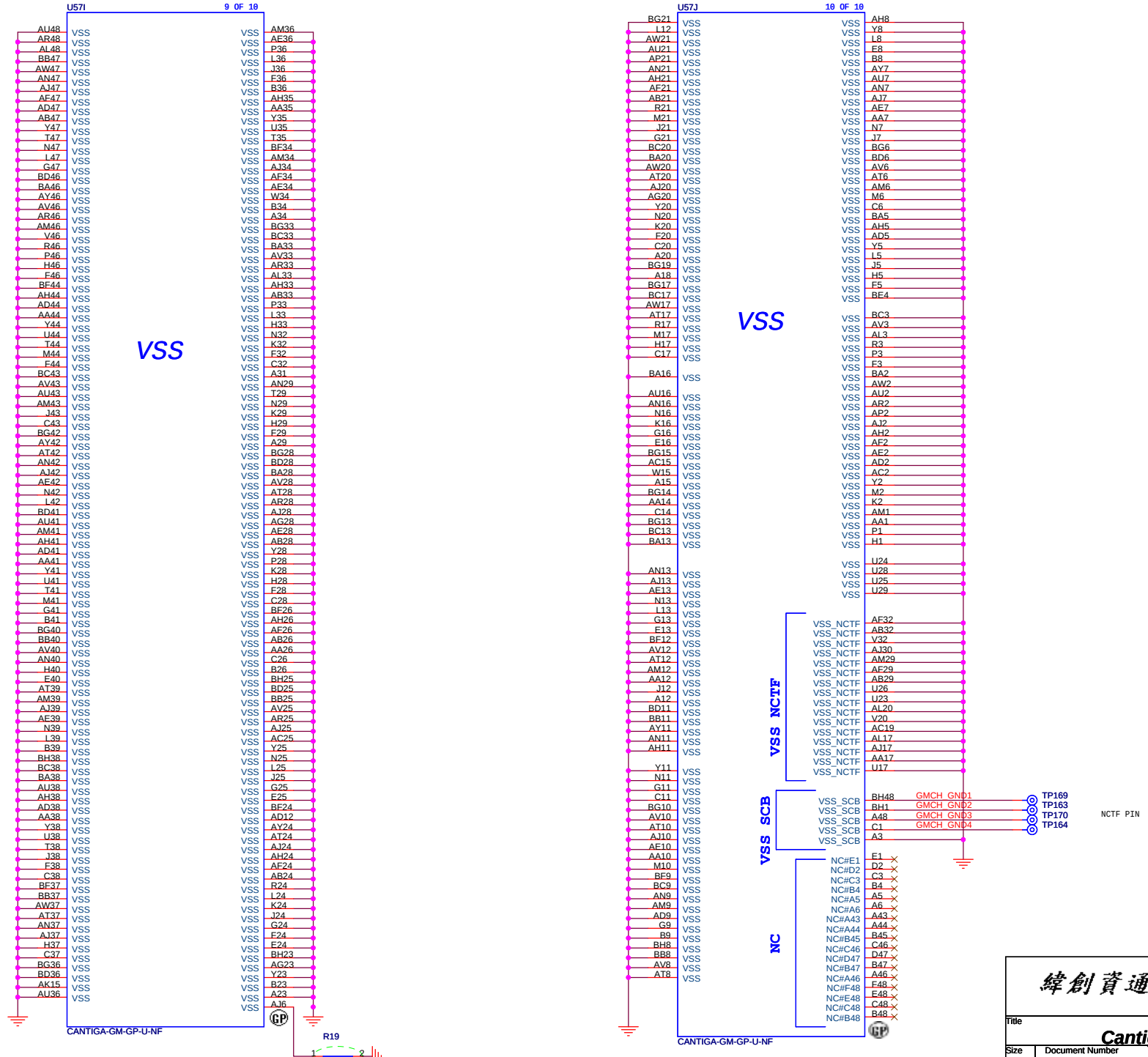

U57H
8 OF 10
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
PEG
DMI
HV
VTT
VTTLF
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_CK
VCCA_SM_CK_NCTF
VCCA_TV_DAC
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCC_AXF
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_DMI
VTT
VTTLF1
VTTLF2
VTTLF3
CANTIGA-GM-GP-U-NF
852mA
0502 PV
350mA
200mA
106mA
1782mA
456mA
0429 PV
1218
1106 DB
120ohm 100MHz
220ohm 100MHz
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga (5 of 6)
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 10 of 48



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (6 of 6)

Size	Document Number	Rev
	VITAS	SA

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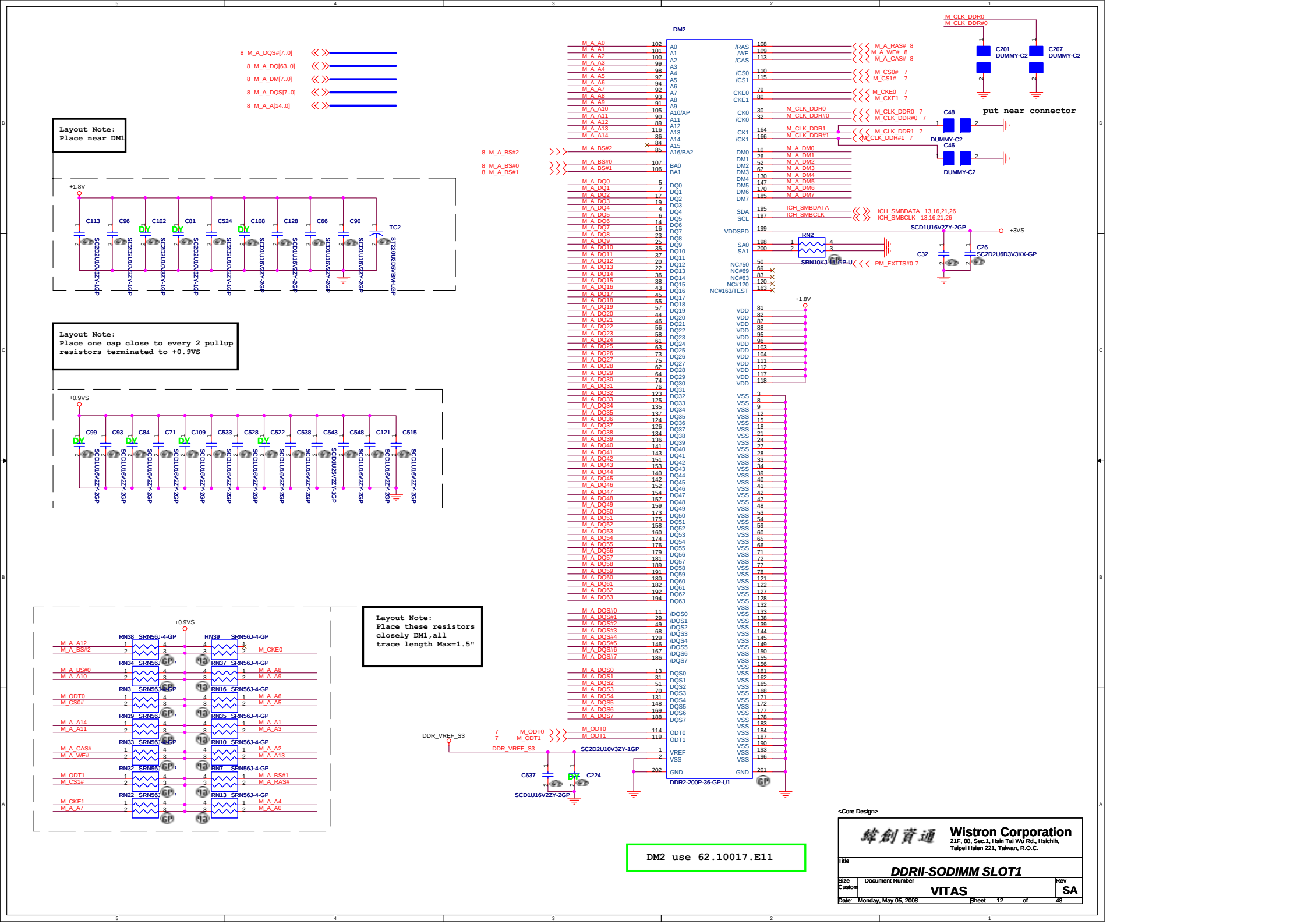
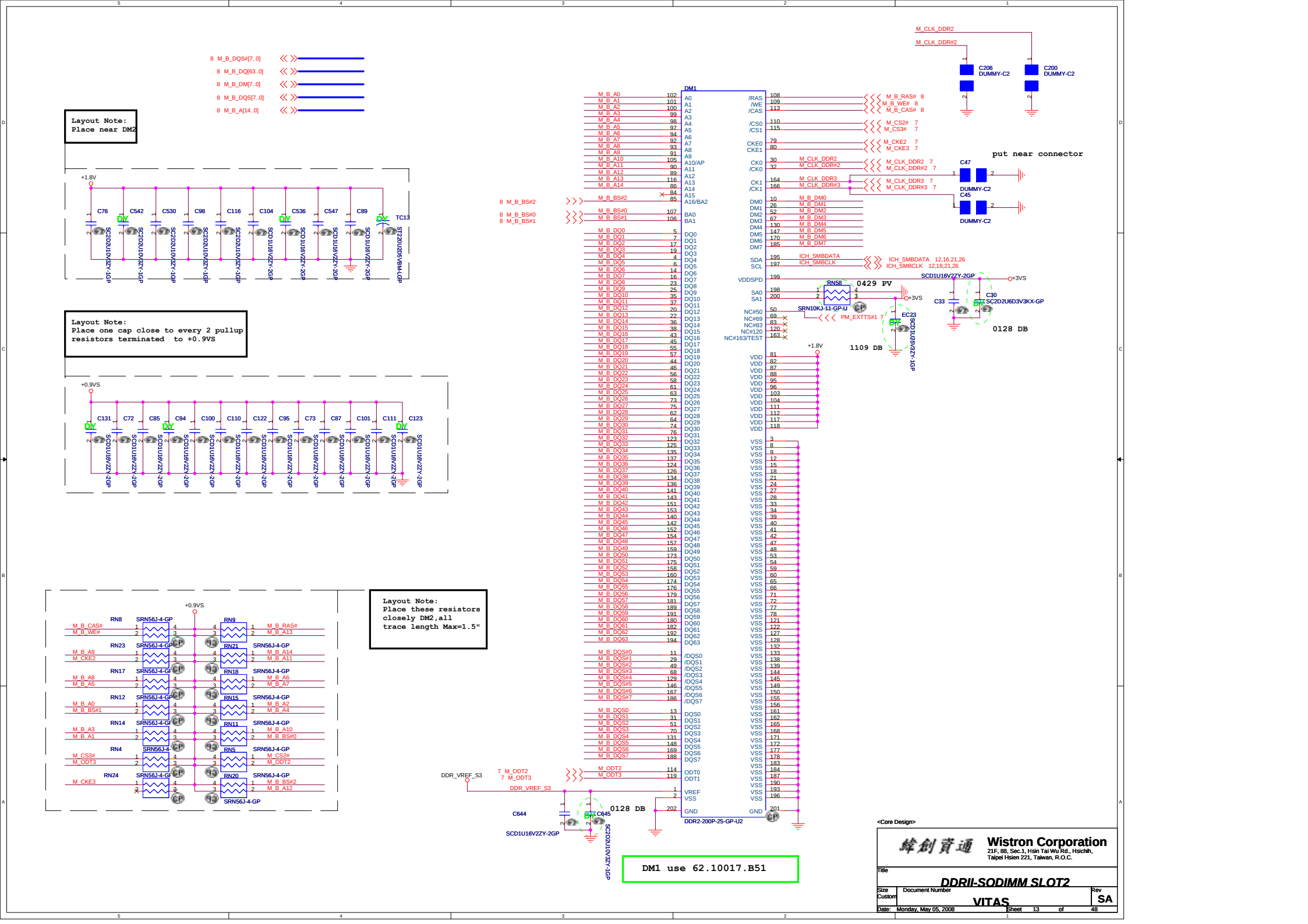

8 M_A_DQS#[7..0]
8 M_A_DQ[63..0]
8 M_A_DM[7..0]
8 M_A_DQS[7..0]
8 M_A_A[14..0]
Layout Note:
Place near DM1
+1.8V
C113 C96 C102 C81 C524 C108 C128 C66 C90 TC2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C99 C93 C84 C71 C109 C533 C528 C522 C538 C543 C548 C121 C515
+0.9VS
RN38 SRN56J-4-GP
RN39 SRN56J-4-GP
RN34 SRN56J-4-GP
RN37 SRN56J-4-GP
RN3 SRN56J-4-GP
RN16 SRN56J-4-GP
RN19 SRN56J-4-GP
RN35 SRN56J-4-GP
RN33 SRN56J-4-GP
RN10 SRN56J-4-GP
RN32 SRN56J-4-GP
RN7 SRN56J-4-GP
RN22 SRN56J-4-GP
RN13 SRN56J-4-GP
M_A_A12
M_A_BS#2
M_CKE0
M_A_BS#0
M_A_A10
M_A_A8
M_A_A9
M_ODT0
M_CS0#
M_A_A6
M_A_A5
M_A_A14
M_A_A11
M_A_A1
M_A_A3
M_A_CAS#
M_A_WE#
M_A_A2
M_A_A13
M_ODT1
M_CS1#
M_A_BS#1
M_A_RAS#
M_CKE1
M_A_A7
M_A_A4
M_A_A0
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14
M_A_BS#2
M_A_BS#0 M_A_BS#1
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
M_ODT0 M_ODT1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
/DQS0 /DQS1 /DQS2 /DQS3 /DQS4 /DQS5 /DQS6 /DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF VSS
GND GND
/RAS /WE /CAS /CS0 /CS1 CKE0 CKE1 CK0 /CK0 CK1 /CK1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL VDDSPD SA0 SA1
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
VDD VSS
DDR2-200P-36-GP-U1
M_A_RAS# 8
M_A_WE# 8
M_A_CAS# 8
M_CS0# 7
M_CS1# 7
M_CKE0 7
M_CKE1 7
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
ICH_SMBDATA 13,16,21,26
ICH_SMBCLK 13,16,21,26
SCD1U16V2ZY-2GP
+3VS
RN2
SRN10K-1-GP
PM_EXTTS#0 7
C32
C26 SC2D2U6D3V3KX-GP
+1.8V
DDR_VREF_S3
M_ODT0 7
M_ODT1 7
SC2D2U10V3ZY-1GP
C637 C224
SCD1U16V2ZY-2GP
M_CLK_DDR0
M_CLK_DDR#0
C201 DUMMY-C2
C207 DUMMY-C2
C48 DUMMY-C2
C46 DUMMY-C2
put near connector
DM2 use 62.10017.E11
<Core Design>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
Sheet 12 of 48


8 M_B_DQS#[7..0]
8 M_B_DQ[63..0]
8 M_B_DM[7..0]
8 M_B_DQS[7..0]
8 M_B_A[14..0]
Layout Note:
Place near DM2
+1.8V
C76 C542 C530 C98 C116 C104 C536 C547 C89 TC13
DY
SCD2U10V2ZY-1GP
SCD1U16V2ZY-2GP
ST220U2R5VBM4-GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C131 C72 C85 C94 C100 C110 C122 C95 C73 C87 C101 C111 C123
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
+0.9VS
RN8 SRN56J-4-GP M_B_CAS# M_B_WE# M_B_RAS# M_B_A13
RN23 M_B_A9 M_CKE2 M_B_A14 M_B_A11
RN17 M_B_A8 M_B_A5 M_B_A6 M_B_A7
RN12 M_B_A0 M_B_BS#1 M_B_A2 M_B_A4
RN14 M_B_A3 M_B_A1 M_B_A10 M_B_BS#0
RN4 M_CS3# M_ODT3 M_CS2# M_ODT2
RN24 M_CKE3 M_BS#2 M_B_A12
RN5 RN9 RN11 RN15 RN18 RN20 RN21
DM1
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
M_B_BS#2 M_B_BS#0 M_B_BS#1
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_ODT2 M_ODT3
DDR_VREF_S3
C644 C645 0128 DB
SCD1U16V2ZY-2GP
SCD2D2U10D3Z-1GP
DDR2-200P-25-GP-U2
/RAS /WE /CAS M_B_RAS# 8 M_B_WE# 8 M_B_CAS# 8
/CS0 /CS1 M_CS2# 7 M_CS3# 7
CKE0 CKE1 M_CKE2 7 M_CKE3 7
CK0 /CK0 M_CLK_DDR2 M_CLK_DDR#2 7
CK1 /CK1 M_CLK_DDR3 M_CLK_DDR#3 7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
SDA SCL ICH_SMBDATA ICH_SMBCLK ICH_SMBDATA 12,16,21,26 ICH_SMBCLK 12,16,21,26
VDDSPD SCD1U16V2ZY-2GP +3VS
SA0 SA1 RN58 0429 PV SRN10KJ-11-GP-U +3VS
NC#50 NC#69 NC#83 NC#120 NC#163/TEST PM_EXTTS#1 7
EC23 SCD1U28V2ZY-1GP 1109 DB
C33 C30 SC2D2U6D3V3KX-GP 0128 DB
+1.8V
VDD VSS
M_CLK_DDR2 M_CLK_DDR#2
C206 DUMMY-C2 C200 DUMMY-C2
put near connector
C47 DUMMY-C2 C45 DUMMY-C2
DM1 use 62.10017.B51
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number VITAS
Rev SA
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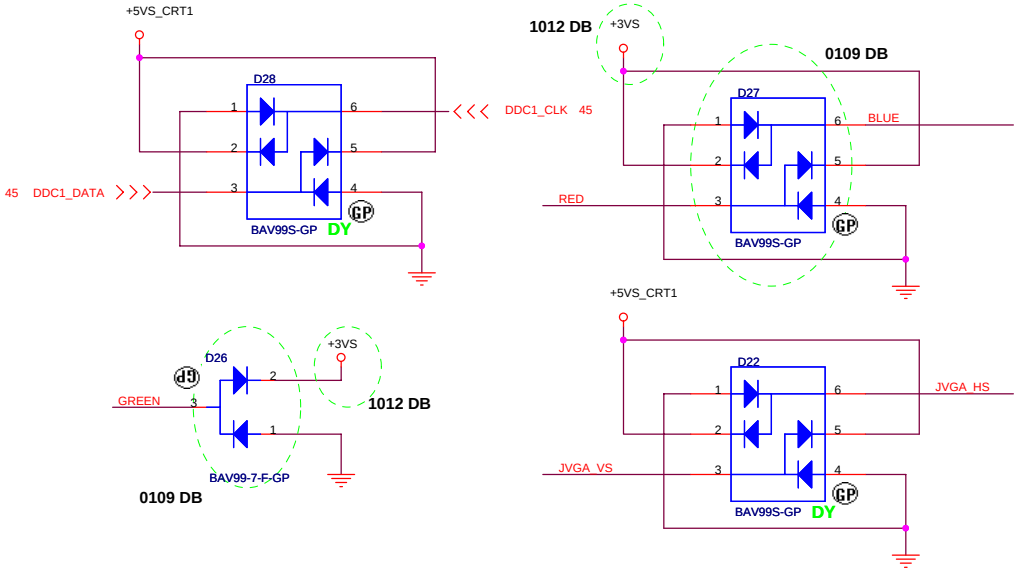
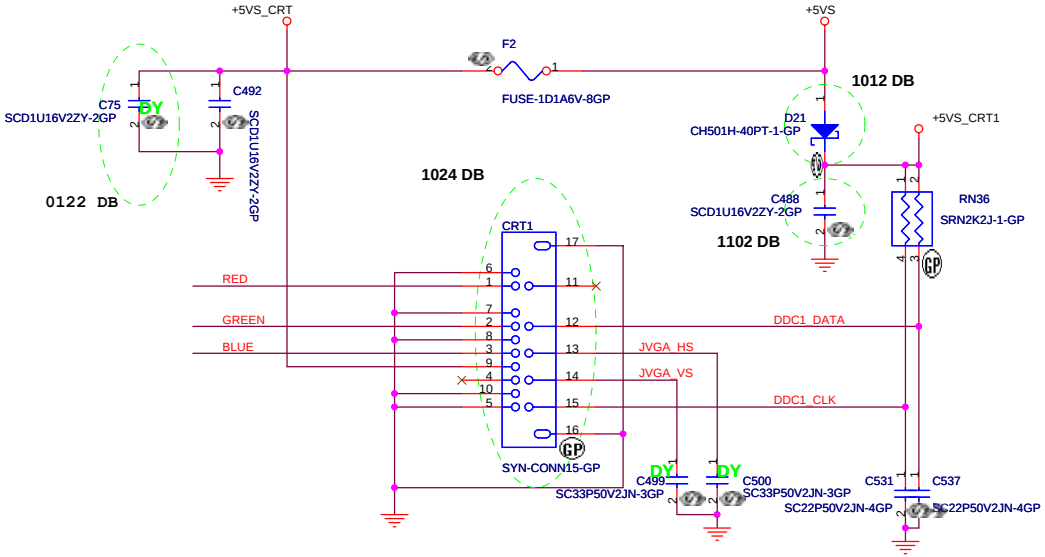
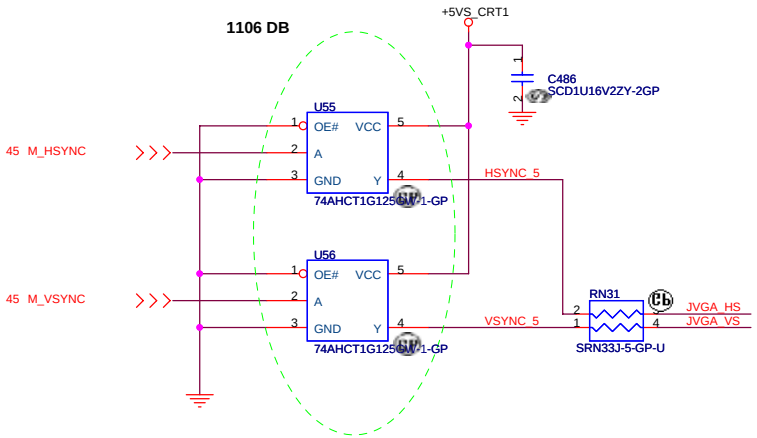
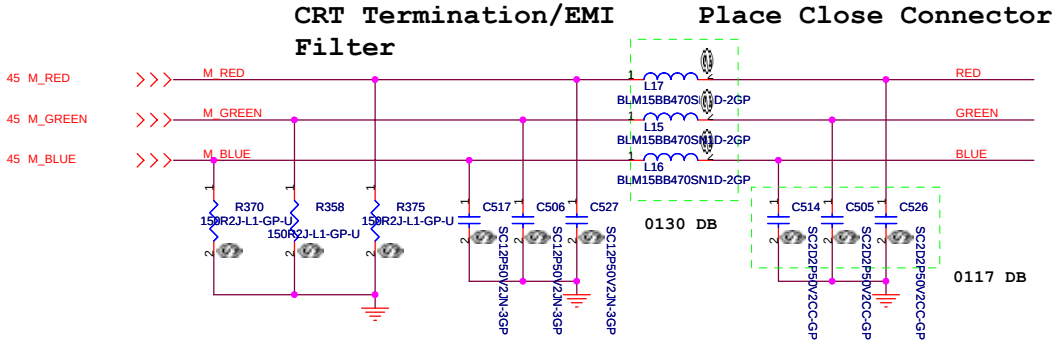
CRT I/F & CONNECTOR





Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size A3	Document Number VITAS	Rev SA
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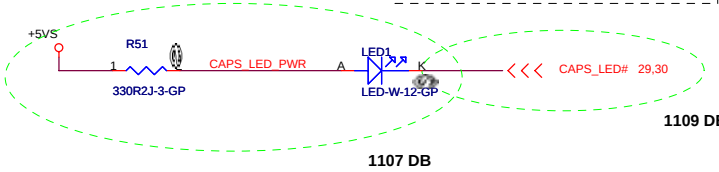
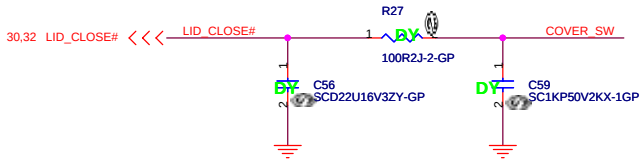
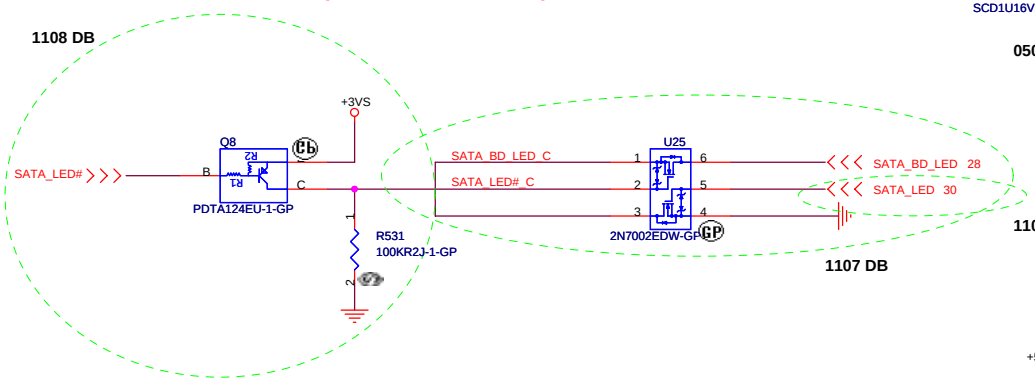
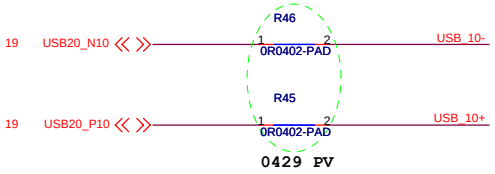
LCD / INVERTER INTERFACE / CAMERA

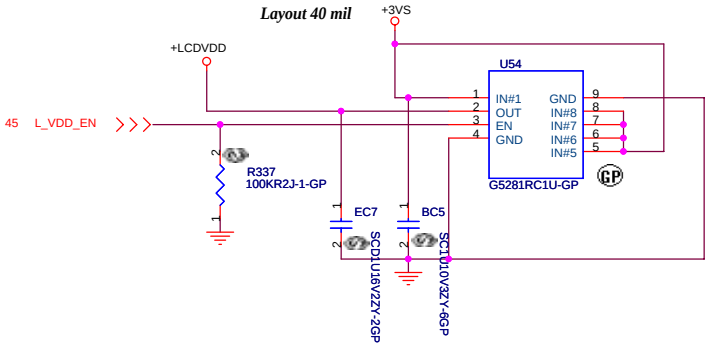
White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70

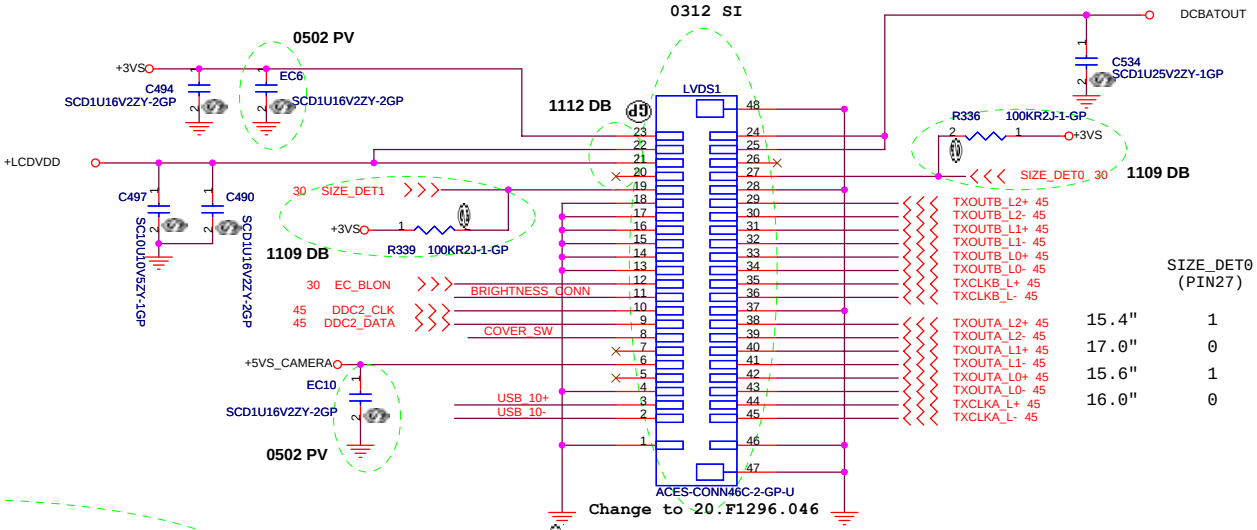




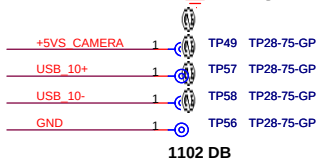


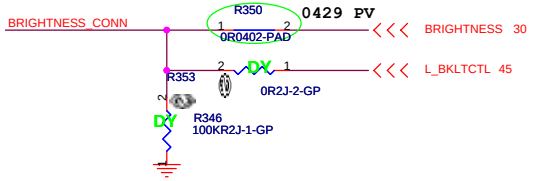


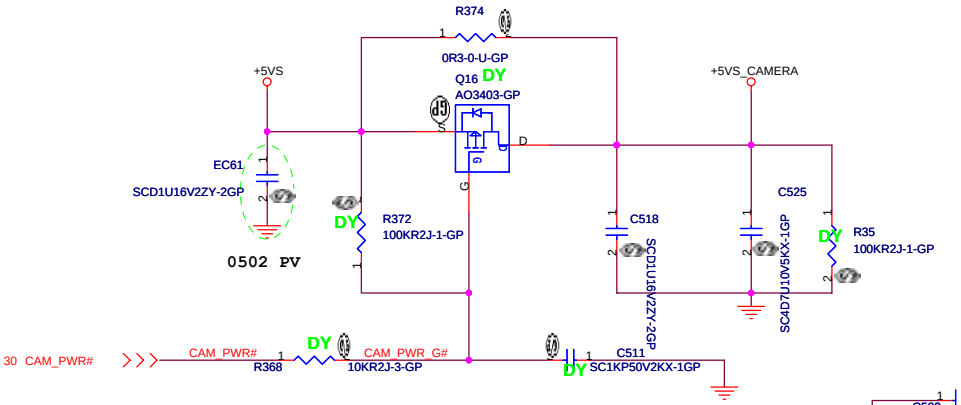


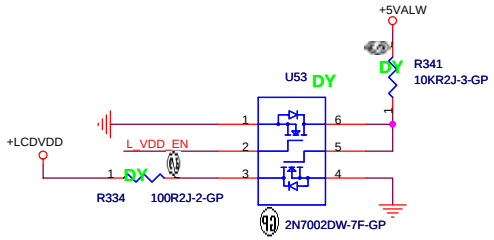


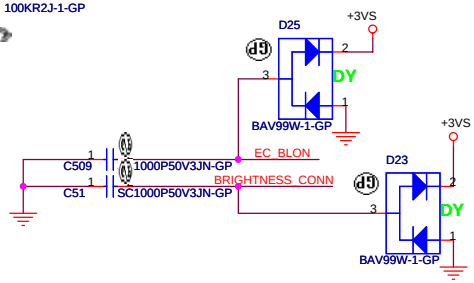
	SIZE_DET0 (PIN27)	SIZE_DET1 (PIN19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0











<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector/CAM/LED

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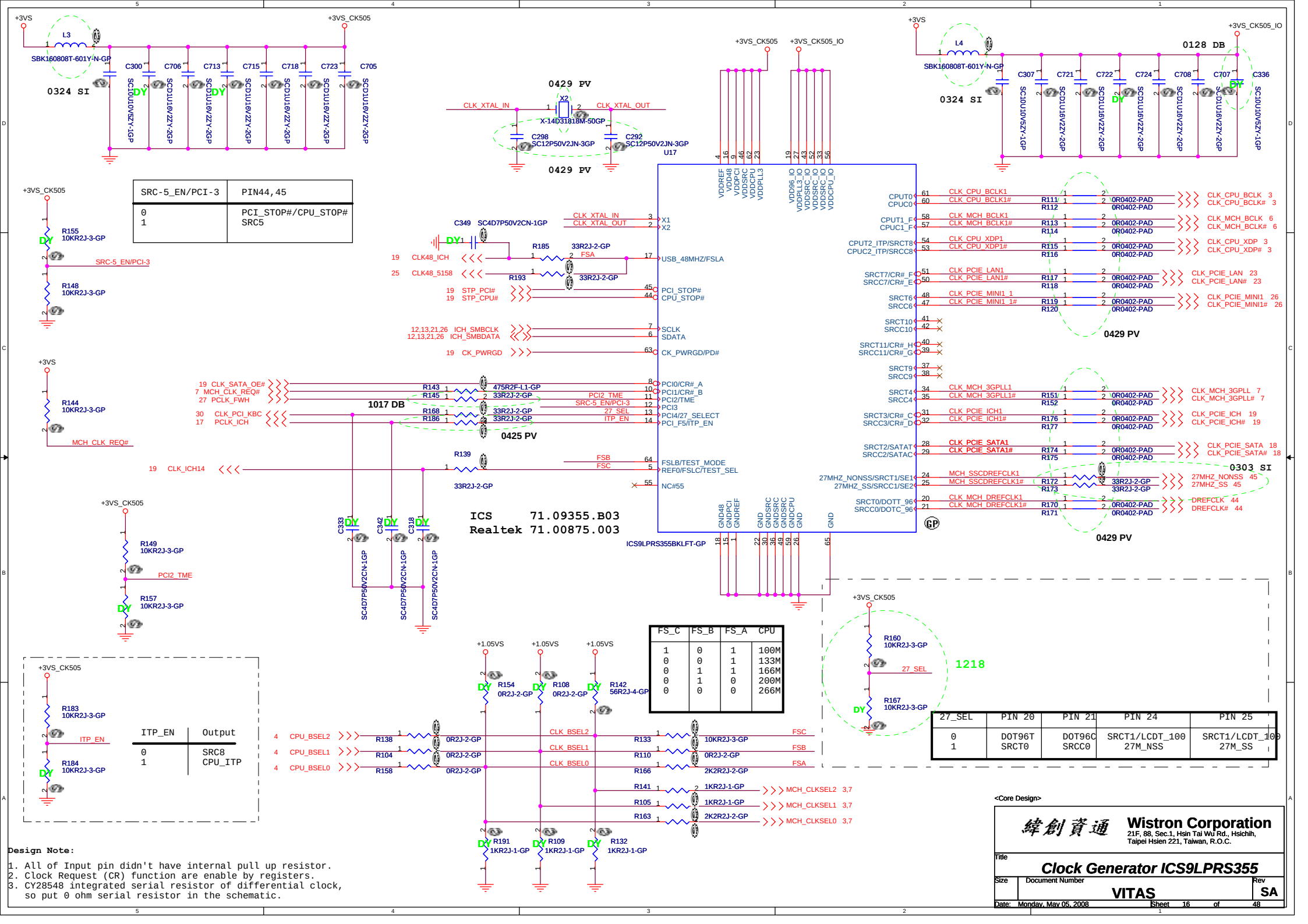
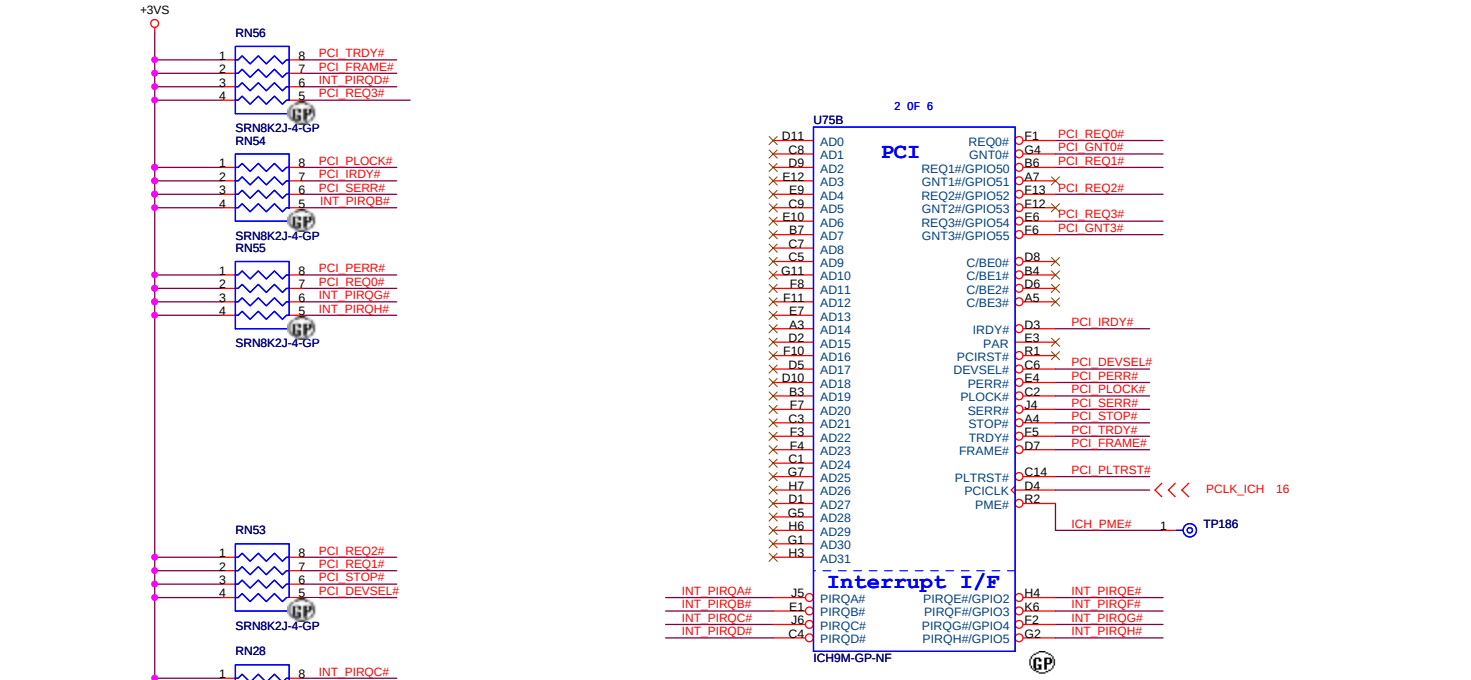
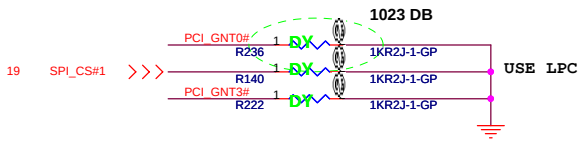
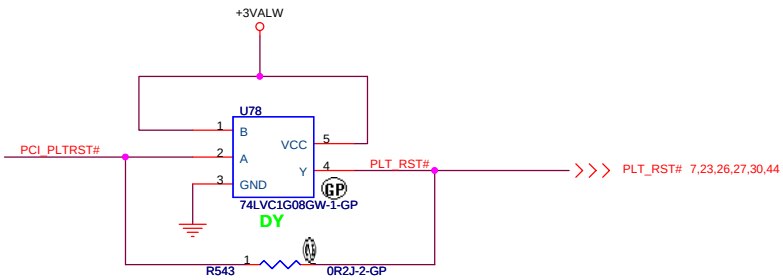

+3VS
+3VS_CK505
+3VS_CK505_IO
L3
SBK160808T-601Y-N-GP
0324 SI
C300
C706
C713
C715
C718
C723
C705
SC10U10V5ZY-1GP
SC1U16V2ZY-2GP
DY
0429 PV
X2
X-14D31818M-50GP
CLK_XTAL_IN
CLK_XTAL_OUT
C298
SC12P50V2JN-3GP
C292
SC12P50V2JN-3GP
U17
L4
0128 DB
C307
C721
C722
C724
C708
C707
C336
SC10U10V5ZY-1GP
SRC-5_EN/PCI-3
PIN44,45
0
PCI_STOP#/CPU_STOP#
1
SRC5
R155
10KR2J-3-GP
R148
10KR2J-3-GP
C349
SC4D7P50V2CN-1GP
R185
33R2J-2-GP
R193
33R2J-2-GP
FSA
CLK48_ICH
CLK48_5158
STP_PCI#
STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
R144
10KR2J-3-GP
MCH_CLK_REQ#
CLK_SATA_OE#
MCH_CLK_REQ#
PCLK_FWH
CLK_PCI_KBC
PCLK_ICH
R143
R145
R168
R186
475R2F-L1-GP
33R2J-2-GP
1017 DB
0425 PV
PCI2_TME
SRC-5_EN/PCI-3
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_ICH14
R139
33R2J-2-GP
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS 71.09355.B03
Realtek 71.00875.003
ICS9LPRS355BKLFT-GP
R149
10KR2J-3-GP
R157
10KR2J-3-GP
C333
C342
C318
SC4D7P50V2CN-1GP
CPUT0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
SRCT0/DOTT_96
SRCC0/DOTC_96
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
CLK_CPU_BCLK1
CLK_CPU_BCLK1#
CLK_MCH_BCLK1
CLK_MCH_BCLK1#
CLK_CPU_XDP1
CLK_CPU_XDP1#
CLK_PCIE_LAN1
CLK_PCIE_LAN1#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_MCH_3GPLL1
CLK_MCH_3GPLL1#
CLK_PCIE_ICH1
CLK_PCIE_ICH1#
CLK_PCIE_SATA1
CLK_PCIE_SATA1#
MCH_SSCDREFCLK1
MCH_SSCDREFCLK1#
CLK_MCH_DREFCLK1
CLK_MCH_DREFCLK1#
R111
R112
R113
R114
R115
R116
R117
R118
R119
R120
R151
R152
R176
R177
R174
R175
R172
R173
R170
R171
0R0402-PAD
0429 PV
0303 SI
R160
10KR2J-3-GP
R167
10KR2J-3-GP
27_SEL
1218
FS_C
FS_B
FS_A
CPU
1
0
1
100M
0
0
1
133M
0
1
1
166M
0
1
0
200M
0
0
0
266M
27_SEL
PIN 20
PIN 21
PIN 24
PIN 25
0
DOT96T
DOT96C
SRCT1/LCDT_100
SRCT1/LCDT_100
1
SRCT0
SRCC0
27M_NSS
27M_SS
R183
10KR2J-3-GP
R184
10KR2J-3-GP
ITP_EN
ITP_EN
Output
0
SRC8
1
CPU_ITP
+1.05VS
R154
0R2J-2-GP
R108
0R2J-2-GP
R142
56R2J-4-GP
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
CLK_BSEL2
CLK_BSEL1
CLK_BSEL0
R138
R104
R158
R133
R110
R166
10KR2J-3-GP
0R2J-2-GP
2K2R2J-2-GP
FSC
FSB
FSA
R141
R105
R163
1KR2J-1-GP
2K2R2J-2-GP
MCH_CLKSEL2
MCH_CLKSEL1
MCH_CLKSEL0
R191
R109
R132
1KR2J-1-GP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS355
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 16 of 48





BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



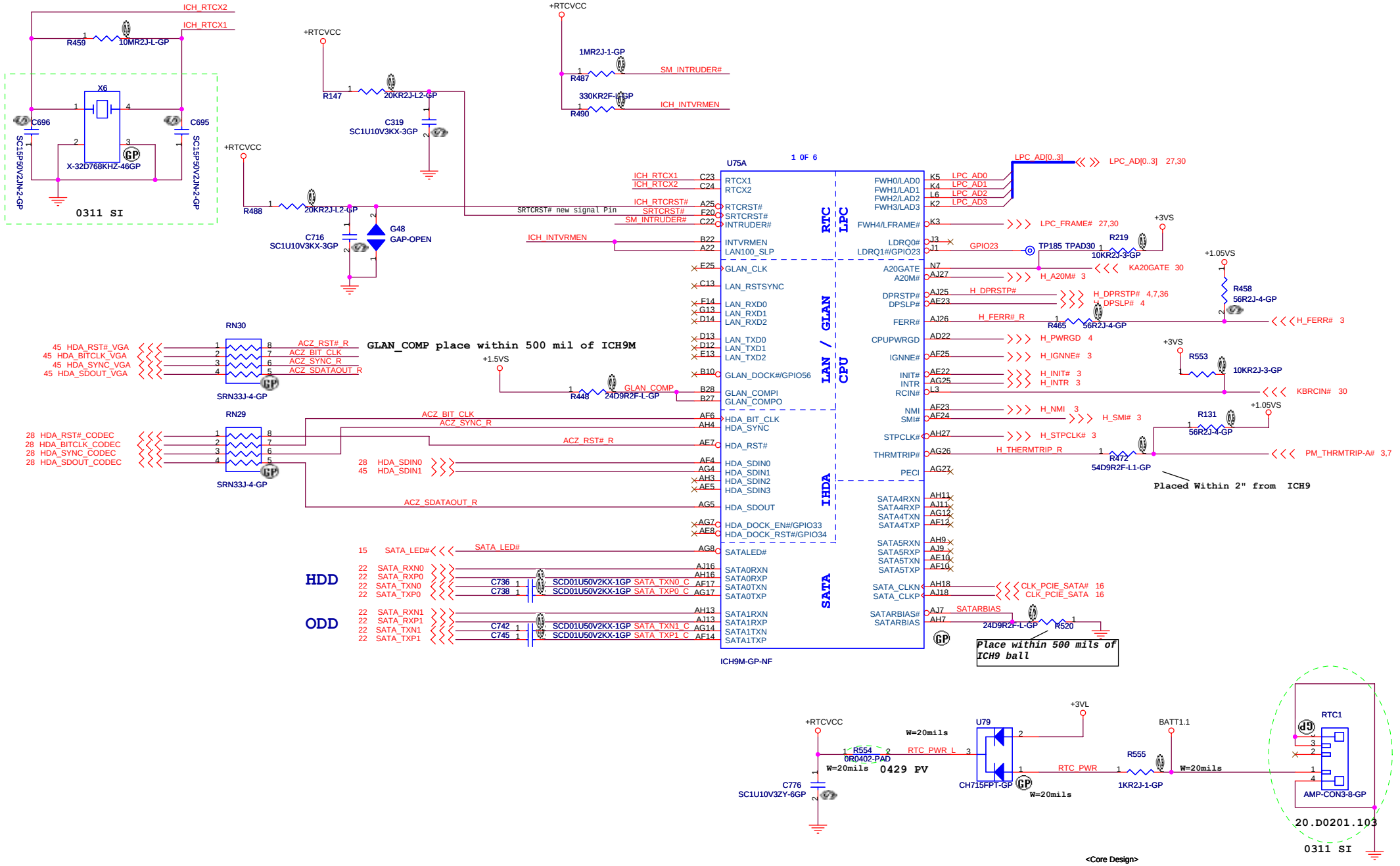
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 17 of 48



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

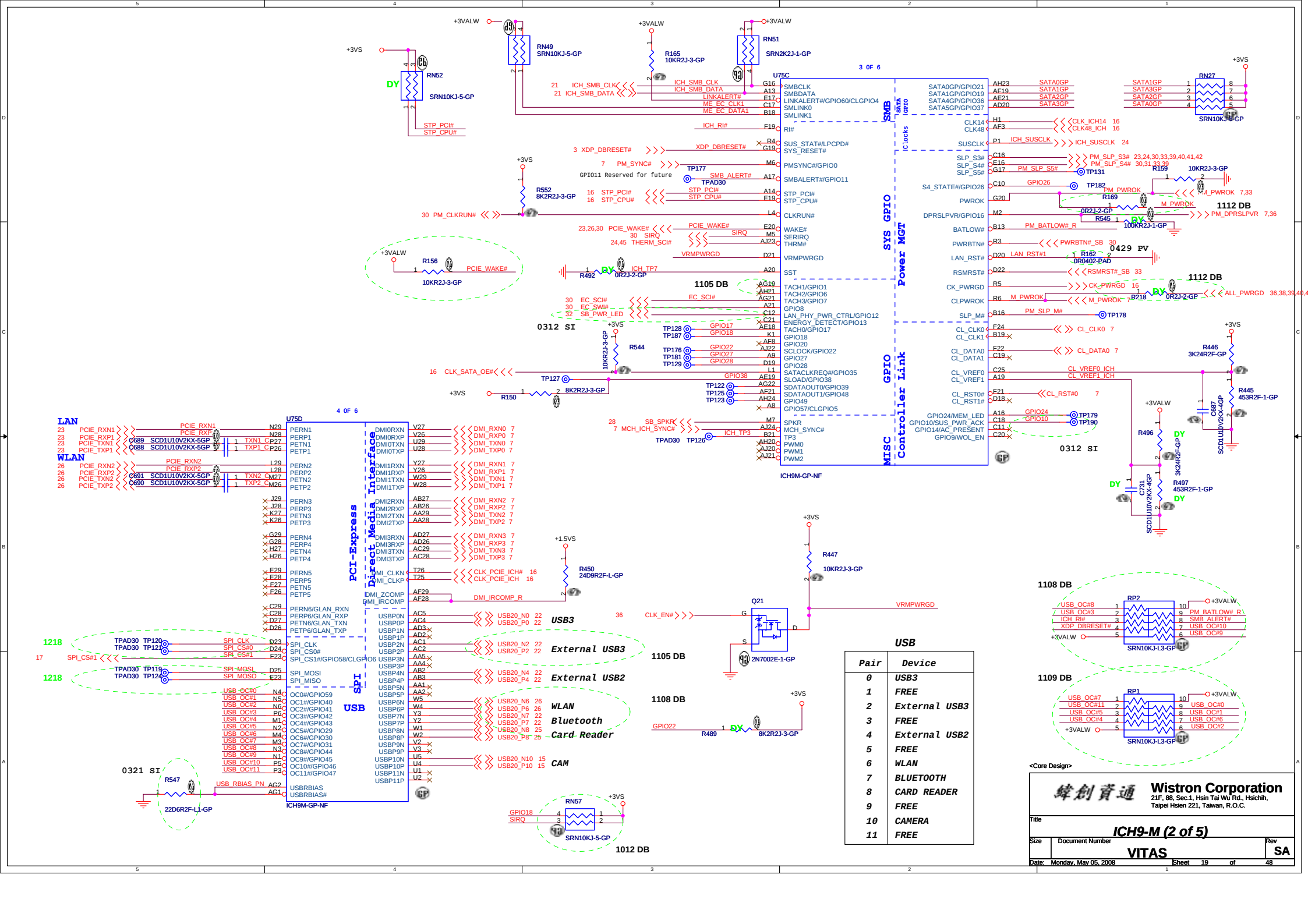
<Core Design>

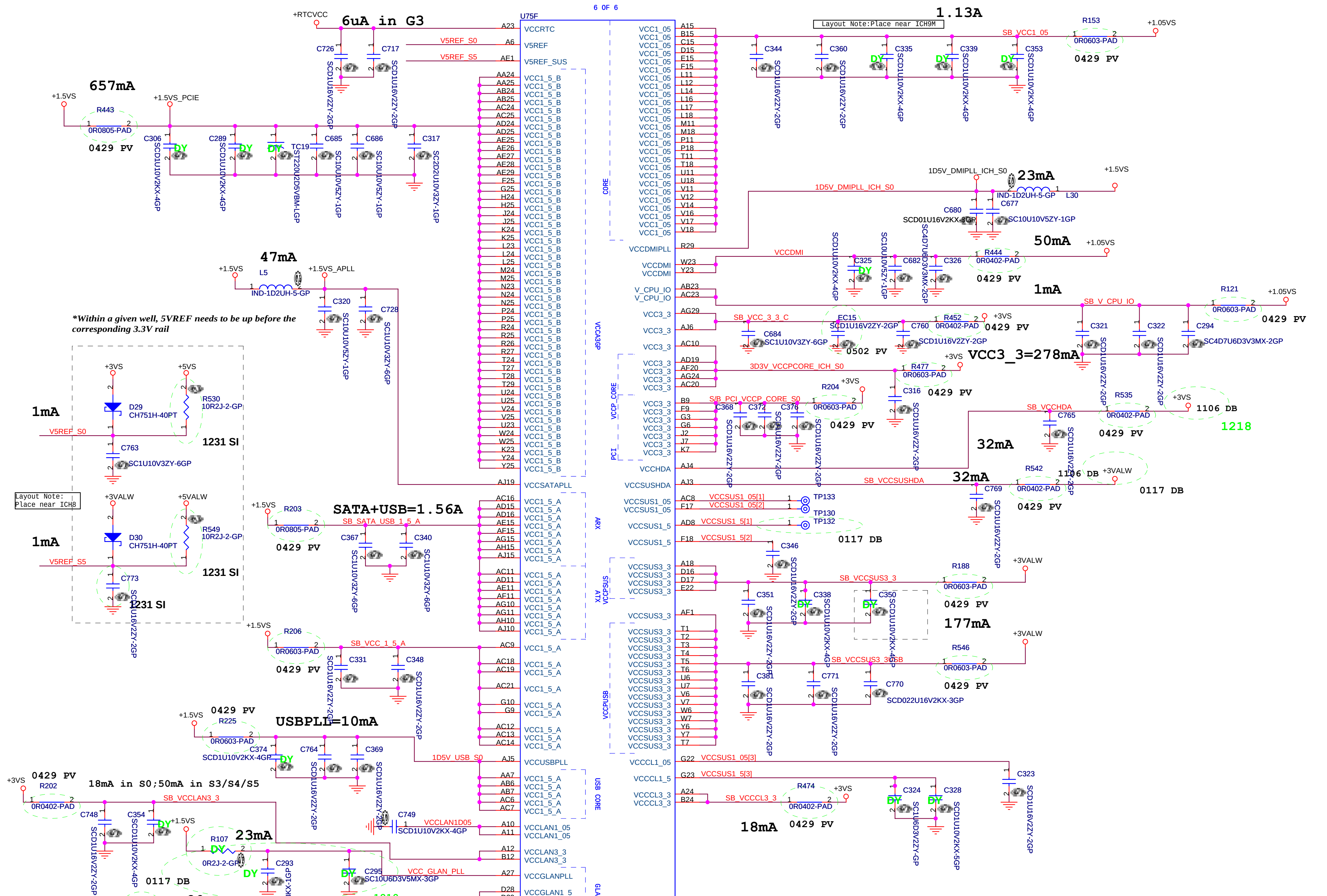
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH9-M (2 of 5)***

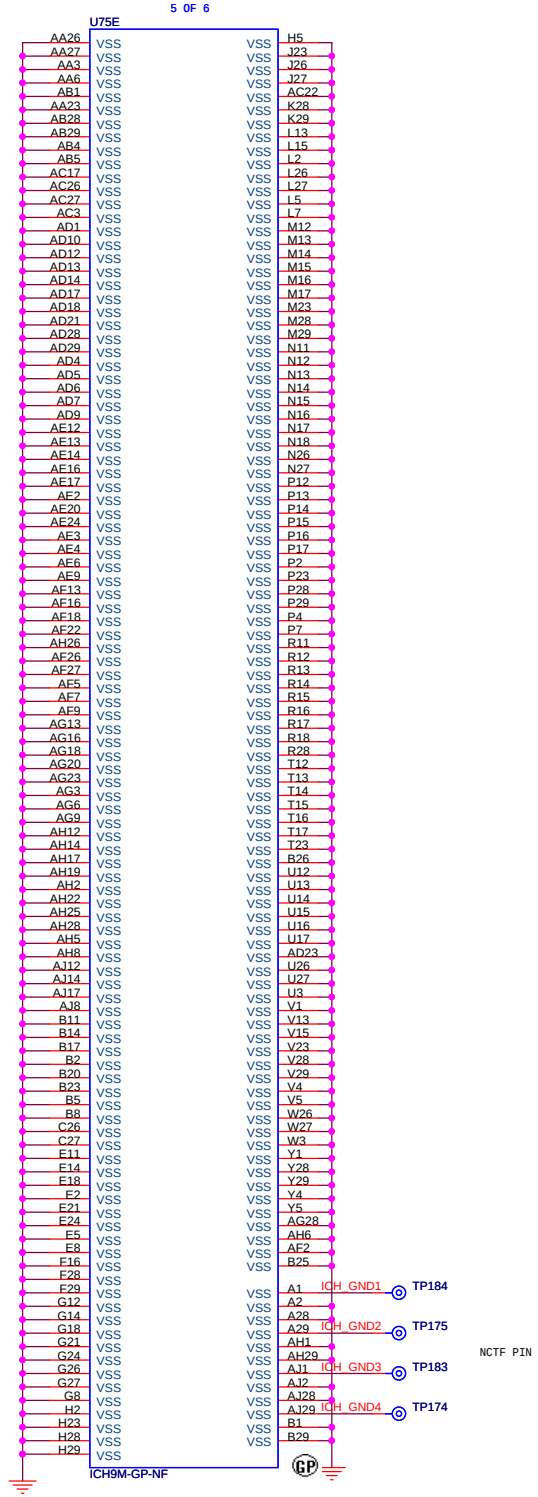
Size	Document Number	Rev
	VITAS	SA

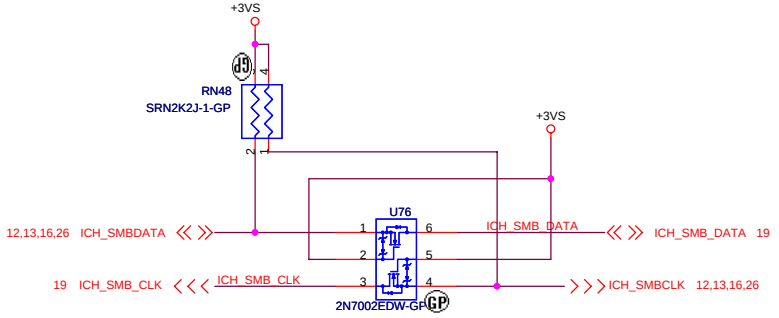
Date: Monday, May 05, 2008 Sheet 18 of 48


U75C
3 OF 6
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SMB
SATA GPIO
IClocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
ICH9M-GP-NF
U75D
4 OF 6
PCI-Express
Direct Media Interface
USB
SPI
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
USBRBIAS
USBRBIAS#
ICH9M-GP-NF
LAN
WLAN
PCIE_RXN1
PCIE_RXP1
PCIE_TXN1
PCIE_TXP1
PCIE_RXN2
PCIE_RXP2
PCIE_TXN2
PCIE_TXP2
SCD1U10V2KX-5GP
USB3
External USB3
External USB2
WLAN
Bluetooth
Card Reader
CAM
USB
Pair
Device
0 USB3
1 FREE
2 External USB3
3 FREE
4 External USB2
5 FREE
6 WLAN
7 BLUETOOTH
8 CARD READER
9 FREE
10 CAMERA
11 FREE
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 5)
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 19 of 48


6 OF 6
U75F
6uA in G3
1.13A
657mA
47mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
50mA
VCC3_3=278mA
32mA
177mA
18mA
Layout Note:Place near ICH9M
Layout Note: Place near ICH8
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B
VCC1_05
VCCDMIPLL
VCCDMI
V_CPU_IO
VCC3_3
VCCHDA
VCCSATAPLL
VCCSUSHDA
VCC1_5_A
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCUSBPLL
VCCCL1_05
VCCCL1_5
VCCCL3_3
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
ICH9M-GP-NF
CORE
VCCA3GP
VCCP_CORE
PCI
ARX
ATX
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
+RTCVCC
+1.5VS
+1.5VS_PCIE
+1.5VS_APLL
+1.05VS
+3VS
+5VS
+3VALW
+5VALW
1D5V_DMIPLL_ICH_S0
SB_VCC1_05
SB_V_CPU_IO
SB_VCC_3_3_C
3D3V_VCCPCORE_ICH_S0
SB_PCI_VCCP_CORE_S0
SB_VCCHDA
SB_VCCSUSHDA
SB_SATA_USB_1_5_A
SB_VCC_1_5_A
SB_VCCSUS3_3
SB_VCCSUS3_3_SB
SB_VCCLAN3_3
SB_VCCCL3_3
1D5V_USB_S0
VCCLAN1D05
VCC_GLAN_PLL
VCCGLAN1_5
3D3V_GLAN_S0
V5REF_S0
V5REF_S5
0429 PV
0117 DB
1106 DB
1231 SI
0502 PV
1218

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH9 (3/5)	
Size	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 20 of 48	

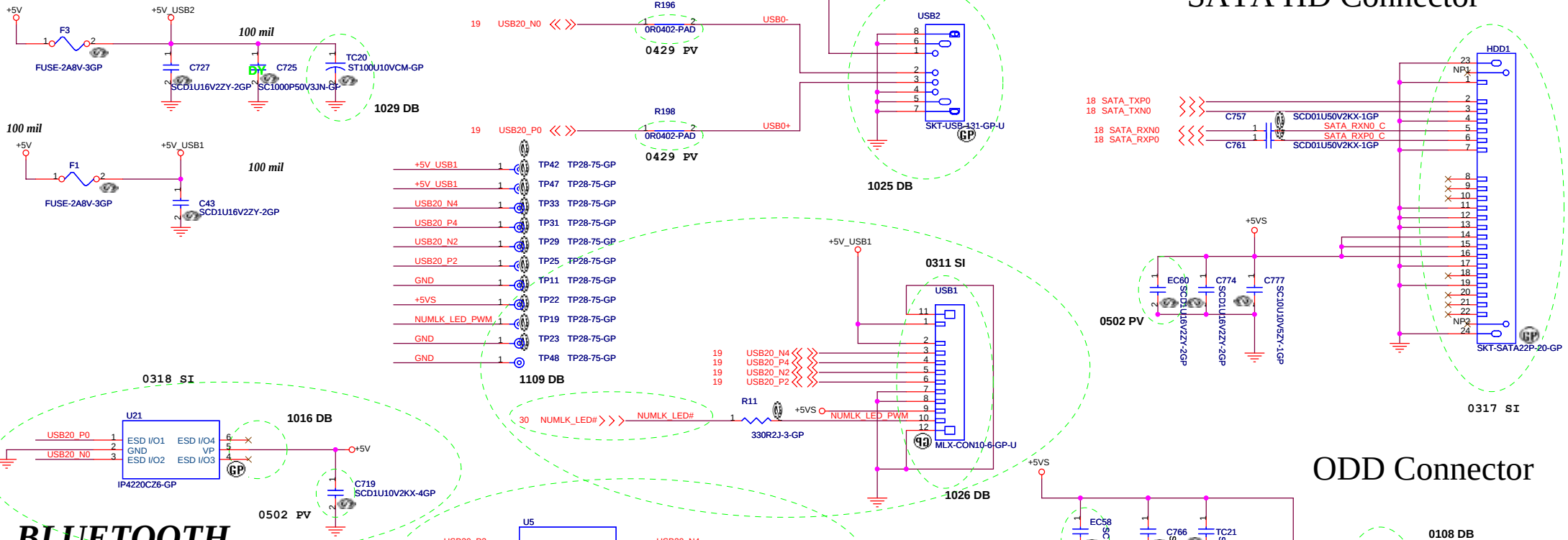




SMBUS

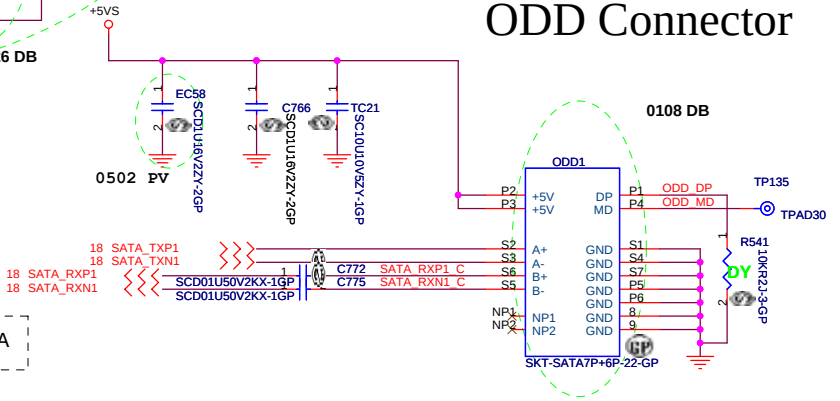
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*ICH9-M (4 of 4)*		
Size	Document Number: VITAS		Rev: SA
Date: Monday, May 05, 2008	Sheet 21 of 48		

USB PORT

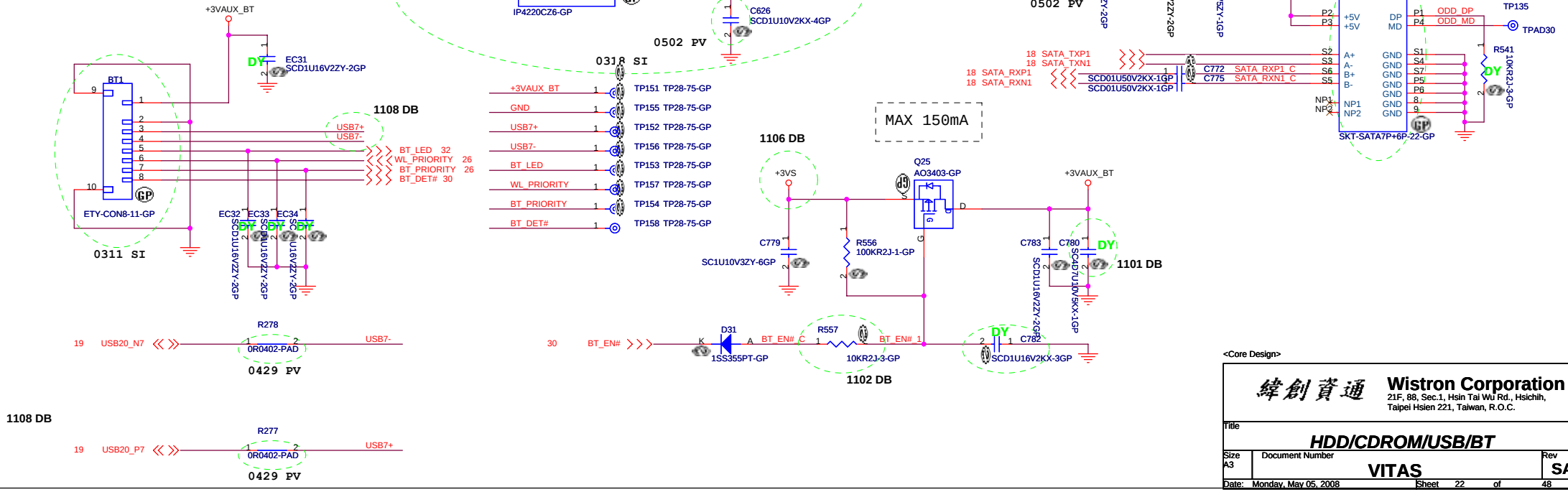


SATA HD Connector

ODD Connector



BLUETOOTH



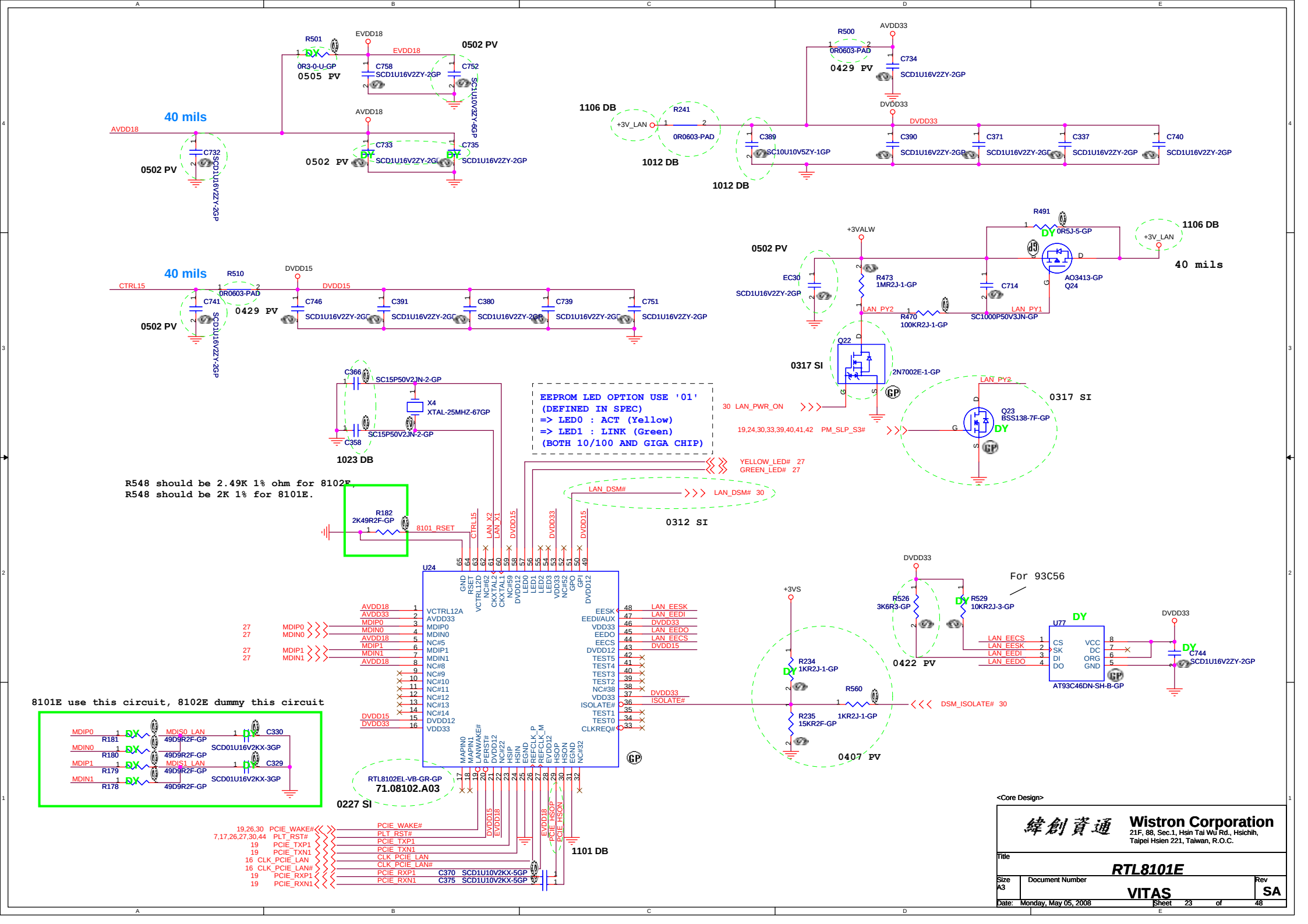
<Core Design>

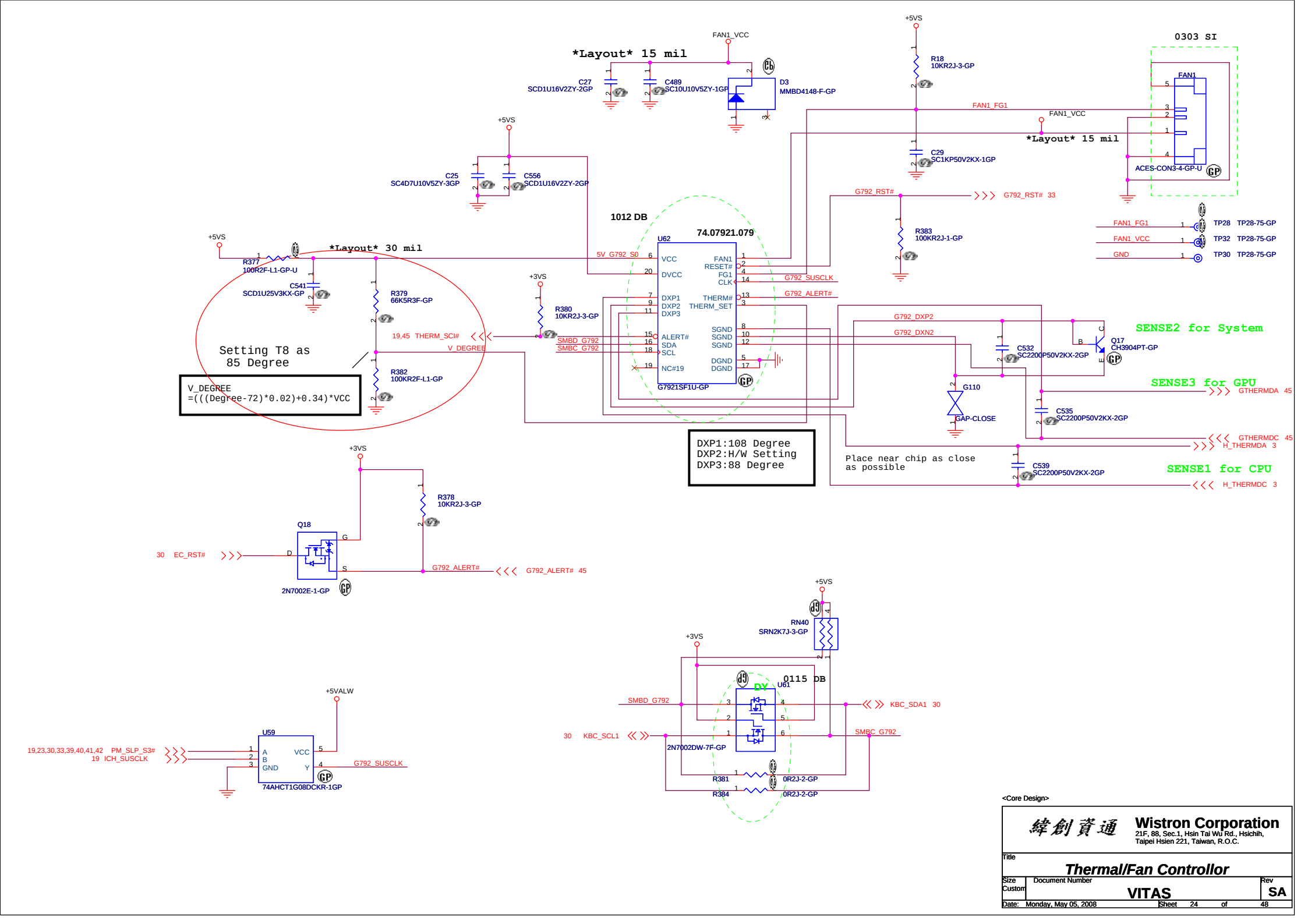
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/USB/BT

Size: A3 | Document Number: VITAS | Rev: SA

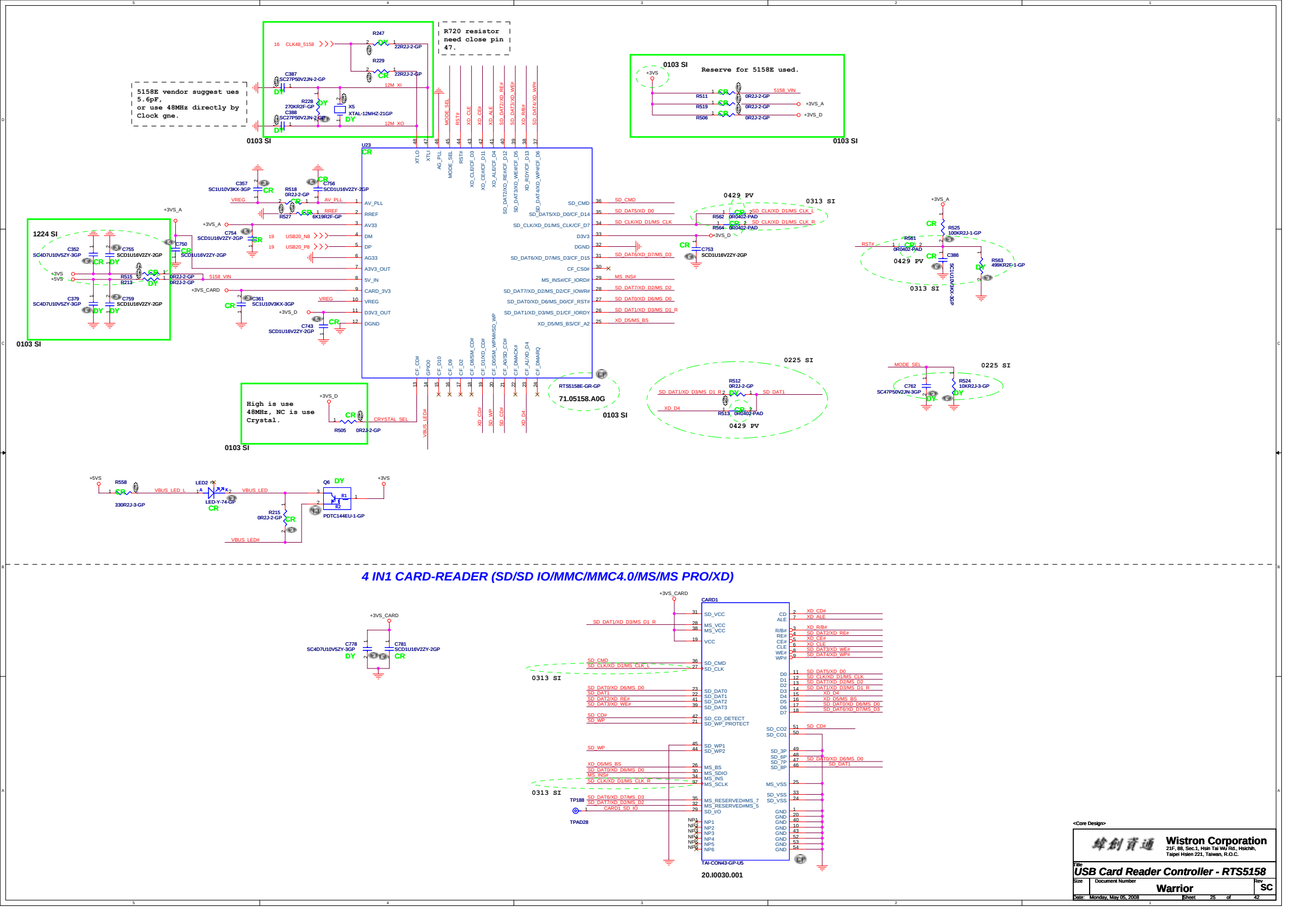
Date: Monday, May 05, 2008 | Sheet 22 of 48


R501
EVDD18
0R3-0-U-GP
0505 PV
0502 PV
C758
SCD1U16V2ZY-2GP
C752
SC1U10V3ZY-6GP
40 mils
AVDD18
C732
SCD1U16V2ZY-2GP
C733
C735
R500
AVDD33
0R0603-PAD
0429 PV
C734
1106 DB
R241
+3V_LAN
1012 DB
DVDD33
C389
SC10U10V5ZY-1GP
C390
C371
C337
C740
R491
DY
0R5J-5-GP
+3VALW
EC30
R473
1MR2J-1-GP
C714
AO3413-GP
Q24
LAN_PY2
LAN_PY1
R470
100KR2J-1-GP
SC1000P50V3JN-GP
Q22
0317 SI
2N7002E-1-GP
30 LAN_PWR_ON
19,24,30,33,39,40,41,42 PM_SLP_S3#
Q23
BSS138-7F-GP
R510
DVDD15
CTRL15
C741
C746
C391
C380
C739
C751
C366
SC15P50V2JN-2-GP
X4
XTAL-25MHZ-67GP
C358
1023 DB
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 AND GIGA CHIP)
YELLOW_LED# 27
GREEN_LED# 27
R548 should be 2.49K 1% ohm for 8102E.
R548 should be 2K 1% for 8101E.
R182
2K49R2F-GP
8101_RSET
LAN_DSM#
LAN_DSM# 30
0312 SI
U24
RTL8102EL-VB-GR-GP
71.08102.A03
0227 SI
1101 DB
8101E use this circuit, 8102E dummy this circuit
MDIP0
MDIN0
MDIP1
MDIN1
R181
R180
R179
R178
49D9R2F-GP
MDI0_LAN
MDI1_LAN
C330
C329
SCD01U16V2KX-3GP
+3VS
R234
1KR2J-1-GP
R235
15KR2F-GP
R560
DSM_ISOLATE# 30
0407 PV
For 93C56
R526
3K6R3-GP
R529
10KR2J-3-GP
0422 PV
U77
AT93C46DN-SH-B-GP
LAN_EECS
LAN_EESK
LAN_EEDI
LAN_EEDO
C744
SCD1U16V2ZY-2GP
19,26,30 PCIE_WAKE#
7,17,26,27,30,44 PLT_RST#
19 PCIE_TXP1
19 PCIE_TXN1
16 CLK_PCIE_LAN
16 CLK_PCIE_LAN#
19 PCIE_RXP1
19 PCIE_RXN1
C370
C375
SCD1U10V2KX-5GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8101E
Size A3
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
Sheet 23 of 48

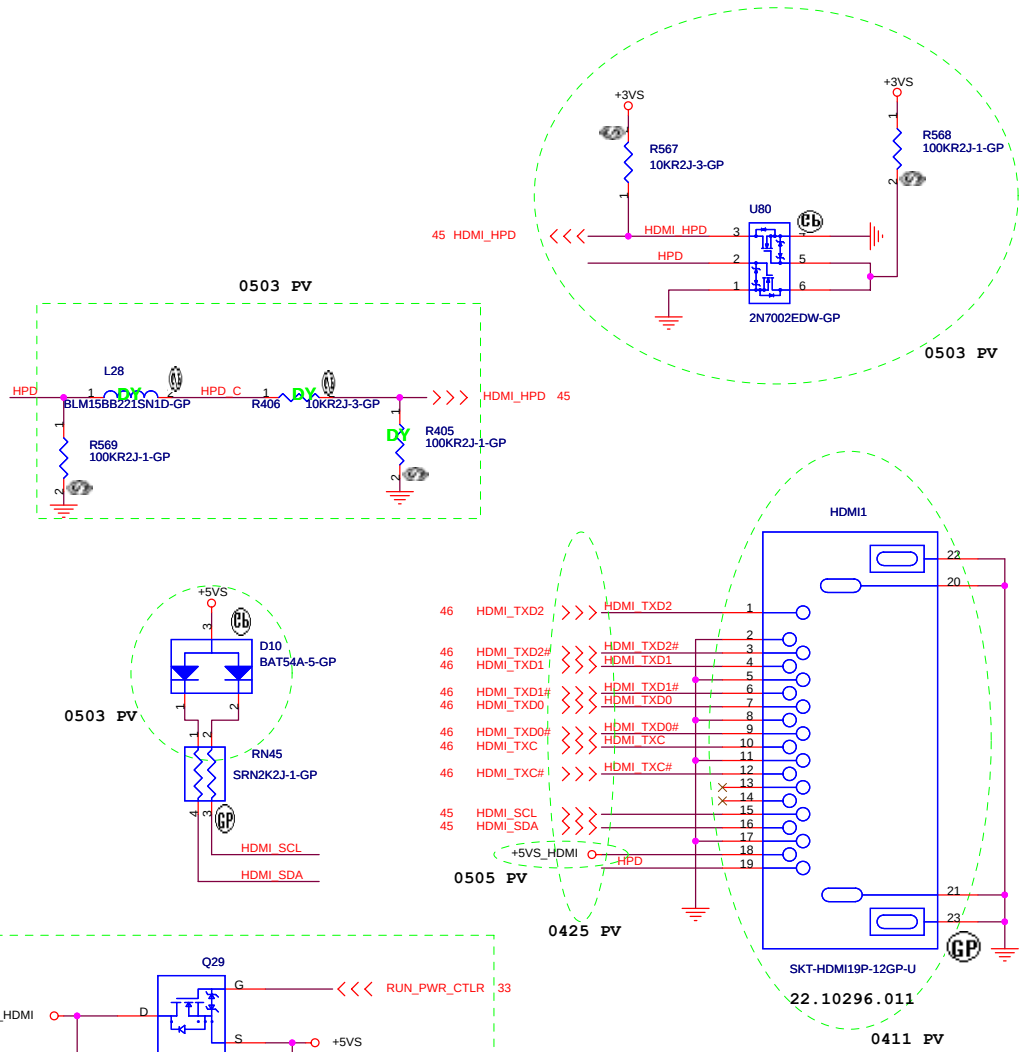


<Core Design>

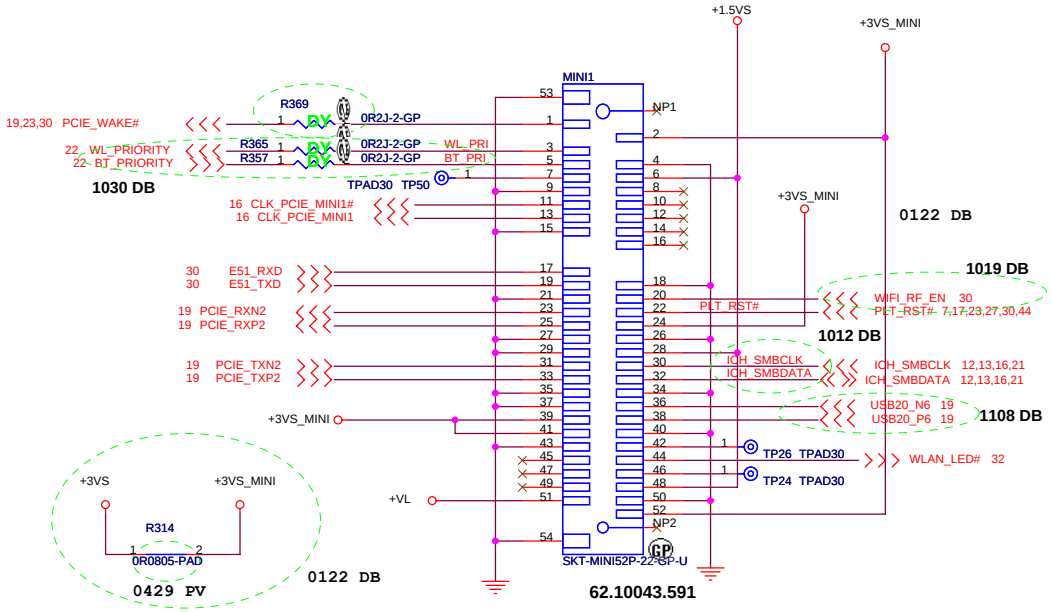
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Thermal/Fan Controllor***
Size: Custom	Document Number: **VITAS**
Rev	**SA**
Date: Monday, May 05, 2008	Sheet 24 of 48

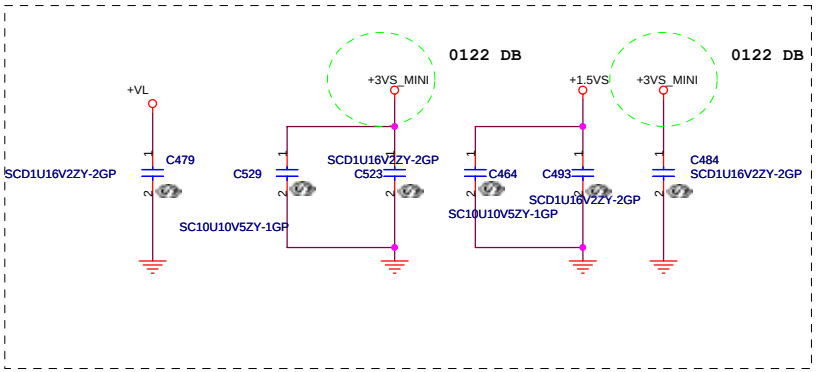

5158E vendor suggest ues 5.6pF, or use 48MHz directly by Clock gne.
R720 resistor need close pin 47.
0103 SI
Reserve for 5158E used.
1224 SI
High is use 48MHz, NC is use Crystal.
RTS5158E-GR-GP
71.05158.A0G
0225 SI
0429 PV
0313 SI
4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)
CARD1
TAI-CON43-GP-U5
20.I0030.001
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
USB Card Reader Controller - RTS5158
Warrior
Monday, May 05, 2008

HDMI Connector



Mini Card Connector1(802.11a/b/g)





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD/HDMI CONN .**

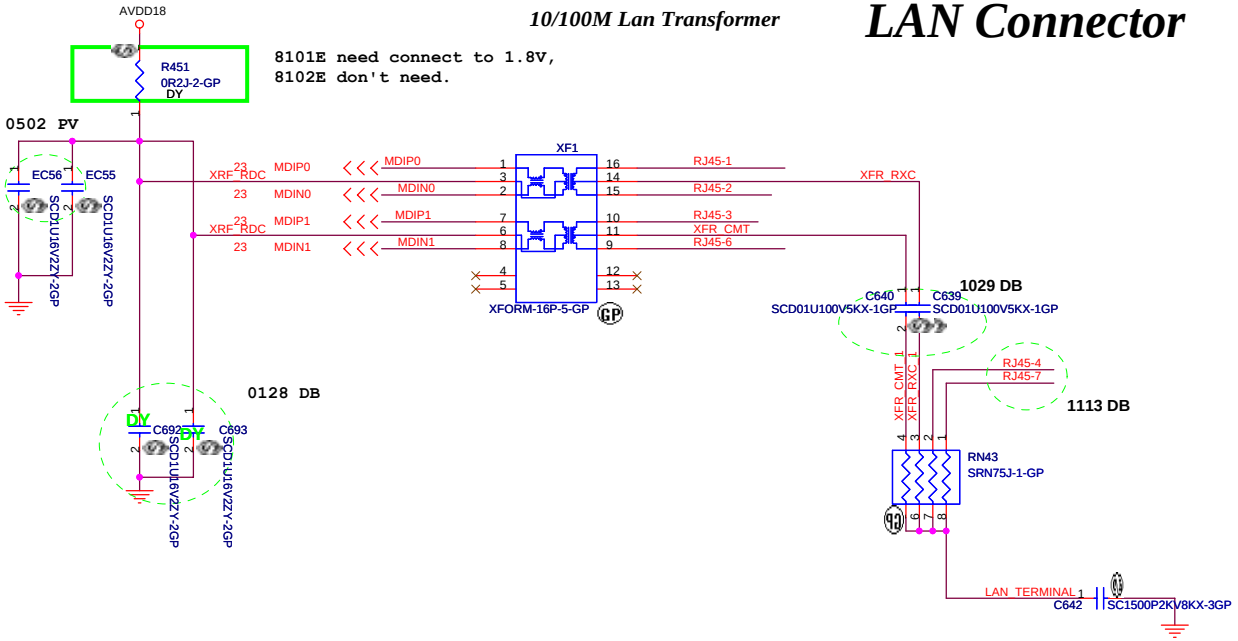
Size	Document Number	Rev
A3	VITAS	SA

Date: Monday, May 05, 2008 Sheet 26 of 48

LAN Connector

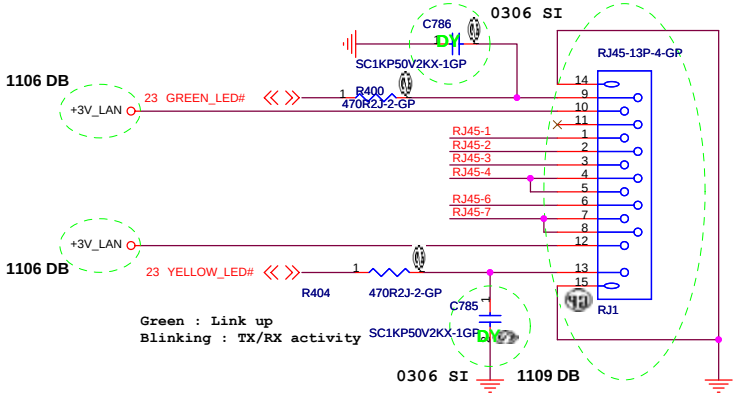
10/100M Lan Transformer

8101E need connect to 1.8V,
8102E don't need.



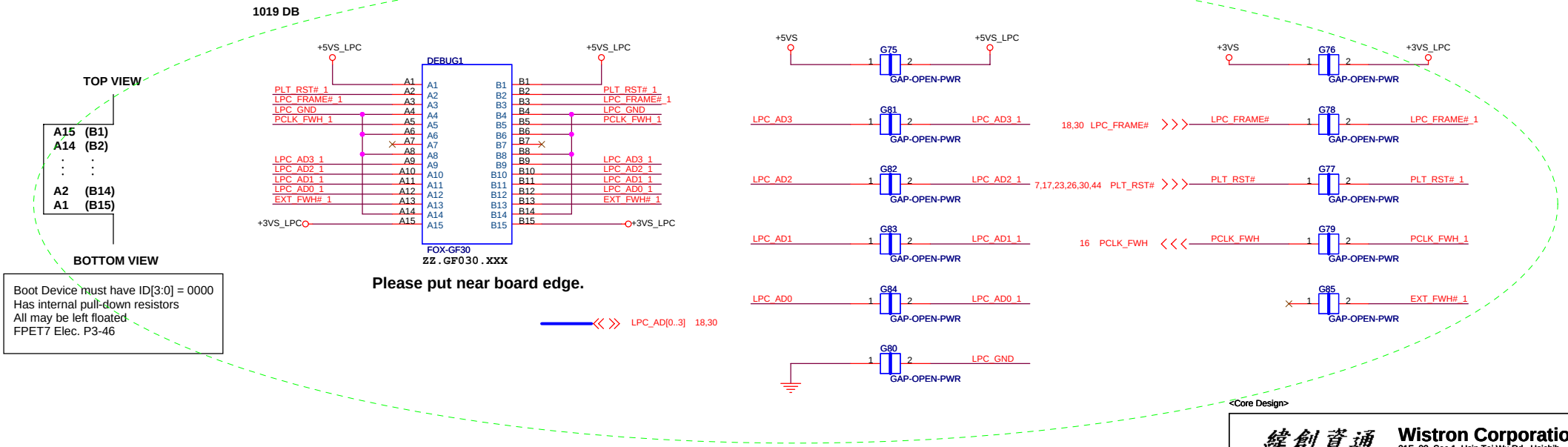
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

Golden Finger for Debug Board



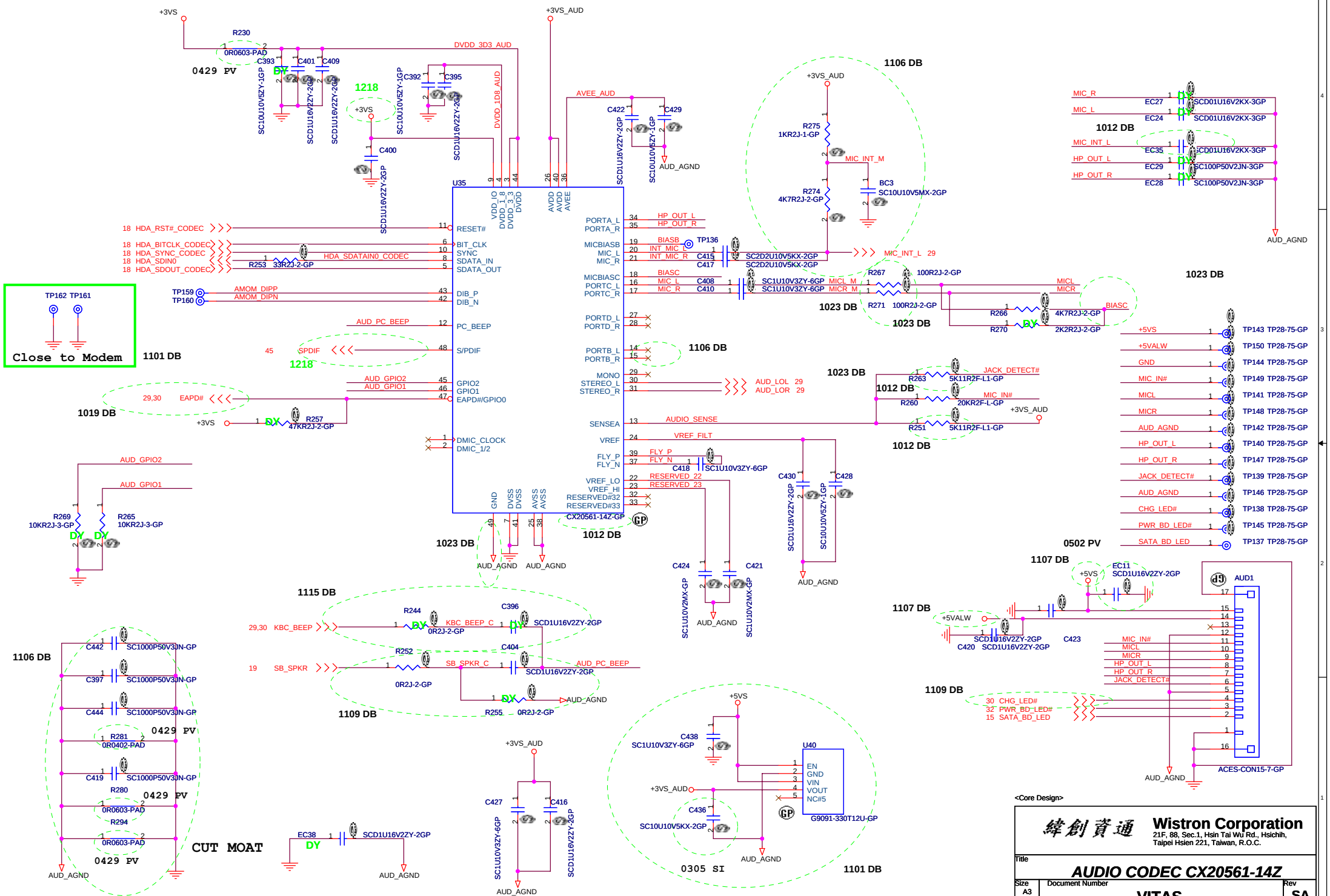
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

Please put near board edge.

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*LAN CONN/Debug*	
Size A3	Document Number VITAS	Rev SA
Date: Monday, May 05, 2008	Sheet 27 of 48	


U35
CX20561-14Z-GP
RESET#
BIT_CLK
SYNC
SDATA_IN
SDATA_OUT
DIB_P
DIB_N
PC_BEEP
S/PDIF
GPIO2
GPIO1
EAPD#/GPIO0
DMIC_CLOCK
DMIC_1/2
BIASB
MIC_L
MIC_R
BIASC
MONO
STEREO_L
STEREO_R
SENSEA
VREF
VREF_FILT
FLY_P
FLY_N
VREF_LO
VREF_HI
RESERVED#32
RESERVED#33
RESERVED_22
RESERVED_23
HP_OUT_L
HP_OUT_R
AUD_LOL 29
AUD_LOR 29
AUDIO_SENSE
MIC_INT_L 29
MIC_INT_M
MICL
MICR
JACK_DETECT#
MIC_IN#
KBC_BEEP_C
SB_SPKR_C
AUD_PC_BEEP
CHG_LED#
PWR_BD_LED#
SATA_BD_LED
AUD_AGND
+3VS
+3VS_AUD
DVDD_3D3_AUD
AVEE_AUD
Close to Modem
1101 DB
1106 DB
1012 DB
1023 DB
1019 DB
1115 DB
1109 DB
1107 DB
1012 DB
0502 PV
0429 PV
CUT MOAT
0305 SI
G9091-330T12U-GP
ACES-CON15-7-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC CX20561-14Z
VITAS
SA
Monday, May 05, 2008
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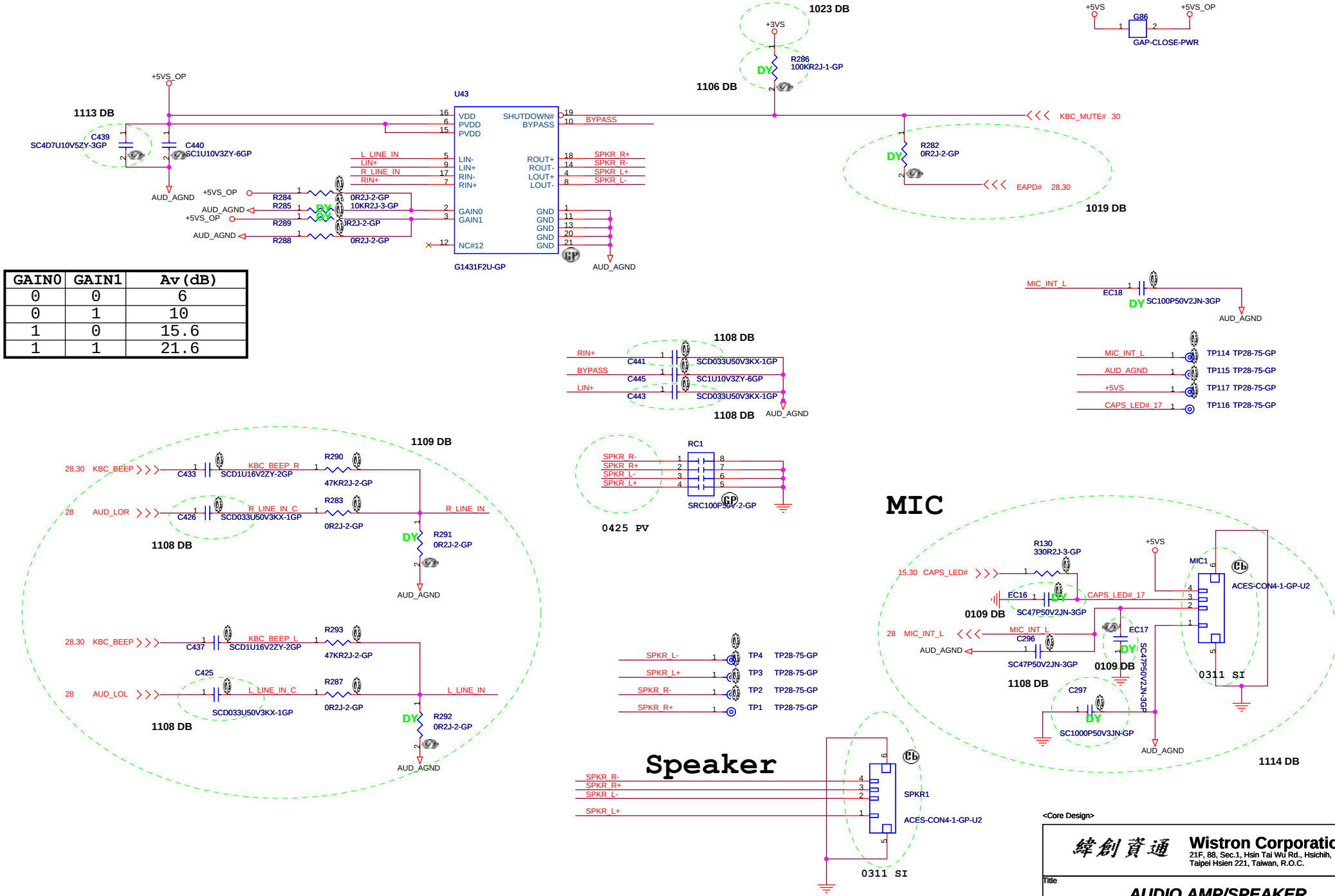
1023 DB
+3VS
R286
100KR2J-1-GP
DY
1106 DB
+5VS
+5VS_OP
G86
GAP-CLOSE-PWR
+5VS_OP
1113 DB
C439
SC4D7U10V5ZY-3GP
C440
SC1U10V3ZY-6GP
AUD_AGND
U43
VDD
PVDD
PVDD
LIN-
LIN+
RIN-
RIN+
GAIN0
GAIN1
NC#12
SHUTDOWN#
BYPASS
ROUT+
ROUT-
LOUT+
LOUT-
GND
L_LINE_IN
LIN+
R_LINE_IN
RIN+
BYPASS
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
R284
R285
R289
R288
0R2J-2-GP
10KR2J-3-GP
G1431F2U-GP
KBC_MUTE# 30
R282
0R2J-2-GP
EAPD# 28,30
1019 DB
GAIN0
GAIN1
Av(dB)
0
0
6
0
1
10
1
0
15.6
1
1
21.6
MIC_INT_L
EC18
SC100P50V2JN-3GP
TP114 TP28-75-GP
TP115 TP28-75-GP
TP117 TP28-75-GP
TP116 TP28-75-GP
AUD_AGND
CAPS_LED# 17
1108 DB
RIN+
BYPASS
LIN+
C441
C445
C443
SCD033U50V3KX-1GP
SC1U10V3ZY-6GP
1109 DB
28,30 KBC_BEEP
KBC_BEEP_R
C433
SCD1U16V2ZY-2GP
R290
47KR2J-2-GP
28 AUD_LOR
R_LINE_IN_C
C426
R283
R_LINE_IN
R291
0R2J-2-GP
KBC_BEEP_L
C437
R293
C425
L_LINE_IN_C
R287
L_LINE_IN
R292
RC1
SPKR_R-
SPKR_R+
SPKR_L-
SPKR_L+
SRC100P50V2-2-GP
0425 PV
MIC
R130
330R2J-3-GP
15,30 CAPS_LED#
EC16
SC47P50V2JN-3GP
0109 DB
MIC_INT_L
C296
EC17
C297
SC1000P50V3JN-GP
MIC1
ACES-CON4-1-GP-U2
0311 SI
1114 DB
TP4
TP3
TP2
TP1
TP28-75-GP
Speaker
SPKR1
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/SPEAKER
Size
A3
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
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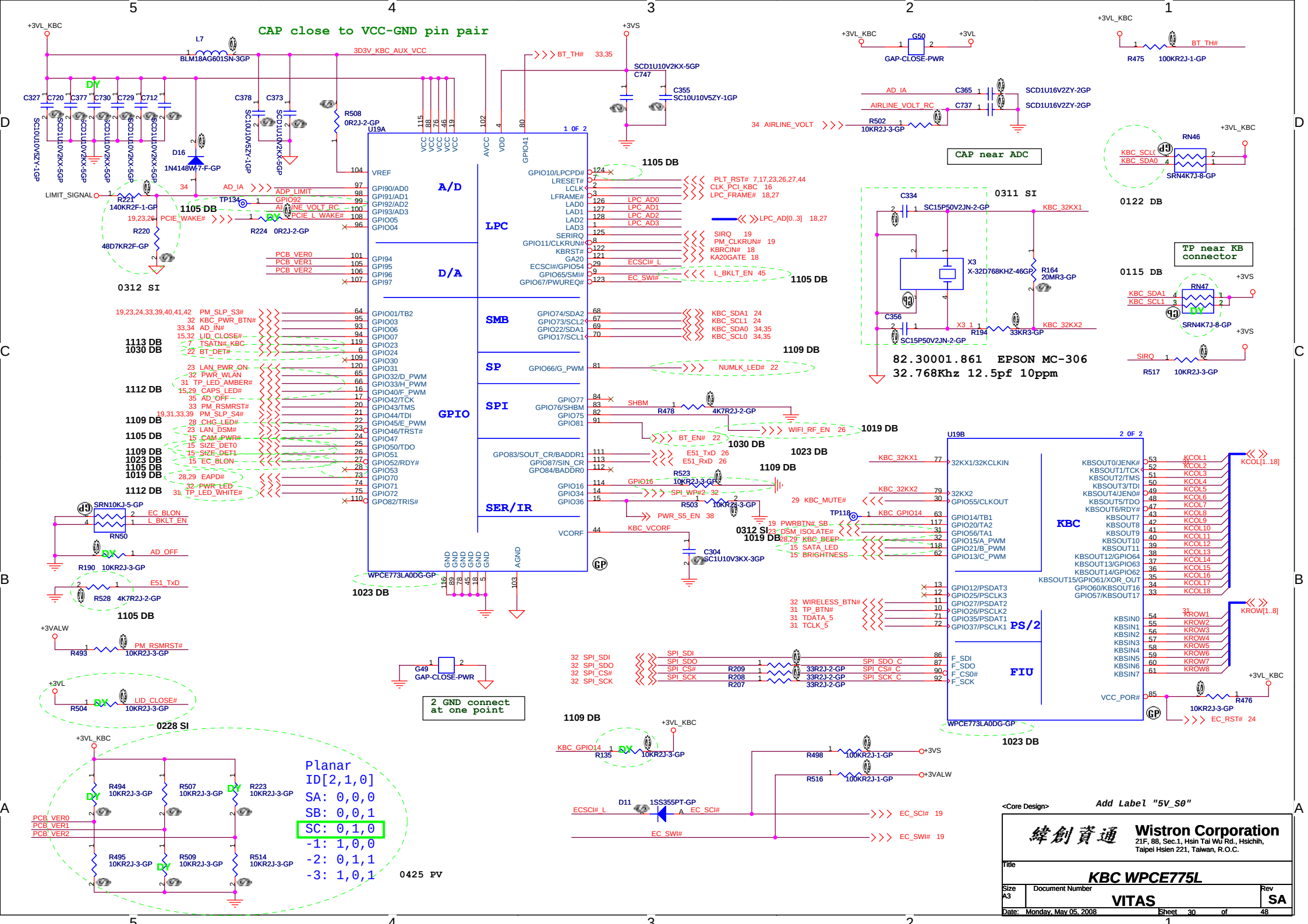
CAP close to VCC-GND pin pair
U19A
WPCE773LA0DG-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
1 0F 2
1105 DB
0312 SI
1113 DB
1030 DB
1112 DB
1109 DB
1023 DB
1019 DB
0228 SI
0425 PV
CAP near ADC
0311 SI
0122 DB
TP near KB connector
0115 DB
82.30001.861 EPSON MC-306
32.768Khz 12.5pf 10ppm
U19B
2 0F 2
KBC
PS/2
FIU
2 GND connect at one point
Planar
ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 1,0,0
-2: 0,1,1
-3: 1,0,1
Add Label "5V_S0"
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPCE775L
VITAS
SA
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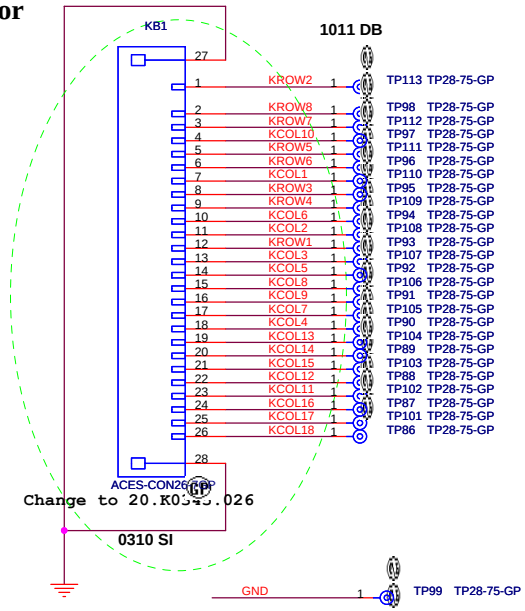
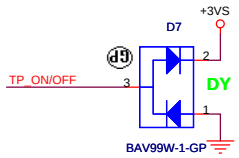
Internal KeyBoard Connector

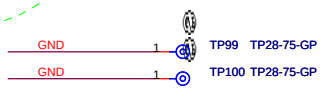
30 KROW[1..8]
30 KCOL[1..18]

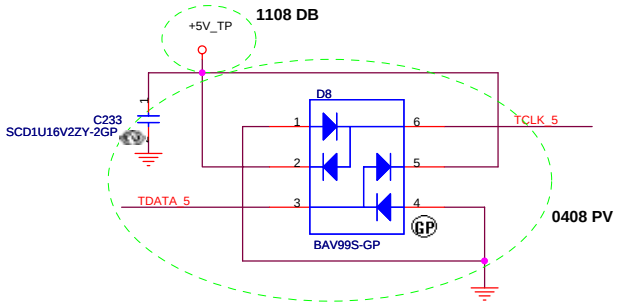
Keyboard matrix (from vendor)

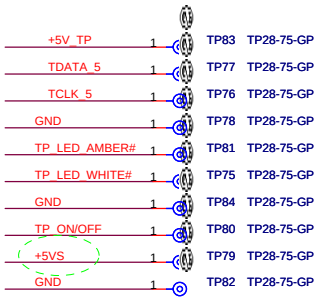
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1





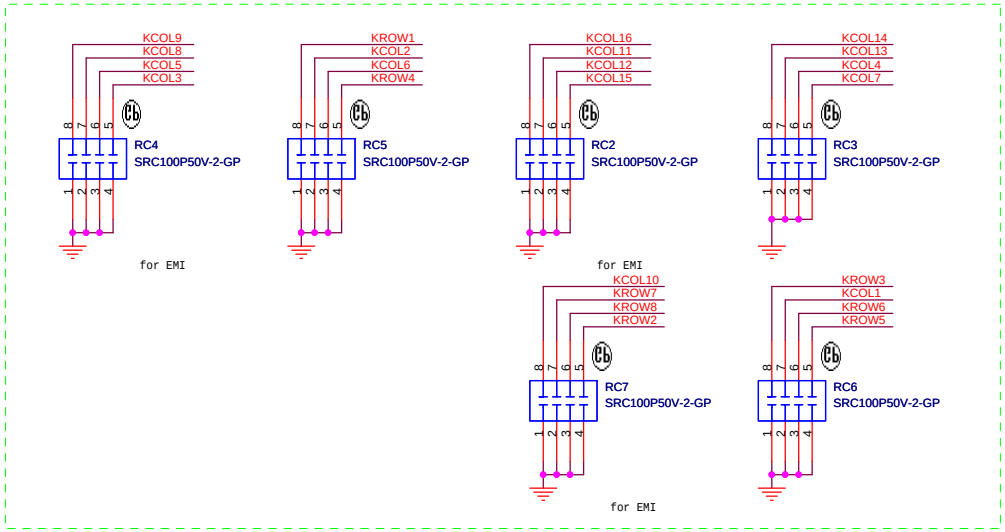






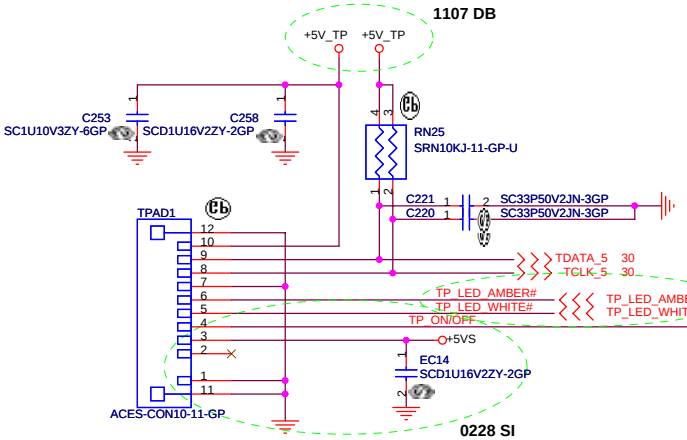
0228 SI

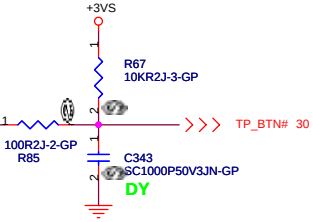
Please populate close TPAD1

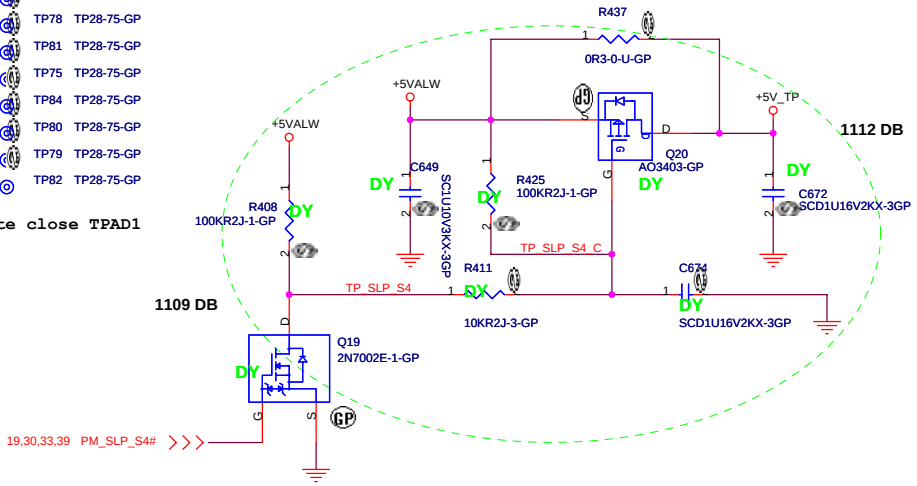


0408 PV

TouchPad Connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN

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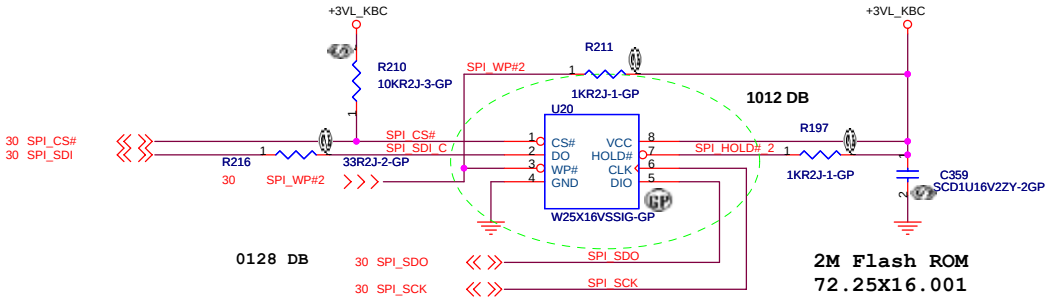

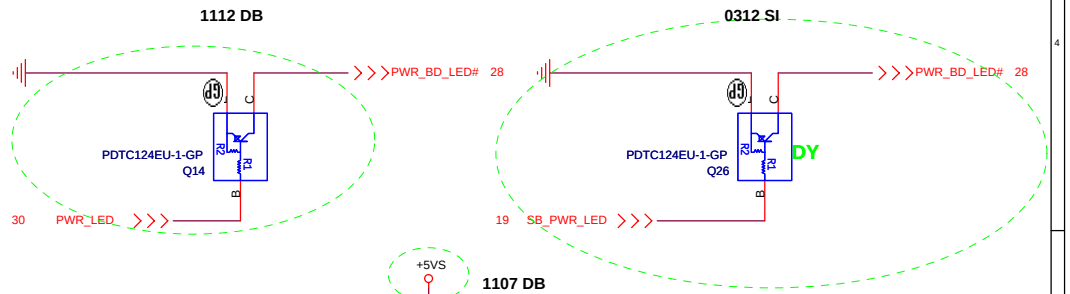

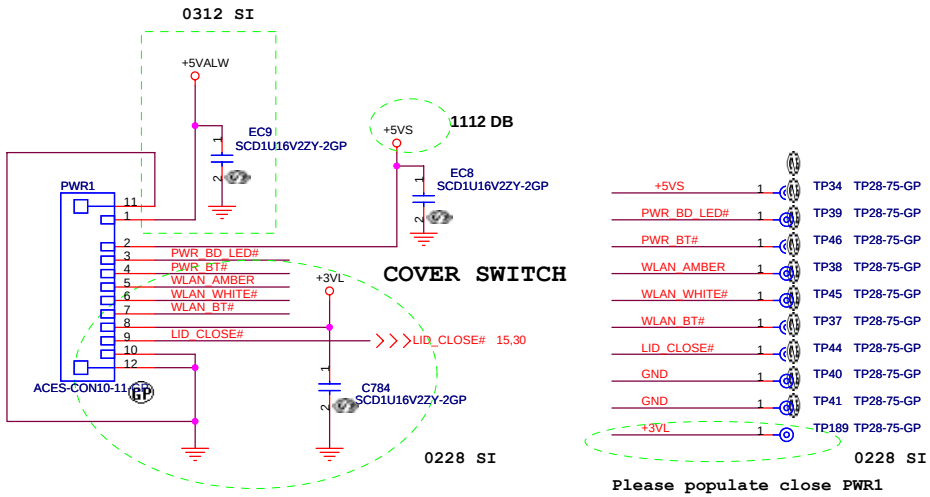

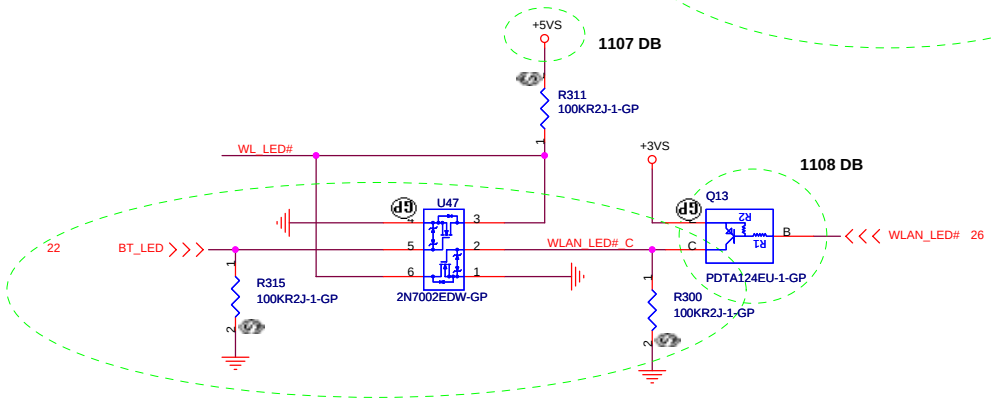

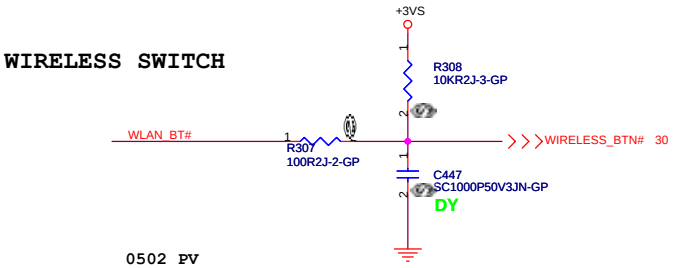

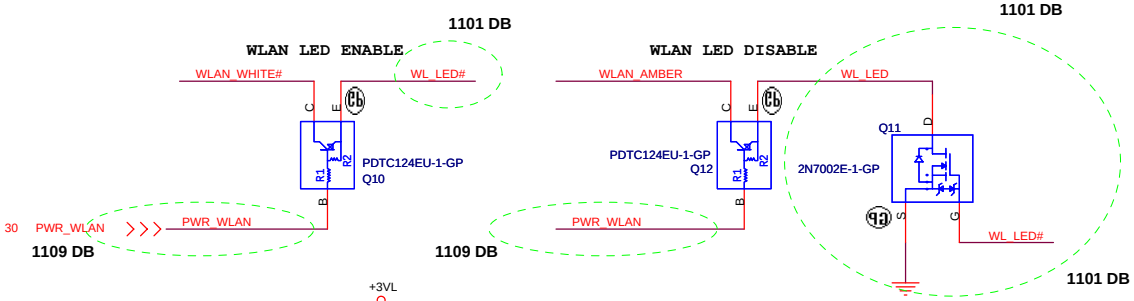

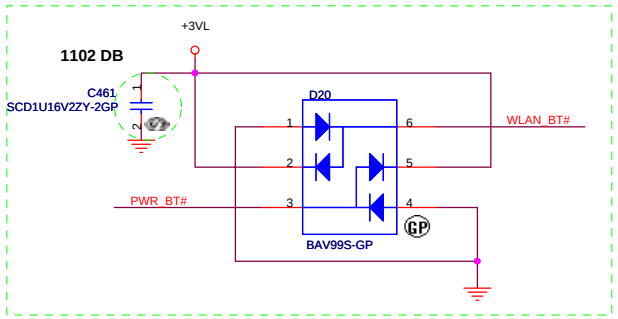

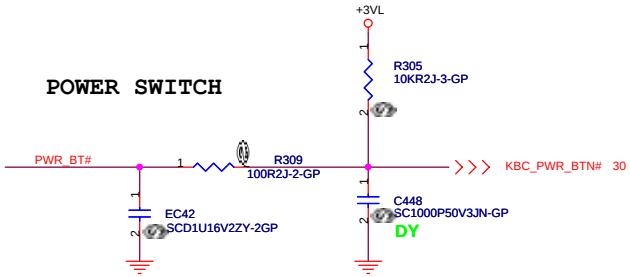

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and CONN.

Size: A3 | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 32 of 48
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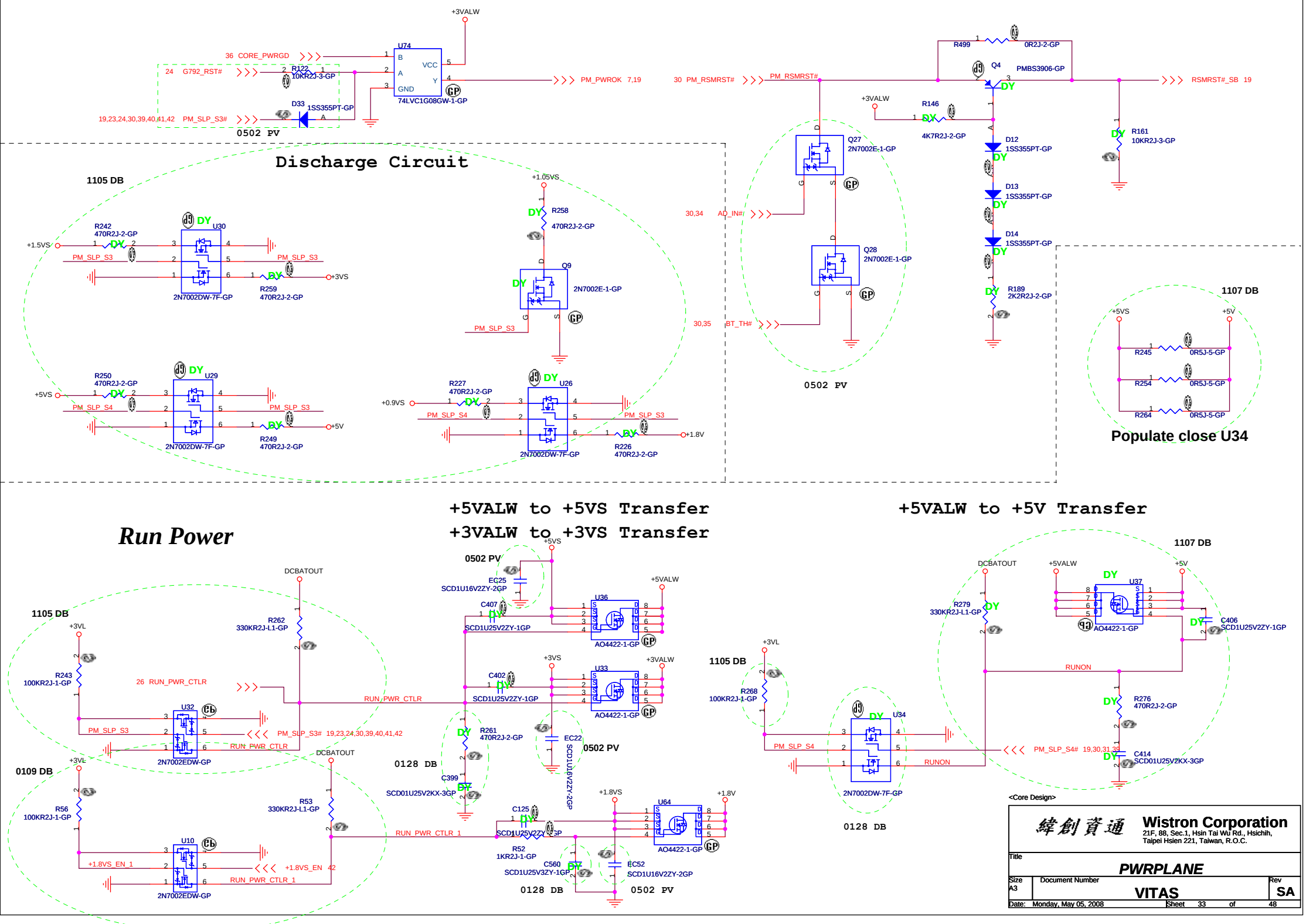
+3VALW
36 CORE_PWRGD
24 G792_RST#
R122
10KR2J-3-GP
U74
74LVC1G08GW-1-GP
PM_PWROK 7,19
19,23,24,30,39,40,41,42 PM_SLP_S3#
D33
1SS355PT-GP
0502 PV
30 PM_RSMRST#
PM_RSMRST#
R499
0R2J-2-GP
Q4
PMBS3906-GP
RSMRST#_SB 19
R146
4K7R2J-2-GP
R161
10KR2J-3-GP
Q27
2N7002E-1-GP
Q28
2N7002E-1-GP
30,34 AD_IN#
30,35 BT_TH#
D12
1SS355PT-GP
D13
1SS355PT-GP
D14
1SS355PT-GP
R189
2K2R2J-2-GP
0502 PV
Discharge Circuit
1105 DB
+1.5VS
R242
470R2J-2-GP
U30
2N7002DW-7F-GP
PM_SLP_S3
R259
470R2J-2-GP
+3VS
+1.05VS
R258
470R2J-2-GP
Q9
2N7002E-1-GP
+5VS
R250
470R2J-2-GP
U29
PM_SLP_S4
R249
470R2J-2-GP
+5V
+0.9VS
R227
470R2J-2-GP
U26
R226
470R2J-2-GP
+1.8V
1107 DB
R245
0R5J-5-GP
R254
0R5J-5-GP
R264
0R5J-5-GP
Populate close U34
Run Power
+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+5VALW to +5V Transfer
DCBATOUT
1105 DB
+3VL
R262
330KR2J-L1-GP
R243
100KR2J-1-GP
26 RUN_PWR_CTLR
U32
2N7002EDW-GP
PM_SLP_S3
PM_SLP_S3# 19,23,24,30,39,40,41,42
RUN_PWR_CTLR
0109 DB
R56
100KR2J-1-GP
R53
330KR2J-L1-GP
U10
+1.8VS_EN_1
+1.8VS_EN 42
RUN_PWR_CTLR_1
0502 PV
EC25
SCD1U16V2ZY-2GP
C407
SCD1U25V2ZY-1GP
U36
AO4422-1-GP
+5VALW
C402
U33
R261
470R2J-2-GP
EC22
SCD1U25V2ZY-1GP
0128 DB
C399
SCD01U25V2KX-3GP
C125
SCD1U25V2ZY-2GP
R52
1KR2J-1-GP
C560
SCD1U25V3ZY-1GP
U64
+1.8VS
+1.8V
EC52
SCD1U16V2ZY-2GP
0128 DB
0502 PV
1105 DB
R268
100KR2J-1-GP
U34
2N7002DW-7F-GP
0128 DB
1107 DB
R279
330KR2J-L1-GP
U37
AO4422-1-GP
C406
SCD1U25V2ZY-1GP
RUNON
R276
470R2J-2-GP
C414
SCD01U25V2KX-3GP
PM_SLP_S4# 19,30,31,35
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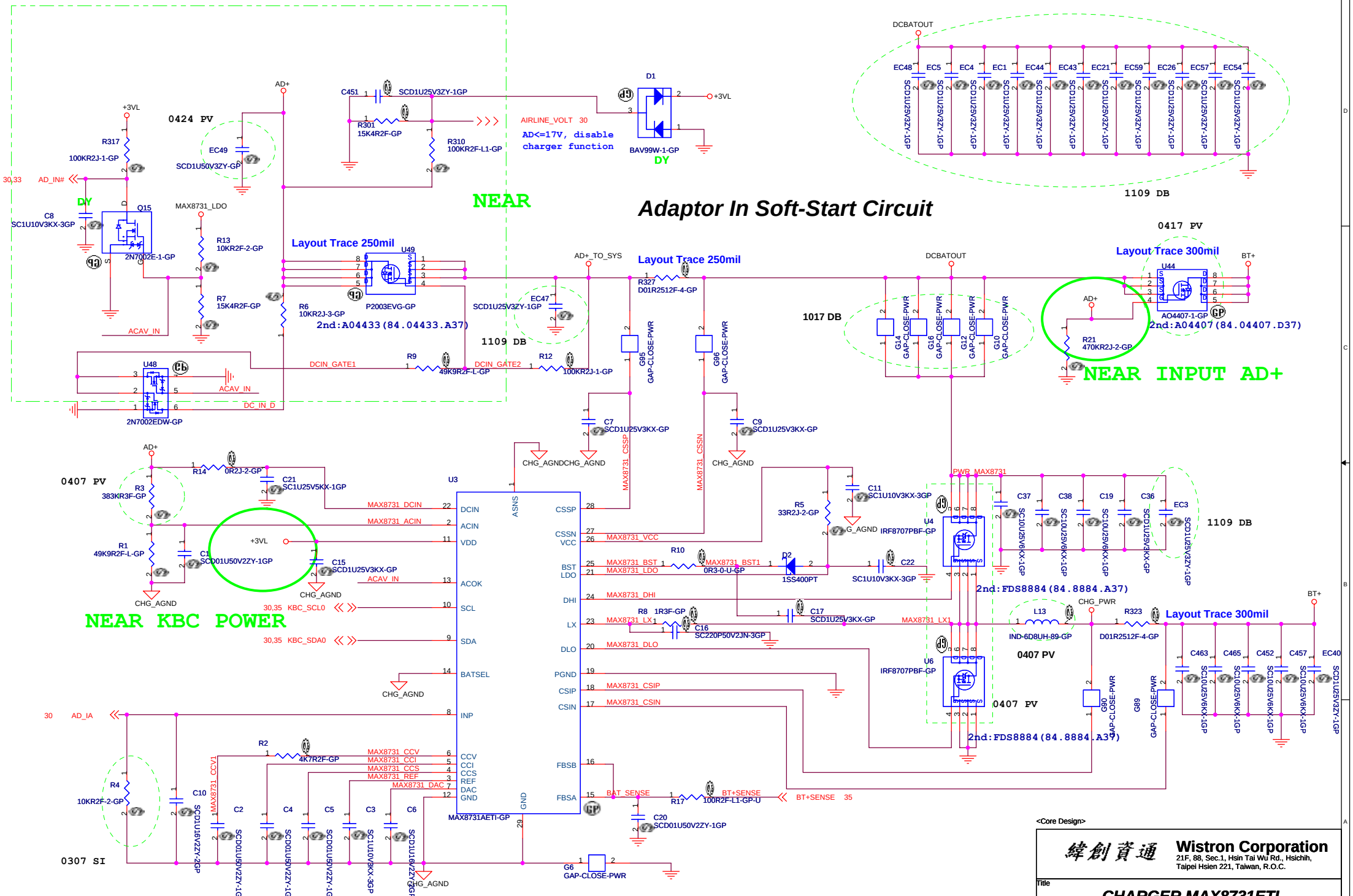
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PWRPLANE
Size A3
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
Sheet 33 of 48


Adaptor In Soft-Start Circuit
NEAR
NEAR INPUT AD+
NEAR KBC POWER
Layout Trace 250mil
Layout Trace 300mil
0424 PV
0417 PV
0407 PV
0307 SI
1109 DB
1017 DB
AD+
AD+_TO_SYS
DCBATOUT
BT+
+3VL
CHG_AGND
ACAV_IN
DC_IN_D
AIRLINE_VOLT 30
AD<=17V, disable charger function
2nd:A04433(84.04433.A37)
2nd:A04407(84.04407.D37)
2nd:FDS8884(84.8884.A37)
MAX8731_LDO
MAX8731AETI-GP
IRF8707PBF-GP
1SS400PT
IND-6D8UH-89-GP
Need Check MAXIM Sming Use MAX8731 or MAX8731A
Core Design
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8731ETI
Size A3
Document Number VITAS
Rev SA
Date: Monday, May 05, 2008
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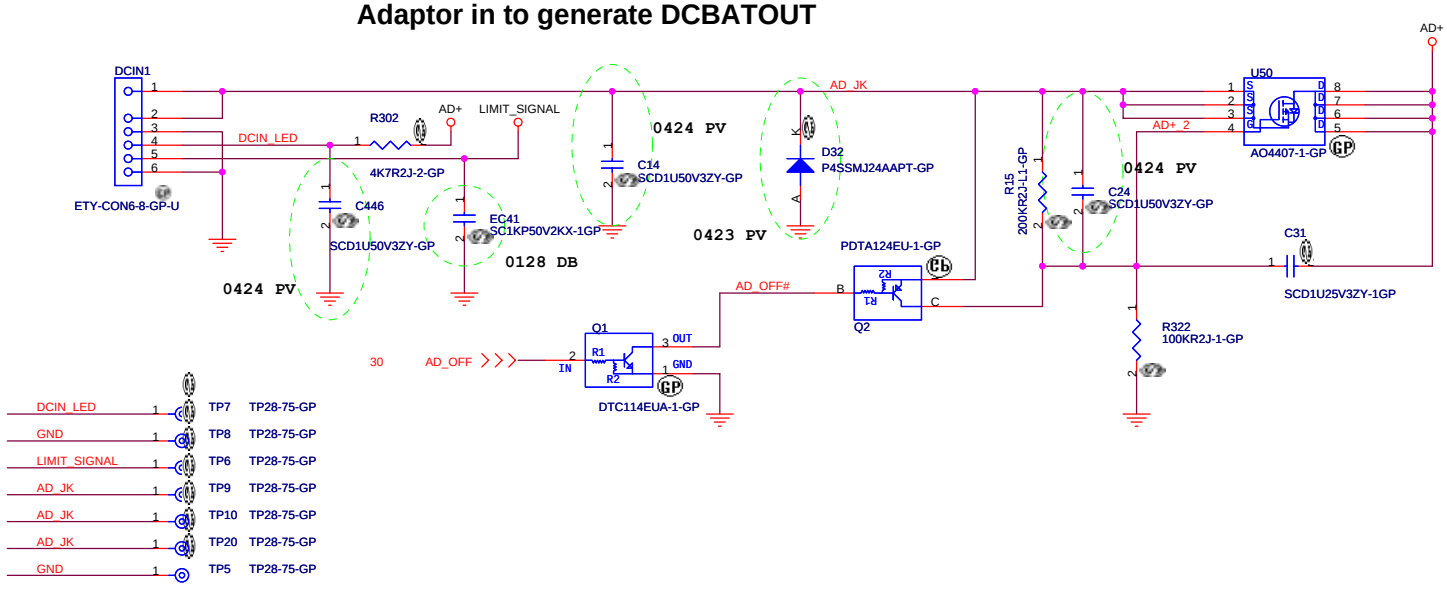
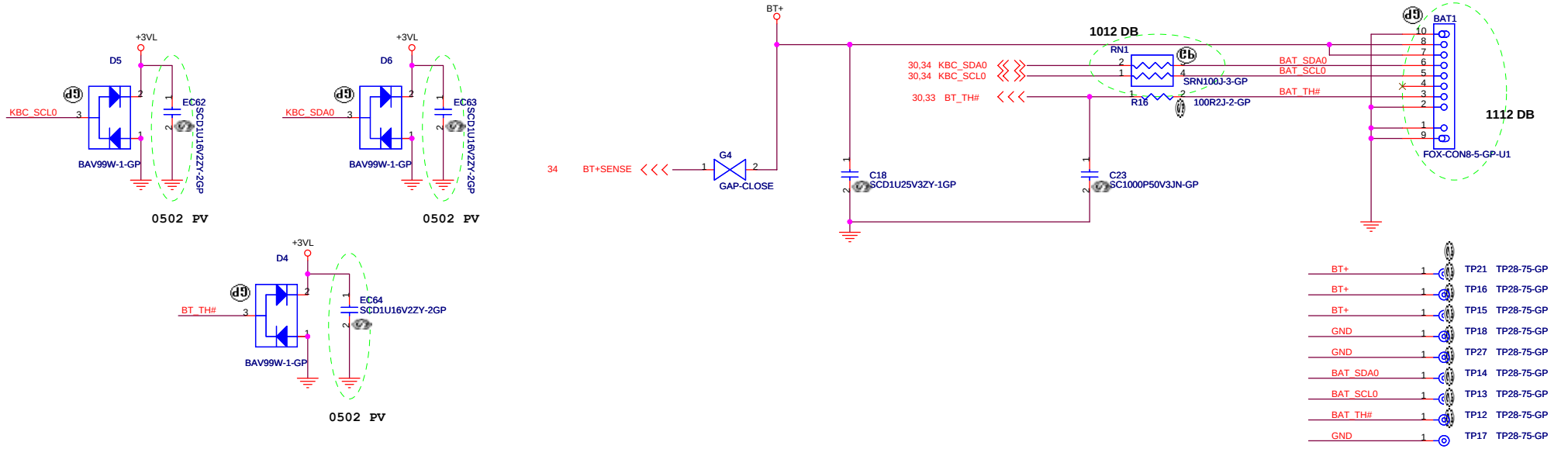
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

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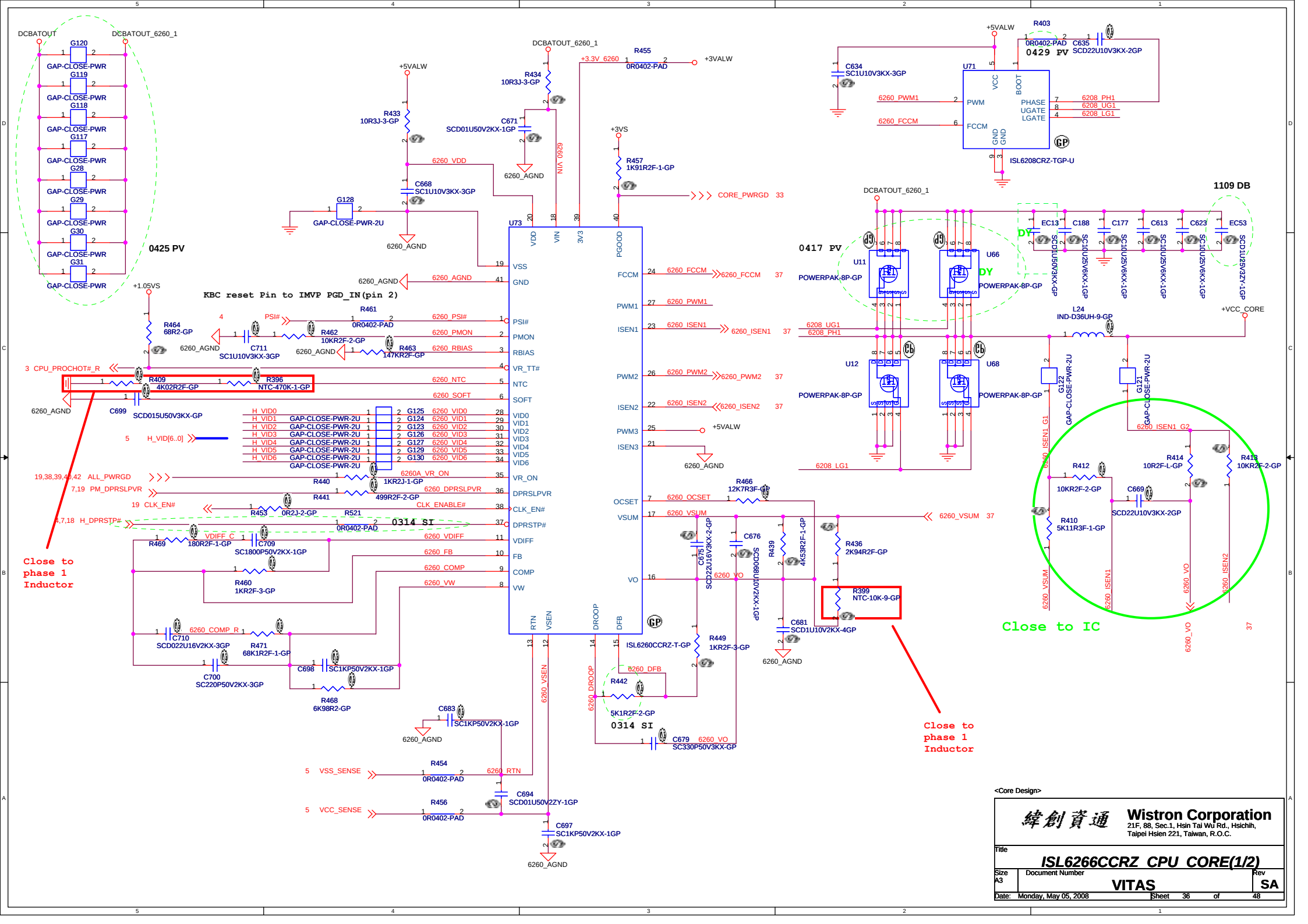

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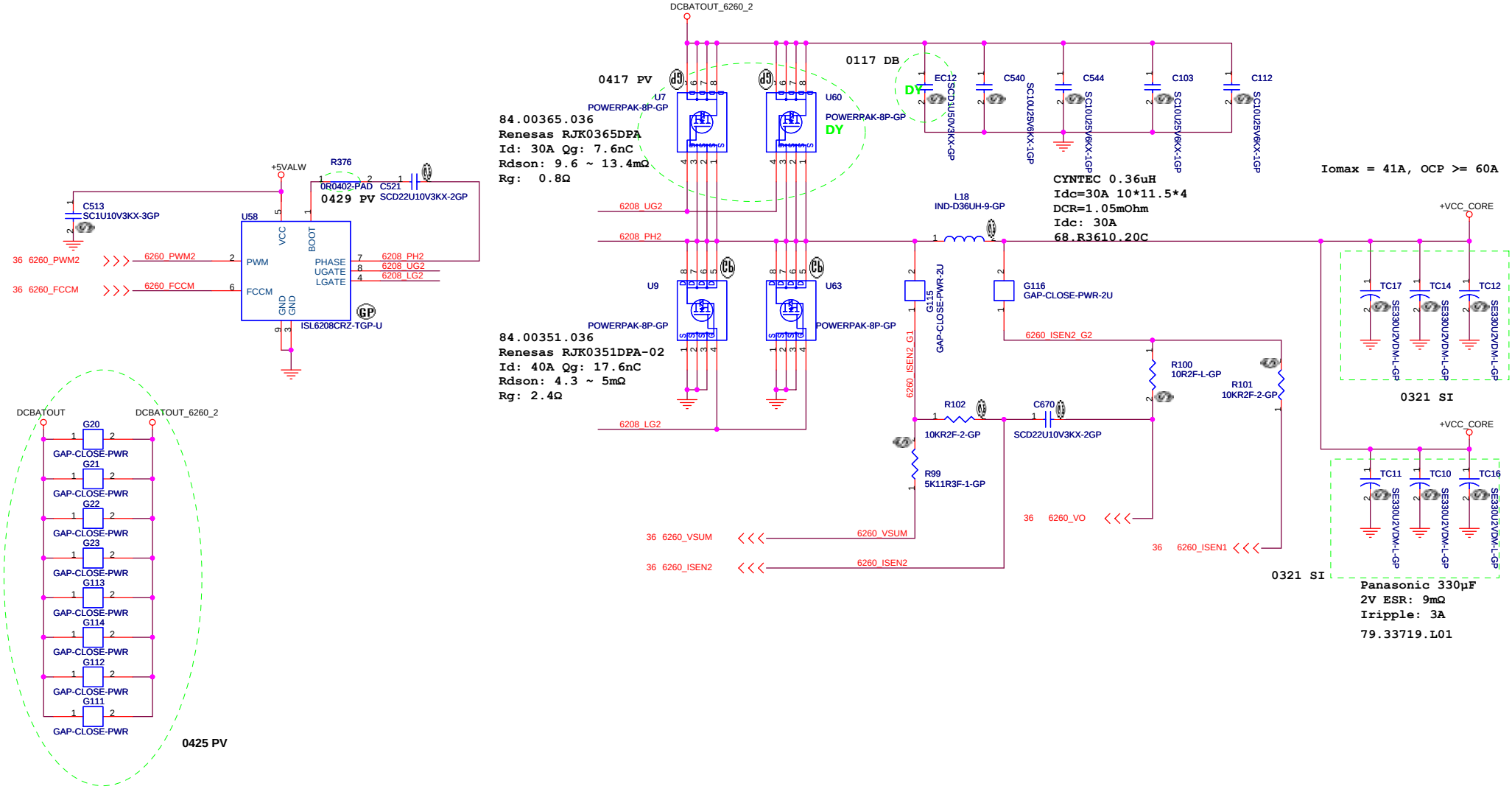
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6266CCRZ CPU CORE(1/2)

Size	Document Number	Rev
A3	VITAS	SA

Date: Monday, May 05, 2008 Sheet 36 of 48



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6260CCRZ CPU CORE(2/2)

Size	Document Number	Rev
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SI4800, SO-8
Id=9A, Qg=8.7~13nC
Rdson=23~30mohm

0407 PV
0425 PV
1101 DB
0117 DB

CYNTEC 3.3uH
Idc=6A
6.5*6.9*3
DCR= 28 ~ 30mOhm
68.3R310.20A

Sanyo 220uF 6.3V
ESR=25mohm
Iripple=2.4A
77.22271.27L

Close to IC TPS51125
Design Current=1.2A
OCP>2A

Design Current=4A
OCP design>6A

0502 PV

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPA51125 +5VALW +3VALW
Size: A3
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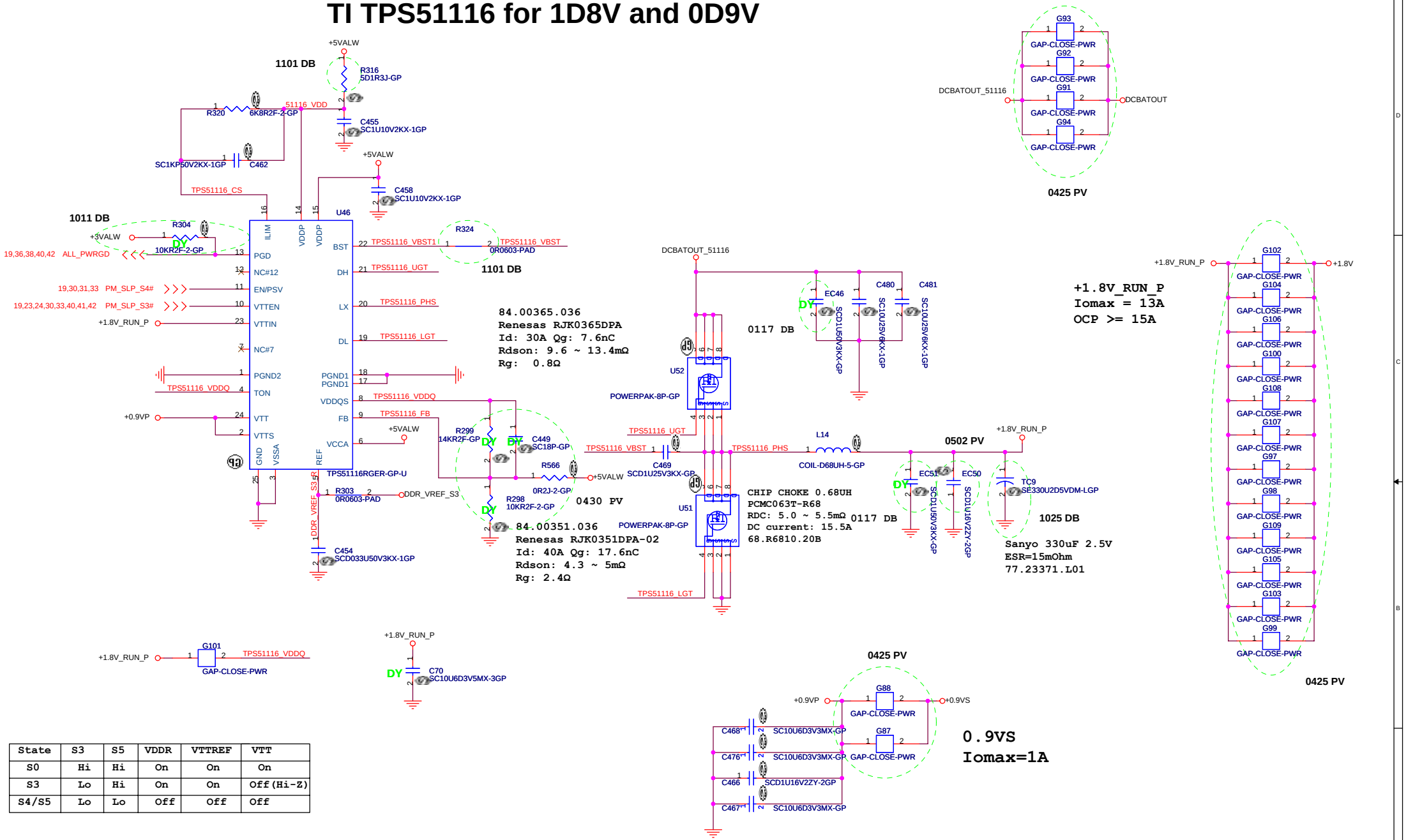
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

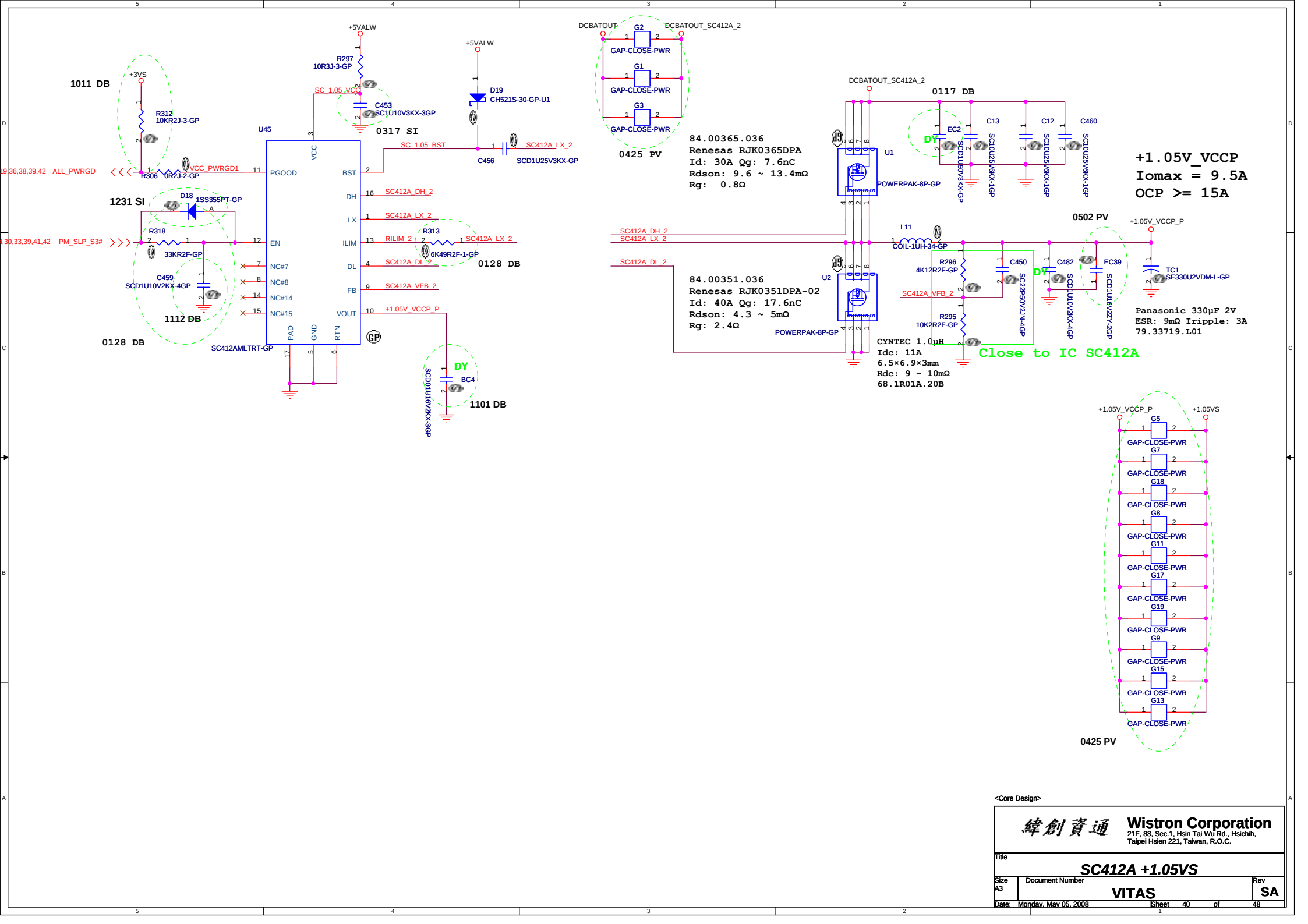
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 39 of 48



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SC412A +1.05VS***

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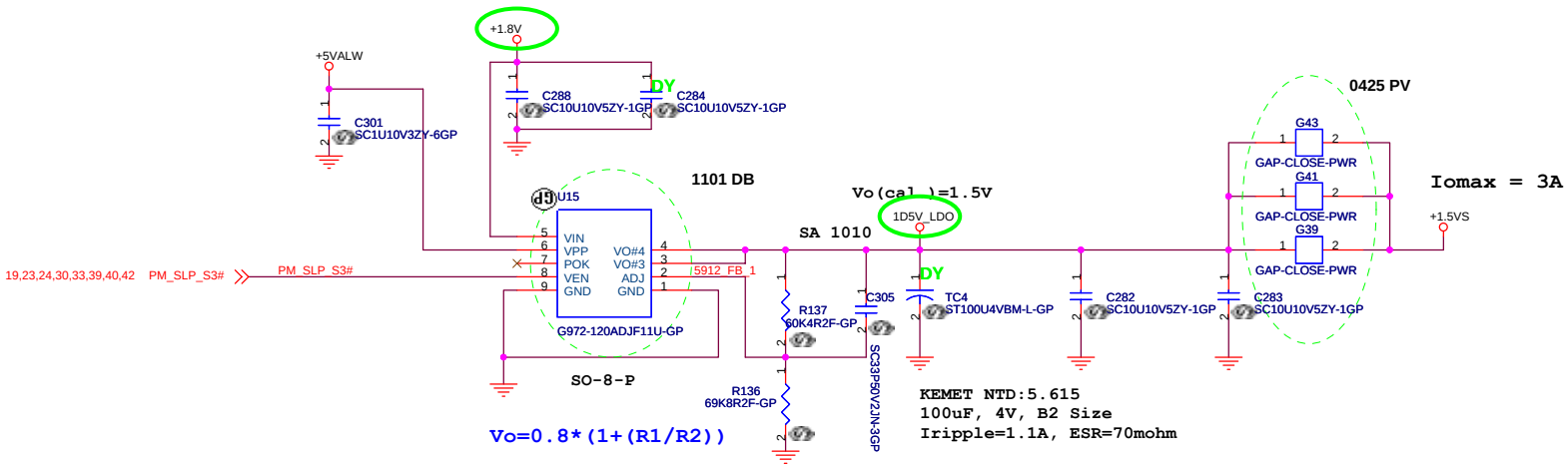

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMT 1D5V LDO***

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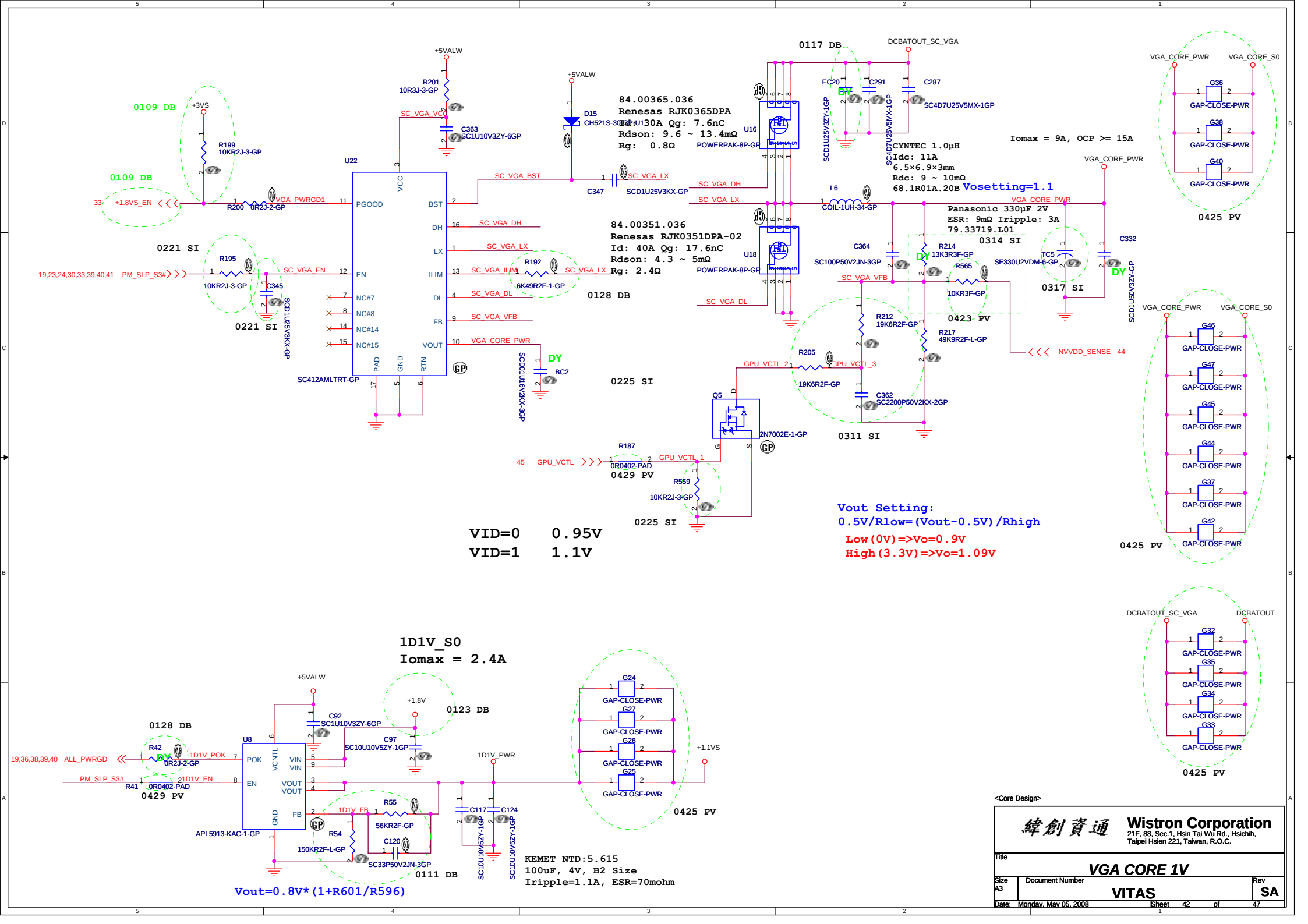
0109 DB
+3VS
R199
10KR2J-3-GP
0109 DB
33
+1.8VS_EN
R200 0R2J-2-GP
VGA_PWRGD1
0221 SI
R195
19,23,24,30,33,39,40,41
PM_SLP_S3#
10KR2J-3-GP
SC_VGA_EN
C345
0221 SI
SCD1U25V3KX-GP
+5VALW
R201
10R3J-3-GP
SC_VGA_VCC
C363
SC1U10V3ZY-6GP
U22
VCC
PGOOD
EN
NC#7
NC#8
NC#14
NC#15
PAD
GND
RTN
BST
DH
LX
ILIM
DL
FB
VOUT
SC_VGA_BST
SC_VGA_DH
SC_VGA_LX
SC_VGA_ILIM
SC_VGA_DL
SC_VGA_VFB
VGA_CORE_PWR
SC412AMLTRT-GP
SCD01U16V2KX-3GP
DY
BC2
+5VALW
D15
CH521S-30-GP
C347
SCD1U25V3KX-GP
84.00365.036
Renesas RJK0365DPA
Id: 130A Qg: 7.6nC
Rdson: 9.6 ~ 13.4mΩ
Rg: 0.8Ω
84.00351.036
Renesas RJK0351DPA-02
Id: 40A Qg: 17.6nC
Rdson: 4.3 ~ 5mΩ
Rg: 2.4Ω
R192
6K49R2F-1-GP
0128 DB
0225 SI
U16
U18
POWERPAK-8P-GP
0117 DB
DCBATOUT_SC_VGA
EC20
DY
C291
C287
SC4D7U25V5MX-1GP
SCD1U25V3ZY-1GP
SC4D7U25V5MX-1GP
CYNTEC 1.0μH
Idc: 11A
6.5×6.9×3mm
Rdc: 9 ~ 10mΩ
68.1R01A.20B
Vosetting=1.1
Iomax = 9A, OCP >= 15A
L6
COIL-1UH-34-GP
VGA_CORE_PWR
Panasonic 330μF 2V
ESR: 9mΩ Iripple: 3A
79.33719.L01
0314 SI
C364
SC100P50V2JN-3GP
R214
13K3R3F-GP
R565
10KR3F-GP
0423 PV
TC5
SE330U2VDM-6-GP
0317 SI
C332
SCD1U50V3ZY-GP
SC_VGA_VFB
R212
19K6R2F-GP
R217
49K9R2F-L-GP
0311 SI
NVVDD_SENSE 44
R205
19K6R2F-GP
GPU_VCTL_2
GPU_VCTL_3
C362
SC2200P50V2KX-2GP
Q5
2N7002E-1-GP
R187
0R0402-PAD
45
GPU_VCTL
GPU_VCTL_1
0429 PV
R559
10KR2J-3-GP
0225 SI
VID=0 0.95V
VID=1 1.1V
Vout Setting:
0.5V/Rlow=(Vout-0.5V)/Rhigh
Low(0V)=>Vo=0.9V
High(3.3V)=>Vo=1.09V
VGA_CORE_PWR
VGA_CORE_S0
G36
G38
G40
GAP-CLOSE-PWR
0425 PV
G46
G47
G45
G44
G37
G42
0425 PV
DCBATOUT_SC_VGA
DCBATOUT
G32
G35
G34
G33
0425 PV
1D1V_S0
Iomax = 2.4A
+5VALW
+1.8V
0123 DB
C92
SC1U10V3ZY-6GP
C97
SC10U10V5ZY-1GP
0128 DB
R42
0R2J-2-GP
19,36,38,39,40
ALL_PWRGD
1D1V_POK
PM_SLP_S3#
R41
0R0402-PAD
1D1V_EN
0429 PV
U8
POK
VCNTL
VIN
EN
VOUT
GND
FB
APL5913-KAC-1-GP
1D1V_PWR
1D1V_FB
R55
56KR2F-GP
R54
150KR2F-L-GP
C120
SC33P50V2JN-3GP
0111 DB
C117
C124
SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
+1.1VS
G24
G27
G26
G25
GAP-CLOSE-PWR
0425 PV
KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Vout=0.8V*(1+R601/R596)
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA CORE 1V
Size
A3
Document Number
VITAS
Rev
SA
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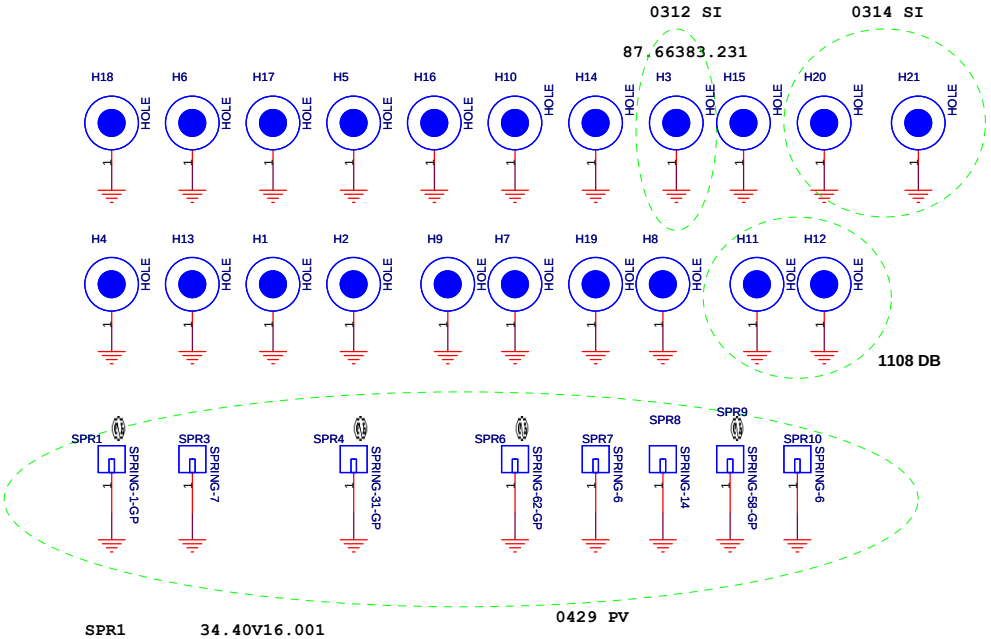

SPR1	34.40V16.001
SPR3	34.49U26.001
SPR4	34.49U24.001
SPR6	34.39S07.003
SPR7	34.13B01.001
SPR8	34.41V01.001
SPR9	34.4B312.002
SPR10	34.13B01.001

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MISC***

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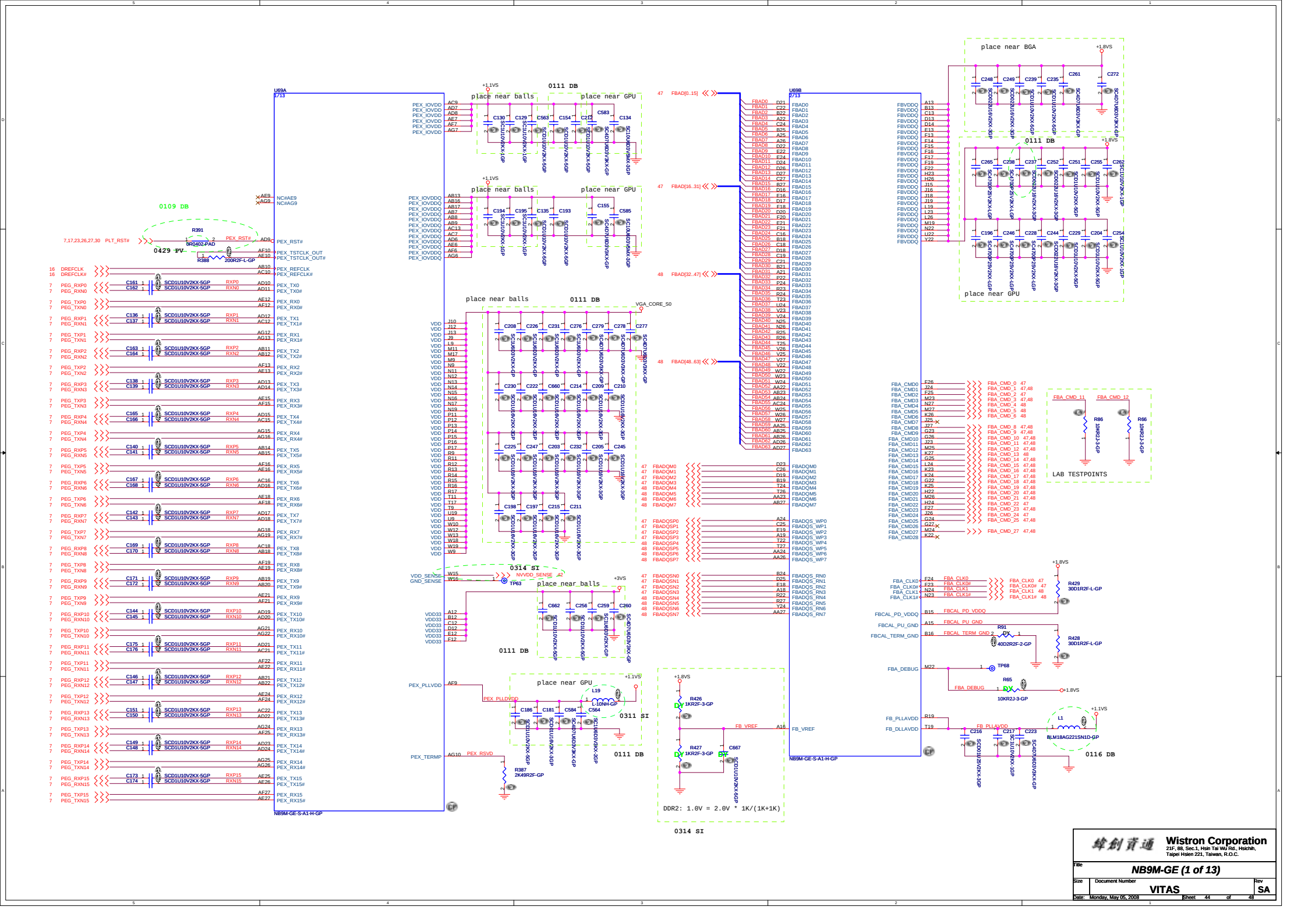
0109 DB
0429 PV
R391
0R0402-PAD
R388
200R2F-L-GP
PLT_RST#
PEX_RST#
NC#AE9
NC#AG9
U69A
U69B
NB9M-GE-S-A1-H-GP
0111 DB
0314 SI
0311 SI
0116 DB
place near balls
place near GPU
place near BGA
VGA_CORE_S0
LAB TESTPOINTS
DDR2: 1.0V = 2.0V * 1K/(1K+1K)
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NB9M-GE (1 of 13)
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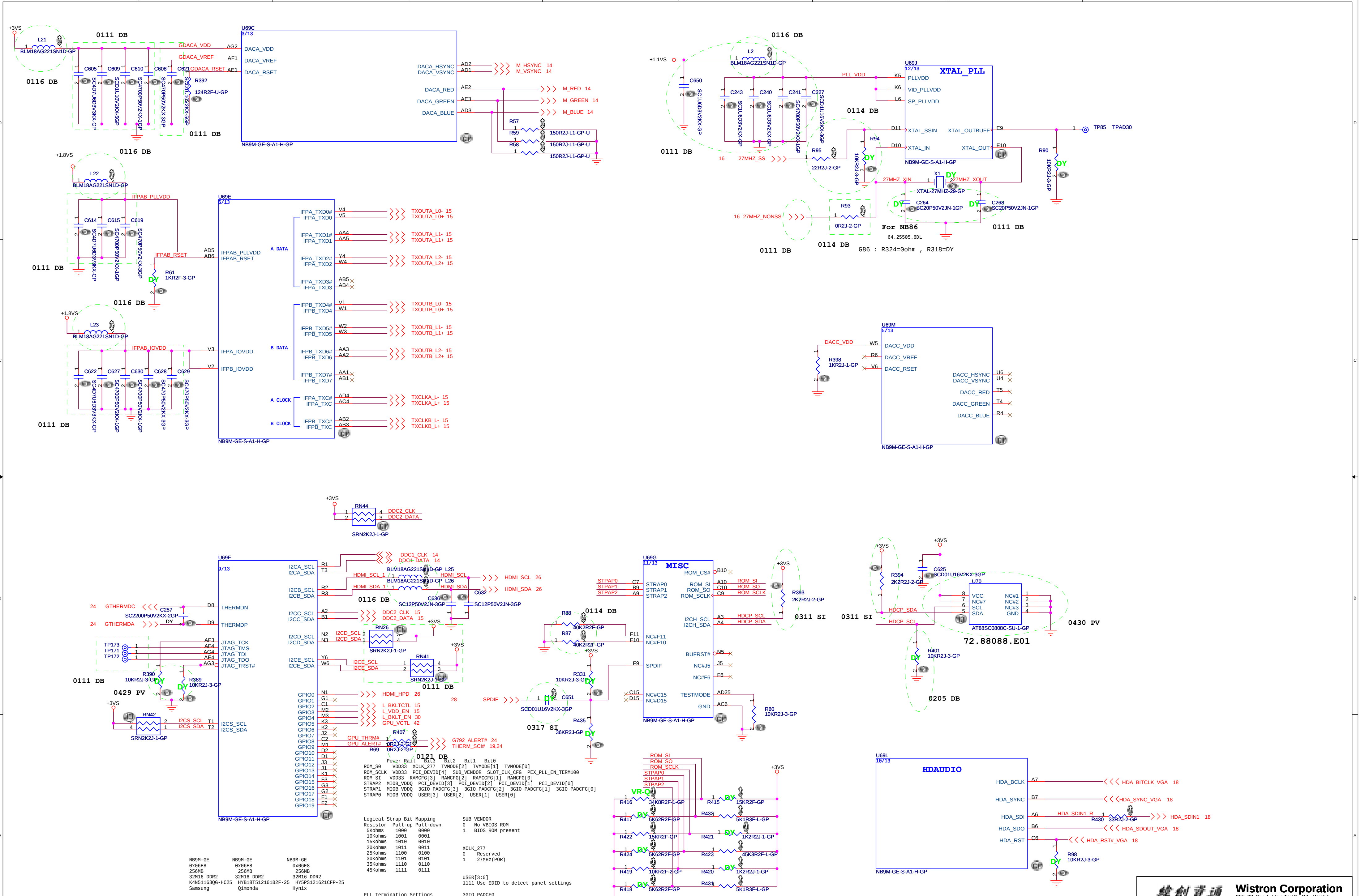
U69C 3/13
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
NB9M-GE-S-A1-H-GP
U69E 6/13
IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD
A DATA
B DATA
A CLOCK
B CLOCK
U69J 12/13
XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
U69M 5/13
DACC_VDD
DACC_VREF
DACC_RSET
U69F 9/13
THERMDN
THERMDP
U69G 11/13
MISC
U69L 18/13
HDAUDIO
0111 DB
0116 DB
0114 DB
0311 SI
0430 PV
0205 DB
0317 SI
0429 PV
0121 DB
For NB86
64.25505.6DL
G86 : R324=0ohm , R318=DY
72.88088.E01
Power Rail   Bit3   Bit2   Bit1   Bit0
ROM_S0   VDD33   XCLK_277   TVMODE[2]   TVMODE[1]   TVMODE[0]
ROM_SCLK   VDD33   PCI_DEVID[4]   SUB_VENDOR   SLOT_CLK_CFG   PEX_PLL_EN_TERM100
ROM_SI   VDD33   RAMCFG[3]   RAMCFG[2]   RAMCFG[1]   RAMCFG[0]
STRAP2   MIOB_VDDQ   PCI_DEVID[3]   PCI_DEVID[2]   PCI_DEVID[1]   PCI_DEVID[0]
STRAP1   MIOB_VDDQ   3GIO_PADCFG[3]   3GIO_PADCFG[2]   3GIO_PADCFG[1]   3GIO_PADCFG[0]
STRAP0   MIOB_VDDQ   USER[3]   USER[2]   USER[1]   USER[0]
Logical Strap Bit Mapping
Resistor   Pull-up   Pull-down
5Kohms   1000   0000
10Kohms   1001   0001
15Kohms   1010   0010
20Kohms   1011   0011
25Kohms   1100   0100
30Kohms   1101   0101
35Kohms   1110   0110
45Kohms   1111   0111
SUB_VENDOR
0   No VBIOS ROM
1   BIOS ROM present
XCLK_277
0   Reserved
1   27MHz(POR)
USER[3:0]
1111 Use EDID to detect panel settings
3GIO_PADCFG
0000   Desktop
0001   Notebook (POR)
PLL Termination Settings
PEX_PLL_EN_TERM
0   Disable (POR)
1   Enable
SLOT_CLOCK_CFG
0   GPU and MCH do not share a common reference clock
1   GPU and MCH share a common reference clock (POR)
NB9M-GE   NB9M-GE   NB9M-GE
0x06E8   0x06E8   0x06E8
256MB   256MB   256MB
32M16 DDR2   32M16 DDR2   32M16 DDR2
K4N51163QG-HC25   HYB18T512161B2F-25   HY5PS121621CFP-25
Samsung   Qimonda   Hynix
ROM_SI   0101   0110   0111

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Title		
NB9M-GE (2 of 3)		
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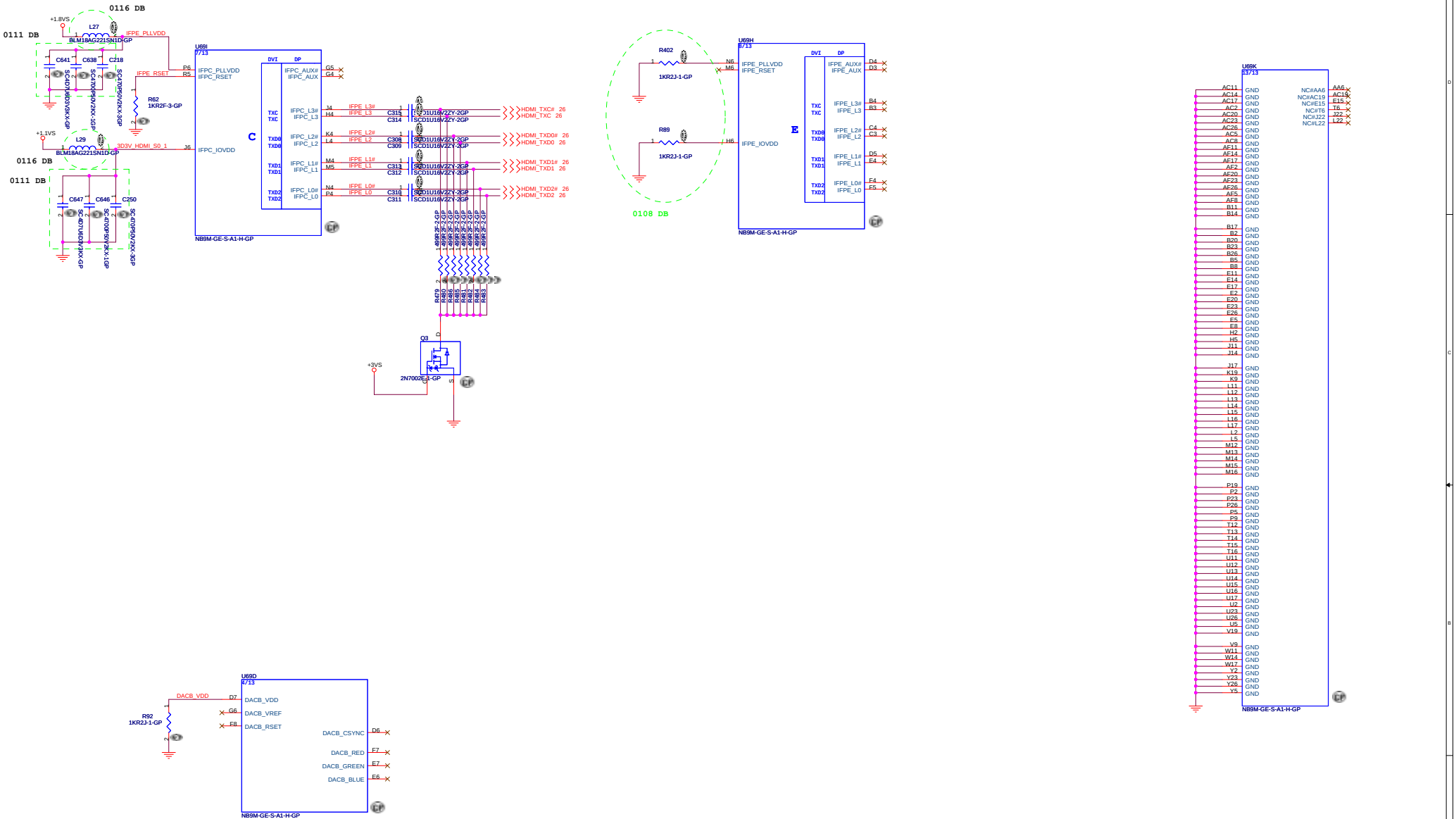

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Title: NB9M-GE (3 of 3)

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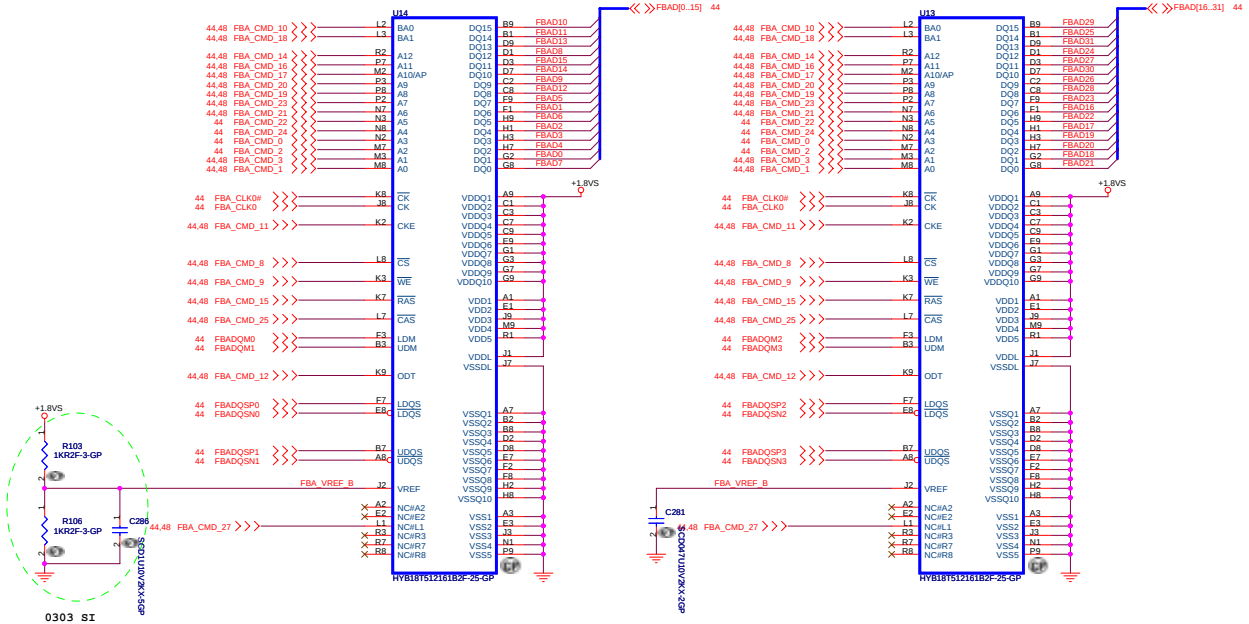
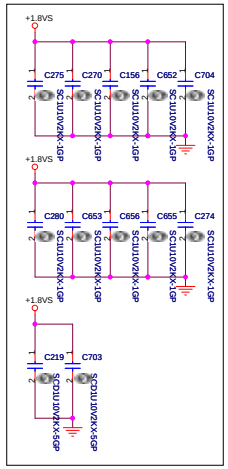
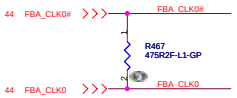
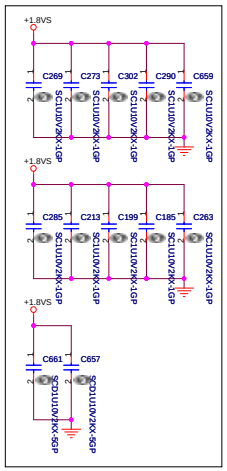


X - cap for CMD





X - cap for CMD



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Title: VRAM1		
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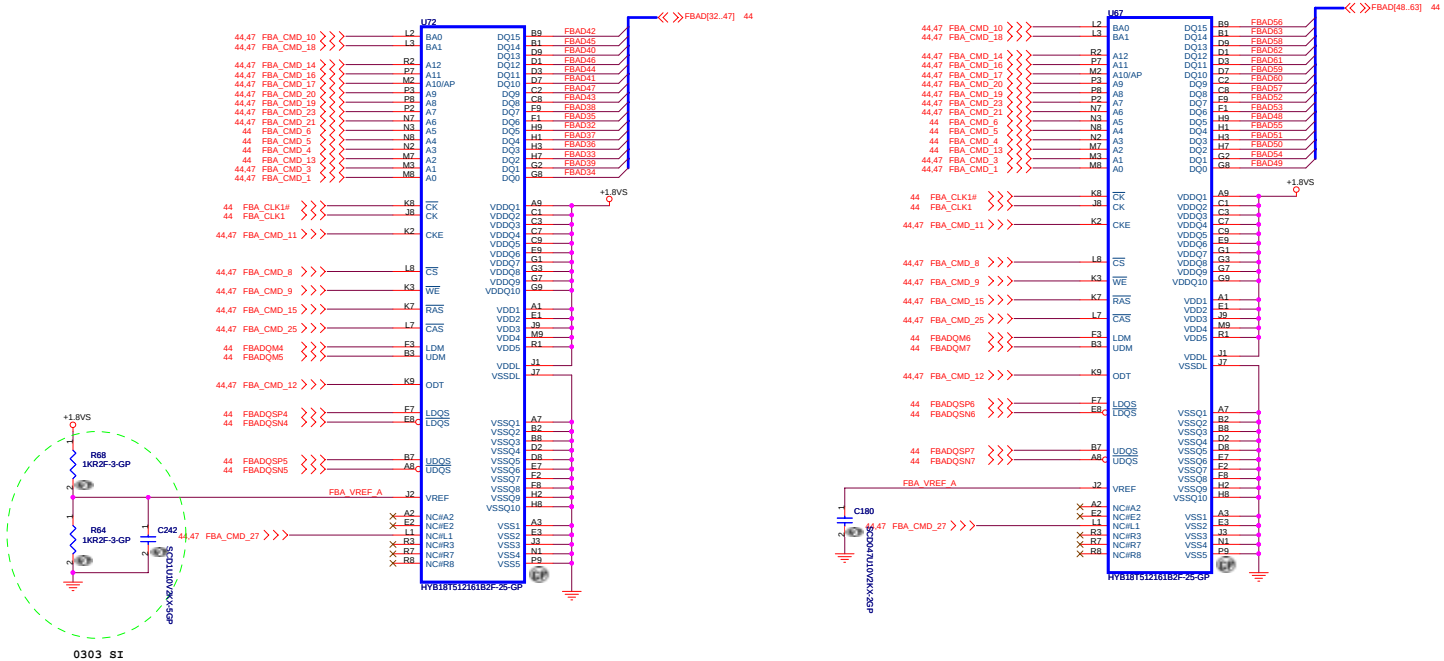
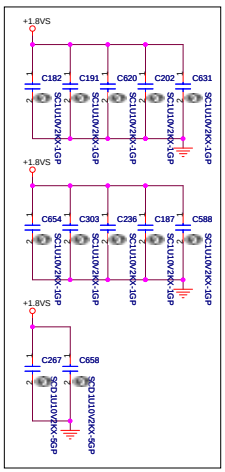
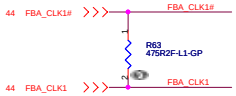
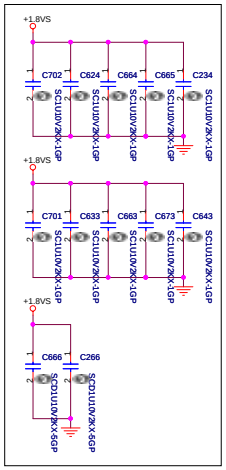


X - cap for CMD





X - cap for CMD



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Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM2

Size: | Document Number: VITAS | Rev: SA

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