

# Compal confidential

## Schematics Document

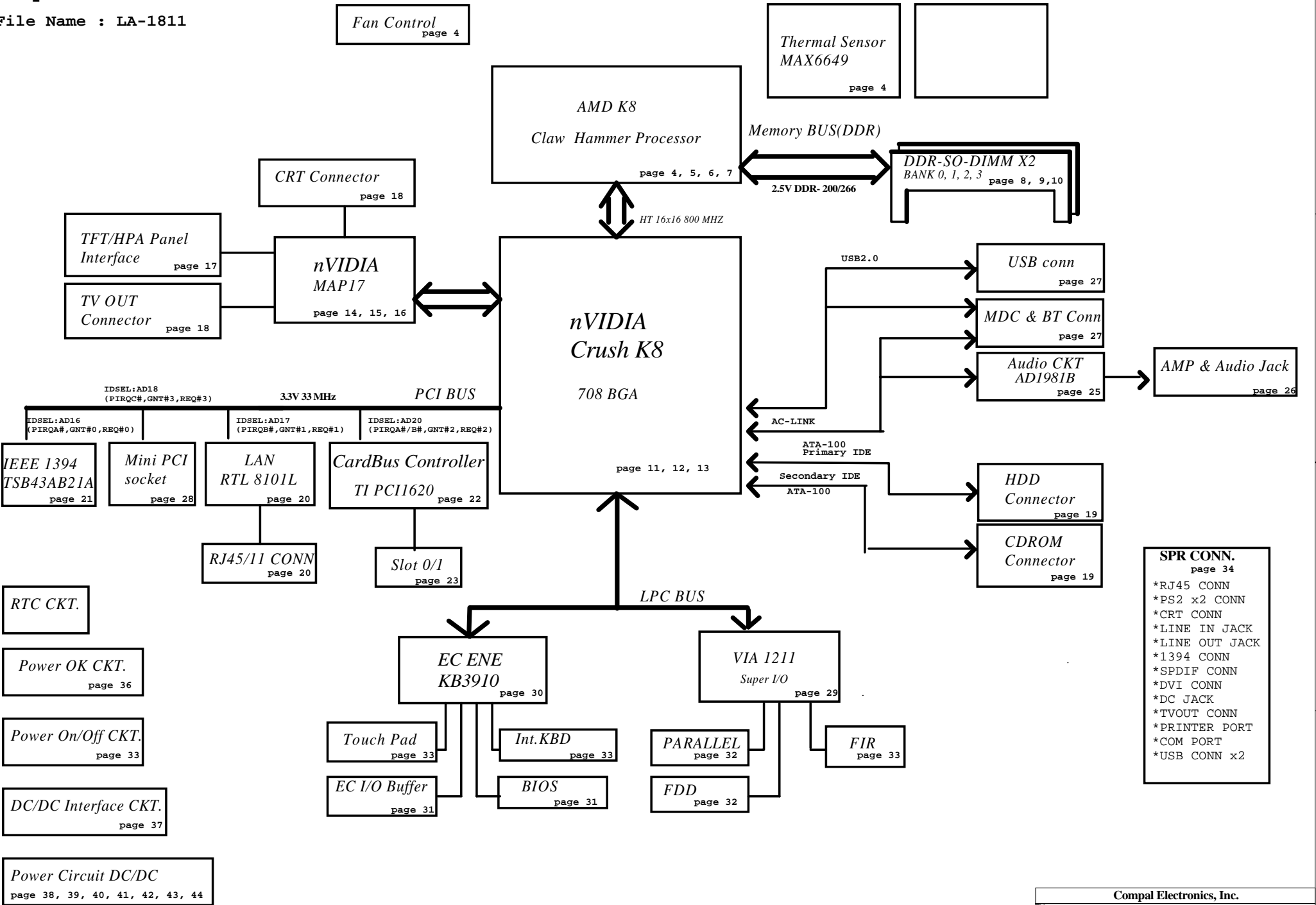
### ClawHammer AMD K8 with nVIDIA Chrush K8

2003-10-15

REV:0.5

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<b>Compal Electronics, Inc.</b>		
Title		
<b>SCHEMATIC, M/B ASSY LA-1851</b>		
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	<b>401254</b>	<b>0B</b>
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- SPR CONN.**  
page 34
- \*RJ45 CONN
  - \*PS2 x2 CONN
  - \*CRT CONN
  - \*LINE IN JACK
  - \*LINE OUT JACK
  - \*1394 CONN
  - \*SPDIF CONN
  - \*DVI CONN
  - \*DC JACK
  - \*TVOUT CONN
  - \*PRINTER PORT
  - \*COM PORT
  - \*USB CONN x2

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## Voltage Rails

power plane State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	O	O	O
S1	O	O	O
S3	O	O	X
S5 S4/AC	O	X	X
S5 S4/AC don't exist	X	X	X

O MEANS ON  
X MEANS OFF

## PCI Devices

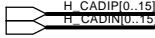
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
<b>INTERNAL</b>				
USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F
<b>EXTERNAL</b>				
VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

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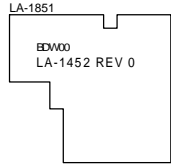
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<11> H\_CADIP[0..15]  
<11> H\_CADIN[0..15]



H\_CADOP[0..15]  
H\_CADON[0..15]

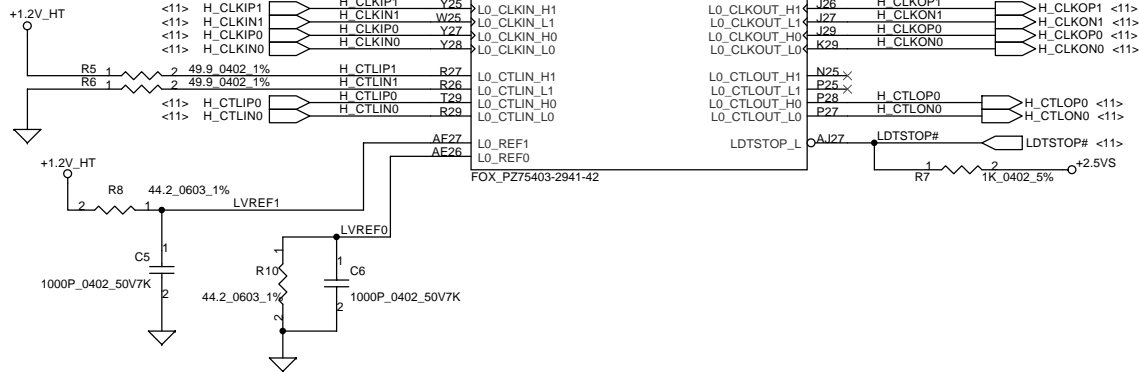


U1A

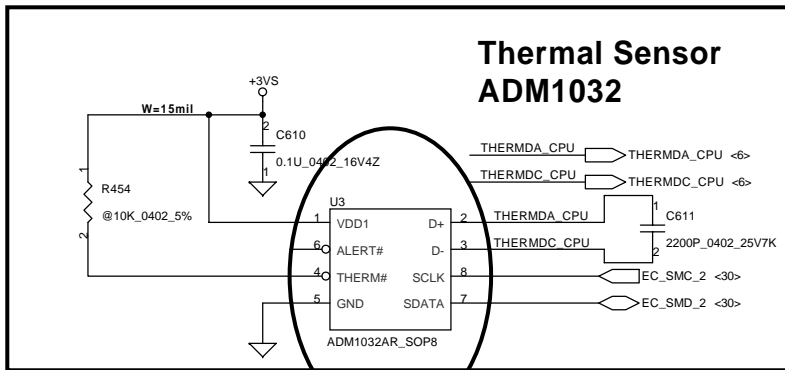
Claw Hammer-DTR

Pin	Signal	Pin	Signal
H_CADIP15	T25	L0_CADIN_H15	N26
H_CADIN15	R25	L0_CADIN_L15	N27
H_CADIP14	U27	L0_CADIN_H14	L25
H_CADIN14	U26	L0_CADIN_L14	M25
H_CADIP13	V25	L0_CADIN_H13	L26
H_CADIN13	U25	L0_CADIN_L13	L27
H_CADIP12	W27	L0_CADIN_H12	J25
H_CADIN12	W26	L0_CADIN_L12	K25
H_CADIP11	AA27	L0_CADIN_H11	G25
H_CADIN11	AA26	L0_CADIN_L11	H25
H_CADIP10	AB25	L0_CADIN_H10	G26
H_CADIN10	AA25	L0_CADIN_L10	G27
H_CADIP9	AC27	L0_CADIN_H9	E25
H_CADIN9	AC26	L0_CADIN_L9	E26
H_CADIP8	AD25	L0_CADIN_H8	E27
H_CADIN8	AC25	L0_CADIN_L8	N29
H_CADIP7	T27	L0_CADIN_H7	P29
H_CADIN7	T28	L0_CADIN_L7	M28
H_CADIP6	U28	L0_CADIN_H6	L29
H_CADIN6	U29	L0_CADIN_L6	M29
H_CADIP5	V27	L0_CADIN_H5	K28
H_CADIN5	V28	L0_CADIN_L5	K27
H_CADIP4	Y29	L0_CADIN_H4	H28
H_CADIN4	W29	L0_CADIN_L4	H27
H_CADIP3	AB29	L0_CADIN_H3	G29
H_CADIN3	AB27	L0_CADIN_L3	H29
H_CADIP2	AB27	L0_CADIN_H2	F28
H_CADIN2	AB28	L0_CADIN_L2	E27
H_CADIP1	AD29	L0_CADIN_H1	E29
H_CADIN1	AC29	L0_CADIN_L1	E29
H_CADIP0	AD27	L0_CADIN_H0	E29
H_CADIN0	AD28	L0_CADIN_L0	E29

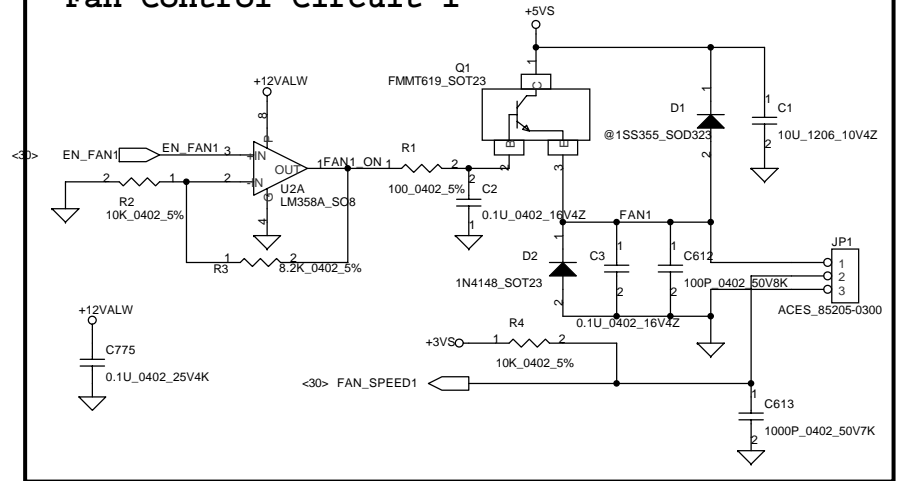
HTT Interface



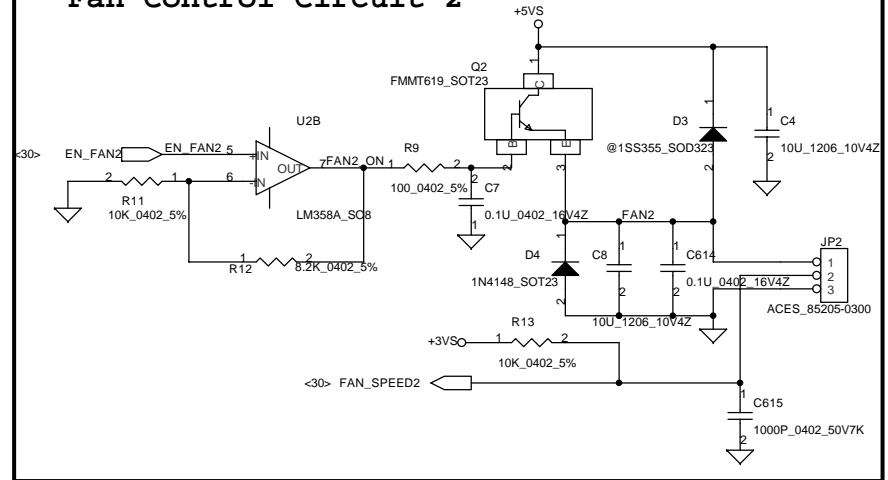
Thermal Sensor ADM1032



Fan Control Circuit 1



Fan Control Circuit 2

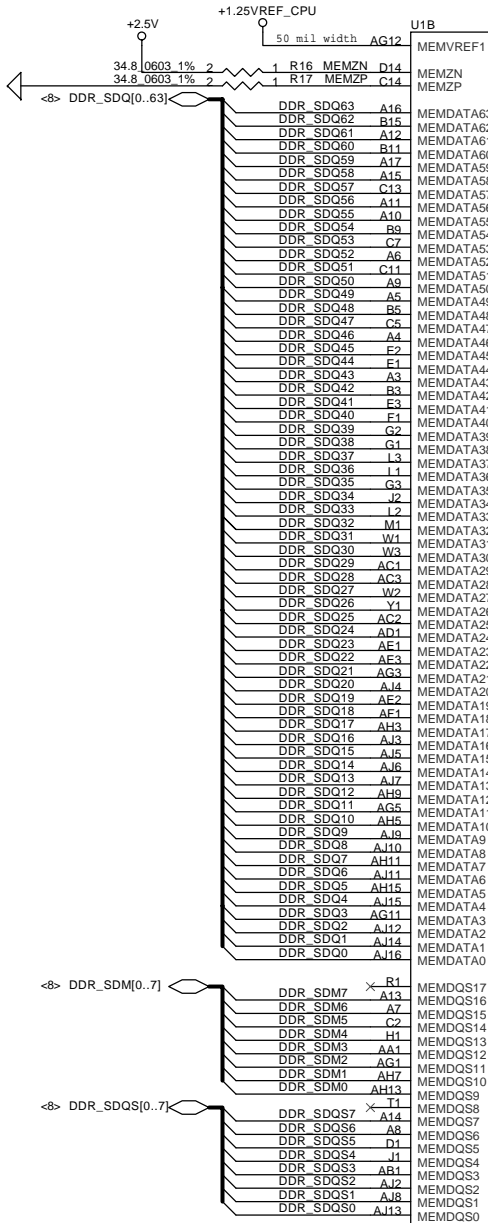


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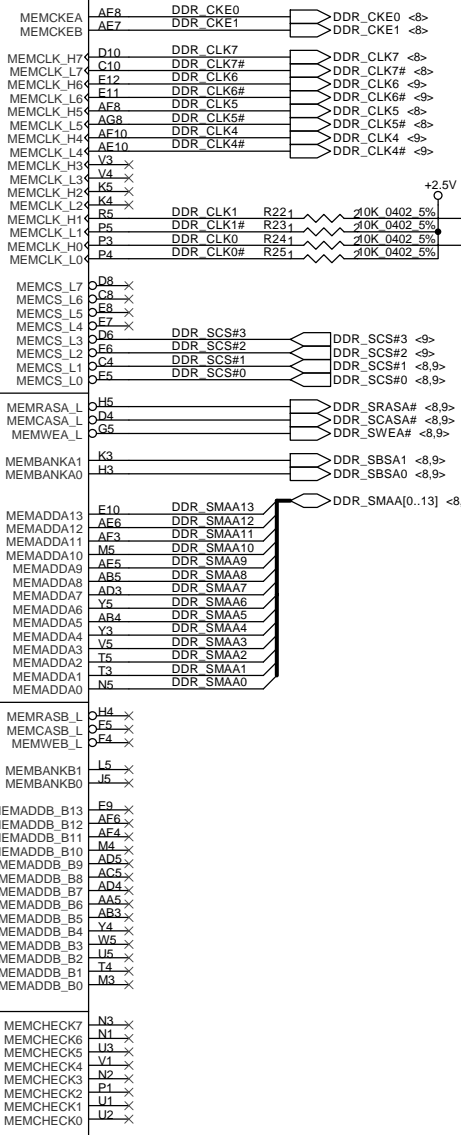


**Claw Hammer-DTR**

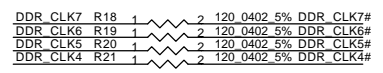
**DDR Memory**

**A CHANGE ADDRESS**

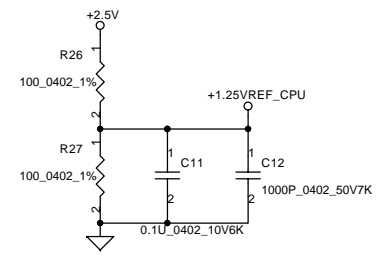
**B CHANGE ADDRESS**



DDR\_CLK5/5# & DDR\_CLK7/7#  
route to nearest DIMM  
DDR\_CLK4/4# & DDR\_CLK6/6#  
route to farthest DIMM



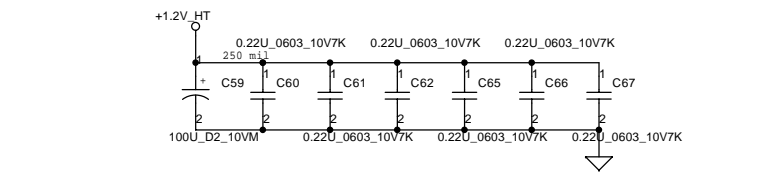
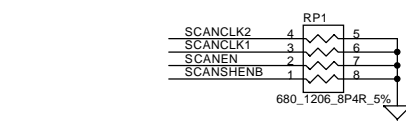
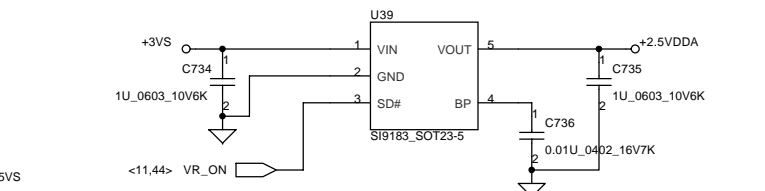
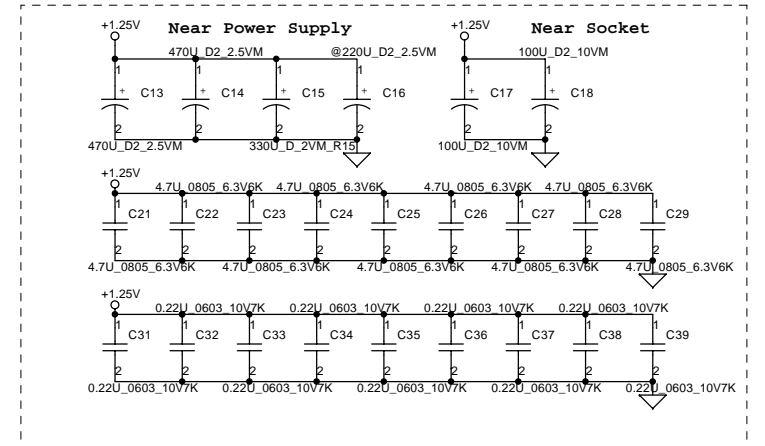
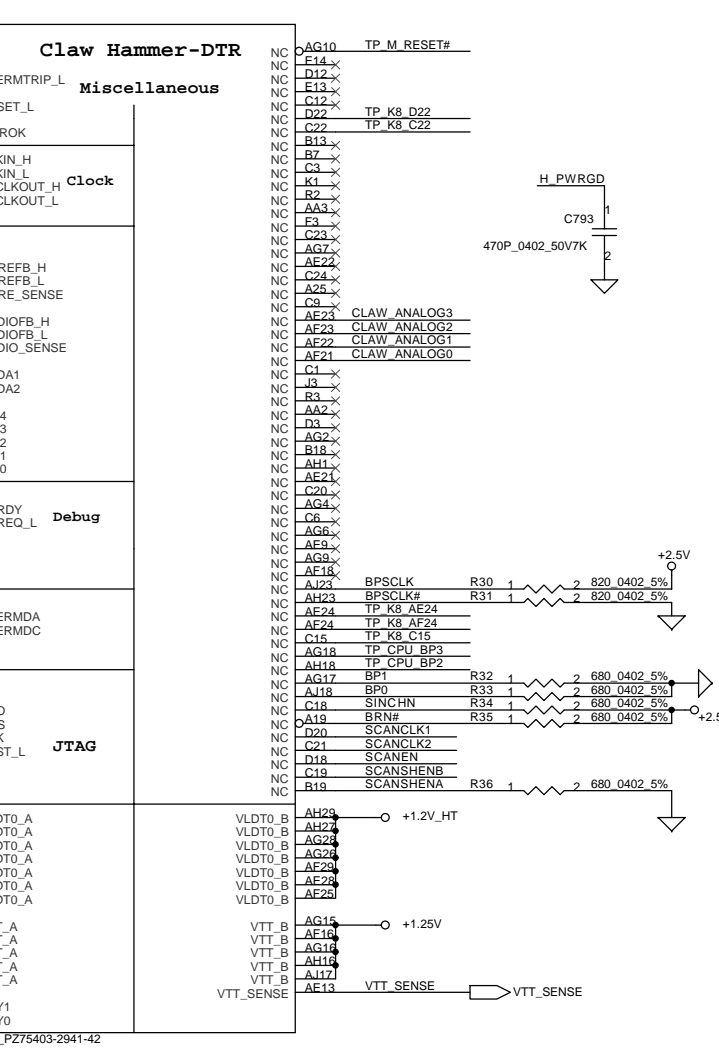
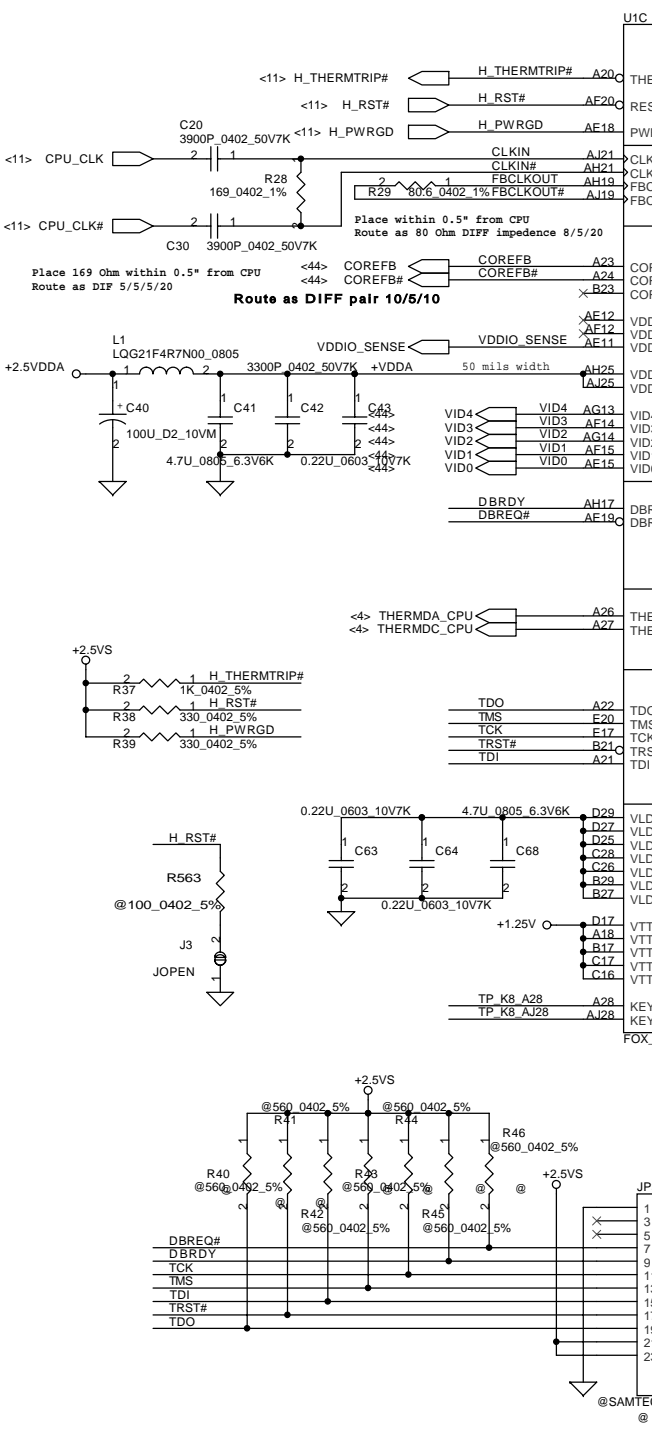
within 1.00"



FOX\_PZ75403-2941-42

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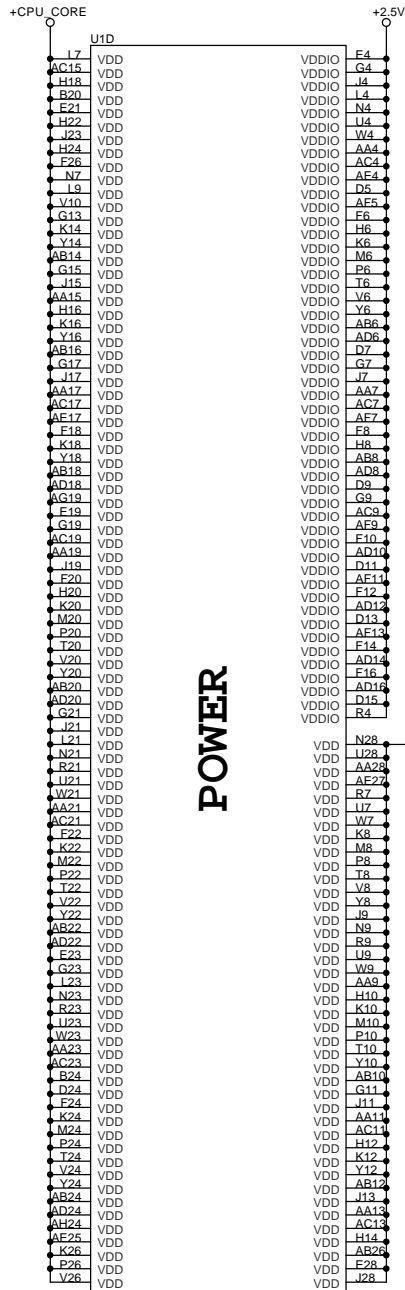


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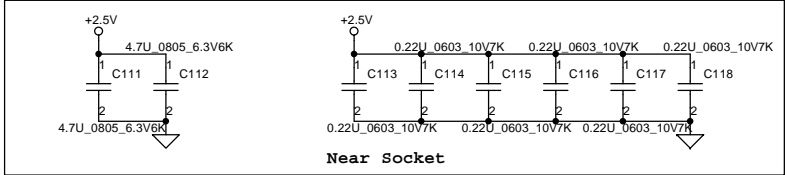
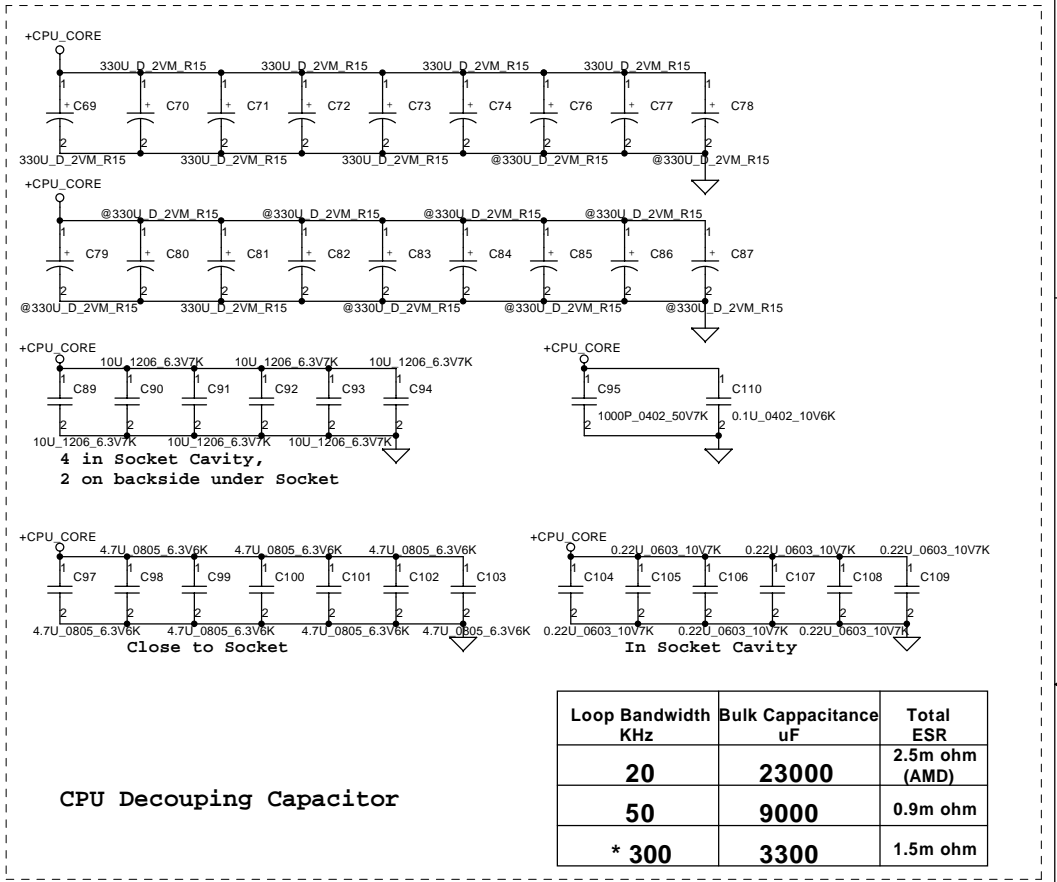
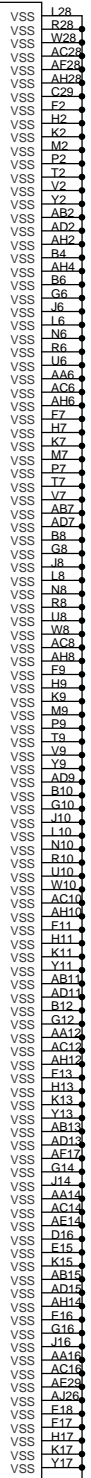
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# POWER



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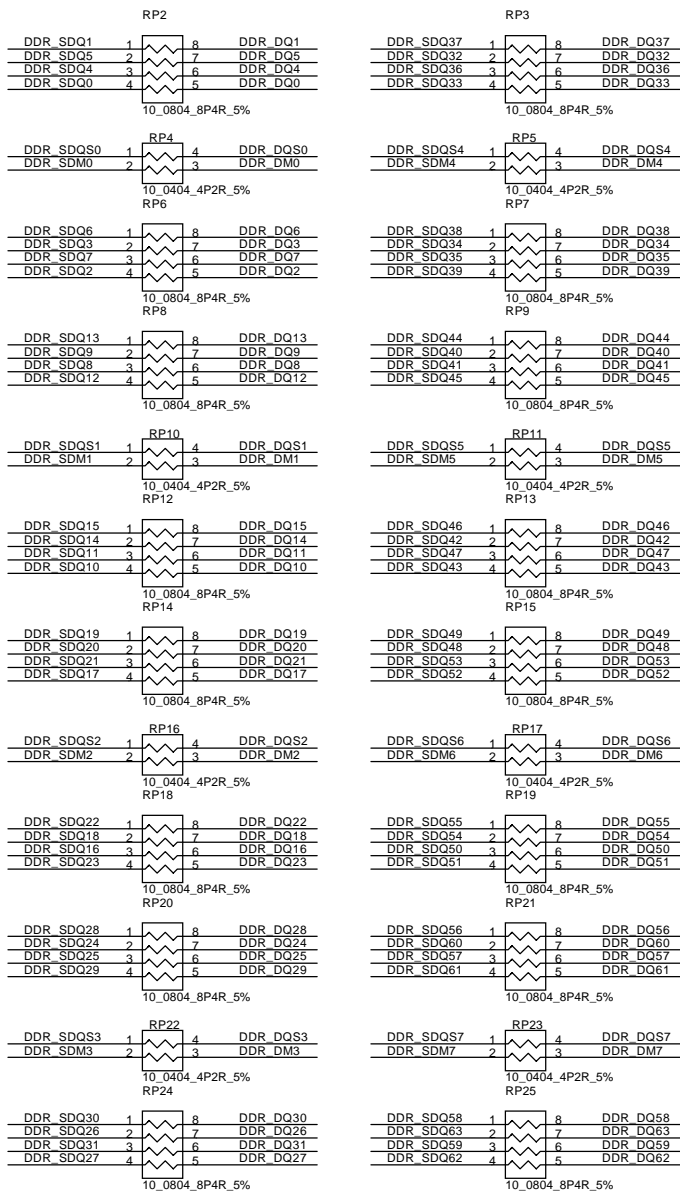
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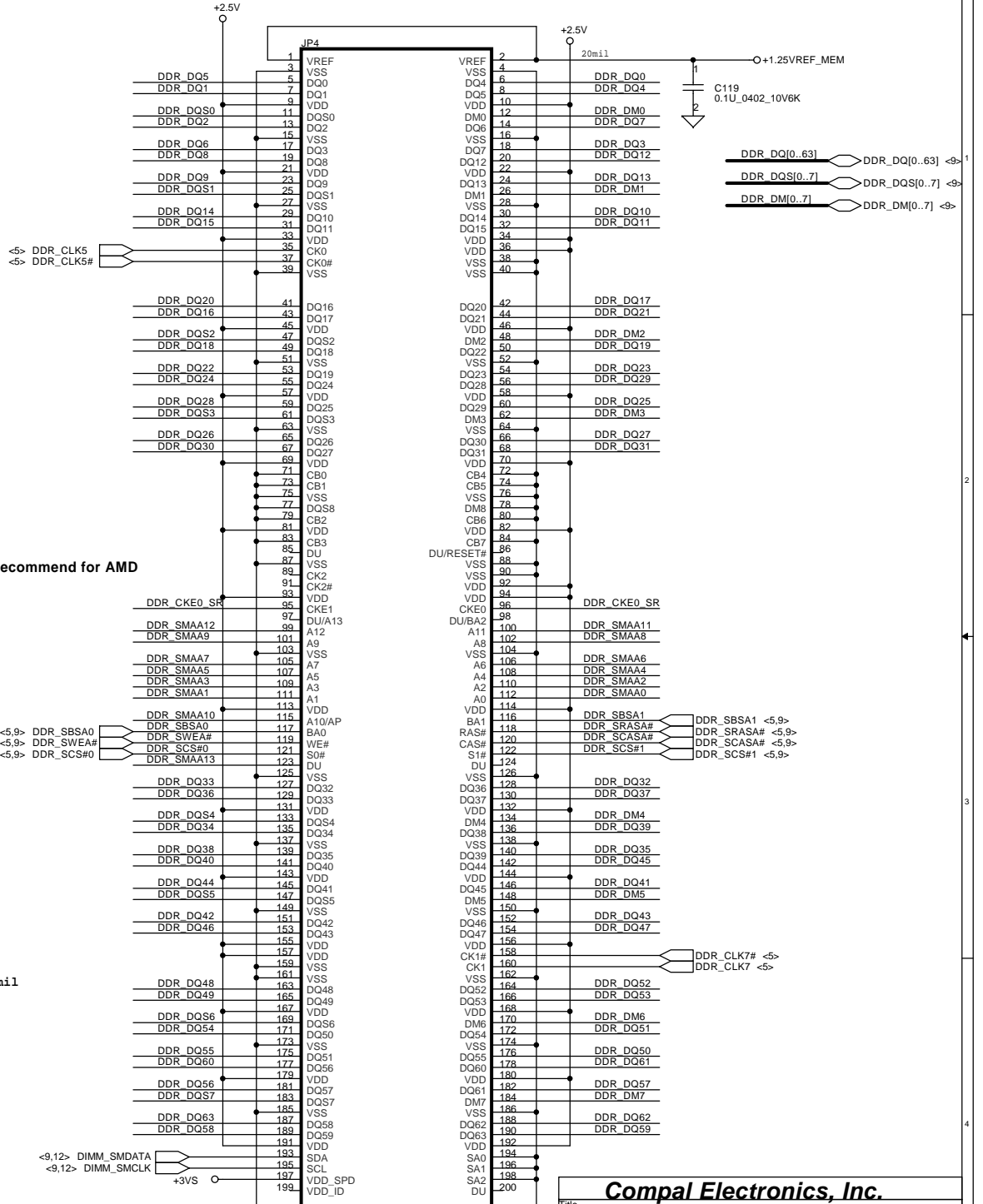
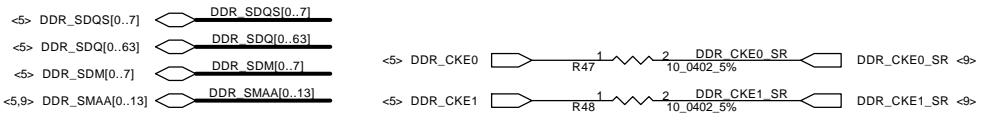
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Note:  
DDR\_SMAA13 Recommend for AMD

Layout note  
Place these resistors  
close to DIMM0,  
all trace length<500 mil



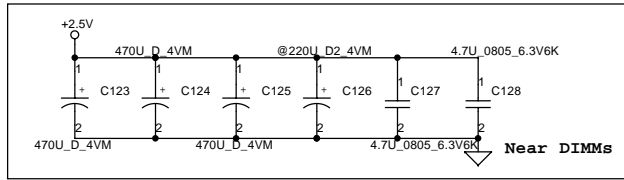
SO-DIMM0  
REVERSE

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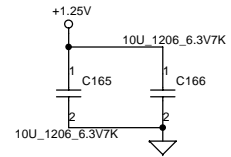
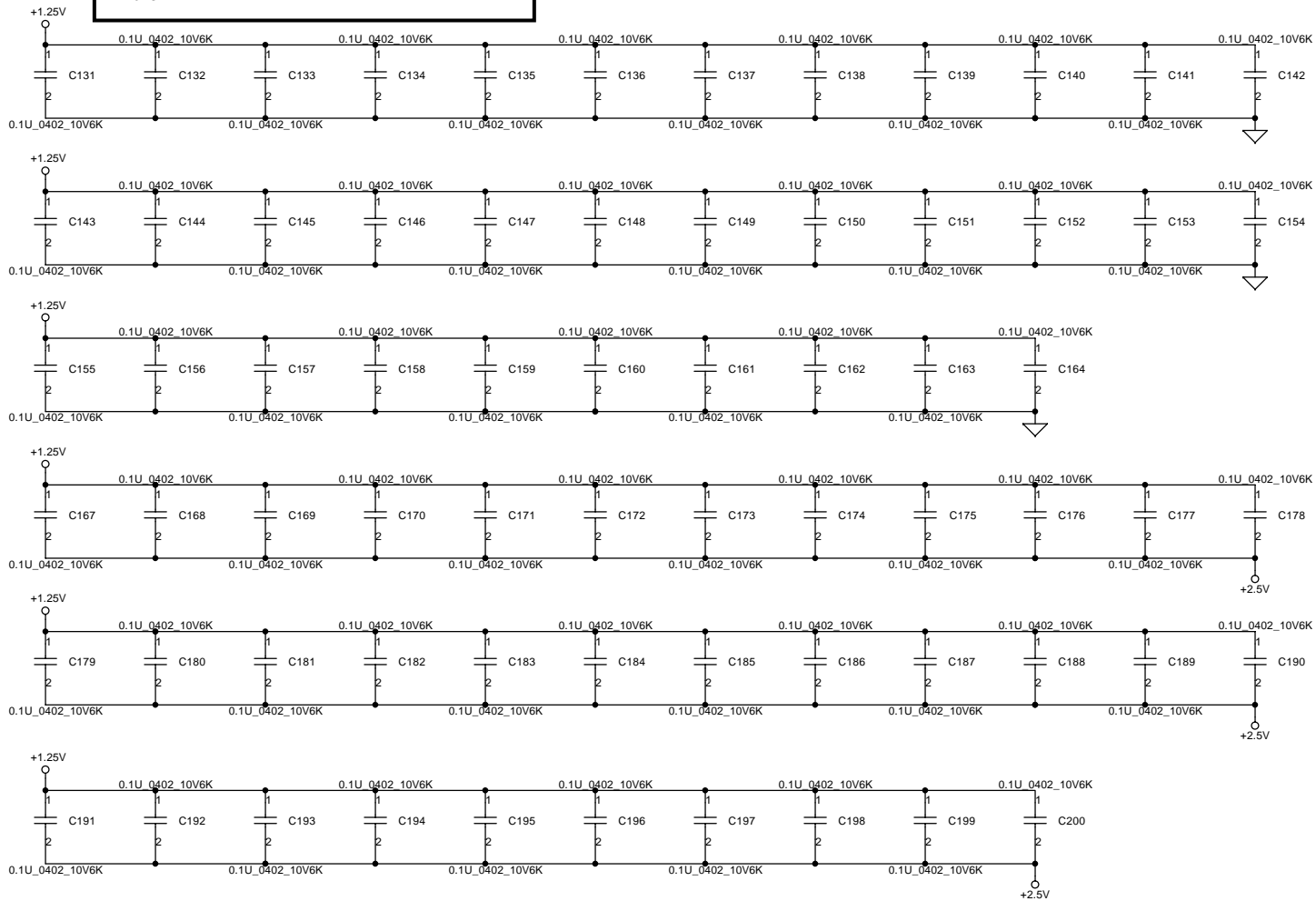
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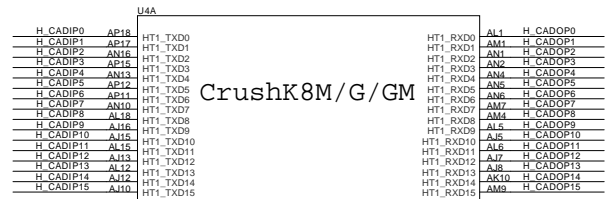
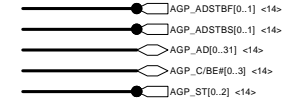
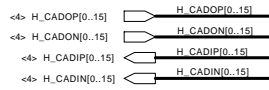


**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25VS



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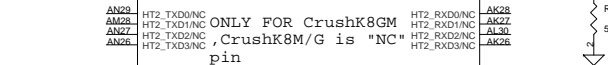
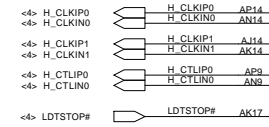
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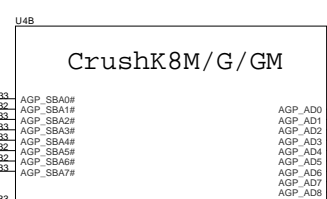
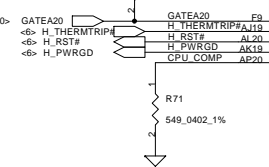
CrushK8M/G/GM



HyperTransport Interface



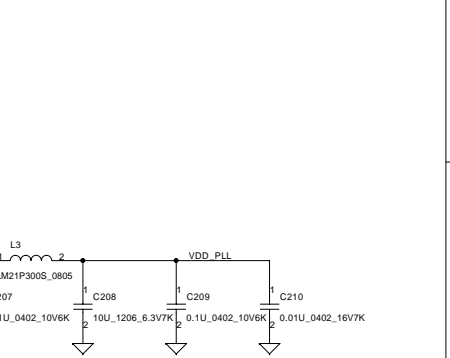
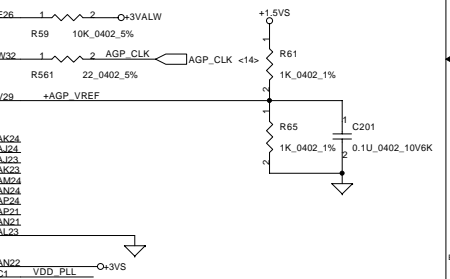
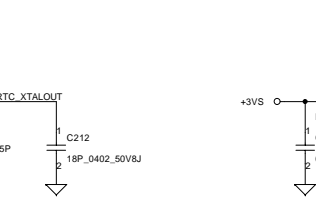
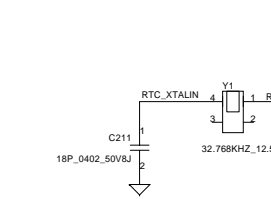
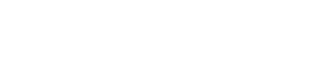
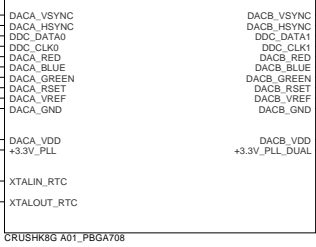
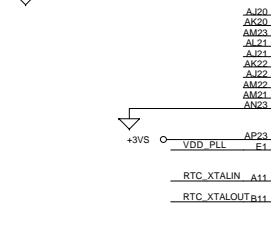
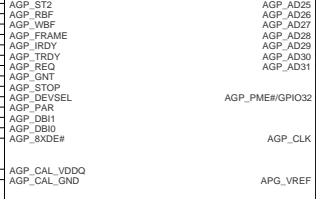
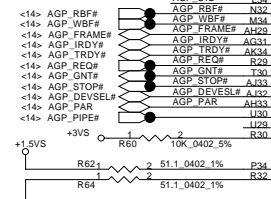
ONLY FOR CrushK8GM  
CrushK8M/G is "NC" pin



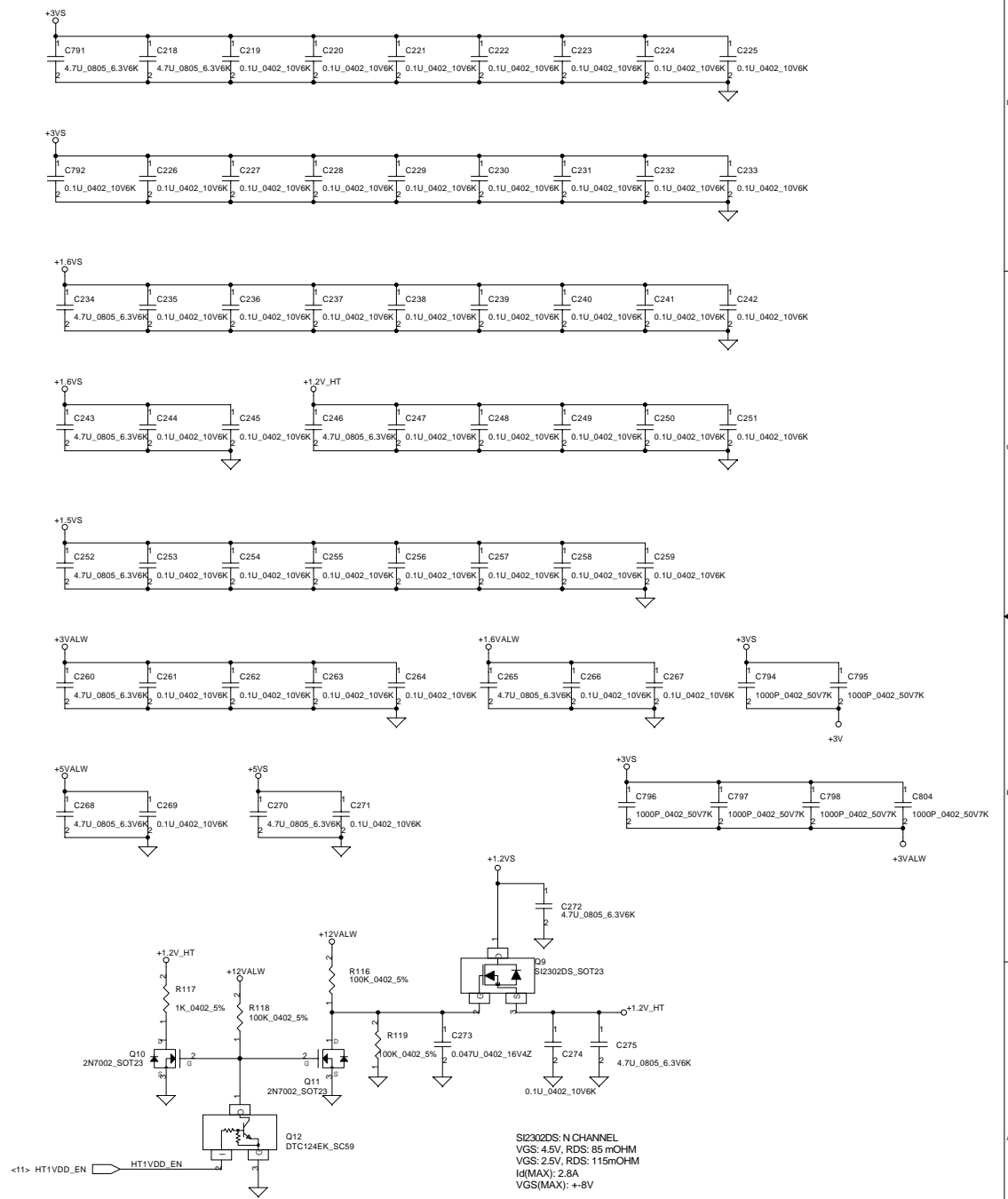
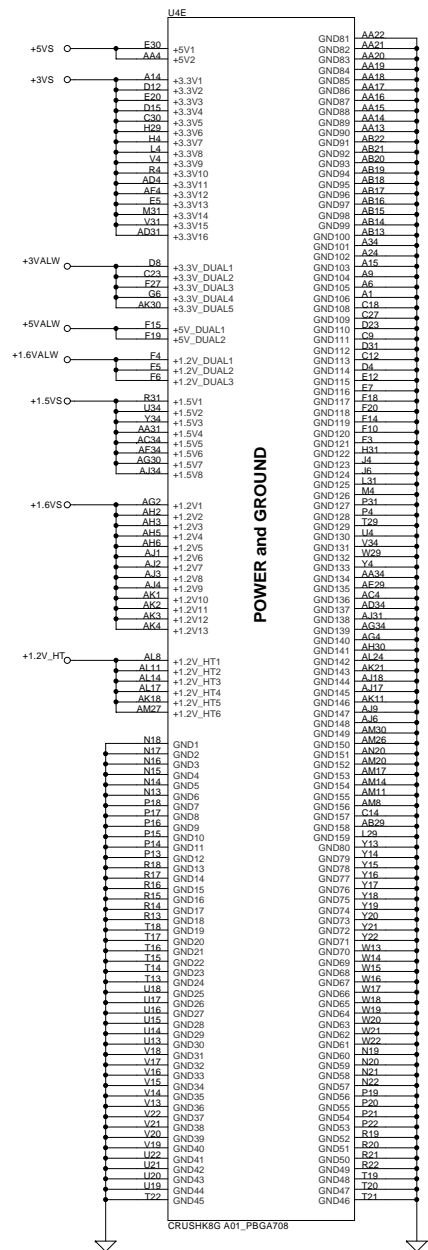
CrushK8M/G/GM



AGP Interface 4x/8x

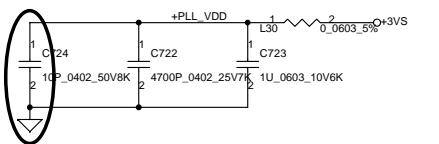
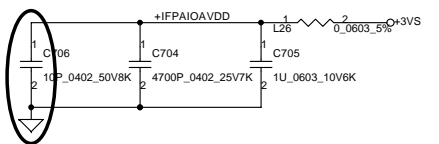
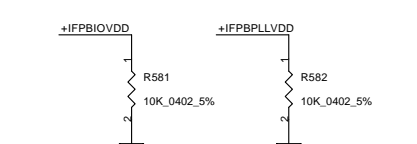
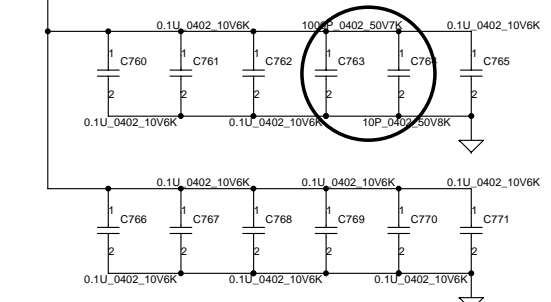
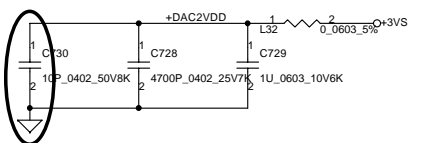
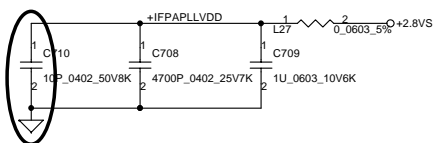
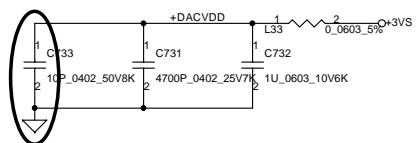
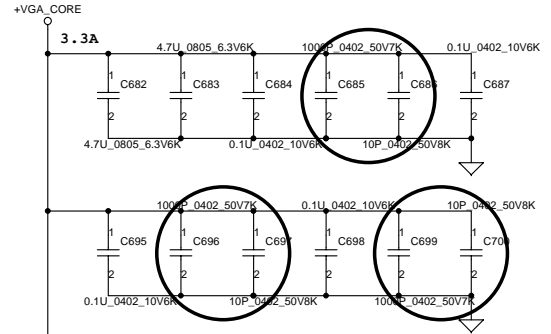
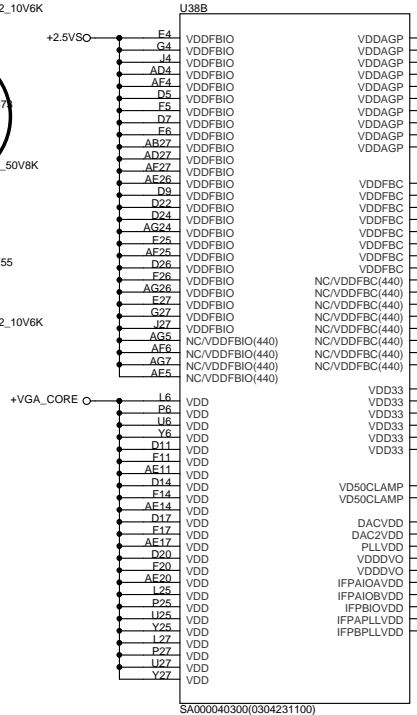
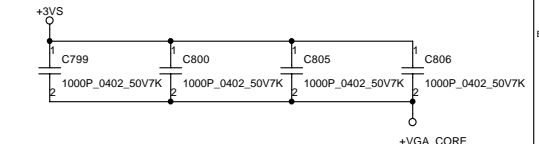
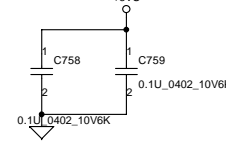
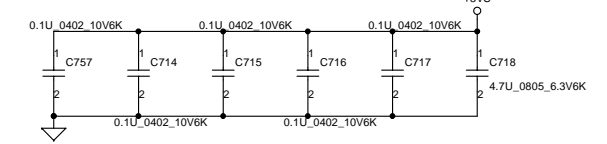
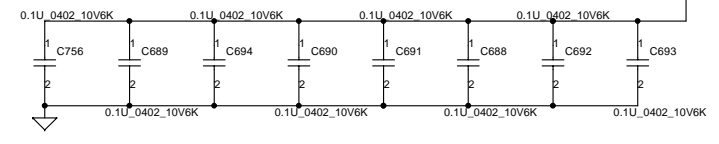
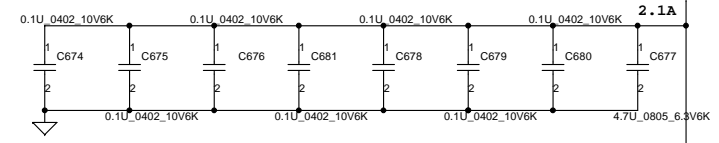
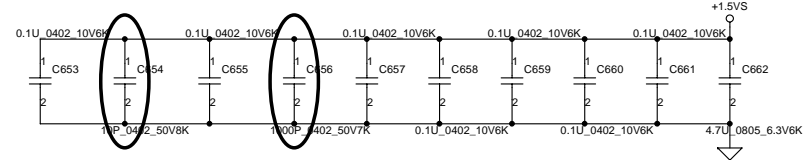
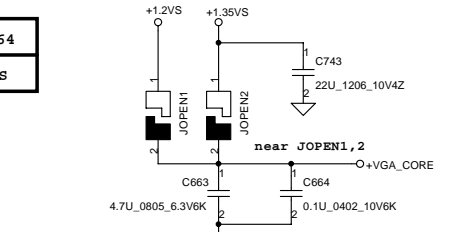
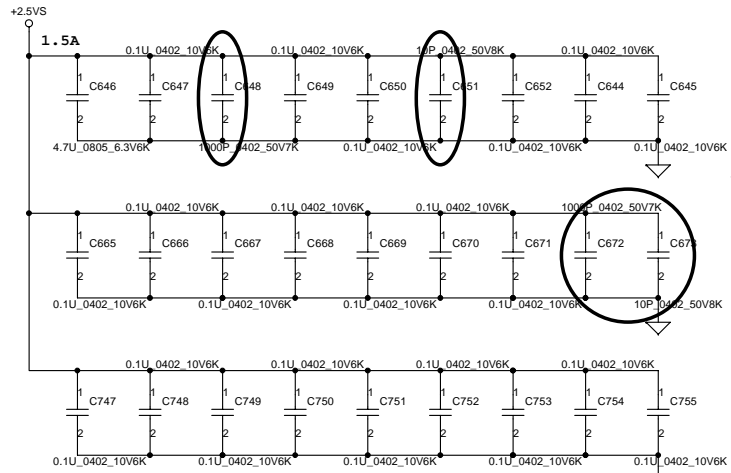








	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS



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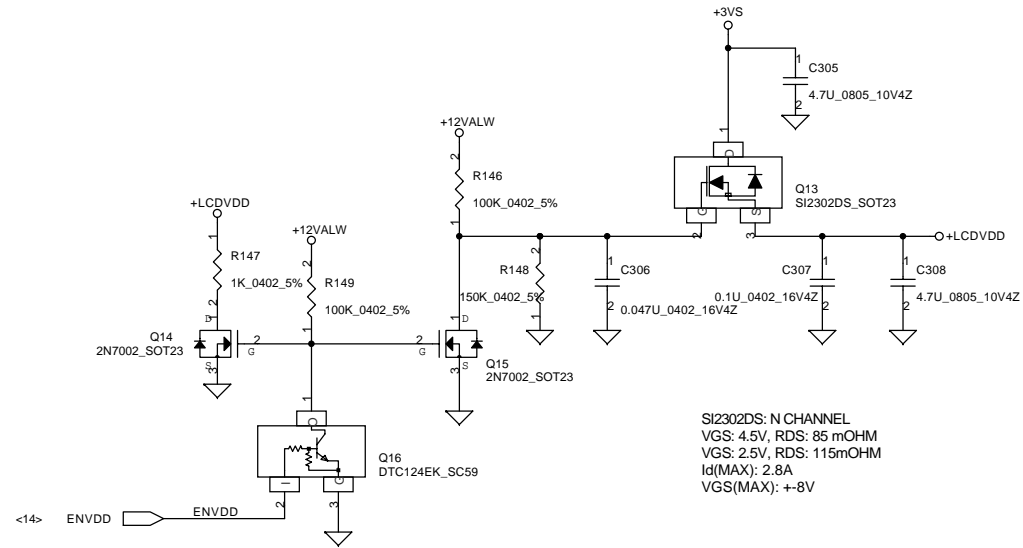
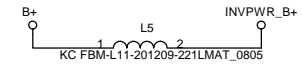
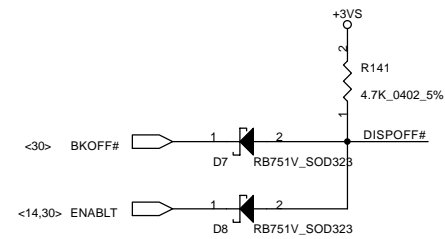
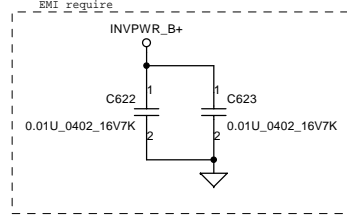
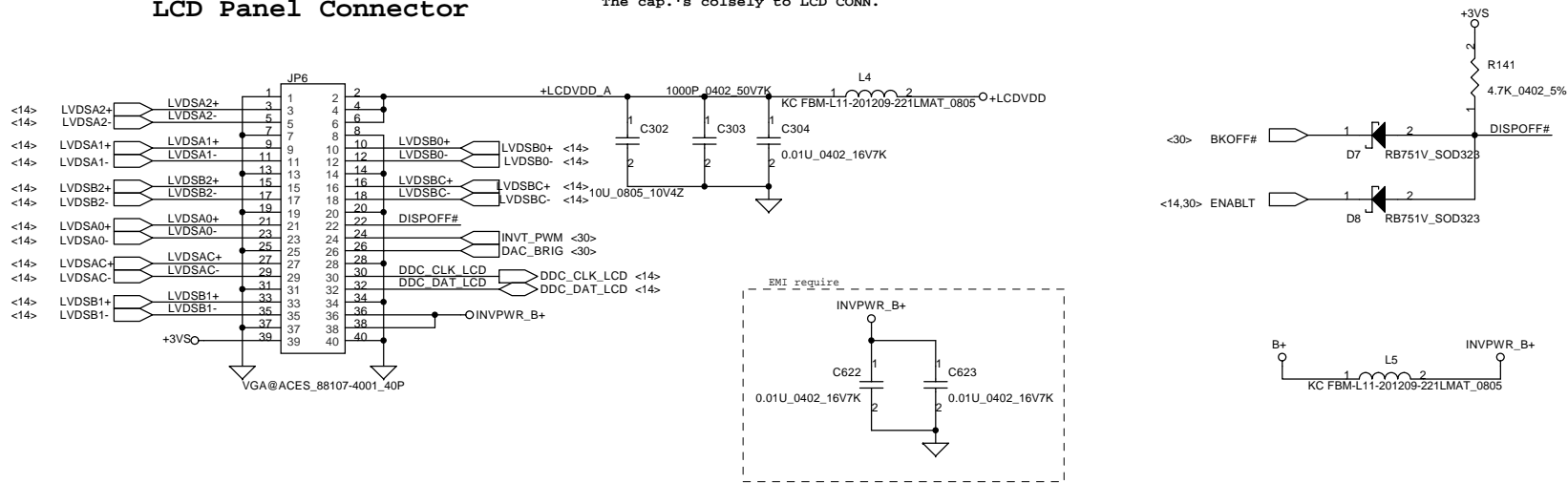
<b>Compal Electronics, Inc.</b>			
<b>SCHEMATIC, MB ASSY LA-1851</b>			
Title			
Size	Document Number		
Custom	<b>401254</b>		
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# LCD Panel Connector

The cap.'s colselly to LCD CONN.

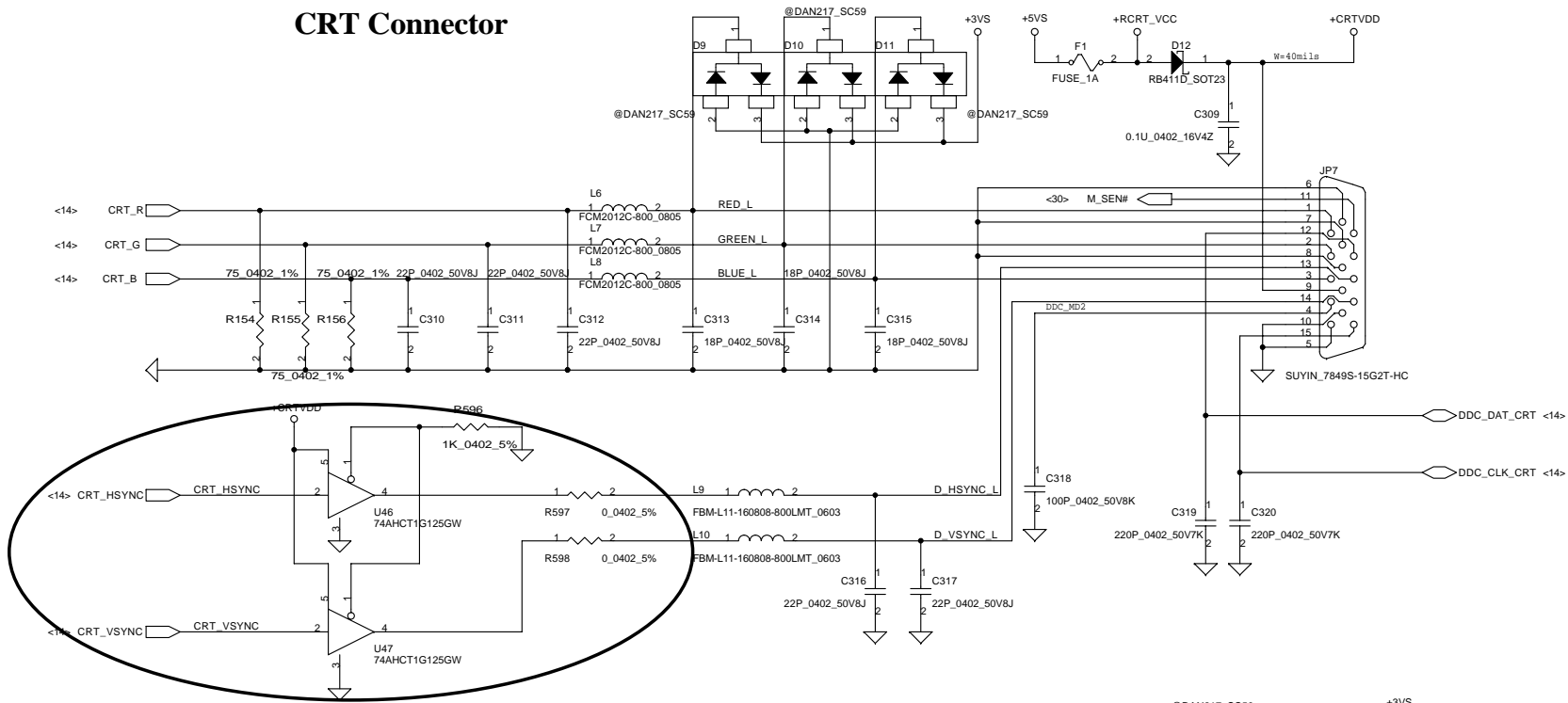


SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +-8V

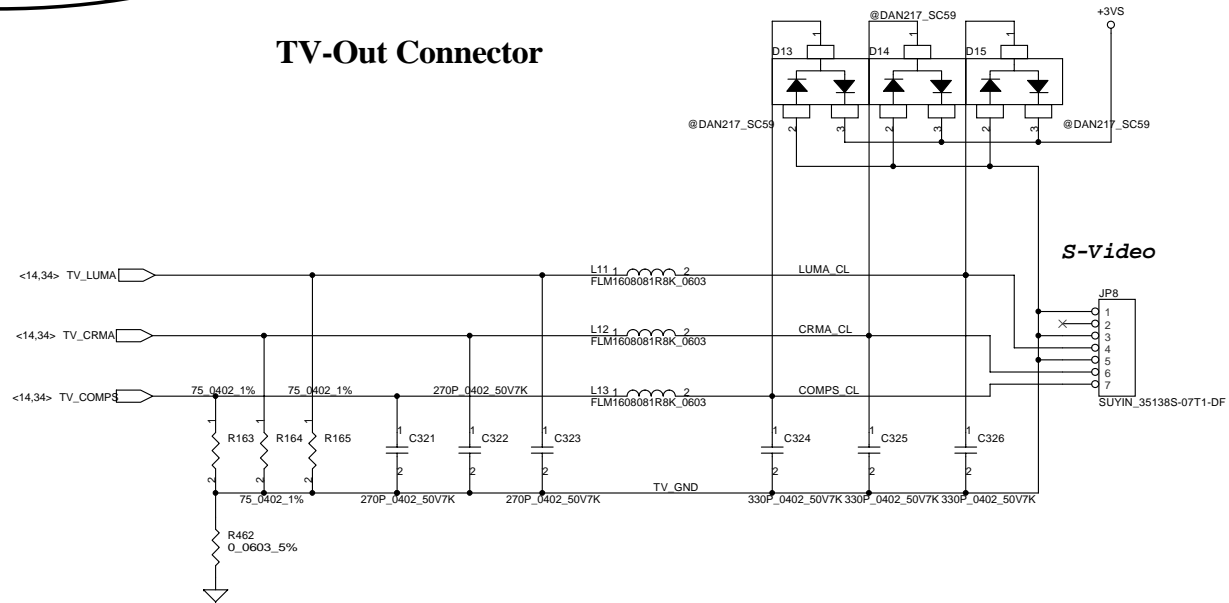
<b>Compal Electronics, Inc.</b>		
Title <b>SCHEMATIC, MB ASSY LA-1851</b>		
Size	Document Number <b>401254</b>	Rev <b>0B</b>
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# CRT Connector



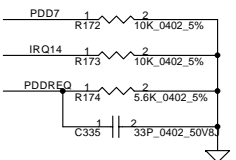
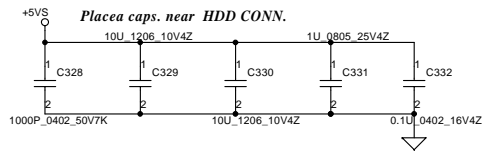
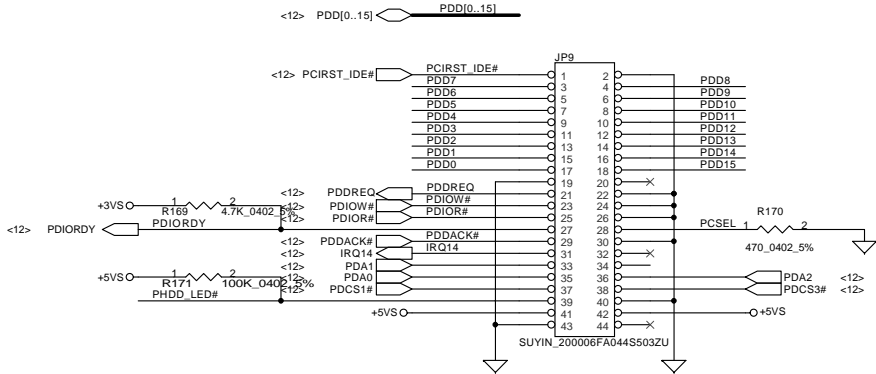
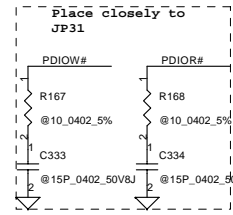
# TV-Out Connector



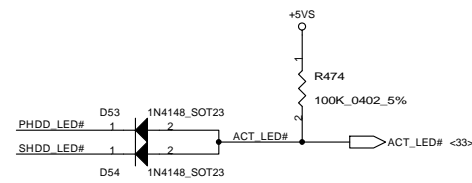
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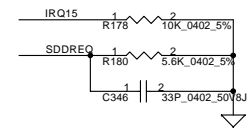
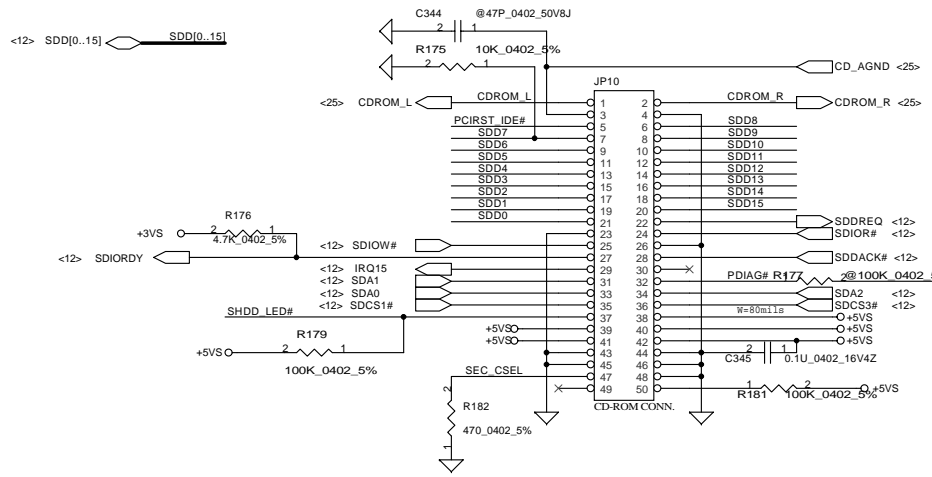
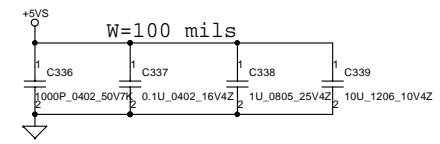
# HDD Connector



# CD-ROM Connector



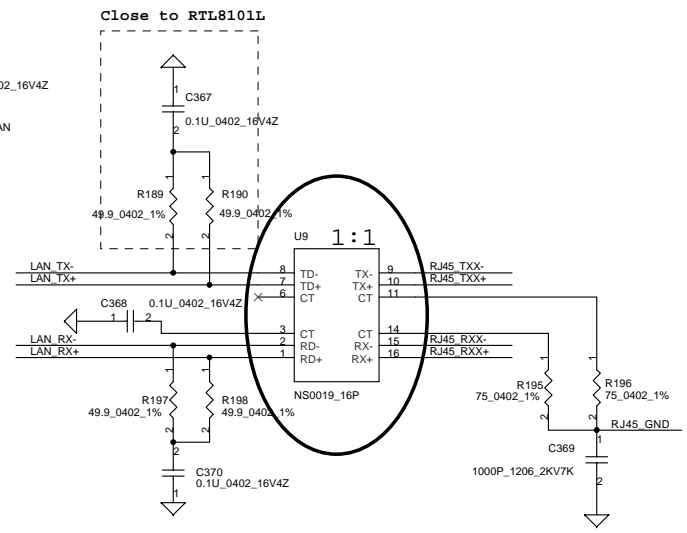
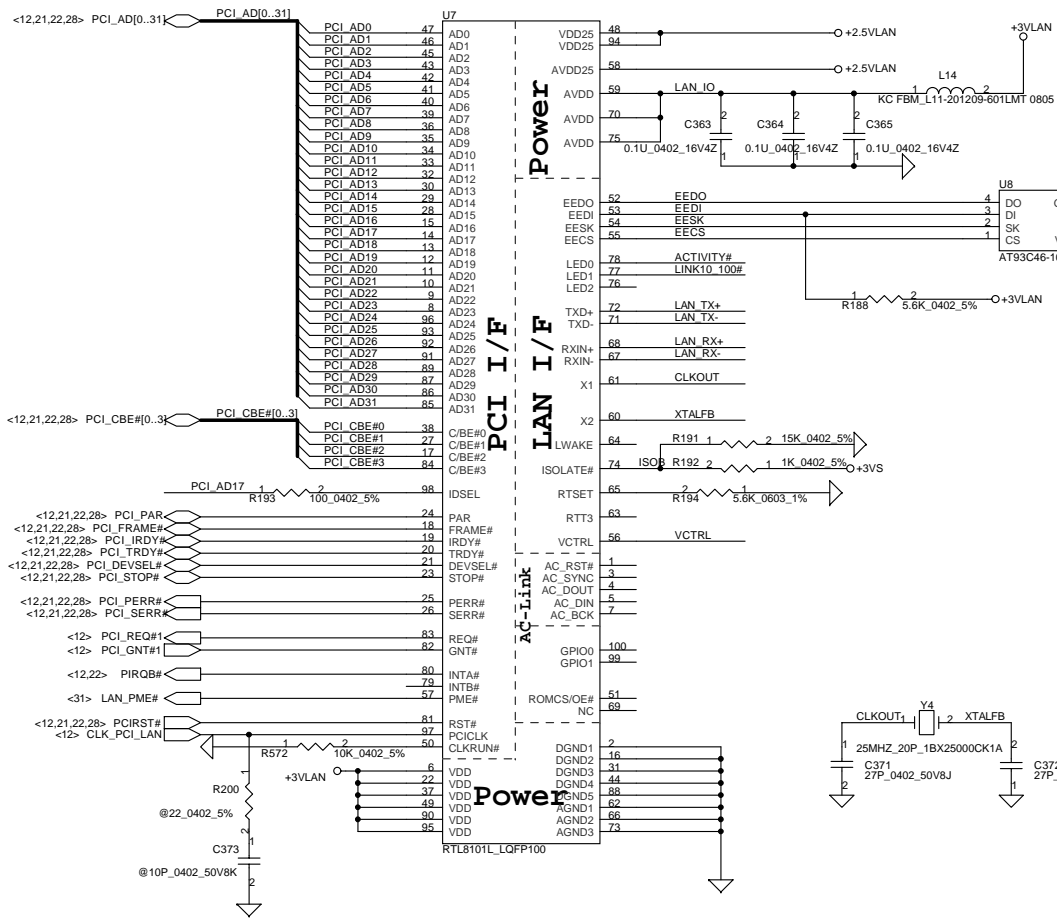
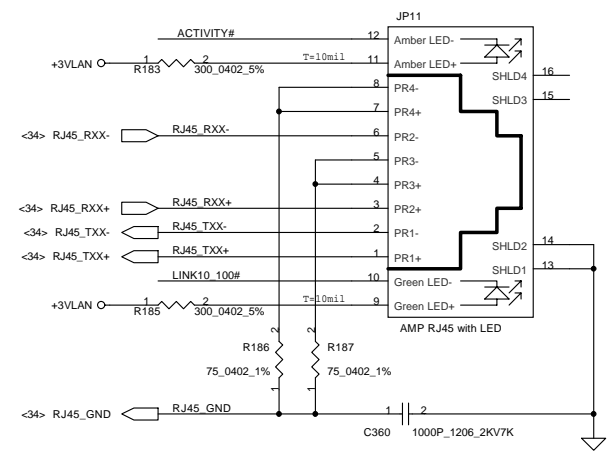
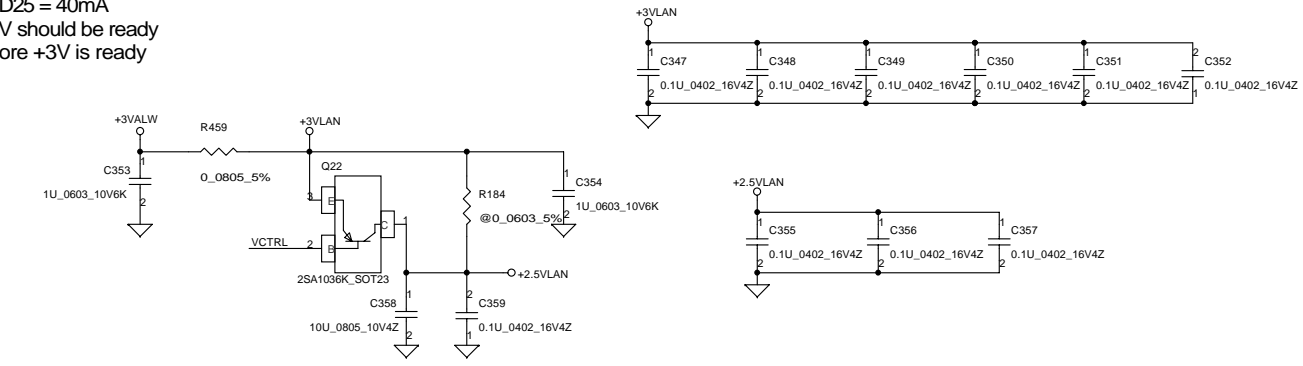
# Place caps. near CDROM CONN.



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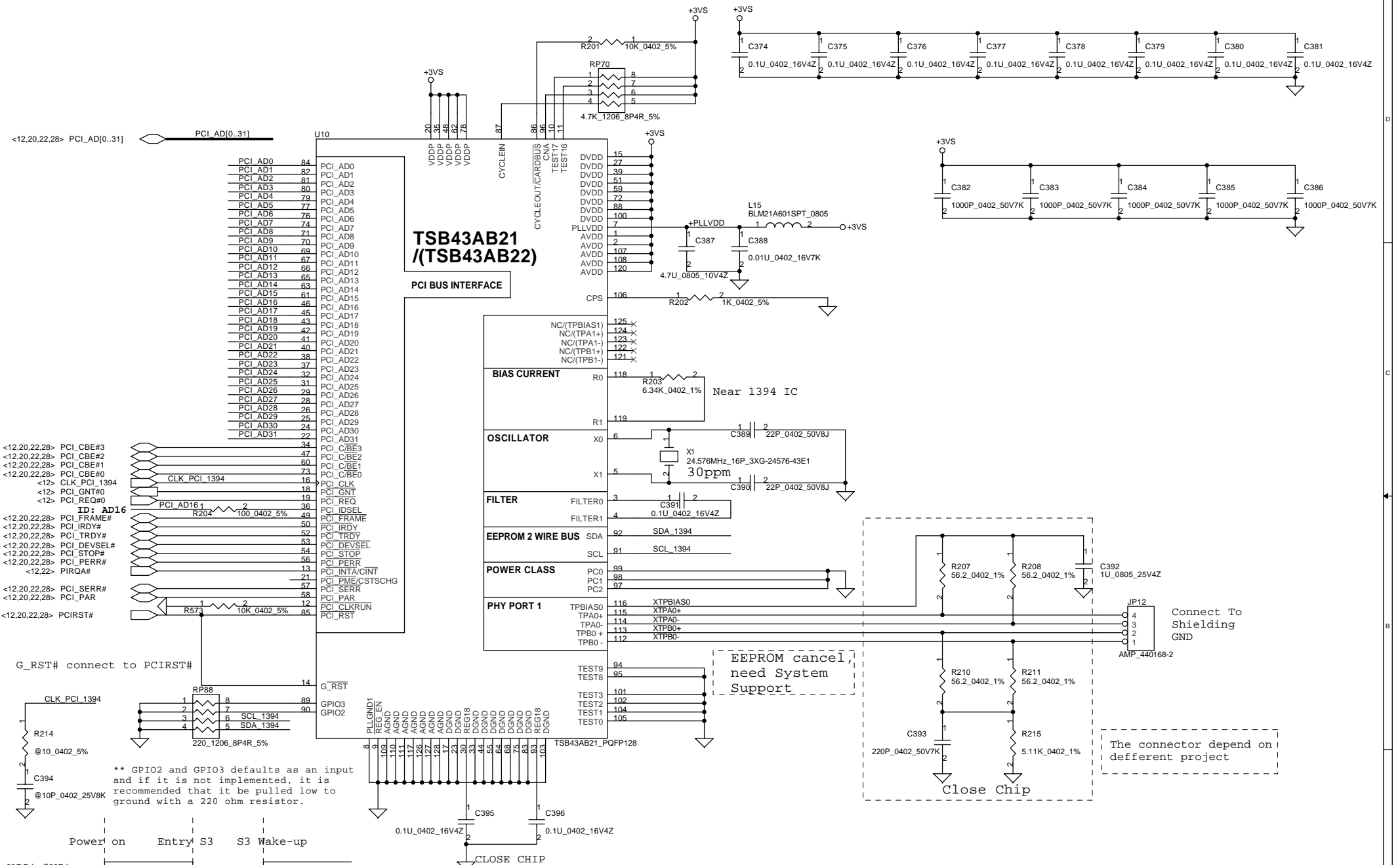
Note : I\_max for  
VDD25 = 40mA  
2.5V should be ready  
before +3V is ready



- Layout Recommend :
1. LAN\_RD+, LAN\_RD- should be equal length as possible
  2. LAN\_TD+, LAN\_TD- should be equal length as possible
  3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
  4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

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<12.0,22.28> PCI\_AD[0..31]

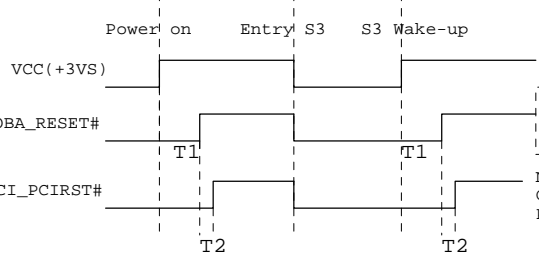
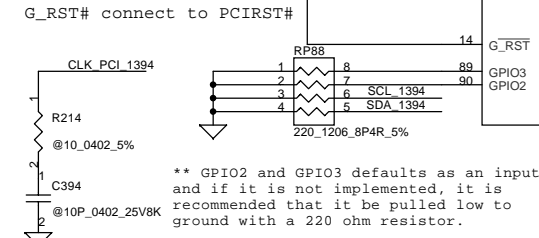
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 <12.20,22.28> PCI\_CBE#2  
 <12.20,22.28> PCI\_CBE#1  
 <12.20,22.28> PCI\_CBE#0  
 <12> CLK\_PCI\_1394  
 <12> PCI\_GNT#0  
 <12> PCI\_REC#0  
 ID: AD16  
 <12.20,22.28> PCI\_FRAME#  
 <12.20,22.28> PCI\_IRDY#  
 <12.20,22.28> PCI\_TRDY#  
 <12.20,22.28> PCI\_DEVSEL#  
 <12.20,22.28> PCI\_STOP#  
 <12.20,22.28> PCI\_PERR#  
 <12.22> PIRQA#  
 <12.20,22.28> PCI\_SERR#  
 <12.20,22.28> PCI\_PAR  
 <12.20,22.28> PCIRST#

PCI_AD0	84	PCI_AD0
PCI_AD1	82	PCI_AD1
PCI_AD2	81	PCI_AD2
PCI_AD3	80	PCI_AD3
PCI_AD4	79	PCI_AD4
PCI_AD5	77	PCI_AD5
PCI_AD6	76	PCI_AD6
PCI_AD7	74	PCI_AD7
PCI_AD8	71	PCI_AD8
PCI_AD9	70	PCI_AD9
PCI_AD10	69	PCI_AD10
PCI_AD11	67	PCI_AD11
PCI_AD12	66	PCI_AD12
PCI_AD13	65	PCI_AD13
PCI_AD14	63	PCI_AD14
PCI_AD15	61	PCI_AD15
PCI_AD16	46	PCI_AD16
PCI_AD17	45	PCI_AD17
PCI_AD18	43	PCI_AD18
PCI_AD19	42	PCI_AD19
PCI_AD20	41	PCI_AD20
PCI_AD21	40	PCI_AD21
PCI_AD22	38	PCI_AD22
PCI_AD23	37	PCI_AD23
PCI_AD24	32	PCI_AD24
PCI_AD25	31	PCI_AD25
PCI_AD26	29	PCI_AD26
PCI_AD27	28	PCI_AD27
PCI_AD28	26	PCI_AD28
PCI_AD29	25	PCI_AD29
PCI_AD30	24	PCI_AD30
PCI_AD31	22	PCI_AD31

**TSB43AB21  
(TSB43AB22)**

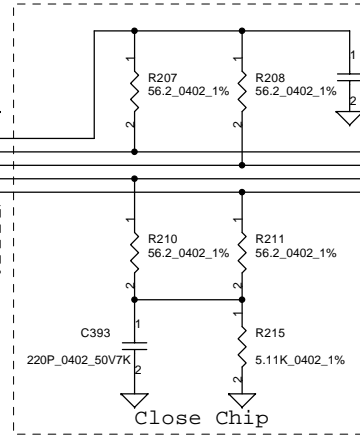
**PCI BUS INTERFACE**

NC(TPBIAS1)	125	X
NC(TPA1+)	124	X
NC(TPA1-)	123	X
NC(TPB1+)	122	X
NC(TPB1-)	121	X
<b>BIAS CURRENT</b>		
R0	118	6.34K_0402_1%
R1	119	
<b>OSCILLATOR</b>		
X0	6	22P_0402_50V8J
X1	5	24.576MHz_16P_3XG-24576-43E1
<b>FILTER</b>		
FILTER0	3	22P_0402_50V8J
FILTER1	4	0.1U_0402_16V4Z
<b>EEPROM 2 WIRE BUS</b>		
SDA	92	SDA_1394
SCL	91	SCL_1394
<b>POWER CLASS</b>		
PC0	99	
PC1	98	
PC2	97	
<b>PHY PORT 1</b>		
TPBIAS0	116	XTPBIAS0
TPA0+	115	XTPA0+
TPA0-	114	XTPA0-
TPB0+	113	XTPB0+
TPB0-	112	XTPB0-



Note: GLOBAL\_RESET#  
Can Connect to  
PCI\_PCIRST#

EEPROM cancel  
need System  
Support



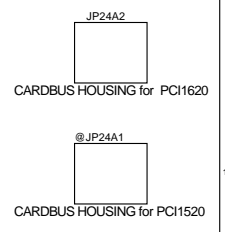
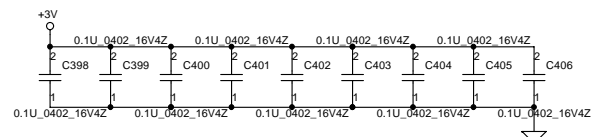
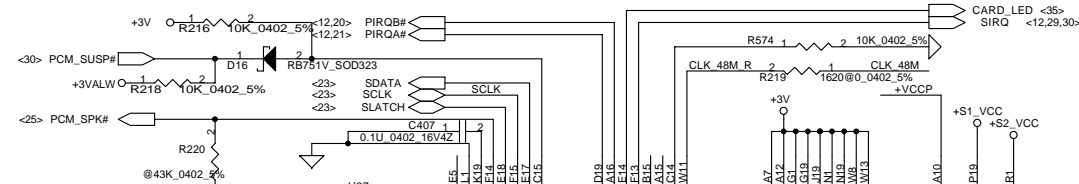
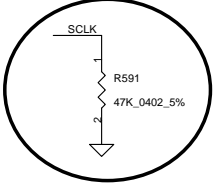
Connect To  
Shielding  
GND

AMP\_440168-2

The connector depend on  
defferent project

Compal Electronics, Inc.		
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S2	Pin	Function
S2_D0	W10	B_CAD27/B_D0
S2_D1	L10	B_CAD29/B_D1
S2_D2	P10	B_CAD08/B_D2
S2_D3	H3	B_CAD10/B_D3
S2_D4	H1	B_CAD1/B_D4
S2_D5	J2	B_CAD3/B_D5
S2_D6	J5	B_CAD5/B_D6
S2_D7	K2	B_CAD05/B_D7
S2_D8	V10	B_CAD28/B_D8
S2_D9	R10	B_CAD30/B_D9
S2_D10	V11	B_CAD31/B_D10
S2_D11	H2	B_CAD4/B_D11
S2_D12	J1	B_CAD4/B_D12
S2_D13	J4	B_CAD6/B_D13
S2_D14	J6	B_RSVD/B_D14
S2_D15	K3	B_CAD8/B_D15
S2_A0	R8	B_CAD26/A_0
S2_A1	W7	B_CAD25/A_1
S2_A2	V7	B_CAD24/A_2
S2_A3	P8	B_CAD23/A_3
S2_A4	V8	B_CAD22/A_4
S2_A5	U8	B_CAD21/A_5
S2_A6	V6	B_CAD20/A_6
S2_A7	U5	B_CAD18/A_7
S2_A8	M6	B_CC/BE1/A_8
S2_A9	M5	B_CAD14/A_9
S2_A10	K6	B_CAD9/A_10
S2_A11	L6	B_CAD12/A_11
S2_A12	T1	B_CC/BE2/A_12
S2_A13	N2	B_CPAR/A_13
S2_A14	N6	B_CPER/A_14
S2_A15	P5	B_CIRDY/A_15
S2_A16	P6	B_CCLK/A_16
S2_A17	M3	B_CAD16/A_17
S2_A18	M5	B_RSVD/A_18
S2_A19	N3	B_CBLOCK/A_19
S2_A20	P2	B_CSTOP/A_20
S2_A21	P3	B_CDEVSL/A_21
S2_A22	R2	B_CTRDY/A_22
S2_A23	R3	B_CFRAME/A_23
S2_A24	W4	B_CAD17/A_24
S2_A25	R6	B_CAD19/A_25

FUNCTION POWER

# CARDBUS CONTROLLER PCI1520 PBGA 209

SLOT B

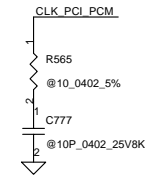
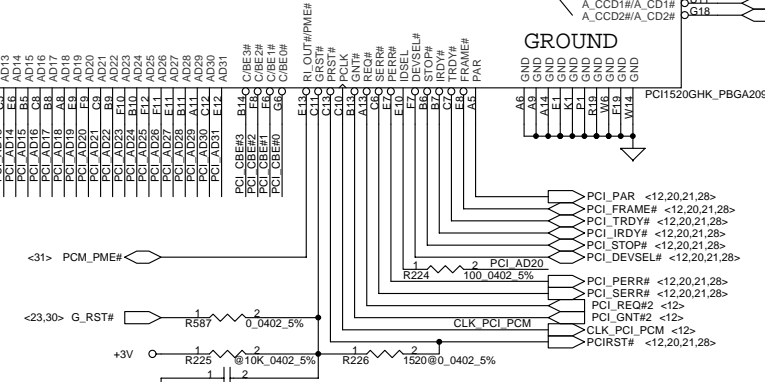
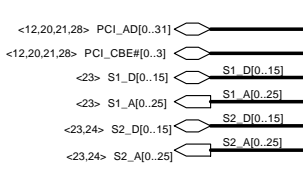
SLOT A

<23,24>	S2_RST	W5	B_CRST#/B_RESET
<23,24>	S2_WE#	N6	B_CGNT/B_WE#
<23>	S2_IOWR#	M1	B_CAD15/B_IOWR#
<23>	S2_IORD#	L5	B_CAD13/B_IORD#
<23,24>	S2_REG#	L3	B_CC/BE3#/B_REG#
<23,24>	S2_OE#	R7	B_CAD11/A_OE#
<23,24>	S2_INPACK#	R2	B_CREQ#/B_INPACK#
<23,24>	S2_RDY#	V6	B_CINT#/B_IREQ#
<23,24>	S2_BVD2	V8	B_CAUDIO/B_SPKR#
<23,24>	S2_WAIT#	V9	B_CSERR#/B_WAIT#
<23,24>	S2_BVD1	U9	B_CSTSCHG/B_STSCHG#
<23>	S2_WP	R9	B_CCLKRUN/B_IOIS16#
<23,24>	S2_VS1	U8	B_CVS1/B_VS1#
<23,24>	S2_VS2	P7	B_CVS2/B_VS2#
<23,24>	S2_CE1#	K5	B_CC/BE0/B_CE1#
<23>	S2_CE2#	L2	B_CAD10/B_CE2#
<23,24>	S2_CD1#	H6	B_CCD1#/B_CD1#
<23,24>	S2_CD2#	P9	B_CCD2#/B_CD2#

PCI INTERFACE

A_CAD27/A_D0	G17	S1_D0
A_CAD29/A_D1	F18	S1_D1
A_RSVD/A_D2	F17	S1_D2
A_CAD08/A_D3	P11	S1_D3
A_CAD1/A_D4	W12	S1_D4
A_CAD3/A_D5	U12	S1_D5
A_CAD5/A_D6	U13	S1_D7
A_CAD7/A_D7	R12	S1_D5
A_CAD28/A_D8	G14	S1_D8
A_CAD30/A_D9	G15	S1_D10
A_CAD31/A_D10	F19	S1_D11
A_CAD2/A_D11	R11	S1_D11
A_CAD4/A_D12	V12	S1_D12
A_CAD6/A_D13	V13	S1_D14
A_RSVD/A_D14	P13	S1_D15
A_CAD8/A_D15		
A_CAD26/A_A0	H14	S1_A0
A_CAD25/A_A1	H7	S1_A1
A_CAD24/A_A2	K18	S1_A2
A_CAD23/A_A3	K18	S1_A3
A_CAD22/A_A4	L14	S1_A5
A_CAD21/A_A5	L17	S1_A6
A_CAD20/A_A6	M19	S1_A7
A_CAD18/A_A7	U15	S1_A8
A_CC/BE1/A_A8	M19	S1_A9
A_CAD14/A_A9	R13	S1_A10
A_CAD9/A_A10	P14	S1_A11
A_CAD12/A_A11	M17	S1_A12
A_CC/BE2/A_A12	P15	S1_A13
A_CPAR/A_A13	R18	S1_A14
A_CPER/A_A14	N18	S1_A15
A_CIRDY/A_A15	M14	S1_A16
A_CCLK/A_A16	W16	S1_A17
A_GAD16/A_A17	R17	S1_A18
A_RSVD/A_A18	N14	S1_A19
A_CBLOCK/A_A19	P17	S1_A20
A_CSTOP/A_A20	N15	S1_A21
A_CDEVSL/A_A21	M17	S1_A22
A_CTRDY/A_A22	M15	S1_A23
A_CFRAME/A_A23	M18	S1_A24
A_CAD17/A_A24	L19	S1_A25
A_CAD19/A_A25		
A_CRST#/A_RESET	D15	S1_RST <23>
A_CGNT/A_WE#	P18	S1_WE# <23>
A_CAD15/A_IOWR#	R14	S1_IOWR# <23>
A_CAD13/A_IORD#	V15	S1_IORD# <23>
A_CC/BE3/A_REG#	K14	S1_REG# <23>
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A_CREQ#/A_INPACK#	K17	S1_INPACK# <23>
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A_CAUDIO/A_SPKR#	H17	S1_BVD2 <23>
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A_CVS1/A_VS1#	J15	S1_VS1 <23>
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GROUND



**Compal Electronics, Inc.**

**SCHEMATIC, M/B ASSY LA-1851**

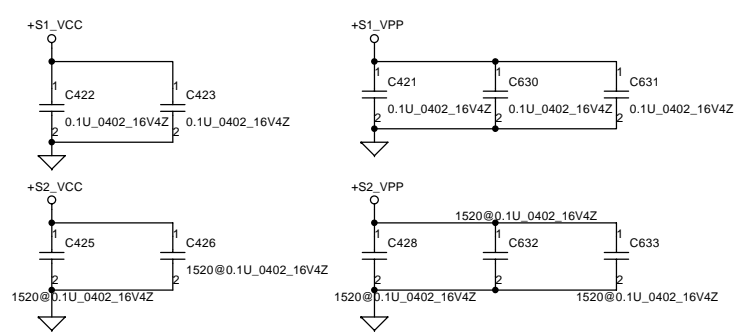
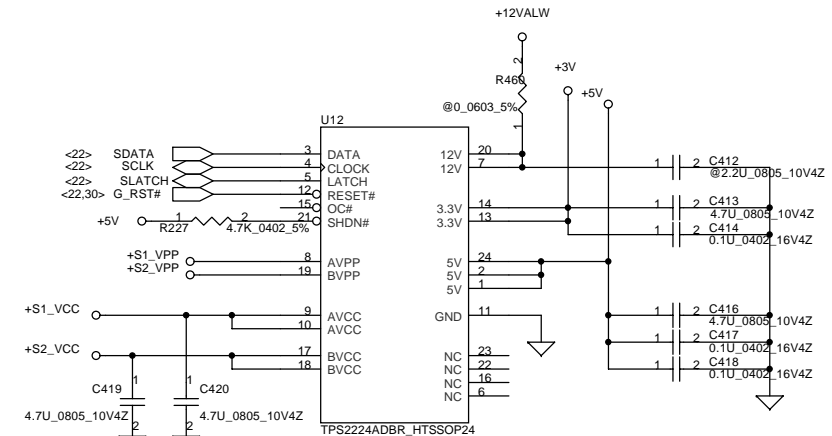
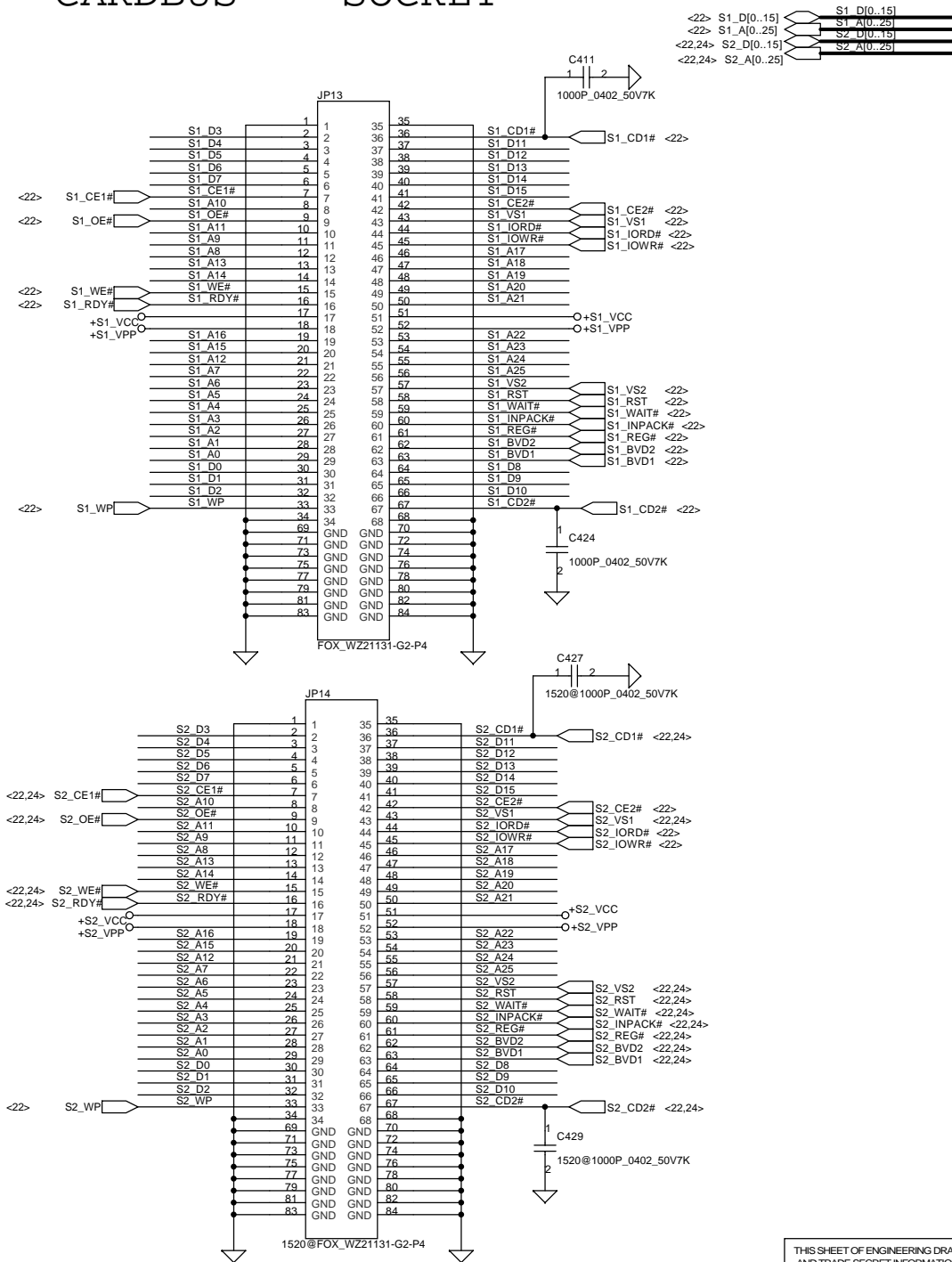
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# PCMCIA POWER CTRL.

## CARDBUS

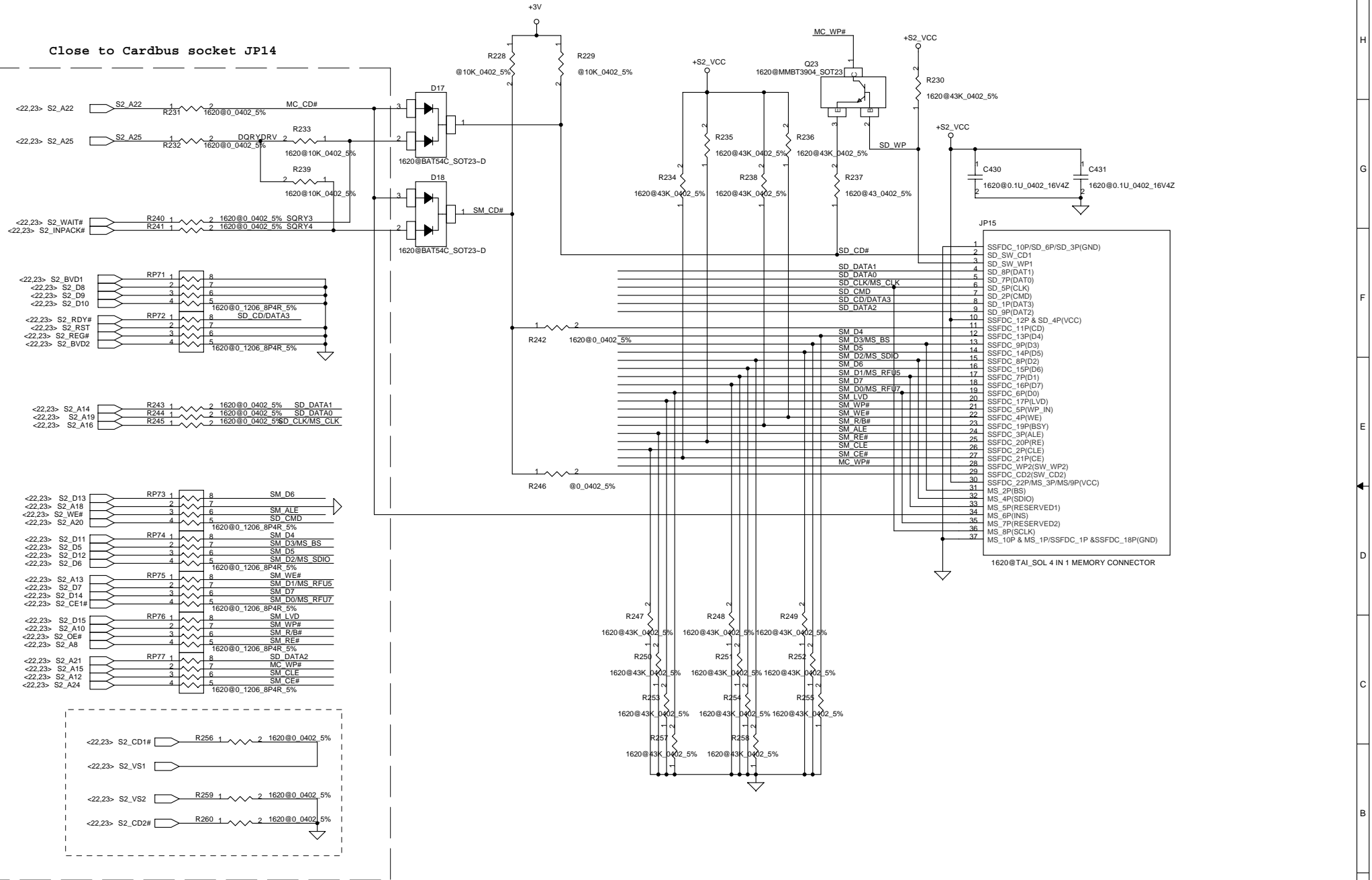
## SOCKET



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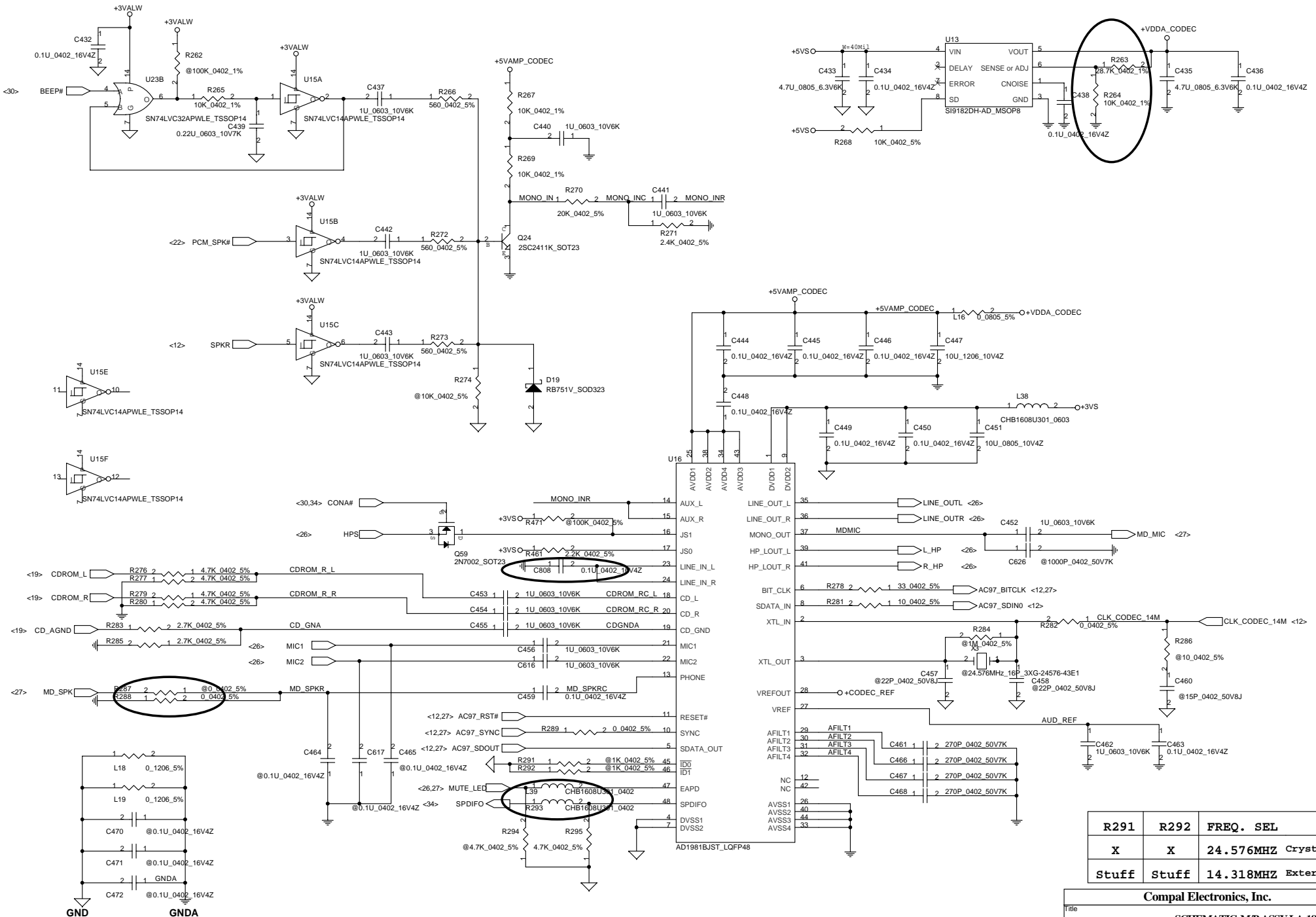
Close to Cardbus socket JP14



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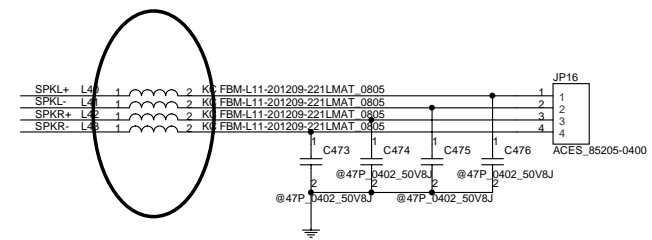
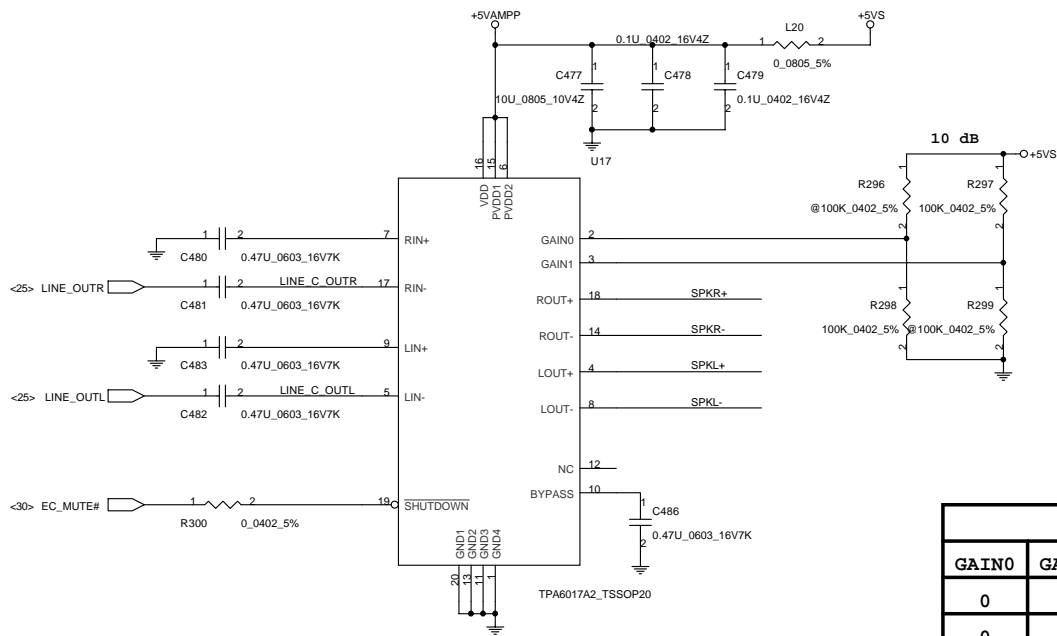
R291	R292	FREQ. SEL
X	X	24.576MHZ Crystal
Stuff	Stuff	14.318MHZ External

**Compal Electronics, Inc.**

**SCHEMATIC, M/B ASSY LA-1851**

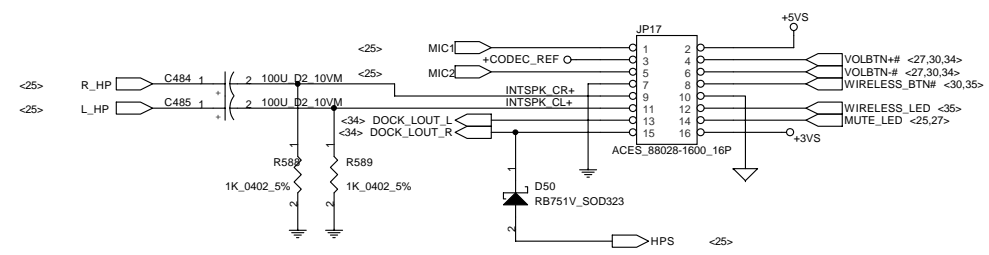
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Custom		
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Gain Settings		
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

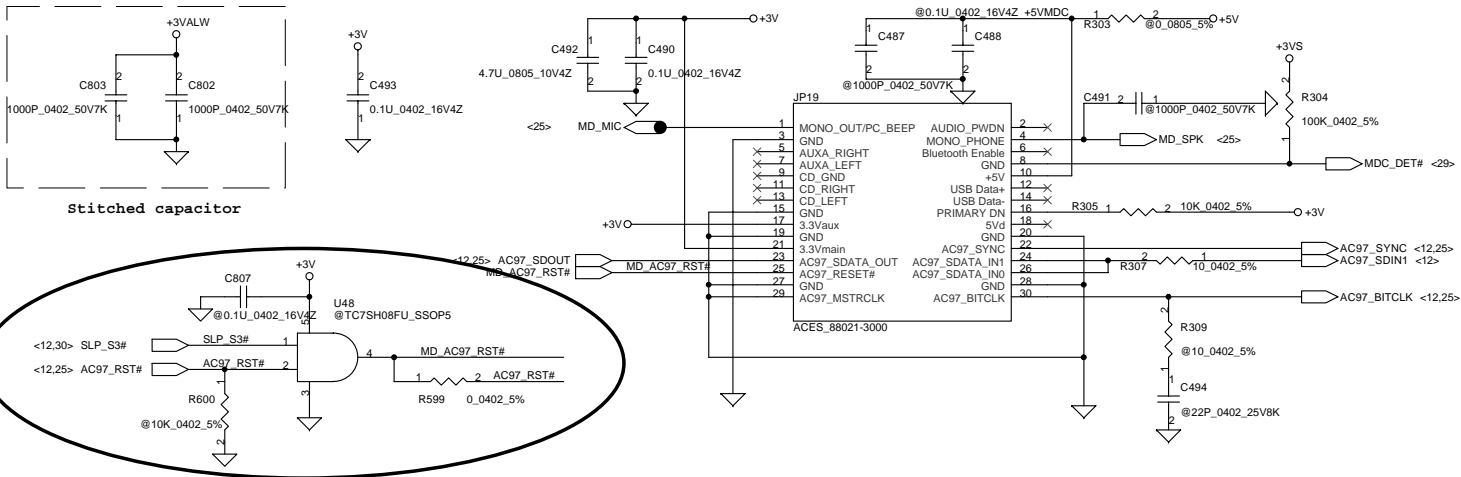
**AUDIO CONNECTOR**



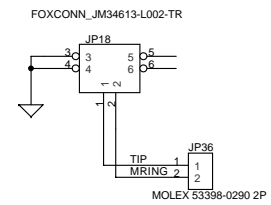
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**MDC Conn.**

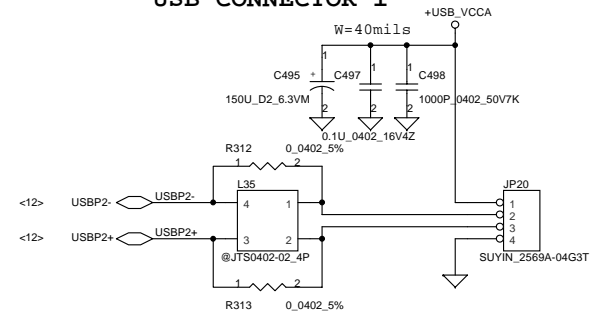


**RJ11 CONN.**

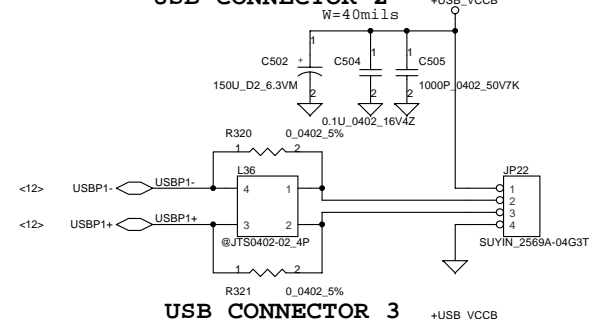


0: Have primary CODEC on mother board

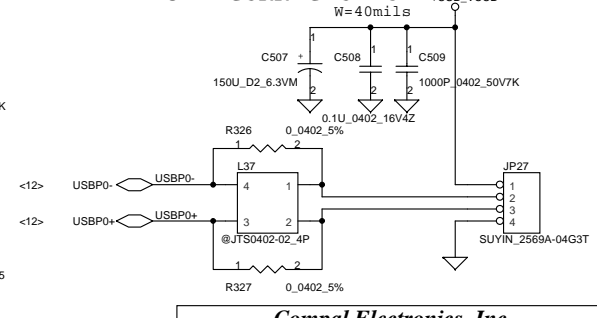
**USB CONNECTOR 1**

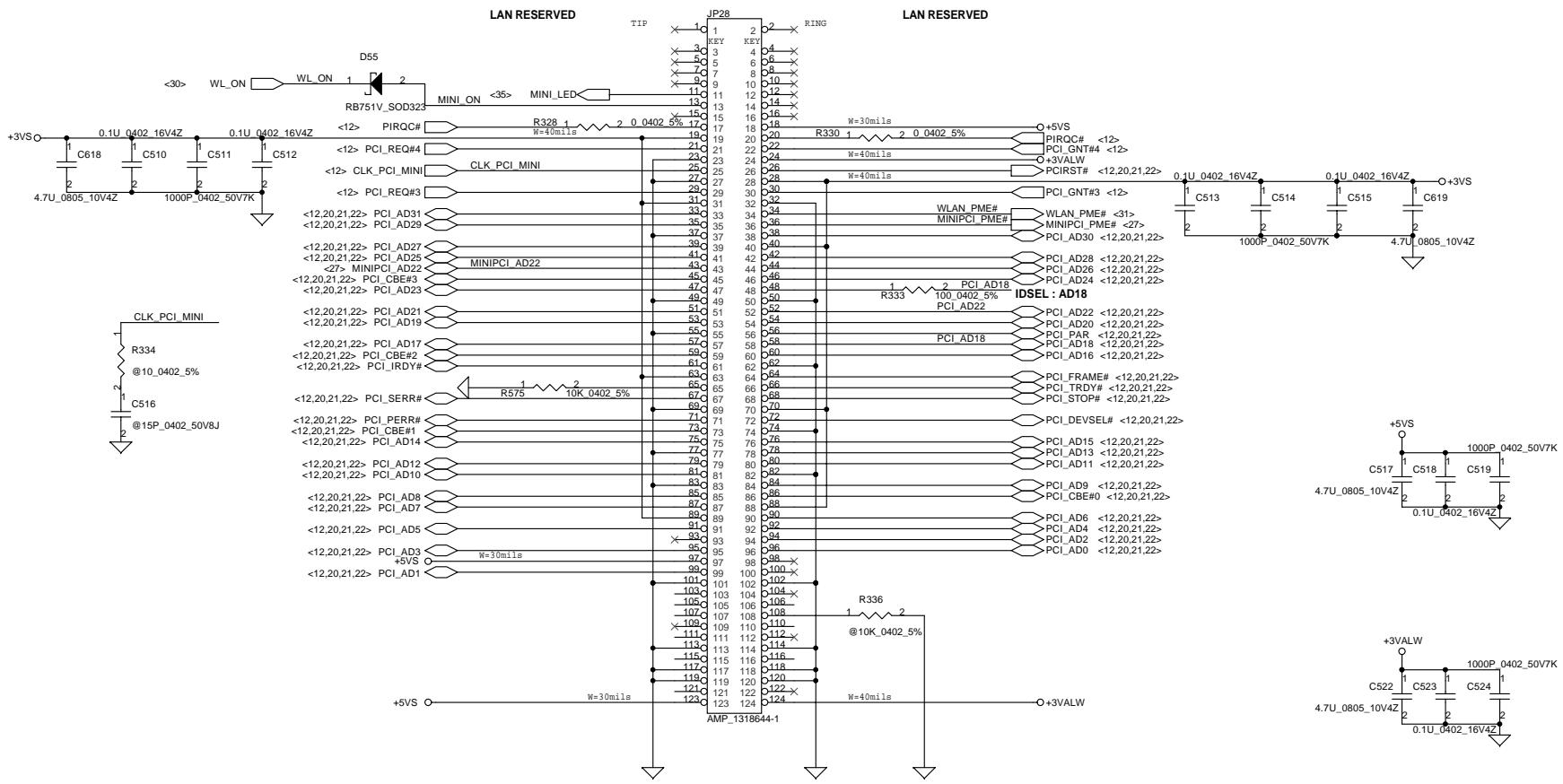


**USB CONNECTOR 2**



**USB CONNECTOR 3**





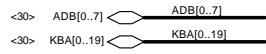
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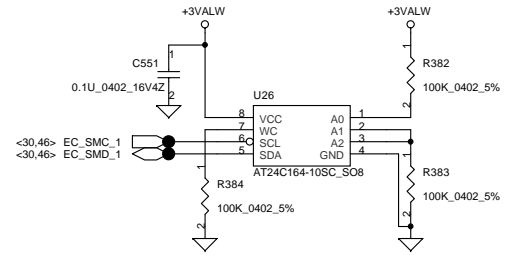
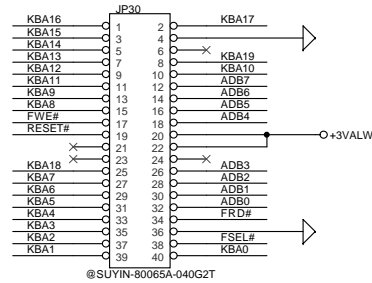
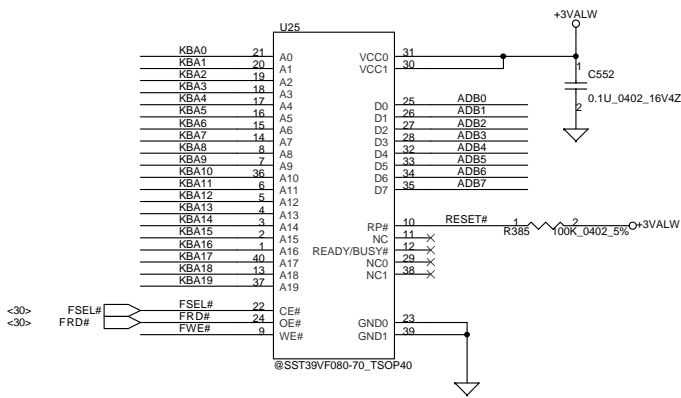
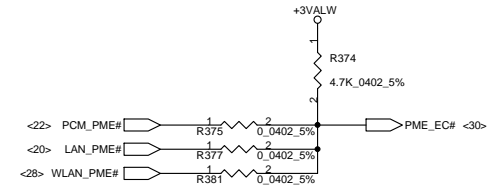
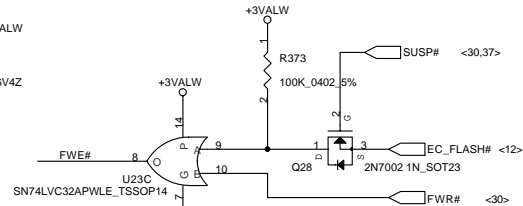
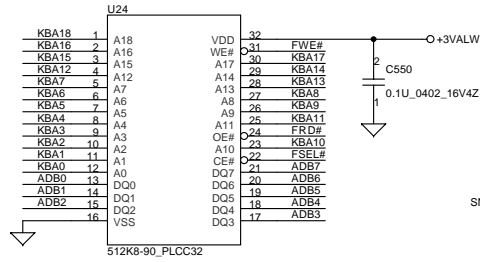
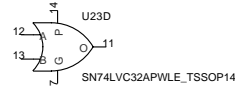
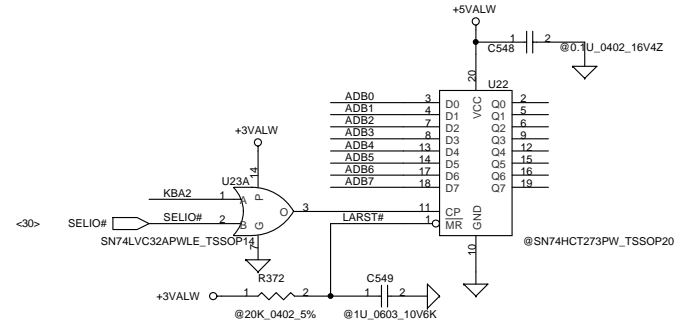




INPUT



OUTPUT

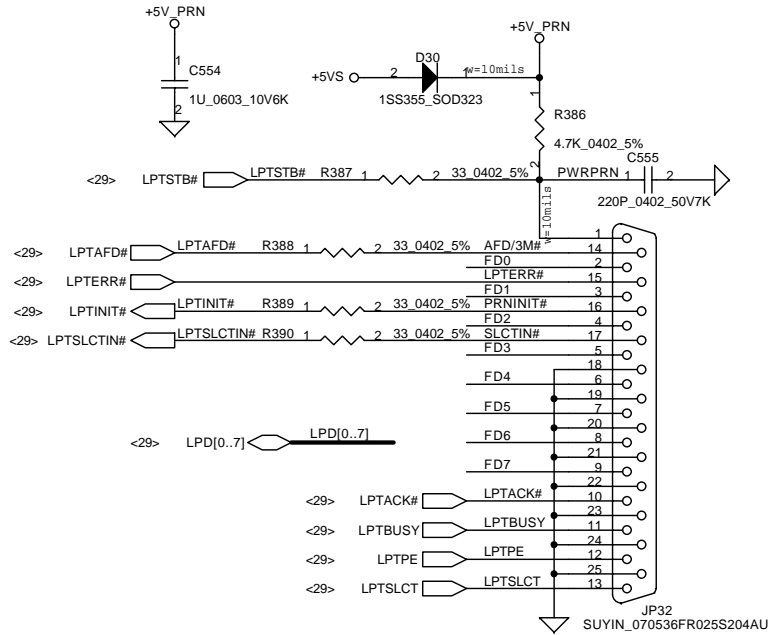


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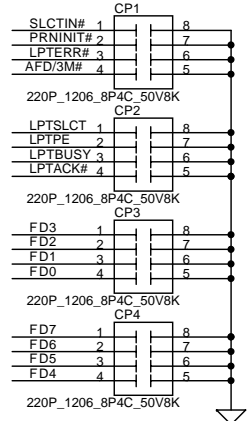
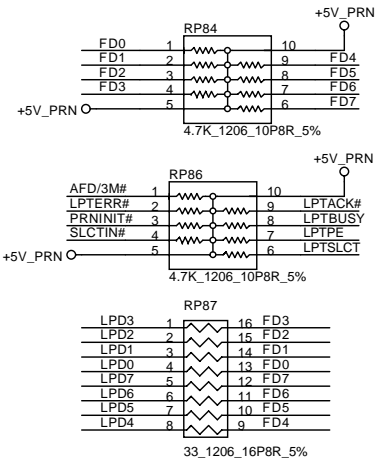
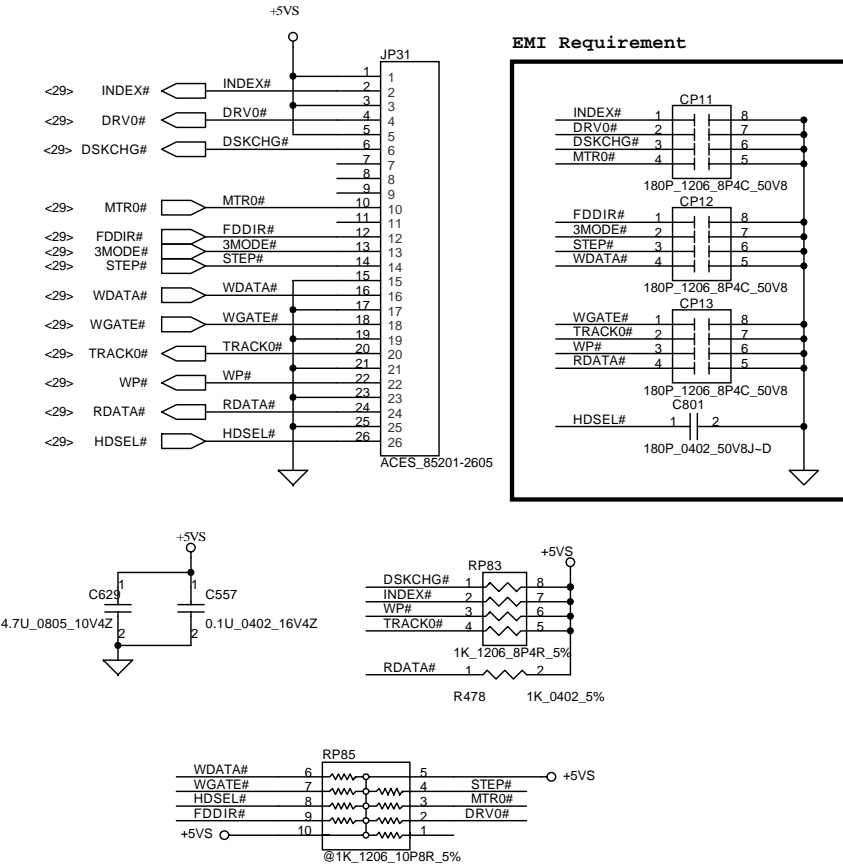
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# Parallel Port



# FDD CONN.



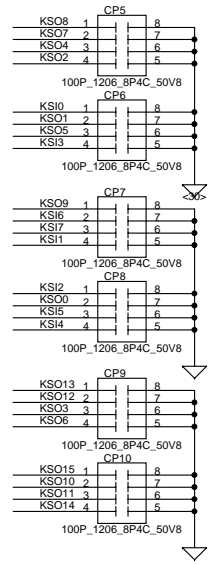
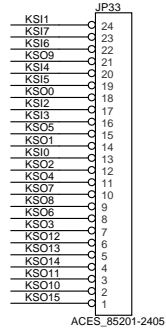
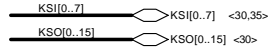
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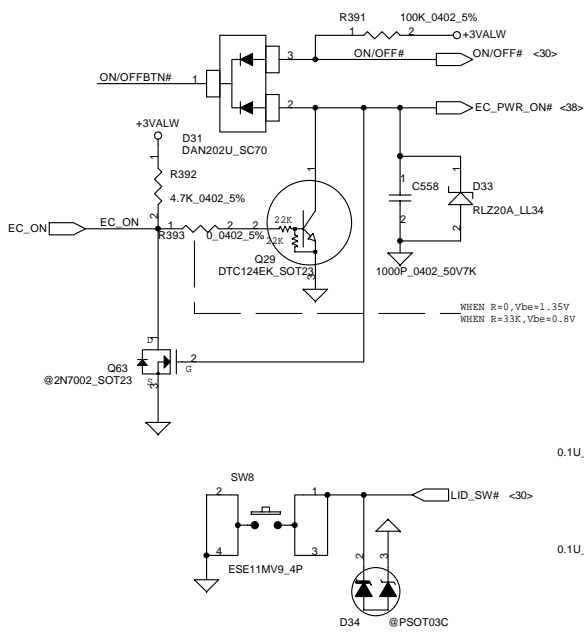
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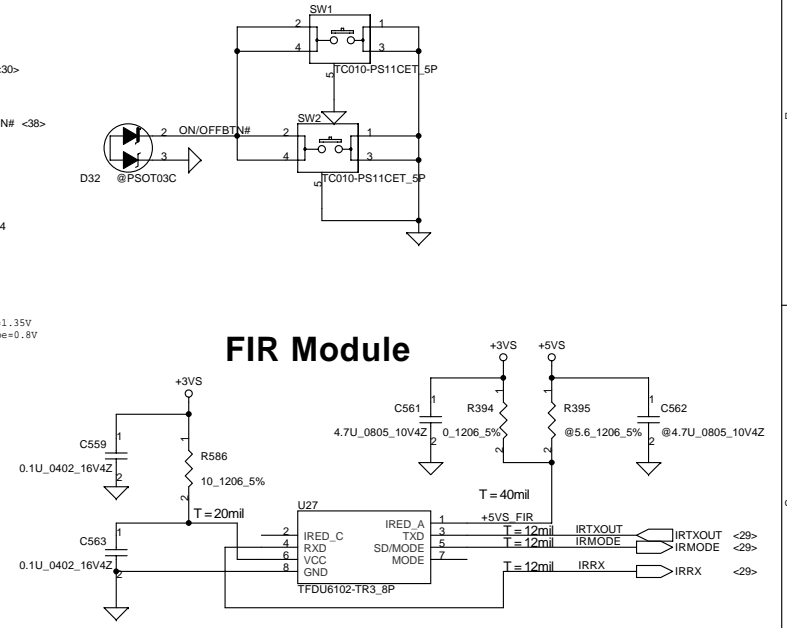
**INT\_KBD CONN.**



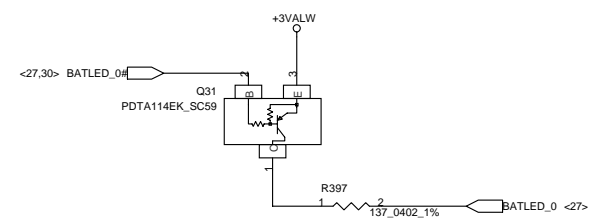
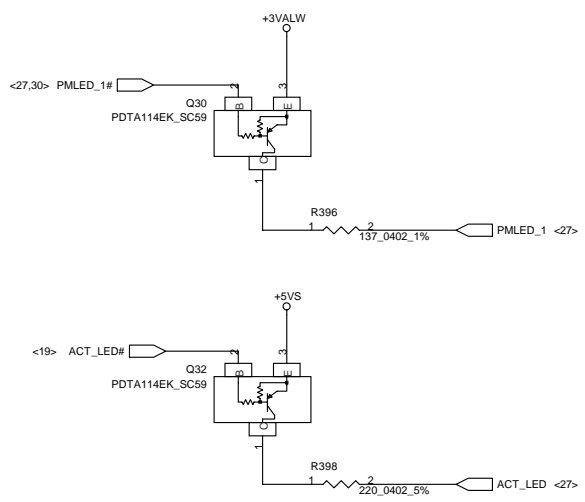
**Power BTN**



**FIR Module**

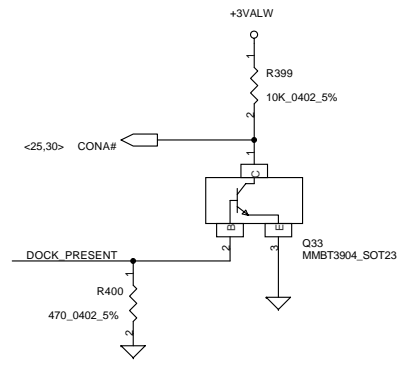
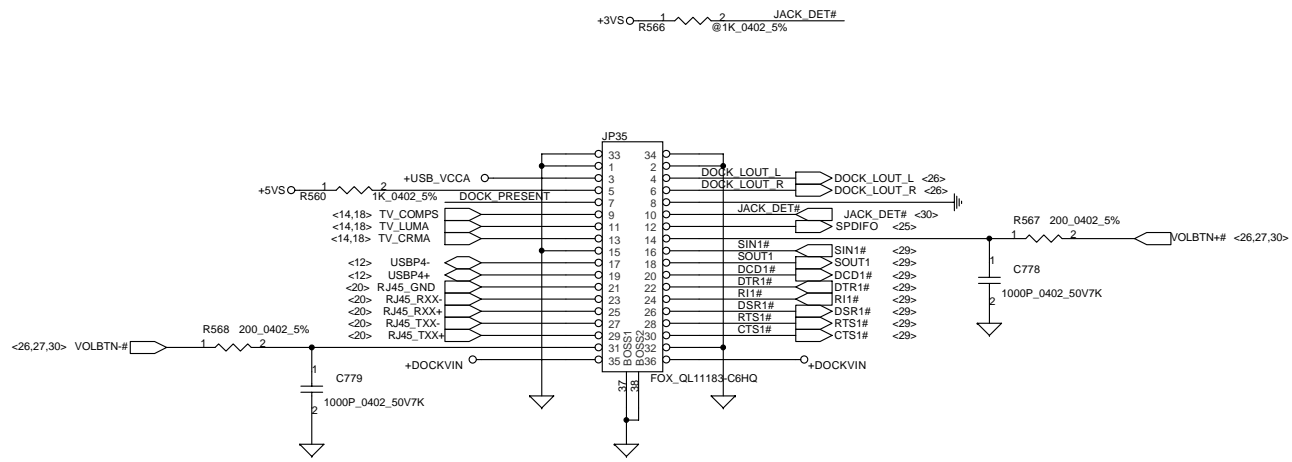


**Touch Pad & Status LED Conn.**

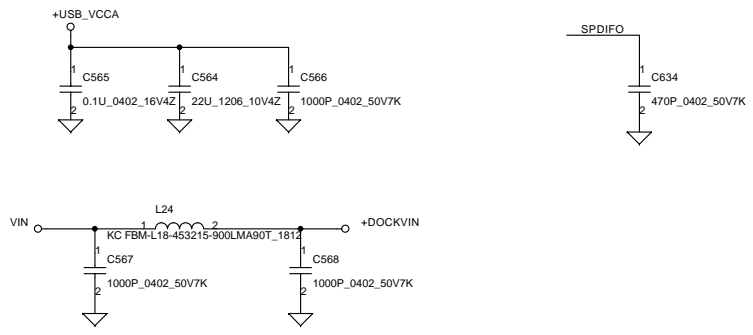
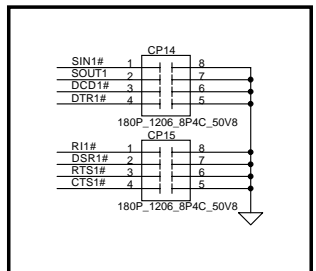


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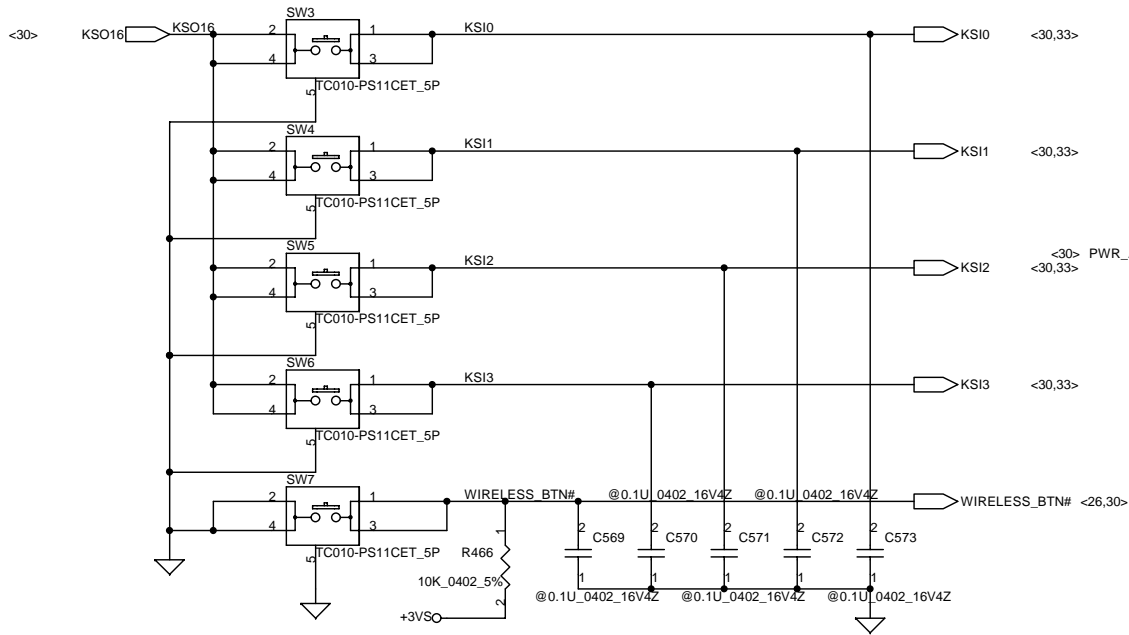


**EMI Requirement**

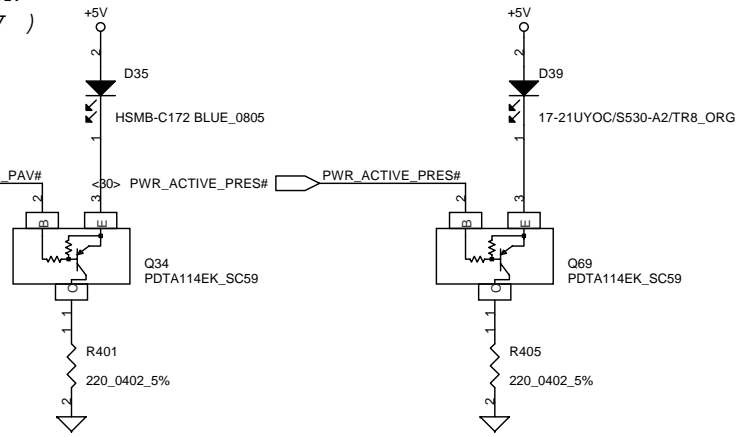


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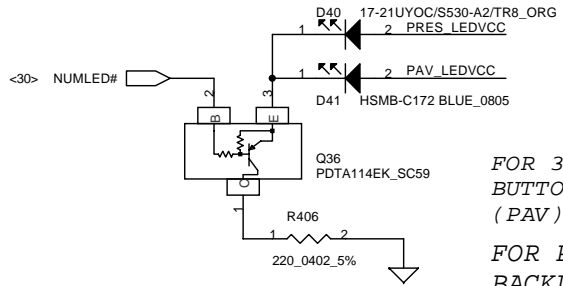
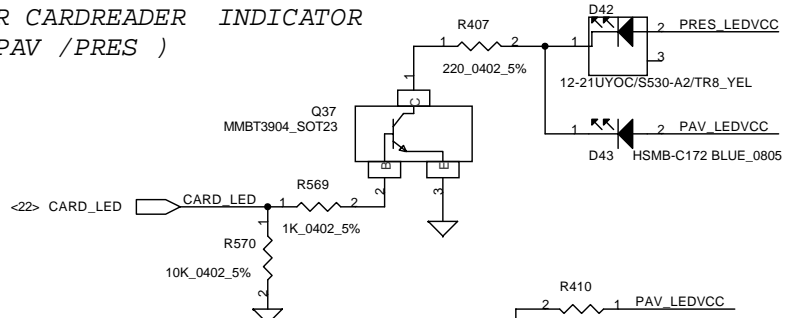
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FOR POWER BUTTON BACKLIGHT ( PAV )

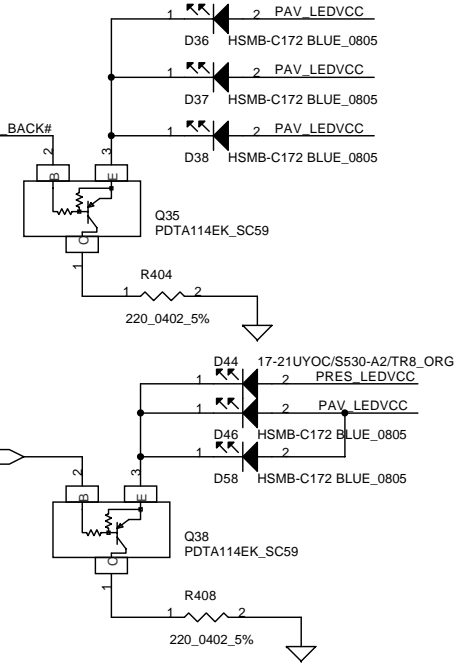


FOR CARDREADER INDICATOR ( PAV / PRES )

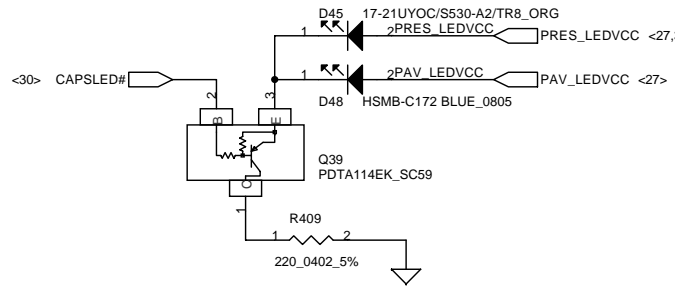
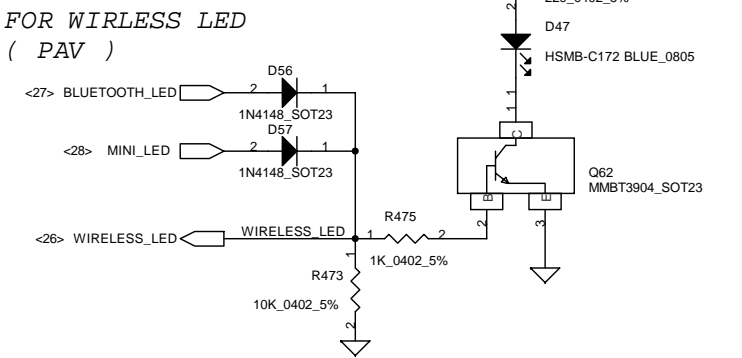


FOR 3 PROGRAMING BUTTON BACKLIGHT ( PAV )

FOR POWER BUTTON BACKLIGHT ( PRES )

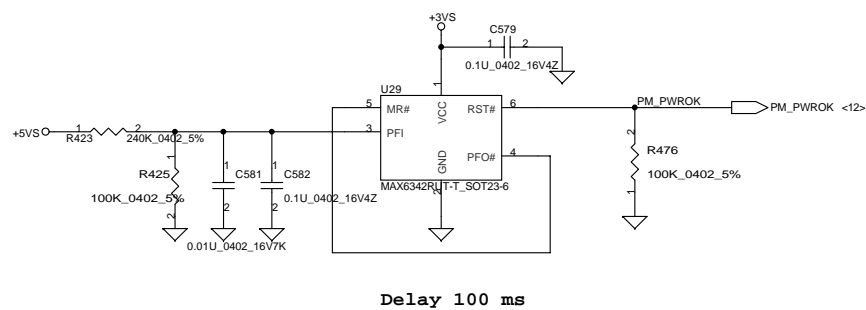
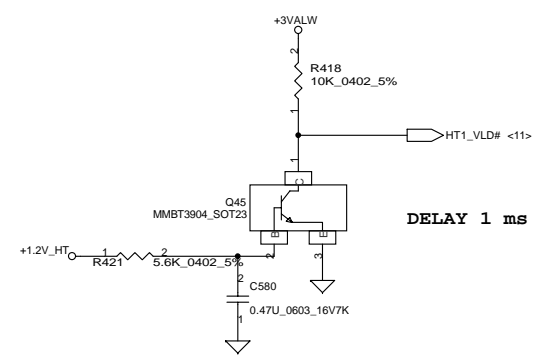
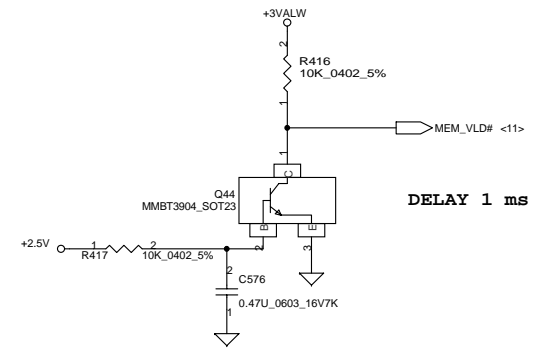
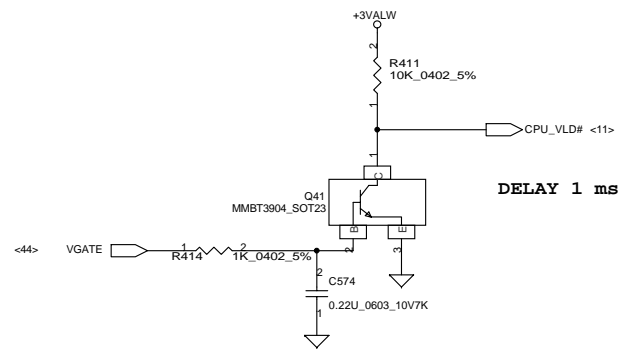
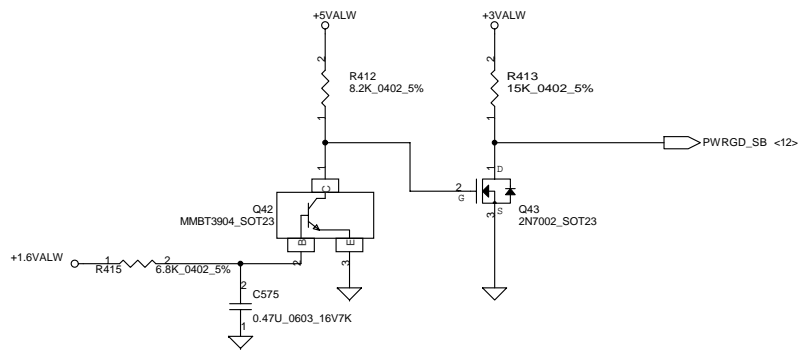


FOR WIRLESS LED ( PAV )



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Delay 100 ms

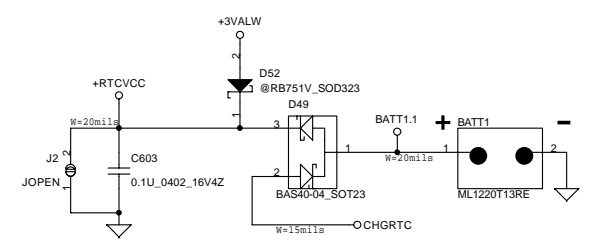
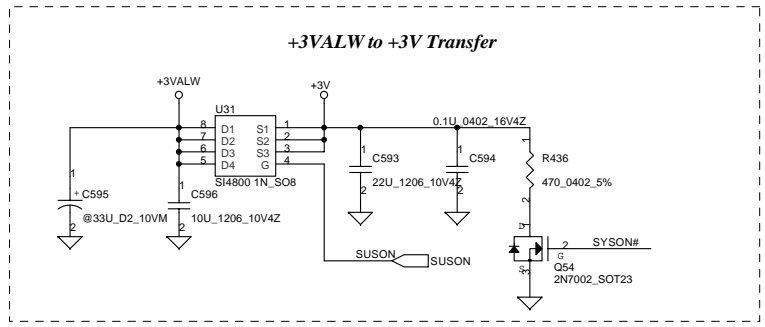
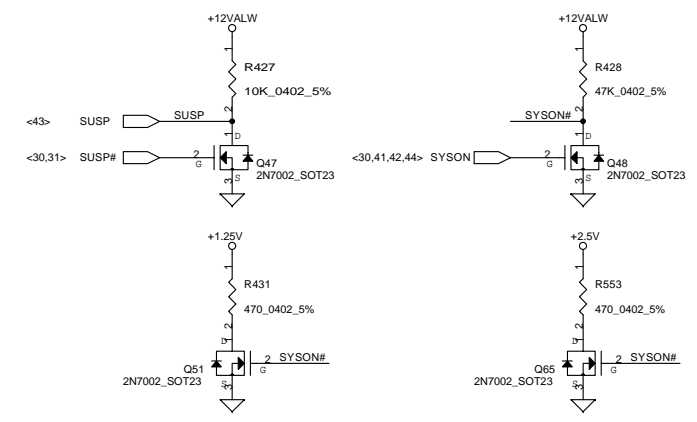
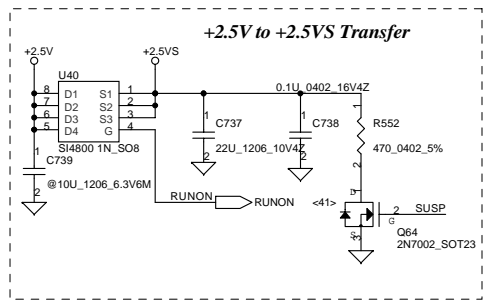
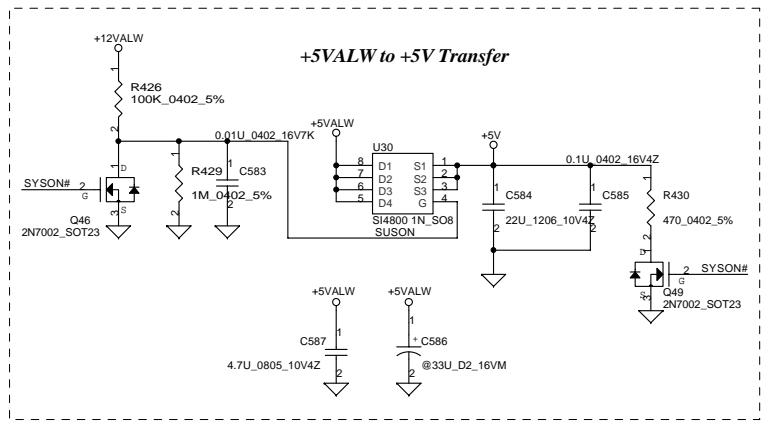
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DELAY 1 ms

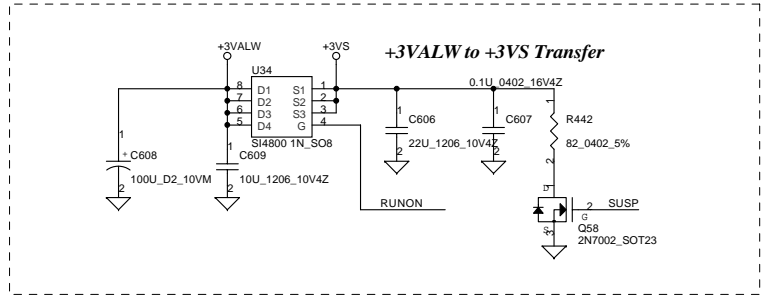
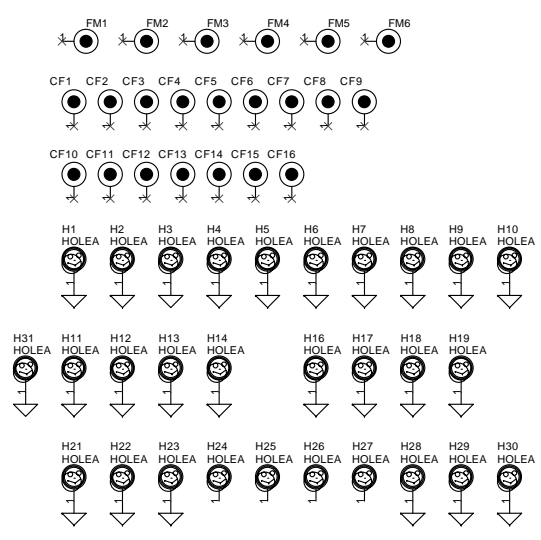
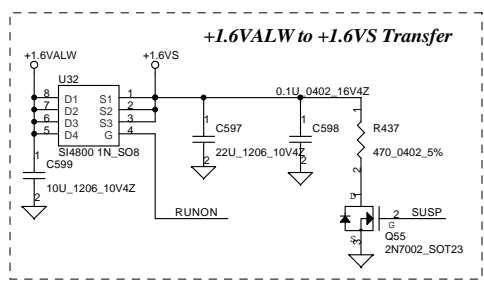
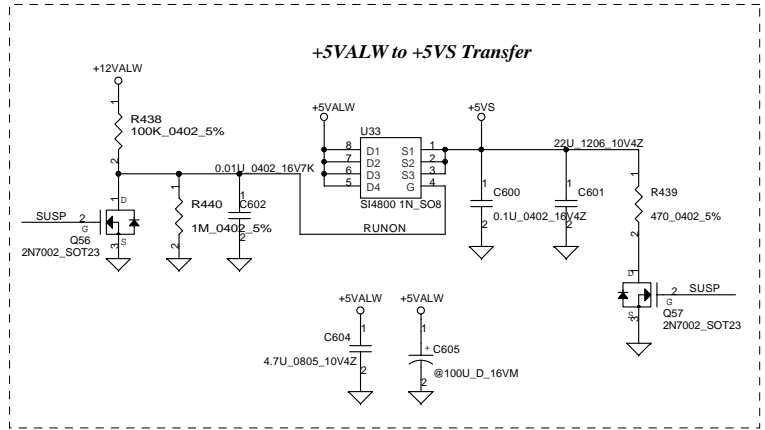
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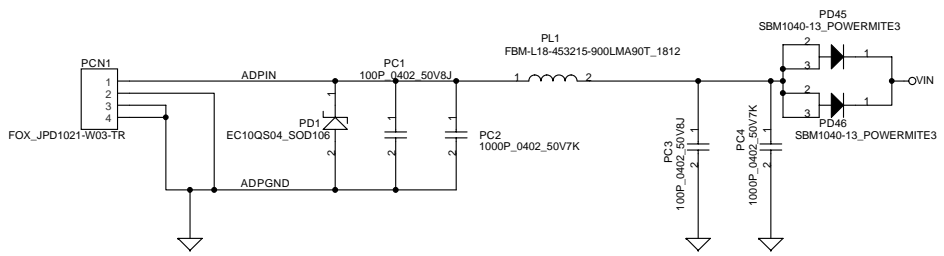


For customer request  
they don't wanna  
charge RTC

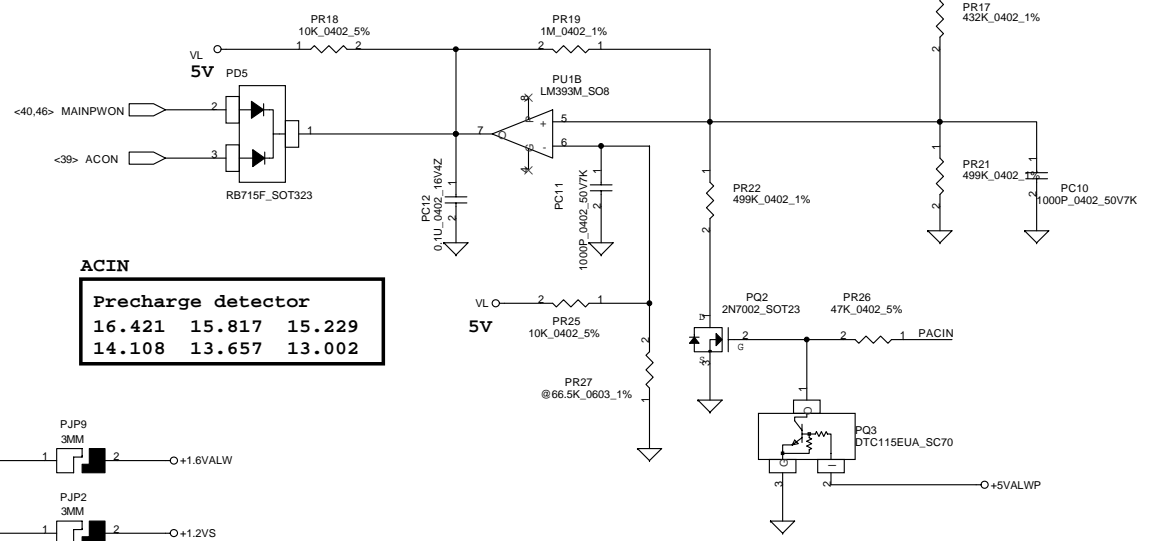
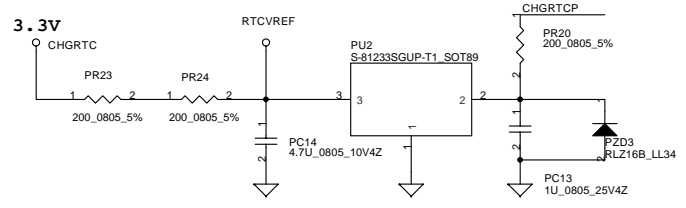
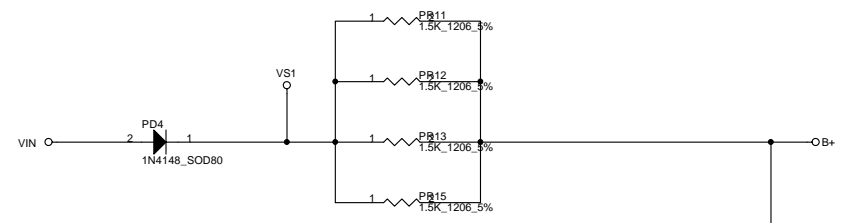
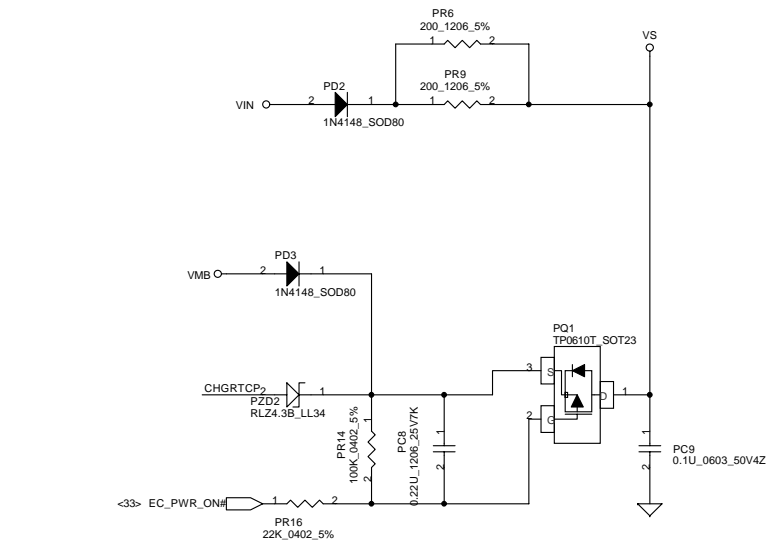
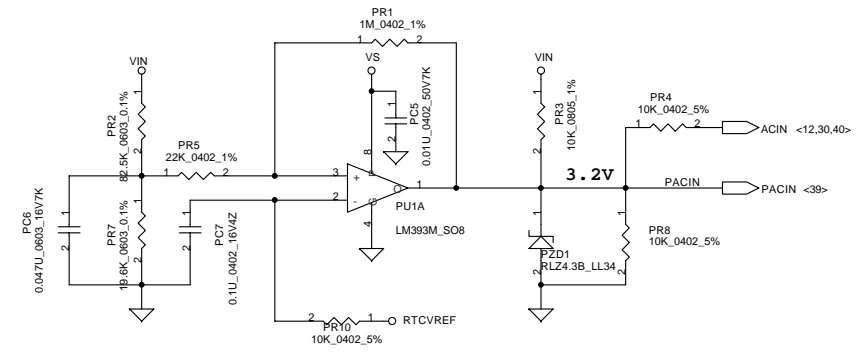


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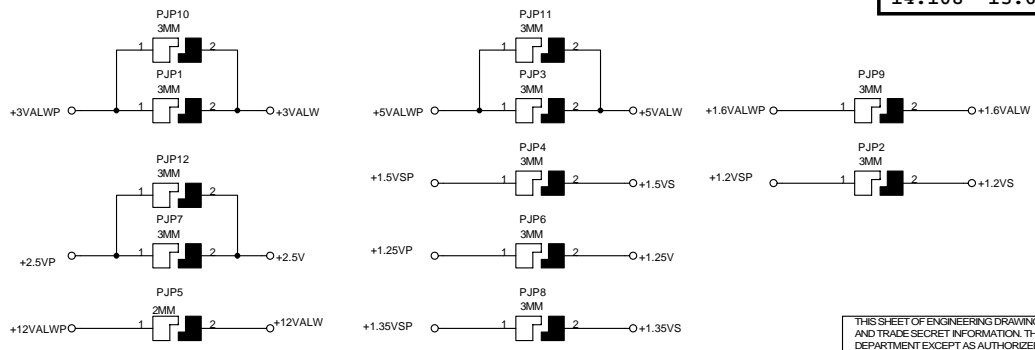
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**VIN detector**  
 17.945 17.343 16.757  
 17.372 16.782 16.207



**ACIN**  
 Precharge detector  
 16.421 15.817 15.229  
 14.108 13.657 13.002



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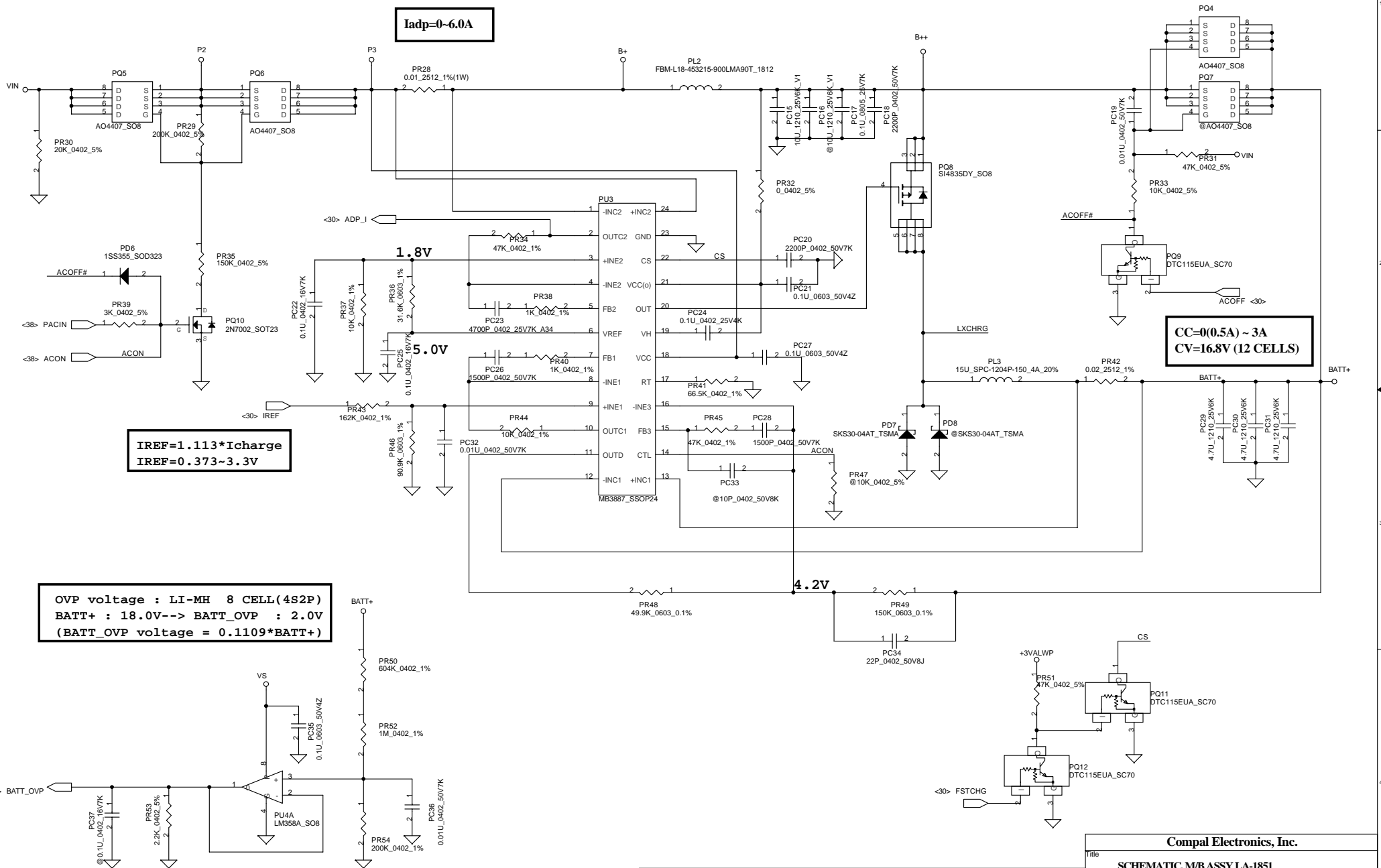
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**I<sub>adp</sub>=0-6.0A**

**CC=0(0.5A) ~ 3A  
CV=16.8V (12 CELLS)**

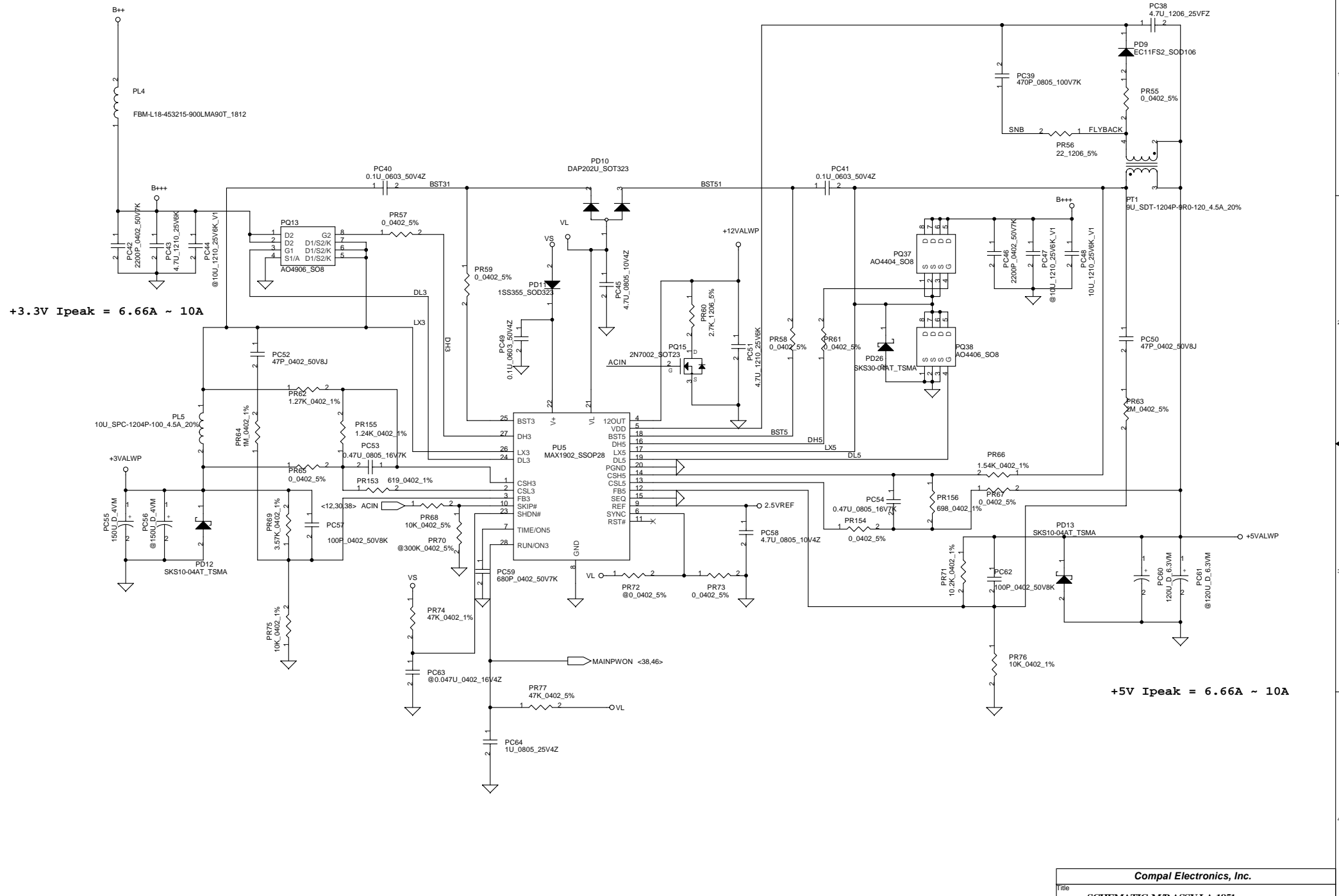
**I<sub>REF</sub>=1.113\*I<sub>charge</sub>  
I<sub>REF</sub>=0.373~3.3V**

**OVP voltage : LI-MH 8 CELL(4S2P)  
BATT+ : 18.0V--> BATT\_OVP : 2.0V  
(BATT\_OVP voltage = 0.1109\*BATT+)**



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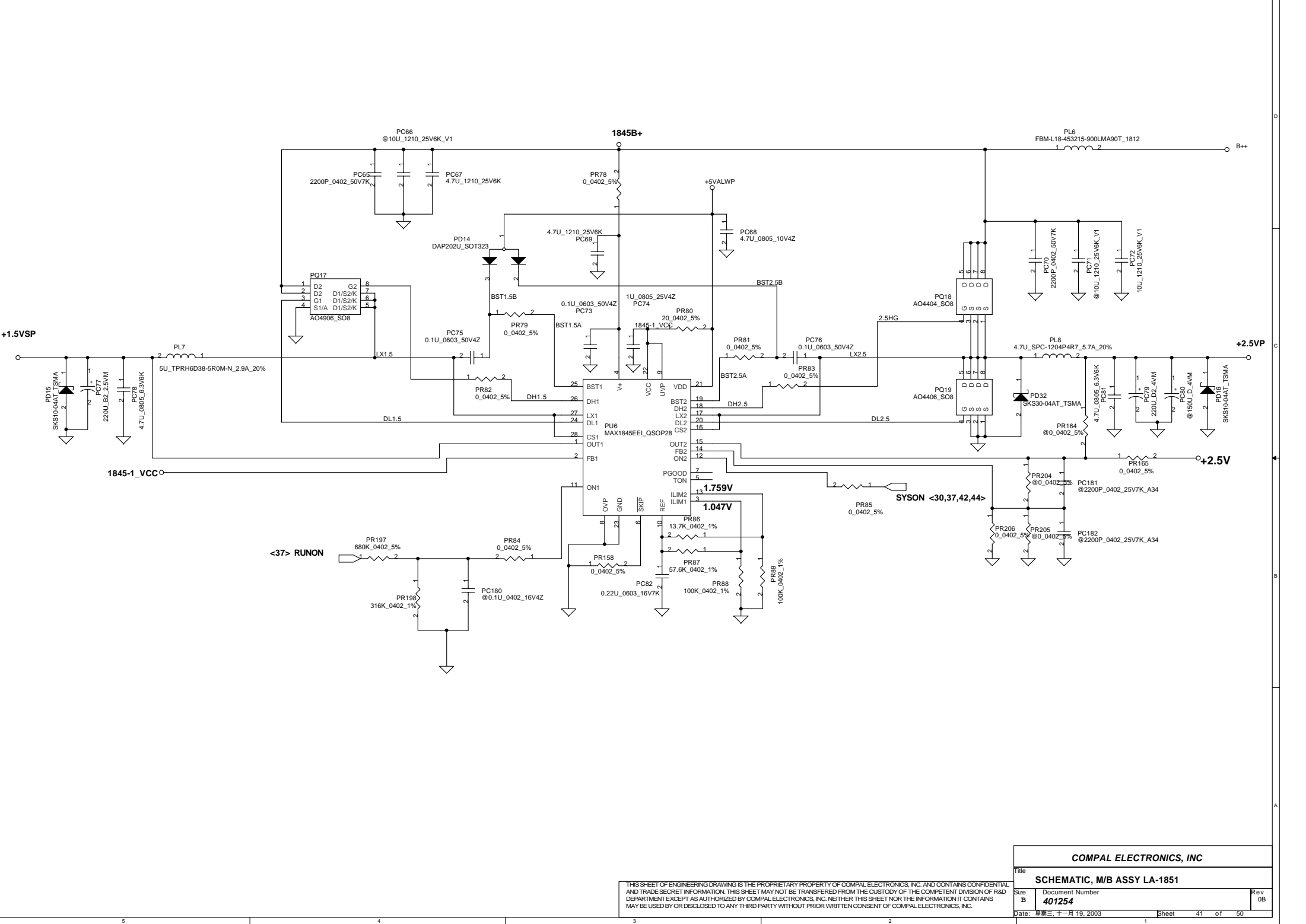
+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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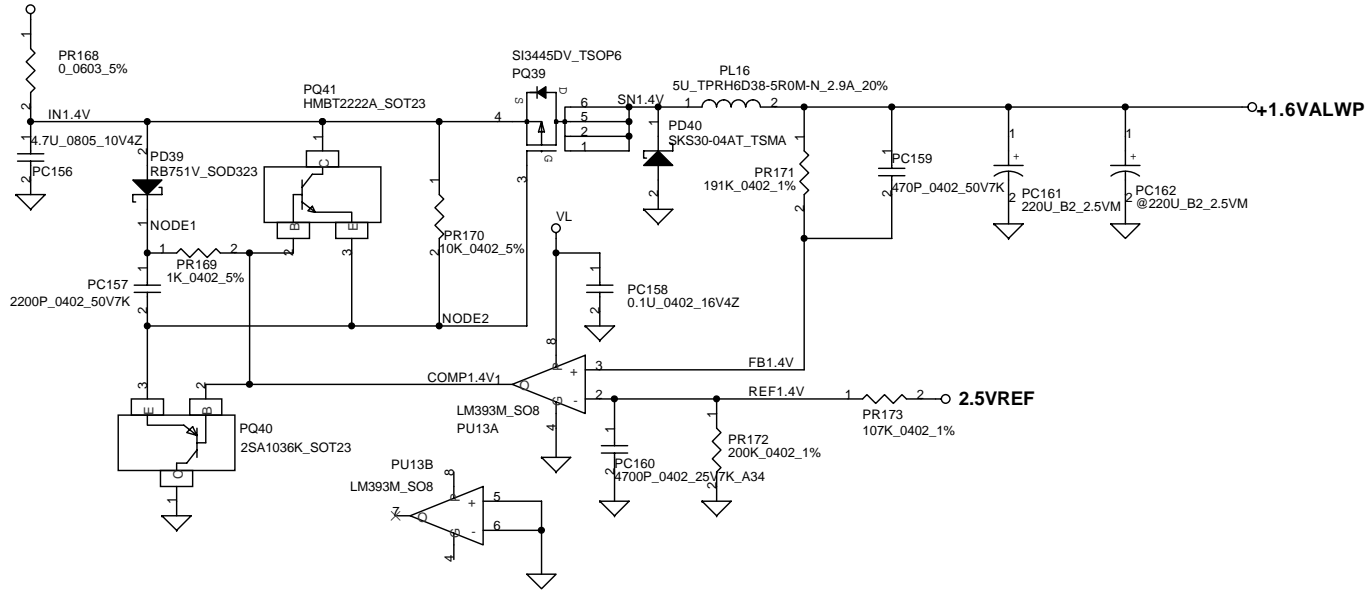




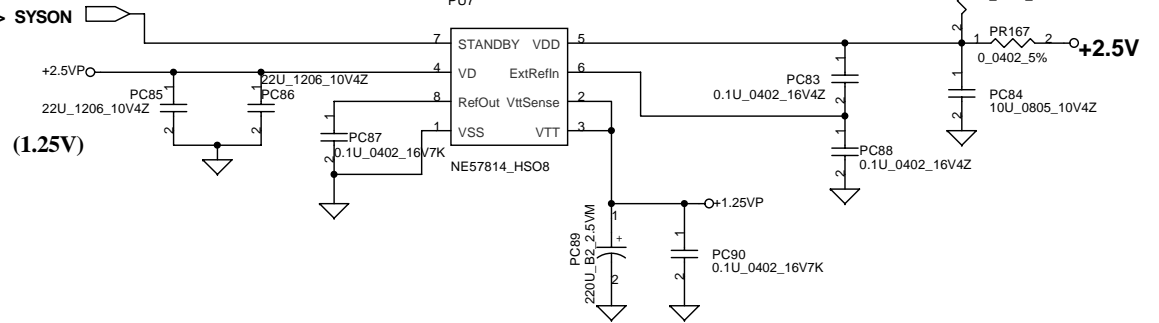
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+5VALWP



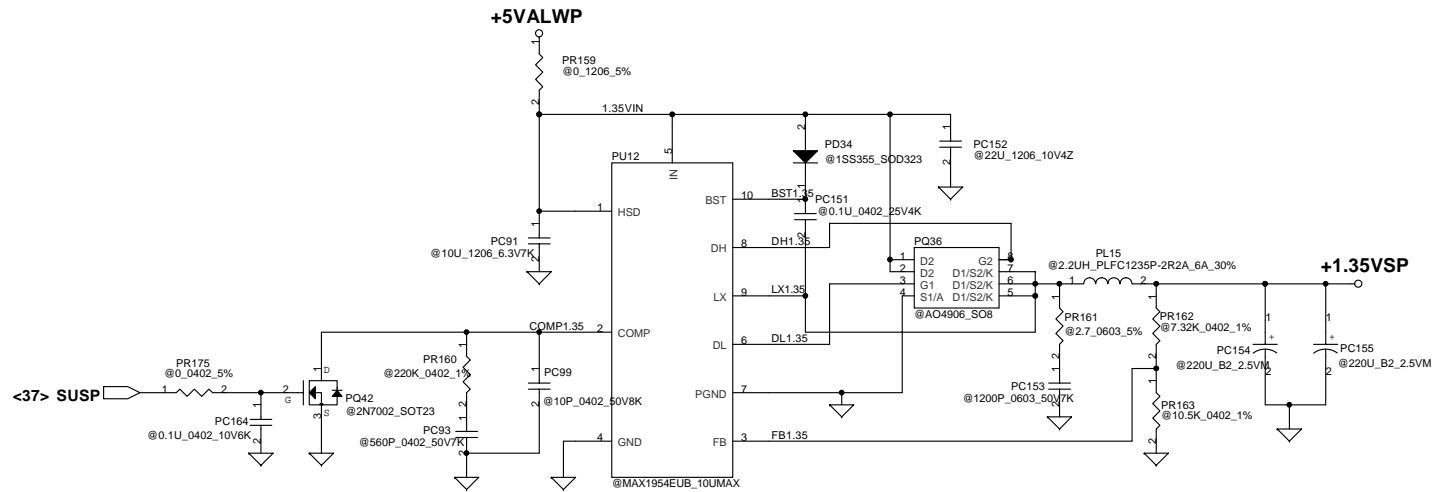
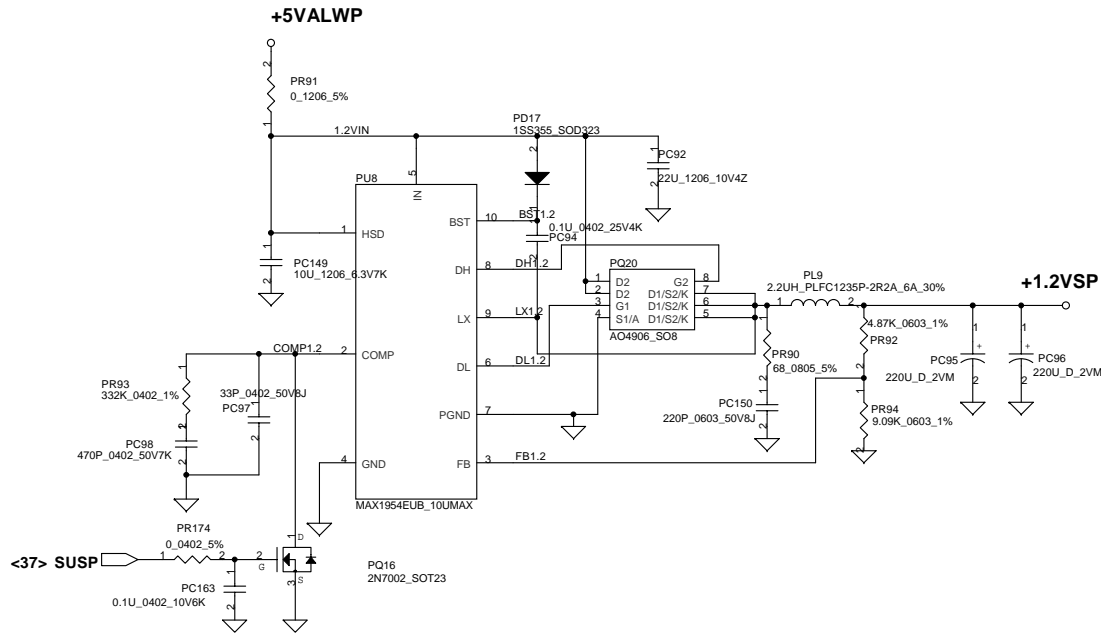
<30,37,41,44> SYSON



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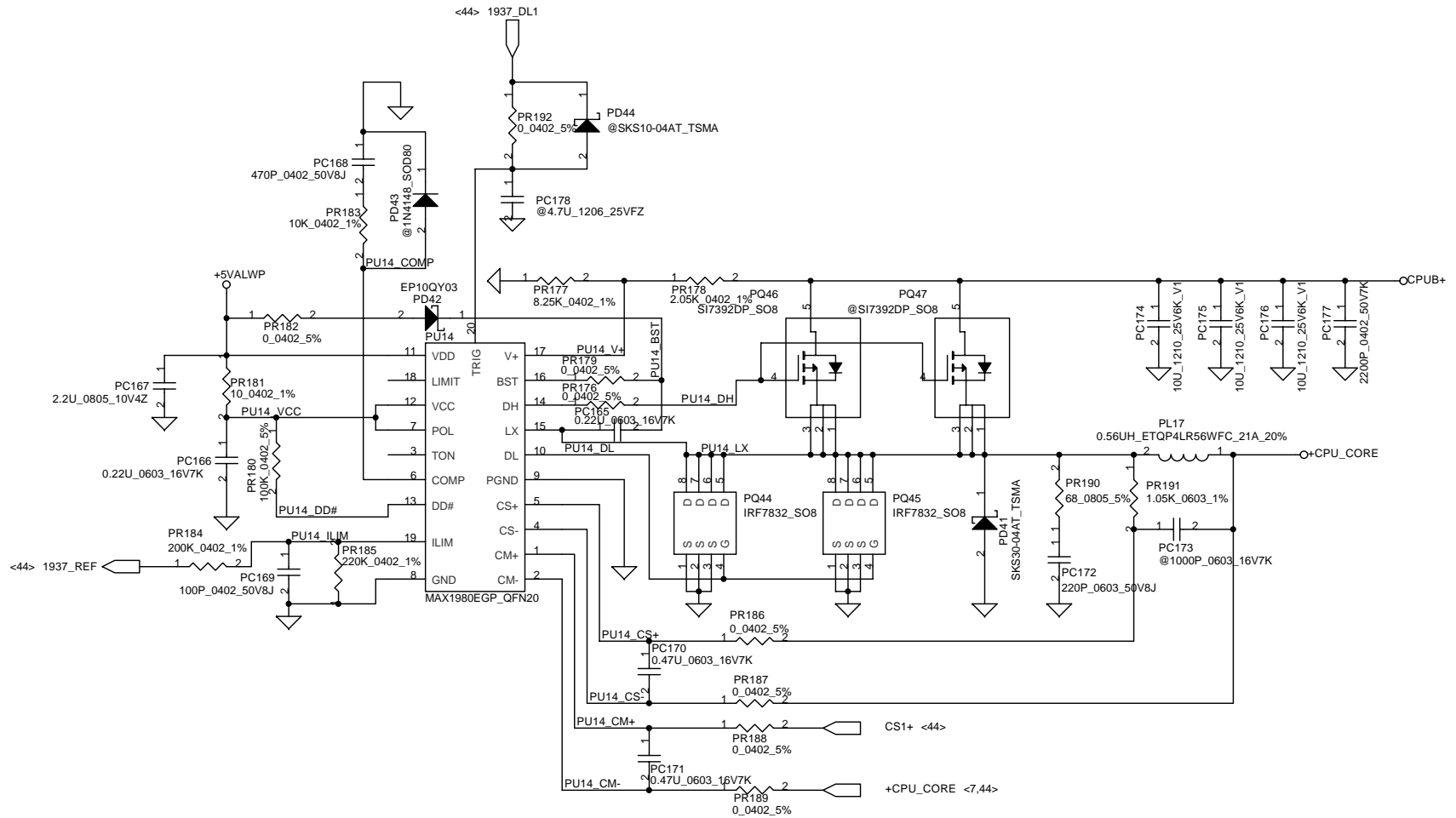
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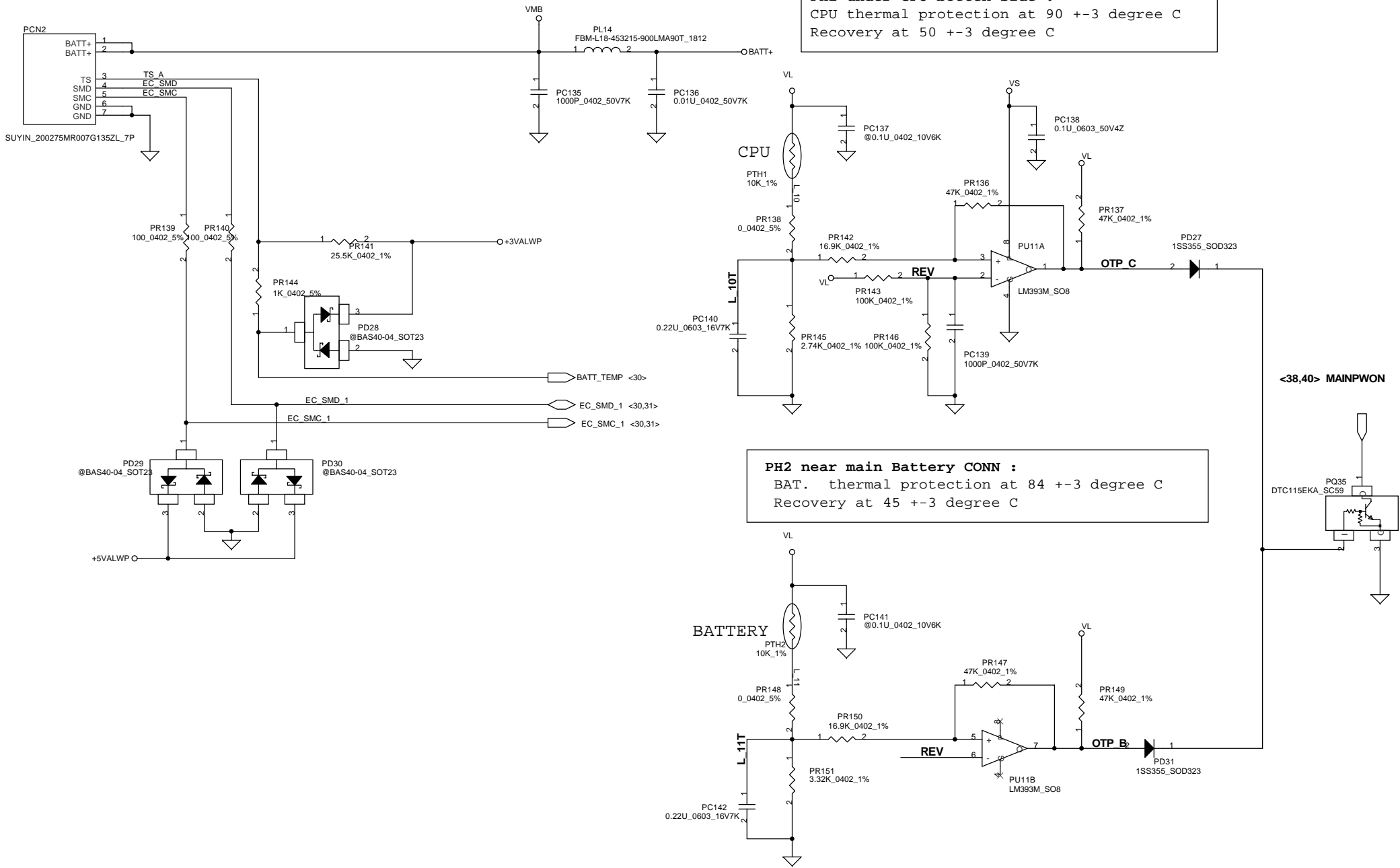
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**PH1 under CPU botten side :**  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 50 +/-3 degree C

**PH2 near main Battery CONN :**  
 BAT. thermal protection at 84 +/-3 degree C  
 Recovery at 45 +/-3 degree C

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# POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Fixed USB 1.1 rising/falling time error	P12	Delete C785, C786, C787, C788, C789, & C790	0.3
2		Fixed TV-out no display	P14	Swap TV_CRMA and TV_COMPS	0.3
3		Prevent PCI1620 latched up	P22	Reserve G_RST# to pin U37.C11	0.3
4		Design change (solve for HR60 audio issue)	P26	Move two load resistors from sub-board to M/B and swap JP17.2 and JP17.3	0.3
5		Supported wake up from TP	P27	Change TP connector JP26's power pin from +5VS to +5V	0.3
6		EMI required (solve for 48 MHz noise from FDD connector)	P32	Add CP11, CP12, CP13, and C801	0.3
7		Design change (TFDU6102 design guide)	P33	Delete C560 and C562 & add R586 Change C561 from 10uf to 4.7uf	0.3
8		EMI required (solve for 48 MHz noise from serial port)	P34	Add CP14, and CP15	0.3
9		ID required (for Pavillion)	P35	Add D58	0.3
10		EMI required	P25	Add L38, and L39	0.3
11		Add bypass cap. to solve for AC97 link cross a split plane	P27	Add C802, C803, C804, C805, and C806	0.3
12		Design change (reserve space for power placement and no need too many caps.)	P07	Delete C75, and C88	0.3
13		RealTech 8101L design guide	P20	Change R194 to 5.6K +/- 1%	0.3
14		Solve for SPDIF no output	P34	Delete C634	0.3
15		CPU_CLK is current drive from CK8. So, delete damping resistors.	P11	Change R69, and R70 from 15 ohm to 0 ohm	0.3
16		Solve for burst frequency error	P14	Change C642, and C643 from 18 pF to 22 pF	0.3
17		Solve for chrominance and burst level	P18	Change L11, L12, and L13 to 1.8uH	0.3

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI 1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 ~ 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI 1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop SI 9182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNC average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module ( 16 chips )	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		TI recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5

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