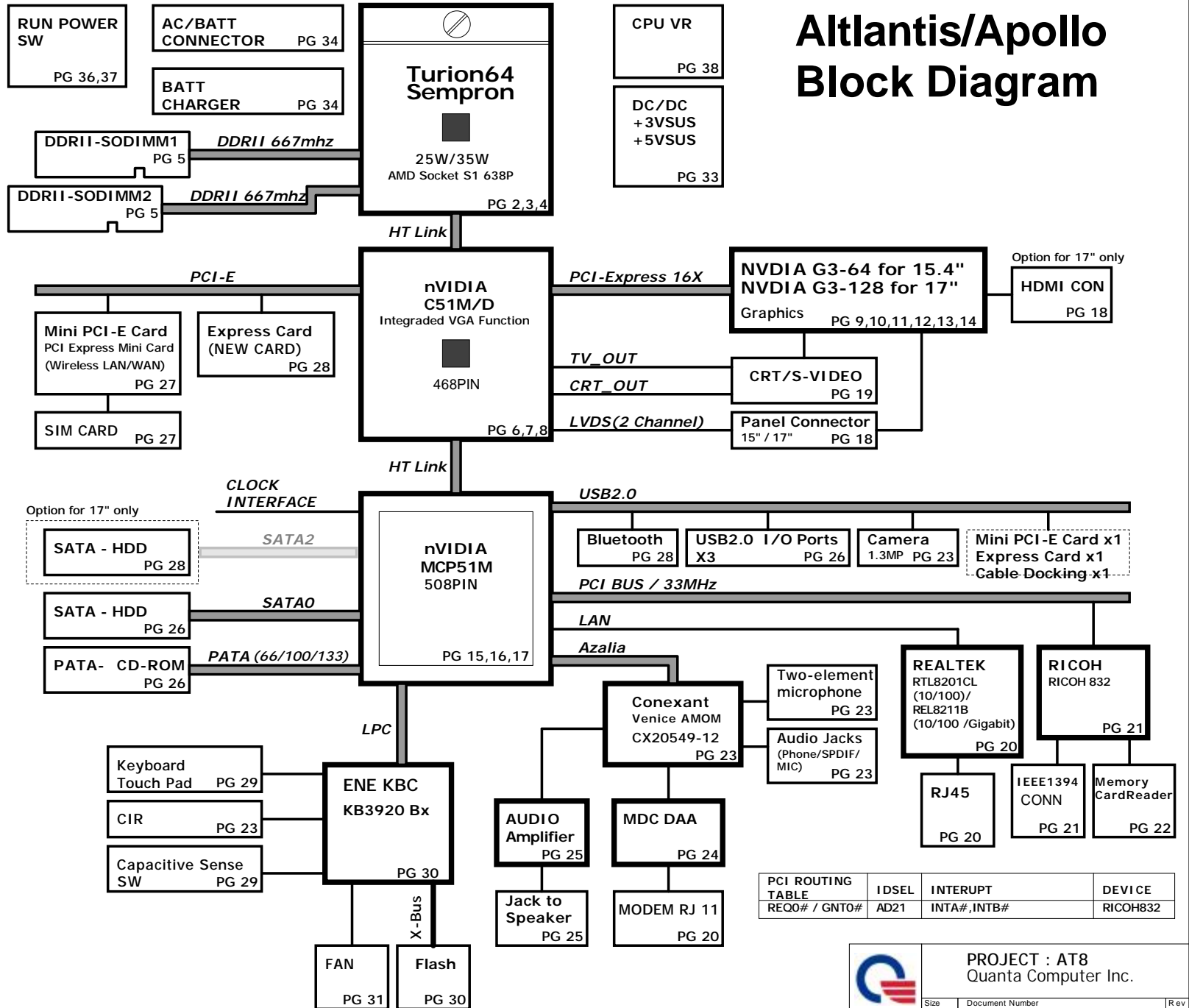


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- Cable Docking**
- TV_OUT
 - VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PG 31

Atlantis/Apollo Block Diagram



VAULE DEFINE
 A=0603,B=0805,C=1206,F=1%,
 OTHER IS 0402

EXAMPLE
 10R=10ohm(0402)
 10A=10ohm(0603)
 10B=10ohm(0805)
 10C=10ohm(1206)
 10/F=10ohm(0402 and 1%)

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

PROJECT : AT8
 Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Thursday, December 29, 2005 Sheet 1 of 38		

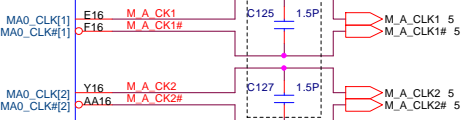
NB5/RD2/HW1

U26B

M_A D063 AA12	MA_DATA[63]	MA_DM[7]	Y13 M_A DOM7
M_A D064 AB12	MA_DATA[62]	MA_DM[6]	YB16 M_A DOM6
M_A D065 AB12	MA_DATA[61]	MA_DM[5]	Y19 M_A DOM5
M_A D066 AB14	MA_DATA[60]	MA_DM[4]	AC24 M_A DOM4
M_A D069 W11	MA_DATA[59]	MA_DM[3]	F24 M_A DOM3
M_A D068 Y12	MA_DATA[58]	MA_DM[2]	E19 M_A DOM2
M_A D057 AD13	MA_DATA[57]	MA_DM[1]	C15 M_A DOM1
M_A D056 AB13	MA_DATA[56]	MA_DM[0]	E12 M_A DOM0
M_A D055 AD15	MA_DATA[55]		
M_A D054 AB15	MA_DATA[54]		
M_A D053 AB12	MA_DATA[53]		
M_A D051 Y14	MA_DATA[52]		
M_A D050 W14	MA_DATA[51]		
M_A D049 Y16	MA_DATA[50]		
M_A D048 AD16	MA_DATA[49]		
M_A D047 Y18	MA_DATA[48]		
M_A D046 AD19	MA_DATA[47]		
M_A D045 AD21	MA_DATA[46]		
M_A D044 AB21	MA_DATA[45]		
M_A D043 AB18	MA_DATA[44]		
M_A D042 AA18	MA_DATA[43]		
M_A D041 AA20	MA_DATA[42]		
M_A D040 Y20	MA_DATA[41]		
M_A D039 AA22	MA_DATA[40]		
M_A D038 Y22	MA_DATA[39]		
M_A D037 W21	MA_DATA[38]		
M_A D036 Y22	MA_DATA[37]		
M_A D035 AA22	MA_DATA[36]		
M_A D034 AB22	MA_DATA[35]		
M_A D033 AB24	MA_DATA[34]		
M_A D032 Y24	MA_DATA[33]		
M_A D031 H24	MA_DATA[32]		
M_A D030 H20	MA_DATA[31]		
M_A D029 E22	MA_DATA[29]		
M_A D028 E21	MA_DATA[28]		
M_A D027 H19	MA_DATA[27]		
M_A D026 H24	MA_DATA[26]		
M_A D025 F22	MA_DATA[25]		
M_A D024 F20	MA_DATA[24]		
M_A D023 C23	MA_DATA[23]		
M_A D022 B22	MA_DATA[22]		
M_A D021 F18	MA_DATA[21]		
M_A D020 E18	MA_DATA[20]		
M_A D019 E20	MA_DATA[19]		
M_A D018 D22	MA_DATA[18]		
M_A D017 C19	MA_DATA[17]		
M_A D016 G18	MA_DATA[16]		
M_A D015 G17	MA_DATA[15]		
M_A D014 C17	MA_DATA[14]		
M_A D013 E14	MA_DATA[13]		
M_A D012 E14	MA_DATA[12]		
M_A D011 H17	MA_DATA[11]		
M_A D09 E16	MA_DATA[10]		
M_A D08 H16	MA_DATA[9]		
M_A D07 E13	MA_DATA[7]		
M_A D06 C13	MA_DATA[6]		
M_A D05 C13	MA_DATA[5]		
M_A D04 H11	MA_DATA[4]		
M_A D03 G14	MA_DATA[3]		
M_A D02 H14	MA_DATA[2]		
M_A D01 F12	MA_DATA[1]		
M_A D00 G12	MA_DATA[0]		

AMD S1 SOCKET

W12 M_A DOS7	MA_DQS[7]
Y15 M_A DOS6	MA_DQS[6]
AB19 M_A DOS5	MA_DQS[5]
AD23 M_A DOS4	MA_DQS[4]
G22 M_A DOS3	MA_DQS[3]
C22 M_A DOS2	MA_DQS[2]
G16 M_A DOS1	MA_DQS[1]
G13 M_A DOS0	MA_DQS[0]
W13 M_A DOS#7	MA_DQS#7
W15 M_A DOS#6	MA_DQS#6
AB20 M_A DOS#5	MA_DQS#5
AC23 M_A DOS#4	MA_DQS#4
G21 M_A DOS#3	MA_DQS#3
C21 M_A DOS#2	MA_DQS#2
G15 M_A DOS#1	MA_DQS#1
H13 M_A DOS#0	MA_DQS#0



TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

K22 M_A BA2	MA_BANK[2]
R20 M_A BA1	MA_BANK[1]
T22 M_A BA0	MA_BANK[0]
T20 M_A RAS#	MA_RAS#
U20 M_A CAS#	MA_CAS#
U21 M_A WE#	MA_WE#

V19 M_A CS#3	MAO_CS#3
J22 M_A CS#2	MAO_CS#2
V22 M_A CS#1	MAO_CS#1
T19 M_A CS#0	MAO_CS#0

J20 M_A CKE1	MAO_CKE[1]
J21 M_A CKE0	MAO_CKE[0]

V20 M_A ODT1	MAO_ODT[1]
U19 M_A ODT0	MAO_ODT[0]

5 M_A_DQ[63..0] M_A_DQ[63..0]
 4.5 M_A_A[15..0] M_A_A[15..0]

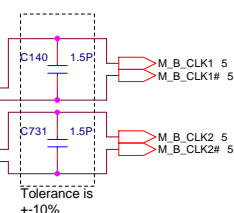
M_A_DOM[7..0] M_A_DOM[7..0] 5
 M_A_DQS[7..0] M_A_DQS[7..0] 5
 M_A_DQS#[7..0] M_A_DQS#[7..0] 5
 M_A_BA[2..0] M_A_BA[2..0] 4.5
 M_A_CS#[3..0] M_A_CS#[3..0] 4.5
 M_A_RAS# M_A_RAS# 4.5
 M_A_CAS# M_A_CAS# 4.5
 M_A_WE# M_A_WE# 4.5
 M_A_CKE1 M_A_CKE1 4.5
 M_A_CKE0 M_A_CKE0 4.5
 M_A_ODT1 M_A_ODT1 4.5
 M_A_ODT0 M_A_ODT0 4.5

U26C

M_B D063 AD11	MB_DATA[63]	MB_DM[7]	AD12 M_B DOM7
M_B D062 AF11	MB_DATA[62]	MB_DM[6]	AC16 M_B DOM6
M_B D061 AE14	MB_DATA[61]	MB_DM[5]	AE22 M_B DOM5
M_B D060 AE14	MB_DATA[60]	MB_DM[4]	AB26 M_B DOM4
M_B D059 Y11	MB_DATA[59]	MB_DM[3]	E25 M_B DOM3
M_B D058 AB11	MB_DATA[58]	MB_DM[2]	A22 M_B DOM2
M_B D057 A12	MB_DATA[57]	MB_DM[1]	E16 M_B DOM1
M_B D056 AF13	MB_DATA[56]	MB_DM[0]	A12 M_B DOM0
M_B D055 AF15	MB_DATA[55]		
M_B D054 AF16	MB_DATA[54]		
M_B D053 AF18	MB_DATA[53]		
M_B D052 AF19	MB_DATA[52]		
M_B D051 AD14	MB_DATA[51]		
M_B D050 AC14	MB_DATA[50]		
M_B D049 AE18	MB_DATA[49]		
M_B D048 AD18	MB_DATA[48]		
M_B D047 AD20	MB_DATA[47]		
M_B D046 AC20	MB_DATA[46]		
M_B D045 AF23	MB_DATA[45]		
M_B D044 AF24	MB_DATA[44]		
M_B D043 AF20	MB_DATA[43]		
M_B D042 AE20	MB_DATA[42]		
M_B D041 AD22	MB_DATA[41]		
M_B D040 AC22	MB_DATA[40]		
M_B D039 AE25	MB_DATA[39]		
M_B D038 AD26	MB_DATA[38]		
M_B D037 AA25	MB_DATA[37]		
M_B D036 AA26	MB_DATA[36]		
M_B D035 AE24	MB_DATA[35]		
M_B D034 AD24	MB_DATA[34]		
M_B D033 AA23	MB_DATA[33]		
M_B D032 AA24	MB_DATA[32]		
M_B D031 G24	MB_DATA[31]		
M_B D030 G23	MB_DATA[30]		
M_B D029 D26	MB_DATA[29]		
M_B D028 C26	MB_DATA[28]		
M_B D027 C22	MB_DATA[27]		
M_B D026 G25	MB_DATA[26]		
M_B D025 E24	MB_DATA[25]		
M_B D024 E23	MB_DATA[24]		
M_B D023 C24	MB_DATA[23]		
M_B D022 B24	MB_DATA[22]		
M_B D021 C20	MB_DATA[21]		
M_B D020 B20	MB_DATA[20]		
M_B D019 C25	MB_DATA[19]		
M_B D018 D24	MB_DATA[18]		
M_B D017 A21	MB_DATA[17]		
M_B D016 D20	MB_DATA[16]		
M_B D015 D18	MB_DATA[15]		
M_B D014 C18	MB_DATA[14]		
M_B D013 D14	MB_DATA[13]		
M_B D012 C14	MB_DATA[12]		
M_B D011 A20	MB_DATA[11]		
M_B D010 A19	MB_DATA[10]		
M_B D09 A16	MB_DATA[9]		
M_B D08 A15	MB_DATA[8]		
M_B D07 A13	MB_DATA[7]		
M_B D06 D12	MB_DATA[6]		
M_B D05 E11	MB_DATA[5]		
M_B D04 G11	MB_DATA[4]		
M_B D03 B14	MB_DATA[3]		
M_B D02 A14	MB_DATA[2]		
M_B D01 A11	MB_DATA[1]		
M_B D00 C11	MB_DATA[0]		

5 M_B_DQ[63..0] M_B_DQ[63..0]
 4.5 M_B_A[15..0] M_B_A[15..0]

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS



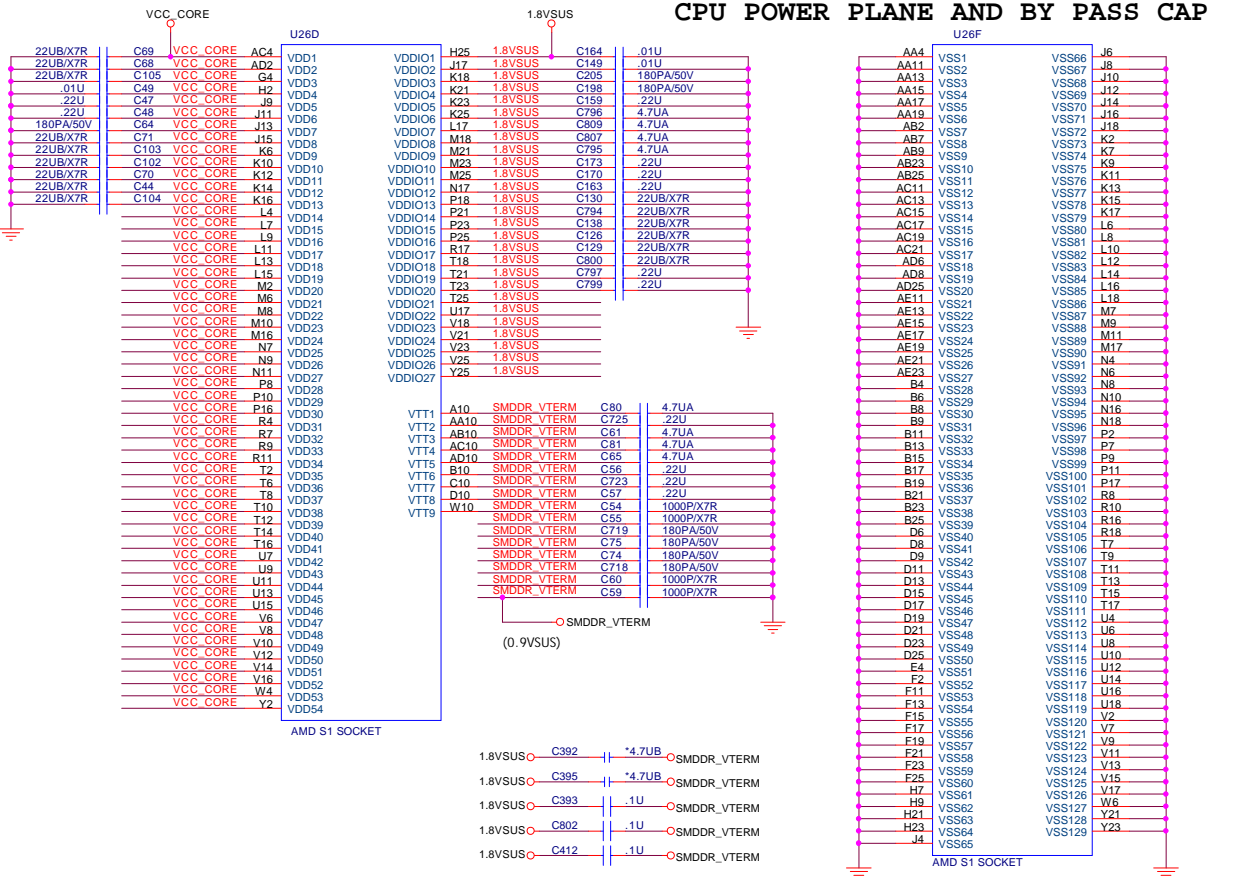
C51MVREF : W = 20MIL AND SPACE = 20MIL

M_B_DOM[7..0] M_B_DOM[7..0] 5
 M_B_DQS[7..0] M_B_DQS[7..0] 5
 M_B_BA[2..0] M_B_BA[2..0] 4.5
 M_B_CS#[3..0] M_B_CS#[3..0] 4.5
 M_B_RAS# M_B_RAS# 4.5
 M_B_CAS# M_B_CAS# 4.5
 M_B_WE# M_B_WE# 4.5
 M_B_CKE1 M_B_CKE1 4.5
 M_B_CKE0 M_B_CKE0 4.5
 M_B_ODT1 M_B_ODT1 4.5
 M_B_ODT0 M_B_ODT0 4.5

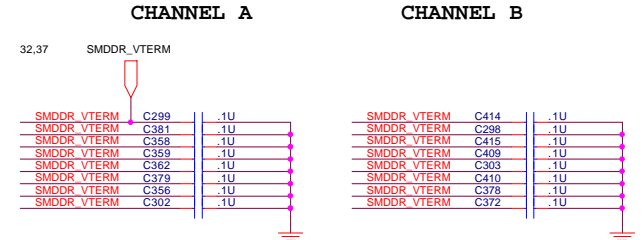
PROJECT : AT8
 Quanta Computer Inc.

Size Custom	Document Number CPU(MEM)/F	Rev 1A
Date: Thursday, December 29, 2005	Sheet 3 of 38	

CPU POWER PLANE AND BY PASS CAP



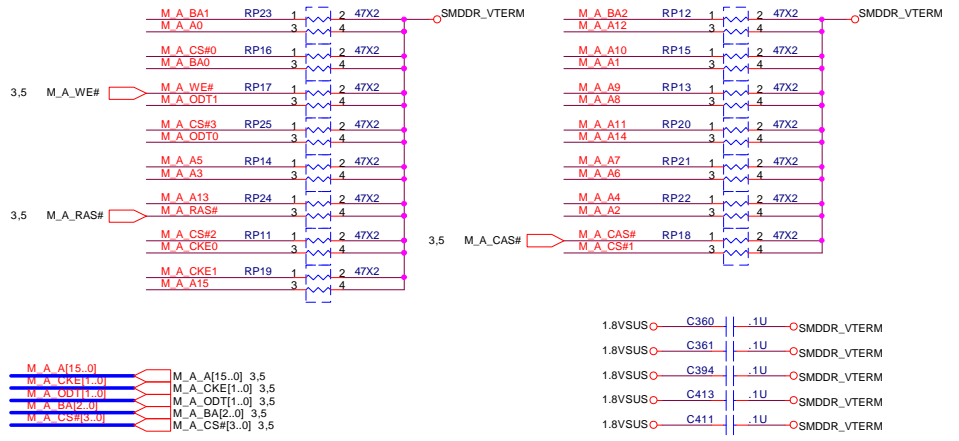
DDR2 TERMINATION BYPASS CAP



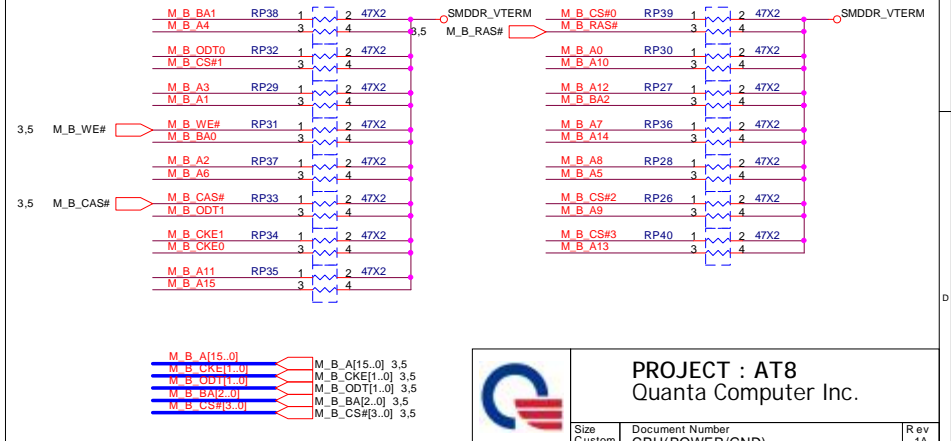
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



DDR1 CHANNEL A TERMINATION

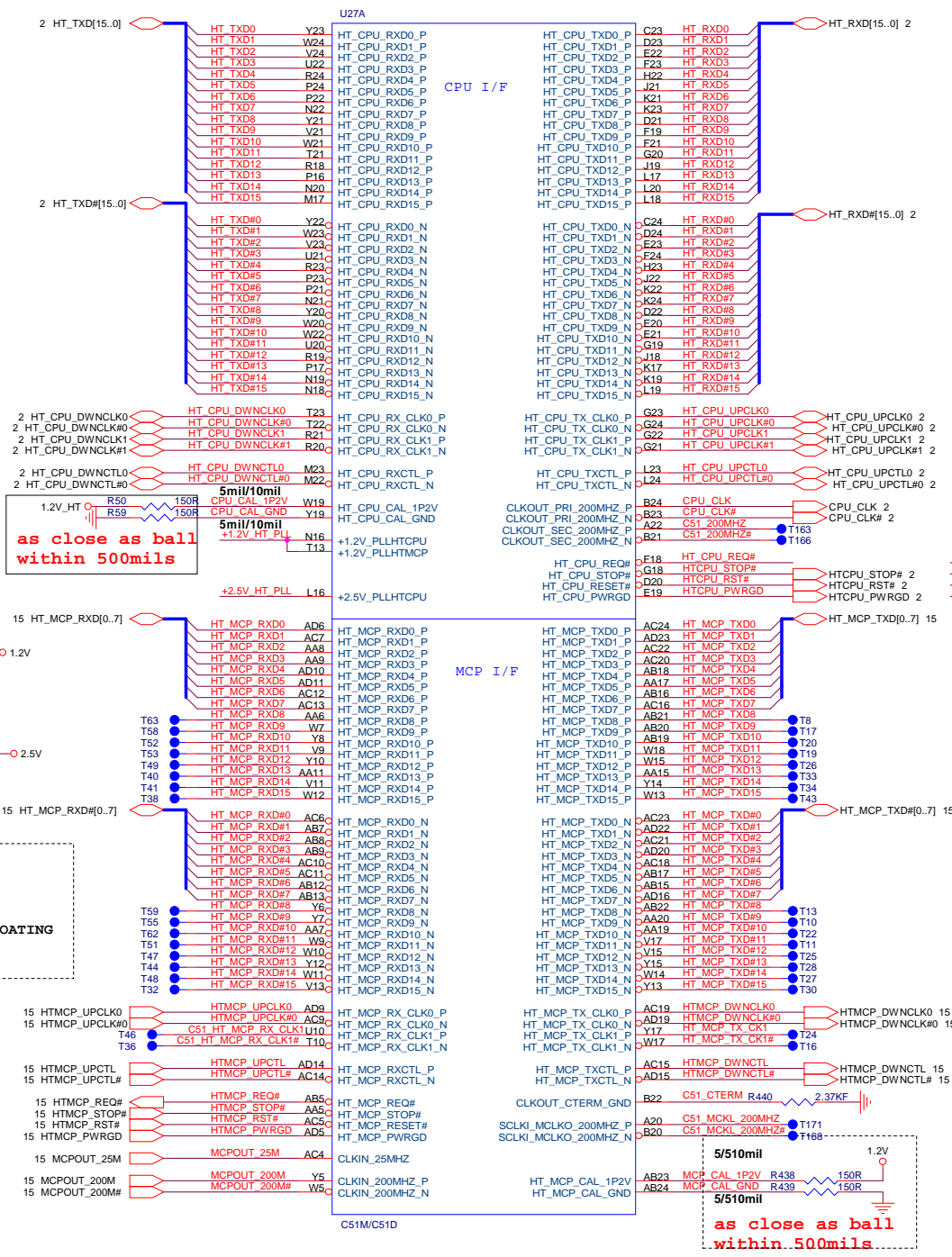


DDR1 CHANNEL B TERMINATION



PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number CPU(POWER/GND)	Rev 1A
Date: Thursday, December 29, 2005	Sheet 4 of 38	



as close as ball within 500mils

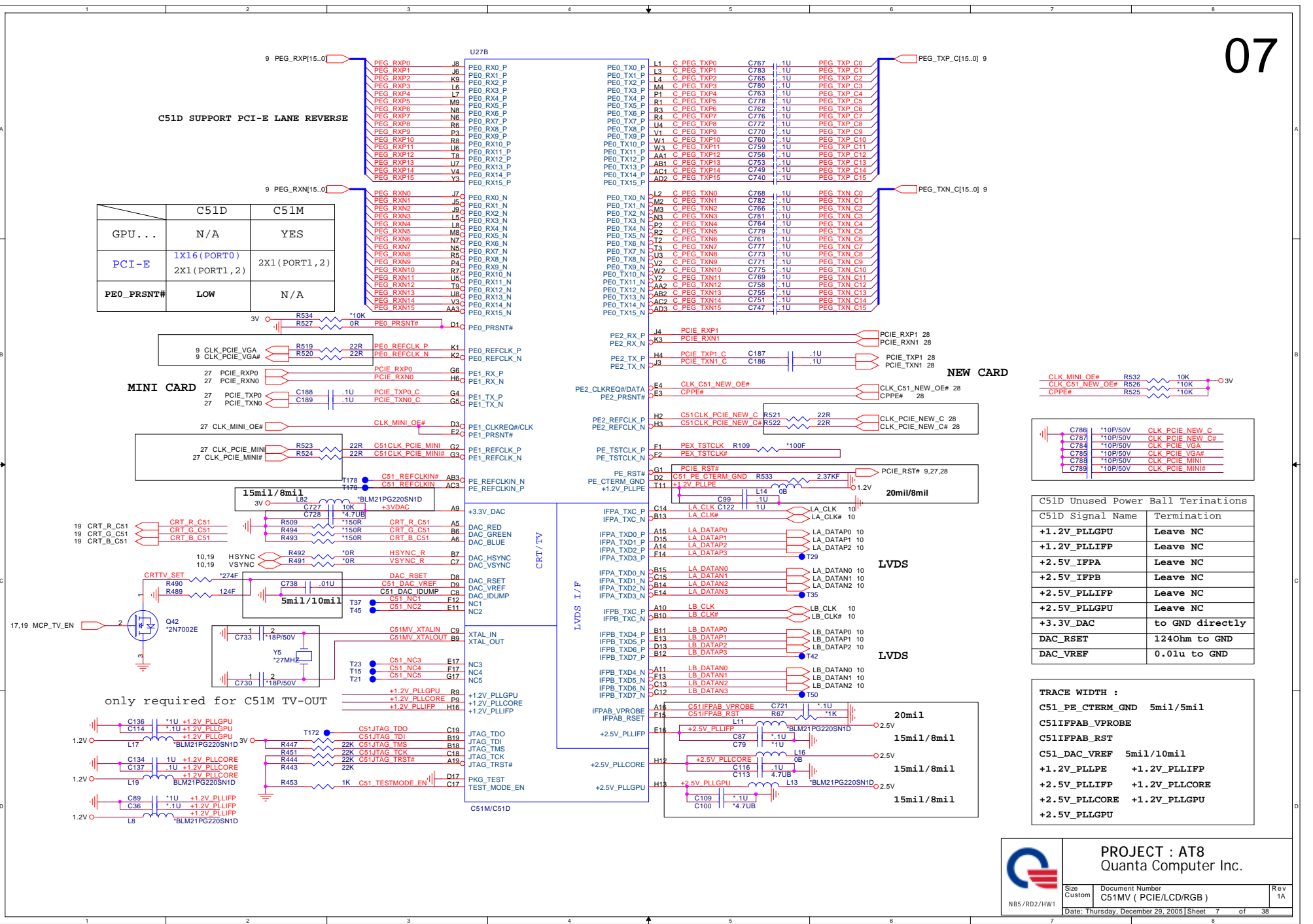
#note from nv design guide
Pull-Hi for rise time
-0.25v

STUFF : 4X4 HT LINK/UNUSED PIN FLOATING
NON-STUFF : 8X8 HT LINK(DEFAULT)

as close as ball within 500mils



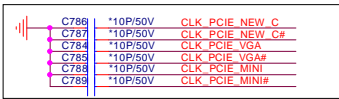
PROJECT : AT8 Quanta Computer Inc.		
Size Custom	Document Number C51MV (HT LINK)	Rev 1A
Date: Thursday, December 29, 2005 Sheet 6 of 38		



	C51D	C51M
GPU...	N/A	YES
PCI-E	1X16 (PORT0) 2X1 (PORT1, 2)	2X1 (PORT1, 2)
PEO_PRSN#	LOW	N/A

MINI CARD

NEW CARD



C51D Unused Power	Ball Terminations
C51D Signal Name	Termination
+1.2V_PLLGPU	Leave NC
+1.2V_PLLIFP	Leave NC
+2.5V_IFPA	Leave NC
+2.5V_IFPB	Leave NC
+2.5V_PLLIFP	Leave NC
+2.5V_PLLGPU	Leave NC
+3.3V_DAC	to GND directly
DAC_RST	1240hm to GND
DAC_VREF	0.01u to GND

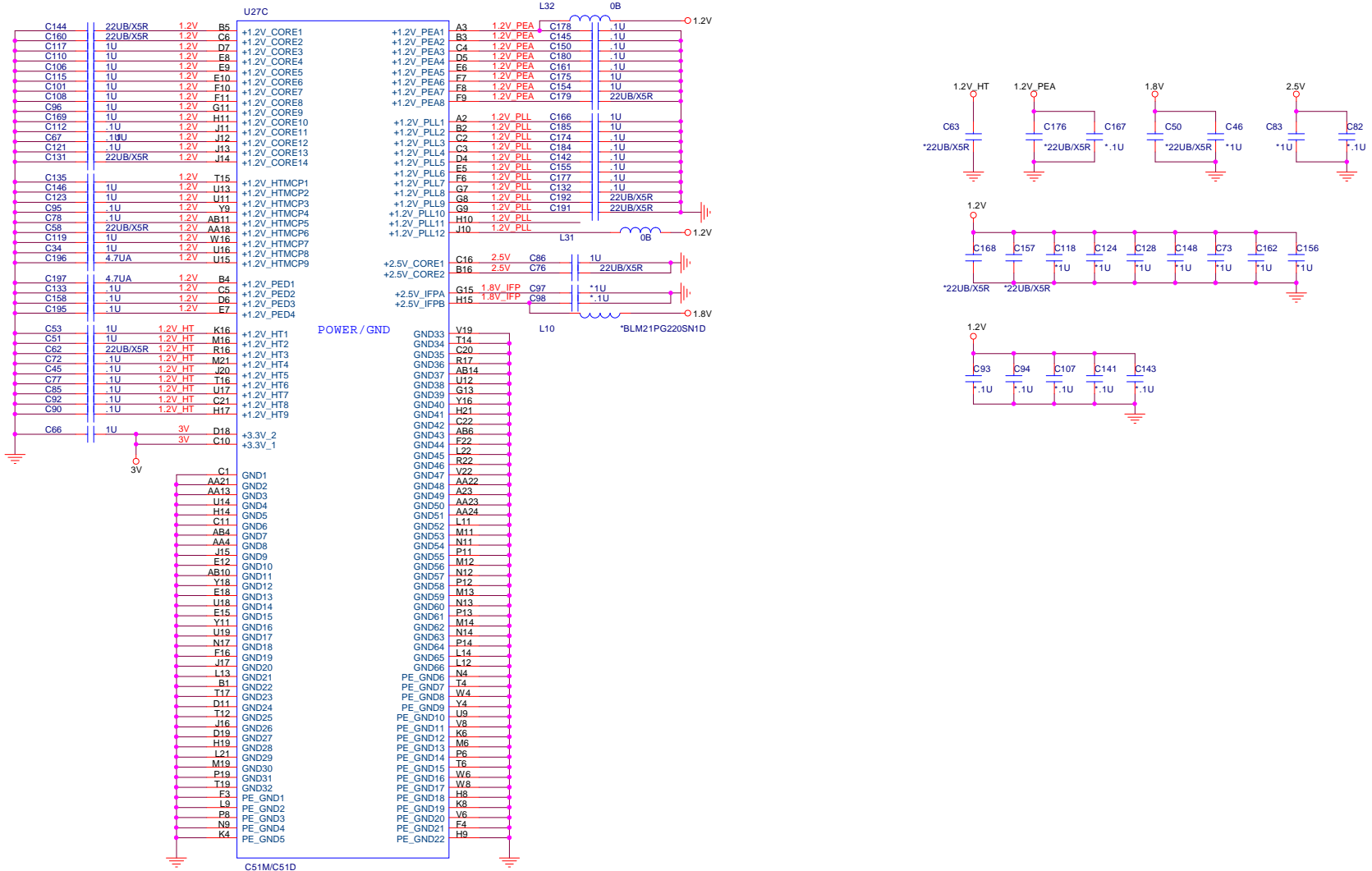
TRACE WIDTH :


C51_PE_TERM_GND	5mil/5mil
C51IFPAB_VPROBE	
C51IFPAB_RST	
C51_DAC_VREF	5mil/10mil
+1.2V_PLLPE	+1.2V_PLLIFP
+2.5V_PLLIFP	+1.2V_PLLCORE
+2.5V_PLLGPU	+1.2V_PLLGPU
+2.5V_PLLCORE	+1.2V_PLLGPU

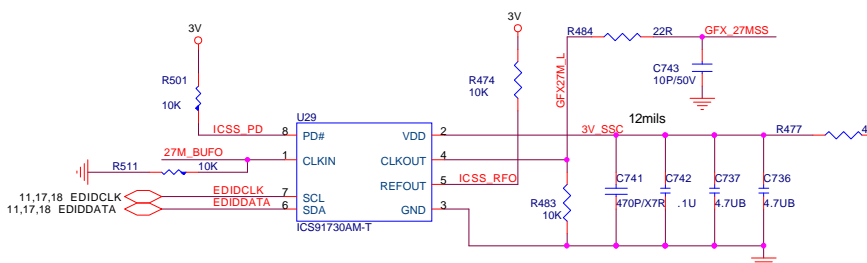
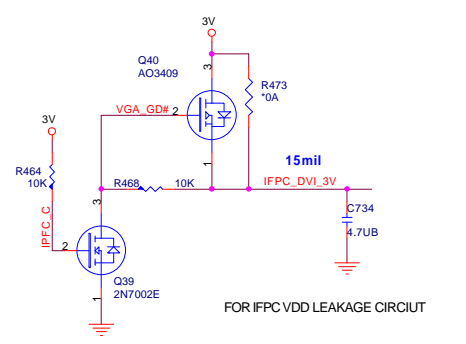
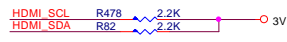
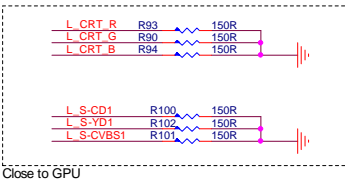
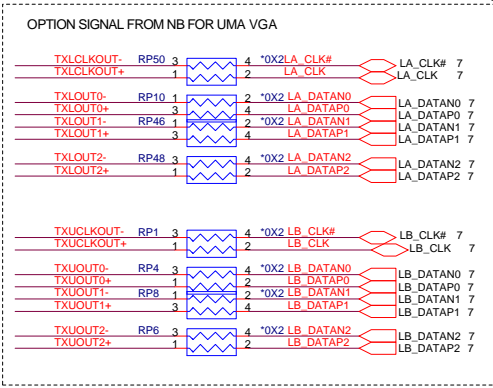
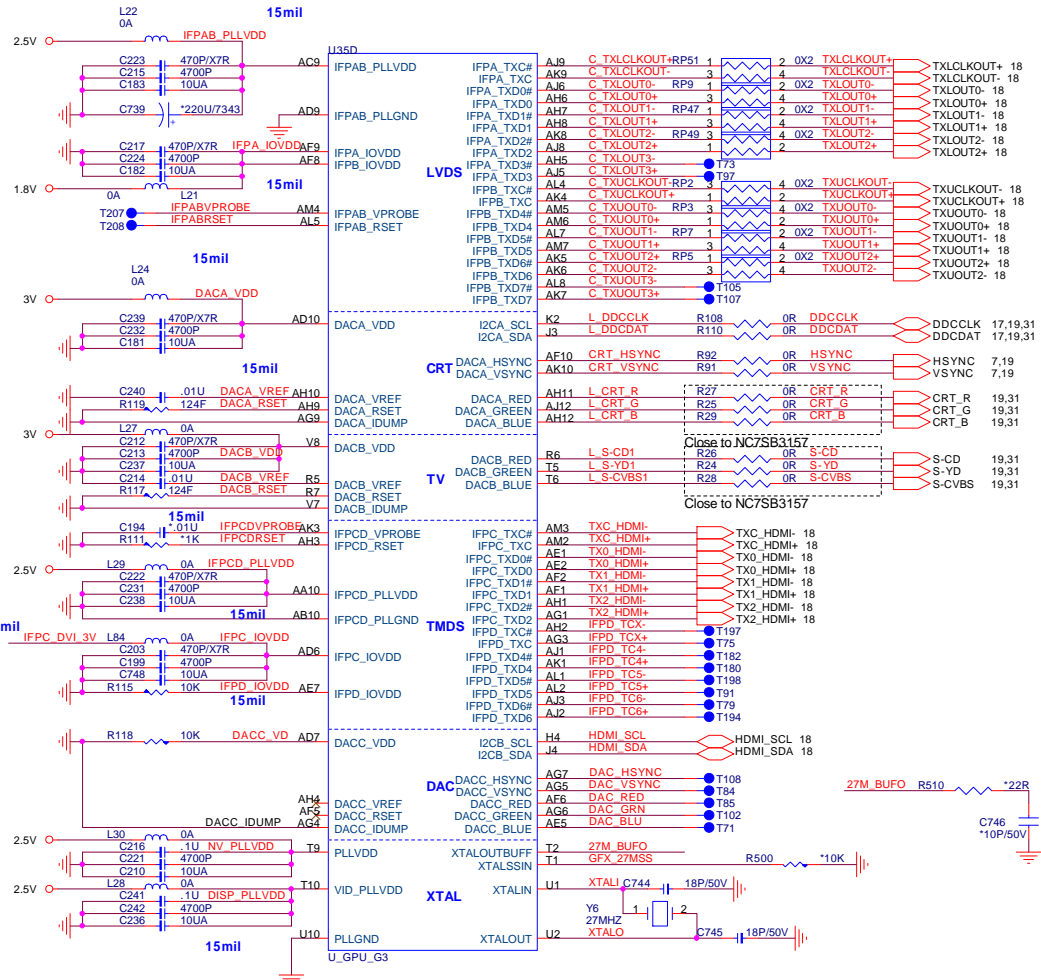
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number C51MV (PCIE/LCD/RGB)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 7 of 38

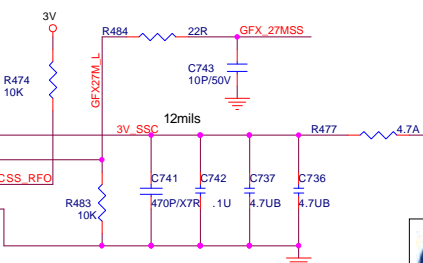
C51M/C51D POWER PLANE/GND & BYPASS



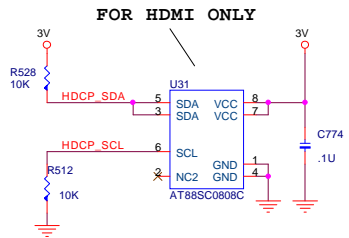
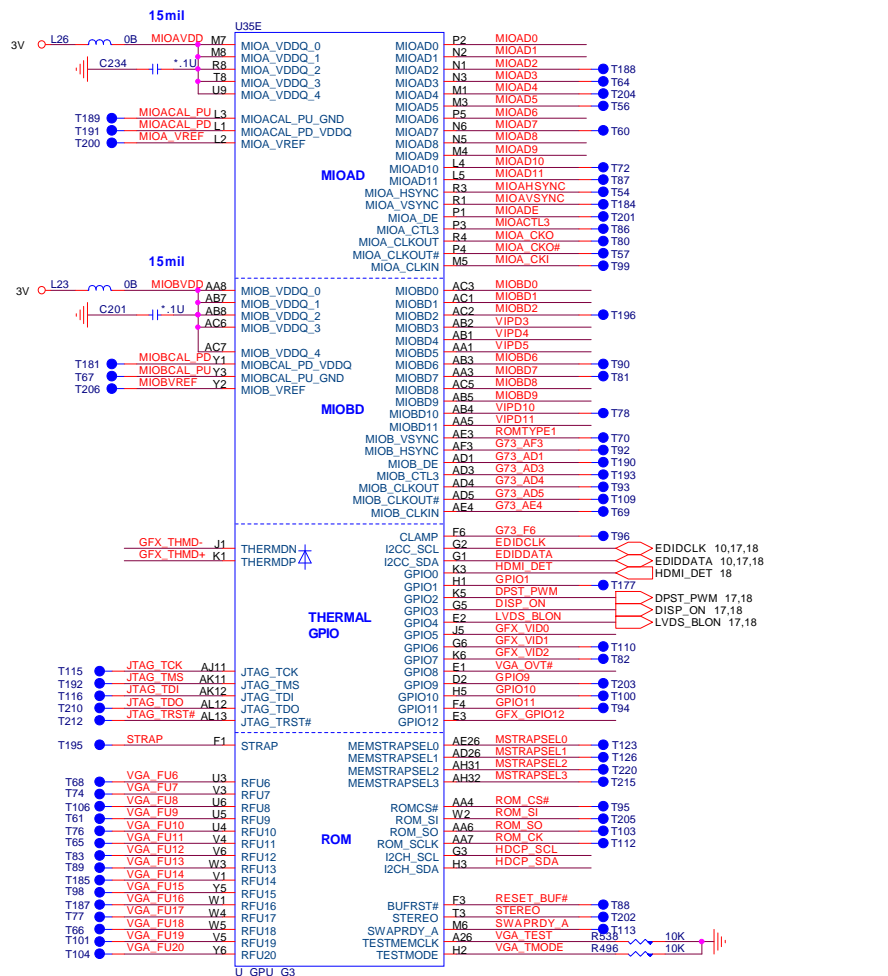
 NB5/RDZ/HW1	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Document Number C51M (POWER/GND)	Date: Wednesday, January 11, 2006 Sheet 8 of 38



SPREAD SPECTRUM



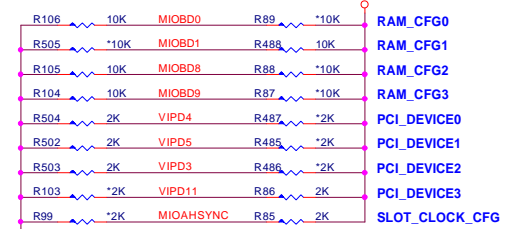
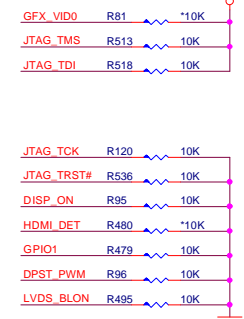
	PROJECT : AT8		Rev 1A
	Quantas Computer Inc.		
Size Custom	Document Number GFX(LVDS, CRT, TV)	Date: Thursday, December 29, 2005 Sheet 10 of 38	



PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0111	G72M-V/G73M-V
others	Reserved

GFX_VID0
 L : Low Voltage
 H : Normal Voltage



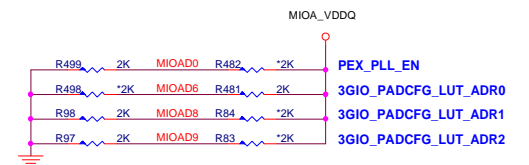
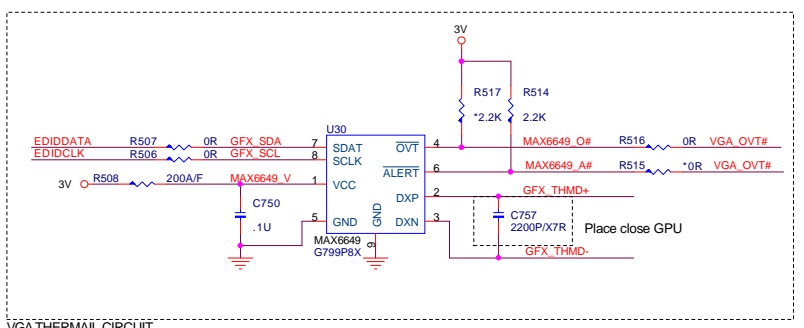
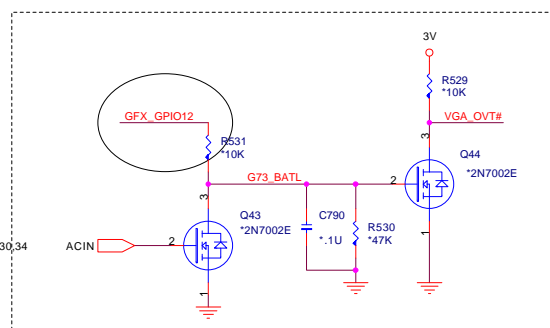
SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN.

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

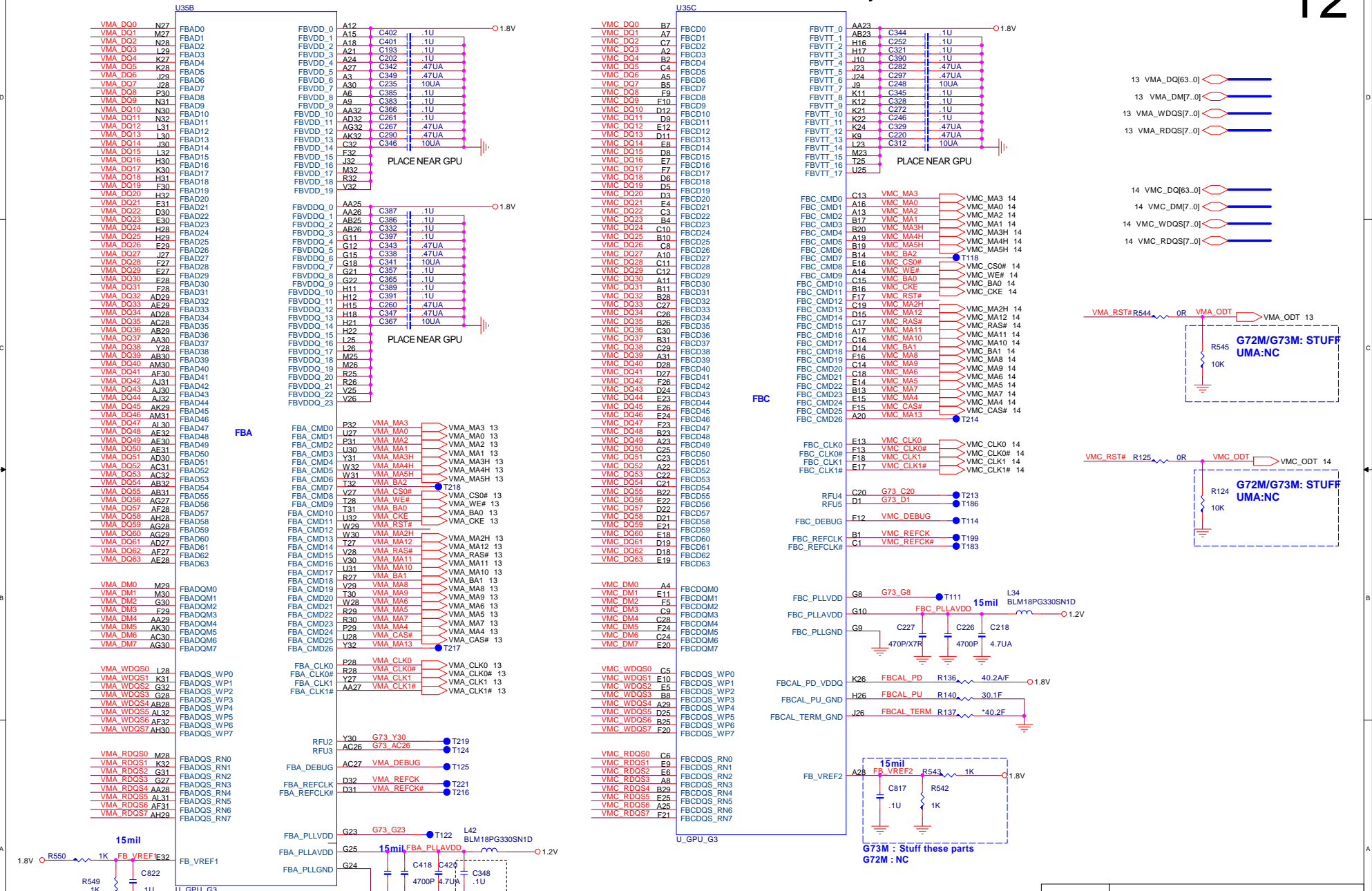
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



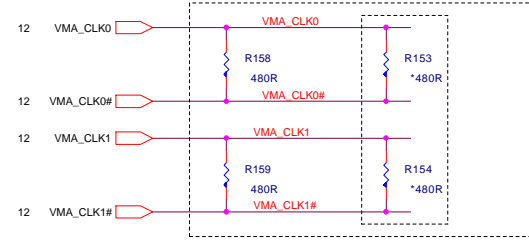
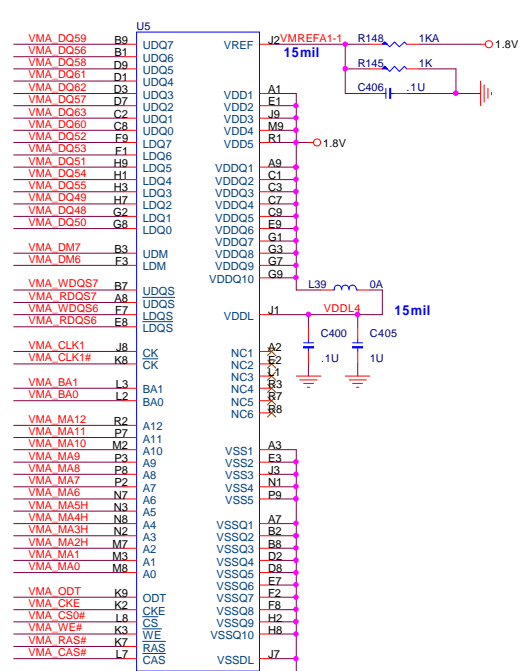
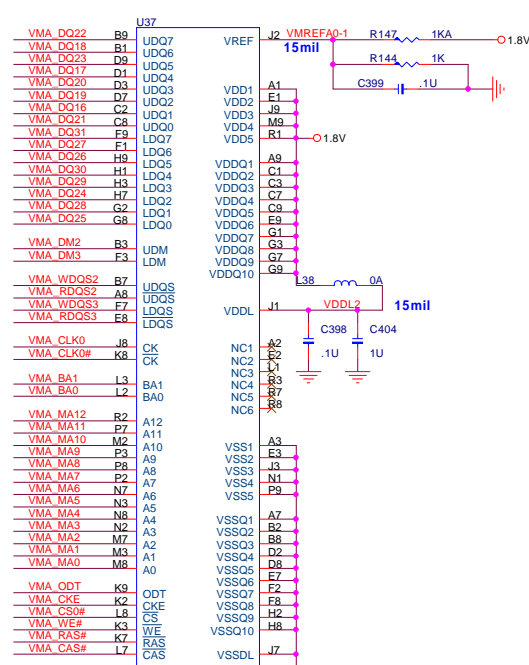
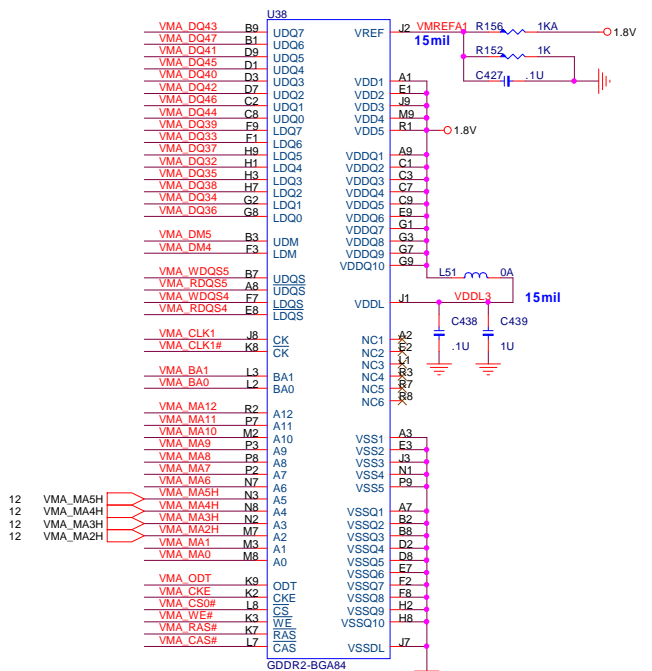
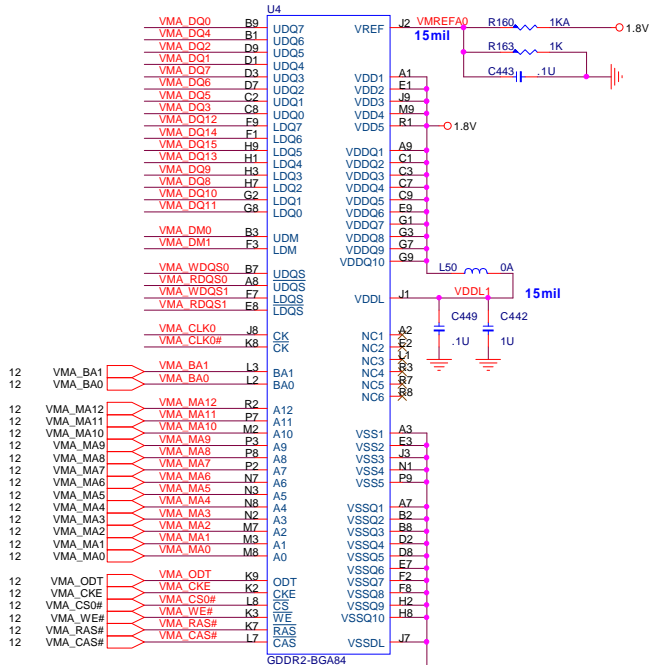
PROJECT : AT8
Quantia Computer Inc.

Size Custom	Document Number	Rev 1A
NB5/RD2/HW1	GFX(ROM, GPIO, STRAP)	
Date: Thursday, December 29, 2005		Sheet 11 of 38

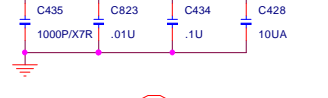
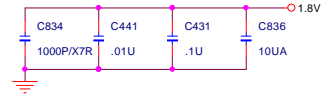
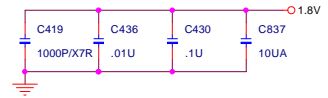
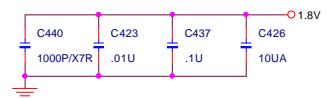
Channel C is available on G73M only



	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Document Number Date: Thursday, December 29, 2005	Rev 1A Sheet 12 of 38




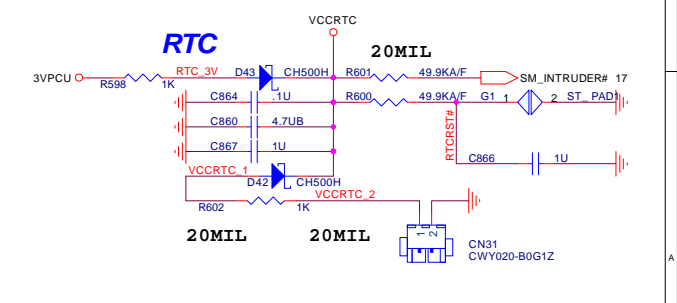
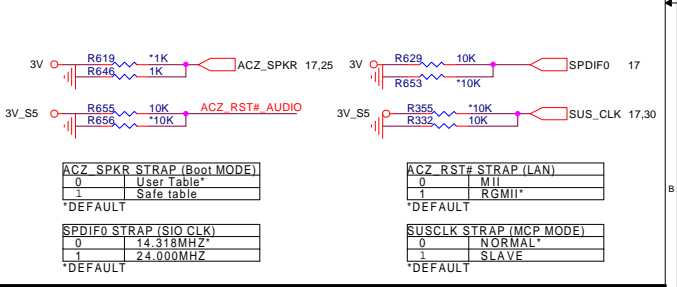
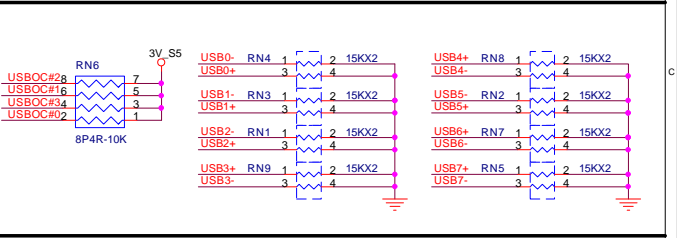
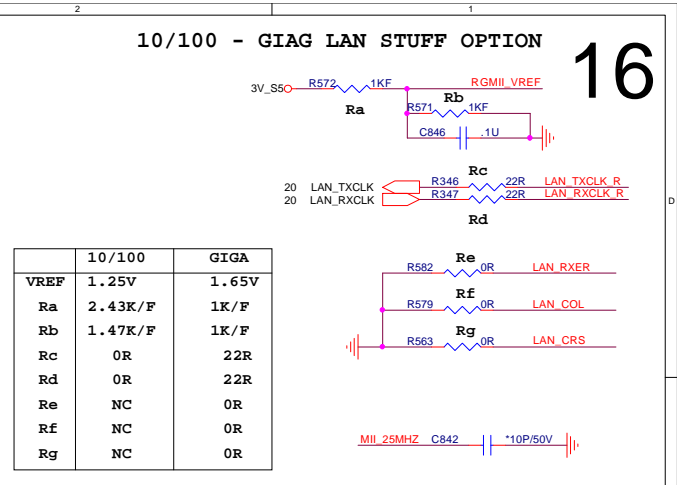
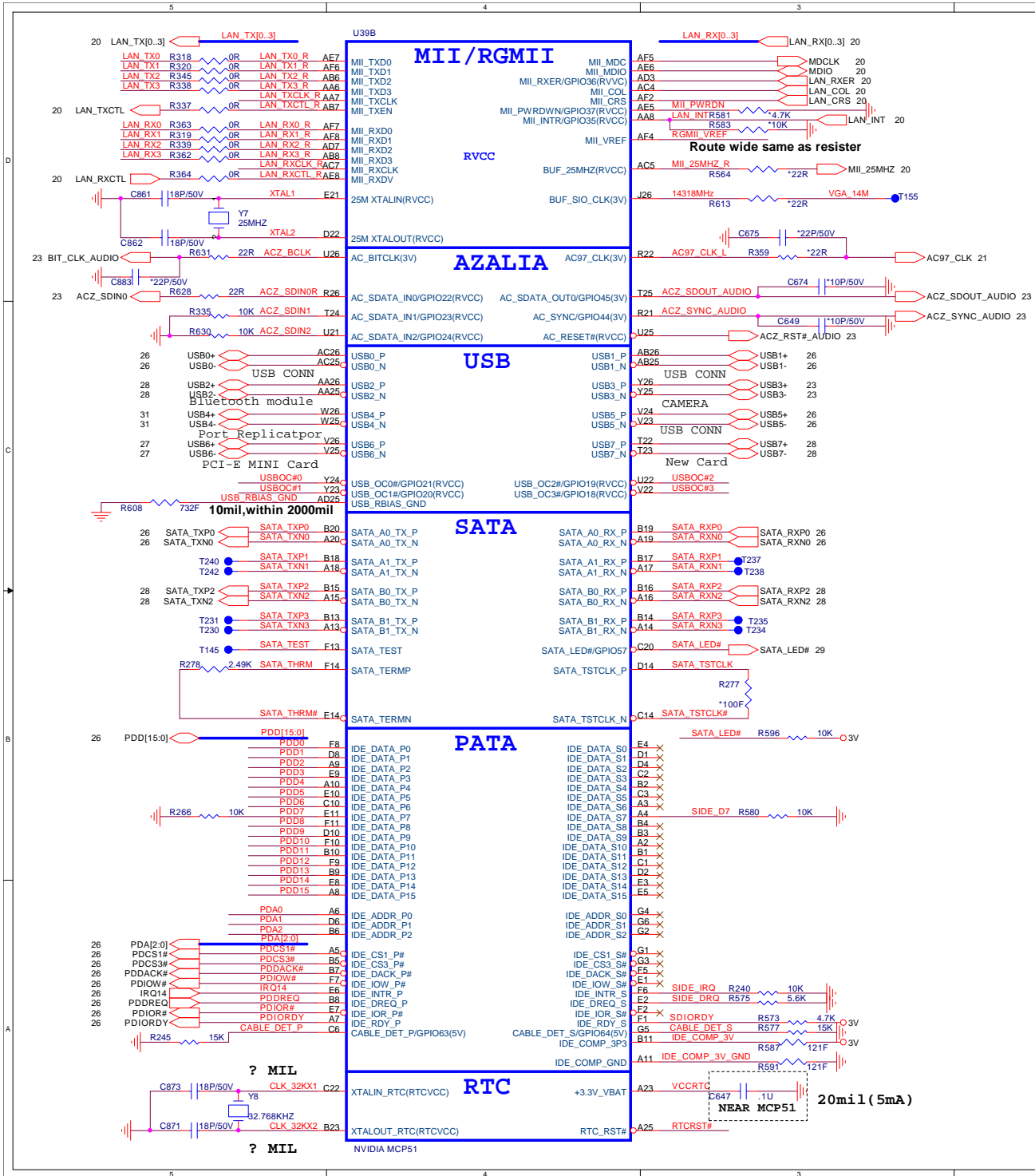
G72M: 120 ohm
G73M: 480 ohm



- 12 VMA_DQ[63..0]
- 12 VMA_DM[7..0]
- 12 VMA_WDQS[7..0]
- 12 VMA_RDQS[7..0]

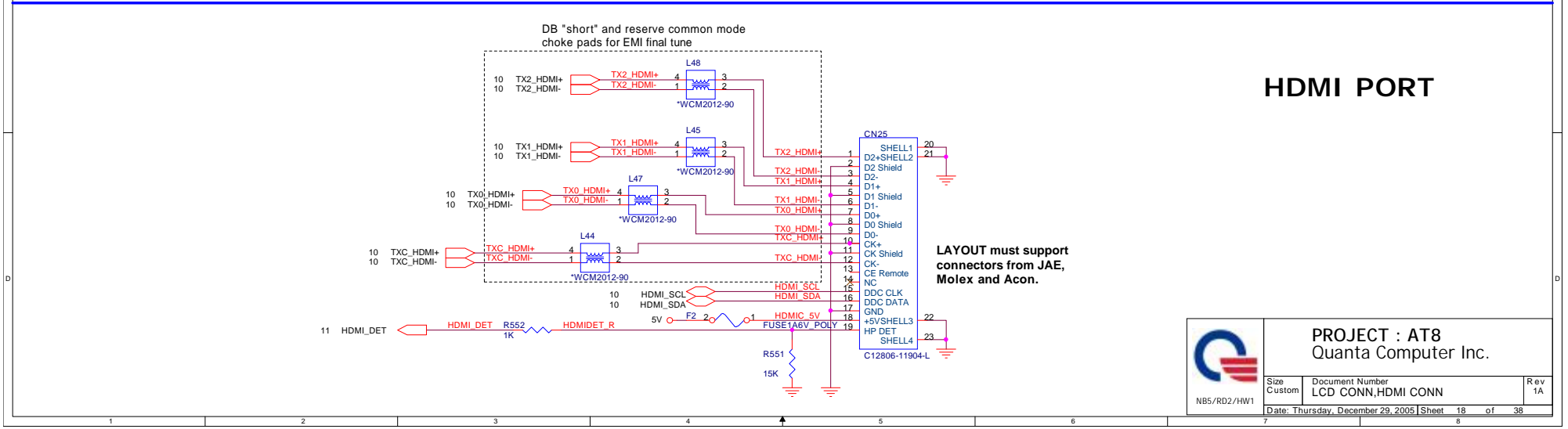
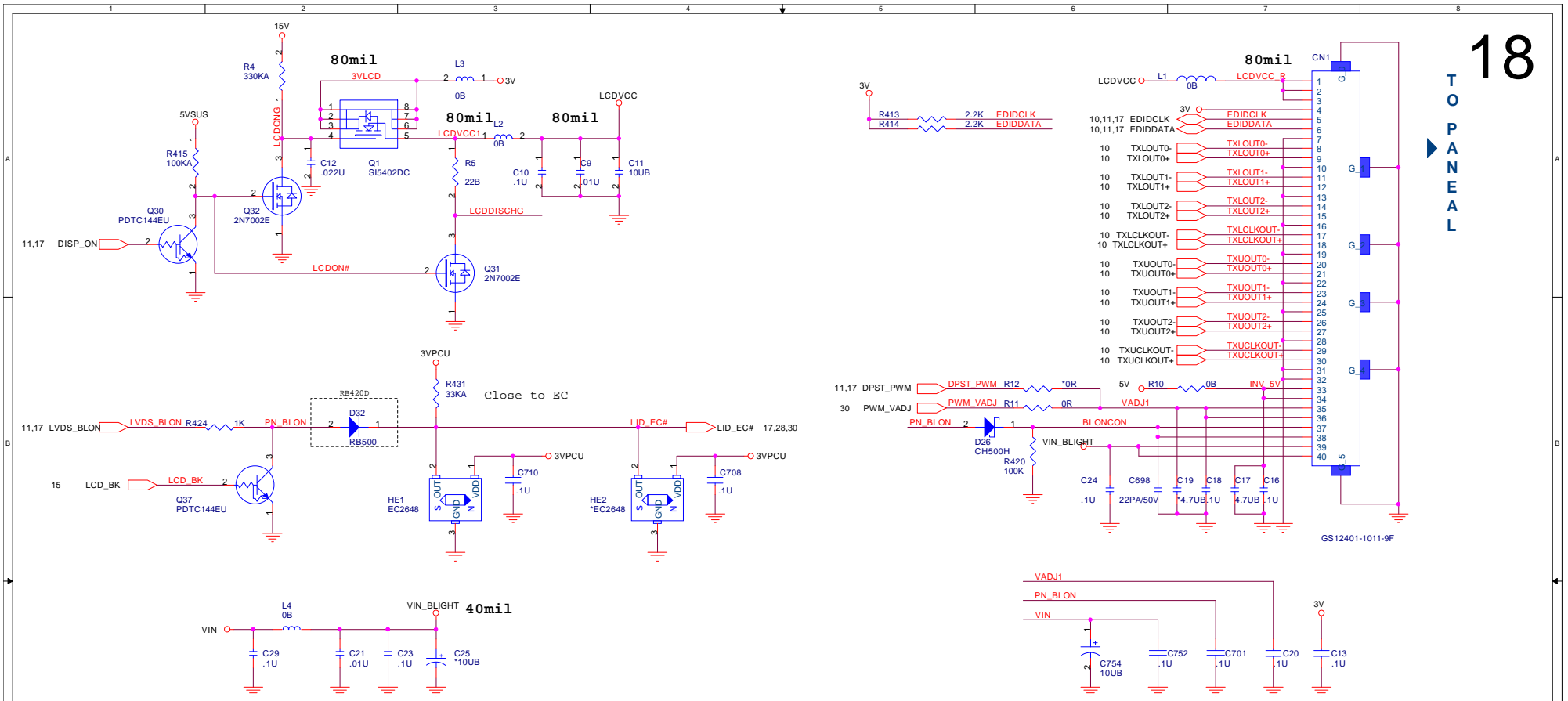
256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

 NB5/RDZ/HW1	PROJECT : AT8 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number VRAM-1 (GDDR2)	Date: Thursday, December 29, 2005

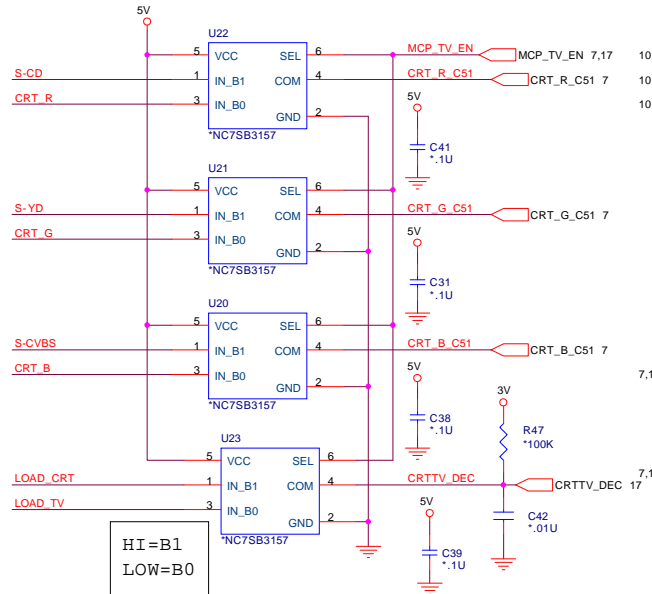


PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MCP51 (1 of 3)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 16 of 38

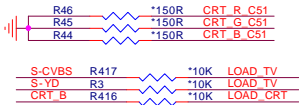


CRT PORT

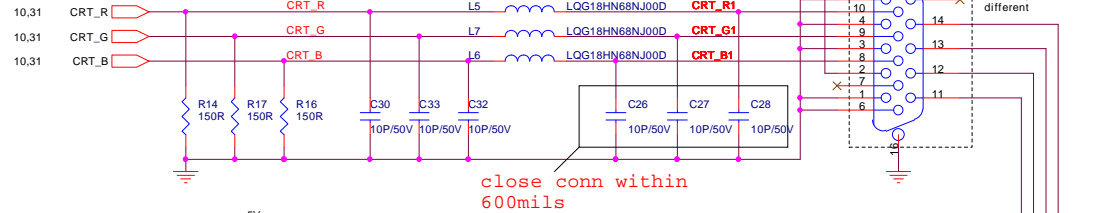


HI=B1
LOW=B0

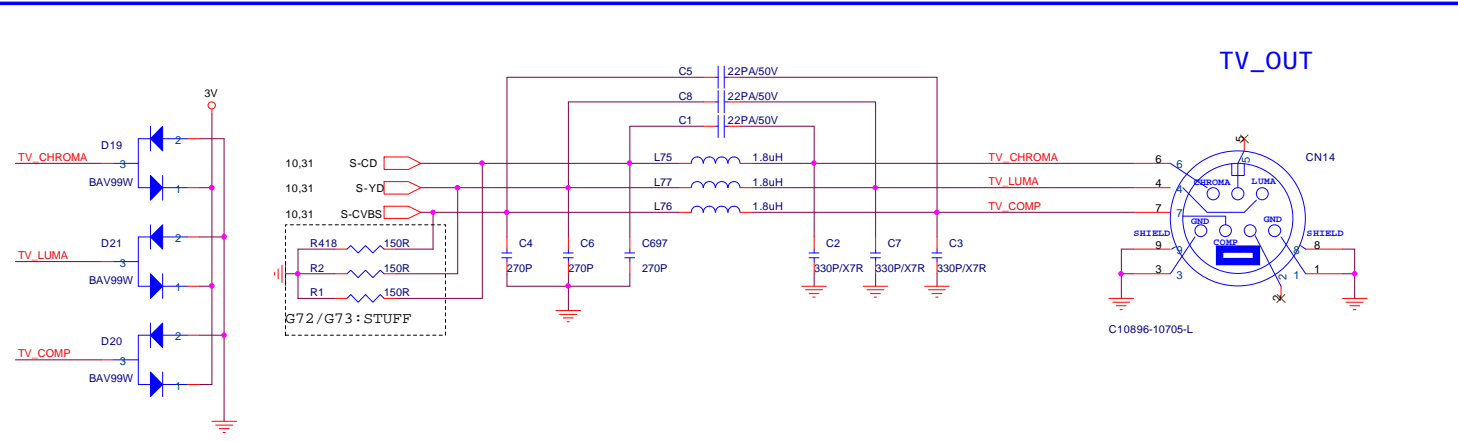
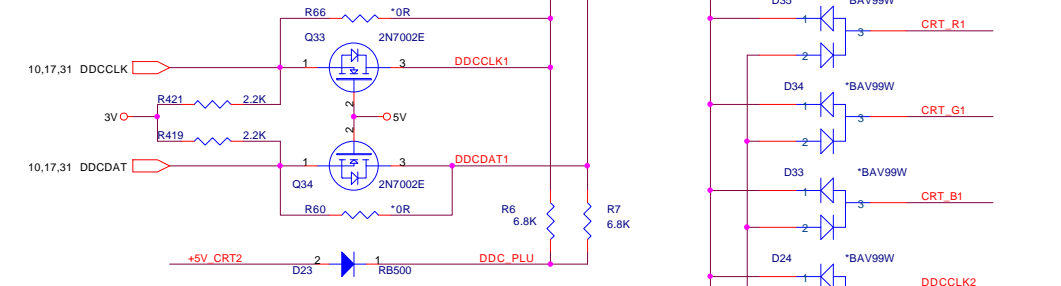
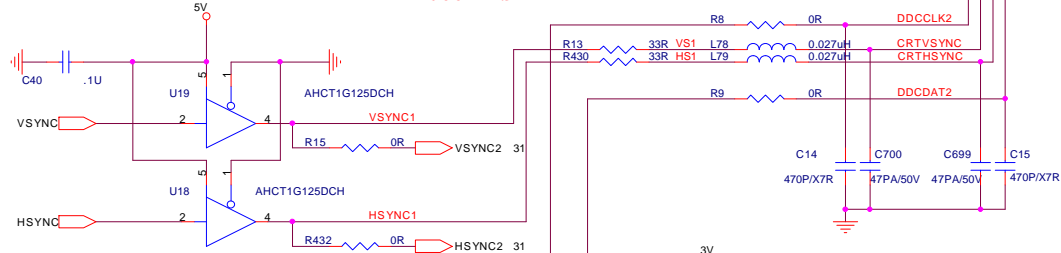
close within
600mils



75-R as possible as
closed to SB

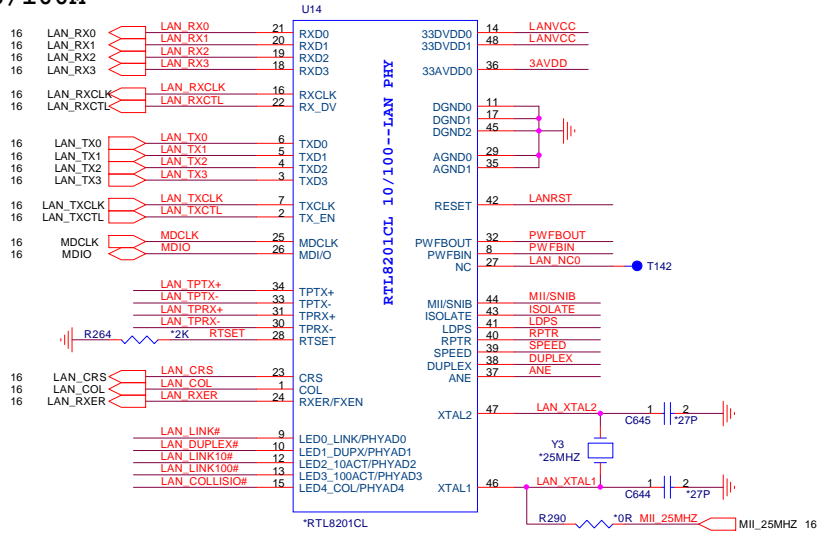


close conn within
600mils

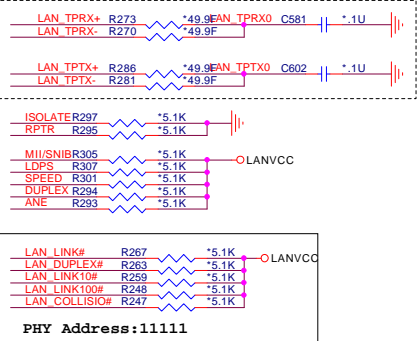


	PROJECT : AT8 Quanta Computer Inc.		
	Size Custom	Document Number CRT_TV_OUT	Rev 1A
	Date: Thursday, December 29, 2005		Sheet 19 of 38

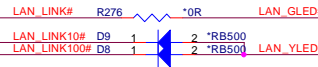
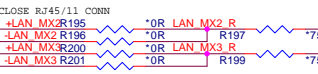
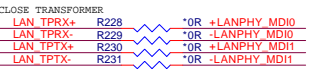
10/100M



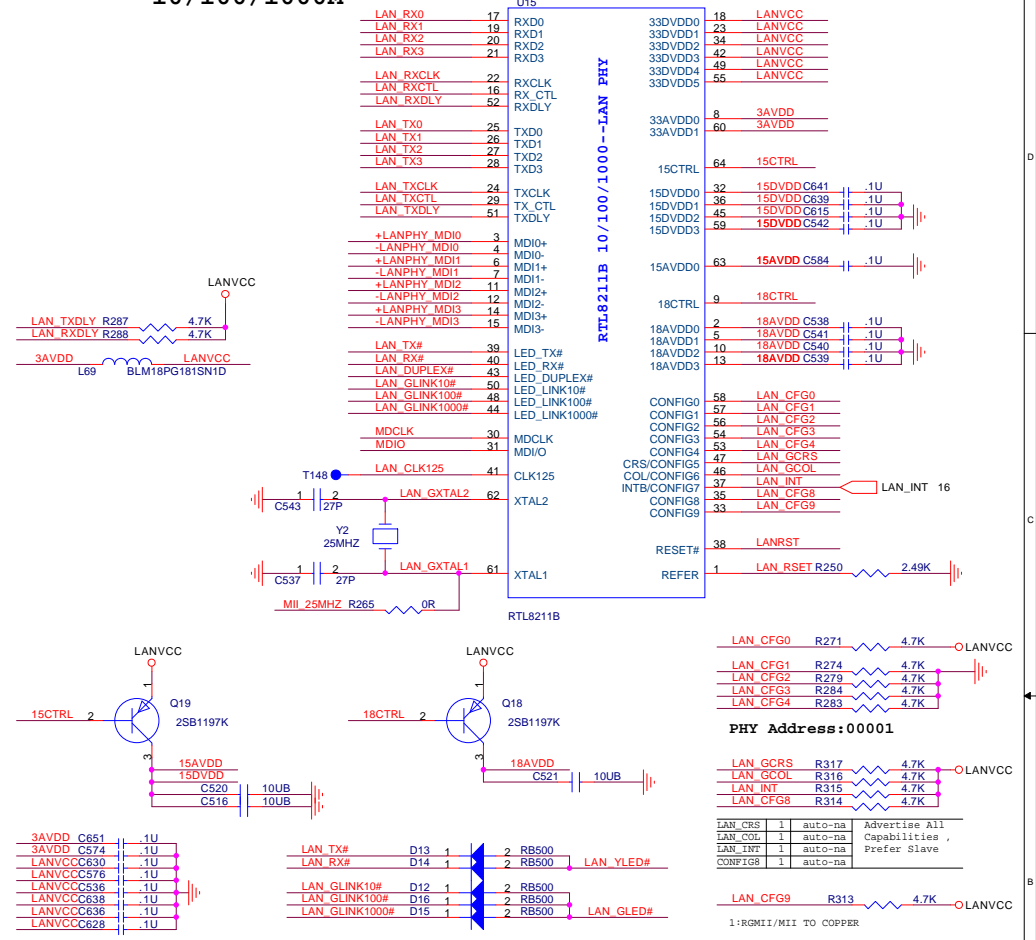
Close To RTL8201CL



LAN_COL	1		RTL8201BL LED
LAN_RXER_R	0	Default	RTL8201CL LED
LAN_RXER_R	1		Fiber Mode
LAN_CRIS	0	Default	UTP Mode
LAN_CRIS	1		Ensure operating at normal mode



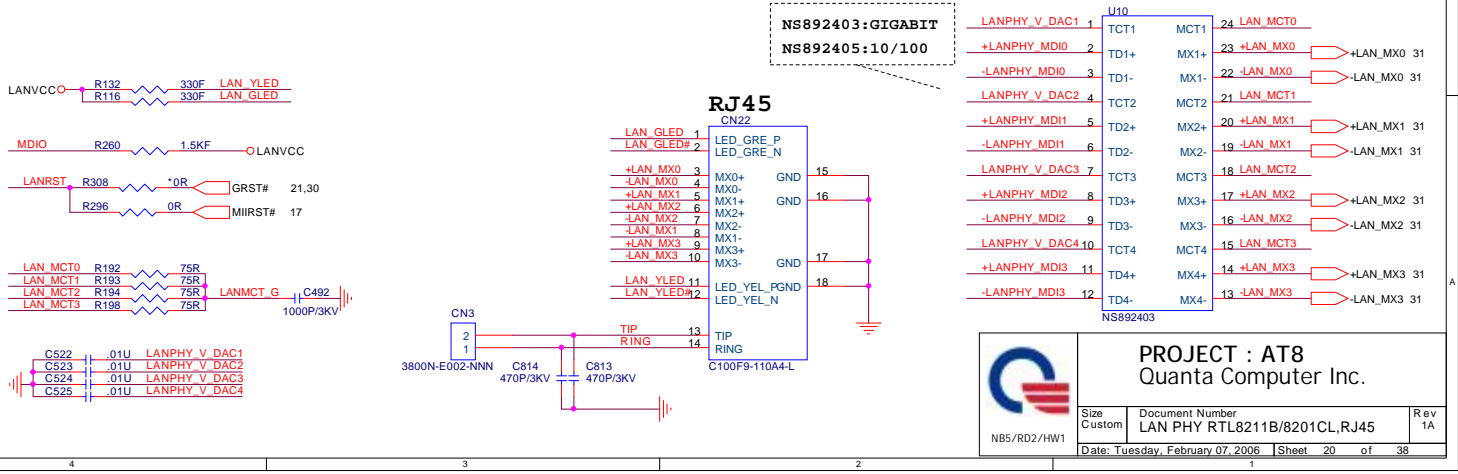
10/100/1000M



PHY Address: 00001

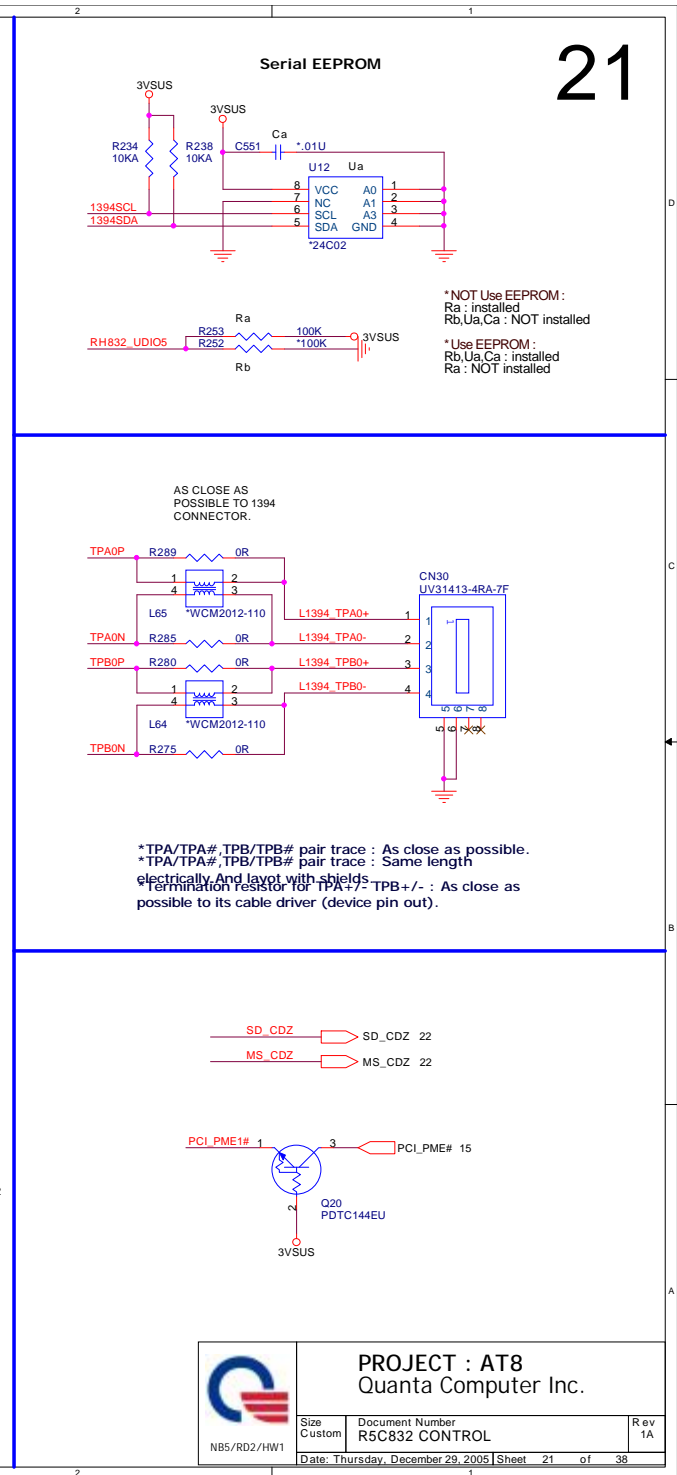
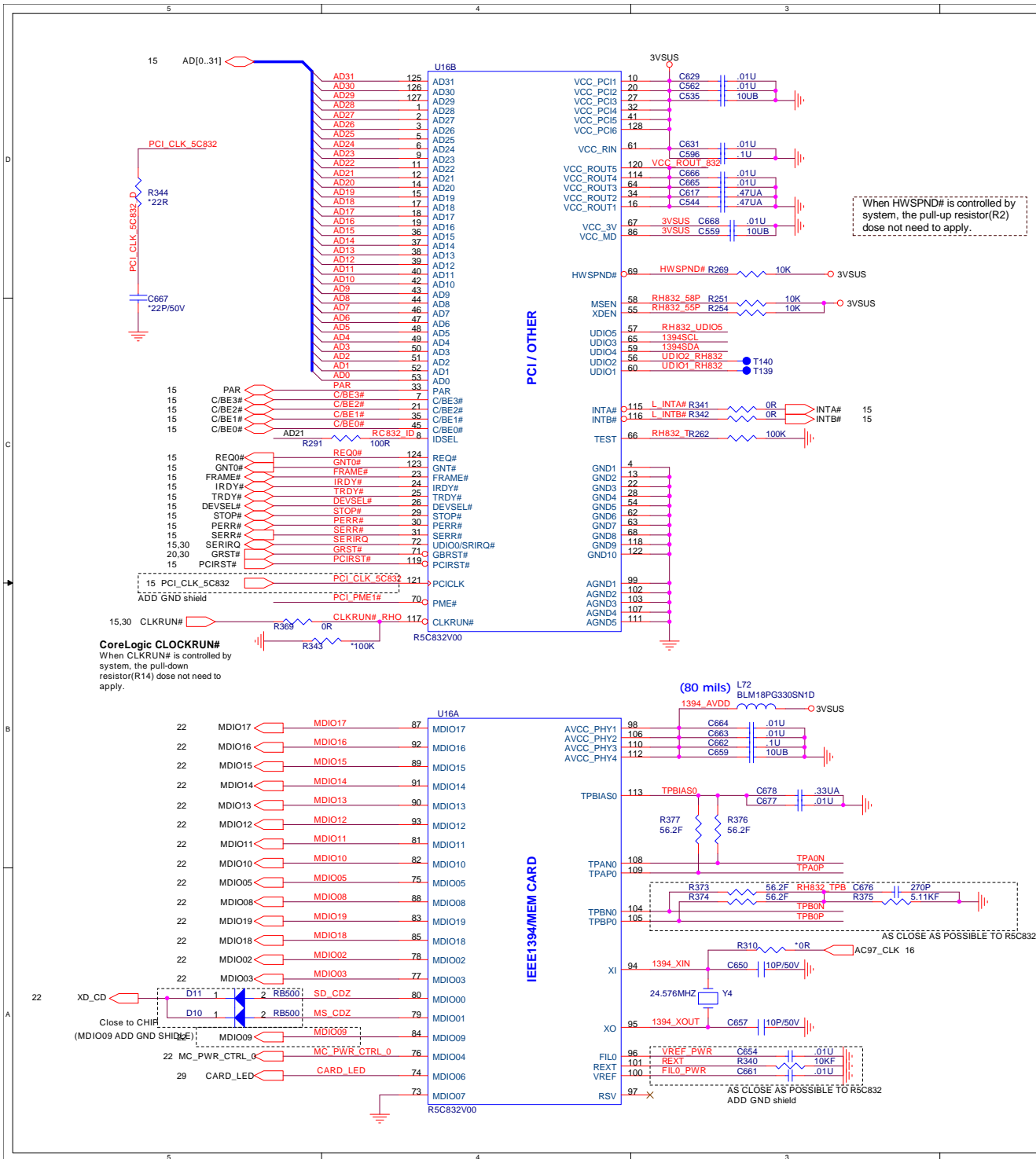
LAN_CRIS	1	auto-na	Advertise All
LAN_COL	1	auto-na	capabilities
LAN_INT	1	auto-na	Prefer Slave
CONFIG	1	auto-na	

1:RG/MII to COPPER



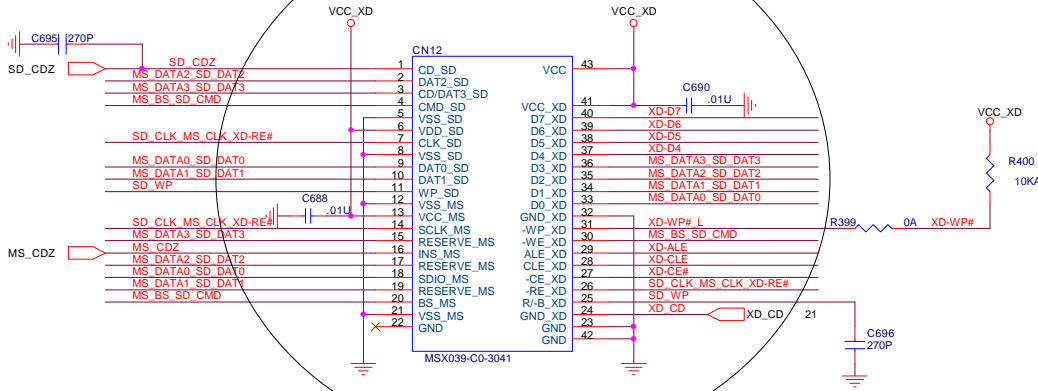
PROJECT : AT8
LAN PHY RTL8211B/8201CL,RJ45

Size Custom	Document Number	Rev 1A
Date: Tuesday, February 07, 2006	LAN PHY RTL8211B/8201CL,RJ45	Sheet 20 of 38

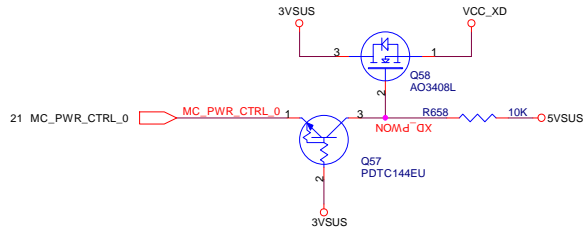
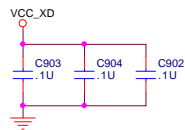
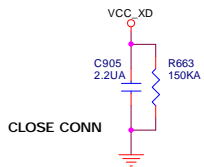


4 IN1 CARD READER
XD, MMC/SD, MS/MSP

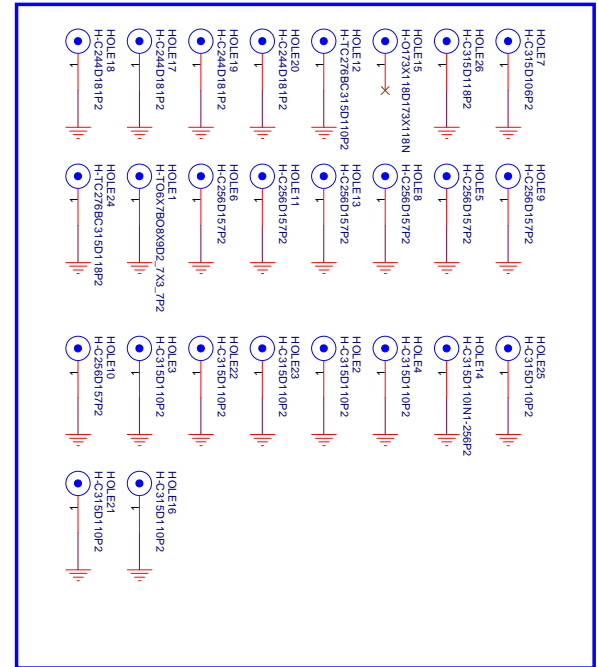
CHECK CONN.



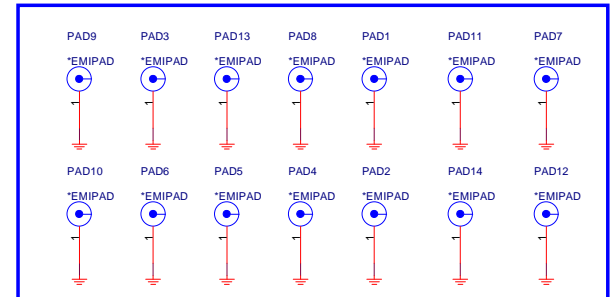
21	MDIO03	R398	56R	SD_WP
21	MDIO17	R409	56R	XD-D7
21	MDIO16	R408	56R	XD-D6
21	MDIO15	R407	56R	XD-D5
21	MDIO14	R406	56R	XD-D4
21	MDIO13	R405	56R	MS_DATA3_SD_DAT3
21	MDIO12	R404	56R	MS_DATA2_SD_DAT2
21	MDIO11	R403	56R	MS_DATA1_SD_DAT1
21	MDIO10	R402	56R	MS_DATA0_SD_DAT0
21	MDIO08	R397	56R	MS_BS_SD_CMD
21	MDIO05	R401	56R	XD-WP#
21	MDIO19	R396	56R	XD-ALE
21	MDIO18	R395	56R	XD-CLE
21	MDIO02	R394	56R	XD-CE#
21	MDIO09	R393	56R	SD_CLK_MS_CLK_XD-RE#



SCREW HOLE



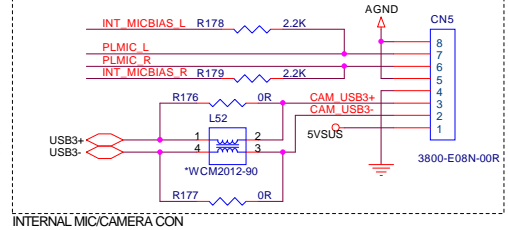
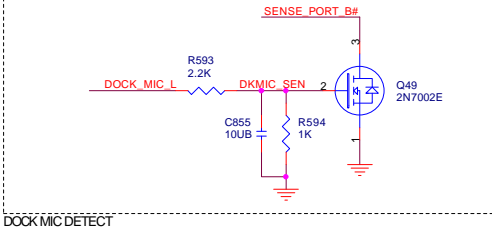
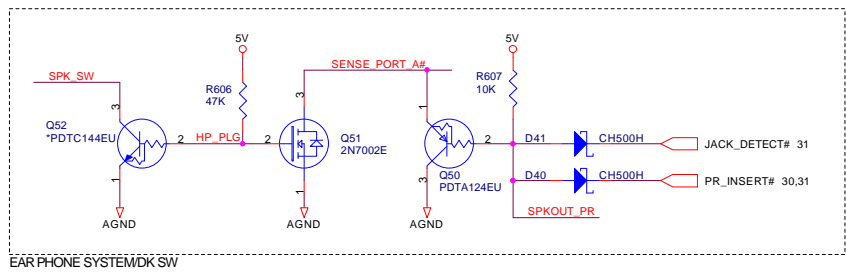
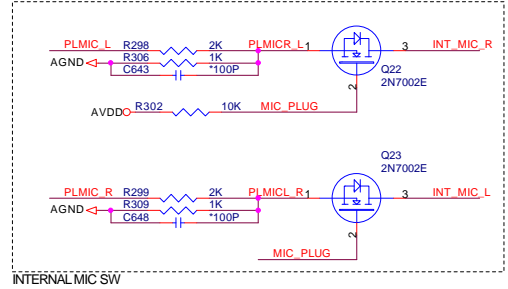
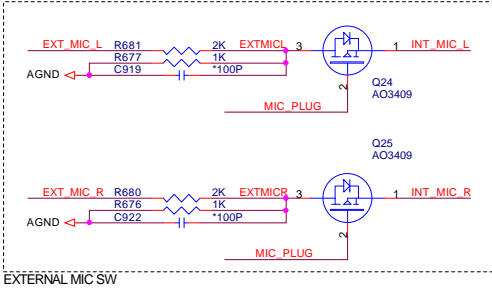
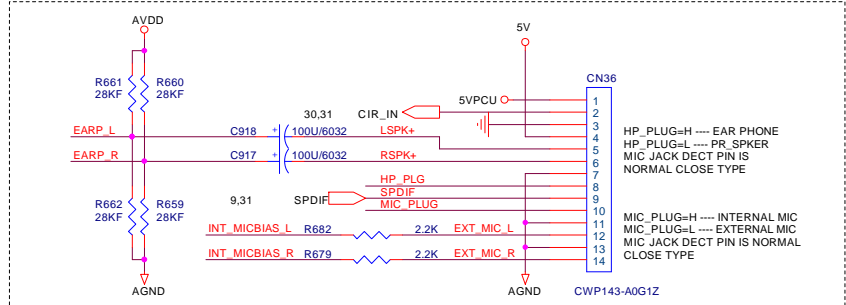
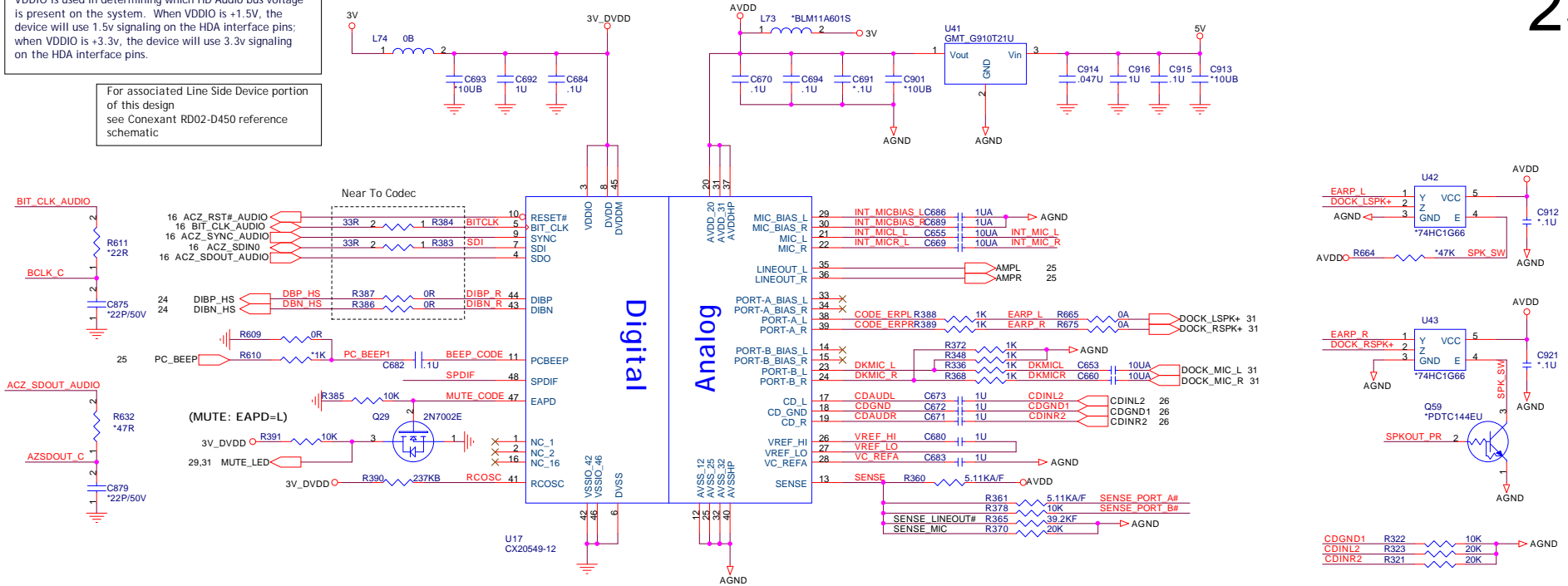
EMI PAD



	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom	Document Number CARD READER CONN
NB5/RD2/HW1	Date: Thursday, December 29, 2005	Sheet 22 of 38
		Rev 1A

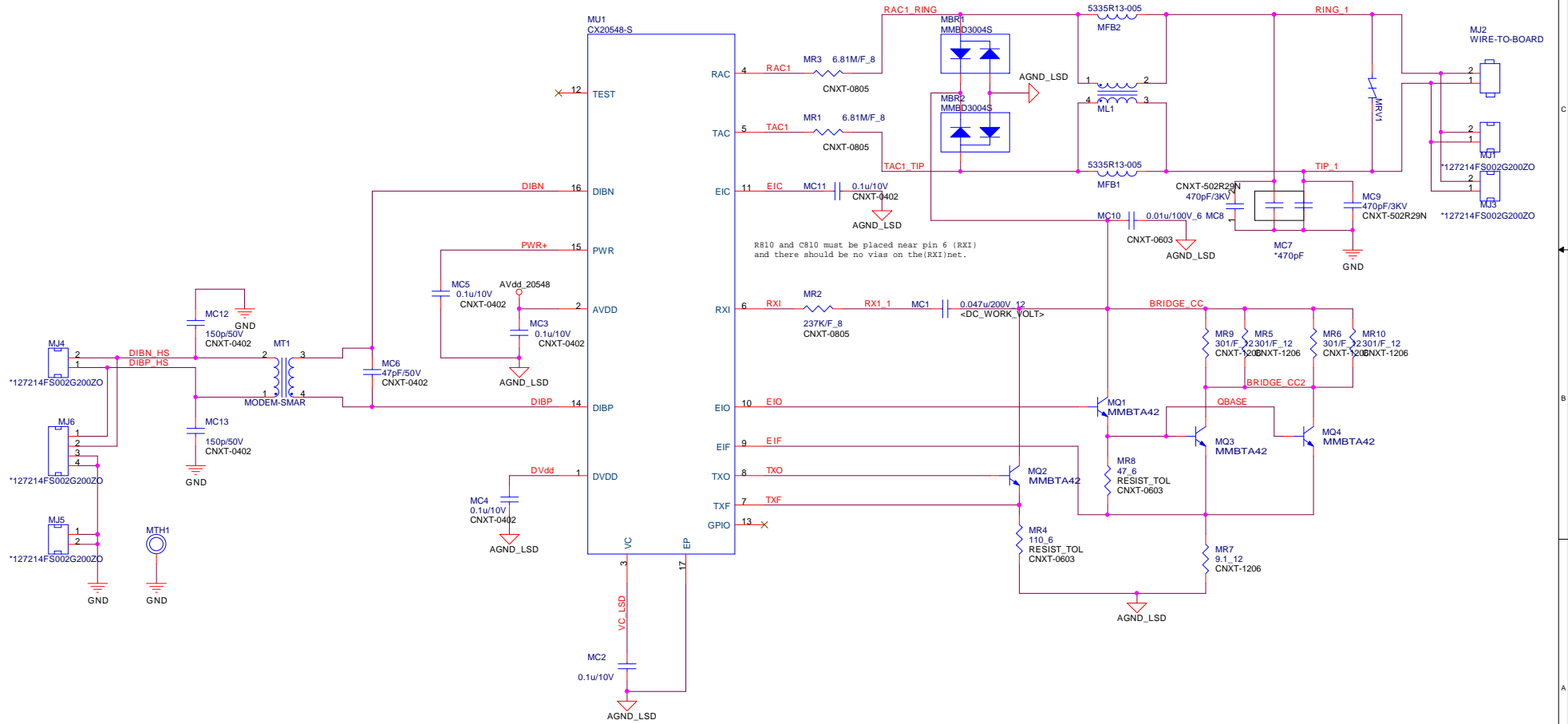
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

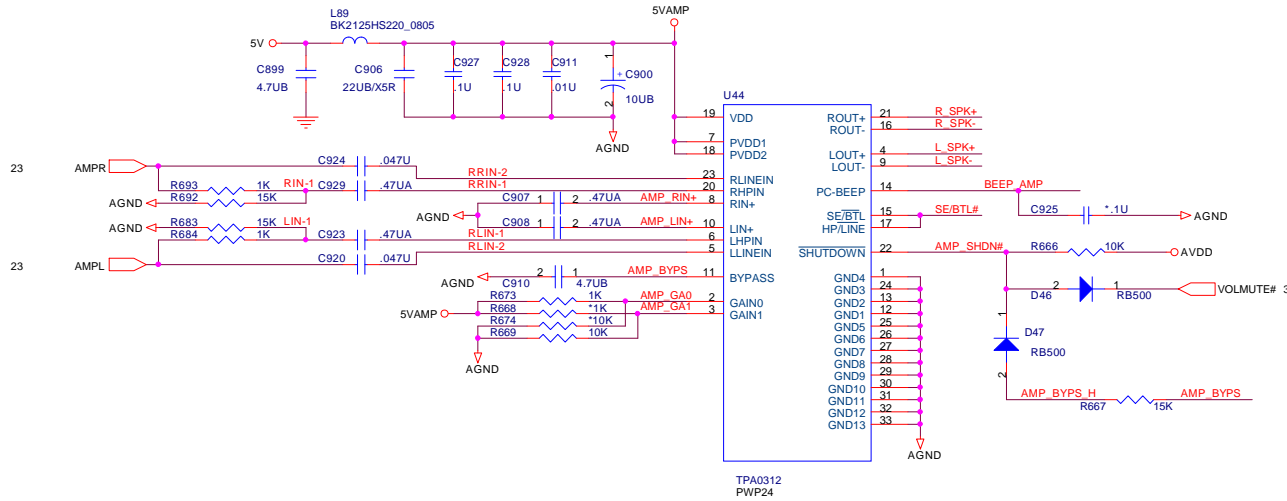


	PROJECT : AT8 Quanta Computer Inc.		
	Size Custom	Document Number Azalia CTRL_CONEXANT20549-12	Rev 1A
	Date: Thursday, December 29, 2005		Sheet 23 of 38

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

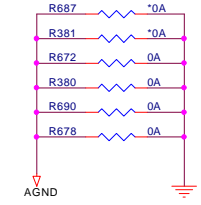


	PROJECT : AT8 Quantia Computer Inc.		
	Size Custom	Document Number MODEM (DAA)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 24 of 38	

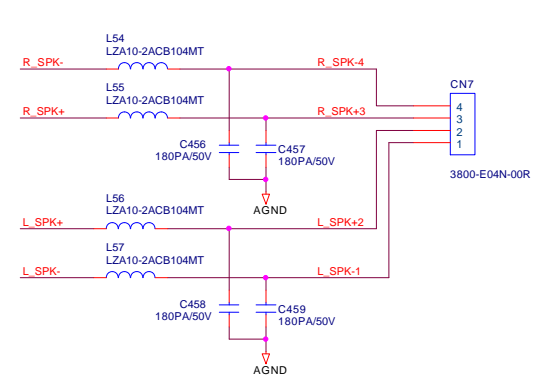


0312 Gain Table

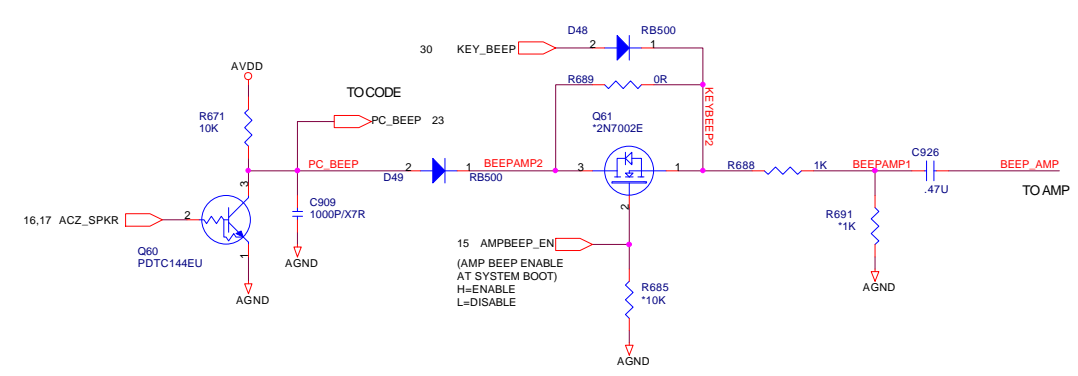
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER

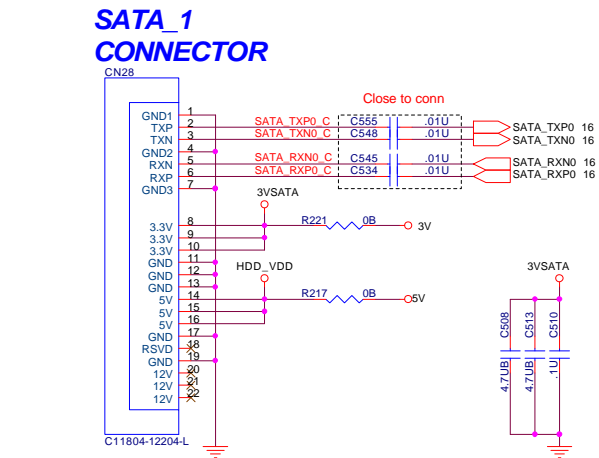
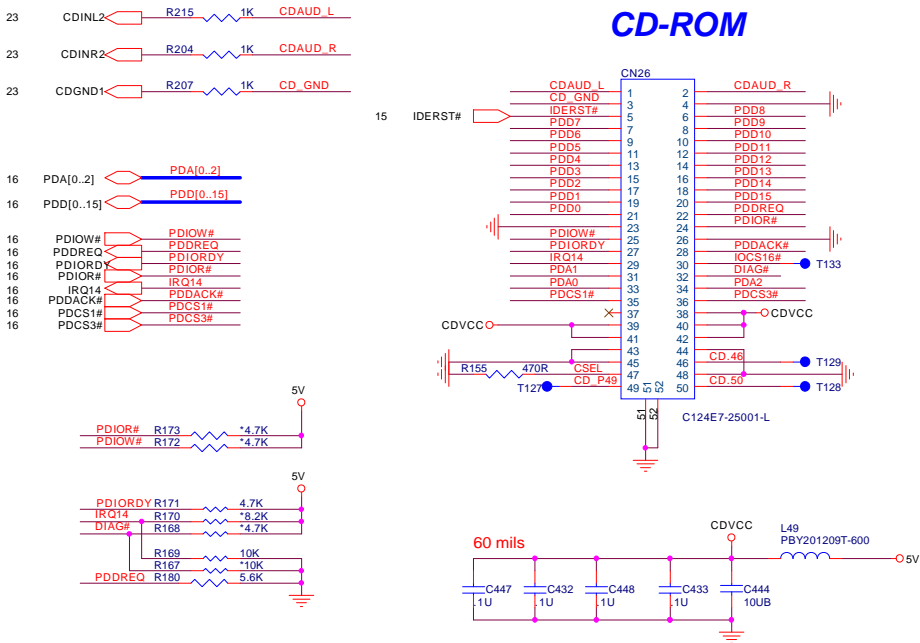


PCSPK BEEP

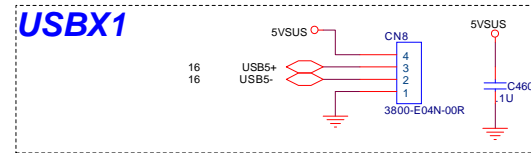
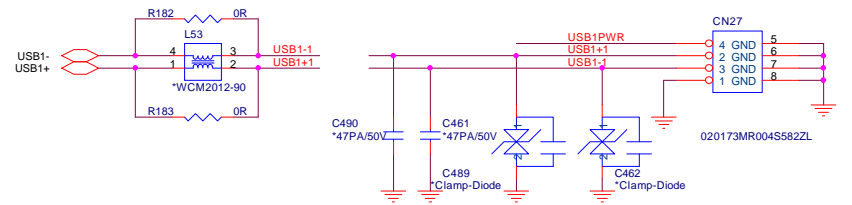
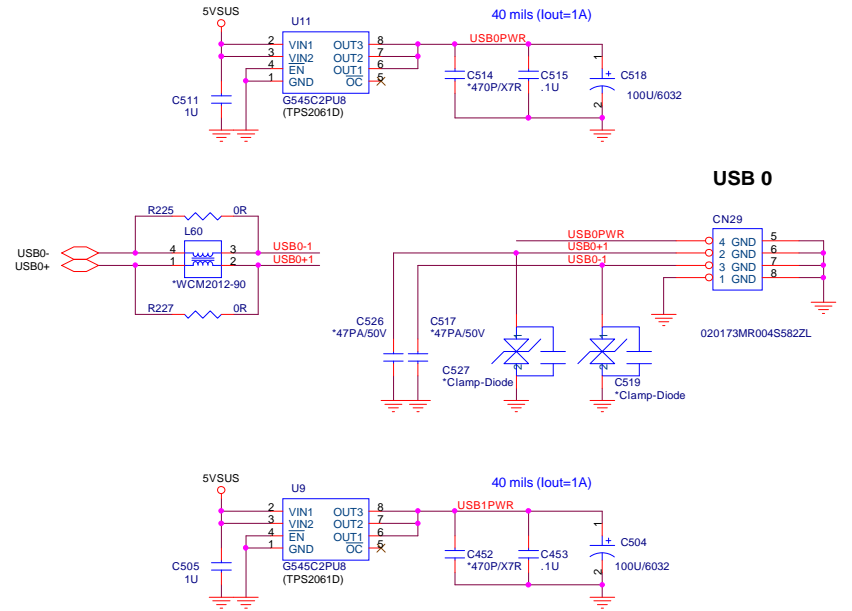


PROJECT : AT8
Quantas Computer Inc.

Size Custom	Document Number JACK, AMP_TPA0312	Rev 1A
Date: Thursday, December 29, 2005 Sheet 25 of 38		



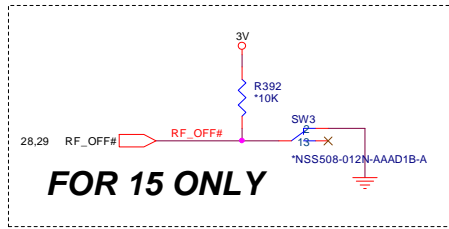
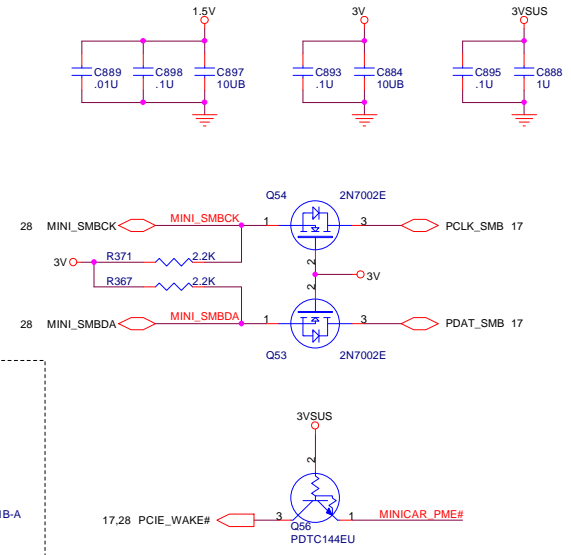
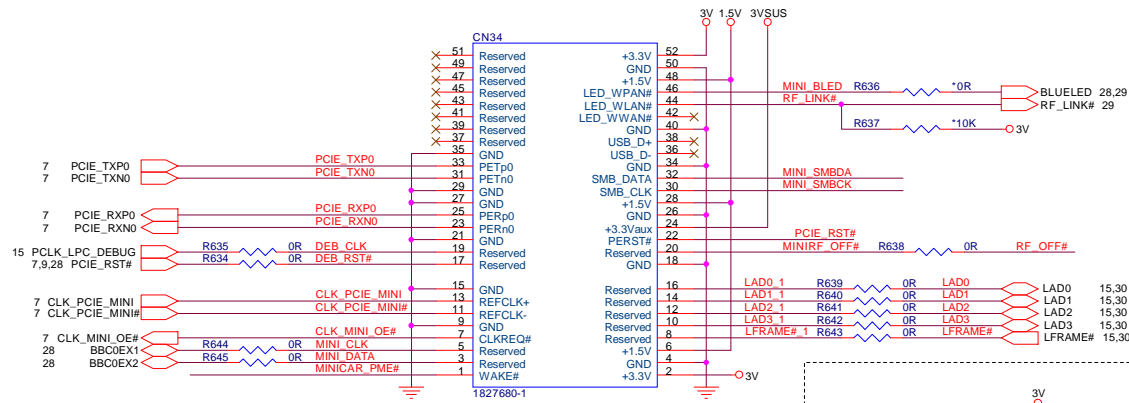
USBX2



TO AD/B

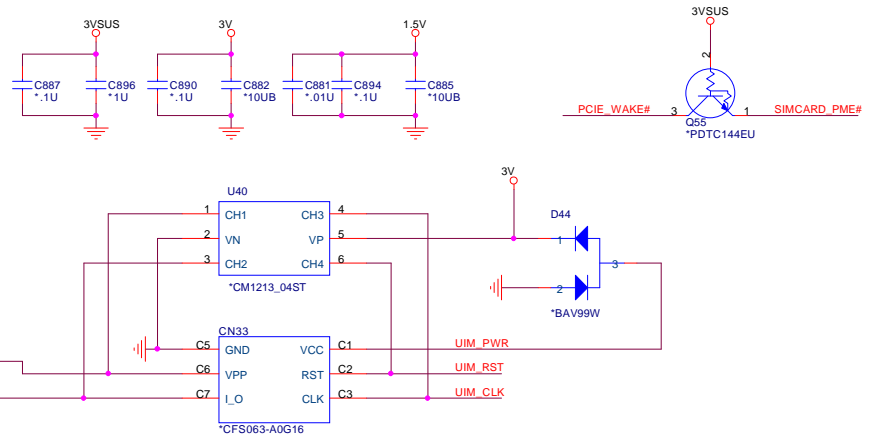
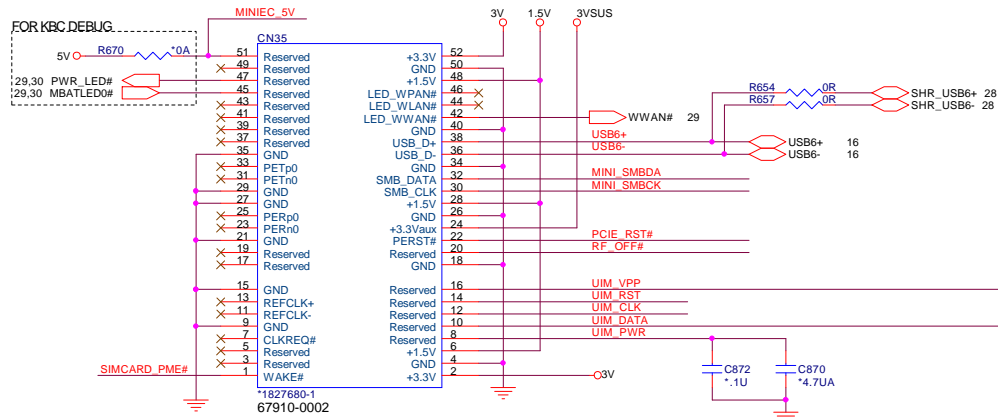
	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Document Number SATA HDD, CD-ROM, USBX2 Date: Thursday, December 29, 2005 Sheet 26 of 38	Rev 1A


Mini PCI-E Card 1 WLAN



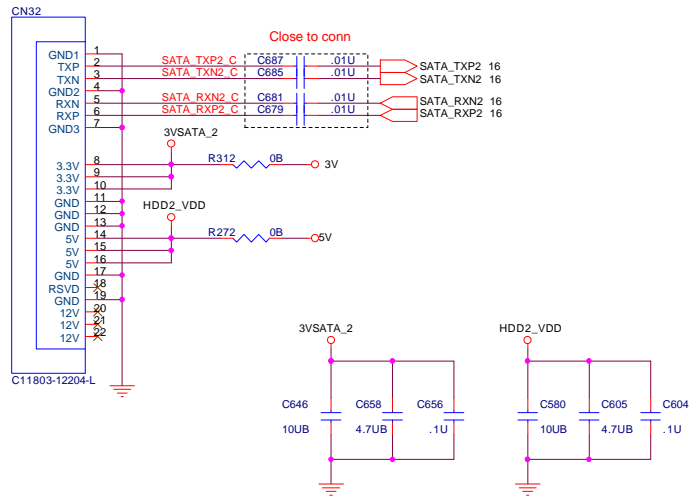
Mini PCI-E Card 2 WWAN(W/SIM)

FOR 15 ONLY

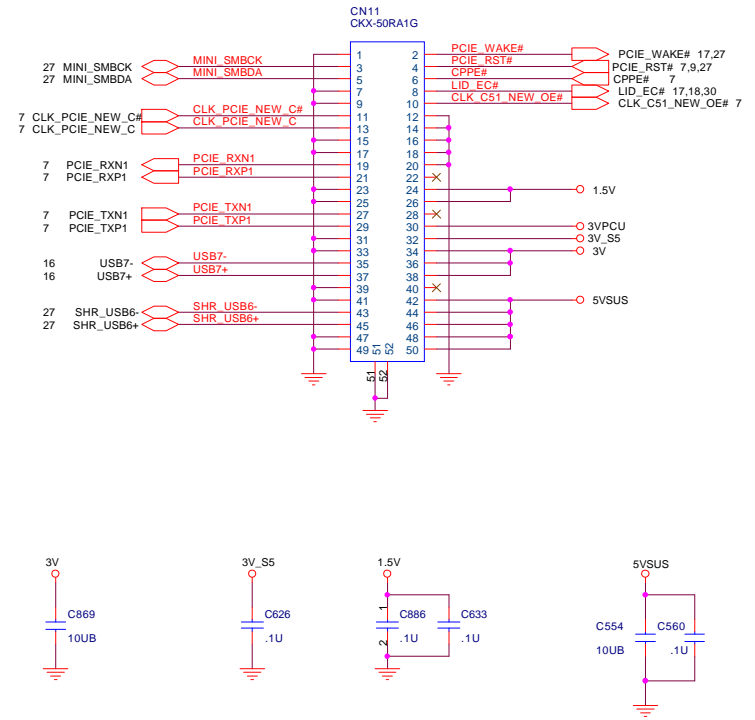


 NB5/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Date: Thursday, December 29, 2005	Document Number MINI CARD Sheet 27 of 38

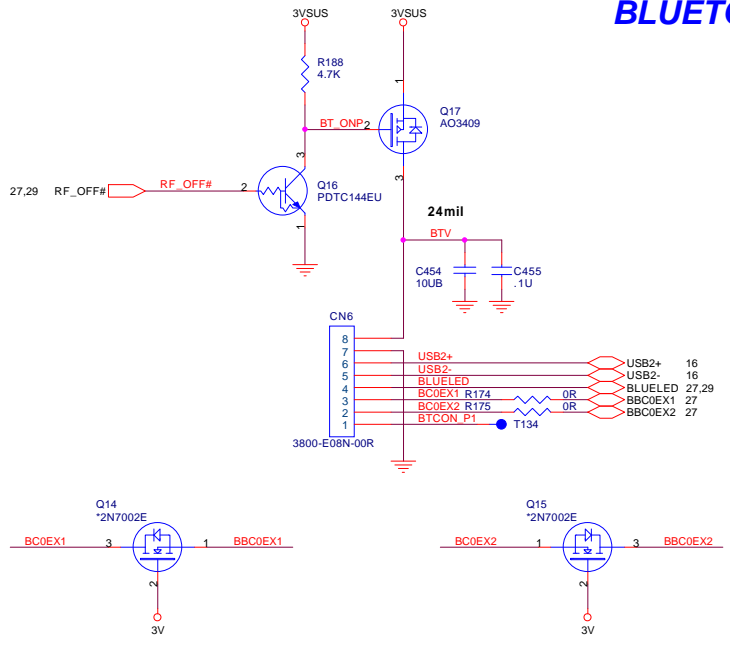
SATA_2 CONNECTOR For 17"W Second HDD




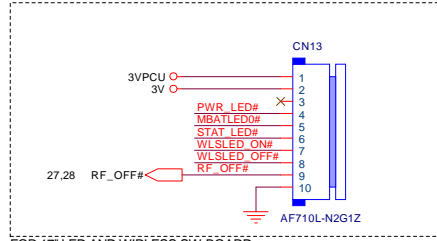
NEWCARD



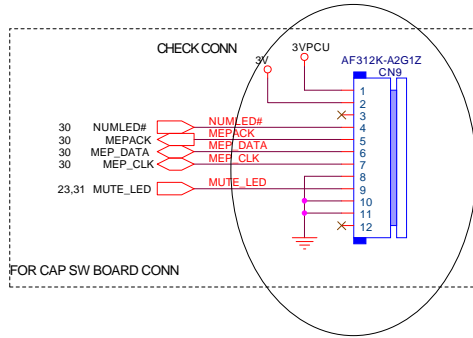
BLUETOOTH



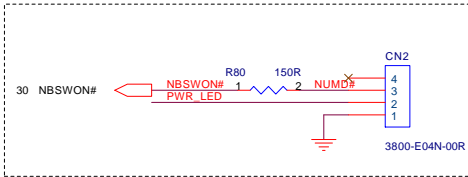
 NB5/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Date: Thursday, December 29, 2005	Document Number NEW CARD/BT



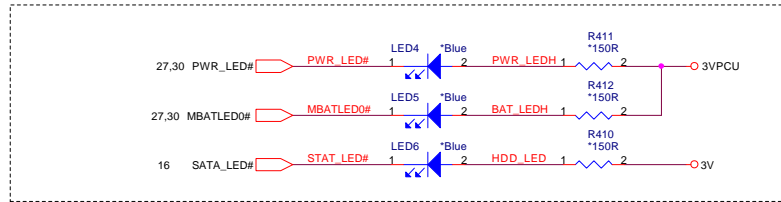
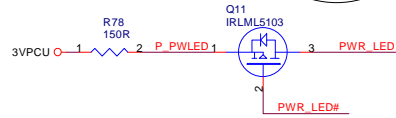
FOR 17" LED AND WIRLESS SW BOARD



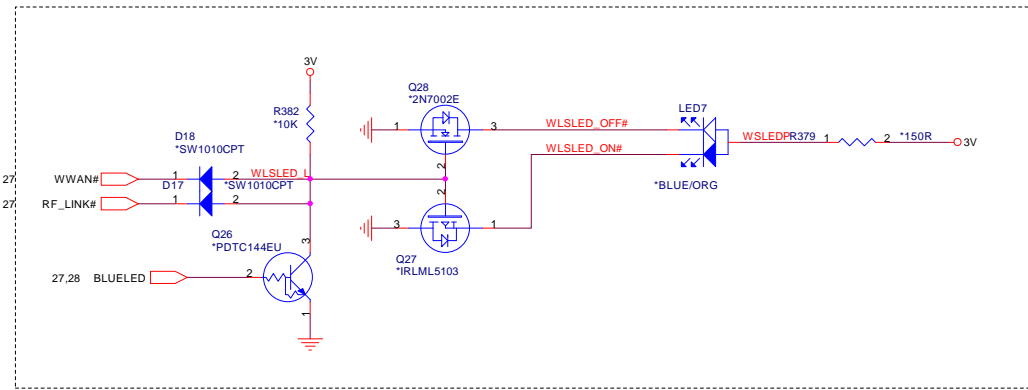
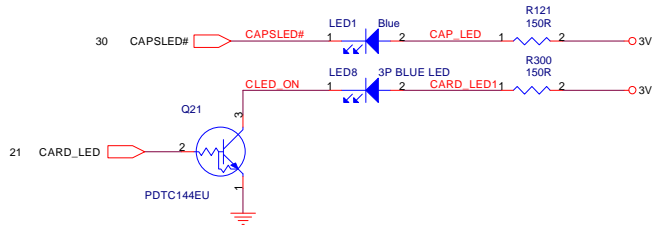
FOR CAP SW BOARD CONN



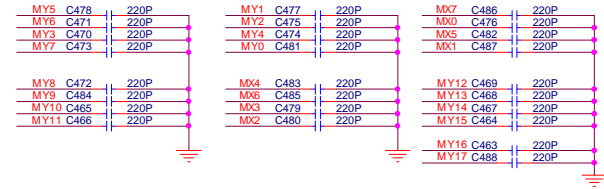
FOR POWER ON SW BOARD



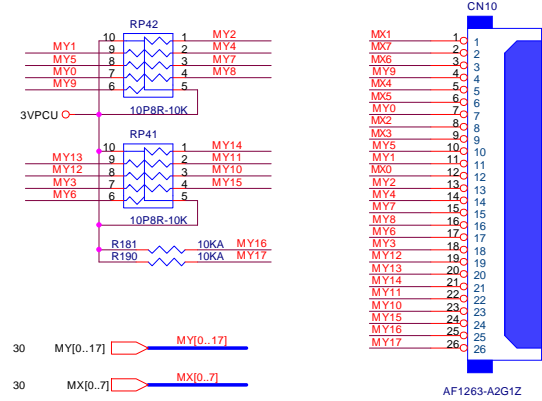
FOR 15.4" LED



FOR WIRELESS LED



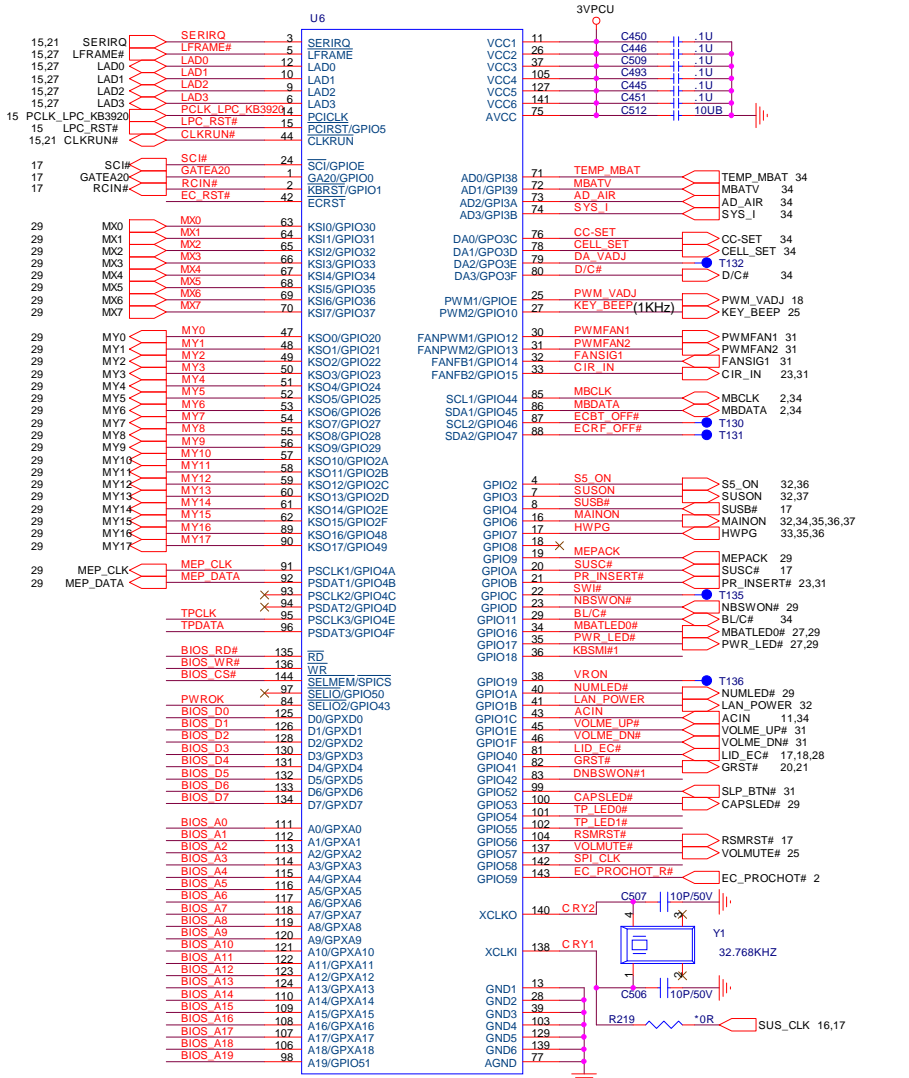
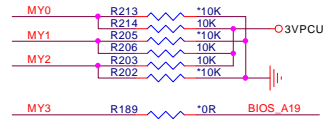
KEYBOARD PULL-UP



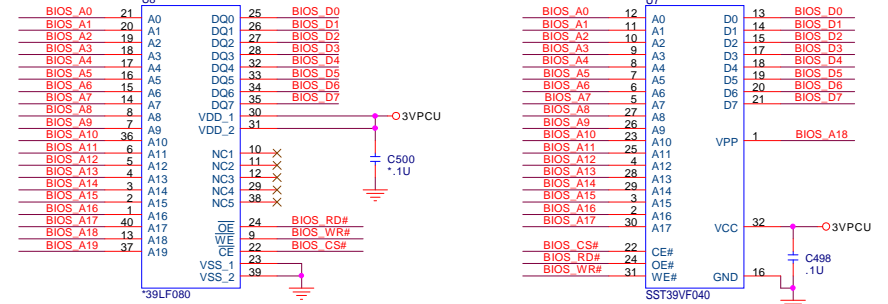
	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom	Document Number LED/KEYBOARD/TP
NB5/RDZ/HW1	Date: Thursday, December 29, 2005	Rev 1A

STRAP PIN

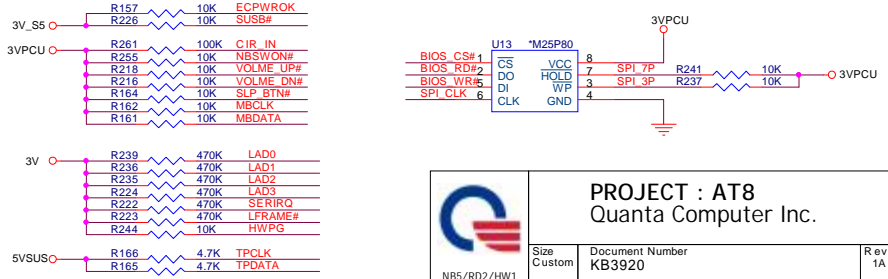
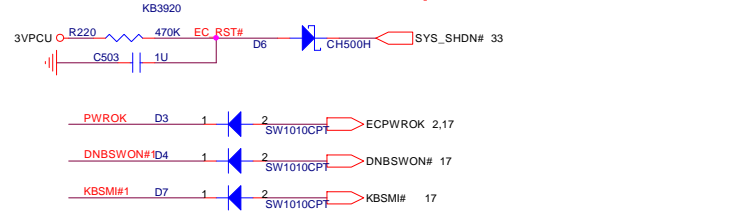
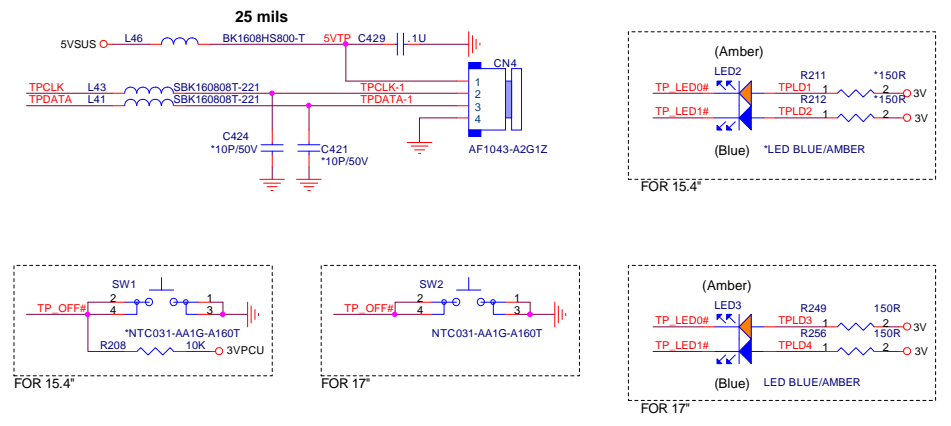
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 3264Hz clock in normal running
MY1	48	TP_PLL: DRLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISH flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



BIOS ROM



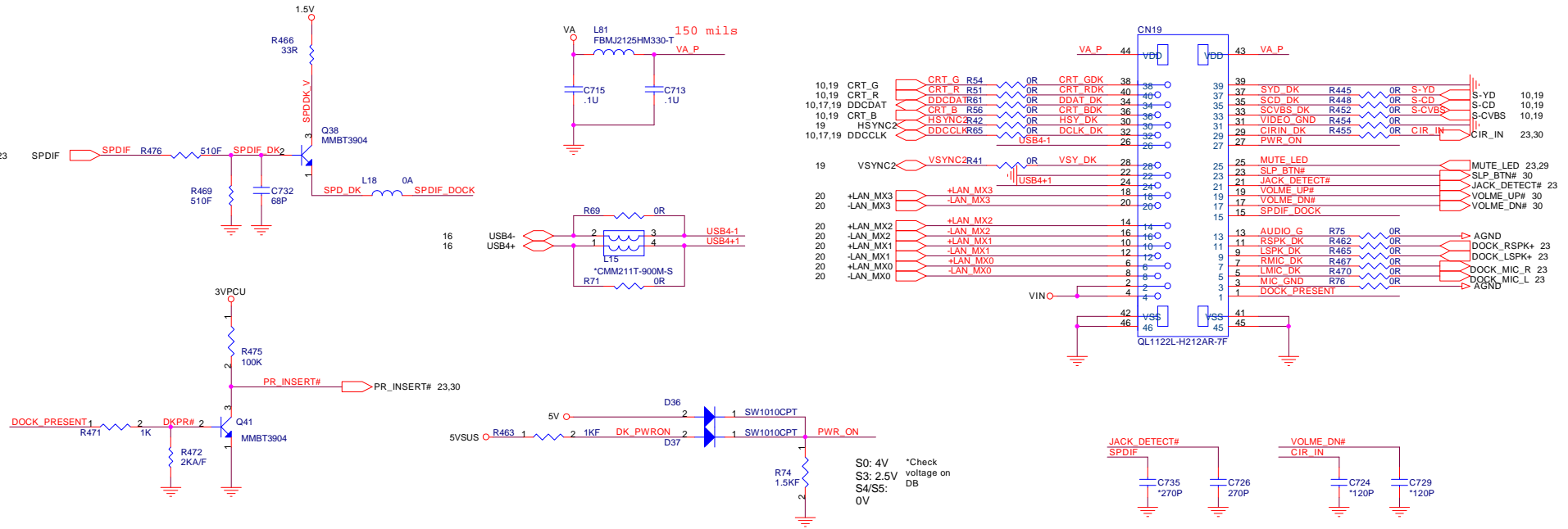
TOUCH PAD CONNECTOR



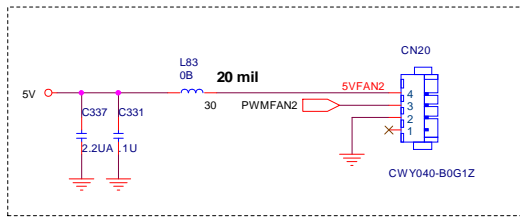
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number KB3920	Rev 1A
Date: Thursday, December 29, 2005 Sheet 30 of 38		

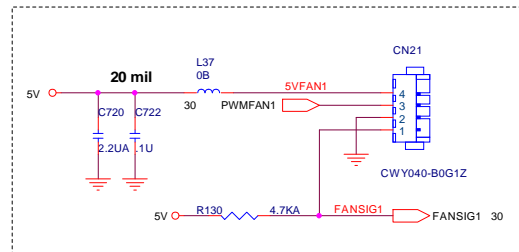
CABLE DOCK



FAN



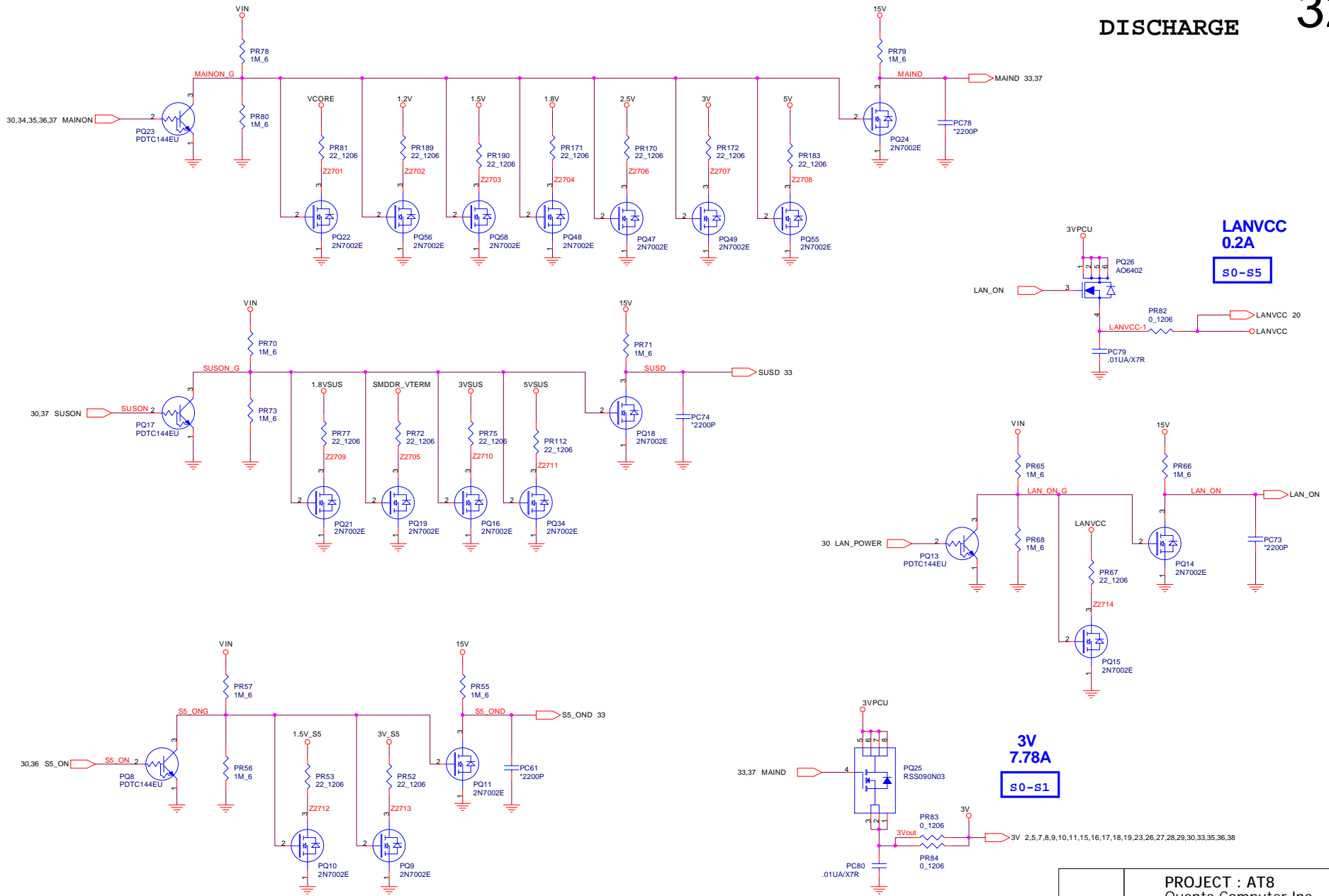
FAN2 PWM CONNECTOR



FAN1 PWM CONNECTOR

	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom	Document Number CABLE DOCKING
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DISCHARGE



LANVCC
0.2A
S0-S5

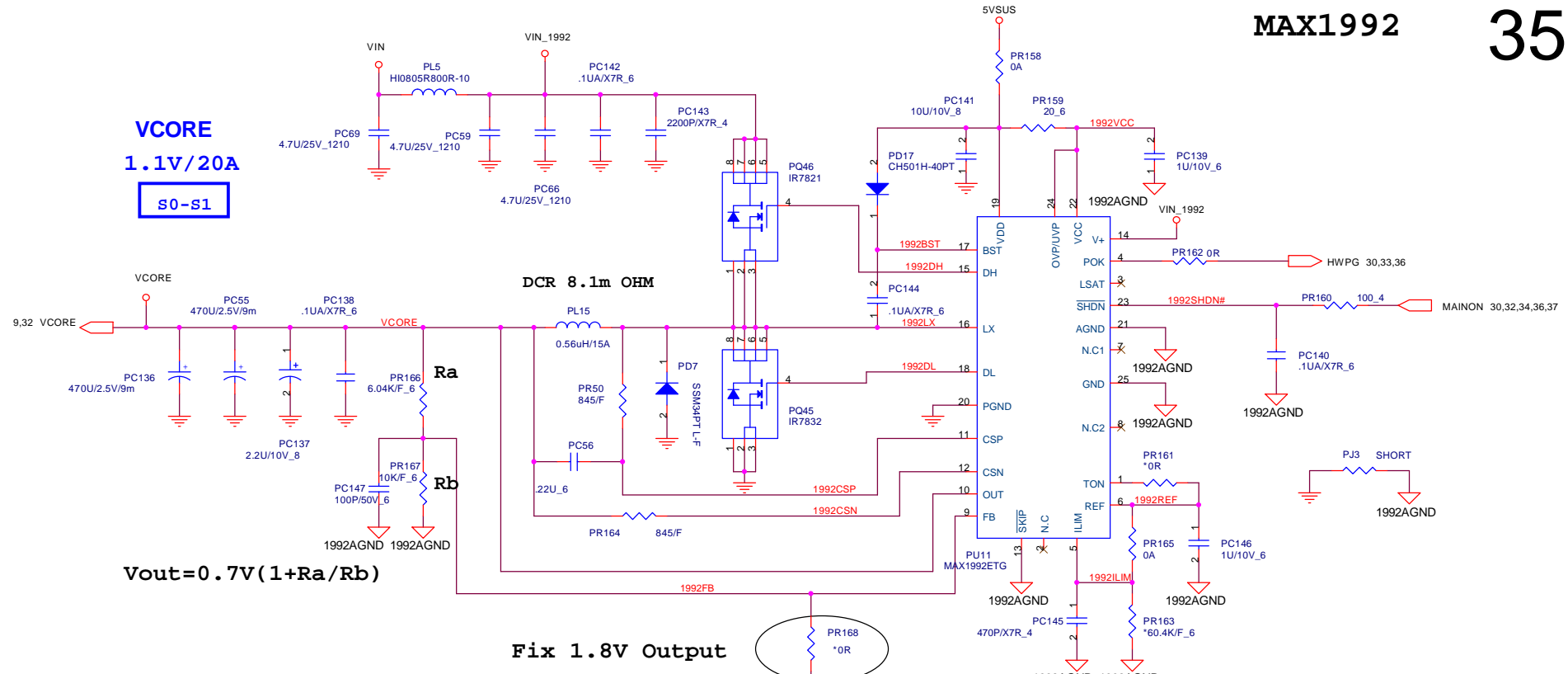
3V
7.78A
S0-S1

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VCORE

1.1V/20A

S0-S1

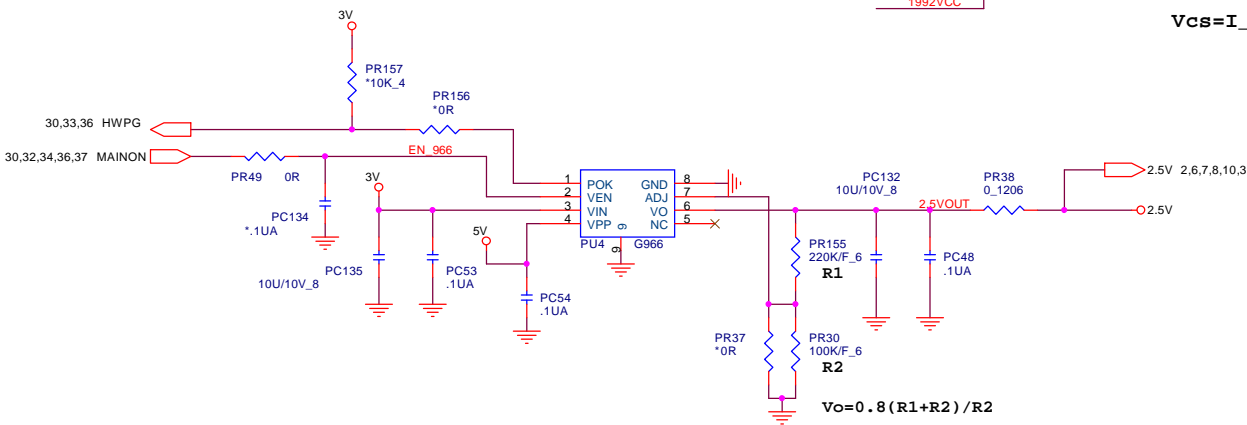


DCR 8.1m OHM

$V_{out} = 0.7V(1 + R_a/R_b)$

Fix 1.8V Output

$V_{cs} = I_L(A) * L_{DCR}(mOHM) = V_{ILIM}(mV) / 10$




2.5V

0.88A

S0-S1

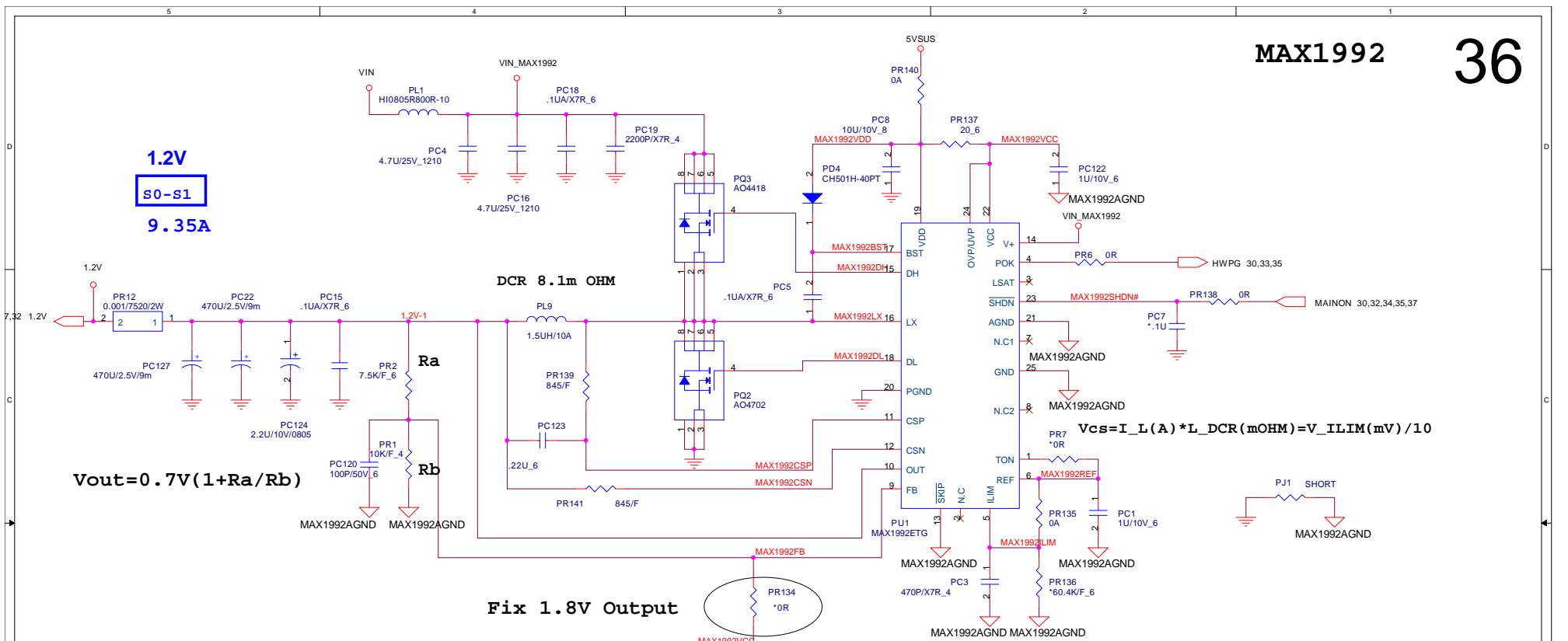
$V_o = 0.8(R1 + R2) / R2$

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1.2V

S0-S1

9.35A

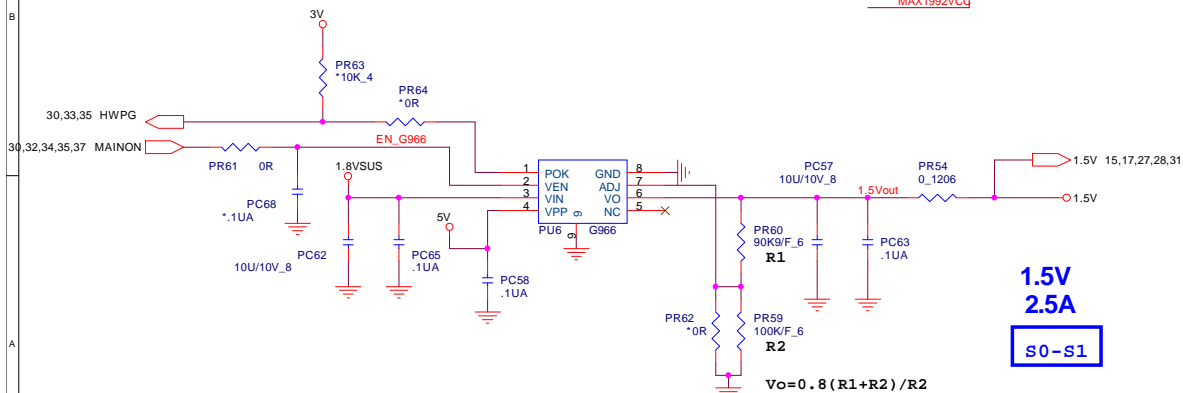


$V_{out} = 0.7V(1 + R_a/R_b)$

DCR 8.1m OHM

$V_{cs} = I_{L(A)} * L_{DCR(mOHM)} = V_{ILIM(mV)} / 10$

Fix 1.8V Output



1.5V
2.5A

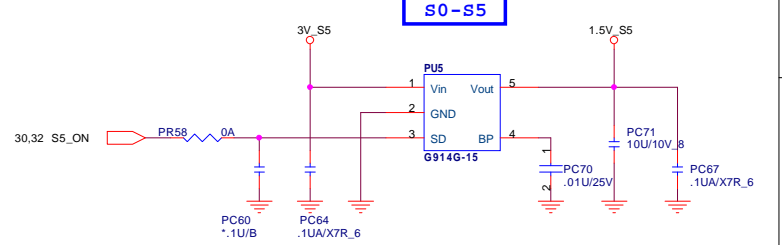
S0-S1

$V_o = 0.8(R_1 + R_2) / R_2$

1.5V_S5

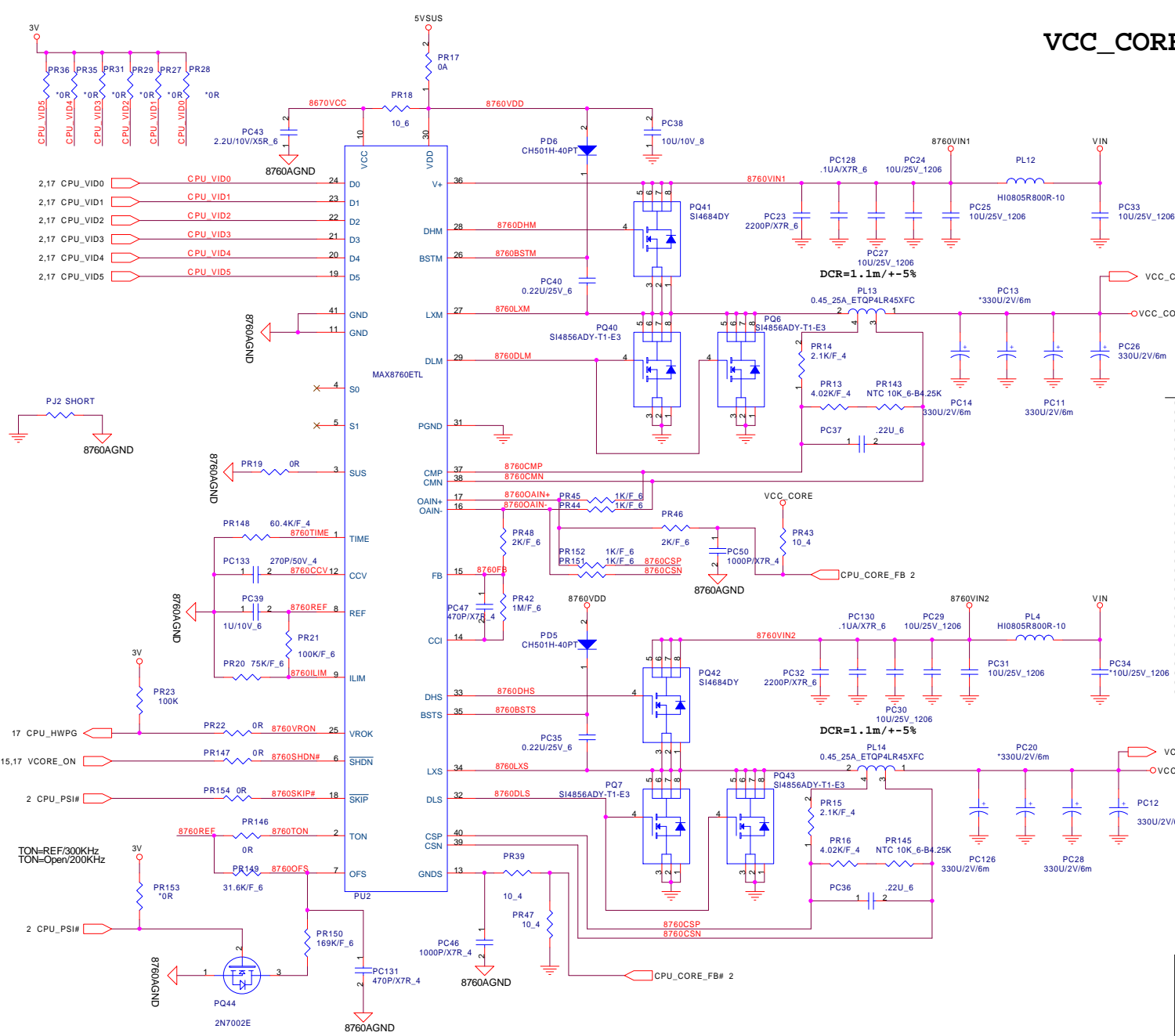
0.2A

S0-S5




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VCC_CORE



OCP=?A
VCC_CORE
35A / 1.05V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	1	0	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	1	0	1	0	0.7000V
0	0	0	1	1	0	1.4000V	1	0	1	0	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	1	0	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V



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