AT6 BLOCK DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU
Yonah/Merom
479P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS954206AG
56pins
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

HyperThansport I/O BUS

NORTH BRIDGE
Calistoga
945PM/GM/GMZ
1466p BGA
PAG 6,7,8,9,10,11

DDRII-SODIMM1
PAG 12,13
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 12,13
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 14,15,16,17,18,19

Option for 17" only
HDMI CON
PAG 20

TV_OUT
CRT_OUT

CRT/S-VIDEO
PAG 25

LVDS(2 Channel)

Panel Connector
15" / 17" PAG 20

DMI LINK

NBSRCCLK, NBSRCCLK#

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

SOUTH BRIDGE
ICH-7m
82801GBM
652P BGA
PAG 21,22,23,24

USB2.0

Bluetooth PAG 35 (5)
USB2.0 I/O Ports X3 PAG 31 (0,1,2)
Camera X1 PAG 28 (3)
Mini PCI-E Card x1 (4,6,7)
Express Card x1
Cable Docking x1

PCI BUS / 33MHz
PCI-E
Azalia

Option for 17" only
SATA - HDD PAG 35
SATA2

SATA - HDD PAG 31
SATA0 150MB

PATA- CD-ROM PAG 31
PATA *(66/100/133)*

LPC

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 32

LAN
Intel Ekron 82562GT/82573L 10/100/GagaLAN
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 26,27

Conexant
Venice AMOM
CX20549-12
PAG 28

Two-element microphone PAG 28

Audio Jacks (Phone/SPDIF/MIC) PAG 28

SIM CARD PAG 32

RJ45 PAG 33

IEEE1394 CONN PAG 26

Memory CardReader PAG 27

ENE KBC
KB3920 Bx
PAG 37

Keyboard Touch Pad PAG 36

CIR PAG 36

Capacitive Sense SW PAG 36

X-Bus

FAN PAG 38

Flash PAG 37

AUDIO Amplifier PAG 30

Jack to Speaker PAG 30

MDC DAA PAG 29

MODEM RJ 11 PAG 33

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

SYSTEM CHARGER(MAX8724) PAG 39

SYSTEM POWER MAX8743A PAG 40

DDR II SMDDR_VTERM 1.8V/1.8VSUS(MAX8632) PAG 41

VCCP +1.5V AND GMCH 1.05V(MAX8743) PAG 42

VGACORE(1.025V)MAX1992 PAG 43

CPU CORE MAX8771 PAG 44

NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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FSC	FSB	FSA	CPU	SRC	PCI	DOT
1	0	1	100	100	33	96
0	0	1	133	100	33	96
0	1	1	166	100	33	96
0	1	0	200	100	33	96
0	0	0	266	100	33	96
1	0	0	333	100	33	96
1	1	0	400	100	33	96
1	1	1	200	100	33	96

02

25 mils

Close to IC <500mils

Place these termination to close CK410M.

MV_Change to CH6102M9900

CK-410M

ICS954206AG-T

SMbus address D2 /IDT

CYP CY28442 /56pins
ICS954206AGT /56pins

ITP_EN=0 Assertion= SRC7

DREFSSCLK Frequency Select.
"0" : 96MHz "1" : 100MHz

FSB Frequency Select

FSB Freq (Mhz)	CPU DRIVEN (default)	R405=0 R406=1K R413=0 R414=1K R416=0 R417=1K
	533	R405=NO STUFF R409=56/F R413=NO STUFF R412=0 R416=NO STUFF R419=0
	667	R405=NO STUFF R409=56/F R413=NO STUFF R414=1K R416=NO STUFF R419=0

PROJECT : AT6
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	CLOCK GENERATOR	2A

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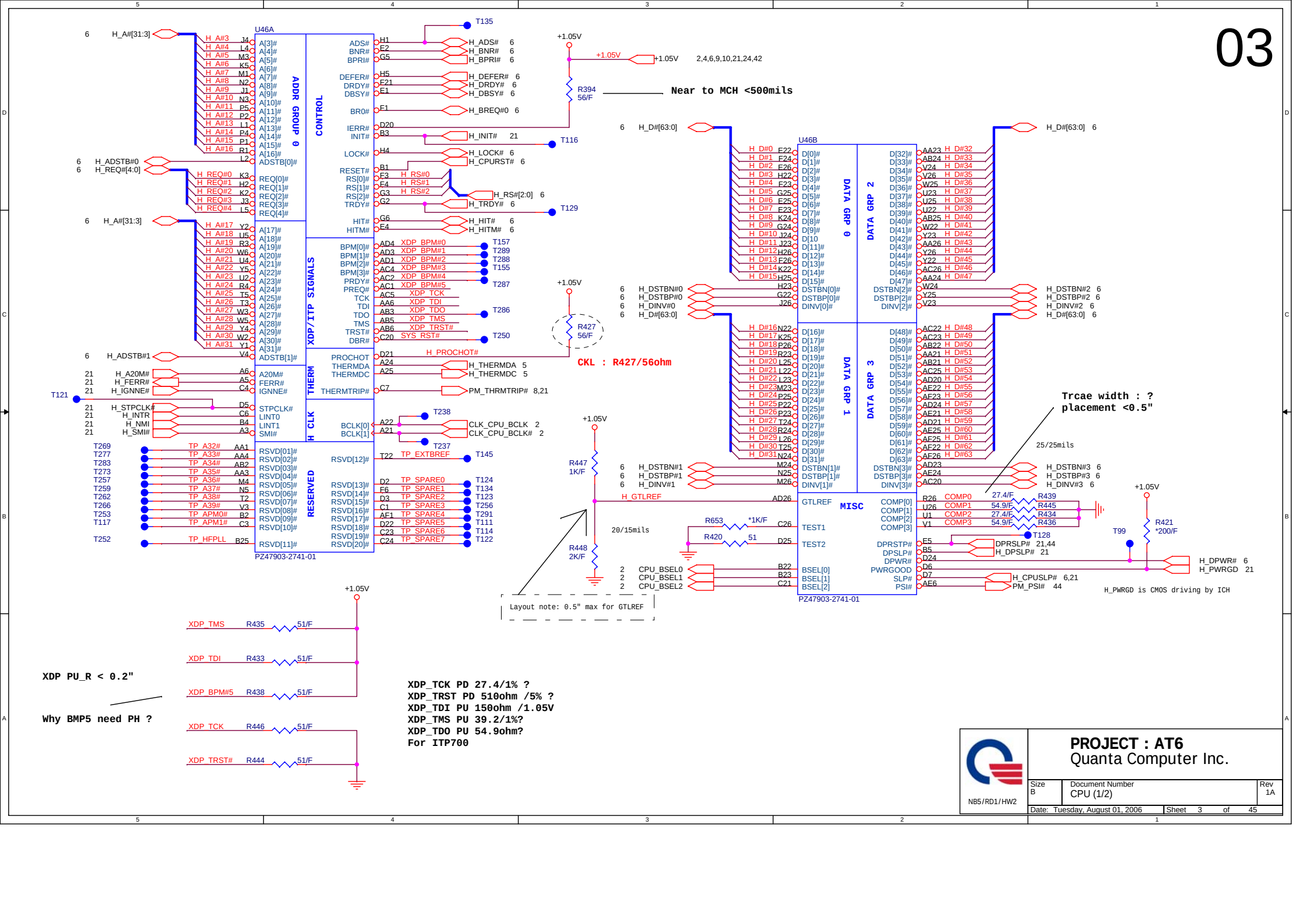
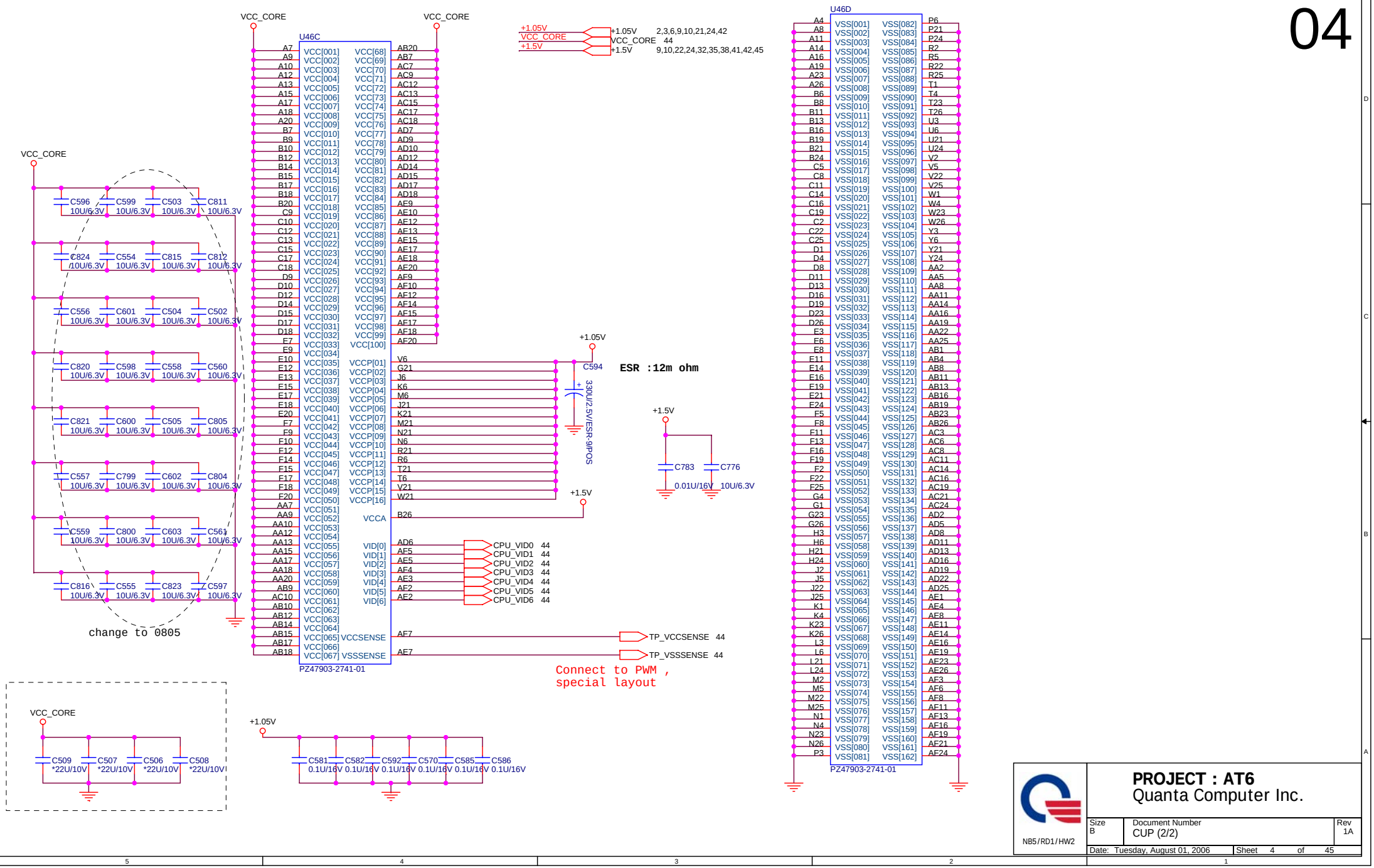
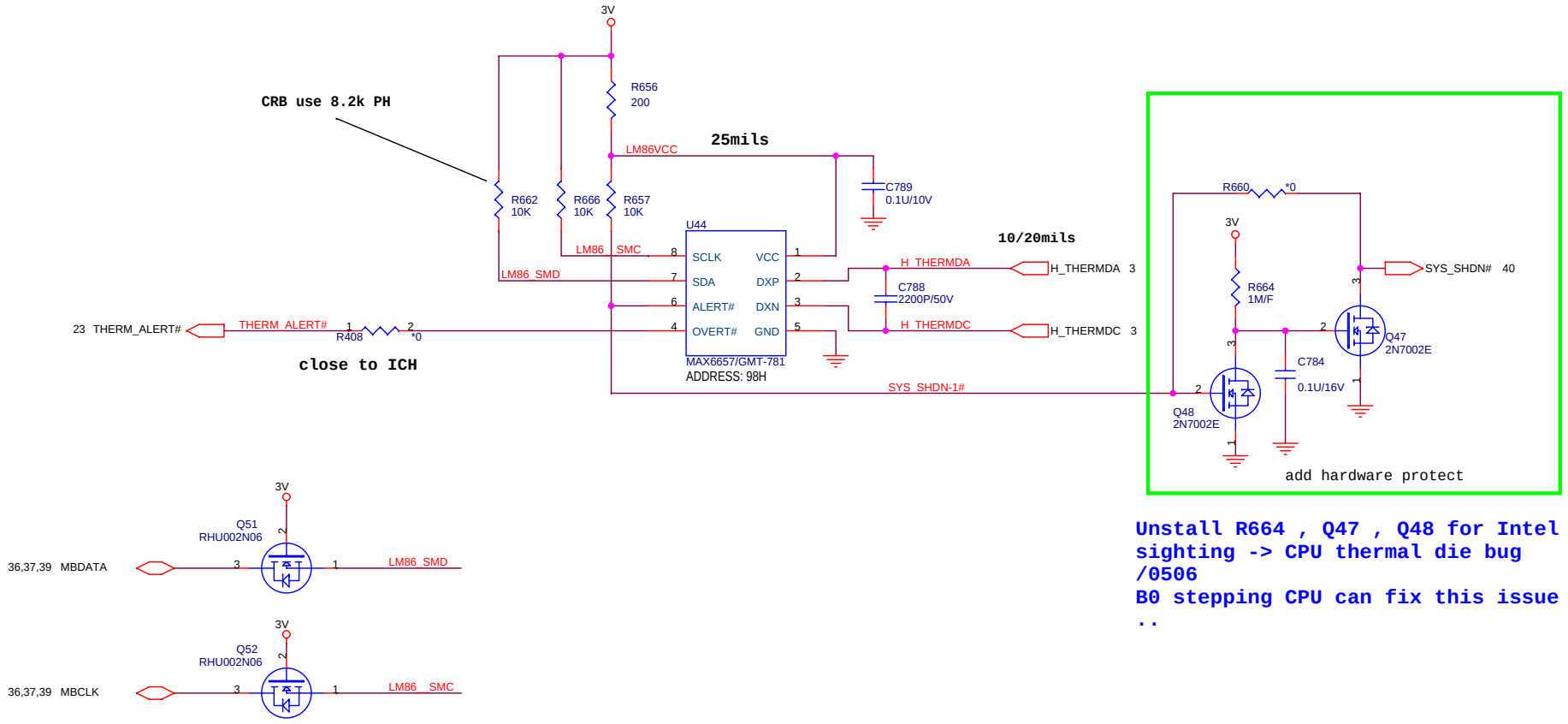
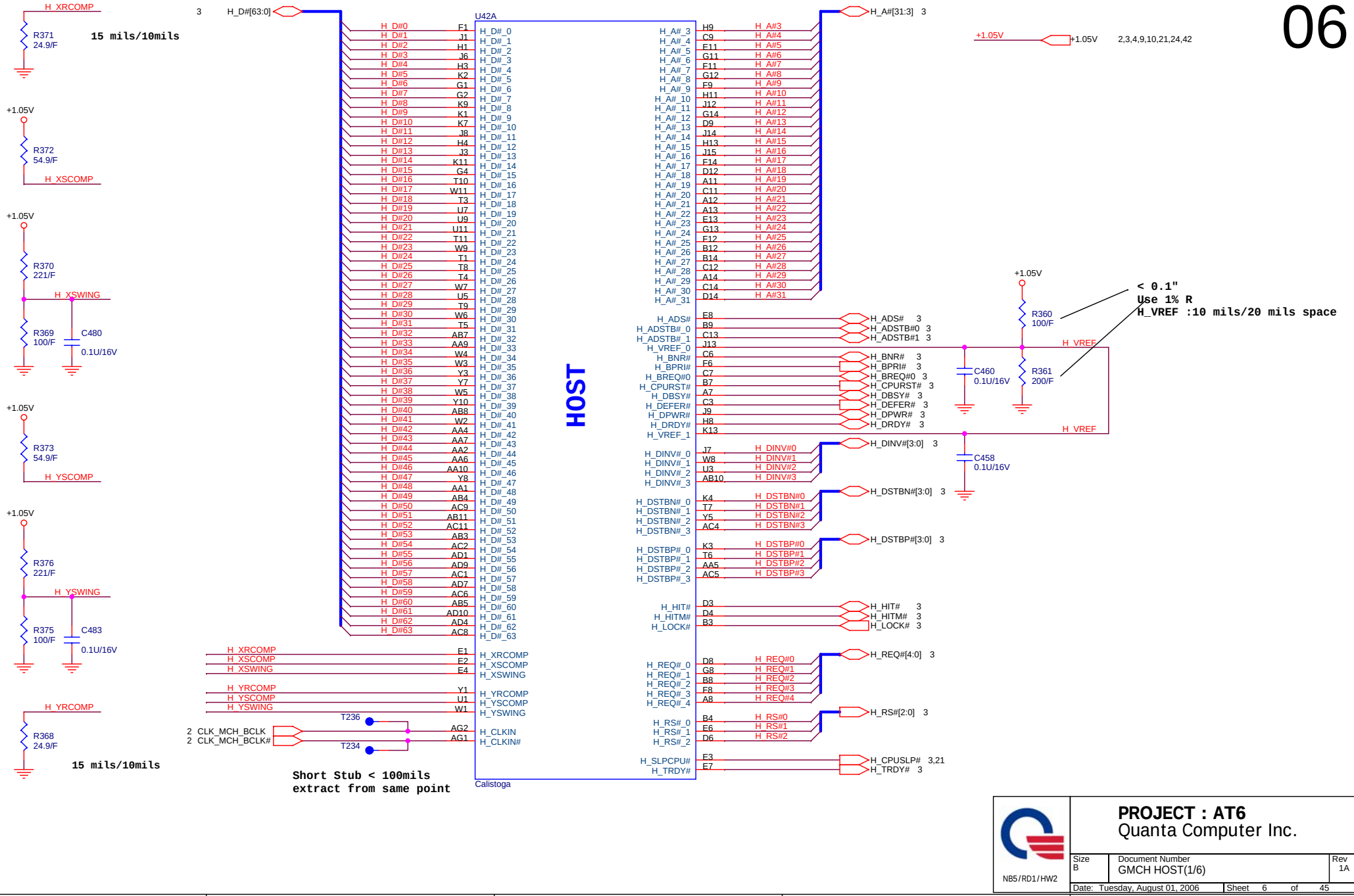

03
U46A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U46B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to MCH <500mils
CKL : R427/56ohm
Trcae width : ?
placement <0.5"
25/25mils
Layout note: 0.5" max for GTLREF
XDP PU_R < 0.2"
Why BMP5 need PH ?
XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700
H_PWRGD is CMOS driving by ICH
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size B
Document Number CPU (1/2)
Rev 1A
Date: Tuesday, August 01, 2006
Sheet 3 of 45


04
VCC_CORE
U46C
PZ47903-2741-01
U46D
PZ47903-2741-01
+1.05V
+1.5V
C594
330U/2.5V/ESR-9/POS
ESR :12m ohm
C783
C776
0.01U/16V
10U/6.3V
change to 0805
TP_VCCSENSE 44
TP_VSSSENSE 44
Connect to PWM , special layout
CPU_VID0 44
CPU_VID1 44
CPU_VID2 44
CPU_VID3 44
CPU_VID4 44
CPU_VID5 44
CPU_VID6 44
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size B
Document Number CUP (2/2)
Rev 1A
Date: Tuesday, August 01, 2006
Sheet 4 of 45



Unstall R664 , Q47 , Q48 for Intel sighting -> CPU thermal die bug /0506
B0 stepping CPU can fix this issue ..

NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.	
Size B	Document Number THERMAL LM86	Rev 2A
Date: Tuesday, August 01, 2006	Sheet 5 of 45	


06
H_XRCOMP
R371
24.9/F
15 mils/10mils
+1.05V
R372
54.9/F
H_XSCOMP
+1.05V
R370
221/F
H_XSWING
R369
100/F
C480
0.1U/16V
+1.05V
R373
54.9/F
H_YSCOMP
+1.05V
R376
221/F
H_YSWING
R375
100/F
C483
0.1U/16V
H_YRCOMP
R368
24.9/F
15 mils/10mils
3 H_D#[63:0]
U42A
HOST
Calistoga
H_D#0 F1 H_D#_0
H_D#1 J1 H_D#_1
H_D#2 H1 H_D#_2
H_D#3 J6 H_D#_3
H_D#4 H3 H_D#_4
H_D#5 K2 H_D#_5
H_D#6 G1 H_D#_6
H_D#7 G2 H_D#_7
H_D#8 K9 H_D#_8
H_D#9 K1 H_D#_9
H_D#10 K7 H_D#_10
H_D#11 J8 H_D#_11
H_D#12 H4 H_D#_12
H_D#13 J3 H_D#_13
H_D#14 K11 H_D#_14
H_D#15 G4 H_D#_15
H_D#16 T10 H_D#_16
H_D#17 W11 H_D#_17
H_D#18 T3 H_D#_18
H_D#19 U7 H_D#_19
H_D#20 U9 H_D#_20
H_D#21 U11 H_D#_21
H_D#22 T11 H_D#_22
H_D#23 W9 H_D#_23
H_D#24 T1 H_D#_24
H_D#25 T8 H_D#_25
H_D#26 T4 H_D#_26
H_D#27 W7 H_D#_27
H_D#28 U5 H_D#_28
H_D#29 T9 H_D#_29
H_D#30 W6 H_D#_30
H_D#31 T5 H_D#_31
H_D#32 AB7 H_D#_32
H_D#33 AA9 H_D#_33
H_D#34 W4 H_D#_34
H_D#35 W3 H_D#_35
H_D#36 Y3 H_D#_36
H_D#37 Y7 H_D#_37
H_D#38 W5 H_D#_38
H_D#39 Y10 H_D#_39
H_D#40 AB8 H_D#_40
H_D#41 W2 H_D#_41
H_D#42 AA4 H_D#_42
H_D#43 AA7 H_D#_43
H_D#44 AA2 H_D#_44
H_D#45 AA6 H_D#_45
H_D#46 AA10 H_D#_46
H_D#47 Y8 H_D#_47
H_D#48 AA1 H_D#_48
H_D#49 AB4 H_D#_49
H_D#50 AC9 H_D#_50
H_D#51 AB11 H_D#_51
H_D#52 AC11 H_D#_52
H_D#53 AB3 H_D#_53
H_D#54 AC2 H_D#_54
H_D#55 AD1 H_D#_55
H_D#56 AD9 H_D#_56
H_D#57 AC1 H_D#_57
H_D#58 AD7 H_D#_58
H_D#59 AC6 H_D#_59
H_D#60 AB5 H_D#_60
H_D#61 AD10 H_D#_61
H_D#62 AD4 H_D#_62
H_D#63 AC8 H_D#_63
H_XRCOMP E1 H_XRCOMP
H_XSCOMP E2 H_XSCOMP
H_XSWING E4 H_XSWING
H_YRCOMP Y1 H_YRCOMP
H_YSCOMP U1 H_YSCOMP
H_YSWING W1 H_YSWING
T236
T234
2 CLK_MCH_BCLK AG2 H_CLKIN
2 CLK_MCH_BCLK# AG1 H_CLKIN#
Short Stub < 100mils
extract from same point
H_A#_3 H9 H_A#3
H_A#_4 C9 H_A#4
H_A#_5 E11 H_A#5
H_A#_6 G11 H_A#6
H_A#_7 F11 H_A#7
H_A#_8 G12 H_A#8
H_A#_9 F9 H_A#9
H_A#_10 H11 H_A#10
H_A#_11 J12 H_A#11
H_A#_12 G14 H_A#12
H_A#_13 D9 H_A#13
H_A#_14 J14 H_A#14
H_A#_15 H13 H_A#15
H_A#_16 J15 H_A#16
H_A#_17 F14 H_A#17
H_A#_18 D12 H_A#18
H_A#_19 A11 H_A#19
H_A#_20 C11 H_A#20
H_A#_21 A12 H_A#21
H_A#_22 A13 H_A#22
H_A#_23 E13 H_A#23
H_A#_24 G13 H_A#24
H_A#_25 F12 H_A#25
H_A#_26 B12 H_A#26
H_A#_27 B14 H_A#27
H_A#_28 C12 H_A#28
H_A#_29 A14 H_A#29
H_A#_30 C14 H_A#30
H_A#_31 D14 H_A#31
H_A#[31:3] 3
+1.05V +1.05V 2,3,4,9,10,21,24,42
H_ADS# E8 H_ADS# 3
H_ADSTB#_0 B9 H_ADSTB#0 3
H_ADSTB#_1 C13 H_ADSTB#1 3
H_VREF_0 J13
H_BNR# C6 H_BNR# 3
H_BPRI# F6 H_BPRI# 3
H_BREQ#0 C7 H_BREQ#0 3
H_CPURST# B7 H_CPURST# 3
H_DBSY# A7 H_DBSY# 3
H_DEFER# C3 H_DEFER# 3
H_DPWR# J9 H_DPWR# 3
H_DRDY# H8 H_DRDY# 3
H_VREF_1 K13
+1.05V
R360
100/F
H_VREF
C460
0.1U/16V
R361
200/F
H_VREF
C458
0.1U/16V
< 0.1"
Use 1% R
H_VREF :10 mils/20 mils space
H_DINV#_0 J7 H_DINV#0
H_DINV#_1 W8 H_DINV#1
H_DINV#_2 U3 H_DINV#2
H_DINV#_3 AB10 H_DINV#3
H_DINV#[3:0] 3
H_DSTBN#_0 K4 H_DSTBN#0
H_DSTBN#_1 T7 H_DSTBN#1
H_DSTBN#_2 Y5 H_DSTBN#2
H_DSTBN#_3 AC4 H_DSTBN#3
H_DSTBN#[3:0] 3
H_DSTBP#_0 K3 H_DSTBP#0
H_DSTBP#_1 T6 H_DSTBP#1
H_DSTBP#_2 AA5 H_DSTBP#2
H_DSTBP#_3 AC5 H_DSTBP#3
H_DSTBP#[3:0] 3
H_HIT# D3 H_HIT# 3
H_HITM# D4 H_HITM# 3
H_LOCK# B3 H_LOCK# 3
H_REQ#_0 D8 H_REQ#0
H_REQ#_1 G8 H_REQ#1
H_REQ#_2 B8 H_REQ#2
H_REQ#_3 F8 H_REQ#3
H_REQ#_4 A8 H_REQ#4
H_REQ#[4:0] 3
H_RS#_0 B4 H_RS#0
H_RS#_1 E6 H_RS#1
H_RS#_2 D6 H_RS#2
H_RS#[2:0] 3
H_SLPCPU# E3 H_CPUSLP# 3,21
H_TRDY# E7 H_TRDY# 3
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size B
Document Number GMCH HOST(1/6)
Rev 1A
Date: Tuesday, August 01, 2006
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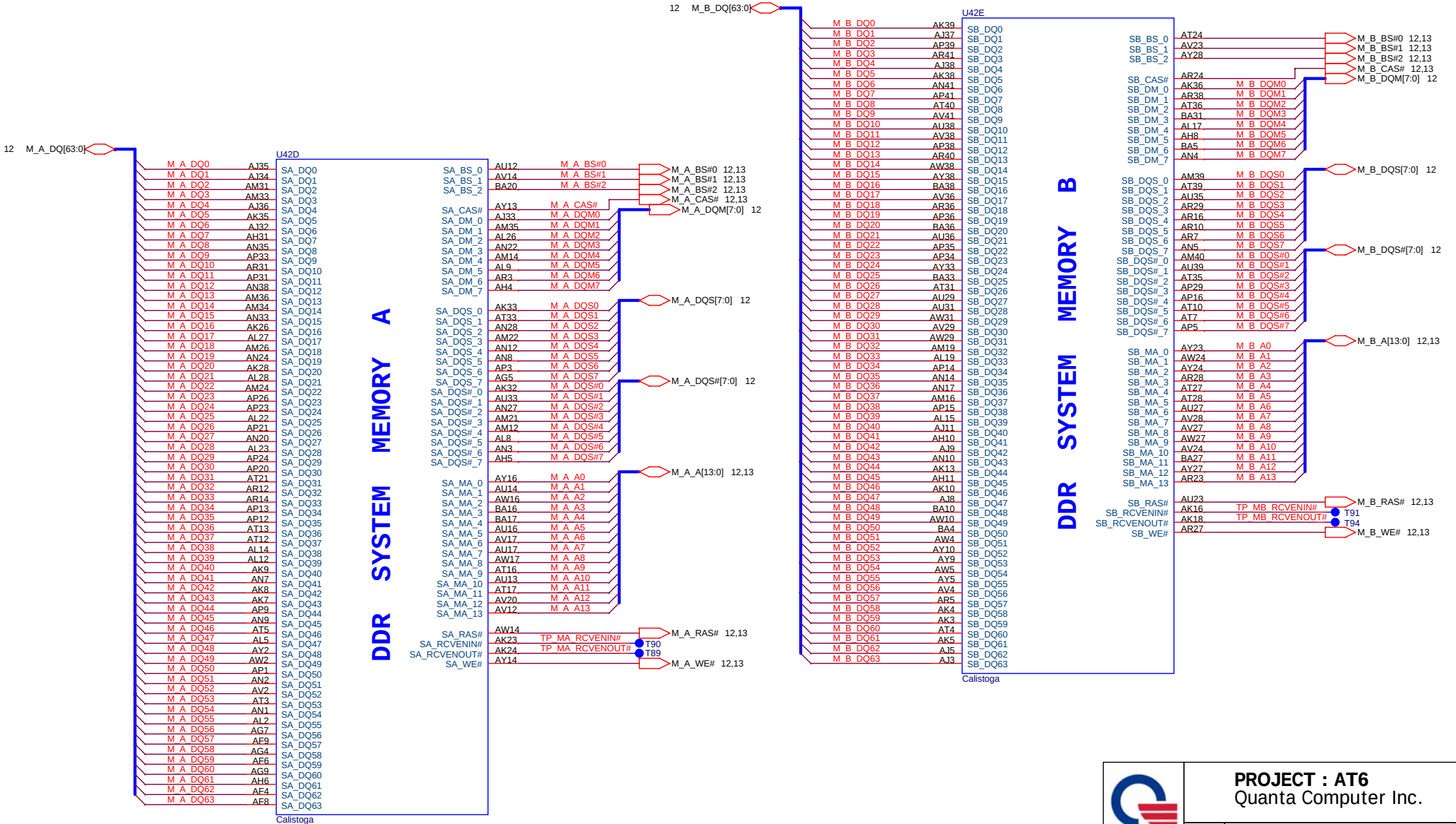
12 M_A_DQ[63:0]
U42D
DDR SYSTEM MEMORY A
SA_DQ0 AJ35
SA_DQ1 AJ34
SA_DQ2 AM31
SA_DQ3 AM33
SA_DQ4 AJ36
SA_DQ5 AK35
SA_DQ6 AJ32
SA_DQ7 AH31
SA_DQ8 AN35
SA_DQ9 AP33
SA_DQ10 AR31
SA_DQ11 AP31
SA_DQ12 AN38
SA_DQ13 AM36
SA_DQ14 AM34
SA_DQ15 AN33
SA_DQ16 AK26
SA_DQ17 AL27
SA_DQ18 AM26
SA_DQ19 AN24
SA_DQ20 AK28
SA_DQ21 AL28
SA_DQ22 AM24
SA_DQ23 AP26
SA_DQ24 AP23
SA_DQ25 AL22
SA_DQ26 AP21
SA_DQ27 AN20
SA_DQ28 AL23
SA_DQ29 AP24
SA_DQ30 AP20
SA_DQ31 AT21
SA_DQ32 AR12
SA_DQ33 AR14
SA_DQ34 AP13
SA_DQ35 AP12
SA_DQ36 AT13
SA_DQ37 AT12
SA_DQ38 AL14
SA_DQ39 AL12
SA_DQ40 AK9
SA_DQ41 AN7
SA_DQ42 AK8
SA_DQ43 AK7
SA_DQ44 AP9
SA_DQ45 AN9
SA_DQ46 AT5
SA_DQ47 AL5
SA_DQ48 AY2
SA_DQ49 AW2
SA_DQ50 AP1
SA_DQ51 AN2
SA_DQ52 AV2
SA_DQ53 AT3
SA_DQ54 AN1
SA_DQ55 AL2
SA_DQ56 AG7
SA_DQ57 AF9
SA_DQ58 AG4
SA_DQ59 AF6
SA_DQ60 AG9
SA_DQ61 AH6
SA_DQ62 AF4
SA_DQ63 AF8
Calistoga
SA_BS_0 AU12
SA_BS_1 AV14
SA_BS_2 BA20
SA_CAS# AY13
SA_DM_0 AJ33
SA_DM_1 AM35
SA_DM_2 AL26
SA_DM_3 AN22
SA_DM_4 AM14
SA_DM_5 AL9
SA_DM_6 AR3
SA_DM_7 AH4
SA_DQS_0 AK33
SA_DQS_1 AT33
SA_DQS_2 AN28
SA_DQS_3 AM22
SA_DQS_4 AN12
SA_DQS_5 AN8
SA_DQS_6 AP3
SA_DQS_7 AG5
SA_DQS#_0 AK32
SA_DQS#_1 AU33
SA_DQS#_2 AN27
SA_DQS#_3 AM21
SA_DQS#_4 AM12
SA_DQS#_5 AL8
SA_DQS#_6 AN3
SA_DQS#_7 AH5
SA_MA_0 AY16
SA_MA_1 AU14
SA_MA_2 AW16
SA_MA_3 BA16
SA_MA_4 BA17
SA_MA_5 AU16
SA_MA_6 AV17
SA_MA_7 AU17
SA_MA_8 AW17
SA_MA_9 AT16
SA_MA_10 AU13
SA_MA_11 AT17
SA_MA_12 AV20
SA_MA_13 AV12
SA_RAS# AW14
SA_RCVENIN# AK23
SA_RCVENOUT# AK24
SA_WE# AY14
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_CAS#
M_A_DQM0
M_A_DQM1
M_A_DQM2
M_A_DQM3
M_A_DQM4
M_A_DQM5
M_A_DQM6
M_A_DQM7
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
M_A_DQS#0
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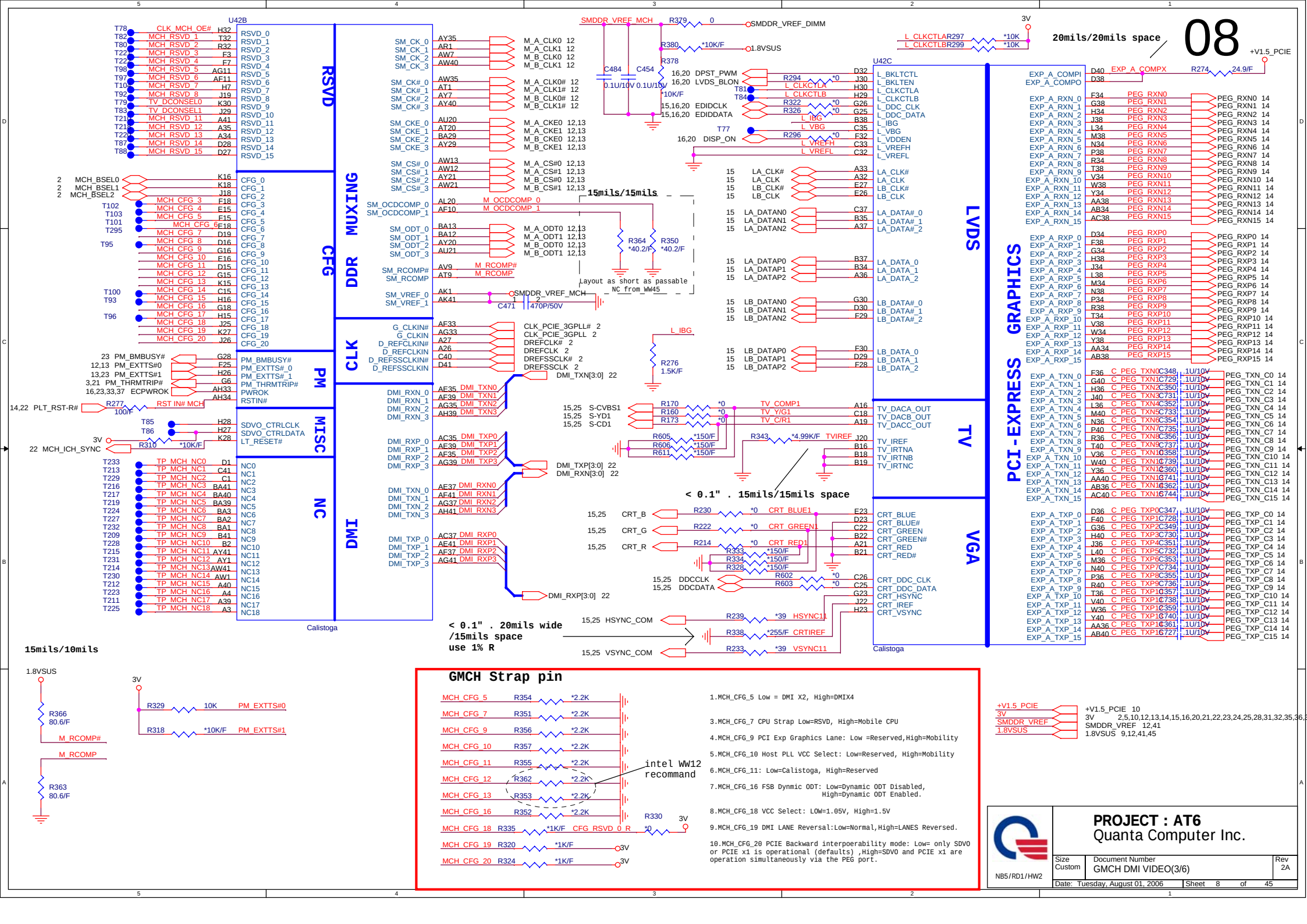
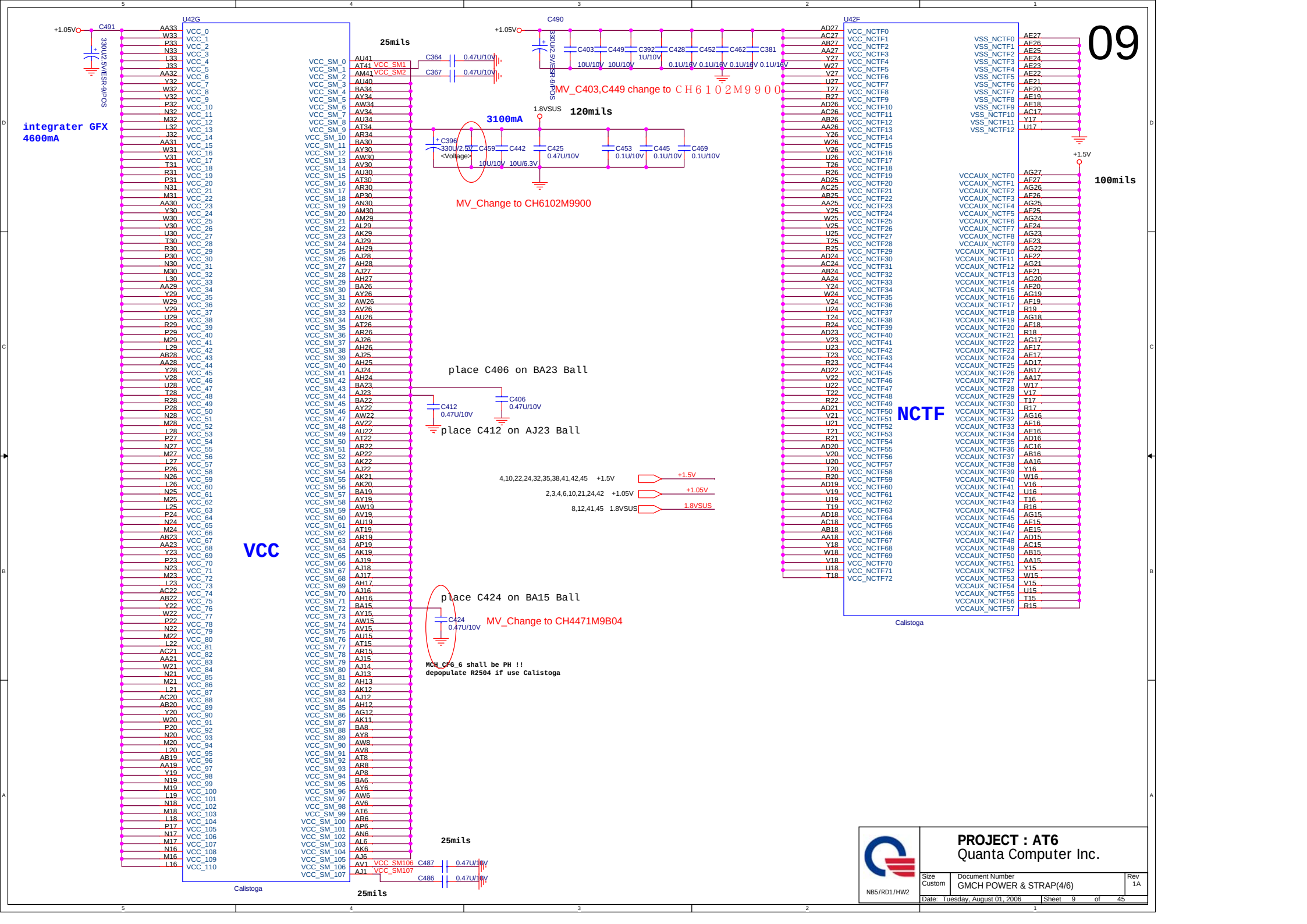
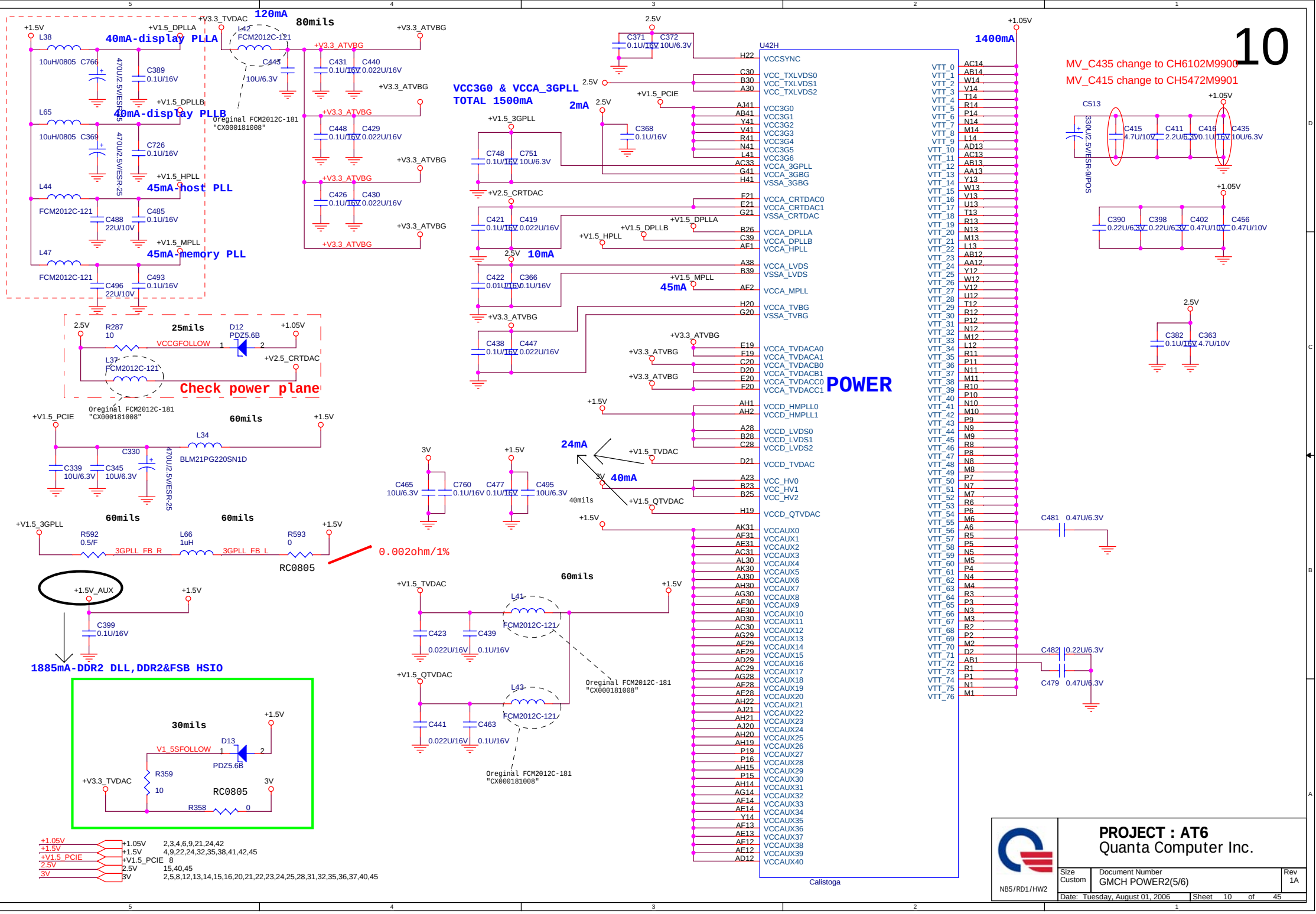
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
TP_MA_RCVENIN#
TP_MA_RCVENOUT#
T90
T89
M_A_BS#0 12,13
M_A_BS#1 12,13
M_A_BS#2 12,13
M_A_CAS# 12,13
M_A_DQM[7:0] 12
M_A_DQS[7:0] 12
M_A_DQS#[7:0] 12
M_A_A[13:0] 12,13
M_A_RAS# 12,13
M_A_WE# 12,13
12 M_B_DQ[63:0]
U42E
DDR SYSTEM MEMORY B
M_B_DQ0 AK39
M_B_DQ1 AJ37
M_B_DQ2 AP39
M_B_DQ3 AR41
M_B_DQ4 AJ38
M_B_DQ5 AK38
M_B_DQ6 AN41
M_B_DQ7 AP41
M_B_DQ8 AT40
M_B_DQ9 AV41
M_B_DQ10 AU38
M_B_DQ11 AV38
M_B_DQ12 AP38
M_B_DQ13 AR40
M_B_DQ14 AW38
M_B_DQ15 AY38
M_B_DQ16 BA38
M_B_DQ17 AV36
M_B_DQ18 AR36
M_B_DQ19 AP36
M_B_DQ20 BA36
M_B_DQ21 AU36
M_B_DQ22 AP35
M_B_DQ23 AP34
M_B_DQ24 AY33
M_B_DQ25 BA33
M_B_DQ26 AT31
M_B_DQ27 AU29
M_B_DQ28 AU31
M_B_DQ29 AW31
M_B_DQ30 AV29
M_B_DQ31 AW29
M_B_DQ32 AM19
M_B_DQ33 AL19
M_B_DQ34 AP14
M_B_DQ35 AN14
M_B_DQ36 AN17
M_B_DQ37 AM16
M_B_DQ38 AP15
M_B_DQ39 AL15
M_B_DQ40 AJ11
M_B_DQ41 AH10
M_B_DQ42 AJ9
M_B_DQ43 AN10
M_B_DQ44 AK13
M_B_DQ45 AH11
M_B_DQ46 AK10
M_B_DQ47 AJ8
M_B_DQ48 BA10
M_B_DQ49 AW10
M_B_DQ50 BA4
M_B_DQ51 AW4
M_B_DQ52 AY10
M_B_DQ53 AY9
M_B_DQ54 AW5
M_B_DQ55 AY5
M_B_DQ56 AV4
M_B_DQ57 AR5
M_B_DQ58 AK4
M_B_DQ59 AK3
M_B_DQ60 AT4
M_B_DQ61 AK5
M_B_DQ62 AJ5
M_B_DQ63 AJ3
Calistoga
SB_BS_0 AT24
SB_BS_1 AV23
SB_BS_2 AY28
SB_CAS# AR24
SB_DM_0 AK36
SB_DM_1 AR38
SB_DM_2 AT36
SB_DM_3 BA31
SB_DM_4 AL17
SB_DM_5 AH8
SB_DM_6 BA5
SB_DM_7 AN4
SB_DQS_0 AM39
SB_DQS_1 AT39
SB_DQS_2 AU35
SB_DQS_3 AR29
SB_DQS_4 AR16
SB_DQS_5 AR10
SB_DQS_6 AR7
SB_DQS_7 AN5
SB_DQS#_0 AM40
SB_DQS#_1 AU39
SB_DQS#_2 AT35
SB_DQS#_3 AP29
SB_DQS#_4 AP16
SB_DQS#_5 AT10
SB_DQS#_6 AT7
SB_DQS#_7 AP5
SB_MA_0 AY23
SB_MA_1 AW24
SB_MA_2 AY24
SB_MA_3 AR28
SB_MA_4 AT27
SB_MA_5 AT28
SB_MA_6 AU27
SB_MA_7 AV28
SB_MA_8 AV27
SB_MA_9 AW27
SB_MA_10 AV24
SB_MA_11 BA27
SB_MA_12 AY27
SB_MA_13 AR23
SB_RAS# AU23
SB_RCVENIN# AK16
SB_RCVENOUT# AK18
SB_WE# AR27
M_B_DQM0
M_B_DQM1
M_B_DQM2
M_B_DQM3
M_B_DQM4
M_B_DQM5
M_B_DQM6
M_B_DQM7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
TP_MB_RCVENIN#
TP_MB_RCVENOUT#
T91
T94
M_B_BS#0 12,13
M_B_BS#1 12,13
M_B_BS#2 12,13
M_B_CAS# 12,13
M_B_DQM[7:0] 12
M_B_DQS[7:0] 12
M_B_DQS#[7:0] 12
M_B_A[13:0] 12,13
M_B_RAS# 12,13
M_B_WE# 12,13
NB5/RD1/HW2
PROJECT : AT6
Quanta Computer Inc.
Size B
Document Number GMCH DDR(2/6)
Rev 1A
Date: Tuesday, August 01, 2006
Sheet 7 of 45


08
20mils/20mils space
U42B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
U42C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
15mils/15mils
Layout as short as passable
NC from WW45
< 0.1" . 15mils/15mils space
< 0.1" . 20mils wide
/15mils space
use 1% R
15mils/10mils
Calistoga
GMCH Strap pin
intel WW12
recommand
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled,
High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number GMCH DMI VIDEO(3/6)
Rev 2A
Date: Tuesday, August 01, 2006
Sheet 8 of 45


09
integrater GFX
4600mA
U42G
VCC
Calistoga
U42F
NCTF
Calistoga
+1.05V
C491
330U/2.5VESR-9/POS
C490
C403
C449
C392
C428
C452
C462
C381
10U/10V
1U/10V
0.1U/16V
MV_C403,C449 change to CH6102M9900
25mils
C364
C367
0.47U/10V
3100mA
120mils
1.8VSUS
C396
330U/2.5V
<Voltage>
C459
C442
C425
0.47U/10V
C453
C445
C469
0.1U/10V
10U/6.3V
MV_Change to CH6102M9900
place C406 on BA23 Ball
C412
C406
place C412 on AJ23 Ball
4,10,22,24,32,35,38,41,42,45 +1.5V
2,3,4,6,10,21,24,42 +1.05V
8,12,41,45 1.8VSUS
place C424 on BA15 Ball
C424
MV_Change to CH4471M9B04
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
25mils
C487
C486
100mils
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size
Custom
Document Number
GMCH POWER & STRAP(4/6)
Rev
1A
Date: Tuesday, August 01, 2006
Sheet 9 of 45

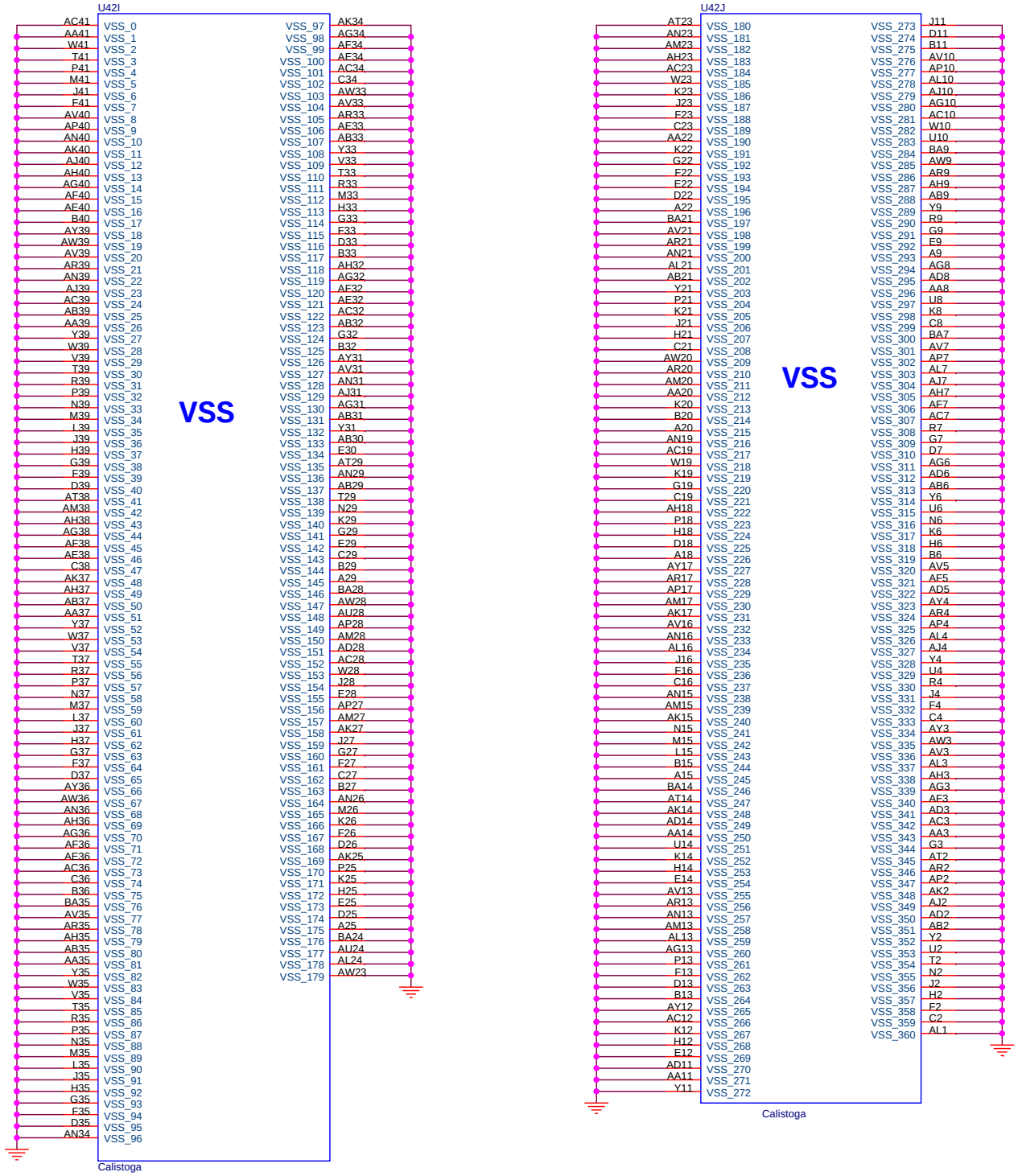


PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH POWER2(5/6)	1A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 Sheet 10 of 45



PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH GND (6/6)	1A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 | Sheet 11 of 45

CGCLK_SMB / CGDAT_SMB → CGCLK_SMB 2,13,32 / CGDAT_SMB 2,13,32

M_A_CKE[0..1] / M_A_CS#[0..1] → M_A_CKE[0..1] 8,13 / M_A_CS#[0..1] 8,13

M_A_RAS# → M_A_RAS# 7,13

M_A_CAS# → M_A_CAS# 7,13

M_A_WE# → M_A_WE# 7,13

M_A_CLK0 → M_A_CLK0 8

M_A_CLK0# → M_A_CLK0# 8

M_A_CLK1 → M_A_CLK1 8

M_A_CLK1# → M_A_CLK1# 8

M_A_BS#[0..2] → M_A_BS#[0..2] 7,13

M_A_ODT[0..1] → M_A_ODT[0..1] 8,13

M_A_DQM[0..7] → M_A_DQM[0..7] 7

M_A_DQ[0..63] → M_A_DQ[0..63] 7

M_A_DQS#[0..7] → M_A_DQS#[0..7] 7

M_A_A[13..0] → M_A_A[13..0] 7,13

M_B_CKE[0..1] / M_B_CS#[0..1] → M_B_CKE[0..1] 8,13 / M_B_CS#[0..1] 8,13

M_B_RAS# → M_B_RAS# 7,13

M_B_CAS# → M_B_CAS# 7,13

M_B_WE# → M_B_WE# 7,13

3V → 3V 2,5,8,10,13,14,15,16,20,21,22,23,24,25,28,31,32,35,36,37,40,45

1.8VSUS → 1.8VSUS 8,9,41,45

M_B_CLK0 → M_B_CLK0 8

M_B_CLK0# → M_B_CLK0# 8

M_B_CLK1 → M_B_CLK1 8

M_B_CLK1# → M_B_CLK1# 8

M_B_BS#[0..2] → M_B_BS#[0..2] 7,13

M_B_ODT[0..1] → M_B_ODT[0..1] 8,13

M_B_DQM[0..7] → M_B_DQM[0..7] 7

M_B_DQ[0..63] → M_B_DQ[0..63] 7

M_B_DQS[0..7] → M_B_DQS[0..7] 7

M_B_DQS#[0..7] → M_B_DQS#[0..7] 7

M_B_A[13..0] → M_B_A[13..0] 7,13

CKEA 0,1

H 9.2

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR

CN25A

CKEB 0,1

H 5.2

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR

CN24A

DIM2_SA0 R454 10K

DIM2_SA1 R455 10K 3V

SMbus address A4

R456 10K DIM1_SA0

R458 10K DIM1_SA1

SMbus address A0

SMDDR_VREF_DIMM

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR

CN25B

SMDDR_VREF_DIMM

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR

CN24B

C765 470P/50V

SMDDR_VREF_DIMM R365 0 SMDDR_VREF 41

R367 1.8VSUS

R617 *10K/F *10K/F

Place these Caps near So-Dimm1.

1.8VSUS

C794 2.2U/6.3V C817 2.2U/6.3V C801 2.2U/6.3V C553 2.2U/6.3V C792 2.2U/6.3V C810 0.1U/10V C797 0.1U/10V C568 0.1U/10V C543 0.1U/10V C790 0.1U/10V C803 0.1U/10V

SMDDR_VREF_DIMM

C768 0.1U/10V C772 2.2U/6.3V

3V

C618 2.2U/6.3V C617 0.1U/10V

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS

C802 2.2U/6.3V C813 2.2U/6.3V C793 2.2U/6.3V C809 2.2U/6.3V C798 2.2U/6.3V C796 2.2U/6.3V C808 0.1U/10V C791 0.1U/10V C530 0.1U/10V C795 0.1U/10V C818 0.1U/10V

SMDDR_VREF_DIMM

C472 0.1U/10V C468 2.2U/6.3V

3V

C619 2.2U/6.3V C621 0.1U/10V

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT6

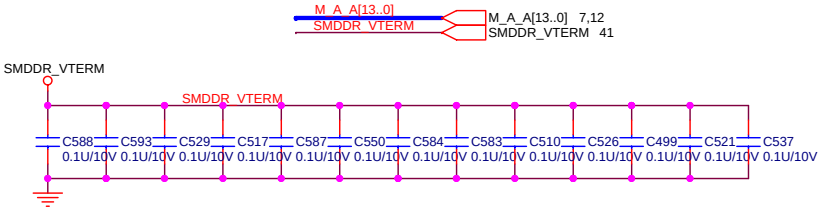
Quanta Computer Inc.

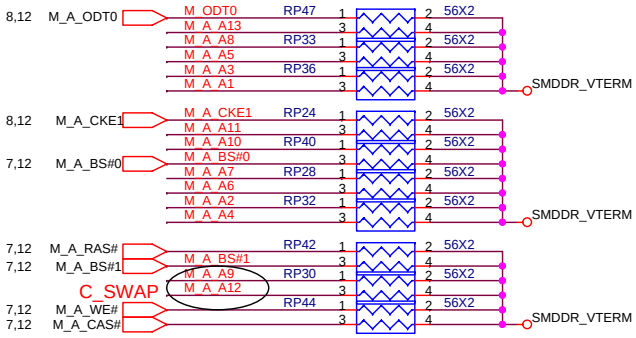
Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	2A

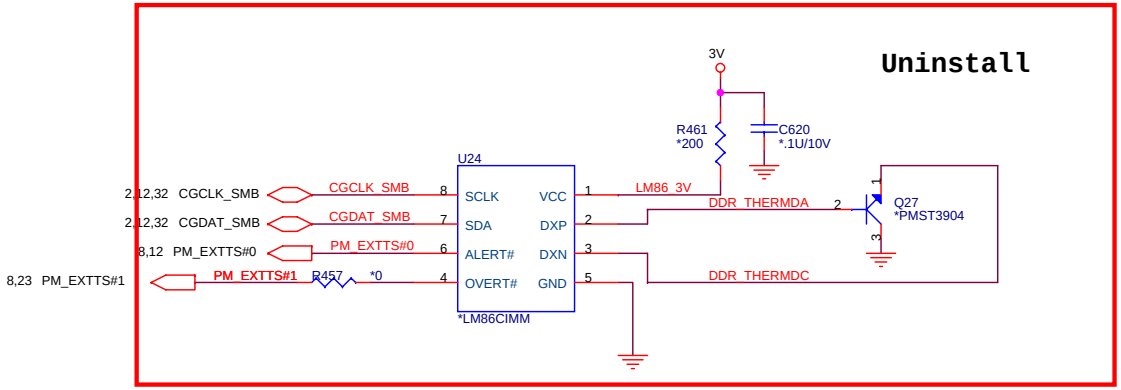
Date: Tuesday, August 01, 2006 Sheet 12 of 45

DDRII DUAL CHANNEL A,B.

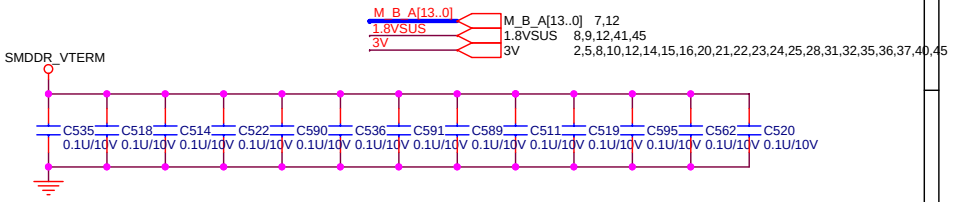
DDRII A CHANNEL



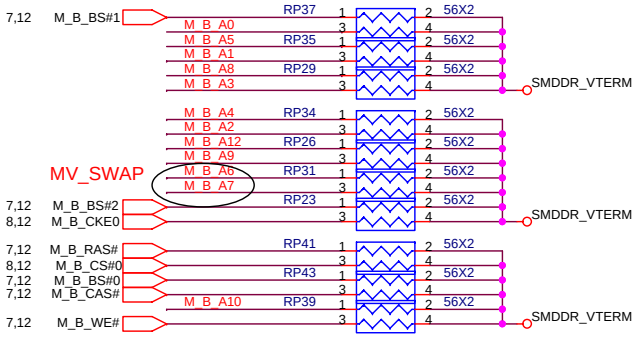


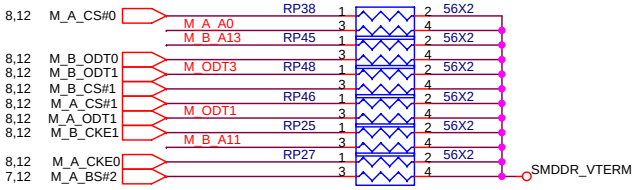


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.		
	Size: B	Document Number: DDRII RES.ARRAY	Rev: 1A
	Date: Tuesday, August 01, 2006	Sheet 13 of 45	

U37F

U_GPU_G3

U37A

PCIE

U_GPU_G3

500mA

1500mA

180mA

20mA

PLACE NEAR GPU

VGA1.2V

VGACORE

3V

For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.

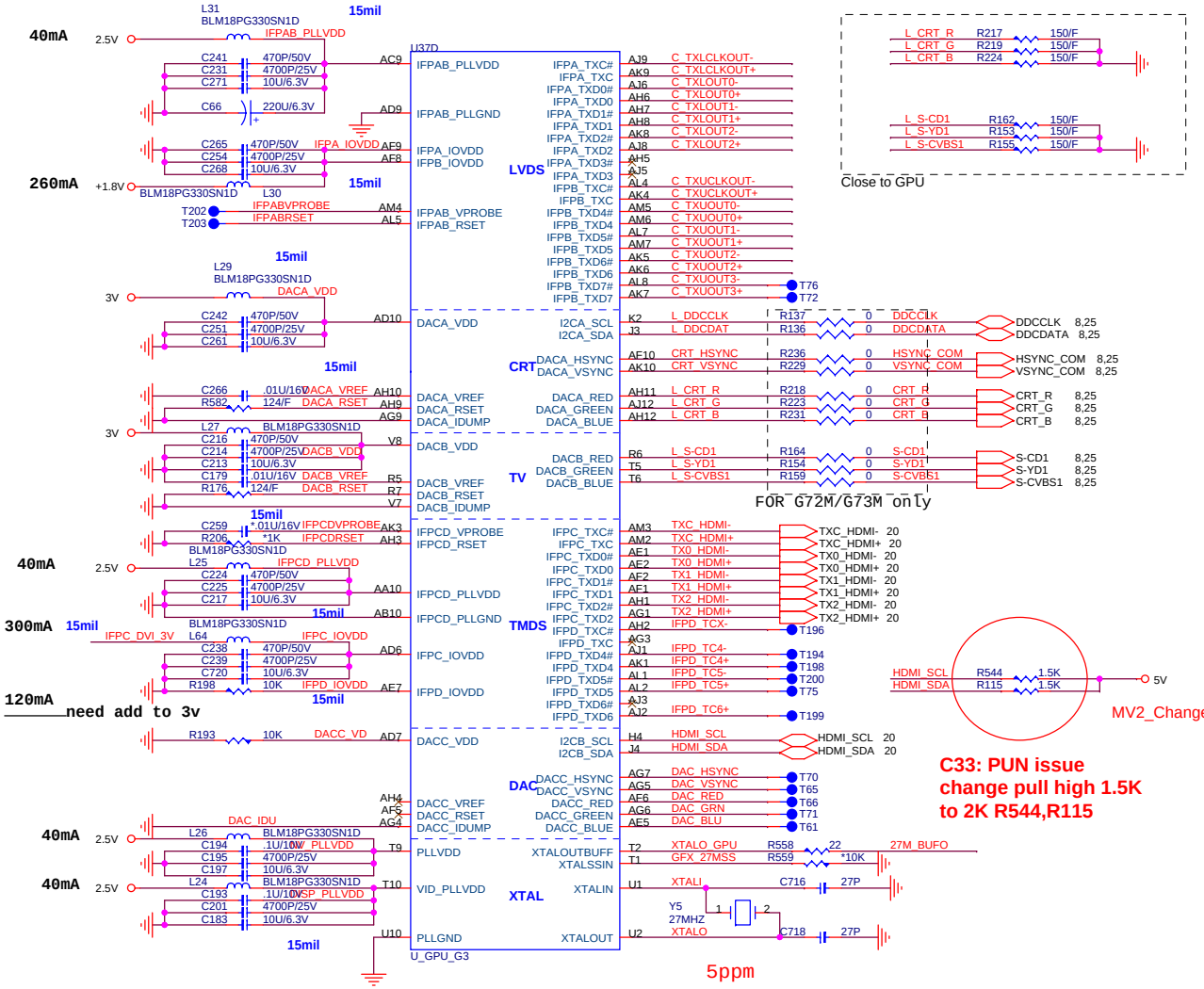
C1 : Bom change 10nh to 0 ohm R733

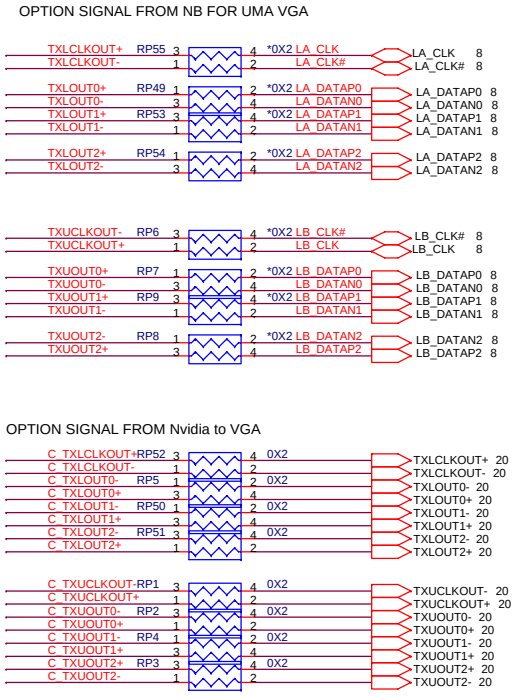
PROJECT : AT6
Quanta Computer Inc.

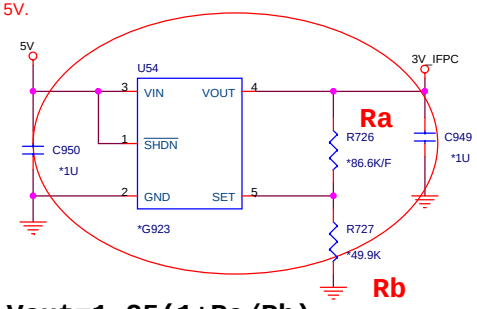
Size	Document Number	Rev
Custom	NVG73M (PCIE I/F)	1A

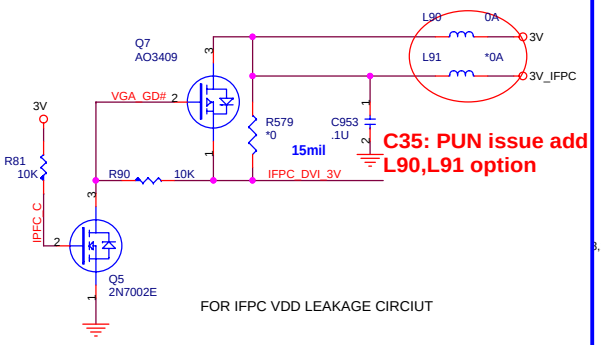
Date: Tuesday, August 01, 2006 Sheet 14 of 45

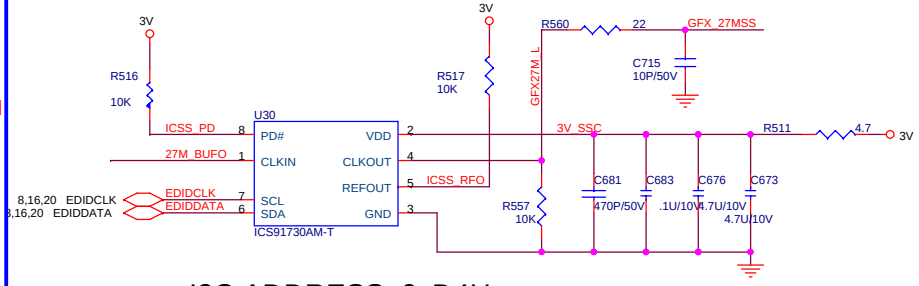
NB5/RD1/HW2









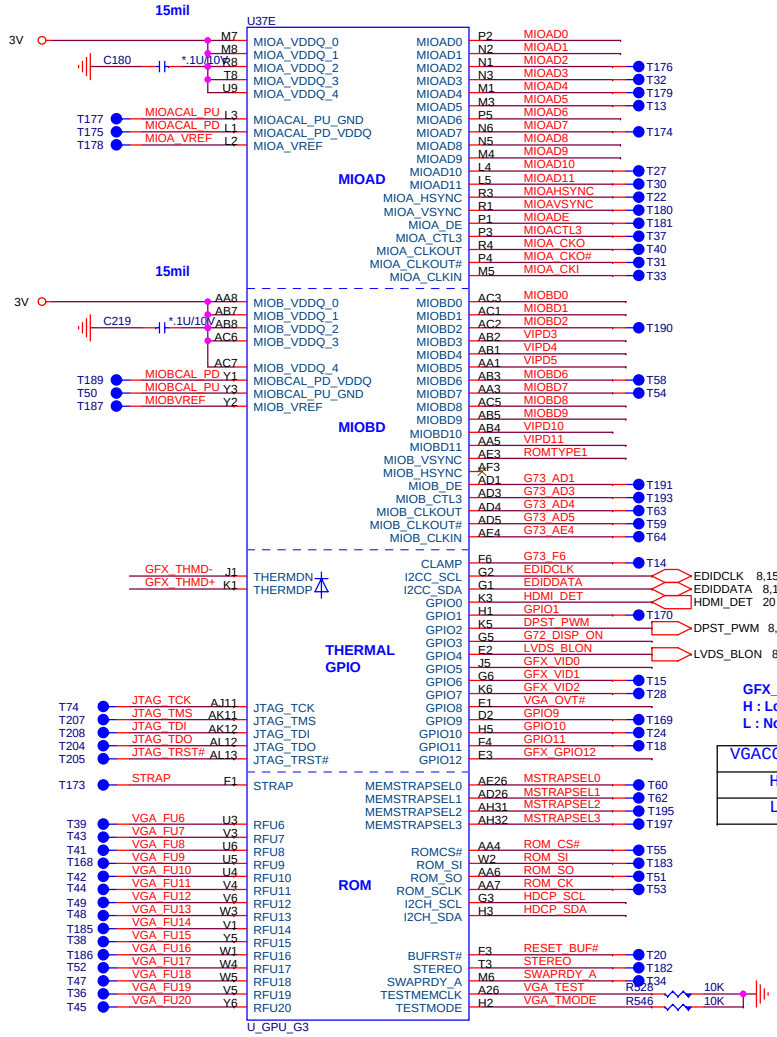


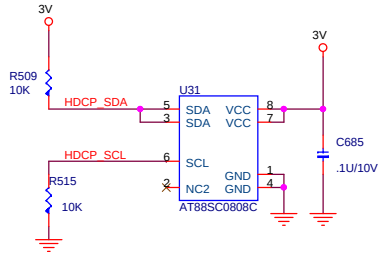
PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	2A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 | Sheet 15 of 45

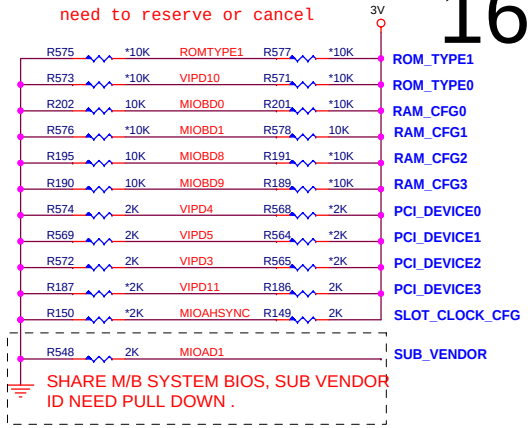


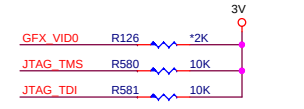


PCI DEVICE

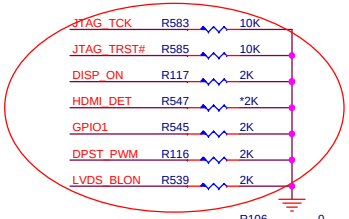
PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

need to reserve or cancel



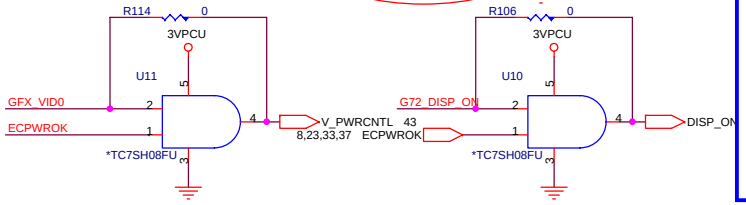


C36: PUN issue change pull down 10K to 2K
R117,R545,R116,R539



GFX_VID0
H : Low Voltage
L : Normal Voltage

VGACORECTL	G73M
HI	1.0V
LO	1.1V

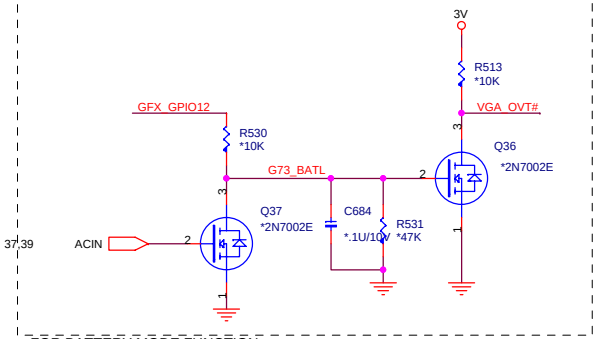


G72M VRAM Configuration Table

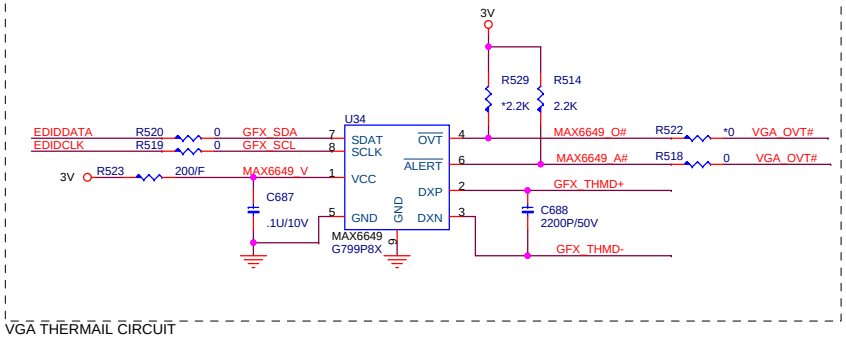
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

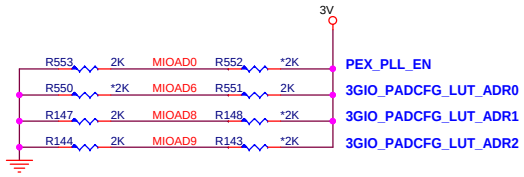
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



FOR BATTERY MODE FUNCTION
GFX_GPIO12=H ENABLE
GFX_GPIO12=L DISABLE



VGA THERMAIL CIRCUIT



PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (ROM/GPIO/STRAP)	2A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 | Sheet 16 of 45

Channel C is available on G73M only

U37B

VMA_DQ0 N27
VMA_DQ1 M27
VMA_DQ2 N28
VMA_DQ3 L29
VMA_DQ4 K27
VMA_DQ5 K28
VMA_DQ6 J29
VMA_DQ7 J28
VMA_DQ8 P30
VMA_DQ9 N31
VMA_DQ10 N30
VMA_DQ11 N32
VMA_DQ12 L31
VMA_DQ13 L30
VMA_DQ14 J30
VMA_DQ15 L32
VMA_DQ16 H30
VMA_DQ17 K30
VMA_DQ18 H31
VMA_DQ19 F30
VMA_DQ20 H32
VMA_DQ21 E31
VMA_DQ22 D30
VMA_DQ23 E30
VMA_DQ24 H28
VMA_DQ25 H29
VMA_DQ26 E29
VMA_DQ27 J27
VMA_DQ28 F27
VMA_DQ29 E27
VMA_DQ30 E28
VMA_DQ31 F28
VMA_DQ32 AD29
VMA_DQ33 AE29
VMA_DQ34 AD28
VMA_DQ35 AC28
VMA_DQ36 AB29
VMA_DQ37 AA30
VMA_DQ38 Y28
VMA_DQ39 AB30
VMA_DQ40 AM30
VMA_DQ41 AF30
VMA_DQ42 AJ31
VMA_DQ43 AJ30
VMA_DQ44 AJ32
VMA_DQ45 AK29
VMA_DQ46 AM31
VMA_DQ47 AL30
VMA_DQ48 AE32
VMA_DQ49 AF30
VMA_DQ50 AE31
VMA_DQ51 AD30
VMA_DQ52 AC31
VMA_DQ53 AC32
VMA_DQ54 AB32
VMA_DQ55 AB31
VMA_DQ56 AG27
VMA_DQ57 AF28
VMA_DQ58 AH28
VMA_DQ59 AG28
VMA_DQ60 AG29
VMA_DQ61 AD27
VMA_DQ62 AE27
VMA_DQ63 AE28

FBAD0 FBAD1 FBAD2 FBAD3 FBAD4 FBAD5 FBAD6 FBAD7 FBAD8 FBAD9 FBAD10 FBAD11 FBAD12 FBAD13 FBAD14 FBAD15 FBAD16 FBAD17 FBAD18 FBAD19 FBAD20 FBAD21 FBAD22 FBAD23 FBAD24 FBAD25 FBAD26 FBAD27 FBAD28 FBAD29 FBAD30 FBAD31 FBAD32 FBAD33 FBAD34 FBAD35 FBAD36 FBAD37 FBAD38 FBAD39 FBAD40 FBAD41 FBAD42 FBAD43 FBAD44 FBAD45 FBAD46 FBAD47 FBAD48 FBAD49 FBAD50 FBAD51 FBAD52 FBAD53 FBAD54 FBAD55 FBAD56 FBAD57 FBAD58 FBAD59 FBAD60 FBAD61 FBAD62 FBAD63

FBA

VMA_DM0 M29
VMA_DM1 M30
VMA_DM2 G30
VMA_DM3 F29
VMA_DM4 AA29
VMA_DM5 AK30
VMA_DM6 AC30
VMA_DM7 AG30

FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7

VMA_WDQS0 L28
VMA_WDQS1 K31
VMA_WDQS2 G32
VMA_WDQS3 G28
VMA_WDQS4 AB28
VMA_WDQS5 AL32
VMA_WDQS6 AF32
VMA_WDQS7 AH30

FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7

VMA_RDQS0 M28
VMA_RDQS1 K32
VMA_RDQS2 G31
VMA_RDQS3 G27
VMA_RDQS4 AA28
VMA_RDQS5 AL31
VMA_RDQS6 AE31
VMA_RDQS7 AH29

FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7

FB_VREF1 E32

+1.8V R540 *1K FB_VREF1 R541 *1K C701 *.1U/10V U_GPU_G3

15mil

G72: Stuff these parts
G73M : NC

FBVDD_0 A12
FBVDD_1 A15
FBVDD_2 A18
FBVDD_3 A21
FBVDD_4 A24
FBVDD_5 A27
FBVDD_6 A3
FBVDD_7 A30
FBVDD_8 A6
FBVDD_9 A9
FBVDD_10 AA32
FBVDD_11 AD32
FBVDD_12 AG32
FBVDD_13 AK32
FBVDD_14 C32
FBVDD_15 F32
FBVDD_16 J32
FBVDD_17 M32
FBVDD_18 R32
FBVDD_19 V32

C111 .1U/10V
C91 .1U/10V
C85 .1U/10V
C112 .1U/10V
C215 .47U/10V
C223 .47U/10V
C152 10U/4V
C105 .1U/10V
C110 .1U/10V
C181 .1U/10V
C88 .1U/10V
C145 .47U/10V
C107 .47U/10V
C178 10U/4V

+1.8V

PLACE NEAR GPU

FBVDDQ_0 AA25
FBVDDQ_1 AA26
FBVDDQ_2 AB25
FBVDDQ_3 AB26
FBVDDQ_4 G11
FBVDDQ_5 G12
FBVDDQ_6 G15
FBVDDQ_7 G18
FBVDDQ_8 G21
FBVDDQ_9 G22
FBVDDQ_10 H11
FBVDDQ_11 H12
FBVDDQ_12 H15
FBVDDQ_13 H18
FBVDDQ_14 H21
FBVDDQ_15 H22
FBVDDQ_16 L25
FBVDDQ_17 L26
FBVDDQ_18 M25
FBVDDQ_19 M26
FBVDDQ_20 R25
FBVDDQ_21 R26
FBVDDQ_22 V25
FBVDDQ_23 V26

C719 .1U/10V
C116 .1U/10V
C240 .1U/10V
C279 .1U/10V
C192 .47U/10V
C222 .47U/10V
C203 10U/4V
C226 .1U/10V
C174 .1U/10V
C92 .1U/10V
C128 .1U/10V
C144 .47U/10V
C182 .47U/10V
C94 10U/4V

+1.8V

PLACE NEAR GPU

C933 + 220U

FBA_CMD0 P32
FBA_CMD1 P31
FBA_CMD2 U30
FBA_CMD3 Y31
FBA_CMD4 W32
FBA_CMD5 W31
FBA_CMD6 T32
FBA_CMD7 V27
FBA_CMD8 T28
FBA_CMD9 T31
FBA_CMD10 U32
FBA_CMD11 W29
FBA_CMD12 W30
FBA_CMD13 T27
FBA_CMD14 V28
FBA_CMD15 V30
FBA_CMD16 U31
FBA_CMD17 R27
FBA_CMD18 V29
FBA_CMD19 T30
FBA_CMD20 W28
FBA_CMD21 R29
FBA_CMD22 R30
FBA_CMD23 P29
FBA_CMD24 U28
FBA_CMD25 Y32
FBA_CMD26

VMA_MA3 U27
VMA_MA0 U27
VMA_MA2 P31
VMA_MA1 U30
VMA_MA3H Y31
VMA_MA4H W32
VMA_MA5H W31
VMA_BA2 T32
VMA_CS0# V27
VMA_WE# T28
VMA_BA0 T31
VMA_CKE U32
VMA_RST# W29
VMA_MA2H W30
VMA_MA12 T27
VMA_RAS# V28
VMA_MA11 V30
VMA_MA10 U31
VMA_BA1 R27
VMA_MA8 V29
VMA_MA9 T30
VMA_MA6 W28
VMA_MA5 R29
VMA_MA7 R30
VMA_MA4 P29
VMA_CAS# U28
VMA_MA13 Y32

T184 T188

VMA_MA3 18
VMA_MA0 18
VMA_MA2 18
VMA_MA1 18
VMA_MA3H 18
VMA_MA4H 18
VMA_MA5H 18
VMA_CS0# 18
VMA_WE# 18
VMA_BA0 18
VMA_CKE 18
VMA_MA2H 18
VMA_MA12 18
VMA_RAS# 18
VMA_MA11 18
VMA_MA10 18
VMA_BA1 18
VMA_MA8 18
VMA_MA9 18
VMA_MA6 18
VMA_MA5 18
VMA_MA7 18
VMA_MA4 18
VMA_CAS# 18
VMA_MA13 18

FBA_CLK0 P28
FBA_CLK0# R28
FBA_CLK1 Y27
FBA_CLK1# AA27

VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#

VMA_CLK0 18
VMA_CLK0# 18
VMA_CLK1 18
VMA_CLK1# 18

RFU2 Y30
RFU3 AC26

G73_Y30 G73_AC26

T192 T57

FBA_DEBUG AC27

VMA_DEBUG

T46

FBA_REFCLK D32
FBA_REFCLK# D31

VMA_REFCK VMA_REFCK#

T163 T171

FBA_PLLVDD G23
FBA_PLLAVDD G25
FBA_PLLGND G24

G73_G23

T17

15mil

FBA_PLLAVDD

L23 BLM18PG330SN1D

VGA1.2V

C101 4700P/25V C93 47U/10V C141 *.1U/10V

C100 470P/50V

For EMI

VREF = FBVDDQ *
Rbot/(Rtop + Rbot)

U37C

VMC_DQ0 B7
VMC_DQ1 A7
VMC_DQ2 C7
VMC_DQ3 A2
VMC_DQ4 B2
VMC_DQ5 C4
VMC_DQ6 A5
VMC_DQ7 B5
VMC_DQ8 F9
VMC_DQ9 F10
VMC_DQ10 D12
VMC_DQ11 D9
VMC_DQ12 E12
VMC_DQ13 D11
VMC_DQ14 E8
VMC_DQ15 D8
VMC_DQ16 E7
VMC_DQ17 F7
VMC_DQ18 D6
VMC_DQ19 D5
VMC_DQ20 D3
VMC_DQ21 E4
VMC_DQ22 C3
VMC_DQ23 B4
VMC_DQ24 C10
VMC_DQ25 B10
VMC_DQ26 C8
VMC_DQ27 A10
VMC_DQ28 C11
VMC_DQ29 C12
VMC_DQ30 A11
VMC_DQ31 B11
VMC_DQ32 B28
VMC_DQ33 C27
VMC_DQ34 C26
VMC_DQ35 B26
VMC_DQ36 C30
VMC_DQ37 B31
VMC_DQ38 C29
VMC_DQ39 A31
VMC_DQ40 D28
VMC_DQ41 D27
VMC_DQ42 F26
VMC_DQ43 D24
VMC_DQ44 E23
VMC_DQ45 E26
VMC_DQ46 E24
VMC_DQ47 F23
VMC_DQ48 B23
VMC_DQ49 A23
VMC_DQ50 C25
VMC_DQ51 C23
VMC_DQ52 A22
VMC_DQ53 C22
VMC_DQ54 C21
VMC_DQ55 B22
VMC_DQ56 E22
VMC_DQ57 D22
VMC_DQ58 D21
VMC_DQ59 E21
VMC_DQ60 E18
VMC_DQ61 D19
VMC_DQ62 D18
VMC_DQ63 E19

FBCD0 FBCD1 FBCD2 FBCD3 FBCD4 FBCD5 FBCD6 FBCD7 FBCD8 FBCD9 FBCD10 FBCD11 FBCD12 FBCD13 FBCD14 FBCD15 FBCD16 FBCD17 FBCD18 FBCD19 FBCD20 FBCD21 FBCD22 FBCD23 FBCD24 FBCD25 FBCD26 FBCD27 FBCD28 FBCD29 FBCD30 FBCD31 FBCD32 FBCD33 FBCD34 FBCD35 FBCD36 FBCD37 FBCD38 FBCD39 FBCD40 FBCD41 FBCD42 FBCD43 FBCD44 FBCD45 FBCD46 FBCD47 FBCD48 FBCD49 FBCD50 FBCD51 FBCD52 FBCD53 FBCD54 FBCD55 FBCD56 FBCD57 FBCD58 FBCD59 FBCD60 FBCD61 FBCD62 FBCD63

FBC

VMC_DM0 A4
VMC_DM1 F11
VMC_DM2 E5
VMC_DM3 C9
VMC_DM4 C28
VMC_DM5 F24
VMC_DM6 C24
VMC_DM7 E20

FBCDQM0 FBCDQM1 FBCDQM2 FBCDQM3 FBCDQM4 FBCDQM5 FBCDQM6 FBCDQM7

VMC_WDQS0 C5
VMC_WDQS1 E10
VMC_WDQS2 E5
VMC_WDQS3 B8
VMC_WDQS4 A29
VMC_WDQS5 D25
VMC_WDQS6 B25
VMC_WDQS7 E20

FBCDQS_WP0 FBCDQS_WP1 FBCDQS_WP2 FBCDQS_WP3 FBCDQS_WP4 FBCDQS_WP5 FBCDQS_WP6 FBCDQS_WP7

VMC_RDQS0 C6
VMC_RDQS1 E9
VMC_RDQS2 E6
VMC_RDQS3 A8
VMC_RDQS4 B29
VMC_RDQS5 E25
VMC_RDQS6 A25
VMC_RDQS7 F21

FBCDQS_RN0 FBCDQS_RN1 FBCDQS_RN2 FBCDQS_RN3 FBCDQS_RN4 FBCDQS_RN5 FBCDQS_RN6 FBCDQS_RN7

U_GPU_G3

FBVTT_0 AA23
FBVTT_1 AB23
FBVTT_2 H16
FBVTT_3 H17
FBVTT_4 J10
FBVTT_5 J23
FBVTT_6 J24
FBVTT_7 J9
FBVTT_8 K11
FBVTT_9 K12
FBVTT_10 K21
FBVTT_11 K22
FBVTT_12 K24
FBVTT_13 K9
FBVTT_14 L23
FBVTT_15 M23
FBVTT_16 T25
FBVTT_17 U25

C150 .1U/10V
C106 .1U/10V
C97 .1U/10V
C125 .1U/10V
C146 .47U/10V
C147 .47U/10V
C149 10U/4V
C160 .1U/10V
C98 .1U/10V
C96 .1U/10V
C692 .1U/10V
C142 .47U/10V
C151 .47U/10V
C148 10U/4V

+1.8V

PLACE NEAR GPU

FBC_CMD0 C13
FBC_CMD1 A16
FBC_CMD2 A13
FBC_CMD3 B17
FBC_CMD4 B20
FBC_CMD5 A19
FBC_CMD6 B19
FBC_CMD7 B14
FBC_CMD8 E16
FBC_CMD9 A14
FBC_CMD10 C15
FBC_CMD11 B16
FBC_CMD12 E17
FBC_CMD13 C19
FBC_CMD14 D15
FBC_CMD15 C17
FBC_CMD16 A17
FBC_CMD17 C16
FBC_CMD18 D14
FBC_CMD19 F16
FBC_CMD20 C14
FBC_CMD21 C18
FBC_CMD22 E14
FBC_CMD23 B13
FBC_CMD24 E15
FBC_CMD25 F15
FBC_CMD26 A20

VMC_MA3 VMC_MA0 VMC_MA2 VMC_MA1 VMC_MA3H VMC_MA4H VMC_MA5H VMC_BA2 VMC_CS0# VMC_WE# VMC_BA0 VMC_CKE VMC_RST# VMC_MA2H VMC_MA12 VMC_RAS# VMC_MA11 VMC_MA10 VMC_BA1 VMC_MA8 VMC_MA9 VMC_MA6 VMC_MA5 VMC_MA7 VMC_MA4 VMC_CAS# VMC_MA13

T16 T164

VMC_MA3 19
VMC_MA0 19
VMC_MA2 19
VMC_MA1 19
VMC_MA3H 19
VMC_MA4H 19
VMC_MA5H 19
T16
VMC_CS0# 19
VMC_WE# 19
VMC_BA0 19
VMC_CKE 19
VMC_MA2H 19
VMC_MA12 19
VMC_RAS# 19
VMC_MA11 19
VMC_MA10 19
VMC_BA1 19
VMC_MA8 19
VMC_MA9 19
VMC_MA6 19
VMC_MA5 19
VMC_MA7 19
VMC_MA4 19
VMC_CAS# 19
T164

FBC_CLK0 F13
FBC_CLK0# F13
FBC_CLK1 F18
FBC_CLK1# F17

VMC_CLK0 VMC_CLK0# VMC_CLK1 VMC_CLK1#

VMC_CLK0 19
VMC_CLK0# 19
VMC_CLK1 19
VMC_CLK1# 19

RFU4 C20
RFU5 D1

G73_C20 G73_D1

T166 T172

FBC_DEBUG F12

VMC_DEBUG

T19

FBC_REFCLK B1
FBC_REFCLK# C1

VMC_REFCK VMC_REFCK#

T165 T167

FBC_PLLVDD G8
FBC_PLLAVDD G10
FBC_PLLGND G9

G73_G8

T25

15mil

FBC_PLLAVDD

L22 BLM18PG330SN1D

VGA1.2V

C690 470P/50V C689 4700P/25V C109 4.7U/10V

FBCAL_PD_VDDQ K26
FBCAL_PU_GND H26
FBCAL_TERM_GND J26

FBCAL_PD R171 40.2/F
FBCAL_PU R163 40/F
FBCAL_TERM R161 *40.2/F

+1.8V

FB_VREF2 A28

15mil

FB_VREF2 R542 *1K +1.8V
C695 *.1U/10V R534 *1K

G70,G71: Stuff these parts
G72M,G73M : NC

18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

19 VMC_DQ[63..0]
19 VMC_DM[7..0]
19 VMC_WDQS[7..0]
19 VMC_RDQS[7..0]

VMA_RST# R566 0 VMA_ODT VMA_ODT 18

R570 10K

G72M/G73M: STUFF
UMA:NC

G72M-Z:NO STUFF

VMC_RST# R124 0 VMC_ODT VMC_ODT 19

R118 10K

G72M/G73M: STUFF
UMA:NC

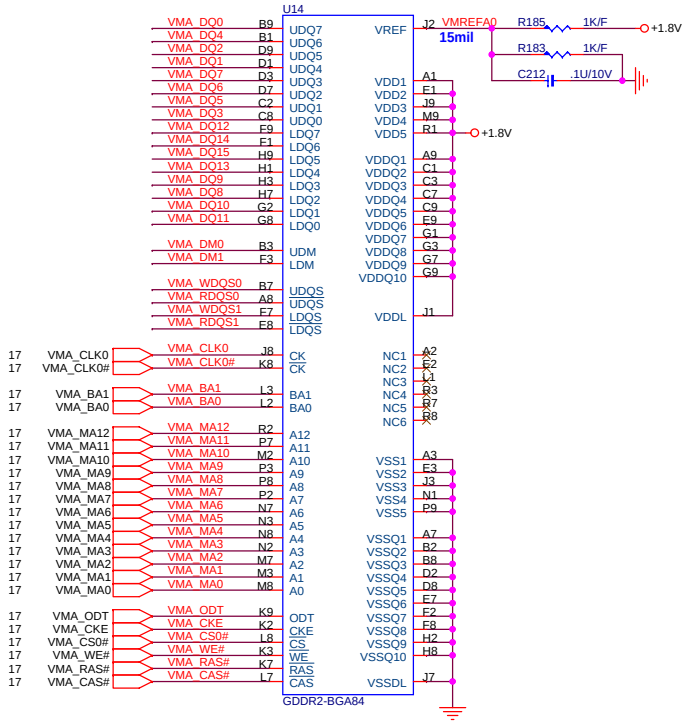
G72M-Z:NO STUFF

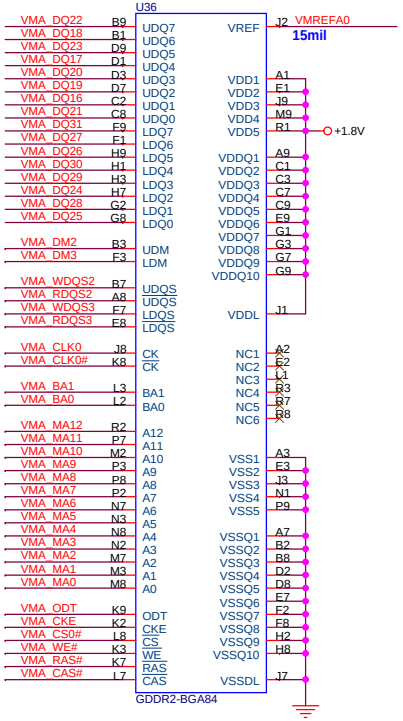
NB5/RD1/HW2

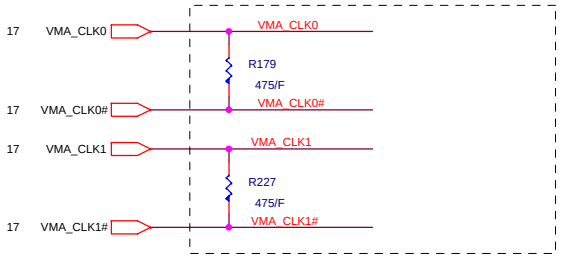
PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (MEM I/F)	2A

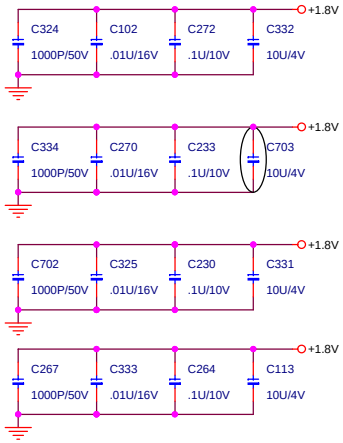
Date: Tuesday, August 01, 2006 Sheet 17 of 45



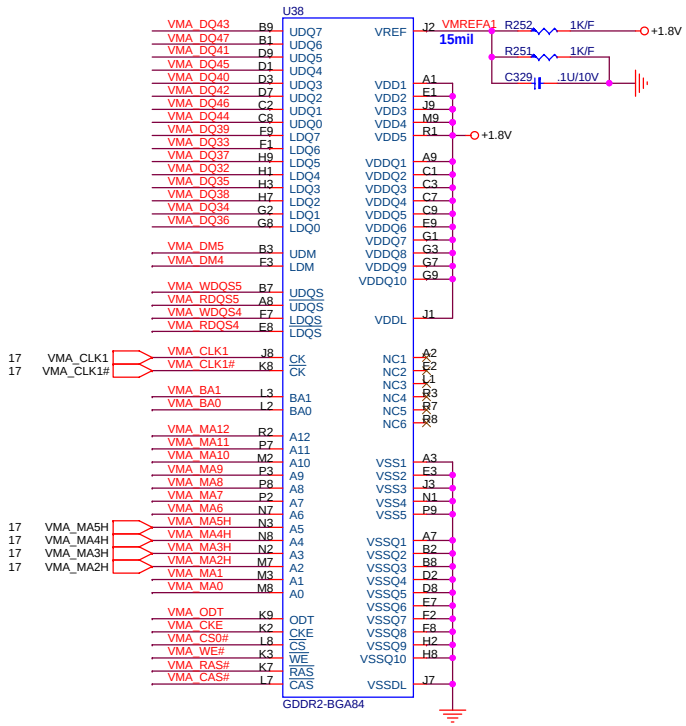


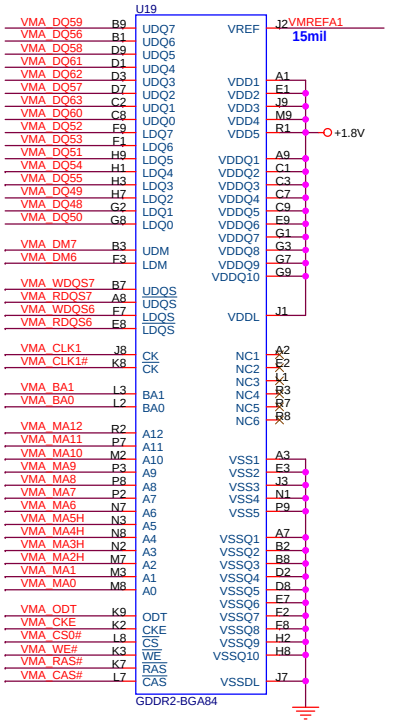


G72M-Z: NO STUFF
G72M:120 ohm
G73M: 480 ohm



17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]





256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01

NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M VRAN-1(GDDR2 BGA84)	1A

Date: Tuesday, August 01, 2006 Sheet 18 of 45

NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.	
	Size: Custom Document Number: NVG73M VREM-2(GDDR2 BGA84)	Rev: 1A
	Date: Tuesday, August 01, 2006	Sheet 19 of 45

TO PANEAL

MV_Change to 0603 package.

Close to EC

C2:change HE1,HE2 layout location and Add HE3 bom also only add HE3 for AT6

DB "short" and reserve common mode choke pads for EMI final tune

For HDMI Nvidia's PUN issue

C3:Add L69,L70,C936,C937 PUN issue

LAYOUT must support connectors from JAE, Molex and Acon.

HDMI PORT

for EMI request

FOX-GS12401-1011

PROJECT : AT6	Quanta Computer Inc.
Size: Custom	Document Number: LCD CONN/HDMI CONN
Rev: 2A	
Date: Tuesday, August 01, 2006	Sheet 20 of 45

NB5/RD1/HW2

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

Place near to Mini-door

VCCRTC
3VPCU
D38 CH500H-40
C835 1U/16V
R687 20K
VCCRTC_2
D37 CH500H-40
R695 1K
R686 1M/F
C845 1U/16V
G1 *SHORT_ PAD1
CN28 CWY020-B0G1Z
C615 15P
C616 15P
Y6 32.768KHZ
R450 10M
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN

U45A

RTXC1 AB1
RTXC2 AB2
RTCRST# AA3
INTRUDER# Y5
INTVRMEN W4

RTC

LAN_EEP_CS W1
LAN_EEP_SK Y1
LAN_EEP_DOUT Y2
LAN_EEP_DIN W3
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN

LPC

33 LAN_JCLK V3
33 LAN_RSTSYNC U3
33 LAN_RXD0 U5
33 LAN_RXD1 V4
33 LAN_RXD2 T5
33 LAN_TXD0 U7
33 LAN_TXD1 V6
33 LAN_TXD2 V7
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2

LAN

CPU

26 ACZ_BCLK U1
ACZ_SYNC R6
ACZ_RST# R5
28 ACZ_SDIN0 T2
ACZ_SDIN1 T3
ACZ_SDIN2 T1
ACZ_SDOUT T4
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT

AC-97/AZALIA

SATALED# AF18
SATA0RXN AF3
SATA0RXP AE3
SATA0TXN AG2
SATA0TXP AH2
SATA2RXN AF7
SATA2RXP AE7
SATA2TXN AG6
SATA2TXP AH6
SATA_CLKN AF1
SATA_CLKP AE1
SATARBIASN AH10
SATARBIASP AG10

SATA

DIOR# AF15
DIOW# AH15
DDACK# AE16
IDEIRQ AH16
IORDY AG16
DDREQ AE15

IDE

ICH7-M

LAD0 AA6
LAD1 AB5
LAD2 AC4
LAD3 Y6
LDRQ0# AC3
LDRQ1#/GPIO23 AA5
LFRAME# AB3
A20GATE AE22
A20M# AH28
CPUSLP# AG27
TP1/DPRSTP# AF24
TP2/DPSLP# AH25
FERR# AG26
GPIO49/CPUPWRGD AG24
IGNNE# AG22
INIT3_3V# AG21
INIT# AE22
INTR AE25
RCIN# AG23
NMI AH24
SMI# AF23
STPCLK# AH22
THERMTRIP# AE26

DD0 AB15
DD1 AE14
DD2 AG13
DD3 AF13
DD4 AD14
DD5 AC13
DD6 AD12
DD7 AC12
DD8 AE12
DD9 AE12
DD10 AB13
DD11 AC14
DD12 AE14
DD13 AH13
DD14 AH14
DD15 AC15
DA0 AH17
DA1 AE17
DA2 AE17
DCS1# AE16
DCS3# AD16

LAD0 32,37
LAD1 32,37
LAD2 32,37
LAD3 32,37
LDRQ#0 T153
LDRQ#1 T141
LFRAME# 32,37
GATEA20 37
H_A20M# 3
TP_H_CPUSLP# R385 *0 H_CPUSLP# 3,6
H_DPRSTP# R R638 0 DPRSLP# 3,44
H_DPSLP# R R396 0/F H_DPSLP# 3
H_FERR# 3
R391 0/F H_PWRGD 3
H_IGNNE# 3
T255
H_INIT# 3
H_INTR 3
RCIN# 37
H_NMI 3
H_SMI# R R639 0/F H_SMI# 3
H_STPCLK# 3
H_THERMTRIP_R R641 24.9/F PM_THRMTRIP# 3,8
PDD[15:0] 31
PDA[2:0] 31
PDCS1# 31
PDCS3# 31

R139 close to MCH

3V
R625 10K
R624 10K
RCIN# GATEA20
+1.05V
R393 *56/F
R640 *56/F
R389 56/F
R634 56
Should be 2" close ICH7

3V
R672 10K
36 SATA_LED#
Review current rating

31 SATA_RXN0
31 SATA_RXP0
31 SATA_TXN0
31 SATA_TXP0
CKL:1n ~ 20nF
C608 3900P/25V SATA_RXN0_C
C607 3900P/25V SATA_RXP0_C
C609 3900P/25V SATA_TXN0_C
C610 3900P/25V SATA_TXP0_C

35 SATA_RXN2
35 SATA_RXP2
35 SATA_TXN2
35 SATA_TXP2
CKL:1n ~ 20nF
C613 3900P/25V SATA_RXN2_C
C614 3900P/25V SATA_RXP2_C
C611 3900P/25V SATA_TXN2_C
C612 3900P/25V SATA_TXP2_C

2 CLK_PCIE_SATA#
2 CLK_PCIE_SATA

3V
R422 8.2K
R426 4.7K
PDIORDY
IRQ14

25mils/15mils

R428 24.9/F SATA_BIAS
Place within 500 mils of ICH7

31 PDIOR#
31 PDIOW#
31 PDDACK#
31 IRQ14
31 PDIORDY
31 PDDREQ
IRQ14
PDIORDY

C775 *SFI0603-050E101NP

ACZ_SDOUT R688 39 ACZ_SDOUT_AUDIO 28
C844 *10P/50V
ACZ_SYNC R690 39 ACZ_SYNC_AUDIO 28
C843 *10P/50V
ACZ_BCLK R691 39 BIT_CLK_AUDIO 28
C842 *10P/50V
ACZ_RST# R689 39 ACZ_RST#_AUDIO 28

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

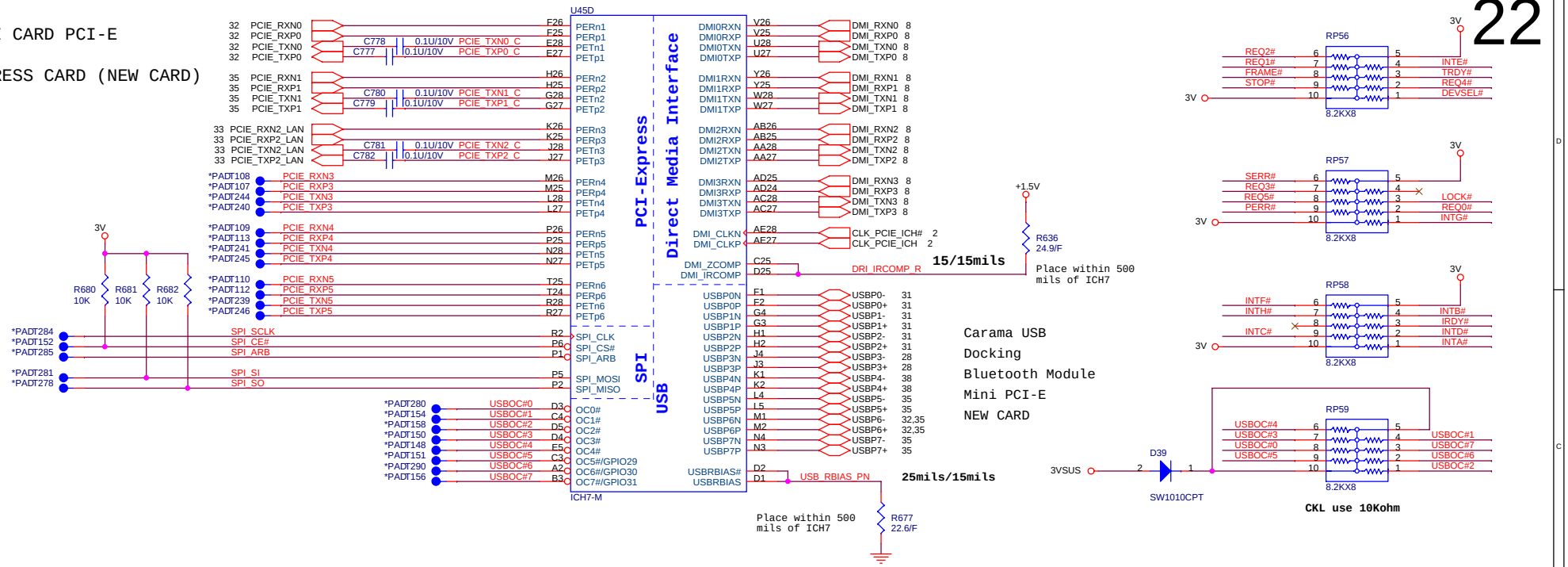
VCCRTC
R453 332K
ICH_INTVRMEN
R452 *0

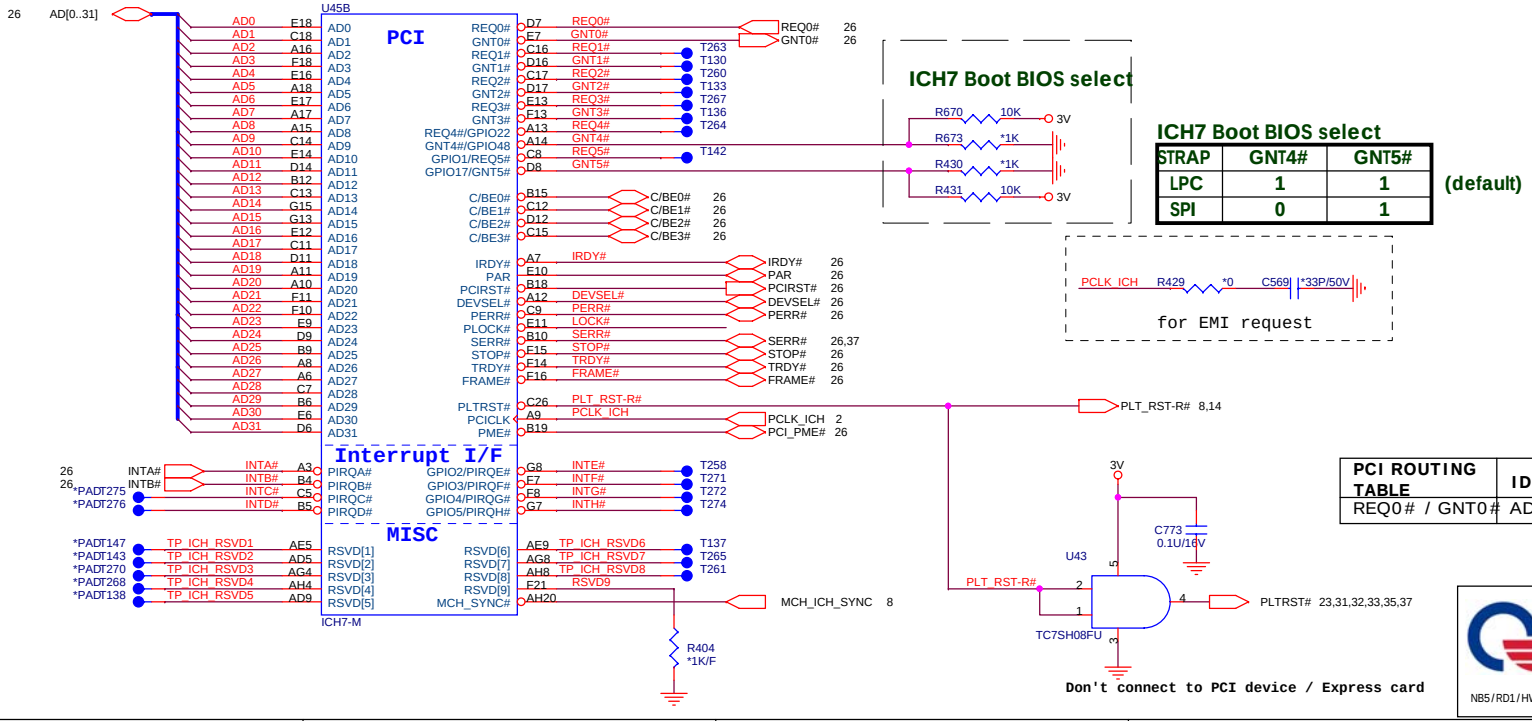
Populate for 82562GX/GZ

LANVCC
R693 *3.6K
U47
LAN_EEP_CS
LAN_EEP_SK
LAN_EEP_DOUT
LAN_EEP_DIN
CS SK DI DO
VCC NC NC GND
R694 *0
C846 *.1U/10V
GND
*93C46-3GR

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)





PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

Date: Tuesday, August 01, 2006 | Sheet 22 of 45

R376
No stuff-->boot
Stuff-->No boot

PCLK_SMB — R645 2.2K — PDAT_SMB
R384
PCIE_WAKE# — R403 1K — PM_BATLOW# R — R649 8.2K

SMB_LINK_ALERT# — R621 10K
SMLINK0 — R620 10K
SMLINK1 — R619 10K
WAKE_SCI# R — R399 *10K

RI# — R696 8.2K
DNBSWON# — R383 10K
SYS_RST#-1 — R618 10K
SMB_ALERT# — R390 10K
KBSMI# — R392 10K

MV_Add R443
BTLED — R443 10K
CLKRUN# — R418 8.2K
SERIRQ — R402 8.2K
SCI# — R424 10K
RSMRST# — R684 10K

to Clock Gen &Lan
&New Card

U45C
ICH7-M

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1
SATA GPIO: GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA2GP, GPIO37/SATA3GP
Clocks: CLK14, CLK48, SUSCLK
SYS & Power MGT: RI#, SPKR, SUS_STAT#, SYS_RST#, GPIO0/BM_BUSY#, GPIO11/SMBALERT#, GPIO18/STPPCI#, GPIO20/STPCPU#, GPIO26, GPIO27, GPIO28, GPIO32/CLKRUN#, GPIO33/AZ_DOCK_EN#, GPIO34/AZ_DOCK_RST#, WAKE#, SERIRQ, THRM#, VRMPWRGD, PWROK, GPIO16/DPRSLPVR, TP0/BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, GPIO9
GPIO: GPIO6, GPIO7, GPIO8, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, GPIO24, GPIO25, GPIO35, GPIO38, GPIO39

R401 *1K/F — 30 ACZ_SPKR
R400 *10K/F — R661 *10K/F — 33 SMB_ALERT# — No ASF support
2 PM_STPPCI# — R407 0/F — PM_STPPCI_ICH#
2 PM_STPCPU# — R398 0/F — PM_STPCPU_ICH#
8 PM_BMBUSY# — R654 0/F
32 RF_OFF# — R729 0/F
26,37 CLKRUN#
32,33,35 PCIE_WAKE#
26,37 SERIRQ
5 THERM_ALERT# — R663 10K
VR_PWRGD_CK410
20 LCD_BK
37 SCI#
37 KBSMI#

Note: Connect to EC; Reserve PH/3V

10/100 stuff R674
1000 stuff R671

R623 0 — PM_EXTTS#1 8,13
DPRSLPVR 44
R647 100/F — PM_BATLOW# 37
R674 *100/F — DNBSWON# 37 — LAN_REST 33,37
C807 *.1U/16V
R671 100/F — PLTRST# 22,31,32,33,35,37
R685 100/F RSMRST# — RSMRST# 33,37

LAN_RST pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#

MV_Add GPIO to control BTLED
FOR 10/100 LAN
WAKE ON LAN

BOARD_ID0, BOARD_ID1, BOARD_ID2, LCDID1, LCDID2
T132 *PAD, T126 *PAD
14M_ICH 2, CLKUSB_48 2
R633 100/F — SUSB# 37
R387 100/F — SUSC# 37
R388 0/F
SWI# 37
DASP_ON
MXM_THERM#
WAKE_SCI# R
R732 *0/F
R683 0/F
R717 100/F
BTLED 36
WAN_OFF# 32
LAN_DISABLE# 33
BT_OFF# 35
AMPBEEP_EN 30

GPIO25 /Suspend rail is a HW strap , don't pull down .

U23 — NL17SZ14DFT2G
2,44 VR_PWRGD_CK410# — VR_PWRGD_CK410

MXM_ON#: 1 -> No MXM Module
0 -> MXM Module
SWI# — R397 10K
MXM_THERM# — R644 *10K — 3V_S5

CLKUSB_48
14M_ICH
R678 10 — R679 33
C840 10P/50V — C841 10P/50V

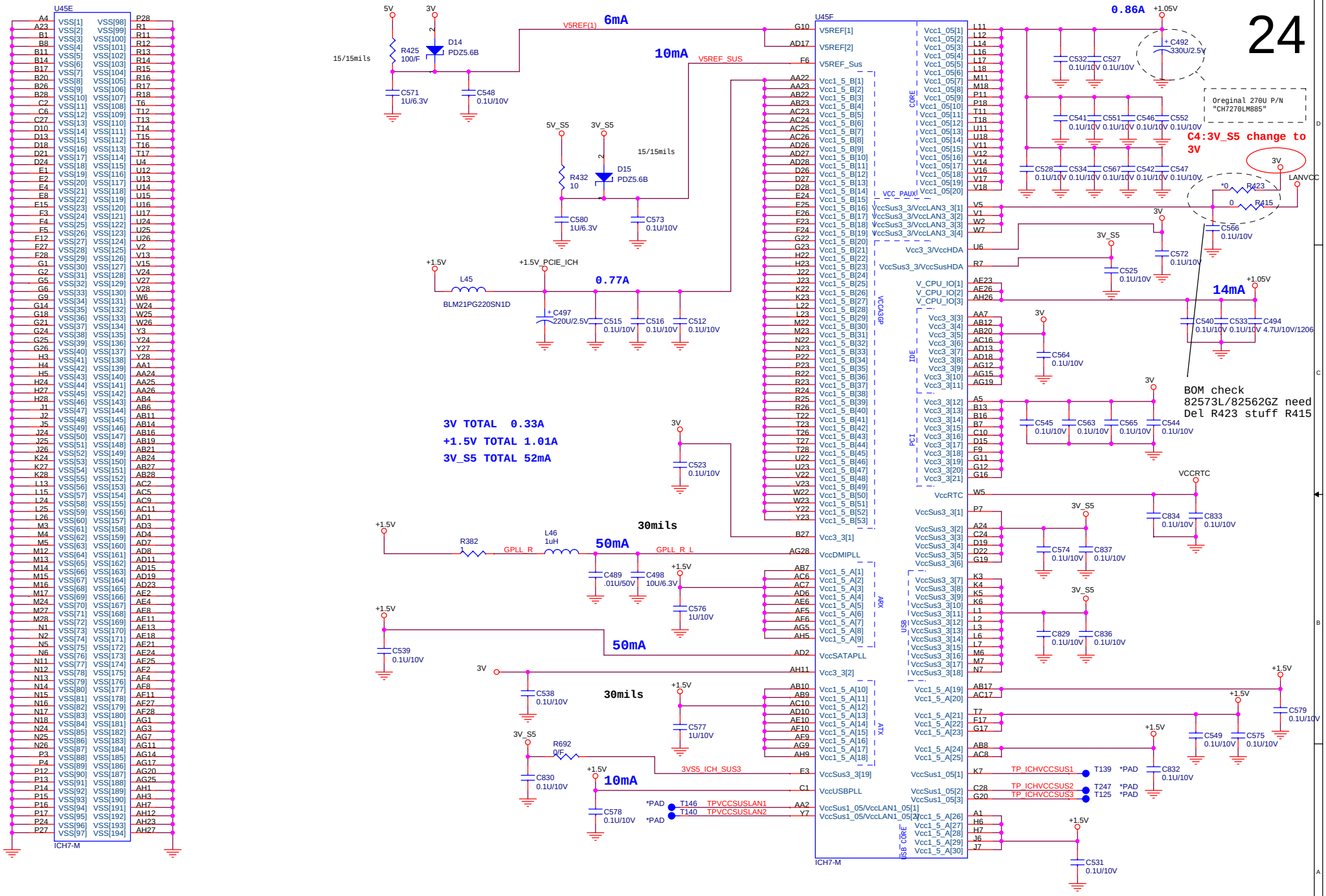
R629 *10K/F — R630 10K — BIOS_REC — R631 *0
R628 10K — R626 0/F — FWH_MFG_MODE — FWH_MFG_MODE_R — R627 *0

R655 *10K — BOARD_ID0 — R658 10K
R669 *10K — BOARD_ID1 — R668 10K
R667 *10K — BOARD_ID2 — R665 10K

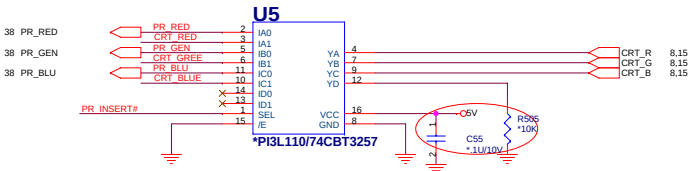
PWM require 6.9K
Change to 6.8K

Board ID	940 GML (0:0)	945GM (0:1)	PM+G72 (1:0)	PM+G73 (1:1)
ID0	R658 Stuff	R658 Stuff	R655 Stuff	R655 Stuff
ID1	R668 Stuff	R669 Stuff	R668 Stuff	R669 Stuff

PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size B | Document Number ICH7-M GPIO(3/4) | Rev 2A
Date: Tuesday, August 01, 2006 | Sheet 23 of 45

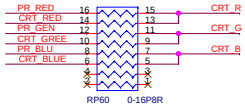

U45E
ICH7-M
U45F
ICH7-M
6mA
10mA
0.77A
0.86A
14mA
3V TOTAL 0.33A
+1.5V TOTAL 1.01A
3V_S5 TOTAL 52mA
30mils
50mA
C4:3V_S5 change to 3V
Oreginal 270U P/N "CH7270LM885"
BOM check
82573L/82562GZ need
Del R423 stuff R415
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
ICH7-M POWER(4/4)
Rev 1A
Date: Tuesday, August 01, 2006
Sheet 24 of 45

CRT SWITCH

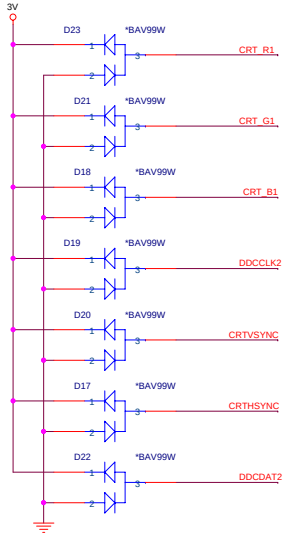


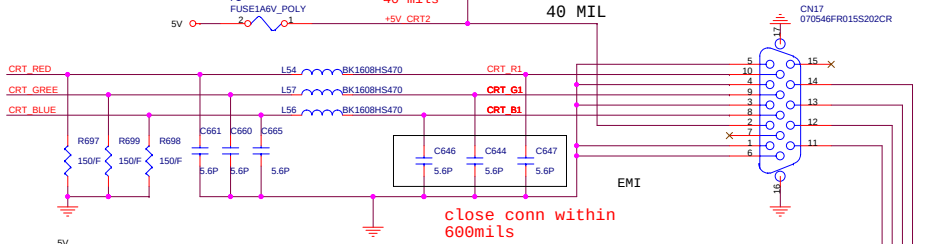
C5: bom del C55,R505

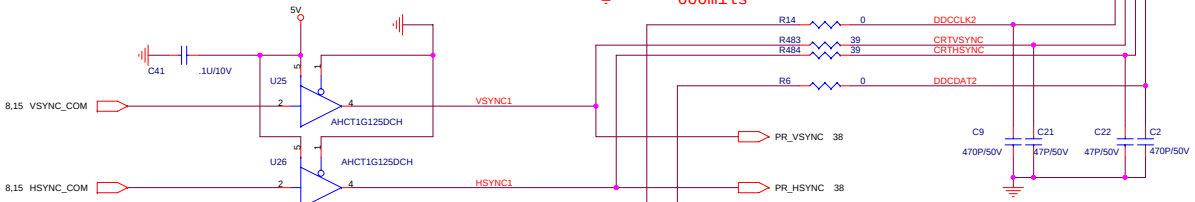
Place under U5 body



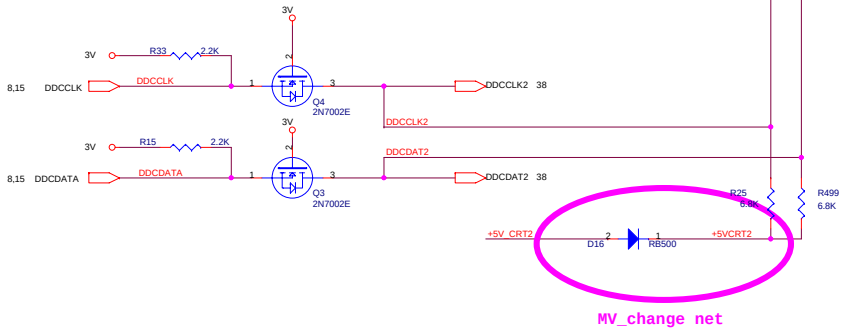
Bom Add





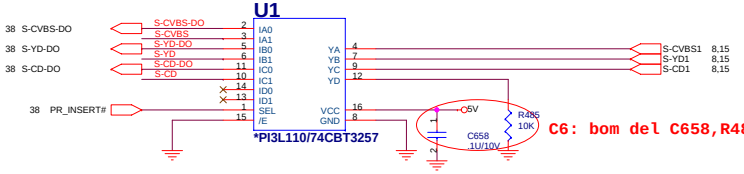


Bom Del U27,C28,U28,U29



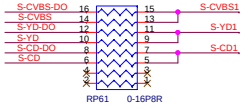
MV_change net

TV_SWITCH

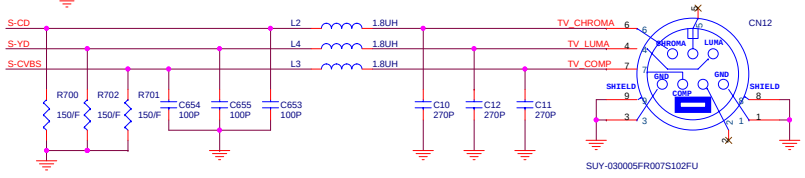


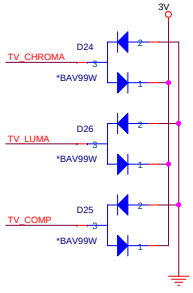
C6: bom del C658,R485

Place under U1 body

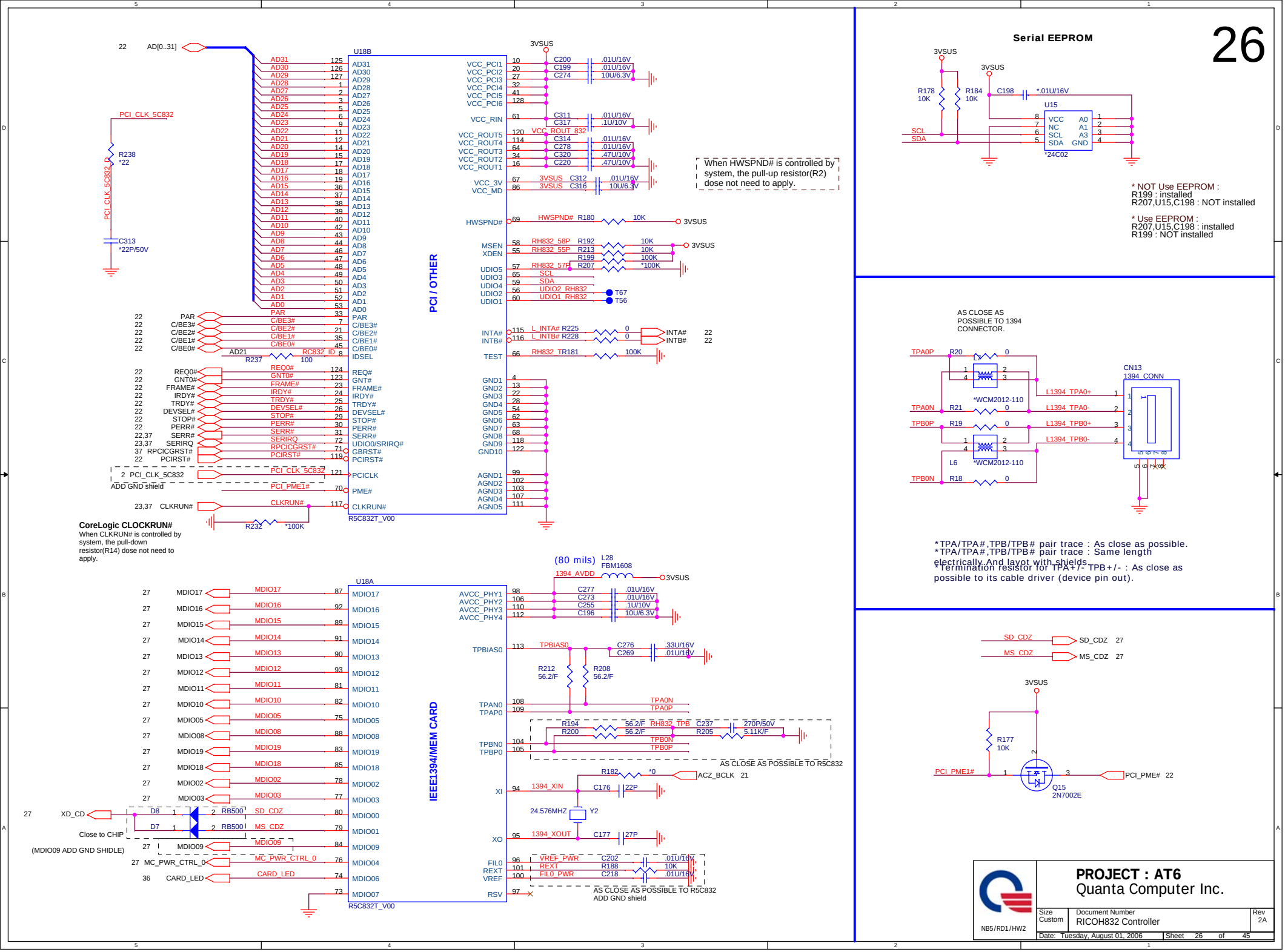


TV_OUT





PROJECT : AT6 Quanta Computer Inc.		
Size: Custom	Document Number: CRT/TV_OUT	Rev: 2A
N85/RD1/HW2	Date: Tuesday, August 01, 2006	Sheet 25 of 45



Serial EEPROM

* NOT Use EEPROM :
R199 : installed
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed

*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

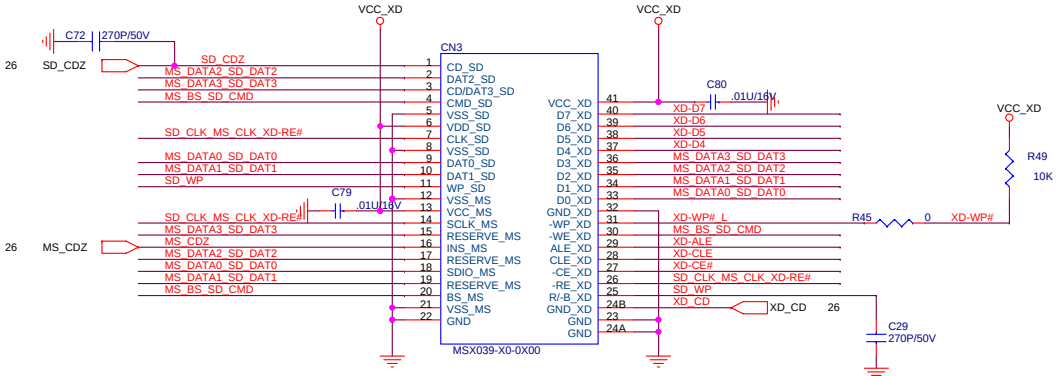
PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RICOH832 Controller	2A

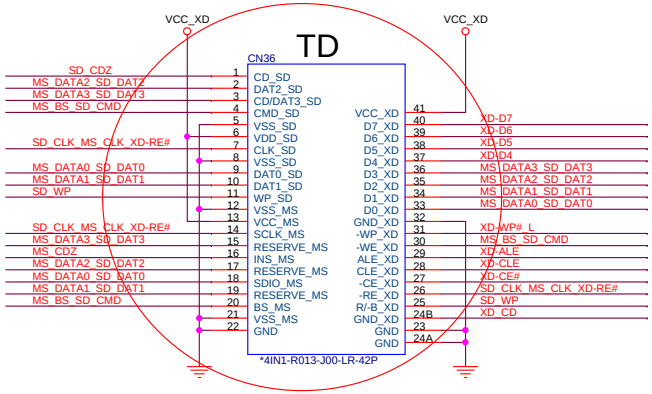
NB5/RD1/HW2

Date: Tuesday, August 01, 2006 Sheet 26 of 45

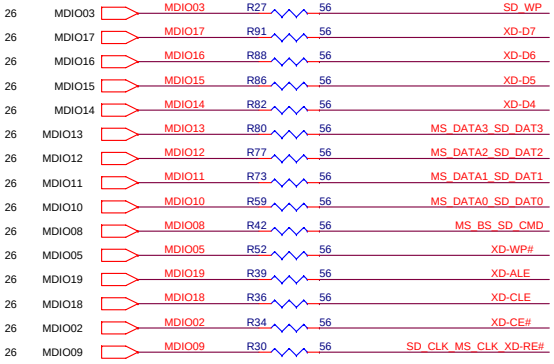
4 IN1 CARD READER
XD,MMC/SD,MS/MSP



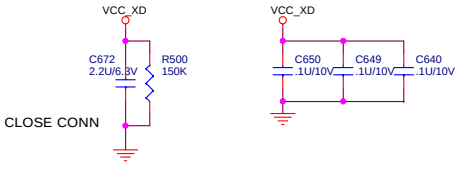
C7: change CN36 footprint

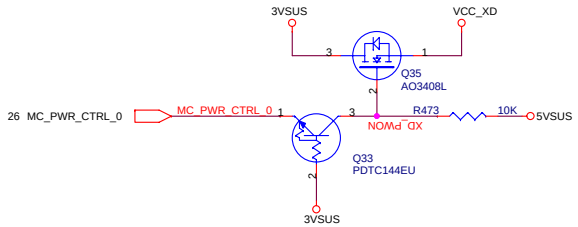


bom create 2'nd source



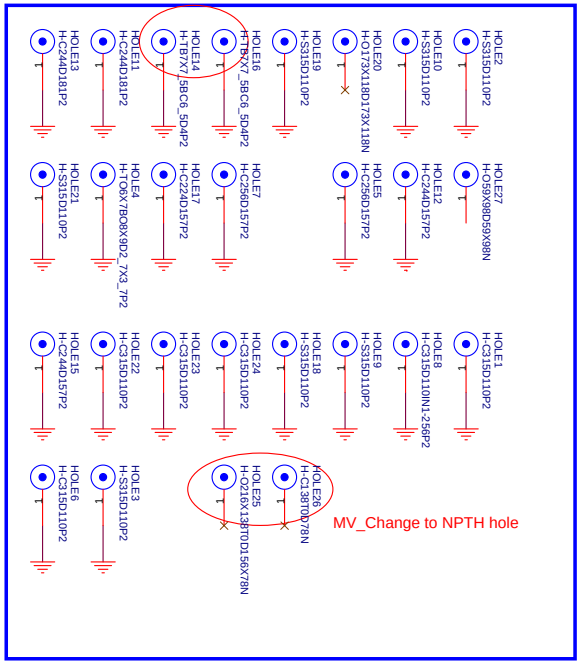
C_Delete reserve circuit for card reader power.



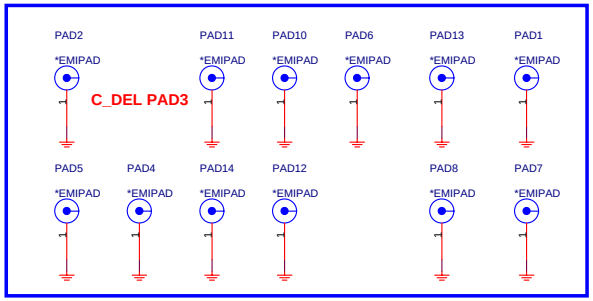


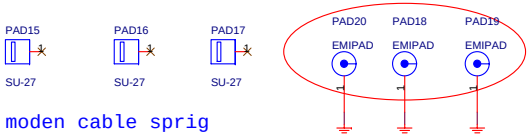
SCREW HOLE

MV_Change footprint



EMI PAD





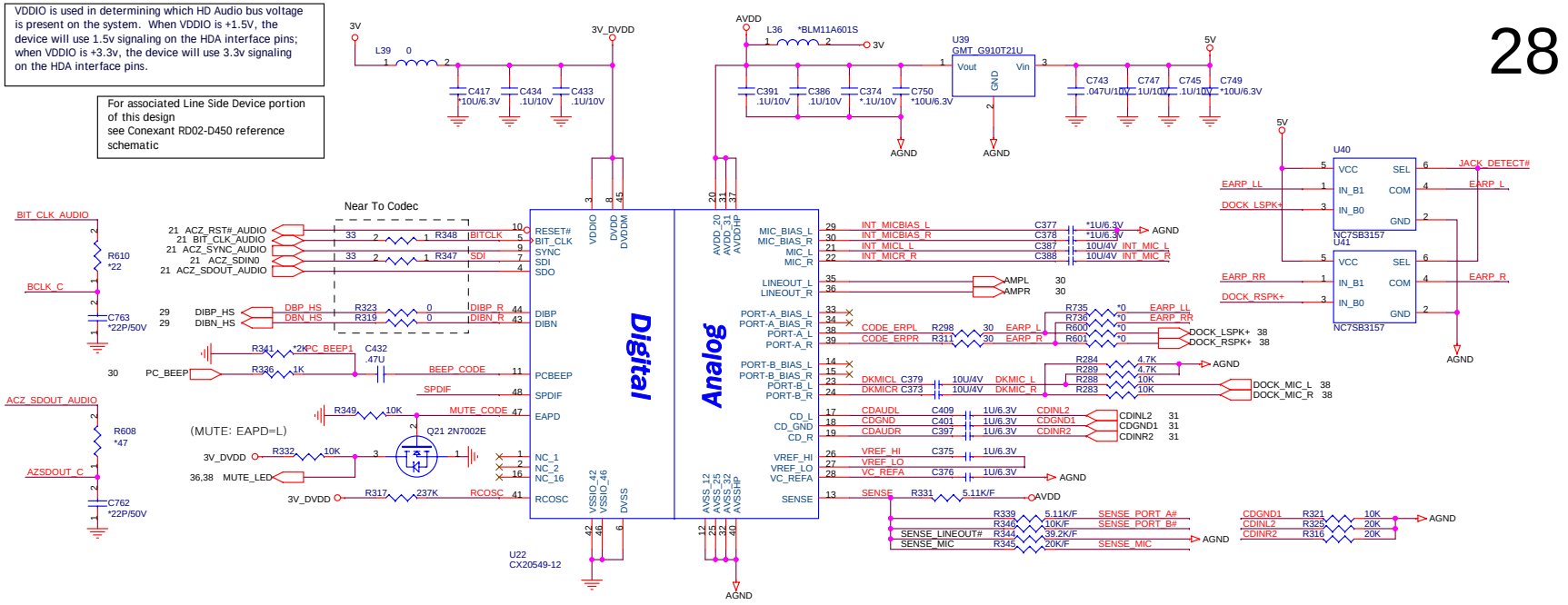
moden cable sprig

C8: Add lock bluetools cable spriq

NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.	
Size Custom	Document Number CARD READER/HOLE	Rev 1A
Date: Tuesday, August 01, 2006	Sheet 27 of 45	

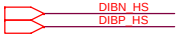
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

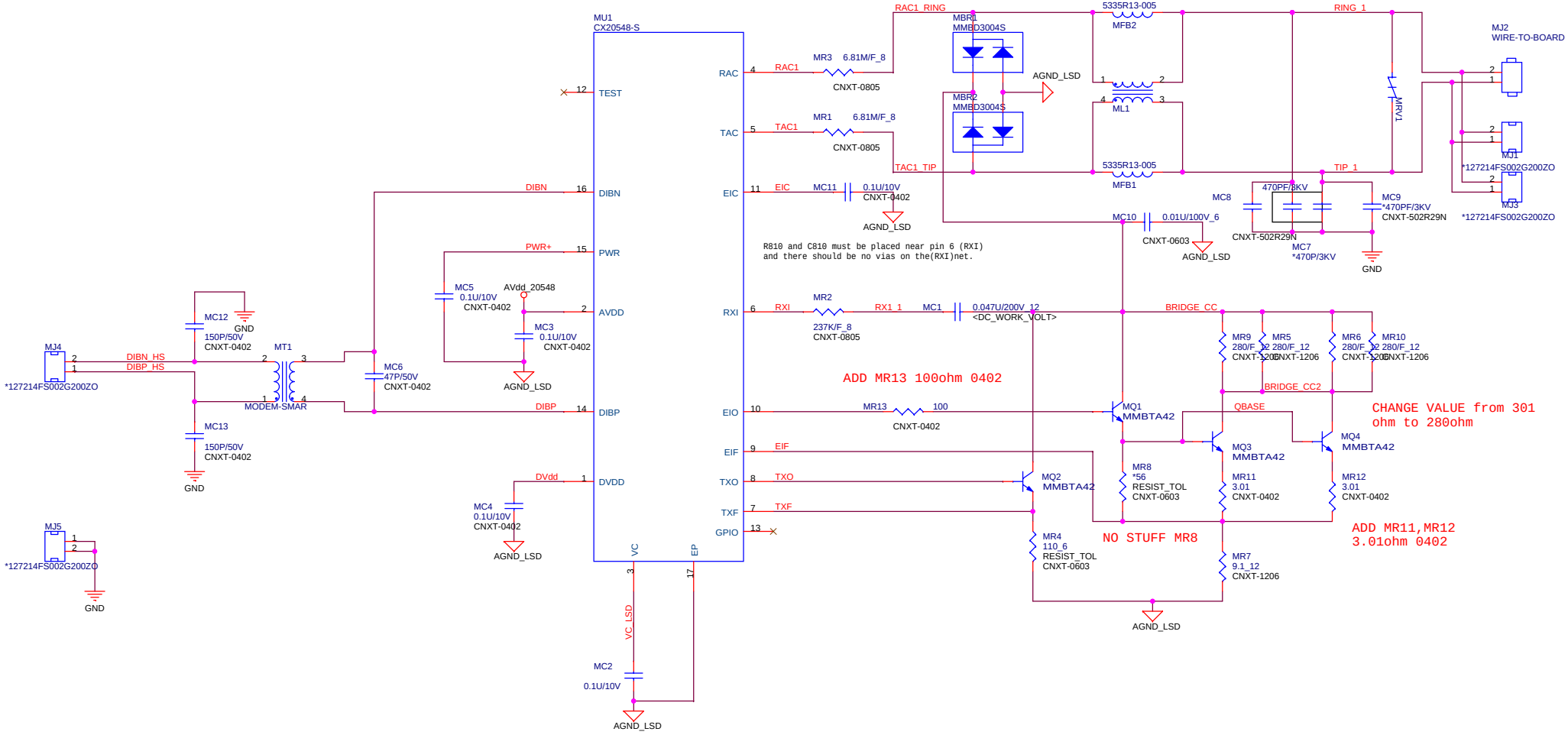
For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic



Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

28 DIBN_HS
28 DIBP_HS





PROJECT : AT6
Quanta Computer Inc.

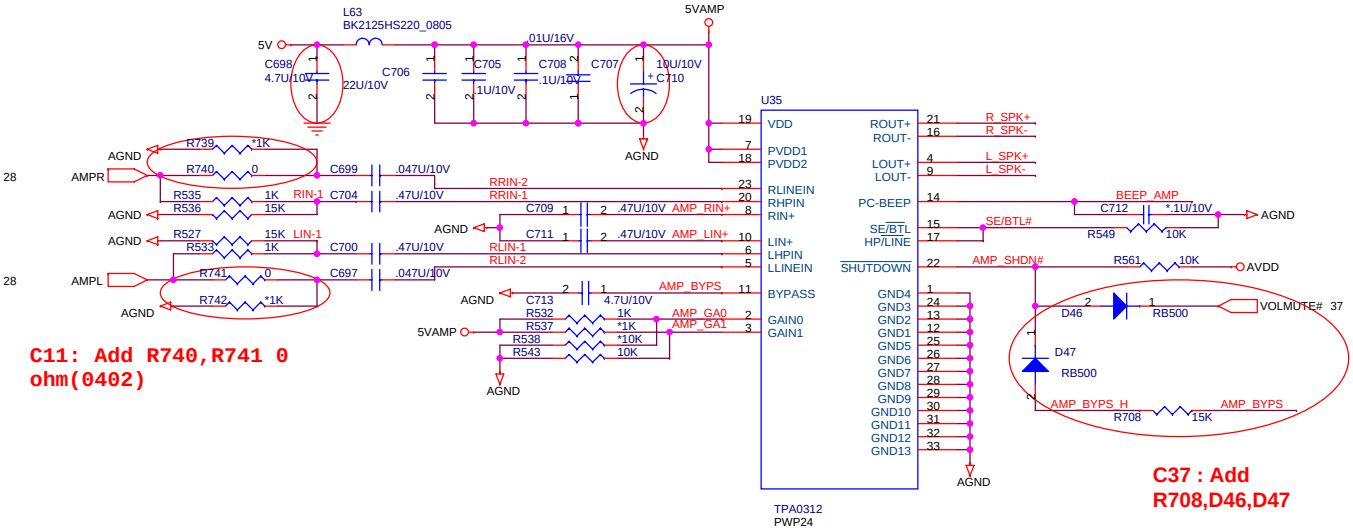
Size	Document Number	Rev
Custom	MODEM(DAA)	1A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 Sheet 29 of 45

AUDIO AMPLIFIER

MV_C710 change to CH6102M9900.
MV_C698 change to CH5472M9901.

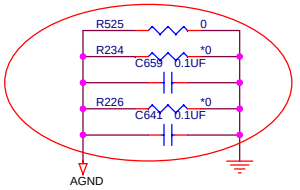


C11: Add R740,R741 0 ohm(0402)

C37 : Add R708,D46,D47

0312 Gain Table

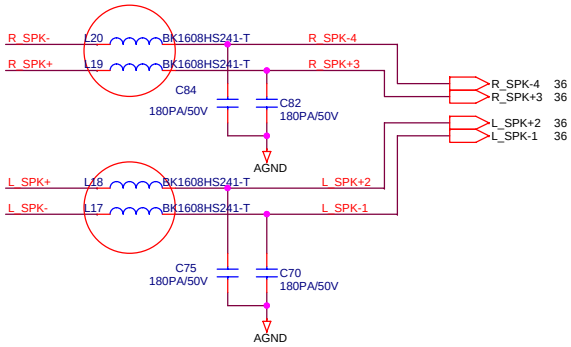
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



C38 : EMI request add R525 0 ohm,R226,R234 del 0 ohm,R524,R526 change from 0 ohm to 0.1u

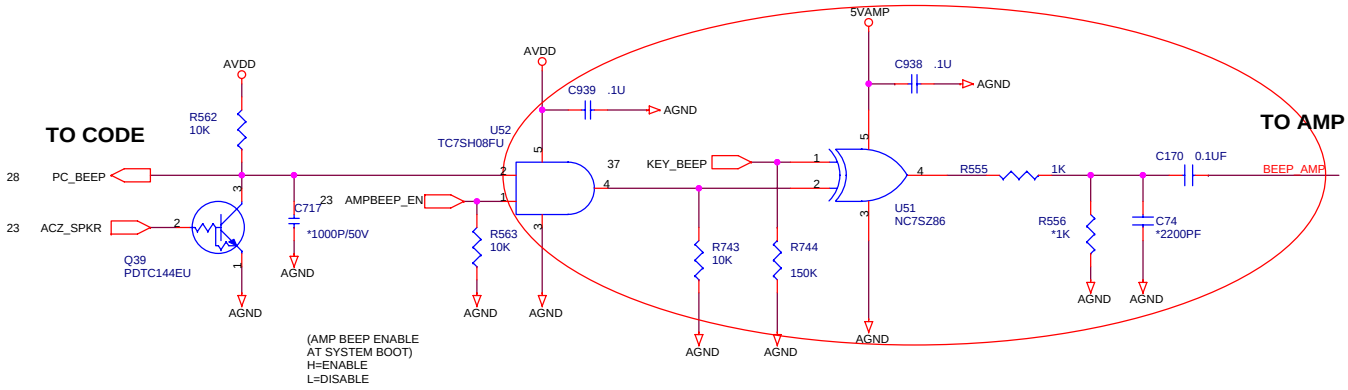
INT. SPEAKER

C12: change L17,L18,L19,L20 value to 240 Ohm



PCSPK BEEP

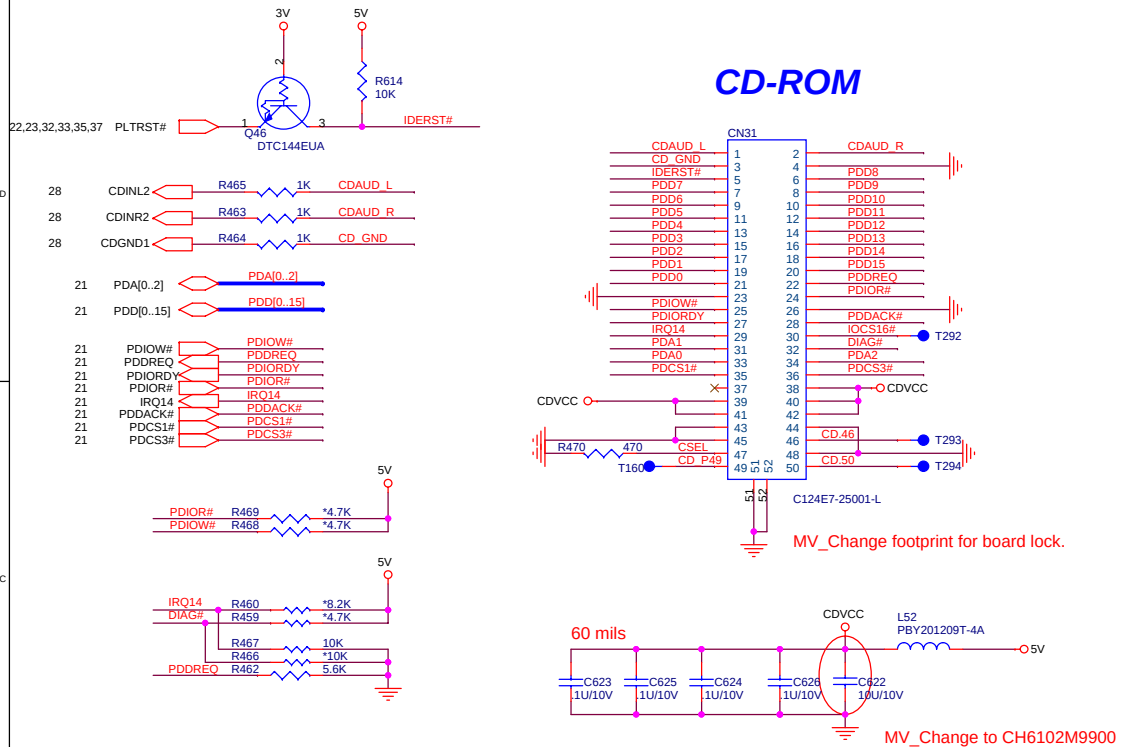
C13: Del Q57,R715,R554,C714 Add C938,U51,R774,R743,U52,C939,R563



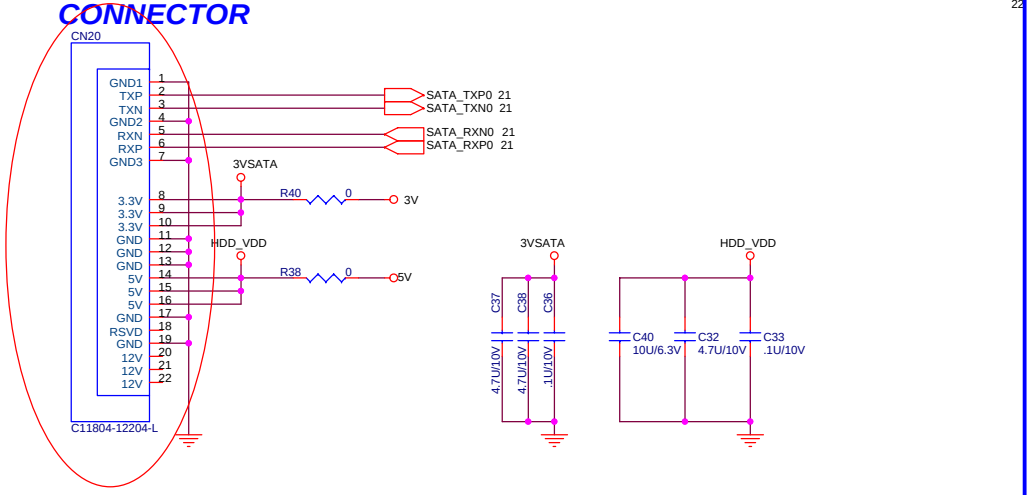
(AMP BEEP ENABLE AT SYSTEM BOOT)
H=ENABLE
L=DISABLE

NB5/RD1/HW2	PROJECT : AT6 Quanta Computer Inc.		
	Size: Custom	Document Number: JACK/AMP_TAP0312	Rev: 2A
	Date: Tuesday, August 01, 2006	Sheet 30 of 45	

CD-ROM

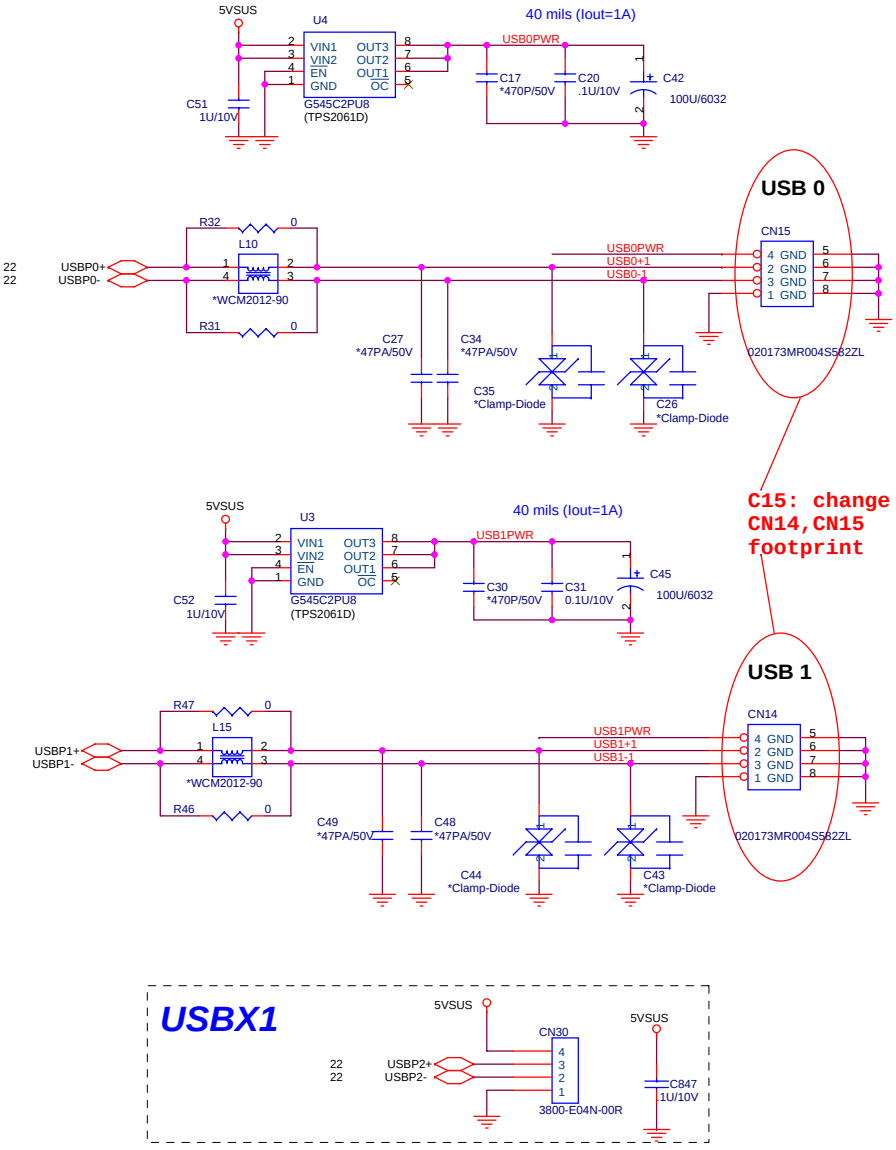


SATA_1 CONNECTOR



C14: change CN20 footprint

USBX2



USBX1

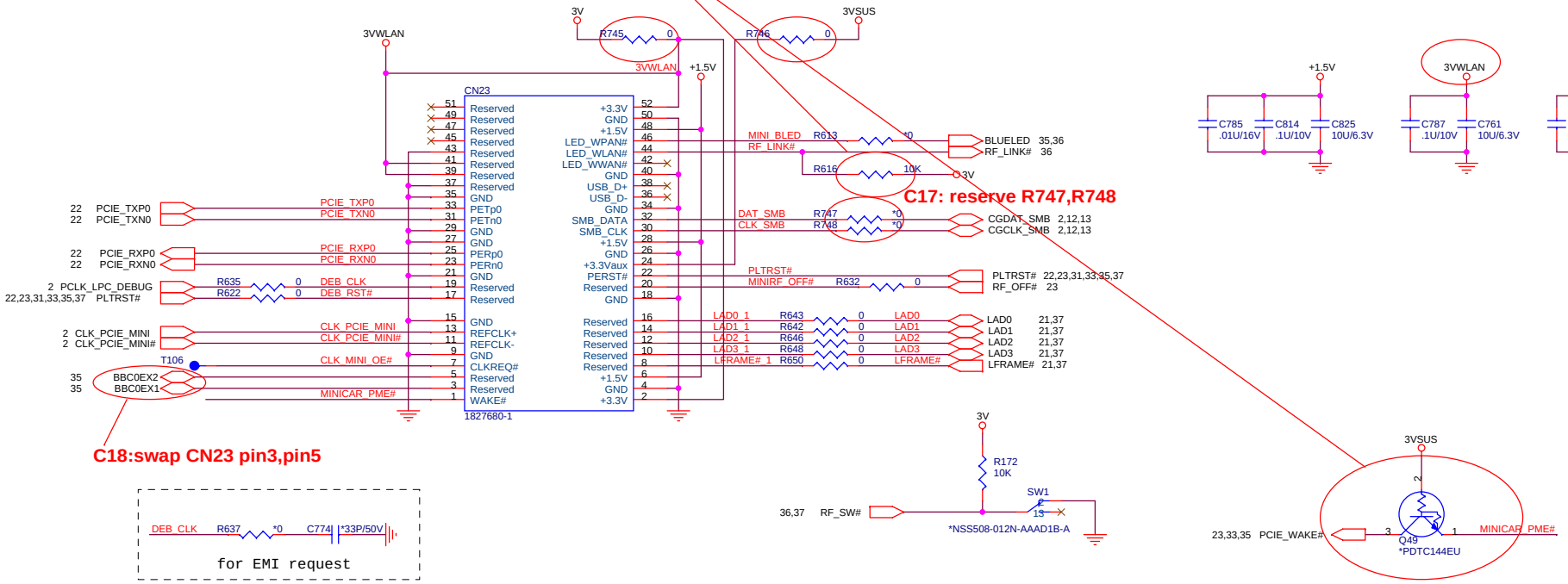
NB5/RD1/HW2	PROJECT : AT6 Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD/CD-ROM/USBX3	Rev: 2A
Date: Tuesday, August 01, 2006	Sheet 31 of 45	

Mini PCI-E Card 1
WLAN

C16: Add Bom R745(RC1206) R746(RC0603) and R616
Del Q49

C17: reserve R747,R748

C18:swap CN23 pin3,pin5

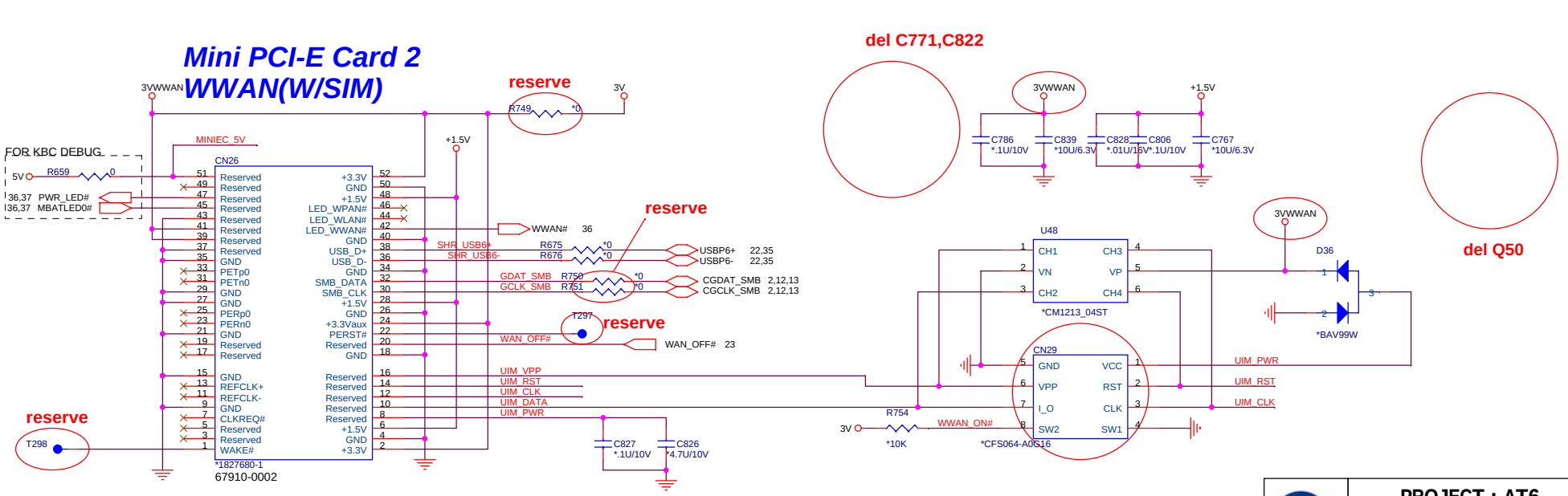


Mini PCI-E Card 2
WWAN(W/SIM)

del C771,C822

del Q50

C_Change to P-TWO footprint.
SDCARD-CSF064-A0G16-1-8P



PROJECT :	AT6
	Quanta Computer Inc.
Size	Custom
Document Number	MINI CARD X2
Rev	1A
Date:	Tuesday, August 01, 2006
Sheet	32 of 45
	NB5/RD1/HW2

T : Stuffed for 82573L(10/100/1000)

E : Stuffed for 82562GZ/GX(10/100)

U9A

82562GZ/GX

PCI Express

Ethernet Port

Control NVM/EEPROM

Test

LEDs

SMBus

JTAG 8257DEI

Thermal Monitoring

SDP Pin

Crystal

LAN Connect Interface

populate R93 for D3 wake up.

Place temination resistors and caps as close to LAN controller as possible

Populate R308 to disable SPI NVM protection.
Populate R309 - Use SPI FLASH
Populate R311 - Sahre SPI with ICH7-M.

for EMI request

573L populated 49.9/F
562GZ/GX populated
54.9/F

SST25LF080A/MX25L8005MC

For 10/100/100 LED option

MV_Add R103

MV_Add R62/C664

MV_Rotate D40

Resistor value:
82573E = 3.3K
82562GZ = 200
Check no stuff

MV_Reserve C669,C670,C671 and C674 for EMI.

RJ45

3800N-E002-NNN

C100F9-110A4-L

C19: change CN19 footprint

NS892403/2404

NS892403:GIGABIT
NS892405:10/100

PROJECT : AT6
Quanta Computer Inc.

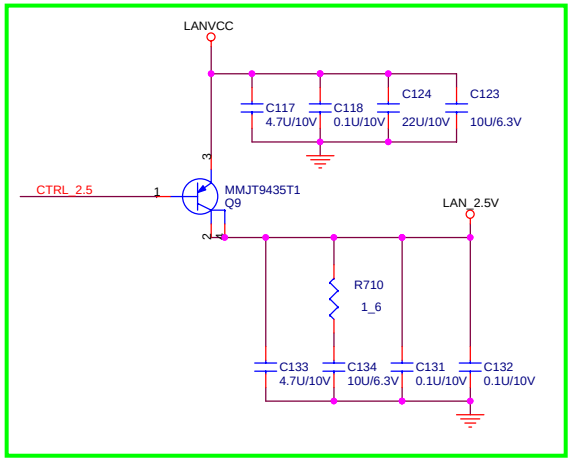
Size	Document Number	Rev
Custom	LAN 82573E/82562GZ	2A

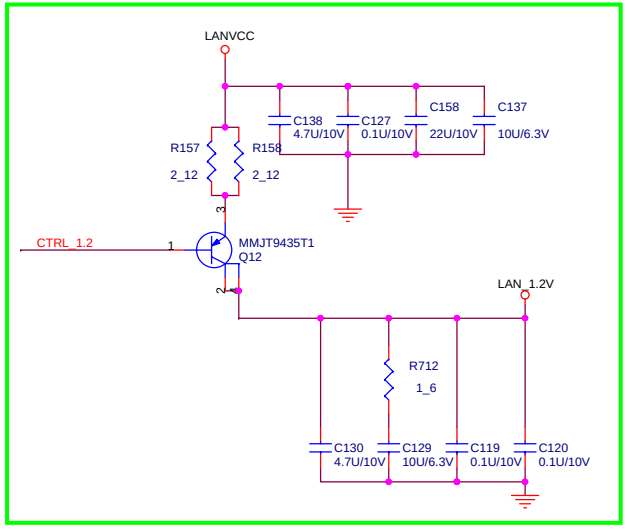
NB5/RD1/HW2

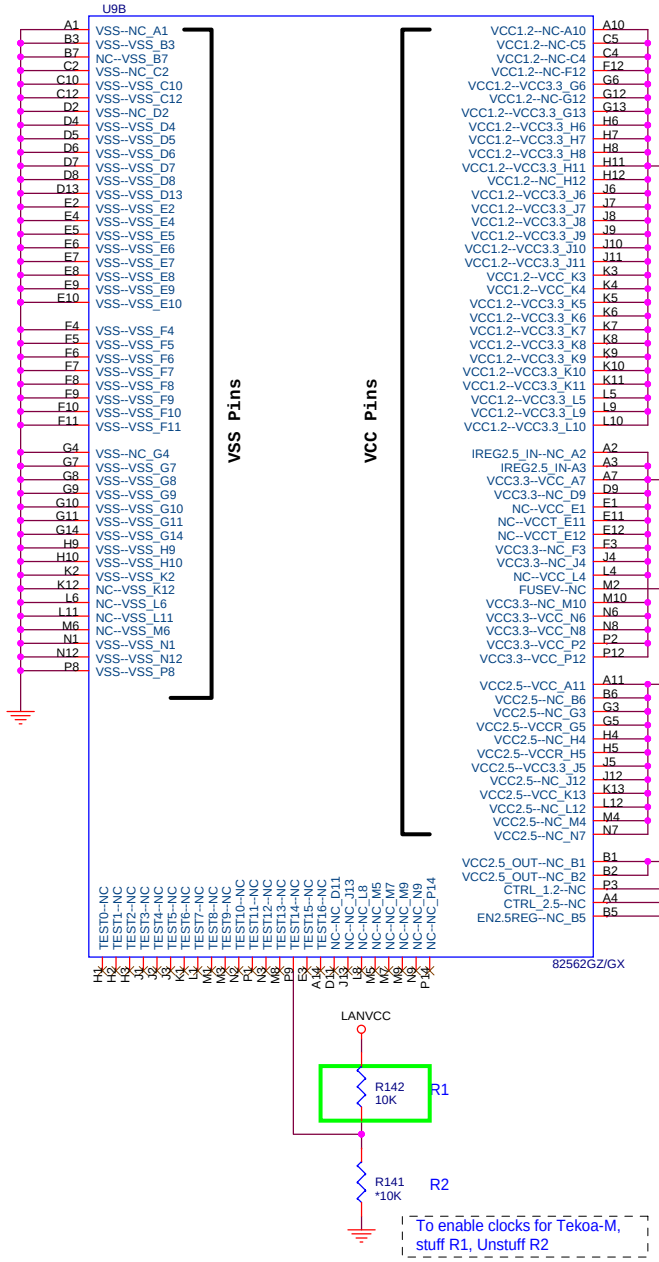
Date: Tuesday, August 01, 2006 | Sheet 33 of 45

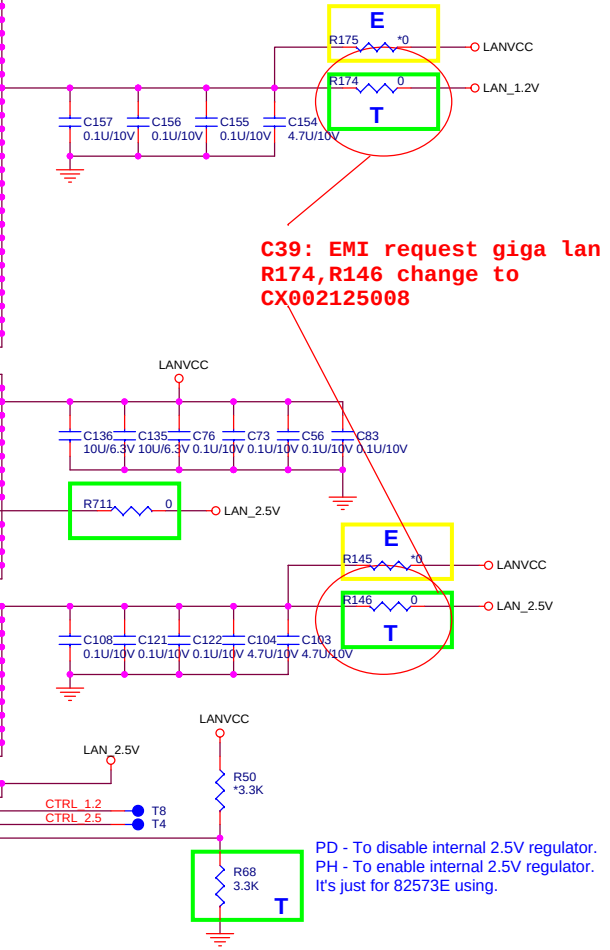
T : Stuffed for 82573L(10/100/1000)

E : Stuffed for 82856GZ/GX(10/100)









NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	2A

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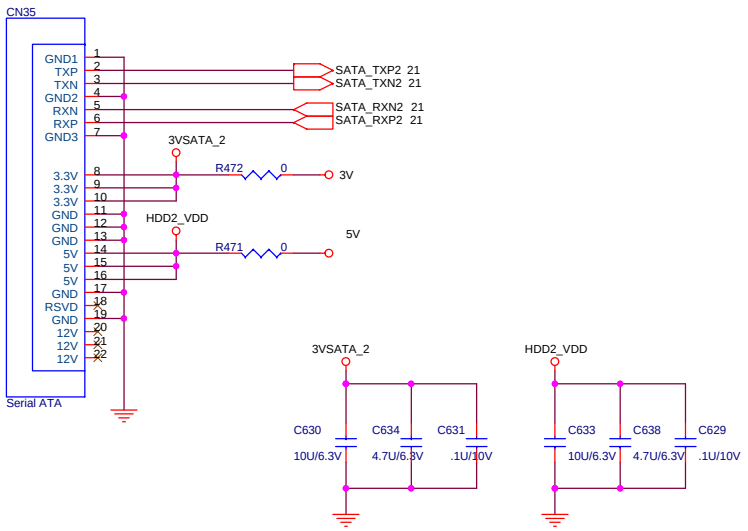
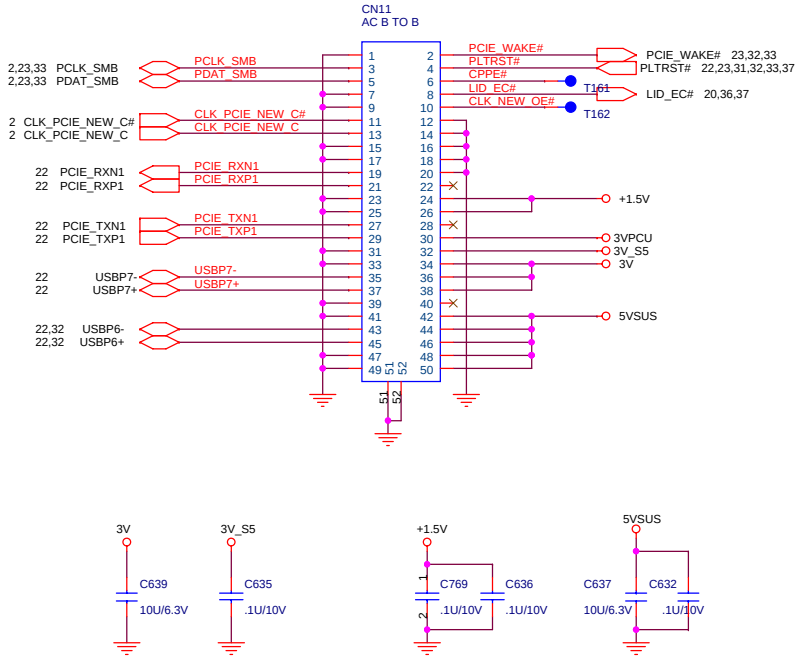
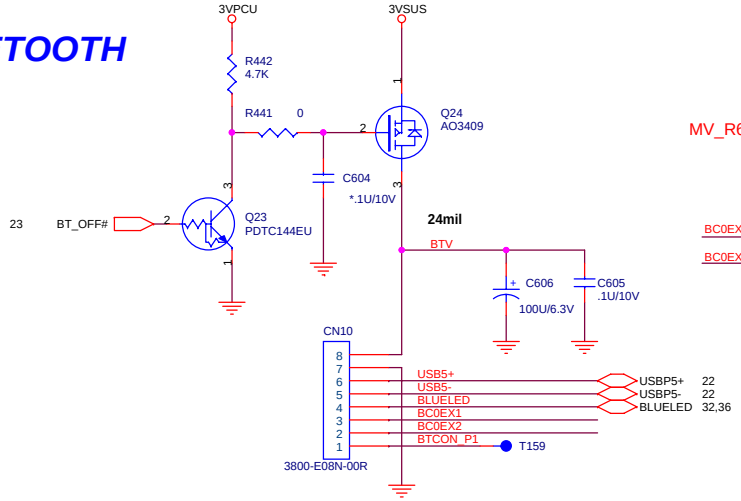
SATA_2 CONNECTOR
For 17"W Second HDD



NEWCARD

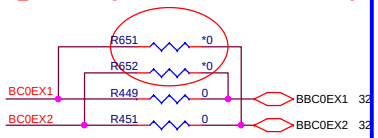


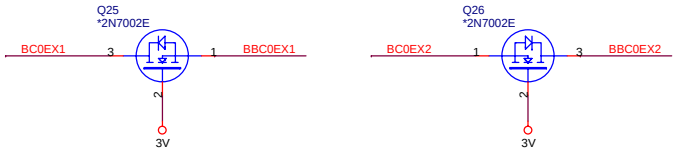
BLUETOOTH



C20: Del R651,R652

MV_R652 change to 0603 size for easier routing.





C_Del the reserve power switch for BT.

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	1A

NB5/RD1/HW2

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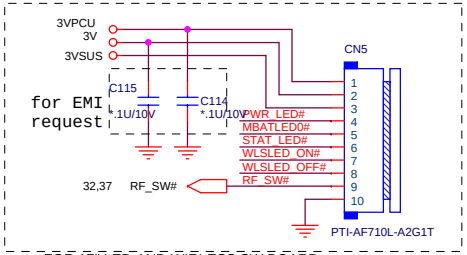
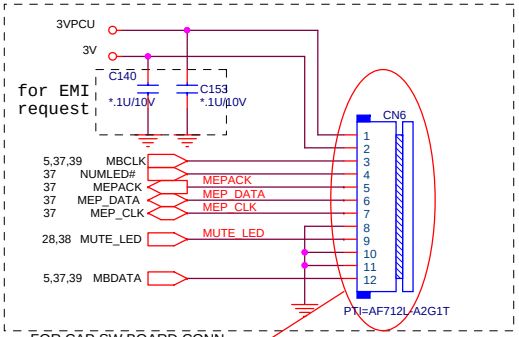
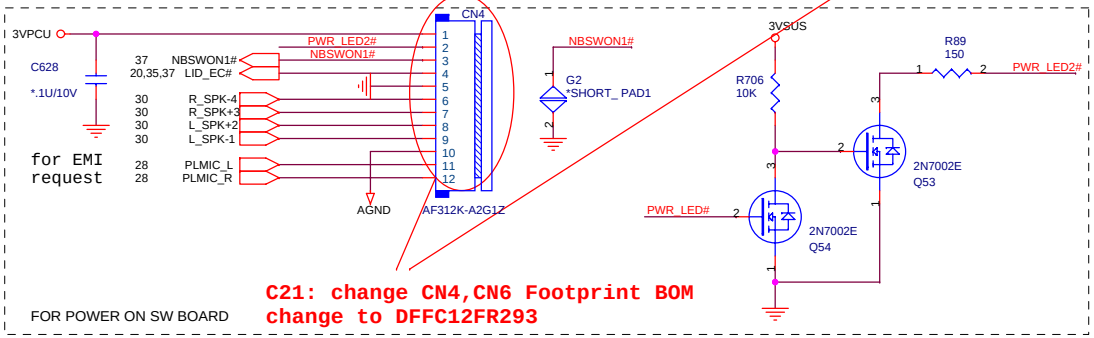


FOR 17" LED AND WIRLESS SW BOARD

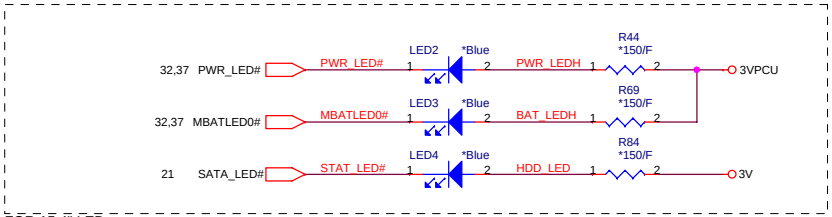


FOR CAP SW BOARD CONN

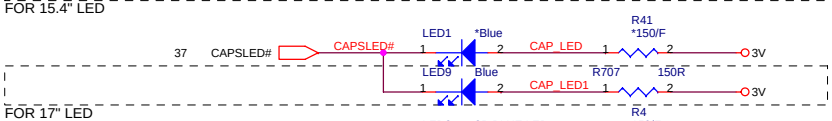


FOR POWER ON SW BOARD

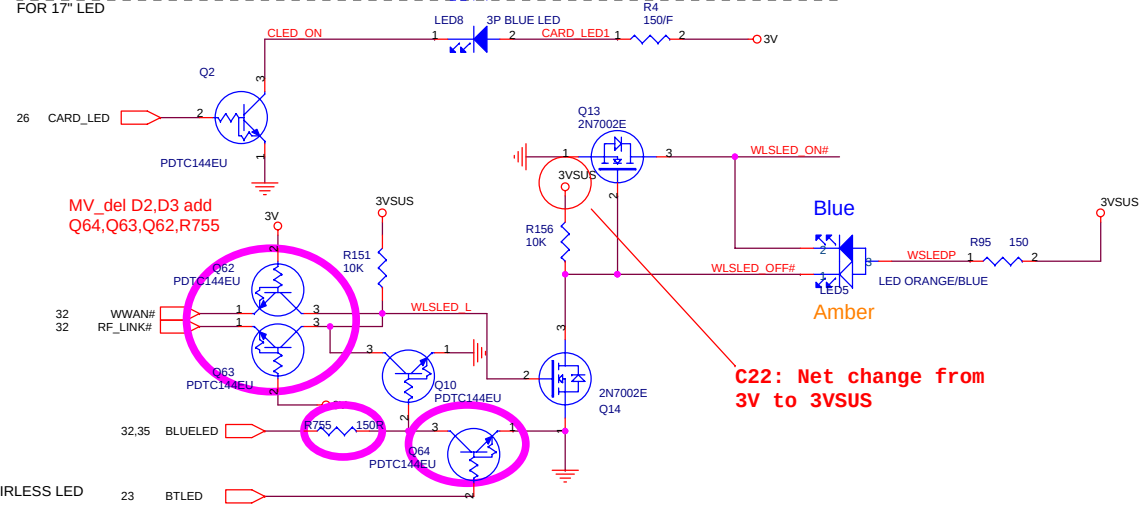
C21: change CN4,CN6 Footprint BOM change to DFFC12FR293



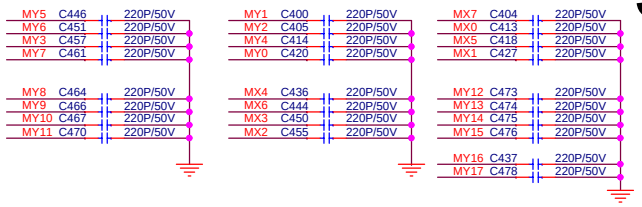
FOR 15.4" LED



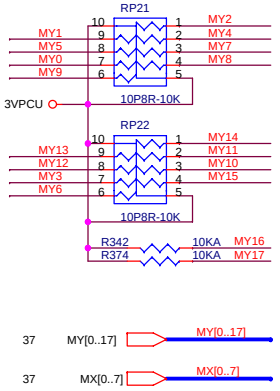
FOR 17" LED

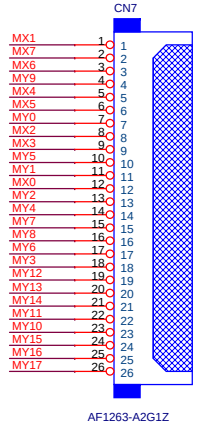


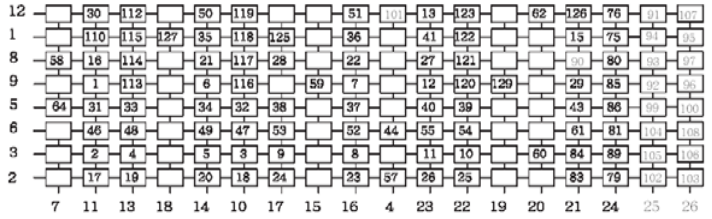
FOR WIRLESS LED



KEYBOARD PULL-UP







NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	2A

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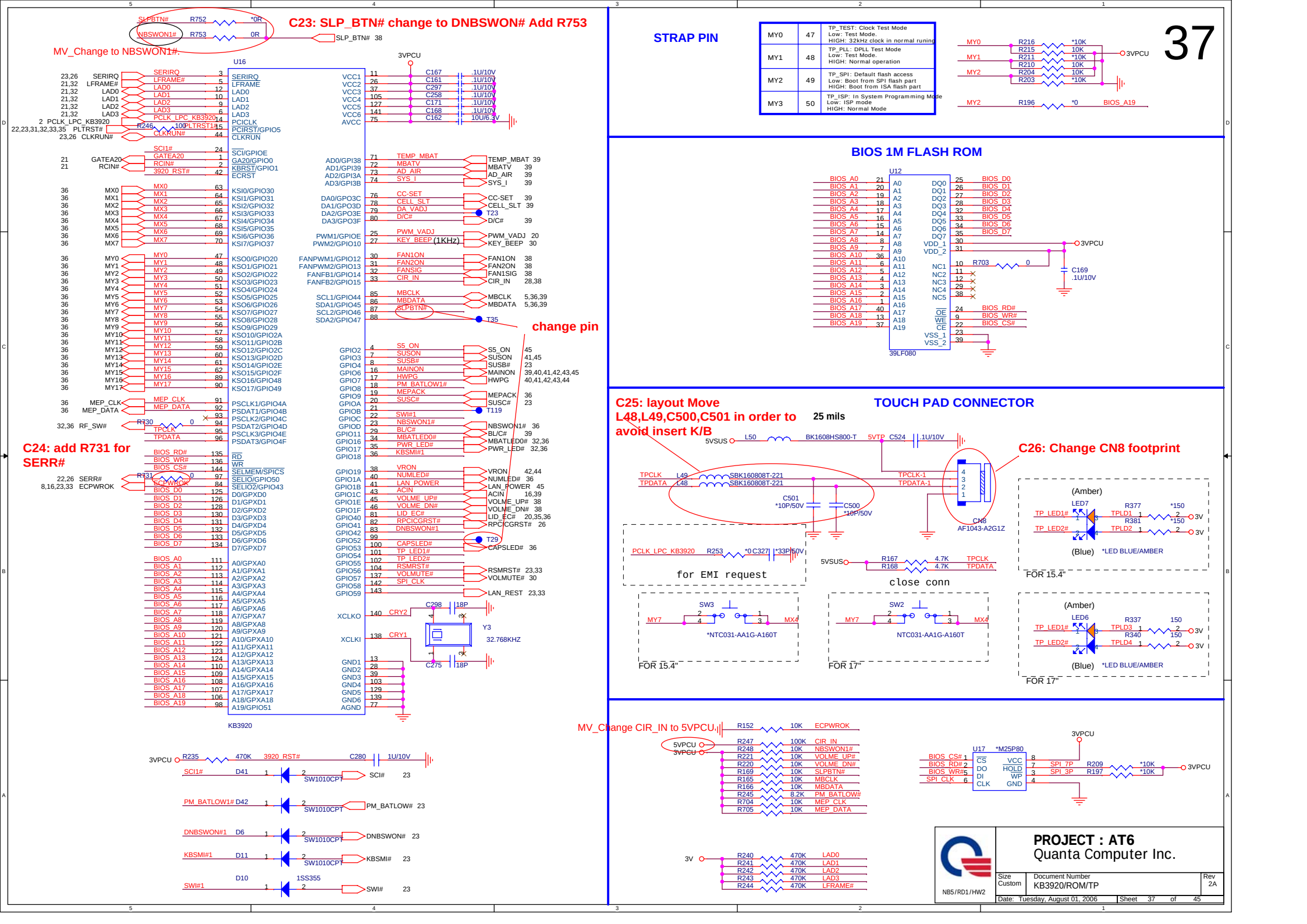
C23: SLP_BTN# change to DNBSWON# Add R753
MV_Change to NBSWON1#.
SLPBTN# R752 *0R
NBSWON1# R753 0R
SLP_BTN# 38
U16
KB3920
C24: add R731 for SERR#
change pin
R731 0
22,26 SERR#
8,16,23,33 ECPWROK
STRAP PIN
MY0 47 TP_TEST: Clock Test Mode Low: Test Mode. HIGH: 32kHz clock in normal runing
MY1 48 TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: Normal operation
MY2 49 TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3 50 TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode
R216 *10K
R215 10K
R211 *10K
R210 10K
R204 10K
R203 *10K
R196 *0
BIOS_A19
3VPCU
37
BIOS 1M FLASH ROM
U12
39LF080
R703 0
C169 .1U/10V
C25: layout Move L48,L49,C500,C501 in order to avoid insert K/B
25 mils
TOUCH PAD CONNECTOR
C26: Change CN8 footprint
5VSUS
L50 BK1608HS800-T
5VTP C524 .1U/10V
TPCLK L49 SBK160808T-221
TPDATA L48 SBK160808T-221
TPCLK-1
TPDATA-1
C501 *10P/50V
C500 *10P/50V
CN8 AF1043-A2G1Z
PCLK_LPC_KB3920 R253 *0 C327 *33P/50V
for EMI request
R167 4.7K TPCLK
R168 4.7K TPDATA
close conn
SW3 MY7 MX4 *NTC031-AA1G-160T
FOR 15.4"
SW2 MY7 MX4 NTC031-AA1G-160T
FOR 17"
(Amber) LED7 R377 *150 R381 *150
TP_LED1# TPLD1
TP_LED2# TPLD2
3V
(Blue) *LED BLUE/AMBER
FOR 15.4"
(Amber) LED6 R337 150 R340 150
TP_LED1# TPLD3
TP_LED2# TPLD4
3V
(Blue) *LED BLUE/AMBER
FOR 17"
MV_Change CIR_IN to 5VPCU.
5VPCU
3VPCU
R152 10K ECPWROK
R247 100K CIR_IN
R248 10K NBSWON1#
R221 10K VOLME_UP#
R220 10K VOLME_DN#
R169 10K SLPBTN#
R165 10K MBCLK
R166 10K MBDATA
R245 8.2K PM_BATLOW#
R704 10K MEP_CLK
R705 10K MEP_DATA
3V
R240 470K LAD0
R241 470K LAD1
R242 470K LAD2
R243 470K LAD3
R244 470K LFRAME#
U17 *M25P80
BIOS_CS# BIOS_RD# BIOS_WR# SPI_CLK
CS DO DI CLK VCC HOLD WP GND
SPI_7P SPI_3P R209 R197 *10K *10K
3VPCU
R235 470K 3920_RST# C280 1U/10V
SCI1# D41 SW1010CPT SCI# 23
PM_BATLOW1# D42 SW1010CPT PM_BATLOW# 23
DNBSWON#1 D6 SW1010CPT DNBSWON# 23
KBSMI#1 D11 SW1010CPT KBSMI# 23
D10 1SS355
SWI#1 SWI# 23
C298 18P
Y3 32.768KHZ
C275 18P
CRY2
CRY1
XCLKO
XCLKI
PROJECT : AT6
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number KB3920/ROM/TP
Rev 2A
Date: Tuesday, August 01, 2006
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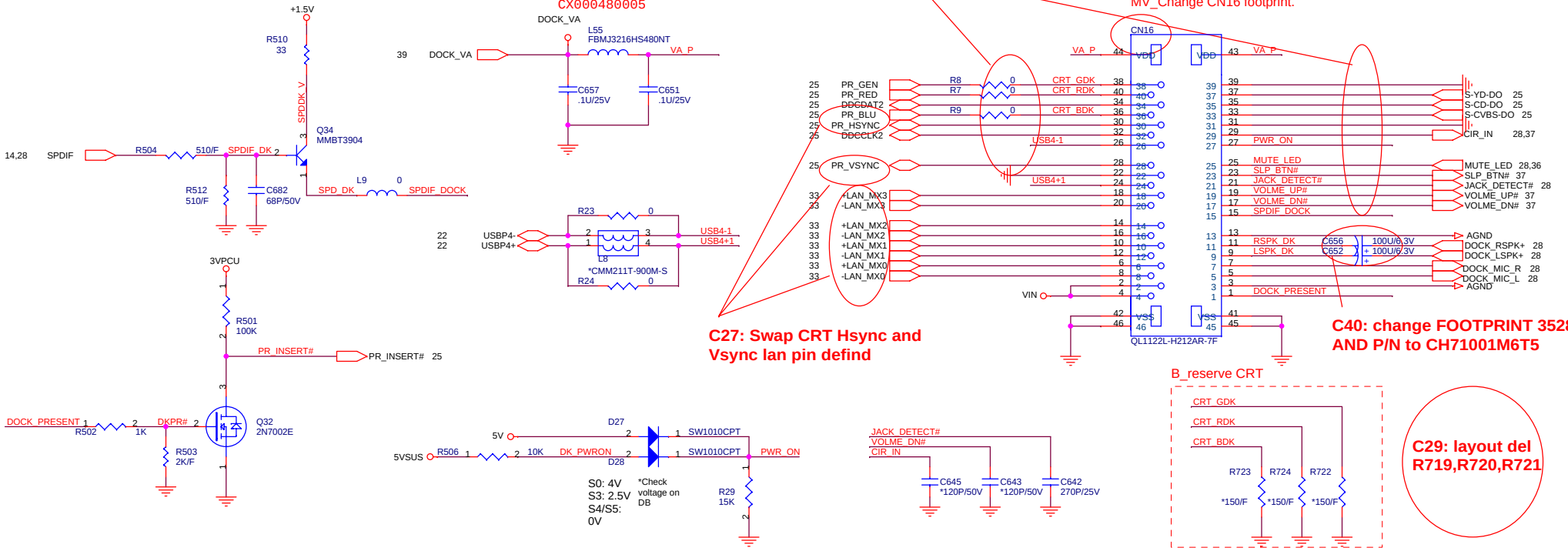
CABLE DOCK

C28: Del R1,R2,R3,R5,R477,R478,R479,R480,R476,R12,R475,R474,R22

support 6A 200mils
CX000480005

MV_Change CN16 footprint.



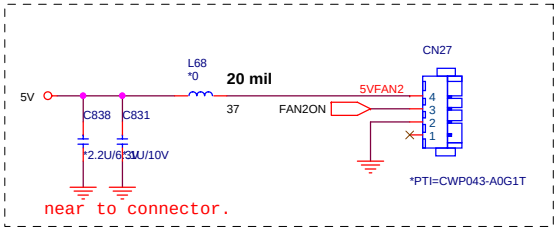
C27: Swap CRT Hsync and Vsync lan pin defind

C40: change FOOTPRINT 3528 AND P/N to CH71001M6T5

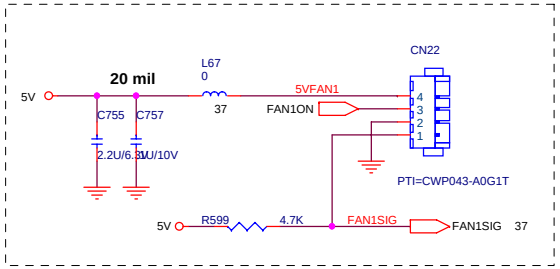
B_reserve CRT

C29: layout del R719,R720,R721

FAN



FAN2 PWM CONNECTOR



FAN1 PWM CONNECTOR

NB5/RD1/HW2	PROJECT : AT6 Quanta Computer Inc.	
	Size: Custom Document Number: CABLE DOCKING/FAN	Rev: 2A
	Date: Tuesday, August 01, 2006	Sheet 38 of 45

C30: Add PD22 for 12cell battery issue

TOP DC_JACK
65W/90W

CELL_SLT = 1 -- 3 S
CELL_SLT = 0 -- 4 S

Battery
6/8/12cell

Iinput=Vcls/Vref * 0.075/RS1
Vref=4.096V,RS1=10m-ohm

ADP	PR141
65W	36.5K/F
90W	20K/F

Battery Low = 8V

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

Change net name from 8724DCIN to VAD-1

PROJECT : AT6
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	SYSTEM CHARGER(MAX8724)	1A

Date: Tuesday, August 01, 2006 Sheet 39 of 45

DC-DC(MAX8734A)

C31: change PR91 value 100K to 150K(RC0402) Add PC175 .1u

C32: change 2.5V power source from 3VSUS to 3VPCU

(7A / 9A Peak)

(7A / 9A Peak)

(1.1A)

2.55A

2A

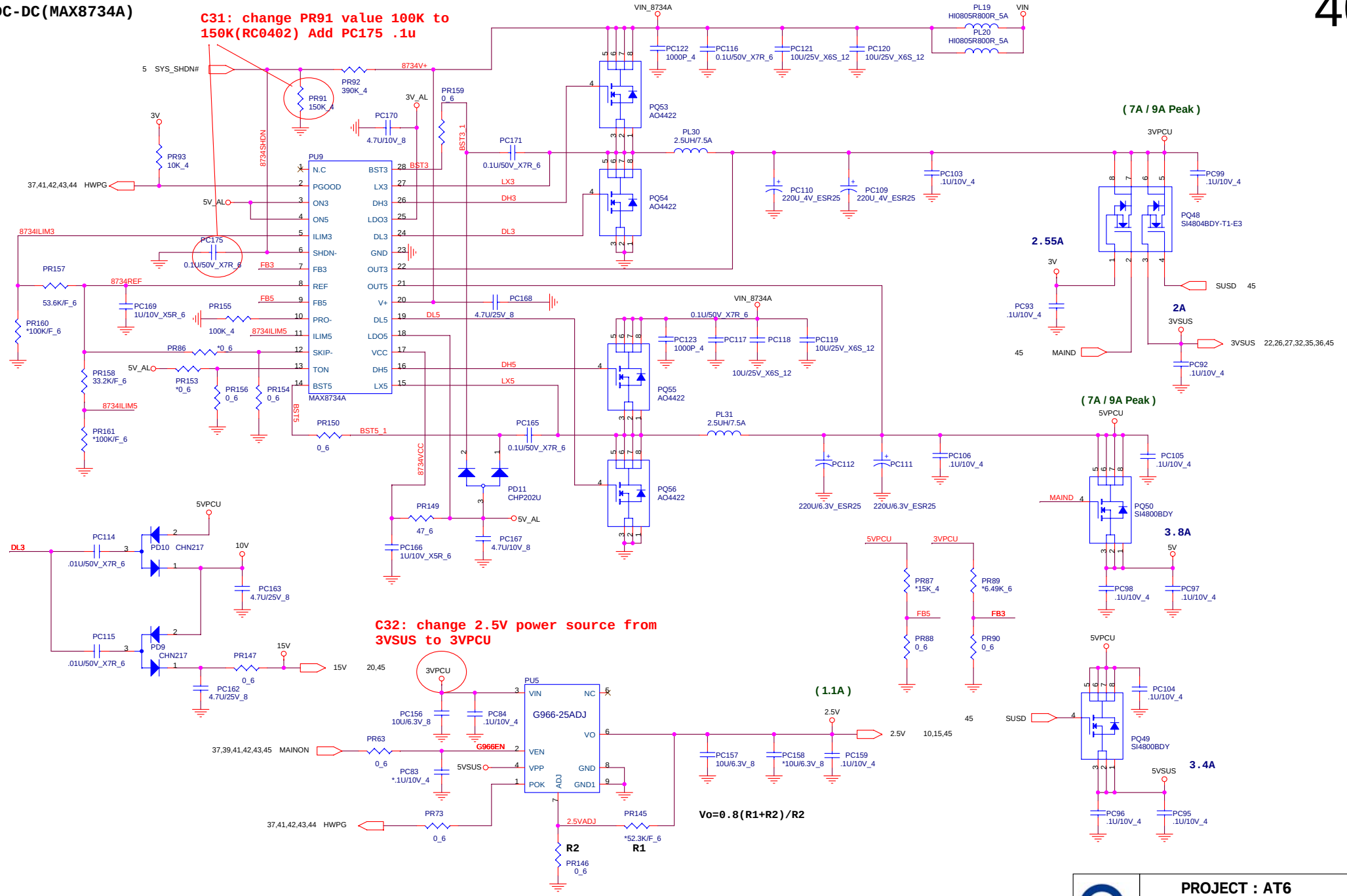
3.8A

3.4A

Vo=0.8(R1+R2)/R2

R2

R1

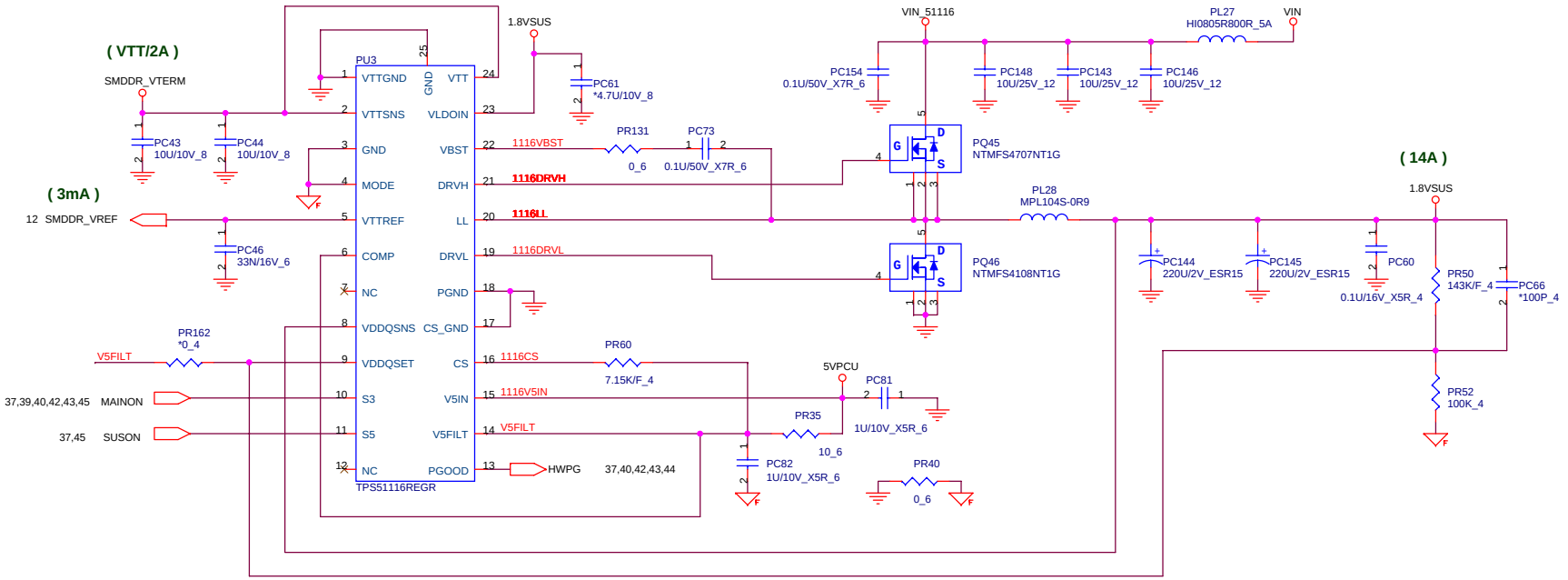


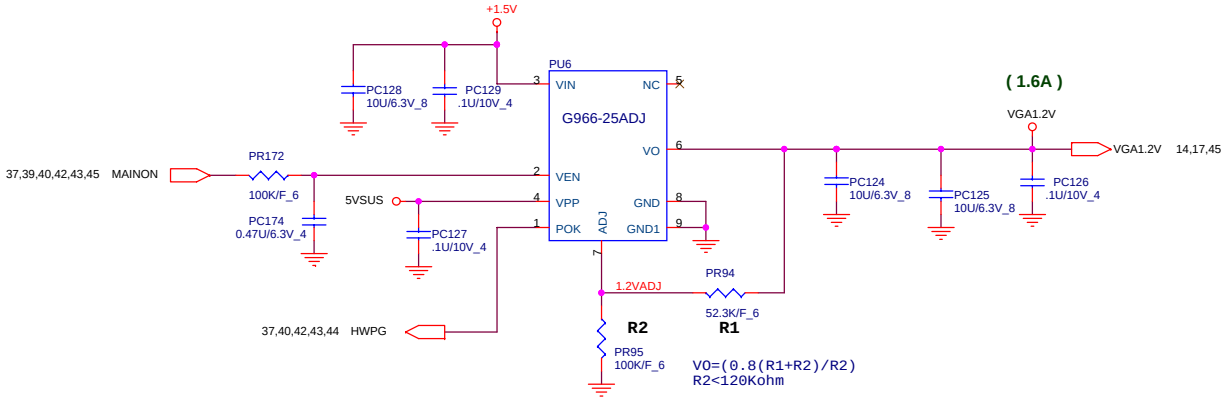
PROJECT : AT6
Quanta Computer Inc.

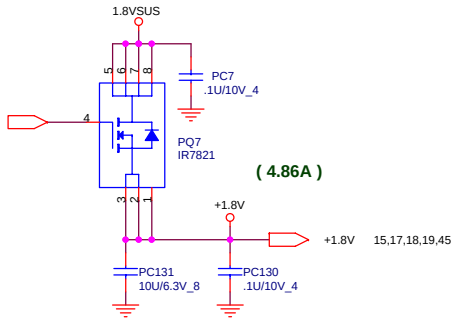
Size	Document Number	Rev
Custom	SYS PWR 5V/3.3V(MAX8734A)	2A

NB5/RD1/HW2

Date: Tuesday, August 01, 2006 Sheet 40 of 45







PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	2A

NB5/RD1/HW2

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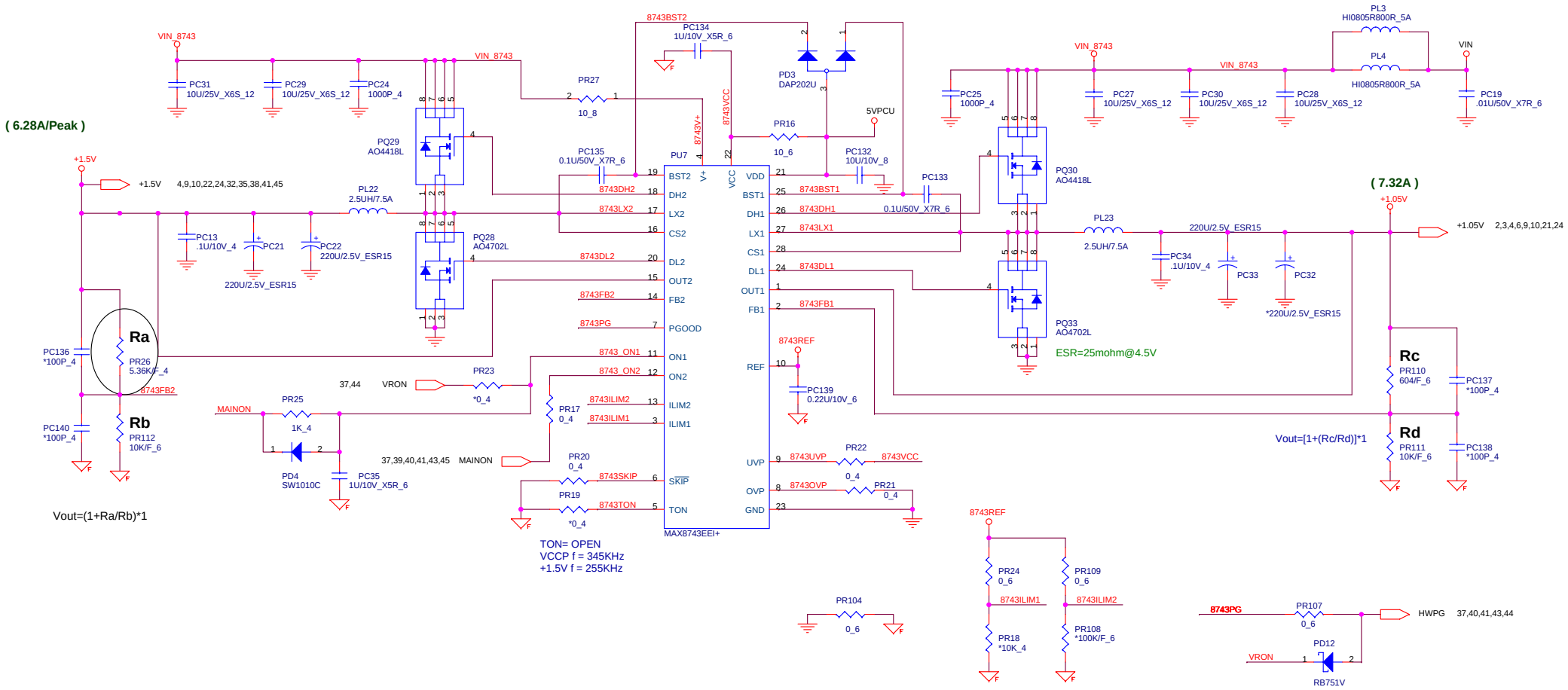
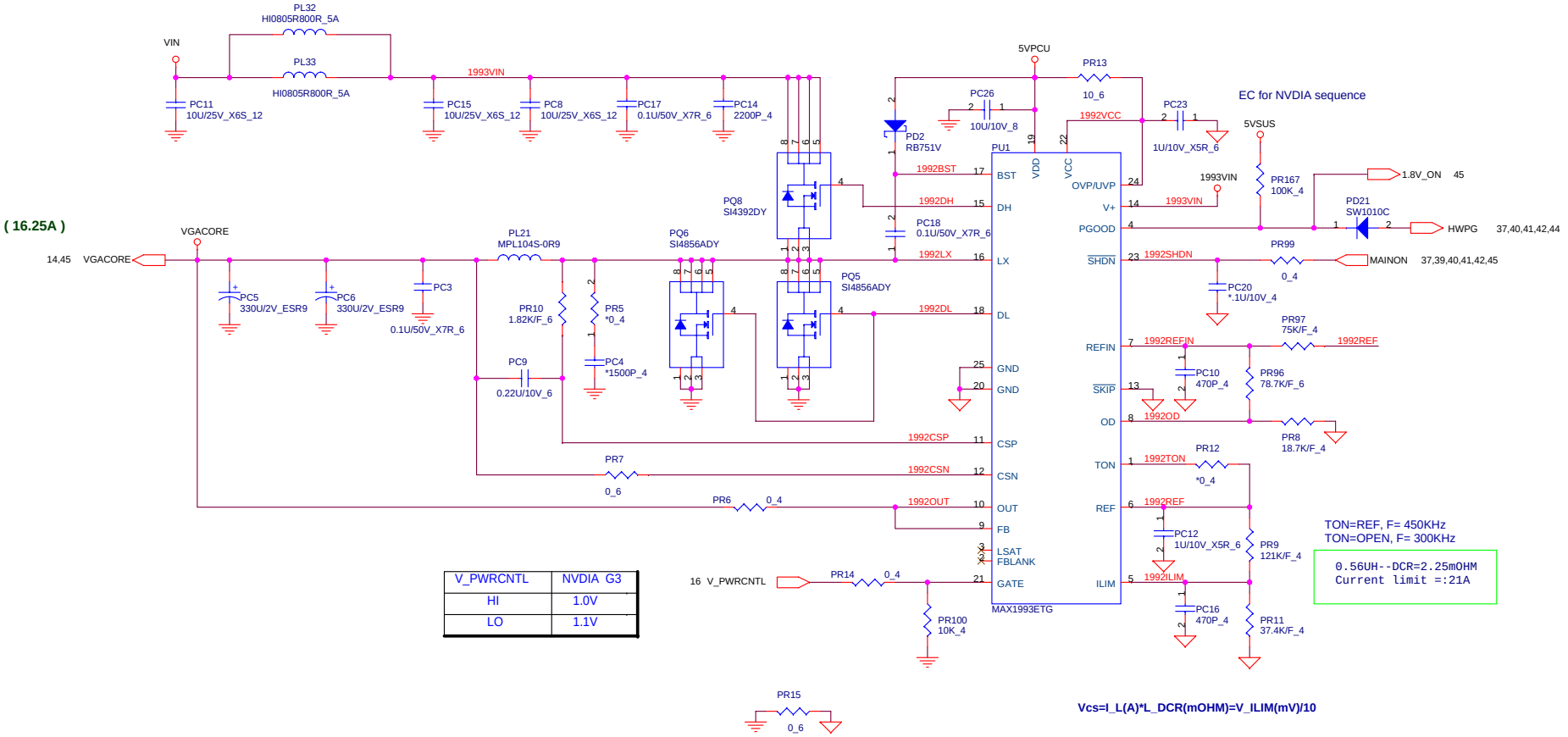


NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
Date: Tuesday, August 01, 2006	Sheet 42 of 45	

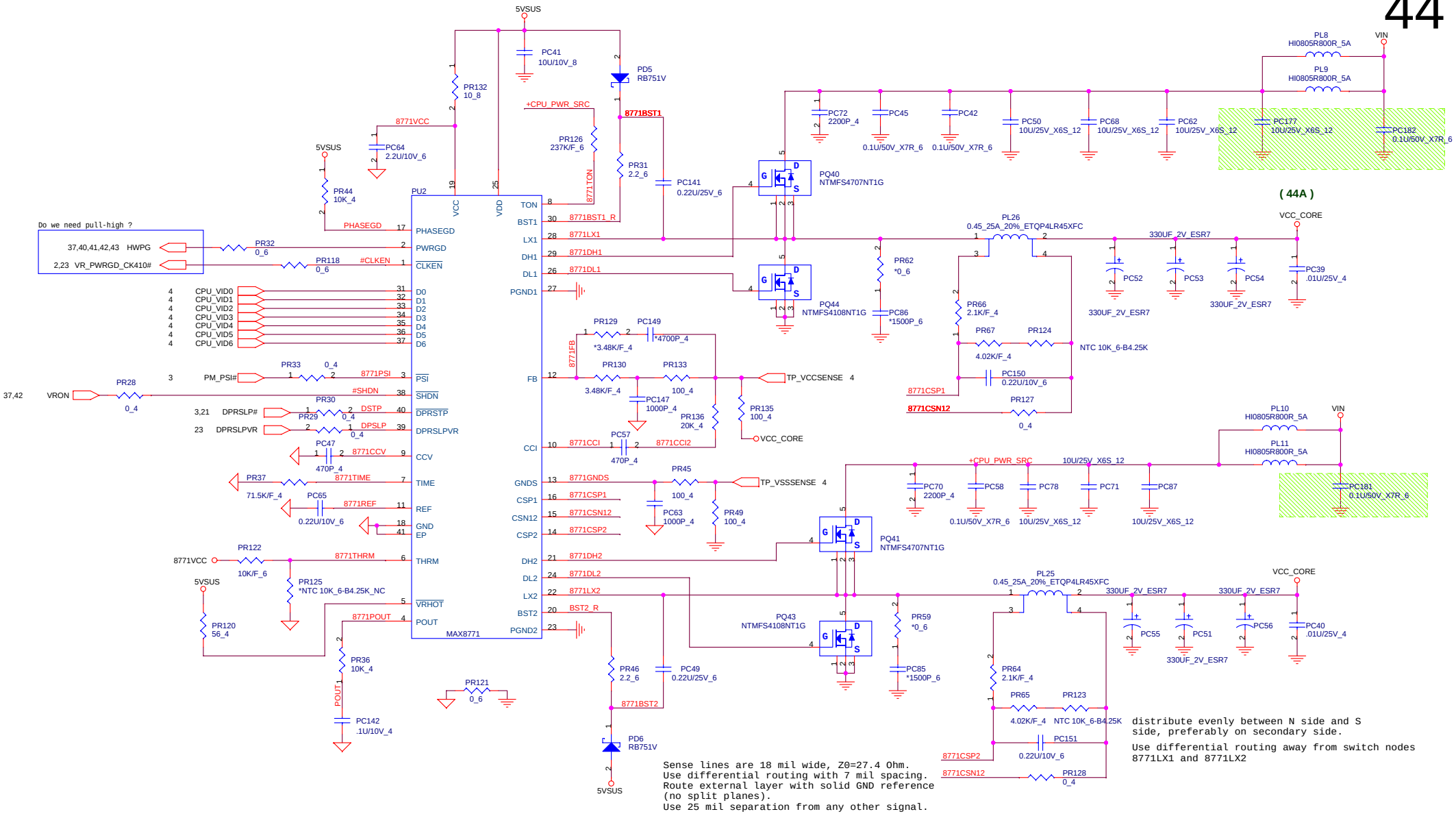


V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

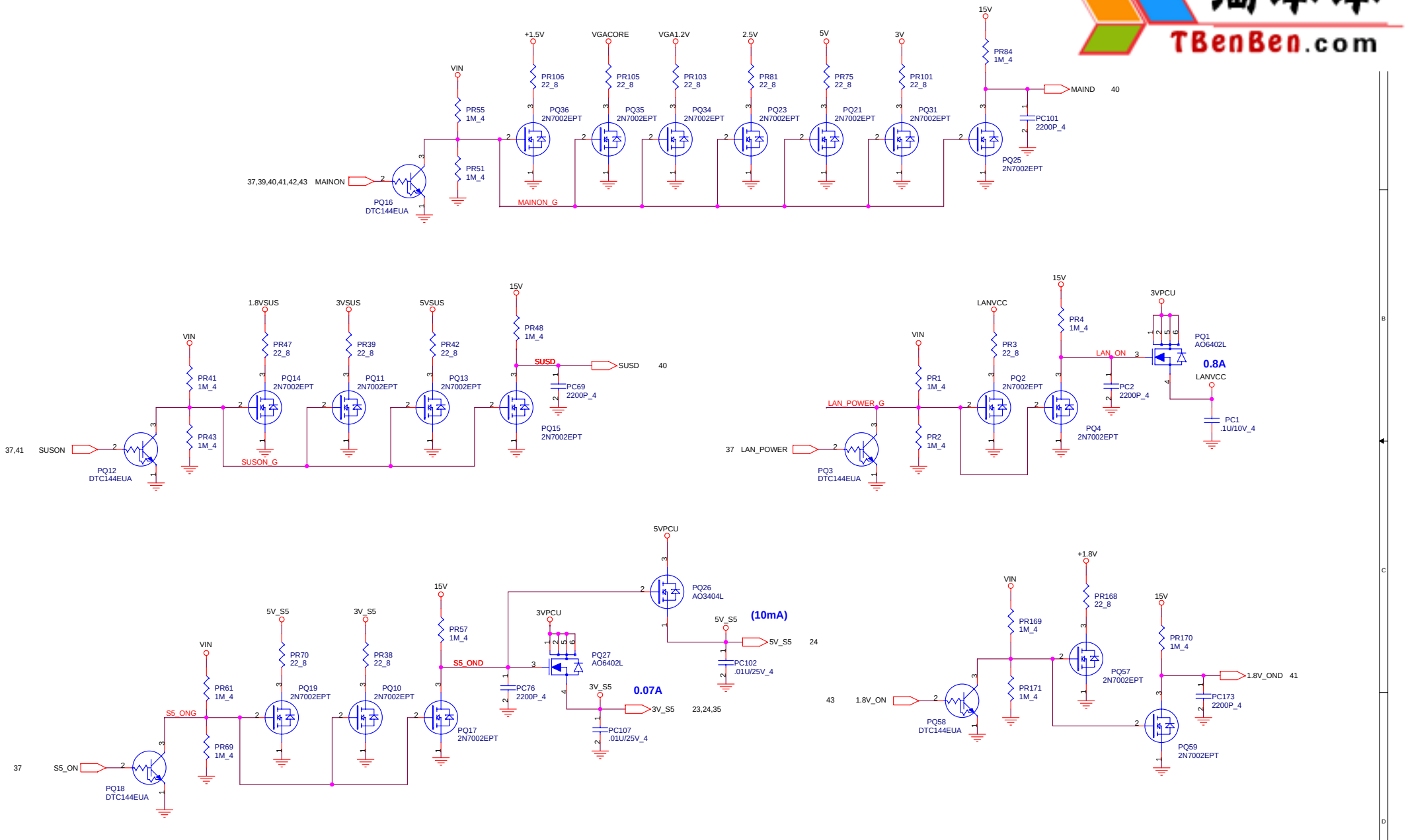
PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGACORE (MAX1993)	2A
Date: Tuesday, August 01, 2006	Sheet 43 of 45	

NB5/RD1/HW2



NB5/RD1/HW2	**PROJECT : AT6** Quanta Computer Inc.	
Size: Custom	Document Number: CPU_CORE(MAX8771)	Rev: 1A
Date: Tuesday, August 01, 2006	Sheet 44 of 45	



PROJECT : AT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	2A
Date: Tuesday, August 01, 2006	Sheet 45 of 45	

NB5/RD1/HW2