

Compal Confidential

ICW50 Schematics Document

AMD Turion/Sempron + Nvidia MCP67-MV

2007 / 04 / 20

Rev:1.0

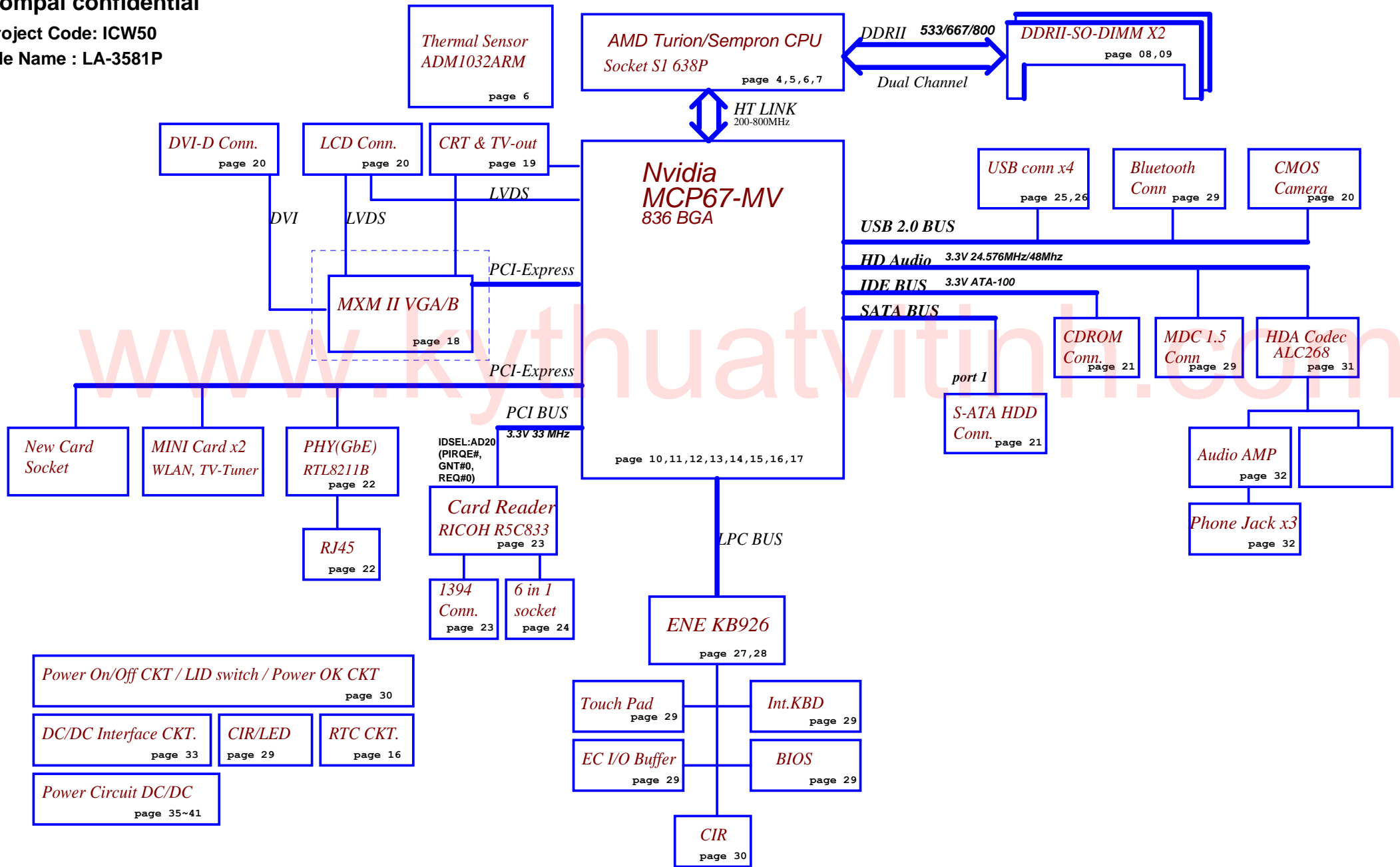
FOR Pre-MP

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Cover Sheet	
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Compal confidential

Project Code: ICW50

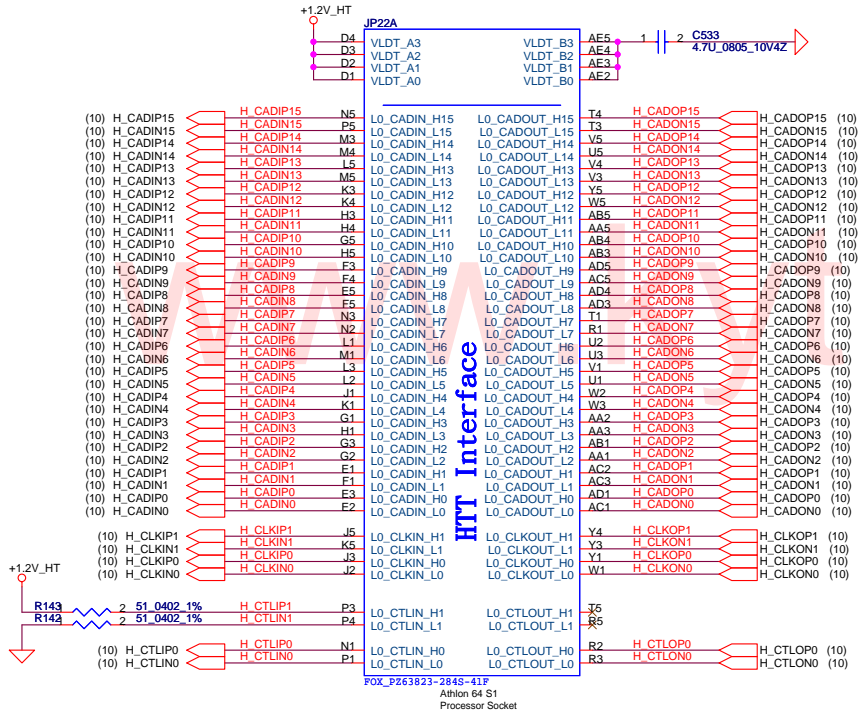
File Name : LA-3581P



Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	BLOCK DIAGRAM	
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				Rev	1.0

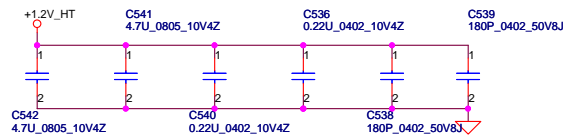
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

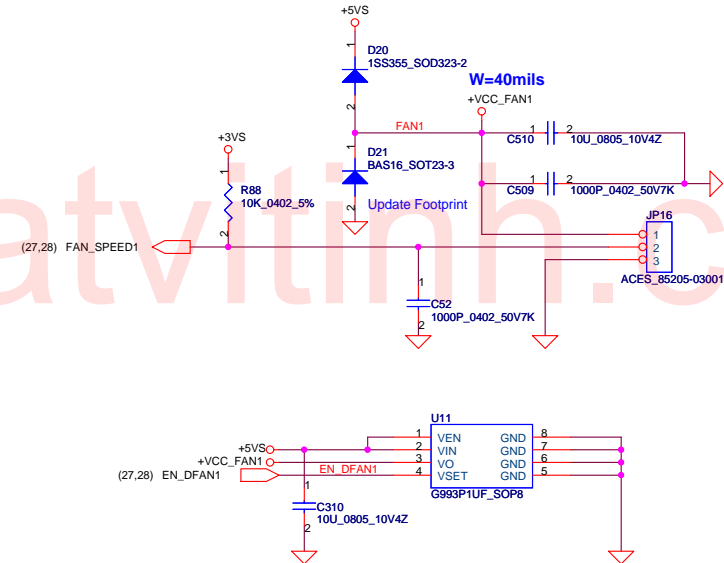


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS. PLACE CLOSE TO VLDTO POWER PINS



FAN Conn

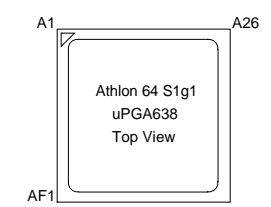
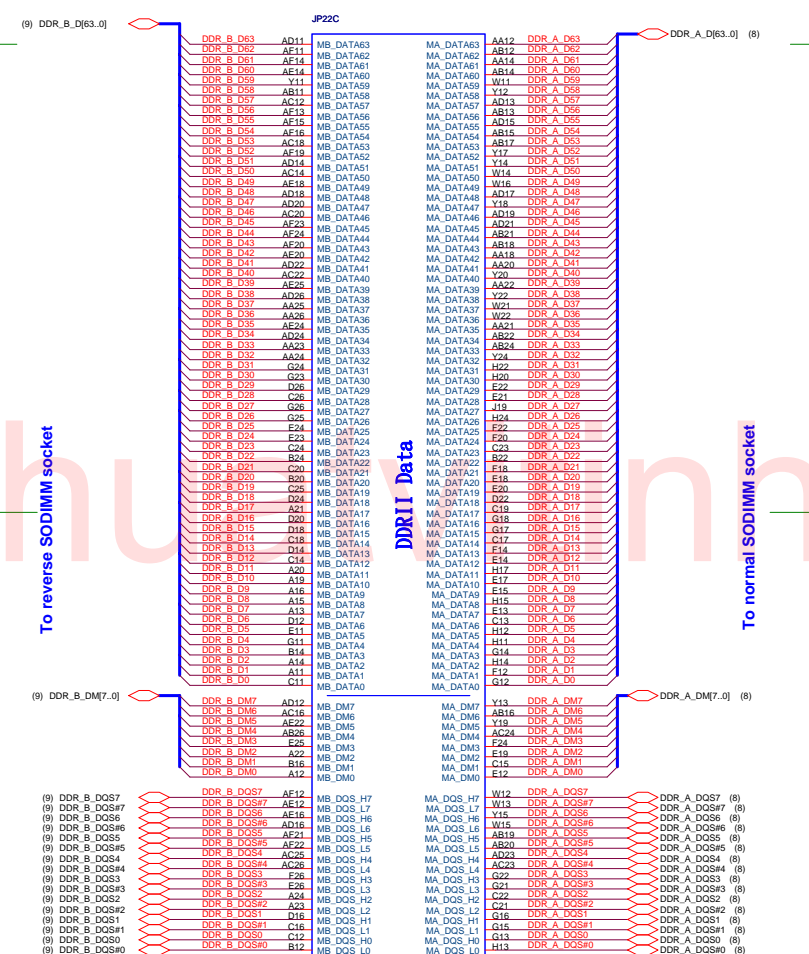
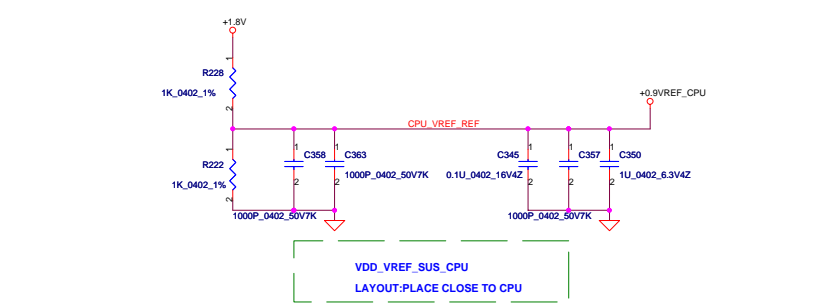
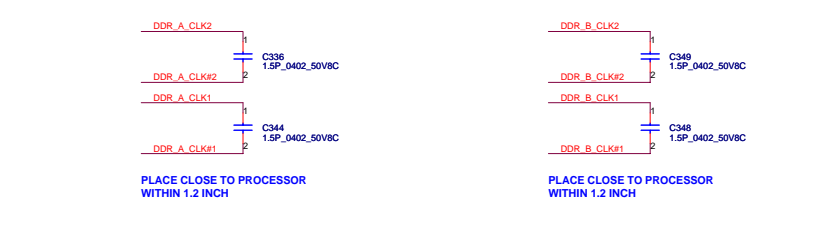
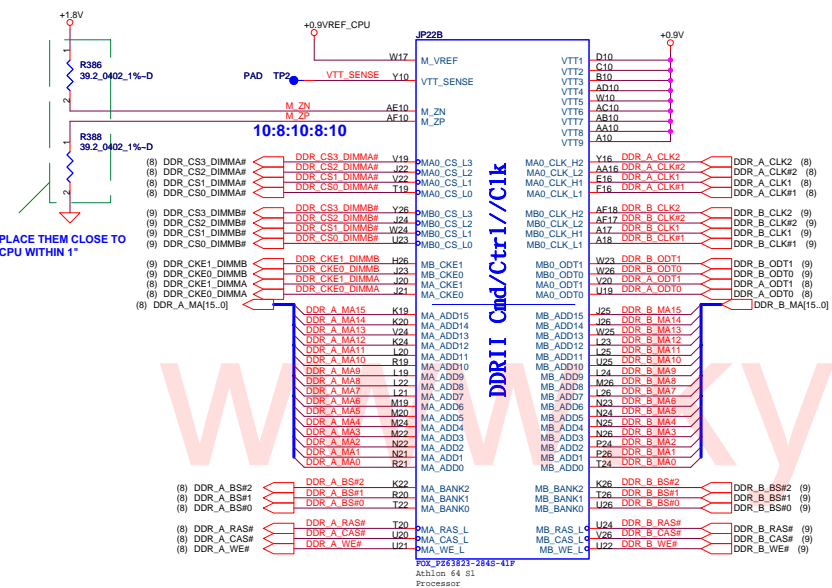


FAN1 Conn

Security Classification		Compal Secret Data		Title		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	AMD CPU HT I/F		
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Processor DDR2 Memory Interface

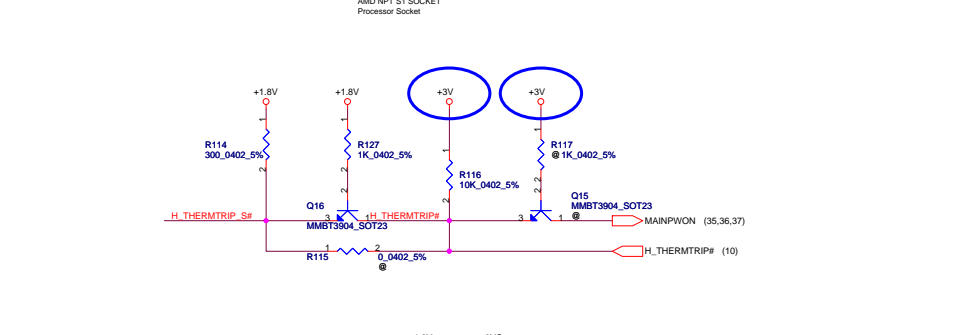
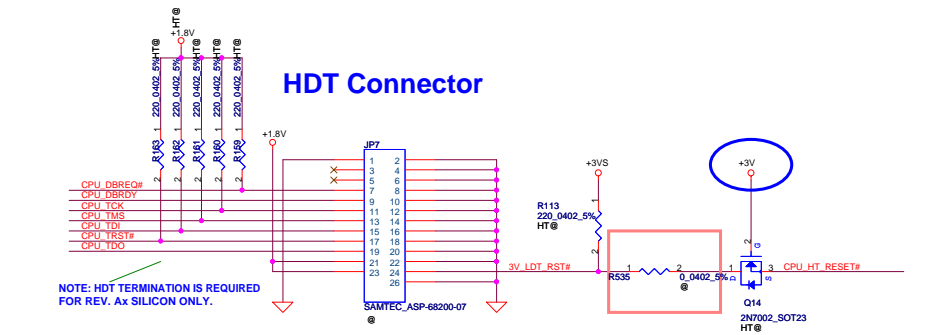
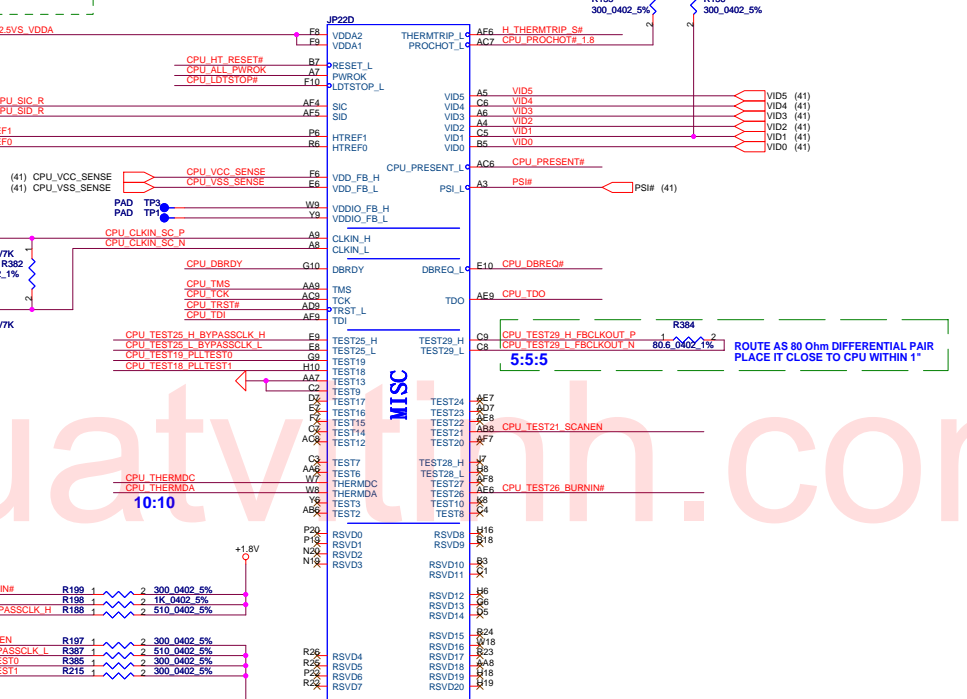
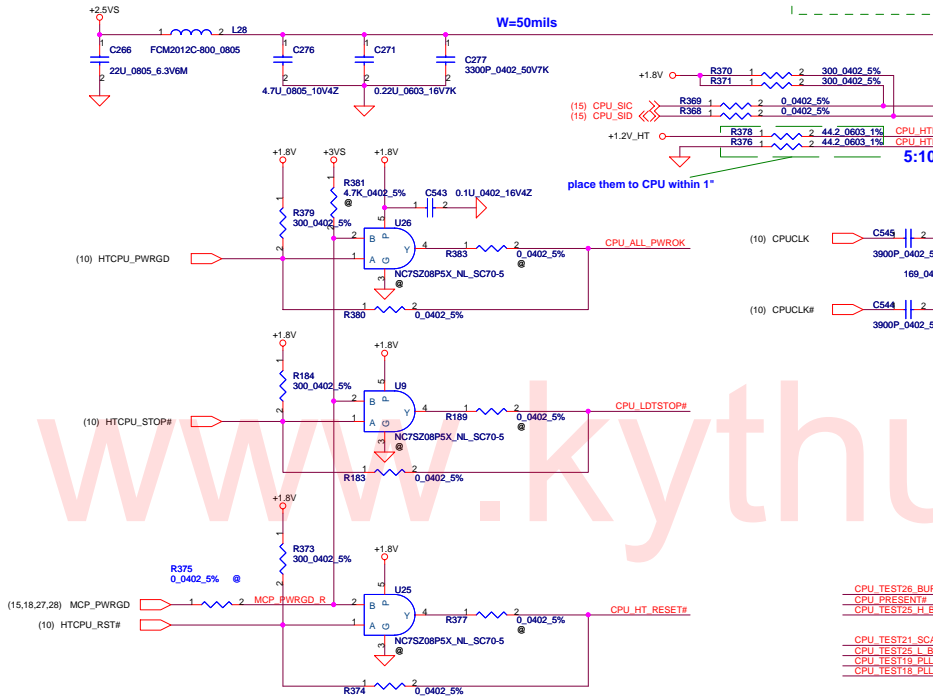
VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



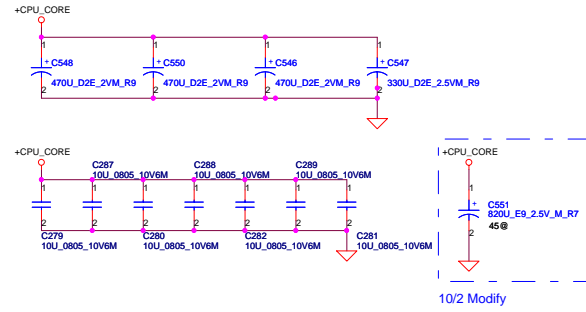
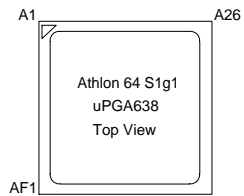
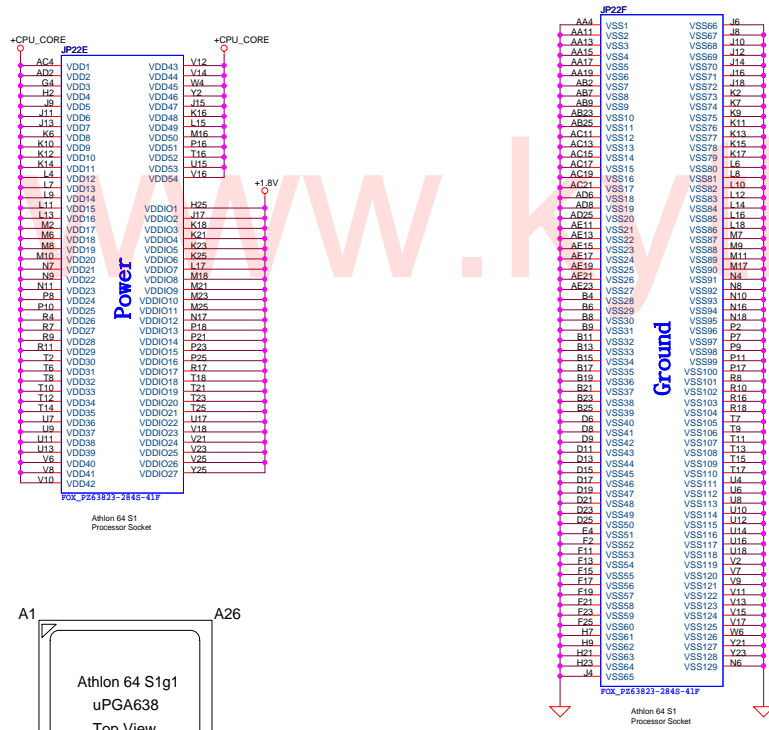
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ATHLON Control and Debug

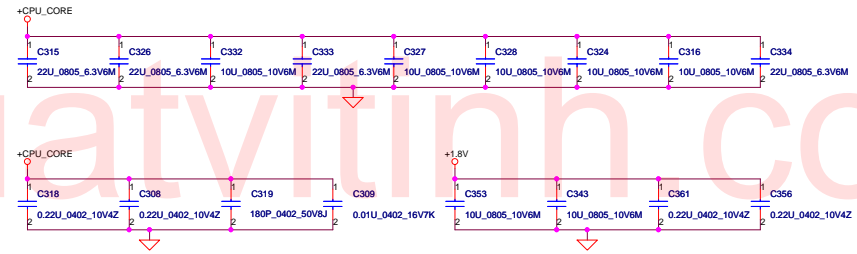
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x23 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.



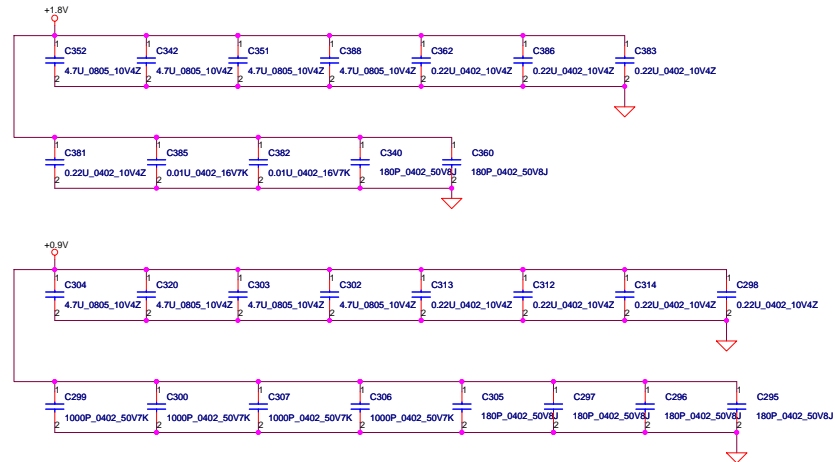
PROCESSOR POWER AND GROUND



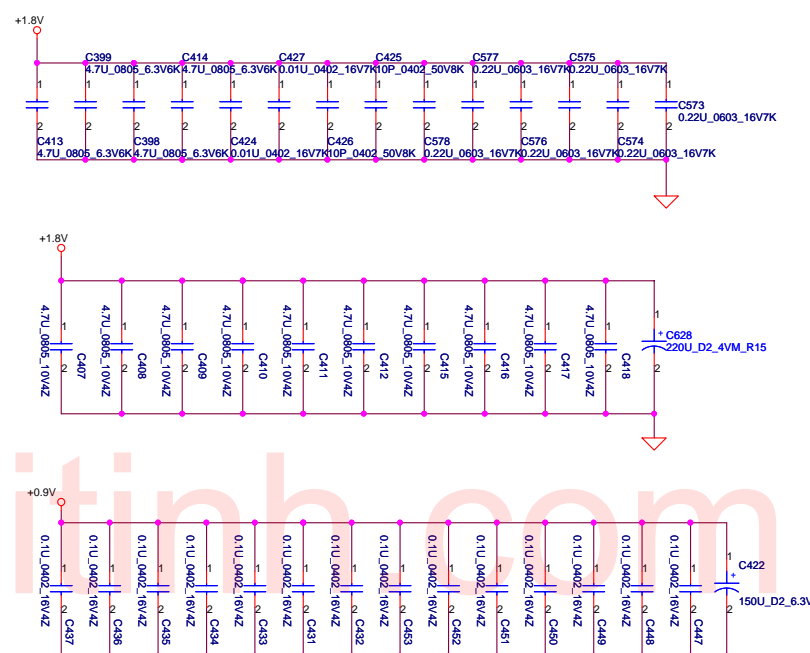
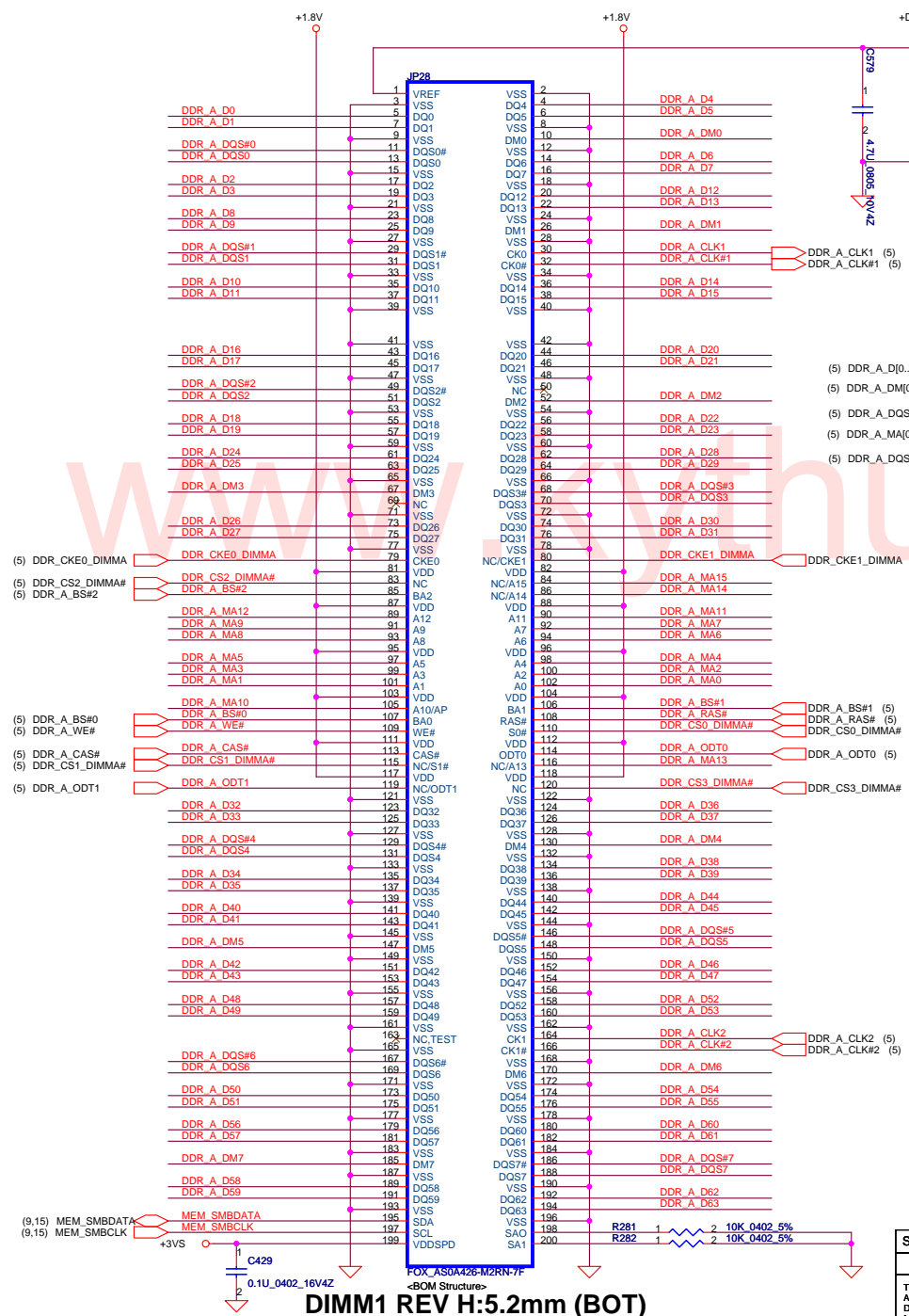
CPU SOCKET S1 DECOUPLING



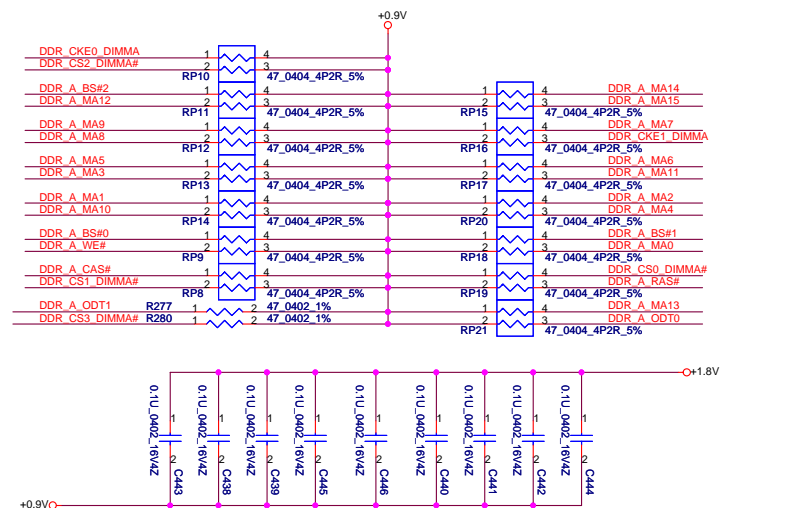
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



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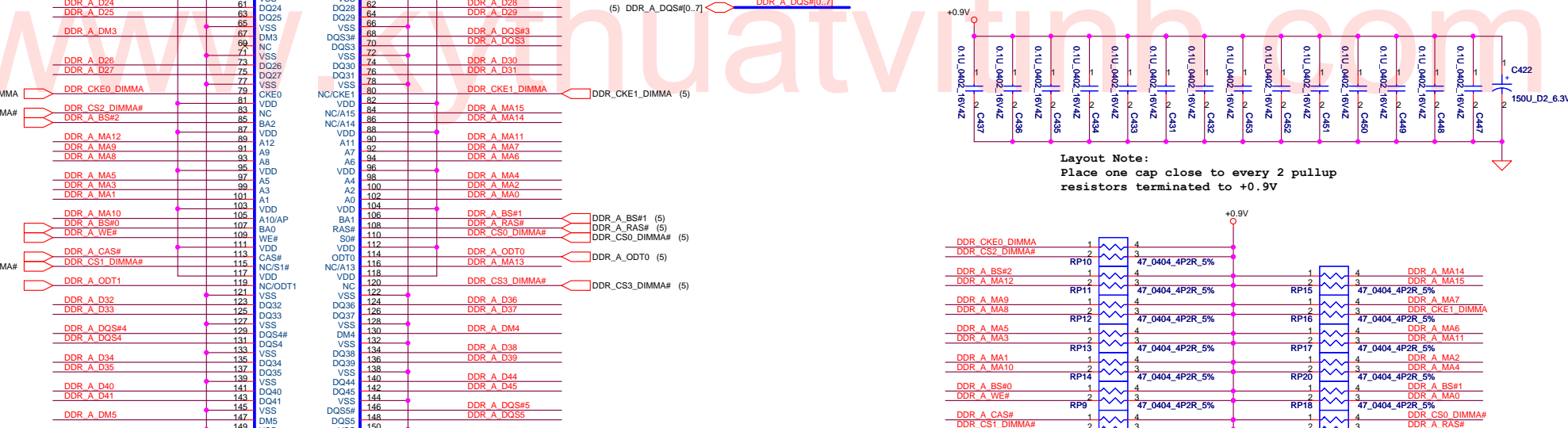


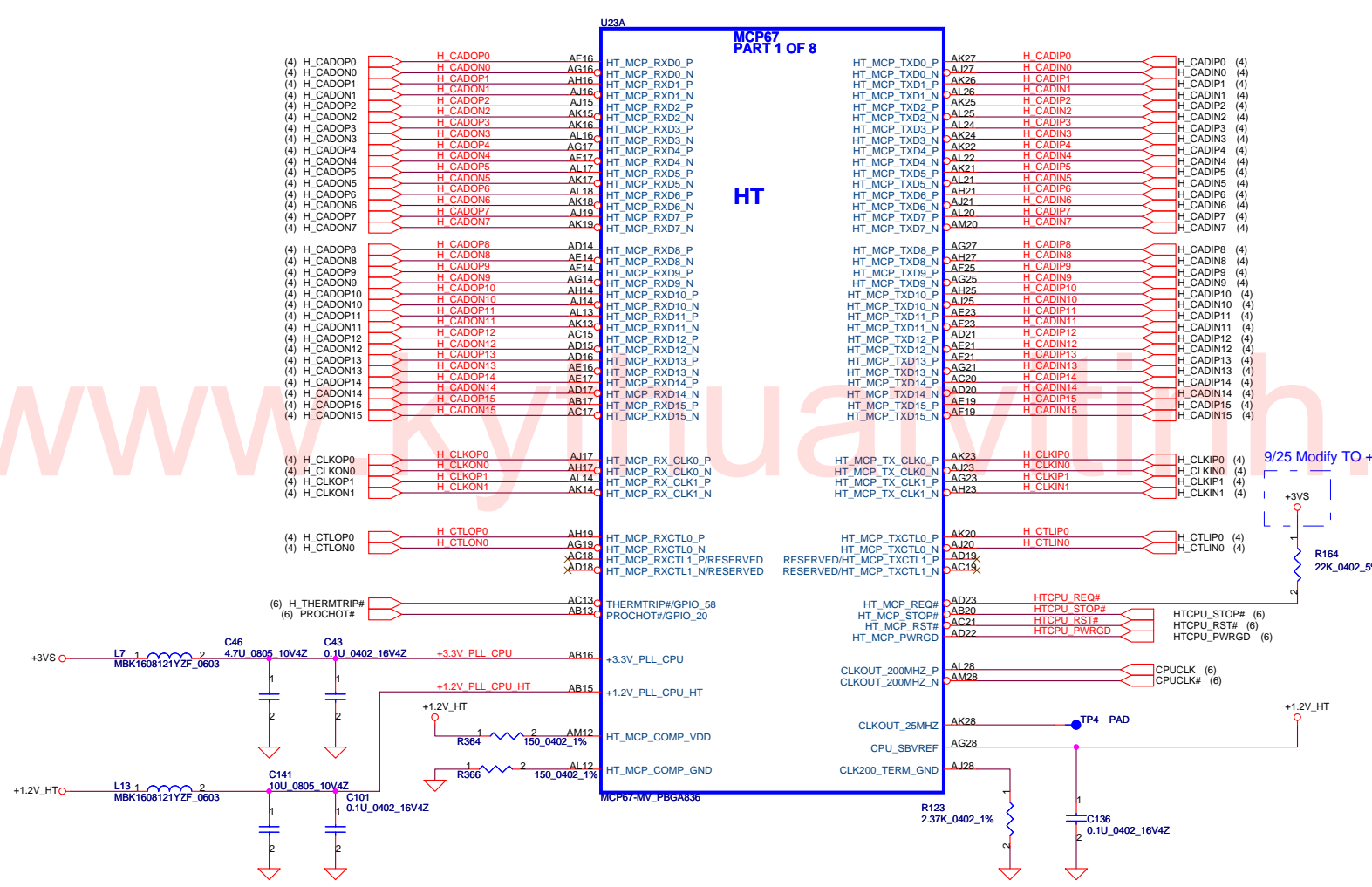
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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9/25 Modify TO +3VS

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(18) PCIE_GTX_C_MRX_P[0..15] PCIE GTX C_MRX_P[0..15]
 (18) PCIE_GTX_C_MRX_N[0..15] PCIE GTX C_MRX_N[0..15]

(18) PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX_P[0..15]
 (18) PCIE_MTX_C_GRX_N[0..15] PCIE MTX C GRX_N[0..15]

U238
MVP67 PART 2 OF 8

CLOSE TO CONNECT

PCIE GFX I/F

- PCIE GTX C_MRX_P0 F23
- PCIE GTX C_MRX_N0 G23
- PCIE GTX C_MRX_P1 F24
- PCIE GTX C_MRX_N1 G24
- PCIE GTX C_MRX_P2 D25
- PCIE GTX C_MRX_N2 D26
- PCIE GTX C_MRX_P3 C28
- PCIE GTX C_MRX_N3 C29
- PCIE GTX C_MRX_P4 D28
- PCIE GTX C_MRX_N4 C30
- PCIE GTX C_MRX_P5 D29
- PCIE GTX C_MRX_N5 D30
- PCIE GTX C_MRX_P6 F26
- PCIE GTX C_MRX_N6 F27
- PCIE GTX C_MRX_P7 F28
- PCIE GTX C_MRX_N7 F29
- PCIE GTX C_MRX_P8 H23
- PCIE GTX C_MRX_N8 H24
- PCIE GTX C_MRX_P9 H24
- PCIE GTX C_MRX_N9 H26
- PCIE GTX C_MRX_P10 H27
- PCIE GTX C_MRX_N10 H28
- PCIE GTX C_MRX_P11 K24
- PCIE GTX C_MRX_N11 K25
- PCIE GTX C_MRX_P12 K27
- PCIE GTX C_MRX_N12 K26
- PCIE GTX C_MRX_P13 K28
- PCIE GTX C_MRX_N13 K29
- PCIE GTX C_MRX_P14 J31
- PCIE GTX C_MRX_N14 J30
- PCIE GTX C_MRX_P15 K31
- PCIE GTX C_MRX_N15 K30

- D24 PCIE MTX GRX_P0
- C24 PCIE MTX GRX_N0
- B24 PCIE MTX GRX_P1
- C167 1 2 0.1U 0402 16V7K VGA@ C166 1 2 0.1U 0402 16V7K
- B25 PCIE MTX GRX_P2
- C196 1 2 0.1U 0402 16V7K VGA@ C195 1 2 0.1U 0402 16V7K
- C25 PCIE MTX GRX_N2
- B26 PCIE MTX GRX_P3
- C169 1 2 0.1U 0402 16V7K VGA@ C168 1 2 0.1U 0402 16V7K
- C26 PCIE MTX GRX_N3
- D27 PCIE MTX GRX_P4
- C198 1 2 0.1U 0402 16V7K VGA@ C197 1 2 0.1U 0402 16V7K
- D28 PCIE MTX GRX_N4
- A28 PCIE MTX GRX_P5
- C171 1 2 0.1U 0402 16V7K VGA@ C170 1 2 0.1U 0402 16V7K
- B28 PCIE MTX GRX_N5
- A29 PCIE MTX GRX_P6
- C199 1 2 0.1U 0402 16V7K VGA@ C198 1 2 0.1U 0402 16V7K
- B29 PCIE MTX GRX_N6
- C200 1 2 0.1U 0402 16V7K VGA@ C199 1 2 0.1U 0402 16V7K
- A30 PCIE MTX GRX_P7
- C172 1 2 0.1U 0402 16V7K VGA@ C171 1 2 0.1U 0402 16V7K
- B30 PCIE MTX GRX_N7
- C173 1 2 0.1U 0402 16V7K VGA@ C172 1 2 0.1U 0402 16V7K
- B31 PCIE MTX GRX_P8
- C201 1 2 0.1U 0402 16V7K VGA@ C200 1 2 0.1U 0402 16V7K
- C32 PCIE MTX GRX_N8
- C202 1 2 0.1U 0402 16V7K VGA@ C199 1 2 0.1U 0402 16V7K
- C31 PCIE MTX GRX_P9
- C174 1 2 0.1U 0402 16V7K VGA@ C173 1 2 0.1U 0402 16V7K
- C32 PCIE MTX GRX_N9
- C175 1 2 0.1U 0402 16V7K VGA@ C174 1 2 0.1U 0402 16V7K
- D31 PCIE MTX GRX_P10
- C203 1 2 0.1U 0402 16V7K VGA@ C202 1 2 0.1U 0402 16V7K
- D32 PCIE MTX GRX_N10
- C204 1 2 0.1U 0402 16V7K VGA@ C203 1 2 0.1U 0402 16V7K
- E30 PCIE MTX GRX_P11
- C176 1 2 0.1U 0402 16V7K VGA@ C175 1 2 0.1U 0402 16V7K
- E31 PCIE MTX GRX_N11
- C177 1 2 0.1U 0402 16V7K VGA@ C176 1 2 0.1U 0402 16V7K
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- C228 1 2 0.1U 0402 16V7K VGA@ C227 1 2 0.1U 0402 16V7K
- F30 PCIE MTX GRX_N12
- C229 1 2 0.1U 0402 16V7K VGA@ C228 1 2 0.1U 0402 16V7K
- G29 PCIE MTX GRX_P13
- C237 1 2 0.1U 0402 16V7K VGA@ C236 1 2 0.1U 0402 16V7K
- G28 PCIE MTX GRX_N13
- C238 1 2 0.1U 0402 16V7K VGA@ C237 1 2 0.1U 0402 16V7K
- H29 PCIE MTX GRX_P14
- C230 1 2 0.1U 0402 16V7K VGA@ C229 1 2 0.1U 0402 16V7K
- H30 PCIE MTX GRX_N14
- C231 1 2 0.1U 0402 16V7K VGA@ C230 1 2 0.1U 0402 16V7K
- H31 PCIE MTX GRX_P15
- C239 1 2 0.1U 0402 16V7K VGA@ C238 1 2 0.1U 0402 16V7K
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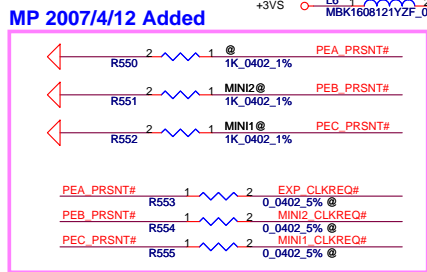
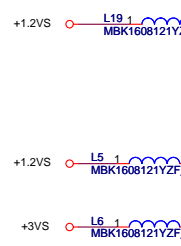


(25,26,27) MCP_PCIE_WAKE#
 (18) PE_PRSNTX16#

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 (26) PCIE_MRX_PTX_N1
 (26) EXP_CLKREQ#

(25) PCIE_MRX_PTX_P2
 (25) PCIE_MRX_PTX_N2
 (25) MINI2_CLKREQ#

(25) PCIE_MRX_PTX_P3
 (25) PCIE_MRX_PTX_N3
 (25) MINI1_CLKREQ#



MCP_PCIE_WAKE#
 R365 2 1 10K 0402 5% @ U31
 R367 2 1 10K 0402 5% @ U30
 R149 2 1 10K 0402 5% @ U29

EXPRESS@
 R146 1 2 0.0402 5%
 R147 1 2 0.0402 5%
 EXPRESS@
 R152 2 1 10K 0402 5%
 EXPRESS@

MINI2@
 R139 1 2 0.0402 5%
 R140 1 2 0.0402 5%
 MINI2@
 R118 2 1 10K 0402 5%
 MINI2@

MINI1@
 R134 1 2 0.0402 5%
 R135 1 2 0.0402 5%
 MINI1@
 R148 2 1 10K 0402 5%
 MINI1@

XN30
 XN31
 XR22
 XU23
 XN30
 XN31
 XR22
 XU23

XP26
 XP27
 XU22
 XV30
 XN30
 XN31
 XR22
 XU23

(14,26) CP_PE#
 R563 1 2 0.0402 5% EXPRESS@

PE0_REFCLK_P# R29 CLK_PCIE_VGA
 PE0_REFCLK_N# R30 CLK_PCIE_VGA#

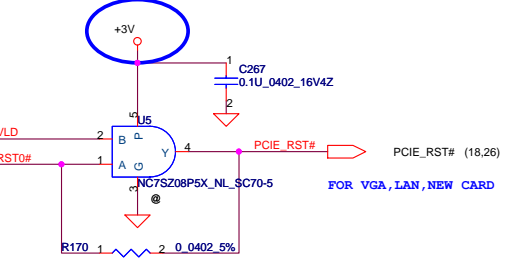
EXPRESS@
 M28 PCIE MTX PRX_P1 C249 1 2 0.1U 0402 16V7K
 M29 PCIE MTX PRX_N1 C248 1 2 0.1U 0402 16V7K

MINI2@
 M24 PCIE MTX PRX_P2 C220 1 2 0.1U 0402 16V7K
 M25 PCIE MTX PRX_N2 C219 1 2 0.1U 0402 16V7K

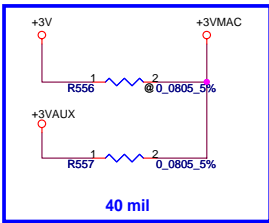
MINI1@
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 M23 PCIE MTX PRX_N3 C234 1 2 0.1U 0402 16V7K

XM30
 XM31
 XT25
 XT26
 XM30
 XM31
 XT25
 XT26

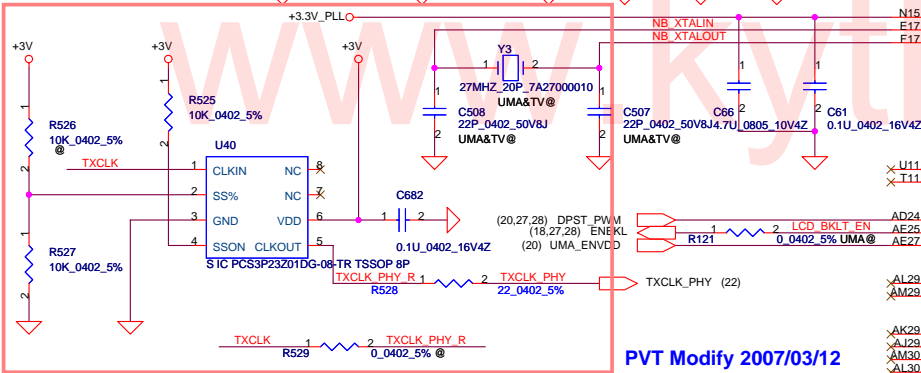
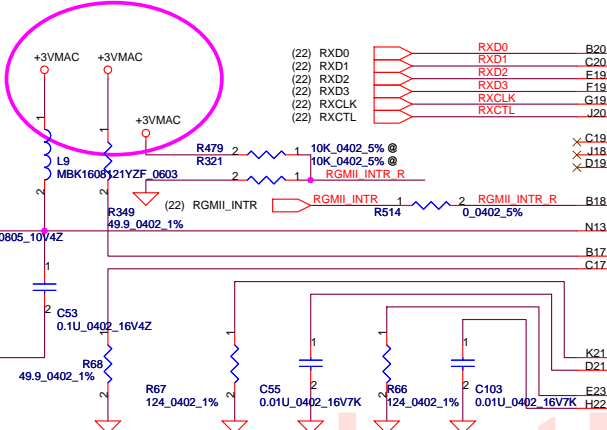
PEX_RST# W30
 PEX_RST# W29
 R165 1 2 0.0402 5% PCIE_RST#



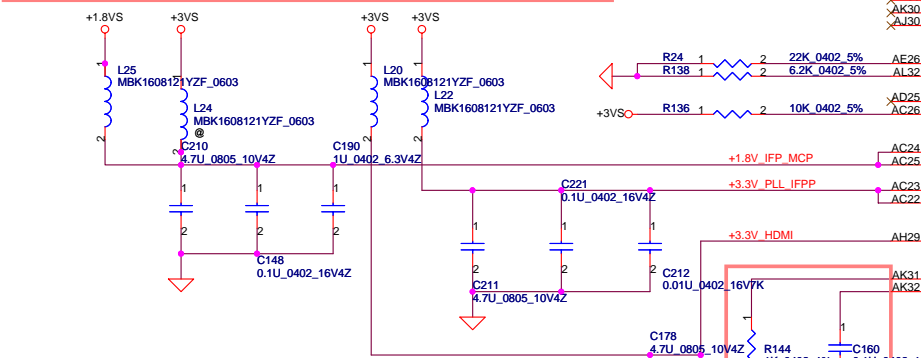
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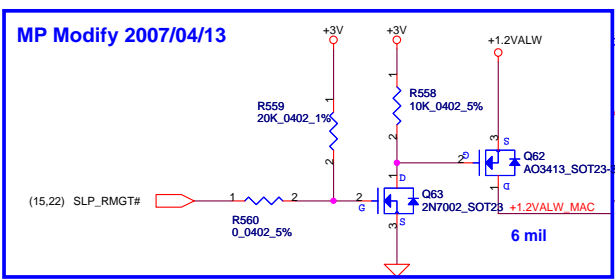
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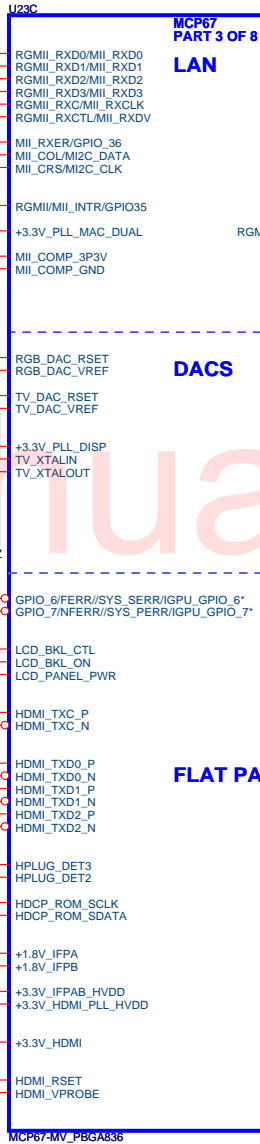
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PVT Modify 2007/03/12



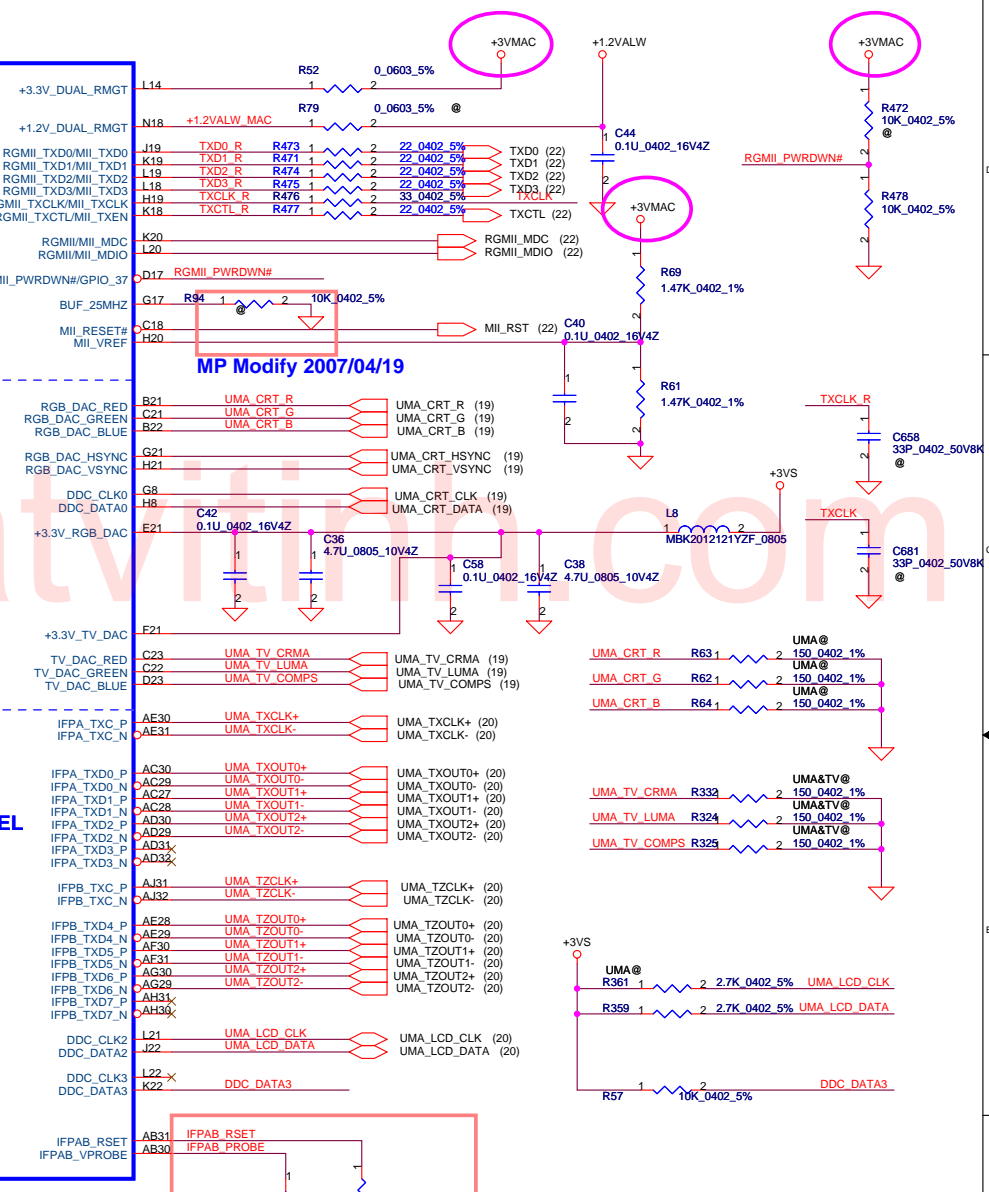
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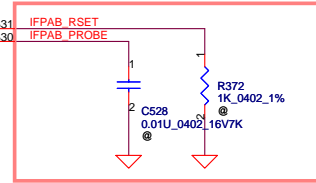
LAN

DACS

FLAT PANEL

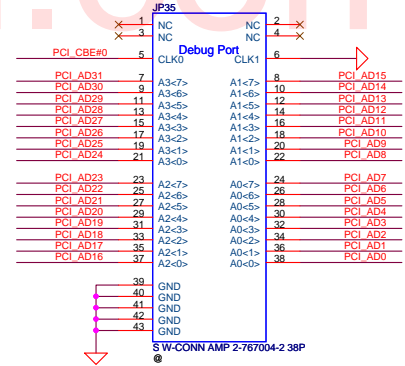
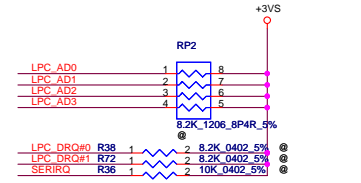
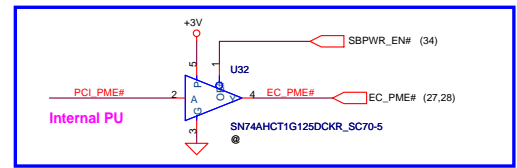
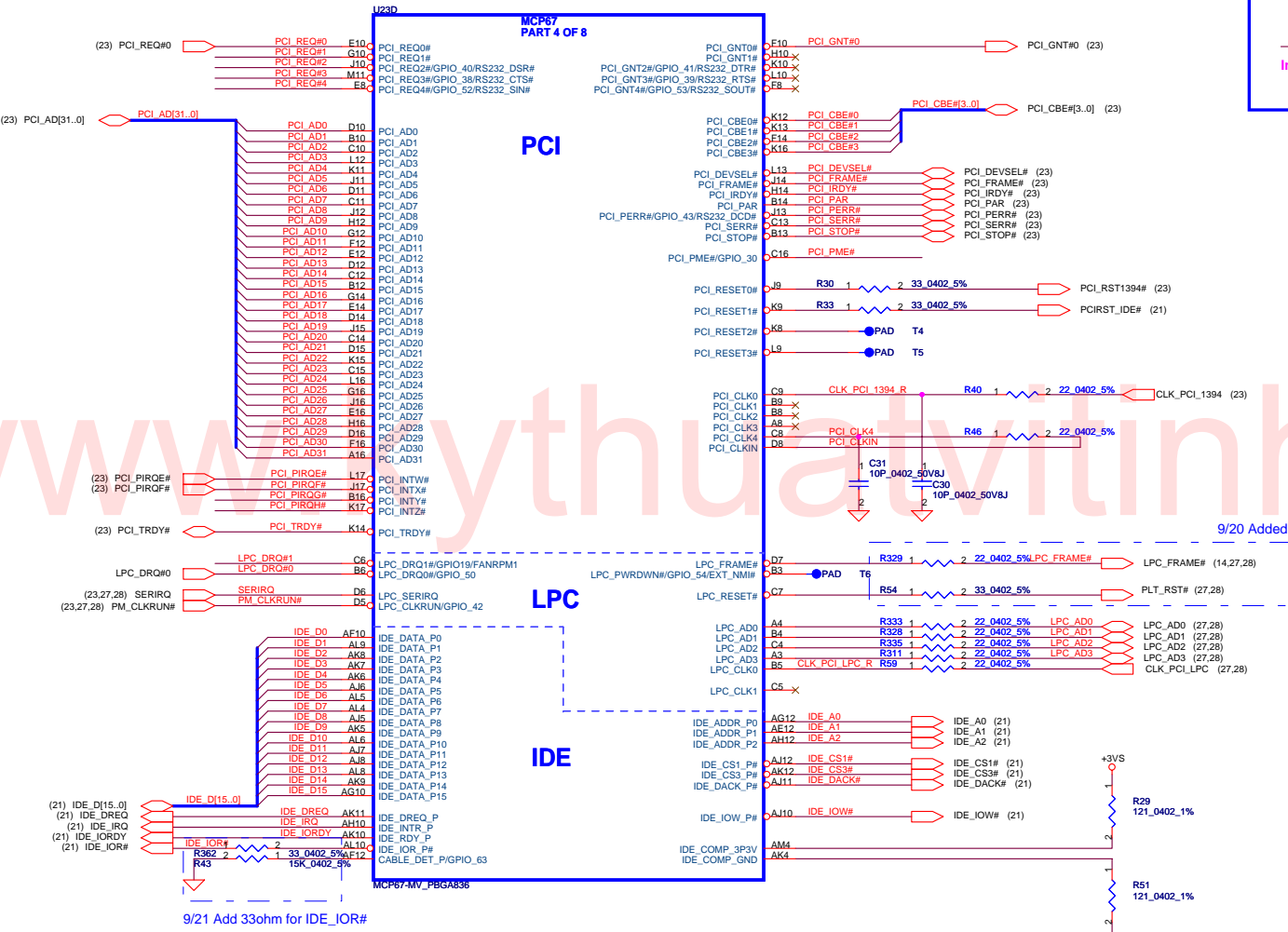
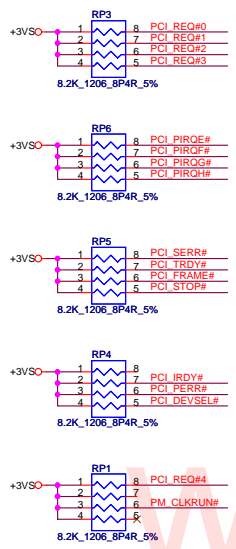


MP Modify 2007/04/19



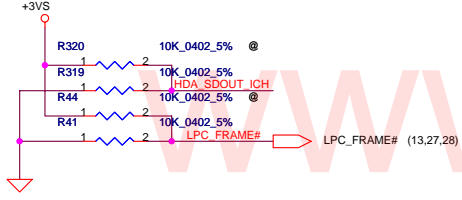
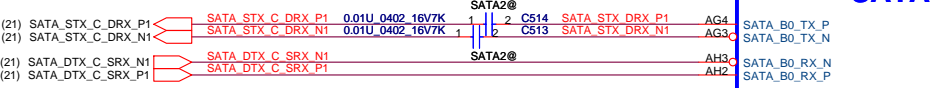
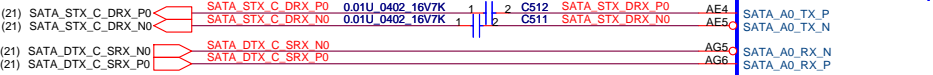
PVT Modify 2007/03/12

Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	MCP67 LAN/ CRT/ LVDS	
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Date:	Friday, April 20, 2007	Sheet	12	of	42



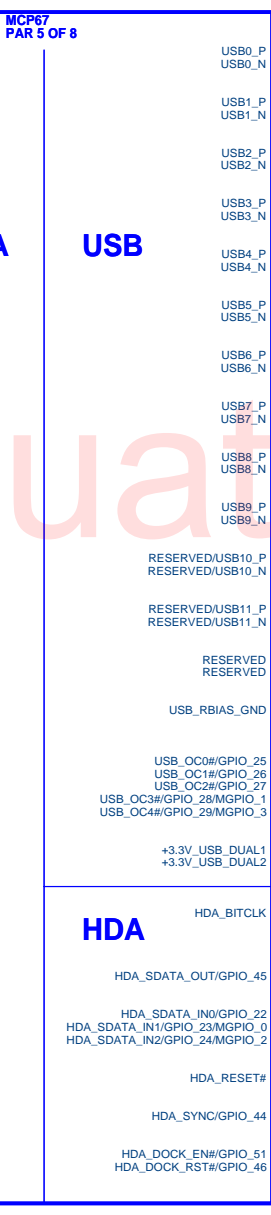
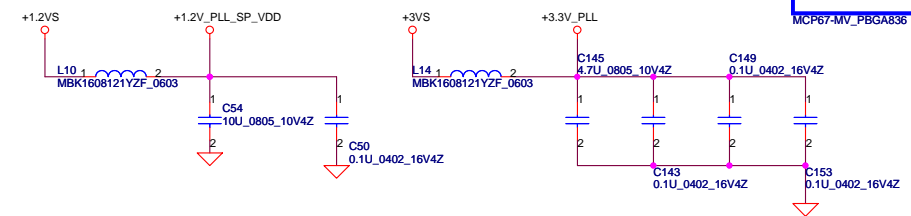
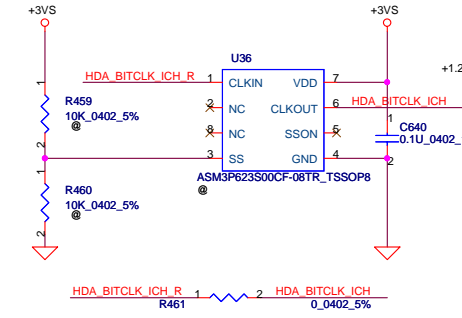
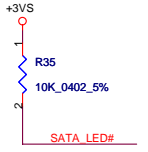
Security Classification	Compal Secret Data		Title
Issued Date	2006/08/18	Deciphered Date	2007/8/18
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PLACE SATA AC COUPLING CAPS CLOSE TO MCP67



HDA_SDOUT	LPC_FRAME	FUNCTION
"0"	"0"	LPC BIOS*
"0"	"1"	PCI BIOS
"1"	"0"	SPI BIOS
"1"	"1"	RESERVED

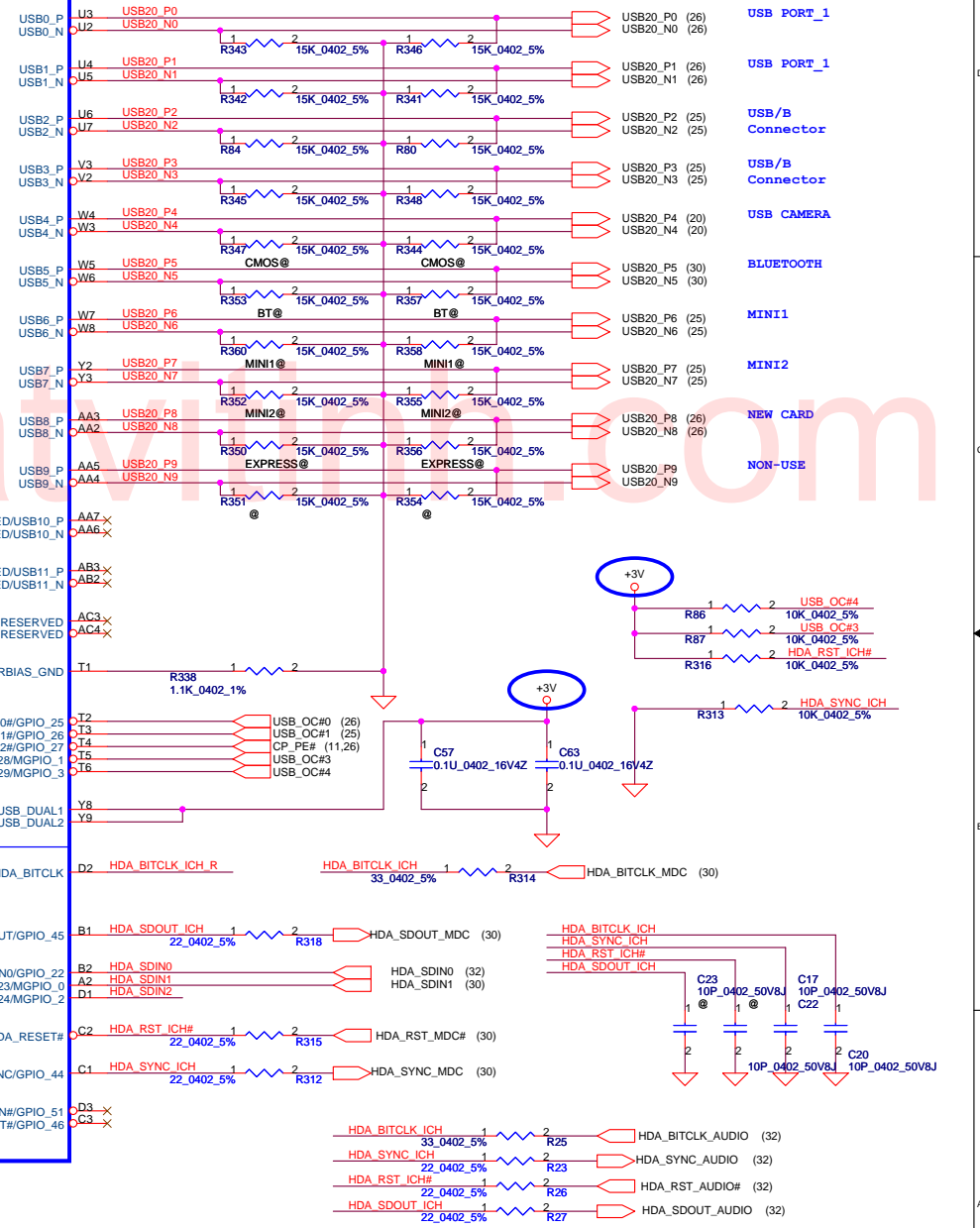
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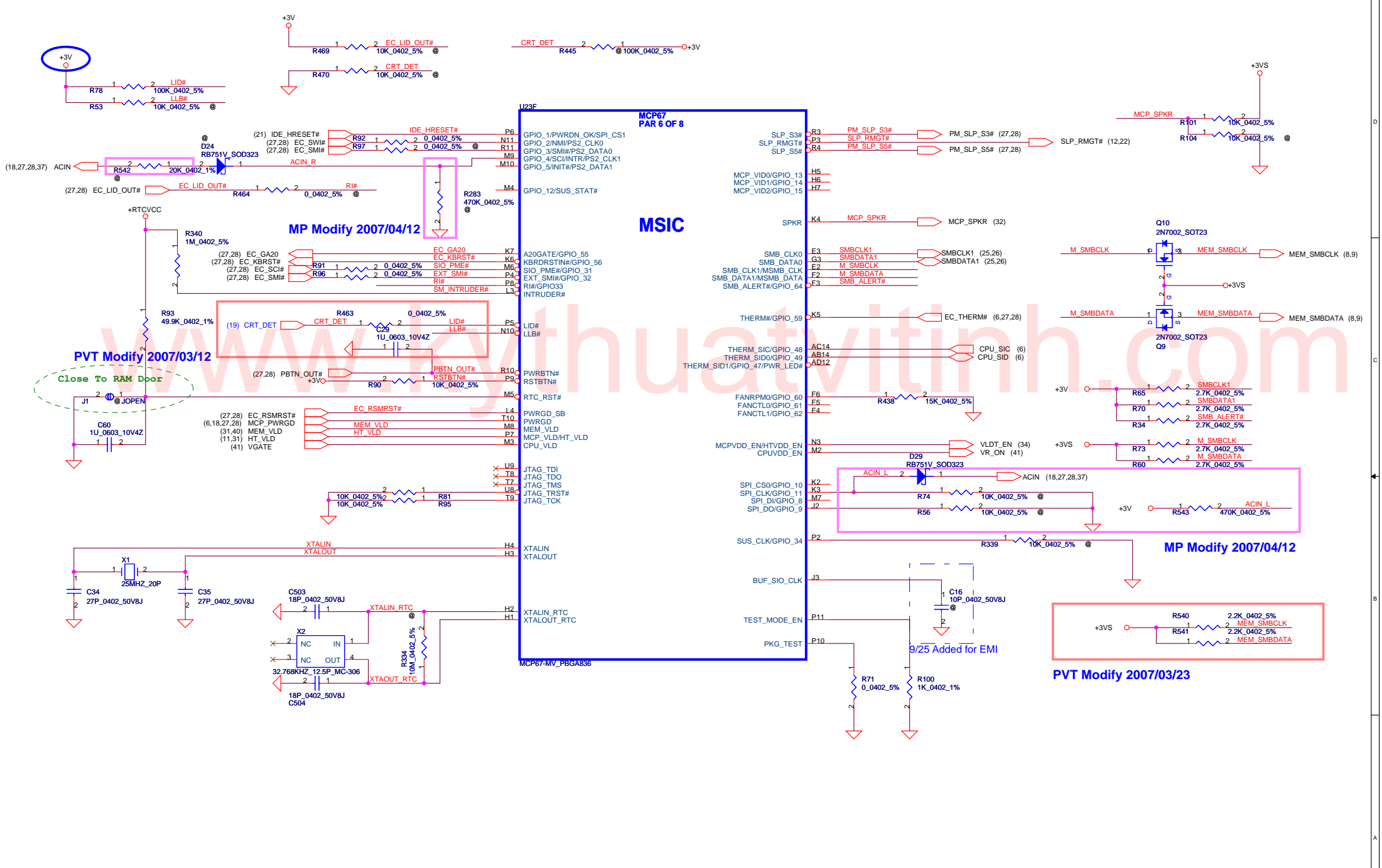
SATA

USB

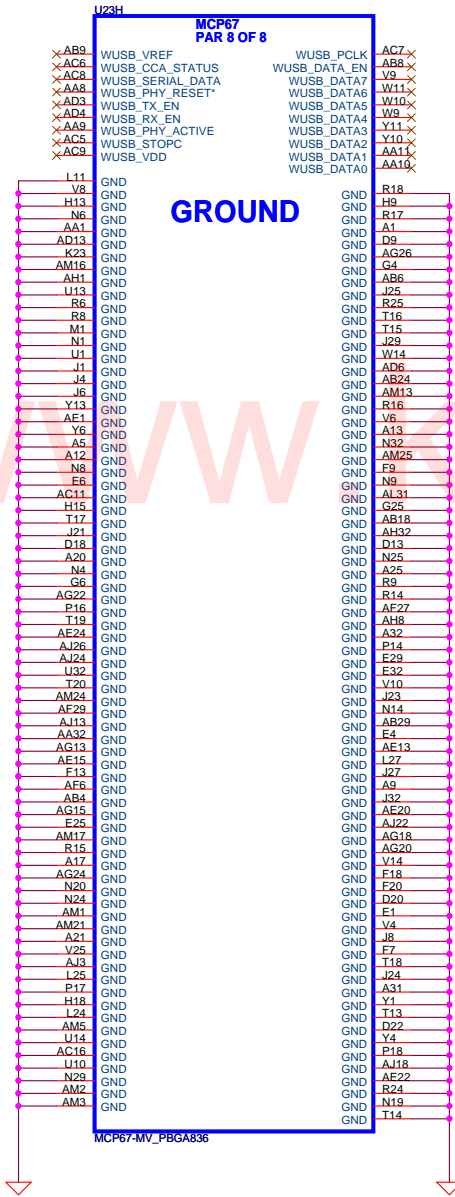
HDA



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	MCP67 SATA/ USB/ HDAUDIO		
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Date:	Friday, April 20, 2007	Sheet	14	of	42	



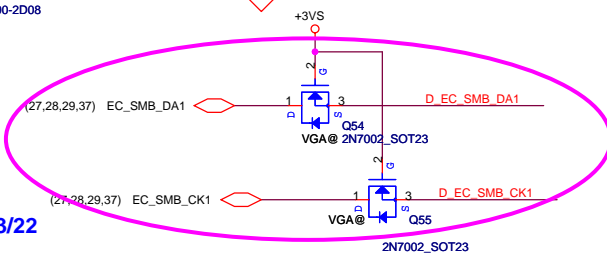
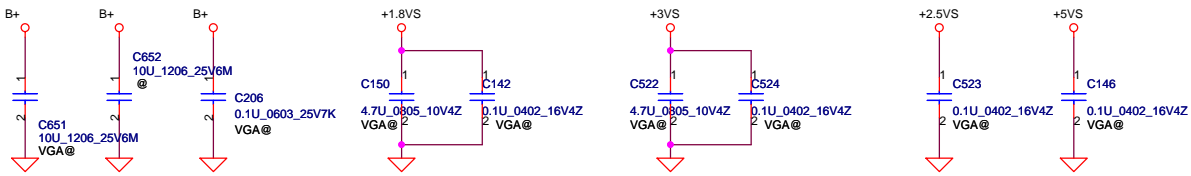
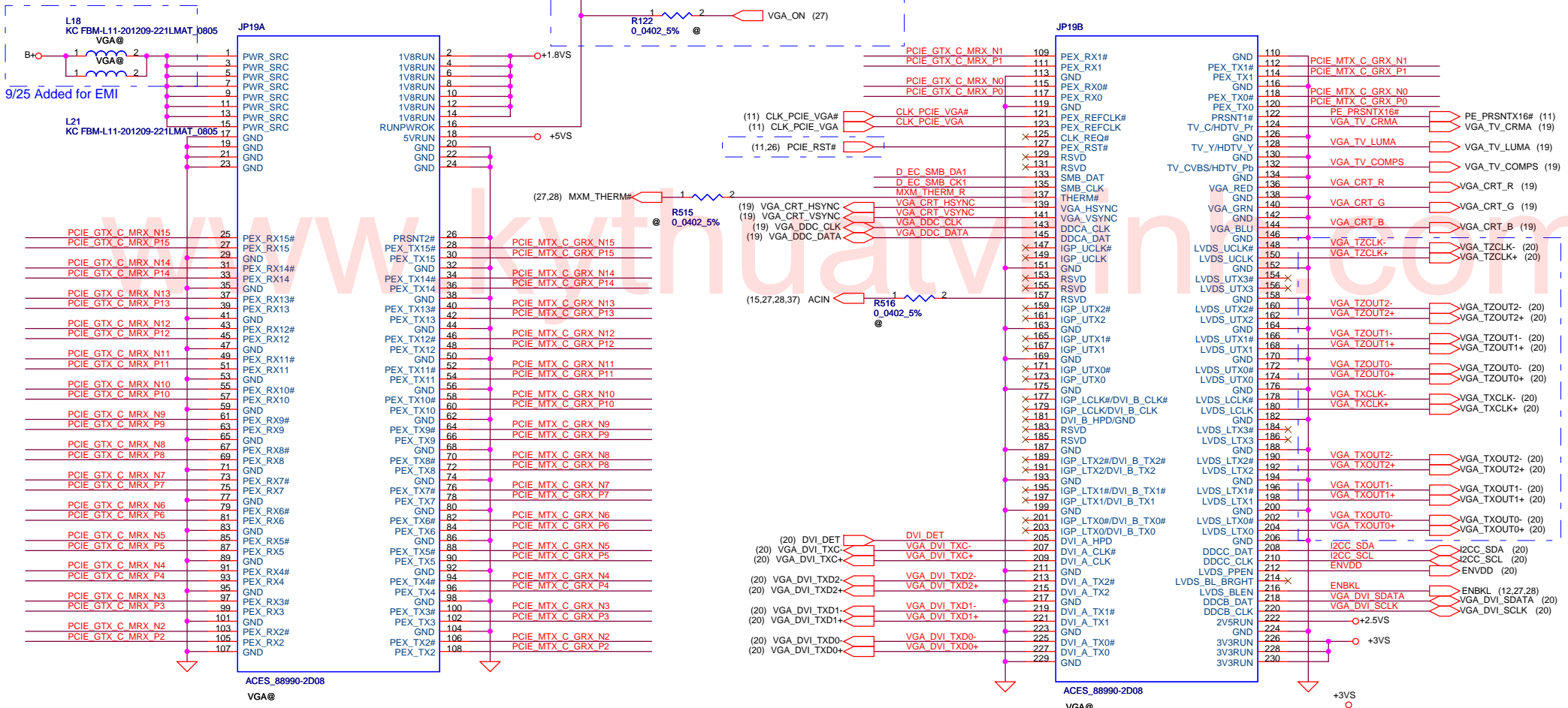
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	MCP67 MISC	
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				MCP67 GROUND	
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				Custom	1.0
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				Friday, April 20, 2007	17 of 42

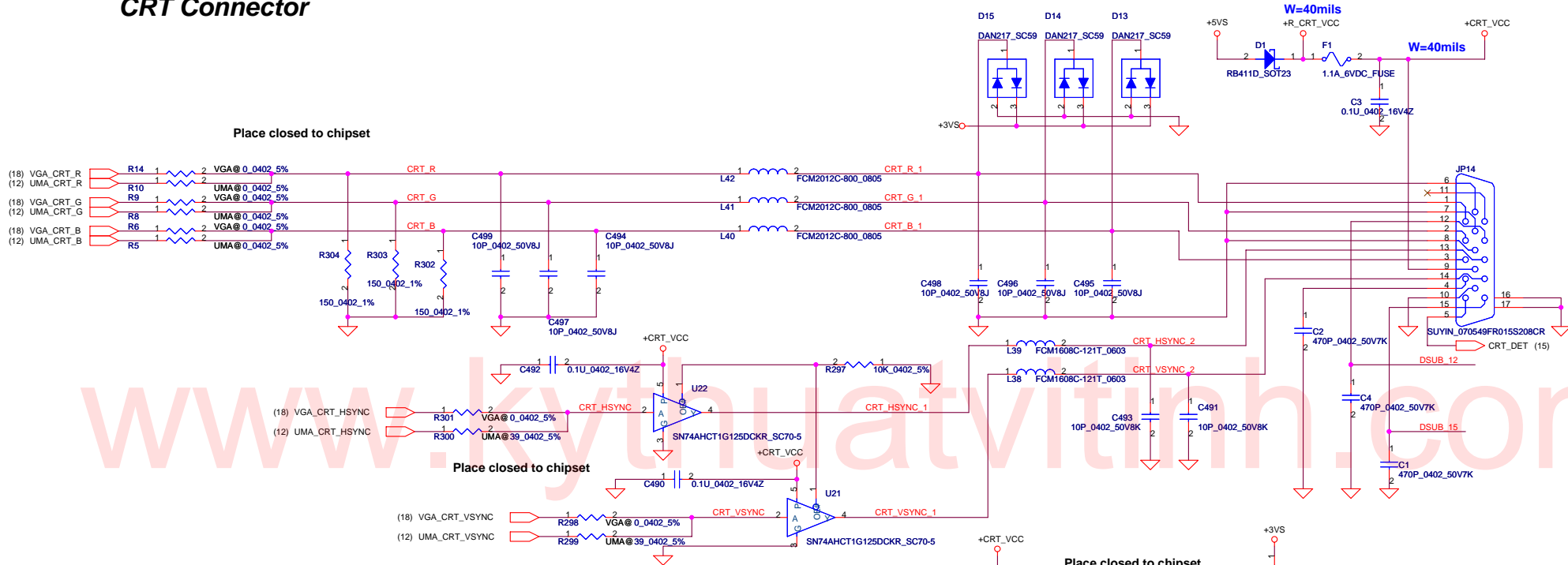
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- (11) PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
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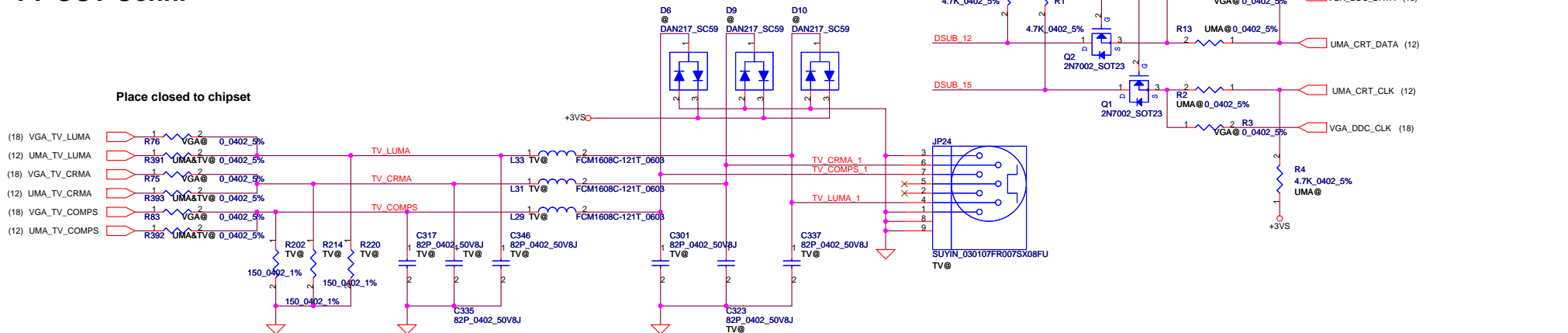
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	MXM Connector
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Size	Document Number	Rev		1.0	
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CRT Connector



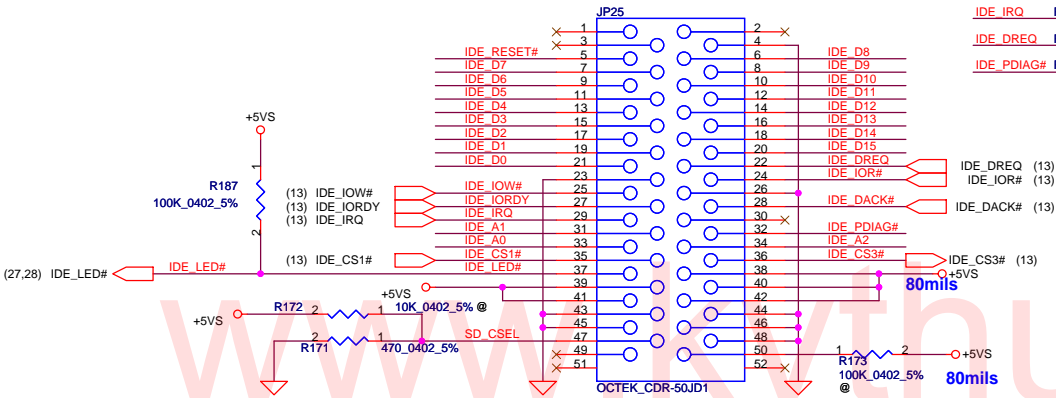
TV-OUT Conn.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	B	Document Number	ICW50 / ICY70 LA-3581P	Rev	1.0
Date:	Friday, April 20, 2007	Sheet	19	of	42

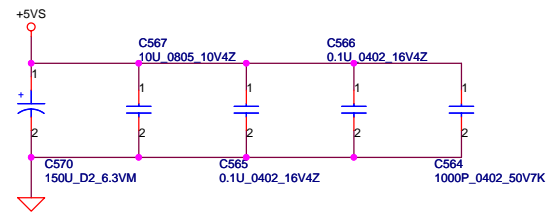
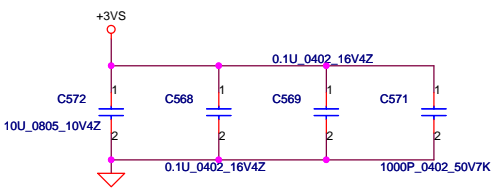
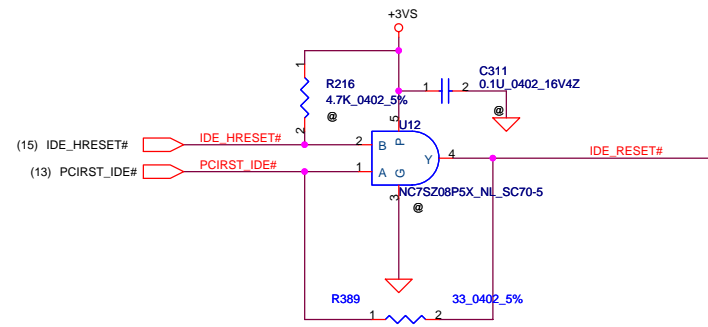
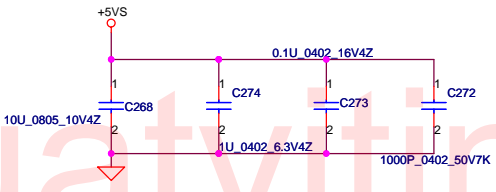
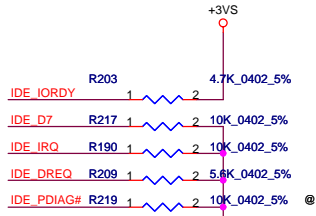
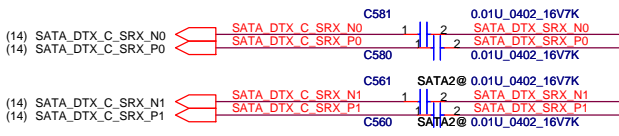
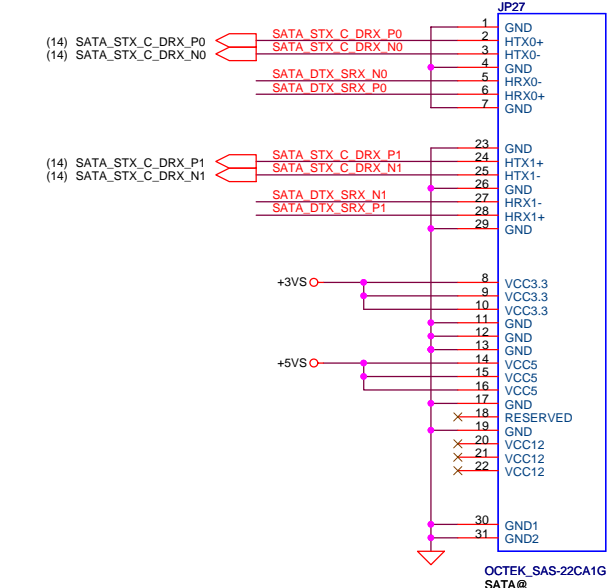
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 (13) IDE_A[0..2]  IDE_A[0..2]

CDROM CONN



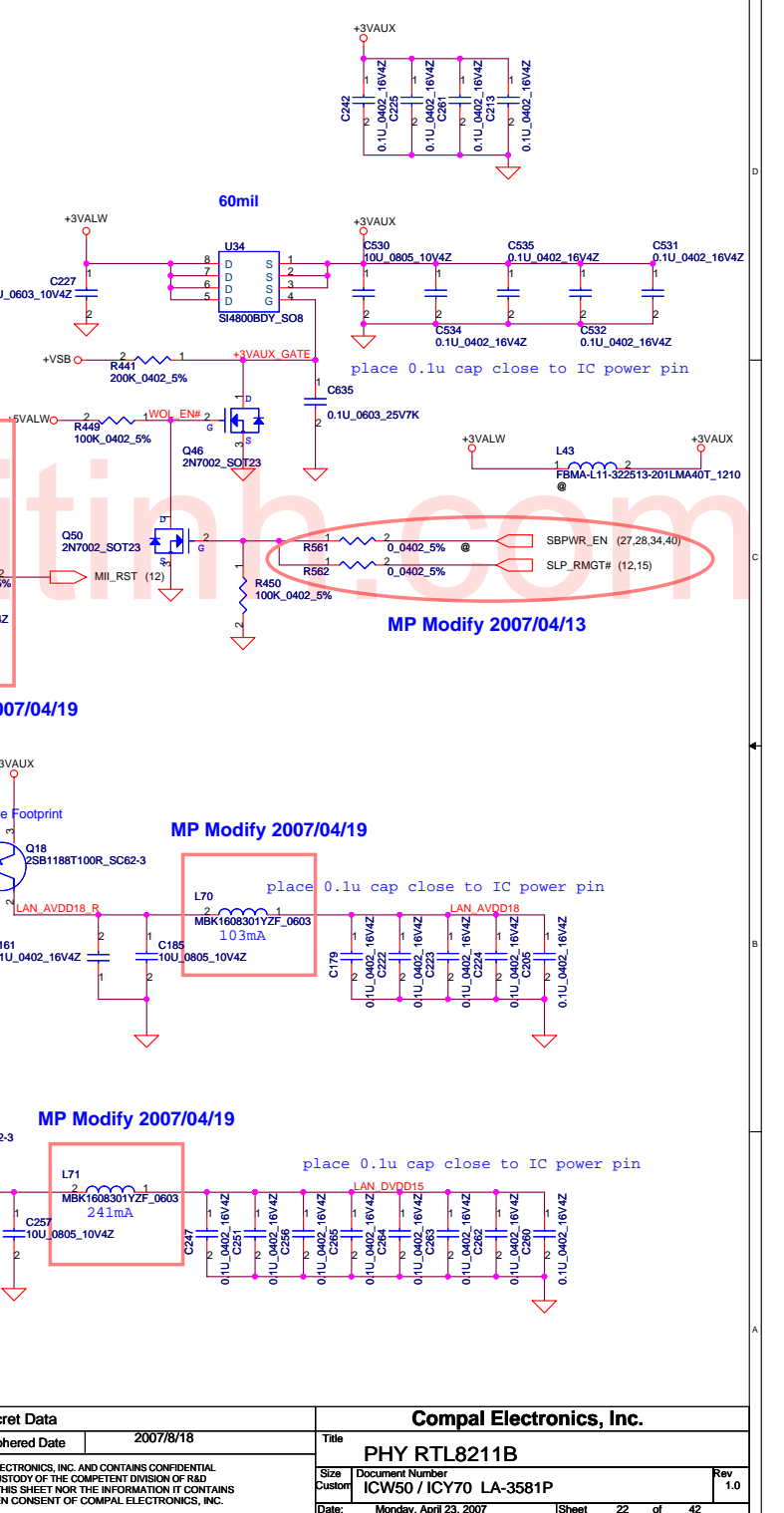
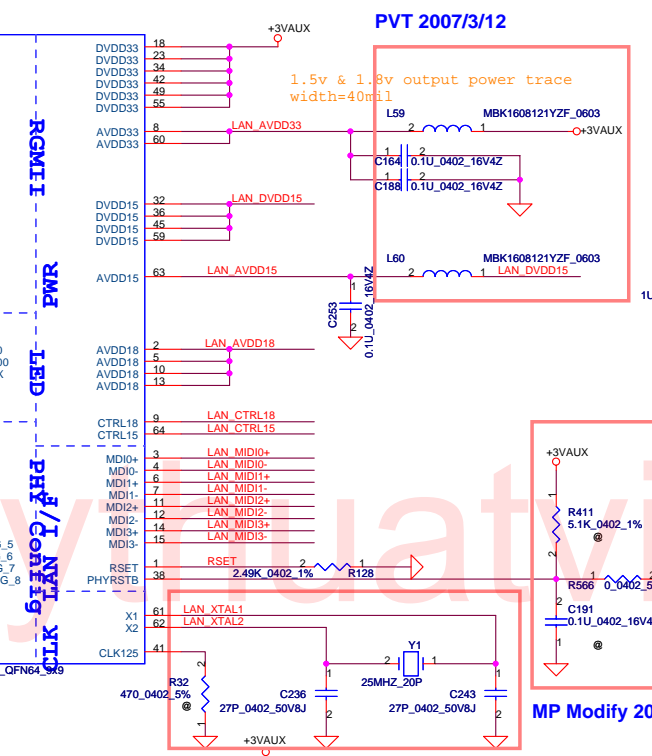
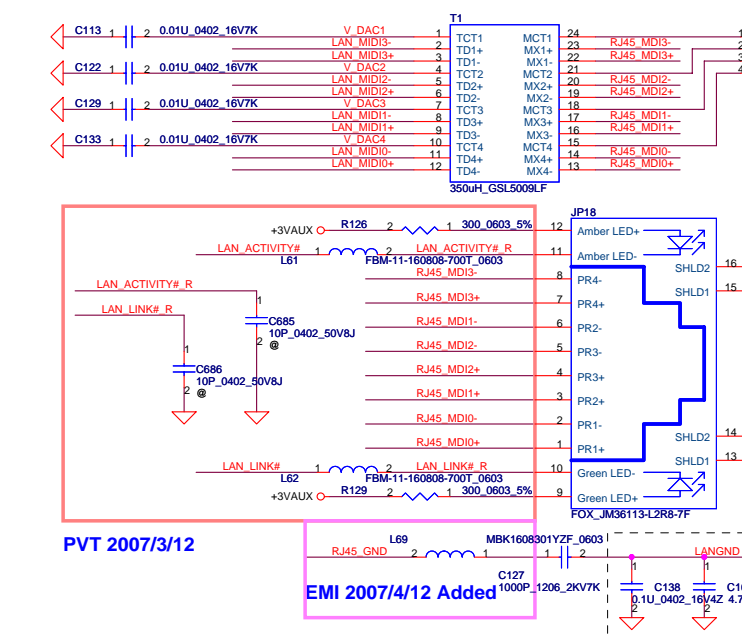
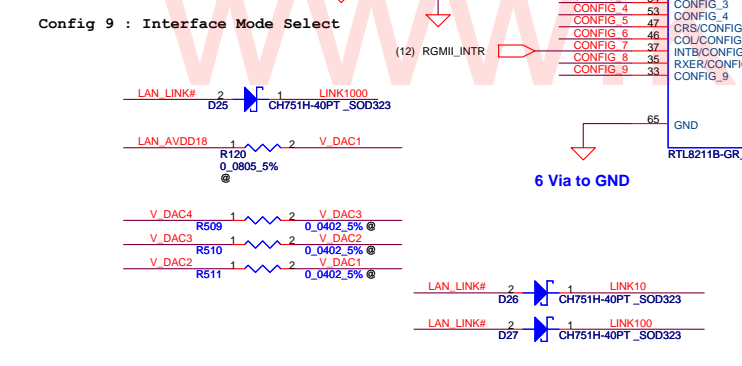
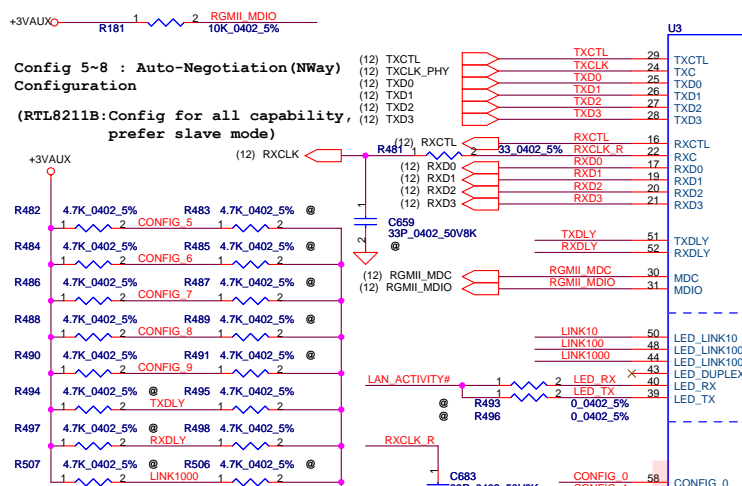
If CDROM is Slave
 then SD_CSEL= Floating
 else SD_CSEL= Low

SATA HDD Conn.(SAS Connector)



Close to SATA HDD

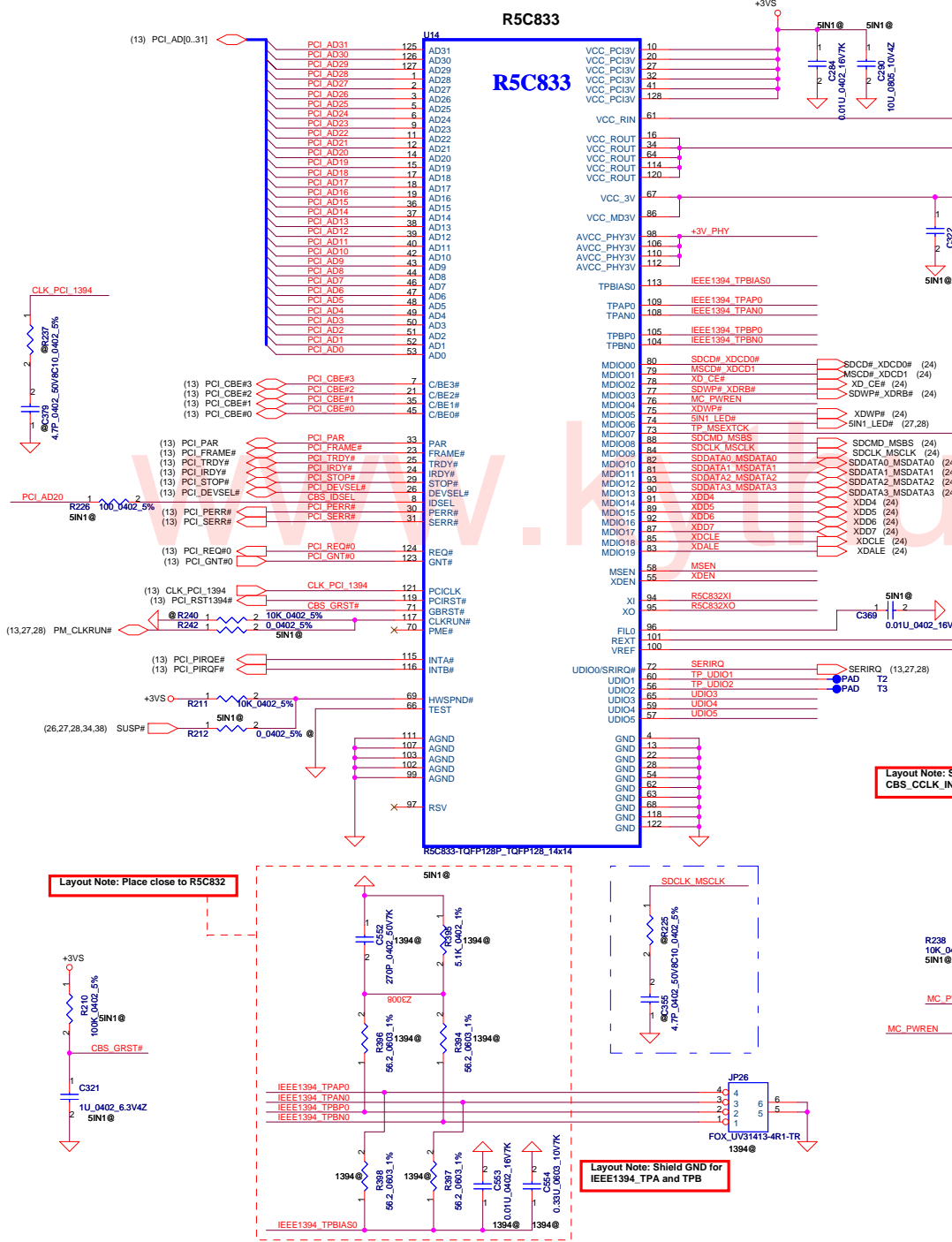
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Compal Electronics, Inc.		
Title	PHY RTL8211B	
Size	Document Number	Rev
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Date:	Monday, April 23, 2007	Sheet 22 of 42



SD, MMC, MS, XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR / BH
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLEd#	MSLED#	XLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLCK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1			XDCDAT1
MDIO12	SDCDAT2			XDCDAT2
MDIO13	SDCDAT3			XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALe

Function set pin define

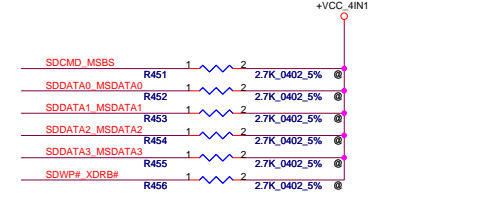
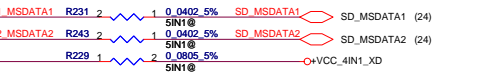
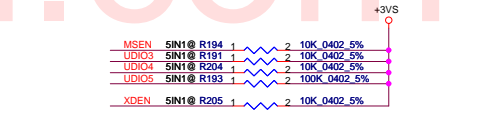
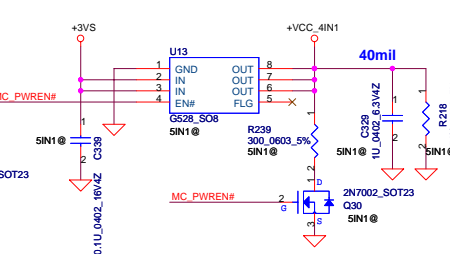
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK

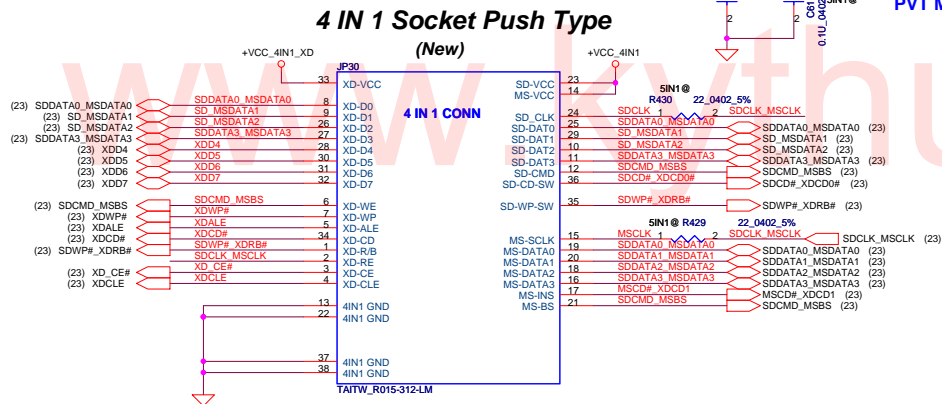
Layout Note: Place close to R5C832 and Shield GND for SD_CLK

Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK

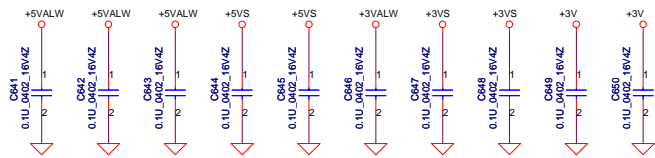
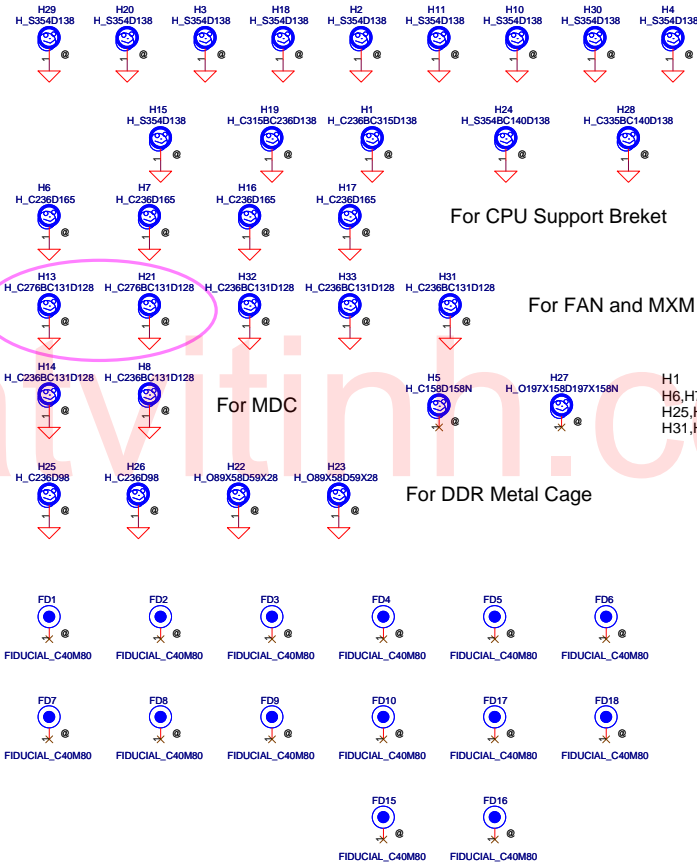
Memory Card Power Switch



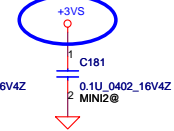
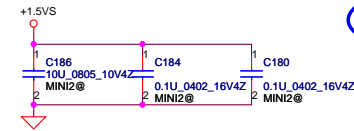
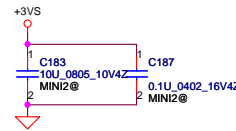
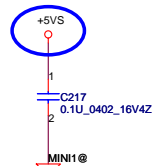
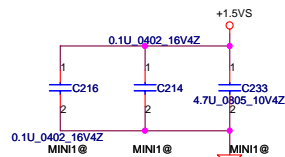
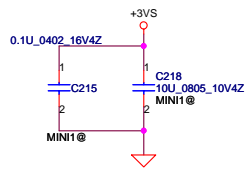
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Issued Date	2005/10/06	Deciphered Date	
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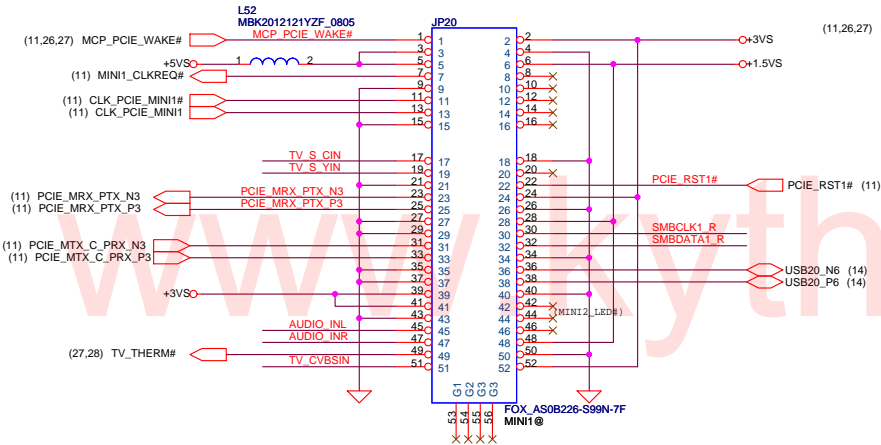
PVT Modify 2007/3/12



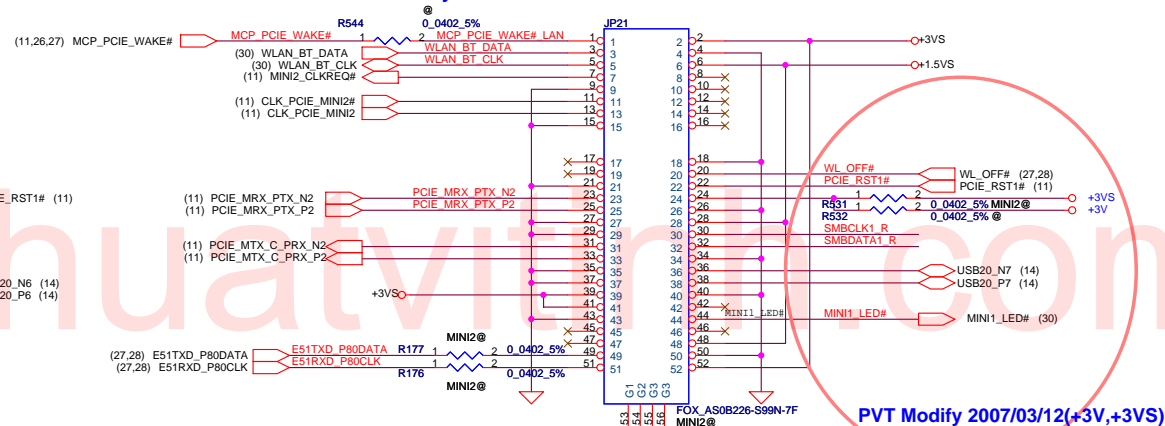
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Issued Date	2005/10/06	Deciphered Date	
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			Document Number ICW50 / ICY70 LA-3581P
			Rev 1.0
			Date: Friday, April 20, 2007
			Sheet 24 of 42



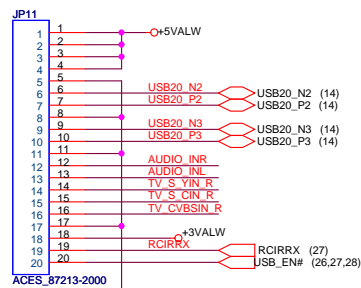
TV TUNNER



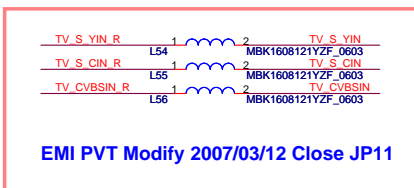
PVT2 Modify 2007/04/12



USB/B Connector



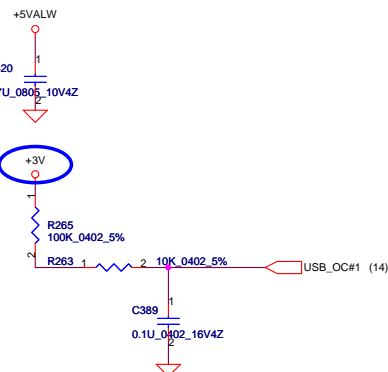
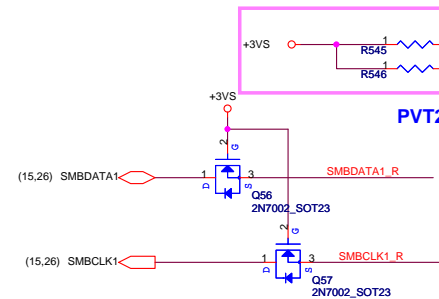
AV-IN Connector CIR



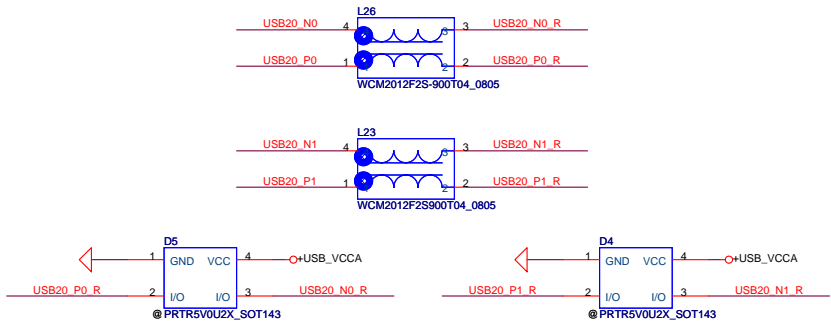
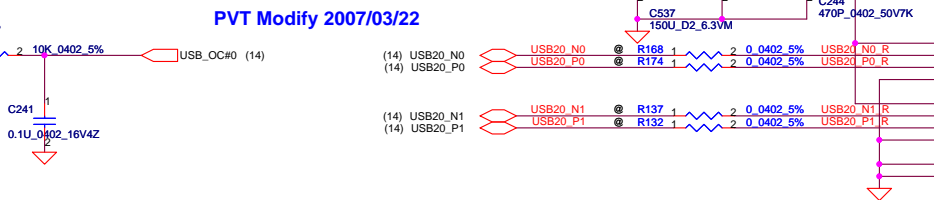
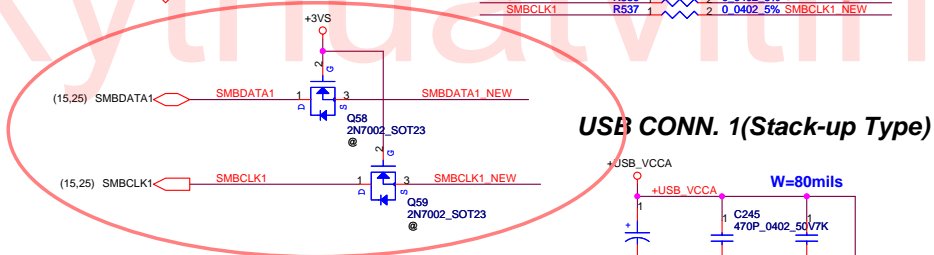
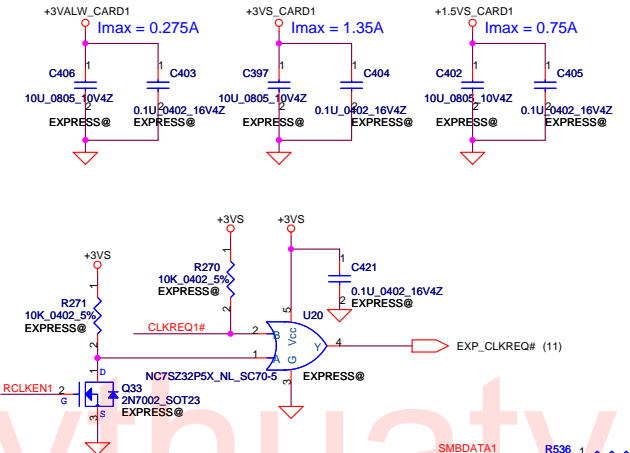
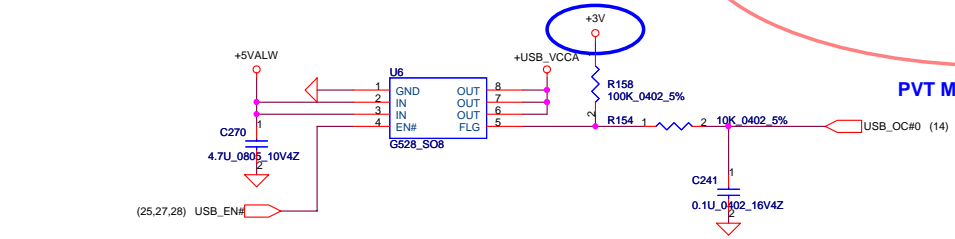
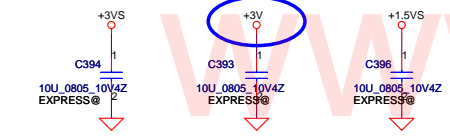
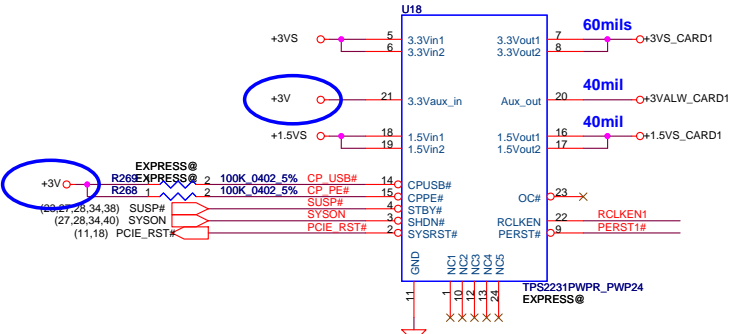
EMI PVT Modify 2007/03/12 Close JP11

Power	Mini Card Power Rating	
	Primary Power (mA)	Auxiliary Power (mA)
	Peak	Normal
+3VS	1000	750
+3VALW	330	250 (wake enable)
+1.5VS	500	375 (5 (Not wake enable))

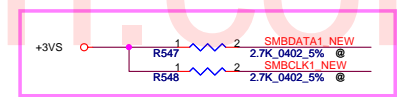
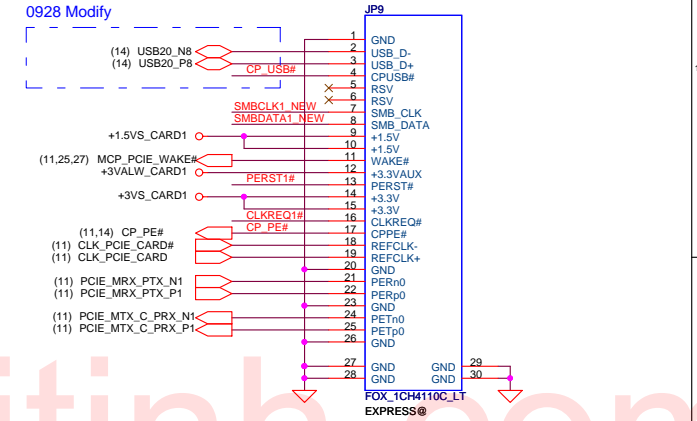
PVT2 Modify 2007/04/12



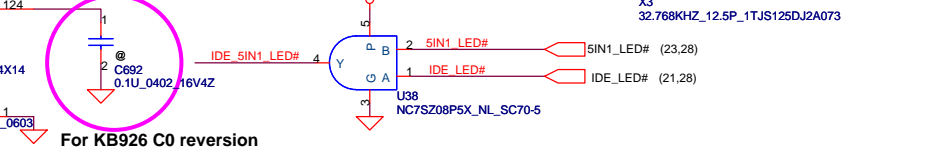
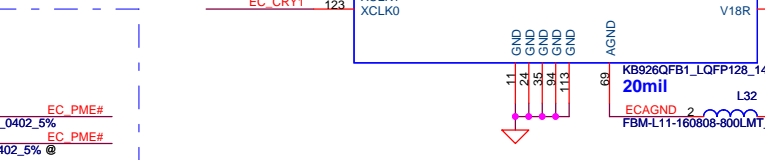
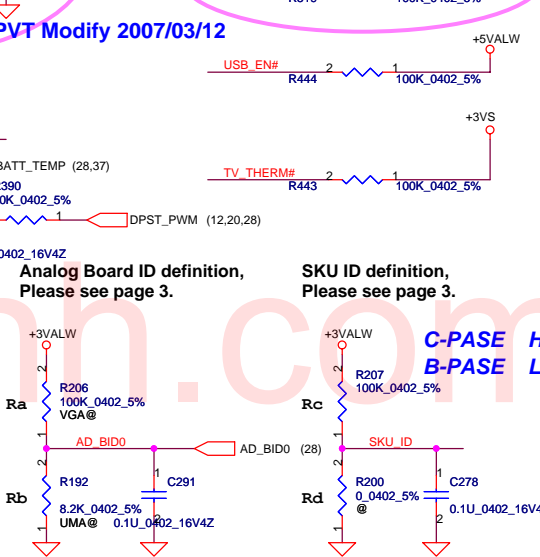
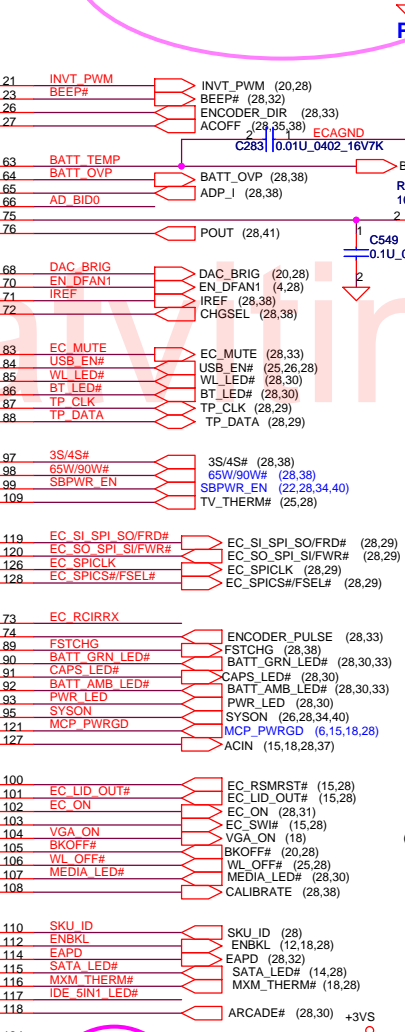
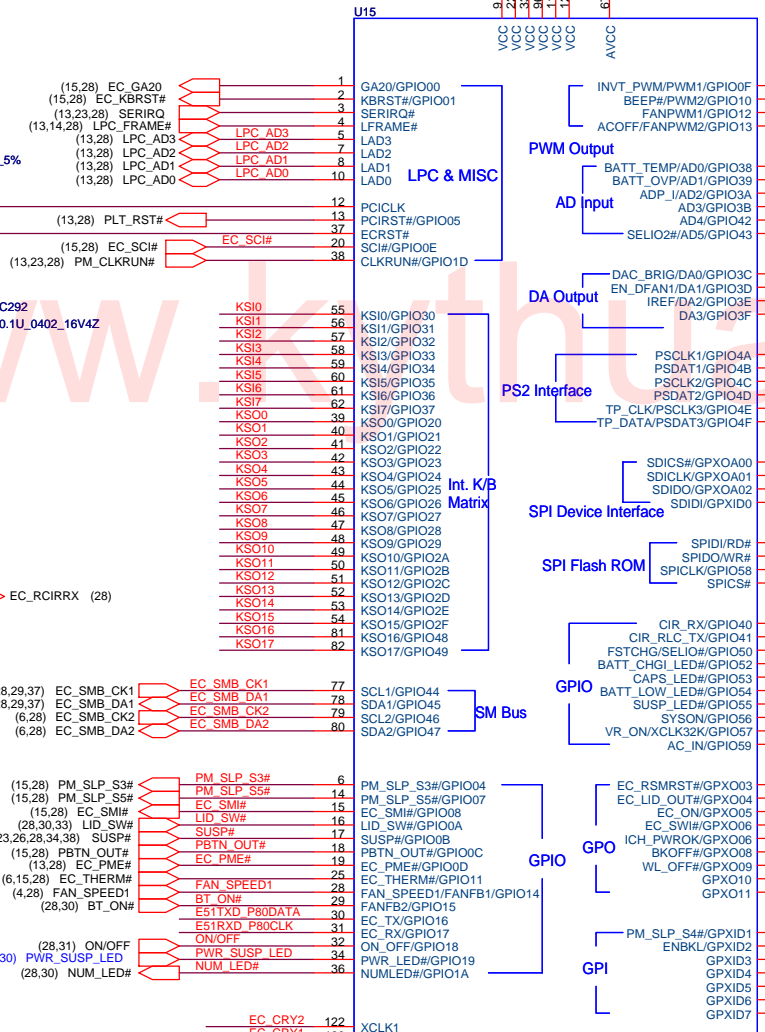
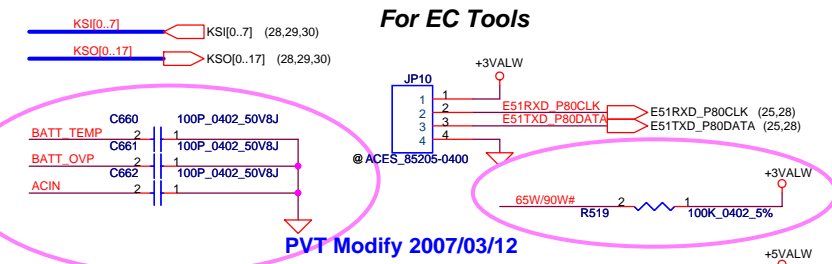
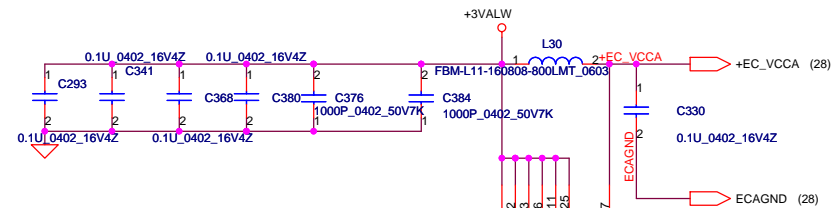
New Card Power Switch



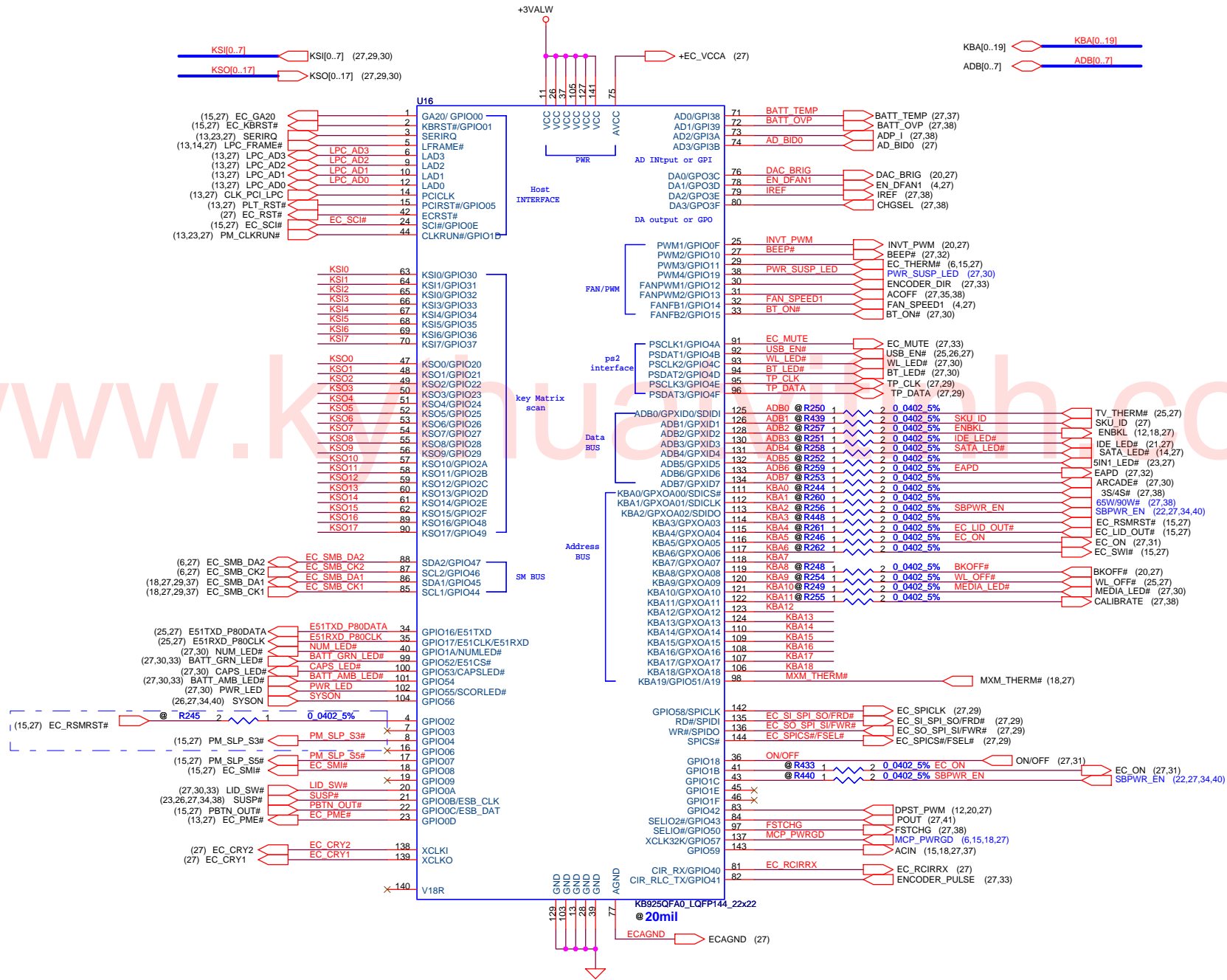
New Card Socket (Left/TOP)



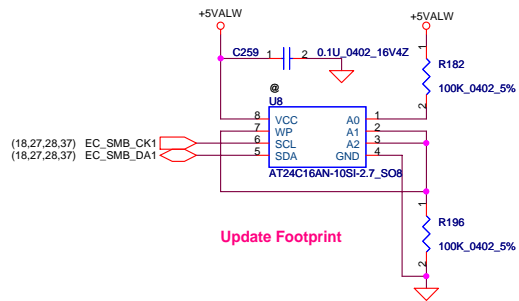
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	
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Title	NEW CARD & USB Connector			
Size B	Document Number	ICW50 / ICY70 LA-3581P	Rev	1.0
Date:	Friday, April 20, 2007	Sheet	26	of 42



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	EC ENE KB926
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Size	Document Number	Rev			
B	ICW50 / ICY70 LA-3581P	1.0	Date:	Friday, April 20, 2007	Sheet 27 of 42

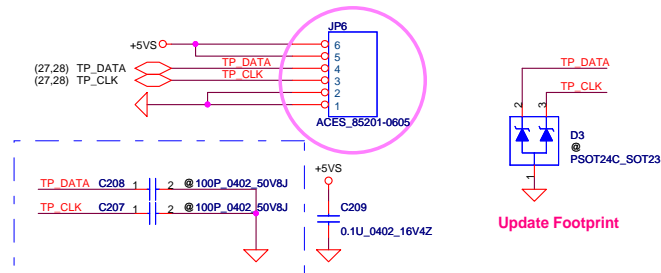


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		Date:	
B	ICW50 / ICY70 LA-3581P	1.0		Friday, April 20, 2007	
				Sheet	28 of 42



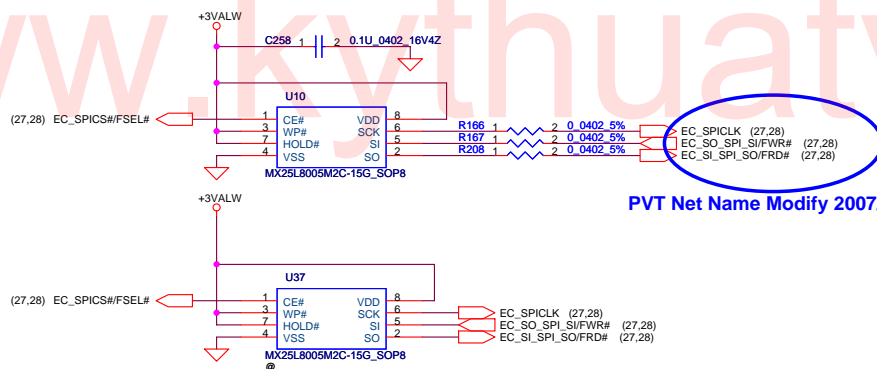
Update Footprint

To TP/B Conn.



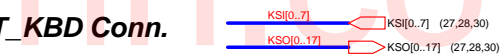
Update Footprint

9/25 Added for EMI

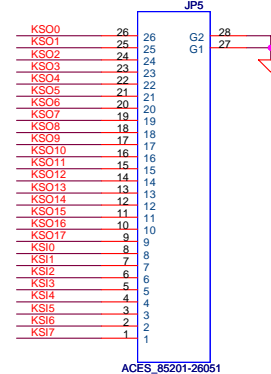


PVT Net Name Modify 2007/3/12

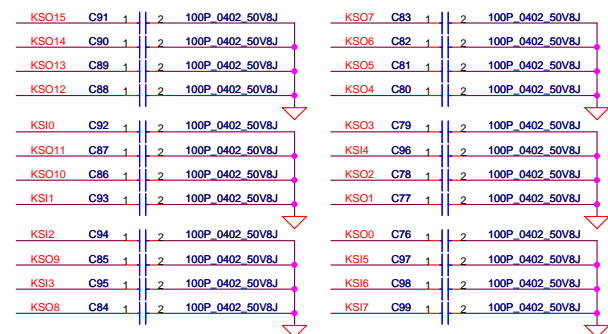
INT_KBD Conn.



(Left)



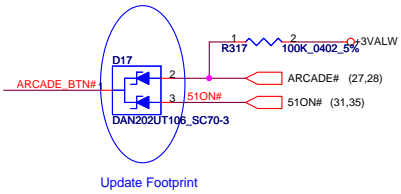
(Right)



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				B	ICW50 / ICY70 LA-3581P
Date:	Monday, April 23, 2007	Sheet	29	of	42
				Rev	1.0

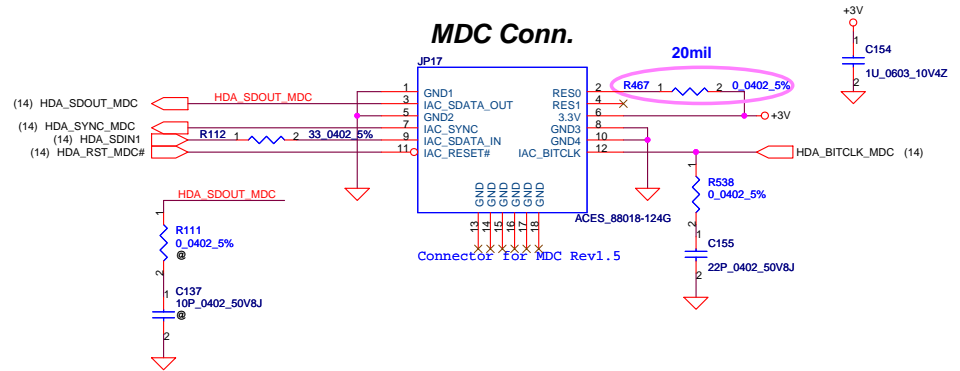
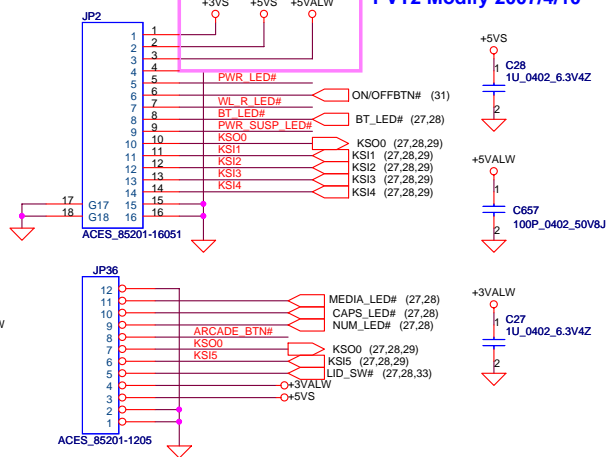
	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

Check 15.4" K/B Matrix

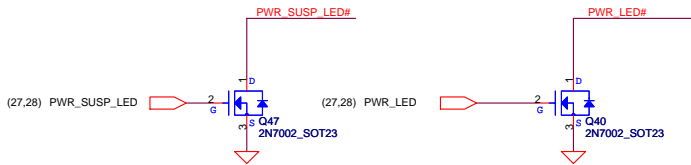
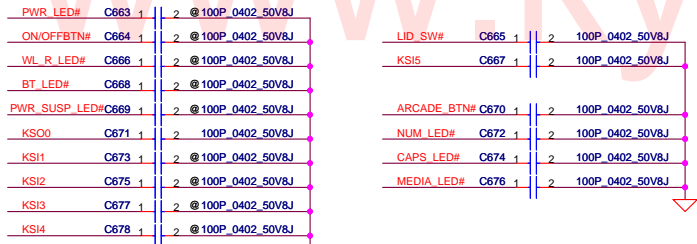


Update Footprint

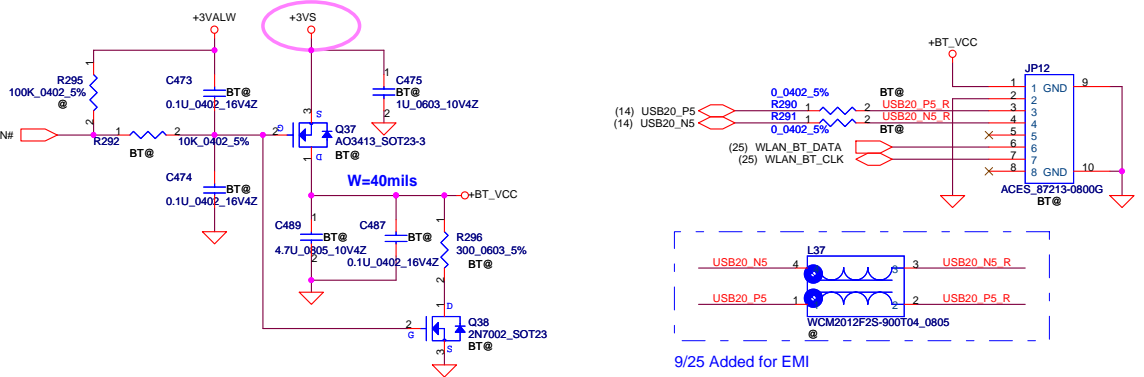
PVT2 Modify 2007/4/10



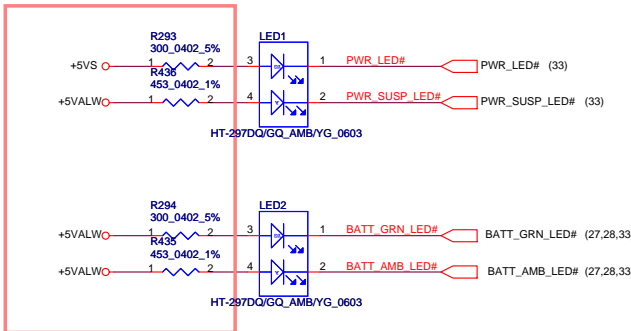
EMI PVT Modify 2007/3/12



Bluetooth Conn.

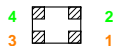


PVT Modify 2007/3/12

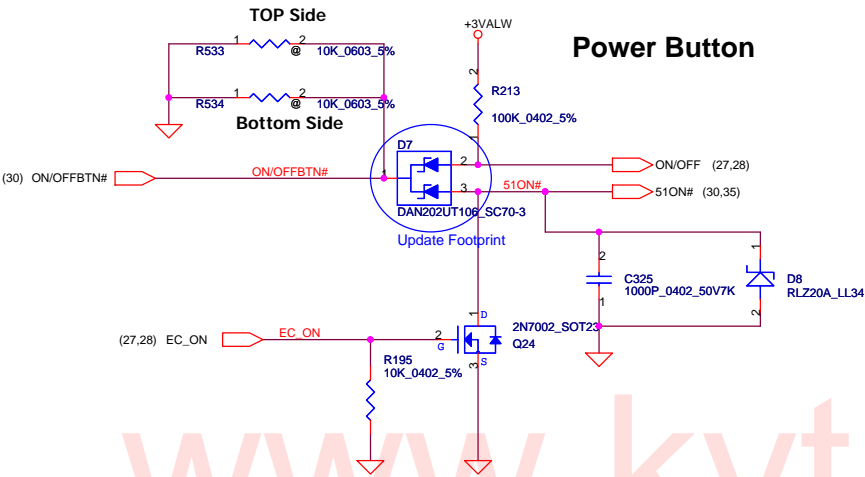


PVT Value Modify to 453E 2007/3/12

Compal Footprint

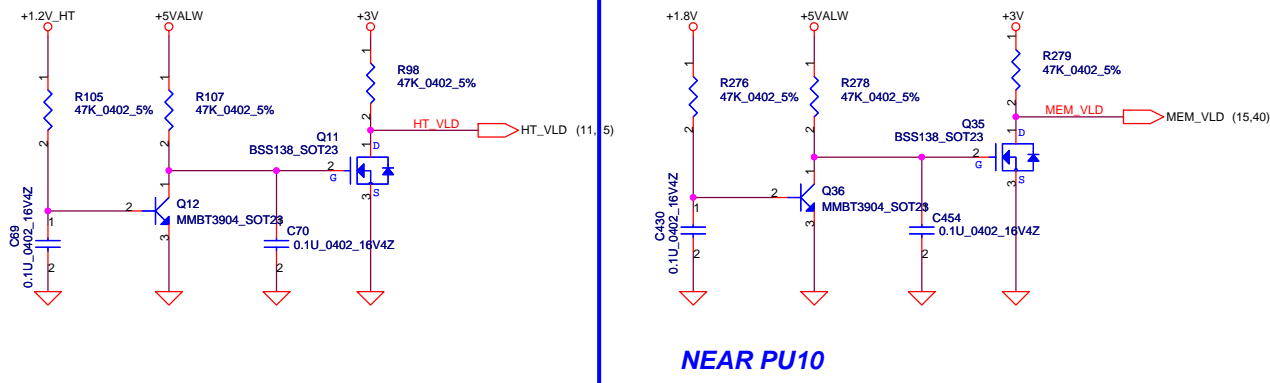


Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	
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B	ICW50 / ICY70 LA-3581P			1.0
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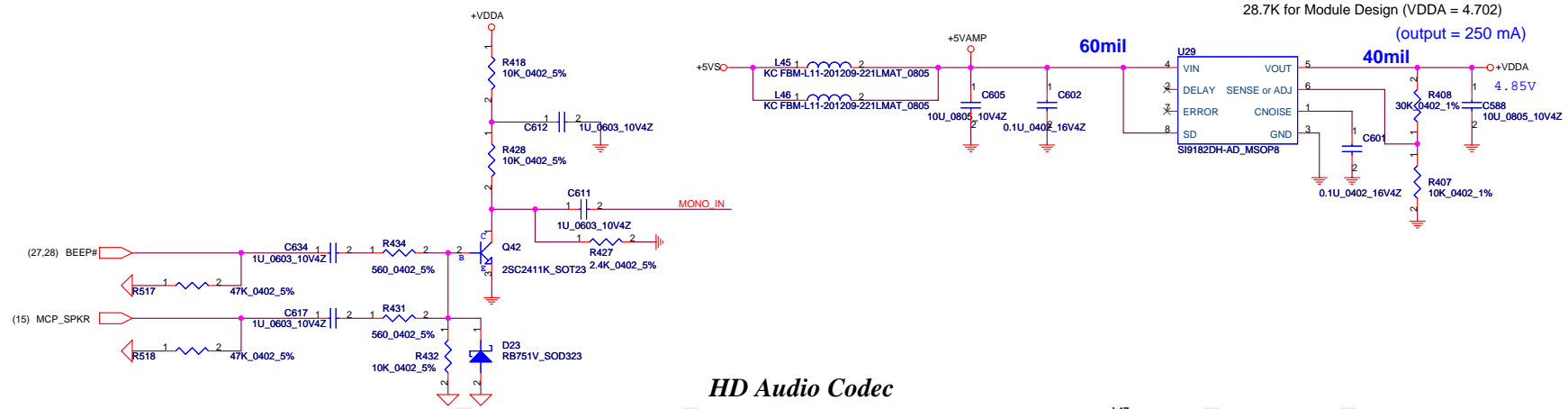
Power ON Circuit



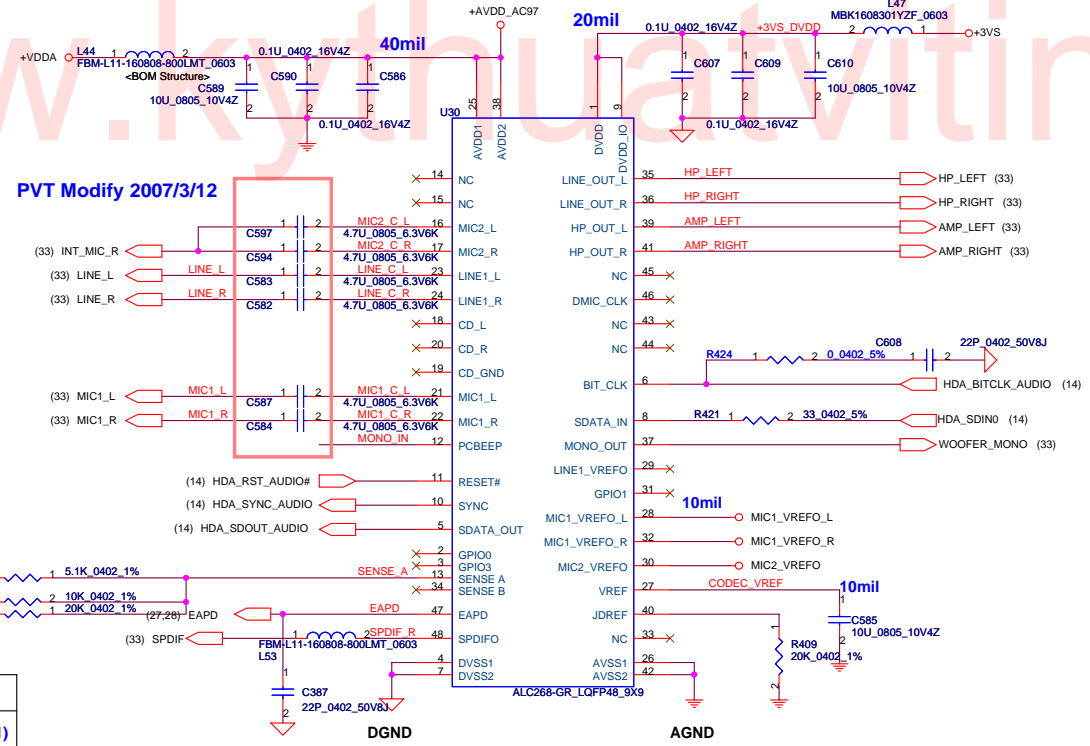
NEAR PU10

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	PWR_OK CIRCUIT/ BTN
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				Document Number ICW50 / ICY70 LA-3581P
				Rev 1.0
			Date: Friday, April 20, 2007	Sheet 31 of 42

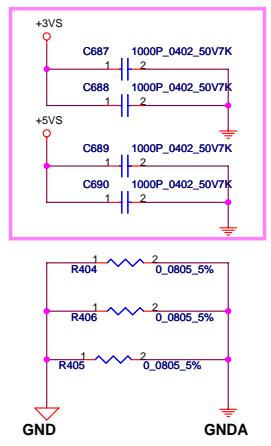
www.kyauatvithinh.com



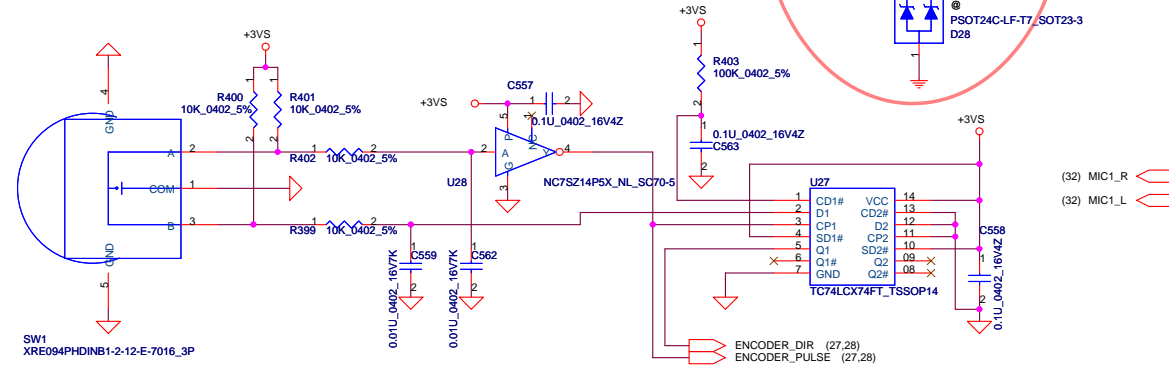
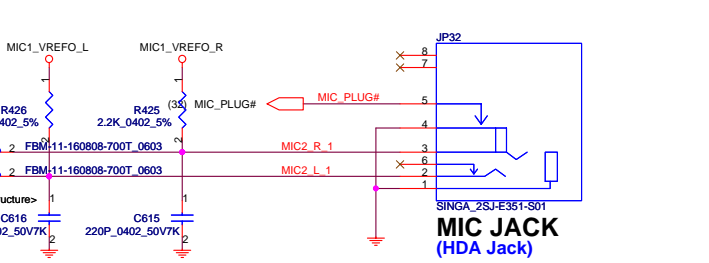
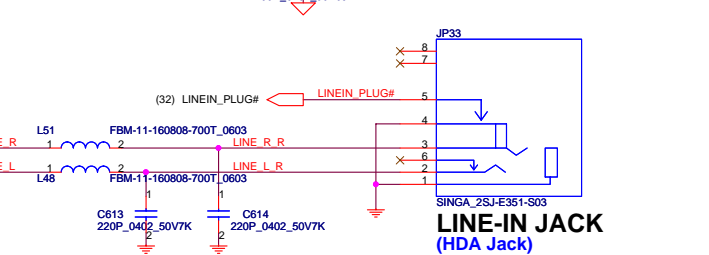
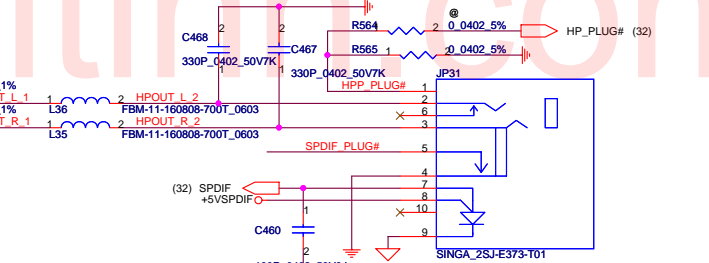
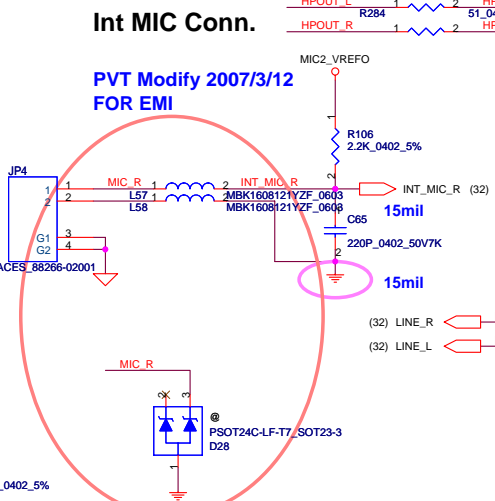
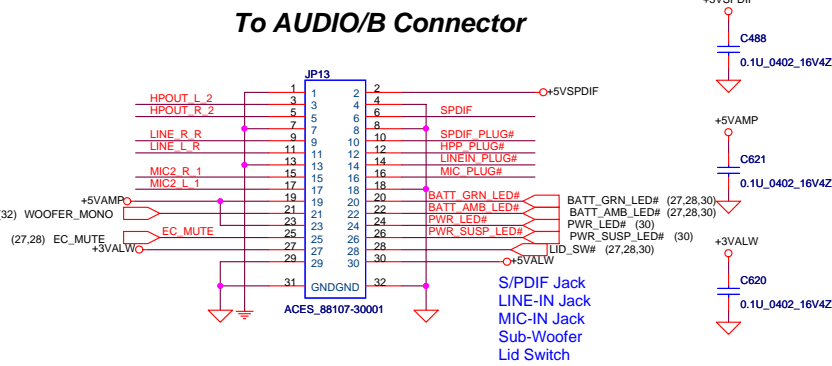
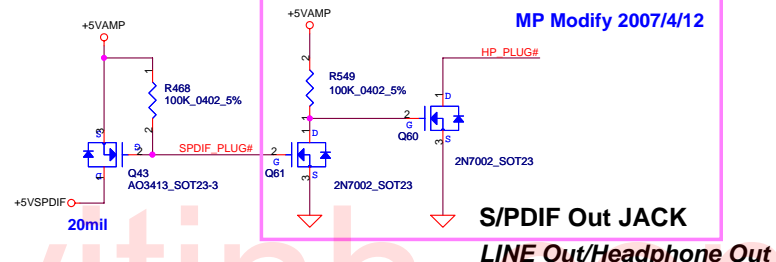
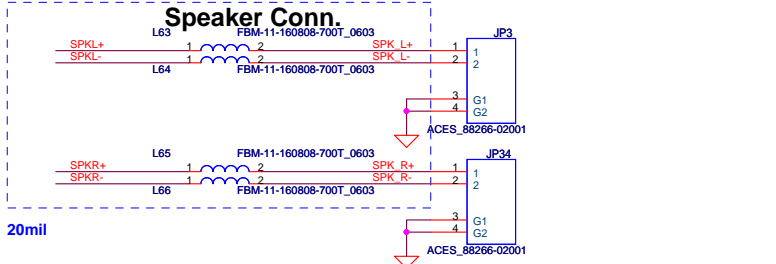
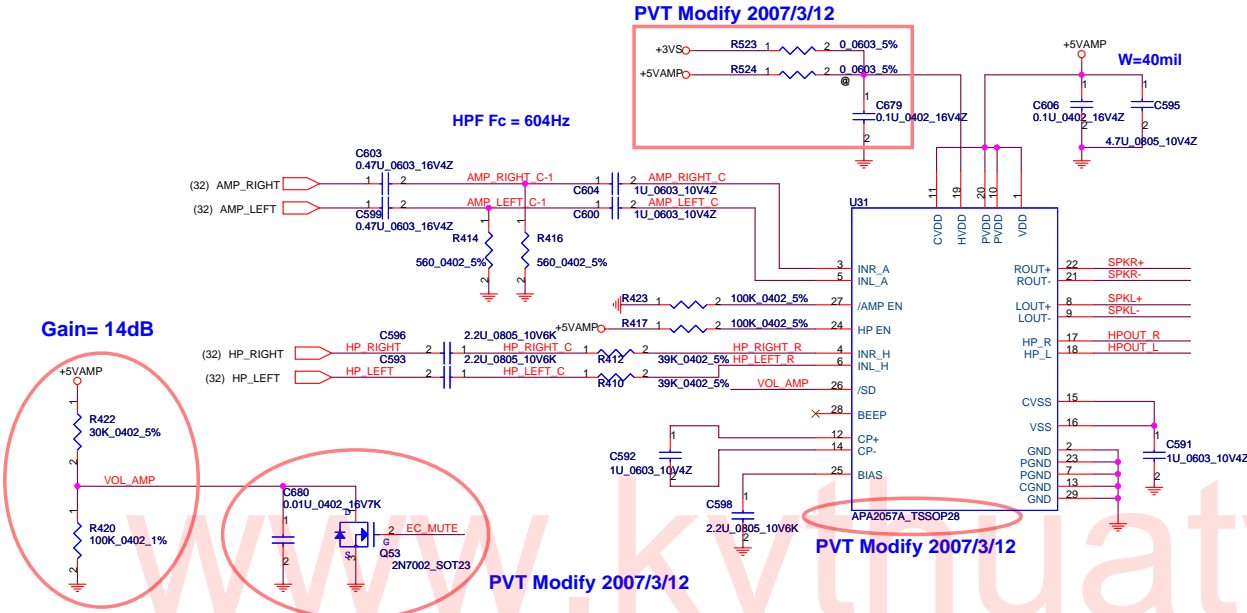
HD Audio Codec



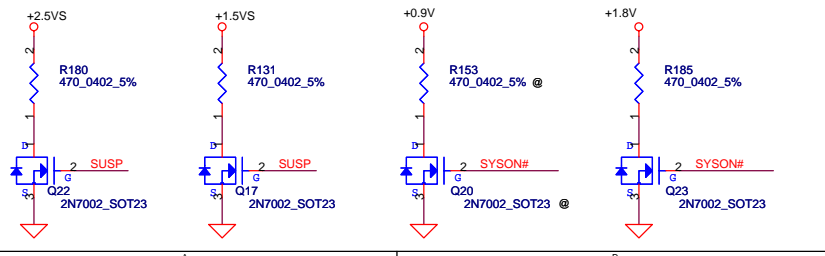
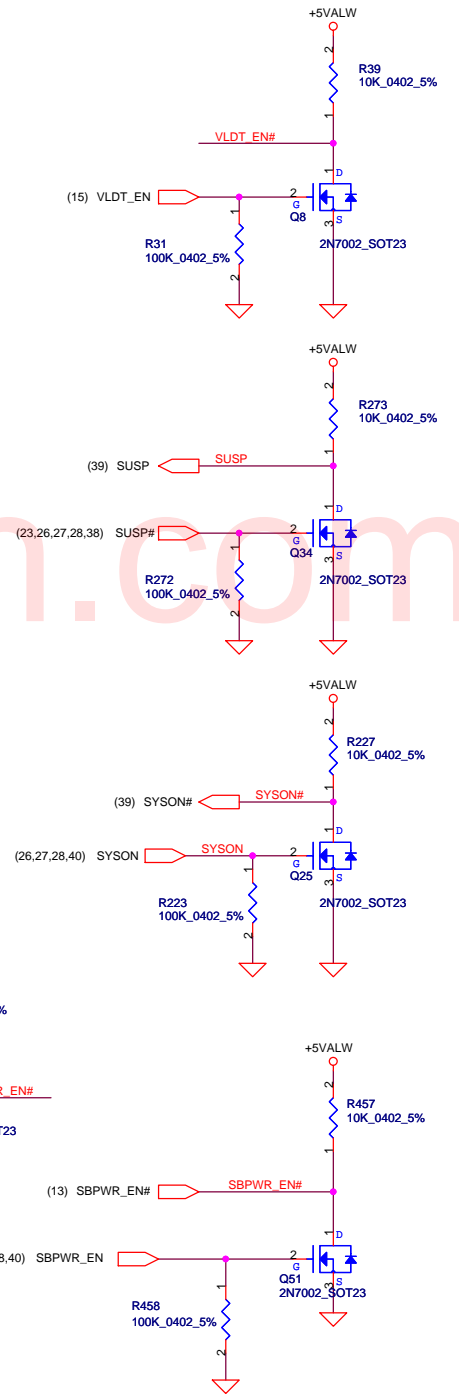
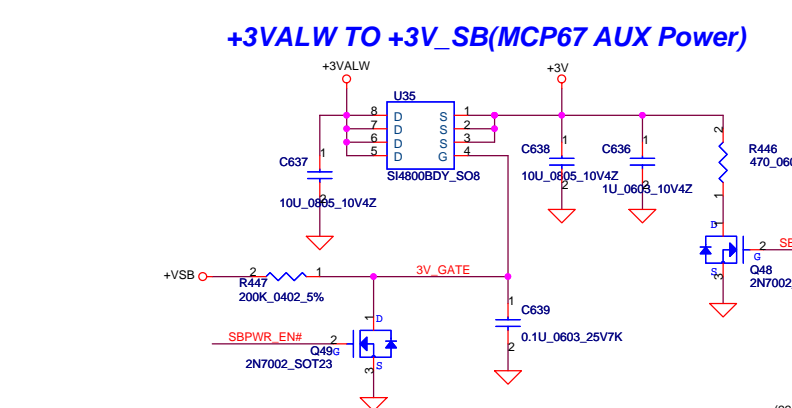
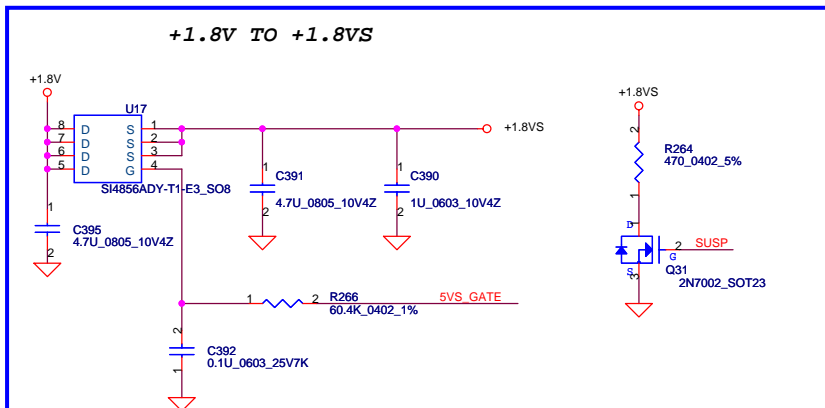
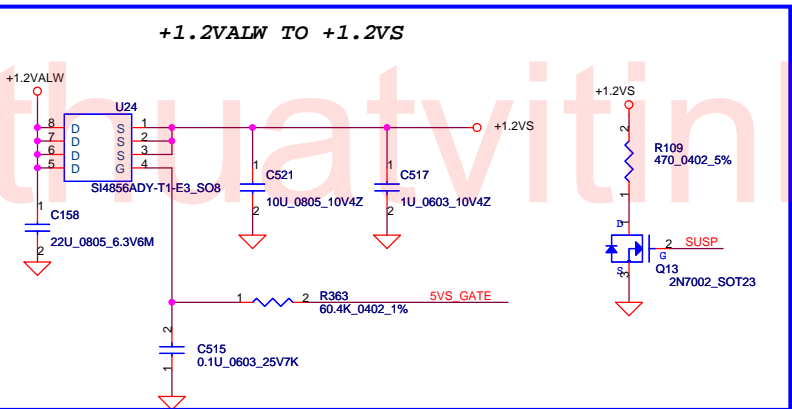
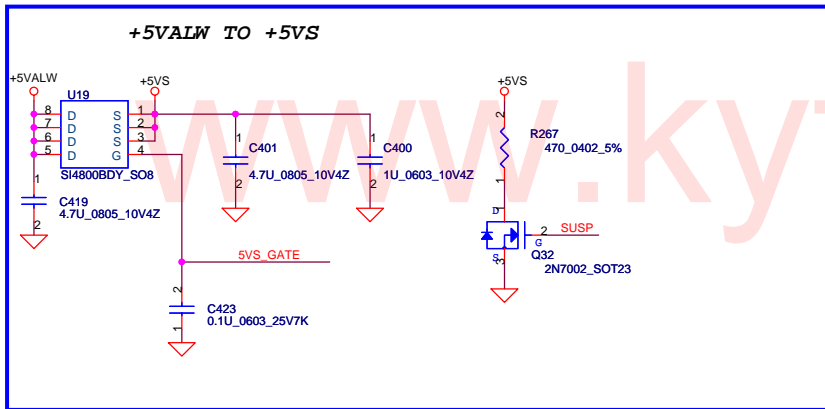
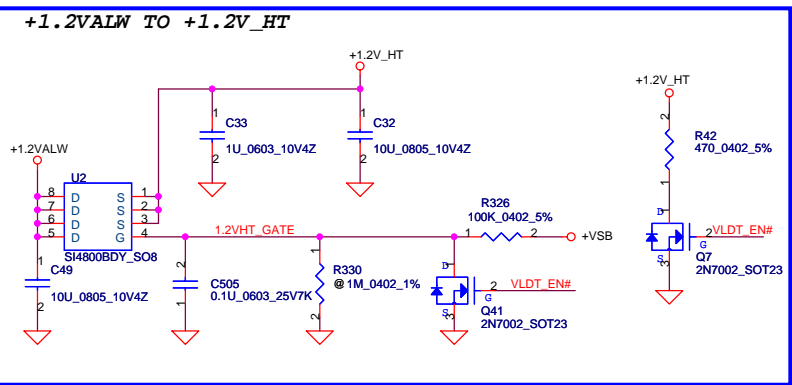
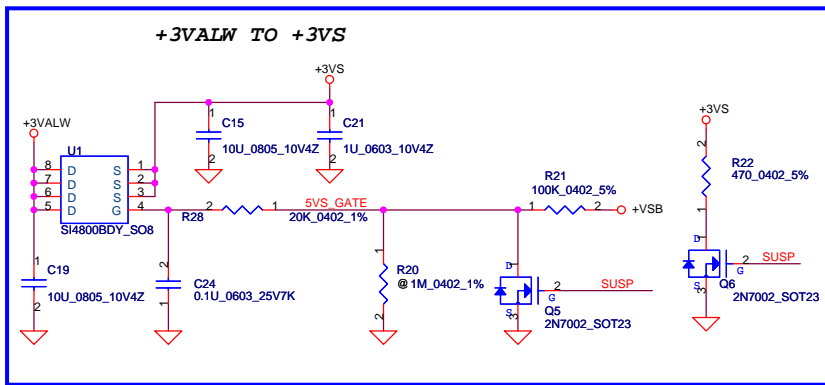
EMI Added 2007/4/12



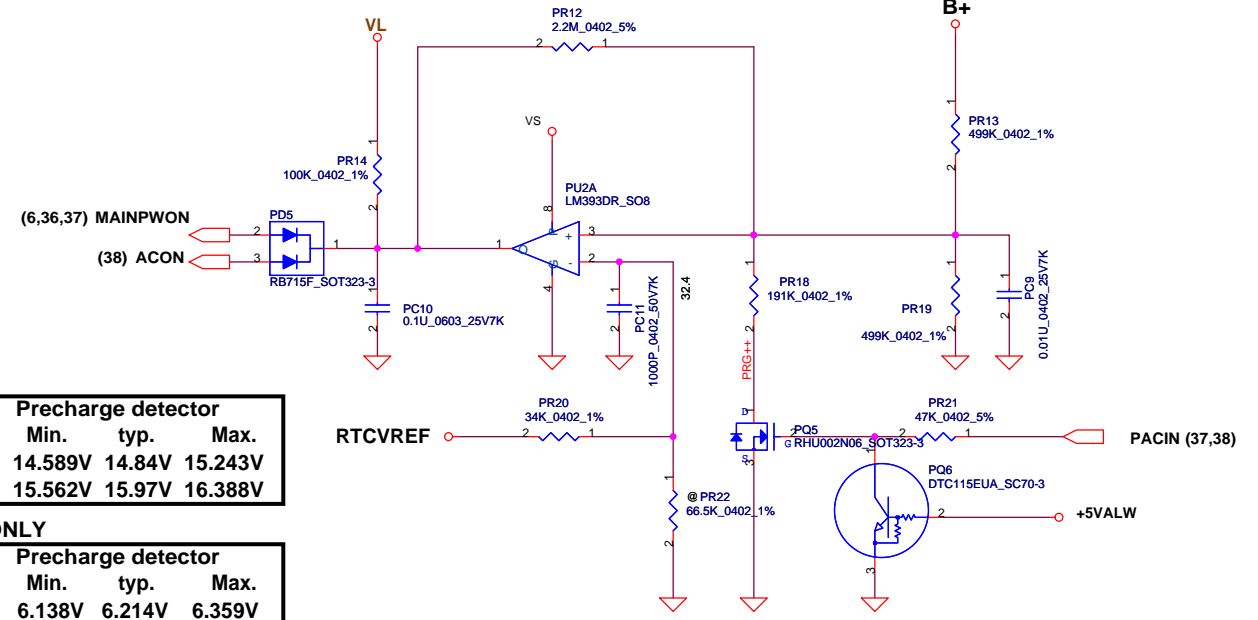
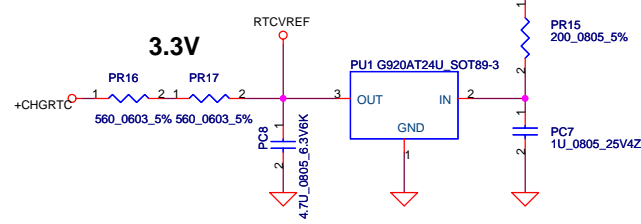
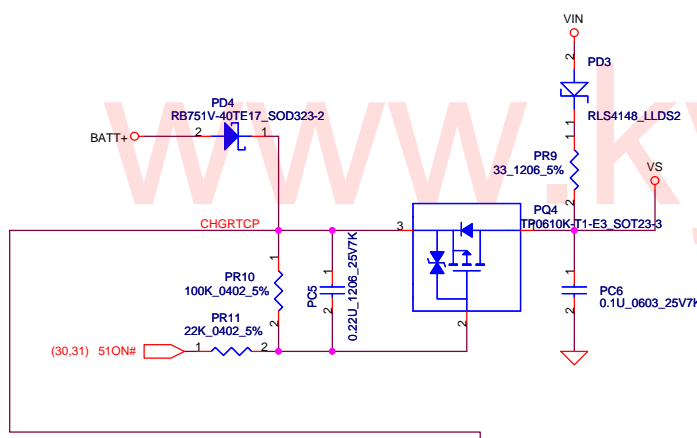
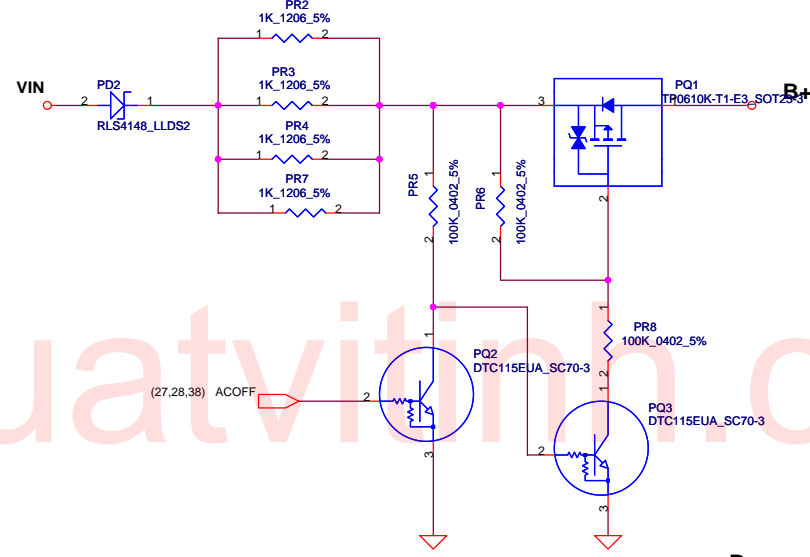
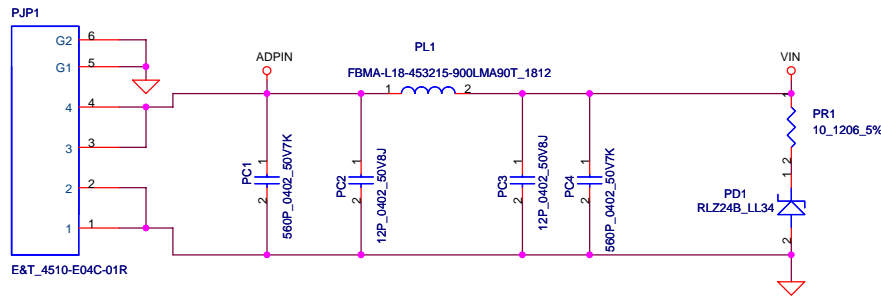
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



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Size	Document Number		Rev		1.0
B	ICW50 / ICY70 LA-3581P		Date:		Friday, April 20, 2007
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC INTERFACE	
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Size	Document Number			Rev	
B	ICW50 / ICY70 LA-3581P			1.0	
Date:	Friday, April 20, 2007	Sheet	34	of	42



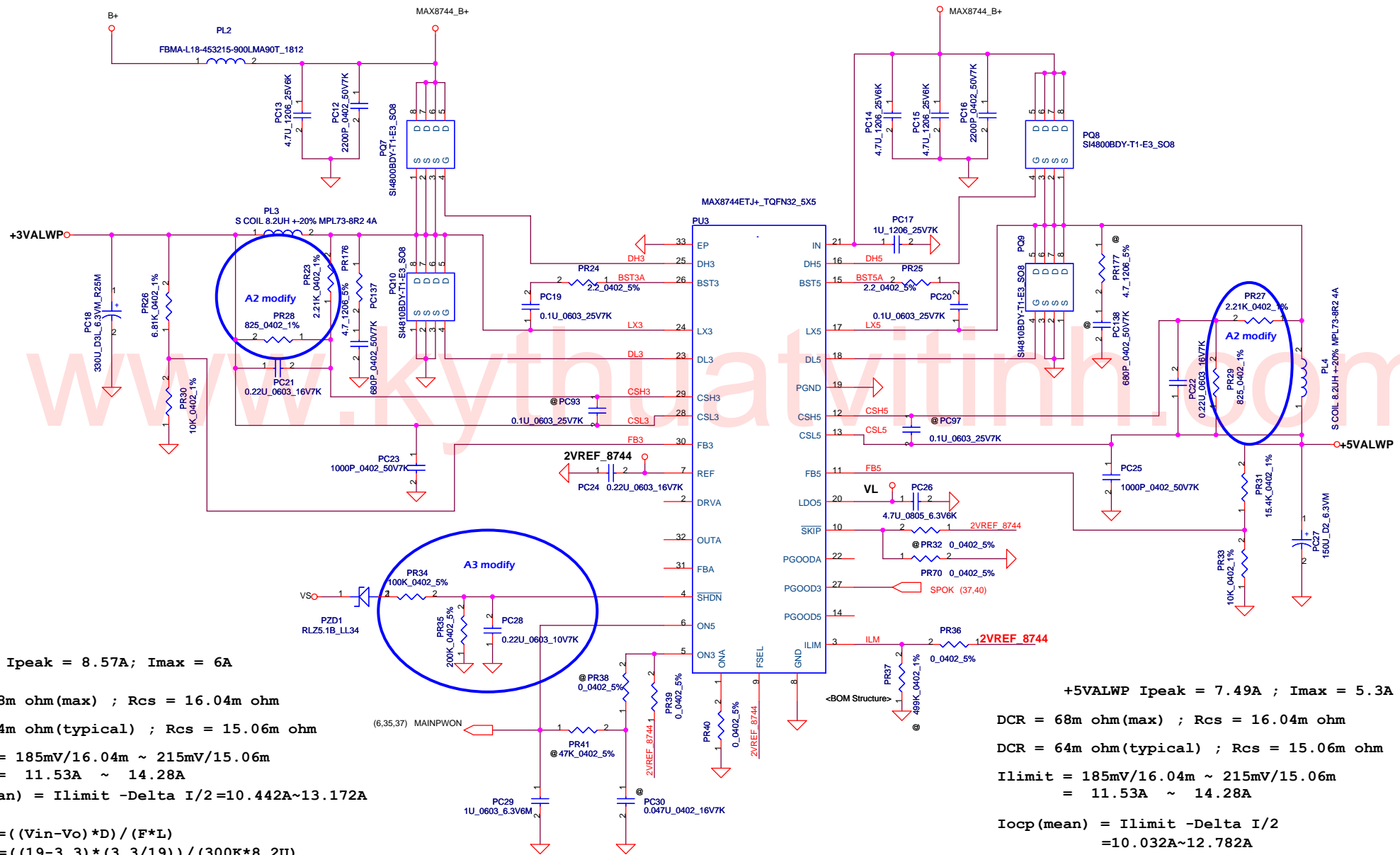
ACIN

	Min.	typ.	Max.
Precharge detector			
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Min.	typ.	Max.
Precharge detector			
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Size B	Document Number	Rev		1.0
	ICW50/ICY70			
Date:	Friday, April 20, 2007	Sheet	35	of 42



+3VALWP Ipeak = 8.57A; Imax = 6A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2 = 10.442A~13.172A

$$\Delta I = ((V_{in} - V_o) * D) / (F * L)$$

$$= ((19 - 3.3) * (3.3 / 19)) / (300K * 8.2U)$$

$$= 1.108A$$

Notes :

$$f_{ESR} \leq f_{OSC} / \pi ; f_{ESR} = 1 / (2 * \pi * RESR * COUT)$$

ON3 = REF ---> 3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 7.49A ; Imax = 5.3A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

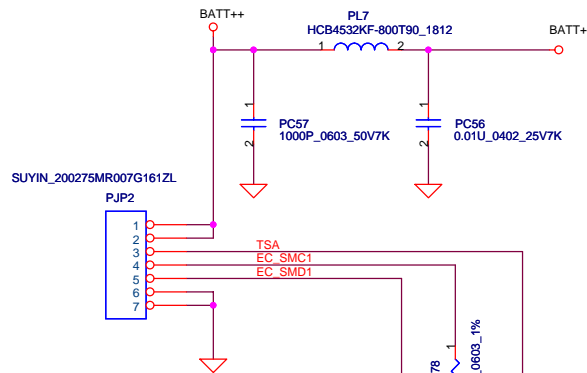
Iocp(mean) = Ilimit -Delta I/2
= 10.032A~12.782A

$$\Delta I = ((V_{in} - V_o) * D) / (F * L)$$

$$= ((19 - 5) * (5 / 19)) / (300K * 8.2U)$$

$$= 1.498A$$

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Issued Date	2006/09/01	Deciphered Date	2007/09/01	Title	+5VALWP/+3VALWP
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				Rev	1.0

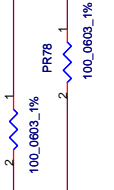


PJP2 battery connector

- SMART Battery:**
 1.BATT+
 2.BATT+
 3.TS
 4.SMC
 5.SMD
 6.GND
 7.GND

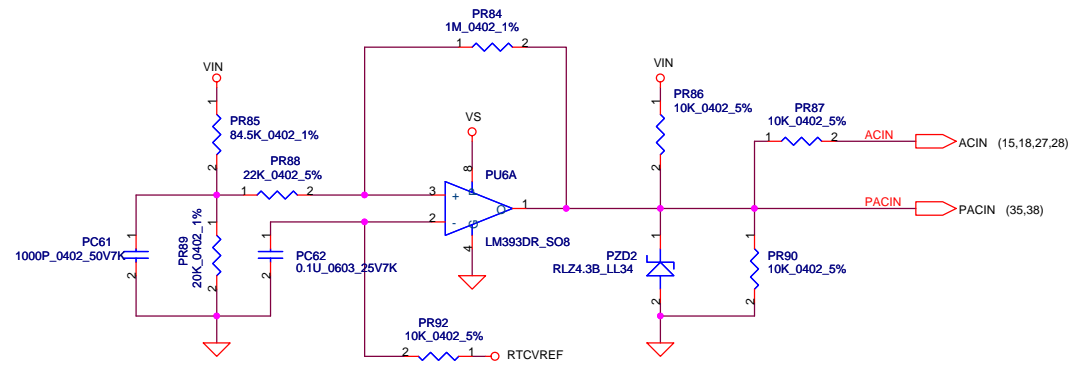
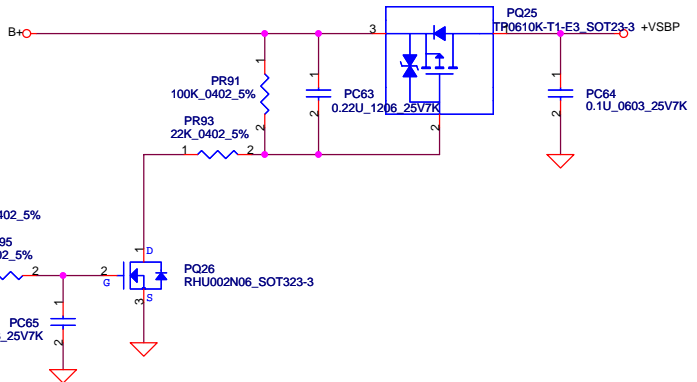
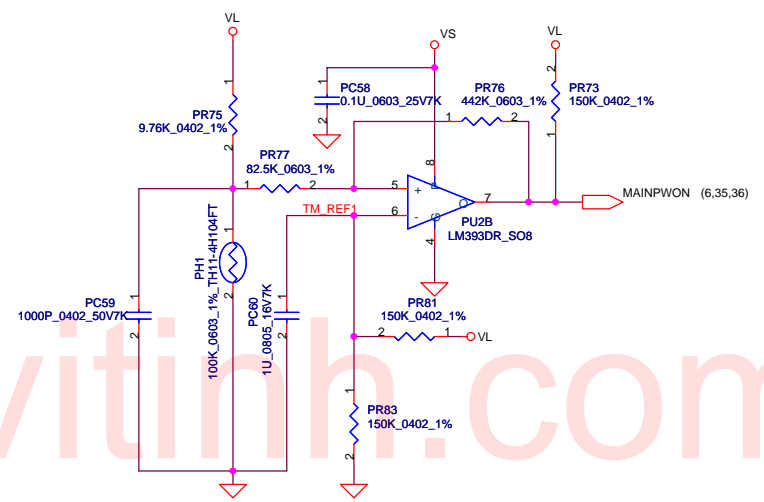
SUYIN_200275MR007G161ZL

TSA
 EC_SMC1
 EC_SMD1



- ▶ BATT_TEMP (27,28)
- ▶ EC_SMB_CK1 (18,27,28,29)
- ▶ EC_SMB_DA1 (18,27,28,29)

PH1 under CPU bottom side :
 CPU thermal protection at **90 degree C**
 Recovery at 70 degree C



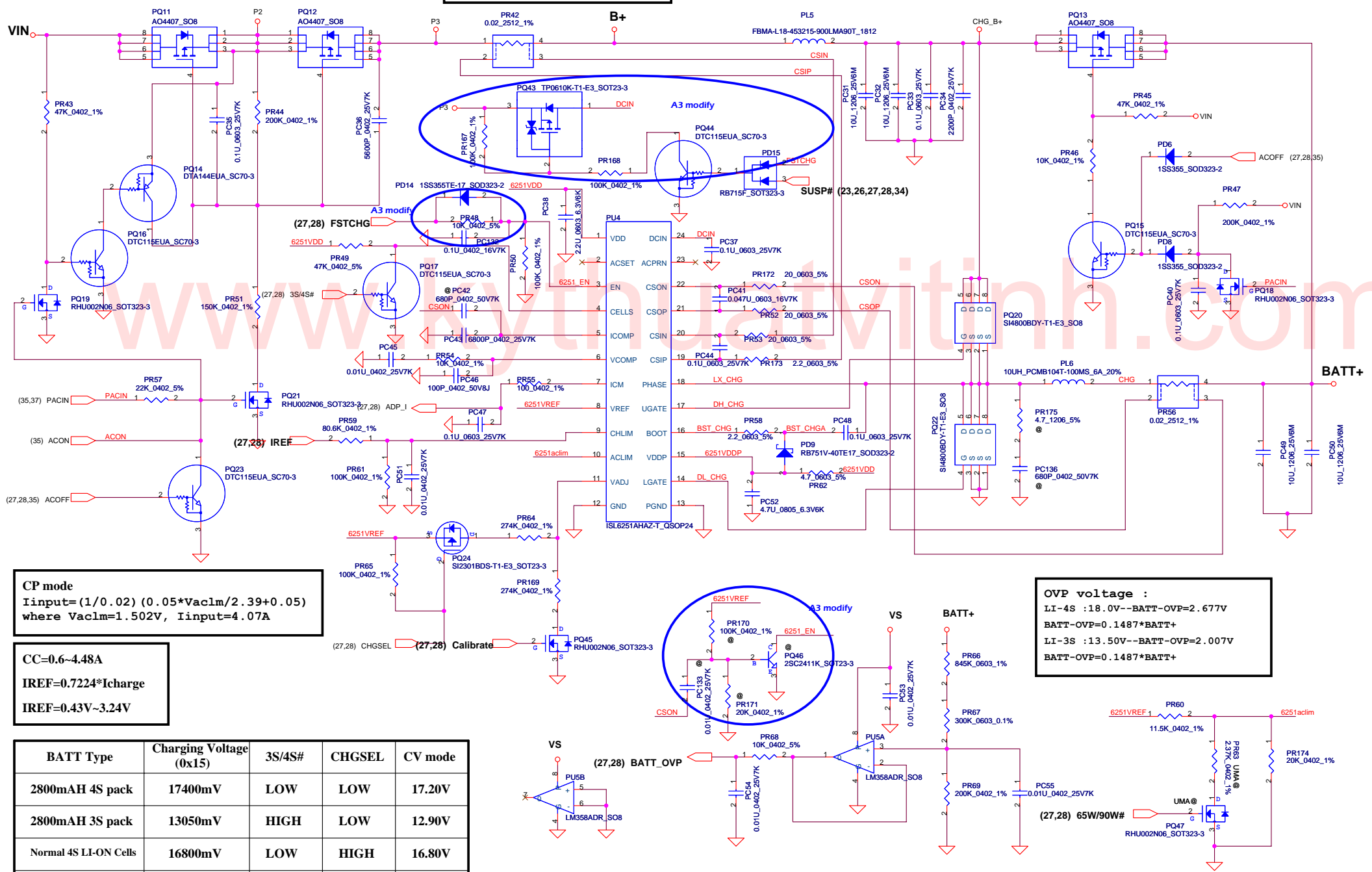
Vin Detector			
	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

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Iada=0~4.74A (90W)

$$ADP_I = 19.9 * I_{adapter} * R_{sense}$$

$$CP = 85\% * I_{ada} ; CP = 4.07A$$



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$
 where $V_{aclm} = 1.502V$, $I_{input} = 4.07A$

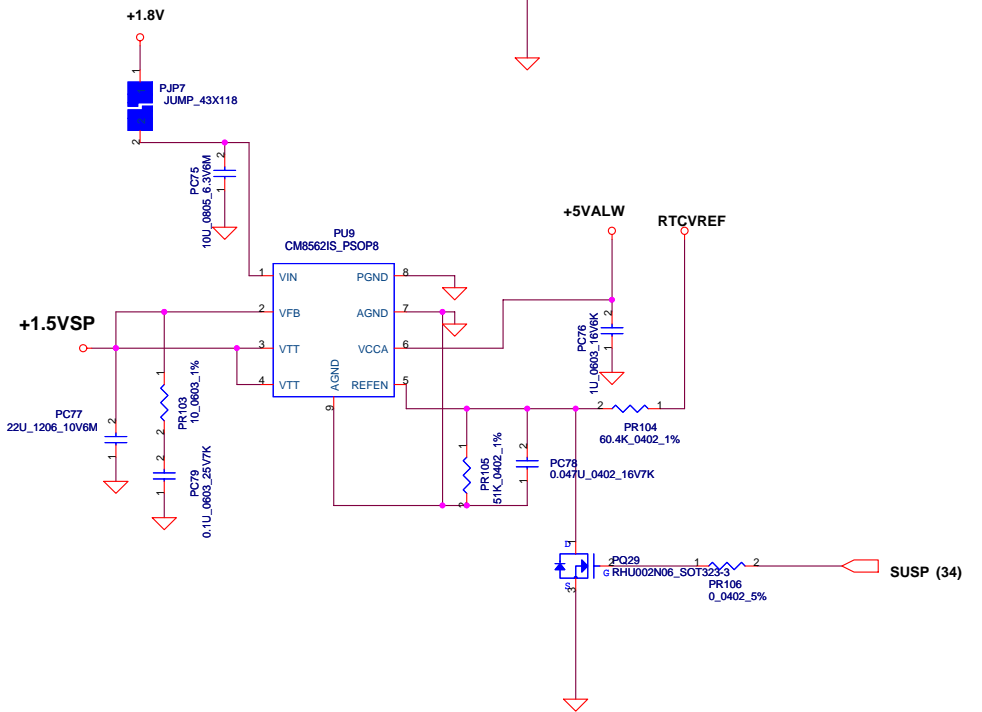
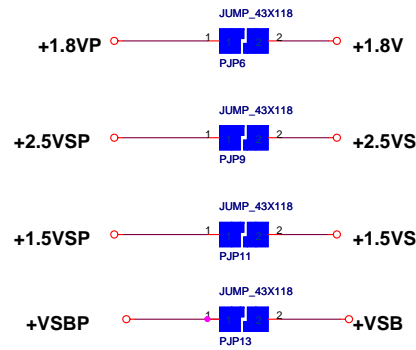
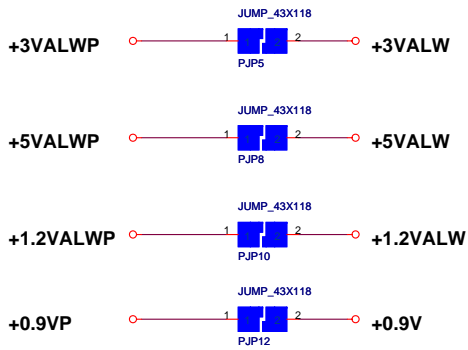
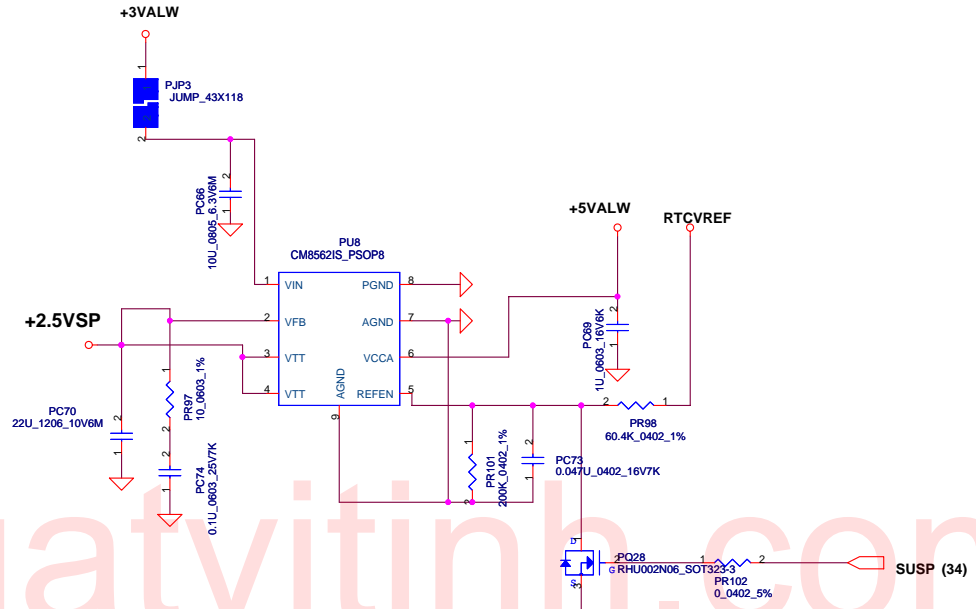
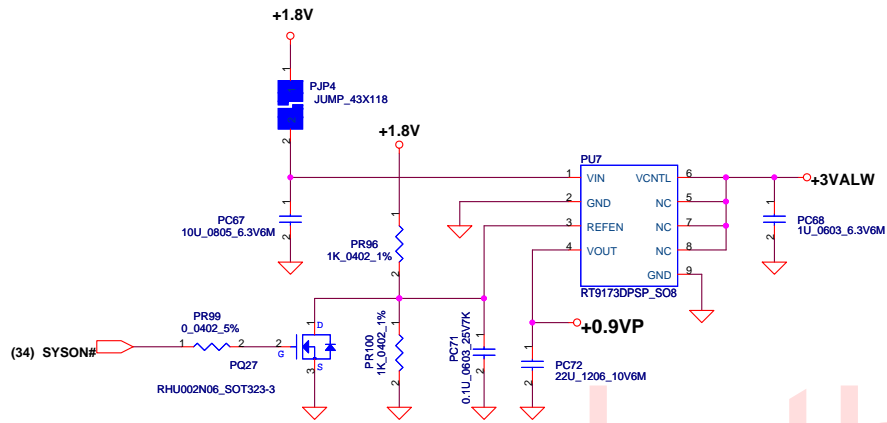
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

OVP voltage :
 LI-4S : 18.0V -- BATT-OVP = 2.677V
 $BATT-OVP = 0.1487 * BATT+$
 LI-3S : 13.50V -- BATT-OVP = 2.007V
 $BATT-OVP = 0.1487 * BATT+$

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

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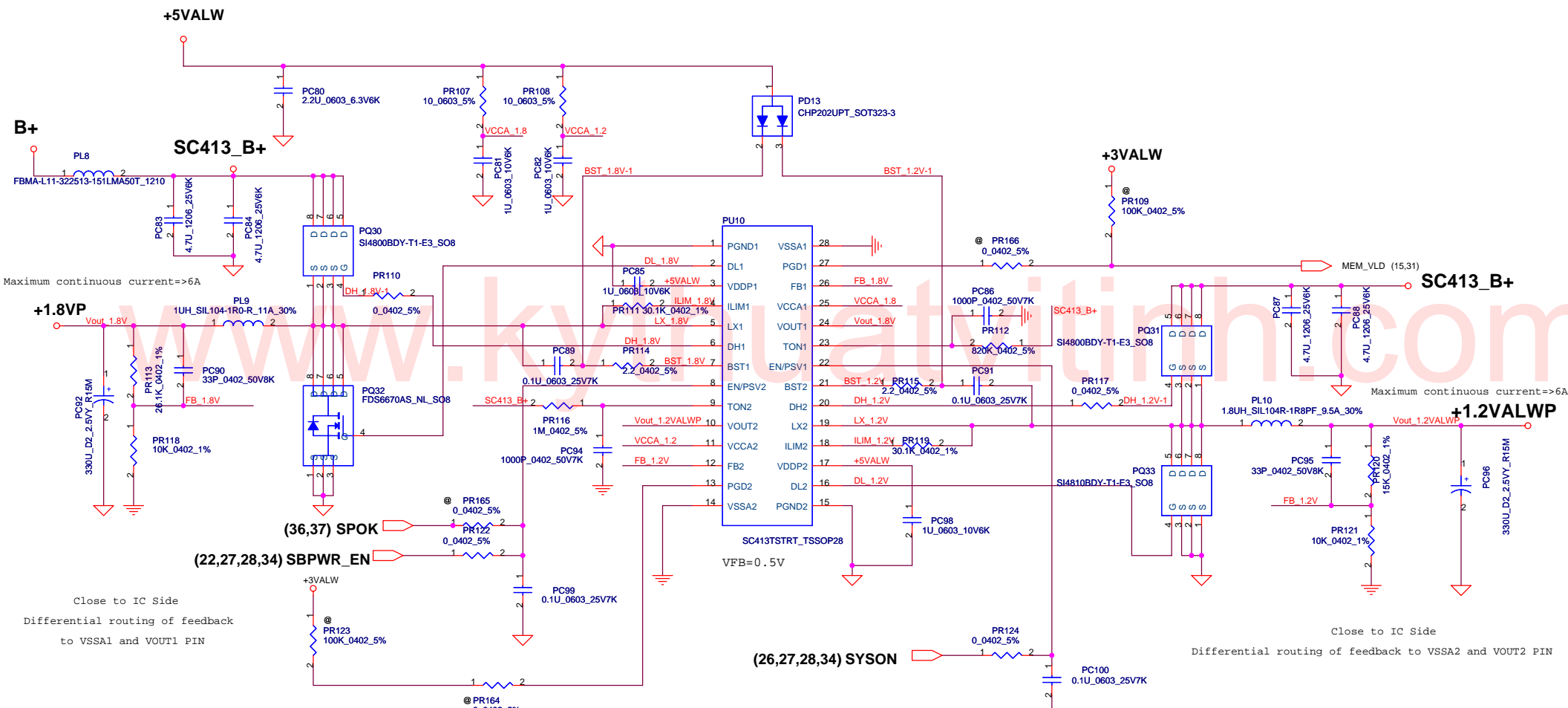
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CHARGER			
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Maximum continuous current=>6A

Maximum continuous current=>6A

Close to IC Side
Differential routing of feedback
to VSSA1 and VOUT1 PIN

Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$
 $I_{peak} = 13.82A, I_{max} = 9.68A$
 $Ton = (3.3E-12 * (PR112 + 37K) * (Vout / VBat)) + 50ns$
 $= 3.3E-12 * (820K + 37K) * (1.805 / 19) + 50ns = 0.319us$
 $FDS6670AS: Rds(on) => Typ: 9 mOhm$
 $Max: 11.5 mOhm$
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
 $I_{ripple} = (vin - vout) * (Ton / L) = 5.485A$
 $I_{valleymin} = 9E-6 * (PR106 / Rds(ON) * max * 1.4) = 16.826A$
 $I_{valleymax} = 11E-6 * (PR106 / Rds(ON) * typ * 1.2) = 30.657A$
 $OCP => 19.5685A \sim 33.3995A$

VFB=0.5V
 $V_o = VFB * (1 + PR120 / PR121) = 1.25V$
 $I_{peak} = 8.54A, I_{max} = 6A$
 $Ton = (3.3E-12 * (PR116 + 37K) * (Vout / VBat)) + 50ns$
 $= 0.2661us$
 $SI4810BDY: Rds(on) => Typ: 16 mOhm$
 $Max: 20 mOhm$
 $I_{valleymin} = 9E-6 * (PR119 / Rds(ON) * max * 1.3) = 10.419A$
 $I_{valleymax} = 11E-6 * (PR119 / Rds(ON) * typ * 1.1) = 18.8125A$
 $I_{ripple} = (vin - vout) * (Ton / L) = 2.631A$
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
 $OCP => 11.7345A \sim 20.128A$

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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
1	BOM Change.	0.4	12	Remove R144, R372, C160, C528.		PVT
2	Added SSC for Lan TXCLK. (EMI Request)	0.4	12	Added U40, R525, R526, R527, R528, C682.		PVT
3	Improve Samsung Memory Module compatibility.	0.4	15	Added R540,R541 2.2K pull up +3VS.		PVT
4	Design Modify. (SCH Change)	0.4	15	Change CRT_DET form GPIO_5 to LID#, Add R78 10K. (Bios Request)		PVT
5	BCIC0172 : When Reset or Cold Boot MCP67 ACIN 會漏電到EC.	0.4	15	D24 反向, 47K Pull High 移除. Added R283 200K Pull Down.		PVT
6	RTC Battery 電壓過低.	0.4	16	Added R539 1K.		PVT
7	Design Modify. (SCH Change)	0.4	22	Change Q50.G Pin Net Name to SBPWR_EN.		PVT
8	Added R-C for BUF_25Mhz (EMI Request).	0.4	22	Added R530,C684.		PVT
9	Design Modify for EMI.	0.4	22	Added L59, L60, L61, L62, C685, C686.		PVT
10	解決+3VS 漏電 when enter S3 Mode.	0.4	25,26	Added Q56, Q57, Q58, Q59, R536, R537.		PVT
11	Design Modify for Acer WLAN LED.	0.4	25	JP21.44 Pin Added MINI1_LED# Net, Added R520, R521.		PVT
12	防止 BATT_TEMP, BATT_OVP, ACIN 被干擾.	0.4	27	Added C660, C661, C662.		PVT
13	Design Modify for Power. (65W/95W Detect Function)	0.4	27	U15.98 Pin Added 65W/95W# Net, Added R519 100K to +3VALW.		PVT
14	Design Modify for EMI.	0.4	30	Added C663~C678.		PVT
15	For AUDIO EA Test.	0.4	32	Change C582, C583, C584, C587,C594, C597 to 4.7uF.		PVT
16	解決關機 bo bo 聲問題.	0.4	33	Added Q53,C680.		PVT
17	Design Modify for EMI.	0.4	33	Added L57, L58 for Mic. L63, L64, L65, L66 for SPK. D28 for ESD.		PVT
18	Change Codec Amp to APA2057RI-TRL_TSSOP28.	0.4	33	Change U31 to SA00001QD00, added R523,R524.		PVT
19	Remove PJP14.	0.4	34	Remove PJP14.		PVT
20	Change MCP67-MV form A01 to A02.	0.4	10~17	Change MCP67-MV form A01 to A02.		PVT
21	解決系統時間延遲問題.	0.4	15	Change C503, C504 form 18pF to 6.8pF.		PVT
22	Improve WLAN Module compatibility.	0.3	11,25	Change WLAN Port form PCIE4 to PCIE2.		DVT2
23	Fixed LAN LED work abnormal.	0.3	22	Added D25,D27,D27, U39.		DVT2
24	Change LAN to RTL8211B.	0.2	22	Change Page 22 all compnent. DVT1		

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