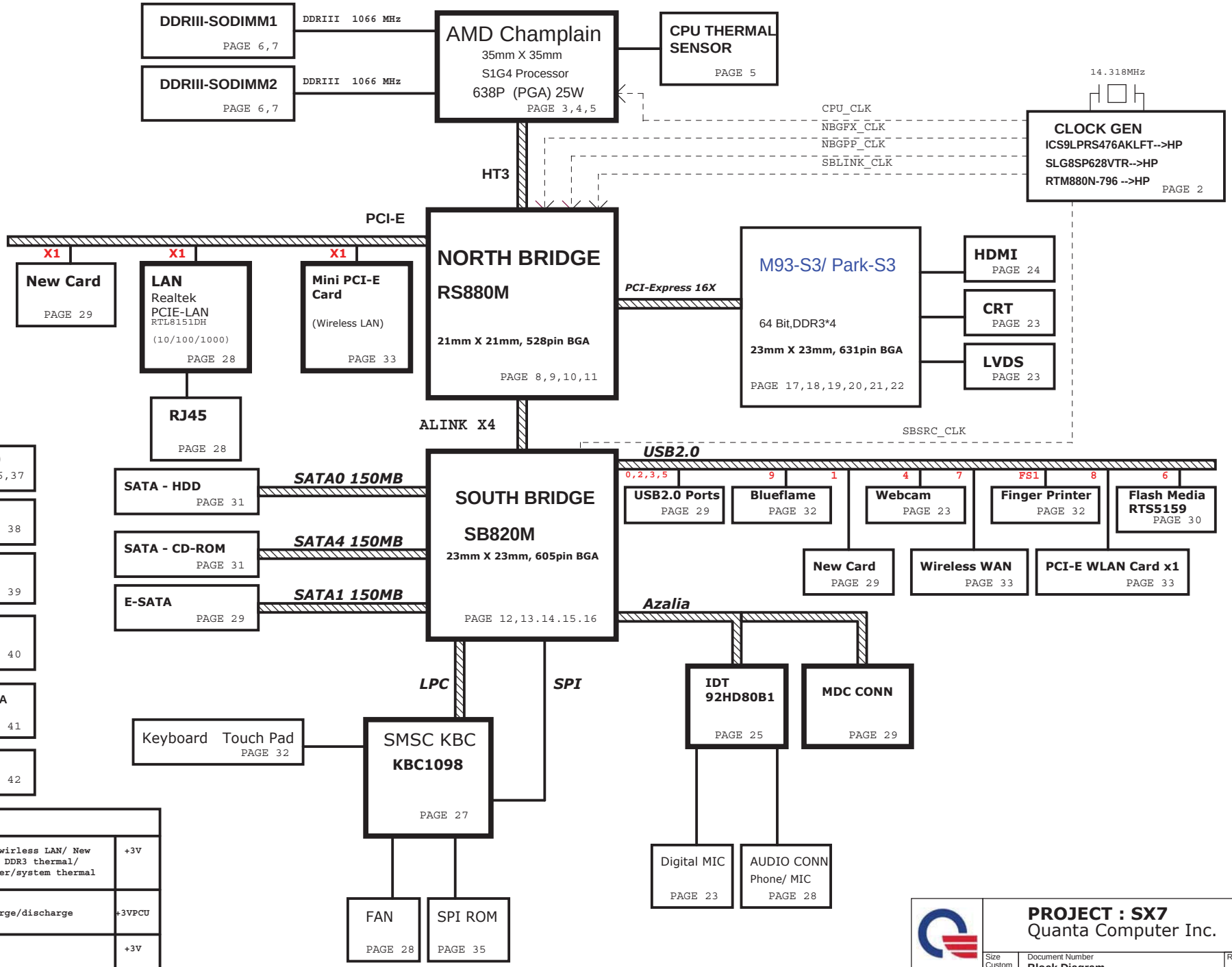
SX7 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



SYSTEM CHARGER(bq24740) PAGE 36,37

3/5VS5 RT8206B PAGE 38

+1.1V(RT8029)/+1.1VS5/+1.8V PAGE 39

DDR3 (RT8207)/+1.0V_VGA PAGE 40

VGACORE(1.1V~0.9V)RT8028A PAGE 41

CPU_CORE ISL6265 PAGE 42

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/ wirless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal	+3V
EC -- AB1A	Battery charge/discharge	+3VPCU
EC -- AB2A	VGA thermal	+3V

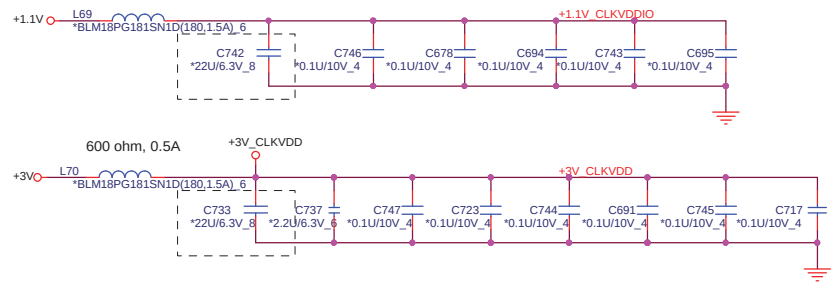
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

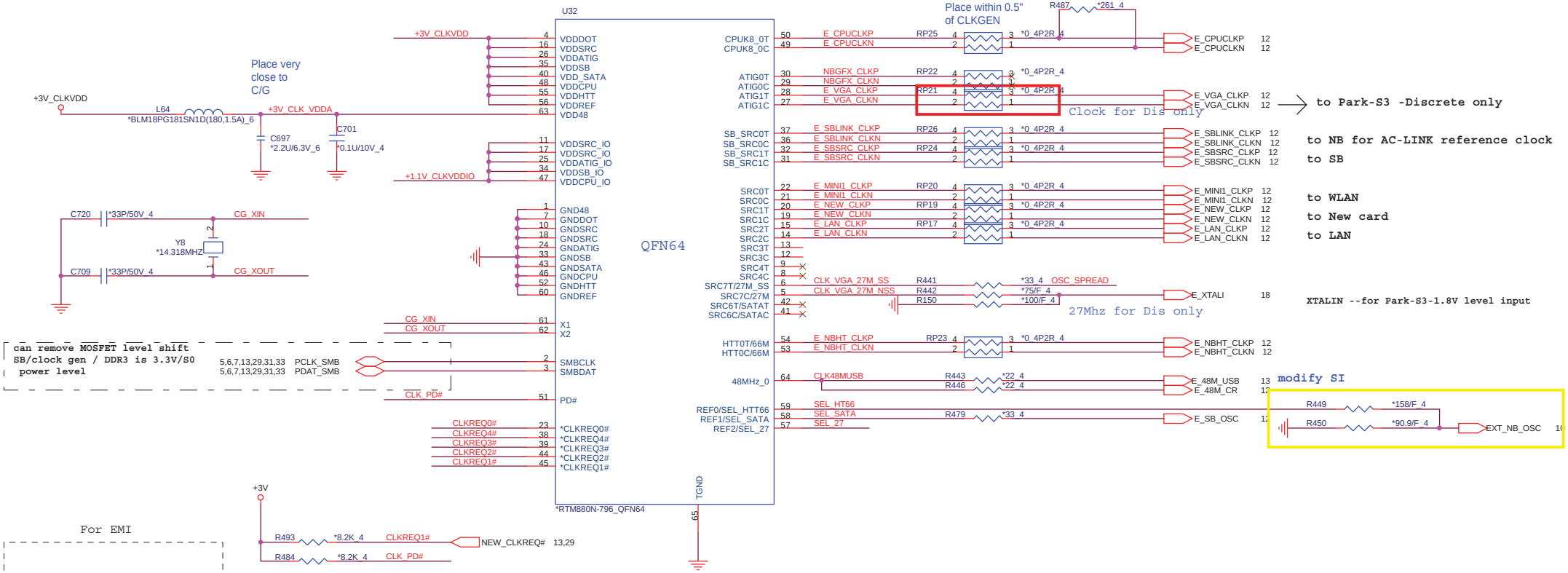
Size	Document Number	Rev
Custom	Block Diagram	3A

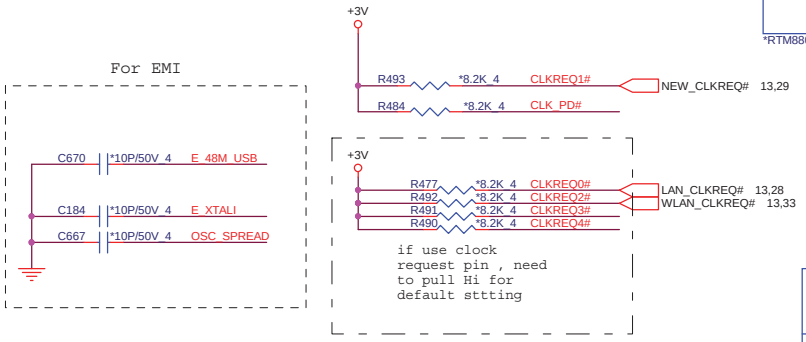
Date: Monday, March 15, 2010 Sheet 1 of 43

CLOCKS name	Discrete	Clock pin function
NBGFX_CLKP NBGFX_CLKN	NA	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP21 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP26 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R441,R442 STUFF	To Park-S3 27Mhz - Discrete only



Need check the net name for the short pad

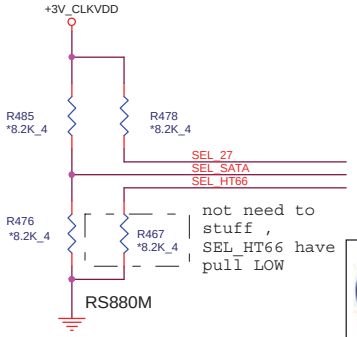




IDT ICS9LPRS480AKLFT--ALPRS480000
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



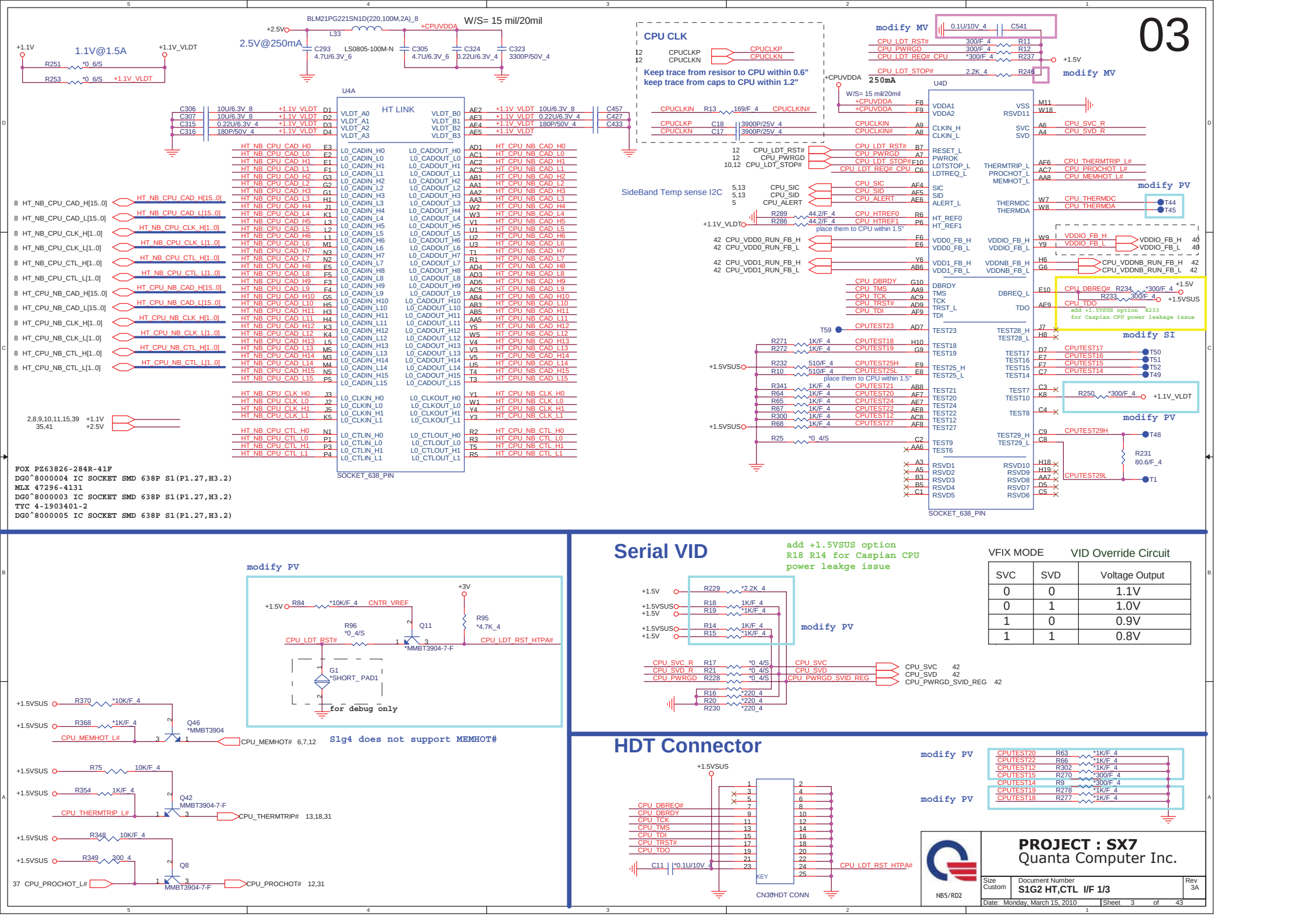
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	3A

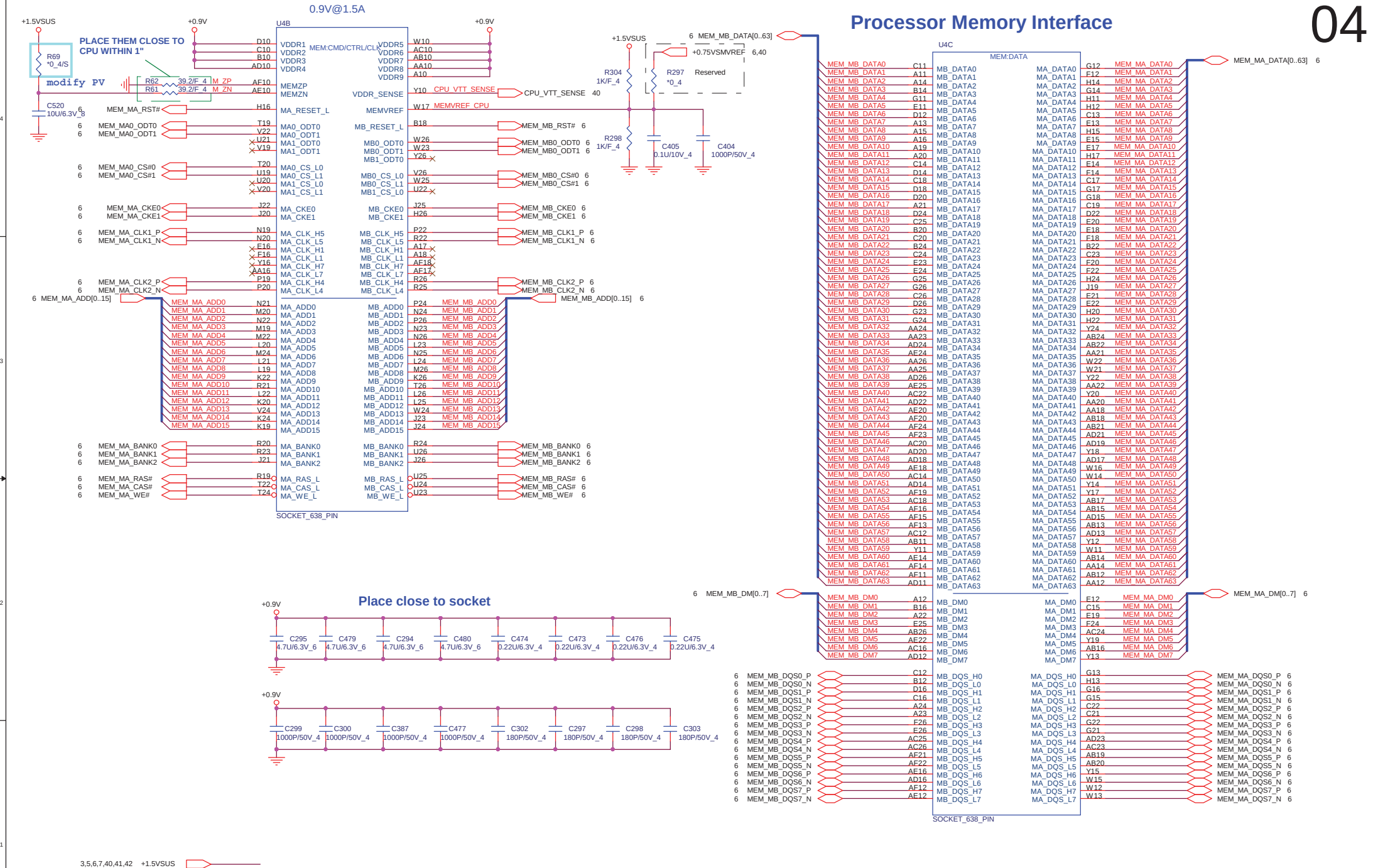
Date: Monday, March 15, 2010 Sheet 2 of 43

NB5/RD2


03
1.1V@1.5A
2.5V@250mA
BLM21PG221SN1D(220,100M,2A)_8
W/S= 15 mil/20mil
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
HT LINK
SOCKET_638_PIN
SideBand Temp sense I2C
modify MV
modify PV
modify SI
add +1.5VSUS option R233 for Caspian CPU power leakage issue
place them to CPU within 1.5"
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
modify PV
for debug only
S1g4 does not support MEMHOT#
Serial VID
add +1.5VSUS option R18 R14 for Caspian CPU power leakge issue
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
HDT Connector
CN30HDT CONN
PROJECT : SX7
Quanta Computer Inc.
S1G2 HT,CTL I/F 1/3
Size Custom
Document Number
Rev 3A
Date: Monday, March 15, 2010
Sheet 3 of 43

Processor Memory Interface

04



PROJECT : SX7
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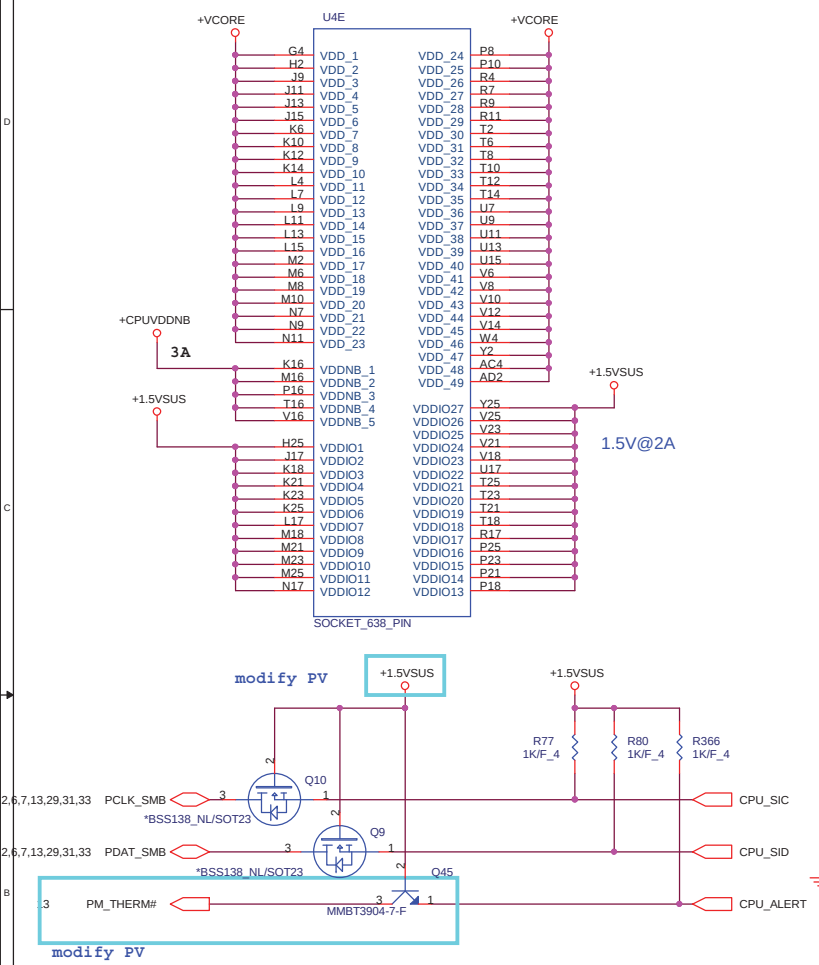
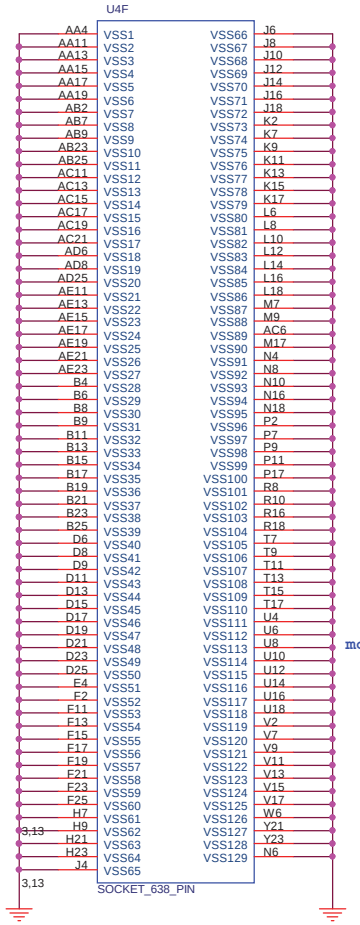
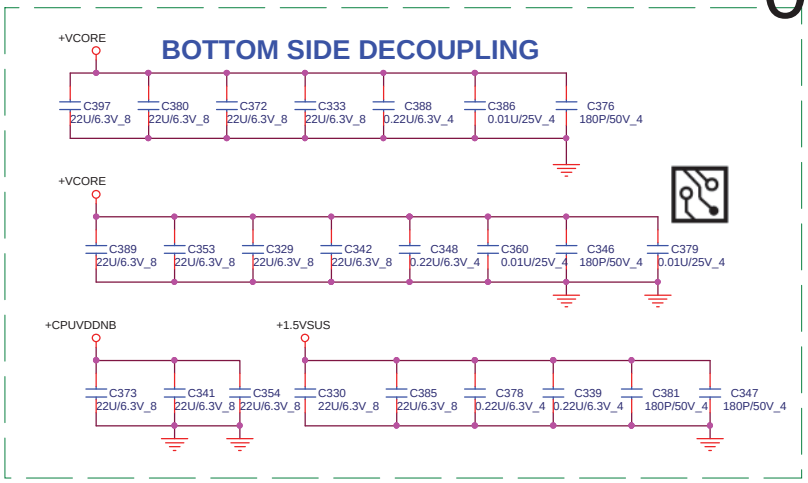
Size	Document Number	Rev
Custom	S1G2 DDRII MEMORY I/F 2/3	3A

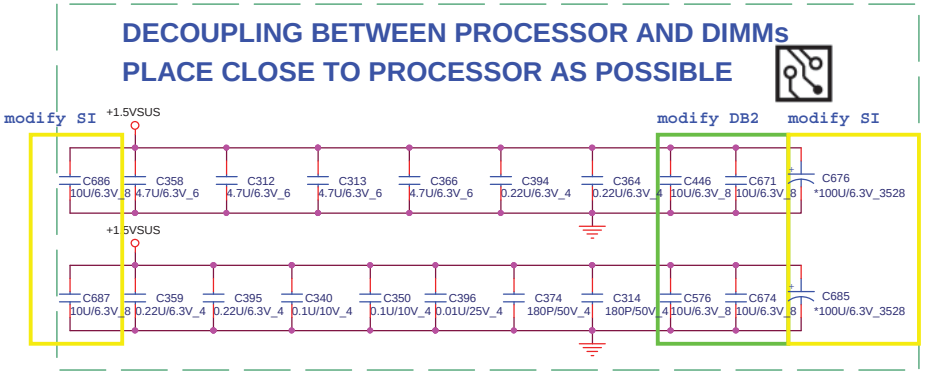
Date: Monday, March 15, 2010 Sheet 4 of 43

NB5/RD2



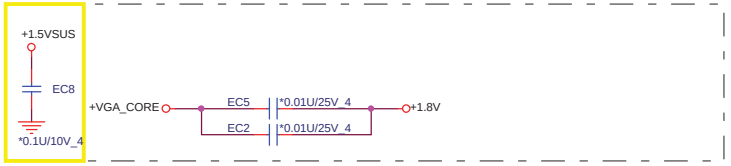


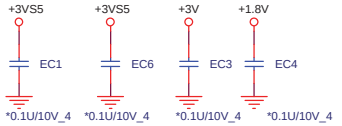




PROCESSOR POWER AND GROUND

For fix HyperTransport nets across plane splits



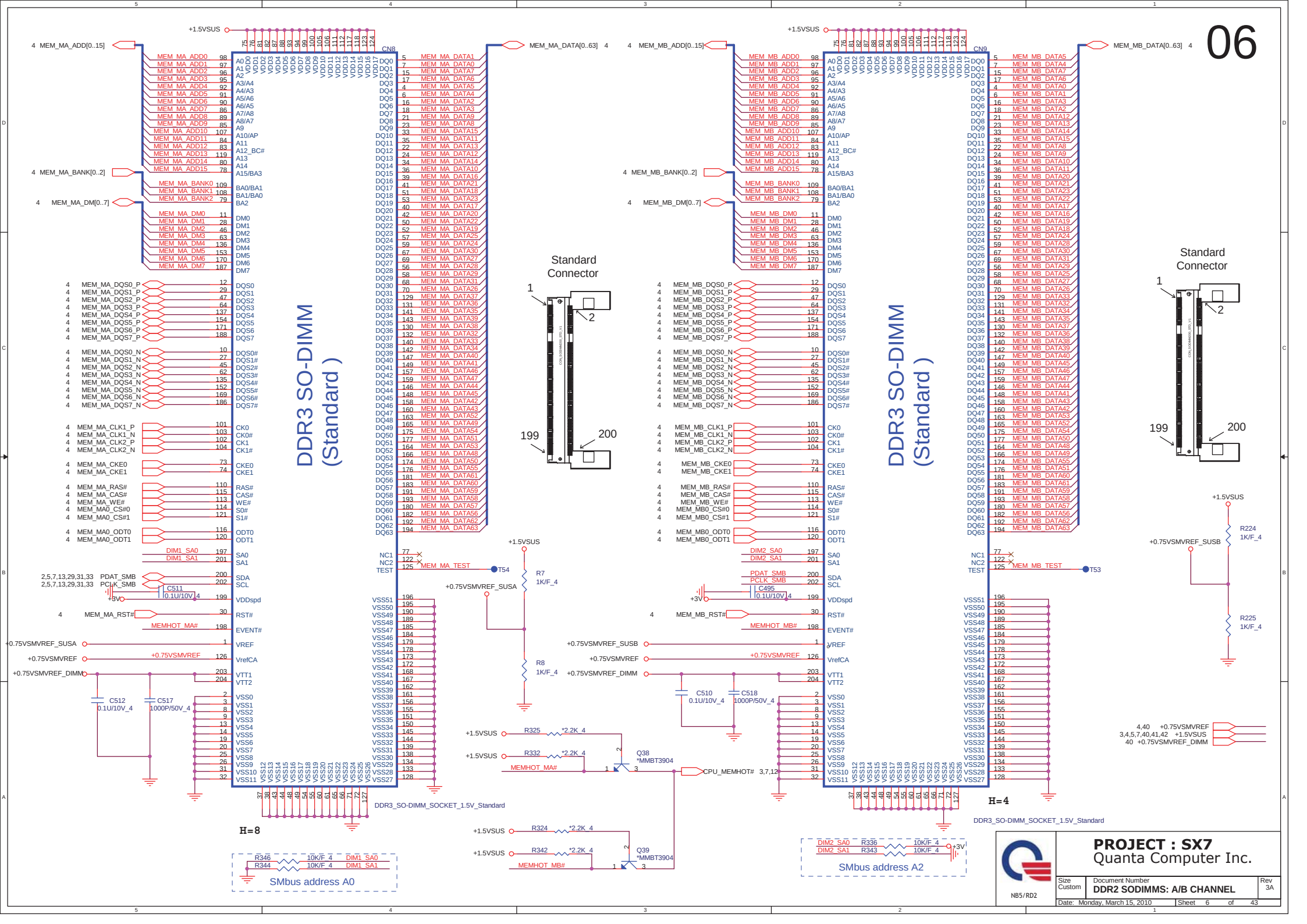


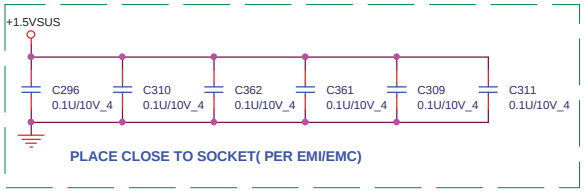
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

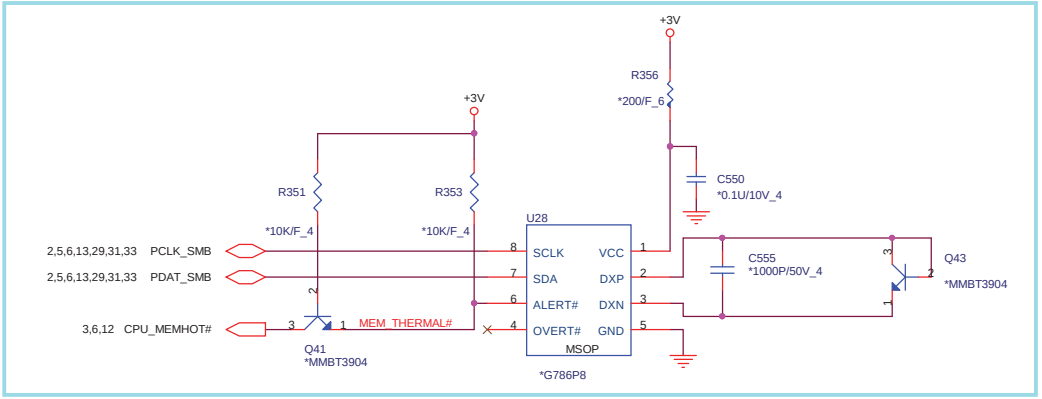
Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	3A

Date: Monday, March 15, 2010 | Sheet 5 of 43


CN8
DDR3 SO-DIMM
(Standard)
H=8
DDR3_SO-DIMM_SOCKET_1.5V_Standard
CN9
DDR3 SO-DIMM
(Standard)
H=4
DDR3_SO-DIMM_SOCKET_1.5V_Standard
Standard Connector
Standard Connector
SMbus address A0
SMbus address A2
+1.5VSUS
+0.75VSMVREF_SUSA
+0.75VSMVREF_SUSB
+0.75VSMVREF
+0.75VSMVREF_DIMM
+3V
MEM_MA_TEST
MEM_MB_TEST
MEMHOT_MA#
MEMHOT_MB#
CPU_MEMHOT# 3,7,12
Q38 *MMBT3904
Q39 *MMBT3904
R7 1K/F_4
R8 1K/F_4
R224 1K/F_4
R225 1K/F_4
C511 0.1U/10V_4
C512 0.1U/10V_4
C517 1000P/50V_4
C510 0.1U/10V_4
C518 1000P/50V_4
C495 0.1U/10V_4
R325 *2.2K_4
R332 *2.2K_4
R324 *2.2K_4
R342 *2.2K_4
R346 10K/F_4
R344 10K/F_4
R336 10K/F_4
R343 10K/F_4
DIM1_SA0
DIM1_SA1
DIM2_SA0
DIM2_SA1
PDAT_SMB
PCLK_SMB
2,5,7,13,29,31,33
4,40 +0.75VSMVREF
3,4,5,7,40,41,42 +1.5VSUS
40 +0.75VSMVREF_DIMM
NB5/RD2
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
DDR2 SODIMMS: A/B CHANNEL
Rev 3A
Date: Monday, March 15, 2010
Sheet 6 of 43



modify PV

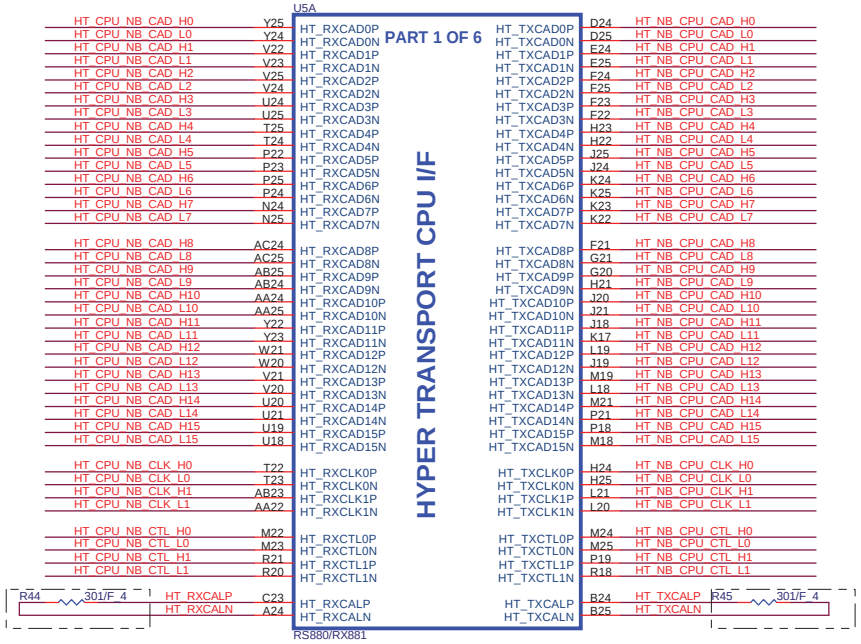


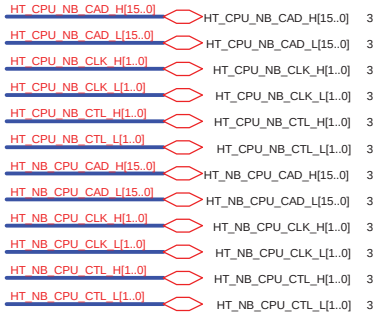
PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	3A

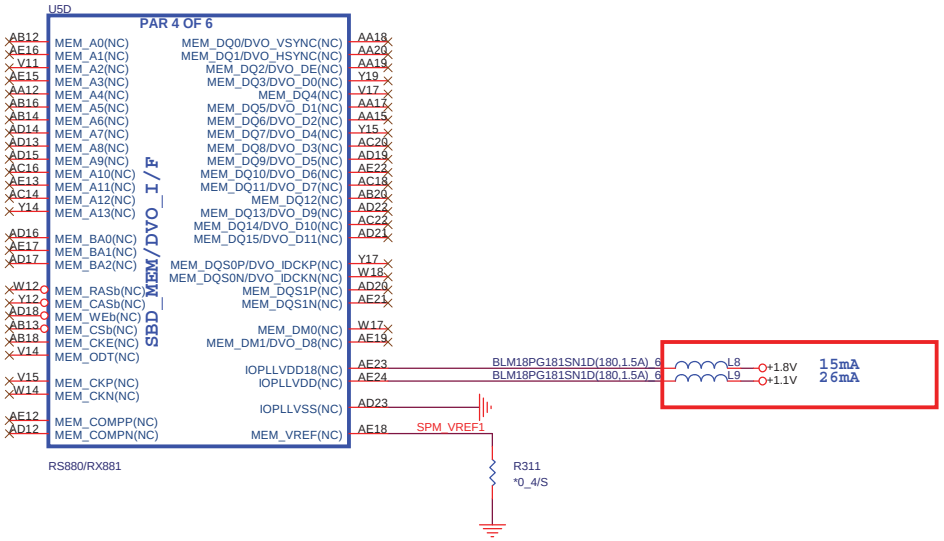
Date: Monday, March 15, 2010 Sheet 7 of 43





signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

This block is for UMA only , Discrete can remove all component

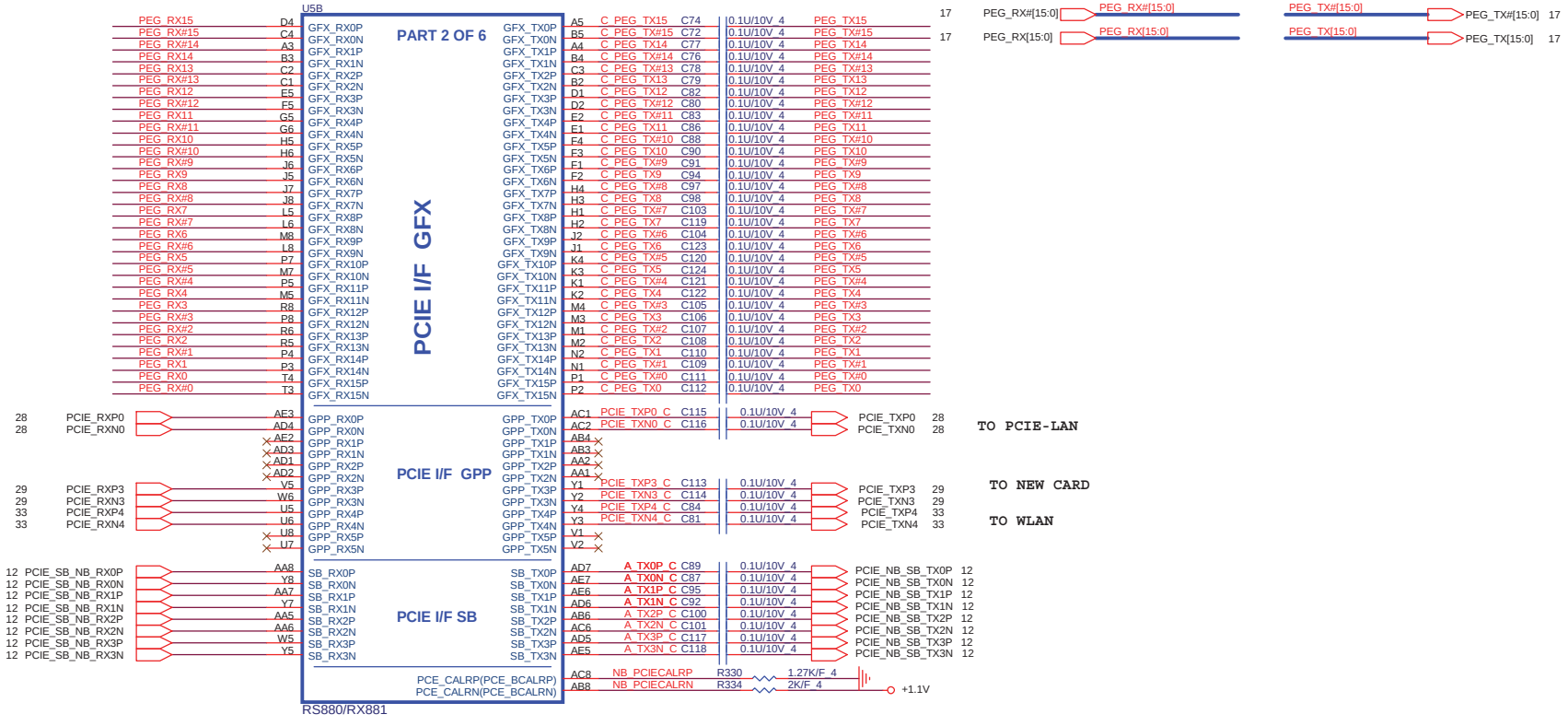


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M-HT LINK I/F 1/5	3A

Date: Monday, March 15, 2010 Sheet 8 of 43

NB5/RD2

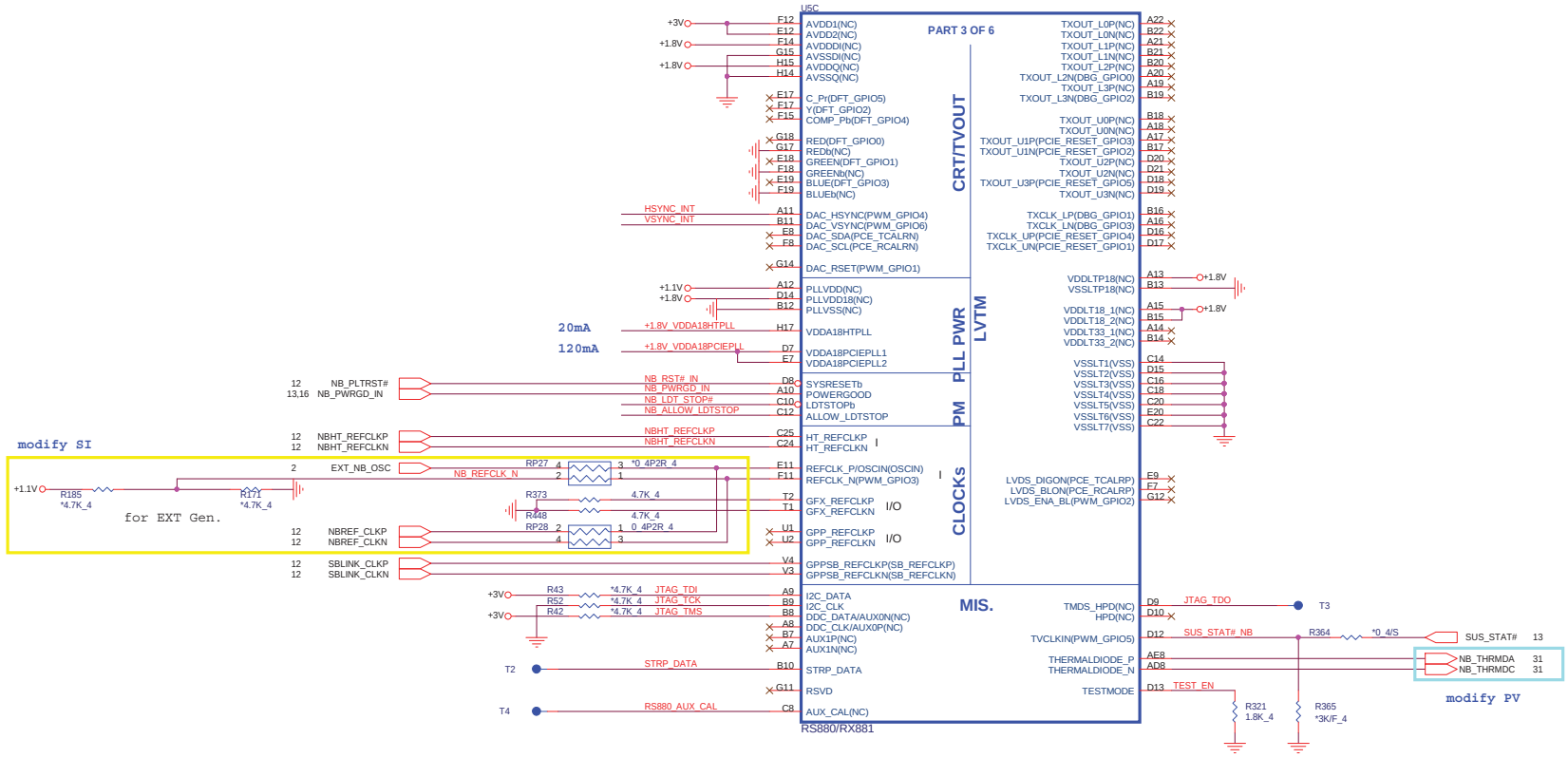


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M-PCIE I/F 2/5	3A

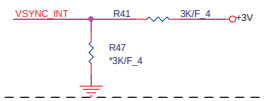
Date: Monday, March 15, 2010 Sheet 9 of 43

NB5/RD2



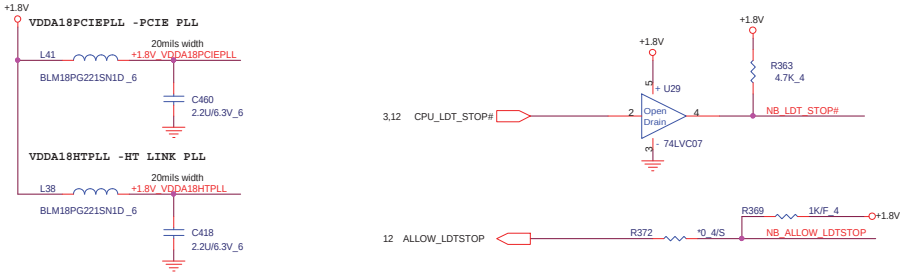
Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

Discrete



Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
(RX881 use DAC_HSYNC)

Discrete

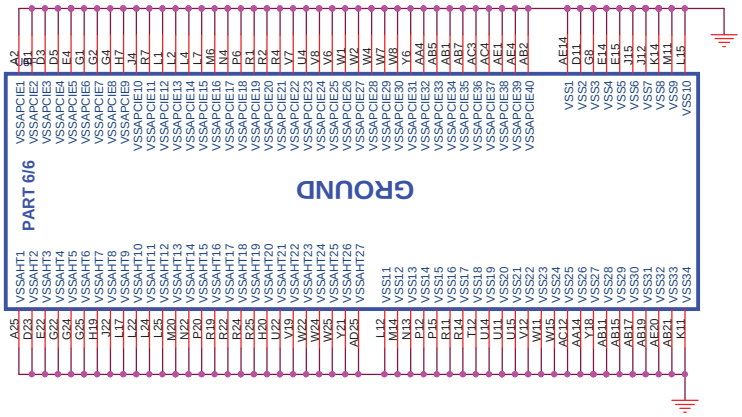


NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

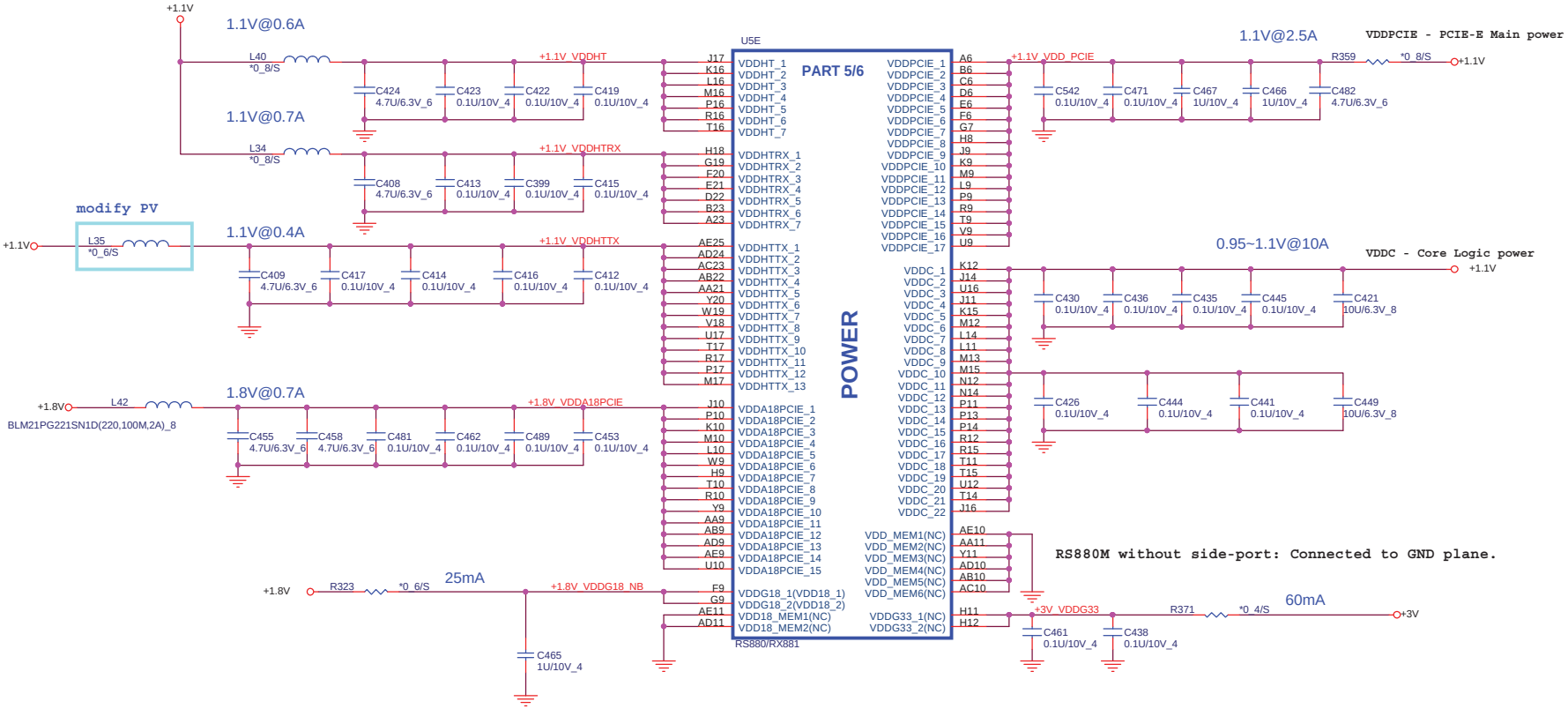
Size	Document Number	Rev
Custom	RS880M-SYSTEM I/F 3/5	3A

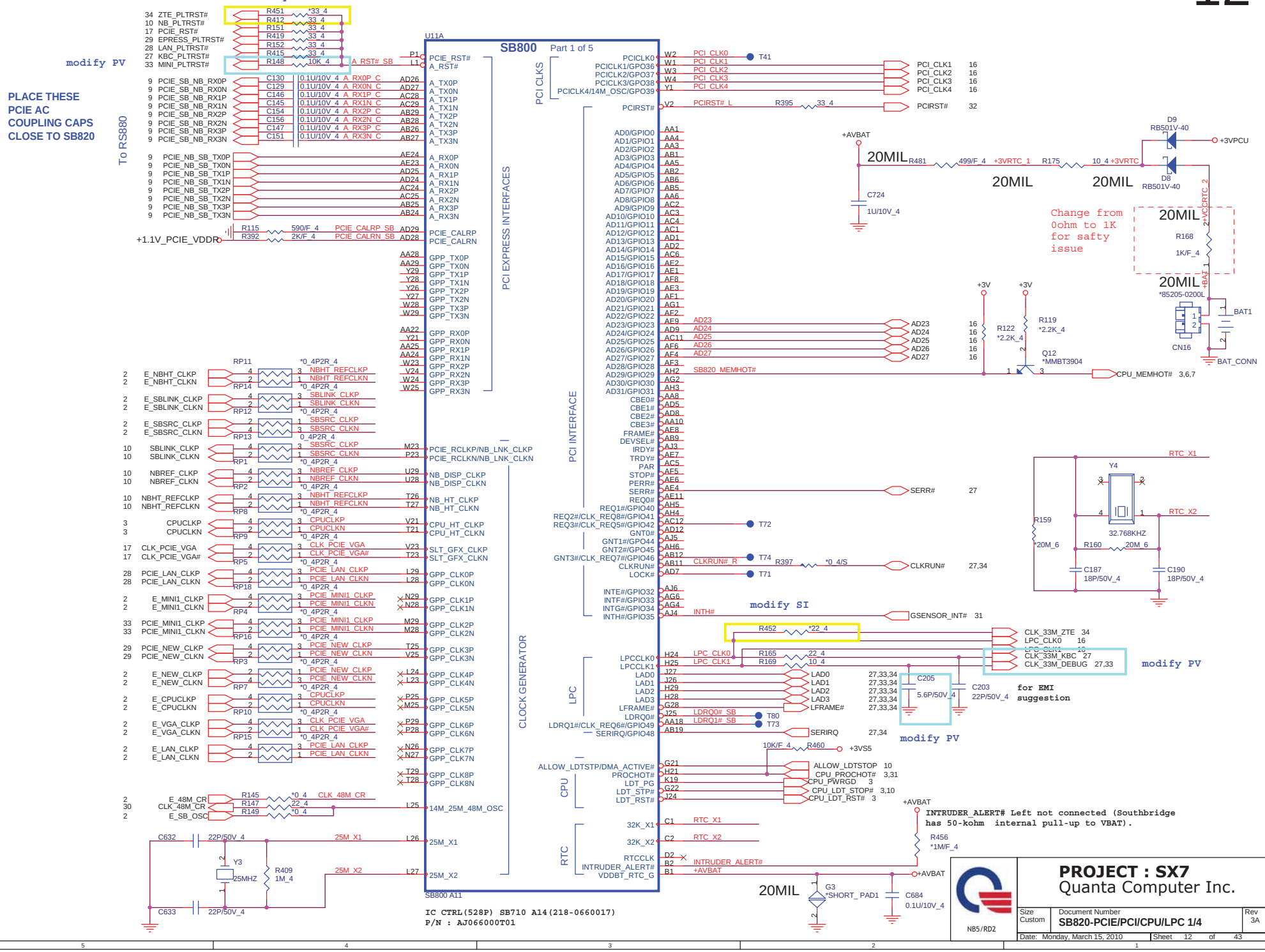
Date: Monday, March 15, 2010 Sheet 10 of 43

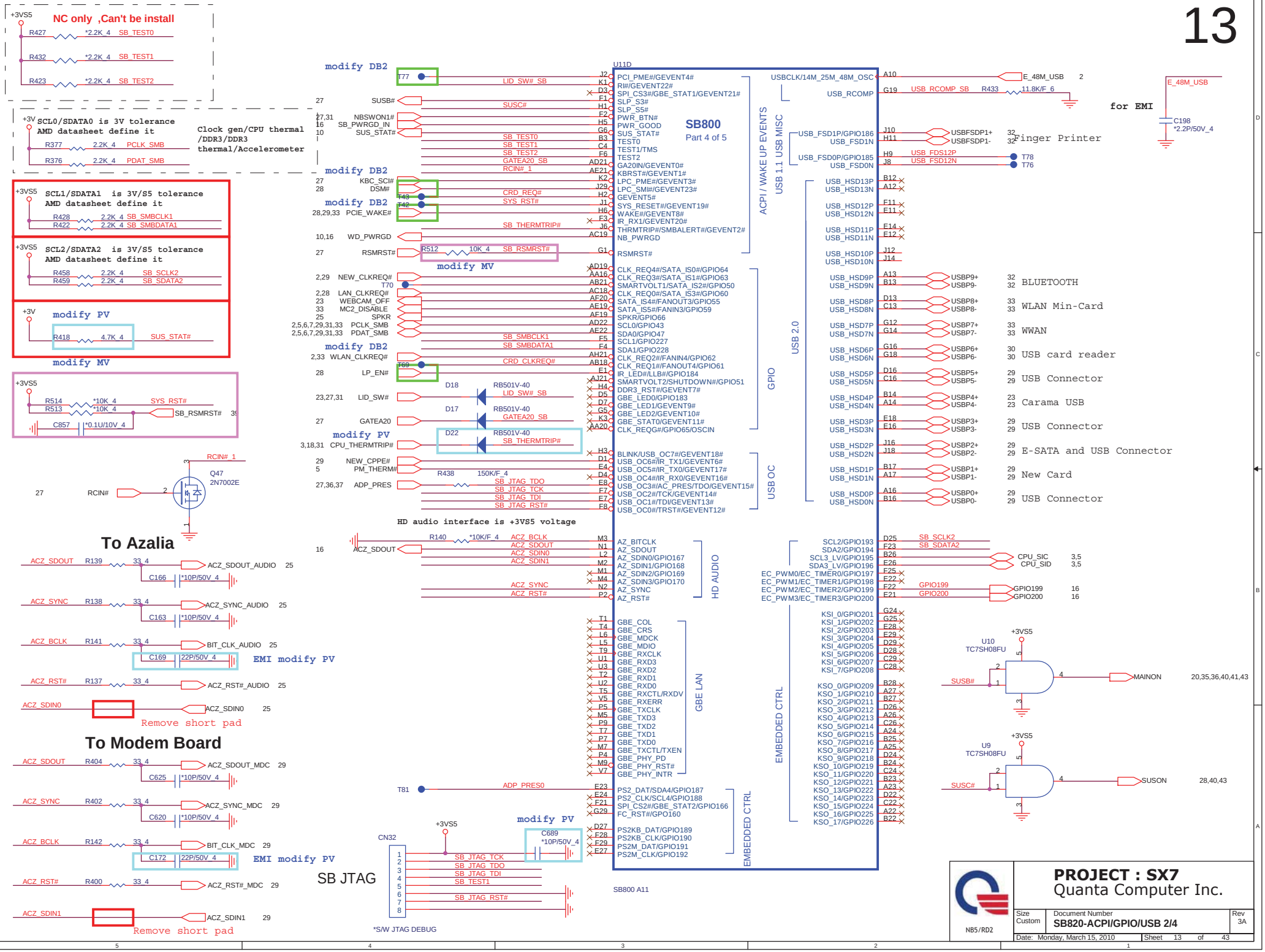


RX881/RS880 POWER DIFFERENCE TABLE

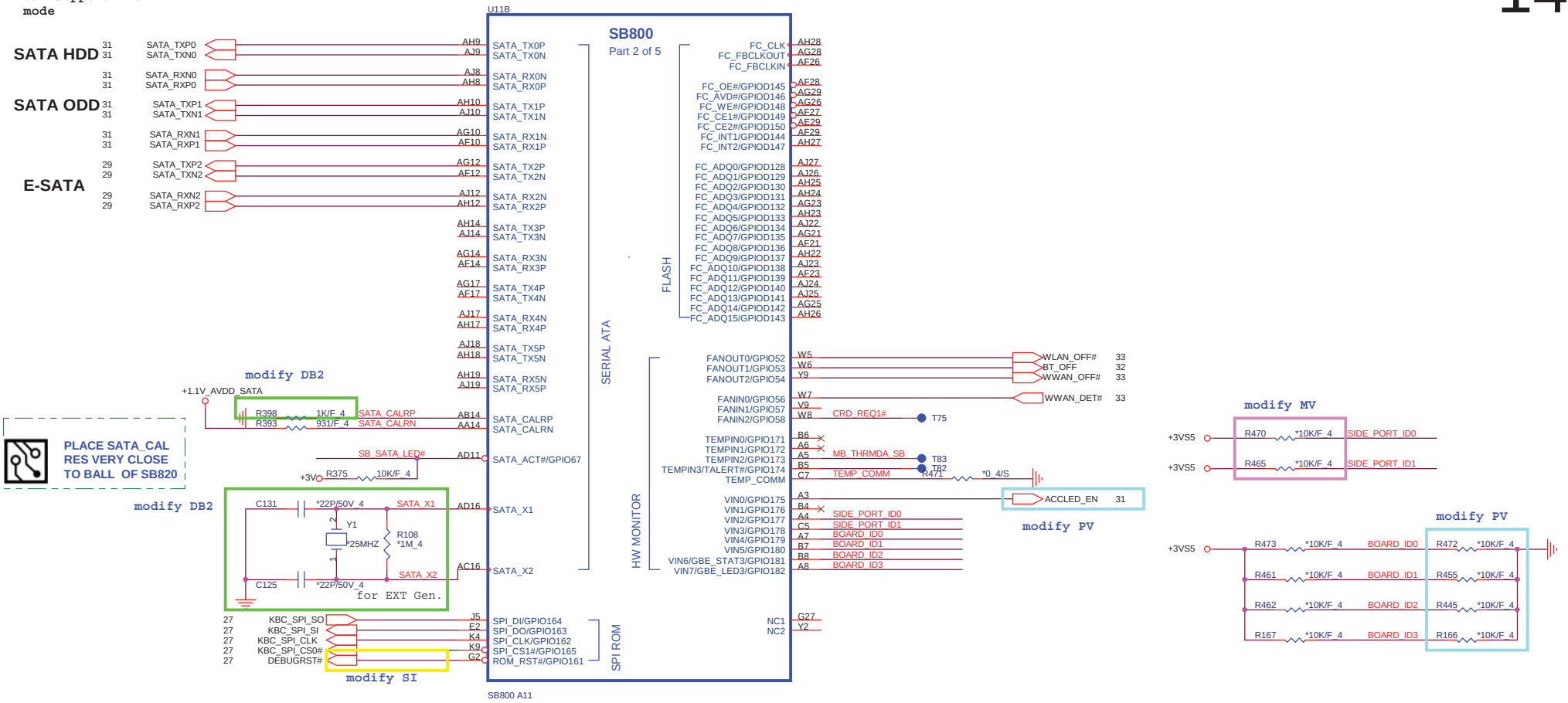
PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

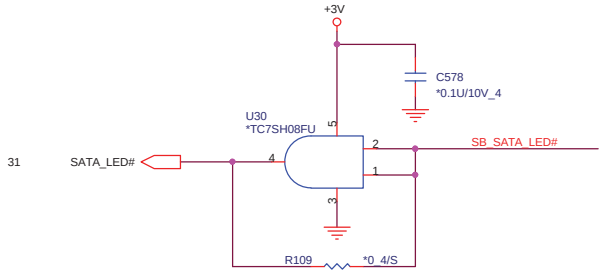



modify SI
modify PV
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820
To RS880
U11A
SB800 Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
+1.1V_PCIE_VDDR
Change from 0ohm to 1K for safty issue
20MIL
+3VPCU
+3VRTC
+VCCRTC_2
+BAT_1
BAT1
CN16
BAT_CONN
CPU_MEMHOT# 3,6,7
SERR# 27
CLKRUN# 27,34
GSENSOR_INT# 31
CLK_33M_ZTE 34
LPC_CLK0 16
CLK_33M_KBC 27
CLK_33M_DEBUG 27,33
for EMI suggestion
SERIRQ 27,34
+3VS5
ALLOW_LDTSTOP 10
CPU_PROCHOT# 3,31
CPU_PWRGD 3
CPU_LDT_STOP# 3,10
CPU_LDT_RST# 3
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
32.768KHZ
Y3 25MHZ
SB800 A11
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
NB5/RD2
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number SB820-PCIE/PCI/CPU/LPC 1/4
Rev 3A
Date: Monday, March 15, 2010
Sheet 12 of 43


NC only ,Can't be install
+3VS5
R427 *2.2K_4 SB_TEST0
R432 *2.2K_4 SB_TEST1
R423 *2.2K_4 SB_TEST2
+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R377 2.2K_4 PCLK_SMB
R376 2.2K_4 PDAT_SMB
Clock gen/CPU thermal
/DDR3/DDR3
thermal/Accelerometer
+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R428 2.2K_4 SB_SMBCLK1
R422 2.2K_4 SB_SMBDATA1
+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R458 2.2K_4 SB_SCLK2
R459 2.2K_4 SB_SDATA2
+3V modify PV
R418 4.7K_4 SUS_STAT#
modify MV
+3VS5
R514 *10K_4 SYS_RST#
R513 *10K_4
SB_RSMRST#
C857 *0.1U/10V_4
RCIN# 1
Q47
2N7002E
27 RCIN#
To Azalia
ACZ_SDOUT R139 33_4 ACZ_SDOUT_AUDIO 25
C166 *10P/50V_4
ACZ_SYNC R138 33_4 ACZ_SYNC_AUDIO 25
C163 *10P/50V_4
ACZ_BCLK R141 33_4 BIT_CLK_AUDIO 25
C169 22P/50V_4
EMI modify PV
ACZ_RST# R137 33_4 ACZ_RST#_AUDIO 25
ACZ_SDIN0 ACZ_SDIN0 25
Remove short pad
To Modem Board
ACZ_SDOUT R404 33_4 ACZ_SDOUT_MDC 29
C625 *10P/50V_4
ACZ_SYNC R402 33_4 ACZ_SYNC_MDC 29
C620 *10P/50V_4
ACZ_BCLK R142 33_4 BIT_CLK_MDC 29
C172 22P/50V_4
EMI modify PV
ACZ_RST# R400 33_4 ACZ_RST#_MDC 29
ACZ_SDIN1 ACZ_SDIN1 29
Remove short pad
modify DB2
T77 LID_SW# SB
27 SUSB#
SUSC#
27,31 NBSWON1#
16 SB_PWRGD_IN
10 SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
GATEA20_SB
RCIN# 1
modify DB2
27 KBC_SCI#
28 DSM#
T43 CRD_REQ#
T42 SYS_RST#
modify DB2
28,29,33 PCIE_WAKE#
SB_THERMTRIP#
10,16 WD_PWRGD
27 RSMRST#
R512 10K_4 SB_RSMRST#
modify MV
2,29 NEW_CLKREQ#
T70
2,28 LAN_CLKREQ#
23 WEBCAM_OFF
33 MC2_DISABLE
25 SPKR
2,5,6,7,29,31,33 PCLK_SMB
2,5,6,7,29,31,33 PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
modify DB2
2,33 WLAN_CLKREQ#
T69 CRD_CLKREQ#
28 LP_EN#
D18 RB501V-40
23,27,31 LID_SW# LID_SW# SB
D17 RB501V-40
27 GATEA20 GATEA20_SB
modify PV
D22 RB501V-40
3,18,31 CPU_THERMTRIP# SB_THERMTRIP#
29 NEW_CPPE#
5 PM_THERM#
R438 150K/F_4
27,36,37 ADP_PRES
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#
HD audio interface is +3VS5 voltage
R140 *10K/F_4
16 ACZ_SDOUT
ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0
ACZ_SDIN1
ACZ_SYNC
ACZ_RST#
T81 ADP_PRES0
CN32
+3VS5
modify PV
C689 *10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
SB JTAG
*S/W JTAG DEBUG
U11D
SB800
Part 4 of 5
PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
SB800 A11
A10 E_48M_USB 2
G19 USB_RCOMP_SB R433 11.8K/F_6
for EMI
E_48M_USB
C198 *2.2P/50V_4
J10 USBFSDP1+ 32
H11 USBFSDP1- 32
Finger Printer
H9 USB_FDS12P T78
J8 USB_FSD12N T76
B12
A12
F11
E11
E14
E12
J12
J14
A13 USBP9+ 32
B13 USBP9- 32
BLUETOOTH
D13 USBP8+ 33
C13 USBP8- 33
WLAN Min-Card
G12 USBP7+ 33
G14 USBP7- 33
WWAN
G16 USBP6+ 30
G18 USBP6- 30
USB card reader
D16 USBP5+ 29
C16 USBP5- 29
USB Connector
B14 USBP4+ 23
A14 USBP4- 23
Carama USB
E18 USBP3+ 29
E16 USBP3- 29
USB Connector
J16 USBP2+ 29
J18 USBP2- 29
E-SATA and USB Connector
B17 USBP1+ 29
A17 USBP1- 29
New Card
A16 USBP0+ 29
B16 USBP0- 29
USB Connector
D25 SB_SCLK2
F23 SB_SDATA2
B26 CPU_SIC 3,5
F26 CPU_SID 3,5
F25
F22
F22 GPIO199 GPIO199 16
F21 GPIO200 GPIO200 16
G24
G25
E28
E29
D29
D28
C29
C28
B28
A27
B27
D26
A26
C26
A24
B25
A25
D24
B24
C24
B23
A23
D22
C22
A22
B22
U10
TC7SH08FU
+3VS5
SUSB#
MAINON 20,35,36,40,41,43
U9
TC7SH08FU
+3VS5
SUSC#
SUSON 28,40,43
NB5/RD2
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
SB820-ACPI/GPIO/USB 2/4
Rev 3A
Date: Monday, March 15, 2010
Sheet 13 of 43

SATA PORT 0,1,2,3
can support AHCI
mode





ID3	ID2	ID1	ID0	
0	0	0	0	SX7 UMA
0	0	0	1	SX7 UMA
0	0	1	0	SX7 Dis
0	0	1	1	SX7 Dis
0	1	0	0	SX7 UMA DF
0	1	0	1	SX7 UMA DF
0	1	1	0	SX7 Dis DF
0	1	1	1	SX7 Dis DF

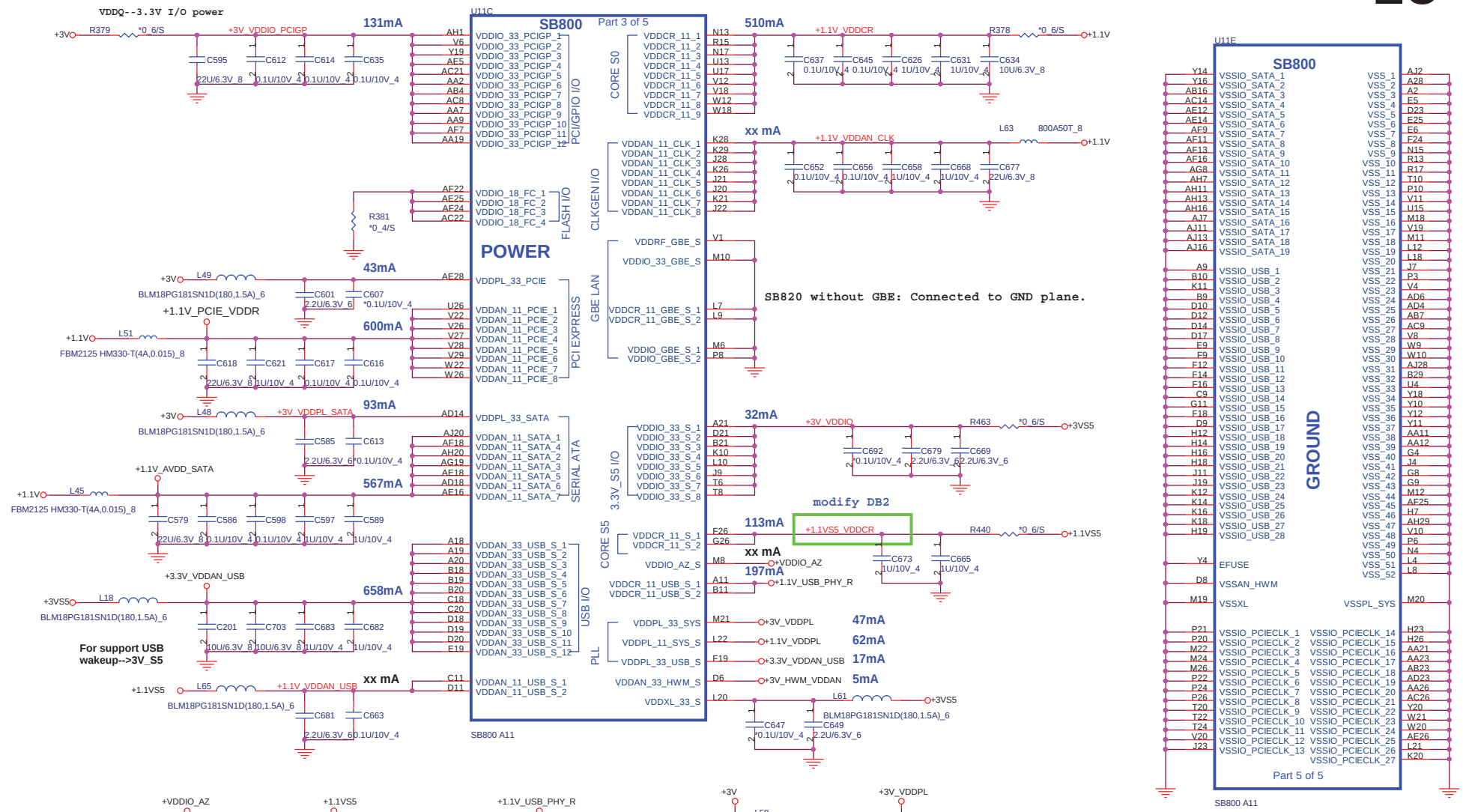
PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	3A

Date: Monday, March 15, 2010 Sheet 14 of 43

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



NB5/RD2

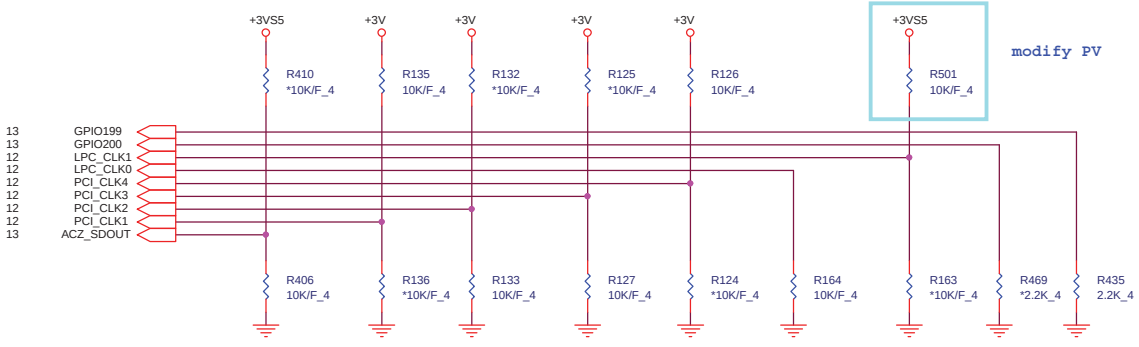
PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PWR/DECOUPLING 4/4	3A

Date: Monday, March 15, 2010 | Sheet 15 of 43

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



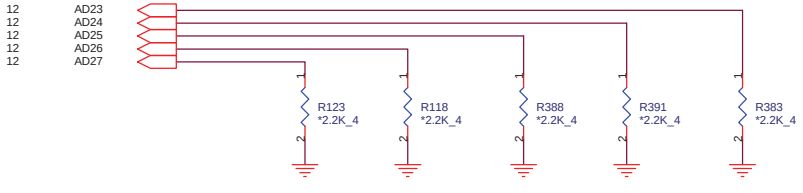
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM

modify DB2

internal have pull Hi 10K

DEBUG STRAPS

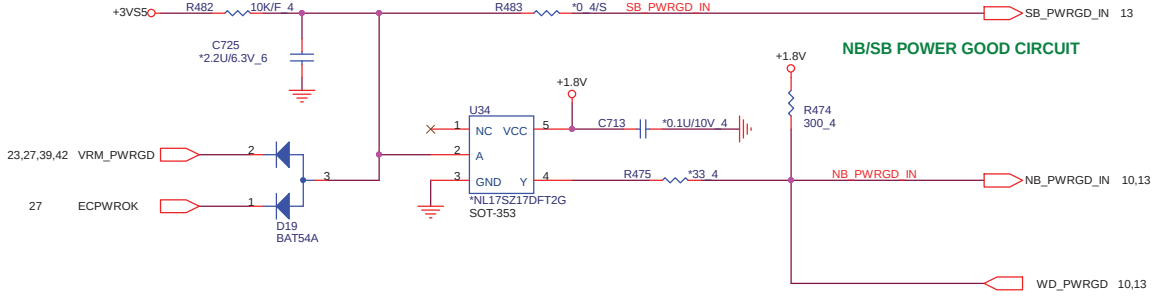
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

NB/SB POWER GOOD CIRCUIT



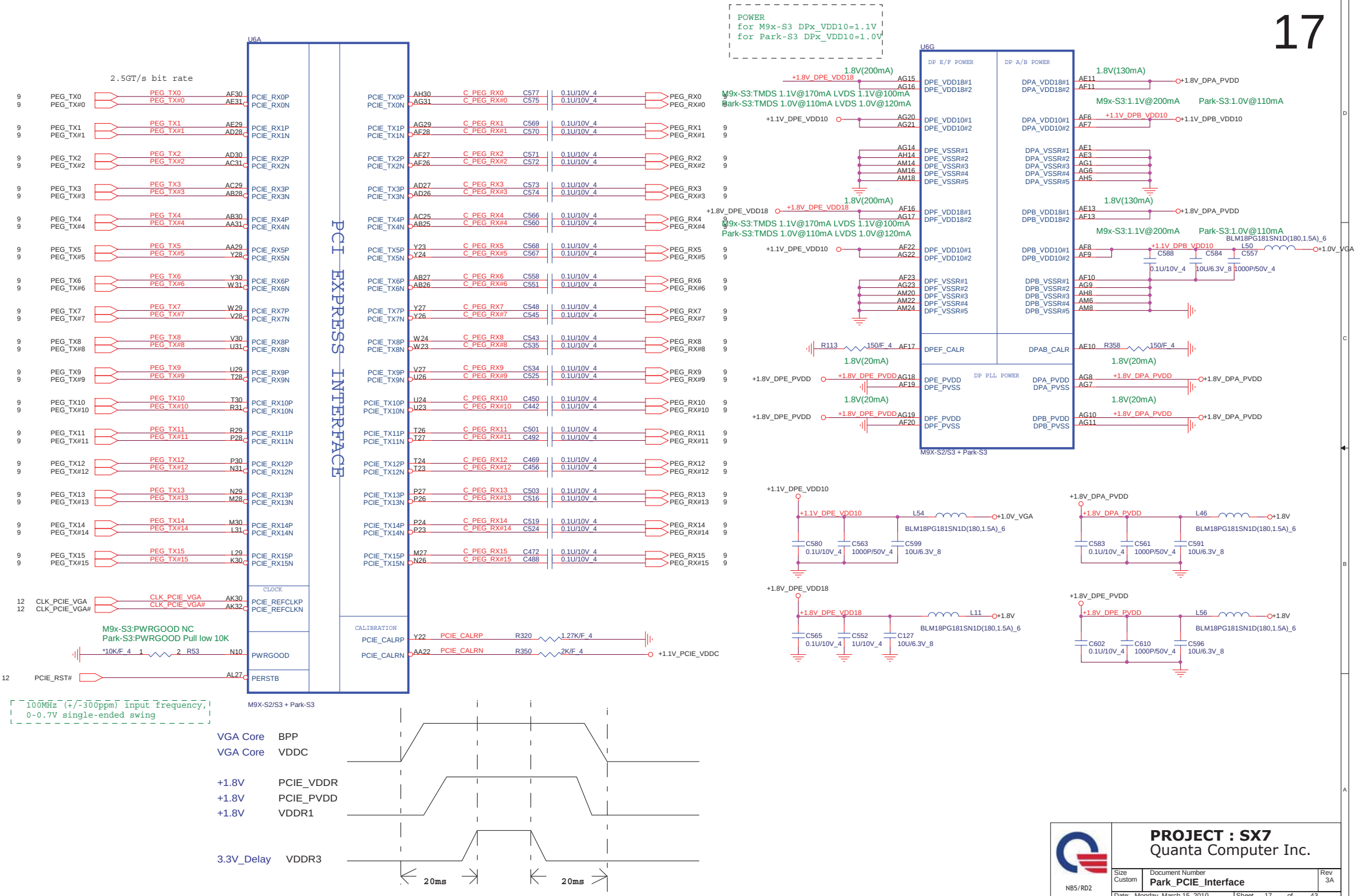
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	3A

Date: Monday, March 15, 2010 Sheet 16 of 43



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_PCIE_Interface	3A

NB5/RD2

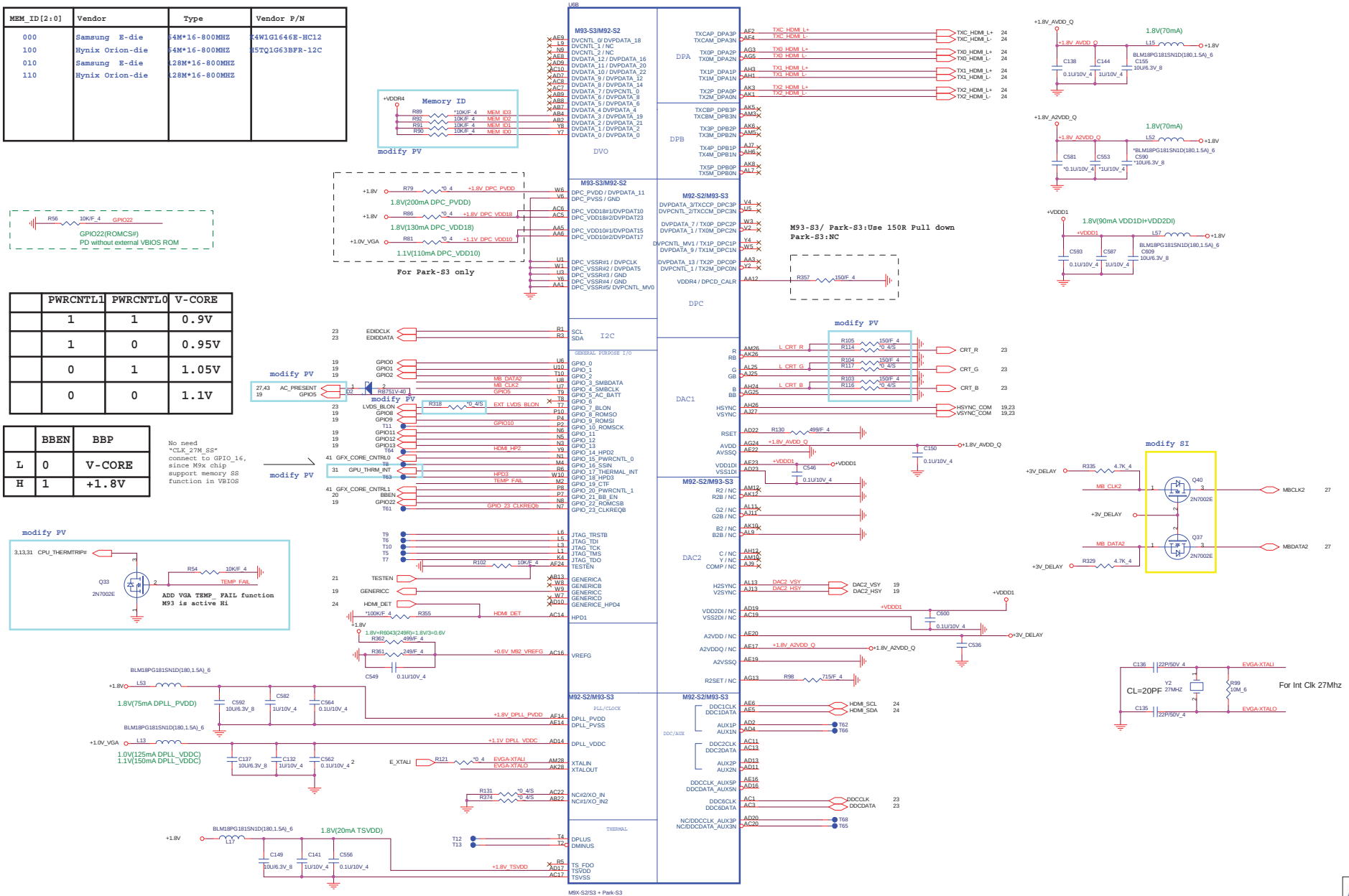
Date: Monday, March 15, 2010 Sheet 17 of 43

MEM_ID[2:0]	Vendor	Type	Vendor P/N
000	Samsung E-die	64M*16-800MHZ	K4W1G1646E-HC12
100	Hynix Orion-die	64M*16-800MHZ	H5TQ1G63BFR-12C
010	Samsung E-die	128M*16-800MHZ	
110	Hynix Orion-die	128M*16-800MHZ	

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

No need "CLK_27M_SS" connect to GPIO_16, since M9x chip support memory SS function in VBIOS

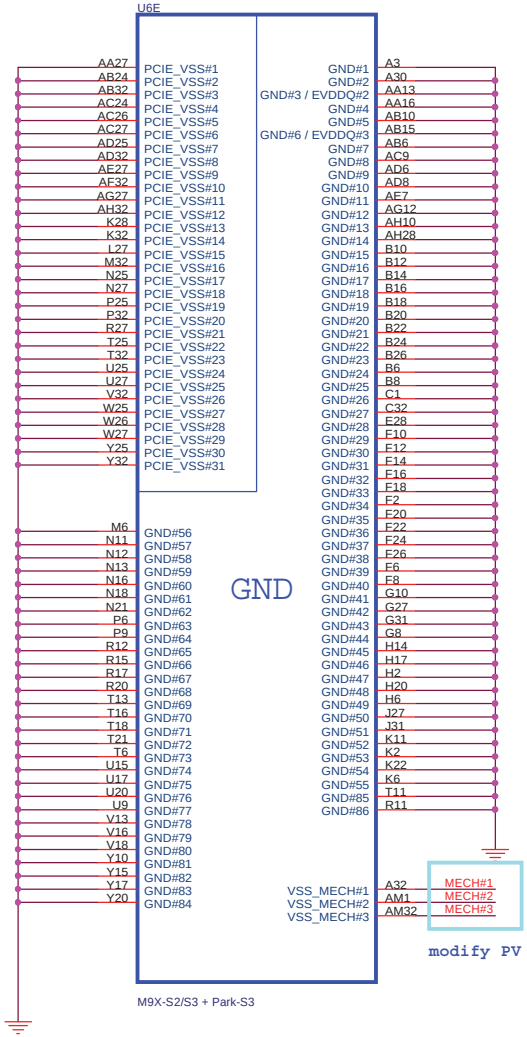


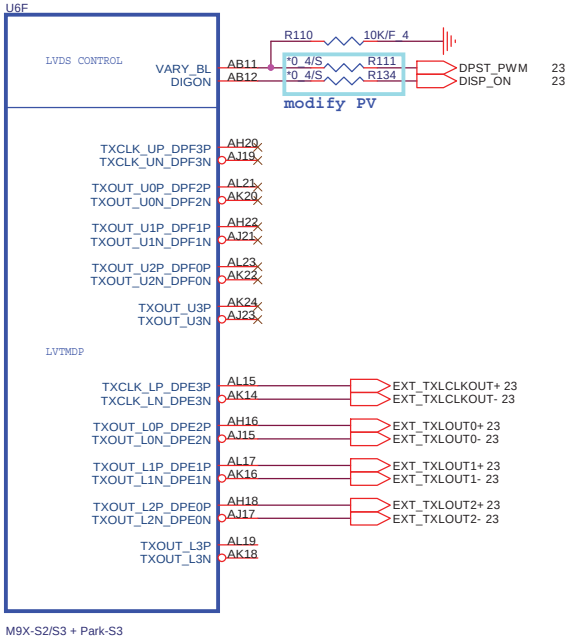
PROJECT : SX7
Quanta Computer Inc.

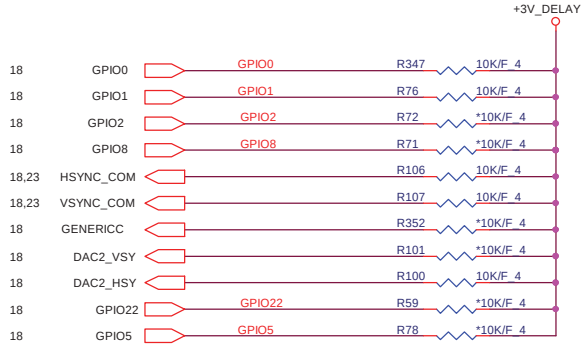
Size	Document Number	Rev
Custom	Park_Main	3A

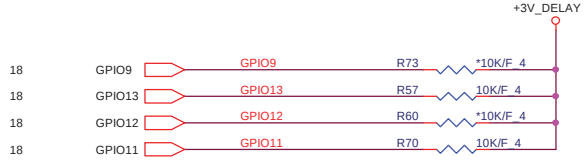
Date: Monday, March 15, 2010 Sheet 18 of 43

N85/RD2

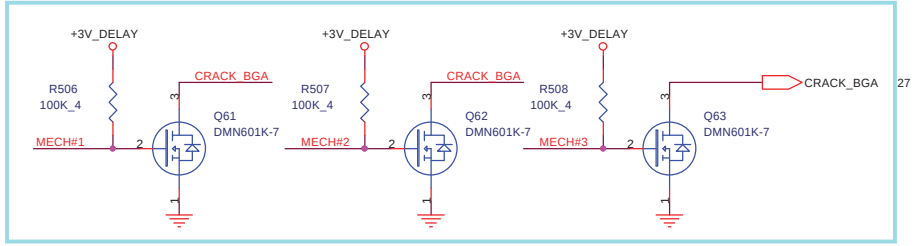








modify PV



Pin Straps description

Strap Name			Default Value
TX_PWRS_ENB	GPIO0	**PCI Express Full TX Output Swing** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	**Enable CLKREQ# Power Management** 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	**AUD[1] AUD[0]** 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

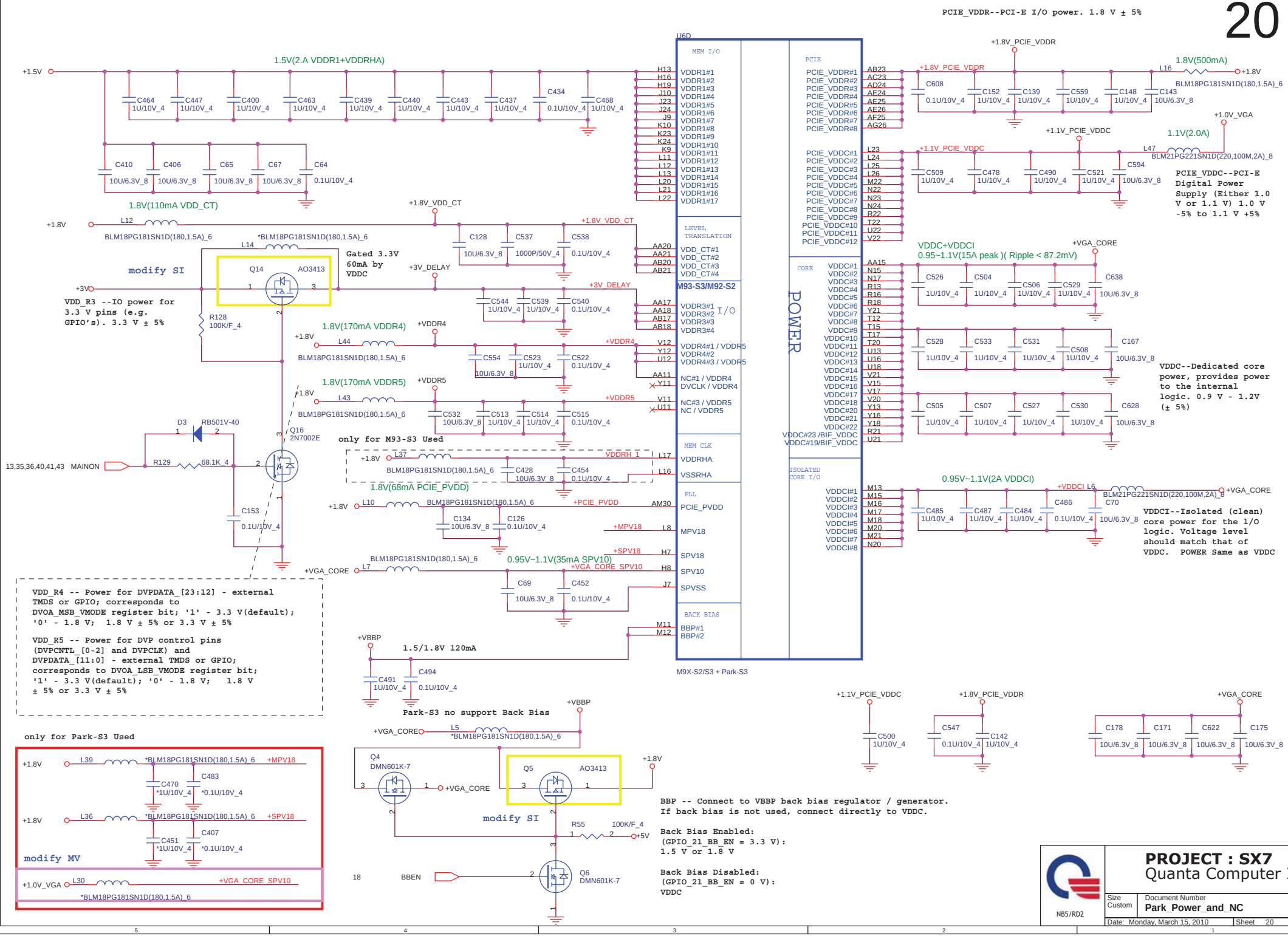
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_GND / LVDS/ Straps	3A

Date: Monday, March 15, 2010 Sheet 19 of 43

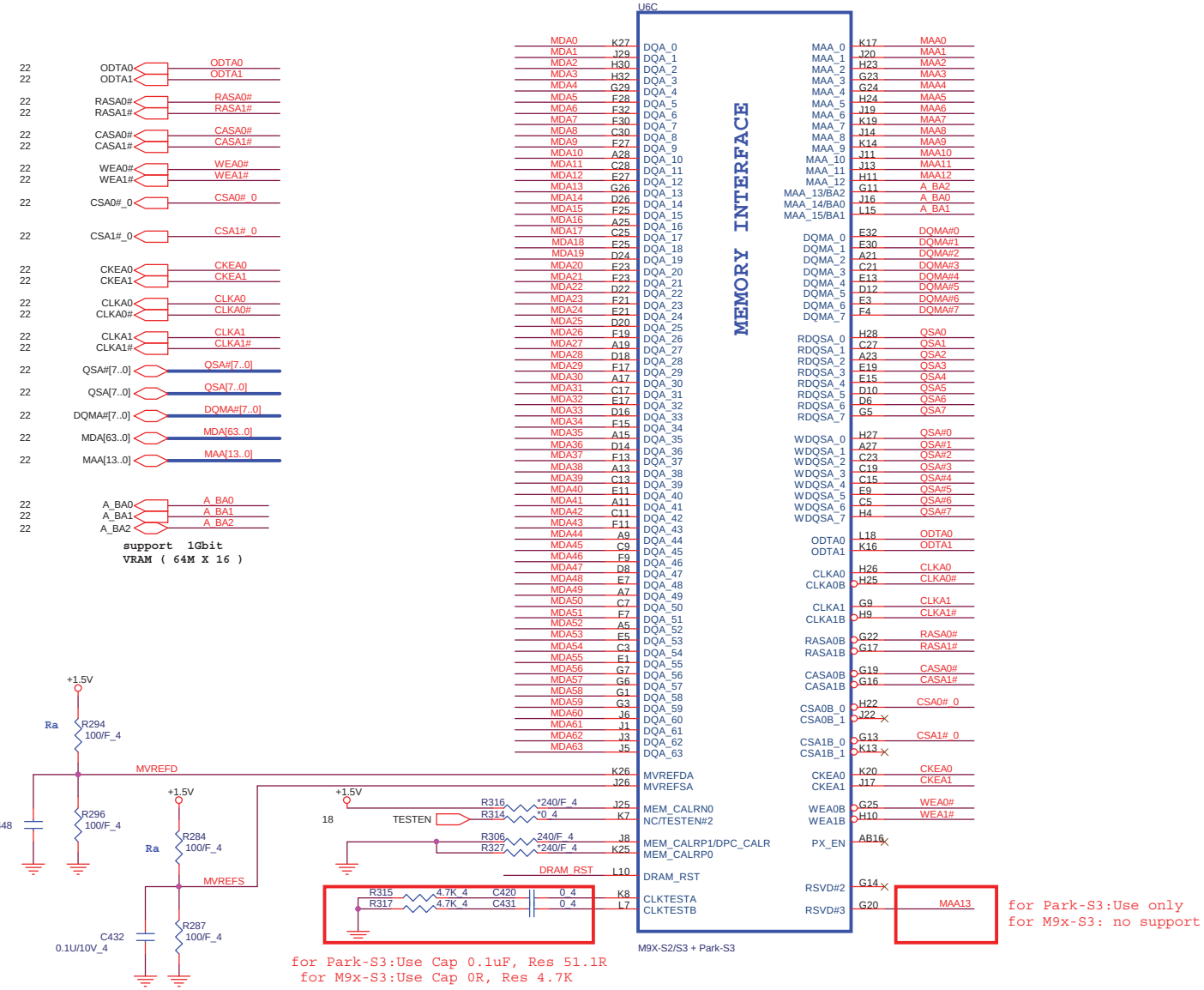


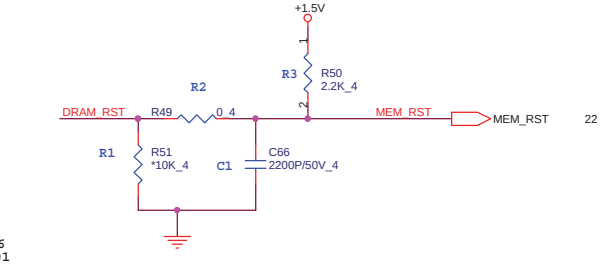
PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_Power_and_NC	3A

Date: Monday, March 15, 2010 Sheet 20 of 43

NB5/RD2





	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01

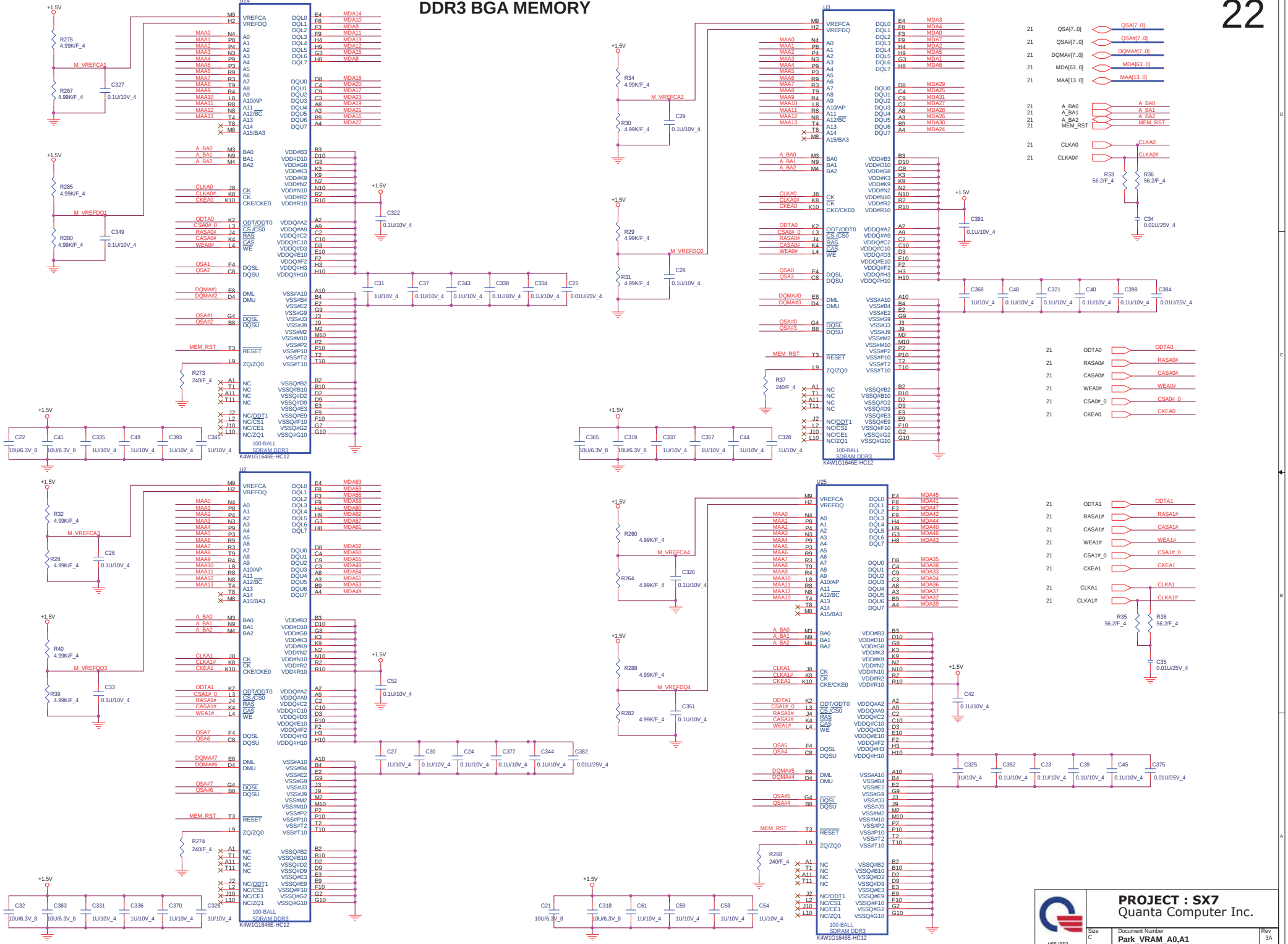
NB5/RD2

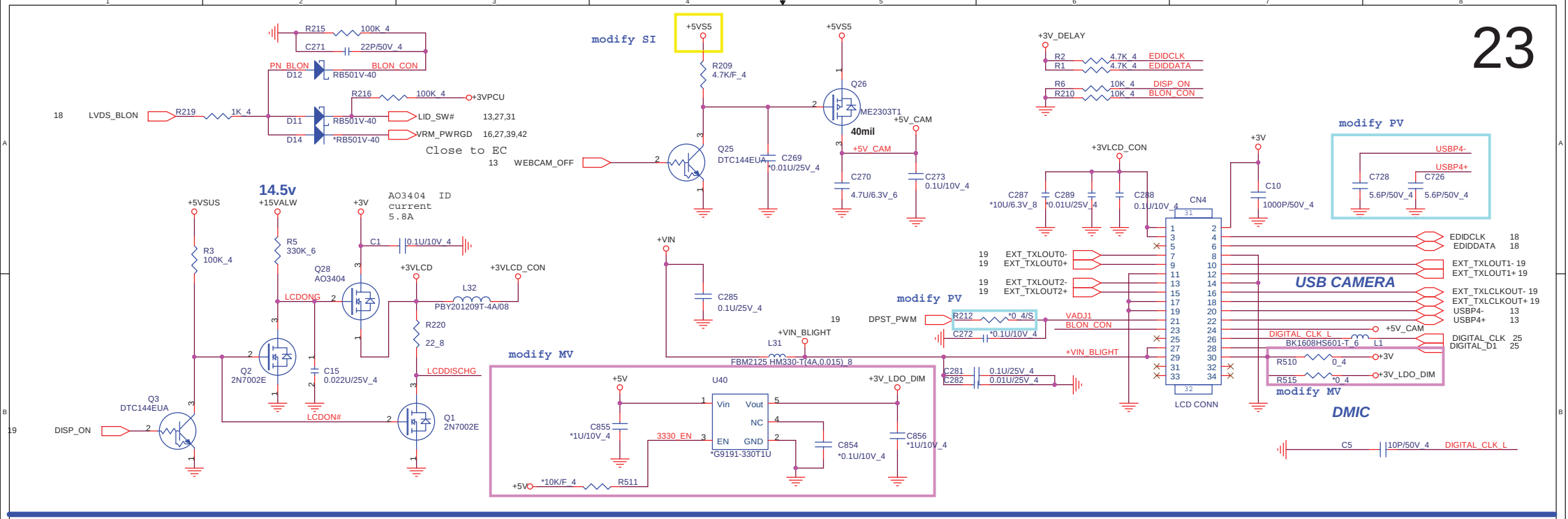
PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_MEM_Interface	3A

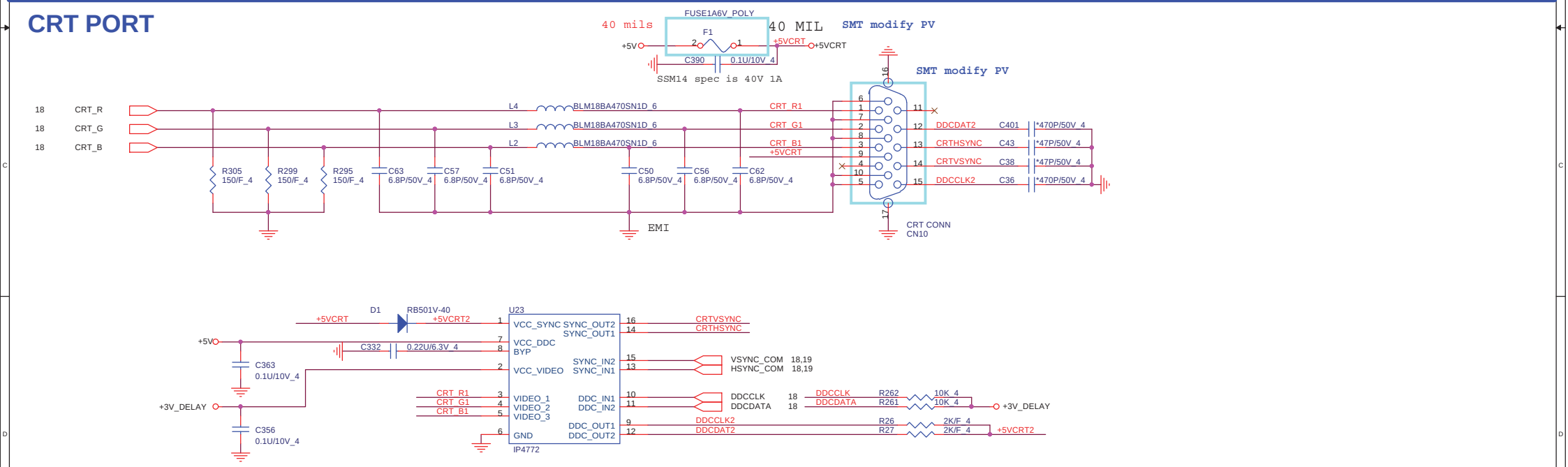
Date: Monday, March 15, 2010 Sheet 21 of 43

DDR3 BGA MEMORY





CRT PORT



2,3,5,6,7,10,11,12,13,14,15,16,20,25,27,28,29,30,31,32,33,34,35,37,43 +3V
12,27,31,32,33,36,37,38 +3VPCU
20,24,25,31,32,33,37,43 +5V
29,43 +5VSUS
38,43 +15VALW
36,38,39,40,41,42,43 +VIN

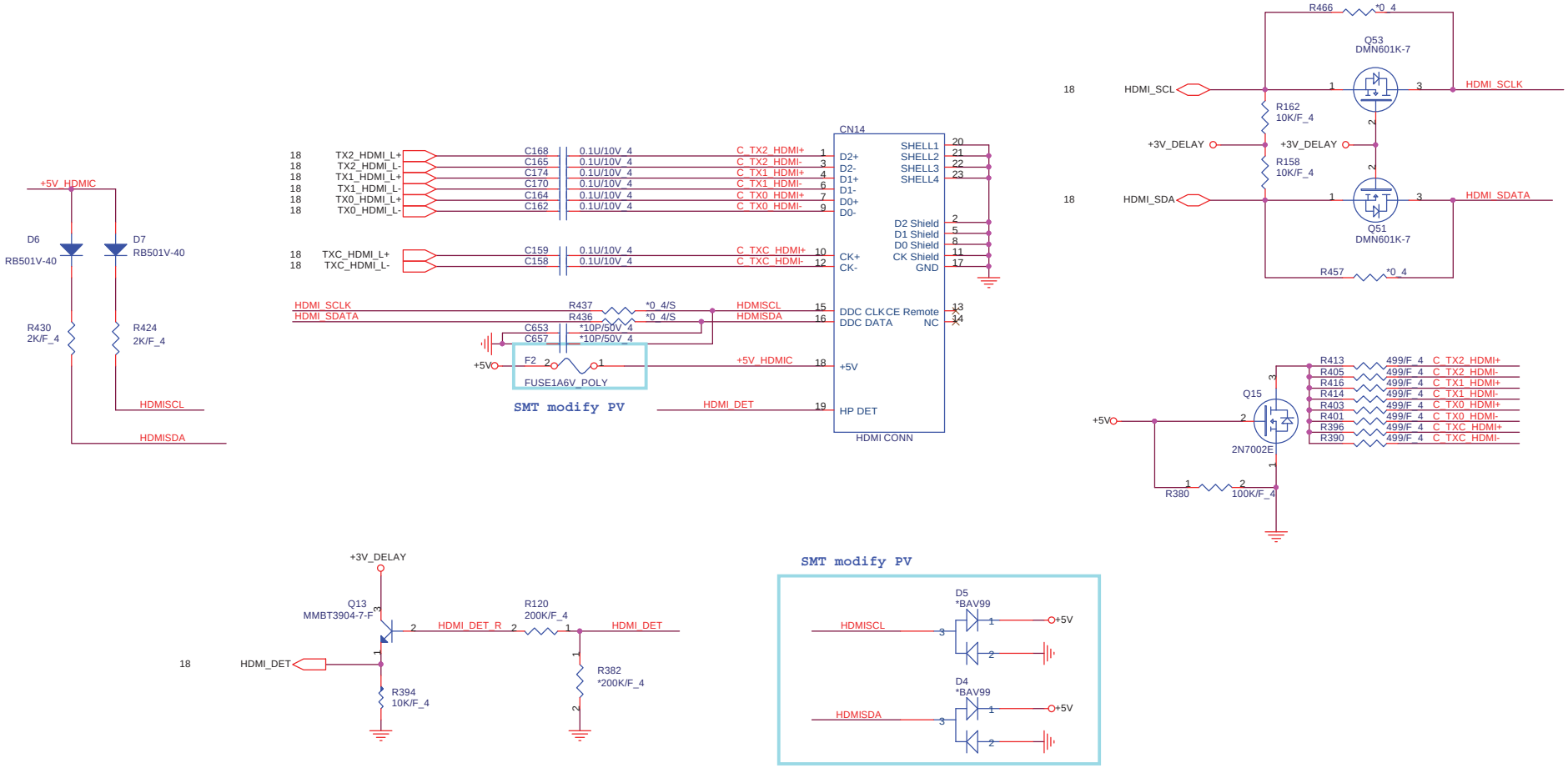
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	3A

Date: Monday, March 15, 2010 Sheet 23 of 43

HDMI PORT



20,23,25,31,32,33,37,43 +5V

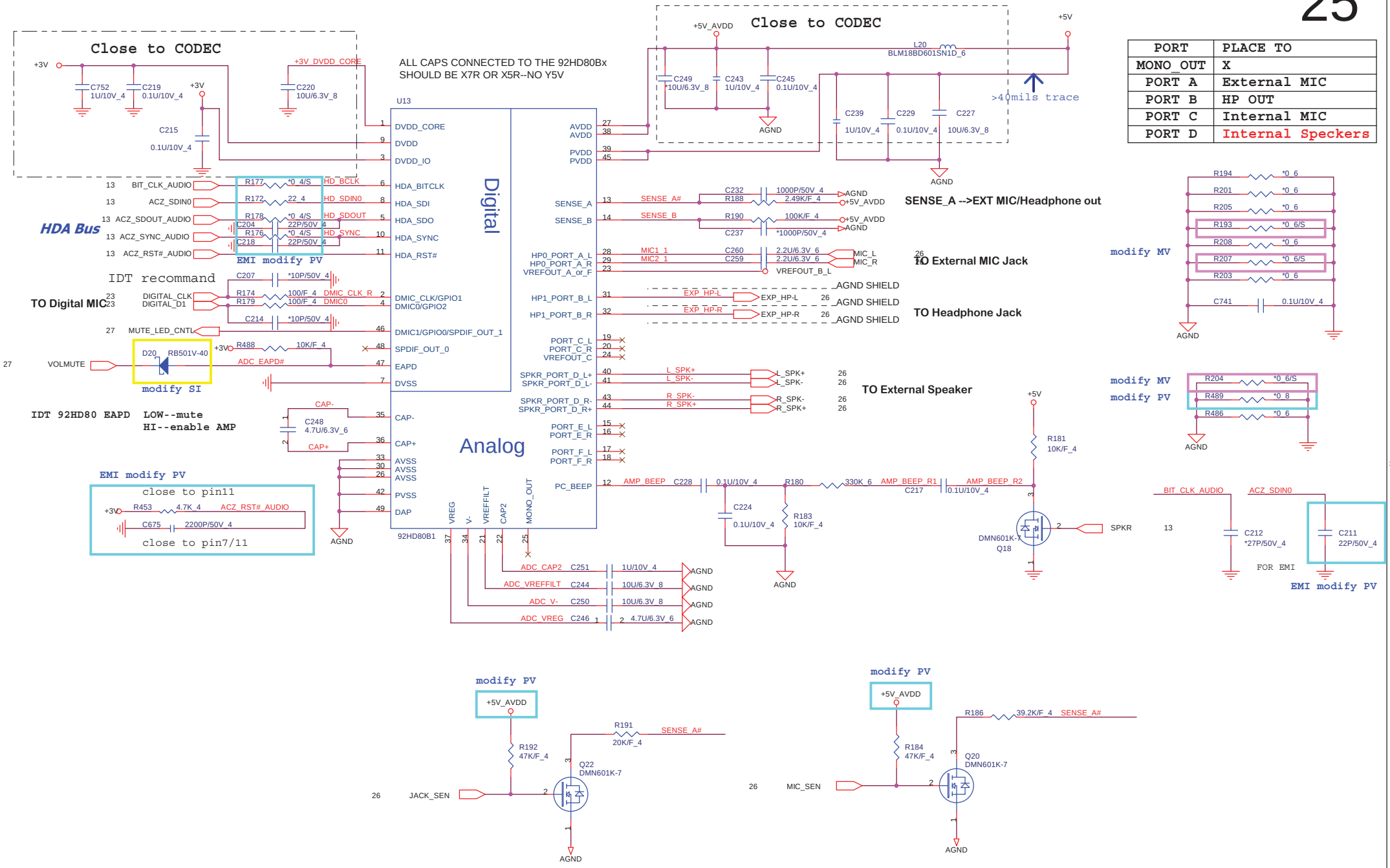
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**HDMI Conn**	3A

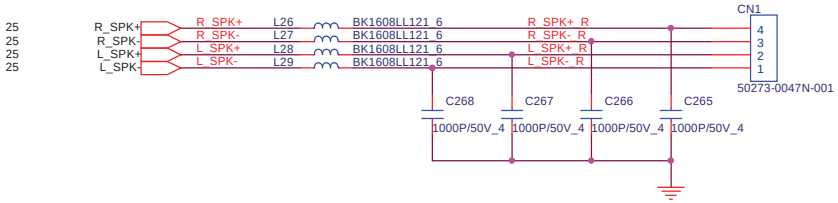
Date: Monday, March 15, 2010 Sheet 24 of 43

PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers



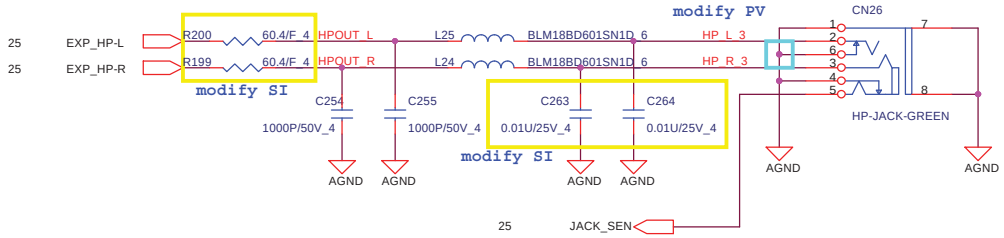
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

INT. SPEAKER



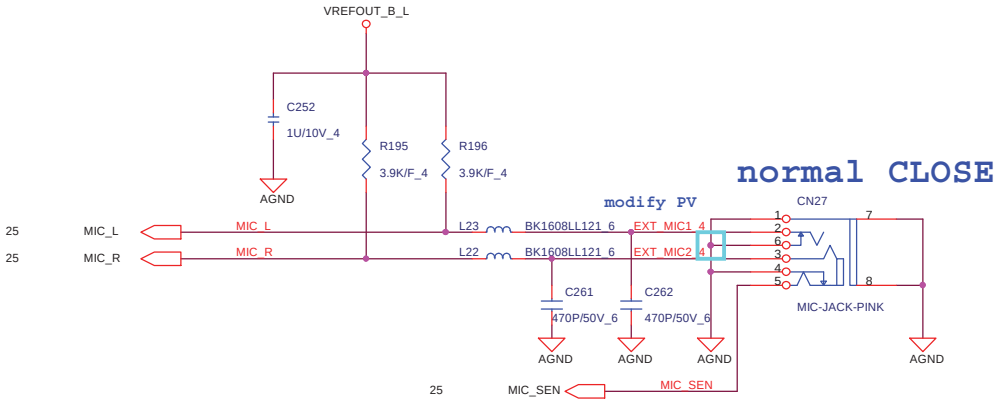
Headphone Jack

normal CLOSE



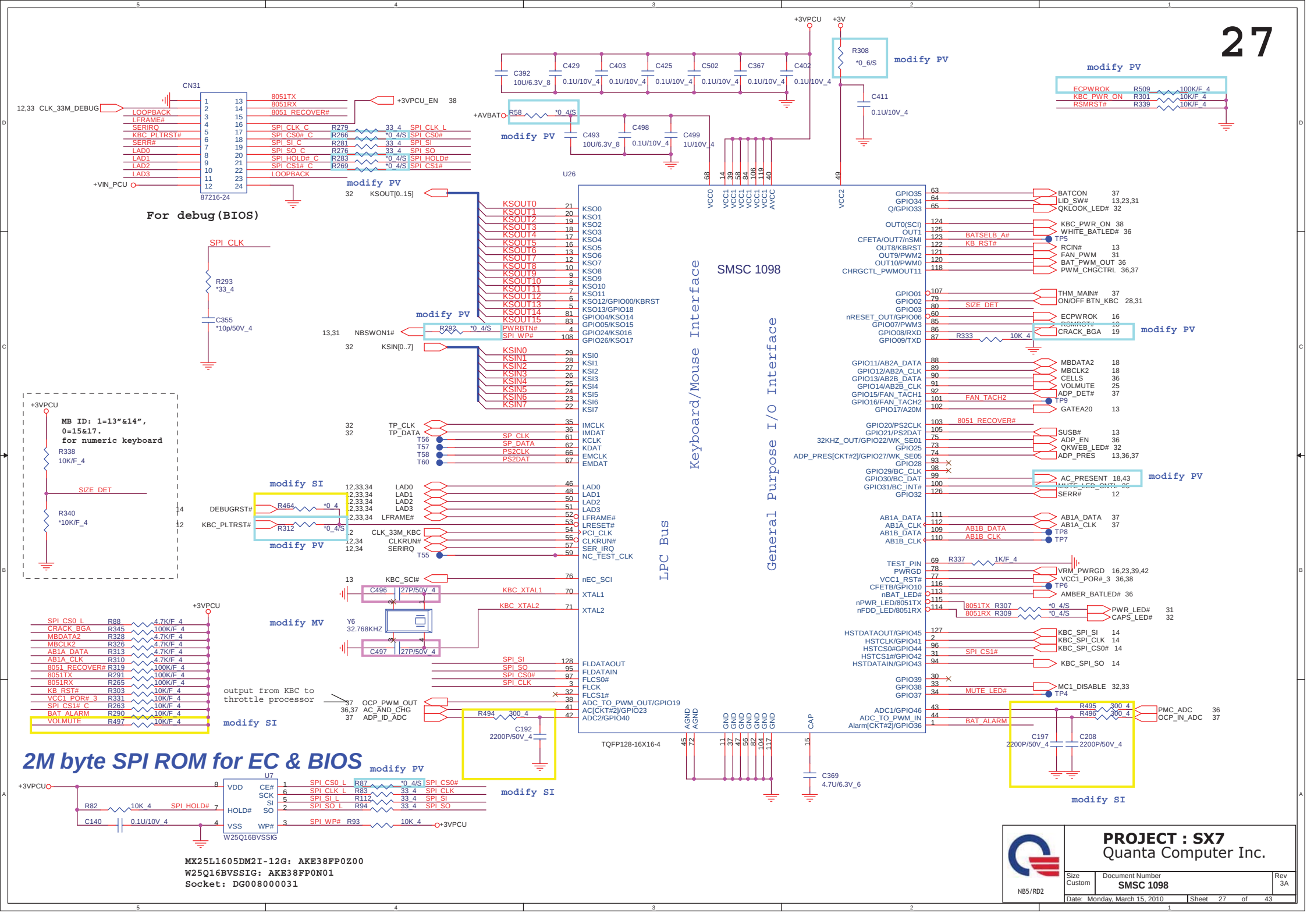
EXT Mic Jack

normal CLOSE

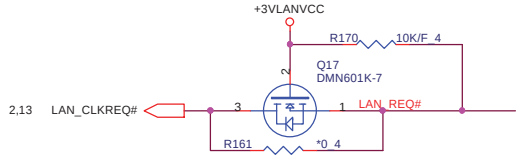


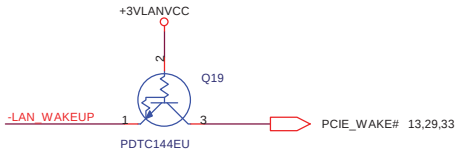
Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.		
Size Custom	Document Number **HP/MIC/SPK**		Rev 3A
	Date: Monday, March 15, 2010	Sheet 26 of 43	

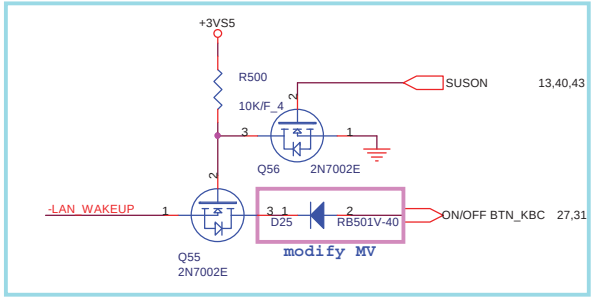

SMSC 1098
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
TQFP128-16X16-4
U26
CN31
87216-24
For debug(BIOS)
modify PV
modify SI
modify MV
2M byte SPI ROM for EC & BIOS
U7
W25Q16BVSSIG
MX25L1605DM2I-12G: AKE38FP0Z00
W25Q16BVSSIG: AKE38FP0N01
Socket: DG008000031
MB ID: 1=13"&14",
0=15&17.
for numeric keyboard
output from KBC to
throttle processor
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
SMSC 1098
Rev 3A
Date: Monday, March 15, 2010
Sheet 27 of 43
NB5/RD2

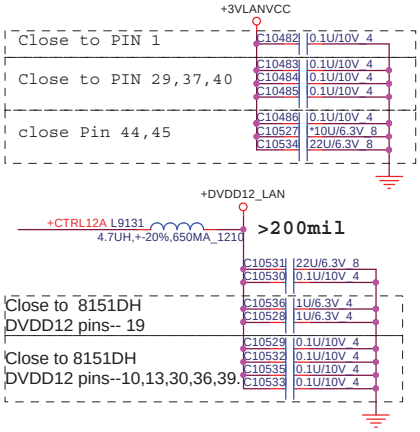
modify DB2

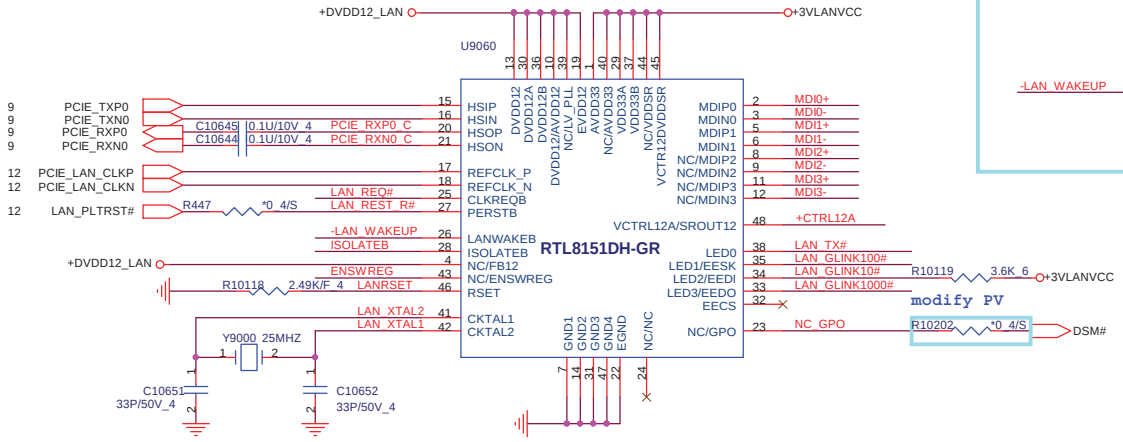




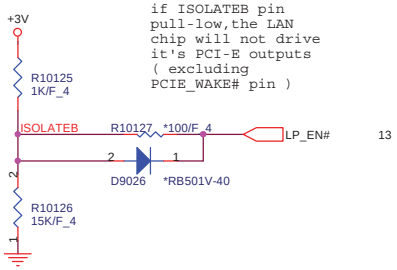
modify PV





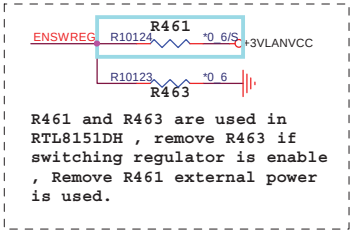


RTL8151DH-GR



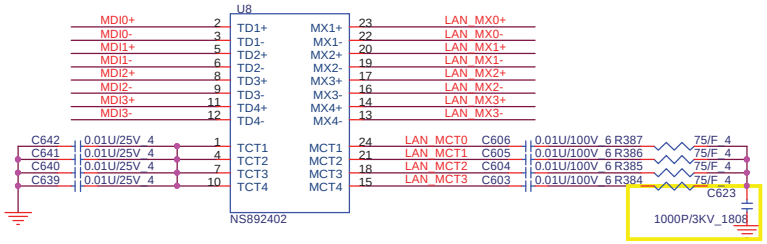
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

modify PV



R461 and R463 are used in RTL8151DH , remove R463 if switching regulator is enable , Remove R461 external power is used.

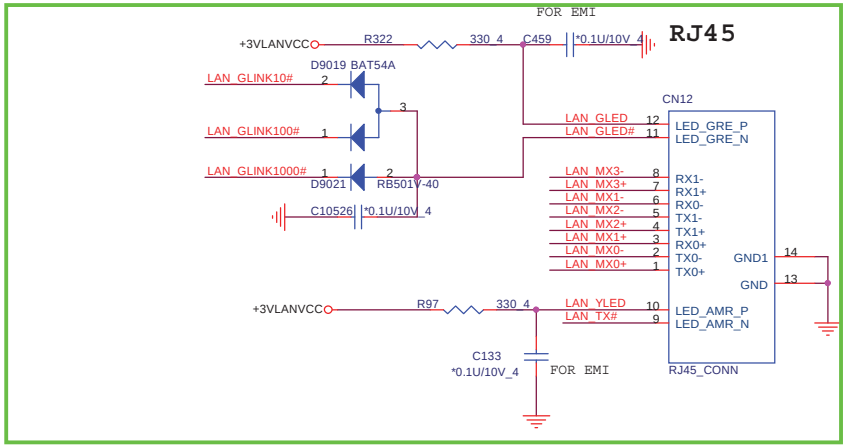
Transformer for 10/100/1000



modify SI

Lan Con.

modify DB2



43 +3VLANVCC
2,3,5,6,7,10,11,12,13,14,15,16,20,23,25,27,29,30,31,32,33,34,35,37,43 +3V

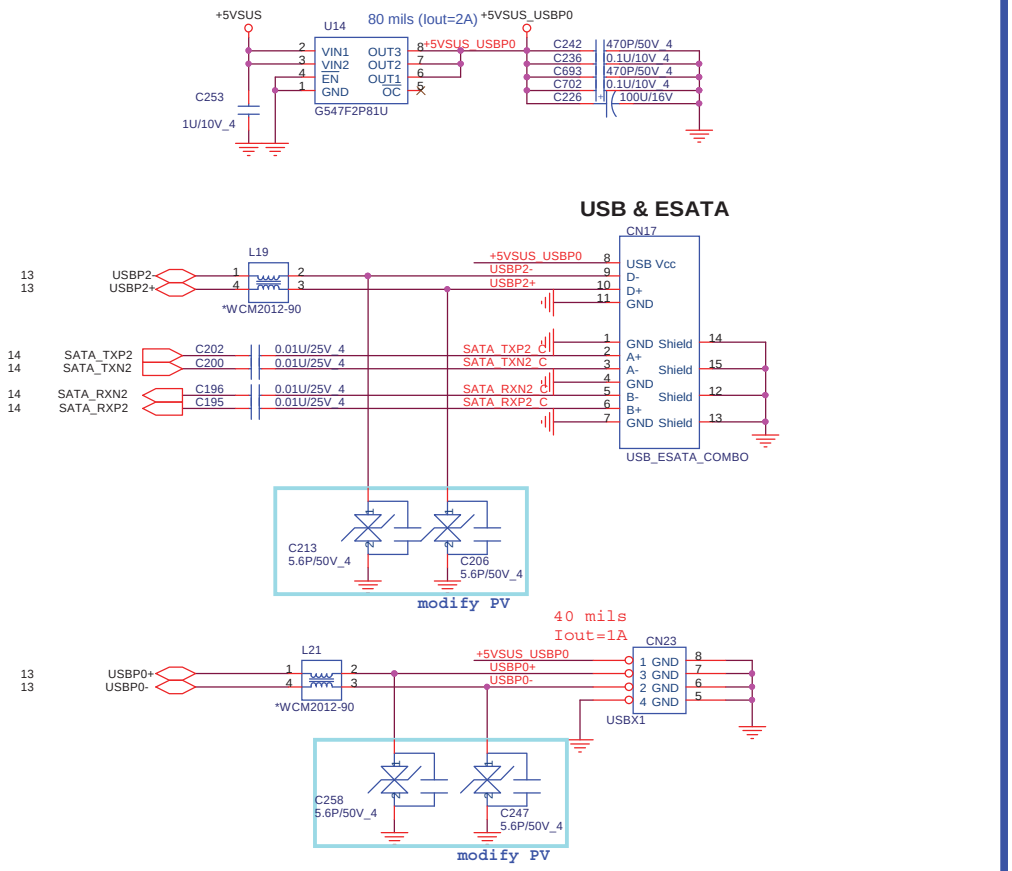
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

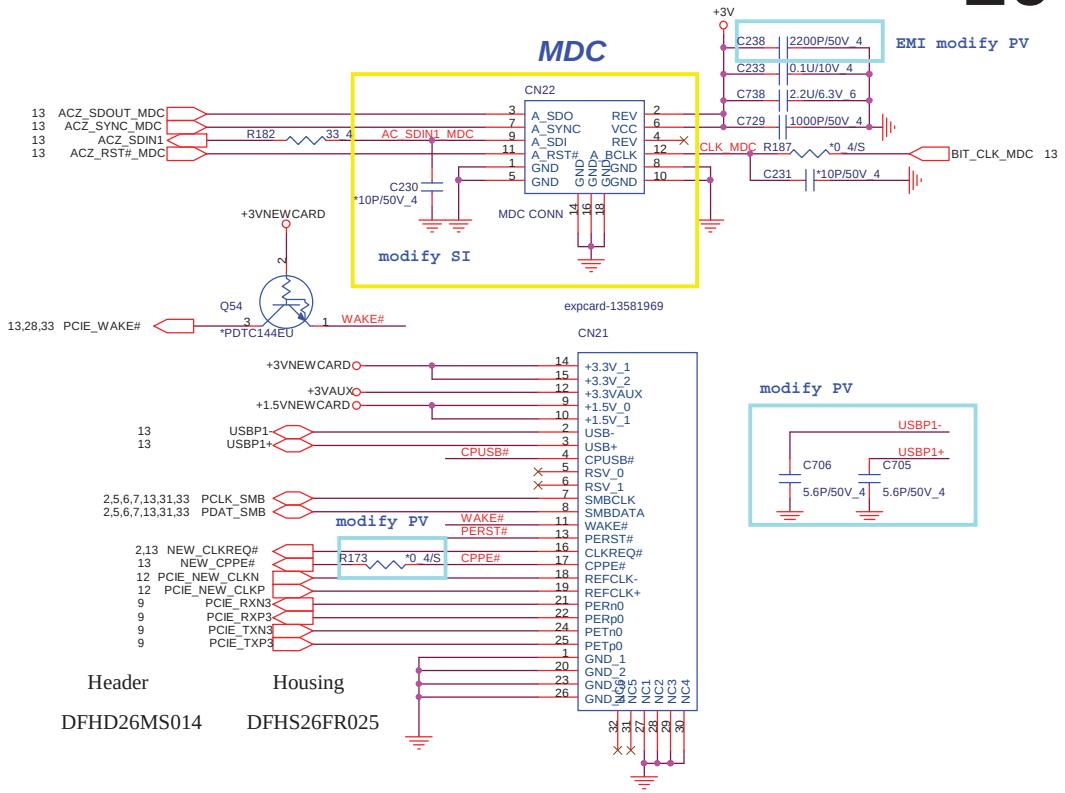
Size	Document Number	Rev
Custom	LAN RTL8151/RJ45	3A

Date: Monday, March 15, 2010 Sheet 28 of 43

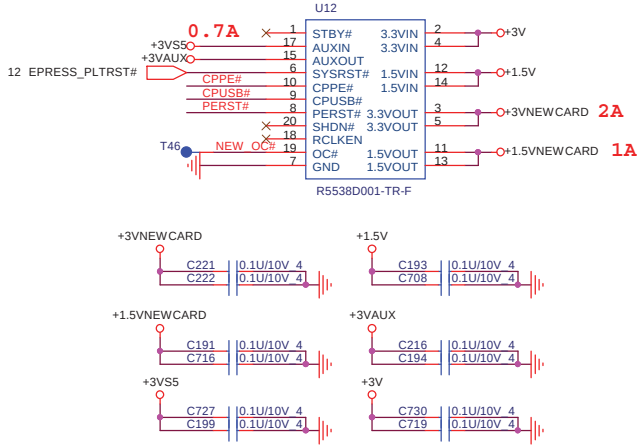
LEFT SIDE USBX1 and E-SATA/USB COMBO



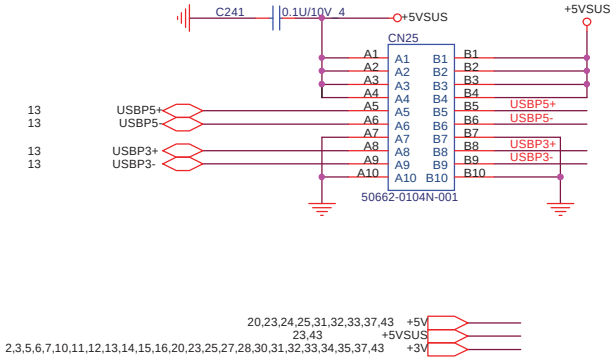
Modem CONN



NEWCARD (PCIEXPRESS*1 + USB*1)



RIGHT SIDE USBX2

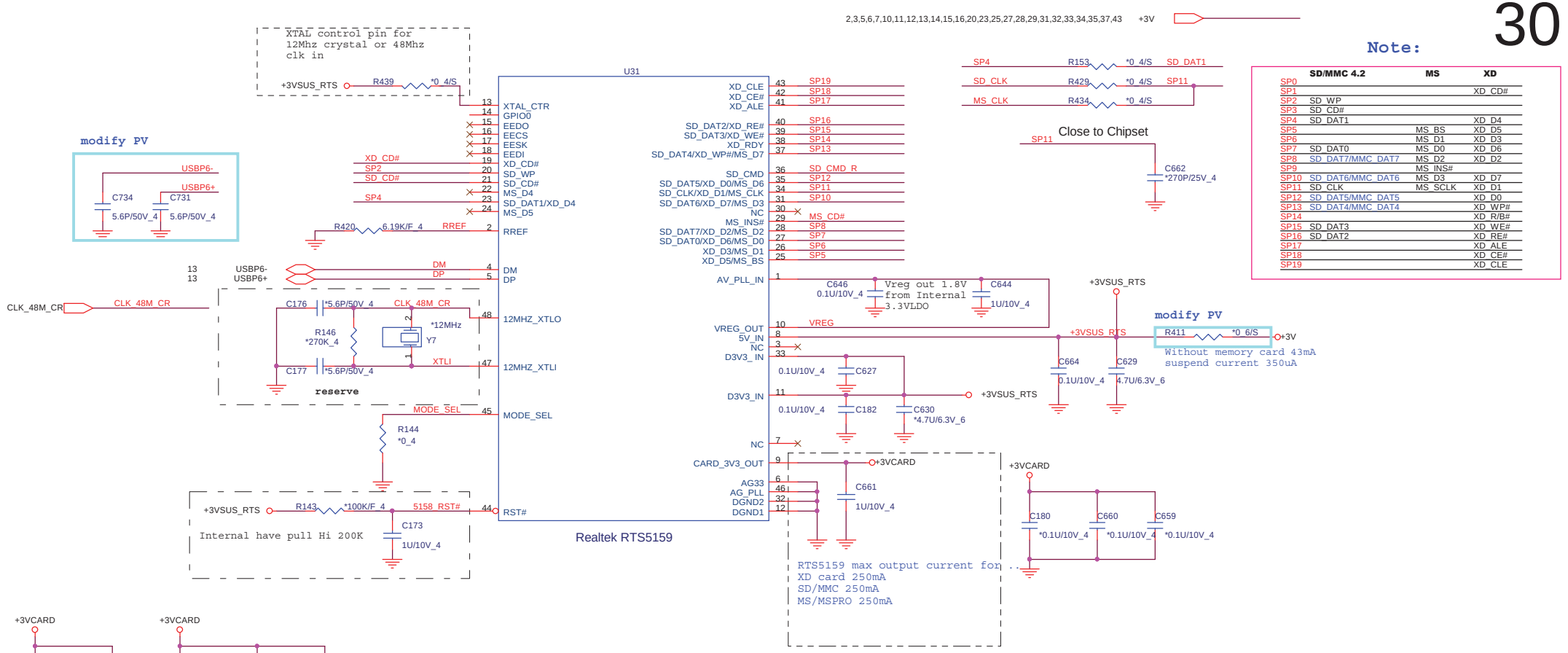


NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXTERNAL USB X2	3A

Date: Monday, March 15, 2010 Sheet 29 of 43



Note:

	SD/MMC 4.2	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7/MMC_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6/MMC_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5/MMC_DAT5		XD_D0
SP13	SD_DAT4/MMC_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

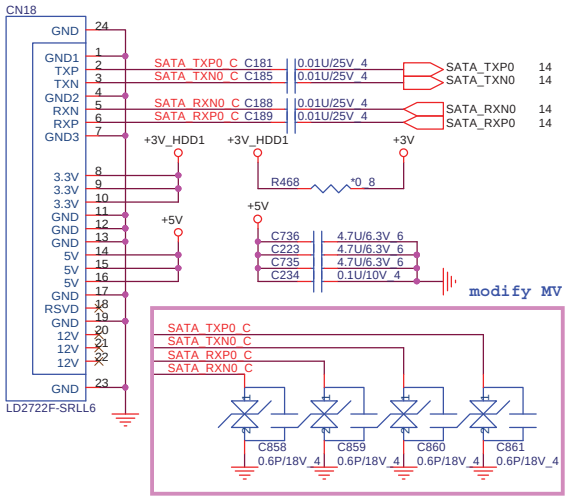
PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

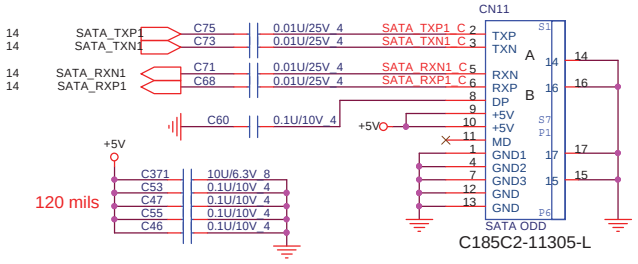
Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	3A

Date: Monday, March 15, 2010 Sheet 30 of 43

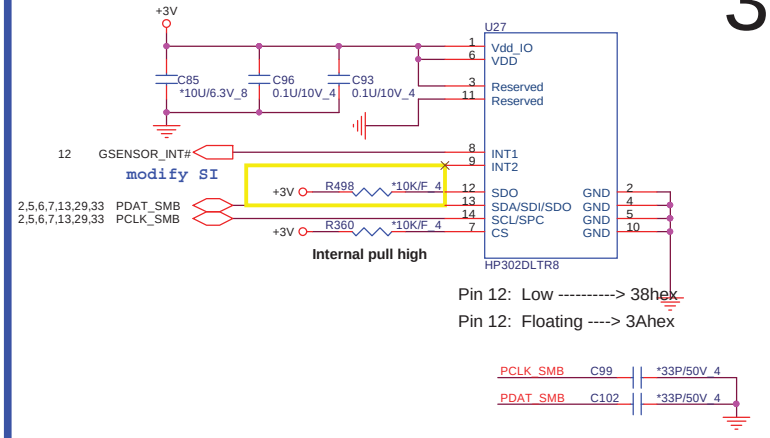
SATA HDD CONNECTOR



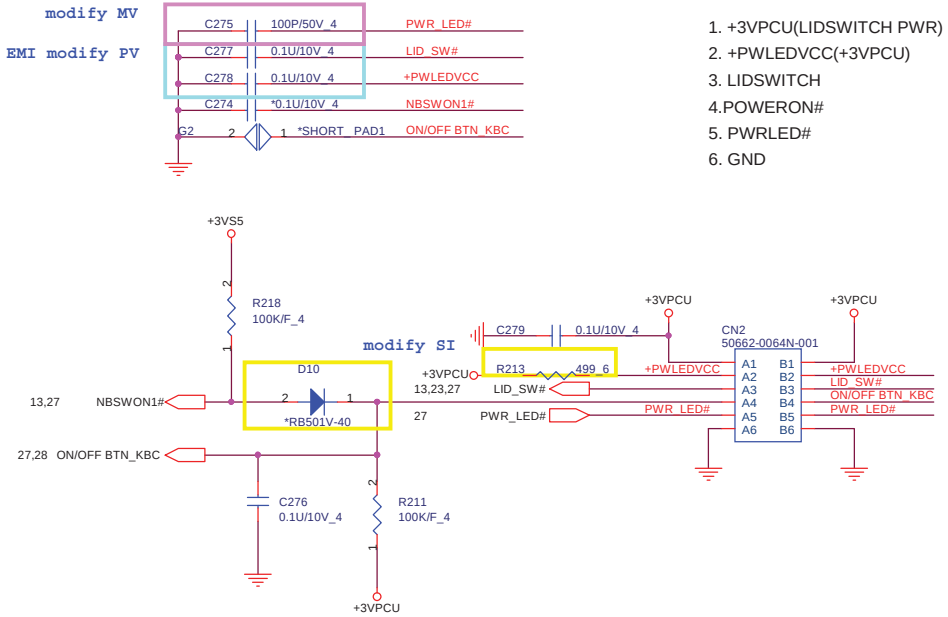
SATA CD-ROM



Accelerometer Sensor

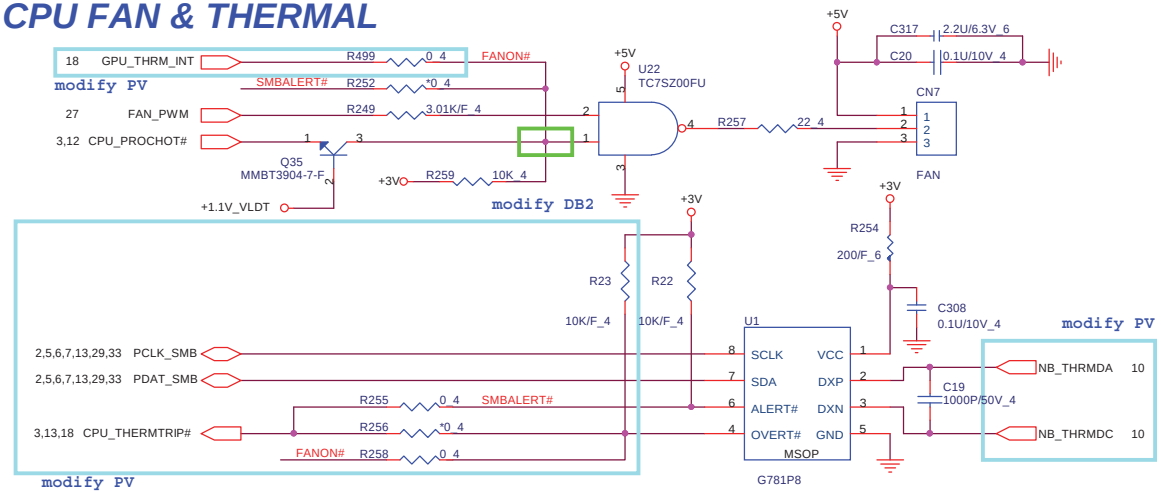


POWER BOTTON CONNECT

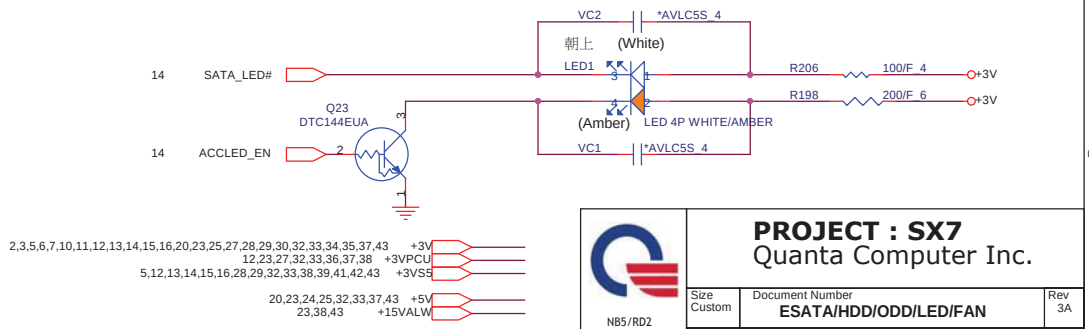


1. +3VPCU(LIDSWITCH PWR)
2. +PWLEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

CPU FAN & THERMAL



LED



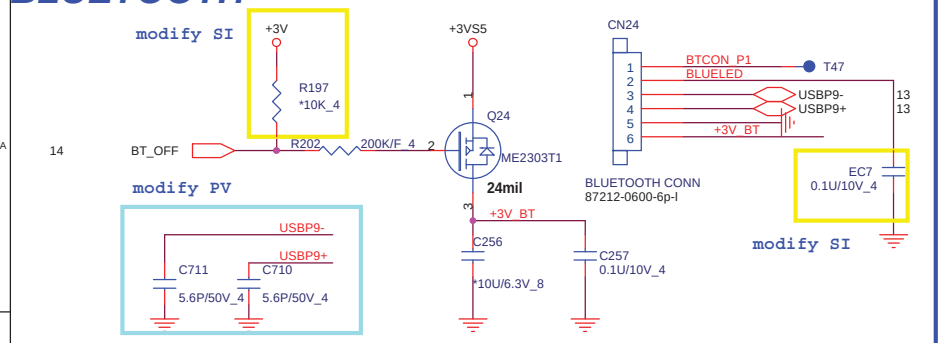
PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ESATA/HDD/ODD/LED/FAN	3A

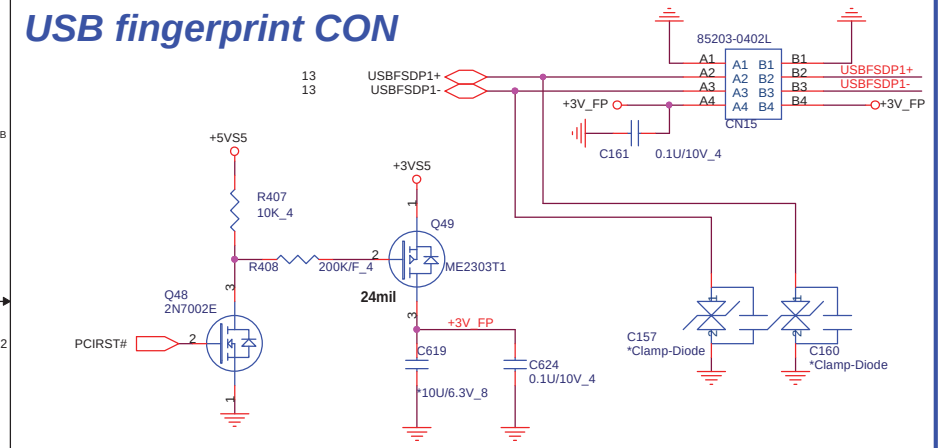
Date: Monday, March 15, 2010 | Sheet 31 of 43

NB5/RD2

BLUETOOTH

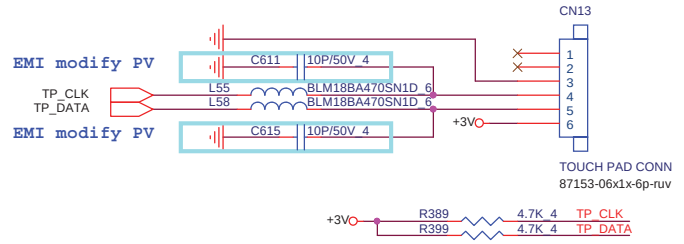


USB fingerprint CON

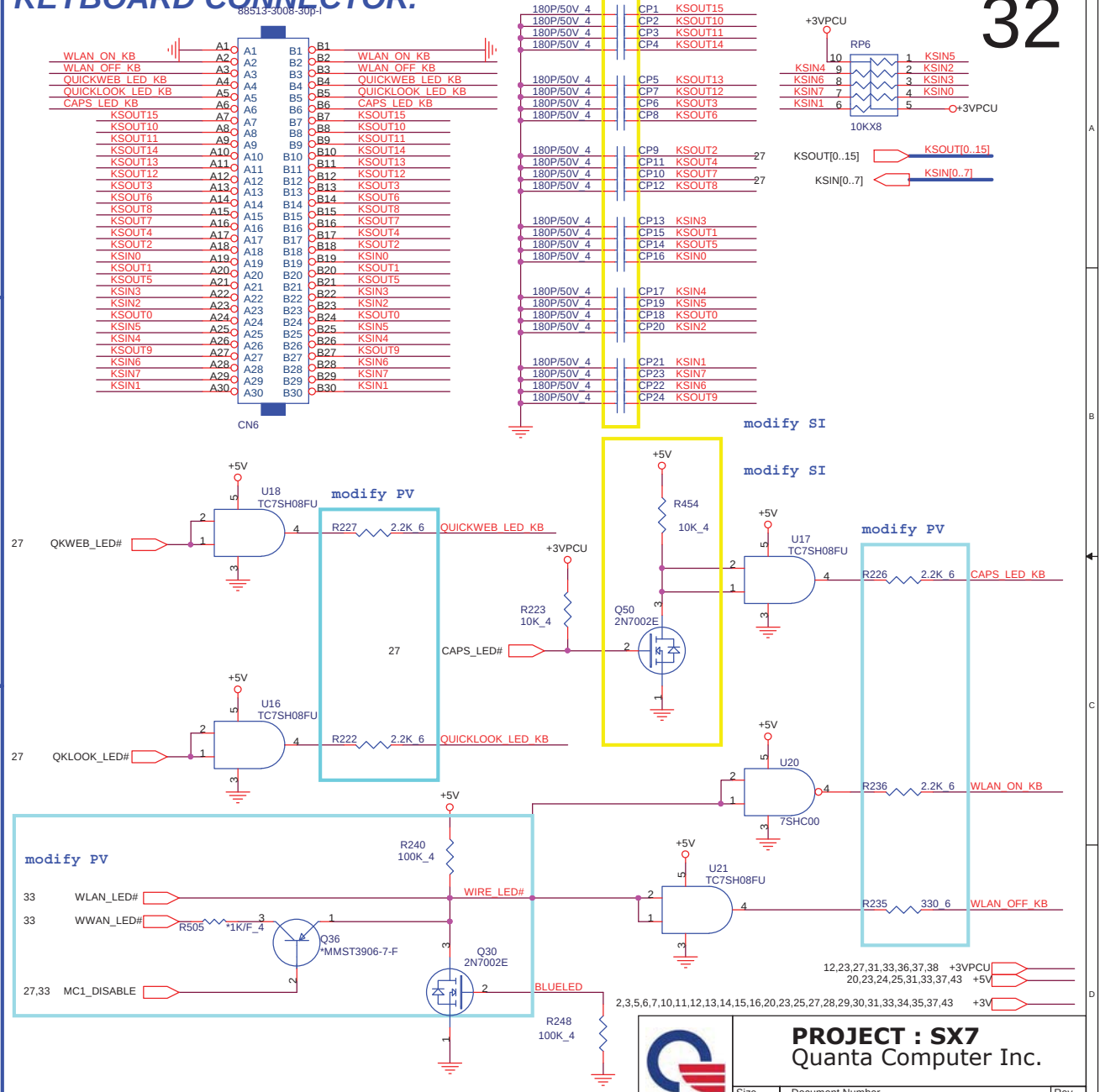


TOUCH PAD CONNECTOR

Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X



KEYBOARD CONNECTOR.



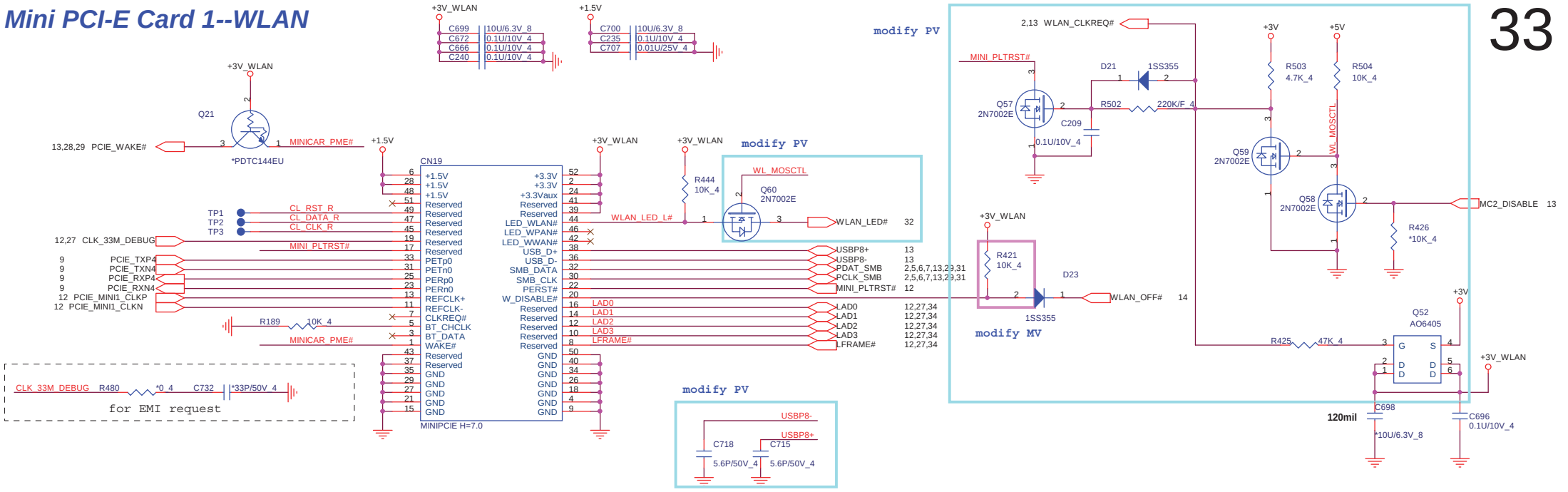
PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

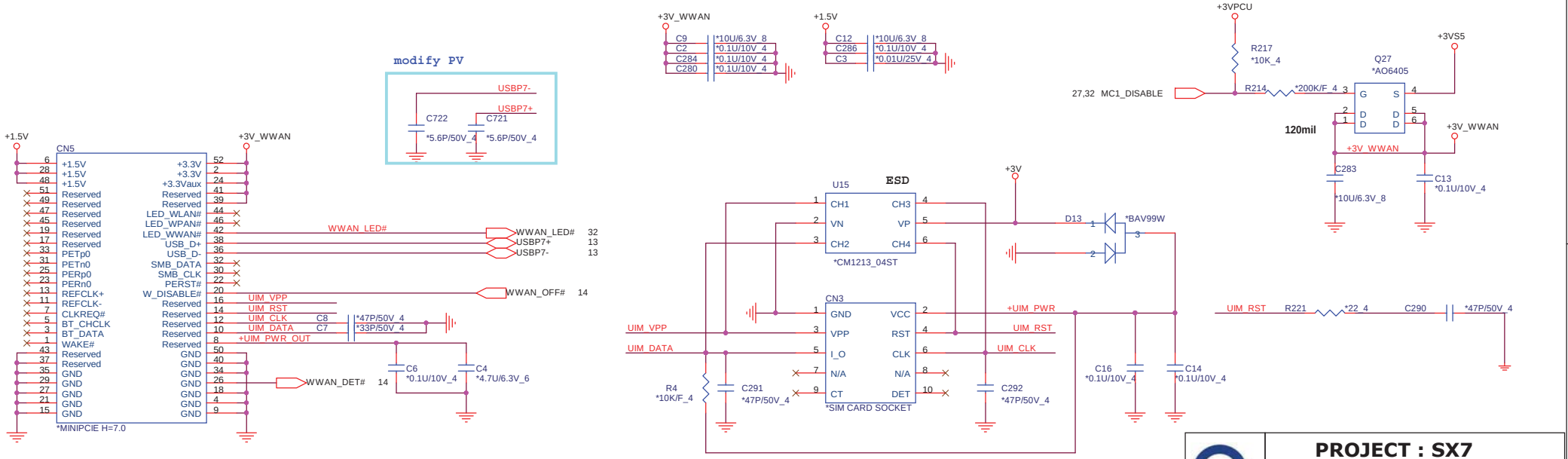
Size	Document Number	Rev
Custom	BT/WC/FT/ESATA/USB/LED	3A

Date: Monday, March 15, 2010 Sheet 32 of 43

Mini PCI-E Card 1--WLAN



Mini PCI-E Card 2 --WWAN

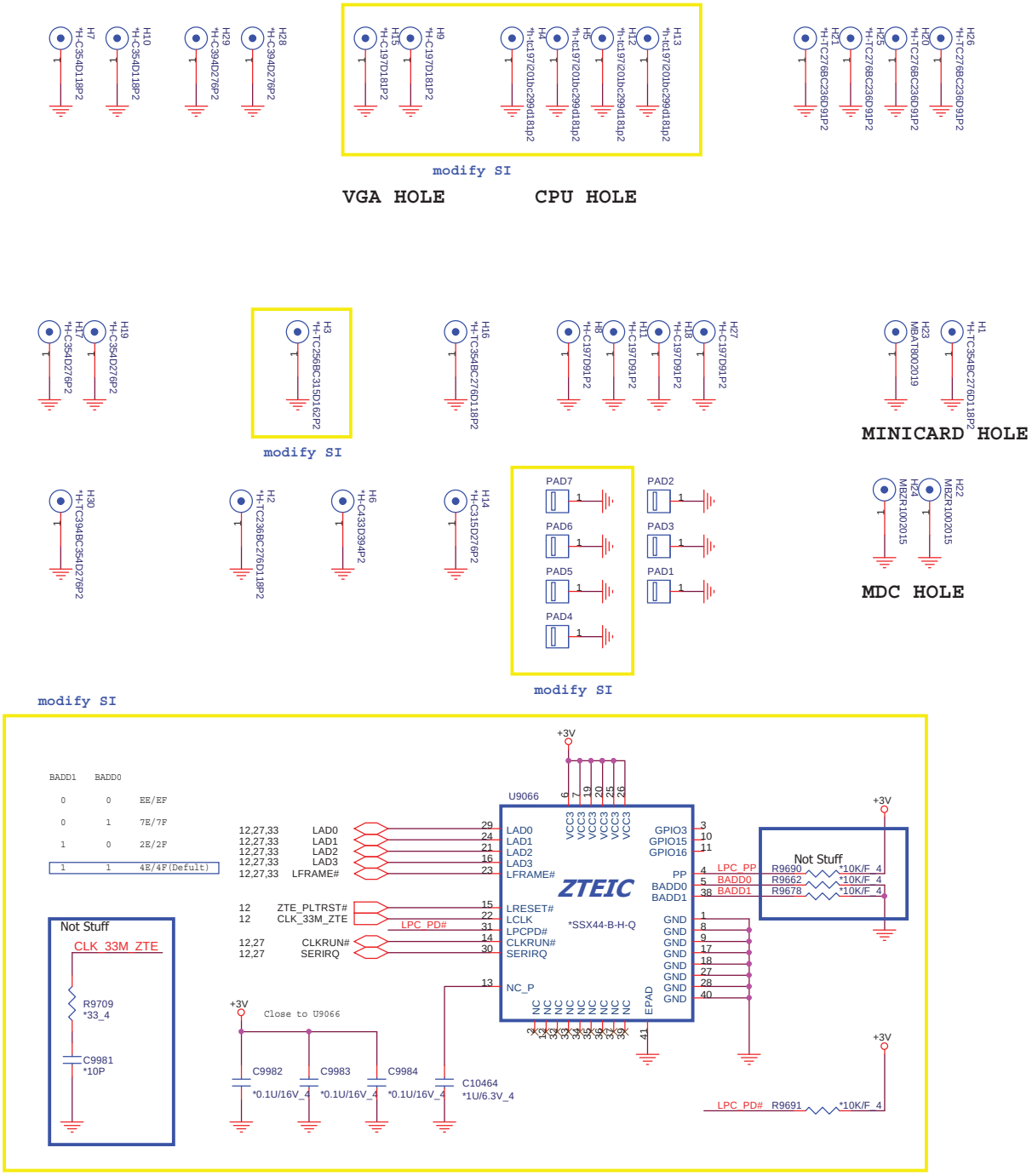


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	3A

Date: Monday, March 15, 2010 Sheet 33 of 43

NB5/RD2

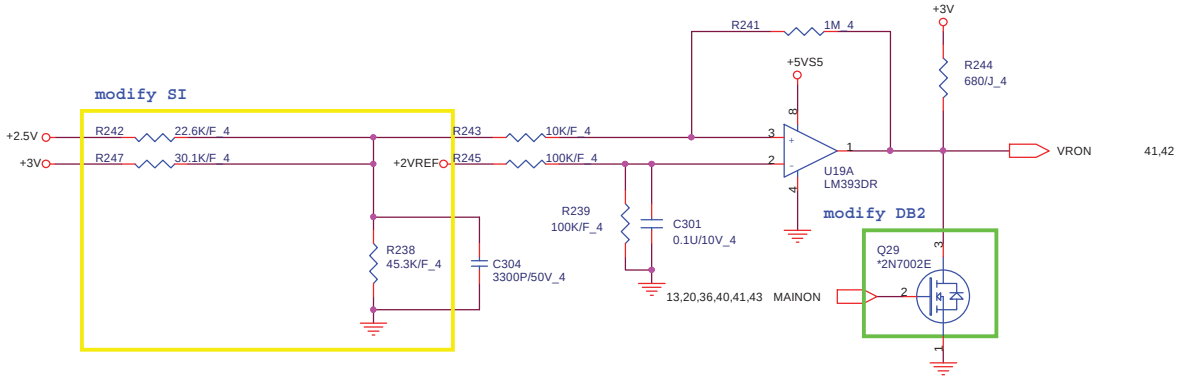


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hole, Nuts	3A

NB5/RD2

Date: Monday, March 15, 2010 Sheet 34 of 43

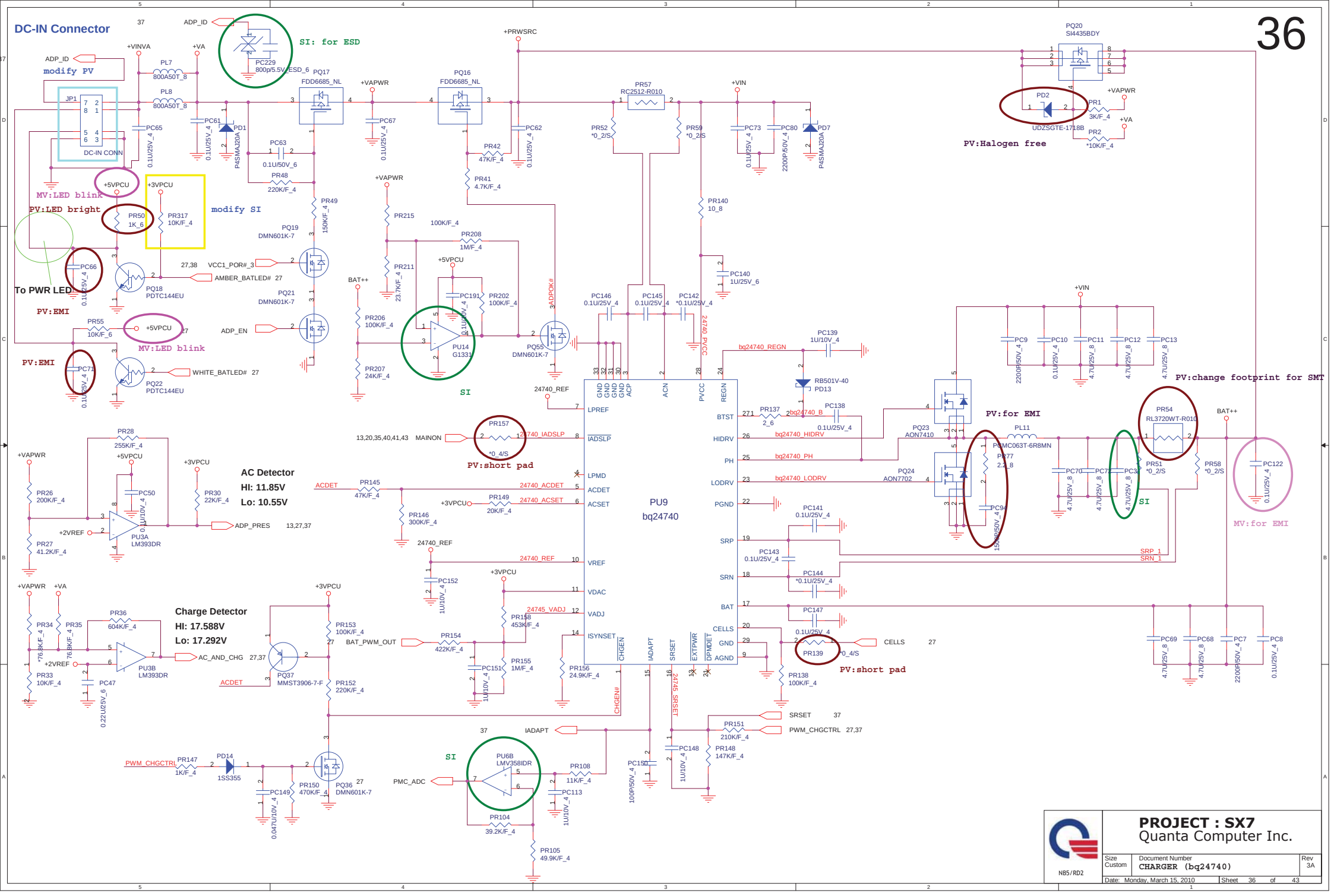


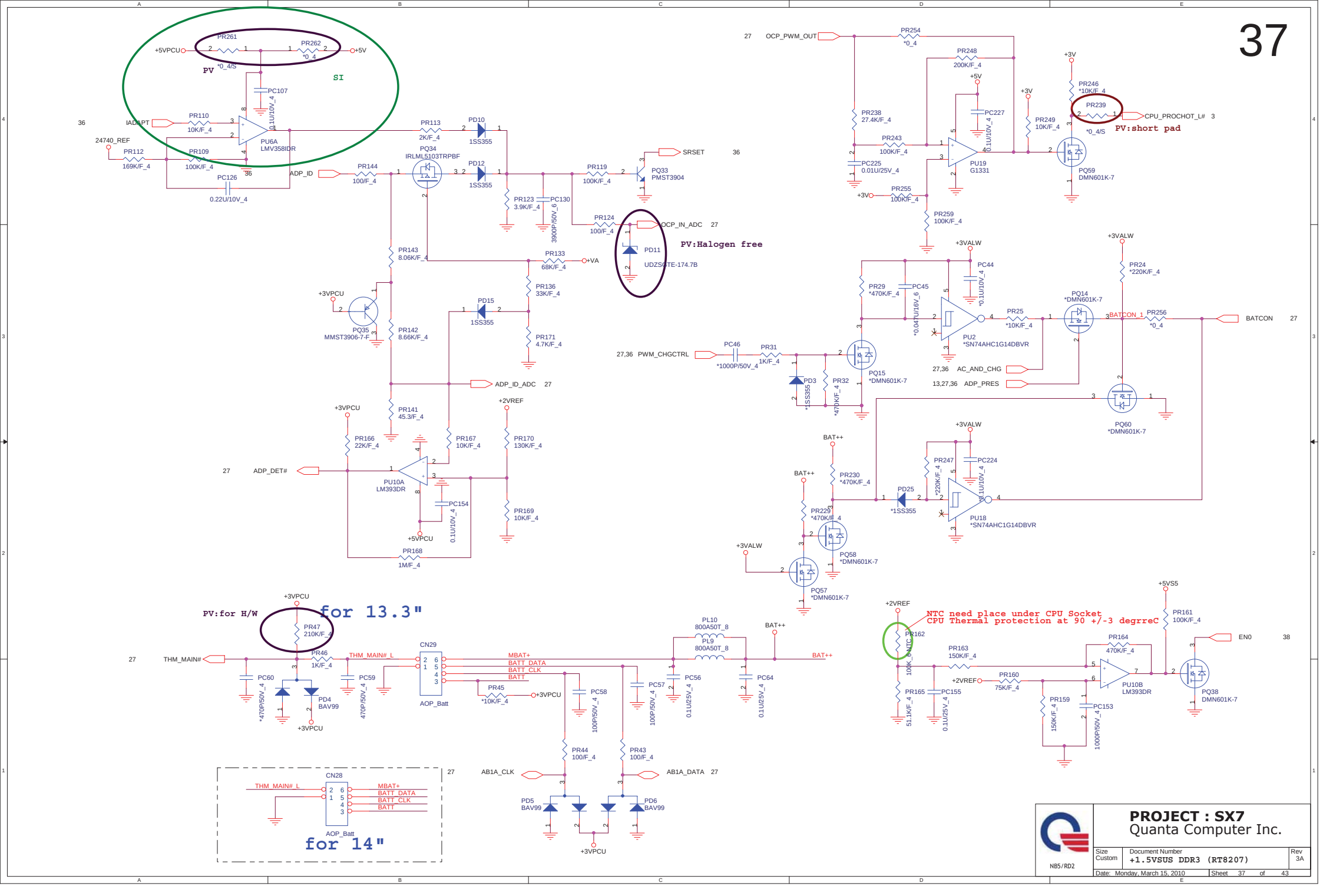
PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	**POWER Sequance**	3A

Date: Monday, March 15, 2010 | Sheet 35 of 43


DC-IN Connector
SI: for ESD
modify PV
MV:LED blink
PV:LED bright
modify SI
To PWR LED
PV:EMI
PV:Halogen free
PV:change footprint for SMT
PV:for EMI
MV:for EMI
SI
PV:short pad
AC Detector
HI: 11.85V
Lo: 10.55V
Charge Detector
HI: 17.588V
Lo: 17.292V
PU9
bq24740
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
CHARGER (bq24740)
Rev 3A
Date: Monday, March 15, 2010
Sheet 36 of 43
NB5/RD2

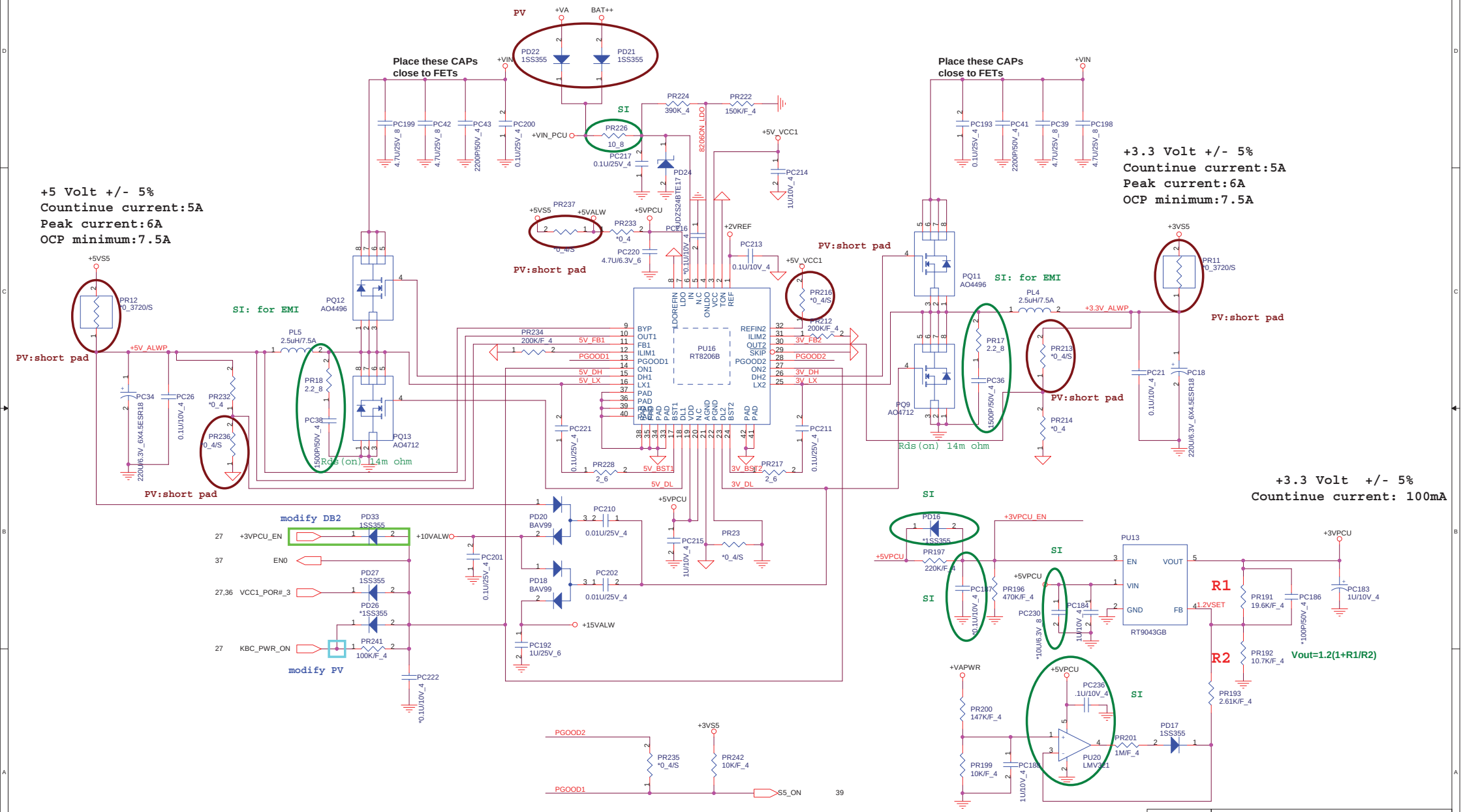


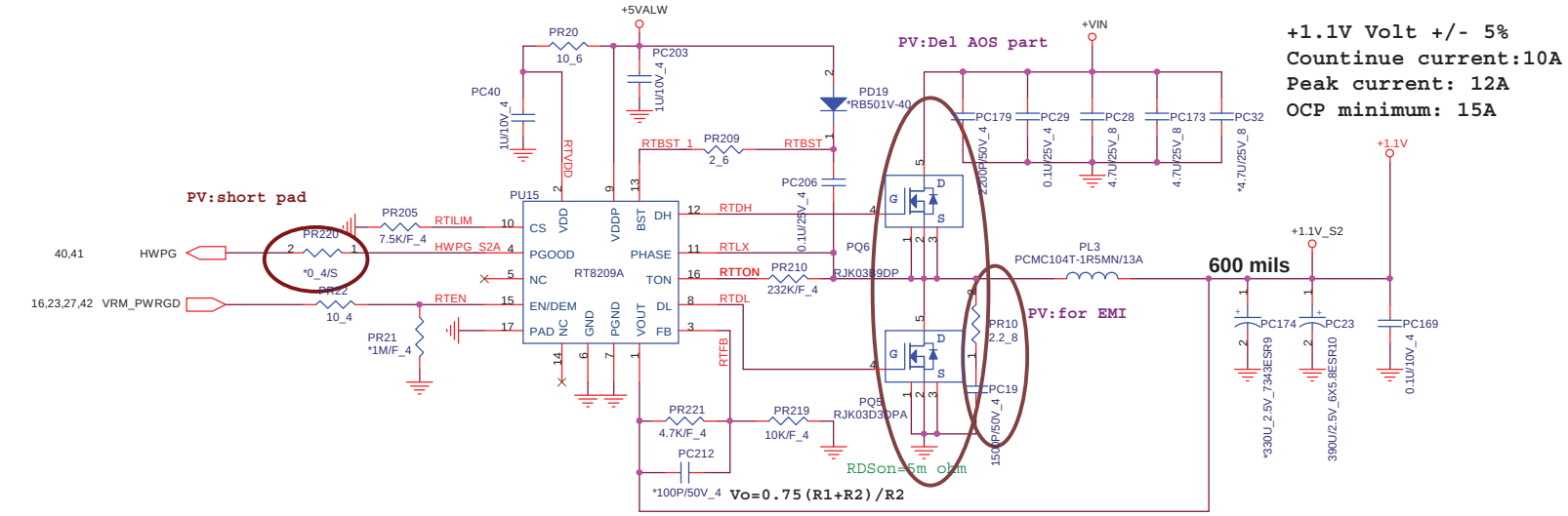
PROJECT : SX7
Quanta Computer Inc.

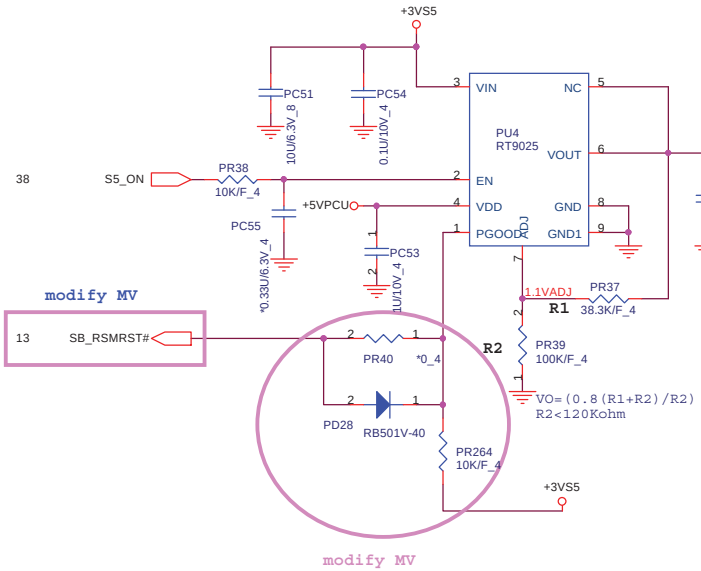
Size	Document Number	Rev
Custom	+1.5VSUS DDR3 (RT8207)	3A

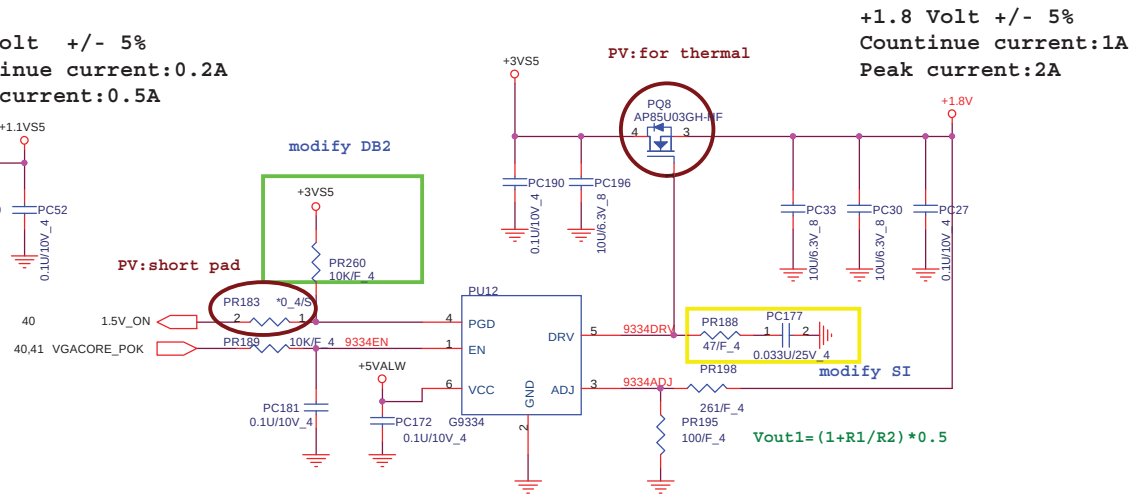
Date: Monday, March 15, 2010 | Sheet 37 of 43

N85/RD2


+5 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current: 100mA
Place these CAPs close to FETs
PV
SI
SI: for EMI
PV:short pad
Rds(on) 14m ohm
modify DB2
modify PV
PU16 RT8206B
PU13 RT9043GB
Vout=1.2(1+R1/R2)
R1
R2
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number +5V/+3V (RT8206B)
Rev 3A
Date: Monday, March 15, 2010
Sheet 38 of 43
NB5/RD2





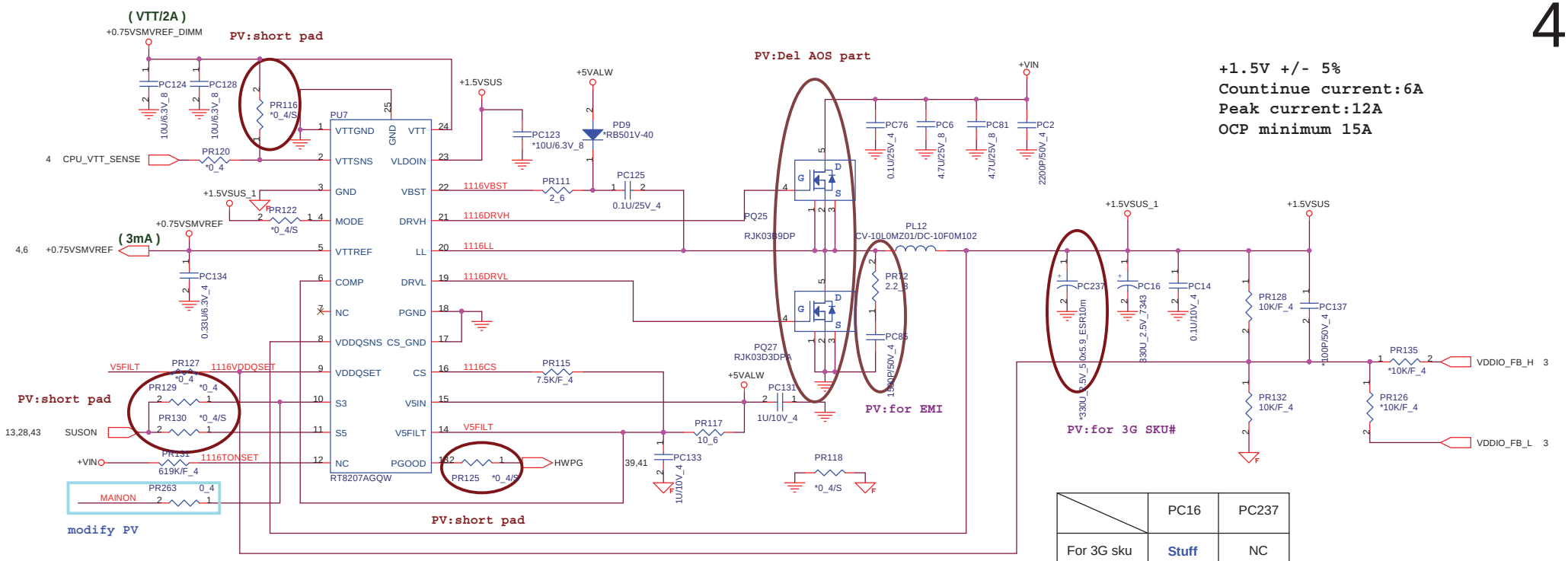


PROJECT : SX7
Quanta Computer Inc.

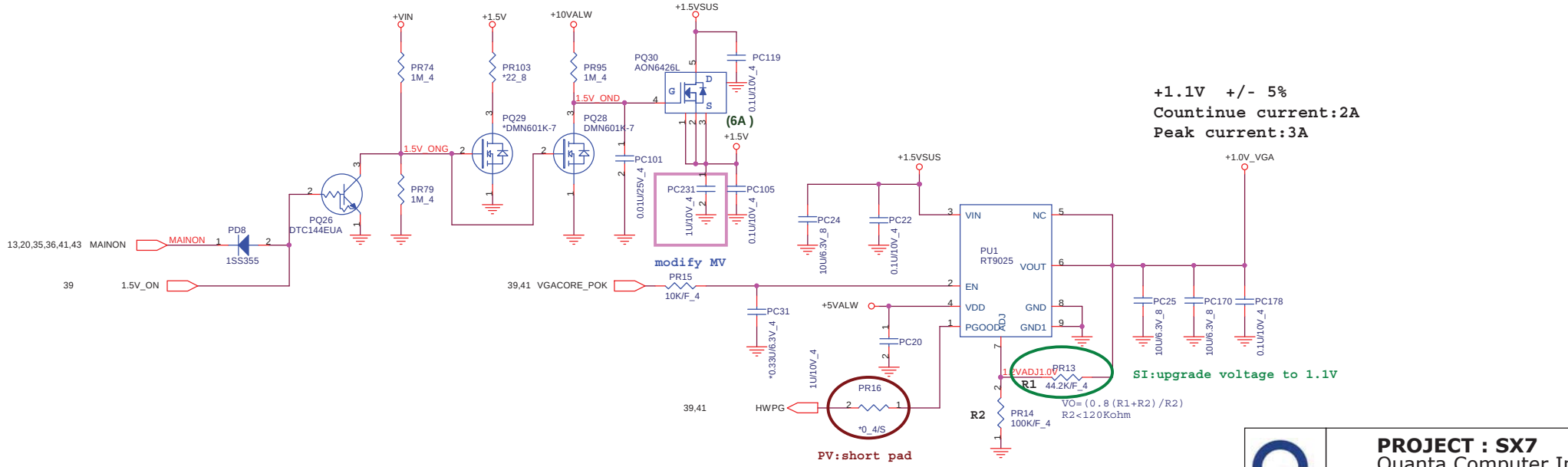
Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

NB5/RD2

Date: Monday, March 15, 2010 Sheet 39 of 43



	PC16	PC237
For 3G sku	Stuff	NC
non 3G sku	NC	Stuff



NB5/RD2

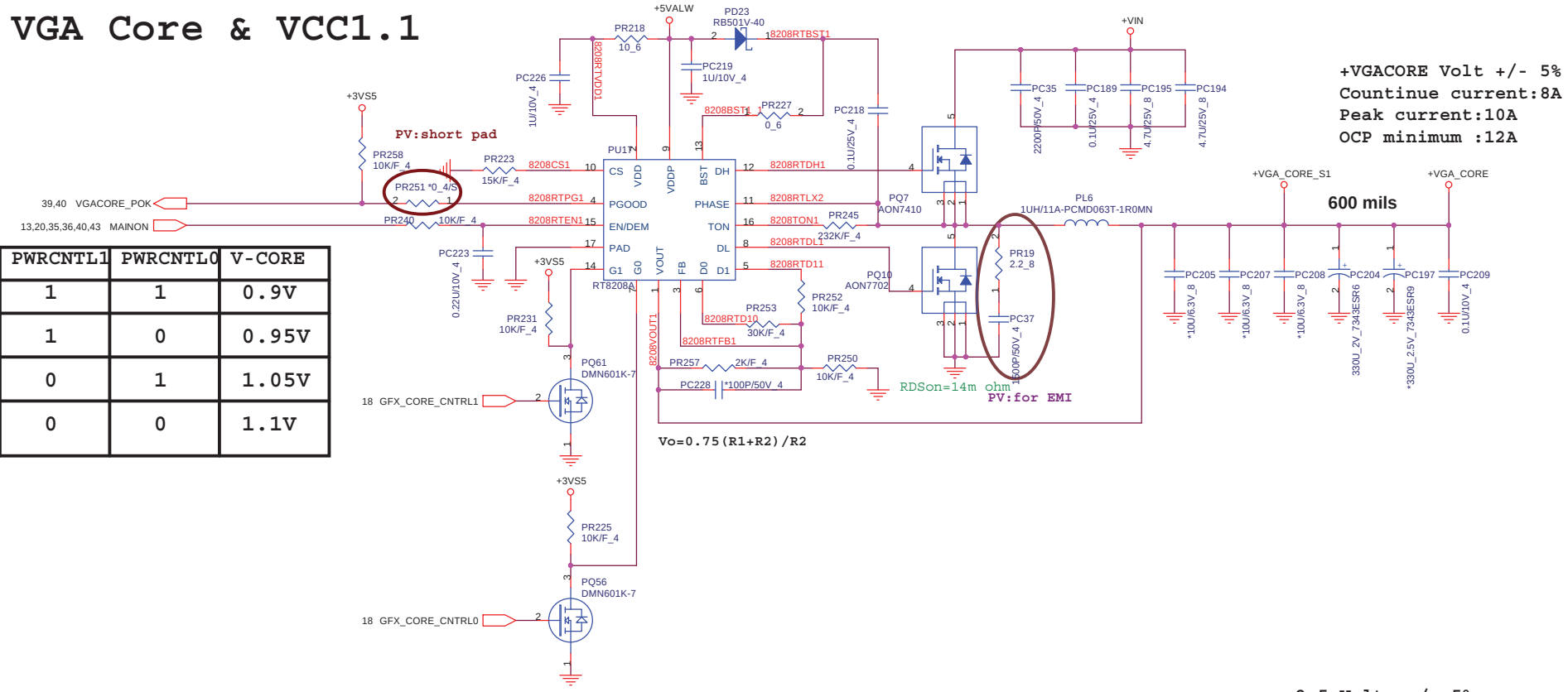
PROJECT : SX7
Quanta Computer Inc.

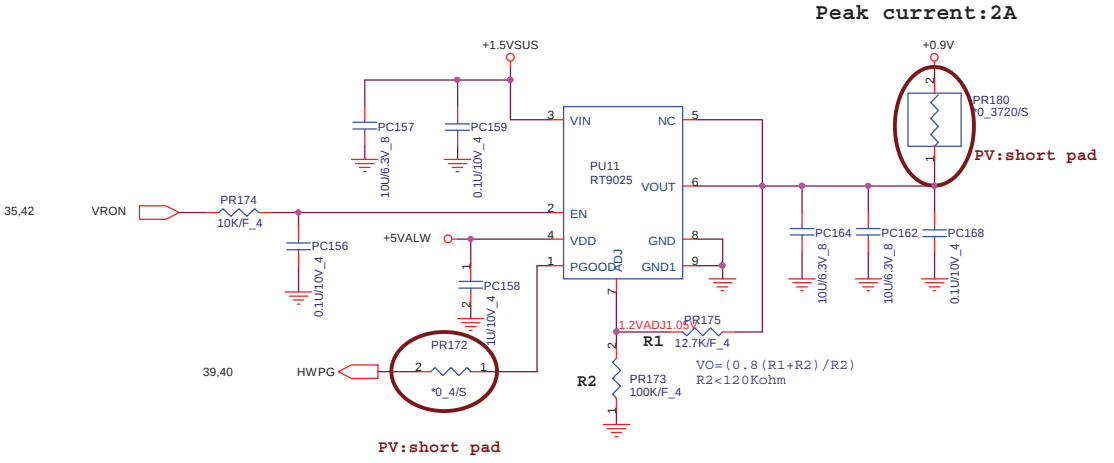
Size	Document Number	Rev
Custom	DDR3 (RT8207)	3A

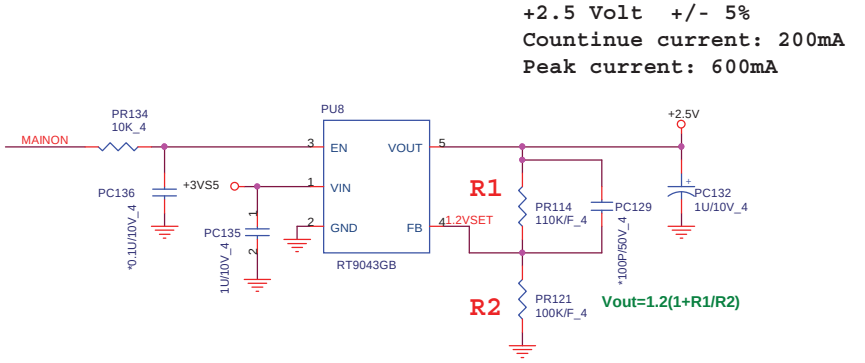
Date: Monday, March 15, 2010 Sheet 40 of 43

VGA Core & VCC1.1

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V







PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

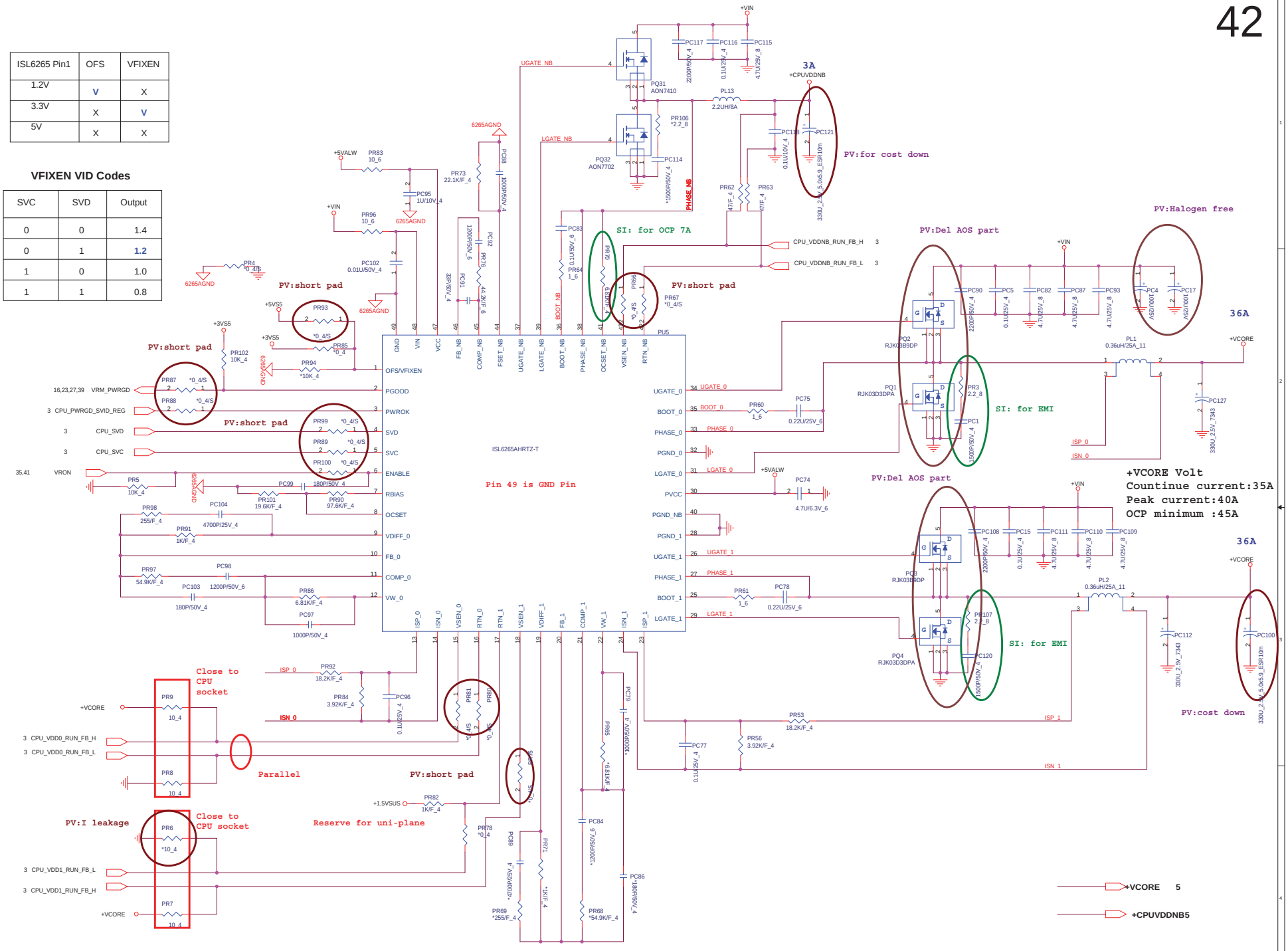
Date: Monday, March 15, 2010 Sheet 41 of 43

NB5/RD2

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

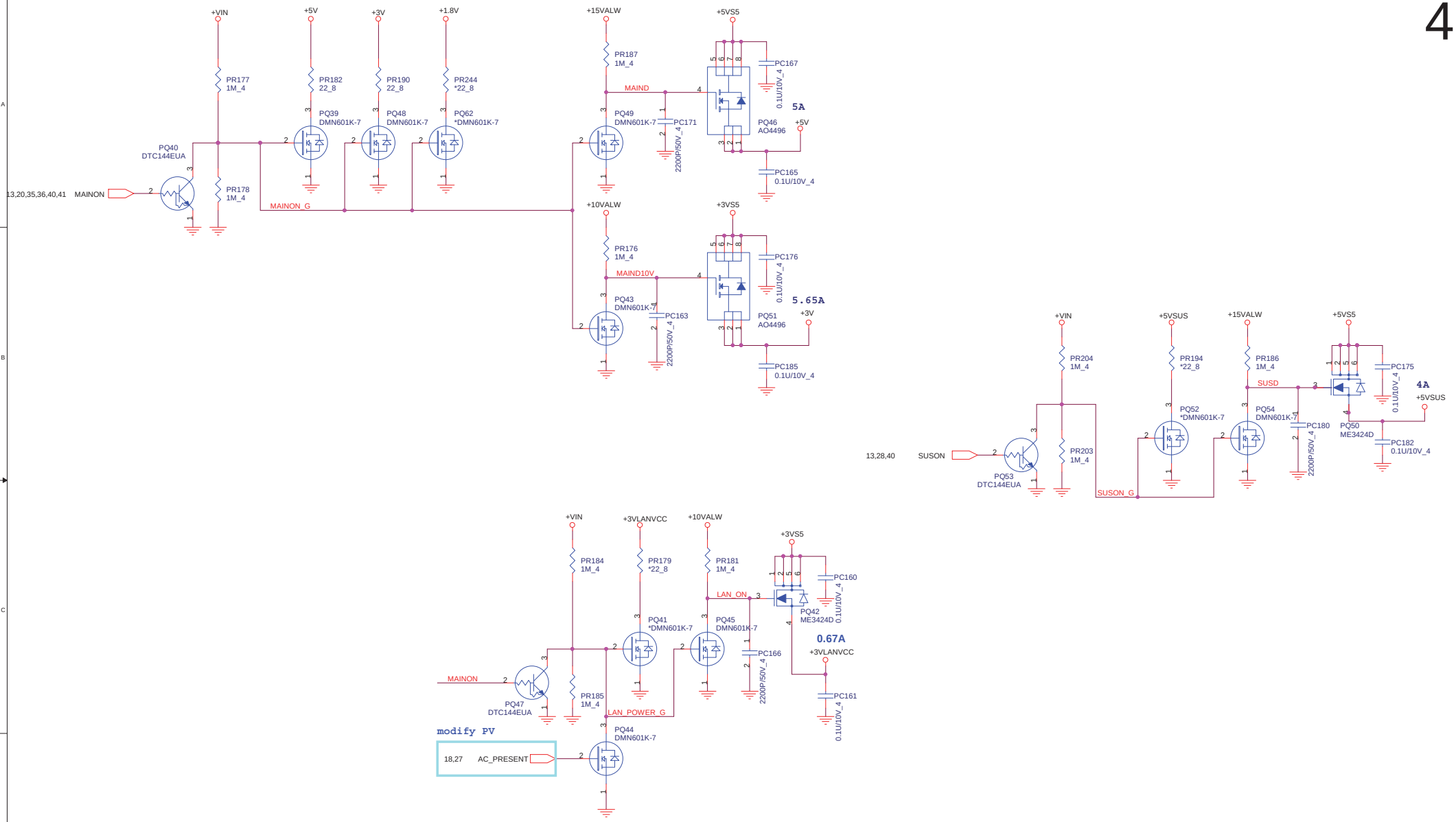


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_CORE(ISL6265)	3A

Date: Monday, March 15, 2010 Sheet 42 of 43

NB5/RD2



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	3A

Date: Monday, March 15, 2010 Sheet 43 of 43

NB5/RD2