LX89 SYSTEM DIAGRAM

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

DDR3-SODIMM1 PAGE 6,7
DDR3-SODIMM2 PAGE 6,7
DDR3 channel A
DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)45W/35W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E
X1
X1

LAN
Realtek
PCIE-LAN
RTL8111D
(10/100/1000)
PAGE 32

Mini PCI-E Card
(Wireless LAN)
PAGE 35

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

PCI-Express 16X
Side port
DDR3 RAM UMA Only PAGE 8

ATI
PARK-PRO 64 bit
Madison 128 bit
29mm X 29mm
PAGE 17,18,19 20,21

HDMI
CRT
LVDS

DDR3 800MHz
VRAM
64MX16X4,64 bit
64MX16X8,128 bit
PAGE 22,23

MUXs (S.G) PAGE 26

HDMI PAGE 27
CRT PAGE 25
LVDS PAGE 24

CRT
LVDS

RJ45 PAGE 32

ALINK X4

SOUTH BRIDGE
SB820
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

SATA - HDD1 PAGE 34 — SATA0 150MB
SATA - CD-ROM PAGE 34 — SATA1 150MB
SATA - HDD2 PAGE 34 — SATA2 150MB
E-SATA PAGE 33 — SATA3 150MB
Accelerometer STM HP302DL PAGE 30 — I2C

LPC
Azalia

BT softbreeze PAGE 34 — 15
FP VFM301 PAGE 34 — 14
Touch Screen PAGE 24

USB1.1
USB2.0

1,8,9 USB2.0 Ports X3 PAGE 29
E-SATA&USB Combo
5 Webcam X1 PAGE 23
2 Flash Media RTS5159 PAGE 26
3 PCI-E WLAN Card x1 PAGE 33

ENE KBC
KB3926 Dx
PAGE 37

Keyboard PAGE 36
Touch Pad PAGE 36

FAN PAGE 28
SPI PAGE 37

IDT
92HD80
PAGE 27

AUDIO Amplifier PAGE 31
Sub Woofer PAGE 31

Digital MIC PAGE 29
AUDIO CONN (Phone/ MIC) PAGE 30
Speaker PAGE 29

SYSTEM CHARGER(ISL6251) PAGE 40
SYSTEM POWER ISL6237 PAGE 34
DDR II SMDDR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
VCCP +1.1V AND +1.2V(RT8204) PAGE 35
VGACORE(1.1V~1.2V)Oz8118 PAGE 38
CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE

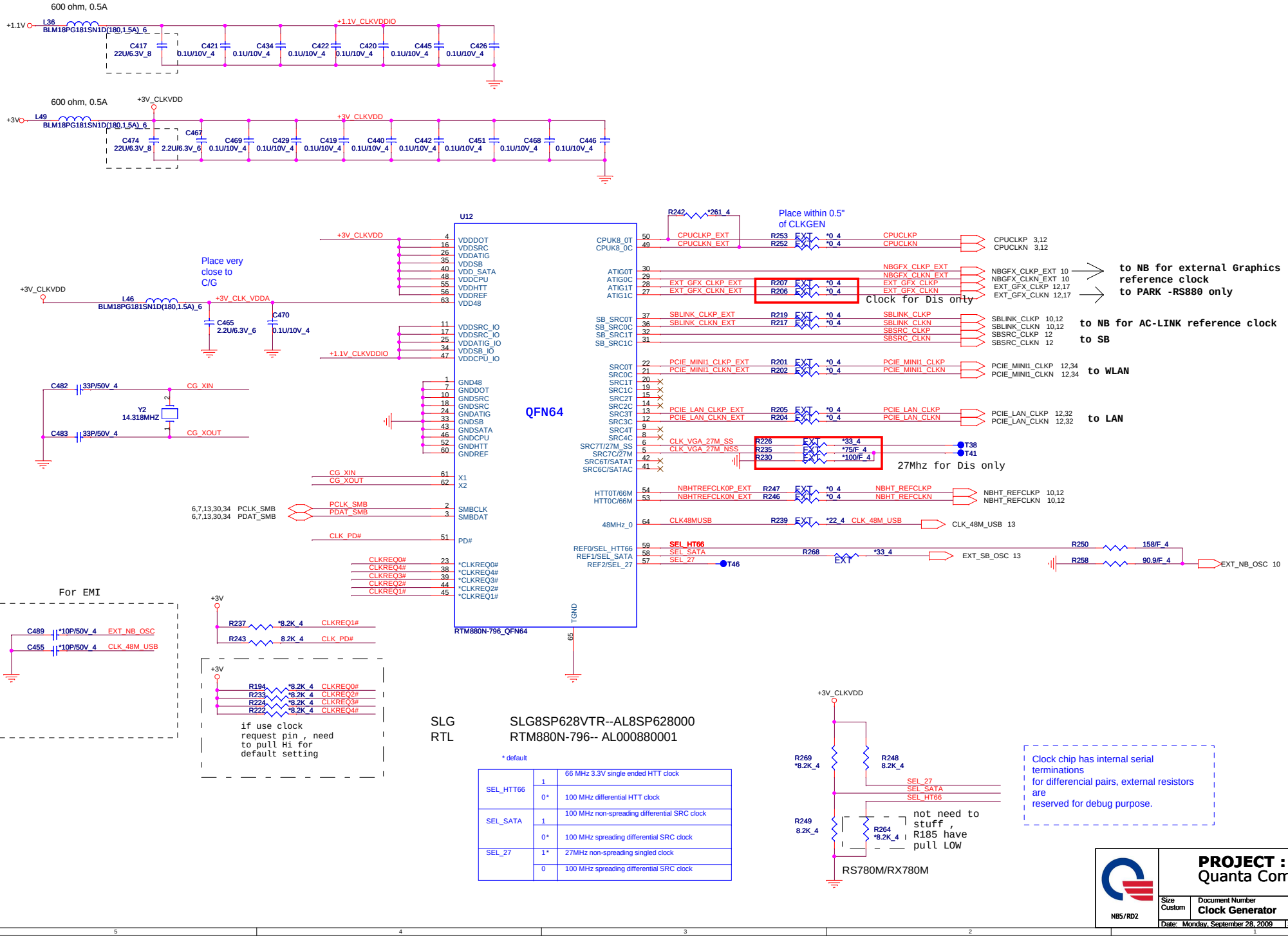
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

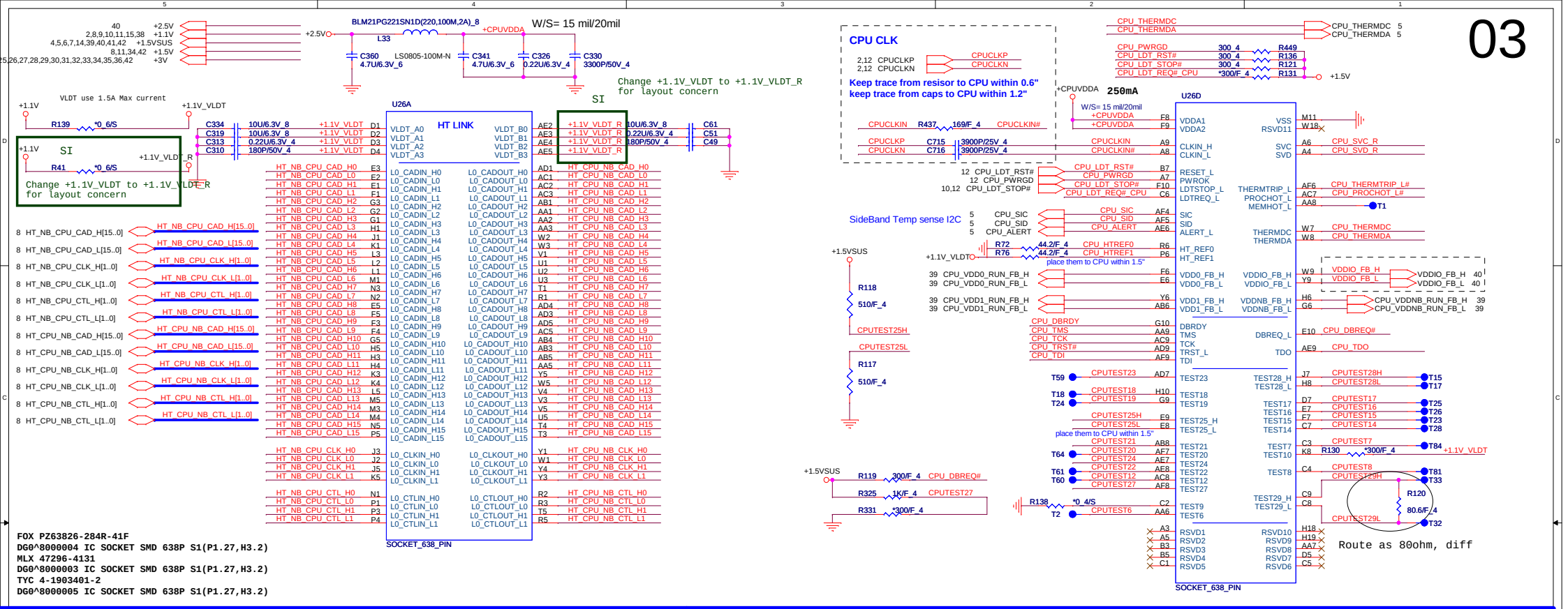
NB5/RD2

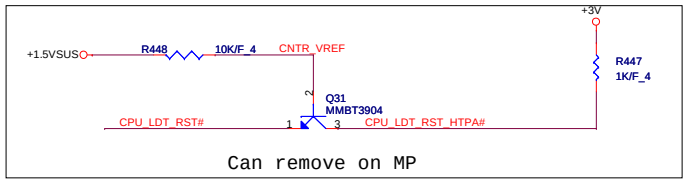
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

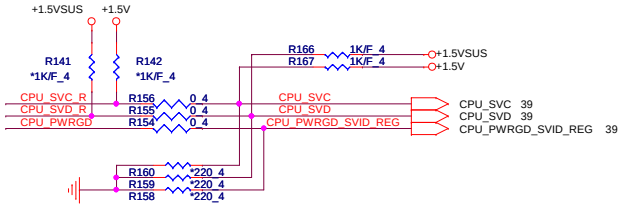
Date: Monday, September 28, 2009 Sheet 1 of 46


600 ohm, 0.5A
+1.1V
L36
BLM18PG181SN1D(180,1.5A)_6
+1.1V_CLKVDDIO
C417 22U/6.3V_8
C421 0.1U/10V_4
C434 0.1U/10V_4
C422 0.1U/10V_4
C420 0.1U/10V_4
C445 0.1U/10V_4
C426 0.1U/10V_4
600 ohm, 0.5A
+3V_CLKVDD
+3V
L49
BLM18PG181SN1D(180,1.5A)_6
C474 22U/6.3V_8
C467 2.2U/6.3V_6
C469 0.1U/10V_4
C429 0.1U/10V_4
C419 0.1U/10V_4
C440 0.1U/10V_4
C442 0.1U/10V_4
C451 0.1U/10V_4
C468 0.1U/10V_4
C446 0.1U/10V_4
U12
QFN64
RTM880N-796_QFN64
Place very close to C/G
L46
BLM18PG181SN1D(180,1.5A)_6
+3V_CLK_VDDA
C465 2.2U/6.3V_6
C470 0.1U/10V_4
C482 33P/50V_4
C483 33P/50V_4
Y2 14.318MHZ
CG_XIN
CG_XOUT
Place within 0.5" of CLKGEN
R242 *261_4
CPUCLKP_EXT
CPUCLKN_EXT
R253 EXT *0_4
R252 EXT *0_4
CPUCLKP
CPUCLKN
CPUCLKP 3,12
CPUCLKN 3,12
NBGFX_CLKP_EXT
NBGFX_CLKN_EXT
EXT_GFX_CLKP_EXT
EXT_GFX_CLKN_EXT
R207 EXT *0_4
R206 EXT *0_4
EXT_GFX_CLKP
EXT_GFX_CLKN
Clock for Dis only
to NB for external Graphics reference clock
to PARK -RS880 only
SBLINK_CLKP_EXT
SBLINK_CLKN_EXT
R219 EXT *0_4
R217 EXT *0_4
SBLINK_CLKP
SBLINK_CLKN
SBSRC_CLKP
SBSRC_CLKN
to NB for AC-LINK reference clock
to SB
PCIE_MINI1_CLKP_EXT
PCIE_MINI1_CLKN_EXT
R201 EXT *0_4
R202 EXT *0_4
PCIE_MINI1_CLKP
PCIE_MINI1_CLKN
to WLAN
PCIE_LAN_CLKP_EXT
PCIE_LAN_CLKN_EXT
R205 EXT *0_4
R204 EXT *0_4
PCIE_LAN_CLKP
PCIE_LAN_CLKN
to LAN
CLK_VGA_27M_SS
CLK_VGA_27M_NSS
R226 EXT *33_4
R235 EXT *75/F_4
R230 EXT *100/F_4
T38
T41
27Mhz for Dis only
NBHTREFCLK0P_EXT
NBHTREFCLK0N_EXT
R247 EXT *0_4
R246 EXT *0_4
NBHT_REFCLKP
NBHT_REFCLKN
CLK48MUSB
R239 EXT *22_4
CLK_48M_USB
SEL_HT66
SEL_SATA
SEL_27
R268 EXT *33_4
T46
EXT_SB_OSC 13
R250 158/F_4
R258 90.9/F_4
EXT_NB_OSC 10
PCLK_SMB
PDAT_SMB
CLK_PD#
CLKREQ0#
CLKREQ4#
CLKREQ3#
CLKREQ2#
CLKREQ1#
For EMI
C489 *10P/50V_4 EXT_NB_OSC
C455 *10P/50V_4 CLK_48M_USB
R237 *8.2K_4 CLKREQ1#
R243 8.2K_4 CLK_PD#
R194 *8.2K_4 CLKREQ0#
R233 *8.2K_4 CLKREQ2#
R224 *8.2K_4 CLKREQ3#
R222 *8.2K_4 CLKREQ4#
if use clock request pin , need to pull Hi for default setting
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001
* default
SEL_HTT66 1 66 MHz 3.3V single ended HTT clock
SEL_HTT66 0* 100 MHz differential HTT clock
SEL_SATA 1 100 MHz non-spreading differential SRC clock
SEL_SATA 0* 100 MHz spreading differential SRC clock
SEL_27 1* 27MHz non-spreading singled clock
SEL_27 0 100 MHz spreading differential SRC clock
R269 *8.2K_4
R248 8.2K_4
R249 8.2K_4
R264 *8.2K_4
not need to stuff , R185 have pull LOW
RS780M/RX780M
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
PROJECT : LX89
Quanta Computer Inc.
Size Custom
Document Number Clock Generator
Rev 1A
Date: Monday, September 28, 2009
Sheet 2 of 46
NB5/RD2

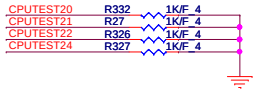


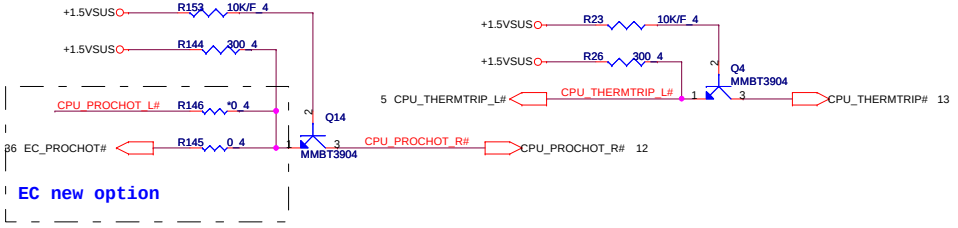


Serial VID

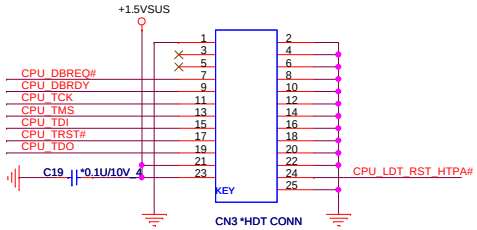


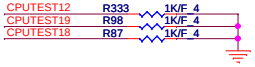
VFIX MODE	VID Override table (VDD)	
SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V





HDT Connector





PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 HT,CTL I/F 1/3	1A
Date: Monday, September 28, 2009	Sheet 3 of 46	

N85/RD2

Processor Memory Interface

35W->+0.9V
45W->+1.05V

PLACE THEM CLOSE TO CPU WITHIN 1"

U26B — MEM:CMD/CTRL/CLK — SOCKET_638_PIN

U26C — MEM:DATA — SOCKET_638_PIN

Place close to socket

Reserved for AMD suggest

Reserved

+VCORE 39
+CPUVDDNB 39
+1.5VSUS 3,4,6,7,14,39,40,41,42
+3VS5 12,13,14,15,16,42
+5V 24,25,26,27,28,29,33,34,35,42
+1.8V 8,10,11,16,26,42

U26E

SOCKET_638_PIN

U26F

SOCKET_638_PIN

BOTTOM SIDE DECOUPLING

+VCORE: C107 22U/6.3V_8, C135 22U/6.3V_8, C154 22U/6.3V_8, C166 22U/6.3V_8, C173 0.22U/6.3V_4, C172 0.01U/16V_4, C171 180P/50V_4

+VCORE: C167 22U/6.3V_8, C168 22U/6.3V_8, C150 22U/6.3V_8, C138 22U/6.3V_8, C106 0.22U/6.3V_4, C108 0.01U/16V_4, C117 180P/50V_4

+CPUVDDNB: C146 22U/6.3V_8, C133 22U/6.3V_8, C158 22U/6.3V_8

+1.5VSUS: C136 22U/6.3V_8, C152 22U/6.3V_8, C162 0.22U/6.3V_4, C174 0.22U/6.3V_4, C175 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.5VSUS: C632 4.7U/6.3V_6, C620 4.7U/6.3V_6, C623 4.7U/6.3V_6, C629 4.7U/6.3V_6, C116 0.22U/6.3V_4, C85 0.22U/6.3V_4

+1.5VSUS: C114 0.22U/6.3V_4, C183 0.22U/6.3V_4, C156 0.01U/16V_4, C624 0.1U/10V_4, C630 180P/50V_4, C91 180P/50V_4, C144 0.1U/10V_4

+CPUVDDNB 4A

+1.5VSUS 2A

+1.5VSUS: R21 2K/F_4, R157 2K/F_4, R25 2K/F_4

+1.5VSUS: R24 390_4, R165 390_4, R29 1K/F_4

Q3 *MMBT3904
19,36,43 MBCLK2 — MBCLK2 — CPU_SIC — CPU_SIC 3
*RB501V-40 D8
Q15 *MMBT3904
19,36,43 MBDATA2 — MBDATA2 — CPU_SID — CPU_SID 3
*RB501V-40 D12
Q6 *MMBT3904
SMBALERT# — CPU_ALERT — CPU_ALERT 3

PROCESSOR POWER AND GROUND

+3V: R147 10K/F_4, R140 10K/F_4, R135 10K/F_4

+3V: R134 200/F_6

C323 0.1U/10V_4

U8 G786P8 MSOP
SCLK, SDA, ALERT#, OVERT#, VCC, DXP, DXN, GND
19,36,43 MBCLK2
19,36,43 MBDATA2
13 PM_THERM#
CPU_THERMDA 3
CPU_THERMDC 3
C315 1000P/50V_4
SMBALERT#

reserve for power shutdown (if can)

R6 *0_4 — SYS_SHDN# — SYS_SHDN# 37
D1 *CH500H

R11 *0_4/S — 3920_RST# — 3920_RST# 36
Q2 MMBT3904
D2 CH501H-40PT
ECPWROK — ECPWROK 16,36
R17 10K/F_4 — +3V

+1.5VSUS: R16 *10K/F_4
Q1 *MMBT3904
3 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — SMBALERT#

PQ18 *2N7002E-G
R35 *10K/F_4 — TEMP_FAIL 19

ADD VGA TEMP_ FAIL function
M92 is active Hi

+3VS5: EC3 *0.1U/10V_4
+3VS5: EC4 *0.1U/10V_4
+3V: EC1 *0.1U/10V_4
+1.8V: EC2 *0.1U/10V_4

Need Check

For fix HyperTransport nets across plane splits

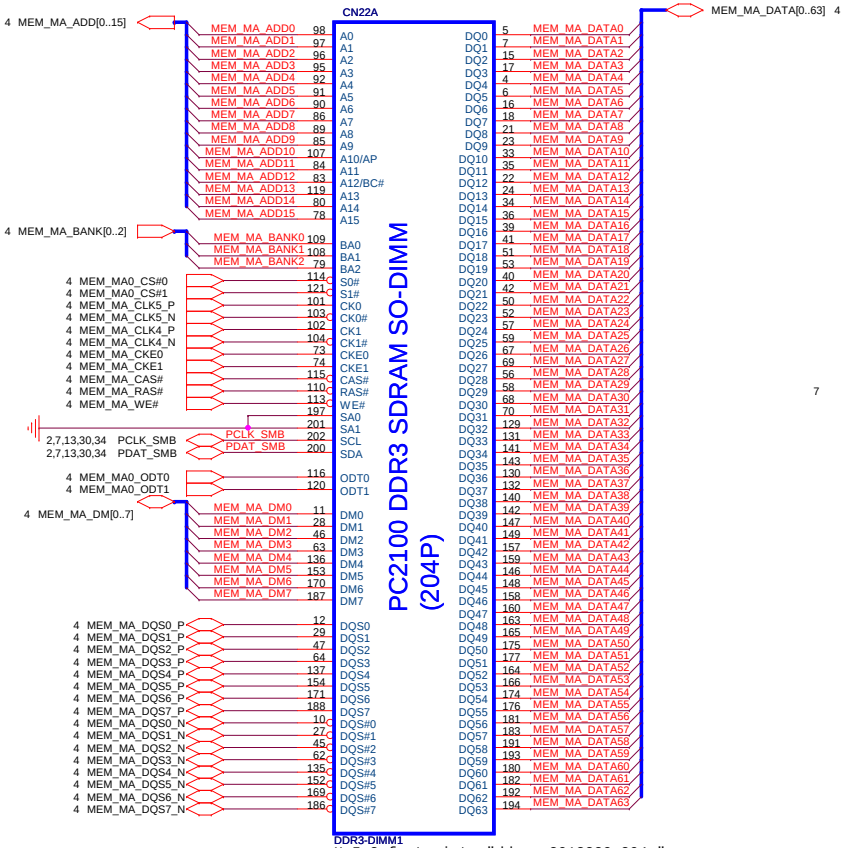
PROJECT : LX89
Quanta Computer Inc.

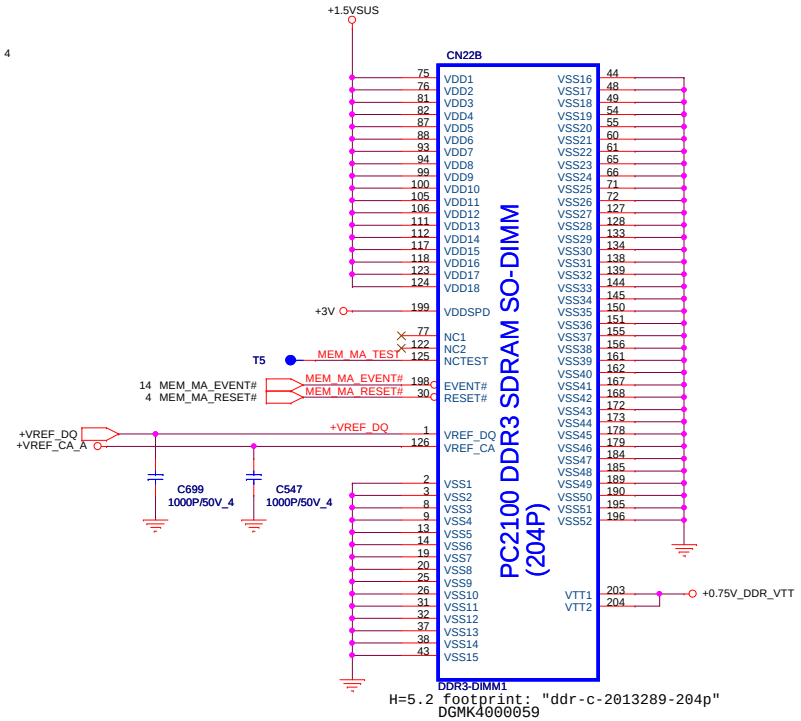
N85/RD2

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

Date: Monday, September 28, 2009 Sheet 5 of 46

+1.5VSUS 3,4,5,7,14,39,40,41,42
+3V 2,3,5,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 7,40



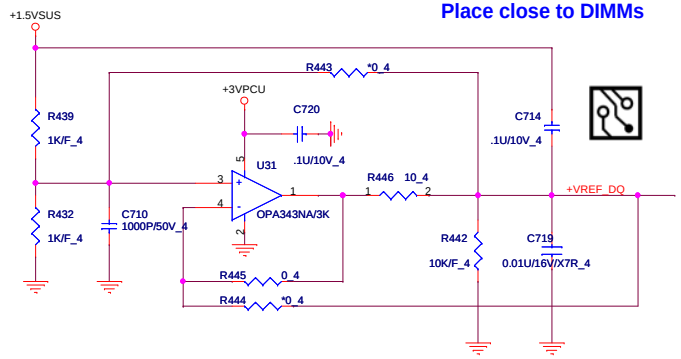


SO-DIMM BYPASS PLACEMENT :

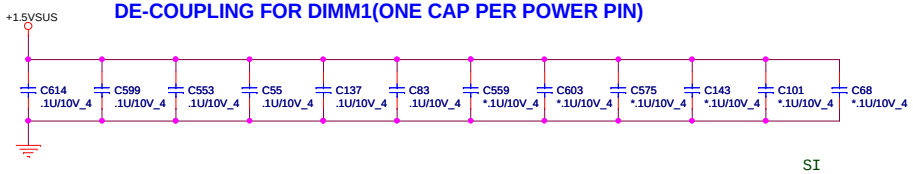
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

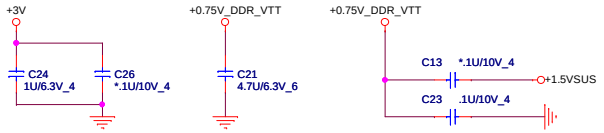
Place close to DIMMs



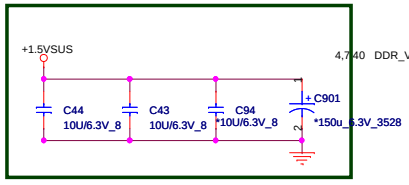
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

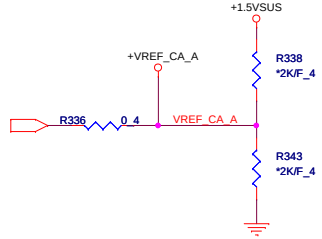


DE-COUPLING FOR DIMM1



SI



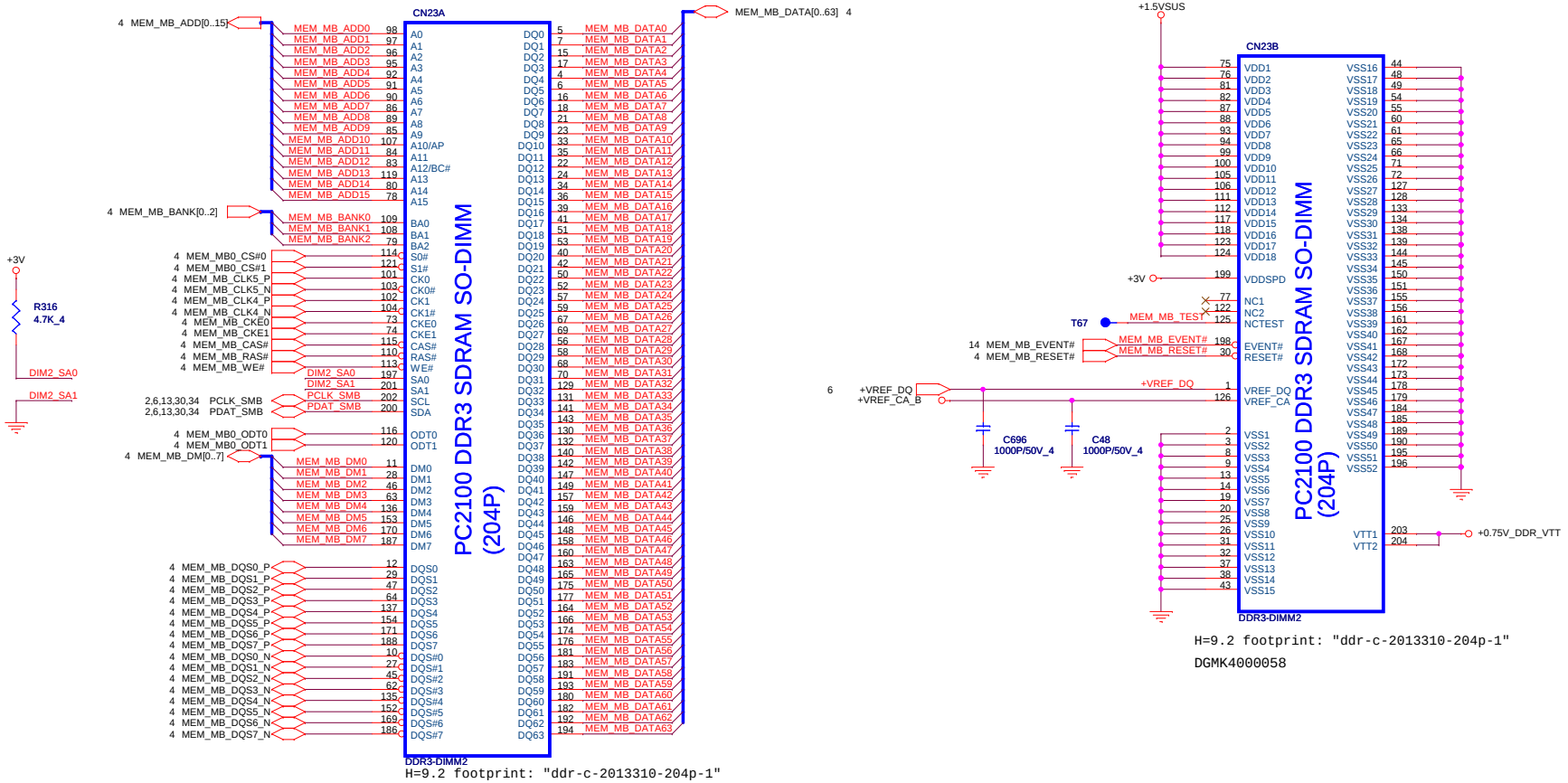


PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SODIMMS: A/B CHANNEL	1A
Date: Monday, September 28, 2009	Sheet 6 of 46	

N85/RD2

+1.5VSUS 3,4,5,6,14,39,40,41,42
+3V 2,3,5,6,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 6,40



H=9.2 footprint: "ddr-c-2013310-204p-1"
DGMK4000058

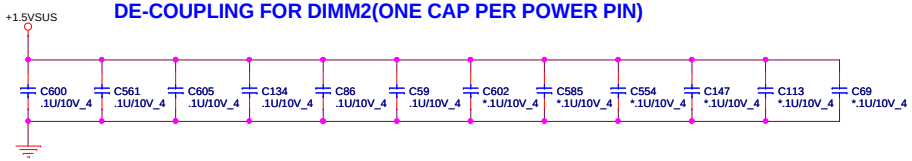
H=9.2 footprint: "ddr-c-2013310-204p-1"
DGMK4000058

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

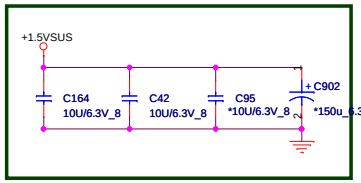
No Vias Between the Trace of PIN to CAP.

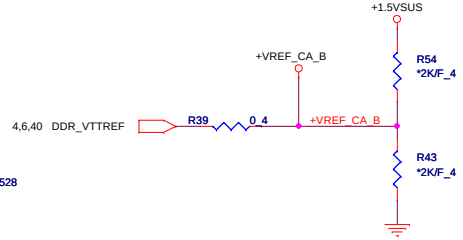
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



DE-COUPLING FOR DIMM2

SI





N85/RD2	**PROJECT : LX89** Quanta Computer Inc.	
Size Custom	Document Number **DDR3 SODIMMS TERMINATIONS**	Rev 1A
Date: Monday, September 28, 2009	Sheet 7 of 46	

+1.5V 3,11,34,42
+1.8V 5,10,11,16,26,42
+1.1V 2,3,9,10,11,15,38

HT_CPU_NB_CAD_H[15..0] → HT_CPU_NB_CAD_H[15..0] 3
HT_CPU_NB_CAD_L[15..0] → HT_CPU_NB_CAD_L[15..0] 3
HT_CPU_NB_CLK_H[1..0] → HT_CPU_NB_CLK_H[1..0] 3
HT_CPU_NB_CLK_L[1..0] → HT_CPU_NB_CLK_L[1..0] 3
HT_CPU_NB_CTL_H[1..0] → HT_CPU_NB_CTL_H[1..0] 3
HT_CPU_NB_CTL_L[1..0] → HT_CPU_NB_CTL_L[1..0] 3
HT_NB_CPU_CAD_H[15..0] → HT_NB_CPU_CAD_H[15..0] 3
HT_NB_CPU_CAD_L[15..0] → HT_NB_CPU_CAD_L[15..0] 3
HT_NB_CPU_CLK_H[1..0] → HT_NB_CPU_CLK_H[1..0] 3
HT_NB_CPU_CLK_L[1..0] → HT_NB_CPU_CLK_L[1..0] 3
HT_NB_CPU_CTL_H[1..0] → HT_NB_CPU_CTL_H[1..0] 3
HT_NB_CPU_CTL_L[1..0] → HT_NB_CPU_CTL_L[1..0] 3

U27A

HYPER TRANSPORT CPU I/F

PART 1 OF 6

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1
		HT_RXCALP	HT_TXCALP	B24	HT_TXCALP
		HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

R419 301/F_4 HT_RXCALP C23, HT_RXCALN A24 — Rb
R418 301/F_4 HT_TXCALP B24, HT_TXCALN B25 — Ra

RS880M

signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

U24

SPM_VREF1	M9	VREFCA	DQU0	E4	SPM_DQ2
SPM_VREF2	H2	VREFDQ	DQU1	F8	SPM_DQ1
			DQU2	F3	SPM_DQ5
SPM_A0	N4	A0	DQU3	E9	SPM_DQ3
SPM_A1	P8	A1	DQU4	H4	SPM_DQ7
SPM_A2	P4	A2	DQU5	H9	SPM_DQ0
SPM_A3	N3	A3	DQU6	G3	SPM_DQ4
SPM_A4	P9	A4	DQU7	H8	SPM_DQ6
SPM_A5	P3	A5			
SPM_A6	R9	A6			
SPM_A7	R3	A7	DQU0	D8	SPM_DQ13
SPM_A8	T9	A8	DQU1	C4	SPM_DQ8
SPM_A9	R4	A9	DQU2	C9	SPM_DQ10
SPM_A10	L8	A10/AP	DQU3	C3	SPM_DQ12
SPM_A11	R8	A11	DQU4	A8	SPM_DQ15
SPM_A12	N8	A12/BC	DQU5	A3	SPM_DQ11
SPM_A13	T4	A13	DQU6	B9	SPM_DQ14
	T8	A14	DQU7	A4	SPM_DQ9
	M8	A15			
			VDD#B3	B3	+1.5V_MEM_VDDQ
SPM_BA0	M3	BA0	VDD#D10	D10	
SPM_BA1	N9	BA1	VDD#G8	G8	
SPM_BA2	M4	BA2	VDD#K3	K3	
			VDD#K9	K9	
			VDD#N2	N2	
SPM_CLKN	J8	CK	VDD#N10	N10	
R50 *100_4 SPM_CLKP	K8	CK	VDD#R2	R2	
SPM_CKE	K10	CKE	VDD#R10	R10	
			VDDQ#A2	A2	+1.5V_MEM_VDDQ
SPM_ODT	K2	ODT	VDDQ#A9	A9	
SPM_CS#	L3	CS	VDDQ#C2	C2	
SPM_RAS#	J4	RAS	VDDQ#C10	C10	
SPM_CAS#	K4	CAS	VDDQ#D3	D3	
SPM_WE#	L4	WE	VDDQ#E10	E10	
			VDDQ#F2	F2	
SPM_DQS0P	F4	DQSL	VDDQ#H3	H3	
SPM_DQS1P	C8	DQSU	VDDQ#H10	H10	
SPM_DM0	E8	DML	VSS#A10	A10	
SPM_DM1	D4	DMU	VSS#B4	B4	
			VSS#E2	E2	
			VSS#G9	G9	
SPM_DQS0N	G4	DQSL	VSS#J3	J3	
SPM_DQS1N	B8	DQSU	VSS#J9	J9	
			VSS#M2	M2	
			VSS#M10	M10	
			VSS#P2	P2	
			VSS#P10	P10	
13 SP_DDR3_RST#	T3	RESET	VSS#T2	T2	
VMA_ZQ2	L9	ZQ	VSS#T10	T10	
			VSSQ#B2	B2	
			VSSQ#B10	B10	
			VSSQ#D2	D2	
			VSSQ#D9	D9	
			VSSQ#E3	E3	
			VSSQ#E9	E9	
			VSSQ#F10	F10	
			VSSQ#G2	G2	
			VSSQ#G10	G10	
	J2	NC#J2			
	L2	NC#L2			
	J10	NC#J10			
	L10	NC#L10			

100-BALL SDRAM DDR3
H5TQ1G63AFR-14C

+1.5V_MEM_VDDQ
R51 10K/F_4
R37 240/F_4

SPM_VREF1: R33 1K/F_4, R28 1K/F_4, C38 0.1U/10V_4, C37 0.1U/10V_4 → +1.5V_MEM_VDDQ
SPM_VREF2: R59 1K/F_4, R68 1K/F_4, C53 0.1U/10V_4, C65 0.1U/10V_4 → +1.5V_MEM_VDDQ

This block is for UMA only , DIS can remove all component

U27D

SBD_MEM/DVO_I/F

PAR 4 OF 6

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)		Y17	SPM_DQS0P
			MEM_DQS0P/DVO_IDCKP(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS0N/DVO_IDCKN(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1P(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)	MEM_DQS1N(NC)		
SPM_CS#	AB13	MEM_CSb(NC)		W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM0(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)		
			IOPLLVDD18(NC)	AE23	+1.8V_IOPLLVDD18
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	+1.1V_IOPLLVDD
SPM_CLKN	W14	MEM_CKN(NC)		AD23	
			IOPLLVSS(NC)		
R371 40.2/F_4 SPM_COMPP	AE12	MEM_COMPP(NC)		AE18	SPM_VREF
R368 40.2/F_4 SPM_COMPN	AD12	MEM_COMPN(NC)	MEM_VREF(NC)		

RS880M

T14

+1.5V_MEM_VDDQ

BLM18PG181SN1D(180,1.5A) L61 +1.8V
BLM18PG181SN1D(180,1.5A) L56 +1.1V
C573 2.2U/6.3V_6
C558 2.2U/6.3V_6

R366 1K/F_4, R367 1K/F_4
C586 0.1U/10V_4, C587 0.1U/10V_4 → +1.5V_MEM_VDDQ

DIS only

40mils wdith or more +1.5V_MEM_VDDQ

+1.5V
R328 0_6
C41 1U/10V_4
C541 10U/6.3V_8
C45 10U/6.3V_8
C54 0.1U/10V_4
C40 0.1U/10V_4
C39 1U/10V_4

N85/RD2

PROJECT : LX89
Quanta Computer Inc.

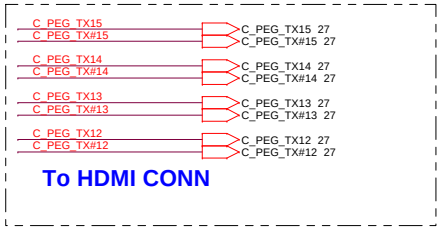
Size	Document Number	Rev
Custom	RS880-HT LINK I/F 1/5	1A
Date: Monday, September 28, 2009	Sheet 8 of 46	

UMA Remove All Cap

Swap pin for Layout

SI

Close to North Bridge



RS880 Display Port Support (muxed on GFX)

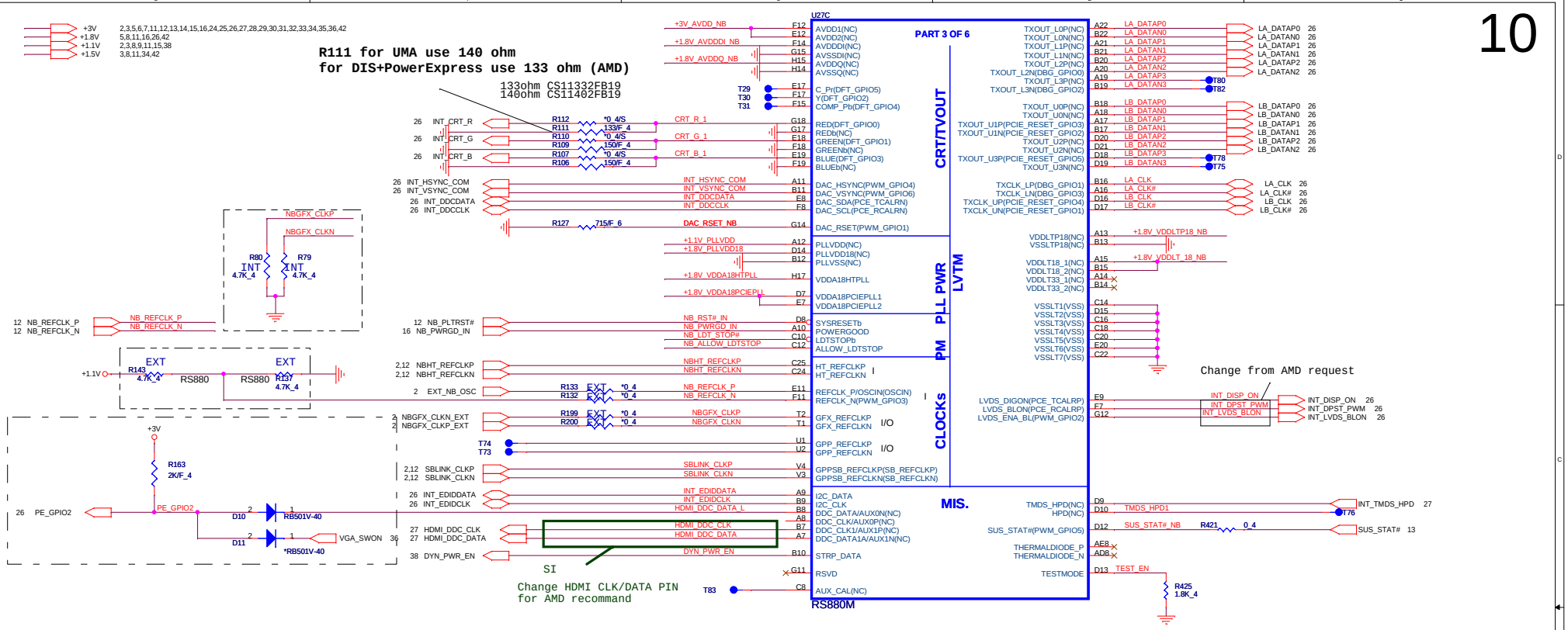
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

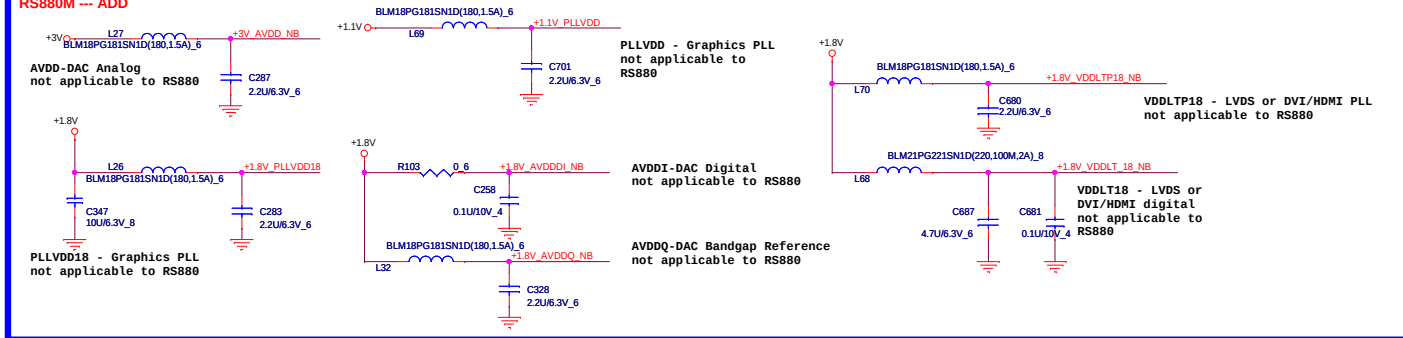
NB5/RD2

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-PCIE I/F 2/5	1A

Date: Monday, September 28, 2009 | Sheet 9 of 46





STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

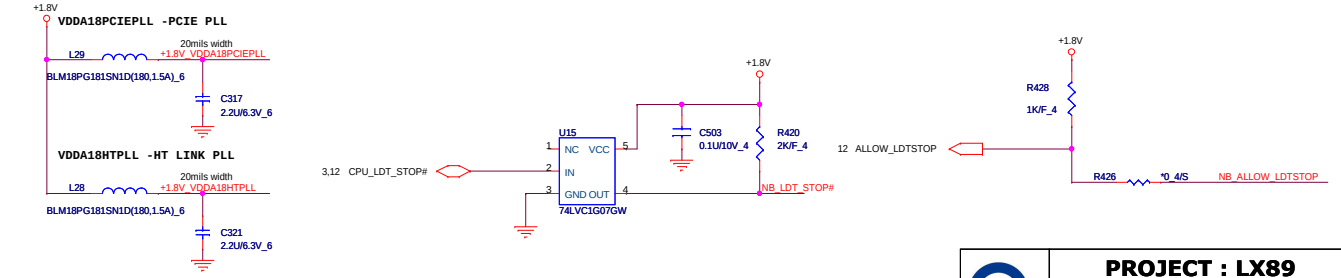
RS880M: Enables Side port memory

RS880M:INT_HSYNC_COM

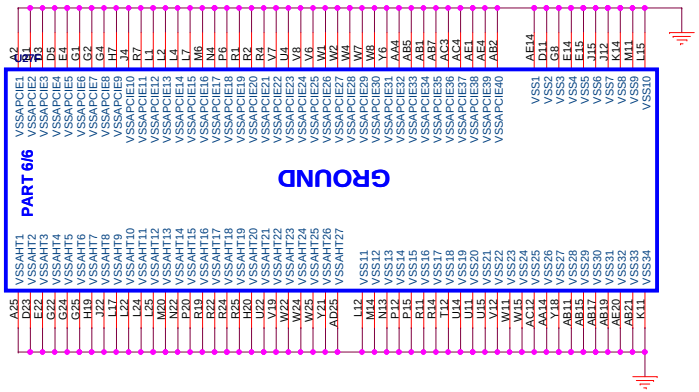
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

For extrnal EEPROM Debug only

RS880



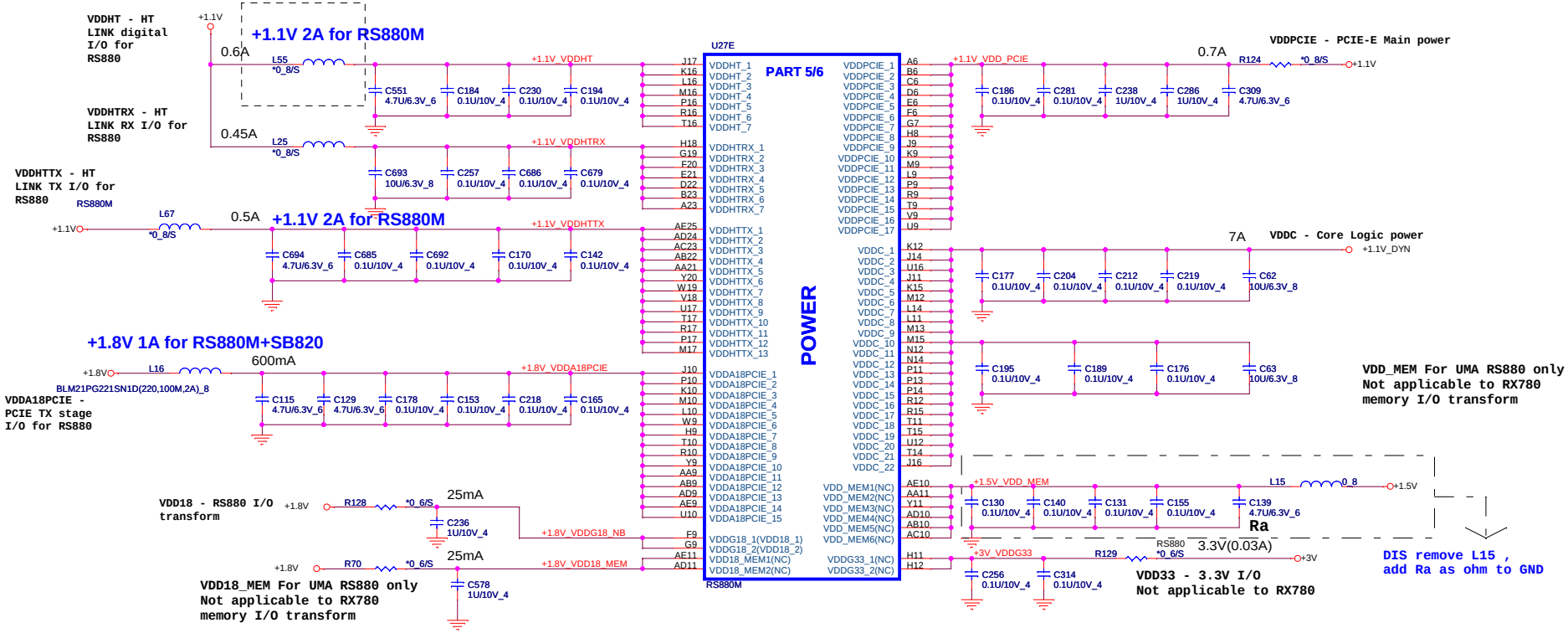
N85/RD2	PROJECT : LX89 Quanta Computer Inc.		
Size: Custom	Document Number: RS880-SYSTEM I/F 3/5		Rev: 1A
Date: Monday, September 28, 2009	Sheet 10 of 46		



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

+1.1V_DYN 38
+3V 2,3,5,6,7,10,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.1V 2,3,8,9,10,15,38
+1.5V 3,8,34,42
+1.8V 5,8,10,16,26,42



PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-POWER5/5	1A

N85/RD2

Date: Monday, September 28, 2009 Sheet 11 of 46

+1.1V_PCIE_VDDR 15
+3V_VGA 21,41
+3VS5 5,13,14,15,16,42
+3VPCU 4,6,24,33,35,36,37,38,39,40,41,42,43

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U7007

To RS880

U42A

SB800 Part 1 of 5

PCI EXPRESS INTERFACES

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

SB800 A11

SI

Add AND gate for the reset input of PCIE devices for AMD recommand

U19 TC7SH08FU

SI Change from VGA_RSTA to A_RST#_R

All the PCI bus has build-in Pull-UP/Down resistors

H=4.2 footprint: "BAT-23_2-4_2"
footprint check ok

BAT_CONN

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

NC,no install by default

+3VS5 R557 *2.2K_4 SB_TEST0
R558 *2.2K_4 SB_TEST1
R280 *2.2K_4 SB_TEST2

+3V SCL0/SDATA0 is 3V tolerance AMD datasheet define it
R223 2.2K_4 PCLK_SMB
R227 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it
R279 2.2K_4 SB_SMBCLK1
R278 2.2K_4 SB_SMBDATA1

remove pull hi (chip internal have pull hi)

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it
R483 2.2K_4 SB_SCLK2
R482 2.2K_4 SB_SDATA2

+3VS5 R535 2.2K_4 DNBSWON#

+3V R277 4.7K_4 SUS_STAT#

To Azalia

ACZ_SDOUT R563 33_4 ACZ_SDOUT_AUDIO 29
C873 *10P/50V_4

ACZ_SYNC R542 33_4 ACZ_SYNC_AUDIO 29
C504 *10P/50V_4

ACZ_BCLK R275 33_4 BIT_CLK_AUDIO 29
C496 10P/50V_4

ACZ_RST# R566 33_4 ACZ_RST#_AUDIO 29

ACZ_SDIN0 ACZ_SDIN0 29

+3VSUS 28,33,34,35,41,42
+3V 2,3,5,6,7,10,11,12,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+3VS5 5,12,14,15,16,42

SB JTAG

CN32 +3VSUS C877 10P/50V_4
1 SB_JTAG_TCK
2 SB_JTAG_TDO
3 SB_JTAG_TDI
4 SB_TEST1
5
6 SB_JTAG_RST#
7
8
*S/W JTAG DEBUG

U42D SB800 Part 4 of 5

14 MEM_GEVEN# MEM_GEVEN# J2
T130 RI# K1
T125 SPI_CS3# D3
36 SUSB# SUSB# F1
36 SUSC# SUSC# H1
36 DNBSWON# DNBSWON# F2
16 SB_PWRGD_IN SB_PWRGD_IN H5
10 SUS_STAT# SUS_STAT# G6
SB_TEST0 B3
SB_TEST1 C4
SB_TEST2 F6
36 GATEA20 GATEA20 AD21
36 RCIN# RCIN# AE21
T126 K2
36 KBSMI# KBSMI# J29
36 SCI# SCI# H2
T127 SYS_RST# J1
32,34 PCIE_WAKE# H6
F3
3 CPU_THERMTRIP# CPU_THERMTRIP# J6
16 WD_PWRGD WD_PWRGD AC19
C497 100P/50V_4
36 RSMRST# RSMRST# G1
T42 AD19
T47 AA16
32,36 LAN_DISABLE# R234 *0_4 LAN_DISABLE#_SB AB21
T44 AC18
33 ACCLED_EN AE20
T43 AE19
29 ACZ_SPKR ACZ_SPKR AF19
2,6,7,30,34 PCLK_SMB PCLK_SMB AD22
2,6,7,30,34 PDAT_SMB PDAT_SMB AE22
SB_SMBCLK1 F5
SB_SMBDATA1 F4
T113 AH21
T45 AB18
T129 E1
T114 AJ21
8 SP_DDR3_RST# H4
T54 D5
T51 D7
T53 G5
T52 K3
2 EXT_SB_OSC EXT_SB_OSC AA20

5 PM_THERM# R554 *0_4 SMBALERT#_1
+3VS5 R556 10K/F_4
SB_JTAG_TDO H3
SB_JTAG_TCK D1
SB_JTAG_TDI E4
SB_JTAG_RST# D4
E8
F7
E7
F8

R276 *10K/F_4 ACZ_BCLK M3
16 ACZ_SDOUT ACZ_SDOUT N1
R538 *10K/F_4 ACZ_SDIN0 L2
R541 *10K/F_4 ACZ_SDIN1 M2
R562 *10K/F_4 ACZ_SDIN2_R M1
R540 *10K/F_4 ACZ_SDIN3_R M4
ACZ_SYNC N2
ACZ_RST# P2
HD audio interface is 3.3S5 voltage

T1 GBE_COL
T4 GBE_CRS
L6 GBE_MDCK
L5 GBE_MDIO
T9 GBE_RXCLK
U1 GBE_RXD3
U3 GBE_RXD2
T2 GBE_RXD1
U2 GBE_RXD0
T5 GBE_RXCTL/RXDV
V5 GBE_RXERR
P5 GBE_TXCLK
M5 GBE_TXD3
P9 GBE_TXD2
T7 GBE_TXD1
P7 GBE_TXD0
M7 GBE_TXCTL/TXEN
P4 GBE_PHY_PD
M9 GBE_PHY_RST#
V7 GBE_PHY_INTR

T39 E23 PS2_DAT/SDA4/GPIO187
T96 E24 PS2_CLK/SCL4/GPIO188
F21 SPI_CS2#/GBE_STAT2/GPIO166
T97 G29 FC_RST#/GPIO160
D27 PS2KB_DAT/GPIO189
F28 PS2KB_CLK/GPIO190
E29 PS2M_DAT/GPIO191
E27 PS2M_CLK/GPIO192

SB800 A11

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
GPIO

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

GBE LAN

EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC A10 CLK_48M_USB CLK_48M_USB 2
USB_RCOMP G19 USB_RCOMP_SB R238 11.8K/F_6
CLK_48M_USB C844 *2.2P/50V_4 for EMI

USB_FSD1P/GPIO186 J10 USBP15+ 33
USB_FSD1N H11 USBP15- 33 BLUETOOTH
USB_FSD0P/GPIO185 H9 USBP14+ 33
USB_FSD0N J8 USBP14- 33 Finger Print

USB_HSD13P B12 T121
USB_HSD13N A12 T120
USB_HSD12P F11 USBP12+ 33
USB_HSD12N E11 USBP12- 33 USB Connector 15.6"
USB_HSD11P E14 USBP11+ 28
USB_HSD11N E12 USBP11- 28 Card reader
USB_HSD10P J12 USBP10+ 34
USB_HSD10N J14 USBP10- 34 WLAN Min-Card
USB_HSD9P A13 T118
USB_HSD9N B13 T119
USB_HSD8P D13
USB_HSD8N C13
USB_HSD7P G12 USBP7+ 34
USB_HSD7N G14 USBP7- 34 USB Connector
USB_HSD6P G16 USBP6+ 33
USB_HSD6N G18 USBP6- 33 USB Connector 17.3" and 15"6 co-layout
USB_HSD5P D16 USBP5+ 33
USB_HSD5N C16 USBP5- 33 USB Connector 17.3"
USB_HSD4P B14 T117
USB_HSD4N A14 T116
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16 USBP2+ 24
USB_HSD2N J18 USBP2- 24 Camera USB
USB_HSD1P B17 USBP1+ 24
USB_HSD1N A17 USBP1- 24 Digitizer Connector
USB_HSD0P A16 USBP0+ 34
USB_HSD0N B16 USBP0- 34 USB & ESATA Combo Connector
USB 2.0

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3
SDA3_LV/GPIO196 E26 5159_RST_R# T36 5159_RST_R# 28
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 SB_GPIO199 SB_GPIO199 16
EC_PWM3/EC_TIMER3/GPIO200 E21 SB_GPIO200 SB_GPIO200 16
SPI/LPC define

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22
EMBEDDED CTRL

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SATA1 HDD

SATA ODD

SATA2 HDD

E-SATA

U42B

SB800

Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB800 A11

+1.1V_AVDD_SATA 15
+3V 2,3,5,6,7,10,11,12,13,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+3VS5 5,12,13,15,16,42

IF USE,power need ready

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

SI
Remove Y6 for AMD recommand

ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX8 Park
0	0	1	0	0	LX9 Park
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	

PROJECT : LX89
Quanta Computer Inc.

N85/RD2

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	1A

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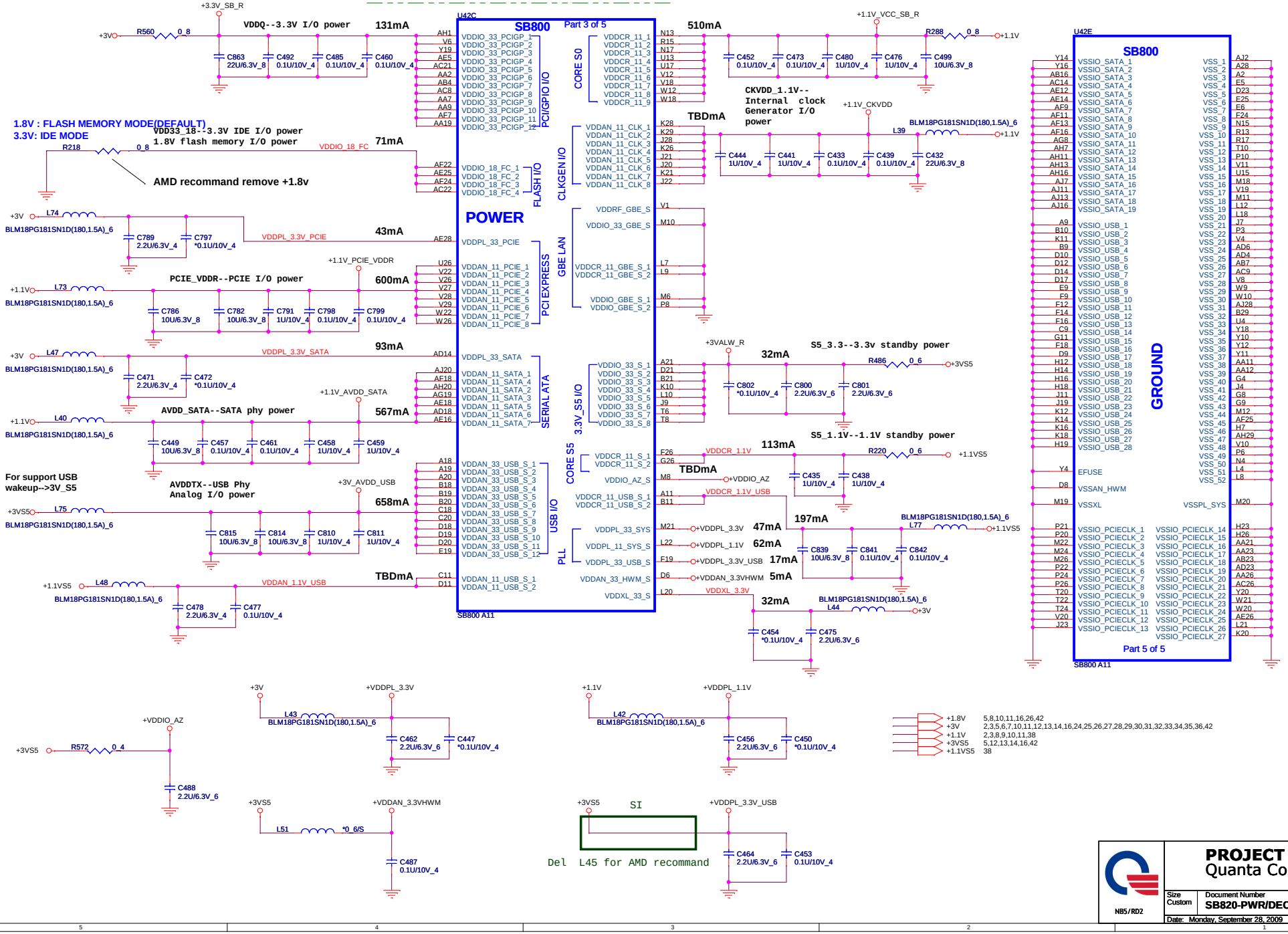
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power



+1.8V	5,8,10,11,16,26,42
+3V	2,3,5,6,7,10,11,12,13,14,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.1V	2,3,8,9,10,11,38
+3VS5	5,12,13,14,16,42
+1.1VS5	38

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PWR/DECOUPLING 4/4	1A

N85/RD2

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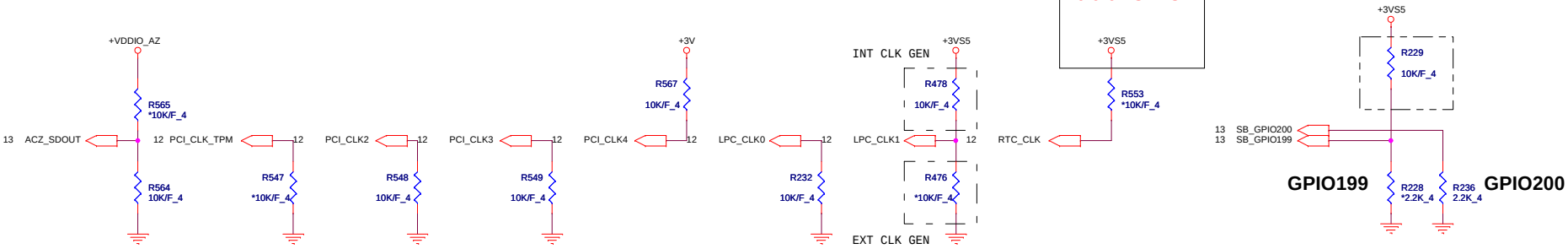
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull Hi 10K , confirm AMD ward this pull Hi not need

+VDDIO_AZ 15
+3V 2,3,5,6,7,10,11,12,13,14,15,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+3VS5 5,12,13,14,15,42
+1.8V 5,8,10,11,26,42

REQUIRED STRAPS

It must ready refore RSMRST#



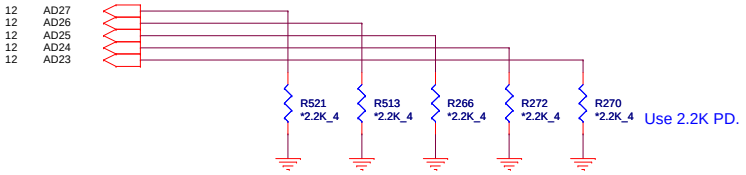
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

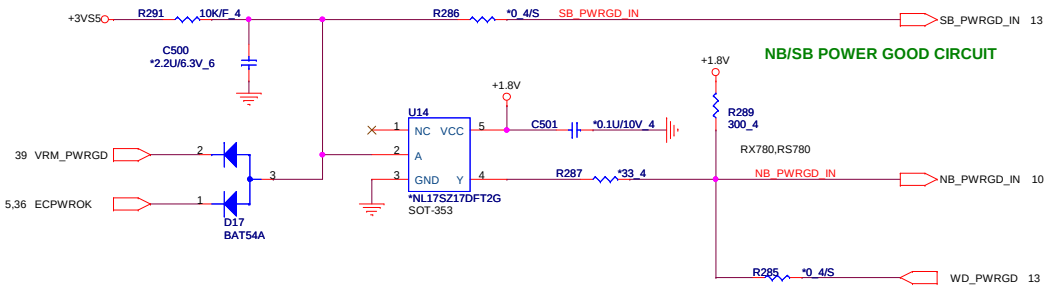
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	1A

N85/RD2

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2.5GT/s bit rate

U28A

PCI EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	C_PEG_RXP0 C231 .1U/10V_4
9	PEG_TX#0	PEG_TX#0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	C_PEG_RXN0 C220 .1U/10V_4
9	PEG_TX1	PEG_TX1	Y35	PCIE_RX1P	PCIE_TX1P	W33	C_PEG_RXP1 C235 .1U/10V_4
9	PEG_TX#1	PEG_TX#1	W36	PCIE_RX1N	PCIE_TX1N	W32	C_PEG_RXN1 C246 .1U/10V_4
9	PEG_TX2	PEG_TX2	W38	PCIE_RX2P	PCIE_TX2P	U33	C_PEG_RXP2 C247 .1U/10V_4
9	PEG_TX#2	PEG_TX#2	V37	PCIE_RX2N	PCIE_TX2N	U32	C_PEG_RXN2 C254 .1U/10V_4
9	PEG_TX3	PEG_TX3	V35	PCIE_RX3P	PCIE_TX3P	U30	C_PEG_RXP3 C213 .1U/10V_4
9	PEG_TX#3	PEG_TX#3	U36	PCIE_RX3N	PCIE_TX3N	U29	C_PEG_RXN3 C205 .1U/10V_4
9	PEG_TX4	PEG_TX4	U38	PCIE_RX4P	PCIE_TX4P	T33	C_PEG_RXP4 C262 .1U/10V_4
9	PEG_TX#4	PEG_TX#4	T37	PCIE_RX4N	PCIE_TX4N	T32	C_PEG_RXN4 C278 .1U/10V_4
9	PEG_TX5	PEG_TX5	T35	PCIE_RX5P	PCIE_TX5P	T30	C_PEG_RXP5 C261 .1U/10V_4
9	PEG_TX#5	PEG_TX#5	R36	PCIE_RX5N	PCIE_TX5N	T29	C_PEG_RXN5 C255 .1U/10V_4
9	PEG_TX6	PEG_TX6	R38	PCIE_RX6P	PCIE_TX6P	P33	C_PEG_RXP6 C280 .1U/10V_4
9	PEG_TX#6	PEG_TX#6	P37	PCIE_RX6N	PCIE_TX6N	P32	C_PEG_RXN6 C285 .1U/10V_4
9	PEG_TX7	PEG_TX7	P35	PCIE_RX7P	PCIE_TX7P	P30	C_PEG_RXP7 C291 .1U/10V_4
9	PEG_TX#7	PEG_TX#7	N36	PCIE_RX7N	PCIE_TX7N	P29	C_PEG_RXN7 C308 .1U/10V_4
9	PEG_TX8	PEG_TX8	N38	PCIE_RX8P	PCIE_TX8P	N33	C_PEG_RXP8 C316 0.1U/10V_4
9	PEG_TX#8	PEG_TX#8	M37	PCIE_RX8N	PCIE_TX8N	N32	C_PEG_RXN8 C312 0.1U/10V_4
9	PEG_TX9	PEG_TX9	M35	PCIE_RX9P	PCIE_TX9P	N30	C_PEG_RXP9 C295 0.1U/10V_4
9	PEG_TX#9	PEG_TX#9	L36	PCIE_RX9N	PCIE_TX9N	N29	C_PEG_RXN9 C294 0.1U/10V_4
9	PEG_TX10	PEG_TX10	L38	PCIE_RX10P	PCIE_TX10P	L33	C_PEG_RXP10 C293 0.1U/10V_4
9	PEG_TX#10	PEG_TX#10	K37	PCIE_RX10N	PCIE_TX10N	L32	C_PEG_RXN10 C292 0.1U/10V_4
9	PEG_TX11	PEG_TX11	K35	PCIE_RX11P	PCIE_TX11P	L30	C_PEG_RXP11 C322 0.1U/10V_4
9	PEG_TX#11	PEG_TX#11	J36	PCIE_RX11N	PCIE_TX11N	L29	C_PEG_RXN11 C327 0.1U/10V_4
9	PEG_TX12	PEG_TX12	J38	PCIE_RX12P	PCIE_TX12P	K33	C_PEG_RXP12 C320 0.1U/10V_4
9	PEG_TX#12	PEG_TX#12	H37	PCIE_RX12N	PCIE_TX12N	K32	C_PEG_RXN12 C325 0.1U/10V_4
9	PEG_TX13	PEG_TX13	H35	PCIE_RX13P	PCIE_TX13P	J33	C_PEG_RXP13 C338 0.1U/10V_4
9	PEG_TX#13	PEG_TX#13	G36	PCIE_RX13N	PCIE_TX13N	J32	C_PEG_RXN13 C343 0.1U/10V_4
9	PEG_TX14	PEG_TX14	G38	PCIE_RX14P	PCIE_TX14P	K30	C_PEG_RXP14 C353 0.1U/10V_4
9	PEG_TX#14	PEG_TX#14	F37	PCIE_RX14N	PCIE_TX14N	K29	C_PEG_RXN14 C351 0.1U/10V_4
9	PEG_TX15	PEG_TX15	F35	PCIE_RX15P	PCIE_TX15P	H33	C_PEG_RXP15 C342 0.1U/10V_4
9	PEG_TX#15	PEG_TX#15	E37	PCIE_RX15N	PCIE_TX15N	H32	C_PEG_RXN15 C345 0.1U/10V_4

CLOCK

2,12	EXT_GFX_CLKP	EXT_GFX_CLKP	AB35 PCIE_REFCLKP
2,12	EXT_GFX_CLKN	EXT_GFX_CLKN	AA36 PCIE_REFCLKN

	10K/F_4 R90	AJ21	NC#1
		AK21	NC#2
		AH16	PWRGOOD
12	PCIE_RST#	AA30	PERSTB

CALIBRATION

PCIE_CALRP	Y30	M72_PCIE_CALRP	R347 1.27K/F_4
PCIE_CALRN	Y29	M72_PCIE_CALRN	R105 2K/F_4 +1.0V_VGA

M97_m2

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

U28H

DP C/D POWER

+1.8V_DPC_VDD18	AP20	DPC_VDD18#1
	AP21	DPC_VDD18#2
+1.0V_DPC_VDD10	AP13	DPC_VDD10#1
	AT13	DPC_VDD10#2
	AN17	DPC_VSSR#1
	AP16	DPC_VSSR#2
	AP17	DPC_VSSR#3
	AW14	DPC_VSSR#4
	AW16	DPC_VSSR#5
+1.8V_DPC_VDD18	AP22	DPD_VDD18#1
	AP23	DPD_VDD18#2
+1.0V_DPC_VDD10	AP14	DPD_VDD10#1
	AP15	DPD_VDD10#2
	AN19	DPD_VSSR#1
	AP18	DPD_VSSR#2
	AW20	DPD_VSSR#3
	AW22	DPD_VSSR#4
		DPD_VSSR#5
R378 150/F_4	AW18	DPCD_CALR

DP A/B POWER

	AN24	DPA_VDD18#1
+1.8V_DPA_VDD18	AP24	DPA_VDD18#2
+1.0V_VGA	AP31	DPA_VDD10#1
	AP32	DPA_VDD10#2
	AN27	DPA_VSSR#1
	AP27	DPA_VSSR#2
	AP28	DPA_VSSR#3
	AW24	DPA_VSSR#4
	AW26	DPA_VSSR#5
	AP25	DPB_VDD18#1
+1.8V_DPA_VDD18	AP26	DPB_VDD18#2
(DPA/B_VDD10 : 1.0V@110mA) +1.0V_VGA	AN33	DPB_VDD10#1
+1.0V_DPA_VDD10 L12 HCB1608KF-181T15_6	AP33	DPB_VDD10#2
C100 10U/6.3V_8 C132 1U/6.3V_4 C120 .1U/10V_4	AN29	DPB_VSSR#1
	AP29	DPB_VSSR#2
	AP30	DPB_VSSR#3
	AW30	DPB_VSSR#4
	AW32	DPB_VSSR#5
R372 150/F_4	AW28	DPAB_CALR

DP E/F POWER

+1.8V_DPE_VDD18	AH34	DPE_VDD18#1
	AJ34	DPE_VDD18#2
+1.0V_DPE_VDD10	AL33	DPE_VDD10#1
	AM33	DPE_VDD10#2
	AN34	DPE_VSSR#1
	AP39	DPE_VSSR#2
	AR39	DPE_VSSR#3
	AU37	DPE_VSSR#4
+1.8V_DPE_VDD18	AF34	DPF_VDD18#1
	AG34	DPF_VDD18#2
+1.0V_DPE_VDD10	AK33	DPF_VDD10#1
	AK34	DPF_VDD10#2
	AF39	DPF_VSSR#1
	AH39	DPF_VSSR#2
	AK39	DPF_VSSR#3
	AL34	DPF_VSSR#4
	AM34	DPF_VSSR#5
R385 150/F_4 DPEF_CALR	AM39	DPEF_CALR

DP PLL POWER

	AU28	DPA_PVDD
	AV27	DPA_PVSS
(DPA/B_PVDD : 1.8V@20mA+20mA) +1.8V_VGA	AV29	DPB_PVDD
+1.8V_DPB_PVDD L58 HCB1608KF-181T15_6	AR28	DPB_PVSS
C594 10U/6.3V_8 C595 1U/6.3V_4 C596 .1U/10V_4	AU18	DPC_PVDD
	AV17	DPC_PVSS
(DPC/D_PVDD:1.8V@20mA+20mA) +1.8V_VGA	AV19	DPD_PVDD
+1.8V_DPC_PVDD	AR18	DPD_PVSS
	AM37	DPE_PVDD
	AN38	DPE_PVSS
(DPE/F_PVDD1.8V@20mA+20mA) +1.8V_VGA	AL38	NC_DPF_PVDD
+1.8V_DPE_PVDD L64 HCB1608KF-181T15_6	AM35	NC_DPF_PVSS
C621 10U/6.3V_8 C618 .1U/10V_4 C619 .1U/10V_4		

M97_m2

(VDD10 M97 1.0V)

(DPE/F_VDD10 : 1.0V@120mA+120mA) +1.0V_VGA
+1.0V_DPE_VDD10 L19 HCB1608KF-181T15_6
C145 10U/6.3V_8 C151 1U/6.3V_4 C141 .1U/10V_4

(DPC/D_VDD10 : 1.0V@110mA+110mA) +1.0V_VGA
+1.0V_DPC_VDD10

(DPE/F_VDD18 : 1.8V@200mA+200mA) +1.8V_VGA
+1.8V_DPE_VDD18 L20 HCB1608KF-181T15_6
C157 10U/6.3V_8 C160 1U/6.3V_4 C159 .1U/10V_4

(DPA_VDD18 : 1.8V@130mA) +1.8V_VGA
+1.8V_DPA_VDD18 L14 HCB1608KF-181T15_6
C98 10U/6.3V_8 C123 1U/6.3V_4 C124 .1U/10V_4

(DPC/D_VDD18 : 1.8V@130mA+130mA) +1.8V_VGA
+1.8V_DPC_VDD18

19,21,40 +1.0V_VGA
19,21,41 +1.8V_VGA

NB5/RD2

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI Park/Madison (PCIE I/F) 1/5	1A

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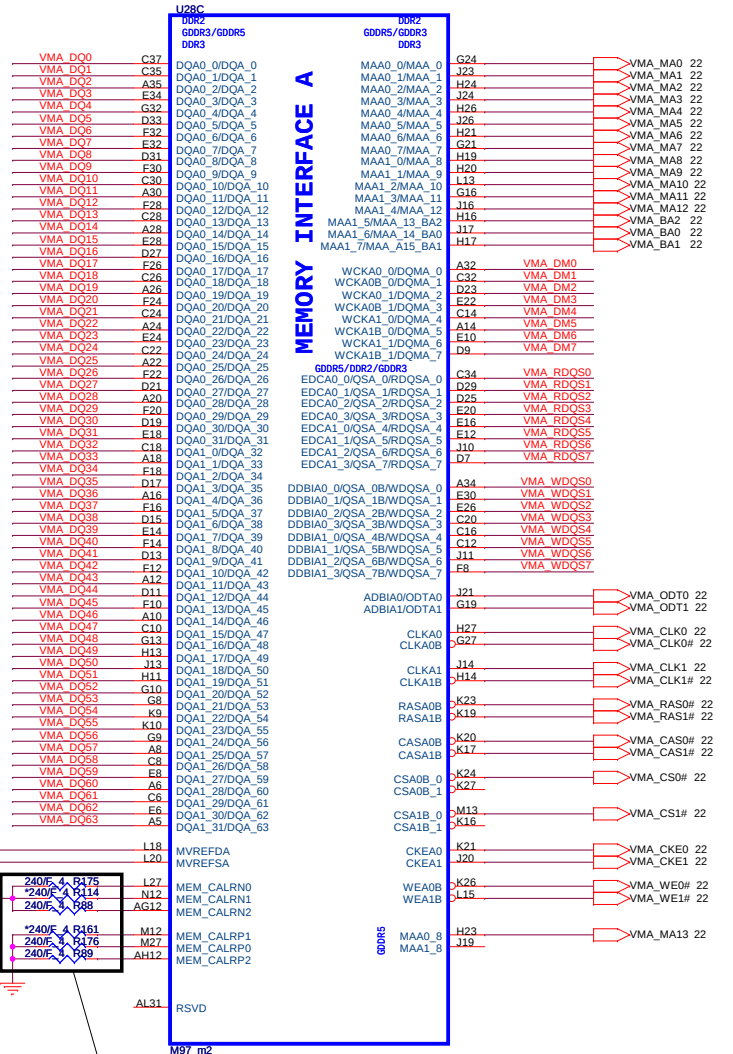
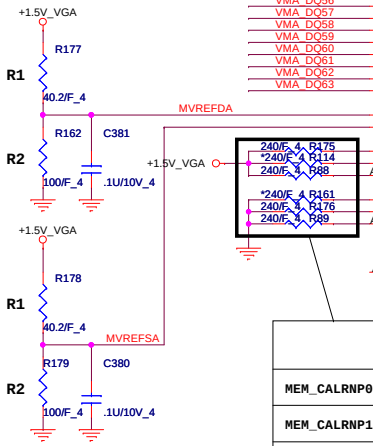
Park, M92M Use Channel B Memory Interface Only

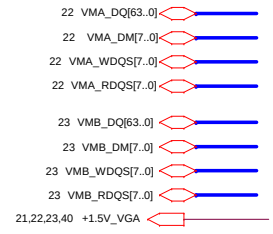


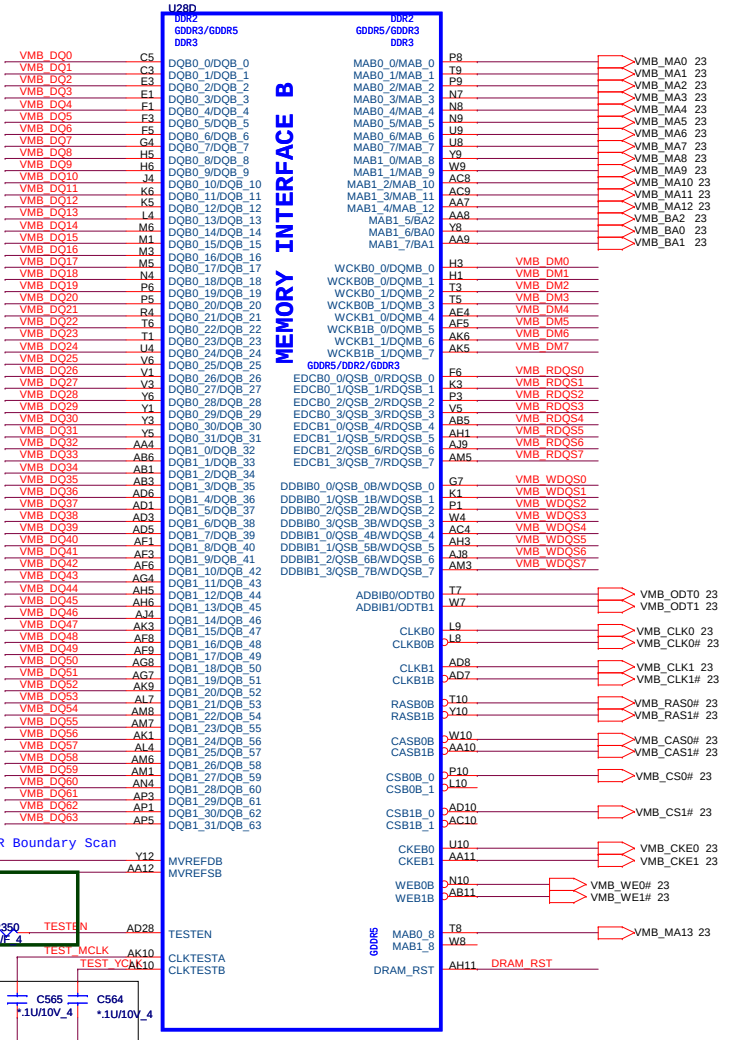


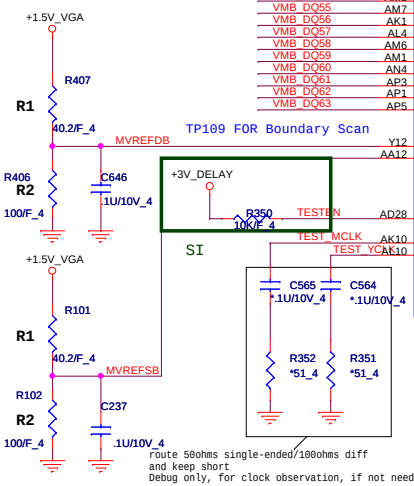
	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

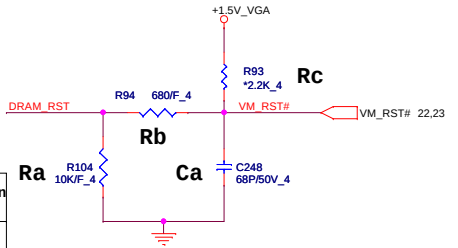
	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
R1	40.2R	40.2R	40.2R
R2	100R	100R	100R







Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF



PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI Park/Madison (MEM I/F) 2/5	1A

Date: Monday, September 28, 2009 | Sheet 18 of 46

NB5/RD2

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0001	Hinyx	64*16-800MHZ	H5TQ1G63BFR-12C
0010			Reserved
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

Memory ID

NC on PARK

NC on PARK

SI

Add Y9 to slove Park JTAG test block intermittently fails to initialize correctly issue

DisplayPort F Configuration

DisplayPort E Configuration
For Single-link panel

DP Channel D is NC on PARK

SI Del R85,R86,R91 for Layout concern

DIS

GenericF/G is NC on PARK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Remove GND SI

DDCxx_AUX4x is NC on PARK

DDCxx_AUX7x is NC on M9x and PARK

DPLL_VDCC M97 1.0V

(1.8V@75mA DPLL_PVDD)

(1.0V@125mA DPLL_VDDC)

(1.8V@20mA TSVDD)

(DAC1_AVDD: 1.8V@70mA)

(DAC2_A2VDDQ: 1.8V@2mA)

(DAC1_VDD1DI:1.8V@100mA)

(DAC2_A2VDD:3.3V@130mA)

SI

Del L13,C94,C95 for +VDDD2 combine with +VDDD1

SI

Del L9 A2VDD can be powered by VDDR3 directly without filter

Thermal Sensor

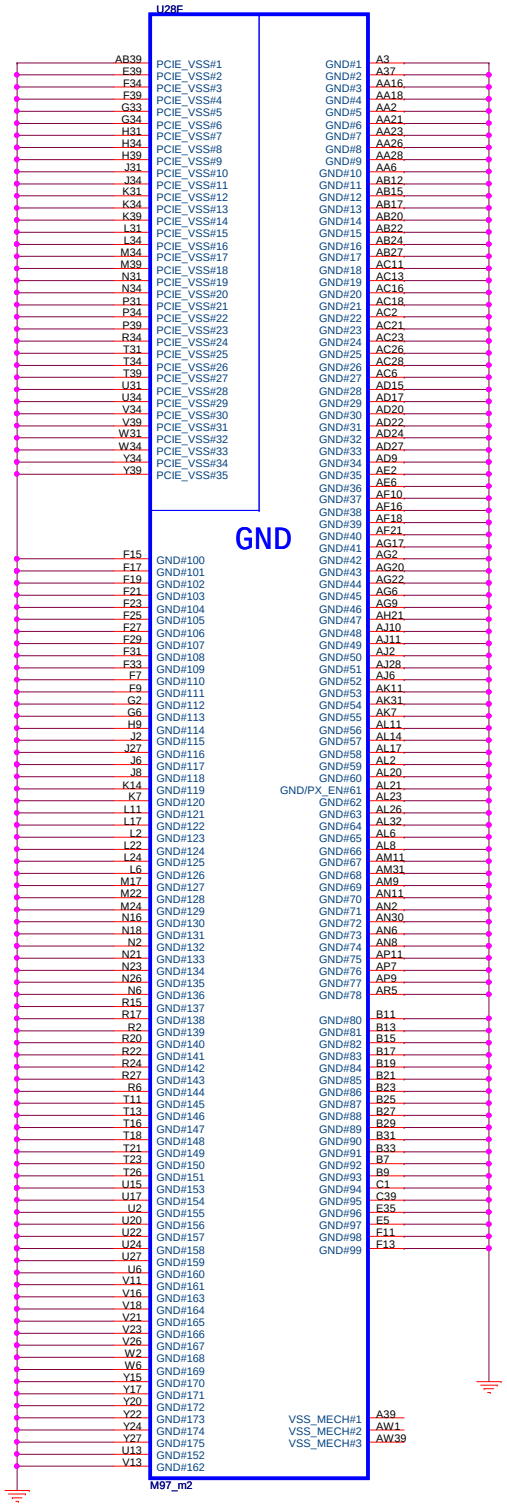
I2C ADDRESS: 9AH

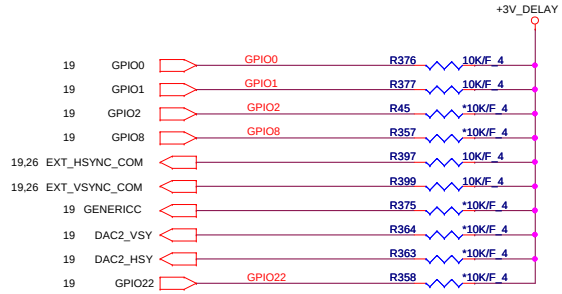
w/s 10 / 10

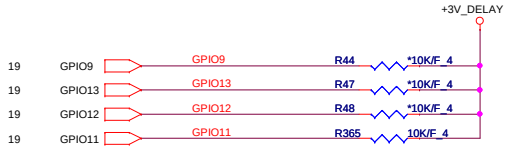
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI Park/Madison (DISPLAY) 3/5	1A
Date: Monday, September 28, 2009	Sheet 19 of 46	

N85/RD2







Memory Aperture size fix 256M

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

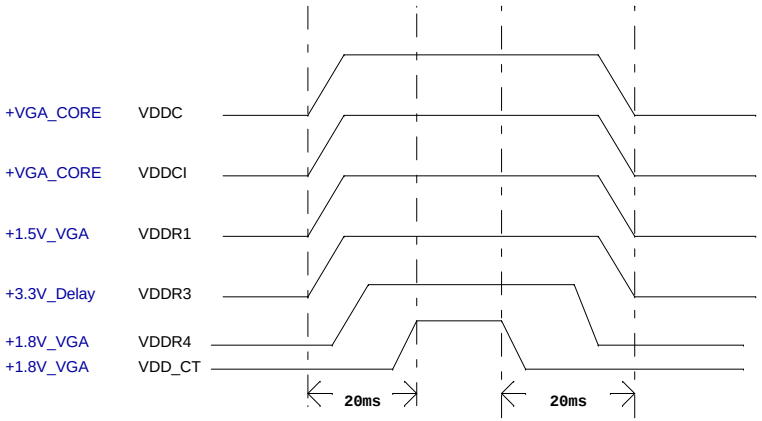
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Power Up/Down Sequence



18,19,21,26,27 +3V_DELAY

NB5/RD2

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI Park/Madison(GND&Str&Ther)4/5	1A
Date: Monday, September 28, 2009	Sheet 20 of 46	

+1.5V_VGA

(VDDR1: 1.5V@7.5A)

C697 2.2U/10V_4, C627 2.2U/10V_4, C737 2.2U/10V_4, C185 1U/6.3V_4, C722 2.2U/10V_4, C378 2.2U/10V_4, C724 2.2U/10V_4

C374 2.2U/10V_4, C126 2.2U/10V_4, C645 2.2U/10V_4, C726 2.2U/10V_4

C770 10U/6.3V_8, C712 10U/6.3V_8, C768 10U/6.3V_8, C634 22U/6.3V_8, C650 22U/6.3V_8, C769 22U/6.3V_8

U28E

MEM I/O

AC7 VDDR1#1, AD11 VDDR1#2, AF7 VDDR1#3, AG10 VDDR1#4, AJ7 VDDR1#5, AK8 VDDR1#6, AL9 VDDR1#7, G11 VDDR1#8, G14 VDDR1#9, G17 VDDR1#10, G20 VDDR1#11, G23 VDDR1#12, G26 VDDR1#13, G29 VDDR1#14, H10 VDDR1#15, J7 VDDR1#16, J9 VDDR1#17, K11 VDDR1#18, K13 VDDR1#19, K8 VDDR1#20, L12 VDDR1#21, L16 VDDR1#22, L21 VDDR1#23, L23 VDDR1#24, L26 VDDR1#25, L7 VDDR1#26, M11 VDDR1#27, N11 VDDR1#28, P7 VDDR1#29, R11 VDDR1#30, U11 VDDR1#31, U7 VDDR1#32, Y11 VDDR1#33, Y7 VDDR1#34

LEVEL TRANSLATION

VDD_CT#1, VDD_CT#2, VDD_CT#3, VDD_CT#4

I/O

VDDR3#1, VDDR3#2, VDDR3#3, VDDR3#4

VDDR4#4, VDDR4#5, VDDR4#7, VDDR4#8

VDDR4#1, VDDR4#2, VDDR4#3, VDDR4#6

NC_VDDRHA, NC_VSSRHA

NC_VDDRHB, NC_VSSRHB

PLL

PCIE_PVDD

MPV18#1, MPV18#2

SPV18

SPV10

SPVSS

VOLTAGE SENESE

FB_VDDC

FB_VDDCI

FB_GND

POWER

PCIE

PCIE_VDDR#1 AA31, PCIE_VDDR#2 AA32, PCIE_VDDR#3 AA33, PCIE_VDDR#4 AA34, PCIE_VDDR#5 V28, PCIE_VDDR#6 W29, PCIE_VDDR#7 W30, PCIE_VDDR#8 Y31

PCIE_VDDC#1 G30, PCIE_VDDC#2 G31, PCIE_VDDC#3 H29, PCIE_VDDC#4 H30, PCIE_VDDC#5 J29, PCIE_VDDC#6 J30, PCIE_VDDC#7 L28, PCIE_VDDC#8 M28, PCIE_VDDC#9 N28, PCIE_VDDC#10 R28, PCIE_VDDC#11 T28, PCIE_VDDC#12 U28

CORE

VDDC#1 AA15, VDDC#2 AA17, VDDC#3 AA20, VDDC#4 AA22, VDDC#5 AA24, VDDC#6 AA27, VDDC#7 AB16, VDDC#8 AB18, VDDC#9 AB21, VDDC#10 AB23, VDDC#11 AB26, VDDC#12 AB28, VDDC#13 AC17, VDDC#14 AC20, VDDC#15 AC22, VDDC#16 AC24, VDDC#17 AC27, VDDC#18 AD18, VDDC#19 AD21, VDDC#20 AD23, VDDC#21 AD26, VDDC#22 AE17, VDDC#23 AE20, VDDC#24 AE22, VDDC#25 AG16, VDDC#26 AG18, VDDC#27 AG21, VDDC#28 AH22, VDDC#29 AH27, VDDC#30 AH28, VDDC#31 M26, VDDC#32 N24, VDDC#33 N27, VDDC#34 R18, VDDC#35 R21, VDDC#36 R23, VDDC#37 R26, VDDC#38 T17, VDDC#39 T20, VDDC#40 T22, VDDC#41 T24, VDDC#42 T27, VDDC#43 U16, VDDC#44 U18, VDDC#45 U21, VDDC#46 U23, VDDC#47 U26, VDDC#48 V17, VDDC#49 V20, VDDC#50 V22, VDDC#51 V24, VDDC#52 V27, VDDC#53 Y16, VDDC#54 Y18, VDDC#55 Y21, VDDC#56 Y23, VDDC#57 Y26, VDDC#58 Y28

ISOLATED CORE I/O

VDDCI#1 AA13, VDDCI#2 AB13, VDDCI#3 AC12, VDDCI#4 AC15, VDDCI#5 AD13, VDDCI#6 AD16, VDDCI#7 M15, VDDCI#8 M16, VDDCI#9 M18, VDDCI#10 M23, VDDCI#11 N13, VDDCI#12 N15, VDDCI#13 N17, VDDCI#14 N20, VDDCI#15 N22, VDDCI#16 R12, VDDCI#17 R13, VDDCI#18 R16, VDDCI#19 T12, VDDCI#20 T15, VDDCI#21 V15, VDDCI#22 Y13

M97_m2

+1.8V_PCIE_VDDR

(1.8V@504mA PCIE_VDDR)

+1.8V_VGA

L17 HCB1608KF-181T15_6

C119 1U/6.3V_4, C118 1U/6.3V_4, C121 10U/6.3V_8

(1.0V@1920mA PCIE_VDDC)

+1.0V_VGA

C311 .1U/10V_4, C270 1U/6.3V_4, C282 2.2U/6.3V_4, C297 2.2U/6.3V_4, C74 10U/6.3V_8

+VGA_CORE

C222 2.2U/10V_4, C288 2.2U/10V_4, C277 2.2U/10V_4, C188 2.2U/10V_4, C275 2.2U/10V_4, C289 2.2U/10V_4, C273 2.2U/10V_4, C226 2.2U/10V_4, C198 2.2U/10V_4, C227 2.2U/10V_4

C224 2.2U/10V_4, C274 2.2U/10V_4, C259 2.2U/10V_4, C290 2.2U/10V_4, C276 2.2U/10V_4, C272 2.2U/10V_4, C225 2.2U/10V_4, C229 2.2U/10V_4, C223 2.2U/10V_4

C249 10U/6.3V_6S, C250 22U/6.3V_8, C192 10U/6.3V_6S, C556 330U_2.5V_3528, C239 10U/6.3V_6S, C252 22U/6.3V_8, C296 10U/6.3V_6S, C228 10U/6.3V_6S, C571 22U/6.3V_8, C271 10U/6.3V_6S

+1.8V_VGA

L62 HCB1608KF-181T15_6

(1.8V@110mA VDD_CT)

+1.8V_VDDC_CT

C604 10U/6.3V_8, C608 1U/6.3V_4, C606 .1U/10V_4

L24 HCB1608KF-181T15_6

+VDDR4

C203 10U/6.3V_8, C201 1U/6.3V_4, C200 .1U/10V_4

+3V_DELAY

(3.3V@60mA VDDR3)

C190 10U/6.3V_8, C187 1U/6.3V_4

(VDDR4 : 1.8V@190mA)

L71 HCB1608KF-181T15_6

+MPV18

C730 10U/6.3V_8, C398 1U/6.3V_4, C390 .1U/10V_4

(1.8V@75mA SPV18)

(Park: 1.8V@75mA +MPV18)

(M97, Broadway and Madison: 1.8V@150mA +MPV18)

L60 HCB1608KF-181T15_6

+SPV18

C577 10U/6.3V_8, C590 1U/6.3V_4, C598 .1U/10V_4

L63 HCB1608KF-181T15_6

(1.8V@40mA PCIE_PVDD)

+PCIE_PVDD

C626 10U/6.3V_8, C631 1U/6.3V_4, C633 1U/6.3V_4

(SPV10 :1.0V@120mA)

+1.0V_VGA

L59 HCB1608KF-181T15_6

+SPV10

C588 10U/6.3V_8, C593 1U/6.3V_4, C597 .1U/10V_4

Add FB Circuit SI-1 Stage

For Madison and Park, VDDCI and VDDC can share one common regulator

(GDDR3/DDR3 1.12V@4A VDDCI)

(GDDR5 1.12V@16A VDDCI)

+VGA_CORE

VDDCI

L18

BLM18SG121TN1D(120,100M,3A)_8

C221 2.2U/6.3V_4, C305 2.2U/6.3V_4, C306 2.2U/6.3V_4

C307 1U/6.3V_4, C251 2.2U/6.3V_4

C253 .1U/10V_4

C279 22U/6.3V_8, C109 22U/6.3V_8, C217 22U/6.3V_8, C112 330U_2.5V_3528, C110 22U/6.3V_8

12,41 +3V_VGA
17,19,40 +1.0V_VGA
41 +VGA_CORE
18,22,23,40 +1.5V_VGA
17,19,41 +1.8V_VGA
18,19,20,26,27 +3V_DELAY

Gated 3.3V 60mA by VDDC

+3V_VGA

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

R470 0_8

Q33 *AO3409

+3V_DELAY

R468 *100K/F_4

D25 *CH501H-40PT L-F

Q32 *2N7002E

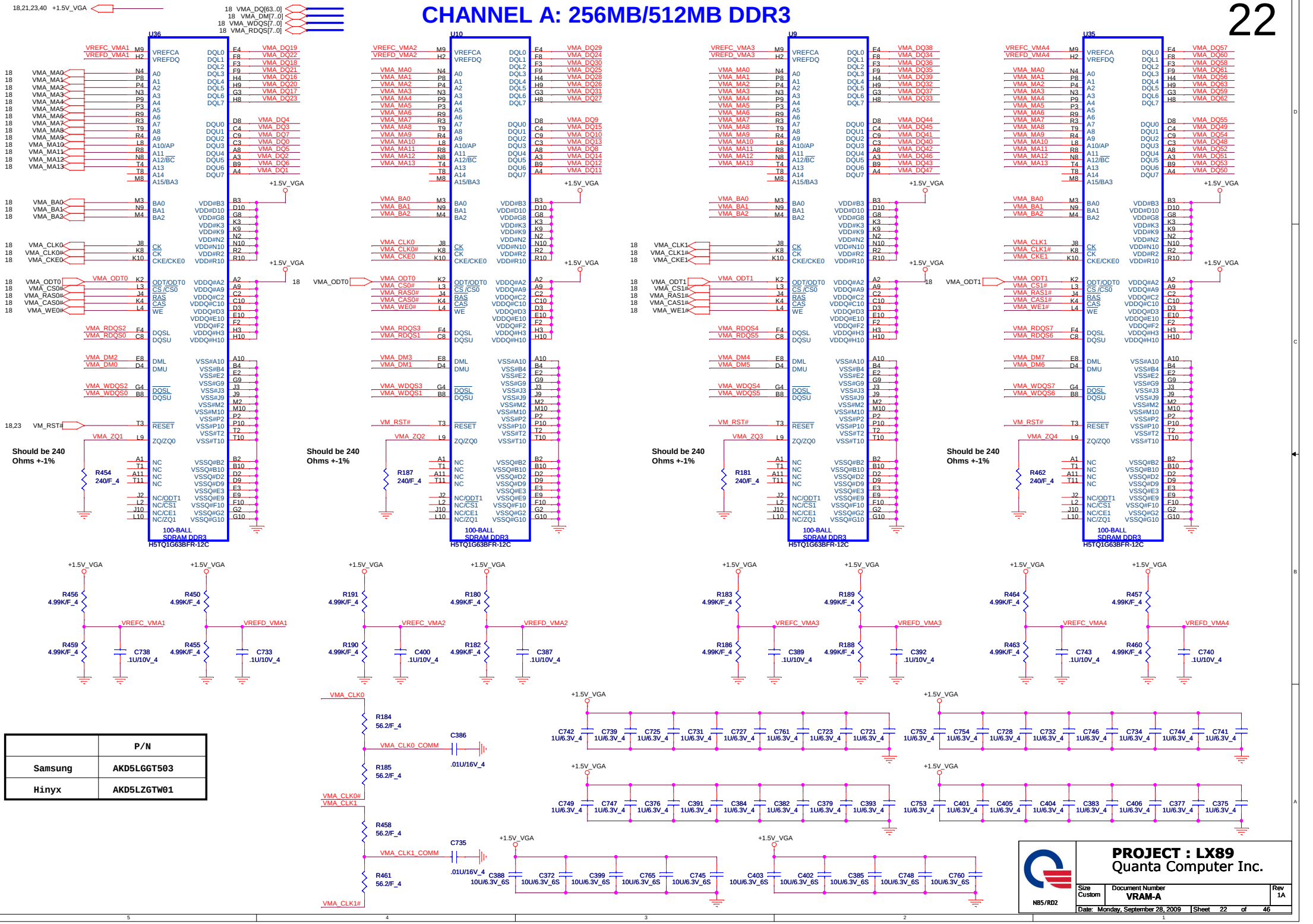
36,42,43 MAINON

R469 *68.1K_4

C764 *0.1U/10V_4

+3V_DELAY circuit

CHANNEL A: 256MB/512MB DDR3



	P/N
Samsung	AKD5LGGT503
Hinyx	AKD5LZGTW01

PROJECT : LX89
Quanta Computer Inc.

NB5/RD2

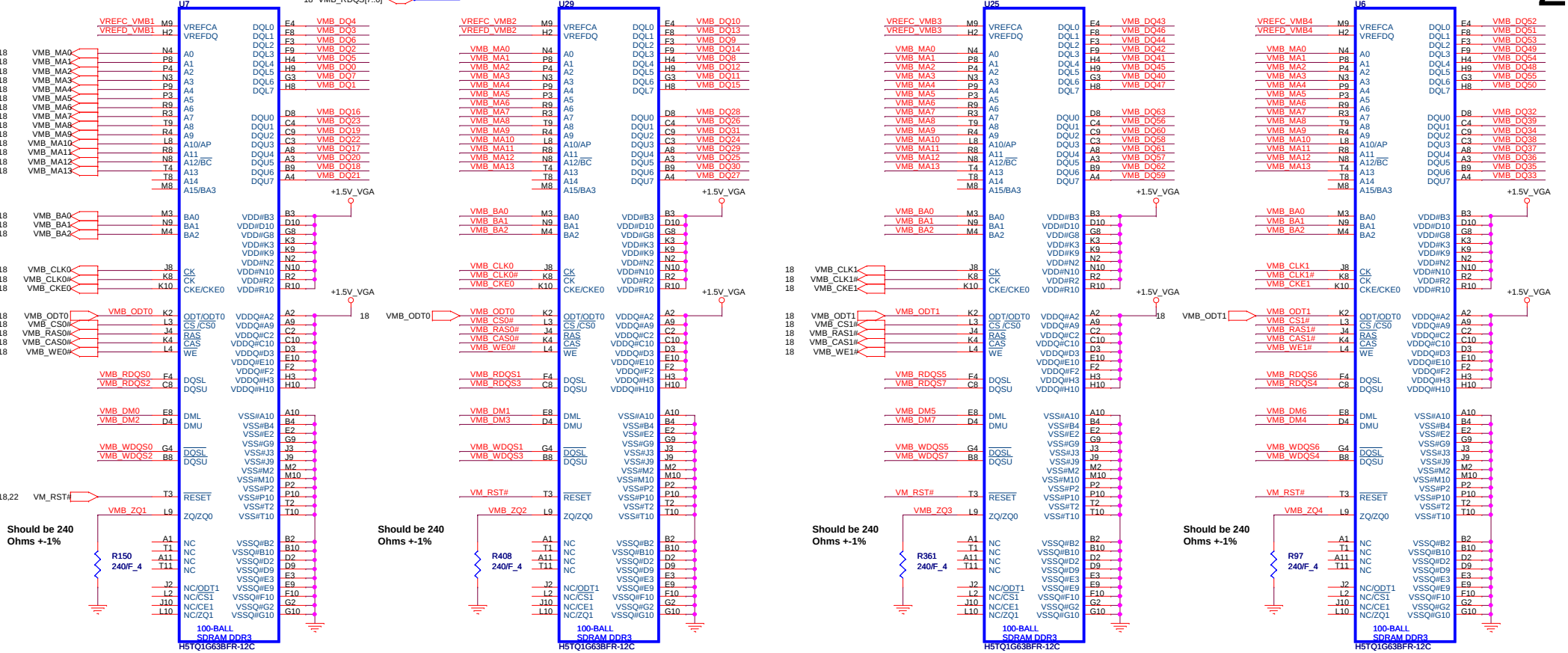
Size	Document Number	Rev
Custom	VRAM-A	1A

Date: Monday, September 28, 2009 Sheet 22 of 46

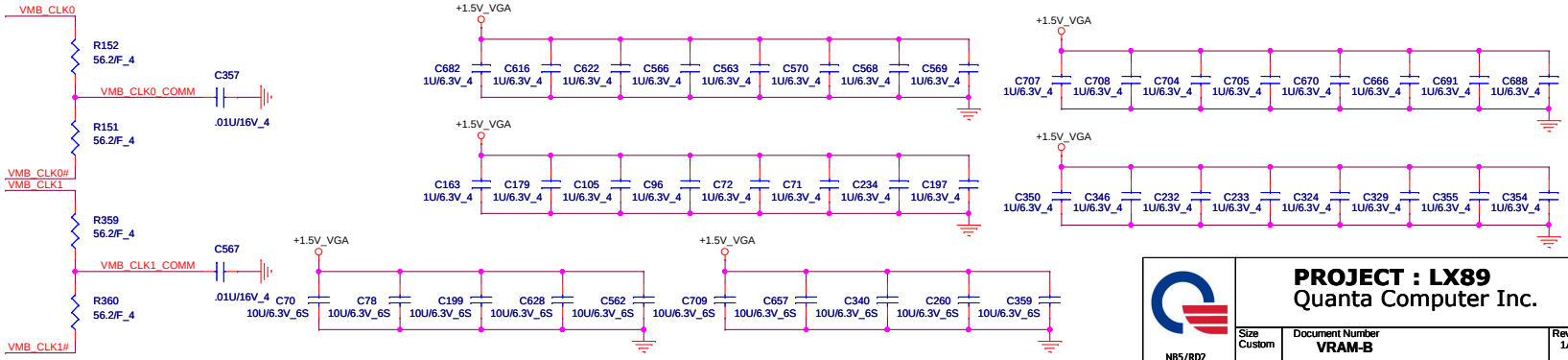
CHANNEL B: 256MB/512MB DDR3

18,21,22,40 +1.5V_VGA

18 VMB_DQ[63..0]
18 VMB_DM[7..0]
18 VMB_WDQS[7..0]
18 VMB_RDQS[7..0]



	P/N
Samsung	AKD5LGGT503
Hinyx	AKD5LZGTW01



NB5/RD2

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B	1A

Date: Monday, September 28, 2009 Sheet 23 of 46

+VIN 31,37,38,39,40,41,42,43
+12VALW 33,35,40,41,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY 18,19,20,21,26,27
+5V 25,26,27,28,29,33,34,35,42

+VIN L53 FBM2125 HM330-T(4A,0.015)_8 +VIN_BLIGHT
C518 0.1U/50V_6
C4 0.01U/50V_4
C2 0.1U/50V_6
C520 *10U/25V_12
C3 0.1U/50V_6

+3VLCD L6 PBY201209T-4A_8 +3VLCD_CON
C32 10U/6.3V_8
C31 0.1U/10V_4
C30 0.01U/16V_4

+12VALW
R320 330K_6
AO3404 ID current 5.8A
N-MOS,5.8A Q27 AO3404
+3V
C539 0.1U/10V_4
+3VLCD
+5V
R321 100K/F_4
LCDONG
R322 22_8
Q26 2N7002E
C532 0.1U/10V_4
LCDDISCHG
Q24 PDTC144EU
26 DISP_ON
R314 2.2K_4
LCDON#
Q25 2N7002E

+5V R303 75/F_6 +LOGO_PWR1
C523 1000P/50V_4

26 LVDS_BLON LVDS_BLON R306 1K/F_4
PN_BLON
D20 CH501H-40PT
BLONCON C522 22P/50V_4
+3VPCU R304 33K_6
R300 100K/F_4
LID_EC# LID_EC# 35,36
HWPG 36,37,38,40,41,42
D21 BAT54A
14 LCD_BK LCD_BK Q23 *PDTC144EU

From Switch
26 DPST_PWM DPST_PWM R311 1K/F_4
26,36 PWM_VADJ PWM_VADJ R305 *1K/F_4 VADJ1
From EC
Vari bright function
C526 *4.7U/6.3V_6
C524 22P/50V_4

+3VLCD_CON
26 EDIDCLK
26 EDIDDATA
+3V
C528 1000P/50V_4
26 TXLOUT0-
26 TXLOUT0+
26 TXLOUT1-
26 TXLOUT1+
26 TXLOUT2-
26 TXLOUT2+
26 TXLCLKOUT-
26 TXLCLKOUT+
26 TXUOUT0-
26 TXUOUT0+
26 TXUOUT1-
26 TXUOUT1+
26 TXUOUT2-
26 TXUOUT2+
26 TXUCLKOUT-
26 TXUCLKOUT+
+LOGO_PWR1
DMIC
29 DIGITAL_D1
29 DIGITAL_CLK
DIGITAL_CLK L54 BK1608HS601-T_6 DIGITAL_CLK_L
+3.9V-CAMARA
CAMERA
13 USBP2-
13 USBP2+
L1 *WCM2012-90
+VIN_BLIGHT
CN4 GS12407-11141-9H

DFHS40FS034
GS12407-11141-9H

CAMERA POWER

+5V +3.9V-CAMARA
U16 YB9210ST25R390
VIN VOUT SHDN GND SET
R299 *0_6
C519 1U/10V_4
R1 R301 *215K/F_4
C521 4.7U/6.3V_6
R2 R302 *100K/F_4

Vout=1.25(1+R1/R2)

Digitizer Connector

13 USBP1+
13 USBP1-
L7 *WCM2012-90
D5 *PJSD05TS
D6 *PJSD05TS
14 DGT_STOP#
14 DGT_RESET
FWE
GND
CN5 TS-FFC-connect

50281-0100n-001-10p-l
DFHD10MR044

Vout=1.25(1+R1/R2)

N85/RD2	PROJECT : LX89 Quanta Computer Inc.		
	Size: Custom	Document Number: LCD CONN	Rev: 1A
	Date: Monday, September 28, 2009	Sheet 24 of 46	

CRT PORT

+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,42
+5V 24,26,27,28,29,33,34,35,42
+3V_DELAY 18,19,20,21,26,27

R19 for UMA use 140 ohm
for DIS+PowerExpress use 150 ohm (AMD)

+5VCRT C11 0.1U/10V_4

+5V F1 FUSE1A6V_POLY 40 mils +5VCRT 40 MIL

DFDS15FR148
dsub-070546fr015s22fzr-15p-v

CRT_R L5 BK1608LL680(0.2A,68)_6 CRT_R1
CRT_G L4 BK1608LL680(0.2A,68)_6 CRT_G1
CRT_B L3 BK1608LL680(0.2A,68)_6 CRT_B1

R19 150/F_4 R18 150/F_4 R10 150/F_4
C34 5.6P/50V_6 C29 5.6P/50V_6 C20 5.6P/50V_6
C22 5.6P/50V_6 C28 5.6P/50V_6 C33 5.6P/50V_6

close conn within 600mils

CRT CONN CN18

26 CRT_R CRT_G CRT_B

SI Add D31~D37 for ME height limit

+3V
D31 *BAV99W CRT_R1
D32 *BAV99W CRT_G1
D33 *BAV99W CRT_B1
+5V
D34 *BAV99W DDCCLK2
D35 *BAV99W CRTVSYNC
D36 *BAV99W CRTHSYNC
D37 *BAV99W DDCDAT2

Del U19,C534,C535 add U46,U47,Q35,Q36 for ME height limit
SI

C536 0.1U/10V_4

U46 AHCT1G125DCH
U47 AHCT1G125DCH

26 VSYNC_COM
26 HSYNC_COM
26 DDCCLK
26 DDCDATA

Q35 2N7002E
Q36 2N7002E

PR_VSYNC
PR_HSYNC
DDCCLK2
DDCDAT2

R3 *0_4/S CRTDDCCLK2
R5 33_4 CRTVSYNC
R7 33_4 CRTHSYNC
R14 *0_4/S CRTDDCDAT2

C8 *470P/50V_4 C12 *47P/50V_4 C16 *47P/50V_4 C25 *47P/50V_4

R4 6.81K_4 R15 6.81K_4

+5VCRT +5VCRT +5V_CRT2 CH501H-40PT D22

HOLE

H8 *H-C217D63P2 H4 *H-C217D63P2
H19 *H-TC315BC354D118P2 H17 *H-TC315BC354D118P2 H15 *H-TC315BC354D118P2
H1 *H-TC315BC354D118P2 H3 *H-TC315BC354D118P2 H14 *H-TC315BC354D118P2 H5 *H-TC315BC354D118P2 H16 *h-tc315i138bc354d118p2
H13 *H-TC276I169BC197D150P2 H9 *H-TC276I169BC197D150P2 H12 *H-TC276I169BC197D150P2 H6 *H-TC276I169BC197D150P2 H10 *H-TC276I169BC197D150P2 H11 *H-TC276I169BC197D150P2
H18 *H-TC236BC354D130P2 H2 *H-TC236BC354D130P2
H7 *h-tc315i138bc354d118p2

PROJECT : LX89
Quanta Computer Inc.

N85/RD2

Size	Document Number	Rev
Custom	CRT&HOLE	1A

Date: Monday, September 28, 2009 Sheet 25 of 46

For Single-link panel

IGPU_Channel-A

DGPU_Channel-A

LVDS Channel Switch

U2 — Pericom PI2PCIE412-DZHE

SELx	Ay
HIGH	B2
LOW	B1

SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

follow AMD reference schematic change for reduce leakage to VDDR3 BUS

IGPU_Channel-B

DGPU_Channel-B

U1 — Pericom PI2PCIE412-DZHE

SELx	Ay
HIGH	B2
LOW	B1

SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

OPTION SIGNAL FROM NB to LVDS for UMA

LVDS/CRT DDC Switch

U22 — 74CBT3257

OPTION SIGNAL FROM NB to LVDS/CRT for UMA

VGA Switch

U23 — PI3V512

OPTION SIGNAL FROM NB to CRT for UMA

DIS Change Vari bright function from EC control

DPST Control

U17 — NLASB3157DFT2G

SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A

OPTION DPST SIGNAL FROM NB to LVDS for UMA

Back Light On conrtol

U18 — NLASB3157DFT2G

OPTION Back Light SIGNAL FROM NB to LVDS for UMA

LCDVcc control

U20 — NLASB3157DFT2G

OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

+5V 24,25,27,28,29,33,34,35,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,27,28,29,30,31,32,33,34,35,36,42
+1.8V 5,8,10,11,16,42

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/CRT Hyper_switch	1A

NB5/RD2

Date: Monday, September 28, 2009 | Sheet 26 of 46

UMA/DISCRETE select for HDMI

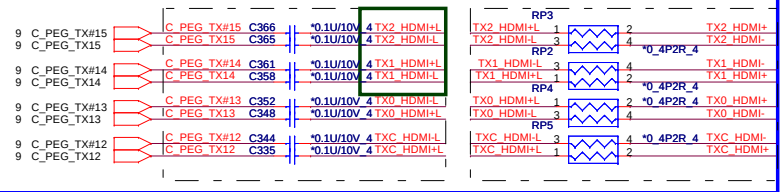
From RS880M

for Layout concern ,placement close north bridge

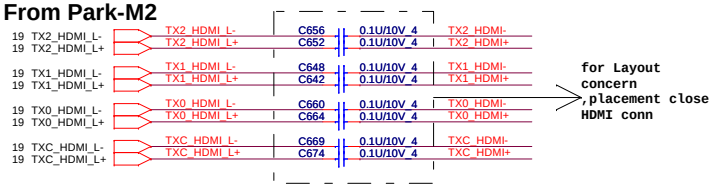
Swap pin for Layout

SI

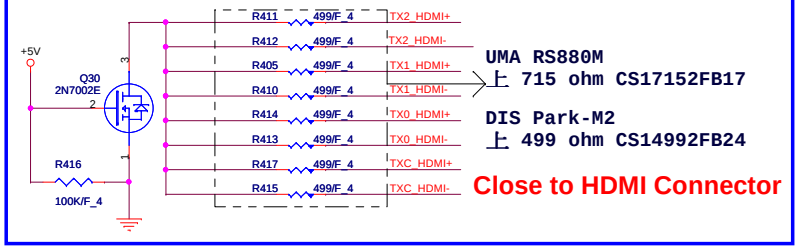
for Layout concern ,placement close HDMI conn



From Park-M2



for Layout concern ,placement close HDMI conn



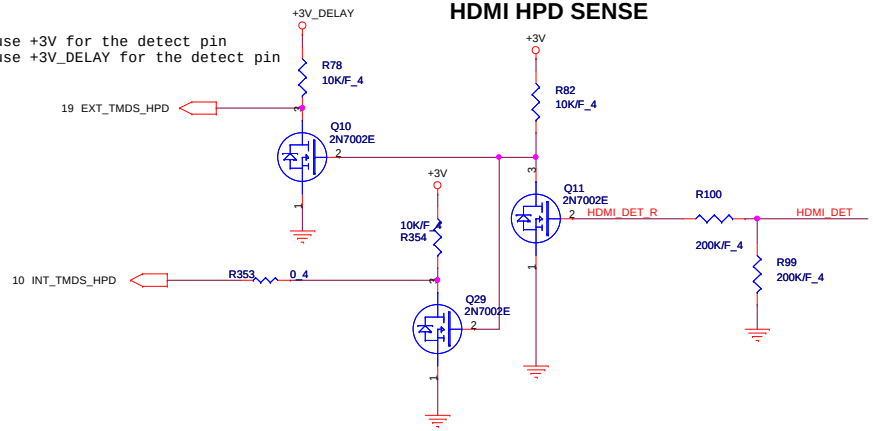
UMA RS880M
上 715 ohm CS17152FB17

DIS Park-M2
上 499 ohm CS14992FB24

Close to HDMI Connector

HDMI HPD SENSE

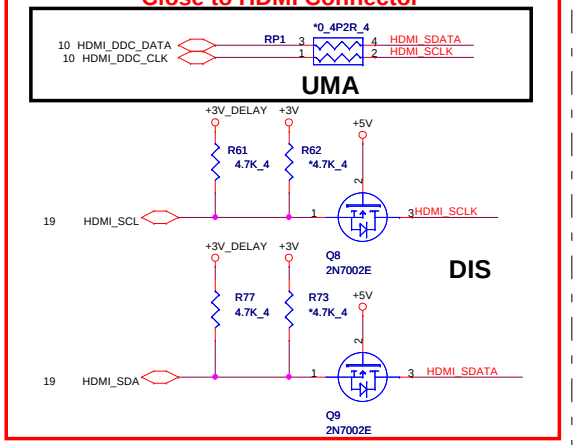
UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



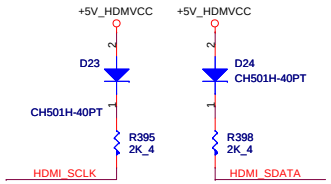
UMA AND DISCRETE HDMI I2C SELECT

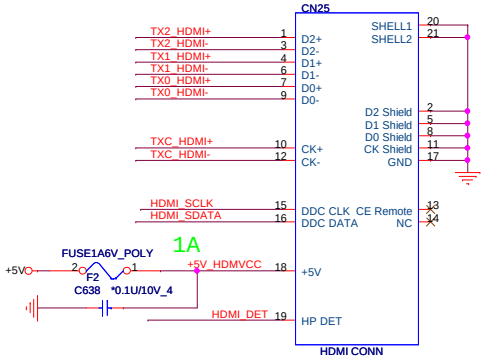
Close to HDMI Connector

Discrete DDC1 is 5V tolerance , the MOSFET level shifter no need
UMA DDC is 3V tolerance,the MOSFET level shifter is need



HDMI PORT





DFHD19MR041
hdmi-100042gr019s168-19p-ldv-v

+5V 24,25,26,28,29,33,34,35,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,28,29,30,31,32,33,34,35,36,42
+3V_DELAY 18,19,20,21,26

N85/RD2	PROJECT : LX89 Quanta Computer Inc.	
Size Custom	Document Number HDMI	Rev 1A
Date: Monday, September 28, 2009	Sheet 27 of 46	

XTAL control pin for
12Mhz crystal or 48Mhz
clk in

+3VSUS R512 *10K/F_4 SI

Del R512 for Internal 12MHz

U43

XTAL_CTR
GPIO0
EEDO
EECS
EESK
EEDI
XD_CD#
SD_WP
SD_CD#
MS_D4
SD_DAT1/XD_D4
MS_D5
RREF
DM
DP
12MHZ_XTLO
12MHZ_XTLI
MODE_SEL
RST#

XD_CLE
XD_CE#
XD_ALE
SD_DAT2/XD_RE#
SD_DAT3/XD_WE#
XD_RDY
SD_DAT4/XD_WP#/MS_D7
SD_CMD
SD_DAT5/XD_D0/MS_D6
SD_CLK/XD_D1/MS_CLK
SD_DAT6/XD_D7/MS_D3
NC
MS_INS#
SD_DAT7/XD_D2/MS_D2
SD_DAT0/XD_D6/MS_D0
XD_D3/MS_D1
XD_D5/MS_BS
AV_PLL_IN
VREG_OUT
5V_IN
NC
D3V3_IN
D3V3_IN
NC
CARD_3V3_OUT
AG33
AG_PLL
DGND2
DGND1

SP19 SP18 SP17 SP16 SP15 SP14 SP13 SD_CMD_R SP12 SP11 SP10 MS_CD# SP8 SP7 SP6 SP5

AL005159B00 -->RTS5159GR

R552 6.19K/F_4 RREF

13 USBP11-
13 USBP11+

C875 5.6P/50V_4 CLK_48M_CR
12MHz
Y7
R573 270K_4
C876 5.6P/50V_4 XTLI
BG612000717

MODE_SEL R585 *0_4

+3VSUS R584 *100K/F_4 5159_RST# C882 1U/10V_4

Internal have pull Hi 200K

Realtek RTS5159

C870 0.1U/10V_4 Vreg out 1.8V from Internal 3.3VLDO C857 1U/10V_4

VREG +3VSUS_RTS R527 *0_8/S +3VSUS

C861 0.1U/10V_4 C862 4.7U/6.3V_6

0.1U/10V_4 C864

D3V3_IN +3VSUS

0.1U/10V_4 C856 C851 4.7U/6.3V_6

+3VCARD

C858 1U/10V_4

RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

+3VCARD

C847 0.1U/10V_4 C848 0.1U/10V_4 C849 0.1U/10V_4

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7 R528 0_4 MS-D0_SD-D0_XD-D6
SP6 R524 0_4 MS-D1_XD-D3_SD_D1
SP8 R531 0_4 MS-D2_XD-D2
SP16 R579 0_4 XD-RE#_SD-D2
SP5 R522 0_4 MS-BS_XD-D5
SP15 R578 0_4 SD-D3_XD-WE
SP11 R569 0_4 SD_CLK_MS_CLK

SP2 R511 0_4 SD_WP
SP13 R576 0_4 XD-WP#
SP19 R582 0_4 XD-CLE
SP4 R510 0_4 XD-D4
SP10 R537 0_4 MS-D3_XD-D7
SP14 R577 0_4 XD-RB#
SP12 R570 0_4 XD-D0
SP17 R580 0_4 XD-ALE
SP18 R581 0_4 XD-CE#
SD_CMD_R R571 0_4 SD-CMD

Close to Chipset

SP11 C869 *5.6P/50V_4 Can not more than 10p

5159_RST# R583 *0_4/S 5159_RST_R# 5159_RST_R# 13

+3VCARD +3VCARD +3VCARD

R298 *10K/F_4

CN15

XD-R/B
XD-RE
XD-CE
XD-CLE
XD-ALE
XD-WE
XD-WP
XD-D0
XD-D1
SD-DAT2
SD-DAT3
SD-CMD
4IN1-GND1
MS-VCC
MS-SCLK
MS-DATA3
MS-INS
MS-DATA2
MS-DATA0

MS-DATA1
MS-BS
4IN1-GND2
SD-VCC
SD-CLK
SD-DAT0
XD-D2
XD-D3
XD-D4
SD-DAT1
XD-D5
XD-D6
XD-D7
XD-VCC
XD-CD-SW
SD-WP-SW
SD-CD-SW
SHIELD1-GND
SHIELD2-GND
BOS
BOS

XD-RB# XD-RE#_SD-D2 XD-CE# XD-CLE XD-ALE SD-D3_XD-WE XD-WP# XD-D0 SP11 XD-RE#_SD-D2 SD-D3_XD-WE SD-CMD SD_CLK_MS_CLK MS-D3_XD-D7 MS_CD# MS-D2_XD-D2 MS-D0_SD-D0_XD-D6

MS-D1_XD-D3_SD_D1 MS-BS_XD-D5 SD_CLK_MS_CLK MS-D0_SD-D0_XD-D6 MS-D2_XD-D2 MS-D1_XD-D3_SD_D1 XD-D4 MS-BS_XD-D5 MS-D0_SD-D0_XD-D6 MS-D3_XD-D7 XD_CD# SD_WP SD_CD#

C517 *270P/25V_4

CARD READER SOCKET

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

DFHD36MR005

4in1-cm4s-125-36p-r-v

+3VCARD

C512 2.2U/6.3V_6 R297 150K/F_4

CLOSE CONN

+3VCARD

C511 0.1U/10V_4 C508 0.1U/10V_4 C850 0.1U/10V_4

CPU FAN

+3V R339 4.7K_6

36 FAN1SIG

30 mil

+5VFAN1

CN20

C545 2.2U/6.3V_6 C544 0.1U/10V_4

FAN CONN

DFHD03MR026

footprint: "85205-03xx-3p-l"

G991 /FON signal have internal pull Hi to VIN , R420 maybe can remove

+5V C542 1U/10V_4

R334 10K/F_4

U3

VIN VO
/FON GND
GND
GND
VSET GND

+5VFAN1

FAN_SMBALERT#

36 FAN1ON

FANPWR = 1.6*VSET

G991PV11

Gnd shape

G991 layout notice

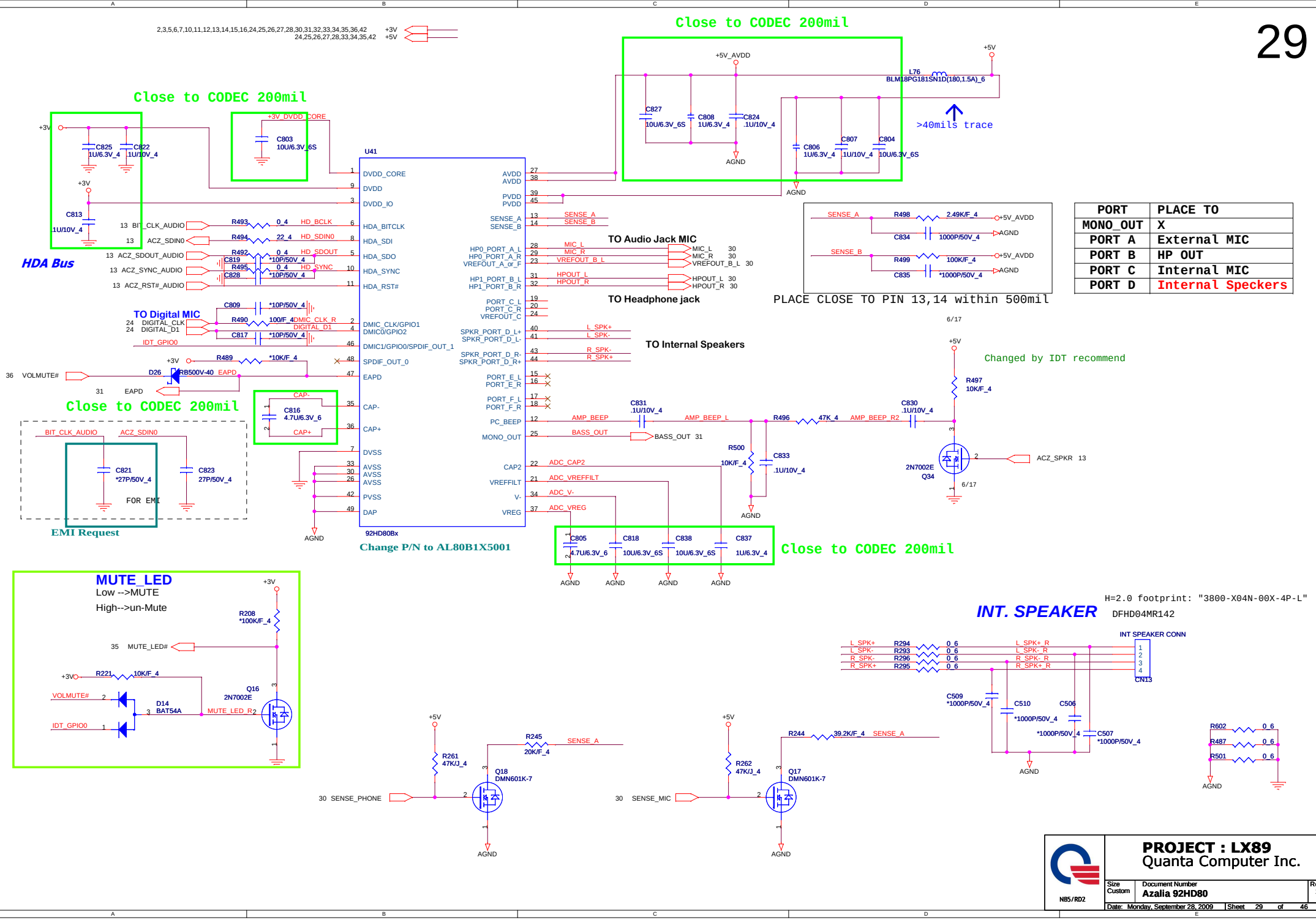
+5V 24,25,26,27,29,33,34,35,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,29,30,31,32,33,34,35,36,42
+3VSUS 13,33,34,35,41,42

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159&CPU FAN	1A

N85/RD2

Date: Monday, September 28, 2009 Sheet 28 of 46



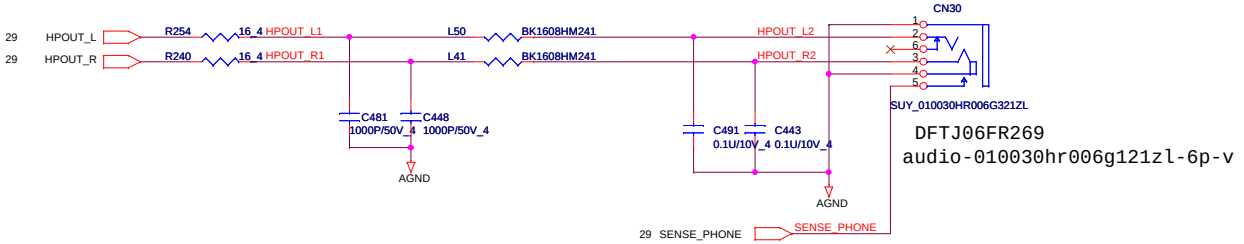
PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

PROJECT : LX89		
Quanta Computer Inc.		
Size: Custom	Document Number: Azalia 92HD80	Rev: 1A
Date: Monday, September 28, 2009	Sheet 29 of 46	
N85/RD2		

33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

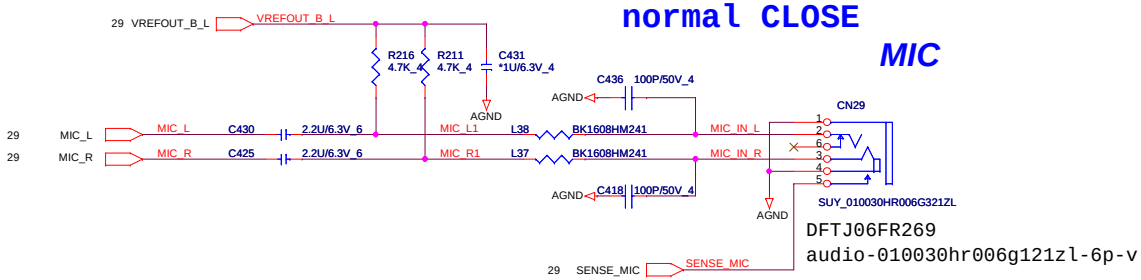
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

normal CLOSE *Line out*



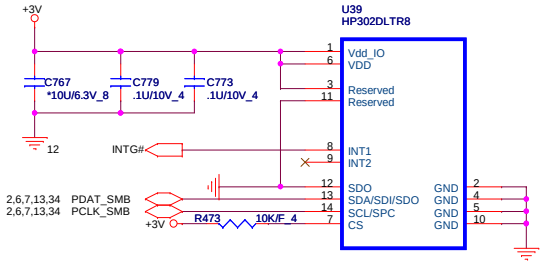
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

normal CLOSE *MIC*



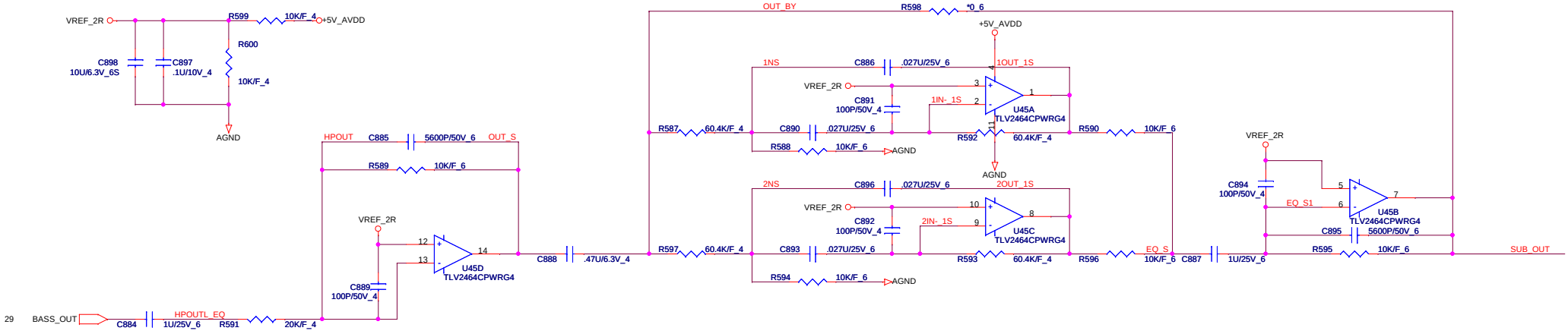
Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



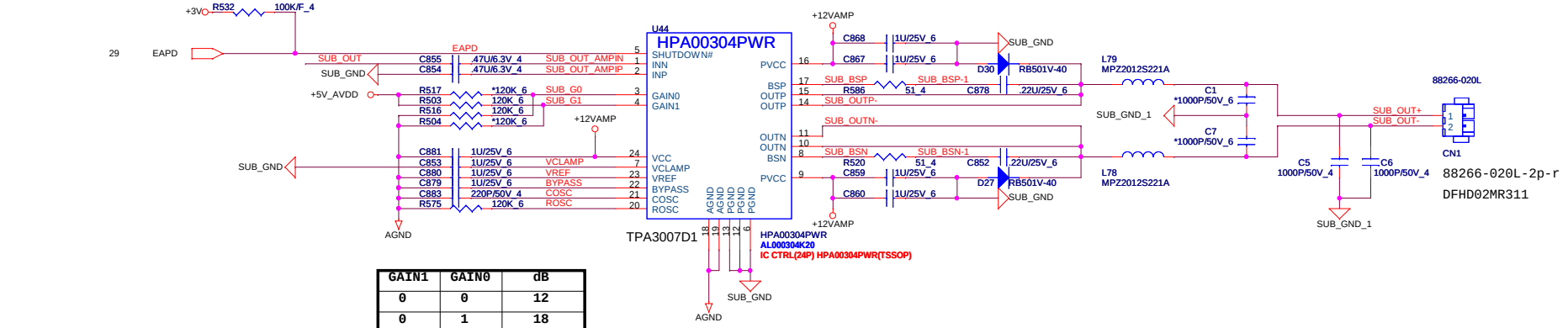
	PROJECT : LX89 Quanta Computer Inc.	
N85/RD2	Size: Custom; Document Number: **Audio Jack/Accelerometer**	Rev: 1A
	Date: Monday, September 28, 2009	Sheet 30 of 46

EQ FOR SUBWOOFER



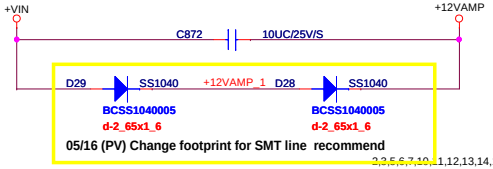
MODEL	UP7
R9402	60.4K/F_6
R9403	60.4K/F_6
R9407	60.4K/F_6
R9408	60.4K/F_6
C5144	0.027U/25V_6
C5146	0.027U/25V_6
C5148	0.027U/25V_6
C5153	0.027U/25V_6

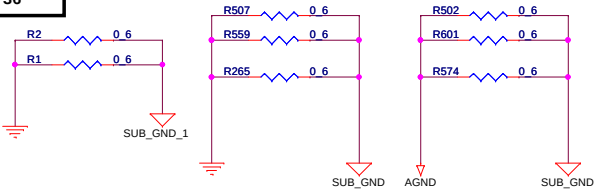
5/27: NA for subwofer function



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

Sub-Woofer power





24,37,38,39,40,41,42,43 +VIN
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42 +3V

+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42
+5V_AVDD 29
+VIN 24,37,38,39,40,41,42,43

PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	1A
N85/RD2	Date: Monday, September 28, 2009	Sheet 31 of 46

T : Stuffed for RTL8111DL(10/100/1000)

for RTL8111DL use close Pin 44,45

for RTL8111DL use

+CTRL12DVDD — R472 *0_6/S short0603 — +3V_LAN

C777 10U/6.3V_8, C772 10U/6.3V_8, C774 0.1U/10V_4

42 +3VLANVCC

+3VLANVCC — R467 *0_8/S short0805 — +3V_LAN

C758 0.1U/10V_4, C778 0.1U/10V_4, C785 0.1U/10V_4, C781 0.1U/10V_4

Close to PIN 1

Y1 25MHZ

C414 33P/50V_4, C411 33P/50V_4

XTAL1, XTAL2

+CTRL12DVDD — R471 2.49K/F_4 — LANRSET

ENSWREG

+3V_LAN, +DVDD12_LAN

LAN_TX#

+CTRL12A

U11 RTL8111DL-VB-GR

AVDD33, MDIP0, MDIN0, NC/FB12, MDIP1, MDIN1, GND1, NC/MDIP2, NC/MDIN2, DVDD12/AVDD12, NC/MDIP3, NC/MDIN3

VCTRL12A/SROUT12, GND4, RSET, VCTR12VDDSR, NC/SWRSC, NC/ENSWREG, CKTAL2, CKTAL1, NC/AVDD33, NC/LV_PLL, LED0, VDD33B

DVDD12B, LED1/EESK, LED2/EEDI, LED3/EEDO, EECS, GND3, DVDD12A, VDD33A, ISOLATEB, PERSTB, LANWAKEB, CLKREQB

LAN_GLINK100# — +DVDD12_LAN

LAN_GLINK10# — R474 3.6K_6 — +3V_LAN

EECS — T34

ISOLATEB

LAN_REST_R# — R475 *0_4 — LAN_REST# 36

PCIE_WAKE# — PCIE_WAKE# 13,34

LAN CABLE DETECT 36

PCIE_RXN2_LAN_C C413 0.1U/10V_4 — PCIE_RXN2_LAN 9

PCIE_RXP2_LAN_C C412 0.1U/10V_4 — PCIE_RXP2_LAN 9

EVDD12

9 PCIE_TXP2_LAN — PCIE_TXP2_LAN

9 PCIE_TXN2_LAN — PCIE_TXN2_LAN

2,12 PCIE_LAN_CLKP — PCIE_LAN_CLKP

2,12 PCIE_LAN_CLKN — PCIE_LAN_CLKN

+3V

R198 *1K/F_4

ISOLATEB — R195 100_4 — LAN_DISABLE# 13,36

R196 15K/F_4

*RB501V-40 D13

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U34 NS892405

TCT1, TD1+, TD1-, TCT2, TD2+, TD2-, TCT3, TD3+, TD3-, TCT4, TD4+, TD4-

MCT1, MX1+, MX1-, MCT2, MX2+, MX2-, MCT3, MX3+, MX3-, MCT4, MX4+, MX4-

C397 .01U/16V_4 V_DAC0 — MDI0+ — MDI0-

C396 .01U/16V_4 V_DAC1 — MDI1+ — MDI1-

C395 .01U/16V_4 V_DAC2 — MDI2+ — MDI2-

C394 .01U/16V_4 V_DAC3 — MDI3+ — MDI3-

LAN_MCT0 — C371 0.01U/100V_0603 — R174 75/F_4

LAN_MX0+, LAN_MX0-

LAN_MCT1 — C370 0.01U/100V_0603 — R173 75/F_4

LAN_MX1+, LAN_MX1-

LAN_MCT2 — C369 0.01U/100V_0603 — R172 75/F_4

LAN_MX2+, LAN_MX2-

LAN_MCT3 — C368 0.01U/100V_0603 — R171 75/F_4

LAN_MX3+, LAN_MX3-

C729 1000P/3KV_1808

+3V_LAN — C793 0.1U/10V_4

U40 TC7SH08FU

12 LAN_PLTRST# — LAN_REST_R#

NS892402:GIGABIT

DB0AT9LAN05

>60mil — L72 4.7UH_8 — >60mil

Power trace Layout 寬度> 60mil

+CTRL12A — +CTRL12A_L

C757 10U/6.3V_8, C763 10U/6.3V_8, C766 0.1U/10V_4

EVDD12

Close to 8111DL DVDD12 pins-- 19

C775 1U/10V_4, C776 1U/10V_4

+DVDD12_LAN

C784 0.1U/10V_4, C771 0.1U/10V_4, C762 0.1U/10V_4, C780 0.1U/10V_4, C783 0.1U/10V_4

Close to 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

L149

RTL8111DL (Gaga lan) use 4.7uH power choke A>600mA tolerance ±15%

RJ45

C128 *.1U/10V_4

CN21

+3V_LAN — R71 56.2/F_4

LAN_YLED — LAN_YLED#

LAN_MX3+, LAN_MX3-, LAN_MX2-, LAN_MX1-, LAN_MX1+, LAN_MX2+, LAN_MX0+, LAN_MX0-

RX1-, RX1+, RX0-, TX1-, TX1+, RX0+, TX0-, TX0+

LED_GRE_P, LED_GRE_N

GND1, GND

+3V_LAN — R57 1K/F_4 — LAN_GLED — LAN_GLED#

C52 *.1U/10V_4

LED_YEL_P, LED_YEL_N

RJ45_CONN

DFTJ12FR104

rj45-1-2006105-4-12p-rdv-v

LAN_GLINK100# — LAN_GLED#

LAN_TX# — LAN_YLED#

C416 *0.01U/16V/X7R_4, C415 *0.01U/16V/X7R_4

Link

N85/RD2

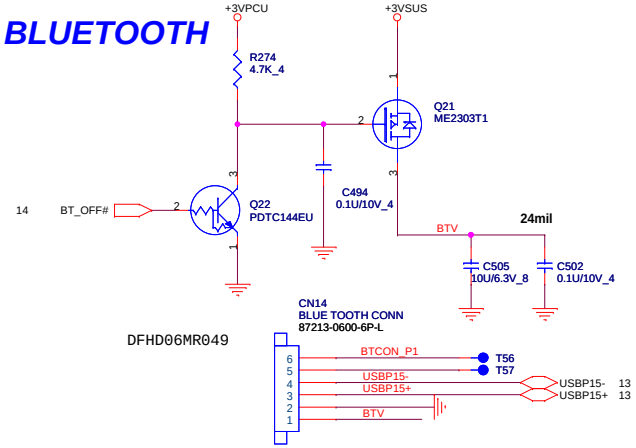
PROJECT : LX89

Quanta Computer Inc.

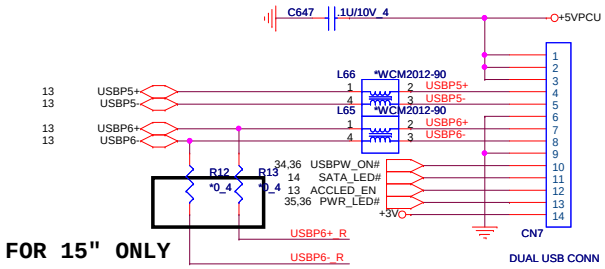
Size	Document Number	Rev
Custom	RTL8111DL/RJ45	1A

Date: Monday, September 28, 2009 Sheet 32 of 46

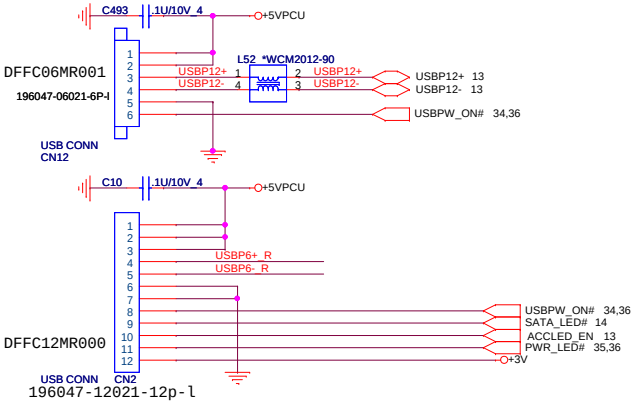
BLUETOOTH



RIGHT SIDE USBX2 for 17"



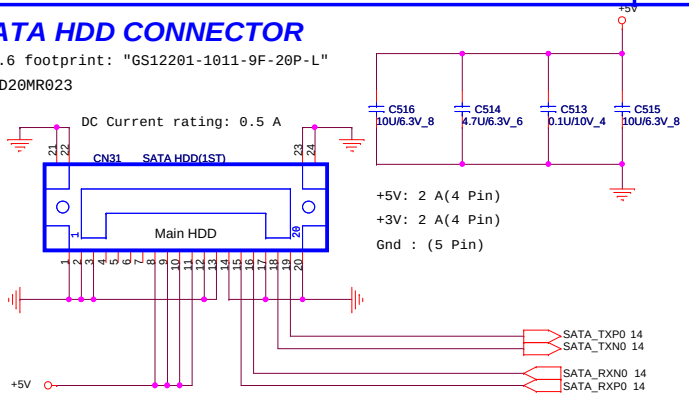
RIGHT SIDE USBX2 for 15"



SATA HDD CONNECTOR

H=2.6 footprint: "GS12201-1011-9F-20P-L"

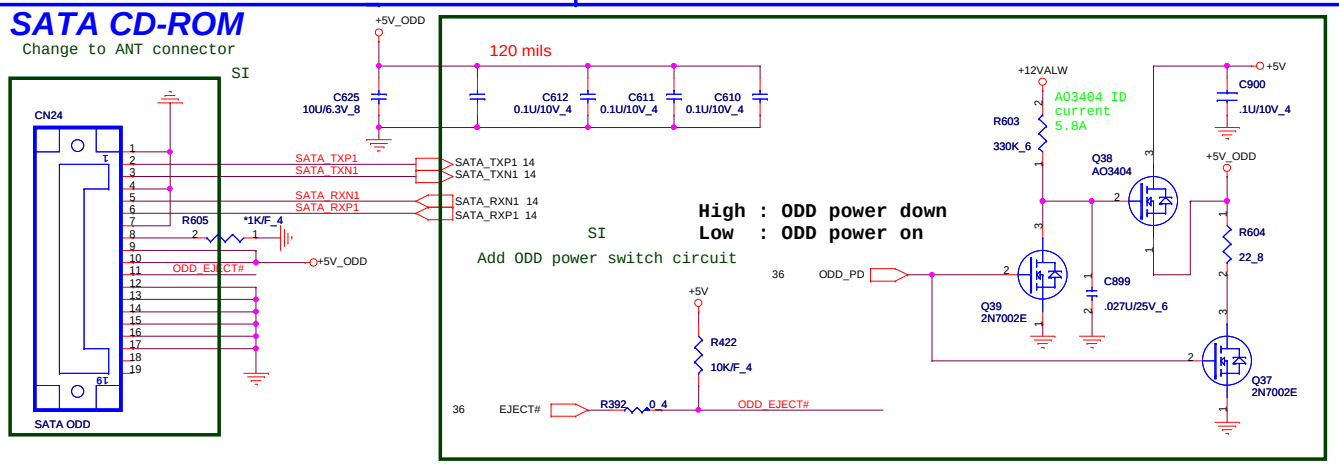
DFHD20MR023



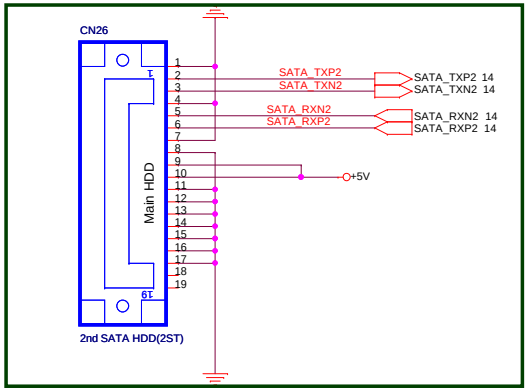
SATA CD-ROM

Change to ANT connector

SI



SATA_2 HDD CONNECTOR FOR 17.3"

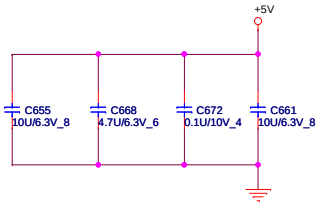


+5V: 2 A(4 Pin)

Gnd : (5 Pin)

SI

Change to ANT connector

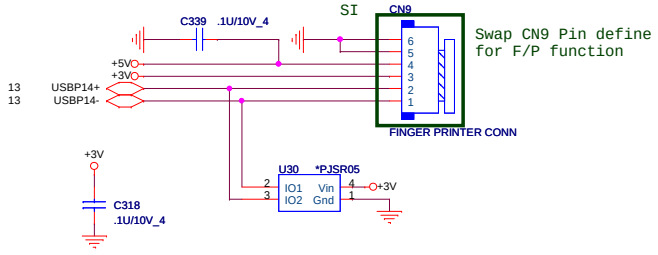


USB Fingerprint CON

DFFC06MR001

196047-06021-6P-l

1. SYSTEM GND
2. SYSTEM GND
3. LED PWR(+5V)
4. USB PWR(+3V)
5. USB1.1+
6. USB1.1-



34,36,37,38,39,40,41,42,43 +5VPCU
13,28,34,35,41,42 +3VSUS
4,6,12,24,35,36,37,38,39,40,41,42,43 +3VPCU
24,25,26,27,28,29,34,35,42 +5V

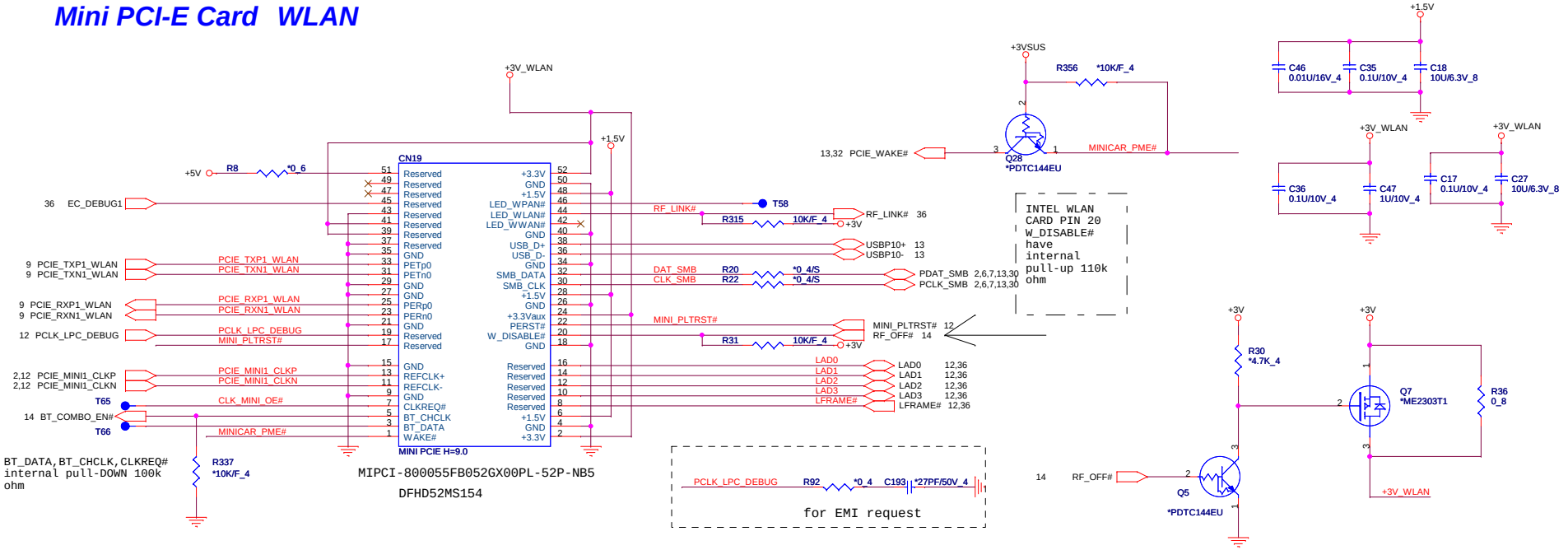
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/FP/USBX2/SATA HDDX2/ODD	1A

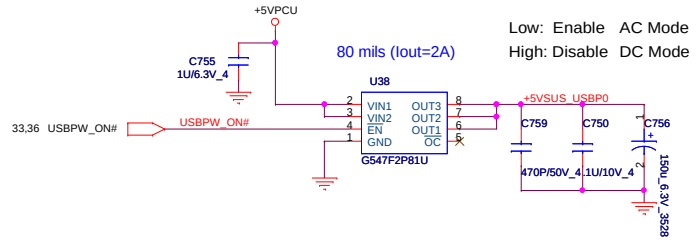
NB5/RD2

Date: Monday, September 28, 2009 Sheet 33 of 46

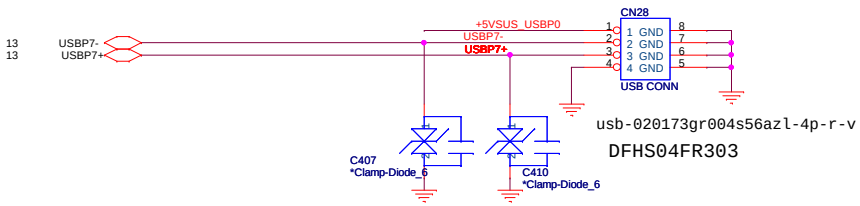
Mini PCI-E Card WLAN



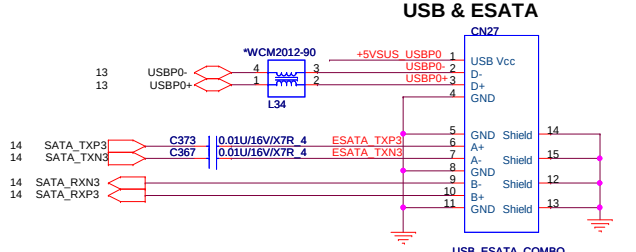
USB2.0 X 1 and E-SATA/USB2.0 COMBO



USB



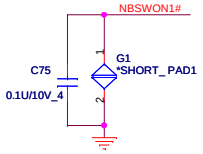
USB & ESATA



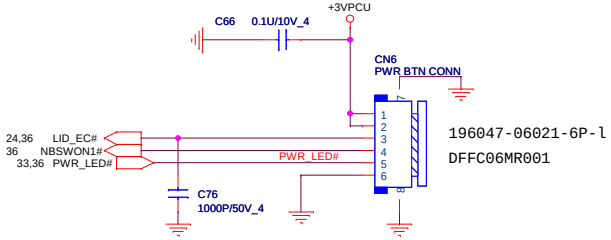
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mini CARD	1A
N85/RD2	Date: Monday, September 28, 2009	Sheet 34 of 46

POWER BUTTON CONNECT



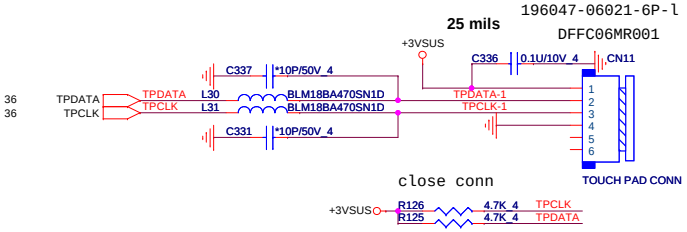
1. +3VPCU(LIDSWITCH PWR)
2.(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND



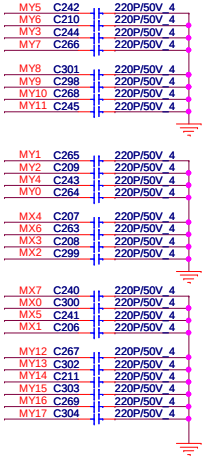
196047-06021-6P-l
DFFC06MR001

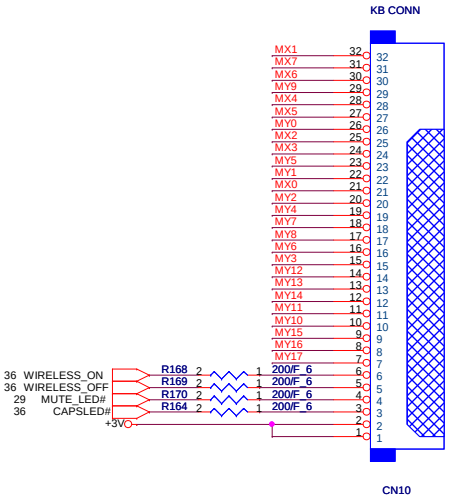
TOUCH PAD CONN

196047-06021-6P-l
DFFC06MR001

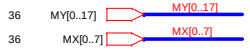


KEYBOARD Con.

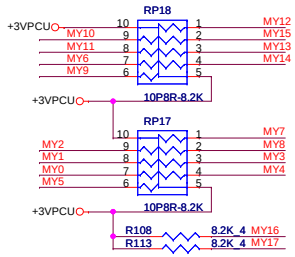




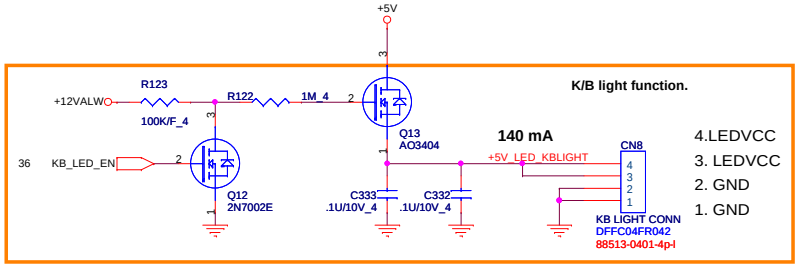
CN10
DFFC32FR024
bl135h-32rla-tand-32p-l

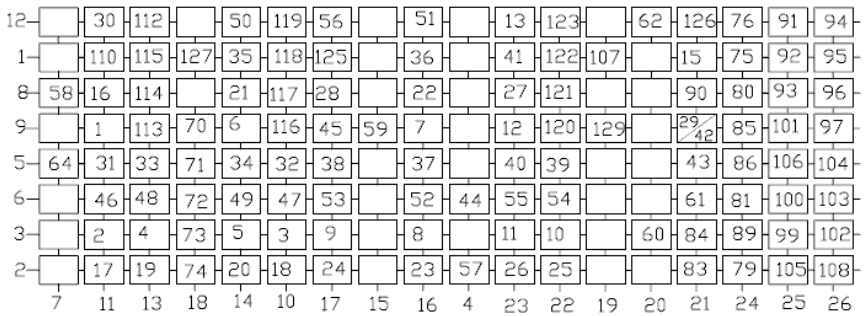


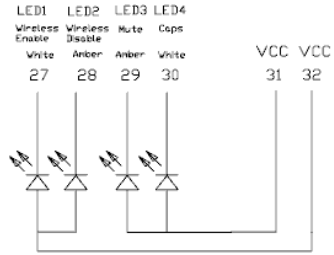
KEYBOARD PULL-UP



Need check pin define







PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW_BOARD	1A

N85/RD2

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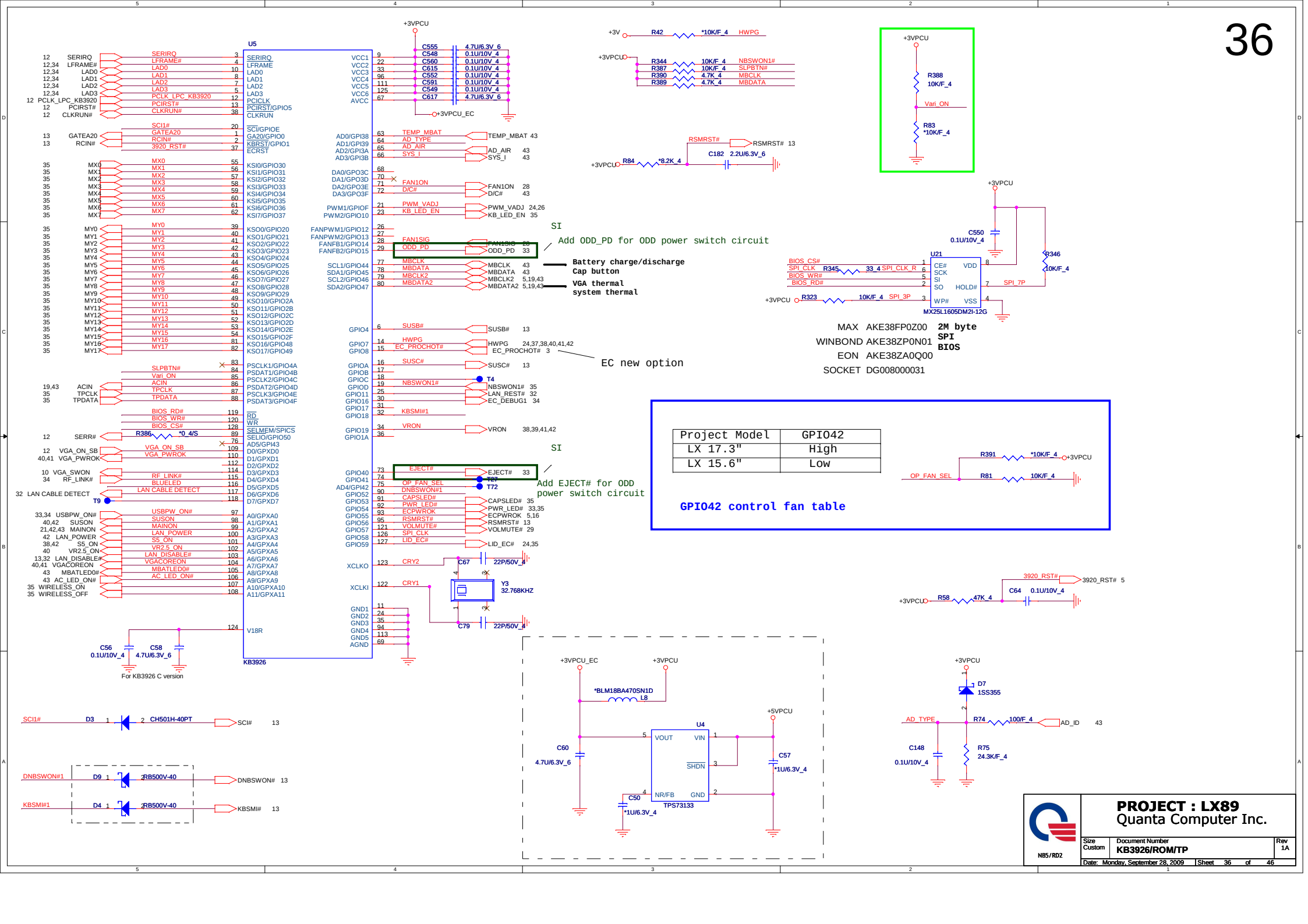
U5
KB3926
For KB3926 C version
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCLK_LPC_KB3920
PCIRST#
CLKRUN#
SCI#
GATEA20
RCIN#
3920_RST#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MY16
MY17
SLPBTN#
Vari_ON
ACIN
TPCLK
TPDATA
BIOS_RD#
BIOS_WR#
BIOS_CS#
R386 *0_4/S
SERR#
VGA_ON_SB
VGA_PWROK
RF_LINK#
BLUELED
LAN CABLE DETECT
T9
USBPW_ON#
SUSON
MAINON
LAN_POWER
S5_ON
VR2.5_ON
LAN_DISABLE#
VGACOREON
MBATLED0#
AC_LED_ON#
WIRELESS_ON
WIRELESS_OFF
+3VPCU
C555 4.7U/6.3V_6
C548 0.1U/10V_4
C560 0.1U/10V_4
C615 0.1U/10V_4
C552 0.1U/10V_4
C591 0.1U/10V_4
C549 0.1U/10V_4
C617 4.7U/6.3V_6
+3VPCU_EC
TEMP_MBAT
AD_TYPE
AD_AIR
SYS_I
FAN1ON
D/C#
PWM_VADJ
KB_LED_EN
FAN1SIG
ODD_PD
MBCLK
MBDATA
MBCLK2
MBDATA2
SUSB#
HWPG
EC_PROCHOT#
SUSC#
NBSWON1#
KBSMI#1
VRON
EJECT#
OP_FAN_SEL
CAPSLED#
PWR_LED#
ECPWROK
RSMRST#
VOLMUTE#
SPI_CLK
LID_EC#
CRY2
CRY1
C67 22P/50V_4
Y3 32.768KHZ
C79 22P/50V_4
C56 0.1U/10V_4
C58 4.7U/6.3V_6
V18R
SCI#
D3 CH501H-40PT
DNBSWON#1
D9 RB500V-40
KBSMI#1
D4 RB500V-40
+3V
R42 *10K/F_4 HWPG
R344 10K/F_4 NBSWON1#
R387 10K/F_4 SLPBTN#
R390 4.7K_4 MBCLK
R389 4.7K_4 MBDATA
RSMRST#
R84 *8.2K_4
C182 2.2U/6.3V_6
R388 10K/F_4
Vari_ON
R83 *10K/F_4
SI
Add ODD_PD for ODD power switch circuit
Battery charge/discharge
Cap button
VGA thermal
system thermal
EC new option
Add EJECT# for ODD
power switch circuit
C550 0.1U/10V_4
U21
BIOS_CS#
SPI_CLK
BIOS_WR#
BIOS_RD#
R345 33_4
SPI_CLK_R
R323 10K/F_4
SPI_3P
SPI_7P
R346 10K/F_4
MX25L1605DM2I-12G
MAX AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00
SOCKET DG008000031
2M byte
SPI
BIOS
Project Model | GPIO42
LX 17.3" | High
LX 15.6" | Low
GPIO42 control fan table
R391 *10K/F_4
R81 10K/F_4
C64 0.1U/10V_4
R58 47K_4
*BLM18BA470SN1D
L8
U4
TPS73133
C60 4.7U/6.3V_6
C57 *1U/6.3V_4
C50 *1U/6.3V_4
+5VPCU
D7 1SS355
R74 100/F_4
AD_ID
C148 0.1U/10V_4
R75 24.3K/F_4
PROJECT : LX89
Quanta Computer Inc.
N85/RD2
Size Custom
Document Number KB3926/ROM/TP
Rev 1A
Date: Monday, September 28, 2009
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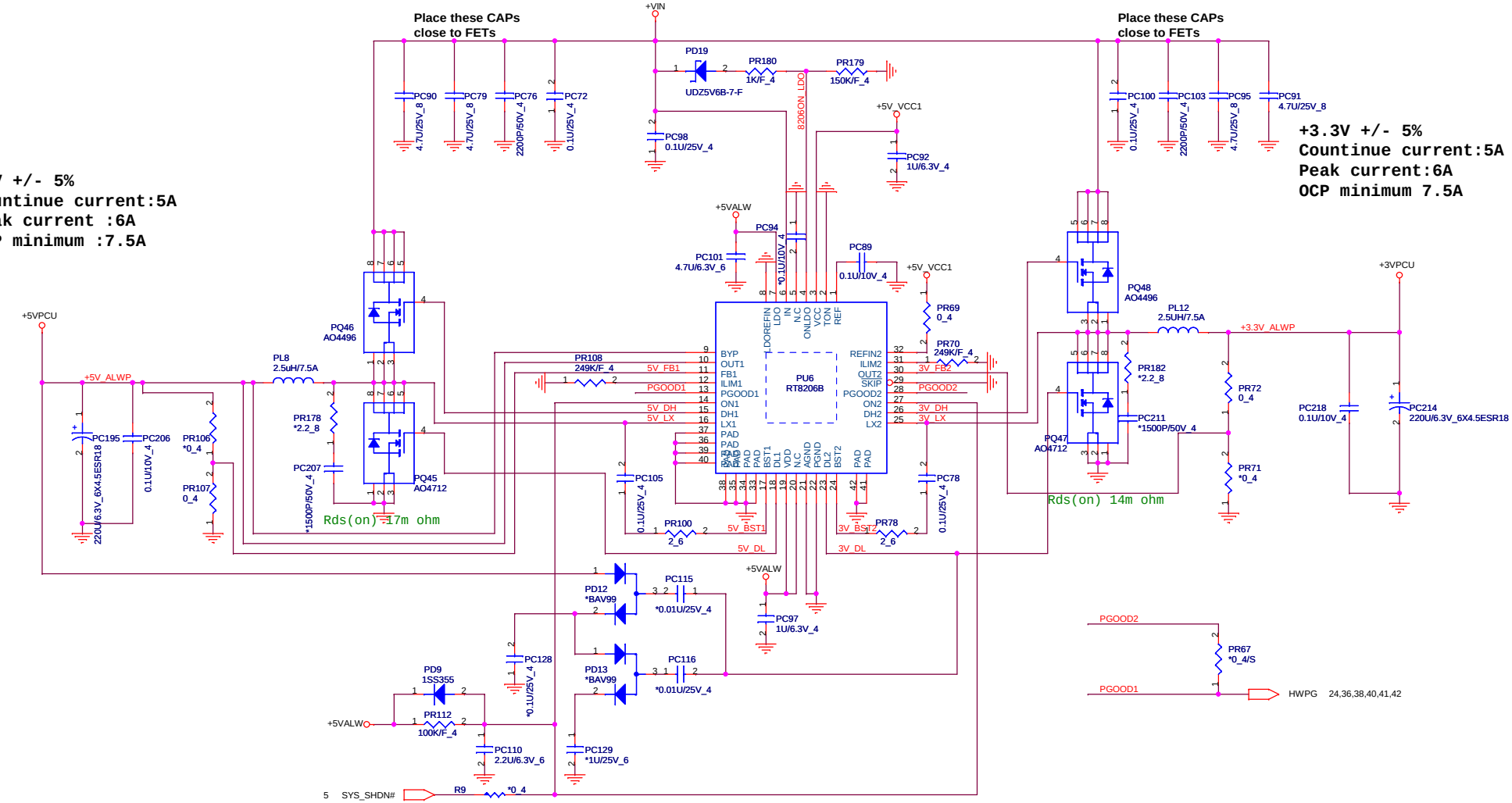
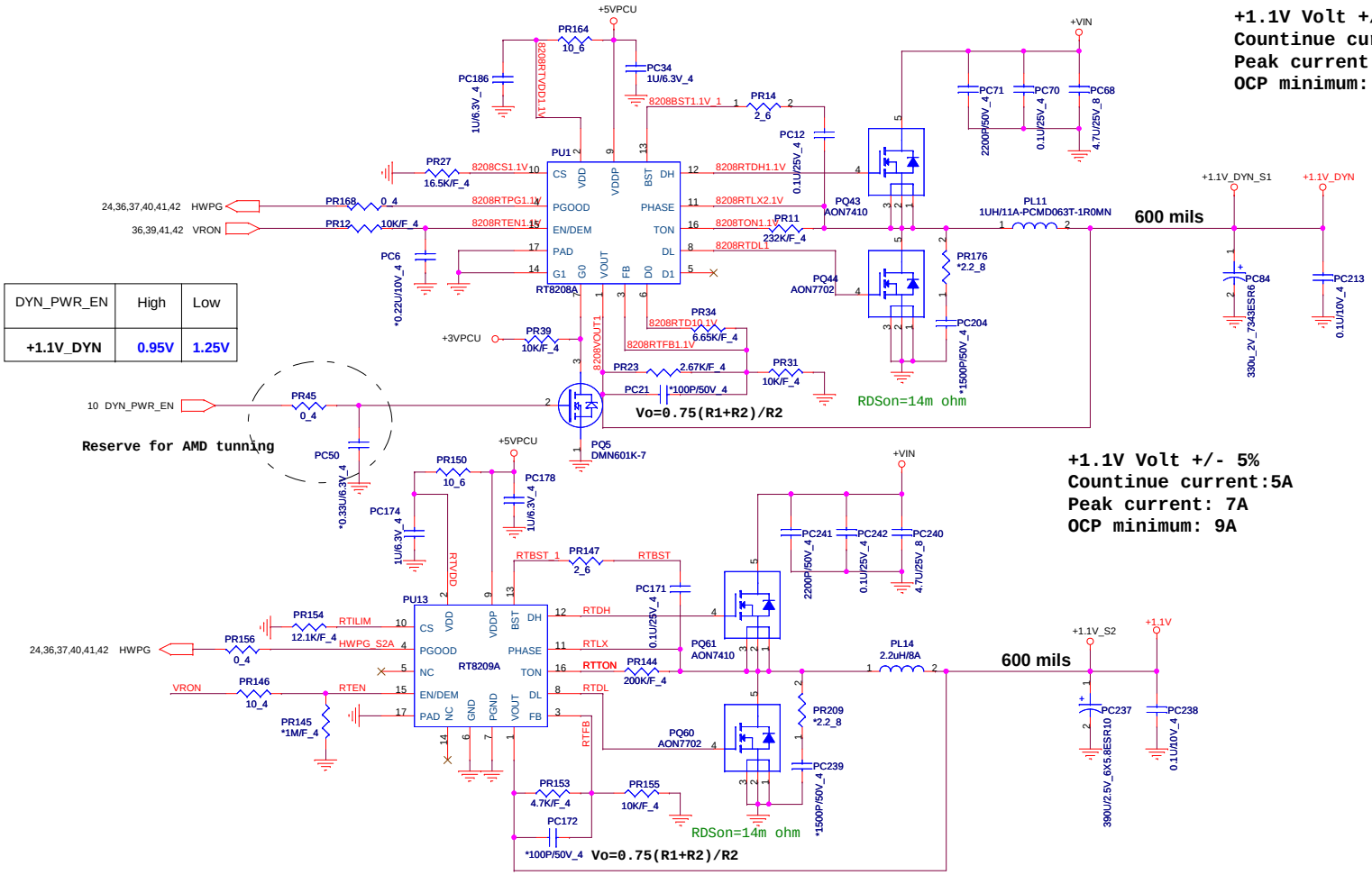
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



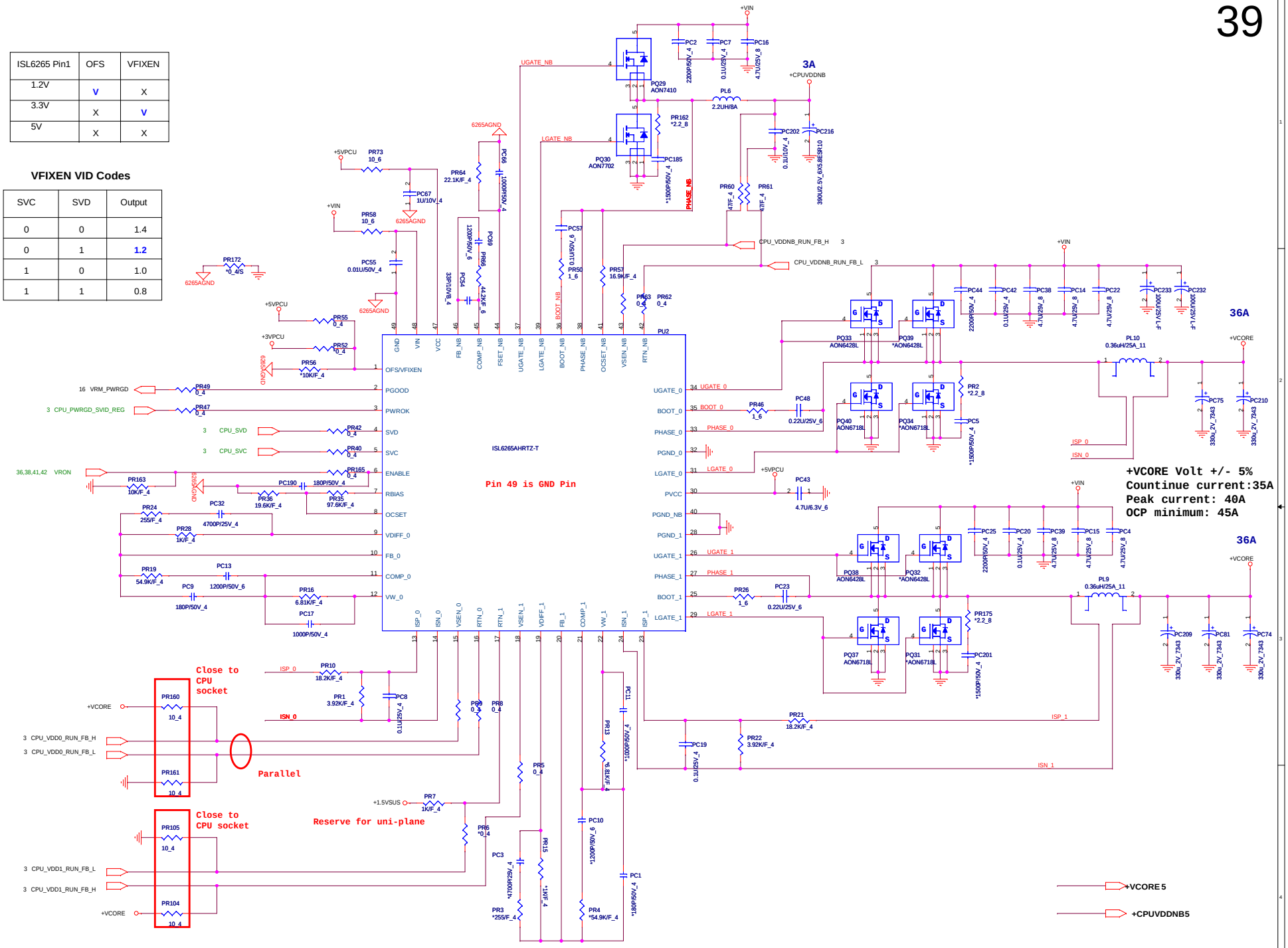
NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Monday, September 28, 2009	Sheet 37 of 46	


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 7A
OCP minimum: 9A
+5VPCU
+VIN
PU1
RT8208A
PQ43 AON7410
PQ44 AON7702
PQ5 DMN601K-7
PL11 1UH/11A-PCMD063T-1R0MN
600 mils
+1.1V_DYN_S1
+1.1V_DYN
PC84 330u_2V_7343ESR6
PC213 0.1U/10V_4
PR168 0_4
PR12 10K/F_4
PR27 16.5K/F_4
PR11 232K/F_4
PR176 *2.2_8
PR34 6.65K/F_4
PR23 2.67K/F_4
PR31 10K/F_4
PR39 10K/F_4
PR45 0_4
PC21 *100P/50V_4
Vo=0.75(R1+R2)/R2
RDSon=14m ohm
Reserve for AMD tunning
24,36,37,40,41,42 HWPG
36,39,41,42 VRON
10 DYN_PWR_EN
+3VPCU
8208CS1.1V
8208RTPG1.1V
8208RTEN1.1V
8208BST1.1V_1
8208RTDH1.1V
8208RTLX2.1V
8208TON1.1V
8208RTDL1
8208VOUT1
8208RTFB1.1V
8208RTD10.1V
PC186 1U/6.3V_4
PC34 1U/6.3V_4
PR14 2_6
PC12 0.1U/25V_4
PC71 2200P/50V_4
PC70 0.1U/25V_4
PC68 4.7U/25V_8
PC6 *0.22U/10V_4
PC204 *1500P/50V_4
PC50 *0.33U/6.3V_4
DYN_PWR_EN | High | Low
+1.1V_DYN | 0.95V | 1.25V
+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 7A
OCP minimum: 9A
PU13
RT8209A
PQ61 AON7410
PQ60 AON7702
PL14 2.2uH/8A
600 mils
+1.1V_S2
+1.1V
PC237 390U/2.5V_6X5.8ESR10
PC238 0.1U/10V_4
PR150 10_6
PC178 1U/6.3V_4
PC174 1U/6.3V_4
PR147 2_6
PC171 0.1U/25V_4
PC241 2200P/50V_4
PC242 0.1U/25V_4
PC240 4.7U/25V_8
PR154 12.1K/F_4
PR156 0_4
PR146 10_4
PR145 *1M/F_4
PR144 200K/F_4
PR209 *2.2_8
PC239 *1500P/50V_4
PR153 4.7K/F_4
PR155 10K/F_4
PC172 *100P/50V_4
Vo=0.75(R1+R2)/R2
RDSon=14m ohm
RTBST_1
RTBST
RTDH
RTLX
RTTON
RTDL
RTFB
RTILIM
RTEN
RVDD
HWPG_S2A
1.1 Volt +/- 5%
Countinue current:0.2A
Peak current:0.5A
PU10 RT9025
+1.1VS5
PC153 10U/6.3V_8
PC151 0.1U/10V_4
PC155 10U/6.3V_8
PC154 10U/6.3V_8
PC156 0.1U/10V_4
PC150 0.33U/6.3V_4
PC152 1U/6.3V_4
PR136 10K/F_4
PR134 0_4
PR137 38.3K/F_4
PR135 100K/F_4
36,42 S5_ON
1.1VADJ
R1
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

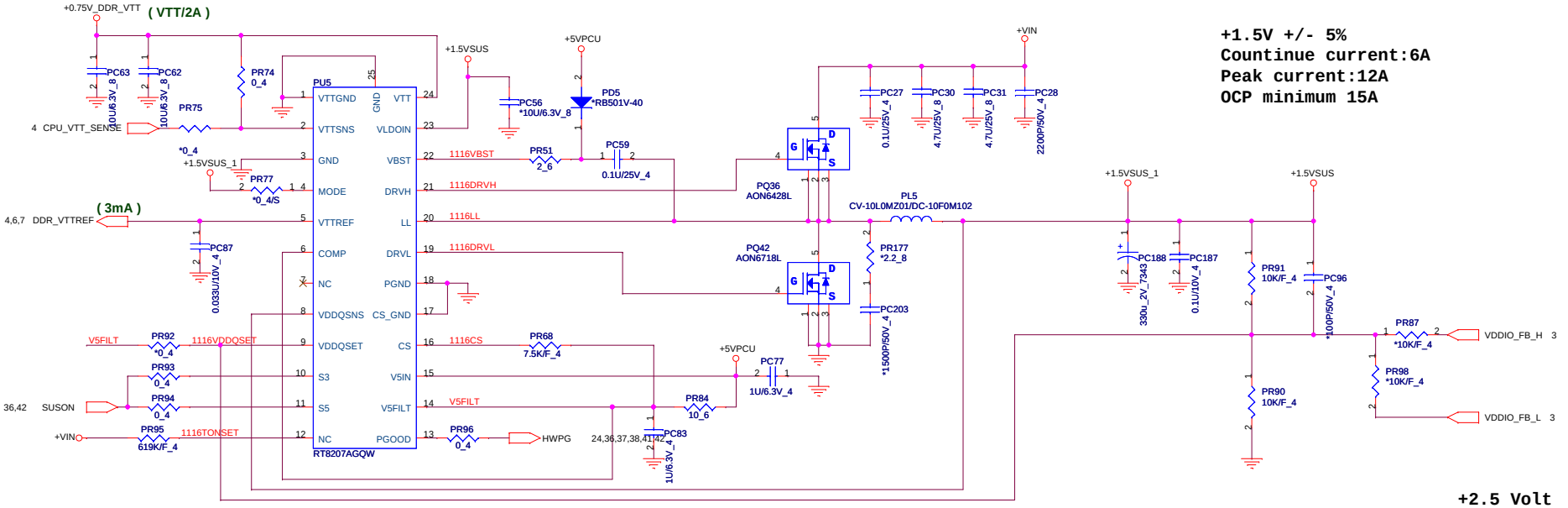
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

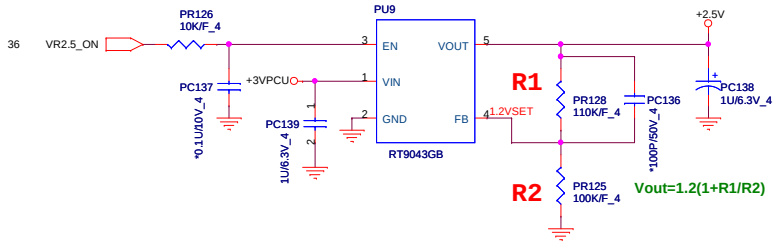


PROJECT : LX89 Quanta Computer Inc.		
NB5/RD2	Size C	Document Number CPU_CORE(ISL6265) Rev 1A
	Date: Monday, September 28, 2009	Sheet 39 of 46

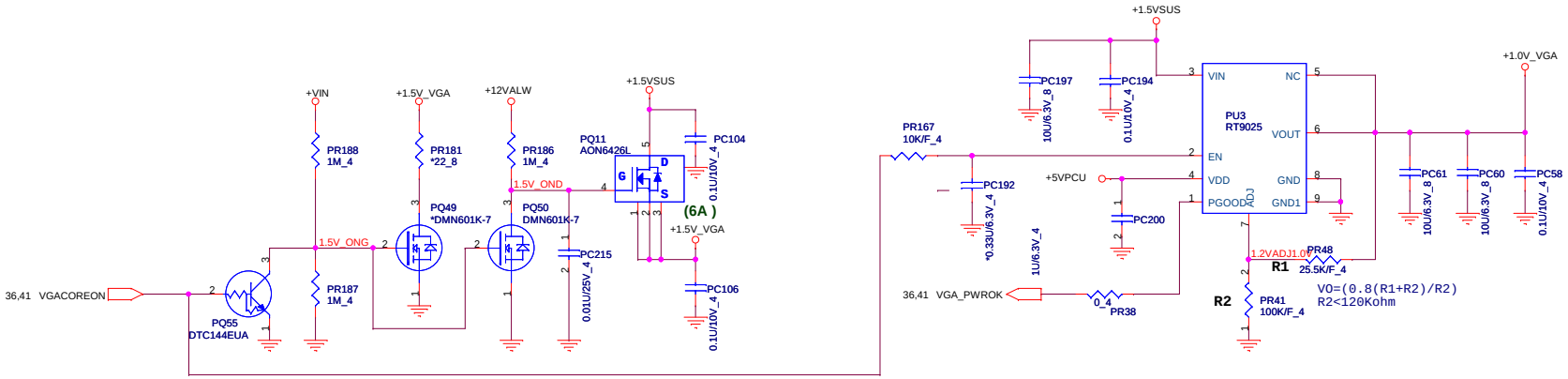
+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA



+1.0V +/- 5%
Countinue current:1.5A
Peak current:3A



PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

N85/RD2

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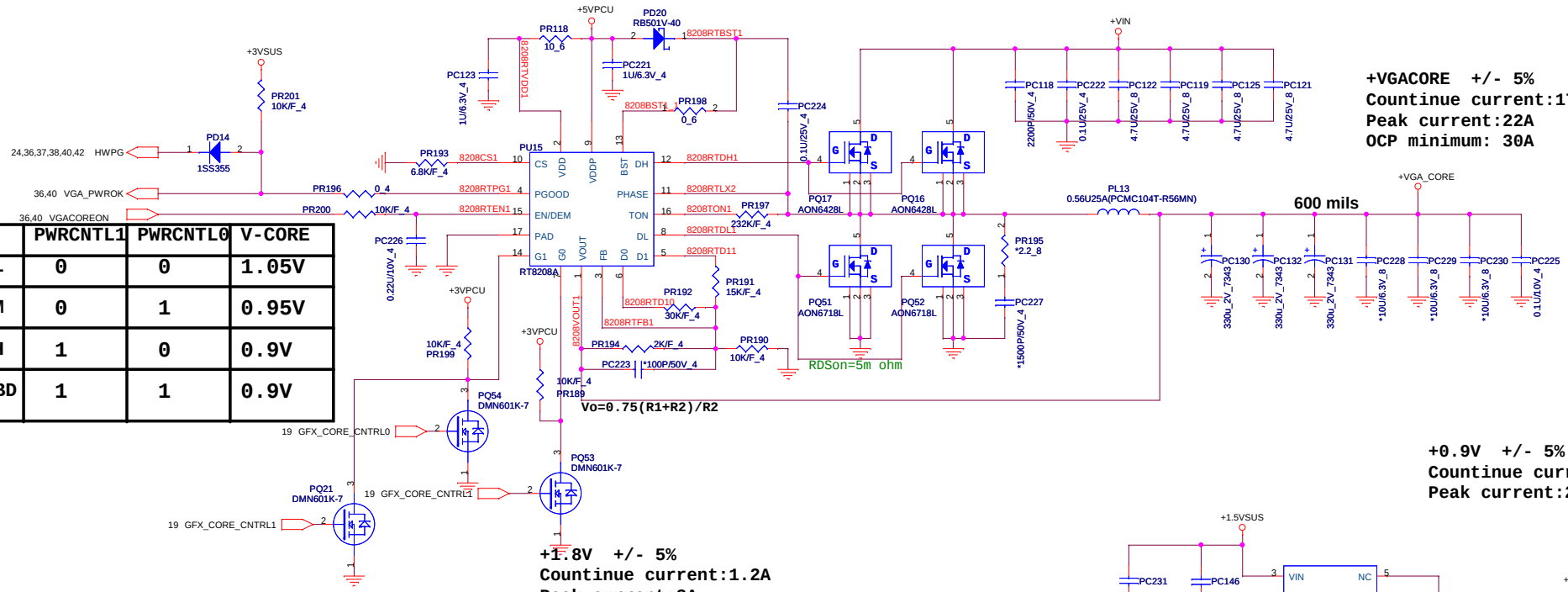
VGA Core

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V



PROJECT	LX89
Quanta Computer Inc.	
Size	Custom
Document Number	+VGACORE (RT8208/1.8V)
Rev	1A
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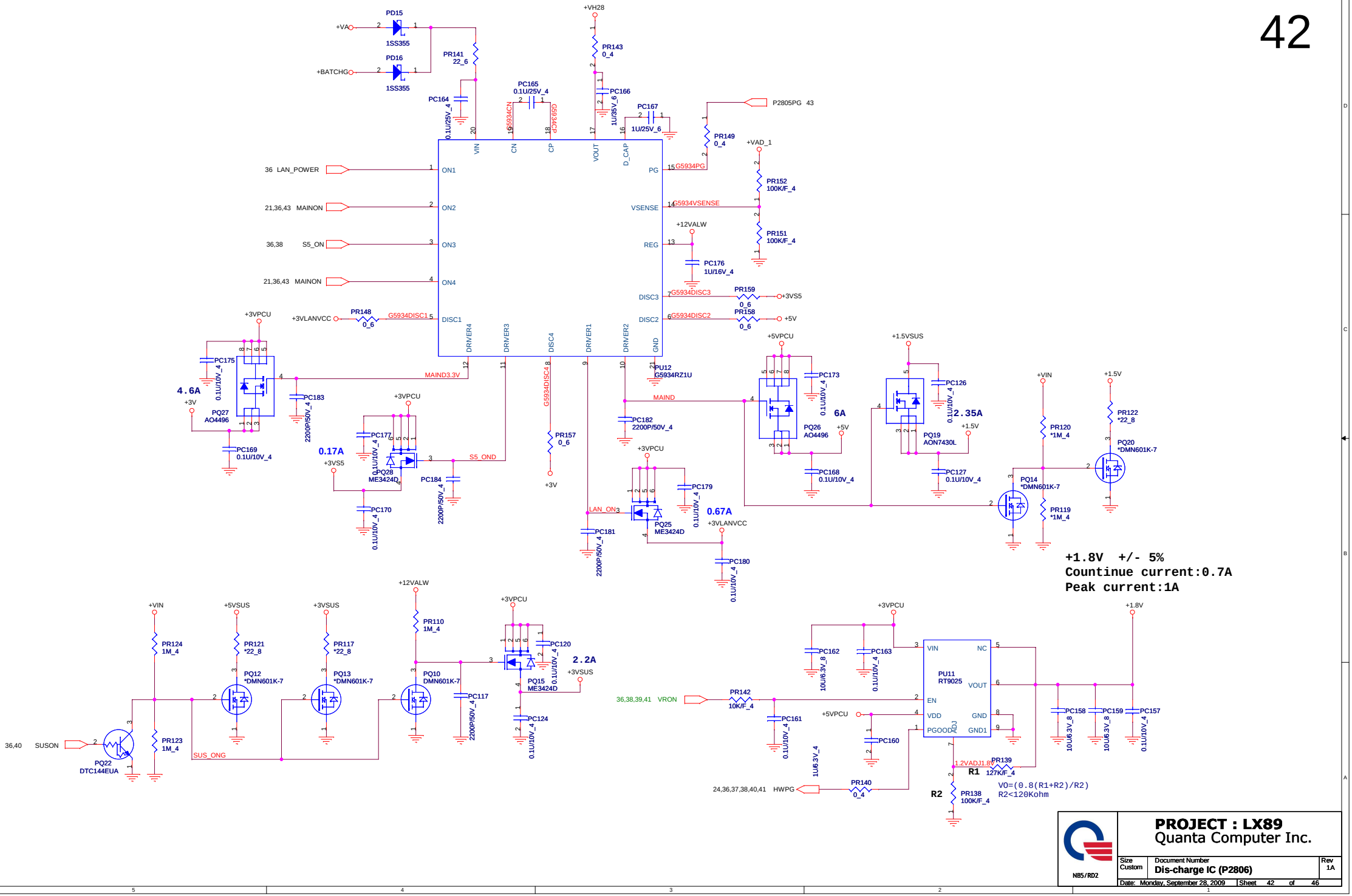

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N85/RD2	Size: Custom	Document Number: Dis-charge IC (P2806)	Rev: 1A
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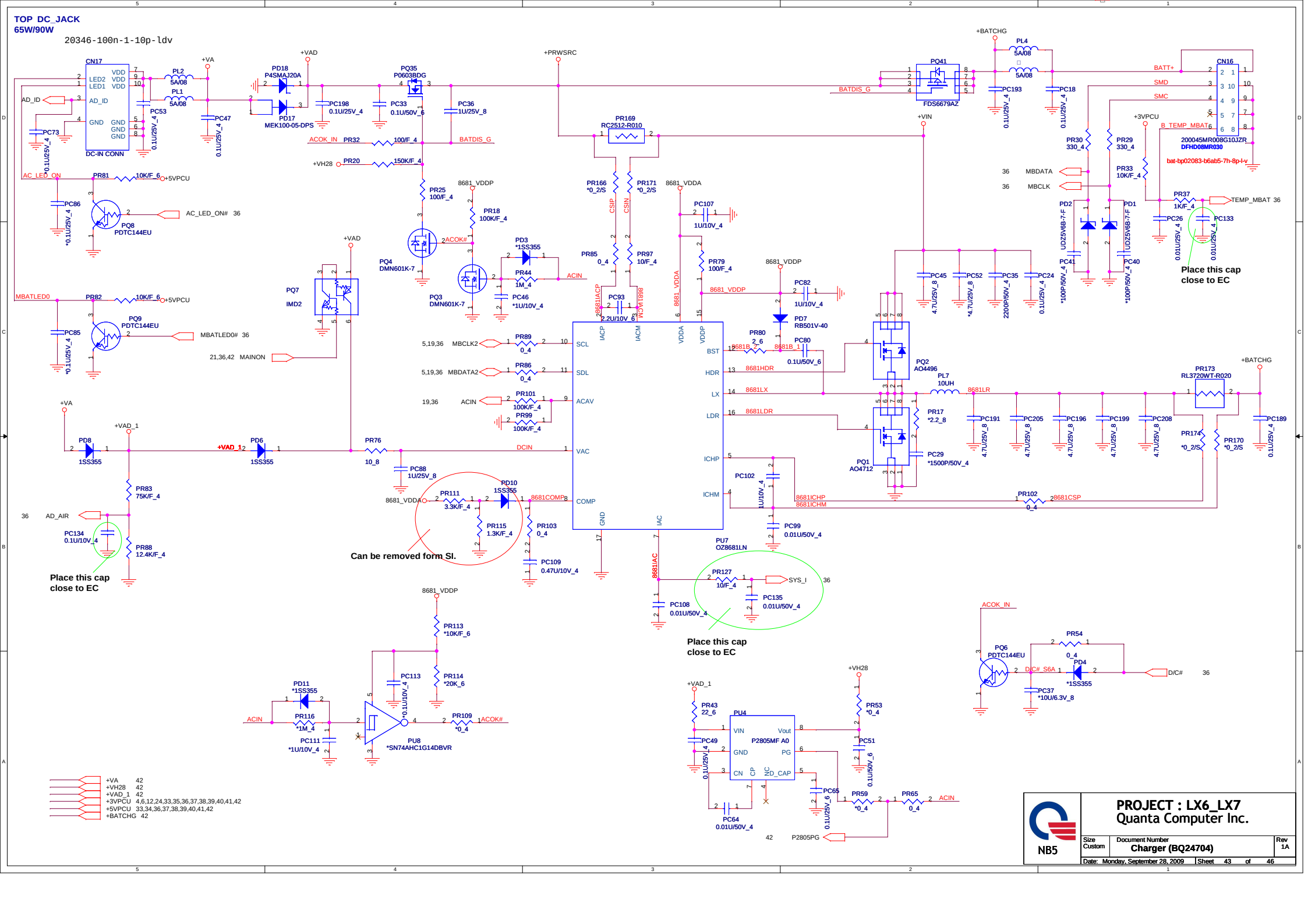
TOP DC_JACK
65W/90W

20346-100n-1-10p-ldv



PROJECT : LX6_LX7	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: Charger (BQ24704)	Rev: 1A
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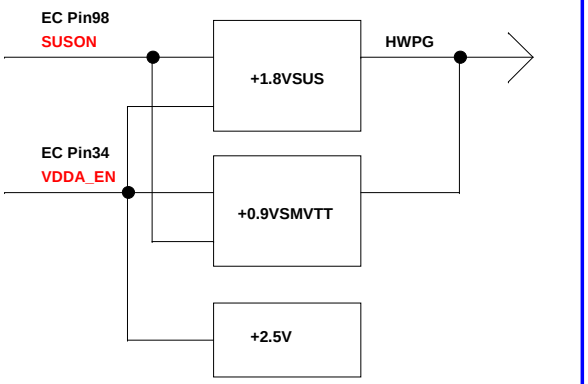
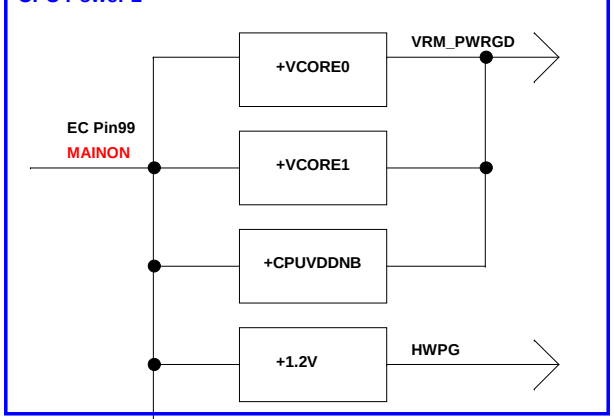
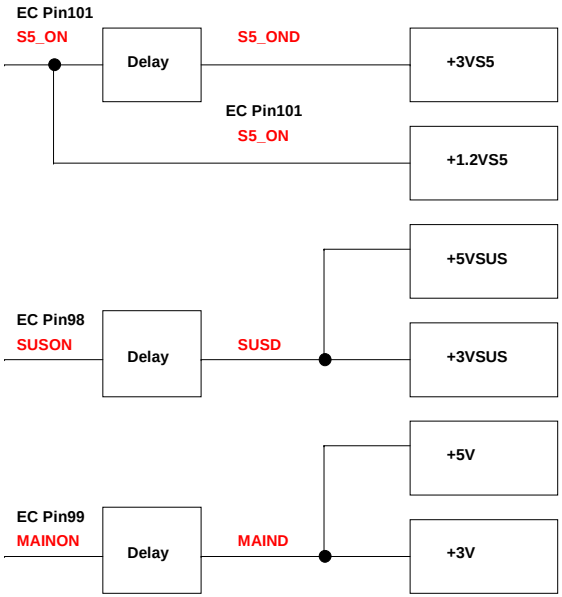
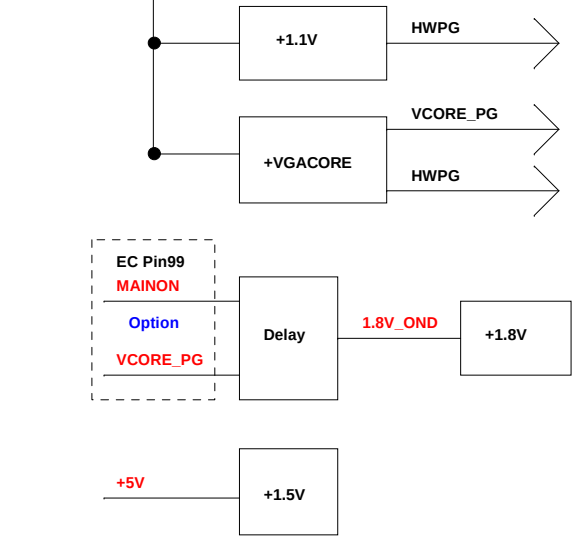
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN 3.3V → NB_PWRGD_IN 1.8V

NB5/RD2

PROJECT : LX89
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Custom	Power control	1A

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Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

Custom<Doc>
N85/RD2

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Quanta Computer Inc.

Size	Document Number	Rev
		1A

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