Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_PM+ICH9-M core logic

2009-02-13

REV : 1.0

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Issued Date	2008/12/10	Deciphered Date	2008/12/10

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Title: *Cover Sheet*

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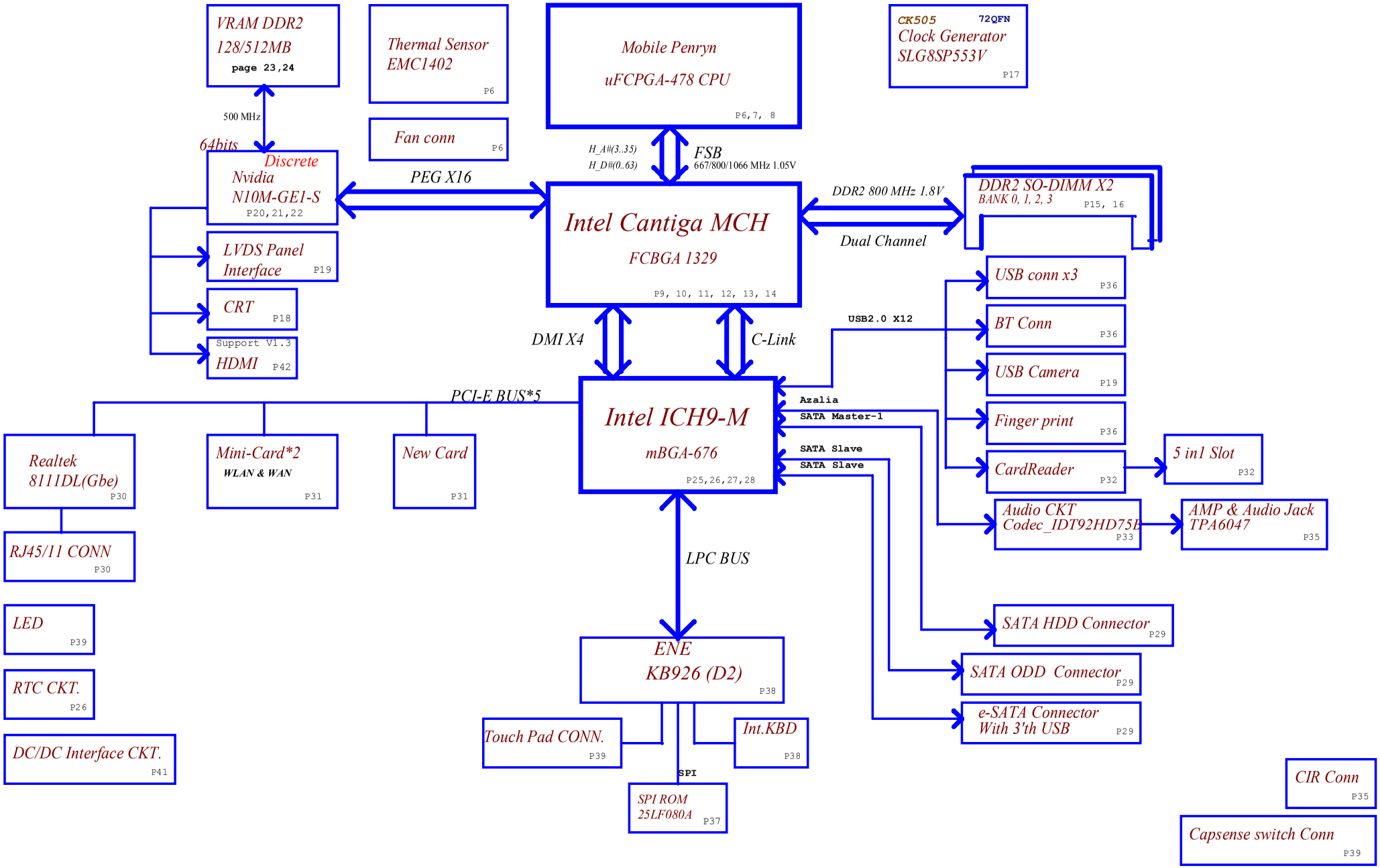
Montevina Consumer Discrete



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Title: **Block Diagram**

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Voltage Rails

O MEANS ON

X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM

NB	SA00002JJ80	R1	FRU
NB	SA00002JJE0	R3	
SB	SA00002JH50	R1	FRU
SB	SA00002JHB0	R3	

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

Symbol Note :

: means Digital Ground

: means Analog Ground

USB assignment:

USB-0 Right side(with ESATA)
USB-1 Left side
USB-2 Left side
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express card
USB-10 X
USB-11 X

PCIe assignment:

PCIe-1 TV tuner/WWAN/Robeson
PCIe-2 X
PCIe-3 WLAN
PCIe-4 GLAN (Marvell)
PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	N10M Thermal Sensor	N10M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI	HDCP
DDC2_DATA DDC2_CLK	N10M	V	X	X	X
3VDDCDA 3VDDCCL	N10M	X	V	X	X
HDMIDAT_VGA HDMICLK_VGA	N10M	X	X	V	X
HDCP_SDA HDCP_SCL	N10M	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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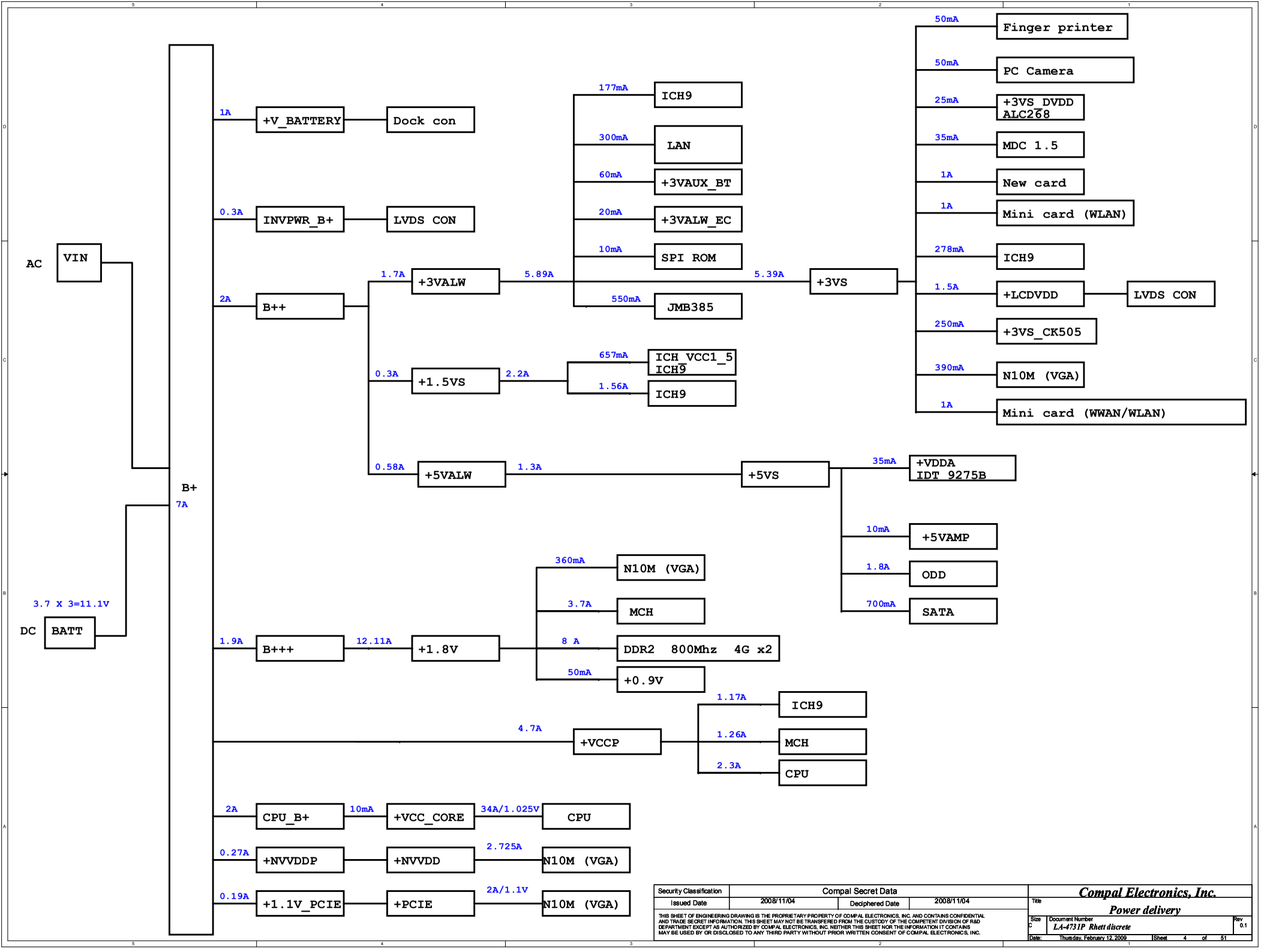

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Title: *Power delivery*

Size: C | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

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Compal Electronics, Inc.

Title: **Power sequence**

Size	Document Number	Rev
Custom	LA-4731P Rhett discrete	0.1

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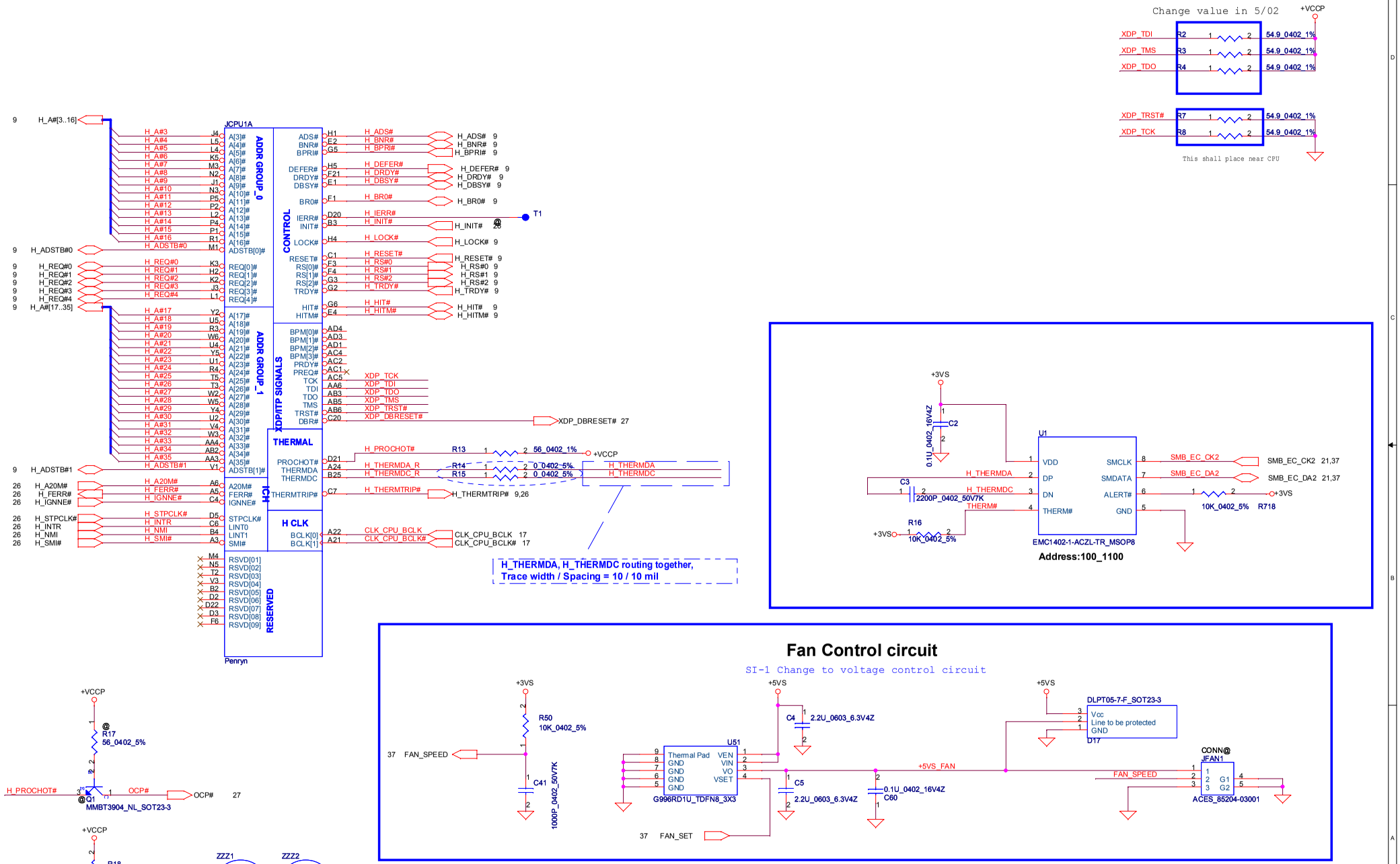

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Compal Electronics, Inc.

Title: Penryn(1/3)-AGTL+/ITP-XDP

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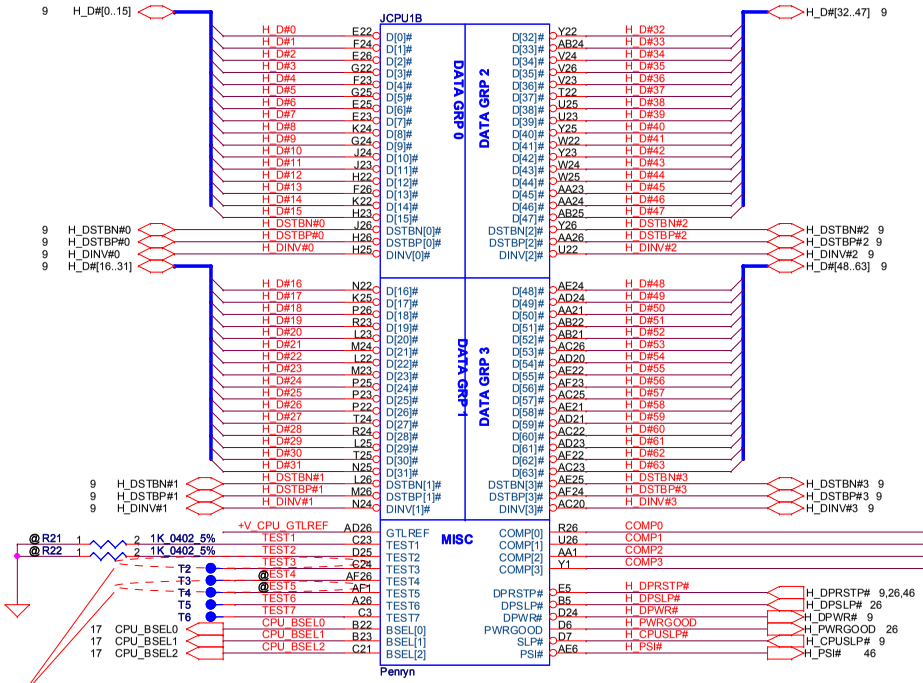
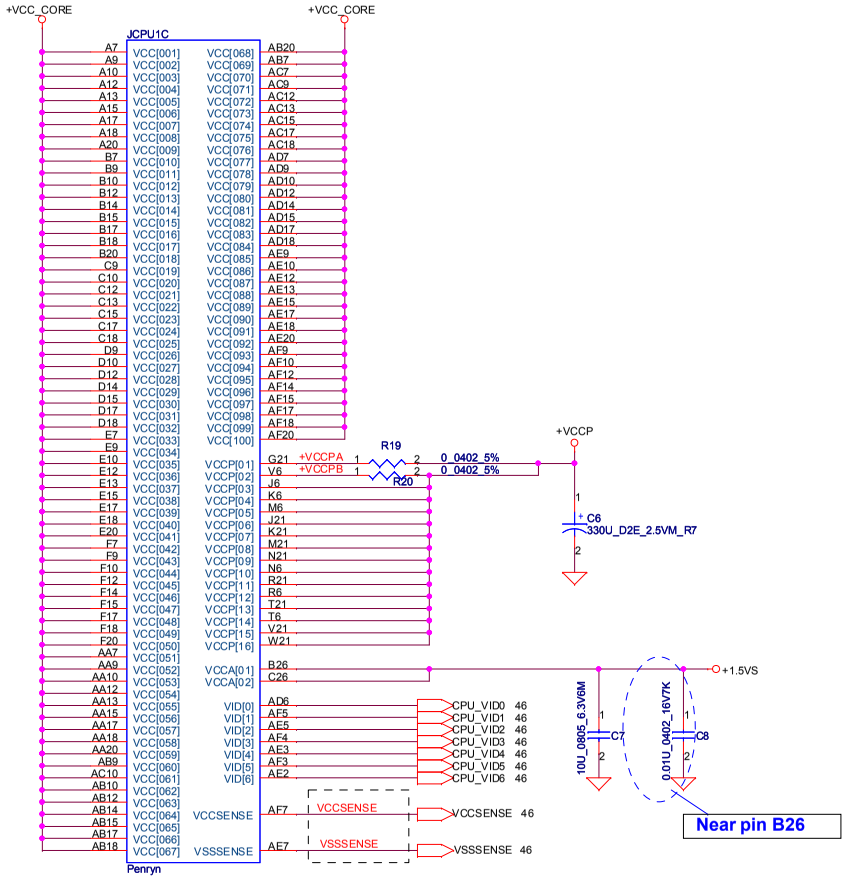


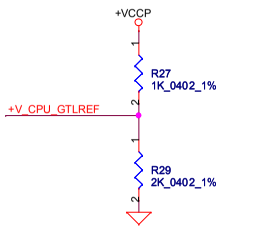
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

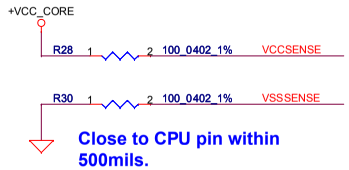
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils.
The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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Title: **Compal Electronics, Inc.**
Penryn(2/3)-AGTL+/ITP-XDP

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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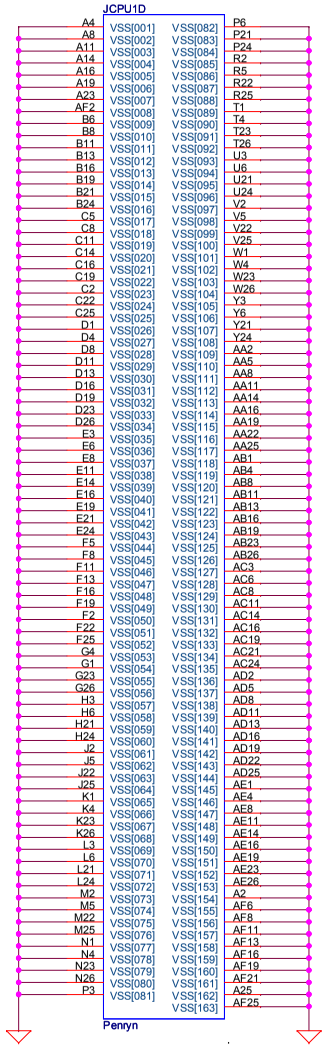

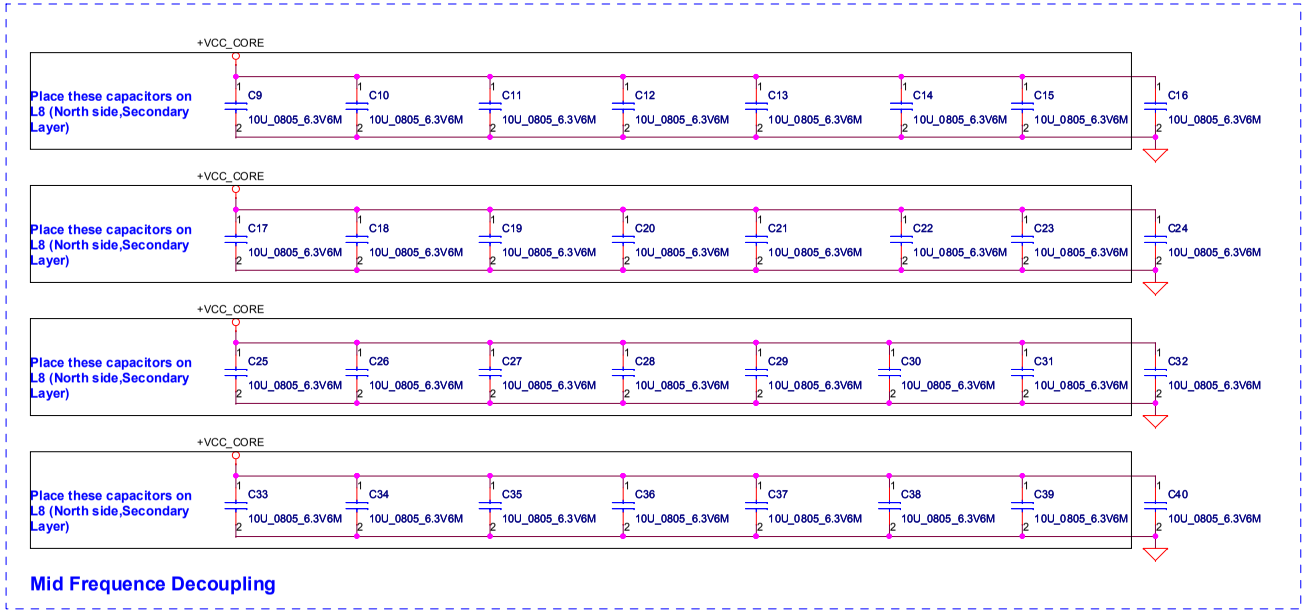

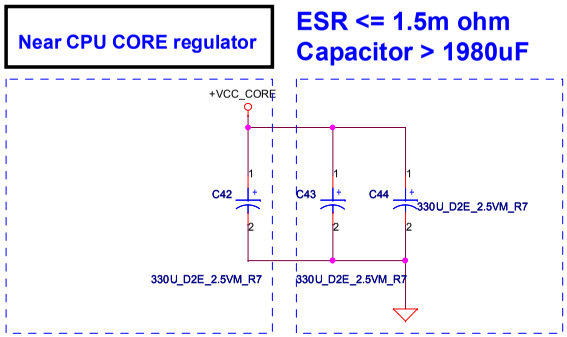

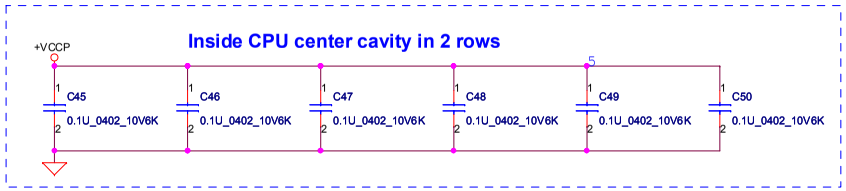

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Title: **Compal Electronics, Inc.**

Penryn(3/3)-AGTL+/ITP-XDP

Size: Custom | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

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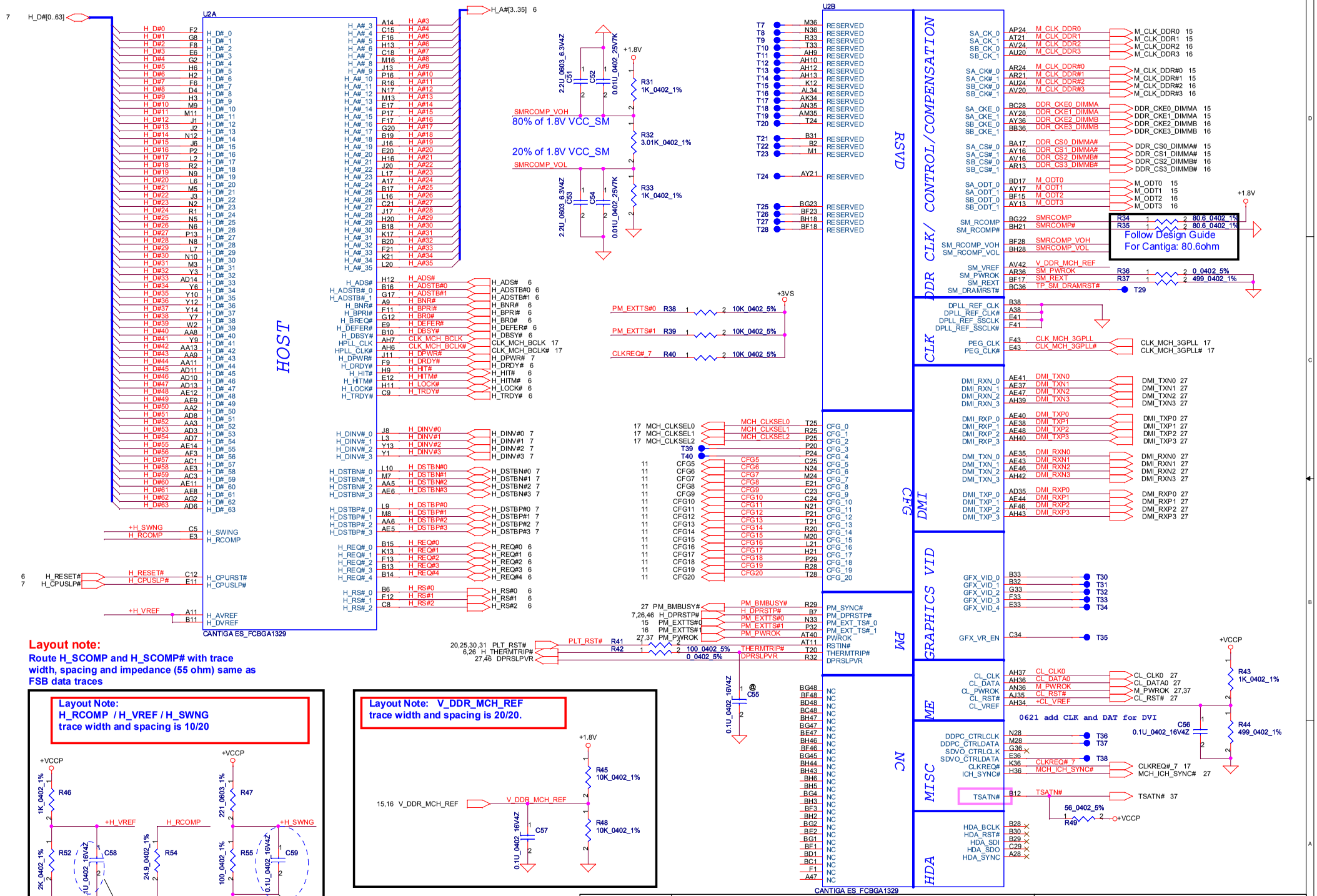

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Title: Cantiga(1/6)-AGTL/DMI/DDR

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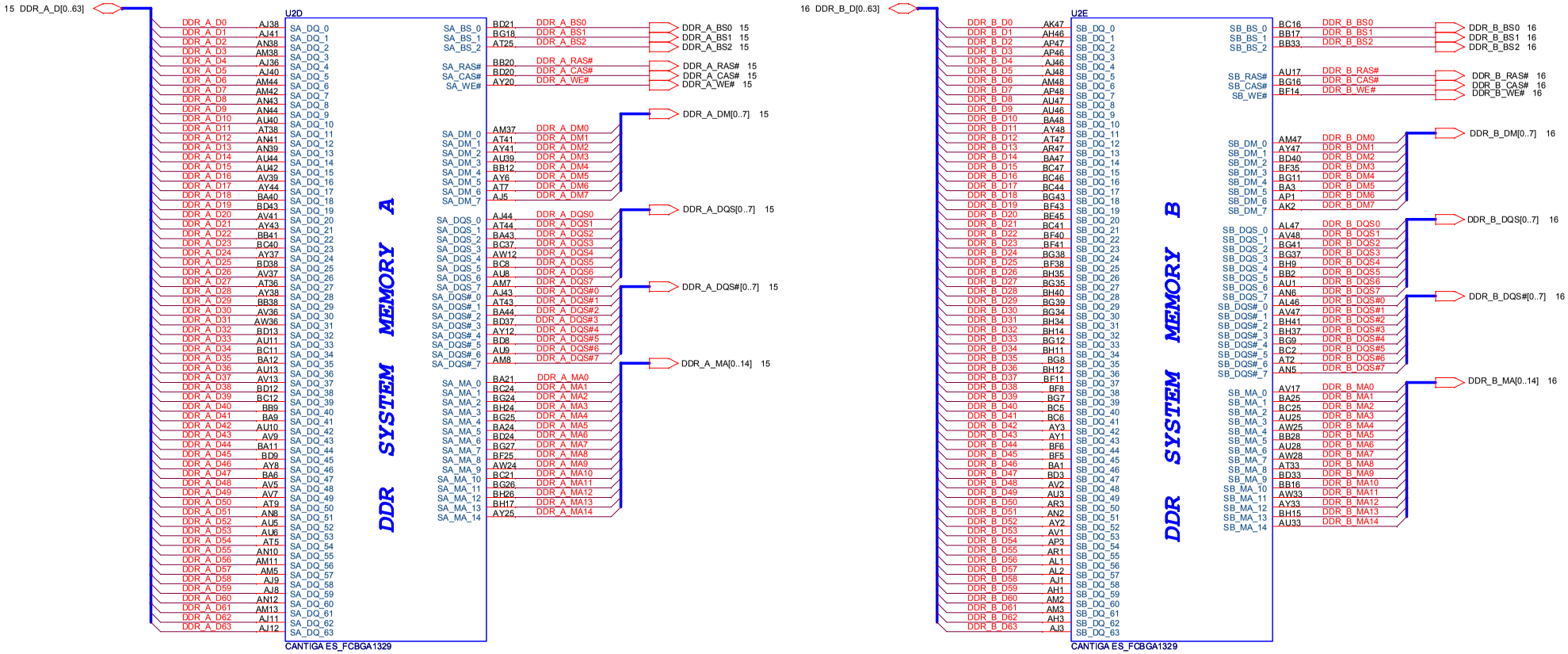

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Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

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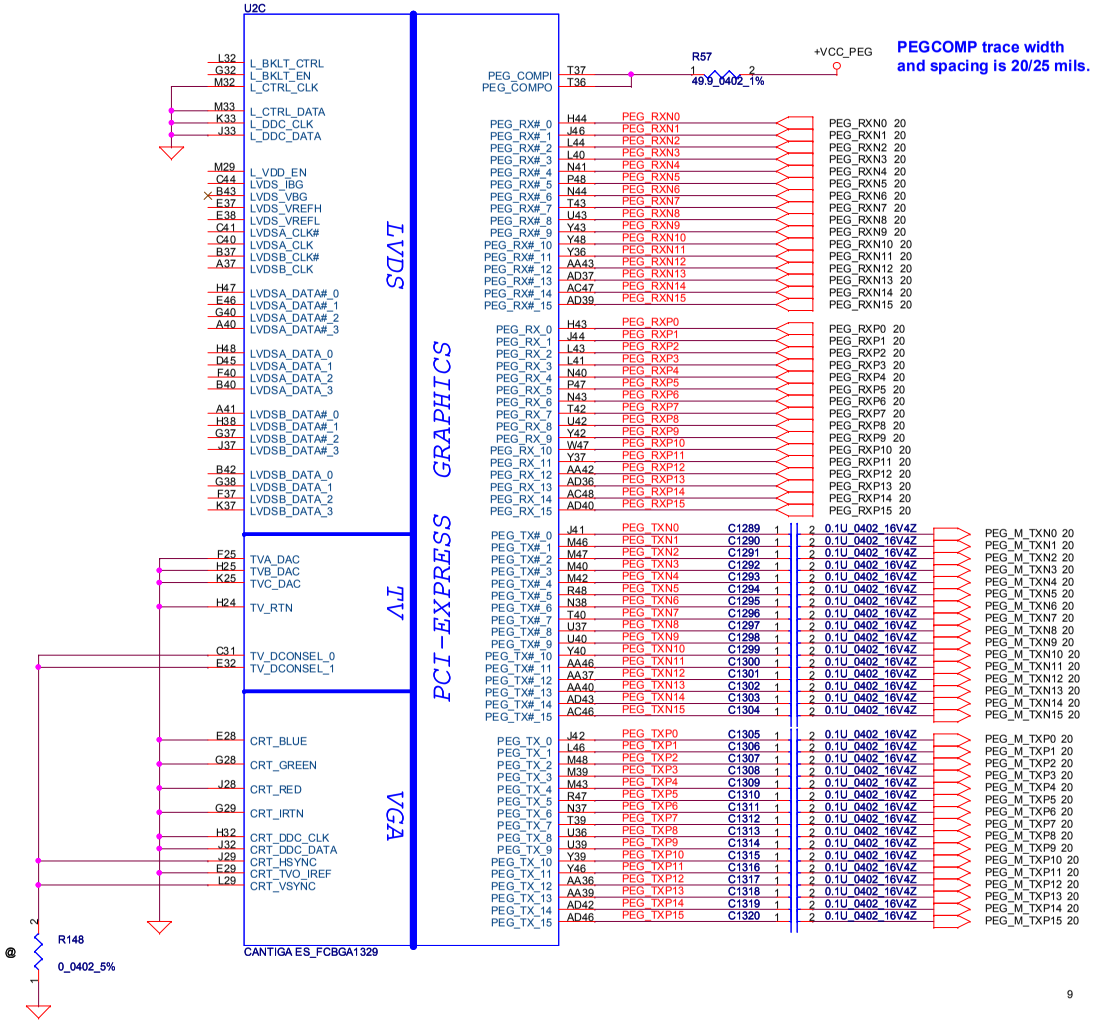
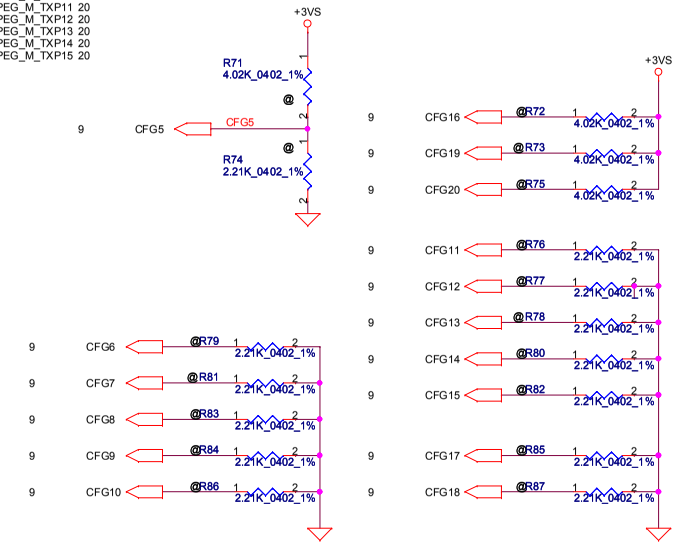


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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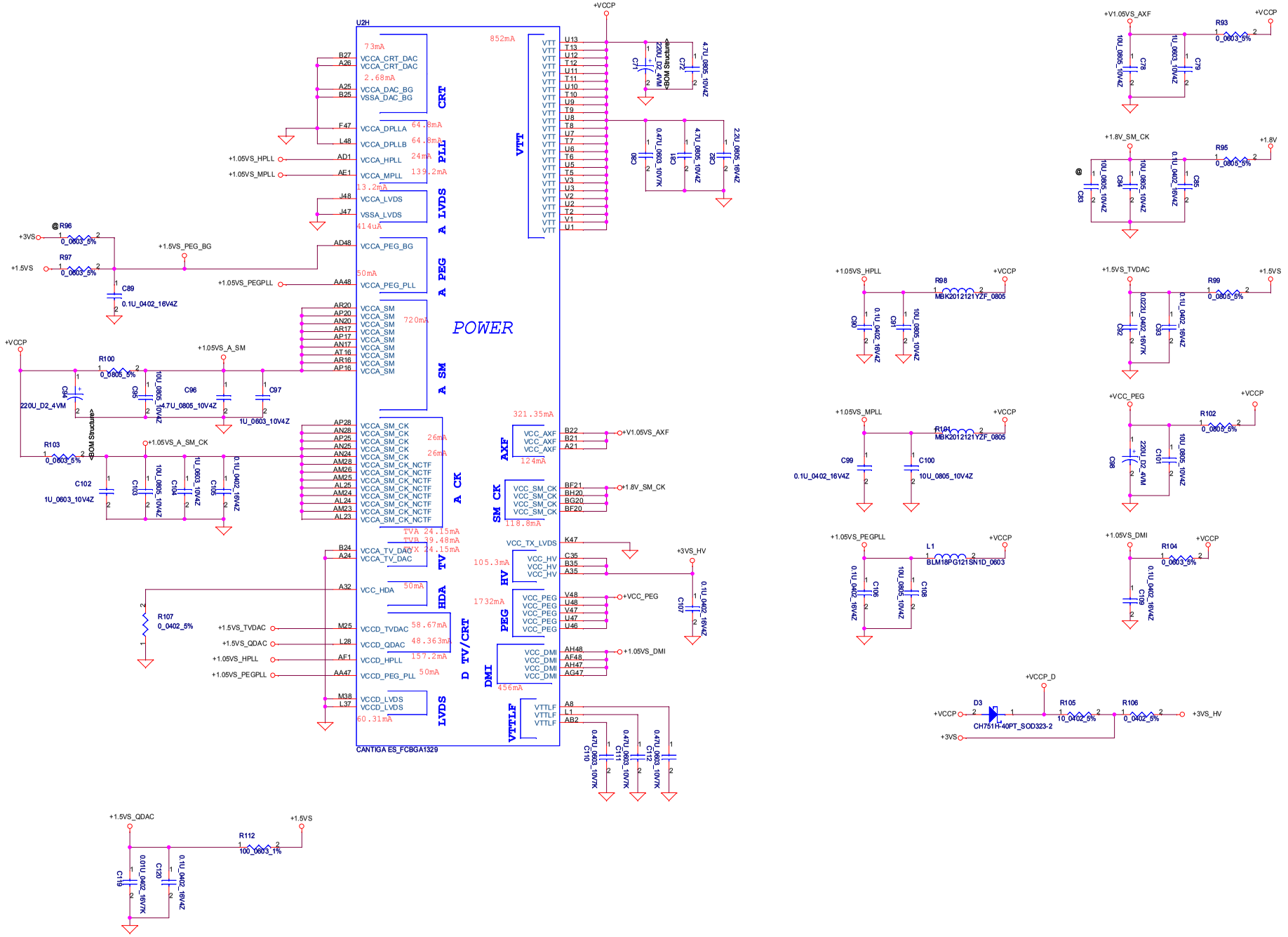

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Title: **Cantiga(4/6)-PWR**

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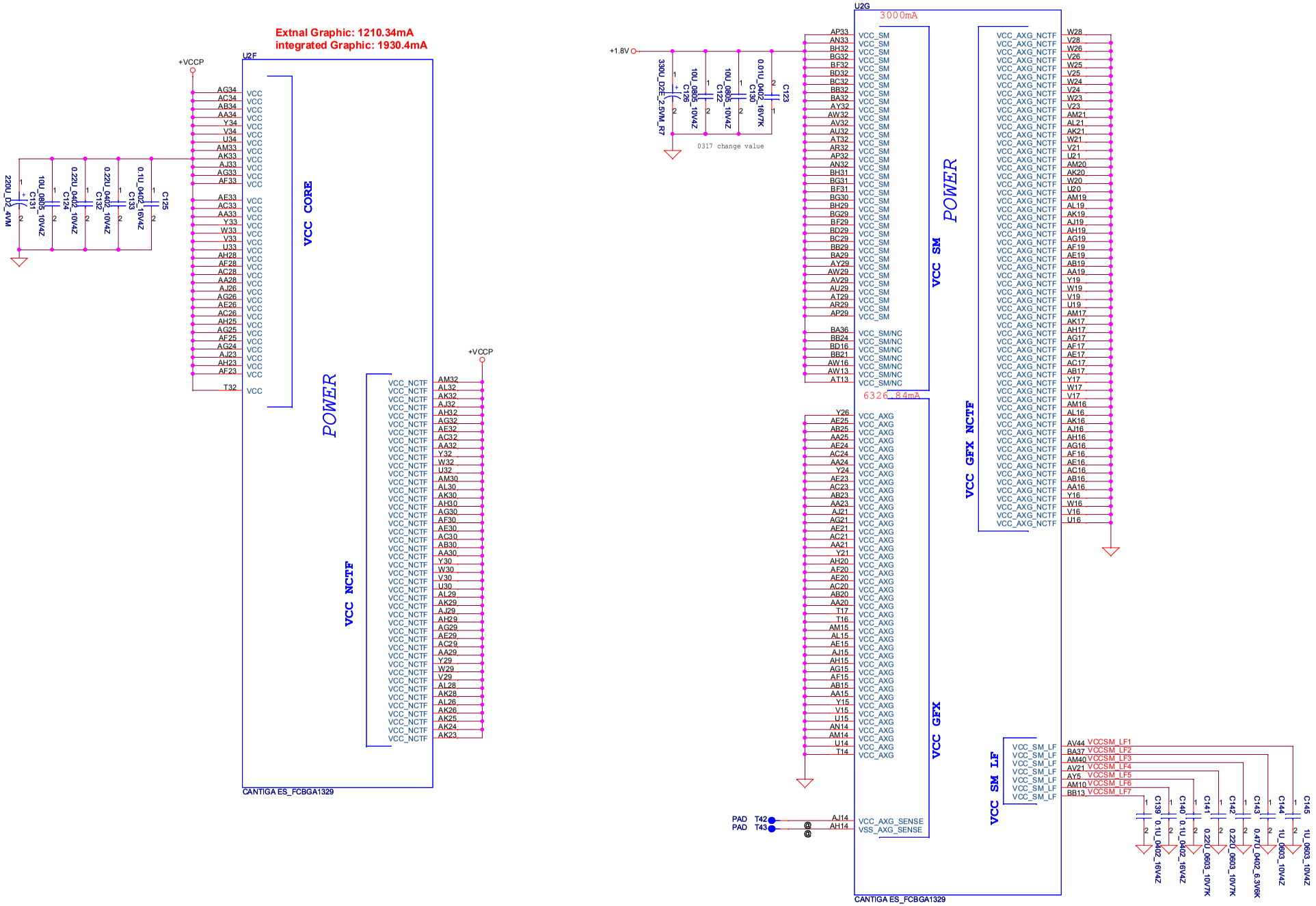

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Title: **Cantiga(5/6)-PWR/GND**

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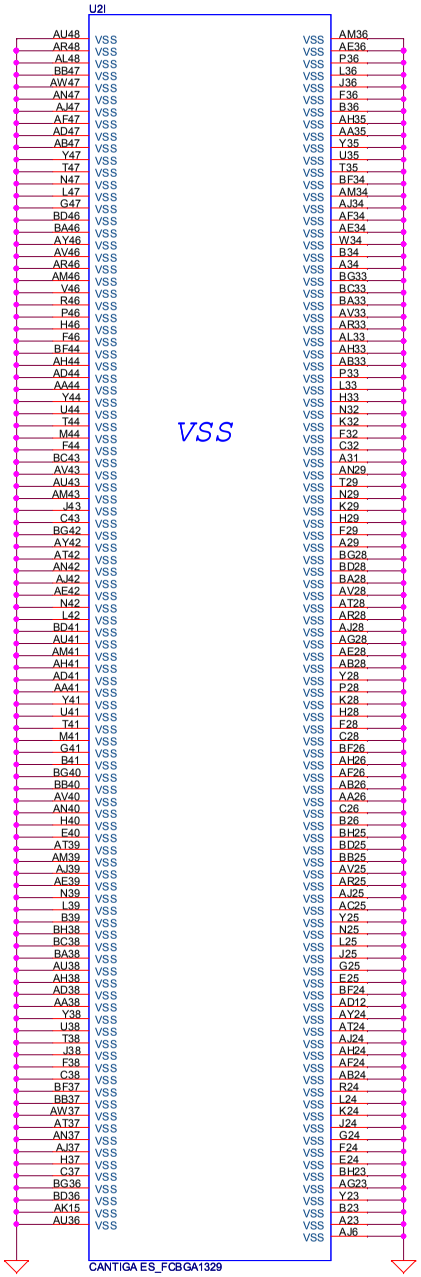

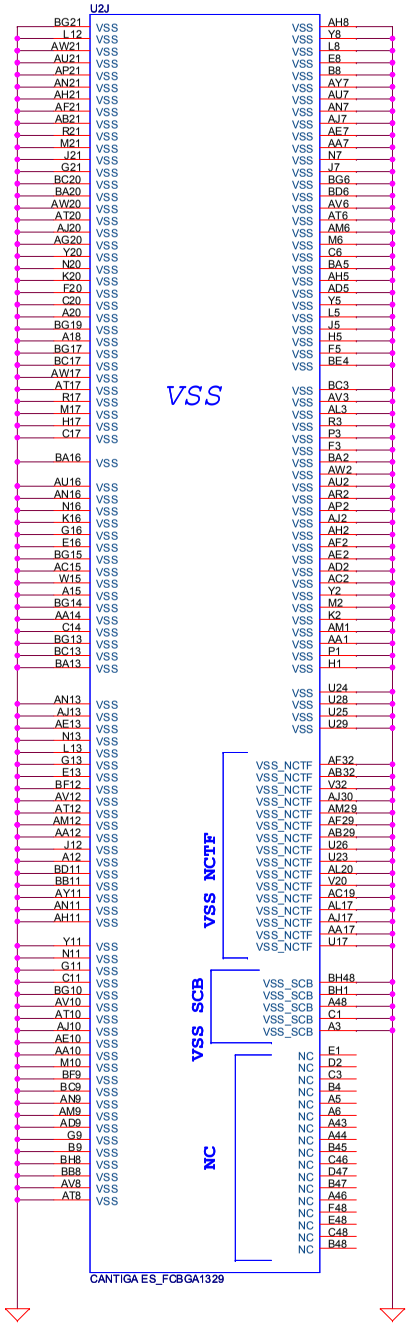

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Title: **Cantiga(6/6)-PWR/GND**

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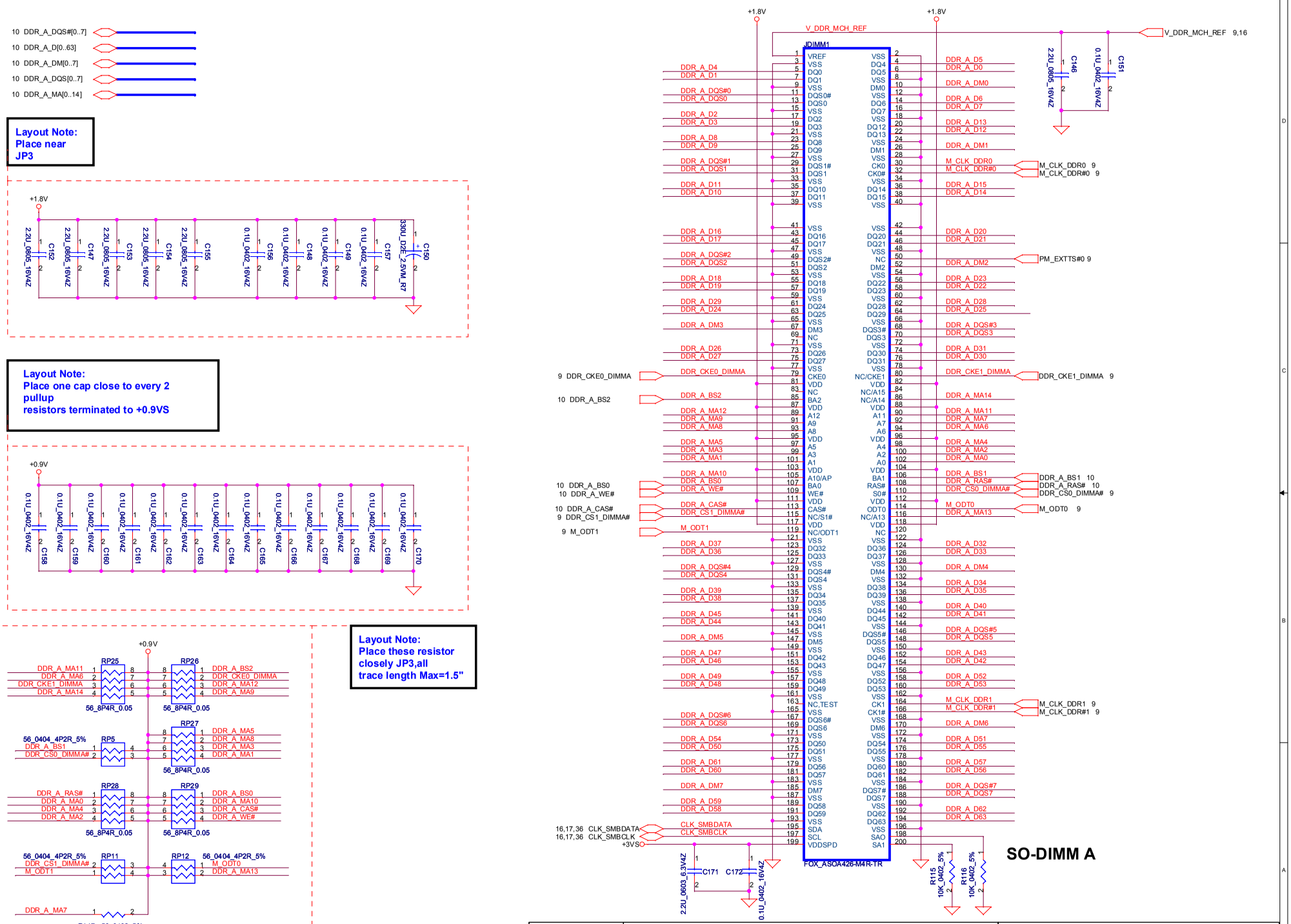

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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

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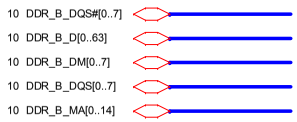
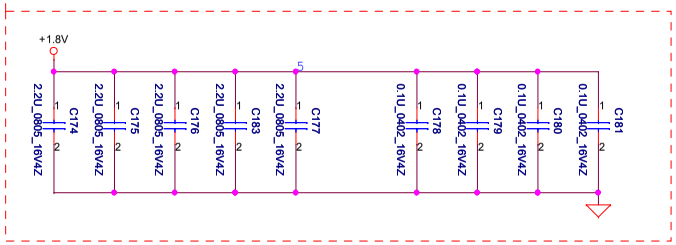
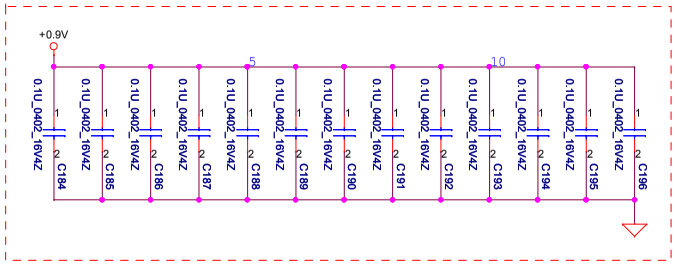


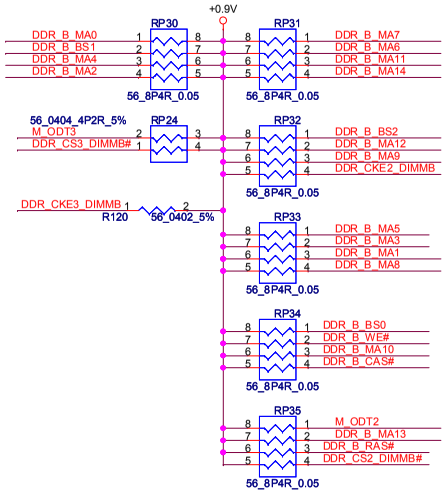
Layout Note:
Place near JP10

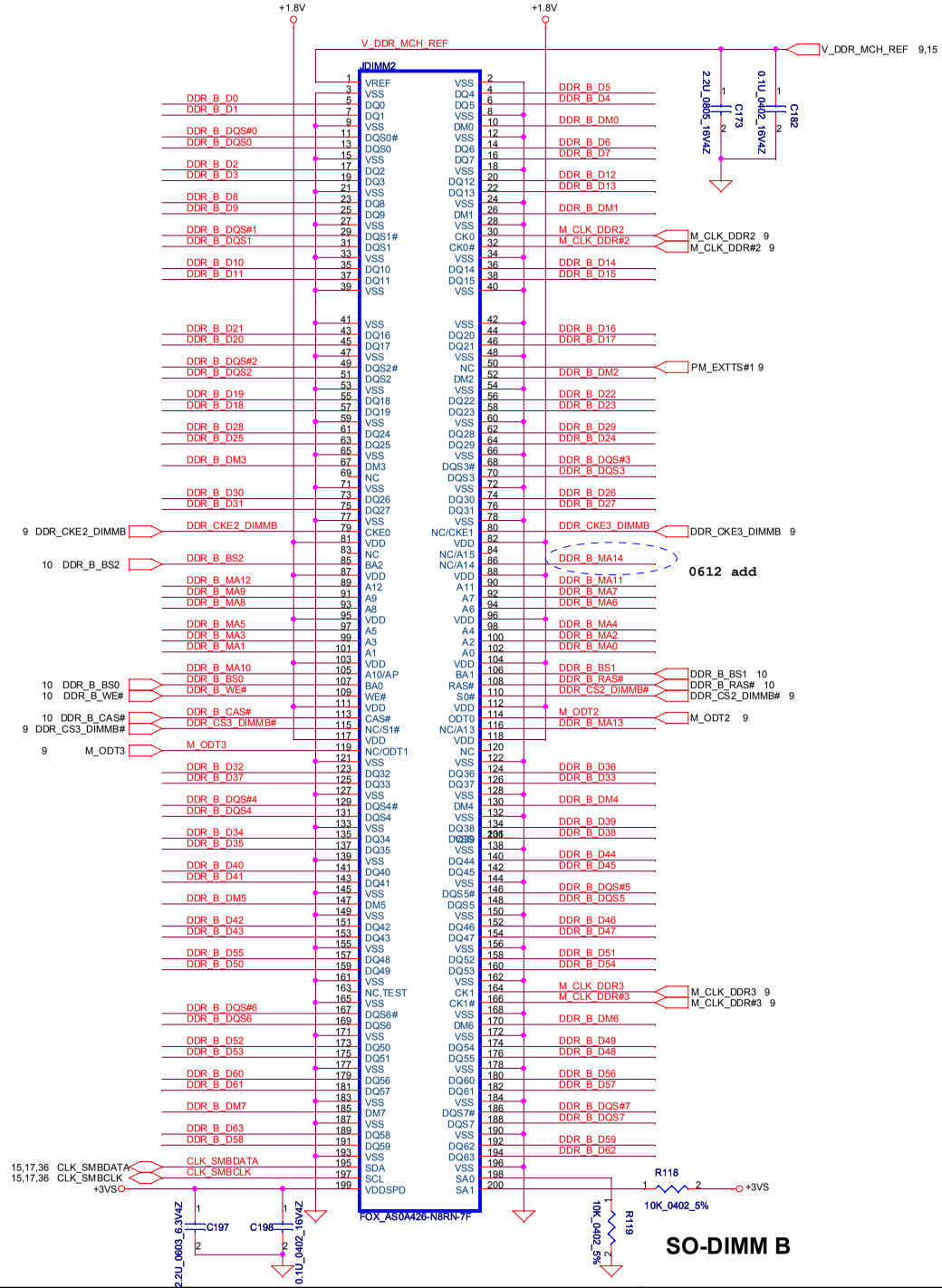


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size: | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 16 of 51

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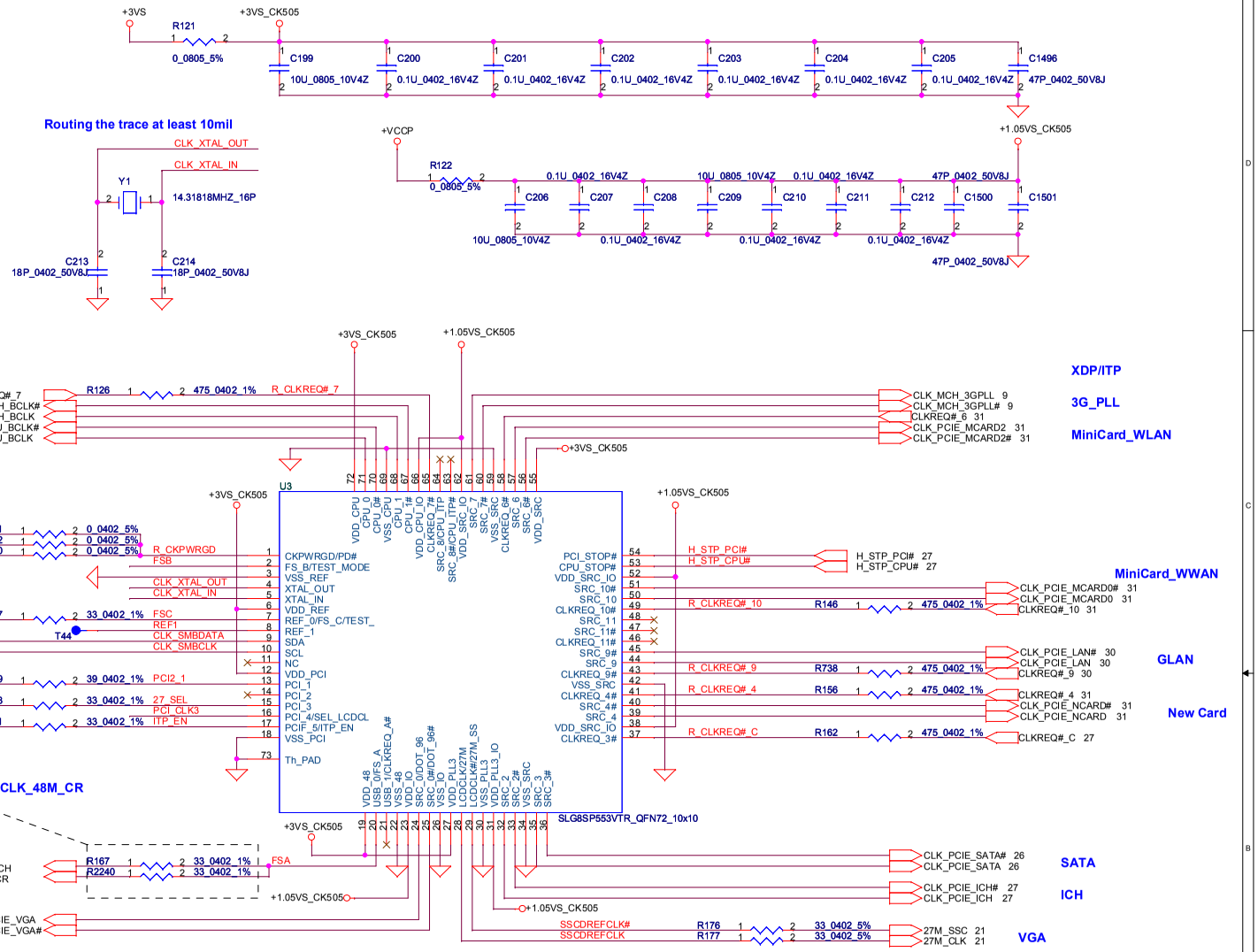
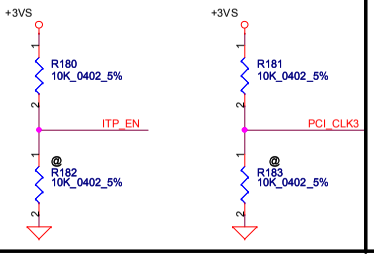
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#	V
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)	V



Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: Clock Generator CK505

Size: | Document Number: LA-4731P Rhett discrete | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 17 of 51

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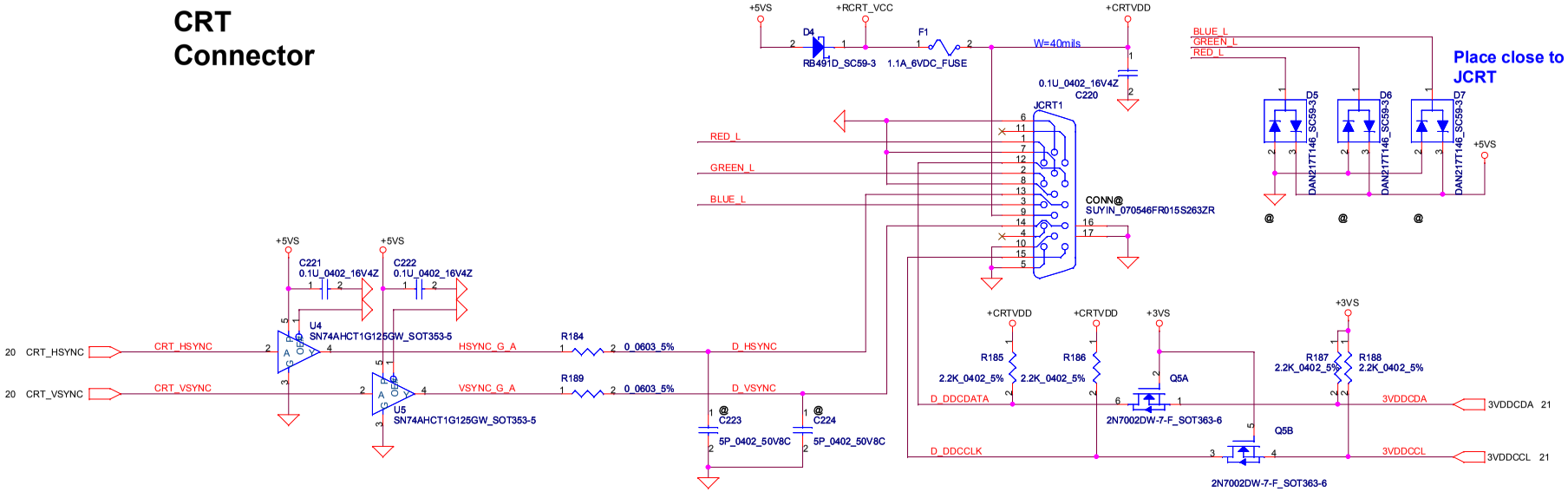
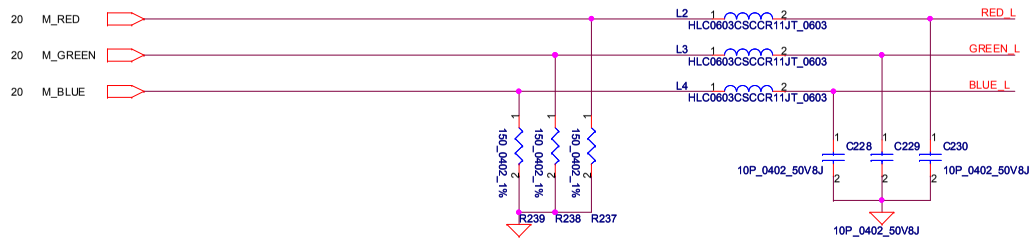
CRT Connector





Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: **CRT Connector**

Size | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 18 of 51

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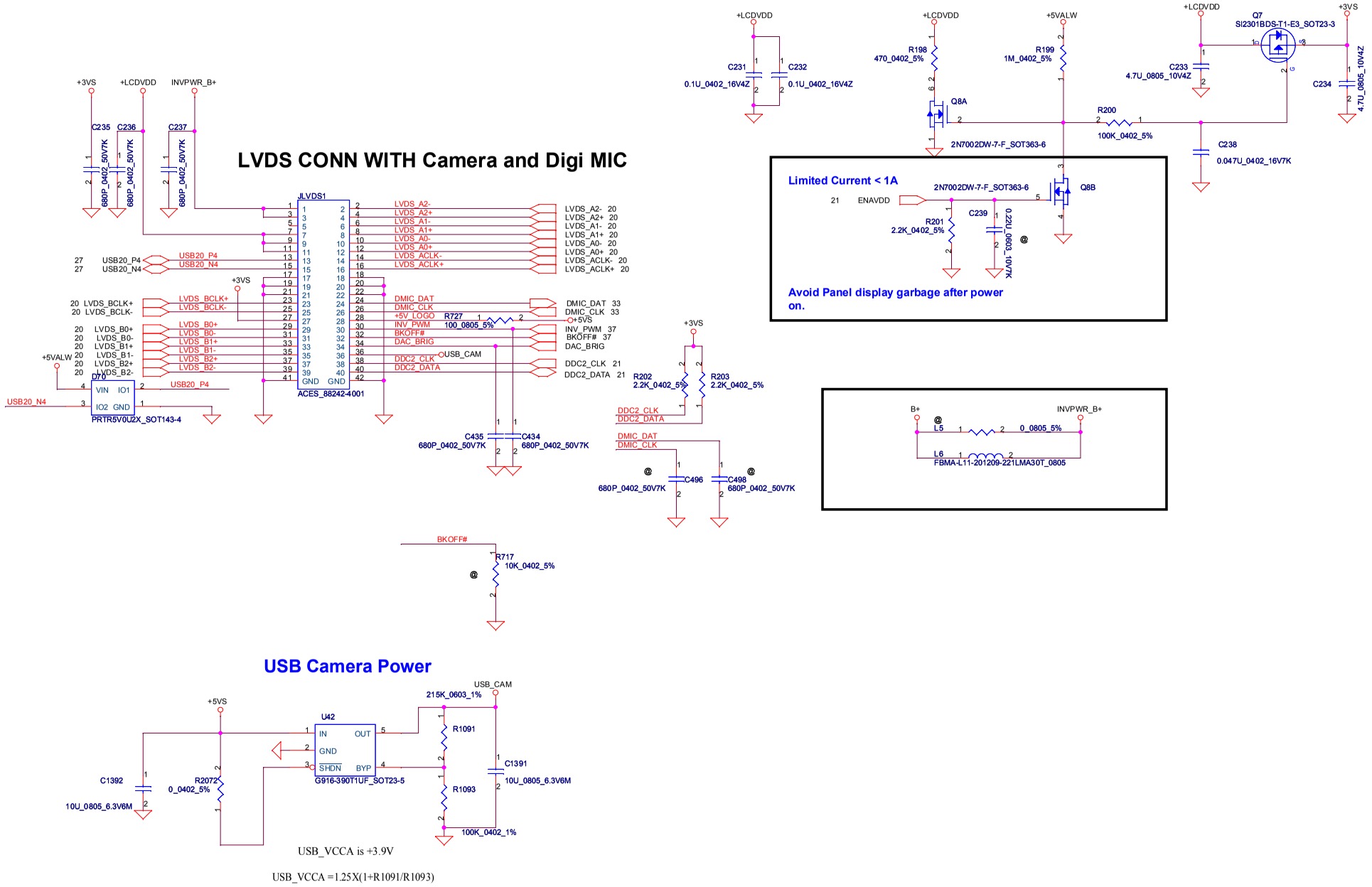

Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: **LCD CONN.**

Size | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 19 of 51

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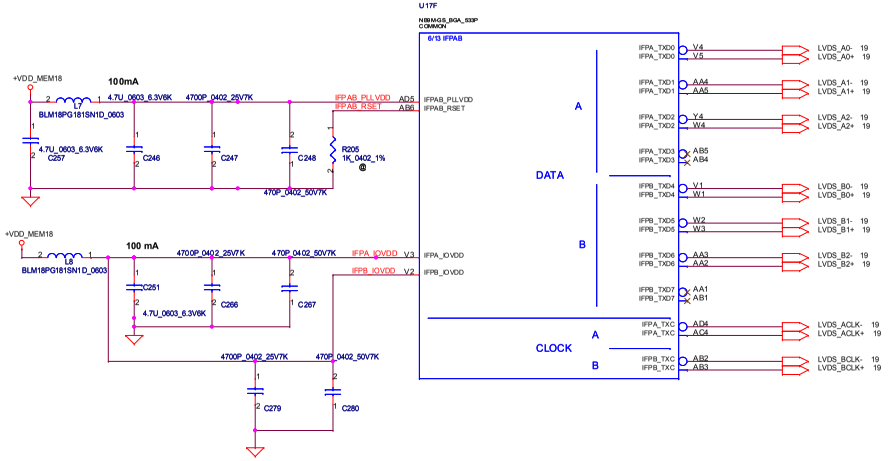
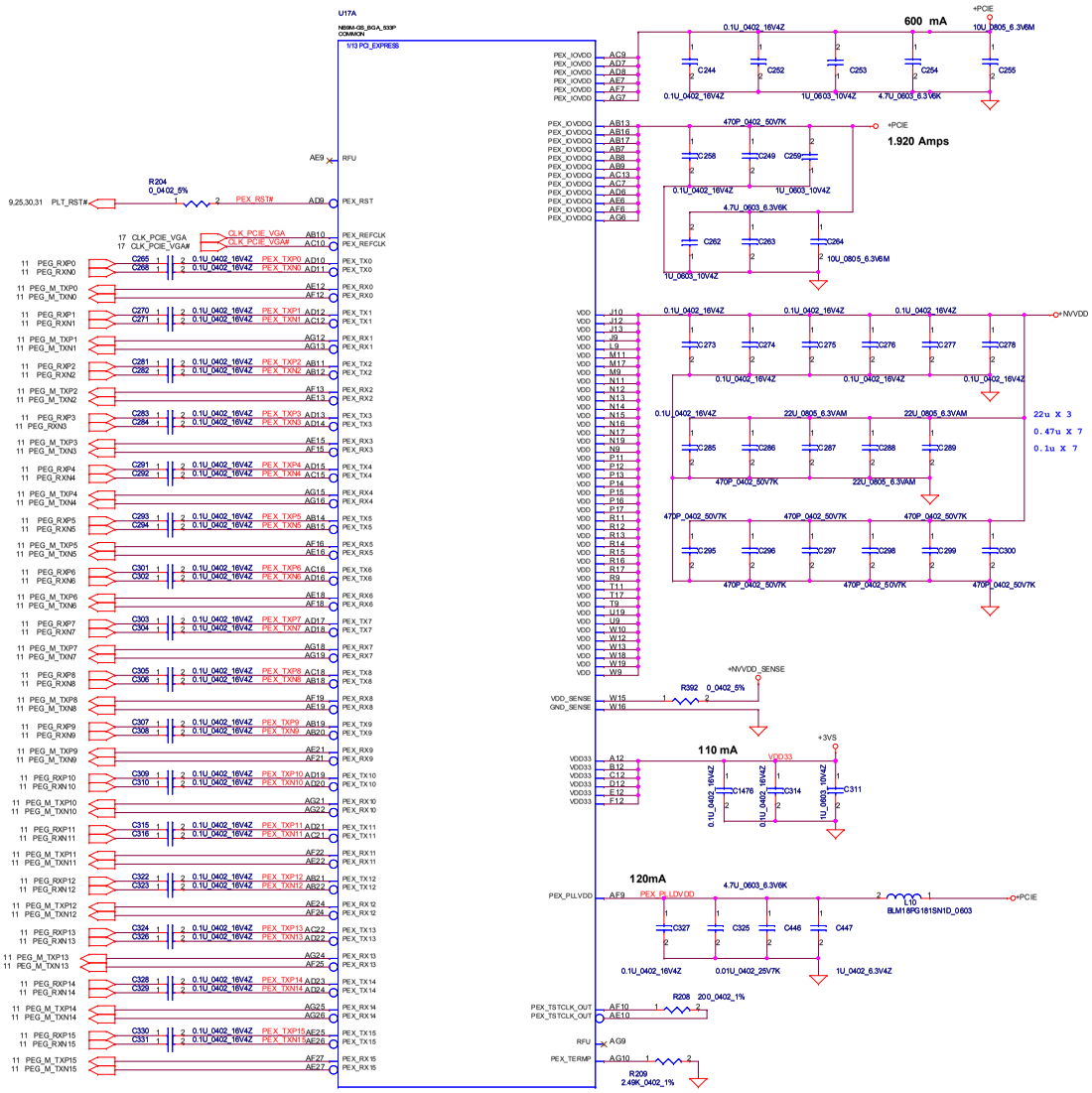
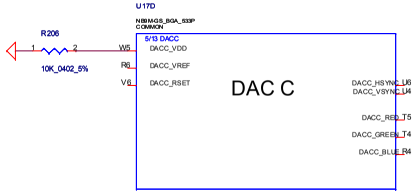
LVDS & DAC Interface

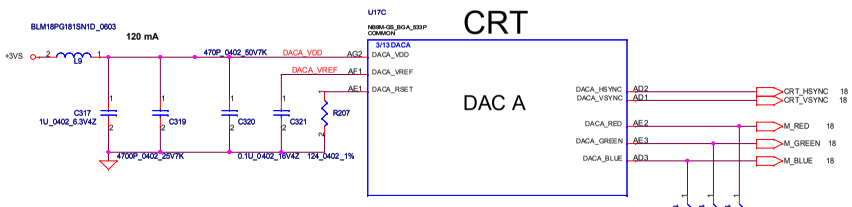


PEG Interface

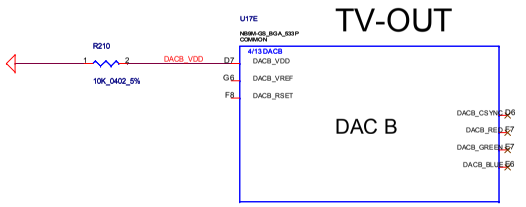




CRT



TV-OUT



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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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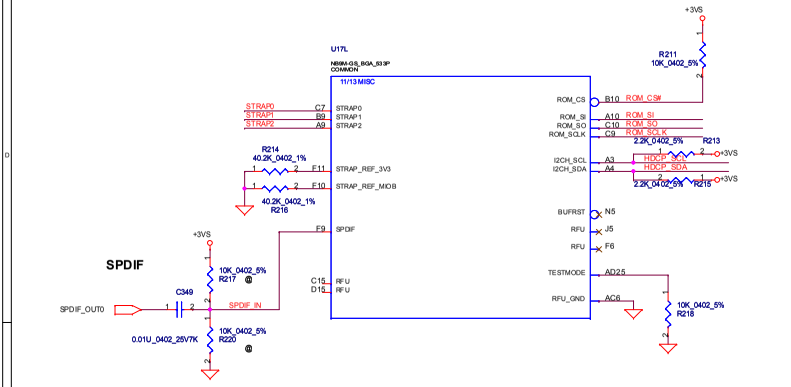
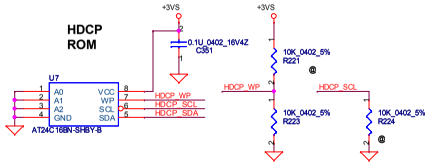
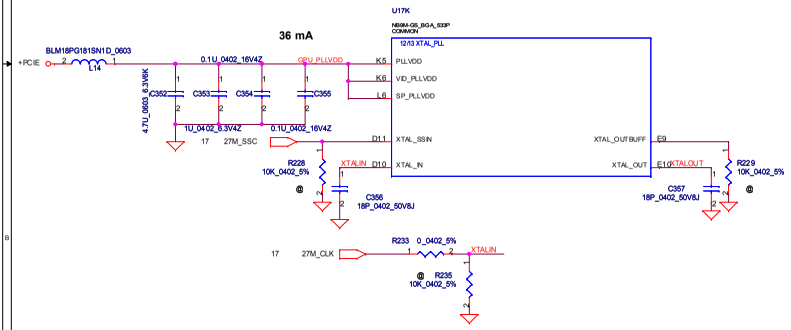
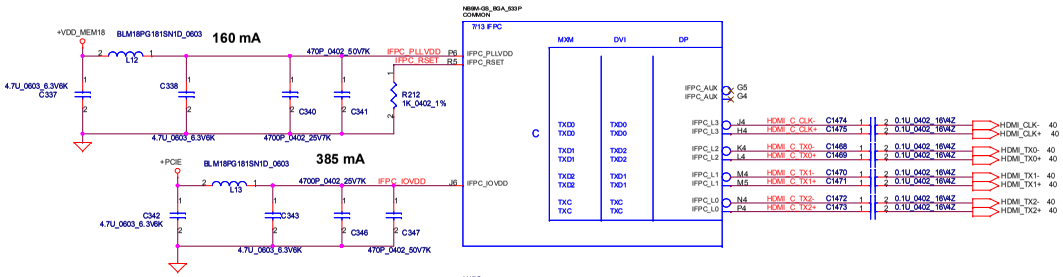
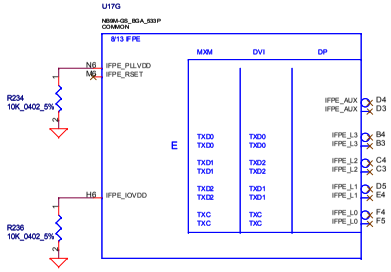
Title	Compal Electronics, Inc.
	PEG & LVDS & DAC
Size / Document Number	LA-4731P Rhett discrete
Rev	0.1
Date: Monday, February 16, 2009	Sheet 20 of 51

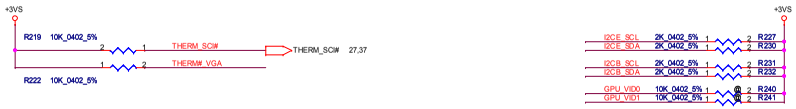


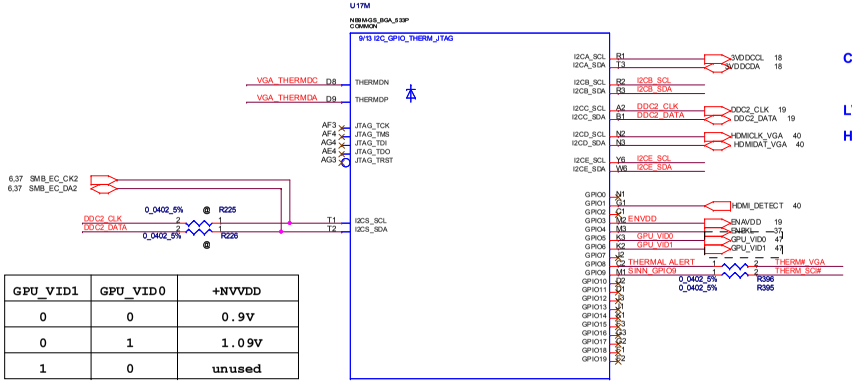




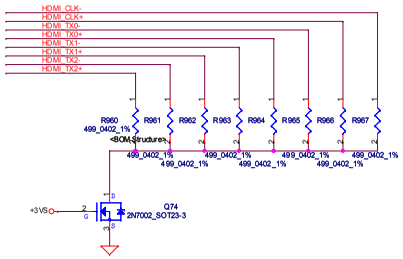








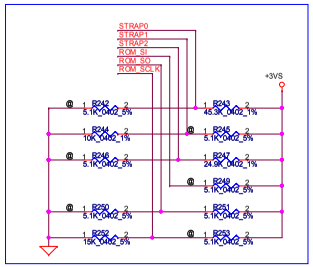
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	unused

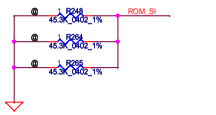
Straps

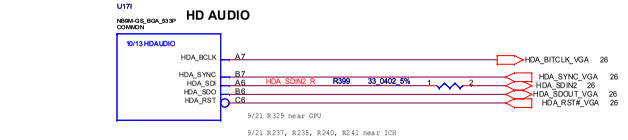
MULTI LEVEL STRAPS



VRAM VENDOR STRAPS

	R248	R264	R265
64MX16 Hynix	5 Kohms		
64MX16 Qimonda		15 Kohms	
64MX16 Samsung			10 Kohms





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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: Straps & HDMI

Size: Custom | Document Number: LA-473 1P Rhet discrete | Rev: 0.1

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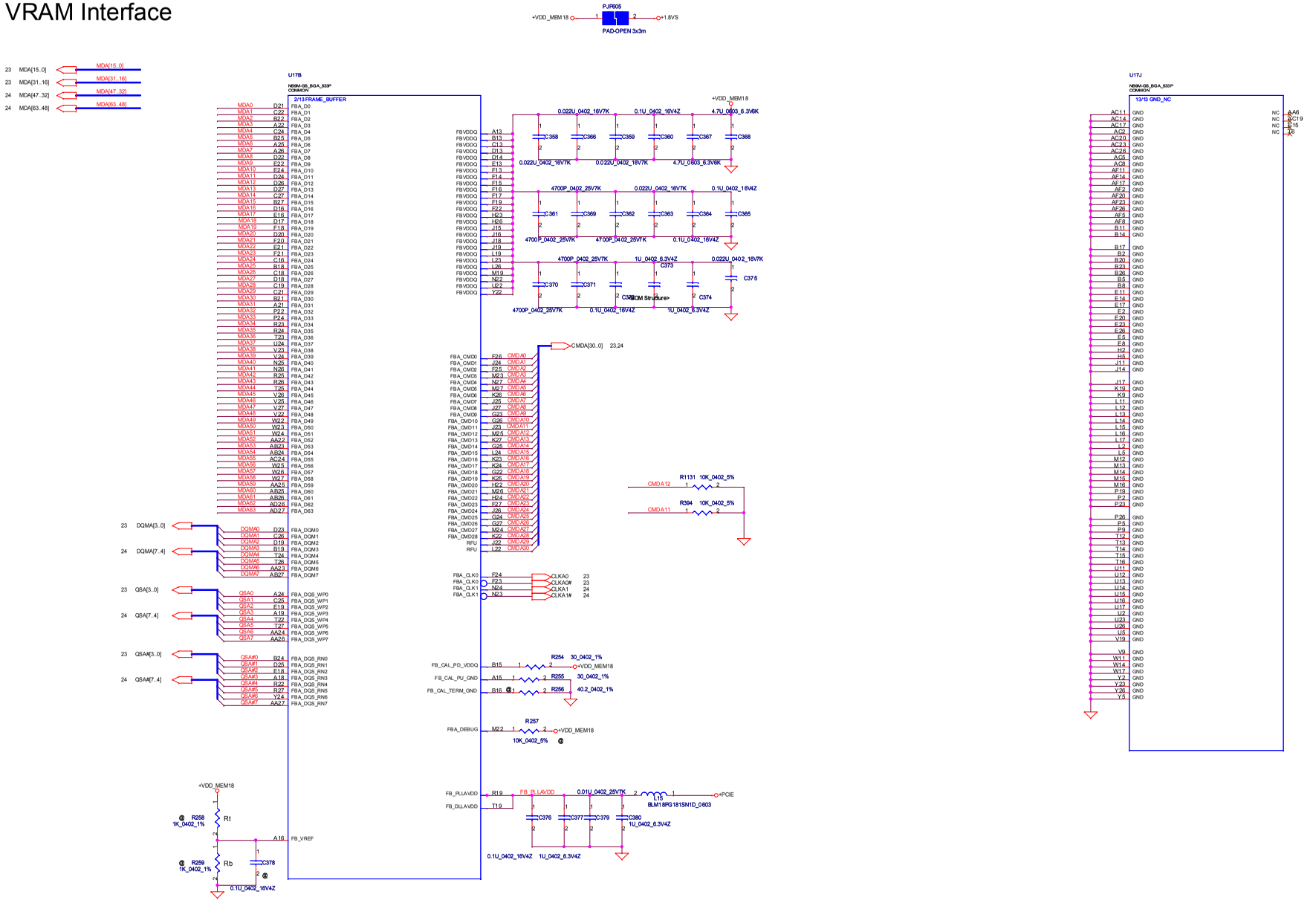
VRAM Interface



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Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: **VRAM / GND**

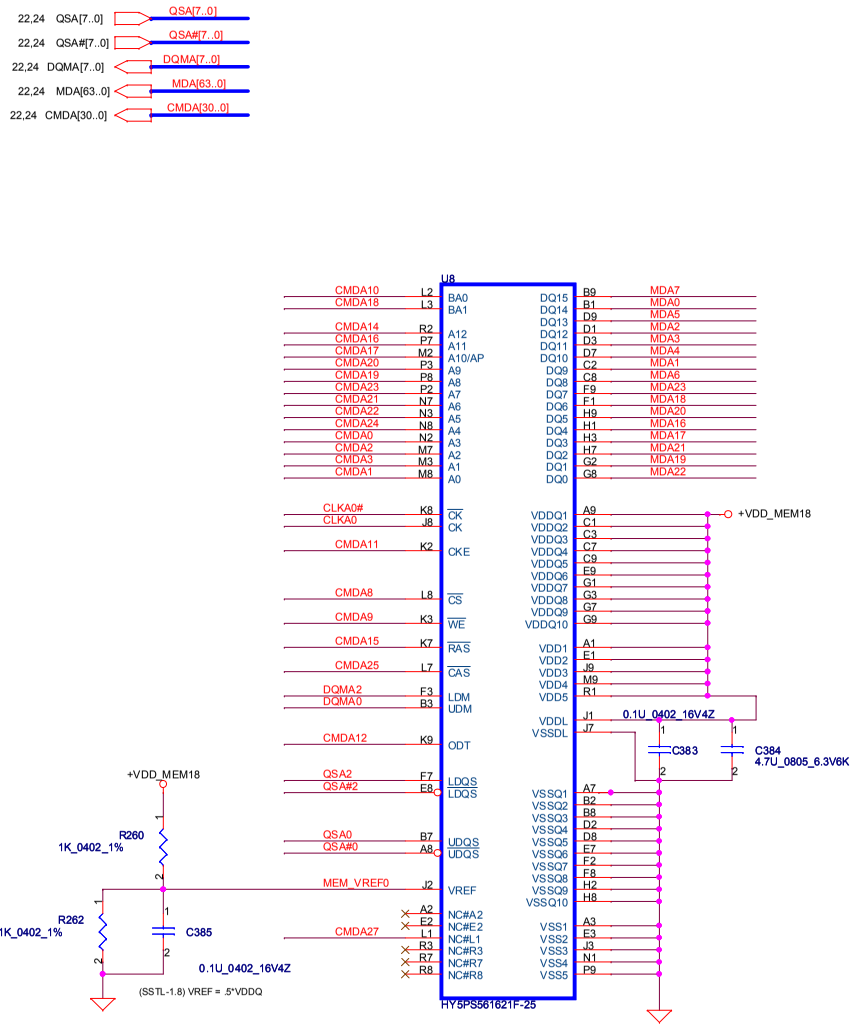
Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

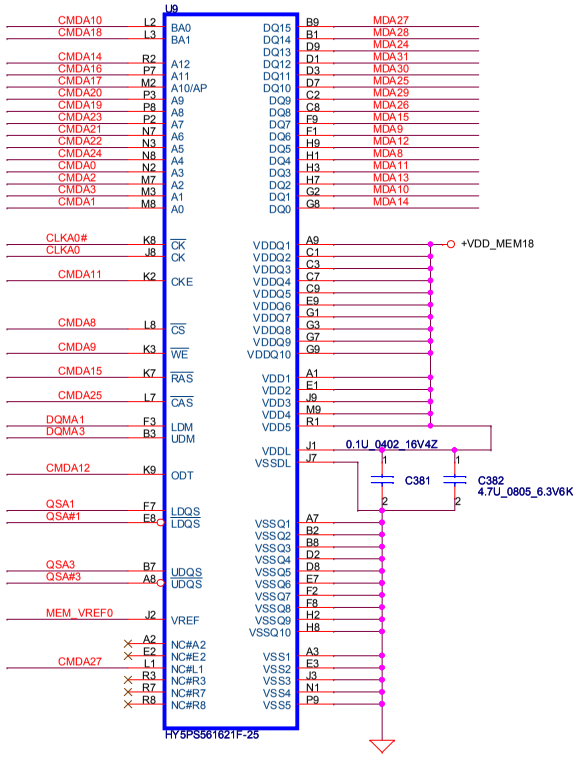
Date: Monday, February 16, 2009 | Sheet 22 of 51

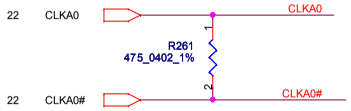
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB
64Mx16 DDR2 400MHz*4==>512MB

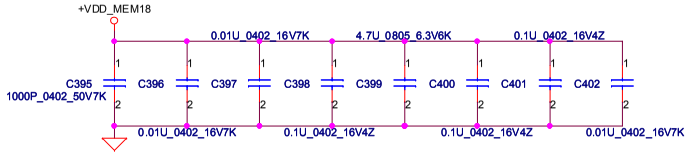
	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



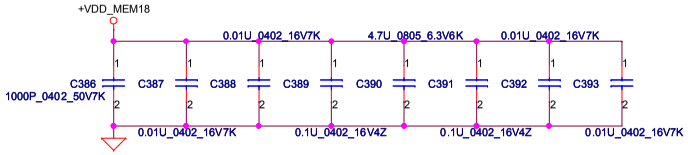




DDR2 BGA MEMORY



DDR BGA MEMORY



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Compal Electronics, Inc.

Title: CHANNEL A EXT. 256M_1

Size: | Document Number: CHANNEL A EXT. 256M_1 | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 7 of 16

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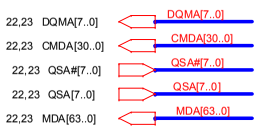
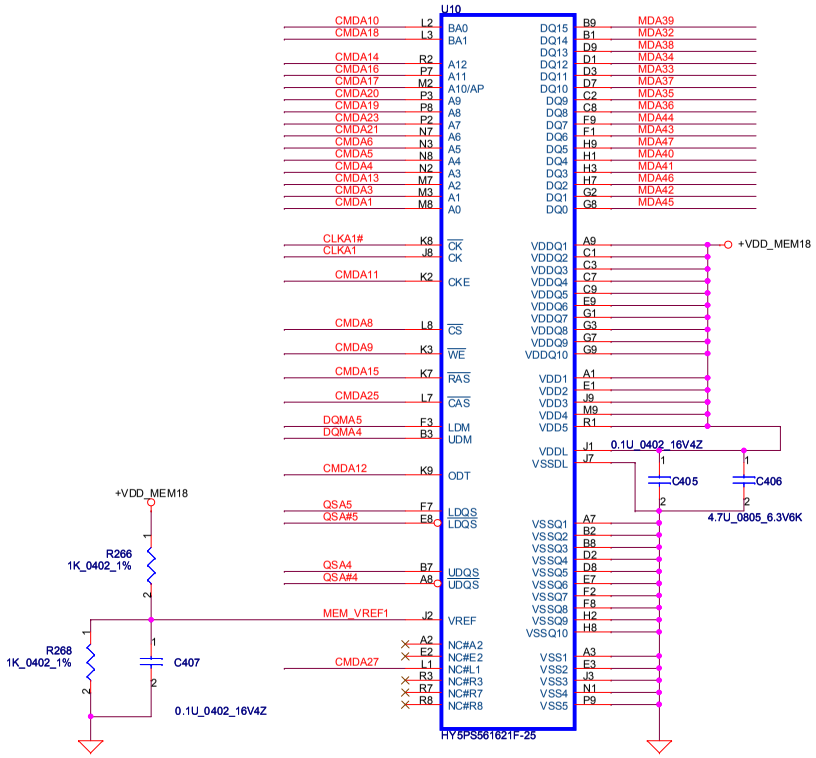
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

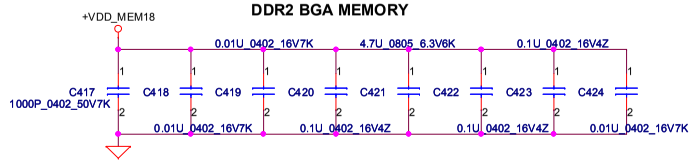
64Mx16 DDR2 400MHz*4==>512MB

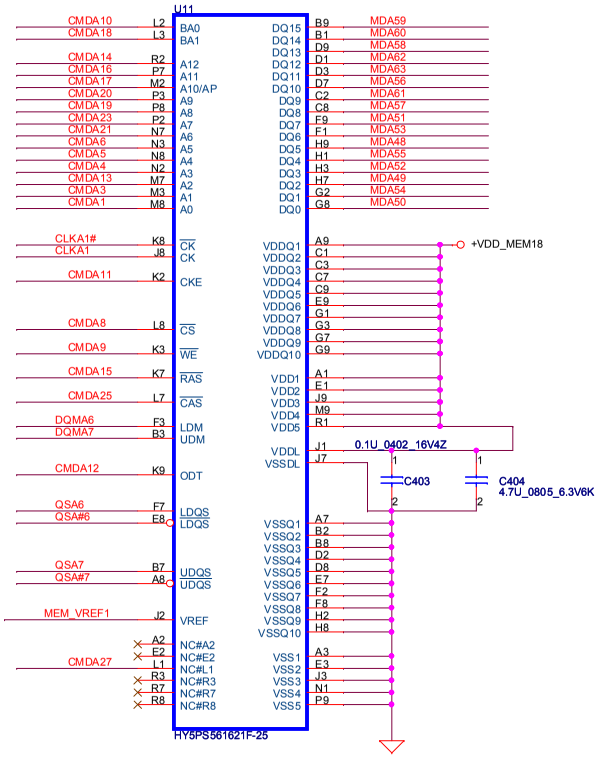


	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

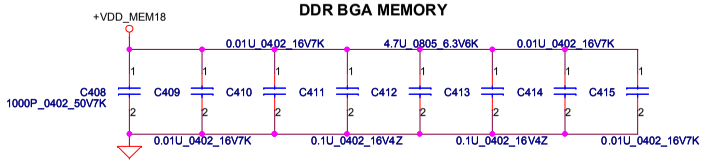


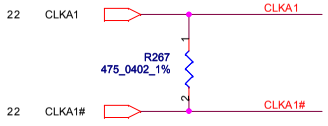
DDR2 BGA MEMORY





DDR BGA MEMORY





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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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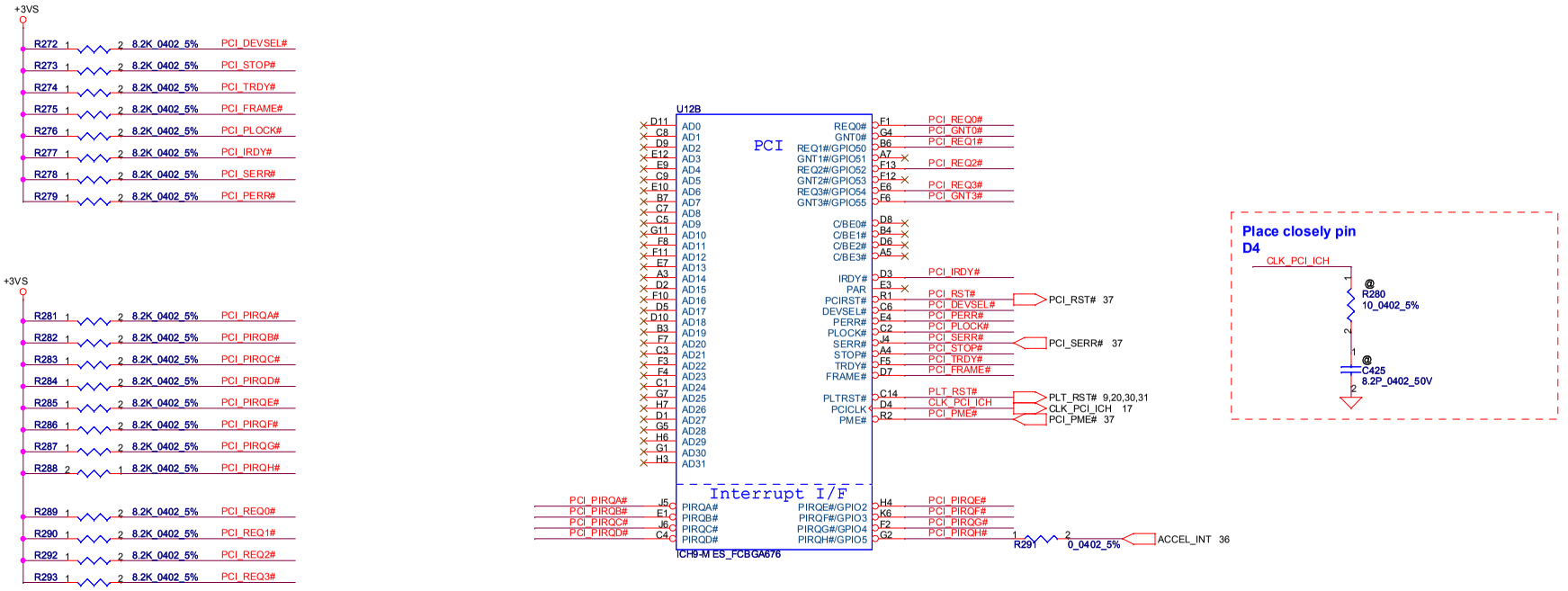
Compal Electronics, Inc.

Title: CHANNEL A EXT. 256M_2

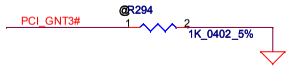
Size | Document Number: CHANNEL A EXT. 256M_2 | Rev 0.1

Date: Monday, February 16, 2009 | Sheet 8 of 16



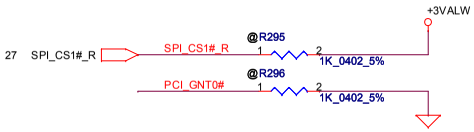
A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default *



Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

Size: | Document Number: LA-4731P Rhett discrete | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 25 of 51

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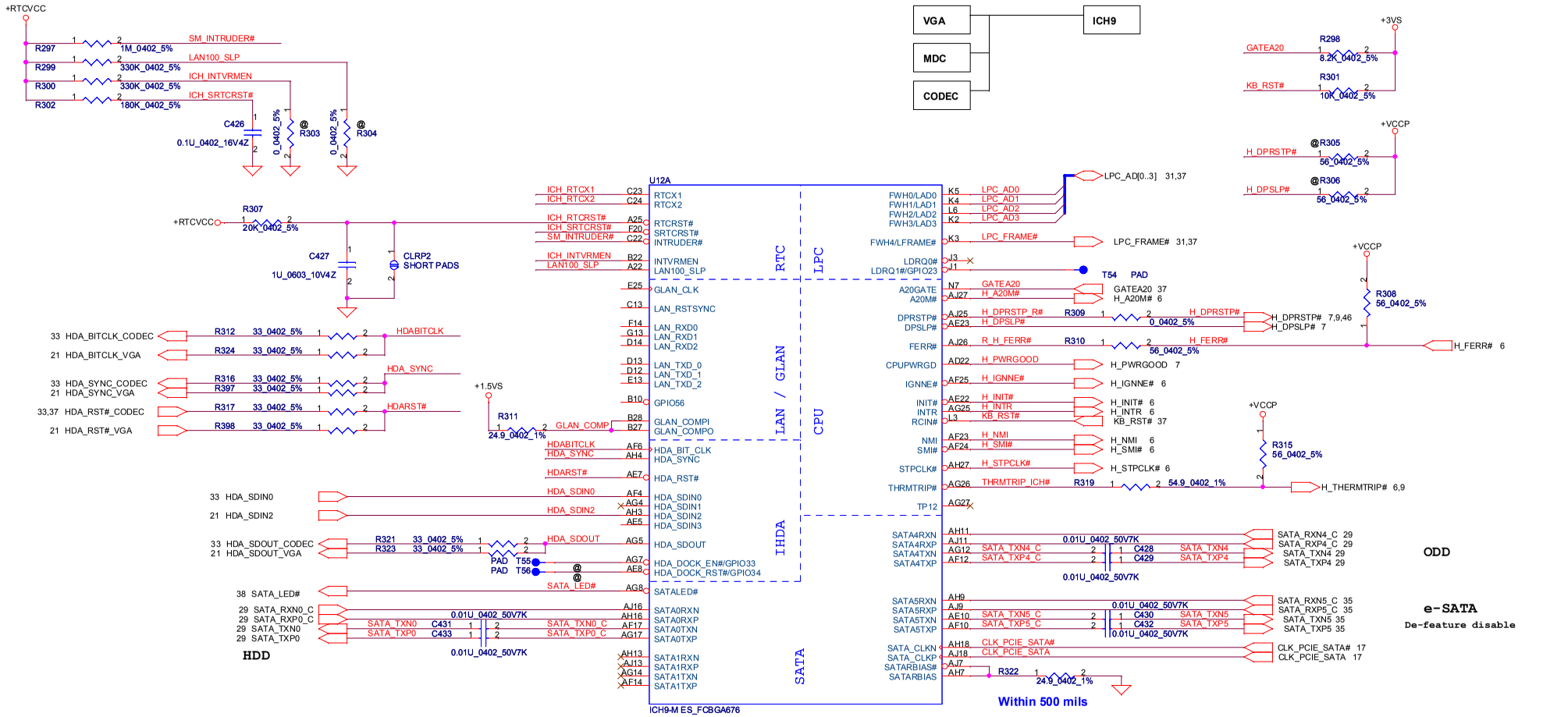

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 26 of 51

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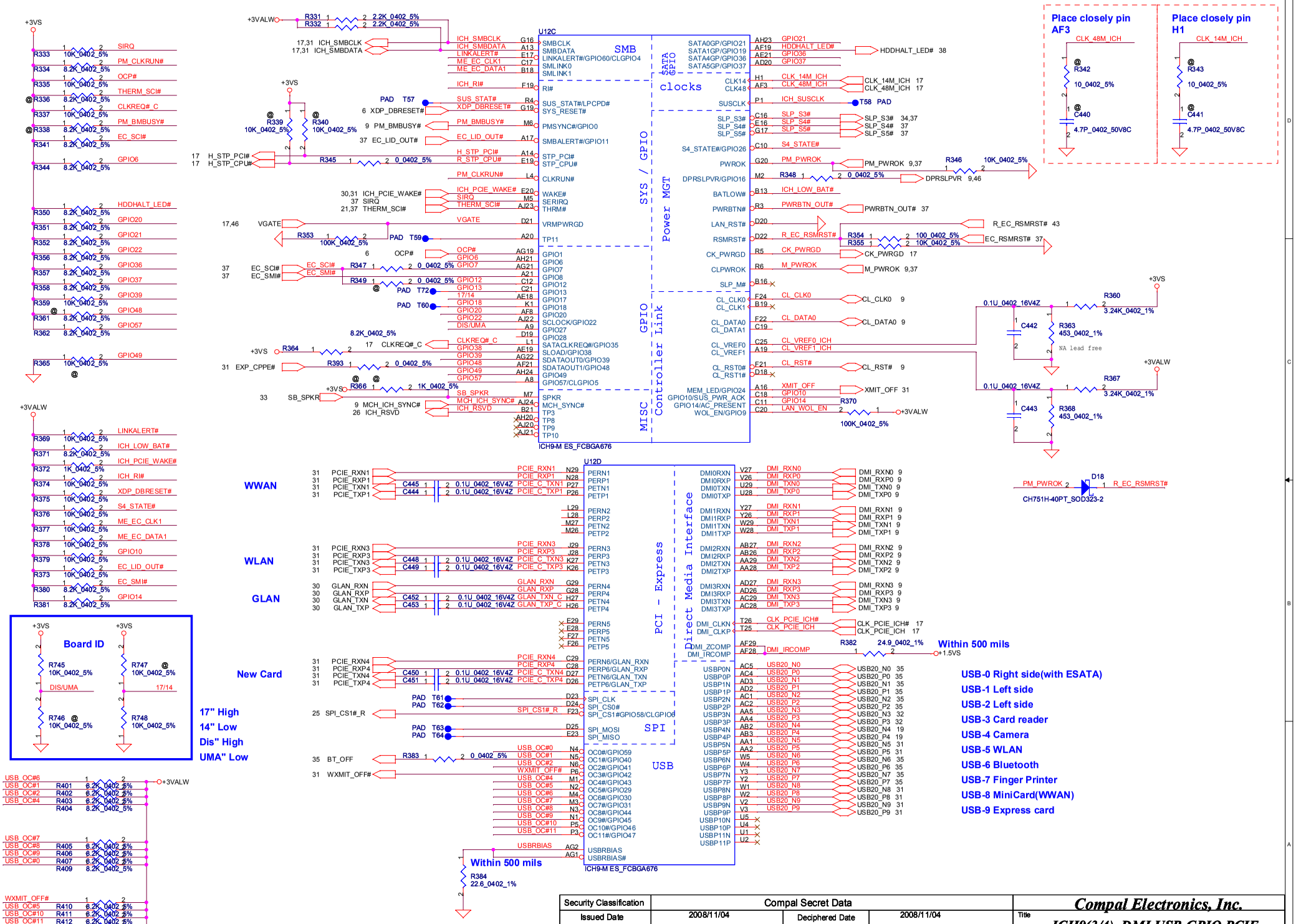

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Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 27 of 51

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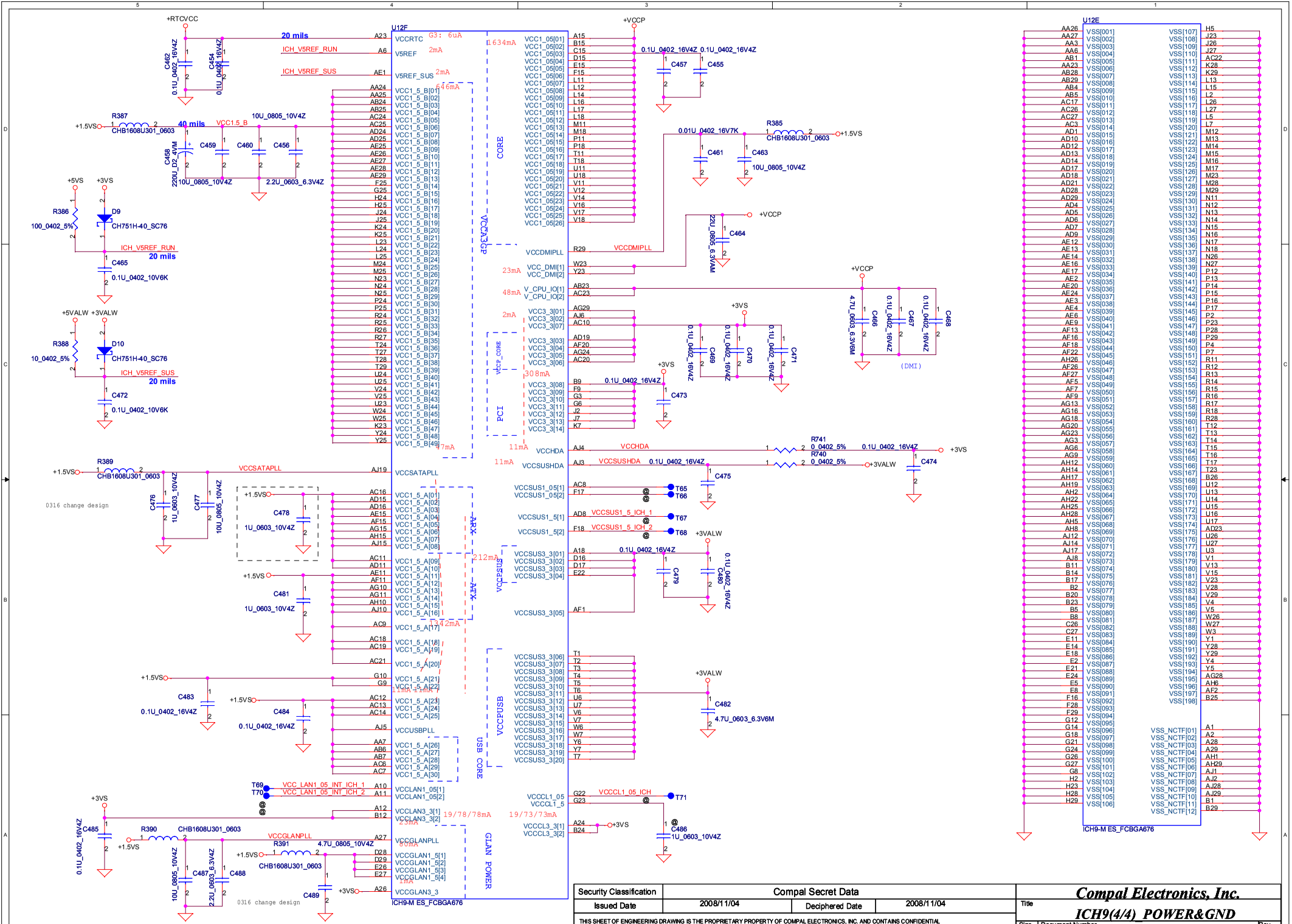

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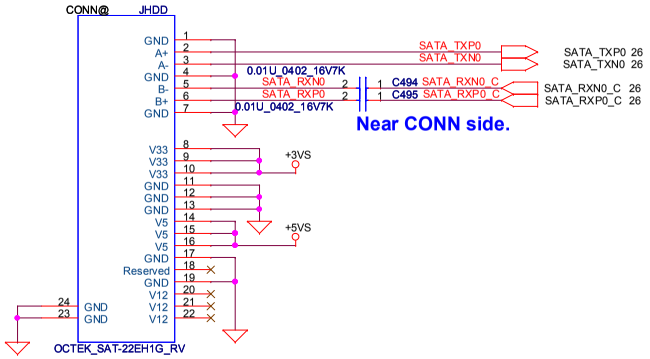
Compal Electronics, Inc.

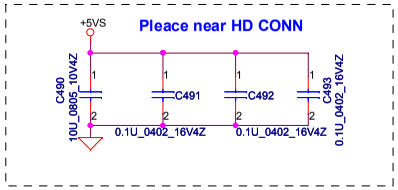
Title: ICH9(4/4)_POWER&GND

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

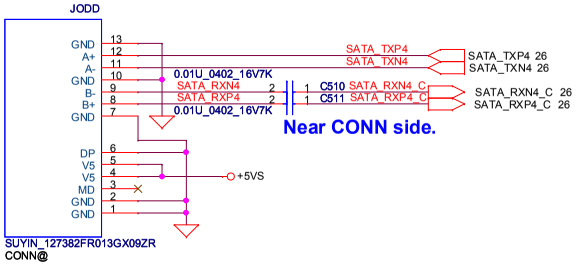
Date: Thursday, February 12, 2009 | Sheet 28 of 51

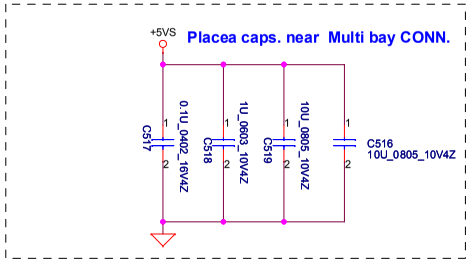
HDD Connector





CD-ROM Connector





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Compal Electronics, Inc.

Title: **HDD & CDROM**

Size: Custom | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 29 of 51

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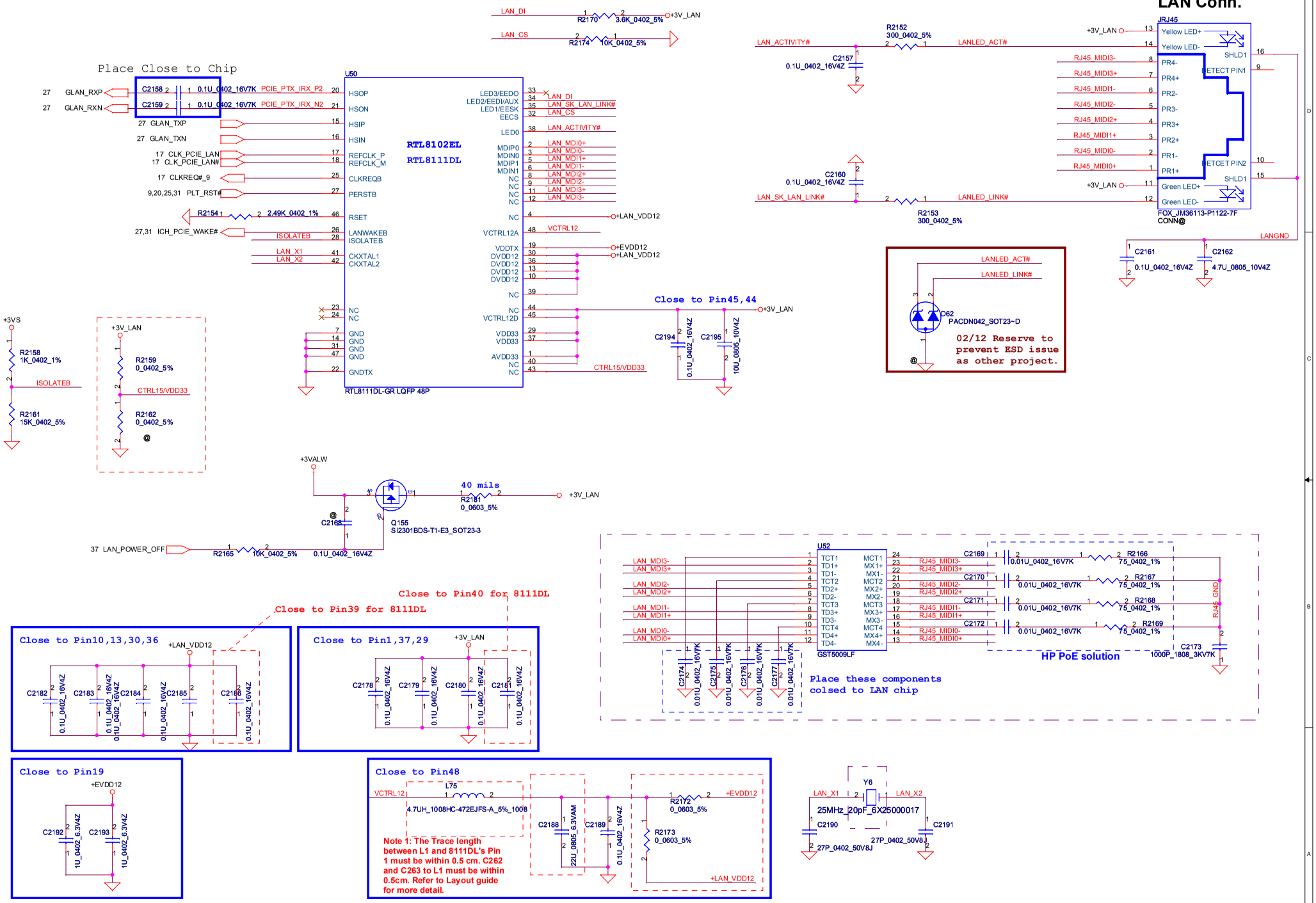
LAN Conn.



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Compal Electronics, Inc.

Title: Realtek 8111DL Giga_LAN

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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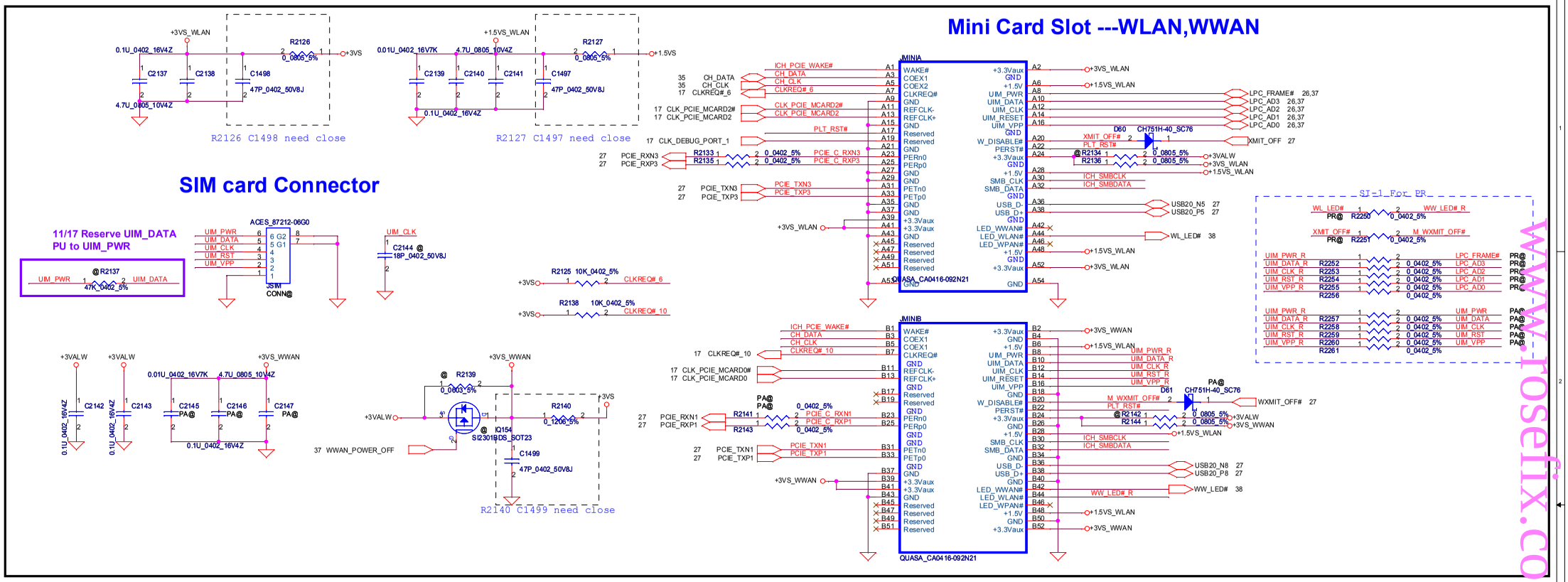
Mini Card Slot ---WLAN,WWAN

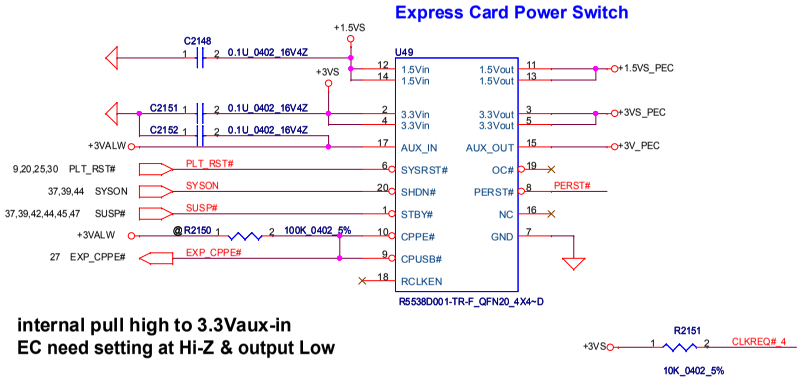


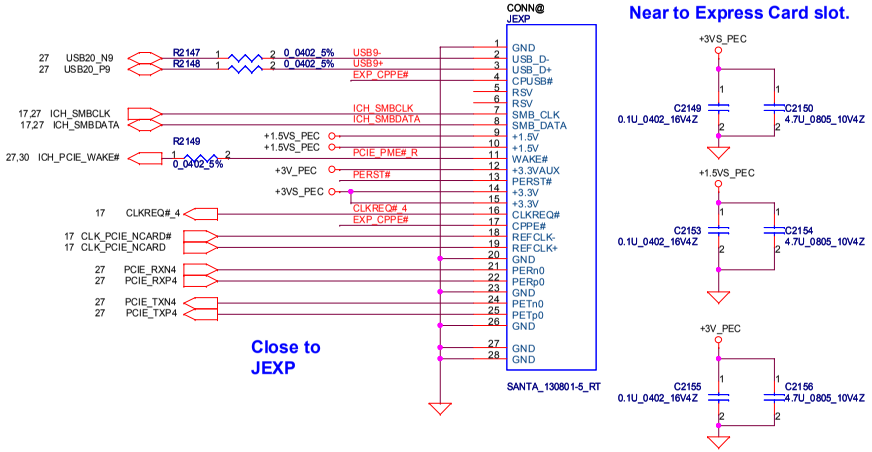
SIM card Connector

11/17 Reserve UIM_DATA
PU to UIM_PWR

New Card

Express Card Power Switch





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Compal Electronics, Inc.

Title: **WLAN, WWAN, New Card**

Size	Document Number	Rev
	LA-4731P Rhett discrete	0.1

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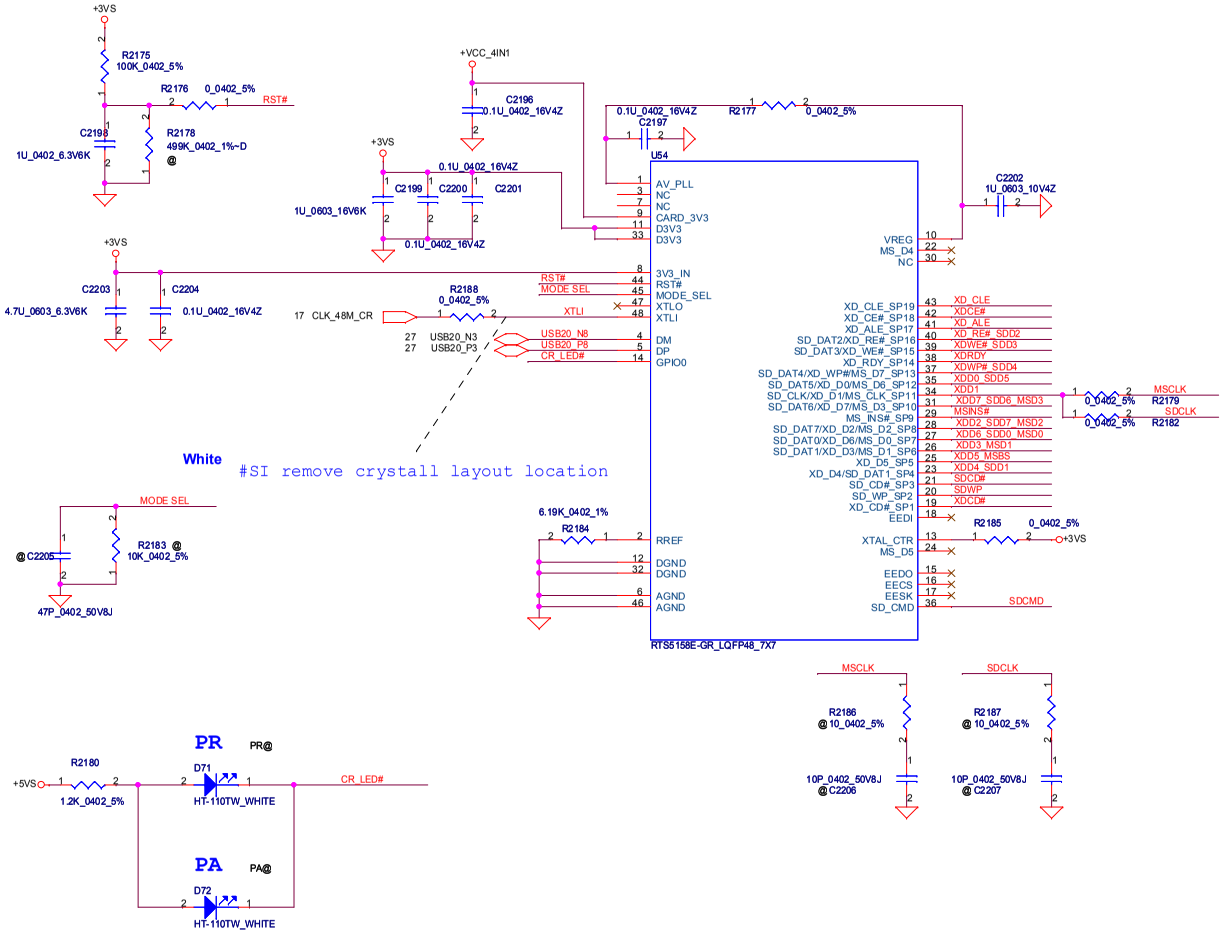

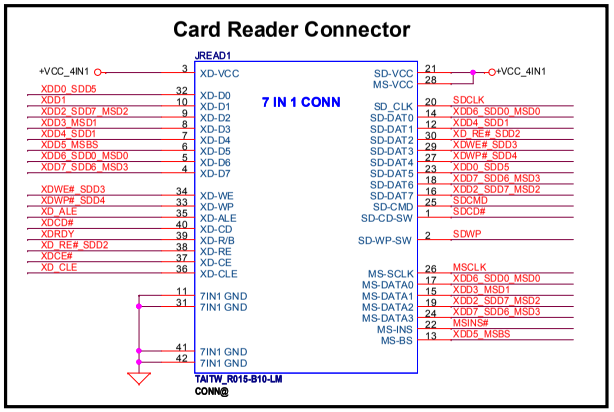

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Compal Electronics, Inc.

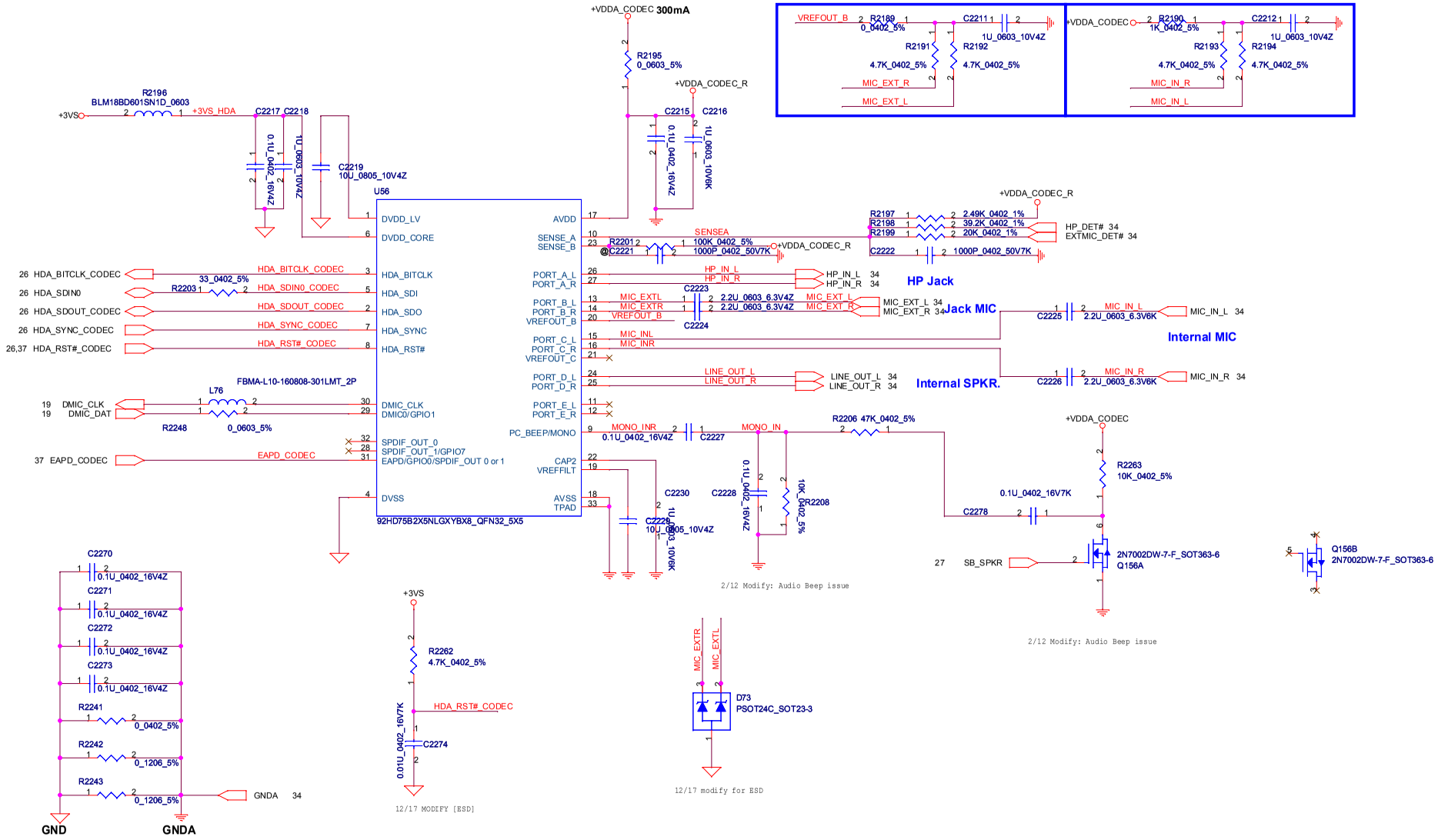
Title: **USB CardReader&CONN**

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 32 of 51

CODEC POWER

(4.75V(4.56~4.94V))



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Title: Codec_IDT9275B

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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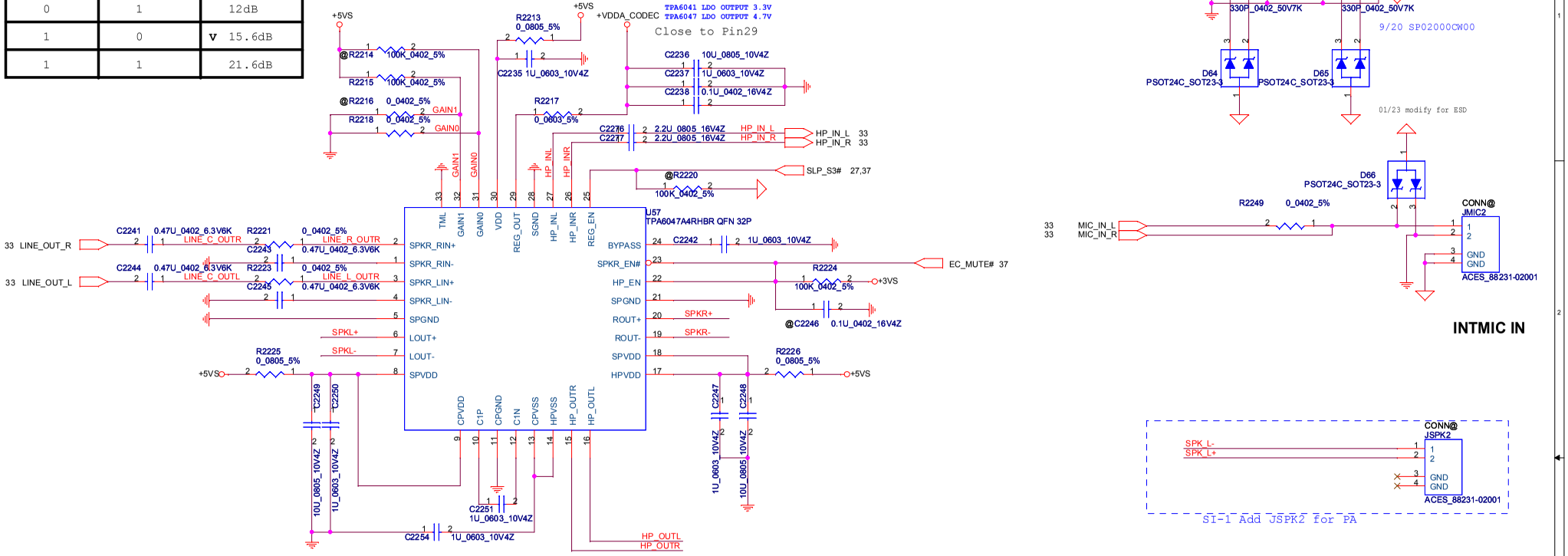
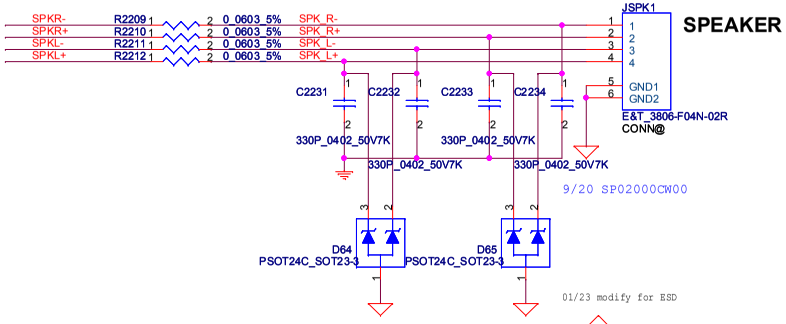
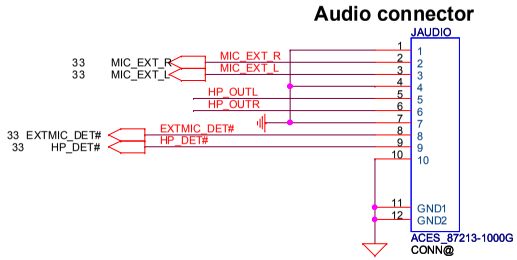
AMP. FOR INTERNAL SPEAKER

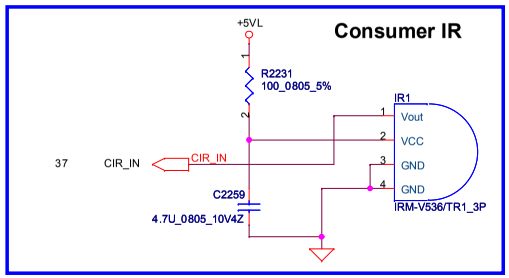
GAIN1	GAIN0	Av(inv)
0	0	10dB
0	1	12dB
1	0	V 15.6dB
1	1	21.6dB





SI-1 Add Audio board connector





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Title: AMP & Audio Jack

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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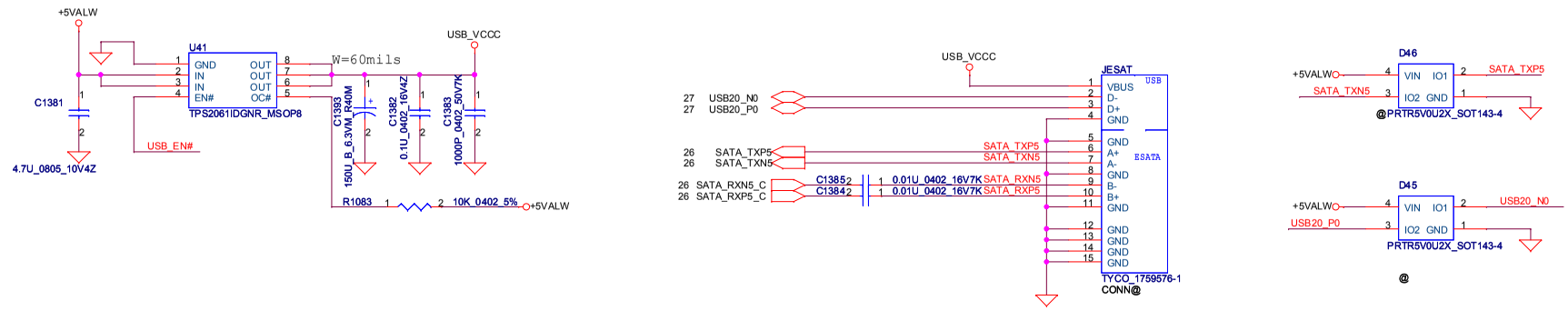
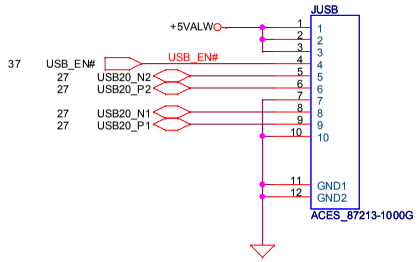
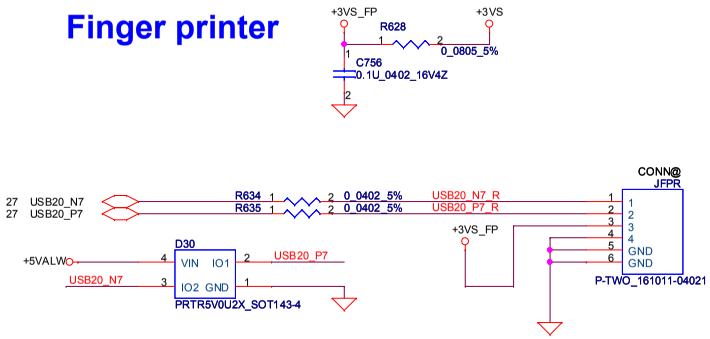
Right side ESATA/USB combination Connector



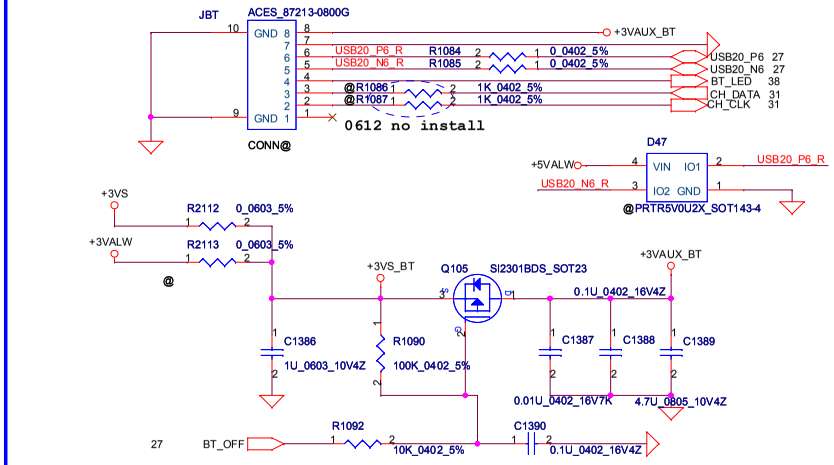
USB cable connector for Right side



Finger printer



BT Connector



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Compal Electronics, Inc.

Title: **USB, BT, eSATA**

Size | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

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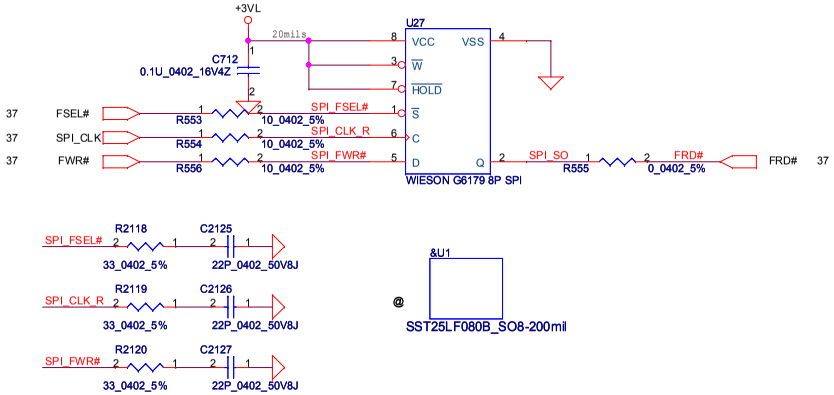
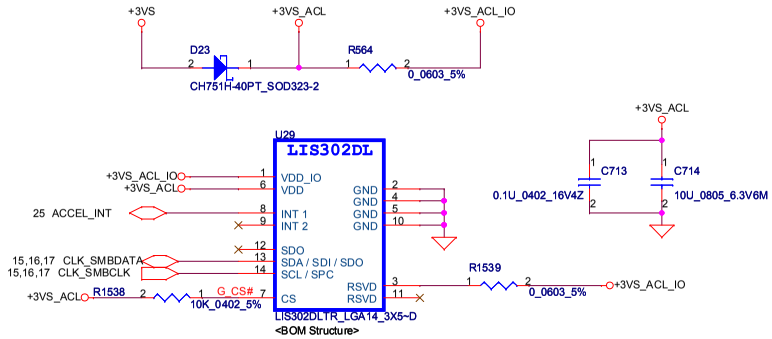
SPI ROM



Acceleromter-1



Must be placed in the center of the system.

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Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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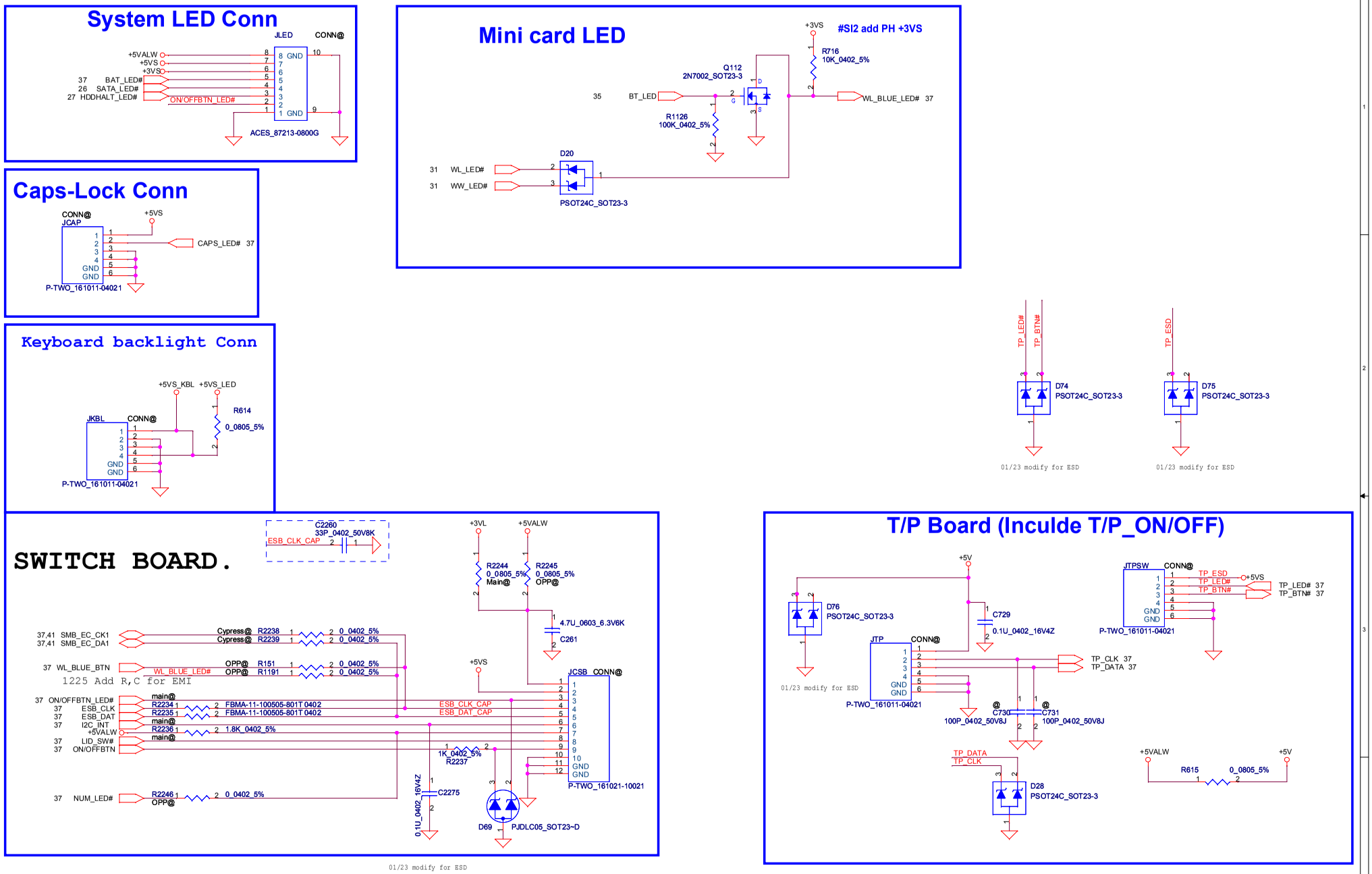

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Compal Electronics, Inc.

Title: LED, TP,KBL,Cab sensor boar

Size | Document Number: LA-4731P Rhett discrete | Rev 0.1

Date: Monday, February 16, 2009 | Sheet 38 of 51

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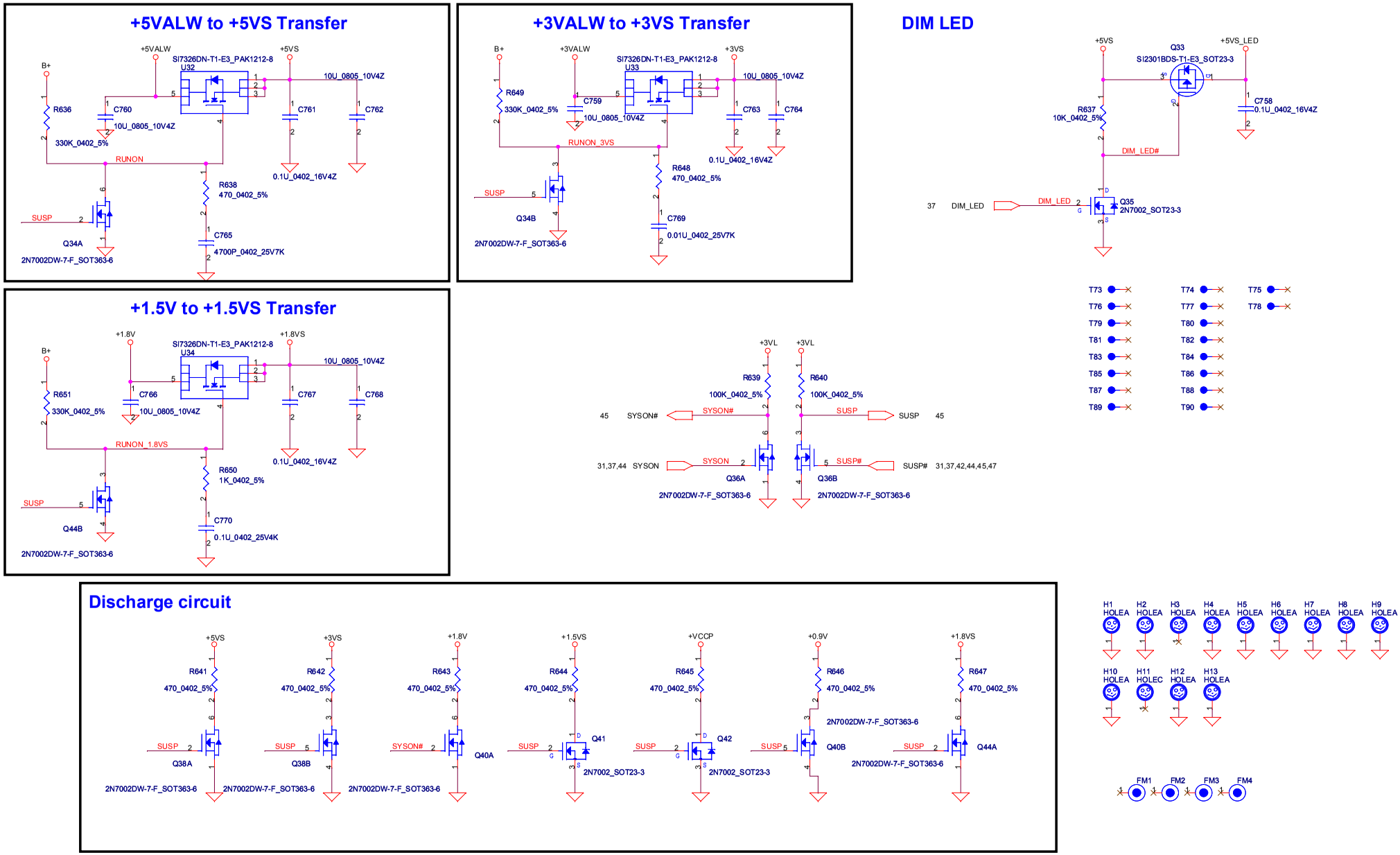

Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: **DC/DC Interface**

Size | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 39 of 51

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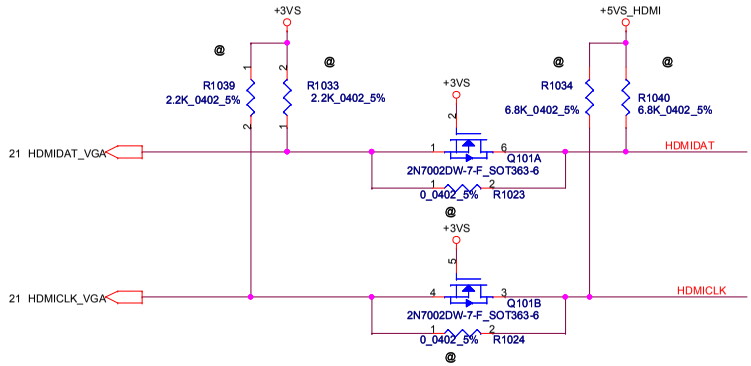
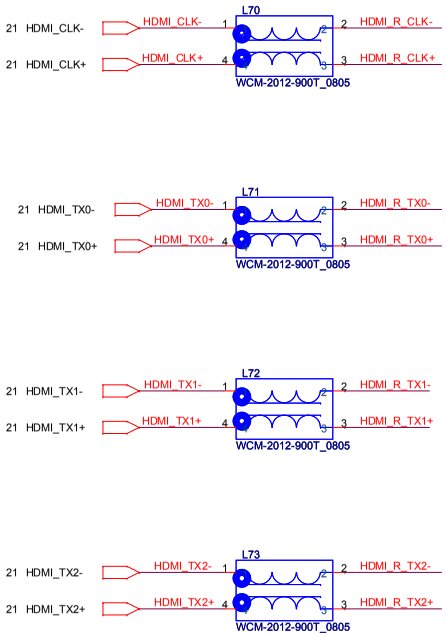
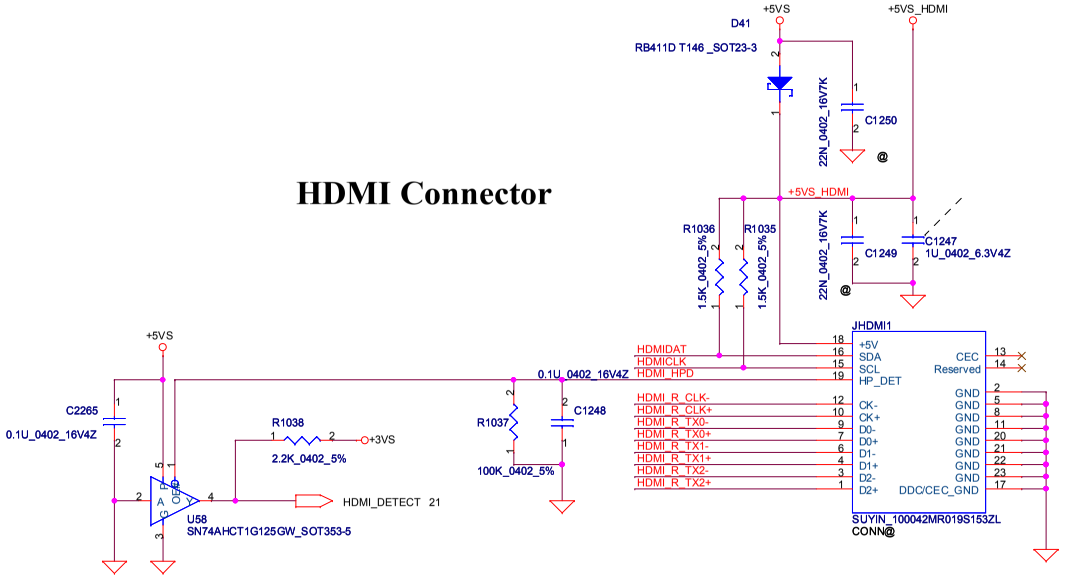




HDMI Connector



for HDMI certification

Security Classification	Compal Secret Data		
Issued Date	2008/11/04	Deciphered Date	2008/11/04

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Compal Electronics, Inc.

Title: HDMI LS & Conn.

Size: Custom | Document Number: LA-4731P Rhett discrete | Rev: 0.1

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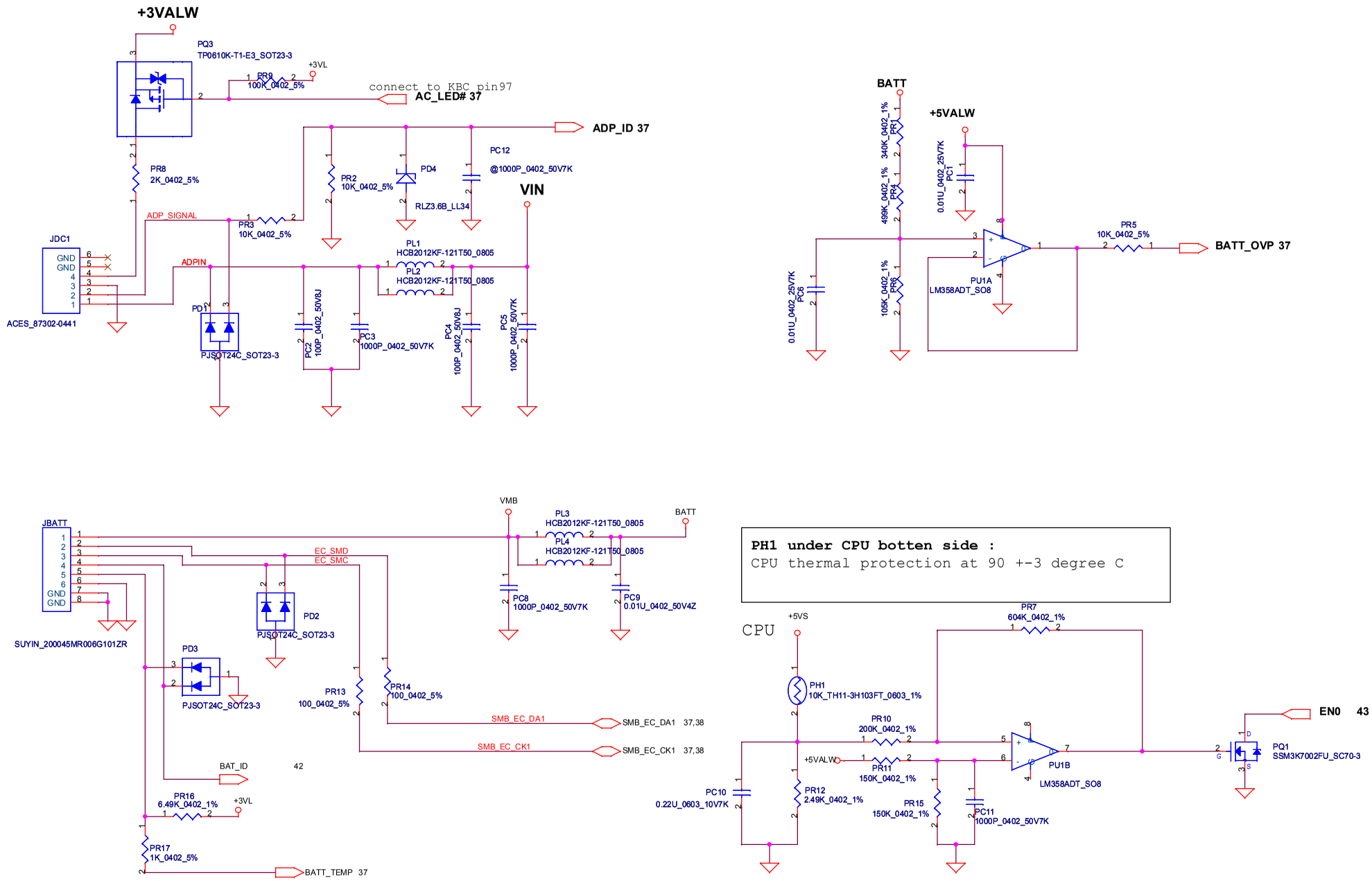

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size | Document Number: *Montevina Consumer Discrete* | Rev 0.1

Date: Monday, February 16, 2009 | Sheet 41 of 51

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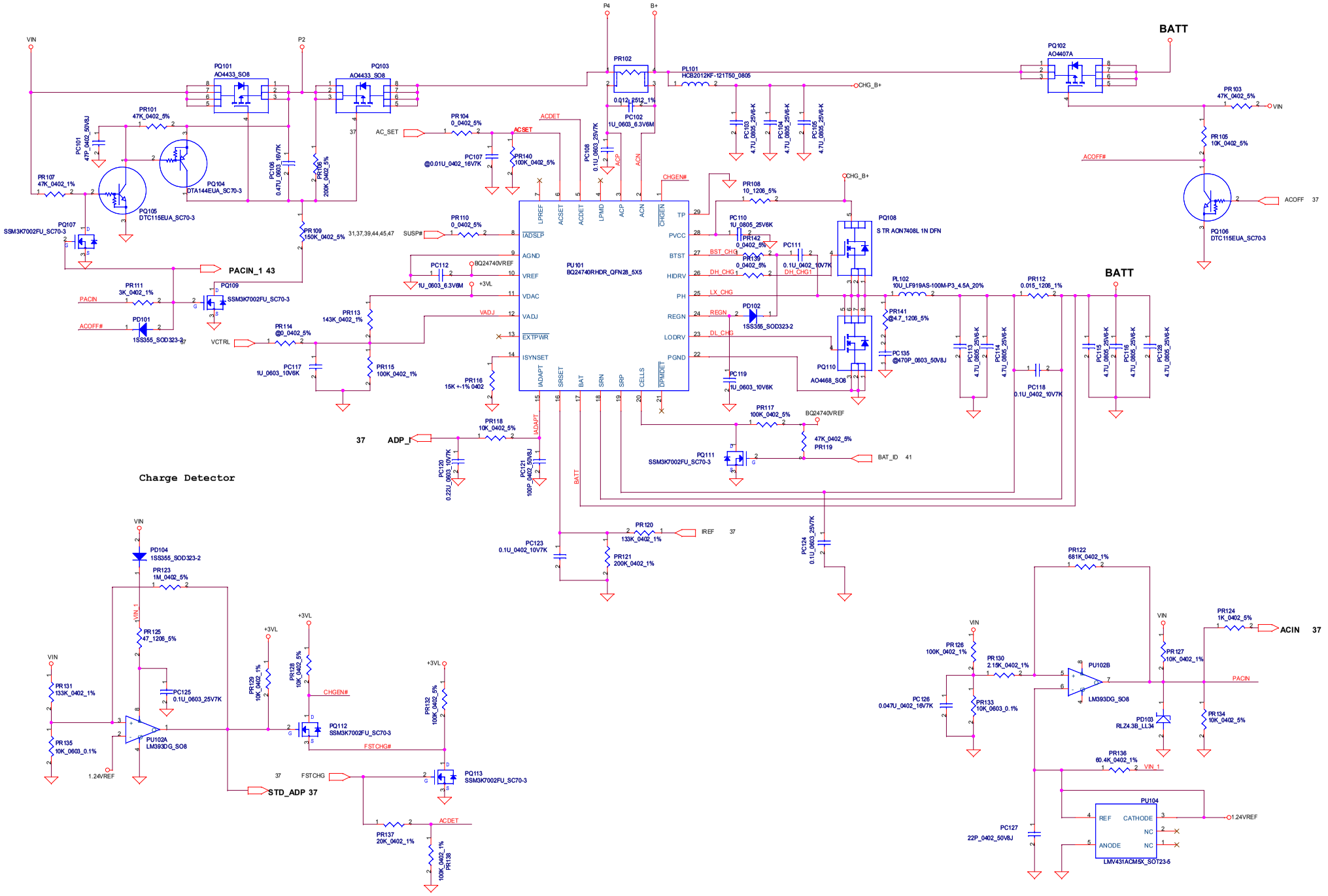

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Issued Date	2007/05/29	Deciphered Date	2008/05/29

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Compal Electronics, Inc.

Title: **Charger**

Size: | Document Number: *LA-4481P* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 42 of 51

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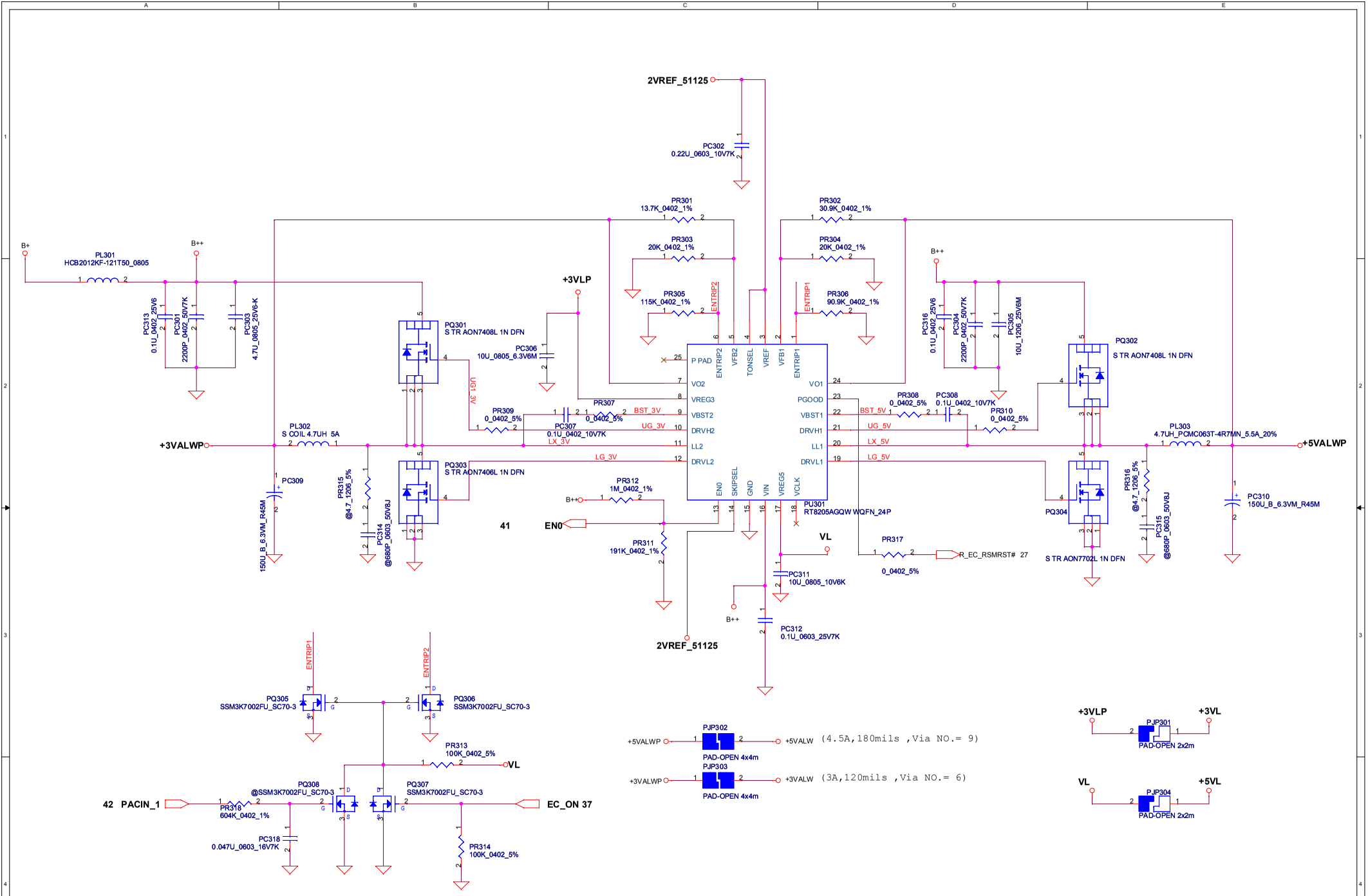

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size: Custom | Document Number: LA-4481P | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 43 of 51

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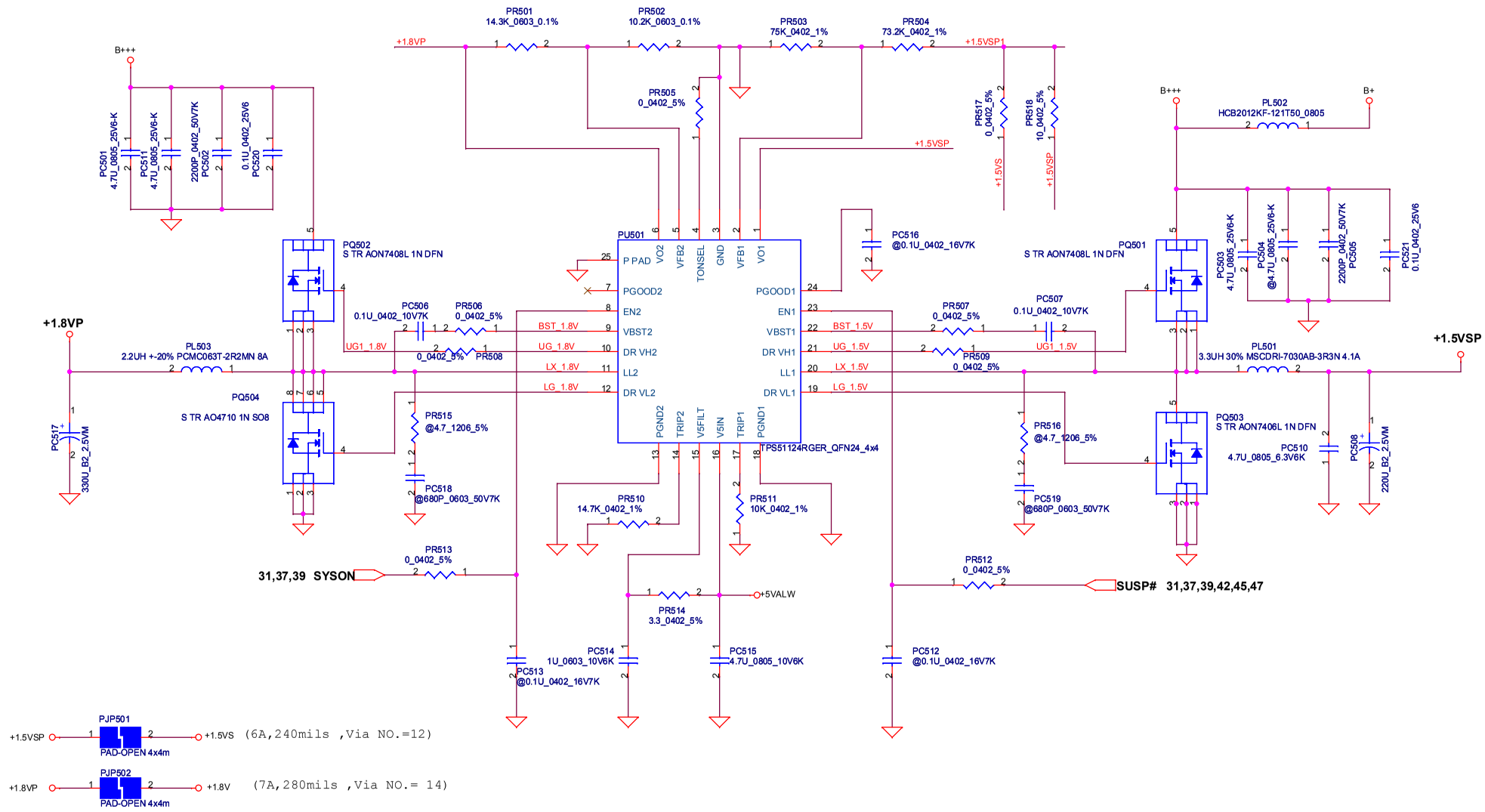

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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Compal Electronics, Inc.

Title: **1.5VSP/1.8VP**

Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.1

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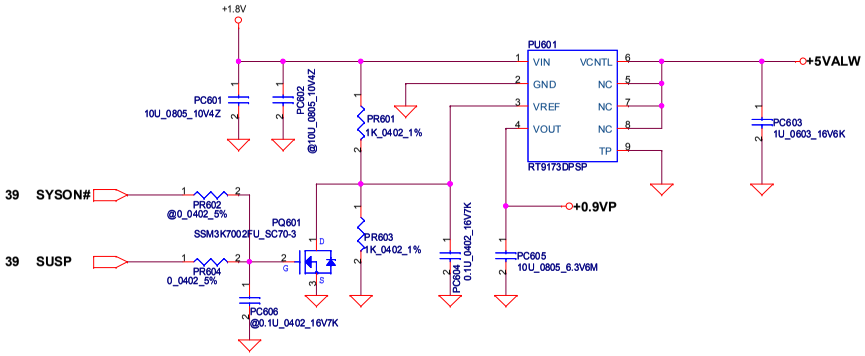

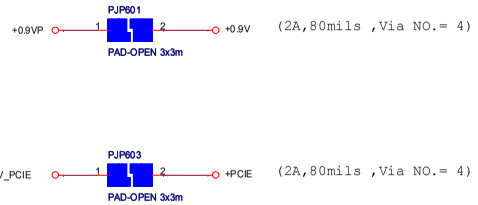

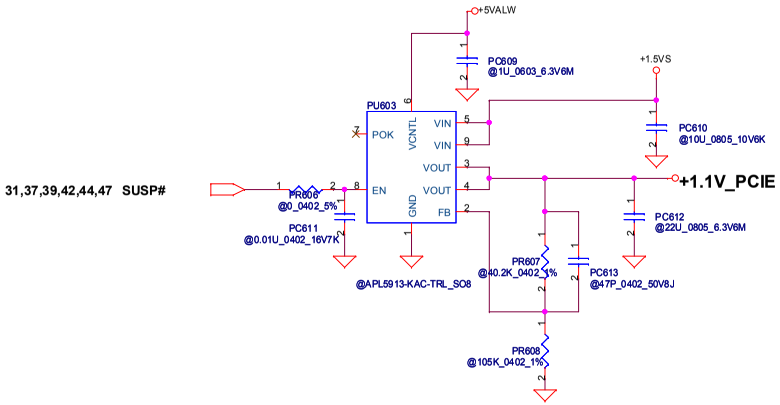

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Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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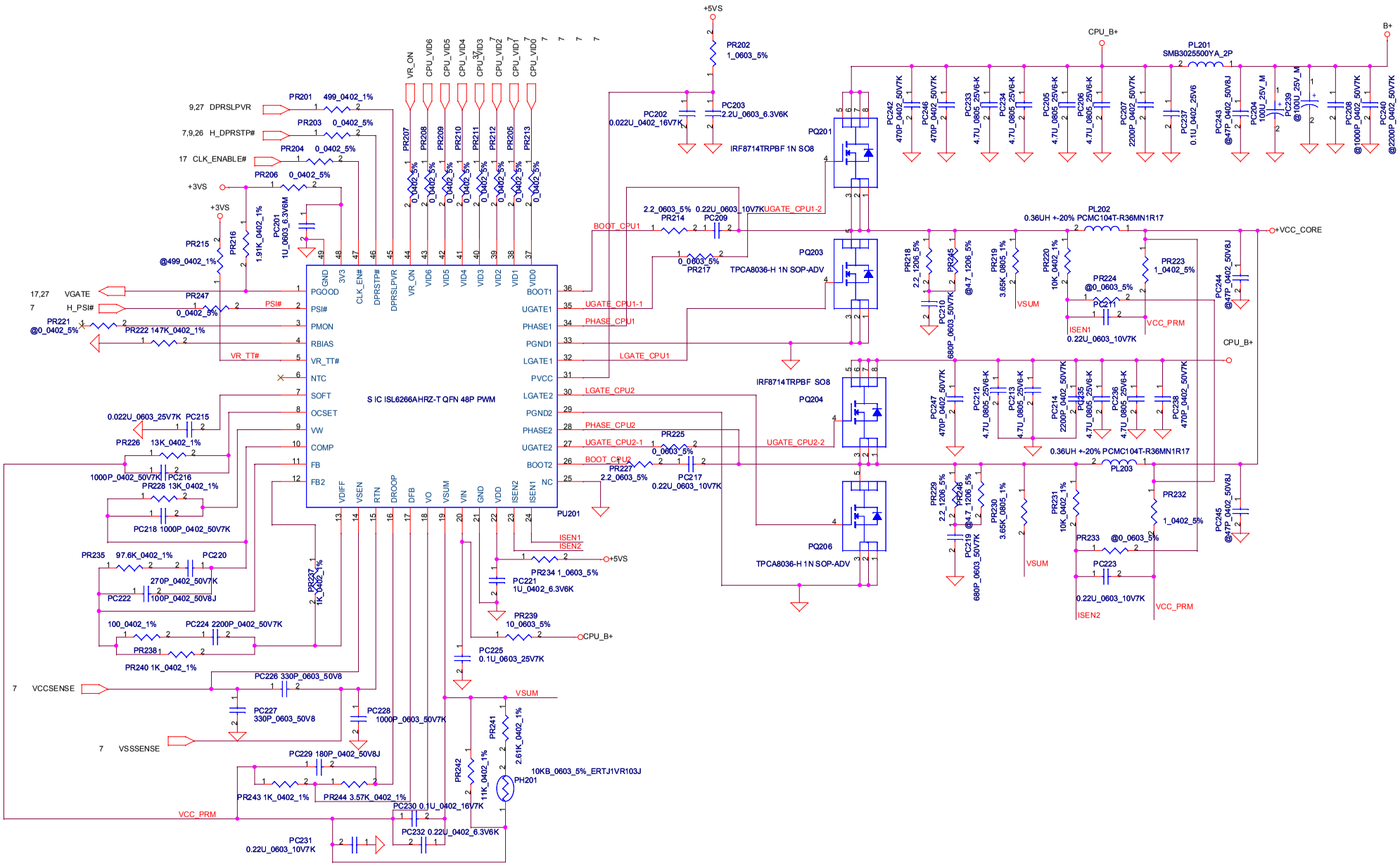
Compal Electronics, Inc.

Title: *0.9VP/1.1V PCIE*

Size | Document Number: *LA-4102P Blade discrete* | Rev: 0.1

Date: Monday, February 16, 2009 | Sheet 45 of 51



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Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom		0.1

Date: Monday, February 16, 2009 | Sheet 46 of 51

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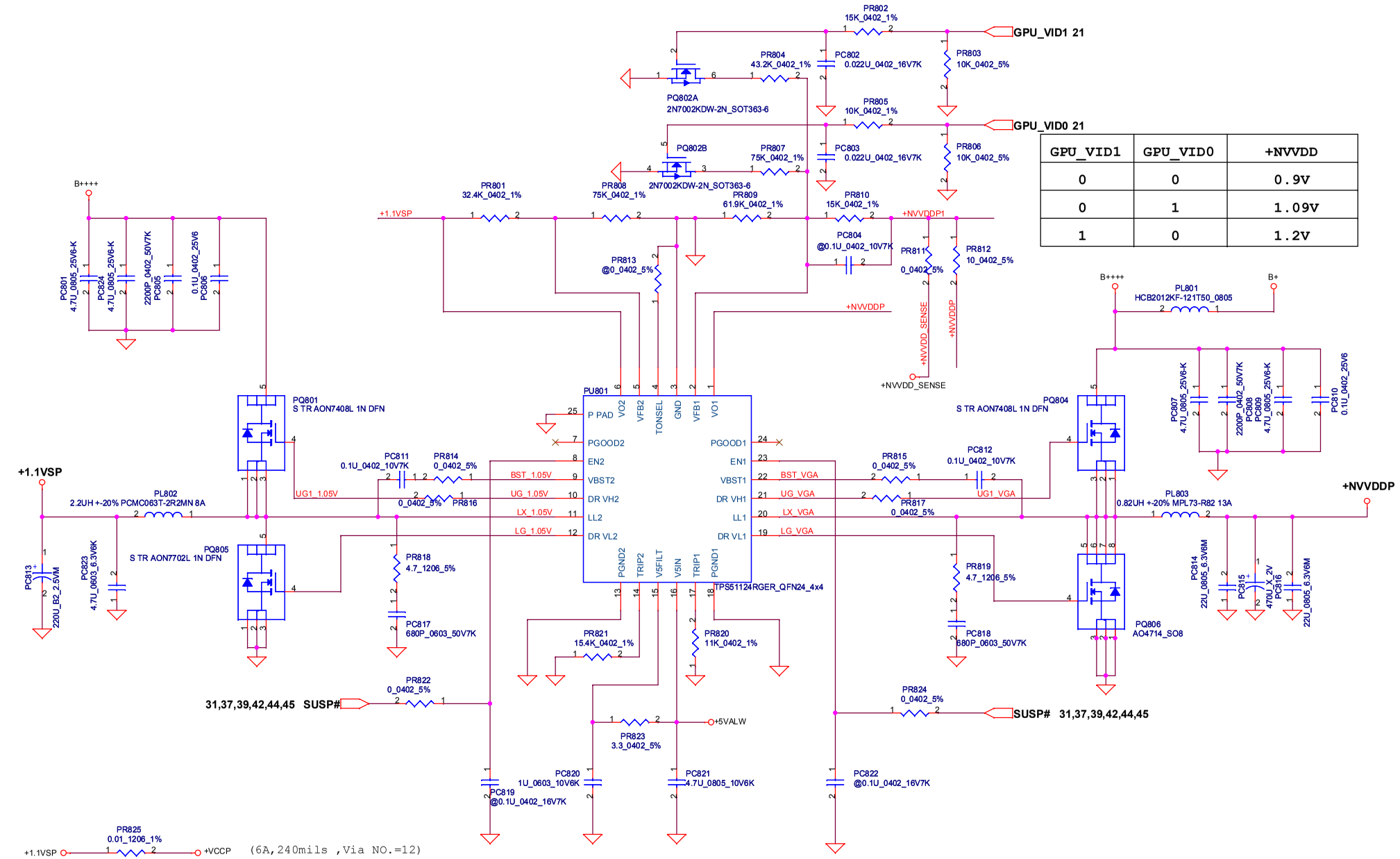

GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	1.2V

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Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

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Compal Electronics, Inc.

Title: **+1.05V_VCCP/VGA_CORE**

Size: | Document Number: LA-4112P | Rev: 0.1

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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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Compal Electronics, Inc.

Title: **Power Changed-List History-1**

Size: Custom | Document Number: LA-4111P | Rev: 0.1

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	31	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	delete VGA external thermal sensor layout location for layout space limitation	29	Del U6,C348,C350	2008/10/08	SI-1
4	Add Audio board	34	Add JAUDIO connecter for audio board	2008/10/08	SI-1
5	delete VGA JTAG for layou space limitation	29	Delete T47,T48,T49,T50,T51	2008/10/08	SI-1
6	Cap board issue	38	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Change JFPR to 6 pin connector	35	change JFPR	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D17,R50,C41	2008/10/08	SI-1
9	Delete HDA SSC	26	Remove U44 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	31	Add R2252 -- R2261	2008/10/08	SI-1
11	PA/PR CardReader LED	32	D72 for PA, D71 for PR	2008/10/08	SI-1
12	EMI request	33	Change R2205 to L76	2008/10/08	SI-1
13	change MIC to 2pin and add SPK connector	34		2008/10/08	SI-1
14	Speaker L & R reverse	34		2008/11/20	SI-2
15	JFPR change to 4 pin	40	Add U58,C2265	2008/11/20	SI-2
16	add buffer on detect pin for certification item 7-12	34		2008/11/20	SI-2
17	*Bom Error [Bug: BT led fail]*	*38*	*Change D20's Part number to SCA00000G00*	2008/12/10	PV
18	*Realtek suggest us to change Cap value*	*30*	*Change C2193 value from 0.1uF to 1uF*	2008/12/10	PV
19	*Slove WWLAN Noise : Add Cap X4 [to GND]*	*26*	*C499 and C2130 default mount, Add C2266 and C2267 [12 PF]*	2008/12/10	PV
20	*Slove WWLAN Noise:Add Cap,change R191val*	*37*	*Add C2268 [22PF] on R191.2 to GND and R191 change to 47 ohm*	2008/12/10	PV
21	*Slove WWLAN Noise:C356,C357 default mou*	*21*	*C356 and C357 default mount*	2008/12/10	PV
22	*Slove SMT issue*	*37*	*Change U30 FOOTPRINT [fromKB926QFA1_LQFP128_14X14 change to ECE5028-NU_VTQFP128_14X14]*		PV
23	*Slove SMT issue*	*37*	*Change JKB FOOTPRINT [from ACES_85202-24051_24P change to ACES_85202-24051_24P-S]*	2008/12/10	PV
24	*Slove ESD issue*	*26*	*ADD C2269 [0.1uF] on BATT1.1 trace (pin 1)*	2008/12/17	PV
25	*Slove ESD issue*	*33*	*Add one Diode [D73] on MIC_EXTR, MIC_EXTL (near chip side)*	2008/12/17	PV
26	*Slove ESD issue*	*33*	*Change cap value [C2270,C2271,C2272,C2273] to 0.1uF*	2008/12/17	PV
27	*Slove Audio issue*	*34*	*Change cap value to 2.2uF [C2239,C2240]*	2008/12/17	PV
28	*Slove non-RoHS Part*	*30*	*Change C2157,C2160,C2215 and C2217 Part number [from SE070104Z00 to SE070104Z80]*	2008/12/17	PV

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	Slove ESD ISSUE	30	ADD R2262 [4.7K] and C2274 [0.01 uF] [Default unmount]	2008/12/17	PV
30	Slov Audio EISSUE	34	Change JAUDIO [Audio conn] pin defination	2008/12/17	PV
31	Slove Audio ISSUE	33	DEL R2204	2008/12/17	PV
32	Slove Q Die and E Die		Just use Qim and Hynix VRAM on PV		
33	ESD Request	38	ADD C2275,D74,D75 and D76		
34	ESD Request	34	Modify D66 location		
35	ESD Request	18	Do not moundt D5,D6 and D7		
36	ESD Request	30	Do not mount D62		
37	ESD Request	35	Do not mount D45 and D46		
38	ESD Request	35	Do not mount D47		
38					
38					

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1					
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Compal Electronics, Inc.

Title: **HW PIR**

Size | Document Number: *LA-4731P Rhett discrete* | Rev: 0.1

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