Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2008-01-01

Diễn Đàn
KyThuatViTinh.Com

Digitally signed by dd
DN: cn=dd, o=dd, ou=dd, email=dddd@yahoo.com, c=US
Date: 2009.11.12 09:03:29 +07'00'

機密 等級 硬體二部
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產出日期
解密日期

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Title: *Cover Sheet*

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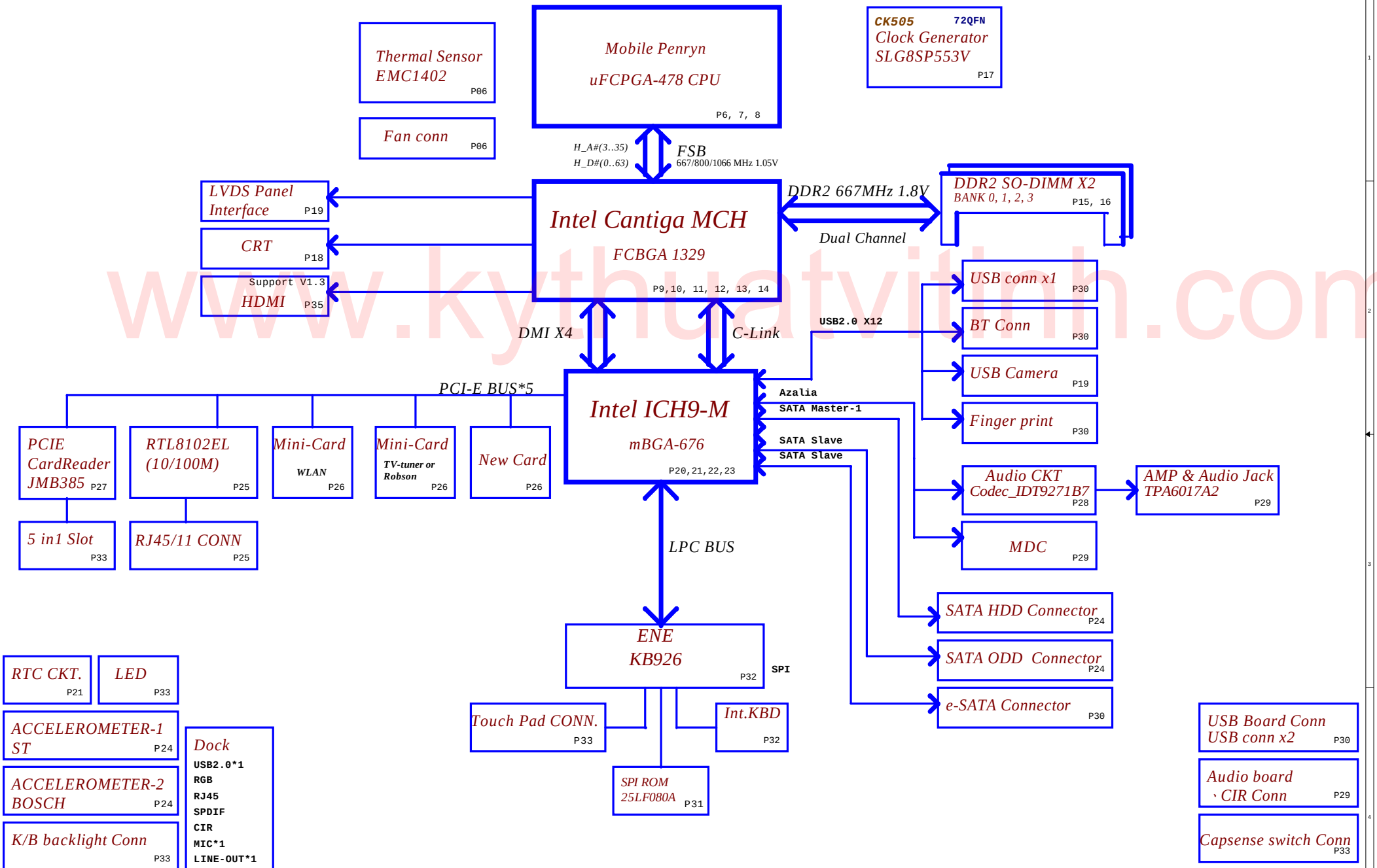
Montevina Consumer 14" UMA



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Title	Block Diagram		
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
43154432L04 : OPP@/DEBUG@
43154432L05 : OPP@/DEBUG@

43154432L01 : UMA GM PA FF (SI-1)
43154432L02 : UMA GM PR FF (SI-1)
43154432L03 : UMA GL PR FF-
43154432L04 : UMA GM OPP (SI-1)
43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
ICH9M A2 ES2 Base : SA00002AN10

DA600007100 --->Main
DAZ03V00100 --->OPP

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Title: Notes List

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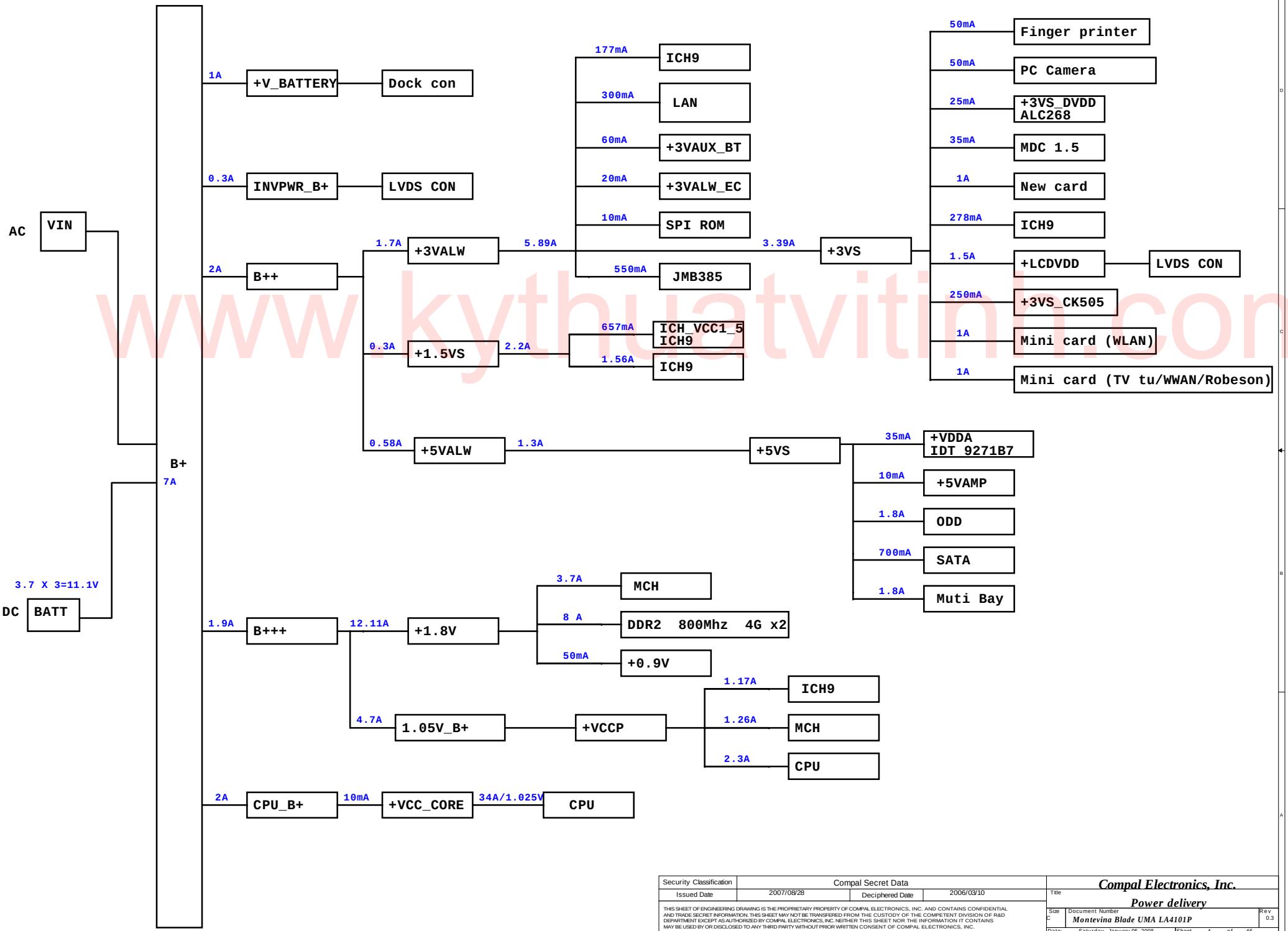

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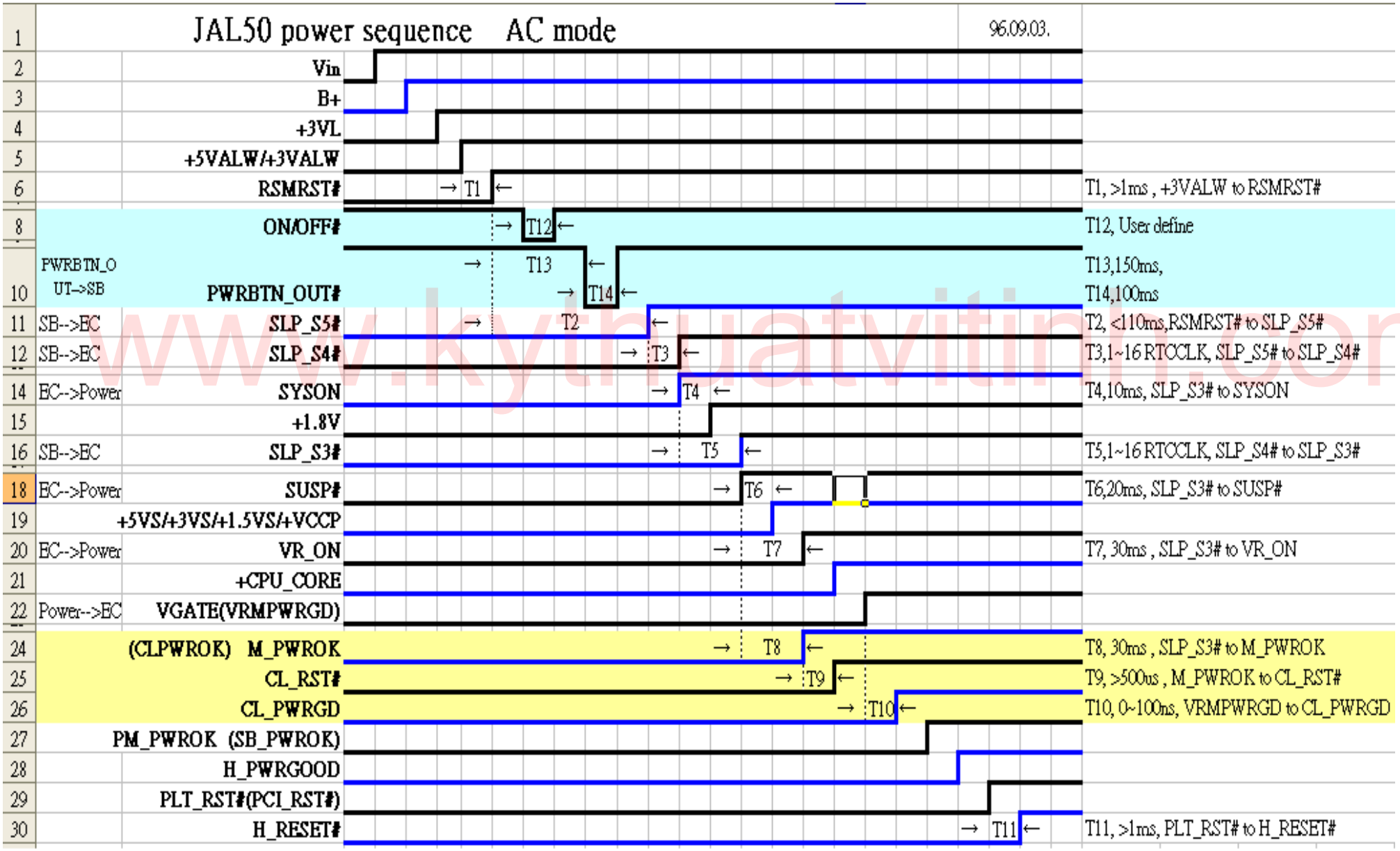

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Compal Electronics, Inc.

Title: **Power sequence**

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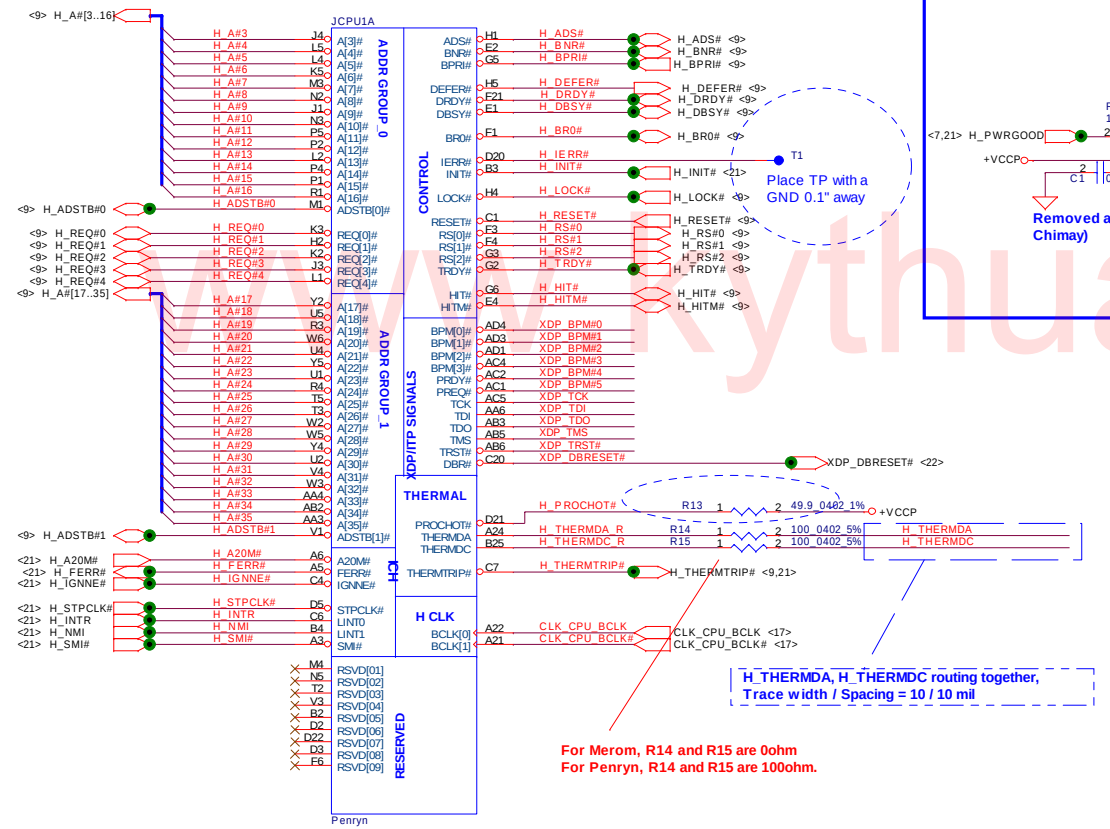
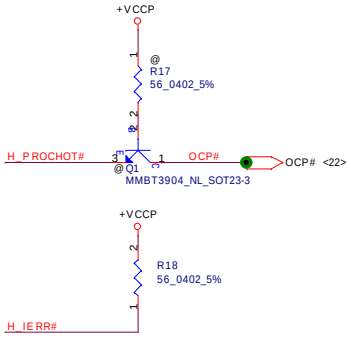
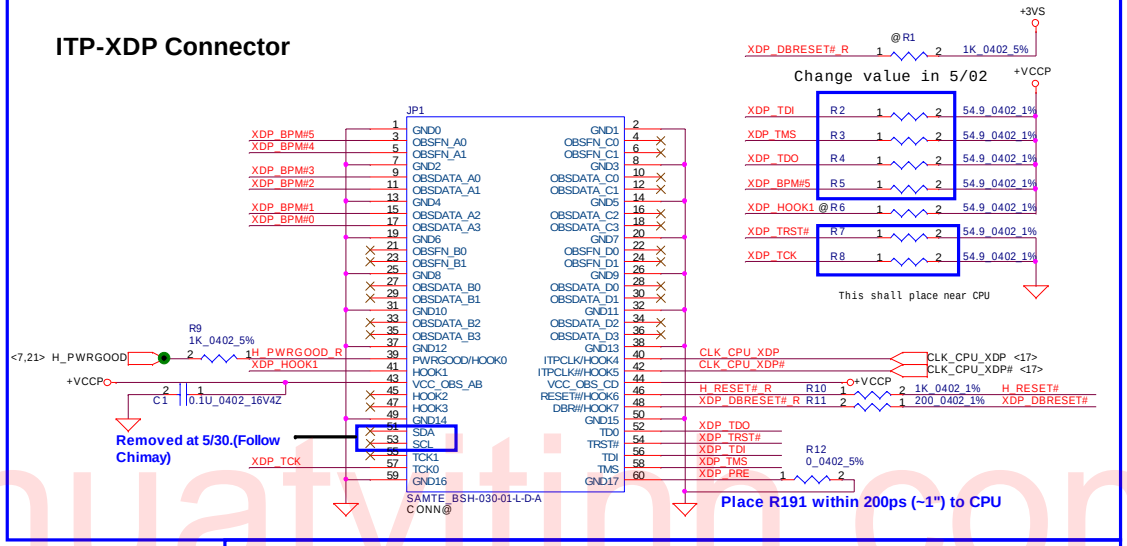
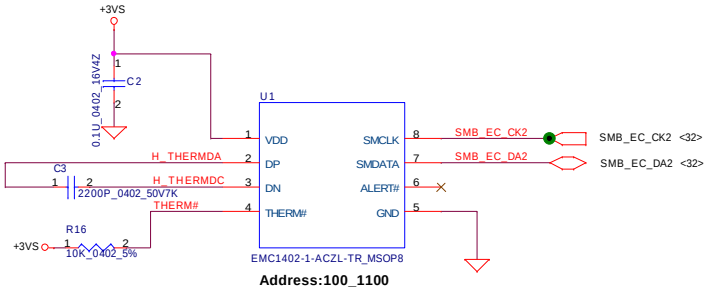


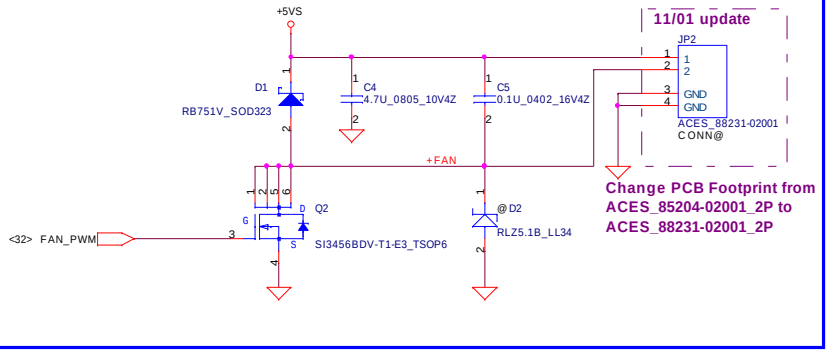


ITP-XDP Connector





PWM Fan Control circuit



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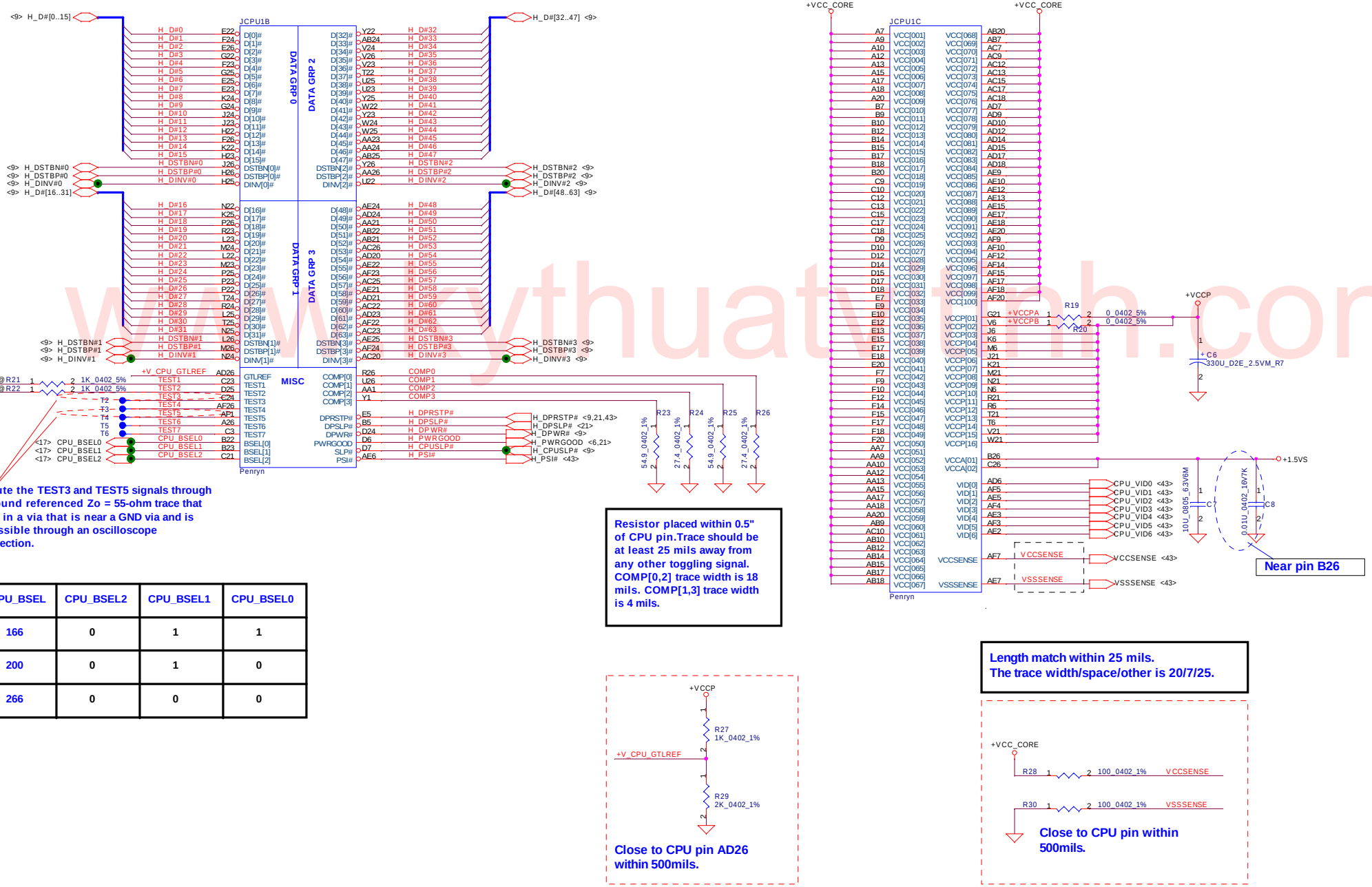

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

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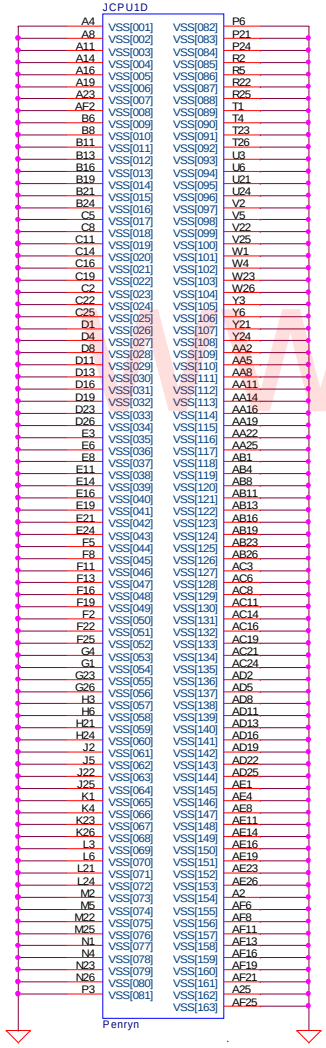
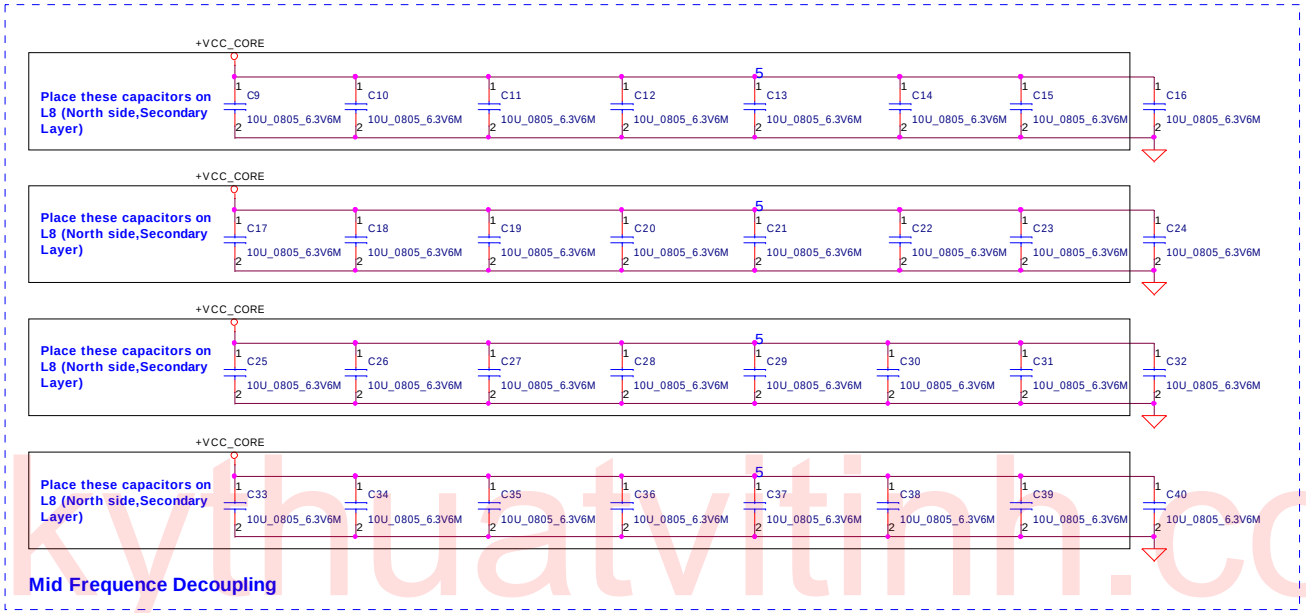
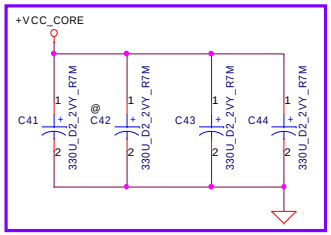


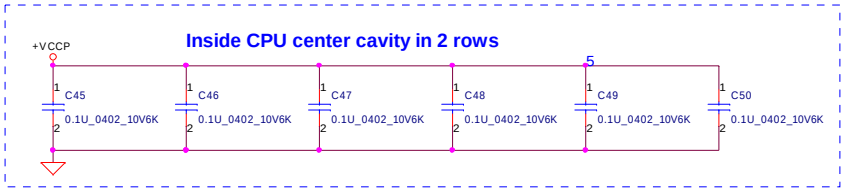


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



11/21 Change ESR=7m ohm



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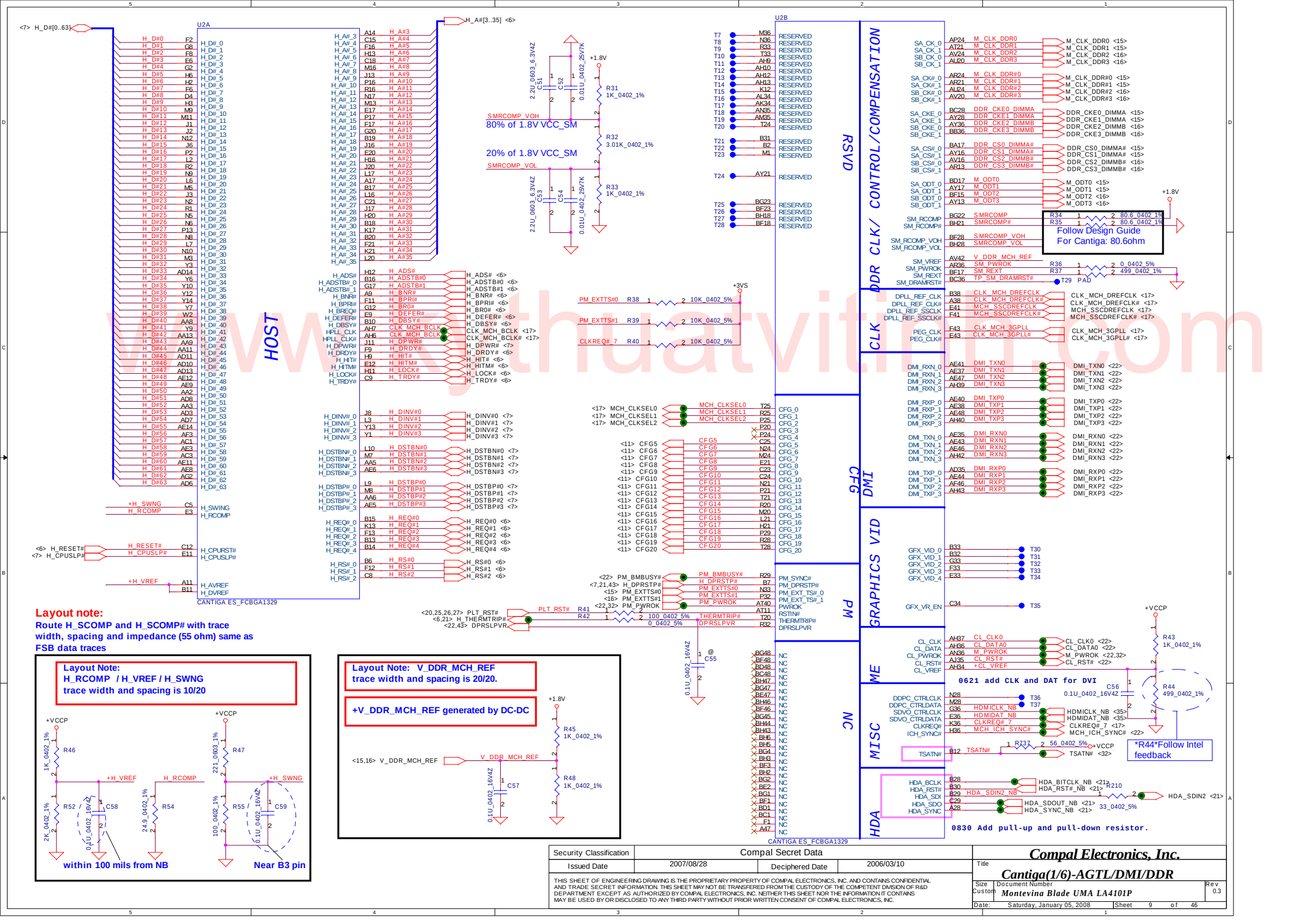
U2A
HOST
CANTIGA ES_FCBGA1329
U2B
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA ES_FCBGA1329
SMRCOMP_VOH
80% of 1.8V VCC_SM
SMRCOMP_VOL
20% of 1.8V VCC_SM
Follow Design Guide
For Cantiga: 80.6ohm
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB
Near B3 pin
Layout Note: V_DDR_MCH_REF
trace width and spacing is 20/20.
+V_DDR_MCH_REF generated by DC-DC
0621 add CLK and DAT for DVI
*R44*Follow Intel feedback
0830 Add pull-up and pull-down resistor.
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Cantiga(1/6)-AGTL/DMI/DDR
Size
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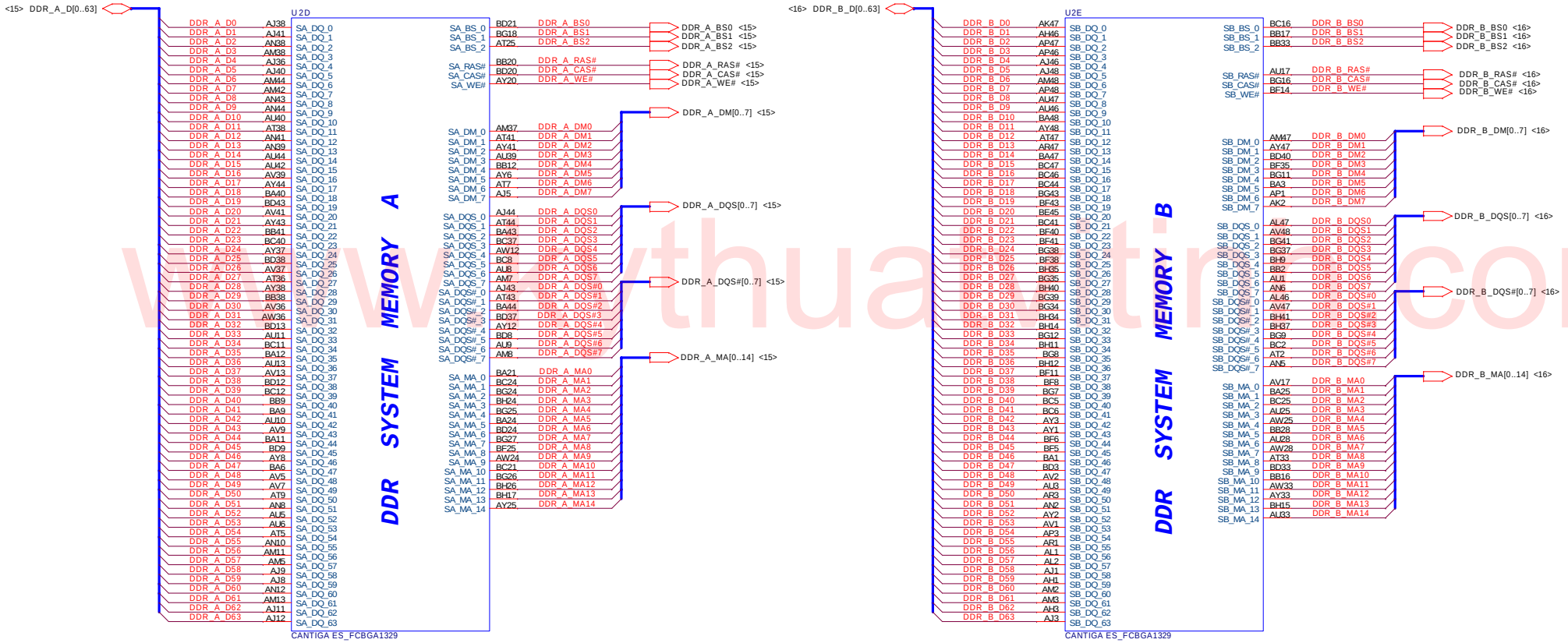

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Title: **Cantiga(2/6)-DDR2 A/B CH**

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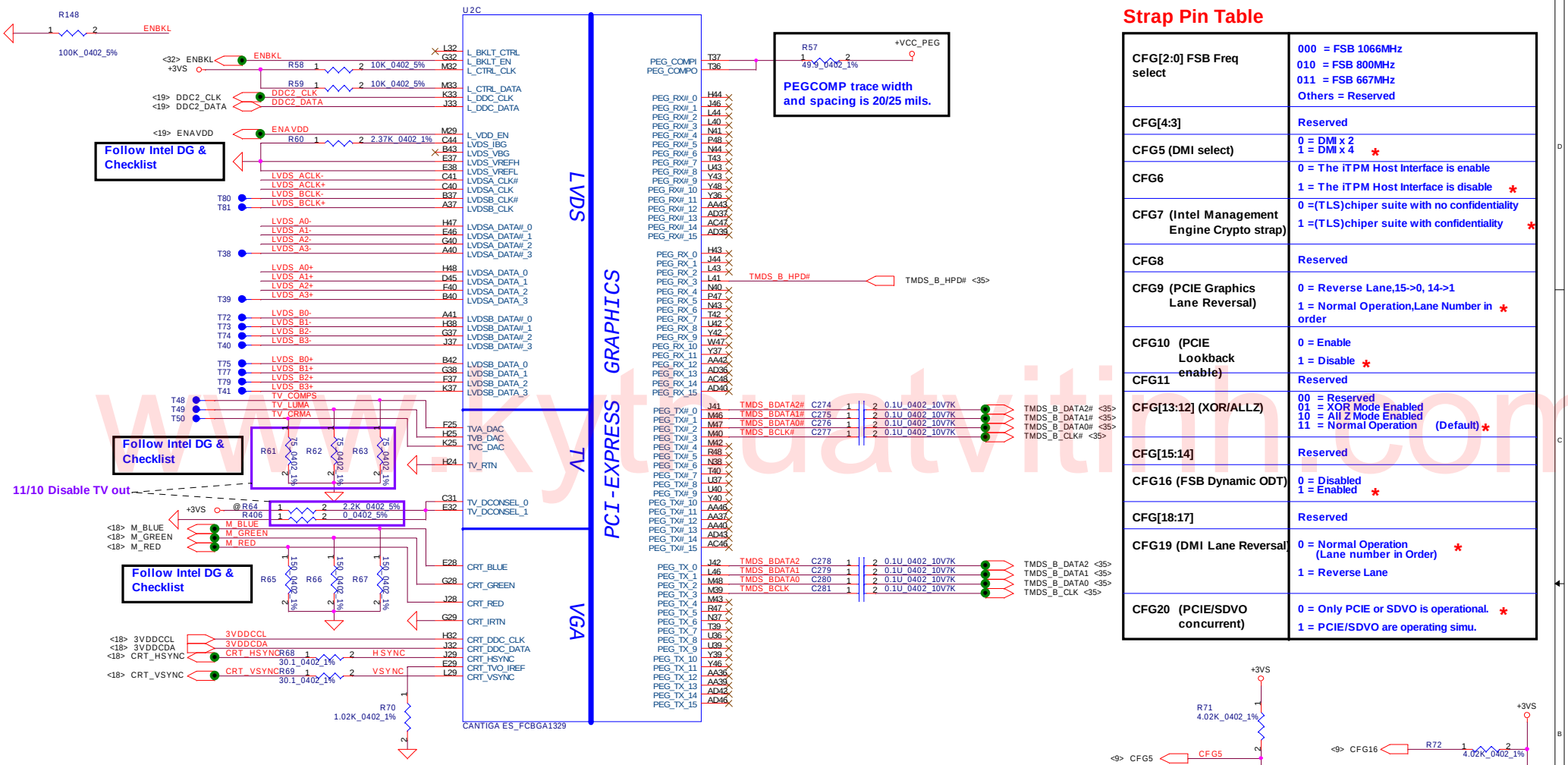

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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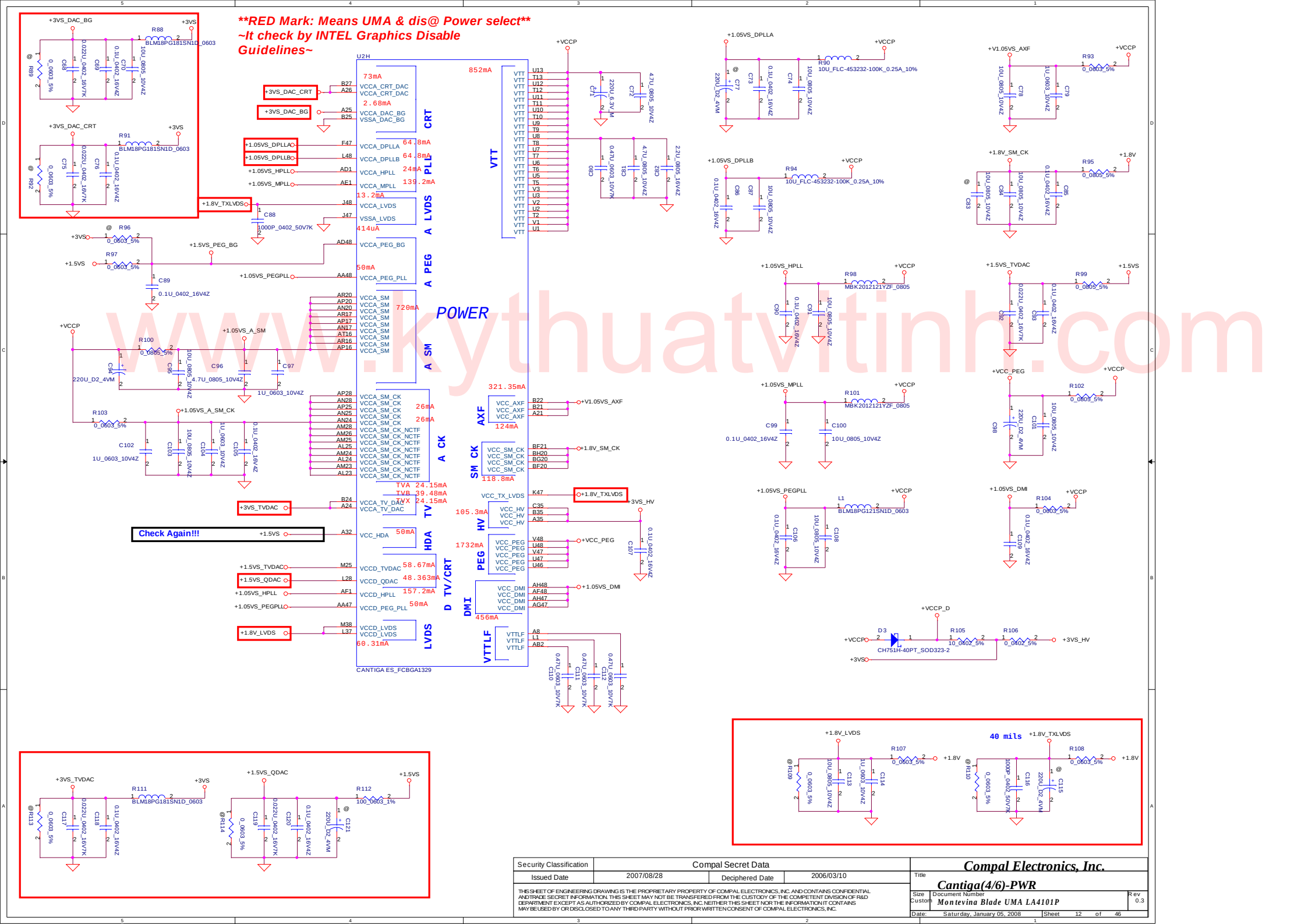

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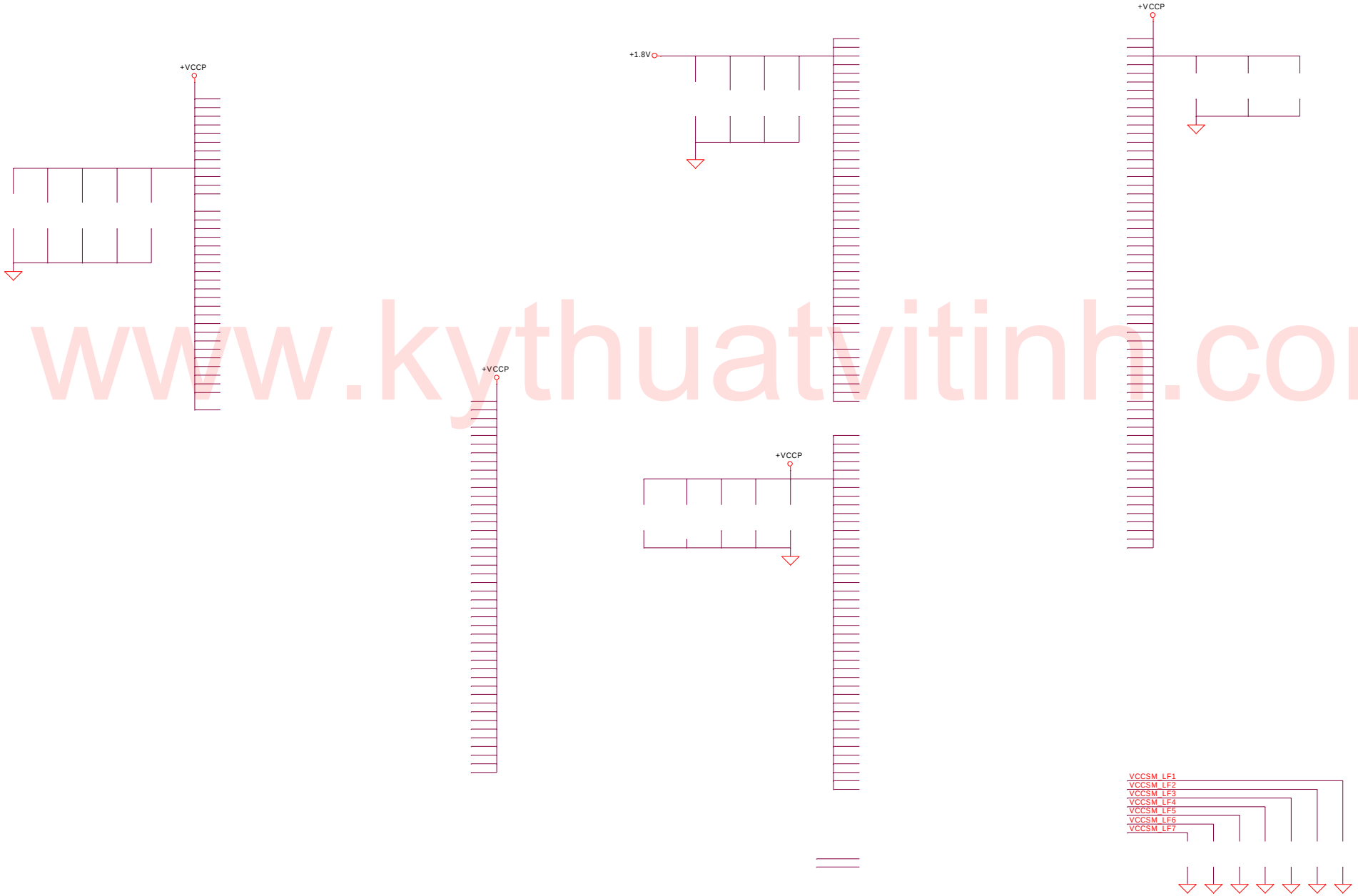

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Title: ***Cantiga(5/6)-PWR/GND***

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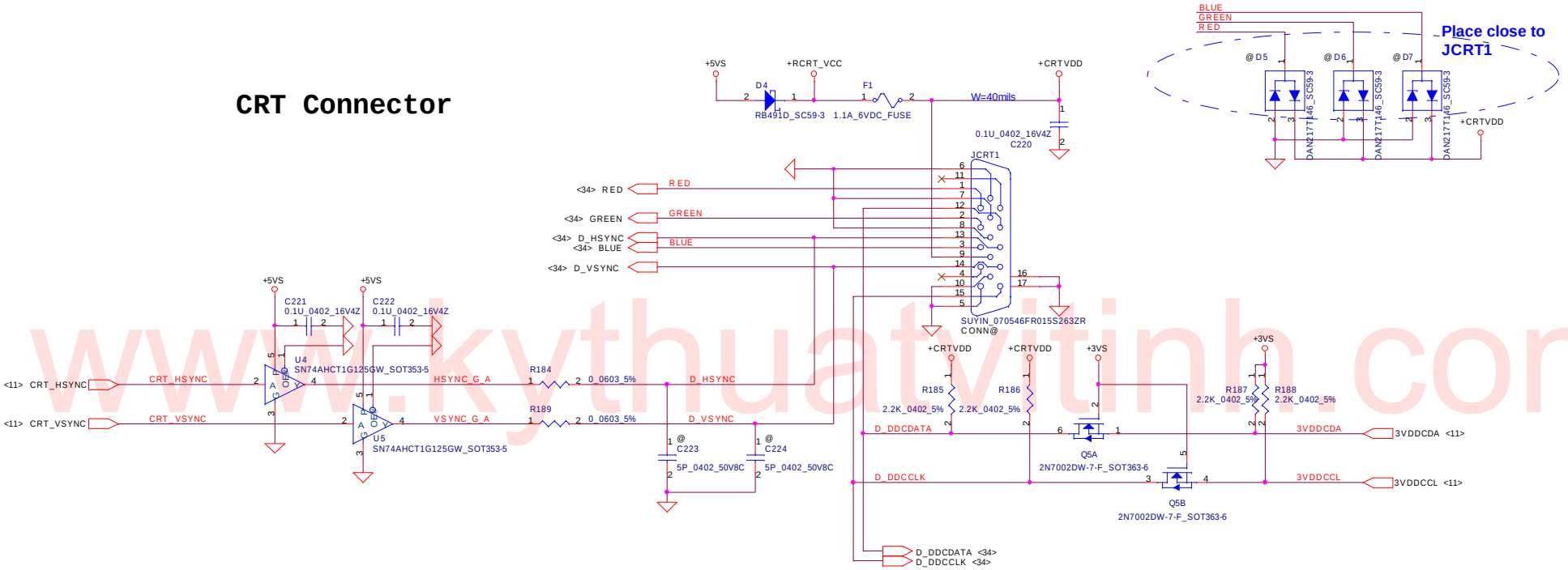
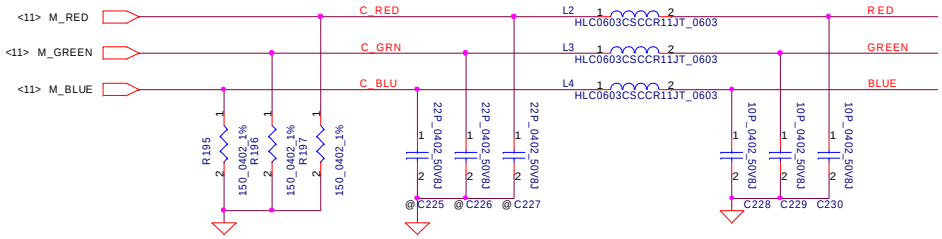
CRT Connector



CRT Termination/EMI Filter

11/07 Change CRT lounting NB-->Docking-->CRT connector



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Title	CRT Connector		
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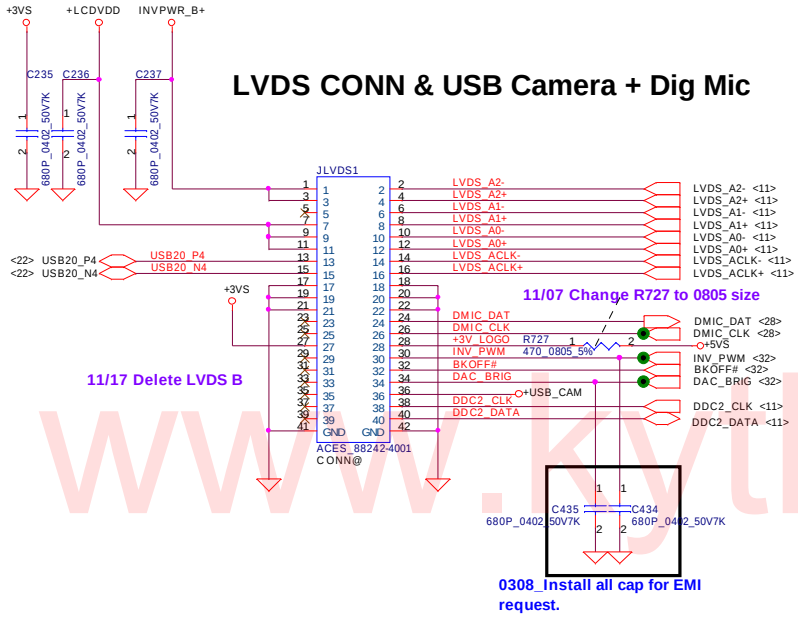
Date: Saturday, January 05, 2008	Sheet 18 of 46		

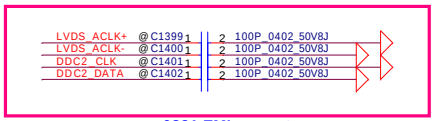
LVDS CONN & USB Camera + Dig Mic



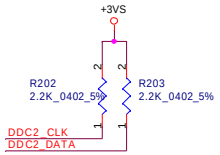
11/07 Change R727 to 0805 size

11/17 Delete LVDS B

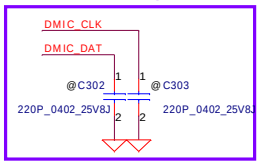
0308_Install all cap for EMI request.



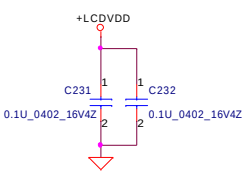
0831 EMI request

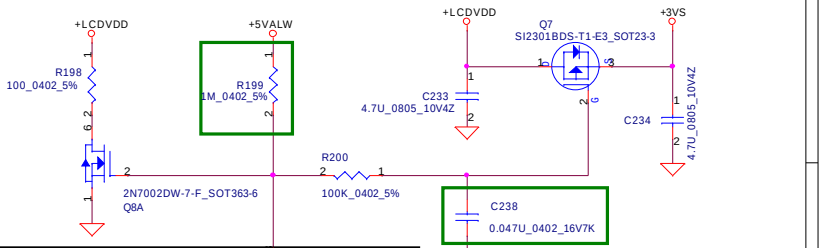


Must close JLVDS1pin 24、26



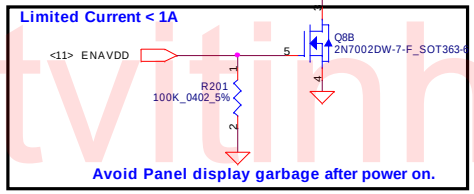
11/09 EMI reserver



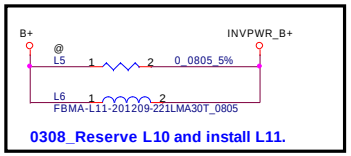


01/03 Change to 0.047u to meet T1 timing

Limited Current < 1A

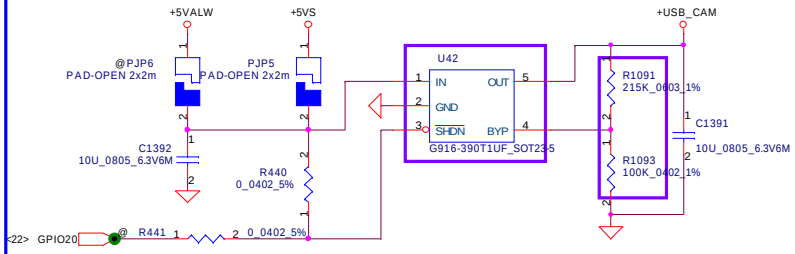


Avoid Panel display garbage after power on.



0308_Reserve L10 and install L11.

USB Camera



11/07 Change U42 to 3.9V LDO(Adjustable)

11/07 Change R1091 to 215K、R1093 to 100K

11/08 Change C1391、C1392 to 0805 size

+USB_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB_CAM=1.25(1+R1091/R1093)

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Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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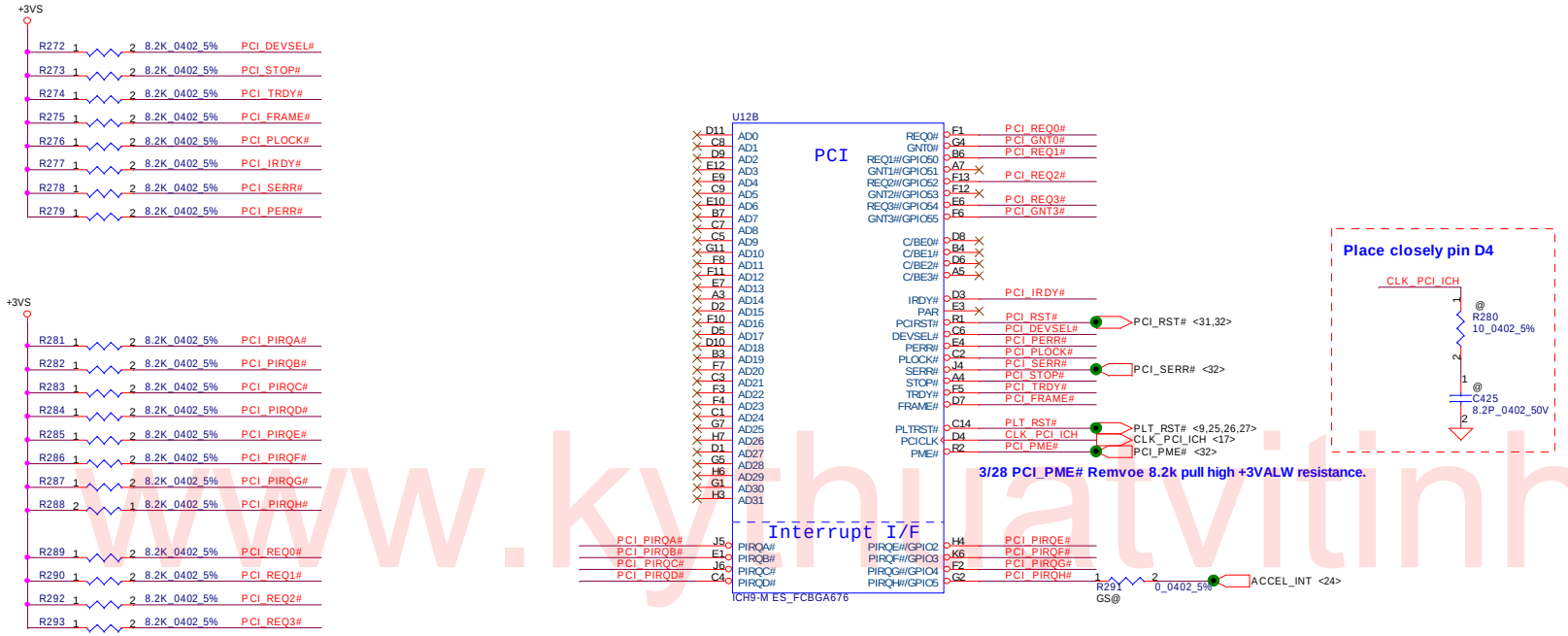
Compal Electronics, Inc.			
Title	LCD CONN.		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 19 of 46		



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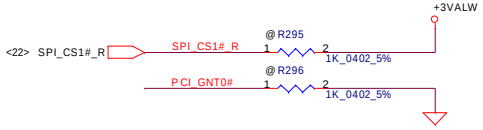
A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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Issued Date	2007/08/28	Deciphered Date	2006/03/10

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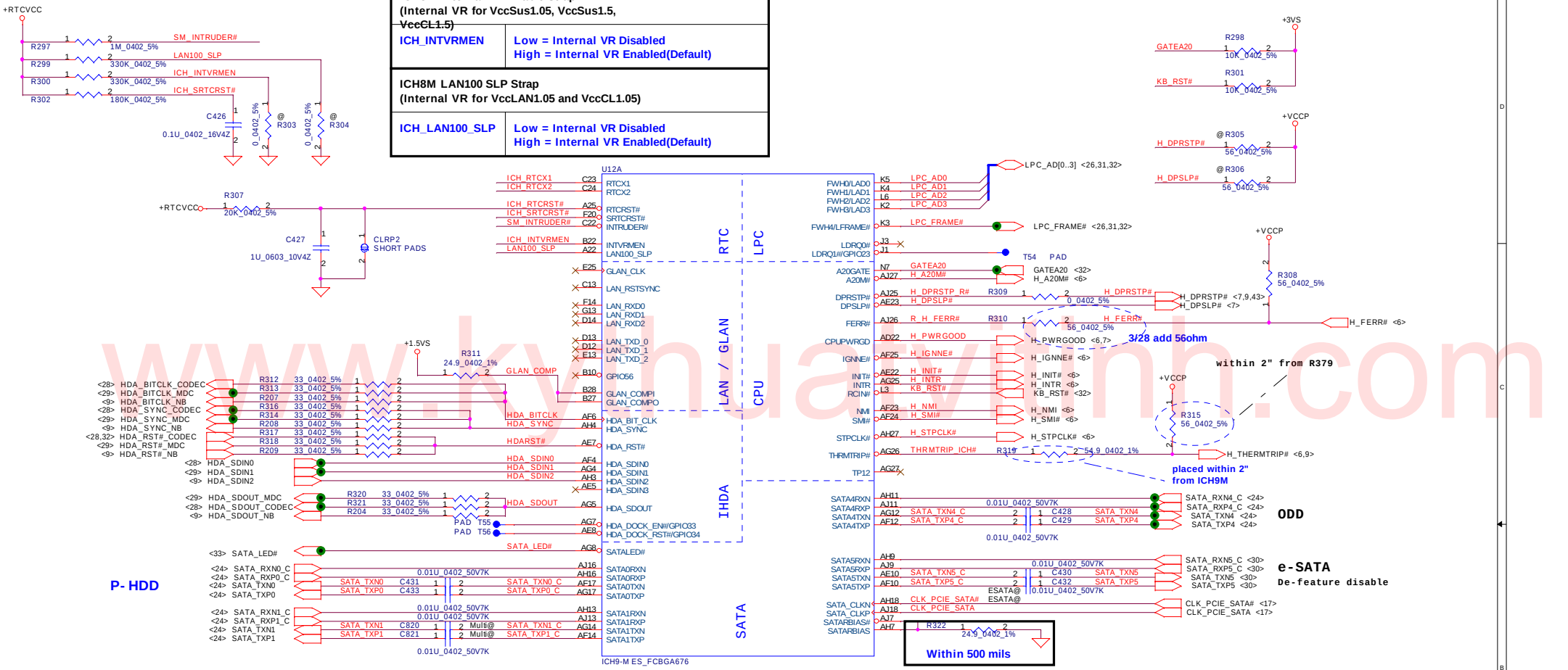
Compal Electronics, Inc.	
Title	ICH9(1/4)-PCI/INT
Size	Document Number: Montevina Blade UMA LA4101P
Rev	0.3
Date: Saturday, January 05, 2008	Sheet 20 of 46

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 21 of 46

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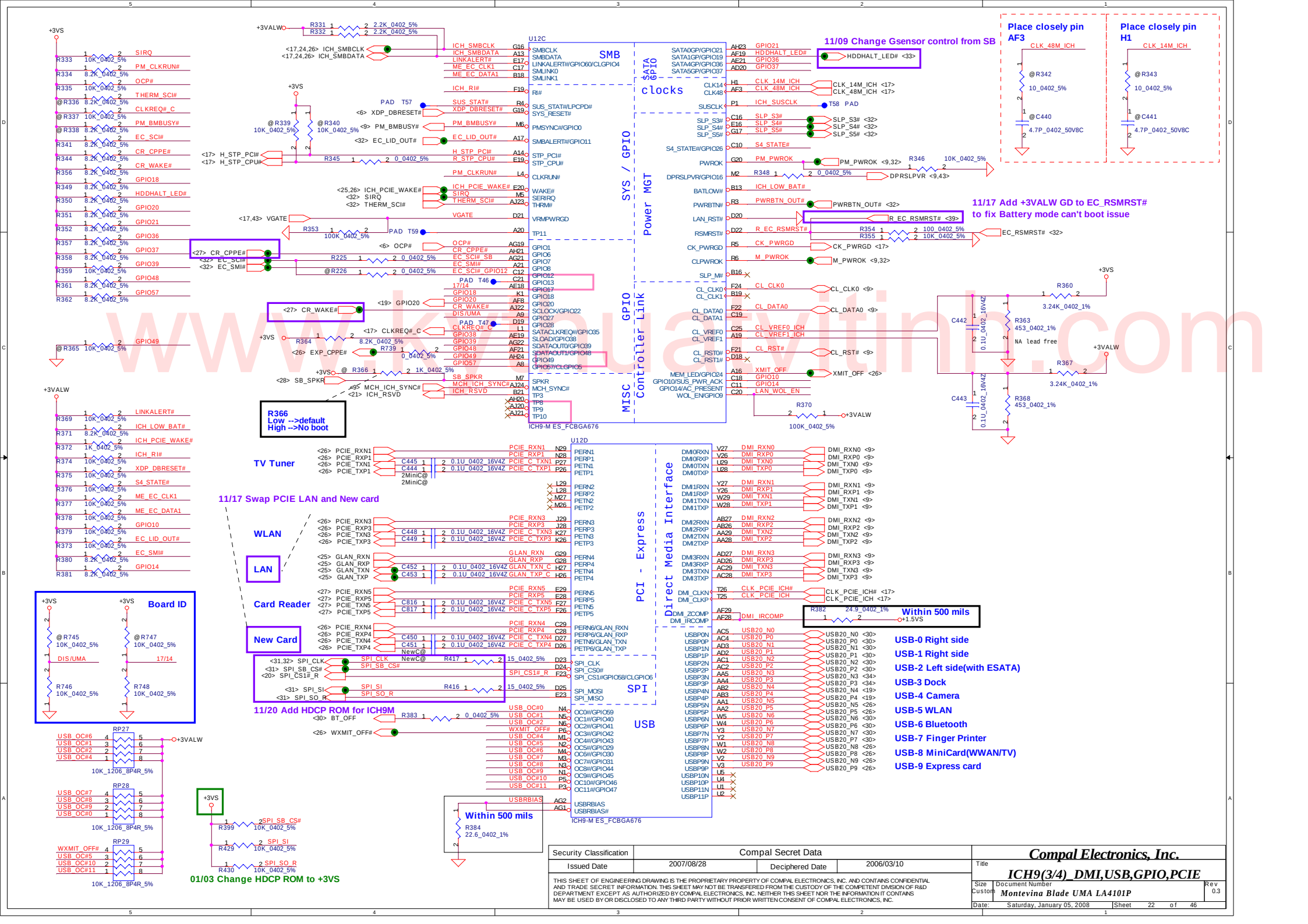
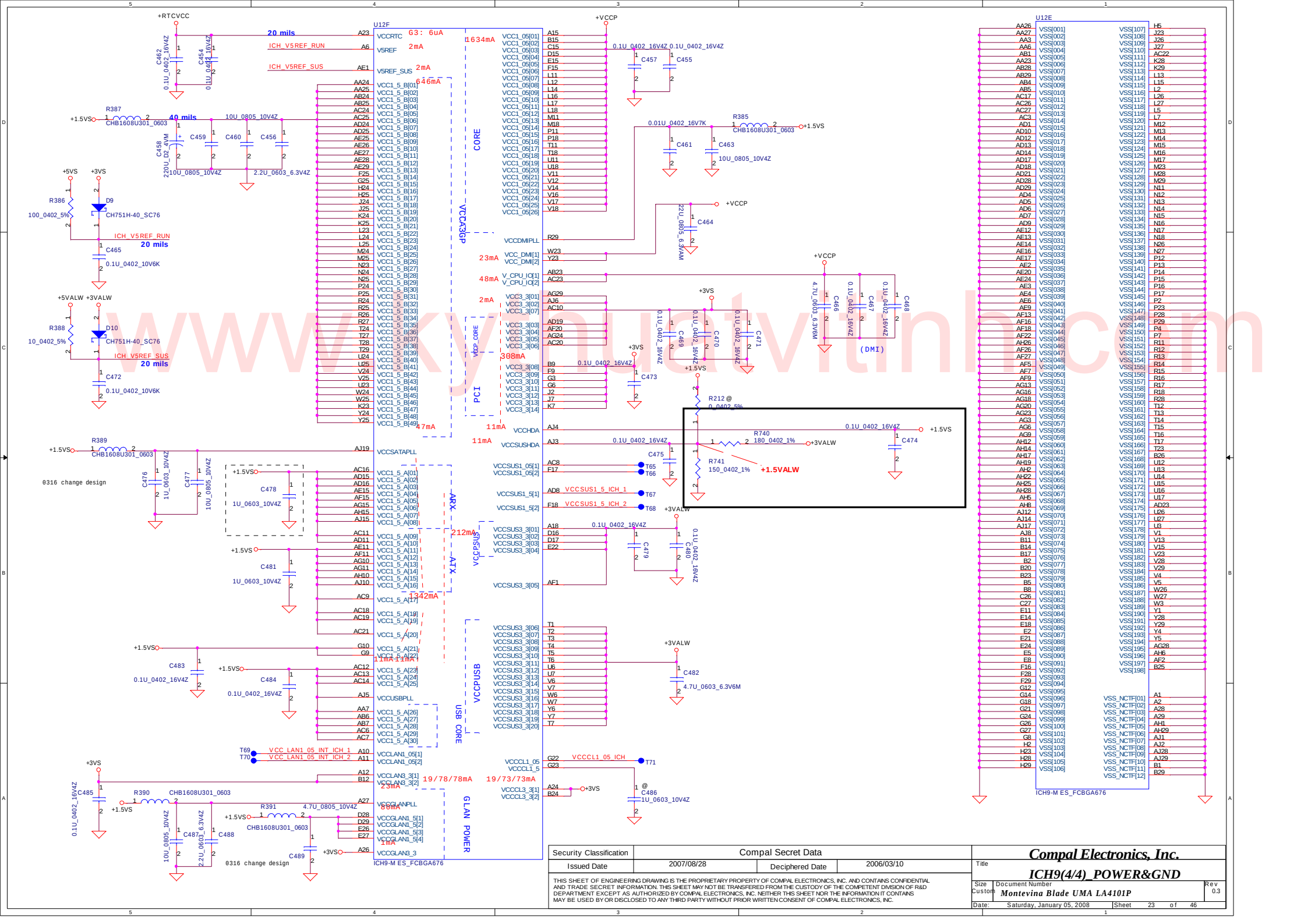


www.kyeuaytinh.com



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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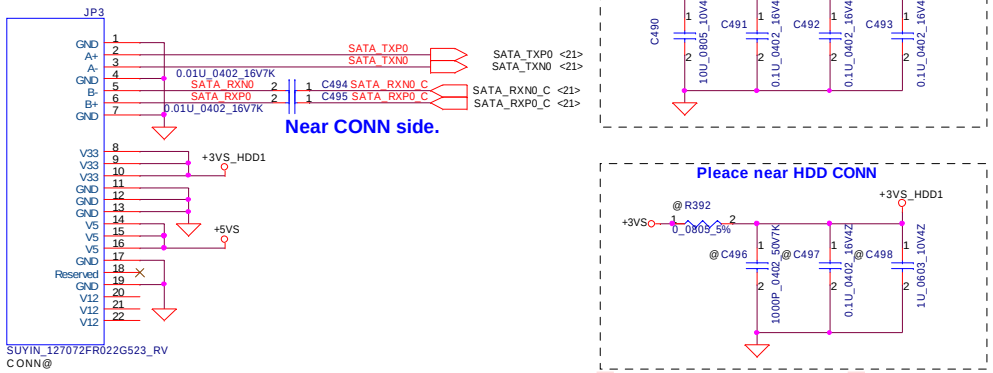
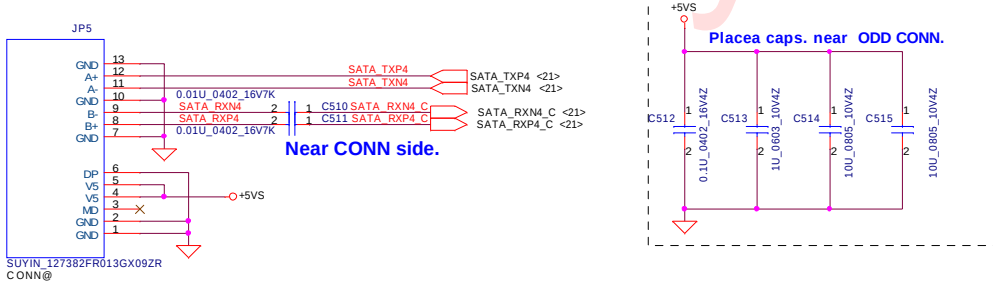
Compal Electronics, Inc.			
Title: ICH9(4/4)_POWER&GND			
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 23 of 46		

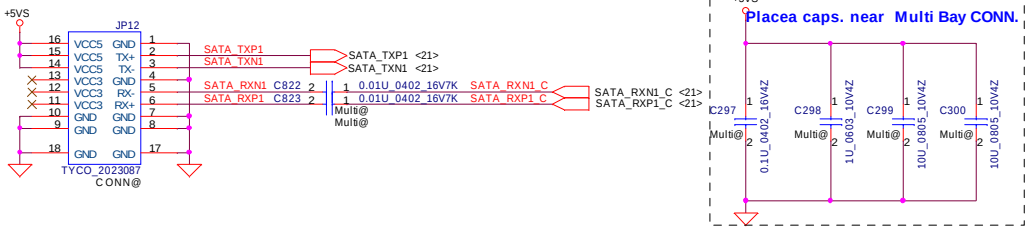
HDD Connector



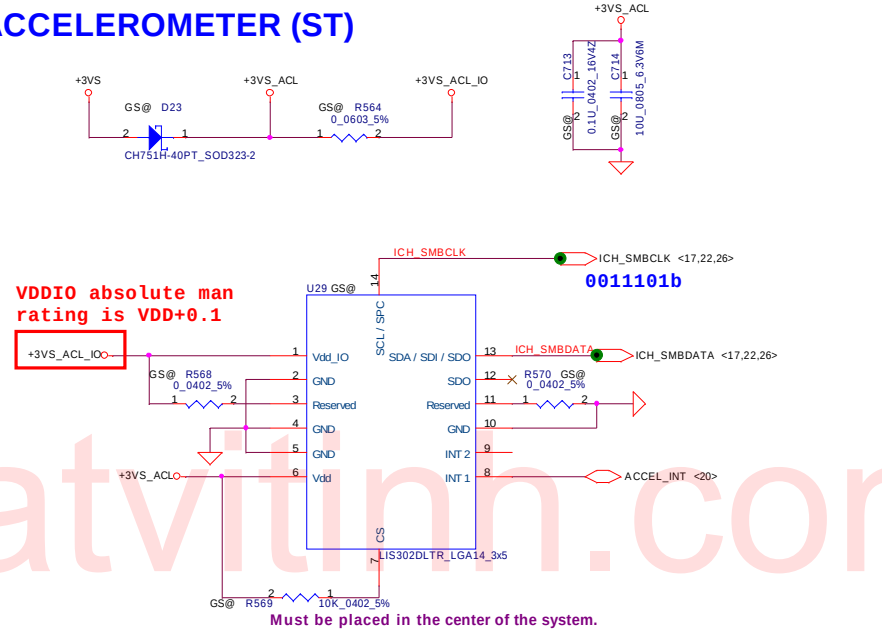
CD-ROM Connector



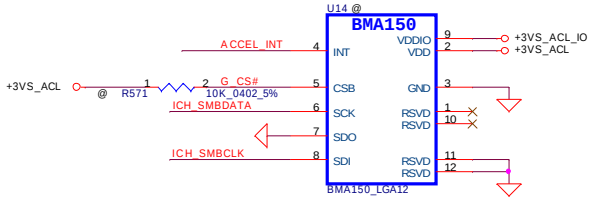
Multi Bay



ACCELEROMETER (ST)



ACCELEROMETER (Bosch)



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ZZZ2
PCB-MB

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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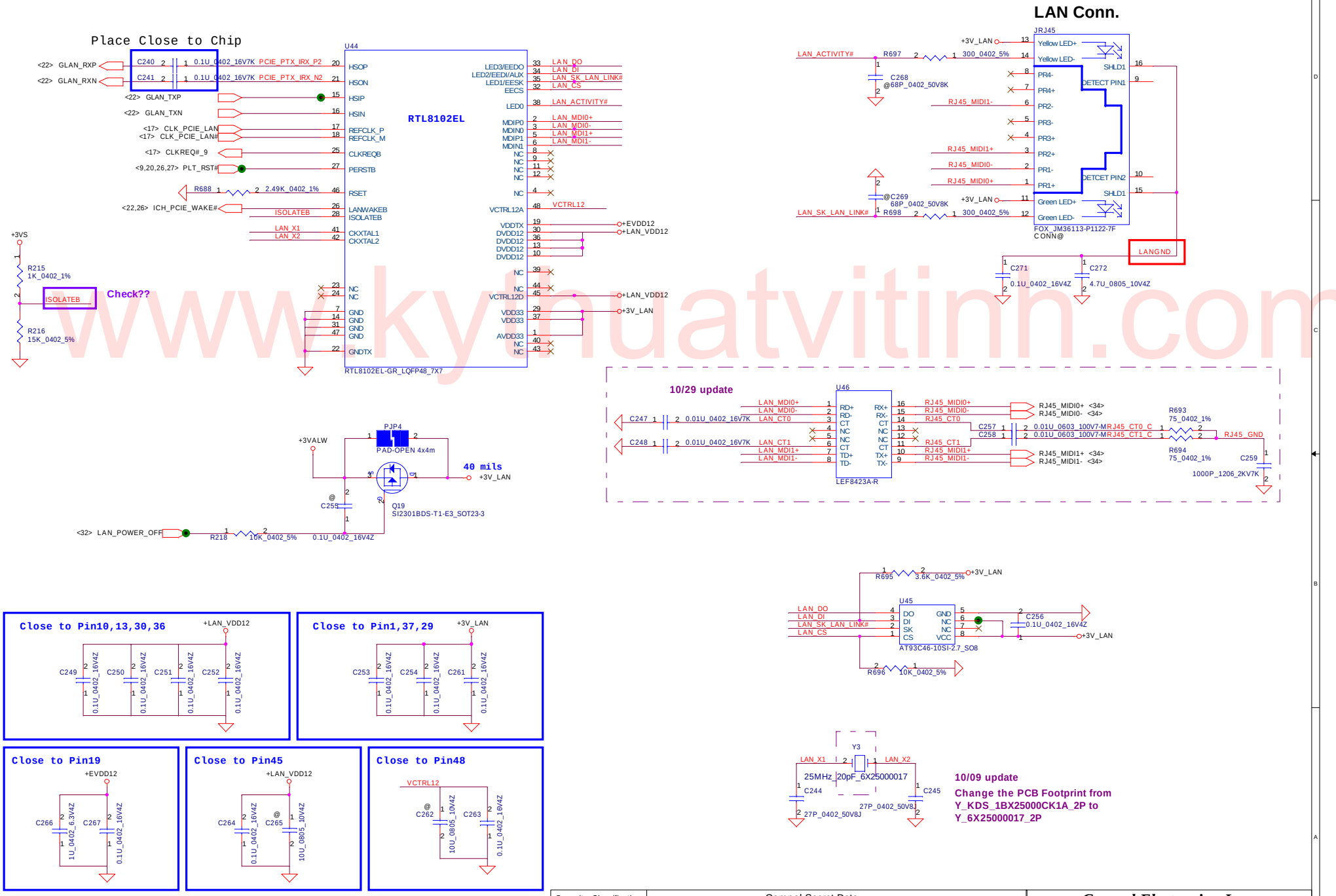
Compal Electronics, Inc.

Title: **HDD & CDROM**

Size: Custom | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 24 of 46



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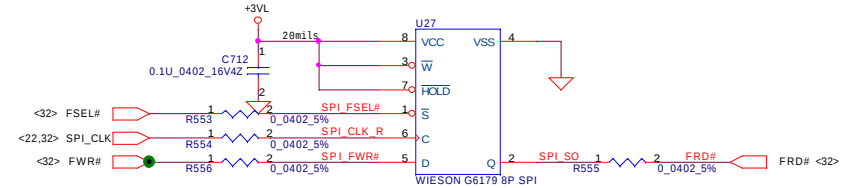
Compal Electronics, Inc.

Title: RTL8102EL LAN

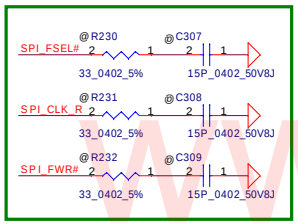
Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 25 of 46

SPI ROM

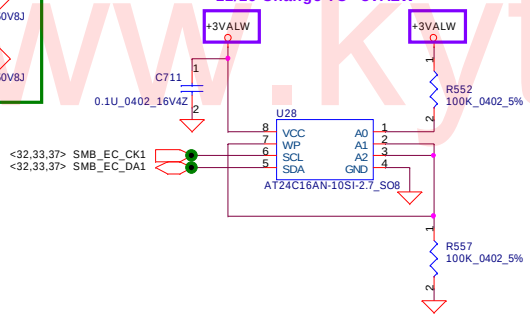


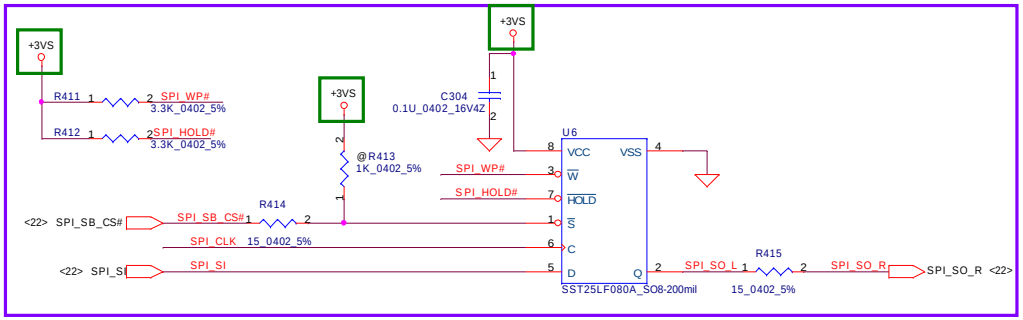
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request

11/16 Change TO +3VALW



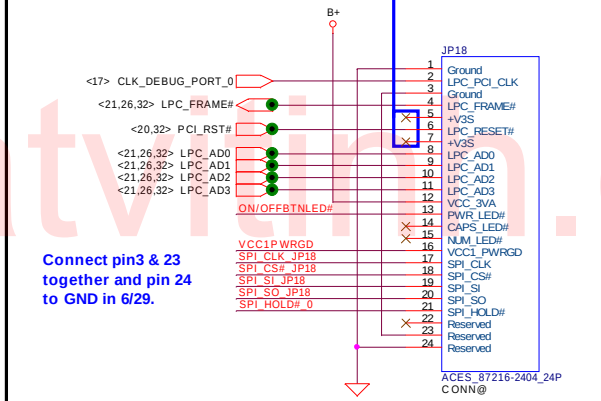


11/17 Add SB HDCP ROM

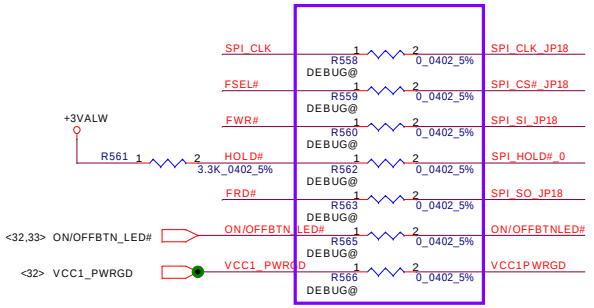
01/03 Change HDCP ROM to +3VS

LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



Connect pin3 & 23 together and pin 24 to GND in 6/29.



11/07 Add 0 Ohm for debug port

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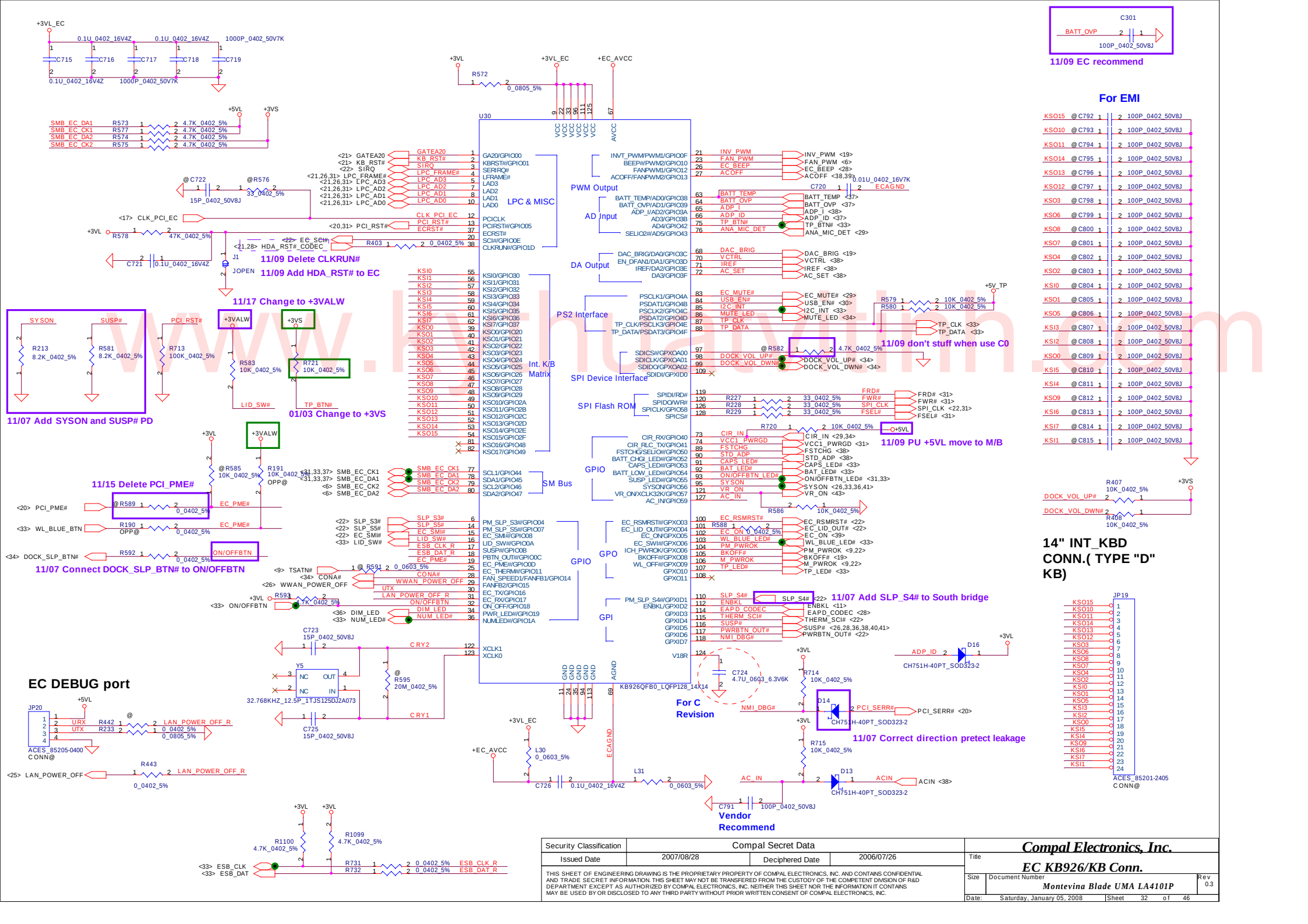
Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 31 of 46


U30
KB926QFB0_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
11/09 EC recommend
For EMI
11/09 Delete CLKRUN#
11/09 Add HDA_RST# to EC
11/17 Change to +3VALW
11/07 Add SYSON and SUSP# PD
01/03 Change to +3VS
11/09 don't stuff when use C0
11/09 PU +5VL move to M/B
11/15 Delete PCI_PME#
11/07 Connect DOCK_SLP_BTN# to ON/OFFBTN
11/07 Add SLP_S4# to South bridge
14" INT_KBD CONN.(TYPE "D" KB)
EC DEBUG port
For C Revision
11/07 Correct direction pretect leakage
Vendor Recommend
Compal Electronics, Inc.
EC KB926/KB Conn.
Montevina Blade UMA LA4101P
Compal Secret Data
2007/08/28
2006/07/26
Saturday, January 05, 2008

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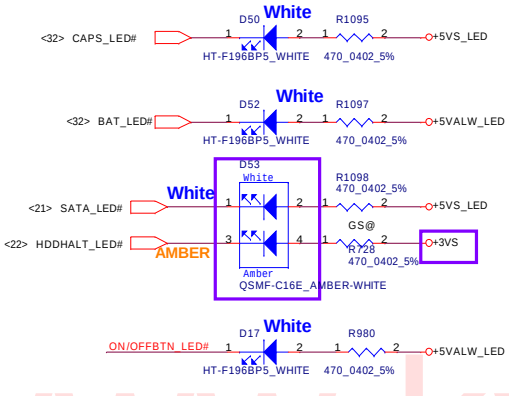
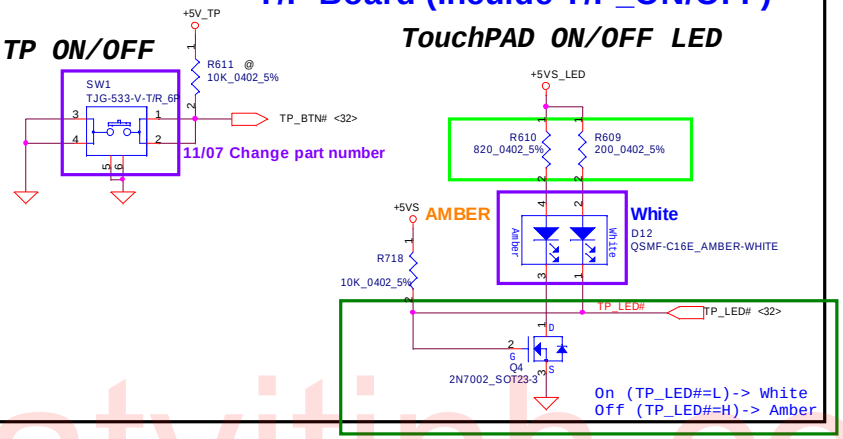
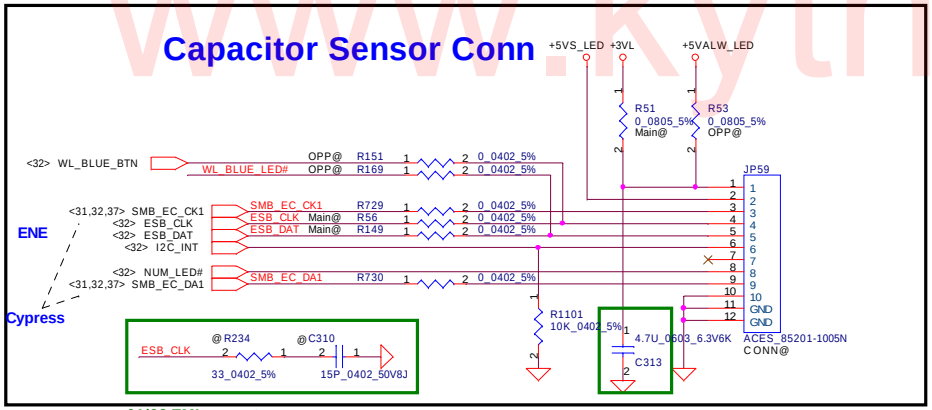
System LED



T/P Board (Inculde T/P_ON/OFF)

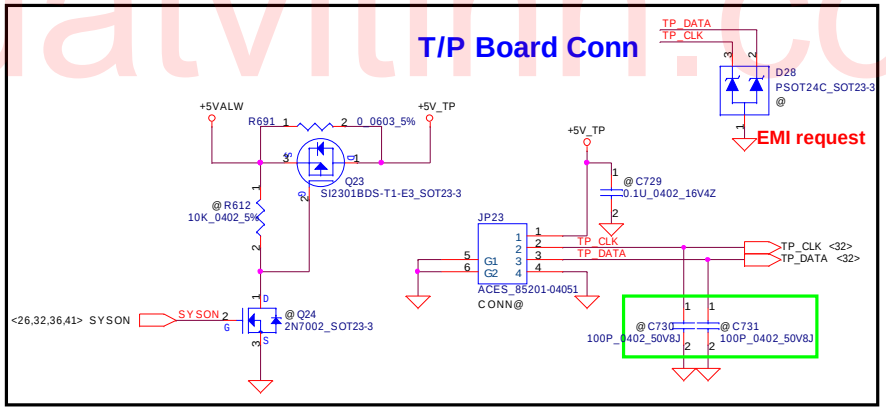


Capacitor Sensor Conn

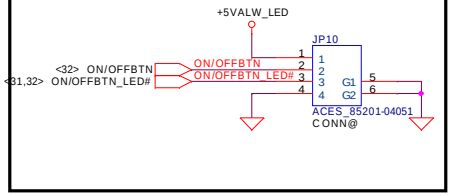


01/03 EMI request

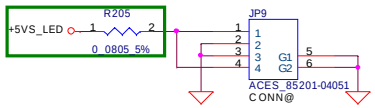
T/P Board Conn



ON/OFF Button Connector

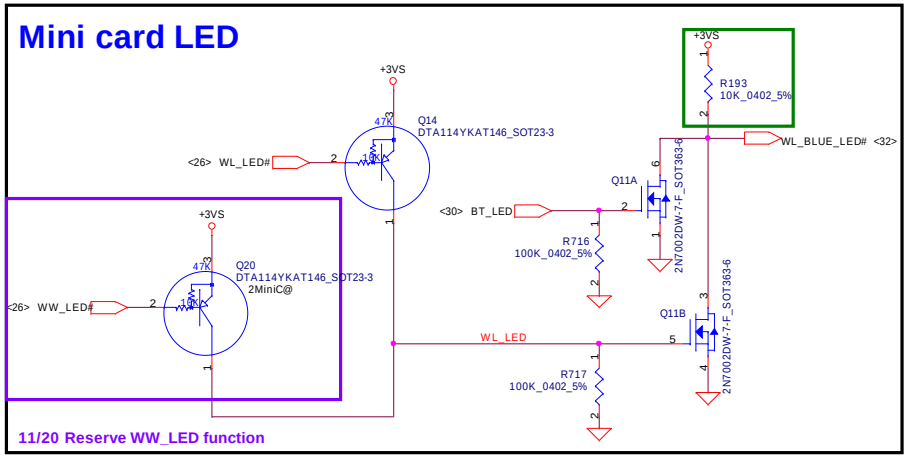


Keyboard backlight Conn

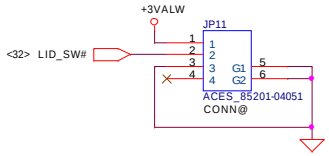


01/03 Keyboard backlight reserve a 0805 size resistor

Mini card LED



Lid Switch Connector



01/03 Change Lid switch connector type

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Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

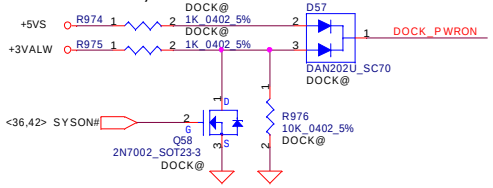
Title: KBD, ON/OFF, SW, CIR

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 33 of 46

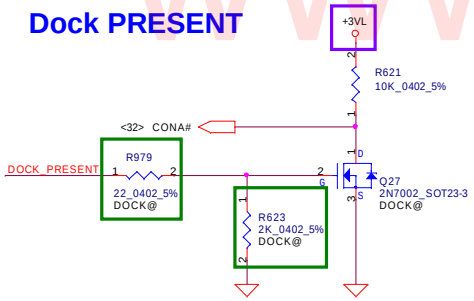
Atlas/ Saturn Dock

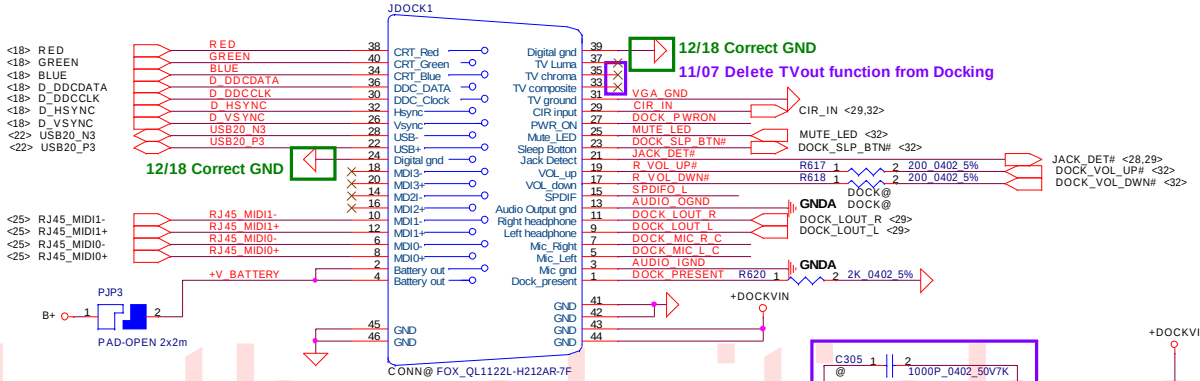
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

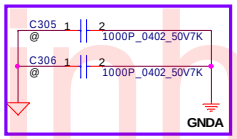


Dock PRESENT

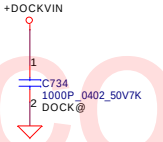
11/12 Change to +3VL





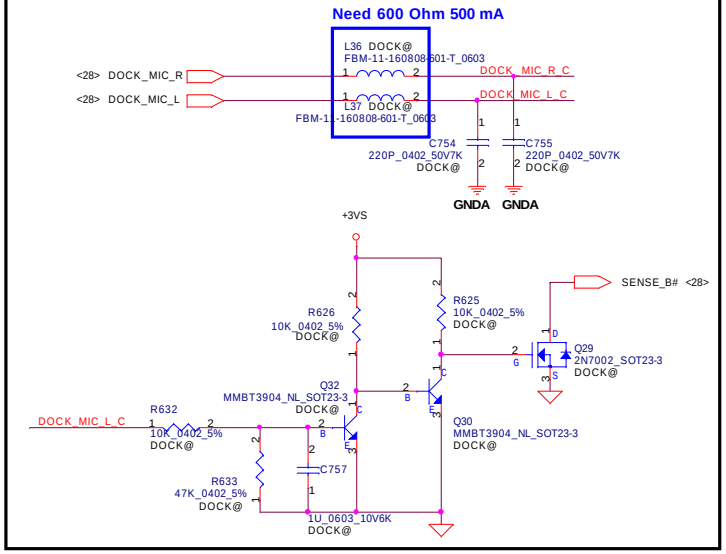


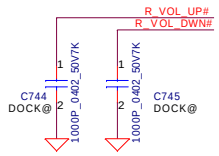
11/17 Reserve

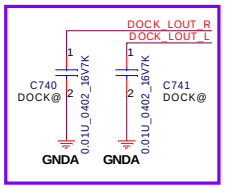


MIC_Dock

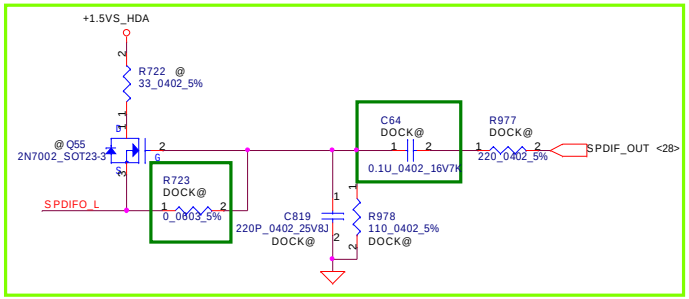
Need 600 Ohm 500 mA







11/17 Recommend



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Compal Electronics, Inc.

Title: **DOCK CONN.**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

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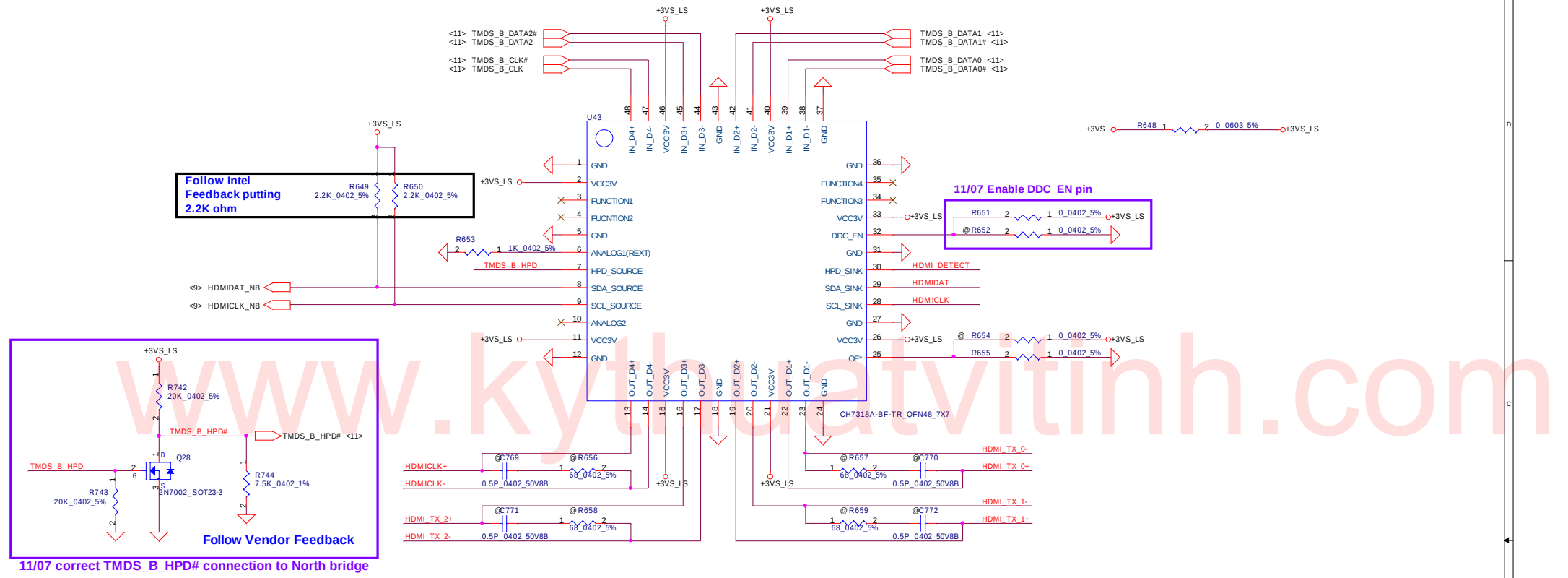

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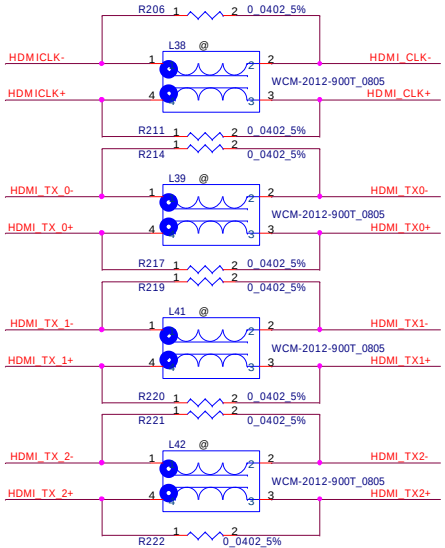
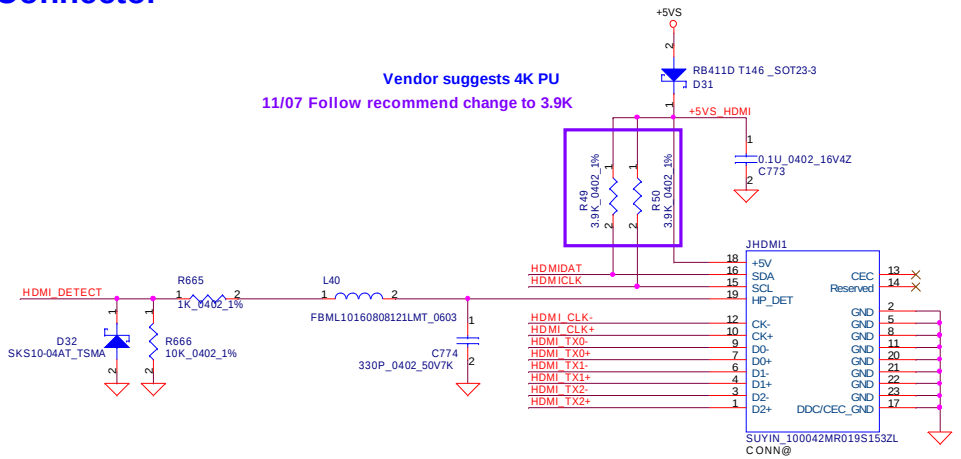


01/03 Reserver 0 ohm co lay with common choke

HDMI Connector



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Compal Electronics, Inc.			
Title: HDMI LS & Conn.			
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
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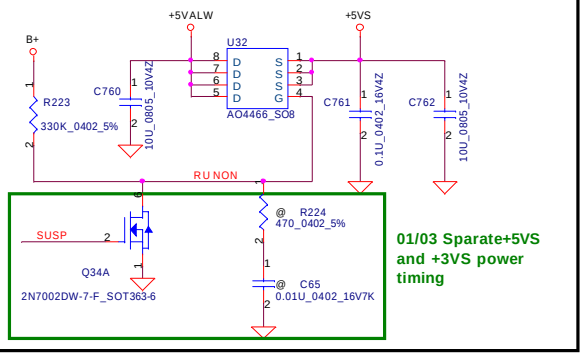
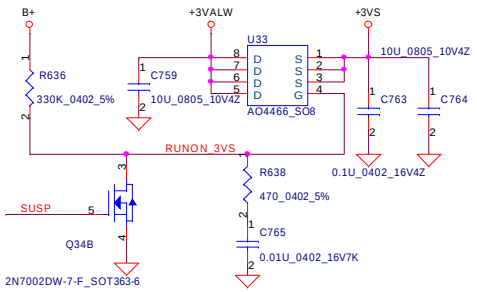
+5VALW to +5VS Transfer

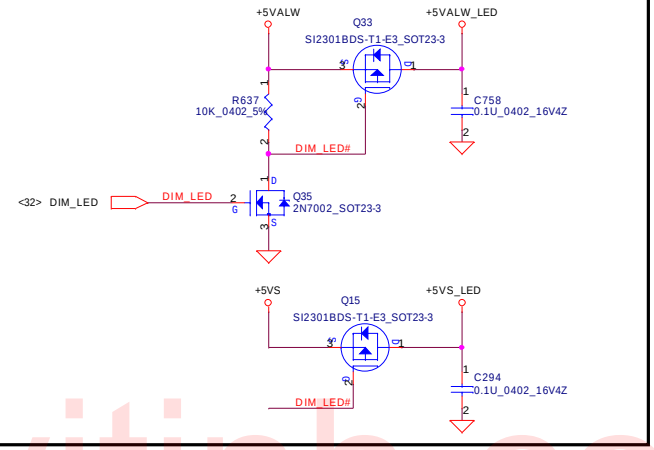


01/03 Sparate+5VS and +3VS power timing

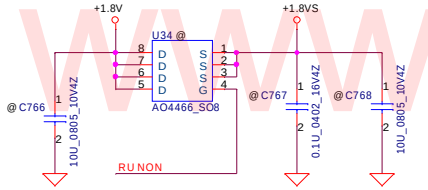
+3VALW to +3VS Transfer



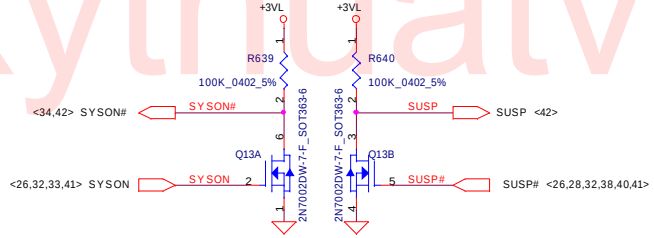
DIM LED



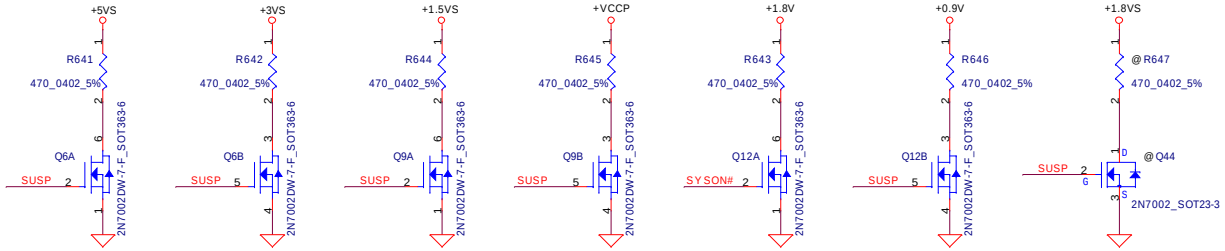
+1.8V to +1.8VS Transfer

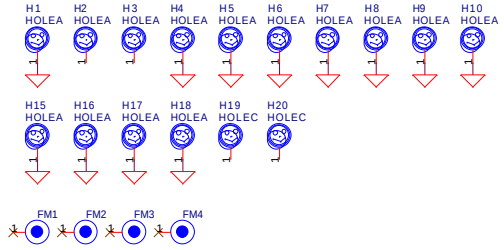


11/07 BOM Delete +1.8VS for Cardreader internal LDO



Discharge circuit





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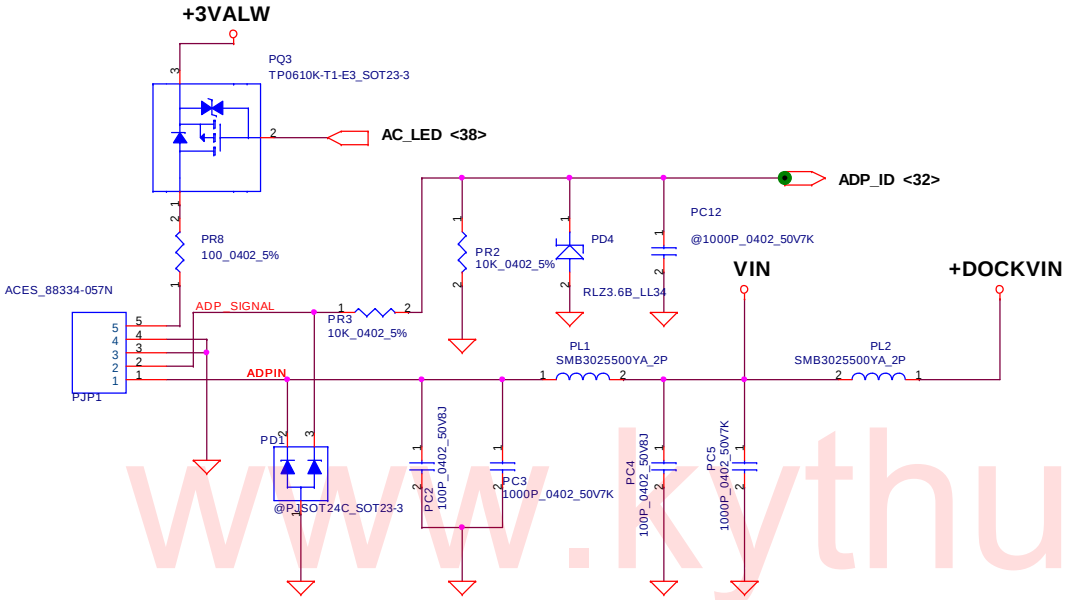
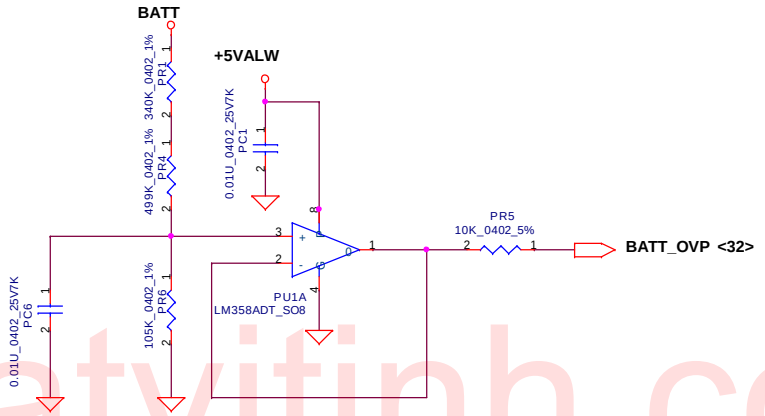
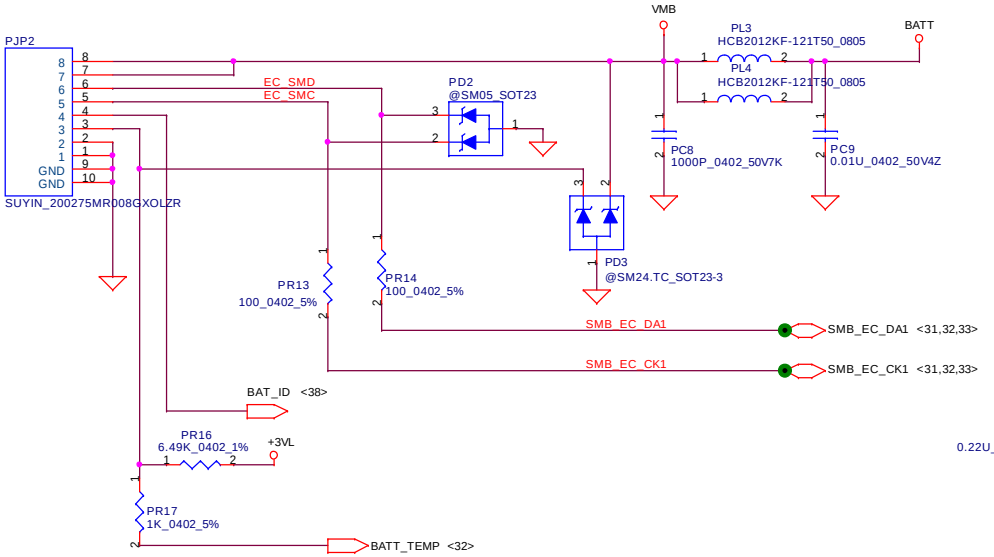
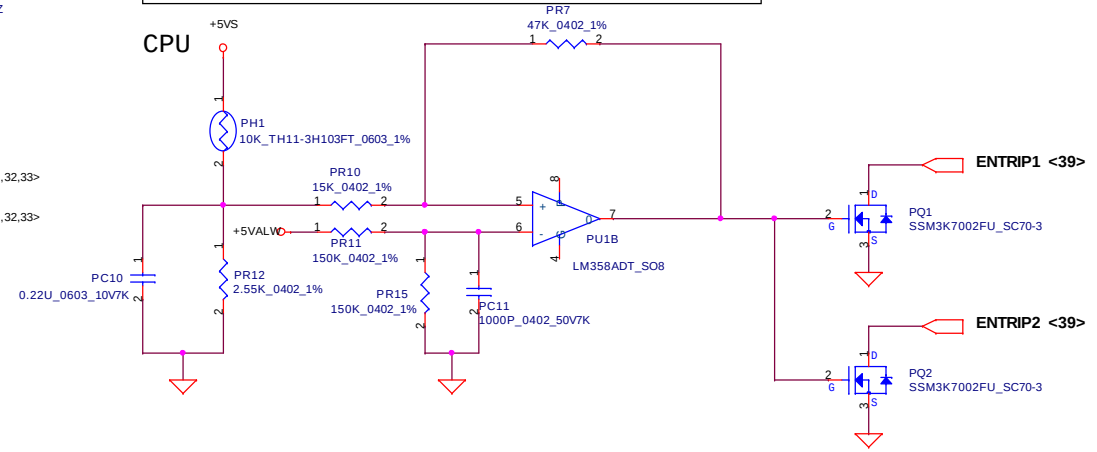
Compal Electronics, Inc.			
Title	DC/DC Interface		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 36 of 46		







PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



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Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

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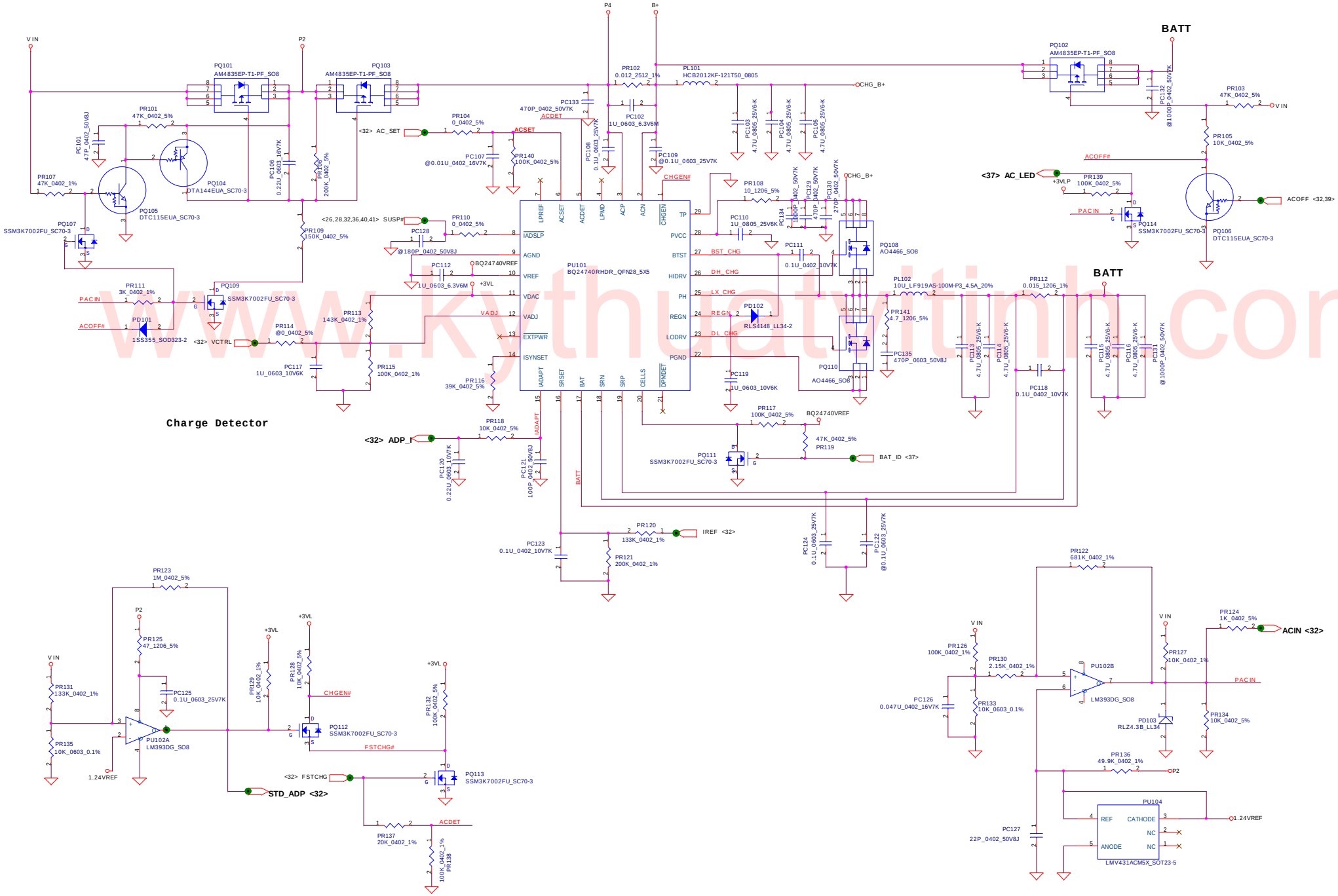

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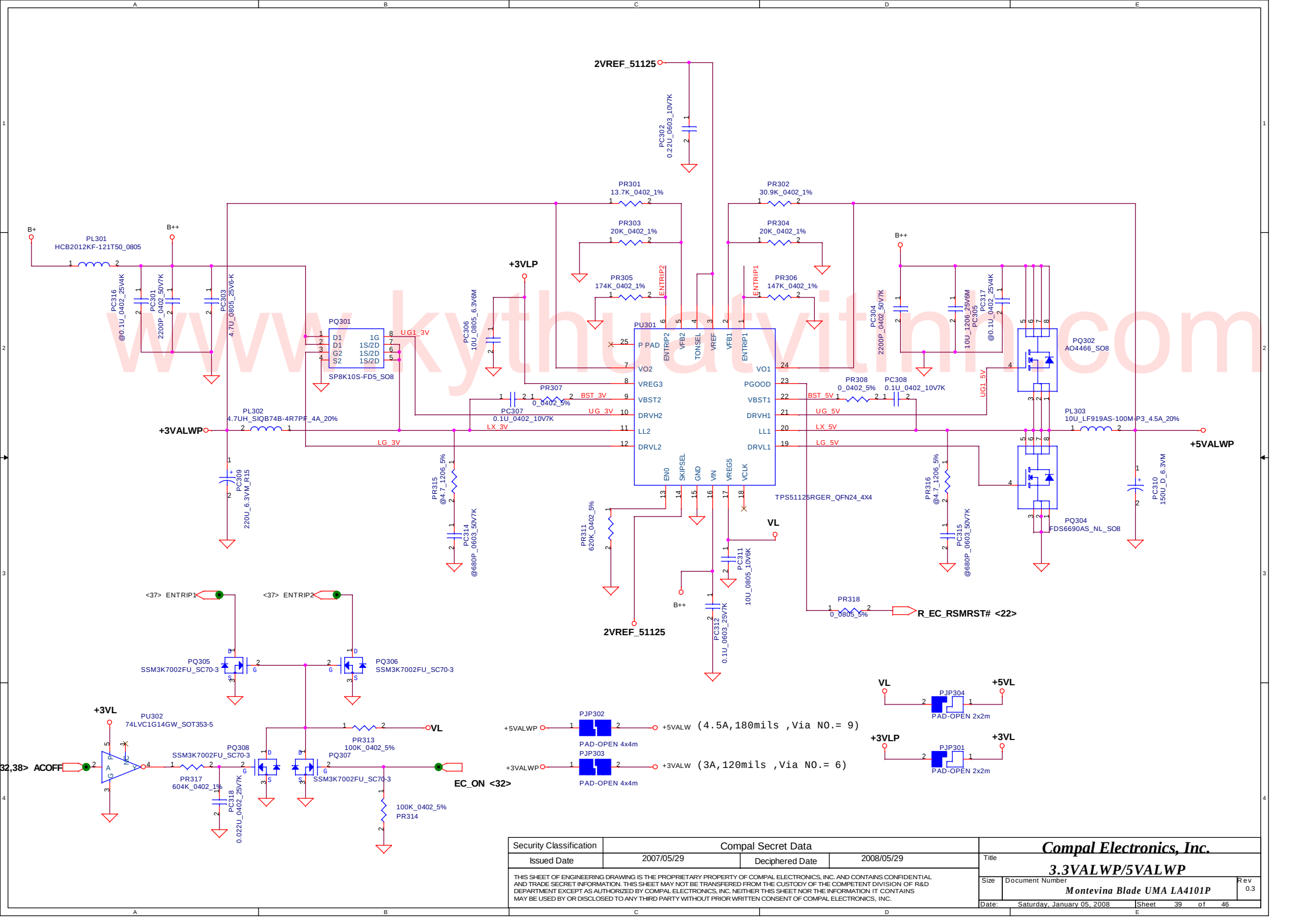
Compal Electronics, Inc.			
Title: Charger			
Size	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 38 of 46		



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Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

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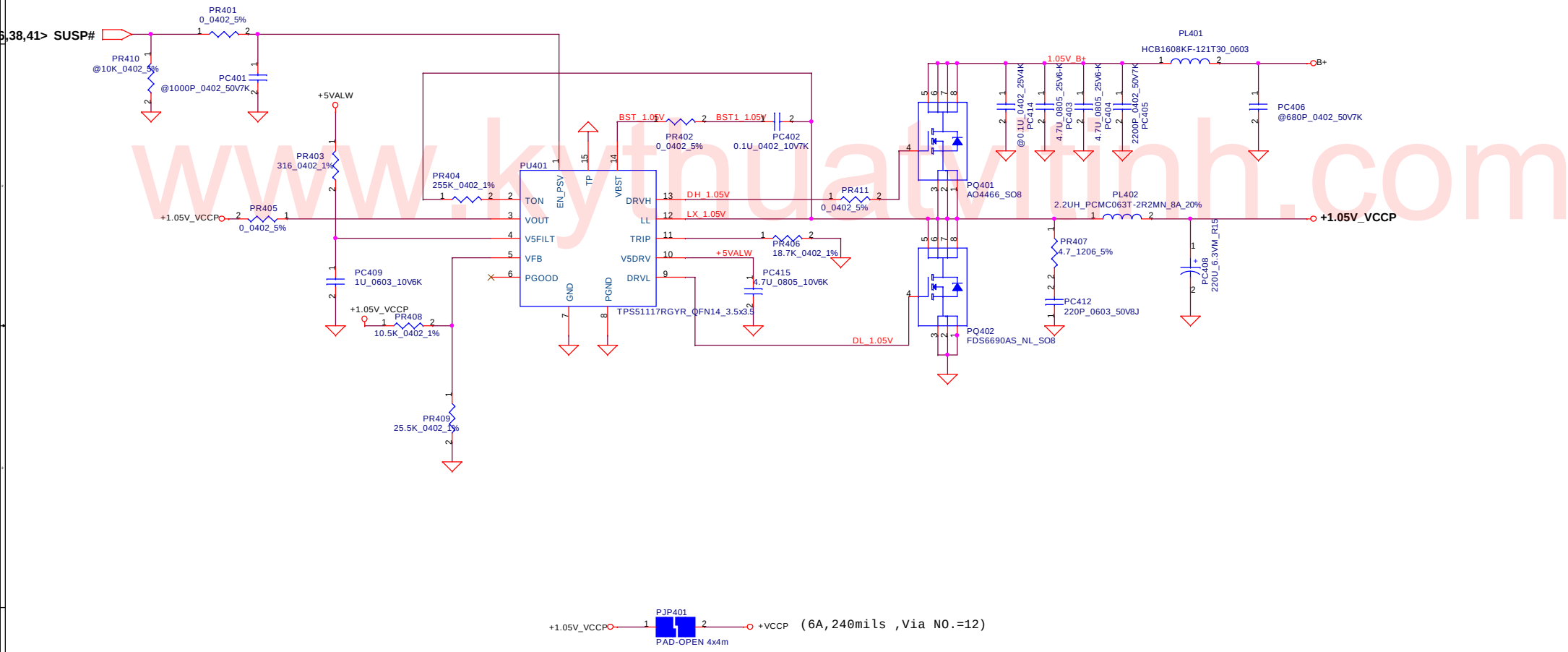

+1.05V_VCCP — PJP401 — +VCCP (6A,240mils ,Via NO.=12)

PAD-OPEN 4x4m

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Compal Electronics, Inc.

Title: **1.05V_VCCP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

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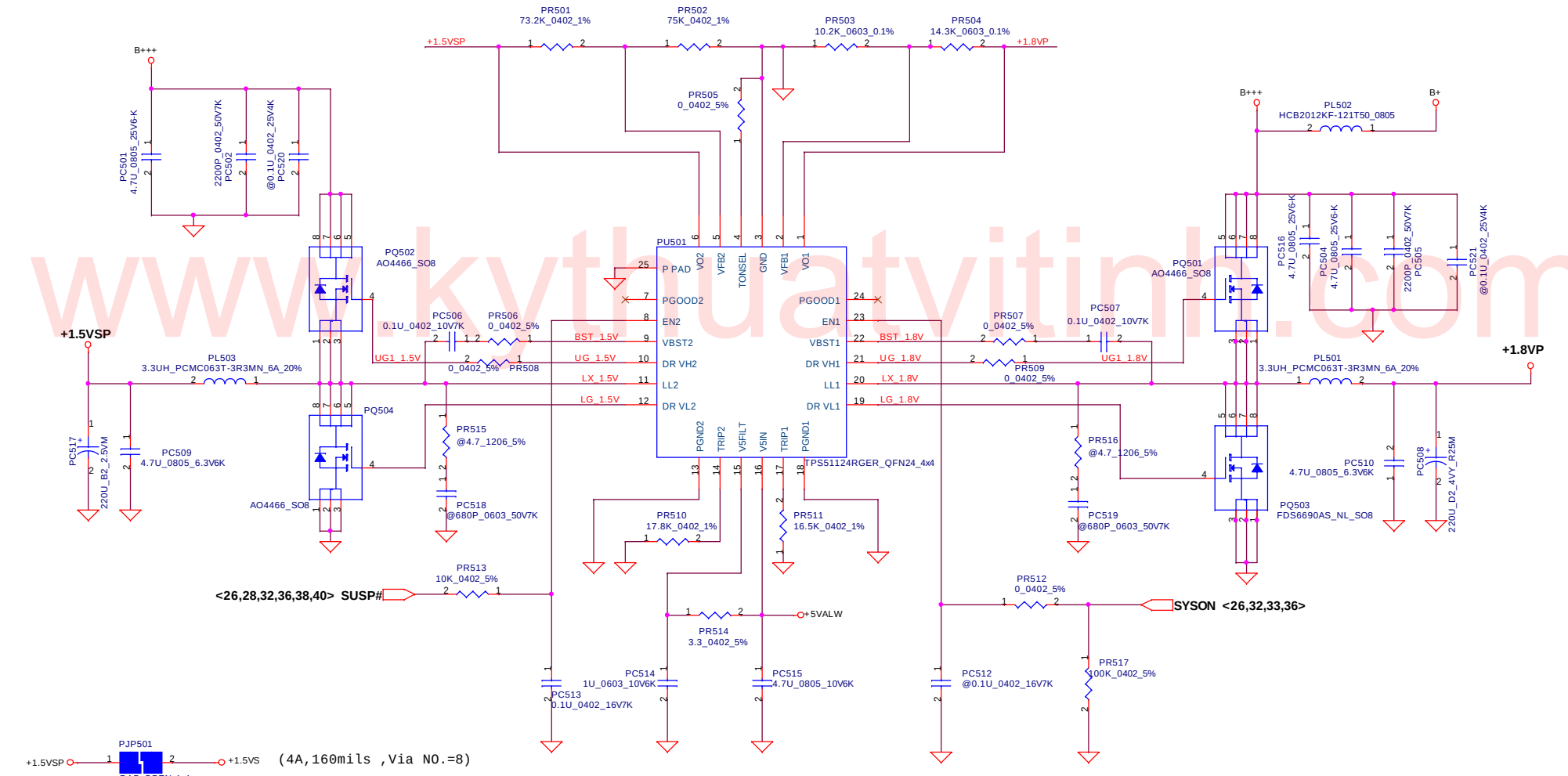

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Compal Electronics, Inc.

Title: **1.5VSP/1.8VP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

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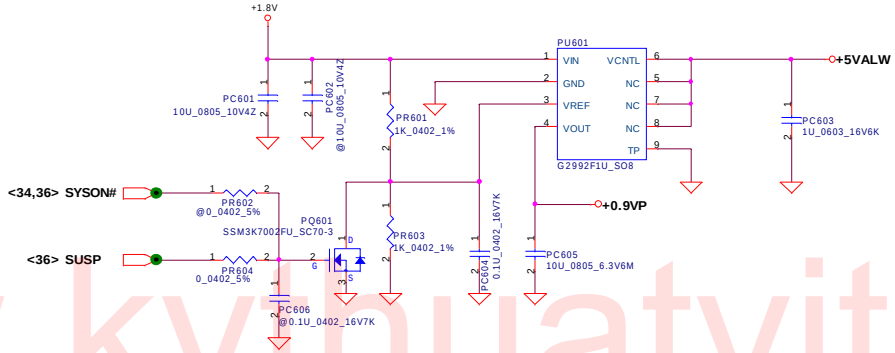

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(2A,80mils ,Via NO.= 4)

Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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Compal Electronics, Inc.

Title: **0.9VP/1.1V_PCIE**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

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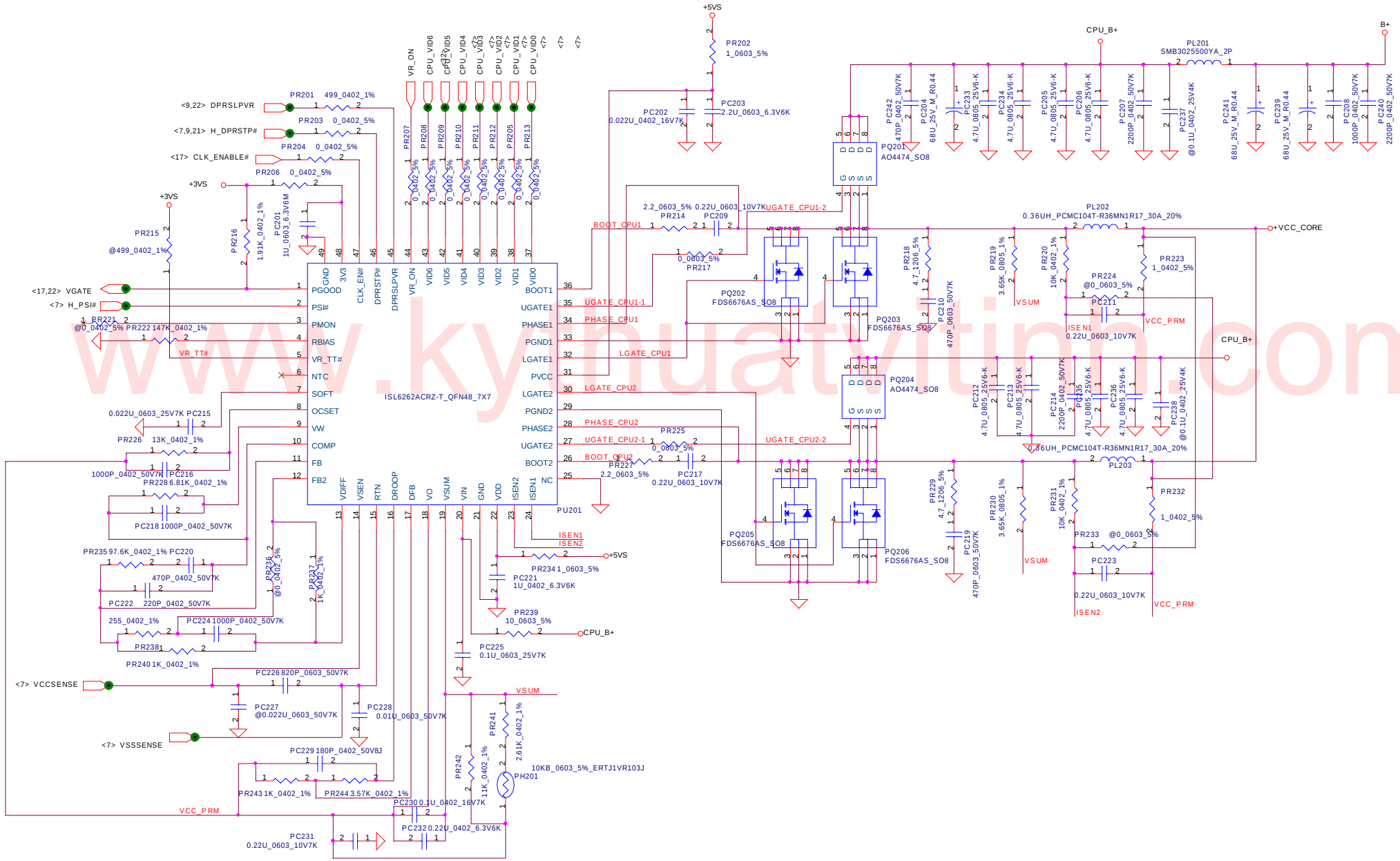

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Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.3

Date: Saturday, January 05, 2008 | Sheet 43 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K，R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#，GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285~C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295□BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction pretect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC_recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC _EN must enable 、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOUT and HDA_SDOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Compal Electronics, Inc.
Title: PIR
Size: Document Number: Montevina Blade UMA LA4101P Rev: 0.3
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
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