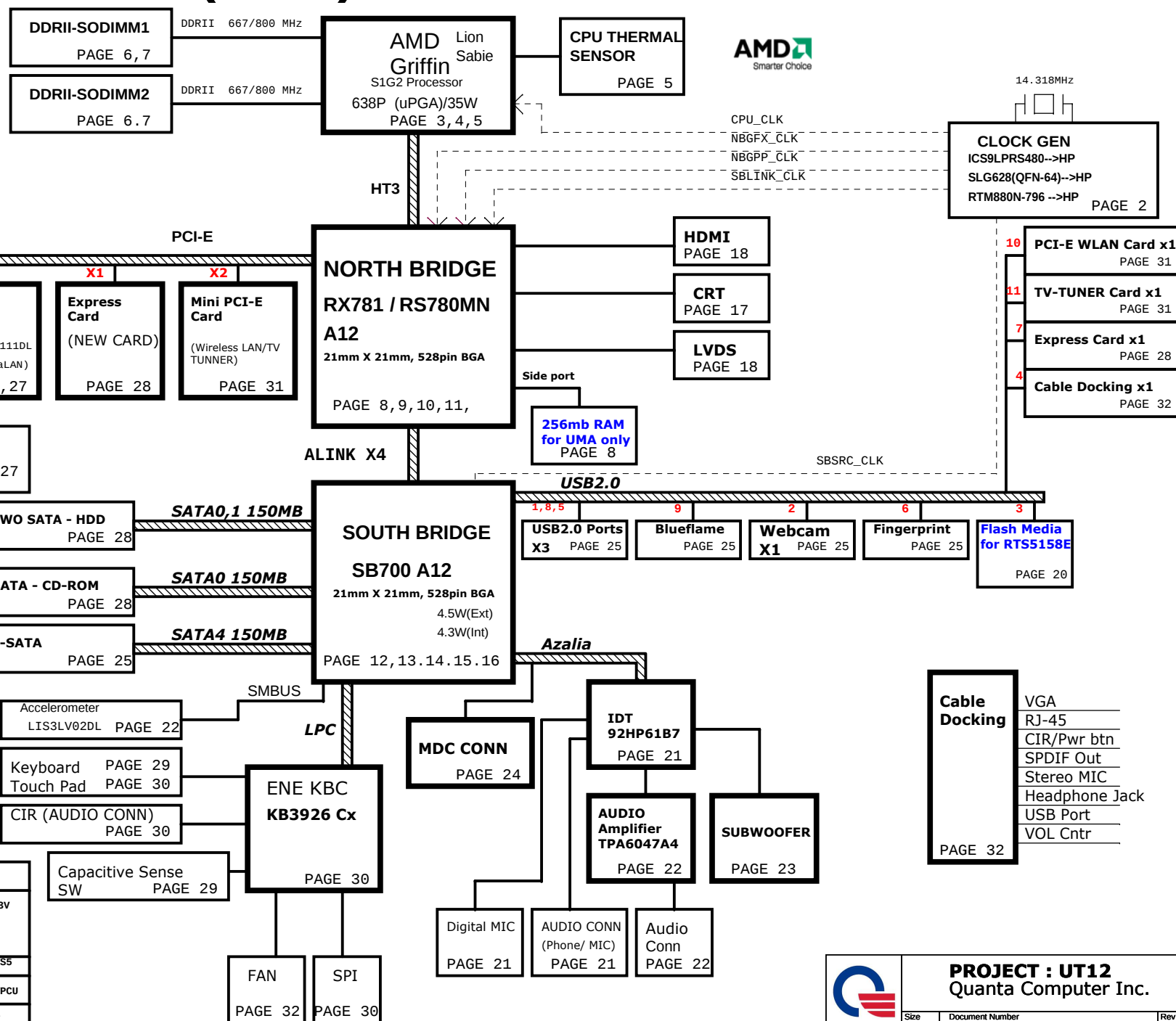


UT12(UMA) SYSTEM DIAGRAM

01

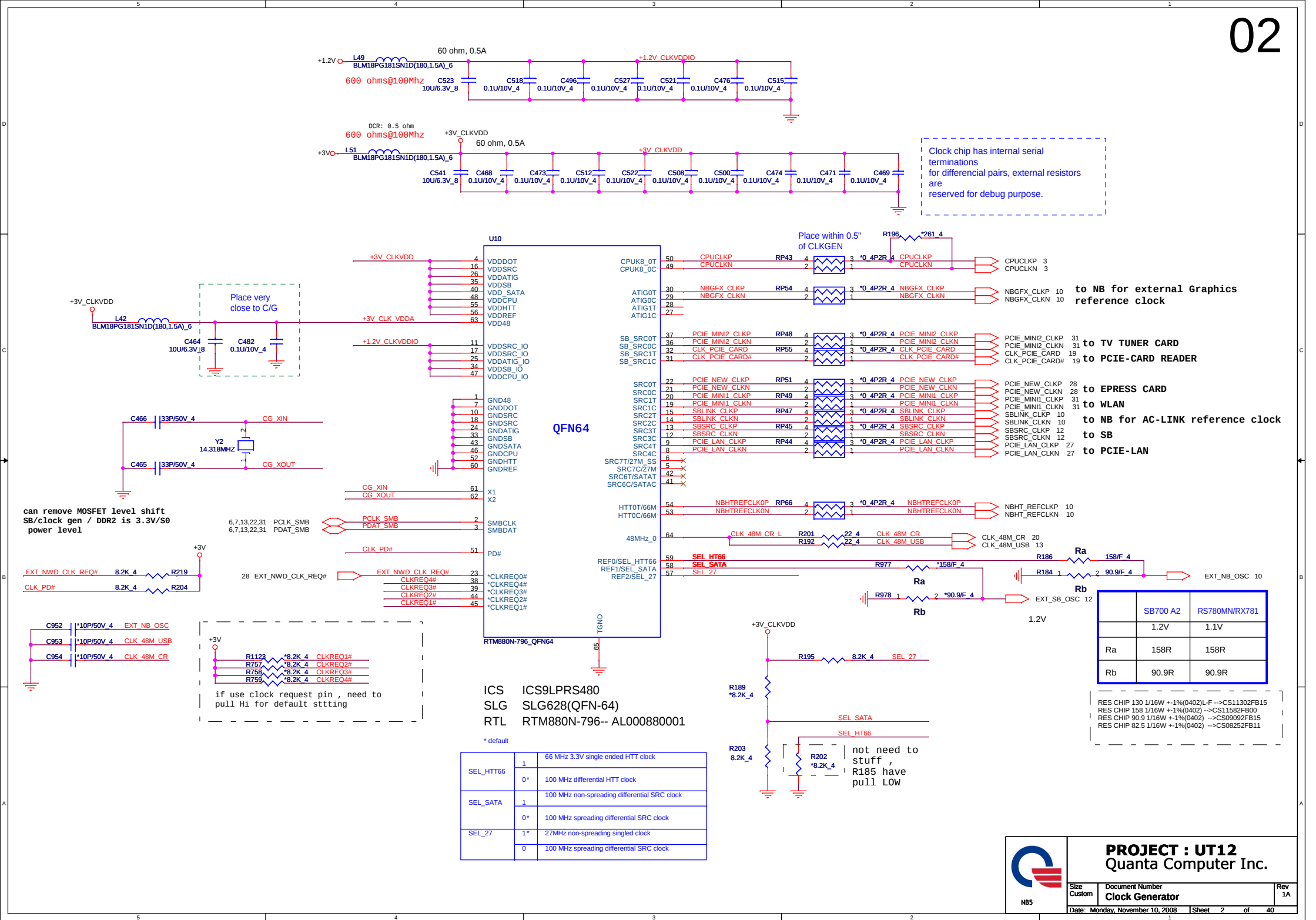
PCB STACK UP

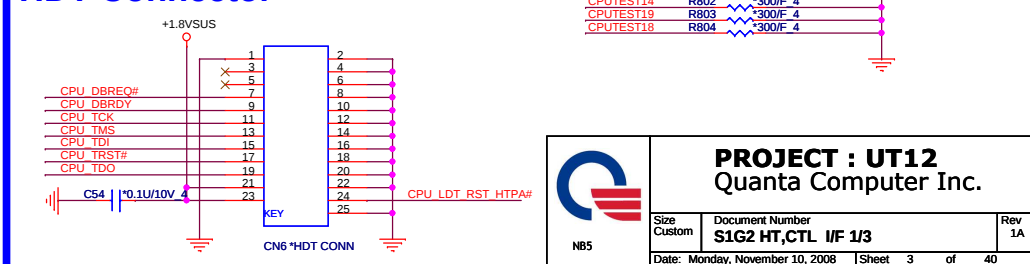
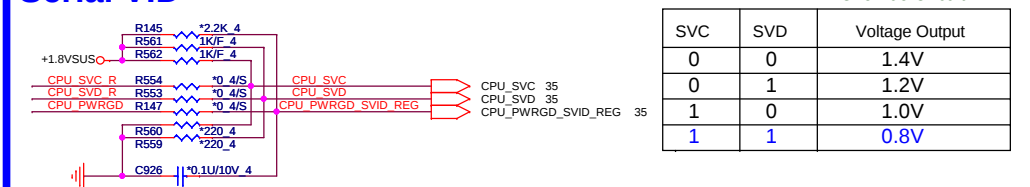
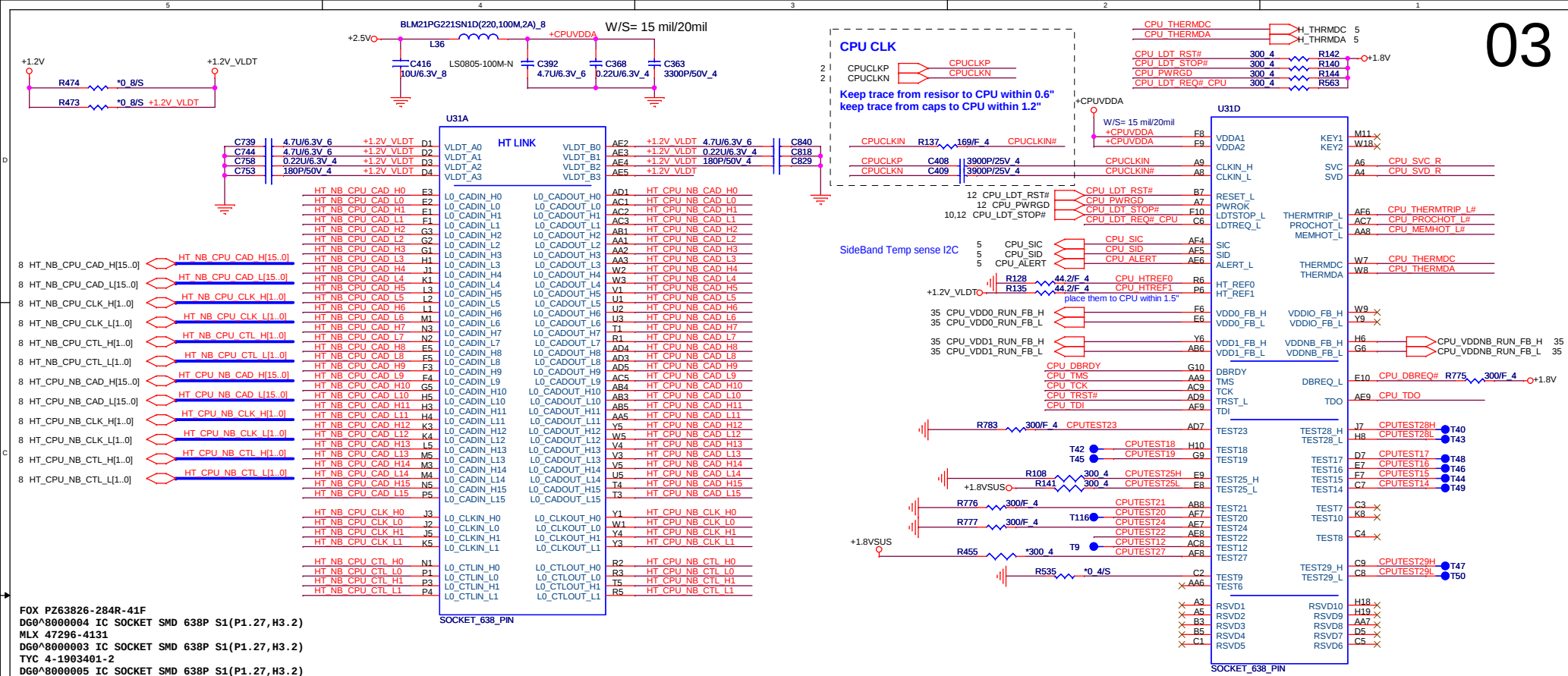
LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT



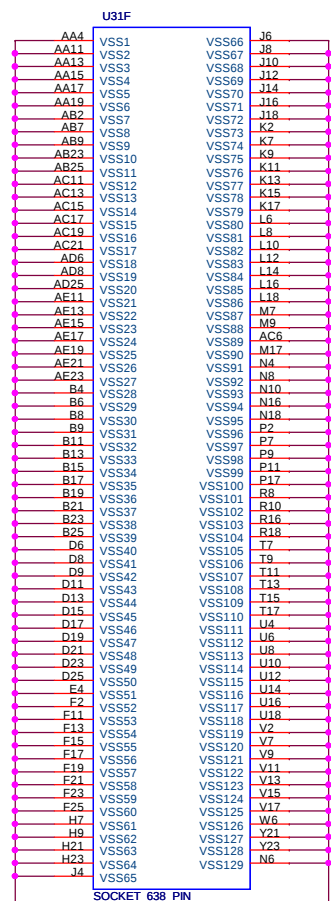
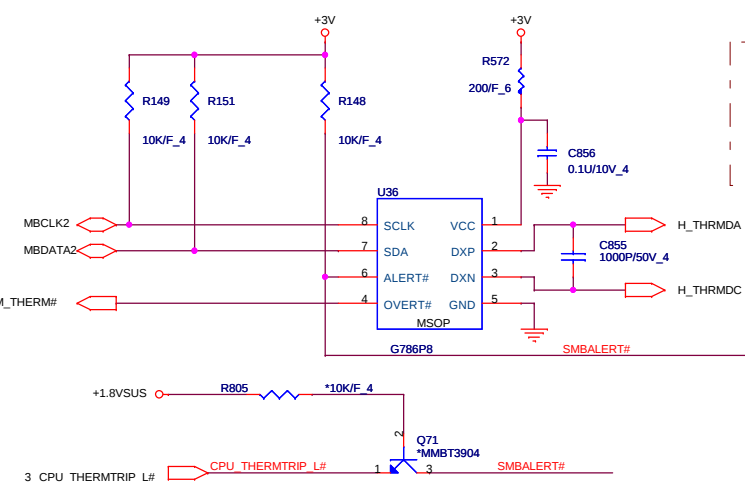
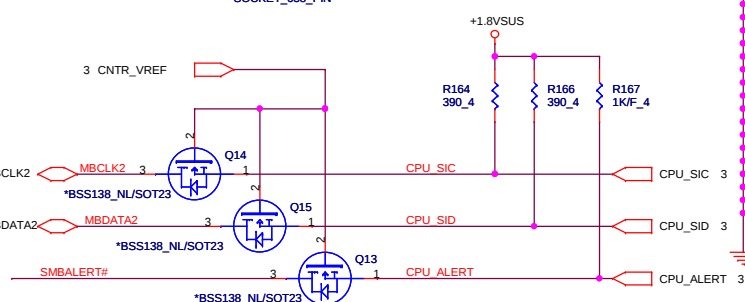
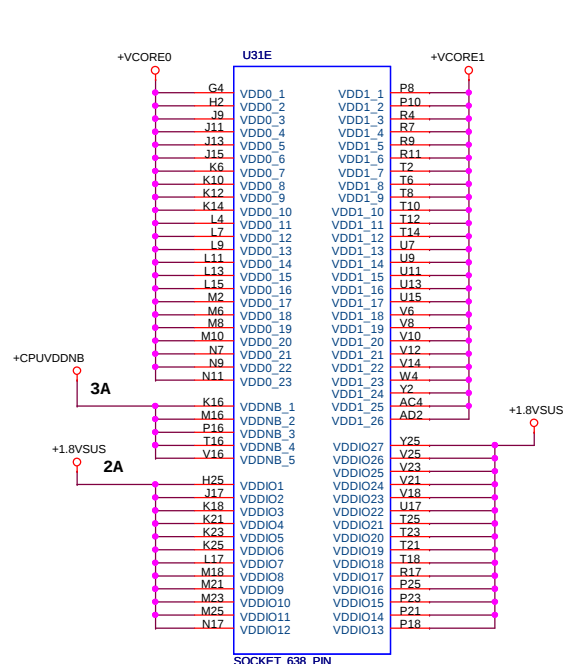
PROJECT : UT12
Quanta Computer Inc.

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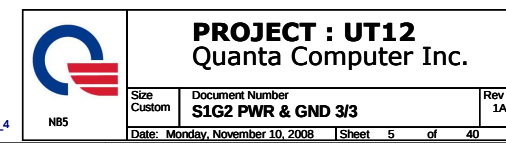
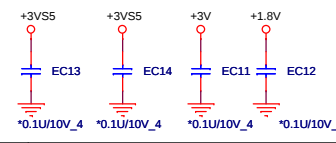
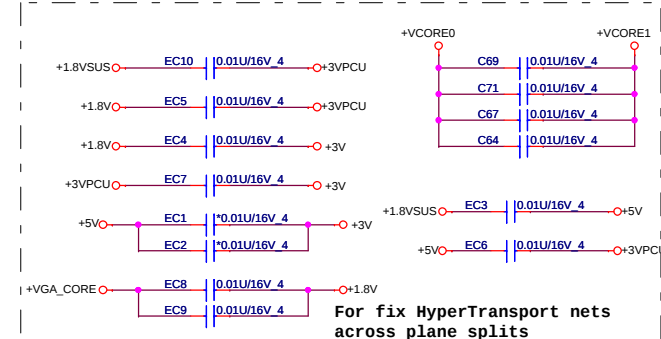
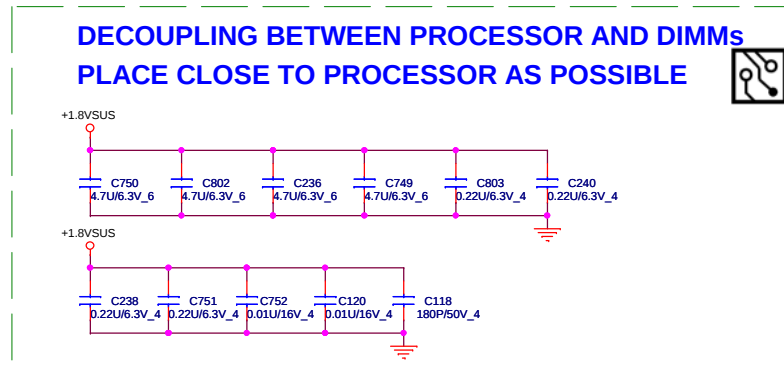
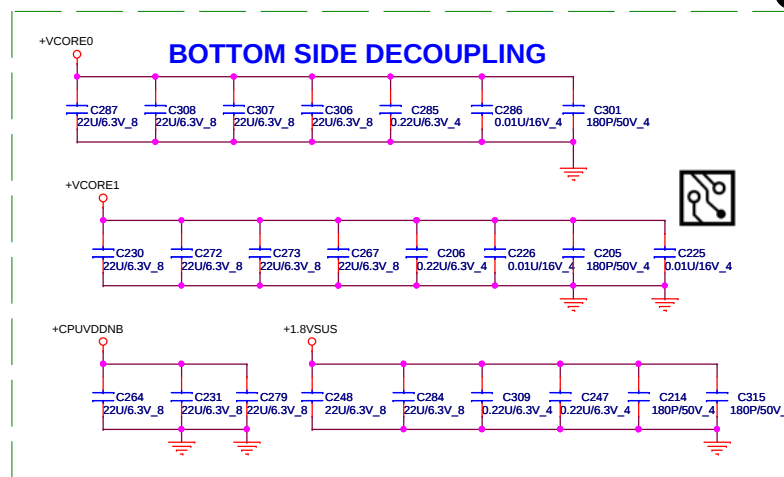
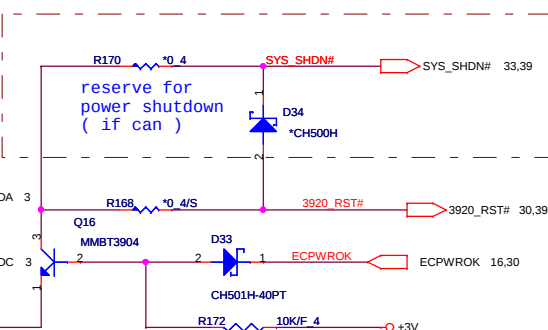


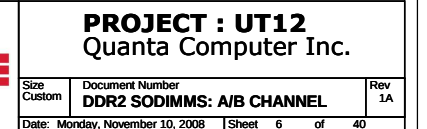


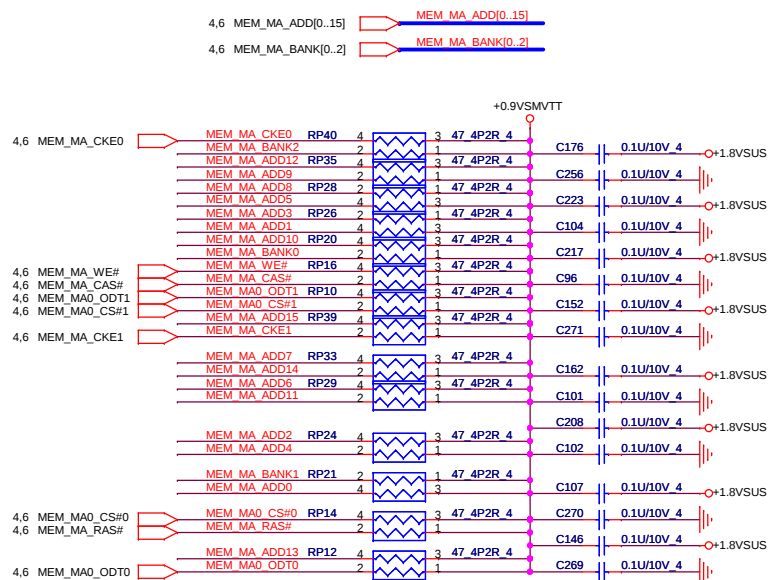




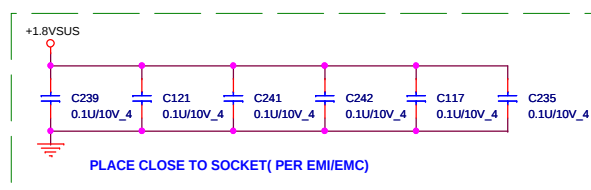
PROCESSOR POWER AND GROUND



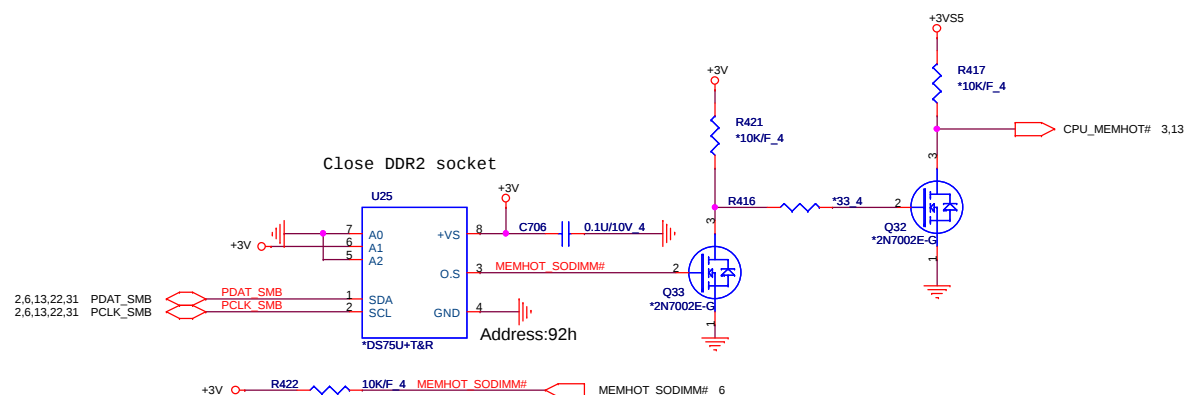
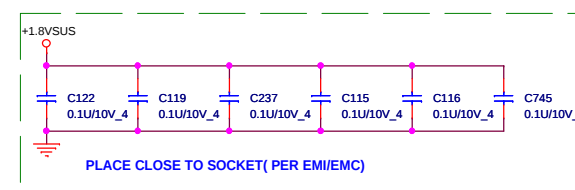


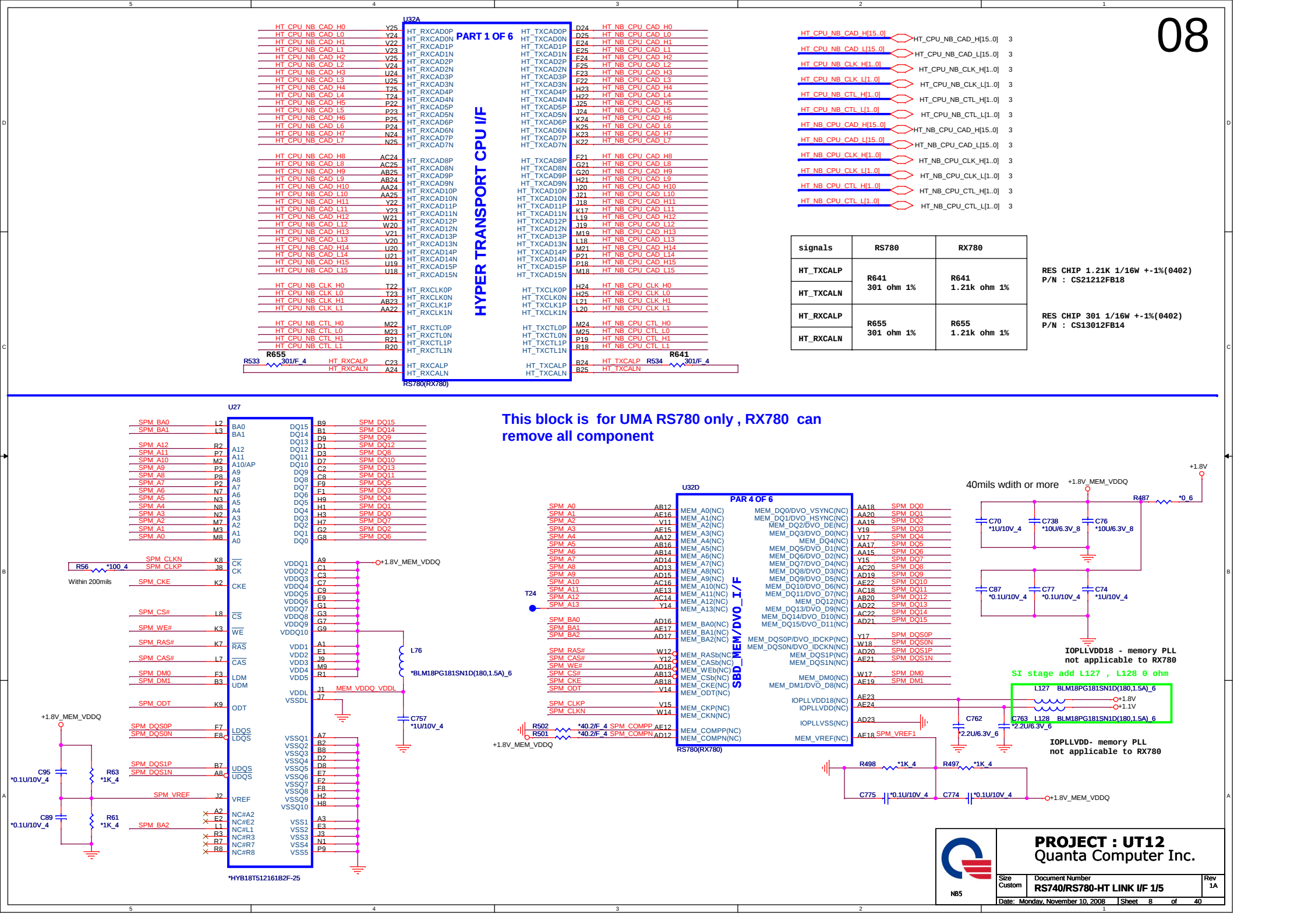


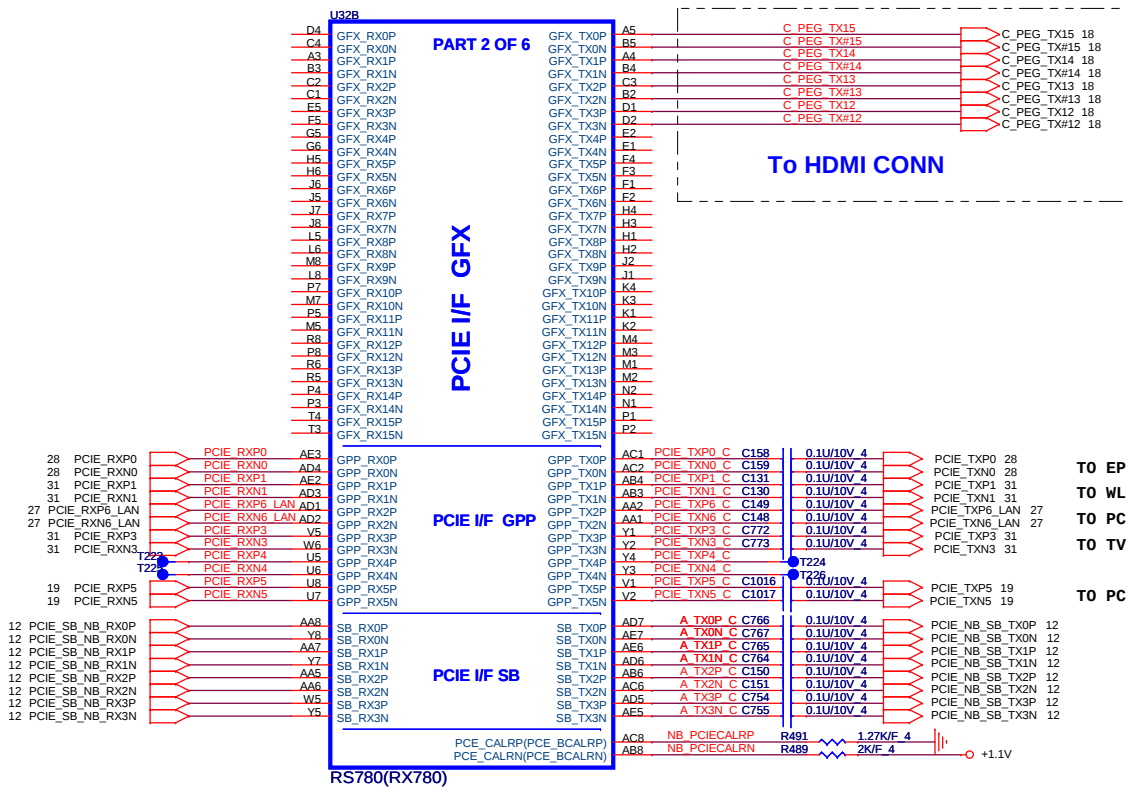
**PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH**



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH







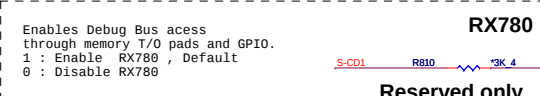
PROJECT : UT12
Quanta Computer Inc.

Size
Custom

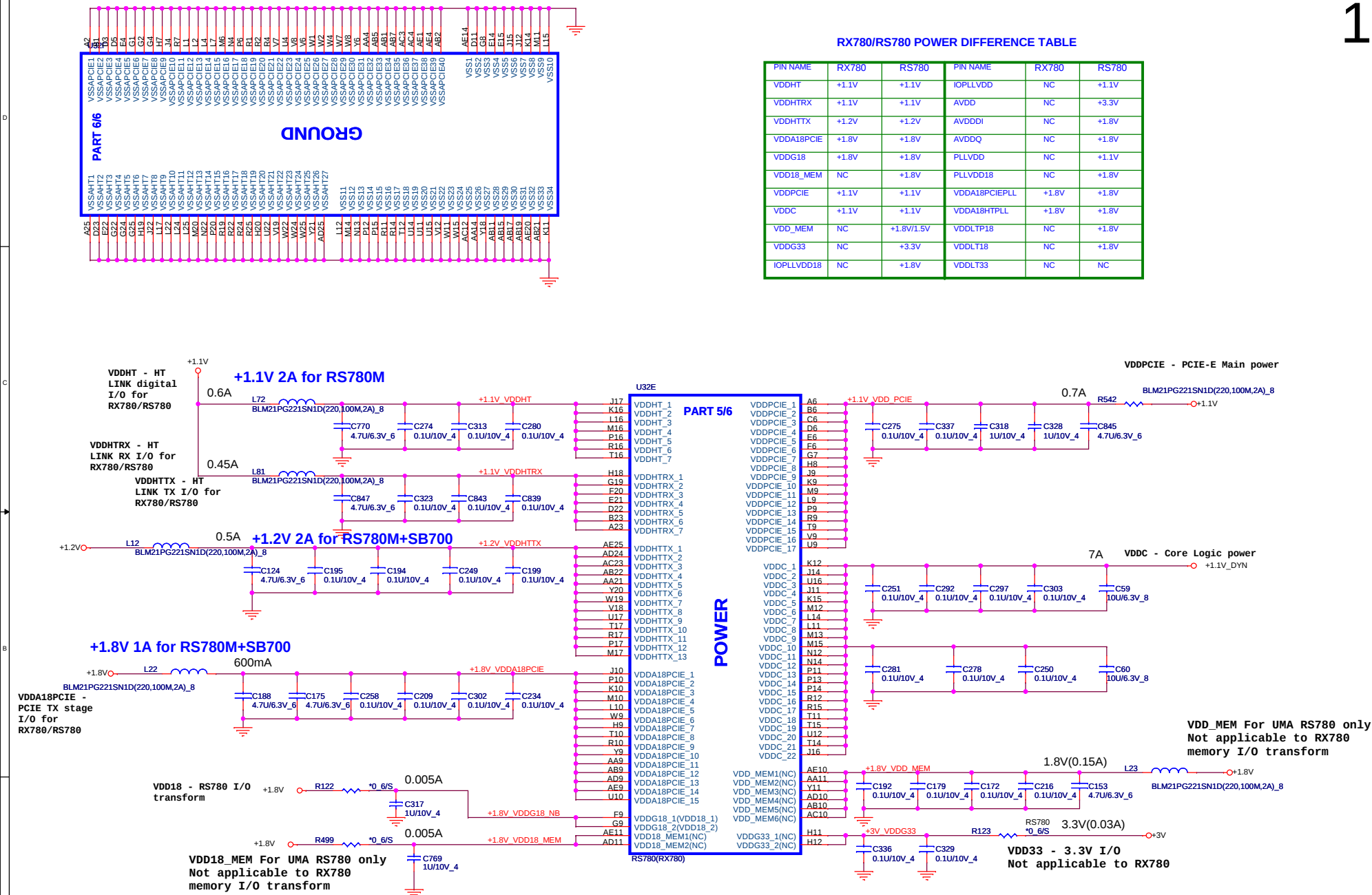
Document Number
RS740/RS780-PCIE I/F 2/5

Rev
1A

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PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTPI8	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLT33	NC	NC





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SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

SATA HDD2

SATA PORT 4,5
are only
support IDE
mode

PLVDD_SATA - -
SATA PLL
POWER

NOTE:

R361 IS 1K 1% FOR 25MHZ
XTAL, 4.99K 1% FOR 100MHZ
INTERNAL CLOCK

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

SI stage remove C548 , C551

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no supprot side port

ID3	ID2	ID1	ID0	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96
0	1	1	0	
0	1	1	1	



Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
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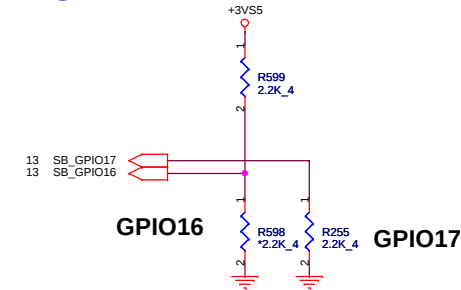
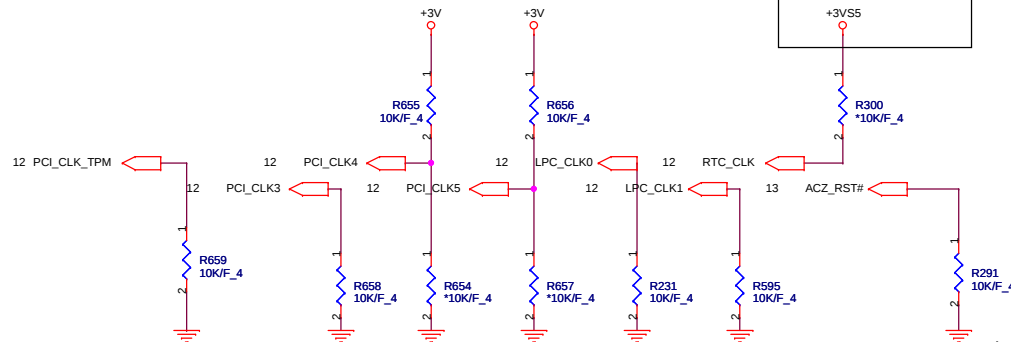


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

16

It must ready
before RSMRST#

REQUIRED STRAPS

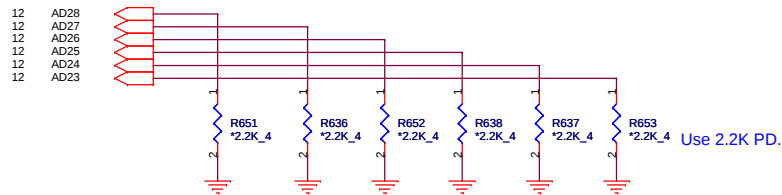


GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

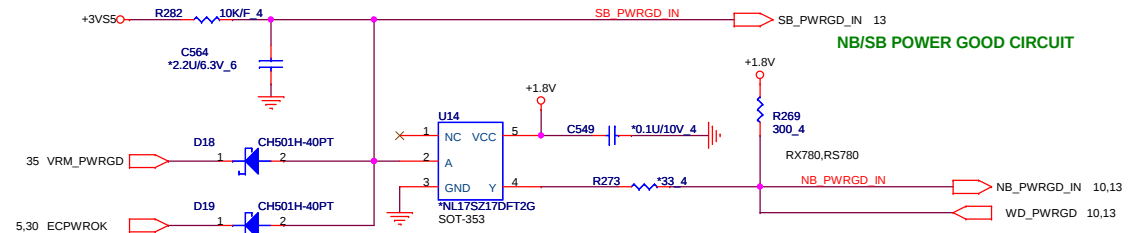
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

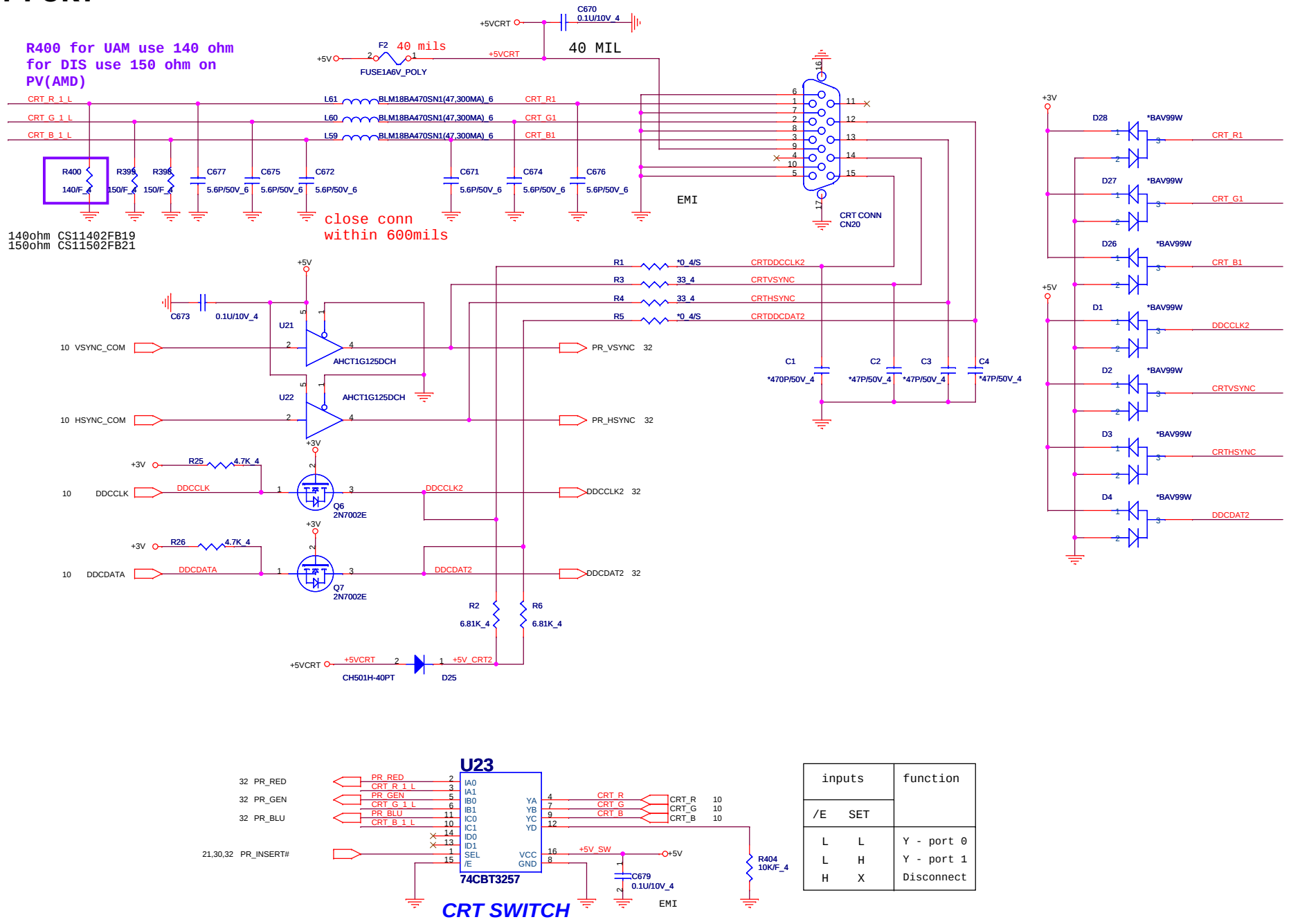


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SB700-STRAPS Rev 1A
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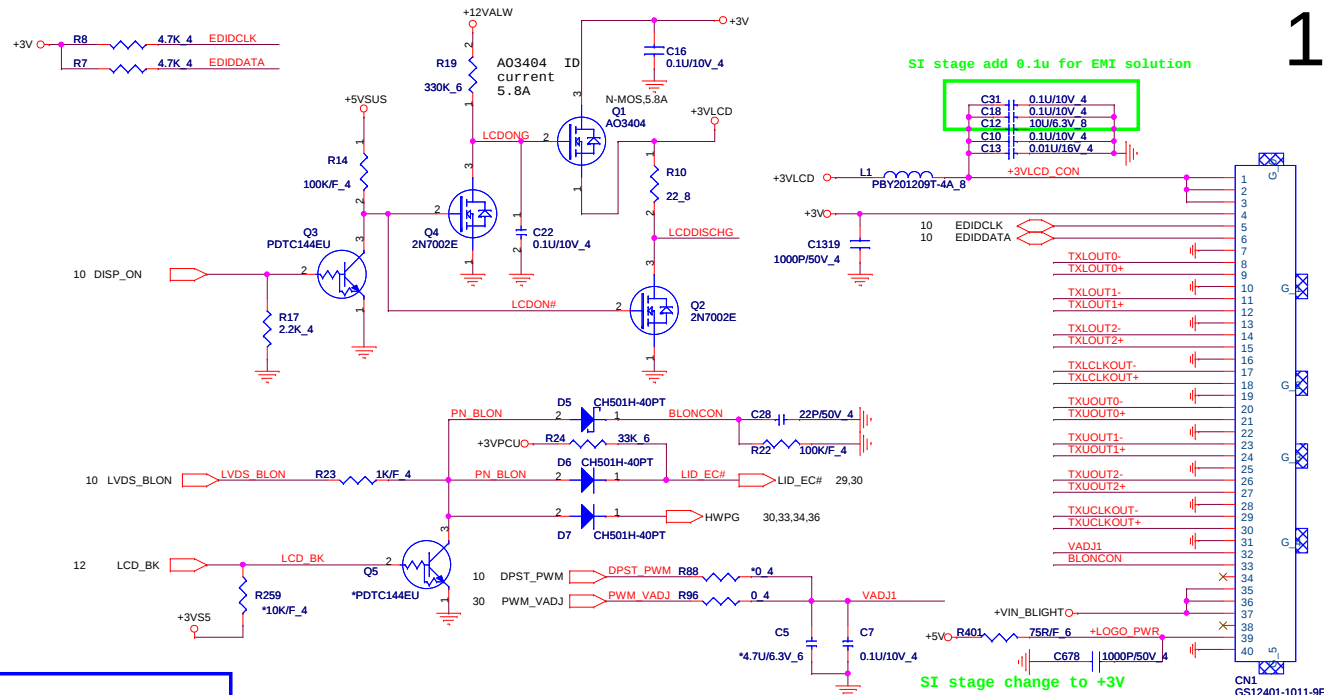
CRT PORT

R400 for UAM use 140 ohm
for DIS use 150 ohm on
PV(AMD)

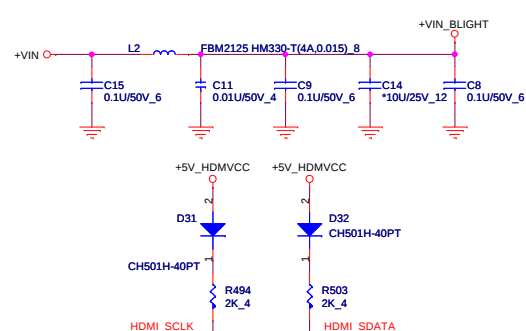
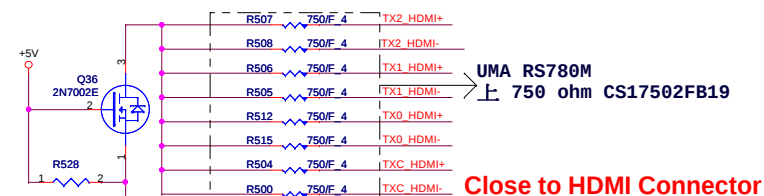
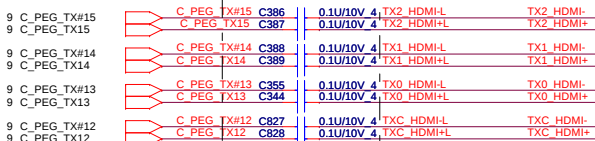


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

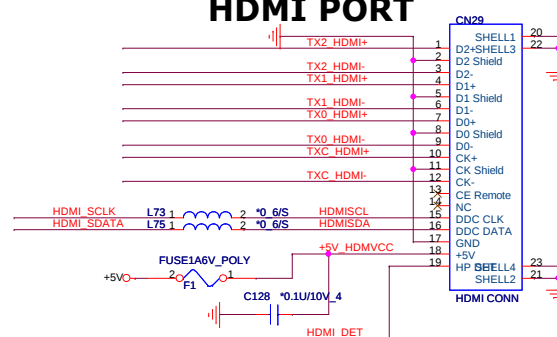
10	LA_CLK#	LA_CLK	TXCLKOUT+
10	LA_CLK#	LA_CLK#	TXCLKOUT-
10	LA_DATAP0	LA_DATAP0	TXL0UT0+
10	LA_DATAN0	LA_DATAN0	TXL0UT0-
10	LA_DATAP1	LA_DATAP1	TXL0UT1+
10	LA_DATAN1	LA_DATAN1	TXL0UT1-
10	LA_DATAP2	LA_DATAP2	TXL0UT2+
10	LA_DATAN2	LA_DATAN2	TXL0UT2-
10	LB_CLK	LB_CLK	TXUCLKOUT+
10	LB_CLK#	LB_CLK#	TXUCLKOUT-
10	LB_DATAP0	LB_DATAP0	TXU0UT0+
10	LB_DATAN0	LB_DATAN0	TXU0UT0-
10	LB_DATAP1	LB_DATAP1	TXU0UT1+
10	LB_DATAN1	LB_DATAN1	TXU0UT1-
10	LB_DATAP2	LB_DATAP2	TXU0UT2+
10	LB_DATAN2	LB_DATAN2	TXU0UT2-



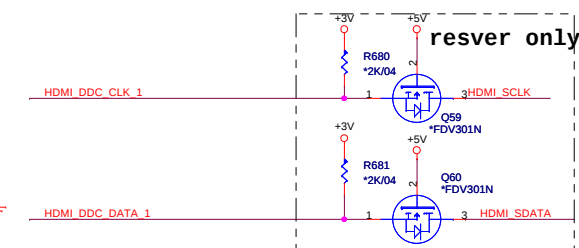
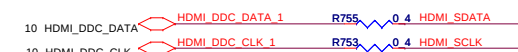
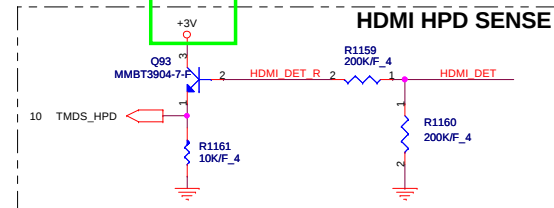
for Layout -
concern
placement close
north bridge

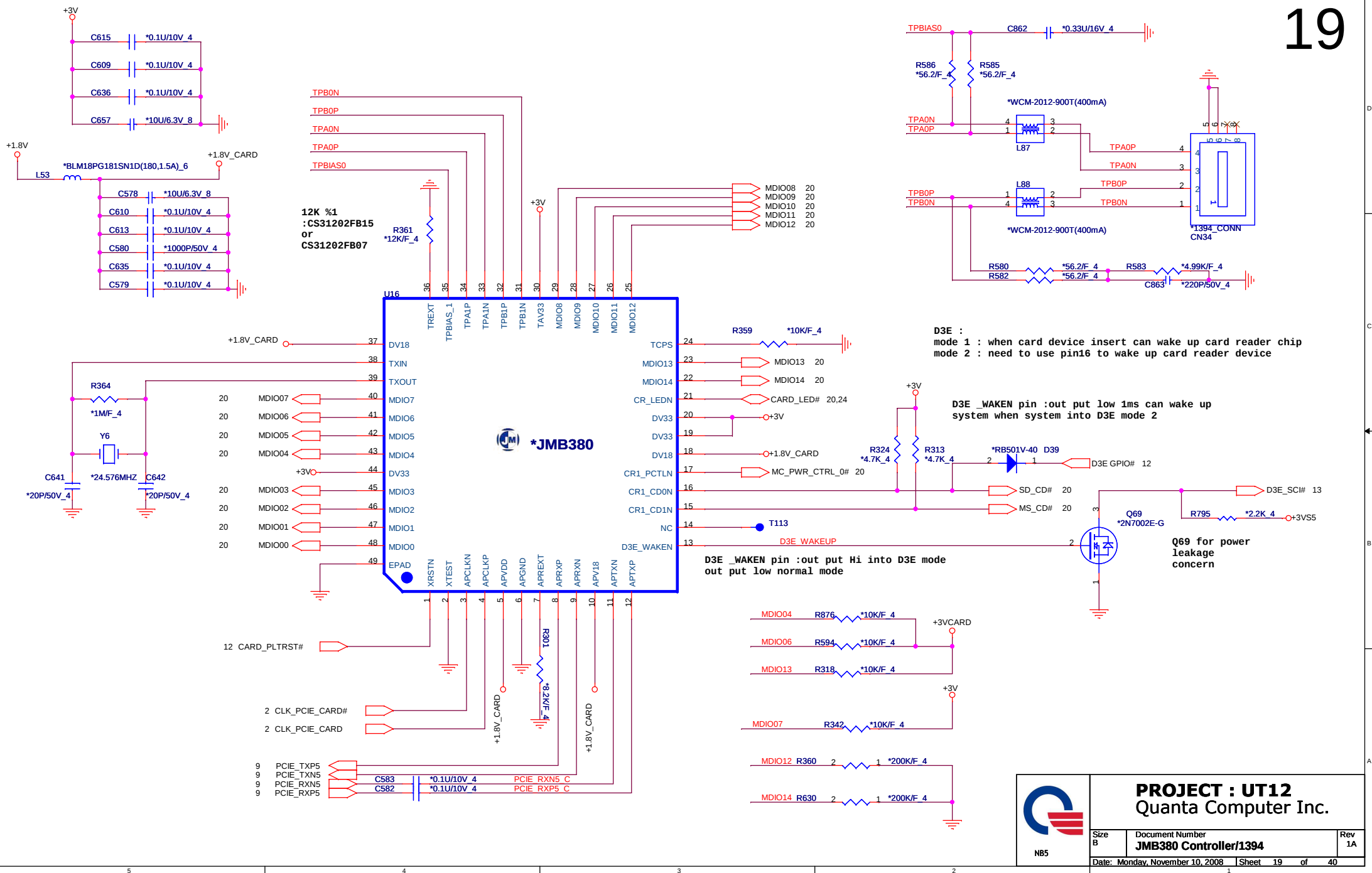


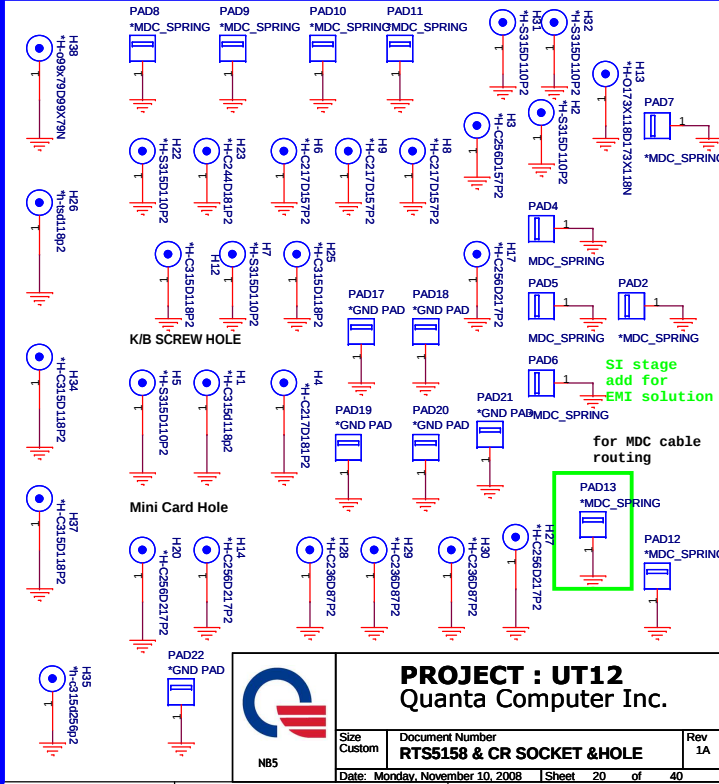
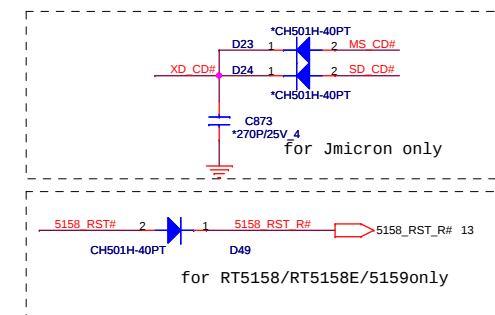
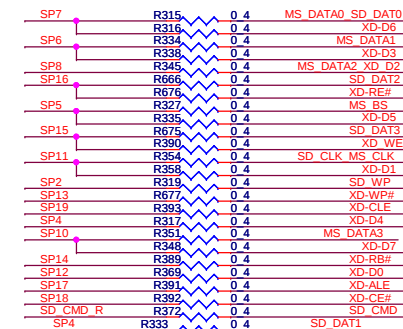
HDMI PORT

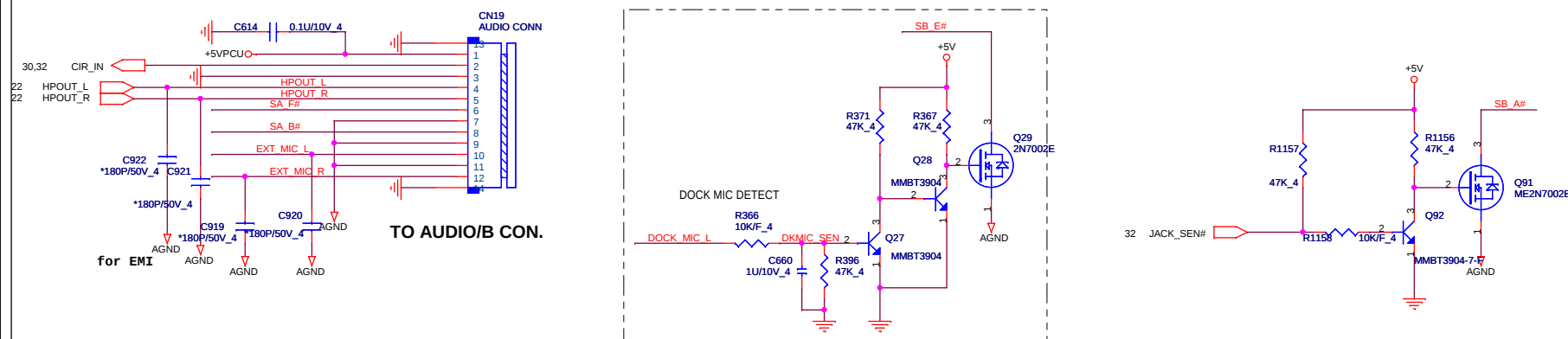
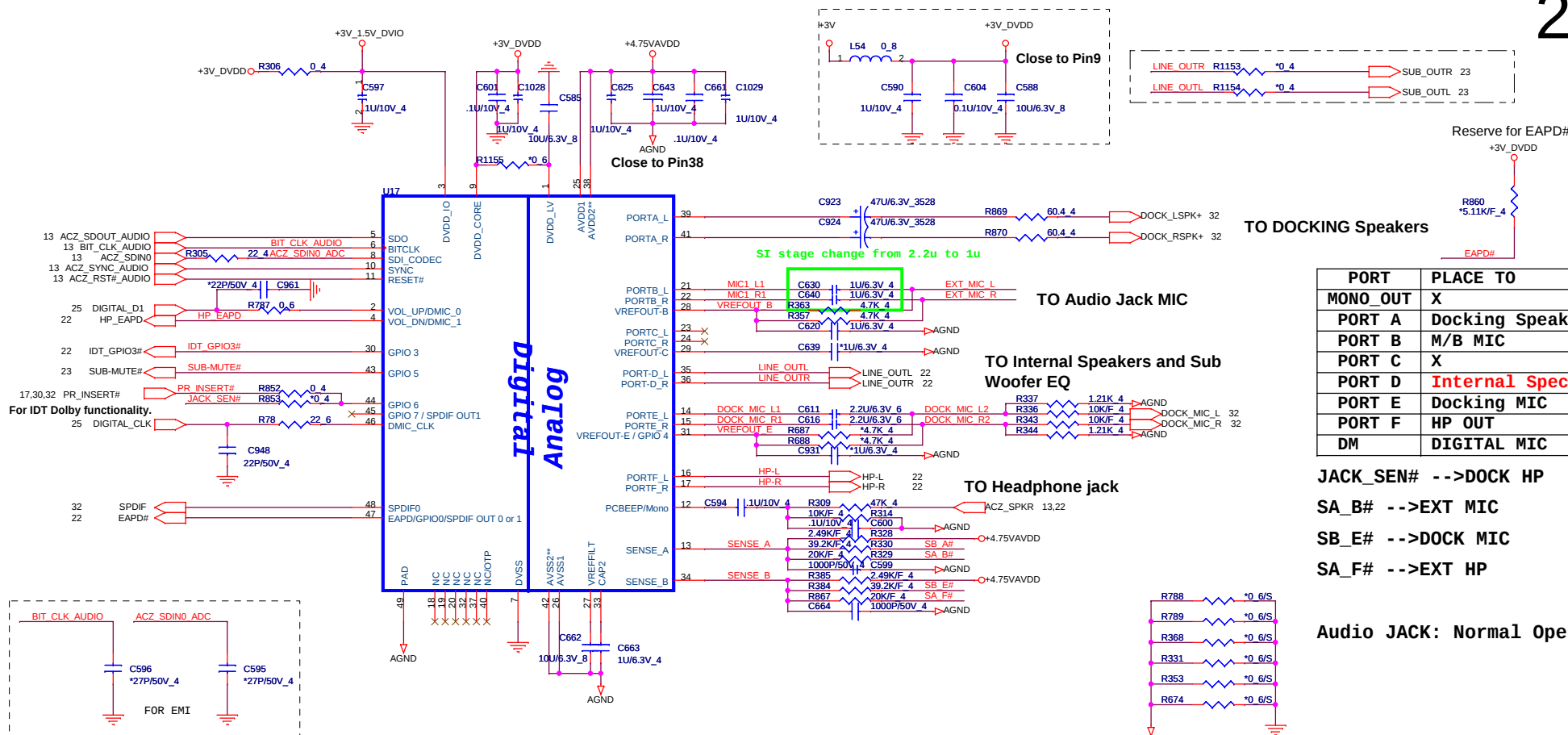


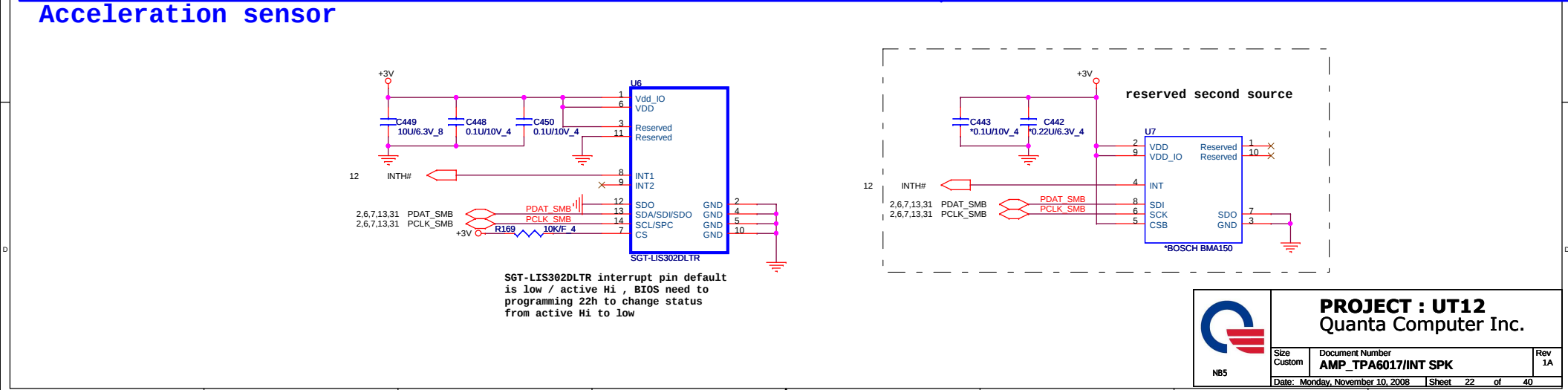
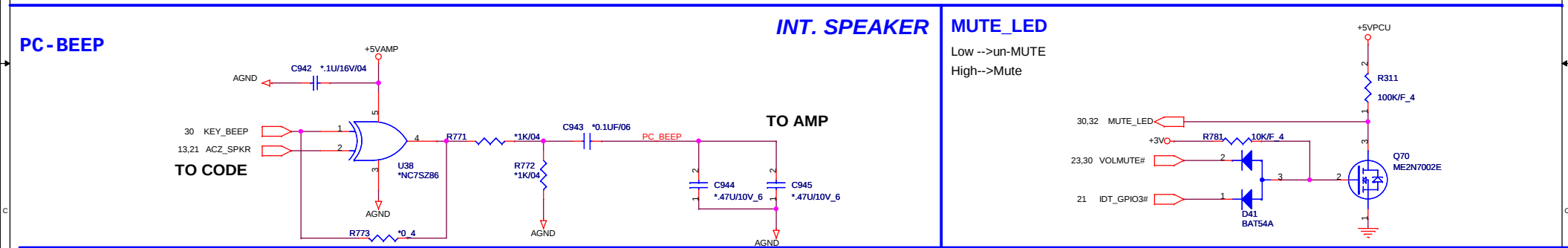
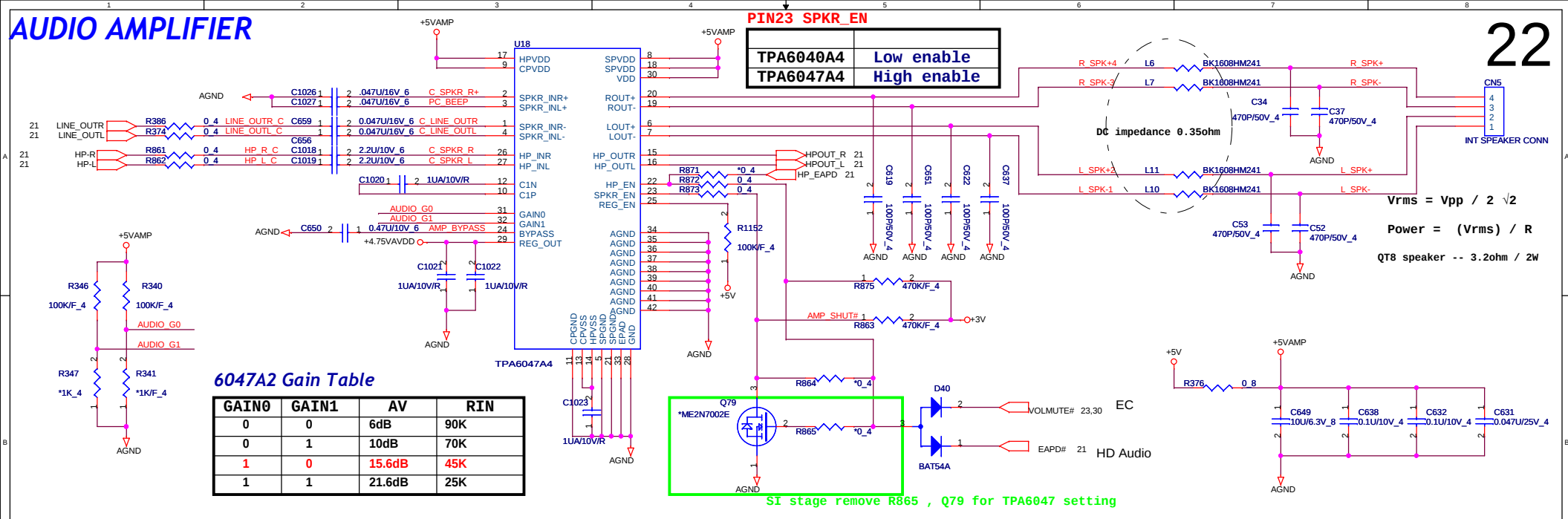
HDMI HPD SENSE





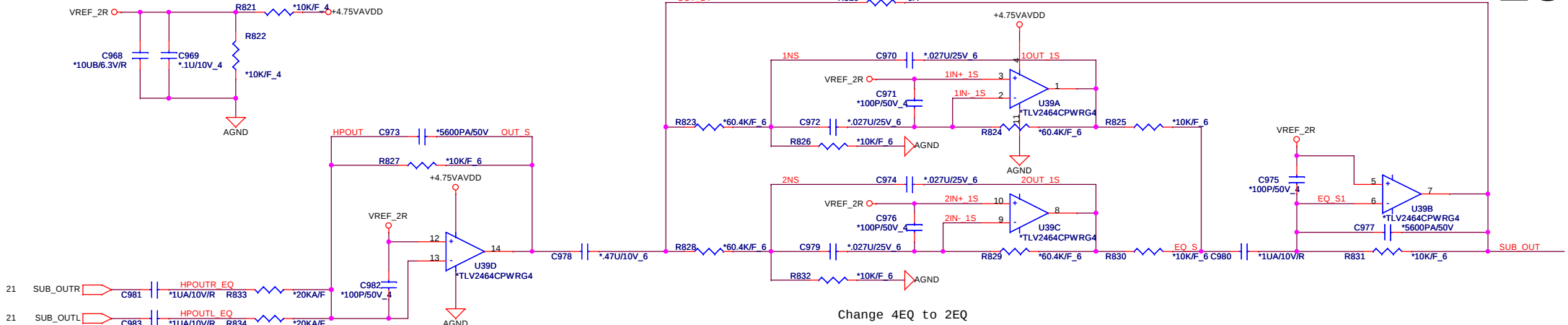




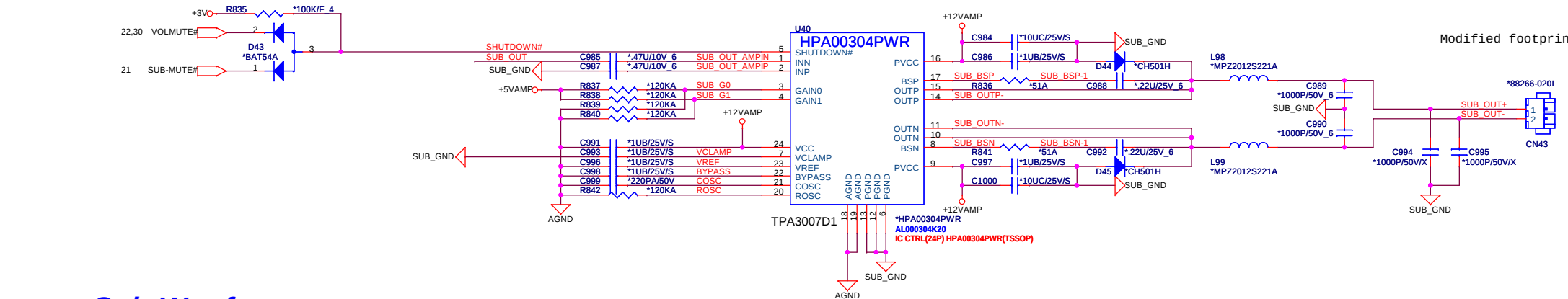


EQ FOR SUBWOOFER

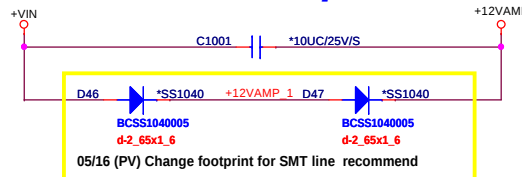
23



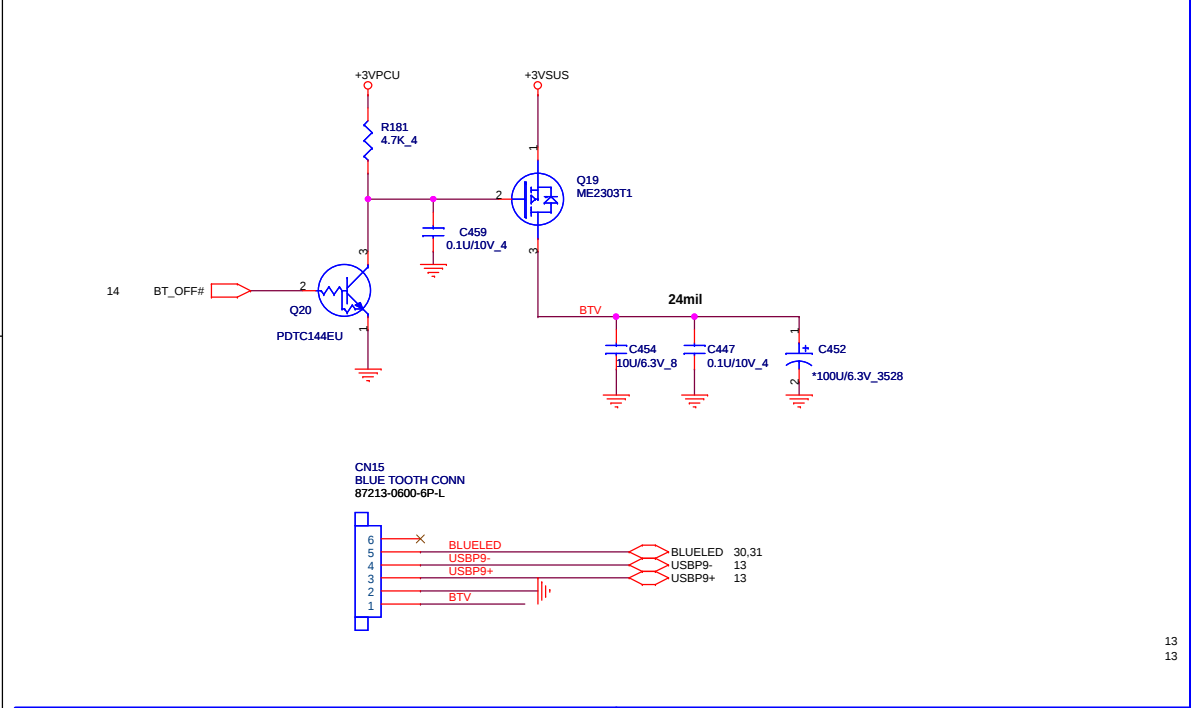
MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C976	0.027U/25V_6	0.039U/16V_6



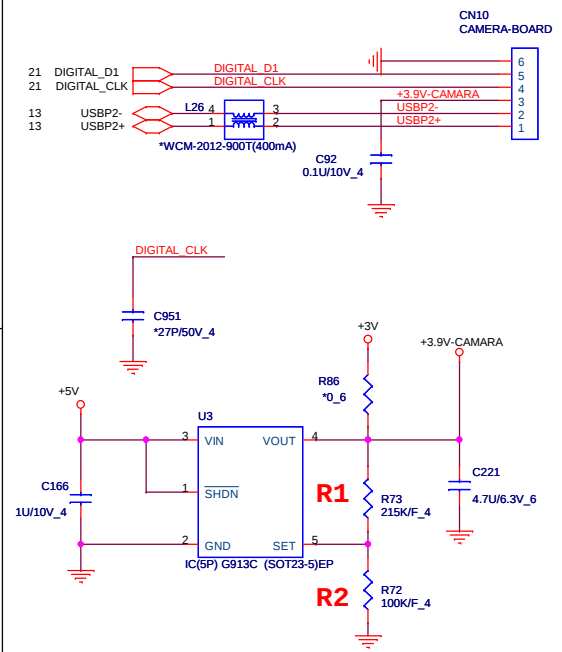
Sub-Woofer power



BLUETOOTH

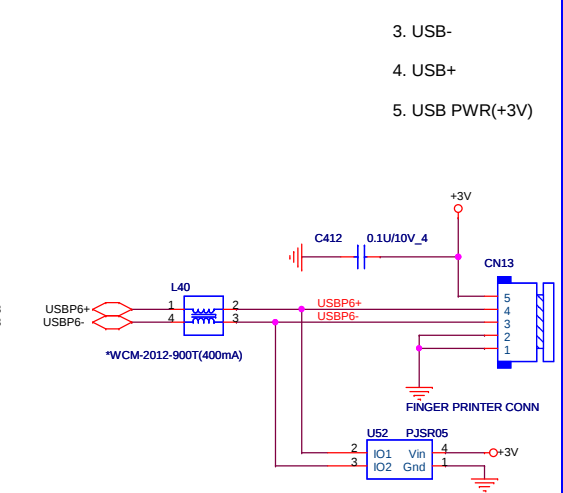


USB CAMERA CONNECT

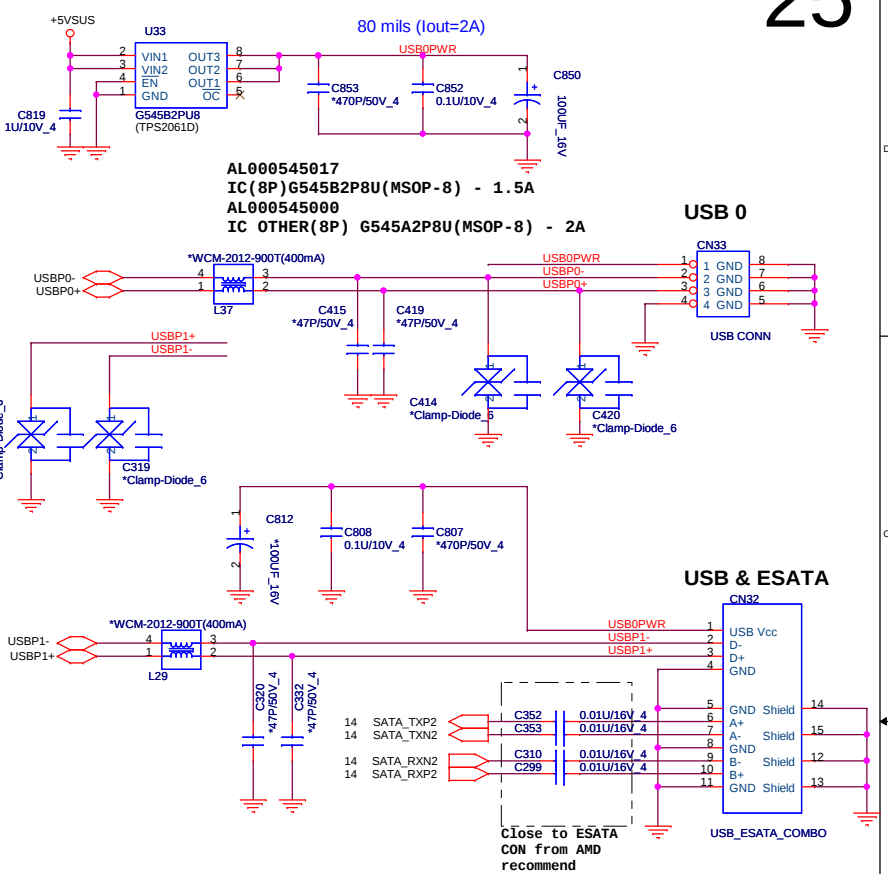


$$V_{out} = 1.25(1 + R1/R2)$$

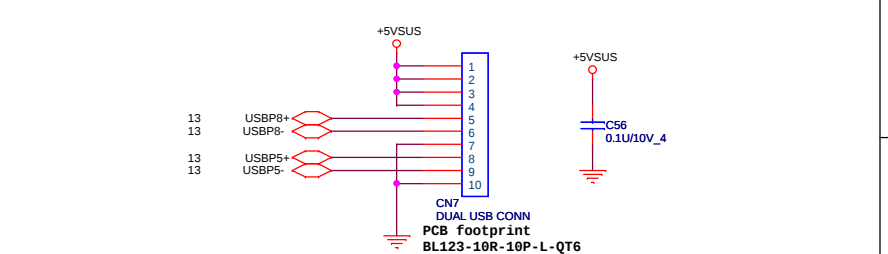
USB Fingerprint CON



LEFT SIDE USBX1 and E-SATA/USB COMBO



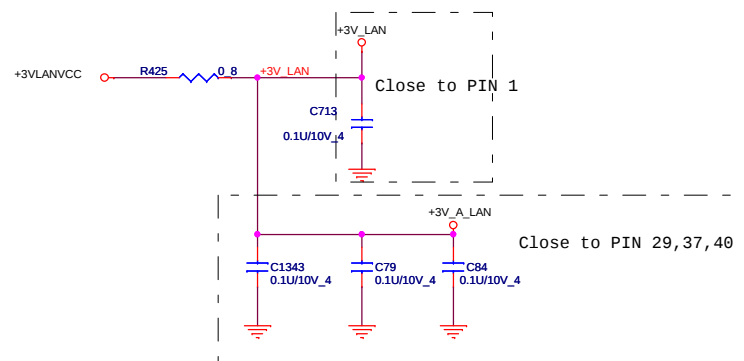
RIGHT SIDE USBX2



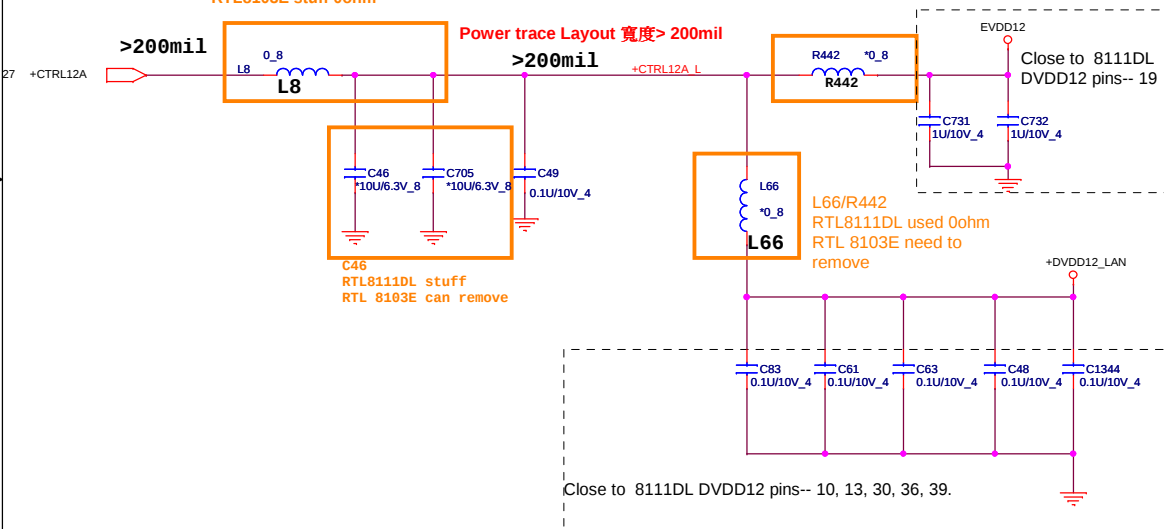


PROJECT : UT12
Quanta Computer Inc.

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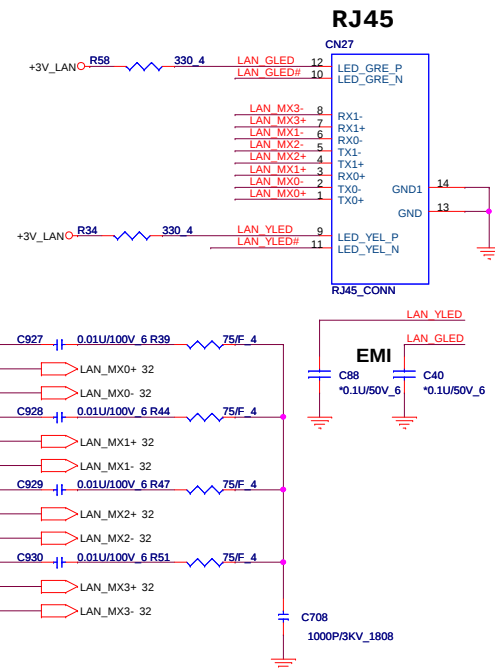
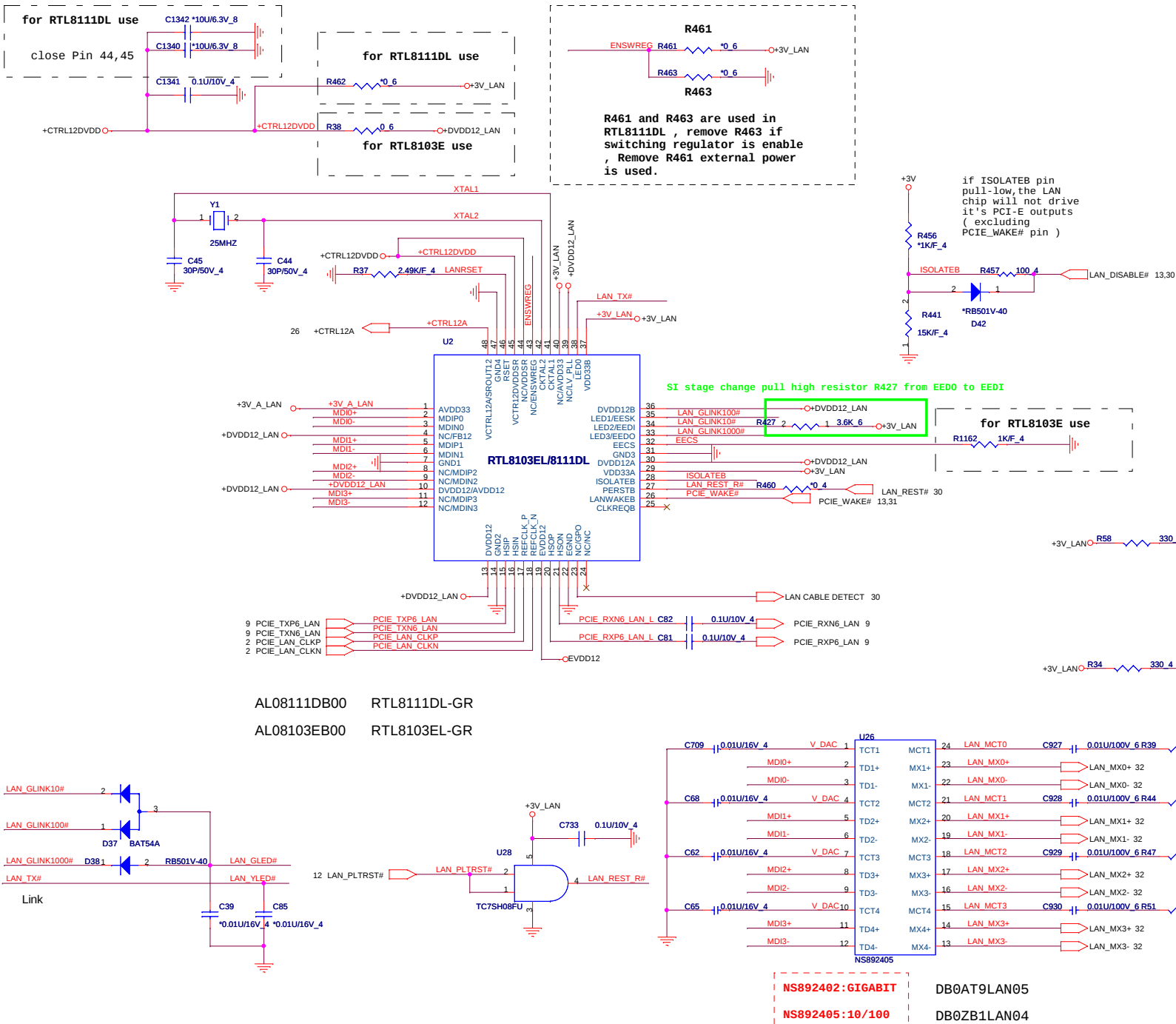


L8
RTL8111DL (Gaga lan) use 4.7uH
power choke A>600mA tolerance
±15%
RTL8103E stuff 0ohm



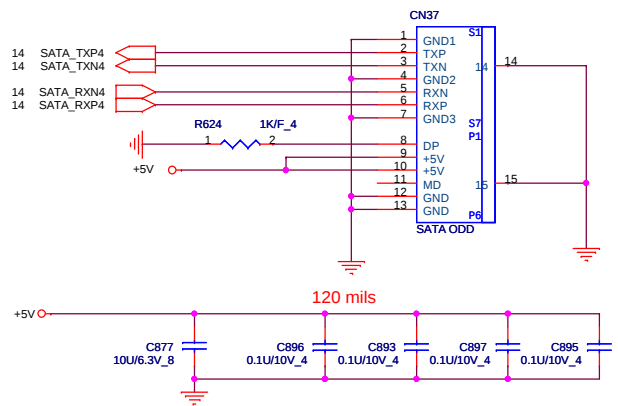
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number LAN Power	Rev 1A
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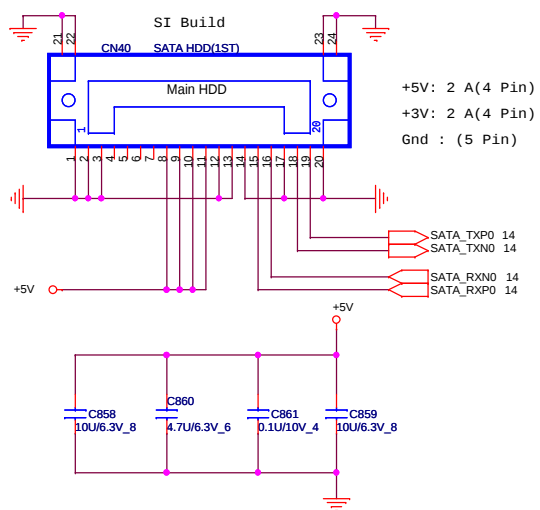


SATA CD-ROM

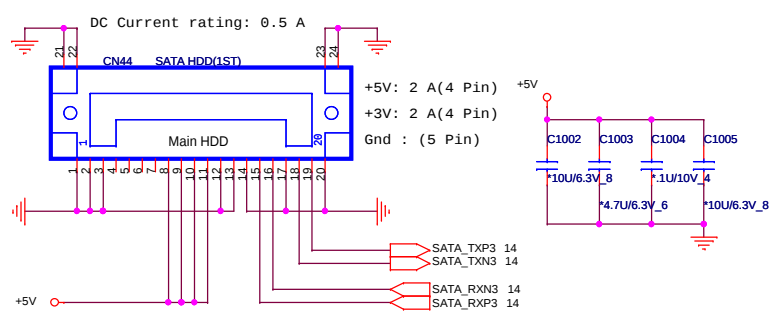
17.3 ODD P/N : DFHS13FR030 or DFHS13FR040
16.3 ODD P/N : DFHD13MR006 , DFHD13MR009 , DFHD13MR008



SATA_1 HDD CONNECTOR

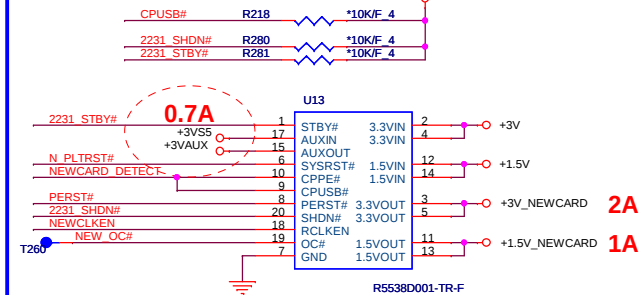
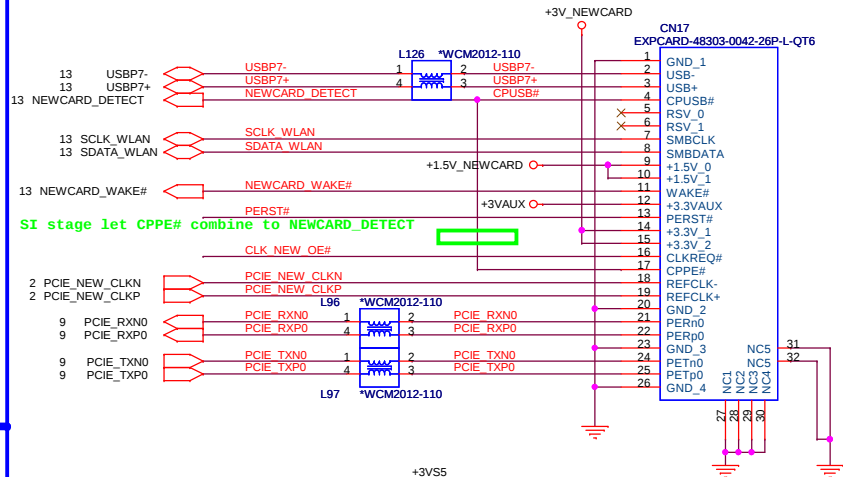


SATA_2 CONNECTOR

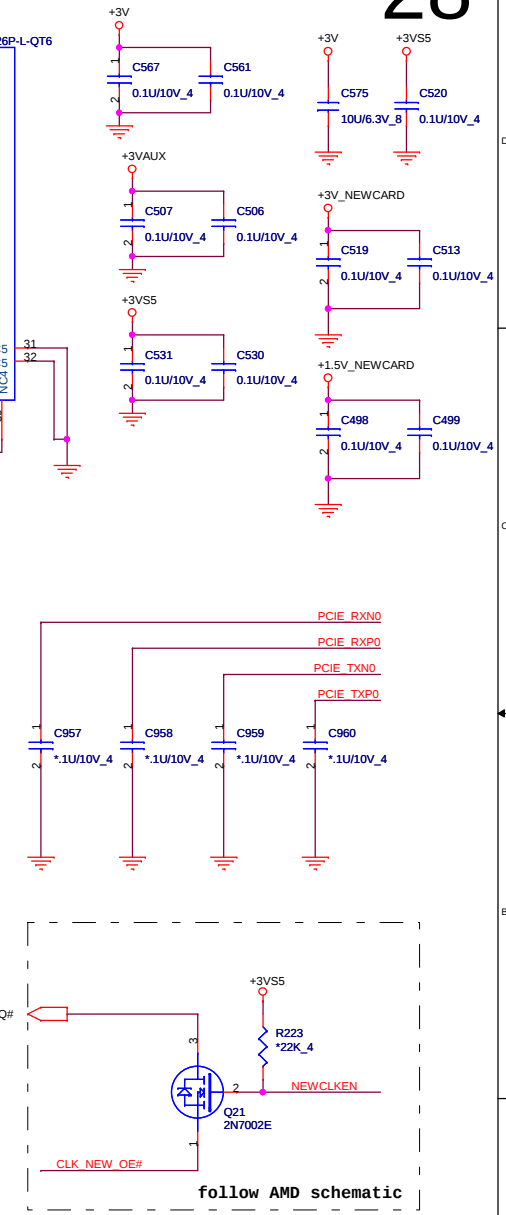
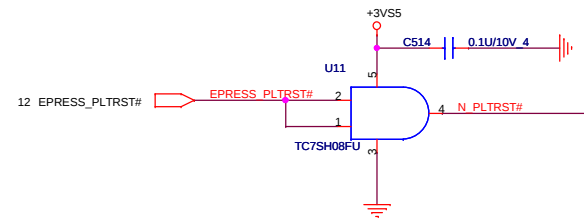


NEWCARD

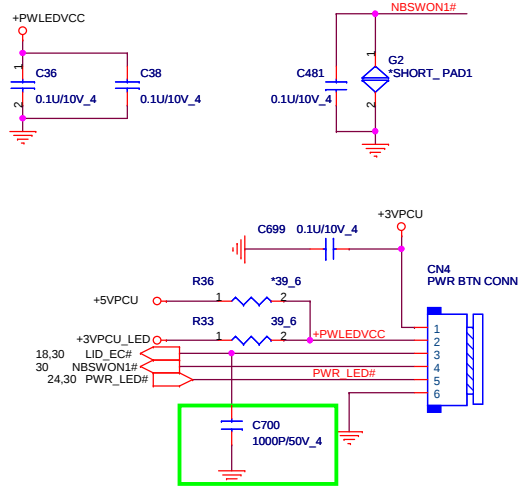
NEWCARD (PCIEXPRESS*1 + USB*1)



R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN



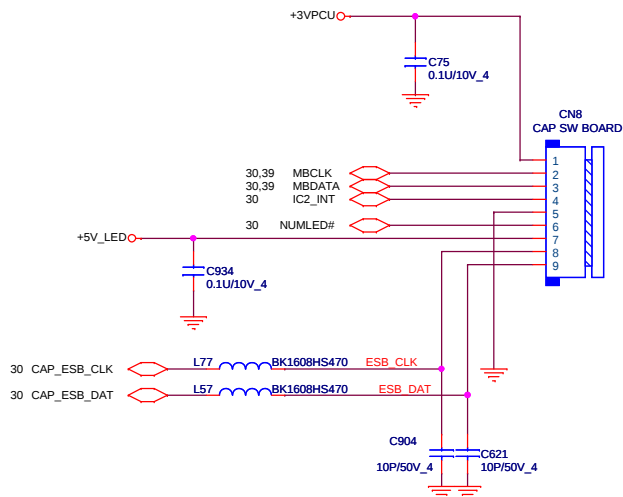
POWER BUTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

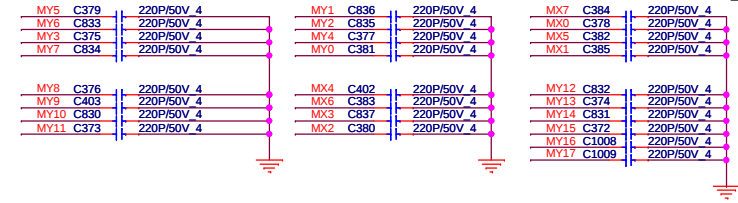
SI stage add 1000P for EMI solution

CAP SW CONNECT

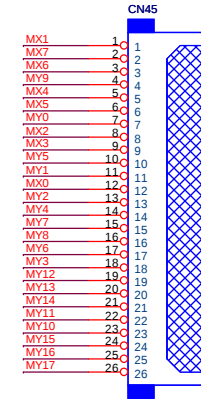
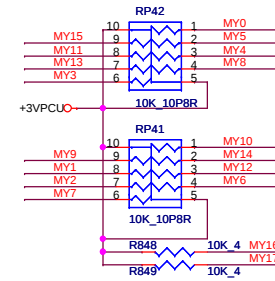


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

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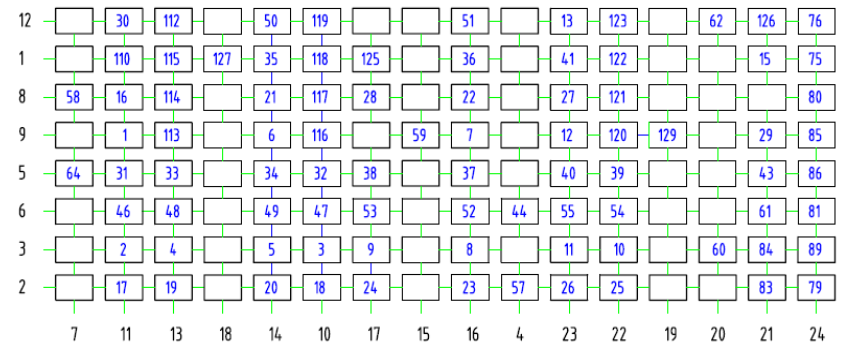
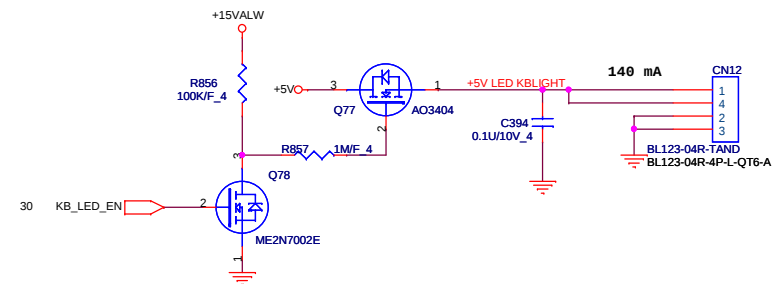


KEYBOARD PULL-UP



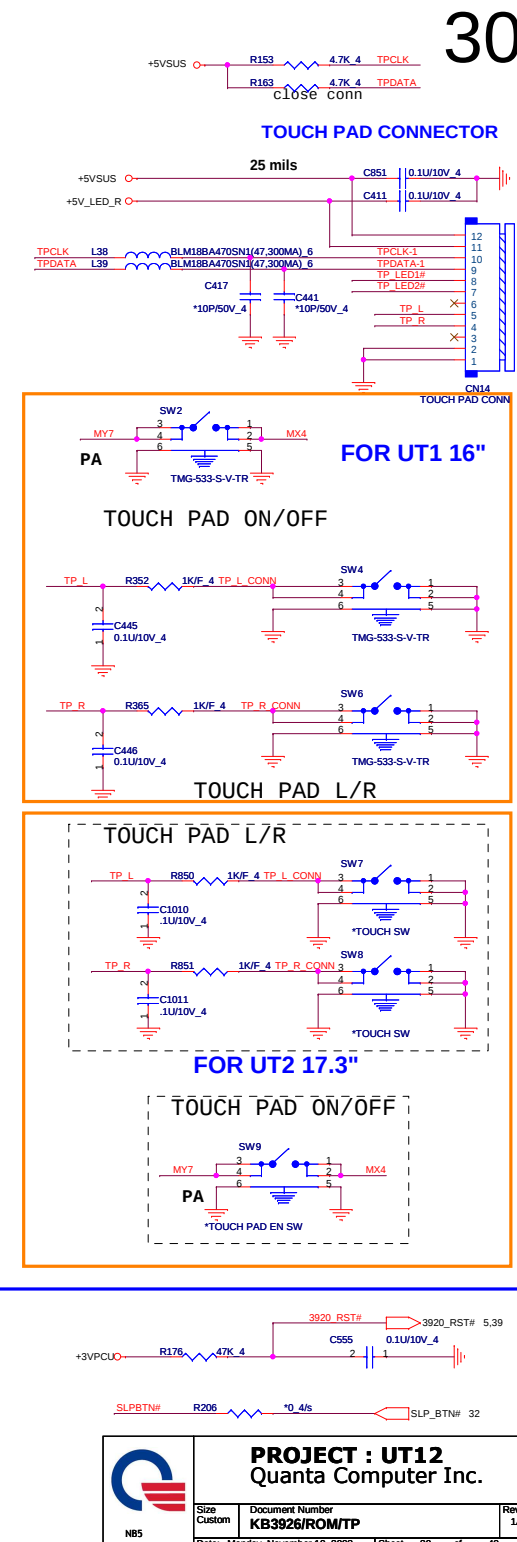
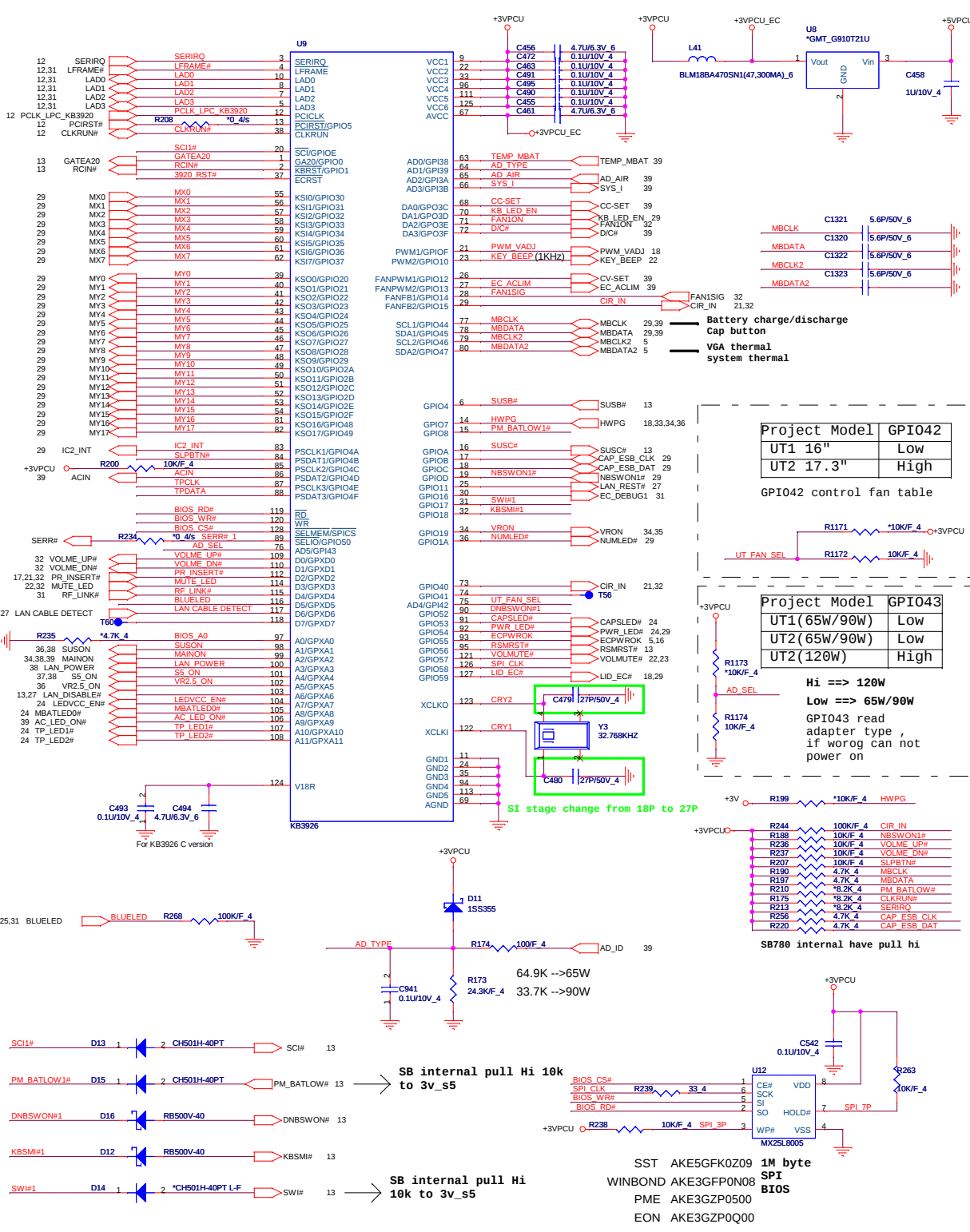
GB1RF260-1253-8F

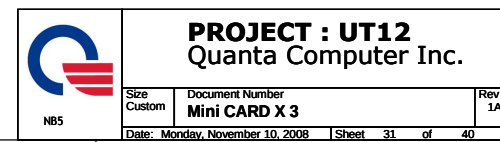
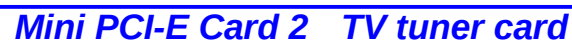
Footprint: "gb1rf260-1253-7f-26p-1"



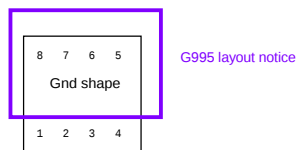
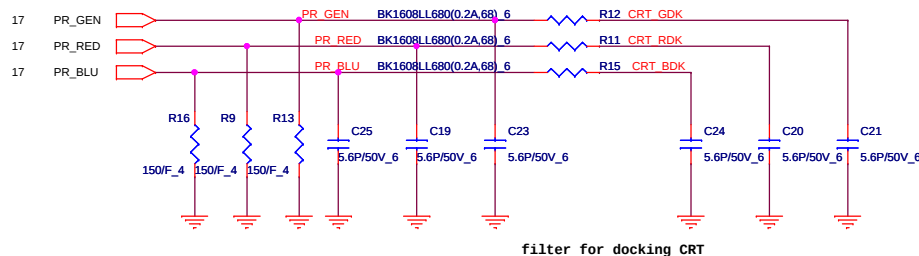
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Quanta Computer Inc.

Size Custom Document Number LED/KEYBOARD/SW Rev 1A
Date: Monday, November 10, 2008 Sheet 29 of 40





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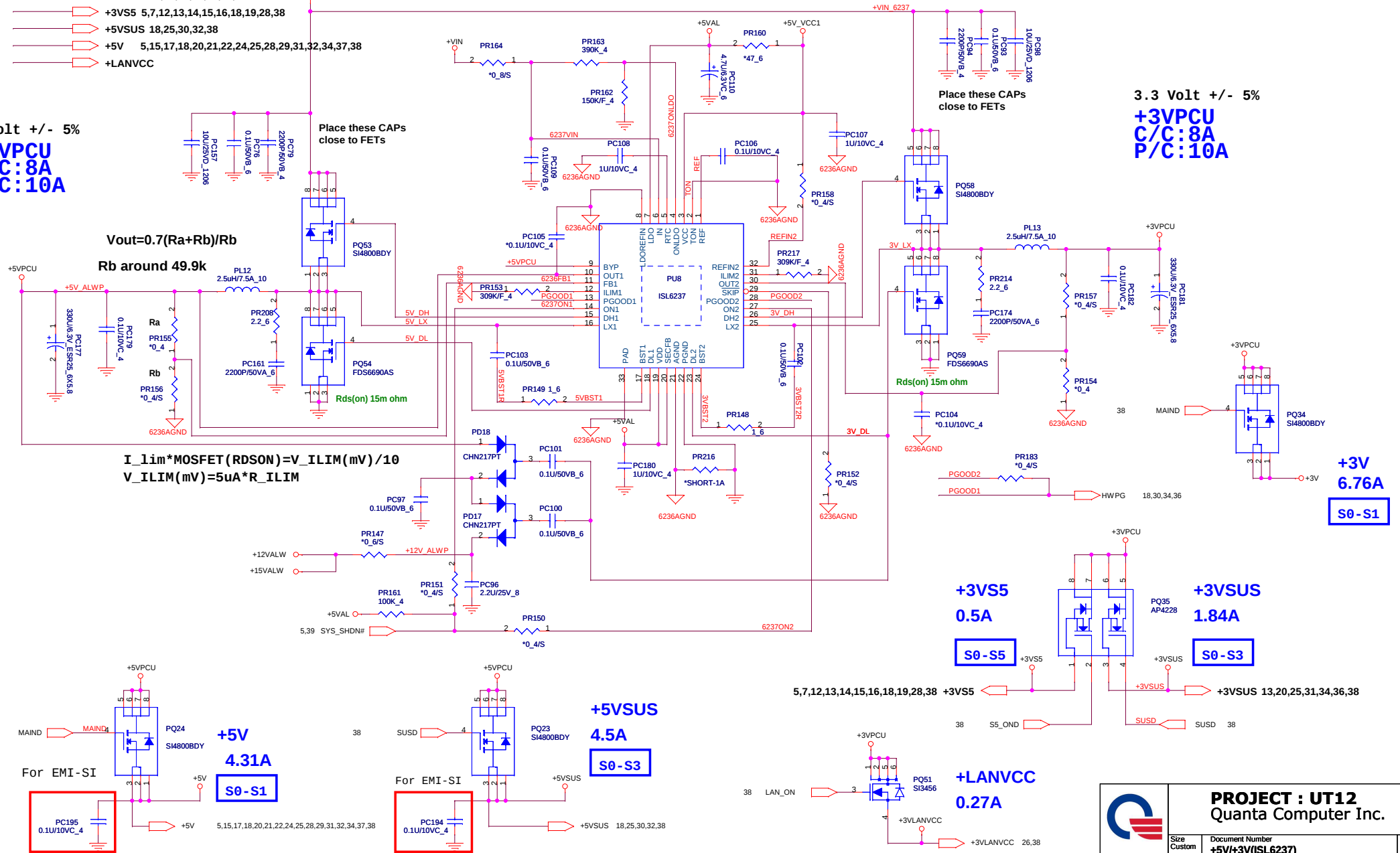


DC/DC +3VPCU/+ 5VPCU/ +12VALW

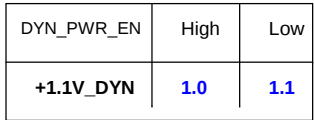
- +5VPCU 21,22,29,30,34,35,36,37
- +3VPCU 5,12,18,24,25,29,30,32,35,36,37,39
- +3VSUS 13,20,25,31,34,36,38
- +3VS5 5,7,12,13,14,15,16,18,19,28,38
- +5VSUS 18,25,30,32,38
- +5V 5,15,17,18,20,21,22,24,25,28,29,31,32,34,37,38
- +LANVCC

5 Volt +/- 5%

+5VPCU
C/C:8A
P/C:10A



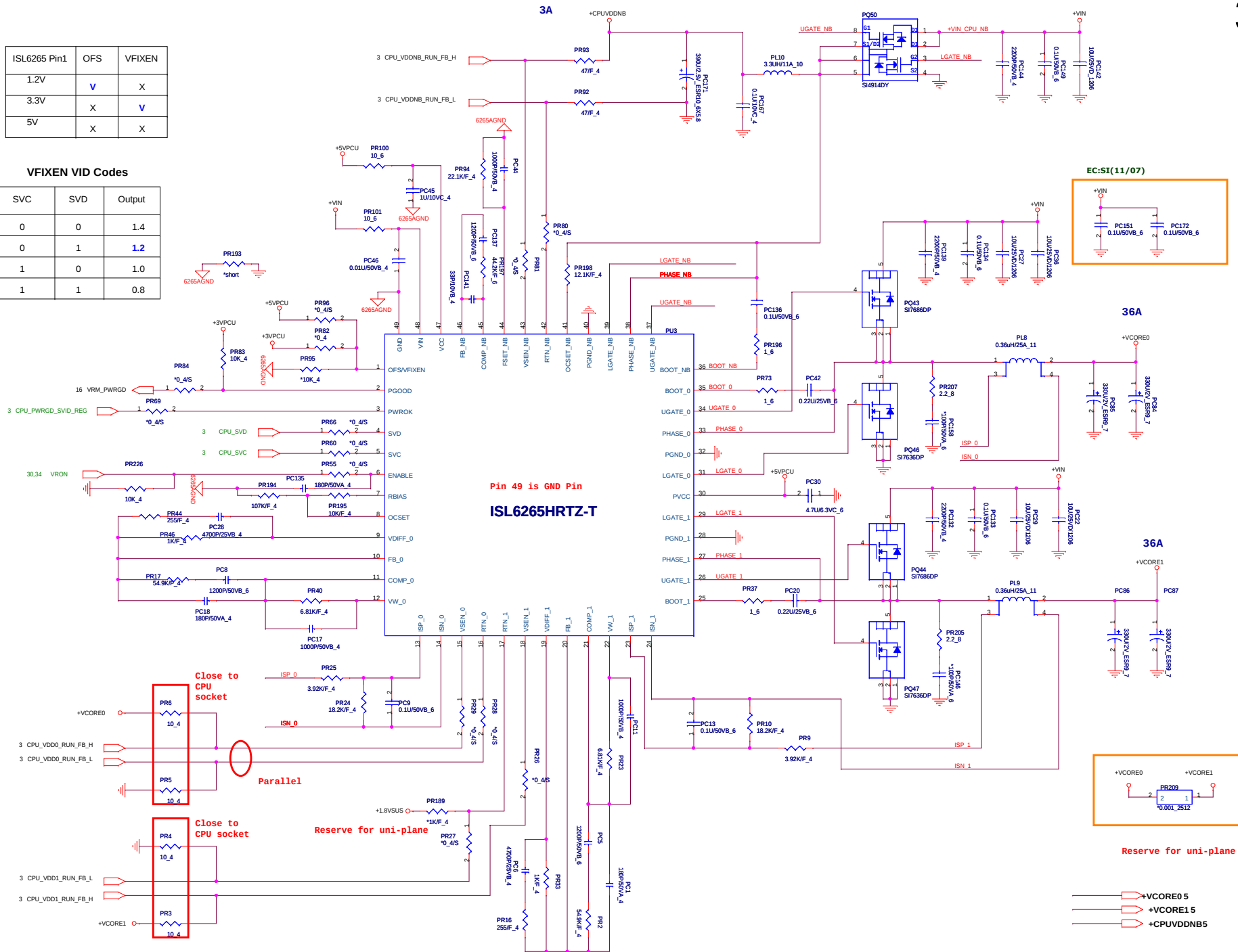
PROJECT : UT12 Quanta Computer Inc.		
Size Custom	Document Number +5V/+3V(ISL6237)	Rev 1A
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

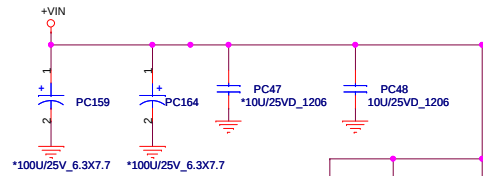
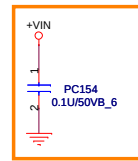


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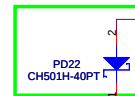
Size C
Document Number
CPU_CORE(ISL6265)
Date: Monday, November 10, 2008 Sheet 35 of 40

 +2.5V 3
 +1.8VSUS 3,4,5,6,7,35,37

EC:SI(11/07)



EC:SI(11/07)



$I_{lim(Valley)} = 10\mu A \cdot R_{ILIM} / R_{DS_ON}$
 For OCP set.

23.65A
S0~S3

+1.8VSUS

PC143 390u/2.5V_6x5.6ESR10

PC153 0.1u/10Vc_4

PC10 100p/50VA_4

Ra PR21 147K/F_4

PC153 0.1u/10Vc_4

PC10 100p/50VA_4

PR36 0.4

51116 V5FILT

Fix 1.8V Output

PR36 0.4

51116 V5FILT

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

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PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

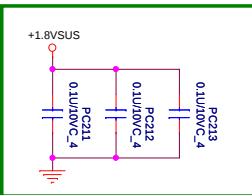
PR36 0.4

PR36 0.4

PR36 0.4

PR36 0.4

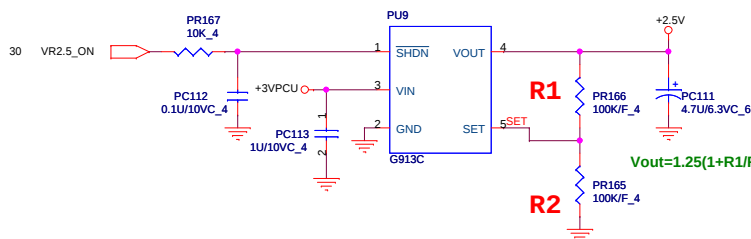
Add 0.1u CAP PC211, PC212, PC213 for EMI



$R_a = (V_{out} - 0.75) / (0.75 \cdot R_b)$
 R_b value from 100K to 300K ohm

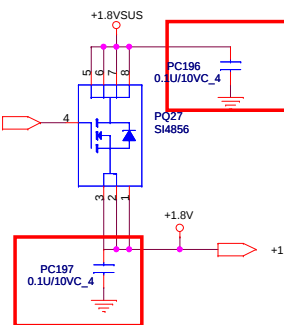
2.5V
0.25A
S0~S1

S0~S1

Close to CPU
SI power

Vout=1.25(1+R1/R2)

For EMI-SI



Discrete:SI4856
UMA:SI4800

For EMI-SI

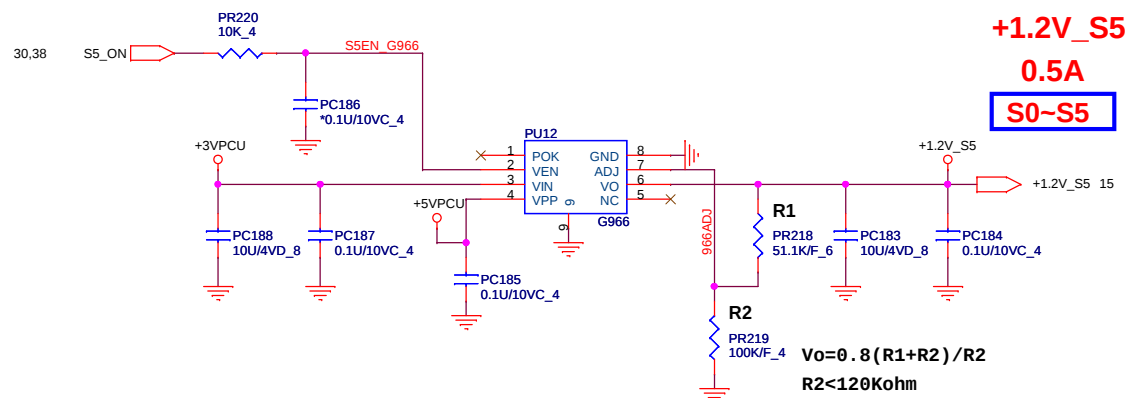
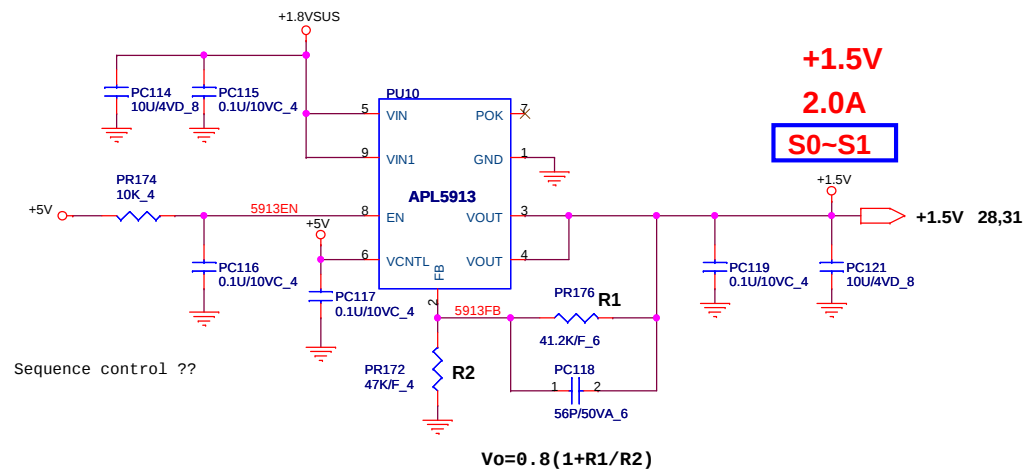
1.8V
10.4A
S0~S1

S0~S1

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

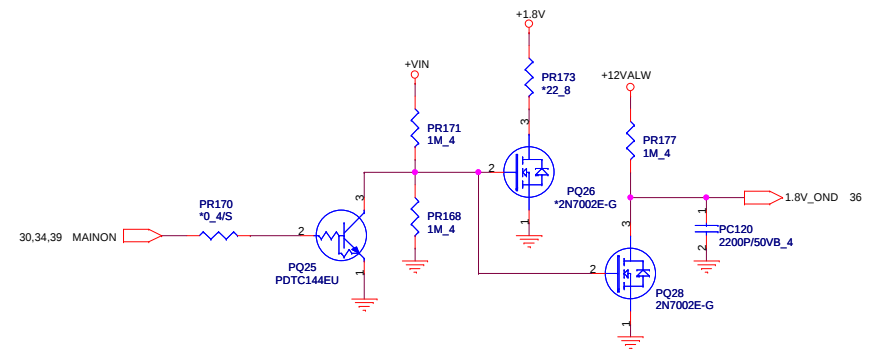
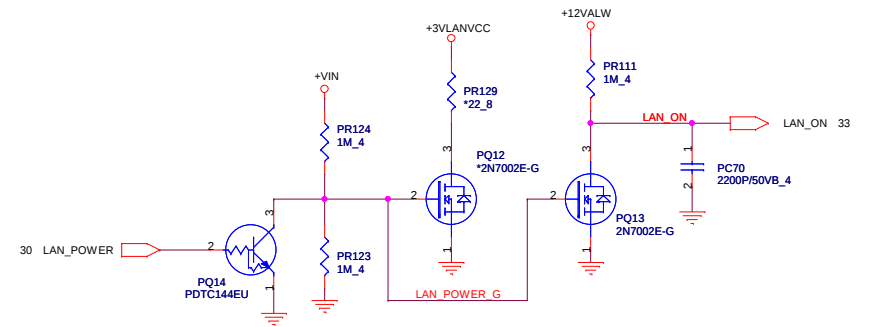
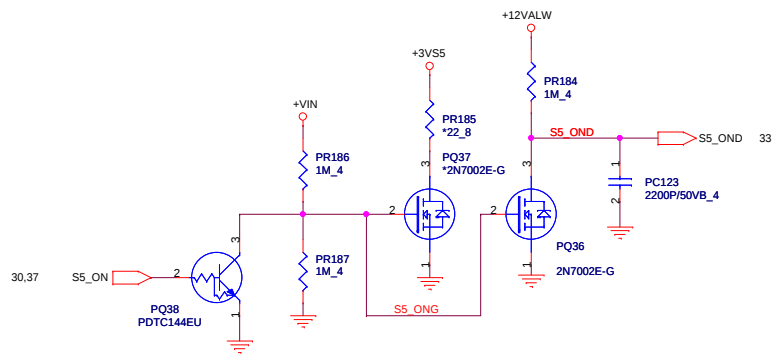
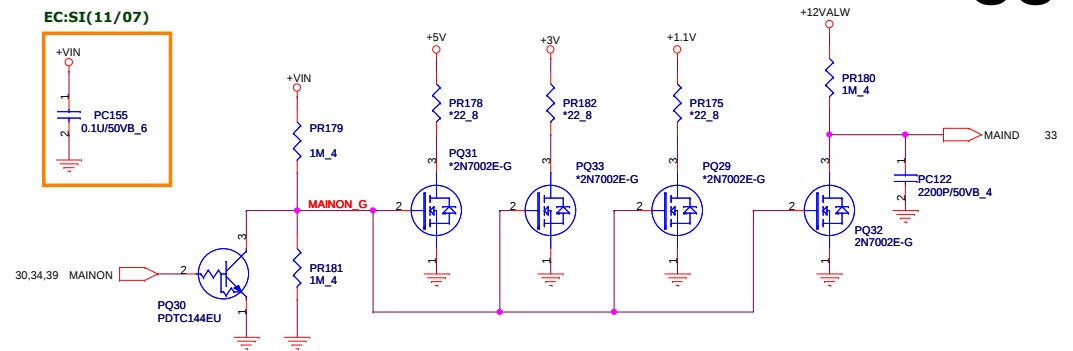
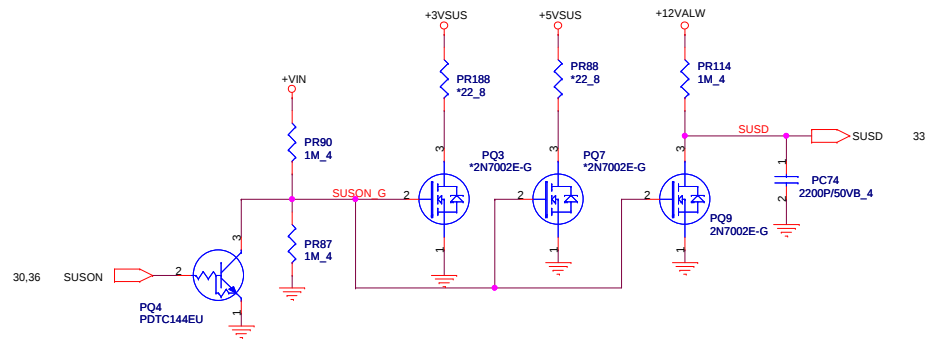
 $V_{TRIP}(mV) = R_{TRIP}(Kohm) \cdot 10(\mu A)$
 $I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_vddqsns/2	DDR
V5IN	1.8	V_vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V



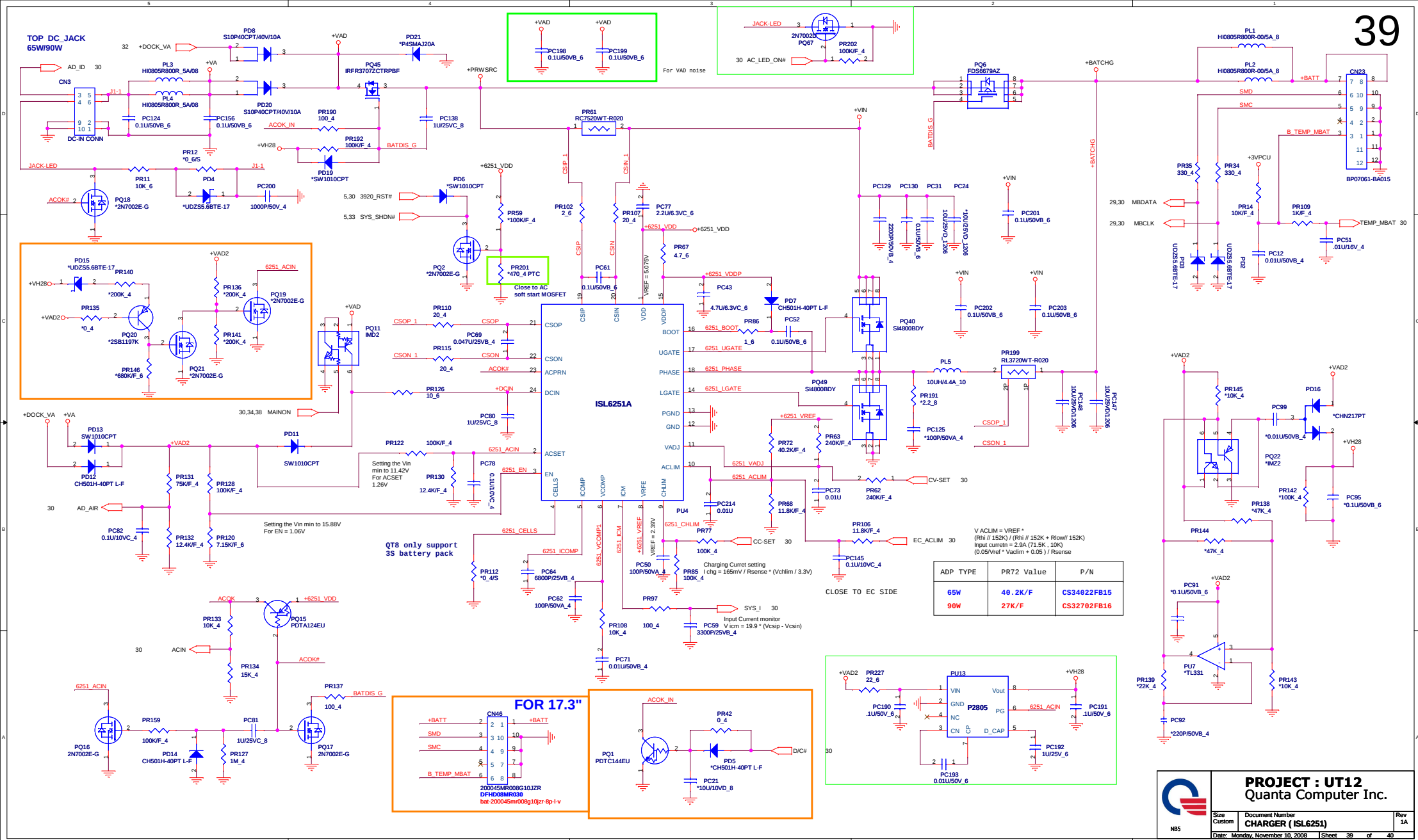
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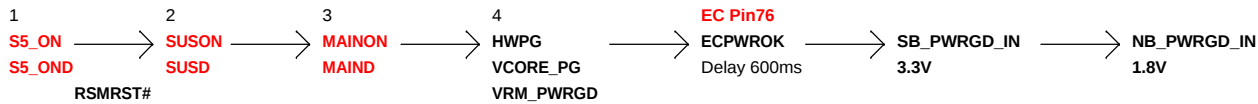
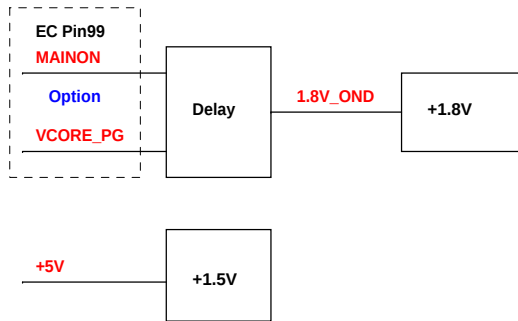
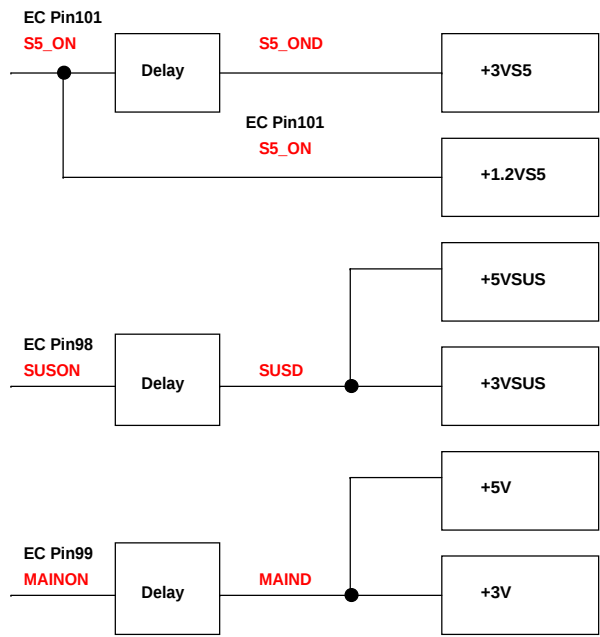
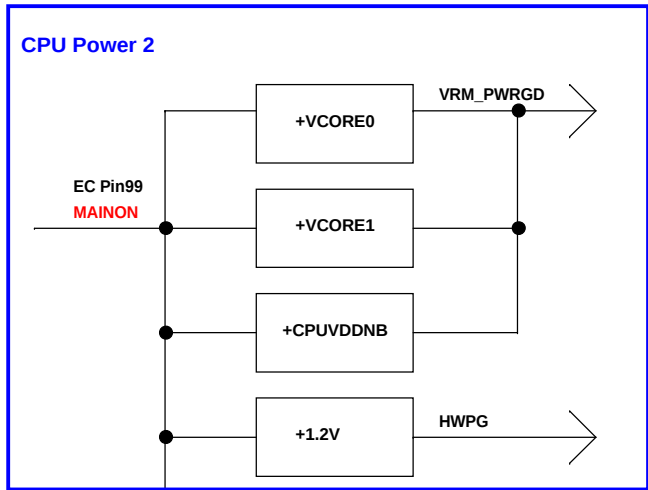
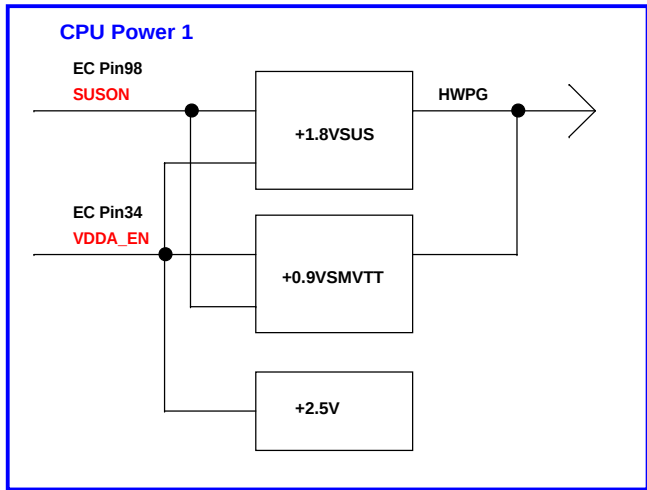
Size B	Document Number VGA PWR OZ8118/1.2V_S5/+1.5	Rev 1A
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Size Custom	Document Number DISCHARGE	Rev 1A
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Size Custom	Document Number Power control	Rev 1A
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