AT3 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1
PAG 13,14
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 13,14
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON
PAG 26

TV_OUT
CRT_OUT

CRT / S-VIDEO
PAG 25

LVDS(2 Channel)

Panel Connector
15" / 17" PAG 26

DMI LINK

NBSRCCLK, NBSRCCLK#

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0
5 | 0,1,2 | 3 | 4,6,7

Bluetooth PAG 35
USB2.0 I/O Ports X3 PAG 32
Camera X1 PAG 32
Mini PCI-E Card x1
Express Card x1
Cable Docking x1

Option for 17" only
SATA - HDD PAG 35
SATA2

SATA - HDD PAG 32
SATA0 150MB

PATA- CD-ROM PAG 32
PATA (66/100/133)

PCI BUS / 33MHz
PCI-E
Azalia

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
10/100/GagaLAN
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

Realtek
ALC 268
PAG 29

Two-element microphone
PAG 29

Audio Jacks
(Phone/ MIC)
PAG 29

LPC

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

Keyboard Touch Pad PAG 36
CIR PAG 36
Capacitive Sense SW PAG 36

X-Bus

FAN PAG 38
Flash PAG 37
SPI PAG 37

AUDIO Amplifier PAG 30
Jack to Speaker PAG 30

MDC DAA
SI3080
PAG 31
MODEM RJ 11 PAG 33

SIM CARD PAG 32
RJ45 PAG 33
IEEE1394 CONN PAG 28
Memory CardReader PAG 27

SYSTEM CHARGER(MAX8724) PAG 41
SYSTEM POWER MAX8778 PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43
VGACORE(1.025V)MAX1992 PAG 45
CPU CORE MAX8771 PAG 44

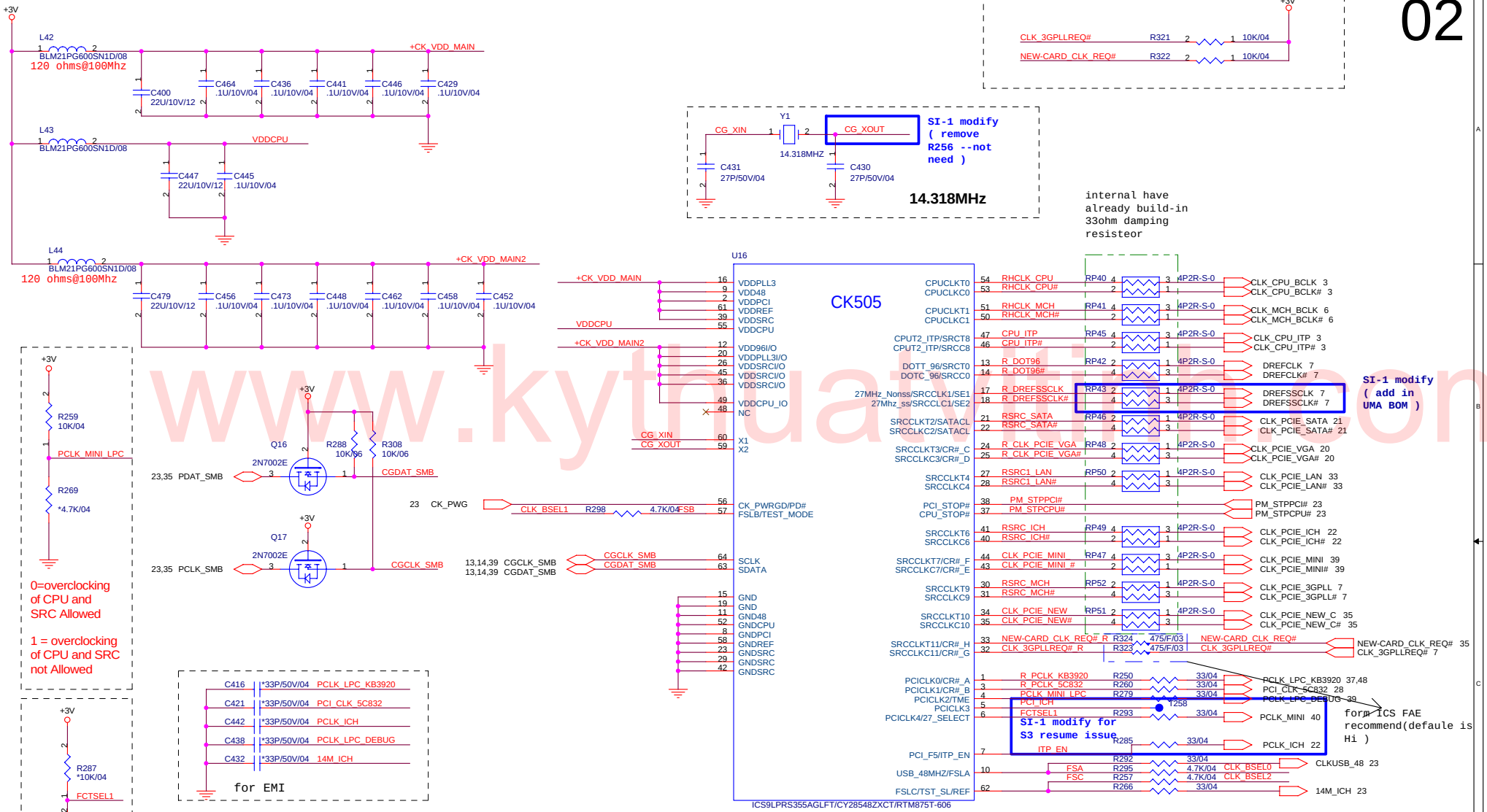
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, September 11, 2006 Sheet 1 of 48



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

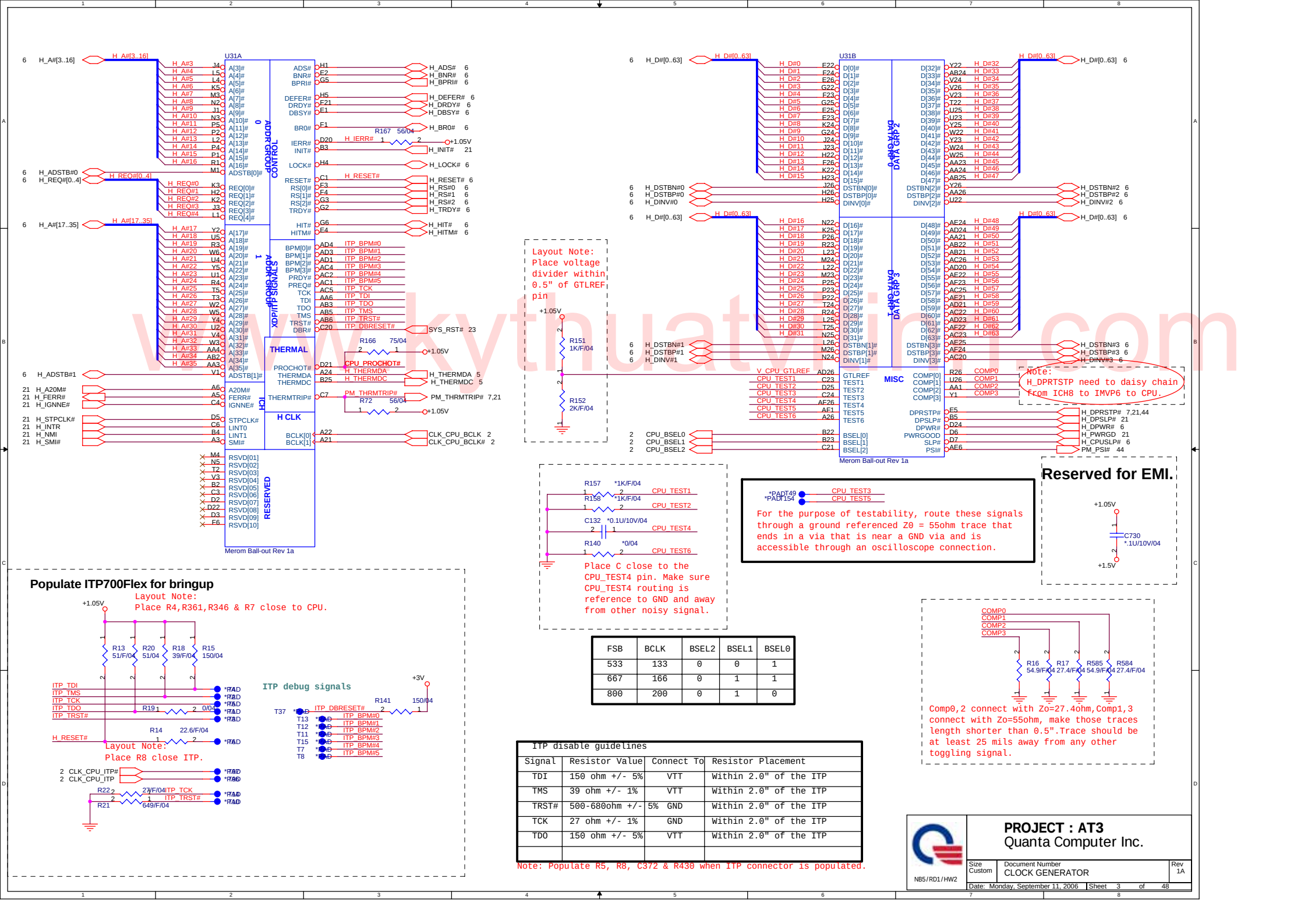
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Monday, September 11, 2006 | Sheet 2 of 48

NB5/RD1/HW2



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

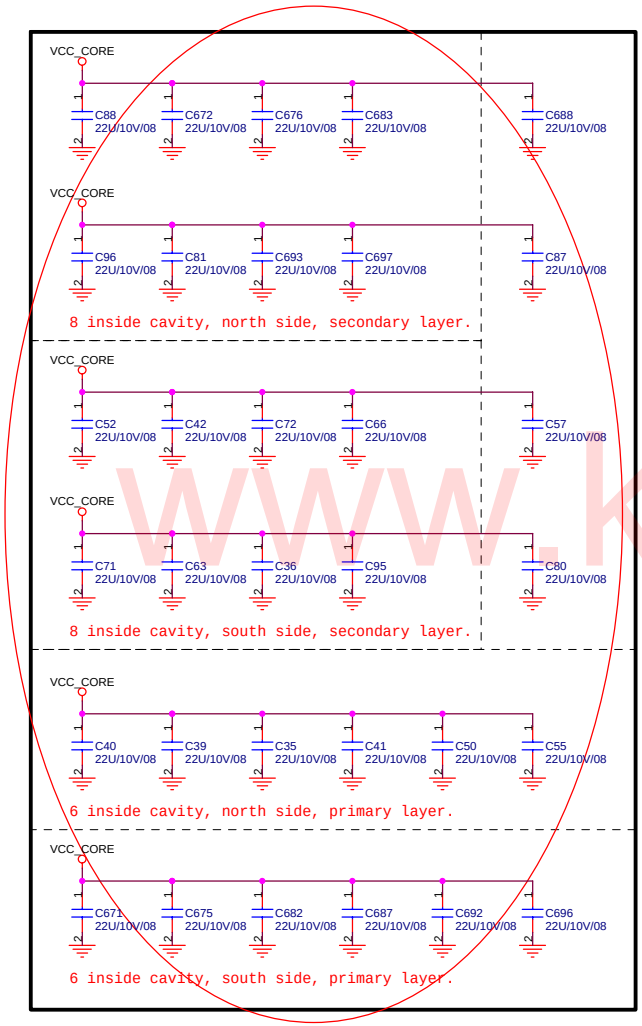
Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

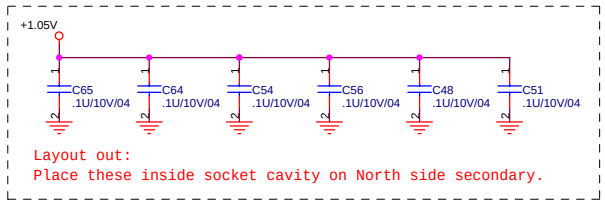
NB5/RD1/HW2

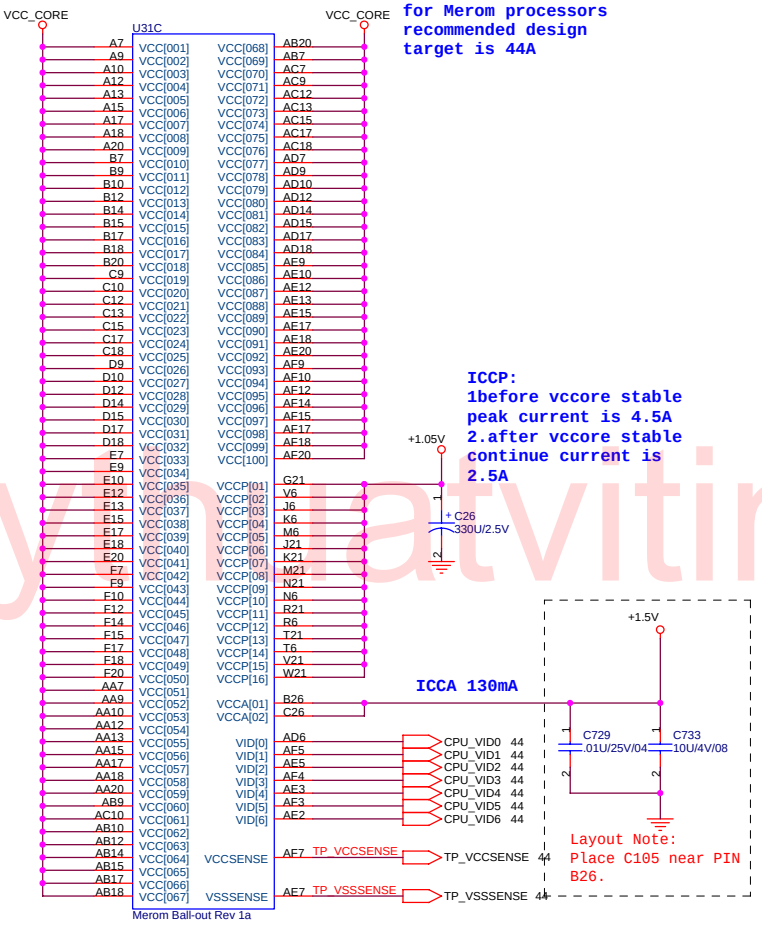
PROJECT : AT3
Quanta Computer Inc.

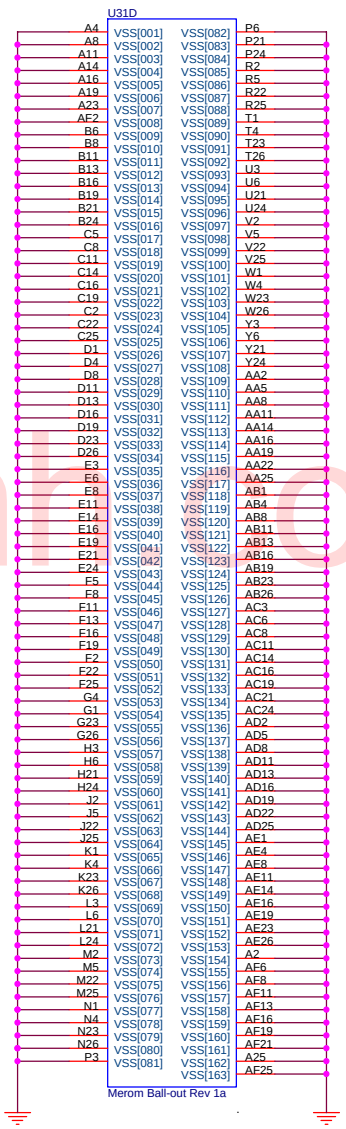
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Monday, September 11, 2006 Sheet 3 of 48







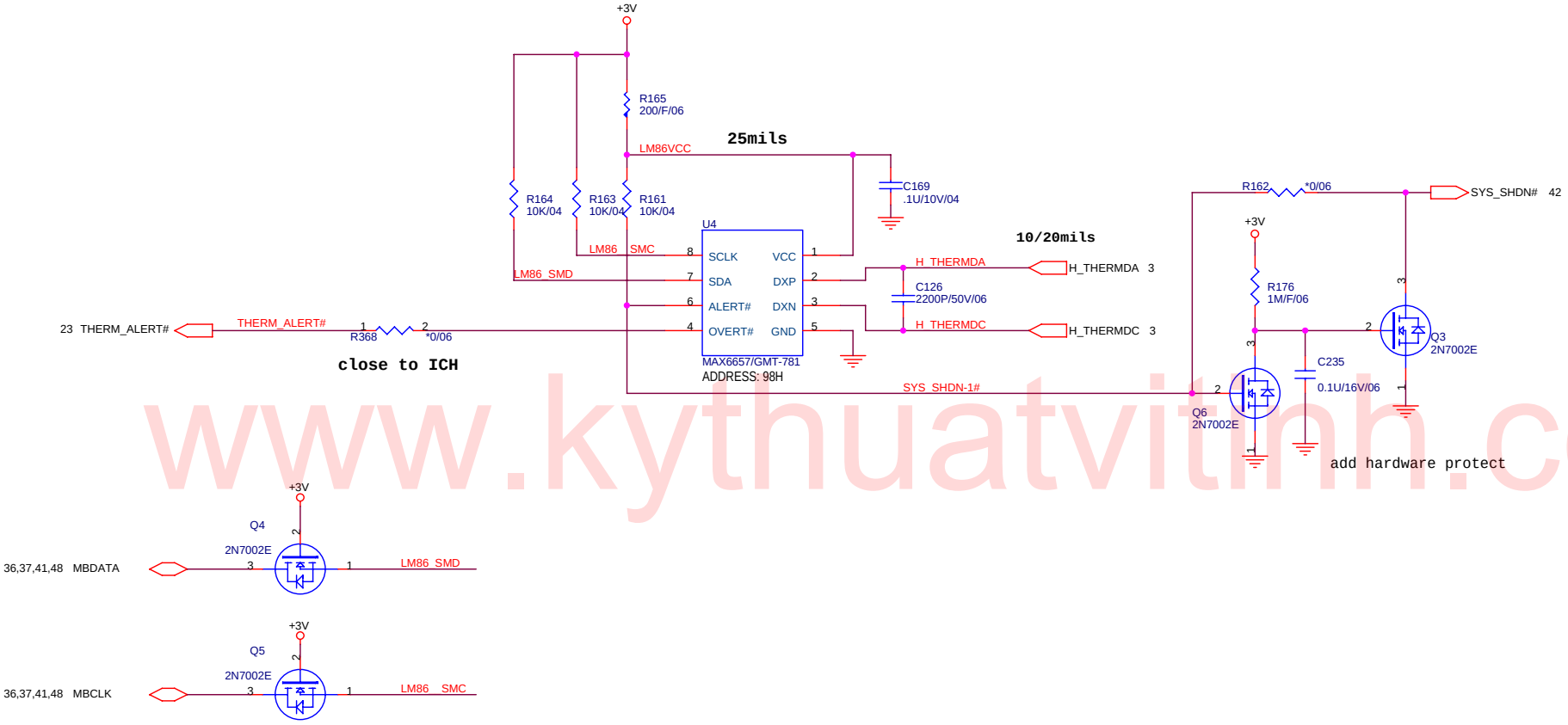


PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom Processor (POWER)	1A

NB5/RD1/HW2

Date: Monday, September 11, 2006 | Sheet 4 of 48



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
B	THERMAL LM86	1A

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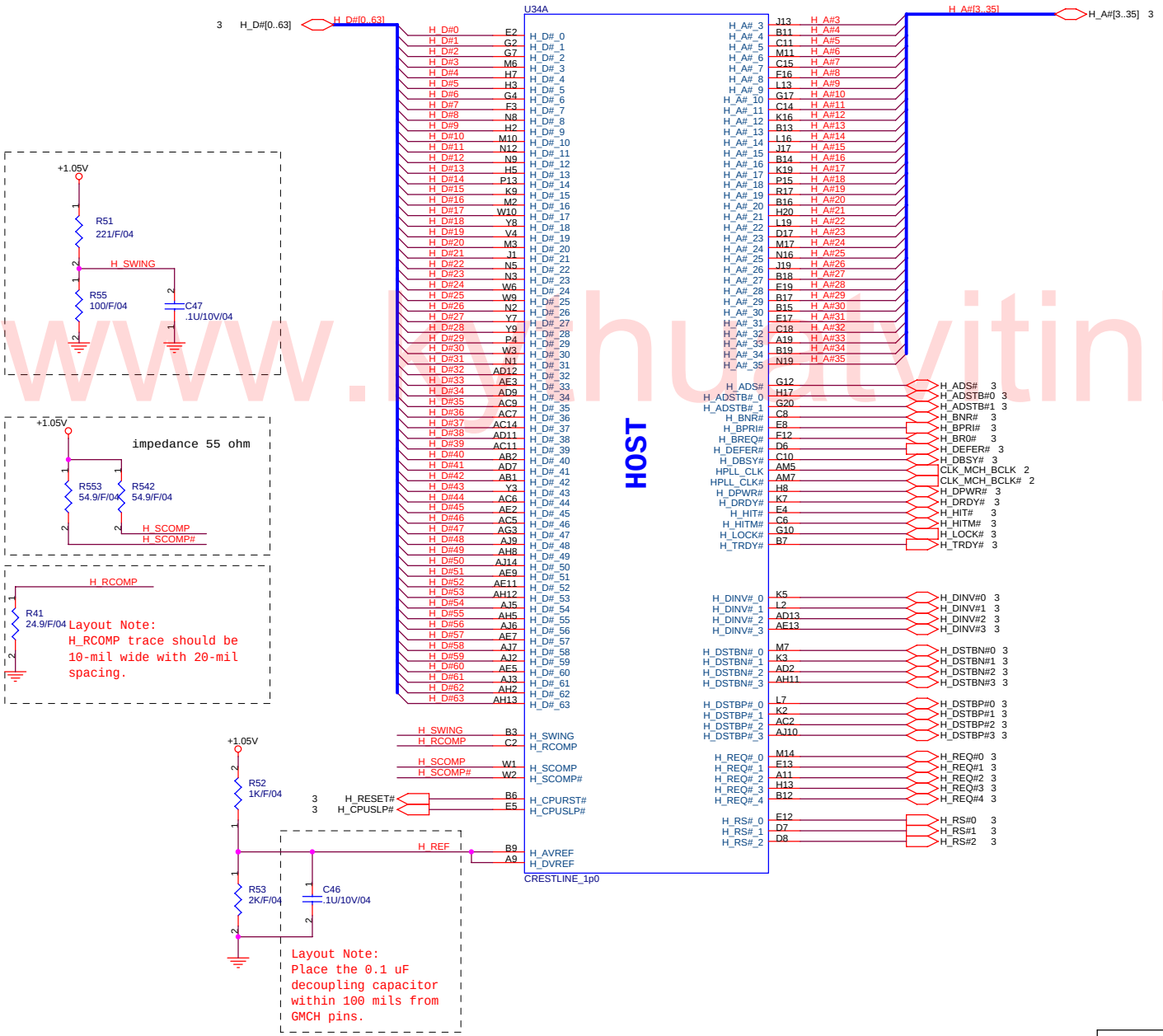
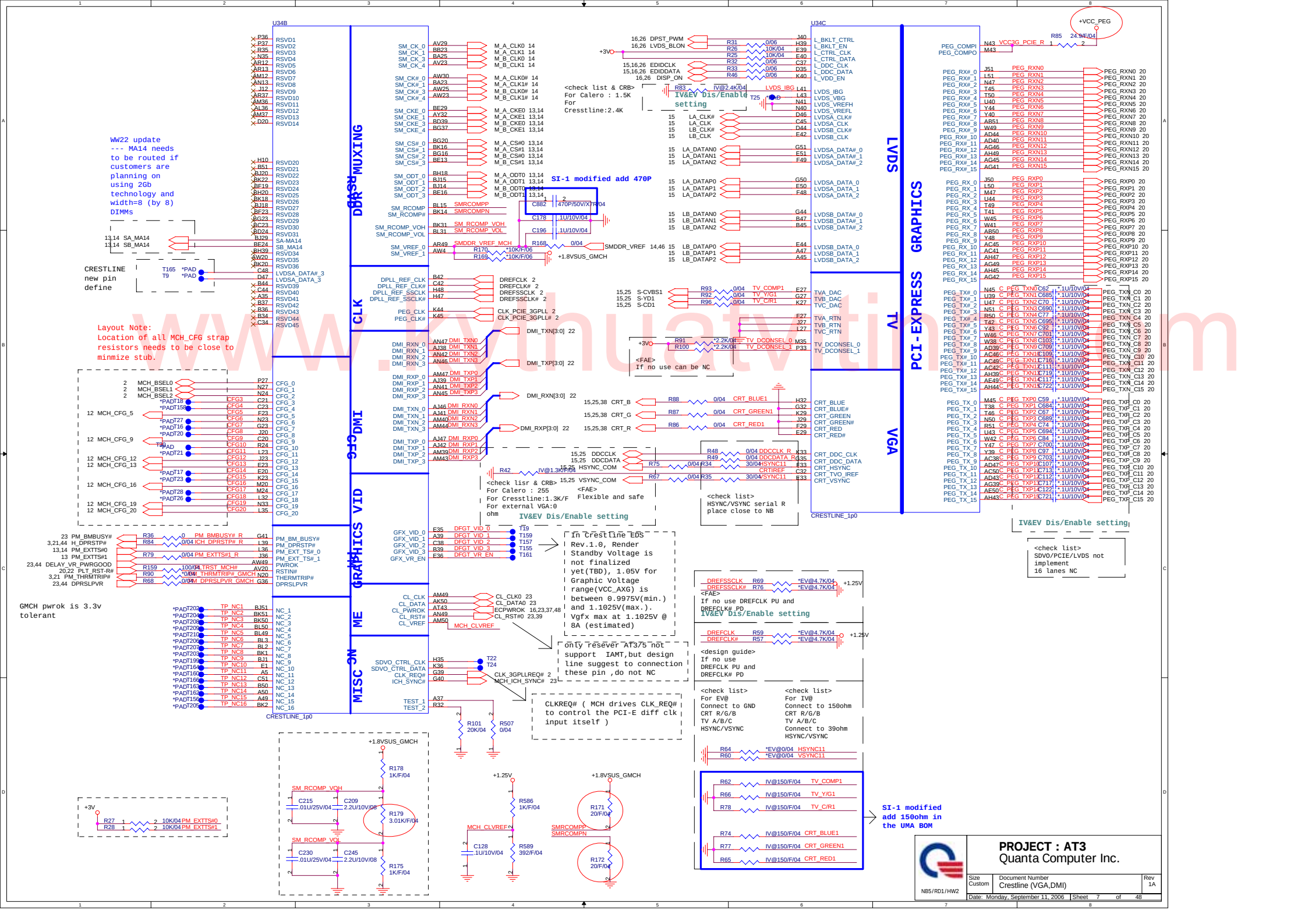


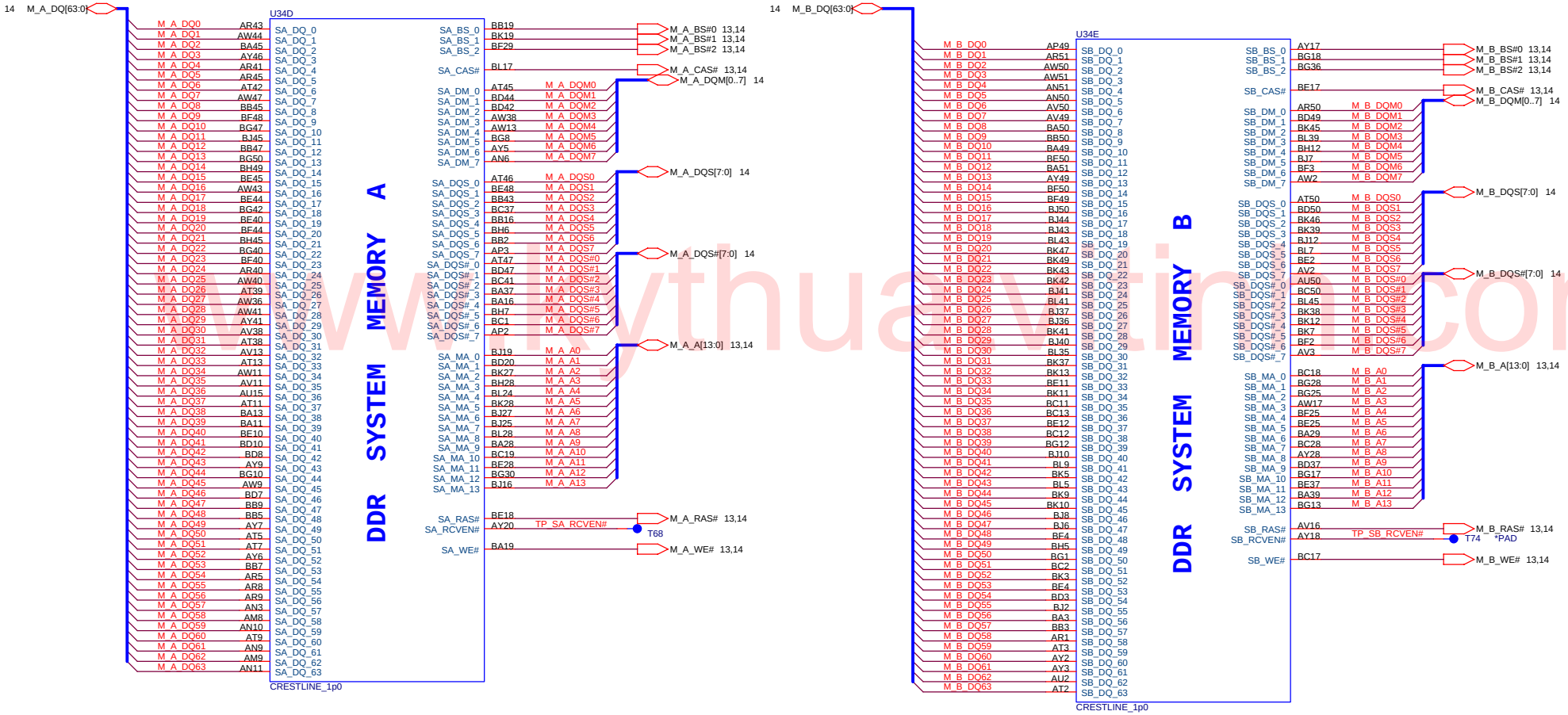
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (HOST)	1A

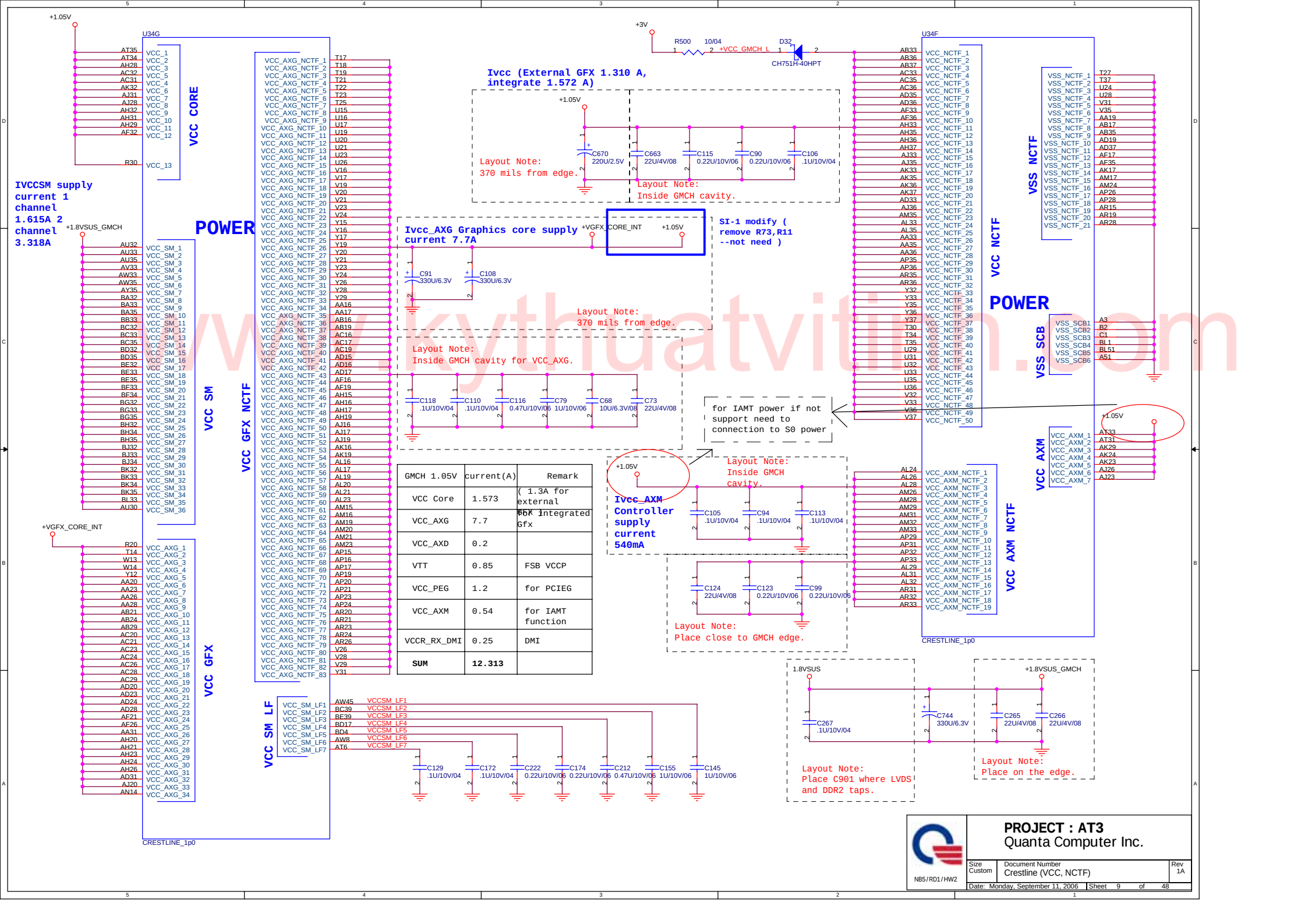
NB5/RD1/HW2

Date: Monday, September 11, 2006 | Sheet 6 of 48





NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (DDR)	Rev: 1A
Date: Monday, September 11, 2006	Sheet 8 of 48	



GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external 6bx integrated Gfx
VCC_AXG	7.7	
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	Crestline (VCC, NCTF)	1A

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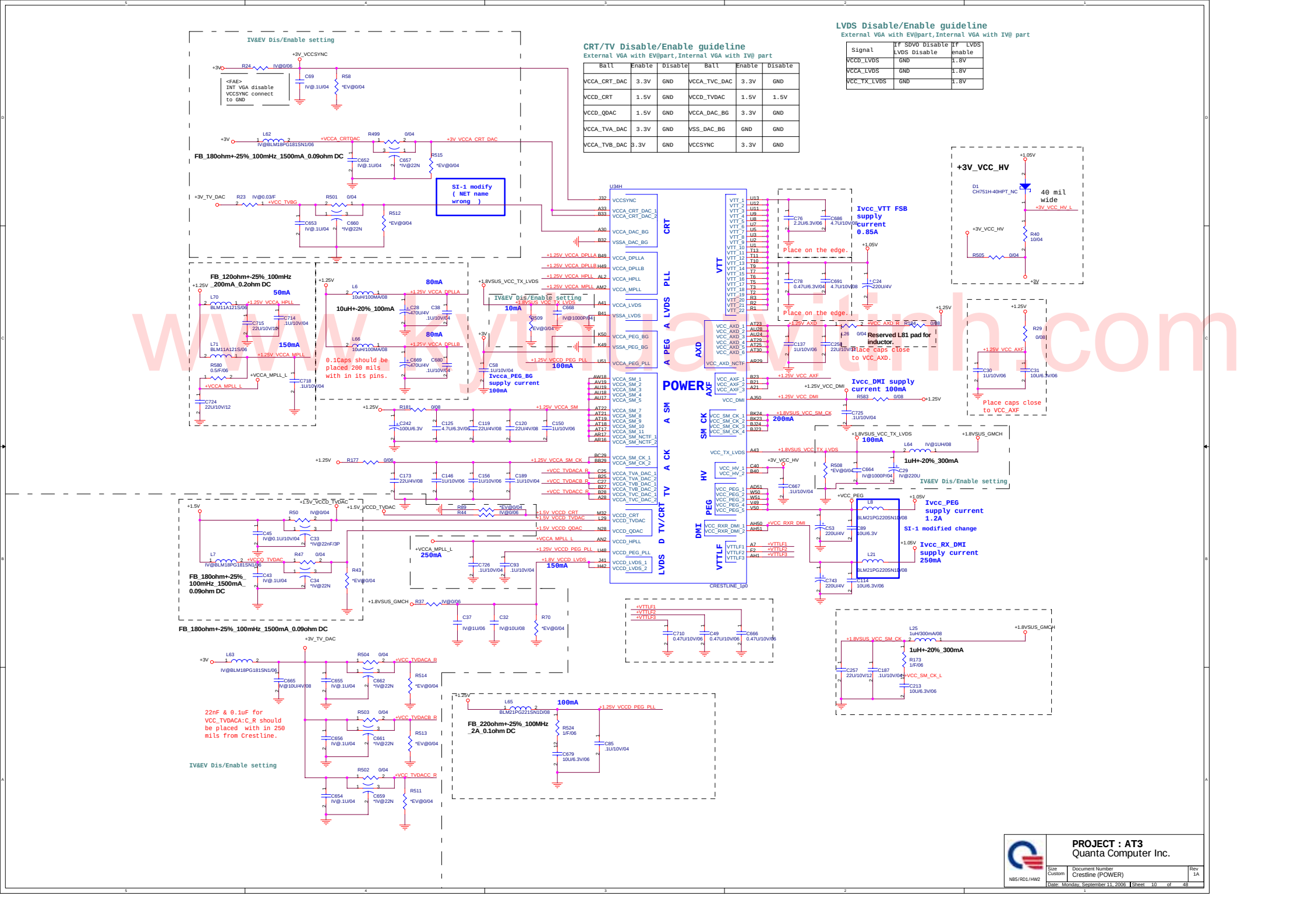
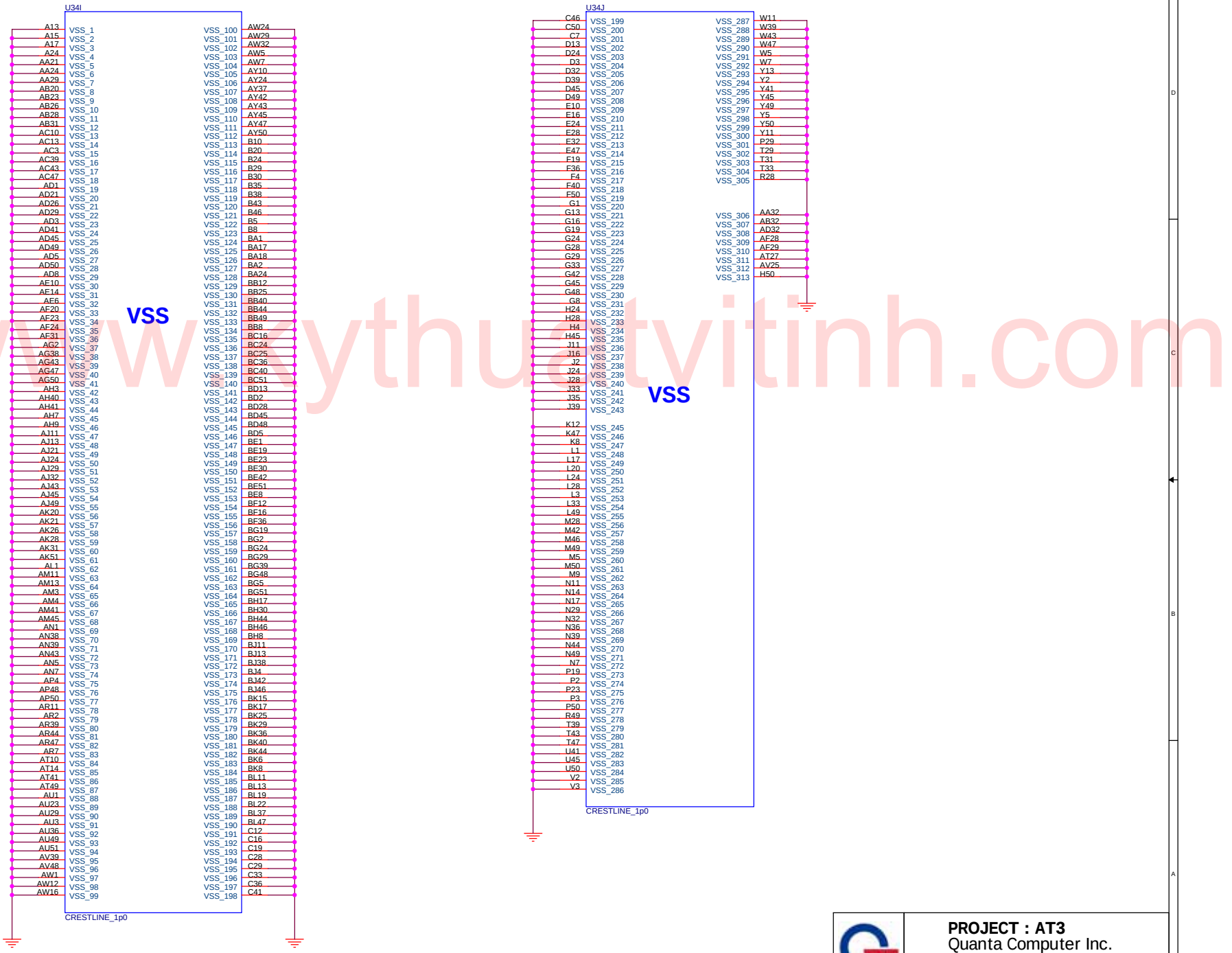


PROJECT : AT3			
Quanta Computer Inc.			
NB5/RD1/HW2	Size: Custom	Document Number: Crestline (POWER)	Rev: 1A
	Date: Monday, September 11, 2006	Sheet 10 of 48	



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom Document Number: Crestline (VSS)	Rev: 1A
	Date: Monday, September 11, 2006	Sheet 11 of 48

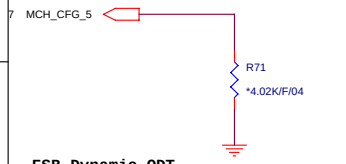
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

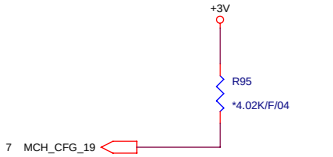
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

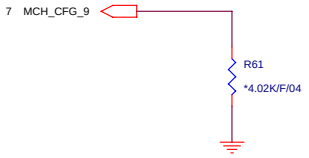


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

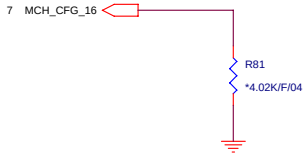


SDVO Present

Strap define at External DVI control page

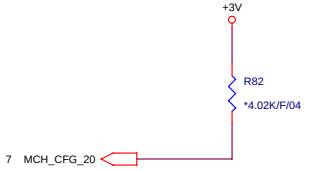
FSB Dynamic ODT

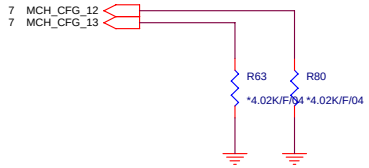
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

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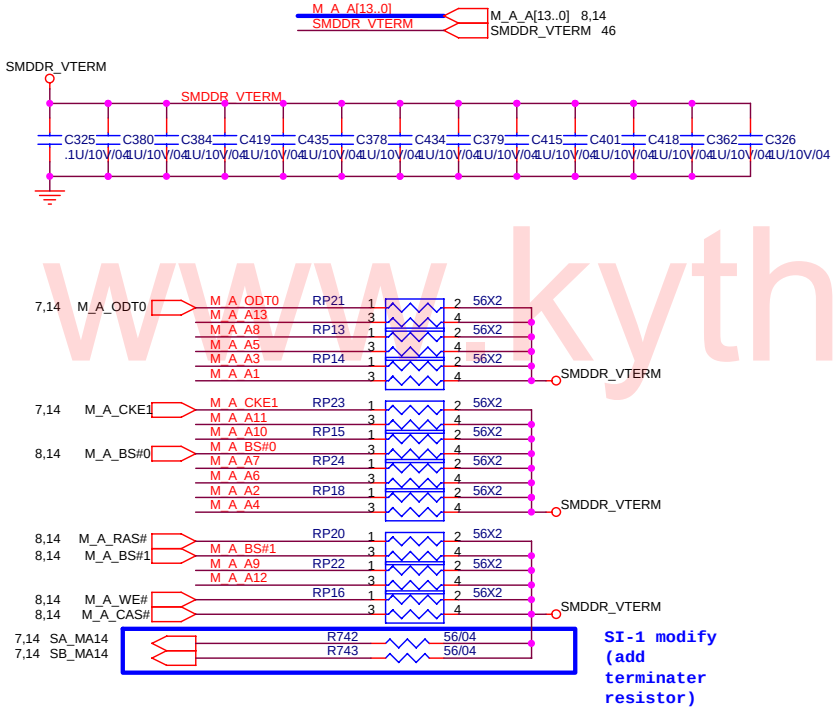
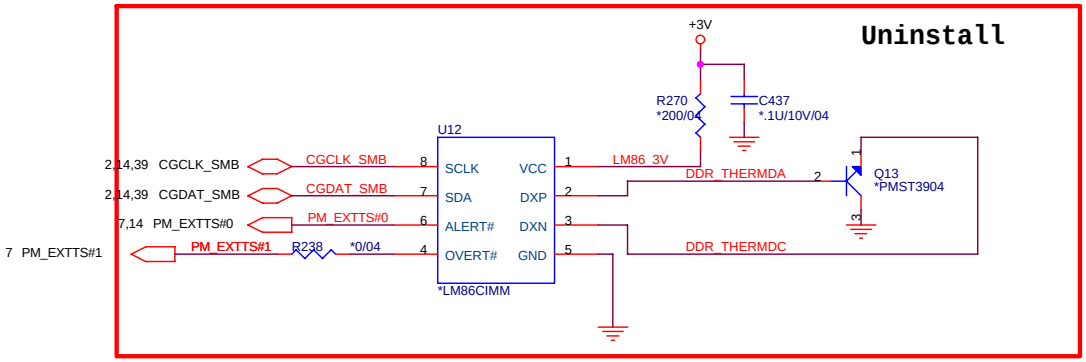
DDRII DUAL CHANNEL A,B.

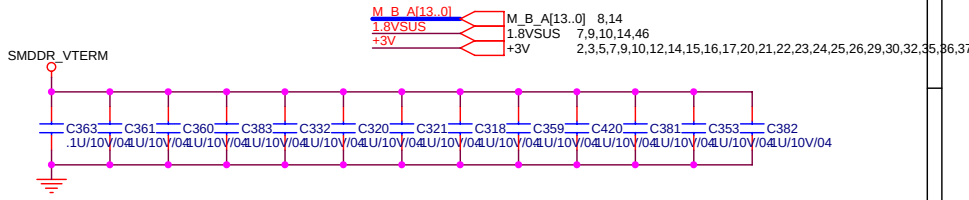
DDRII A CHANNEL



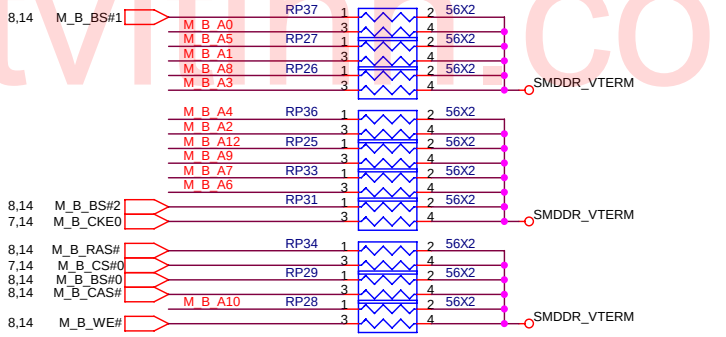
SI-1 modify (add terminater resistor)

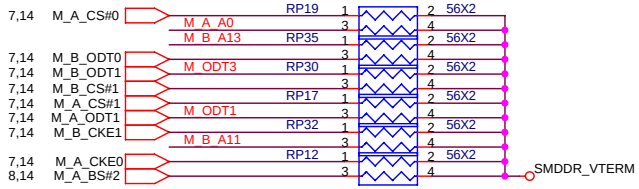


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
B	DDRII RES.ARRAY	1A

Date: Monday, September 11, 2006 Sheet 13 of 48

CGCLK_SMB
CGDAT_SMB
CGCLK_SMB 2,13,39
CGDAT_SMB 2,13,39

M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_CKE[0..1] 7,13
M_A_CS#[0..1] 7,13

M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_RAS# 8,13
M_A_CAS# 8,13
M_A_WE# 8,13

M_A_CLK0
M_A_CLK0# 7
M_A_CLK1 7
M_A_CLK1# 7
M_A_BS#[0..2] 8,13
M_A_ODT[0..1] 7,13

M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
M_A_DQM[0..7] 8
M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DQS#[0..7] 8
M_A_A[13..0] 8,13

+3V
1.8VSUS
+3V 2,3,5,7,9,10,12,13,15,16,17,20,21,22,23,24,25,26,29,30,32,35,36,37,39,40,42,47
1.8VSUS 7,9,10,46

M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_CKE[0..1] 7,13
M_B_CS#[0..1] 7,13

M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_RAS# 8,13
M_B_CAS# 8,13
M_B_WE# 8,13

M_B_CLK0
M_B_CLK0# 7
M_B_CLK1 7
M_B_CLK1# 7
M_B_BS#[0..2] 8,13
M_B_ODT[0..1] 7,13

M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]
M_B_DQM[0..7] 8
M_B_DQ[0..63] 8
M_B_DQS[0..7] 8
M_B_DQS#[0..7] 8
M_B_A[13..0] 8,13

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26A

CKEA 0,1
H 9.2

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24A

CKEB 0,1
H 5.2

SMDDR_VREF_DIMM
SI-1 CHANGE
7,13 PM_EXTTS#0
SB_MA14
M_B_A13
M_B_ODT0
M_B_ODT1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26B

SMDDR_VREF_DIMM
SI-1 CHANGE
7,13 PM_EXTTS#0
SA_MA14
M_A_A13
M_A_ODT0
M_A_ODT1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
SMDDR_VREF_DIMM
R226 0/06
SMDDR_VREF 7,46
R227
1.8VSUS
R603 *10K/F/06
*10K/F/06

DIM2_SA0 R267 10K/04
DIM2_SA1 R268 10K/04
+3V
SMbus address A4

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1
SMbus address A0

Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 .1U/10V/04
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04
SMDDR_VREF_DIMM
C772 .1U/10V/04
C768 2.2U/6.3V/06
+3V
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS
C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 .1U/10V/04
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04
SMDDR_VREF_DIMM
C371 .1U/10V/04
C373 2.2U/6.3V/06
+3V
C372 2.2U/6.3V/06
C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A
Date: Monday, September 11, 2006	Sheet 14 of 48	

YELLOW BLOCK is for G8X chip only

SI-1 modify (change from bead to 0 ohm)

need add to 3v

YELLOW BLOCK is for G8X chip only

FOR G72M/G73M only

OPTION SIGNAL FROM NB FOR UMA VGA

OPTION SIGNAL FROM Nvidia to VGA

C34: PUN issue reserve
U54,C950,c949,R726,R727

Vout=1.25(1+Ra/Rb)

Close to GPU

FOR IFPC VDD LEAKAGE CIRCIUT

SPREAD SPECTRUM

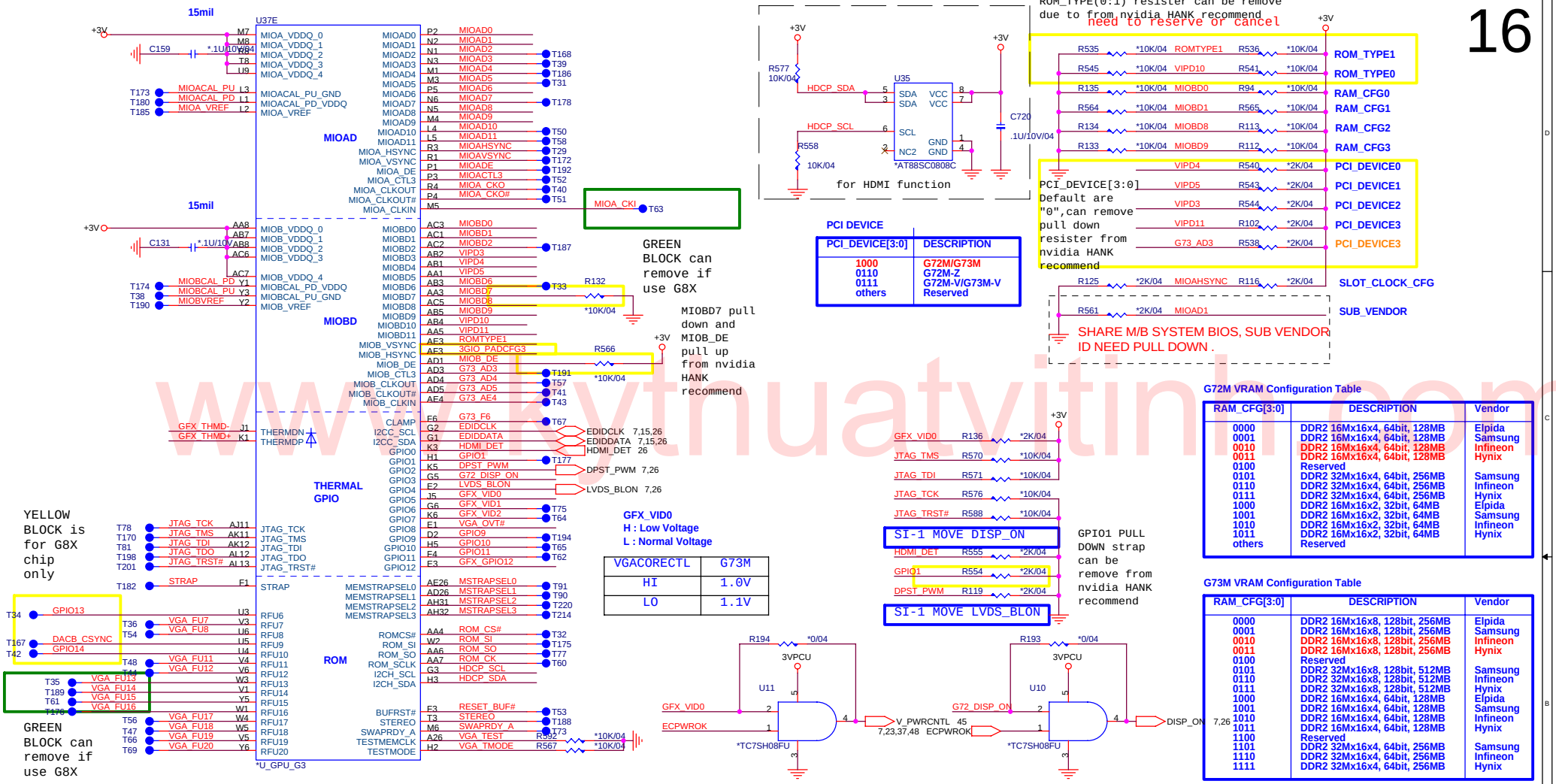
I2C ADDRESS: 0xD4H

PROJECT : AT3
Quanta Computer Inc.

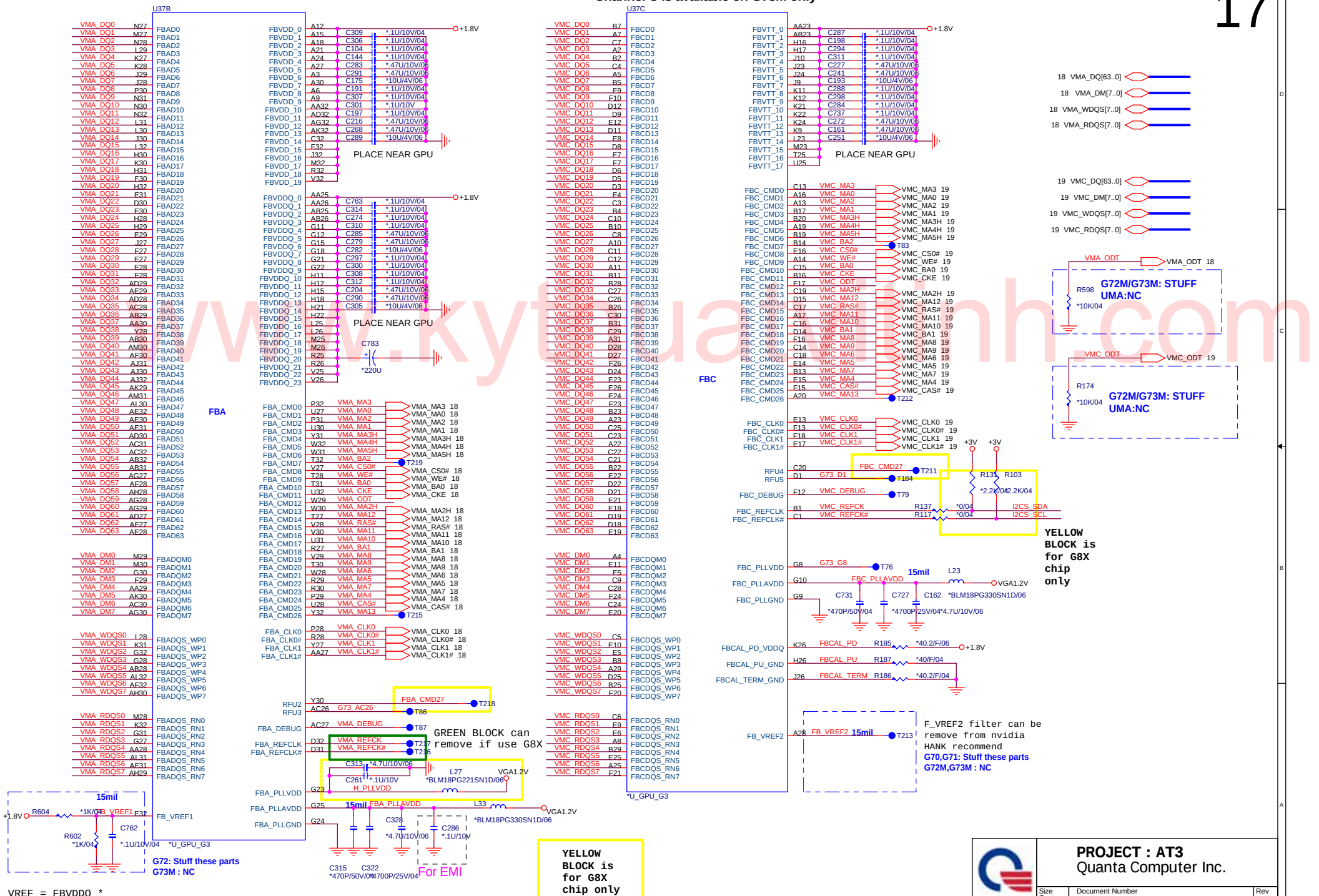
Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A

Date: Monday, September 11, 2006 | Sheet 15 of 48

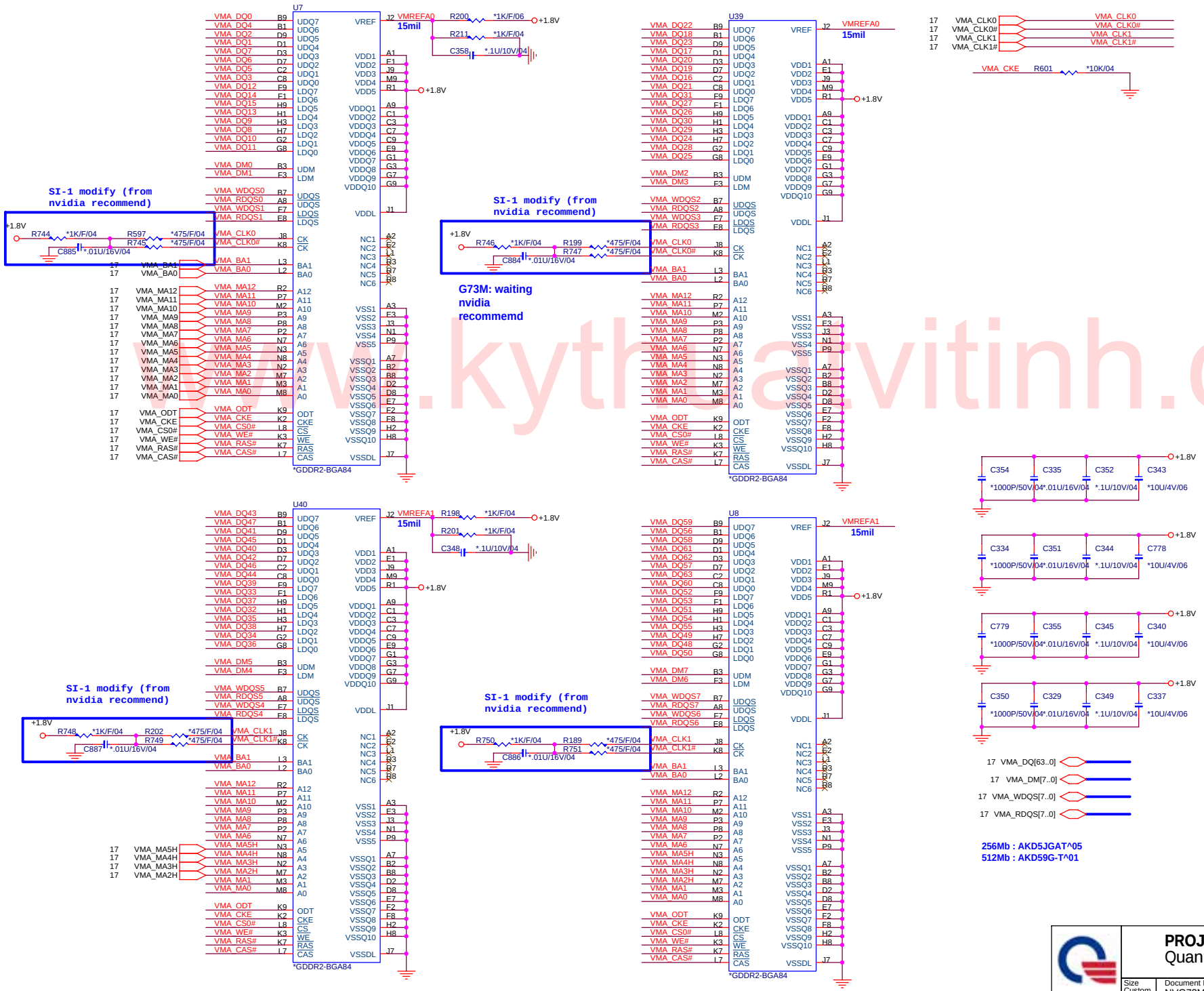
NB5/RD1/HW2



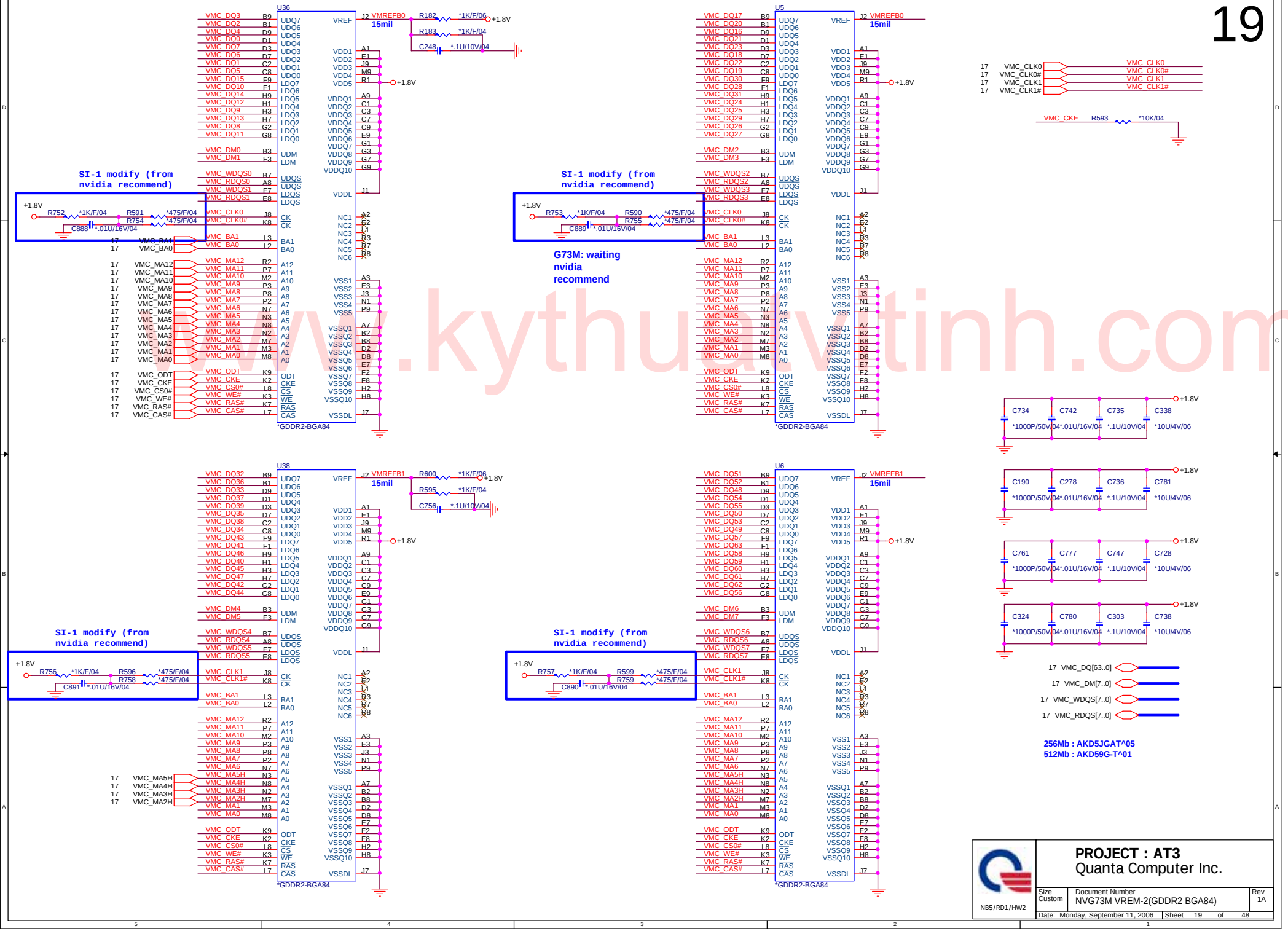
Channel C is available on G73M only

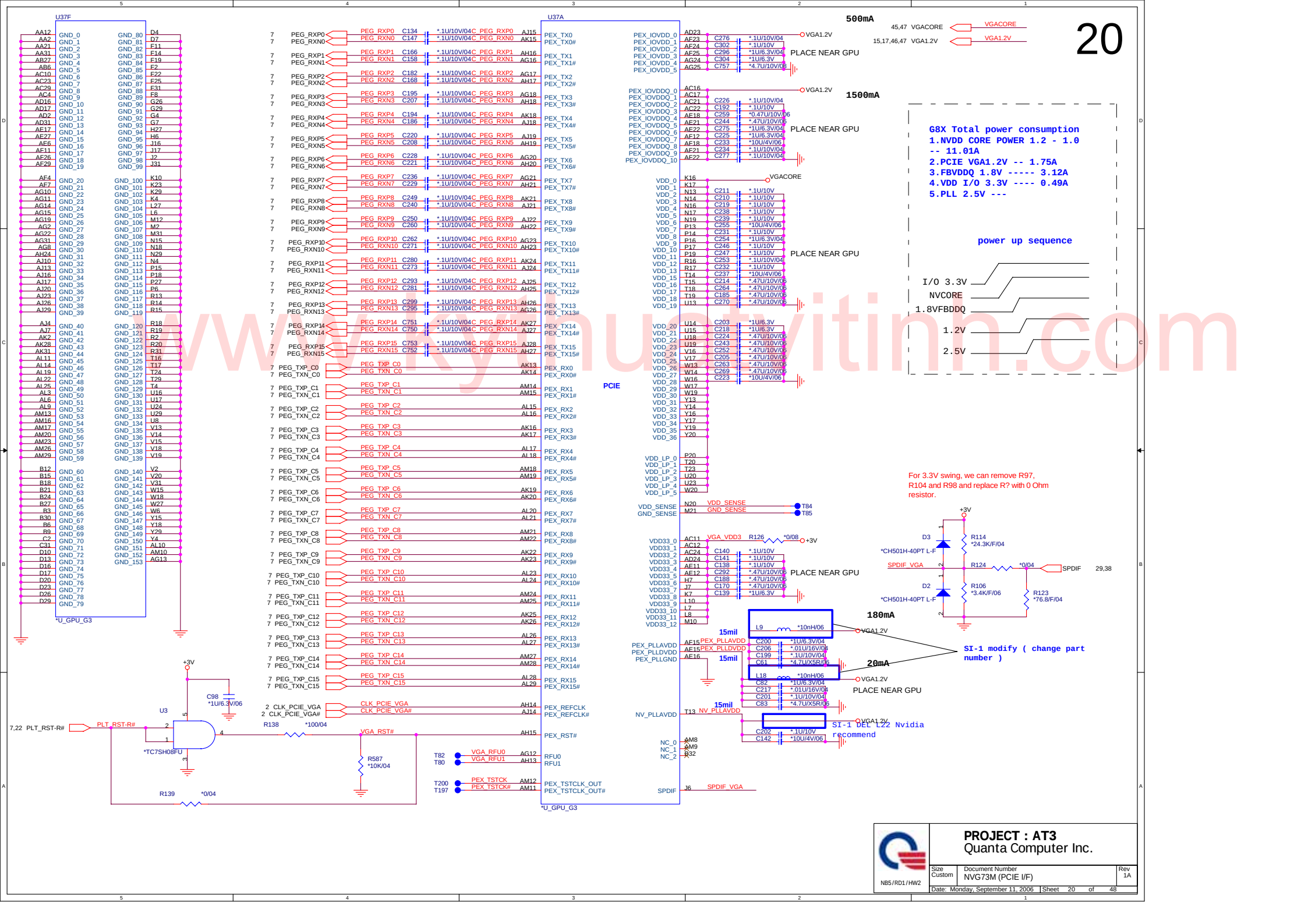


PROJECT : AT3		
Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom	Document Number: NVG73M (MEM I/F)
	Rev: 1A	
	Date: Monday, September 11, 2006	Sheet 17 of 48



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: NVG73M VRAN-1(GDDR2 BGA84)	Rev: 1A
Date: Monday, September 11, 2006	Sheet 18 of 48	

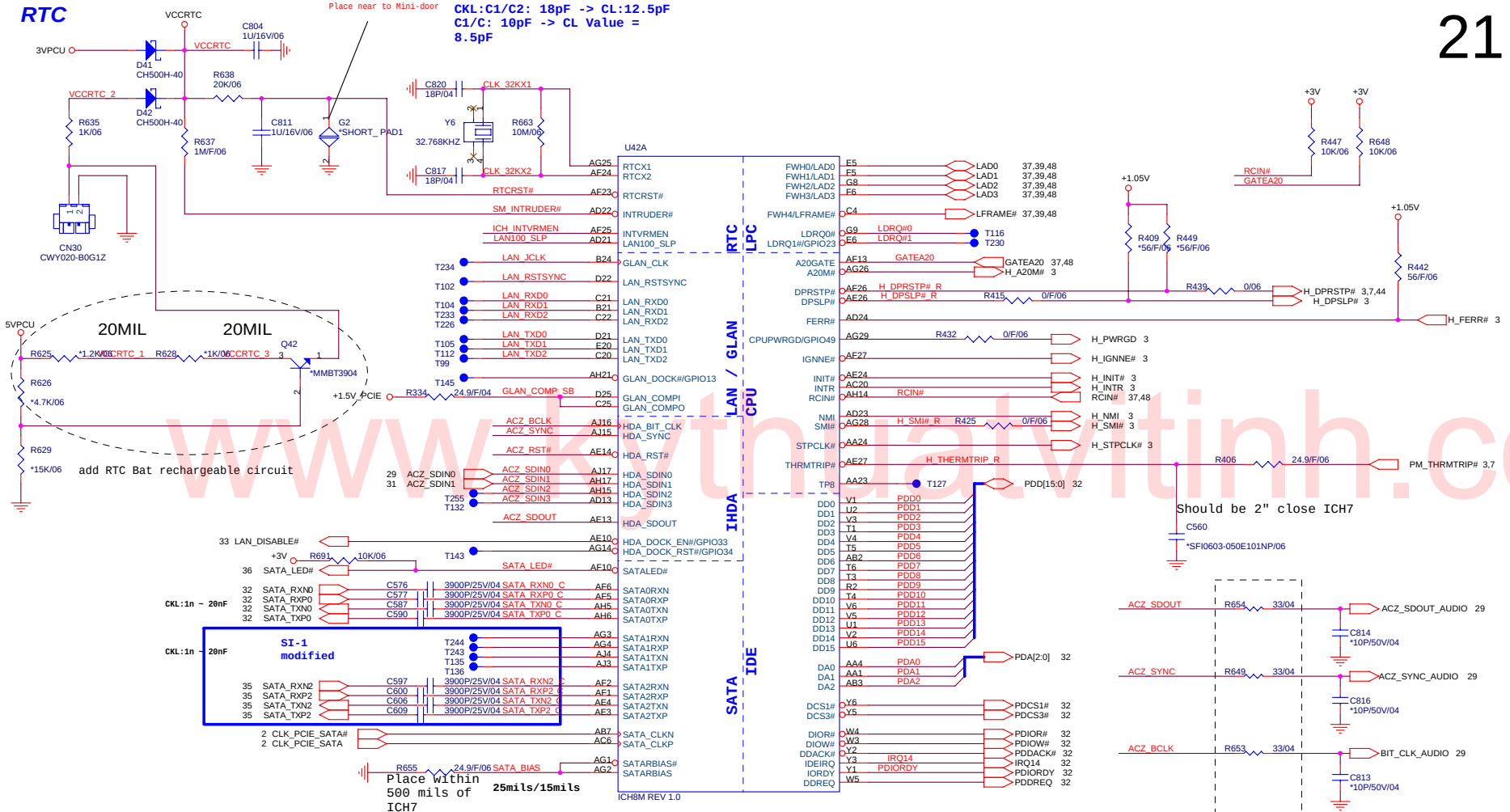




RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

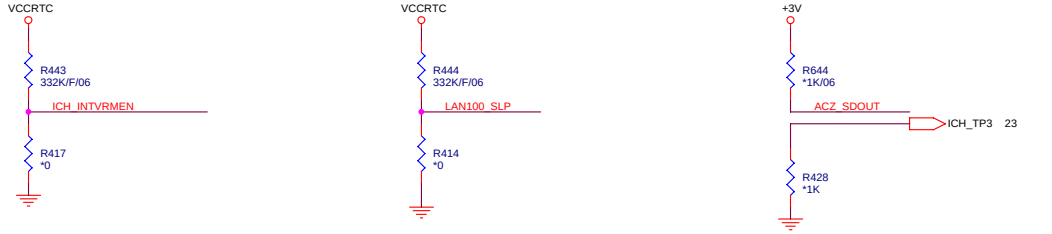
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

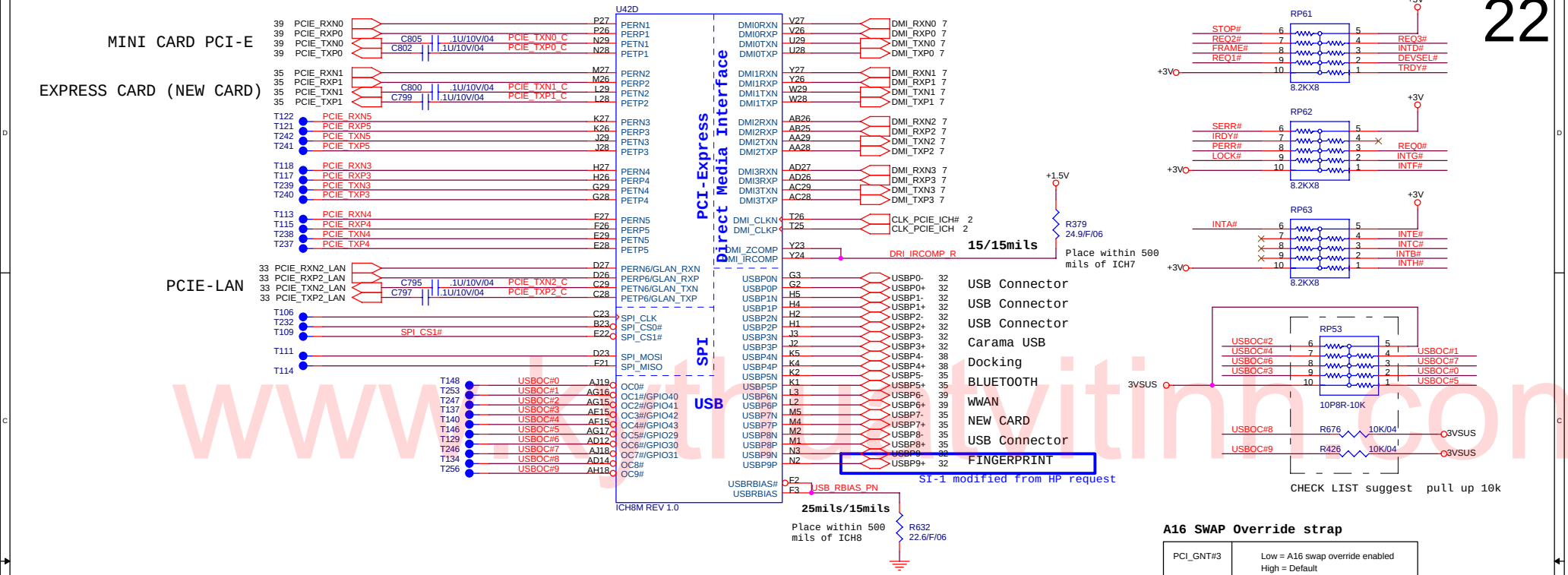


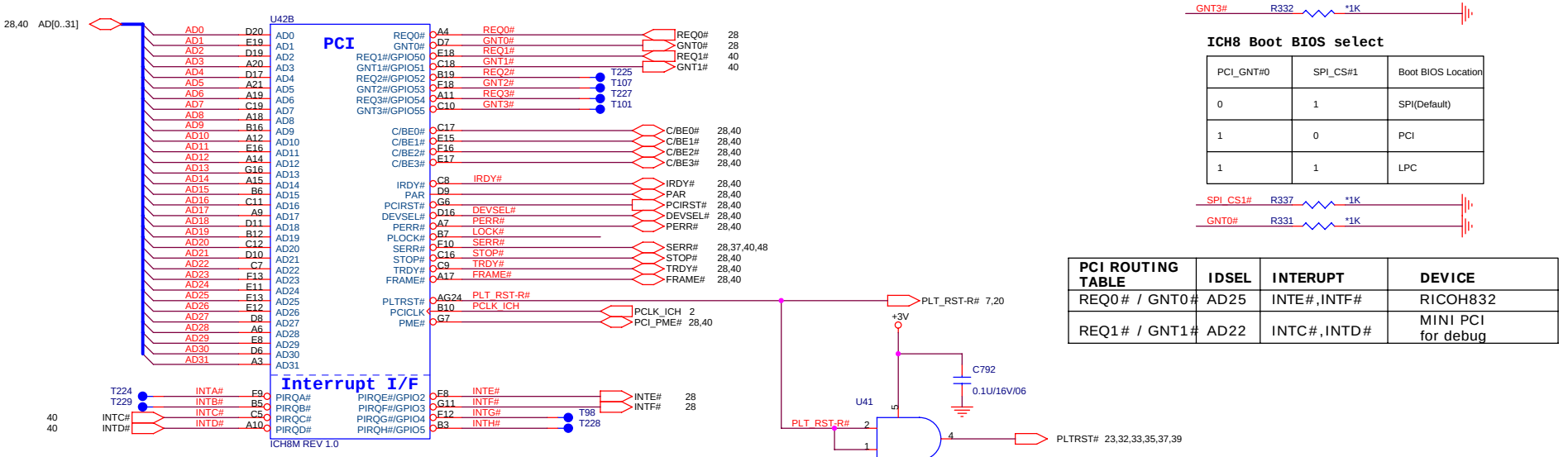
NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.	
Size: Custom	Document Number: ICH7-M HOST(1/4)	Rev: 1A
Date: Monday, September 11, 2006	Sheet 21 of 48	

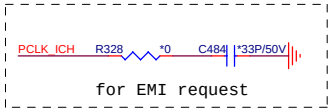
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

PCIE-LAN







A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K

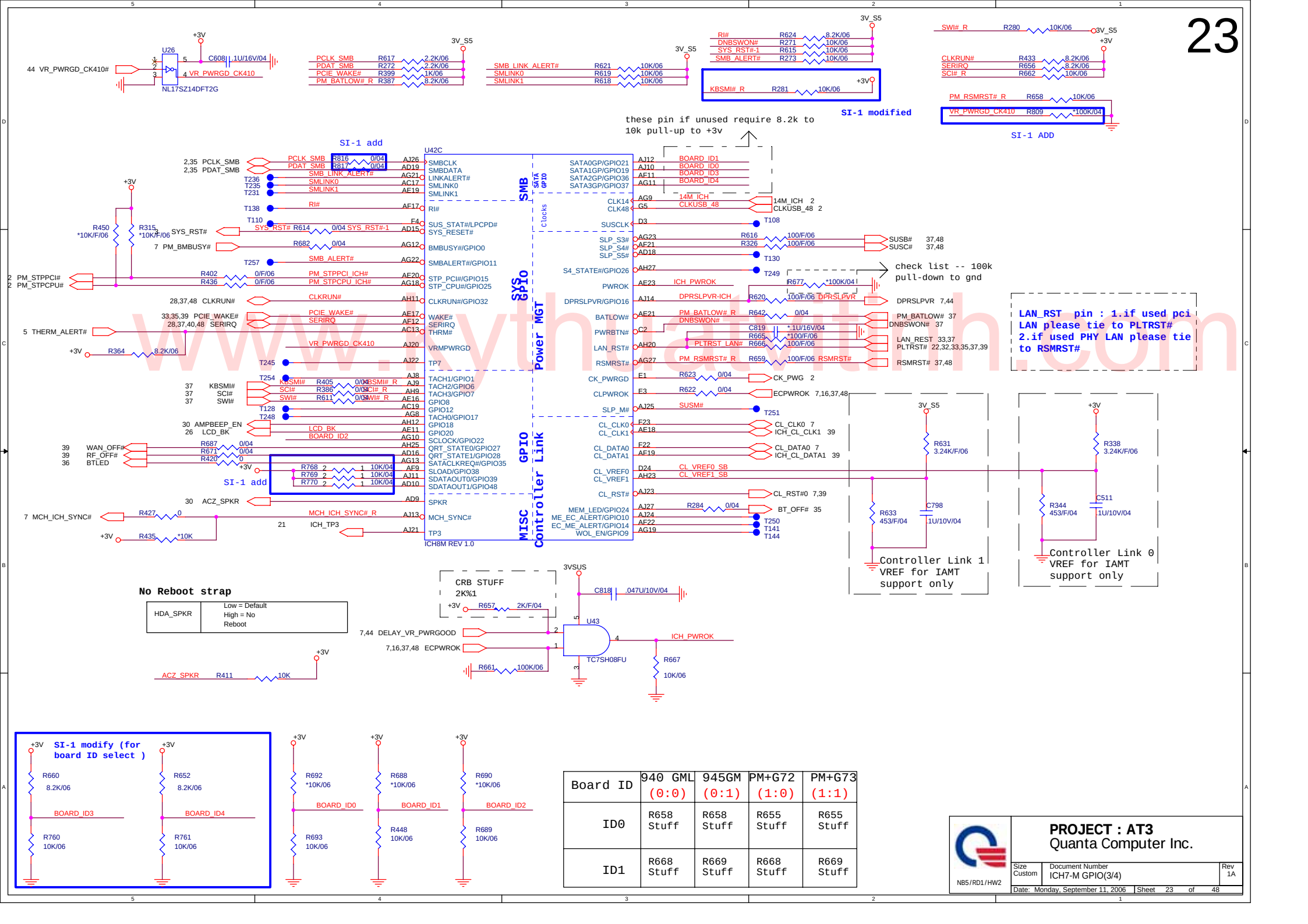
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

NB5/RD1/HW2

Date: Monday, September 11, 2006 Sheet 22 of 48



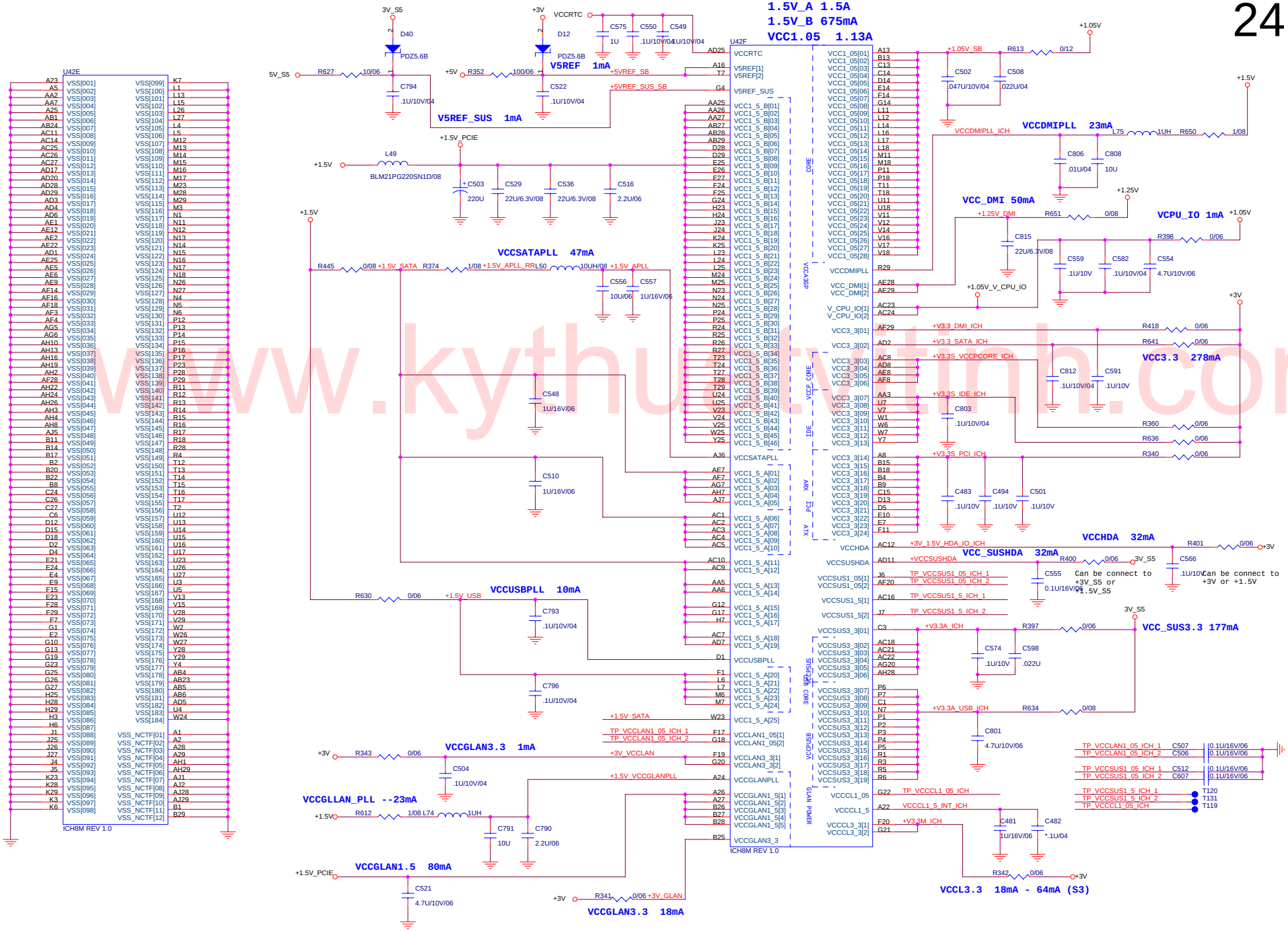
Board ID	940 GML (0:0)	945GM (0:1)	PM+G72 (1:0)	PM+G73 (1:1)
ID0	R658 Stuff	R658 Stuff	R655 Stuff	R655 Stuff
ID1	R668 Stuff	R669 Stuff	R668 Stuff	R669 Stuff

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	ICH7-M GPIO(3/4)	1A

Date: Monday, September 11, 2006 Sheet 23 of 48



NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.	
Size: Custom	Document Number: ICH7-M POWER(4/4)	Rev: 1A
Date: Monday, September 11, 2006	Sheet 24 of 48	

CRT PORT

25

7,15,38 PR_RED
7,15,38 PR_GEN
7,15,38 PR_BLU

SI-1 modified for EMI request

F1 40 mils
FUSE1A6V_POLY SSM14 spec is 40V 1A

5V_CRT2 C7 .1U/10V/04
+5V +5VCRT 40 MIL

CN14 070546FR015S202CR

7,15,38 CRT_R
7,15,38 CRT_G
7,15,38 CRT_B

L60 BK1608HS470/06 CRT_R1
L59 BK1608HS470/06 CRT_G1
L58 BK1608HS470/06 CRT_B1

R496 150/F/04 R495 150/F/04 R492 150/F/04
C649 C647 C645 5.6P/06
C646 C648 C650 5.6P/06

EMI

close conn within 600mils

D30 D27 D26 D23 D24 D25 D29 *BAV99W
CRT_R1 CRT_G1 CRT_B1 DDCCLK2 CRTVSYNC CRTHSYNC DDCDAT2

C27 .1U/10V/04
U30 U29 AHCT1G125DCH

7,15 VSYNC_COM VSYNC1 PR_VSYNC 38
7,15 HSYNC_COM HSYNC1 PR_HSYNC 38

R5 0/04 DDCCLK2
R491 39/04 CRTVSYNC
R490 39/04 CRTHSYNC
R7 0/04 DDCDAT2

C8 C14 C15 C18 *470P/50V/04 *47P/50V/06

R12 2.2K/04 R10 2.2K/04
7,15 DDCCLK DDCCLK DDCCLK2 38
7,15 DDCDATA DDCDATA DDCDAT2 38
Q2 Q1 2N7002E

R4 2.2K/04 R494 2.2K/04
+5VCRT +5V_CRT2
CH501H-40PT L-F D22

38 S-CVBS-DO
38 S-YD-DO
38 S-CD-DO

filter for HDTV

C870 C871 C872 8.2P/50V/06
L1 L3 L2 0.56uH/08
SI-1 MODIFY

7,15 S-CD1 S-CD
7,15 S-YD1 S-YD
7,15 S-CVBS1 S-CVBS

R1 R489 R486 150/F/04
C642 C643 C641 82P/04
C640 C2 C1 82P/X7R/04

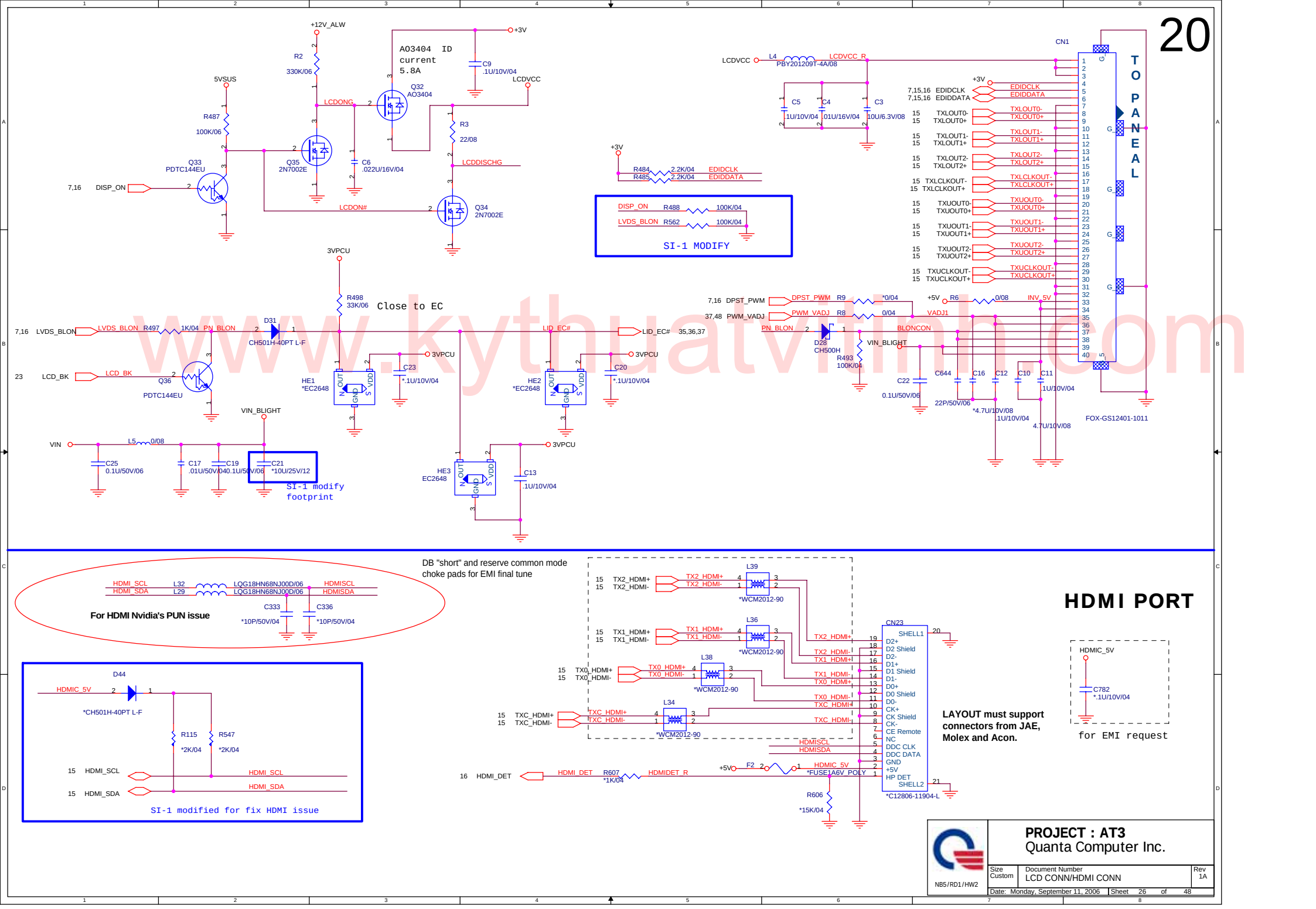
TV_CHROMA TV_LUMA TV_COMP

TV_OUT

CN13 SUY-030005FR007S102FU

D19 D21 D20 *BAV99W
TV_CHROMA TV_LUMA TV_COMP

NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.	
	Size: Custom Document Number: CRT/TV_OUT	Rev: 1A
	Date: Monday, September 11, 2006	Sheet 25 of 48



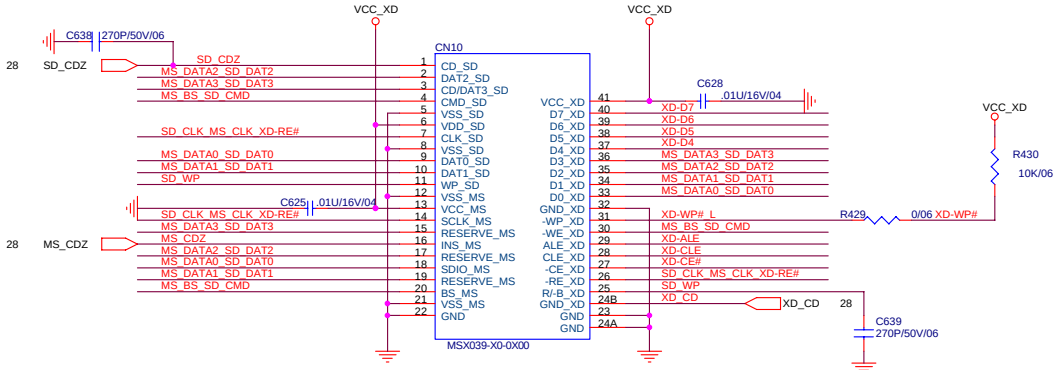
HDMI PORT

DB "short" and reserve common mode choke pads for EMI final tune

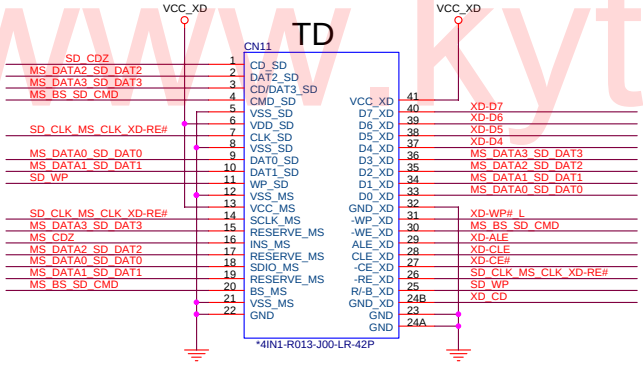
LAYOUT must support connectors from JAE, Molex and Acon.

PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	Size: Custom; Document Number: LCD CONN/HDMI CONN; Rev: 1A
Date: Monday, September 11, 2006	Sheet 26 of 48

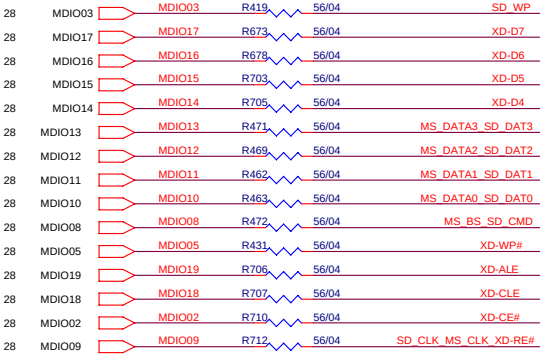
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

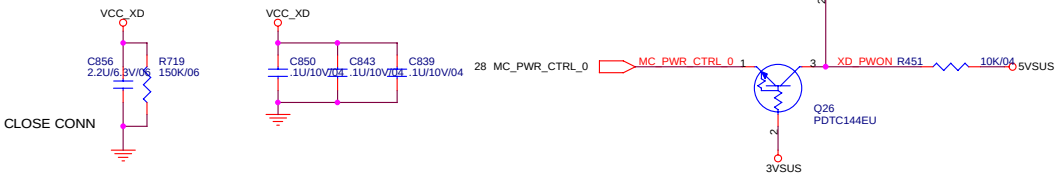


TD

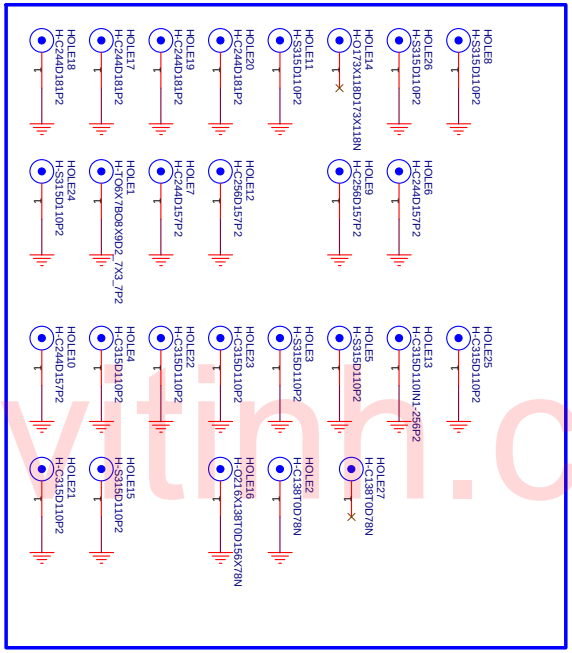


bom create 2'nd source

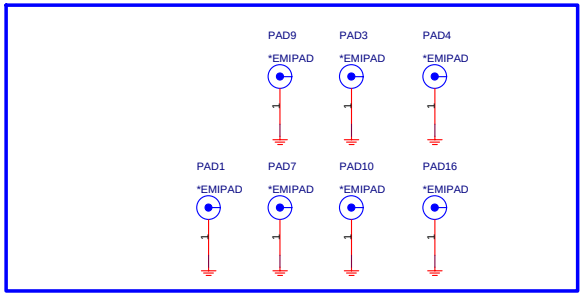




SCREW HOLE



EMI PAD



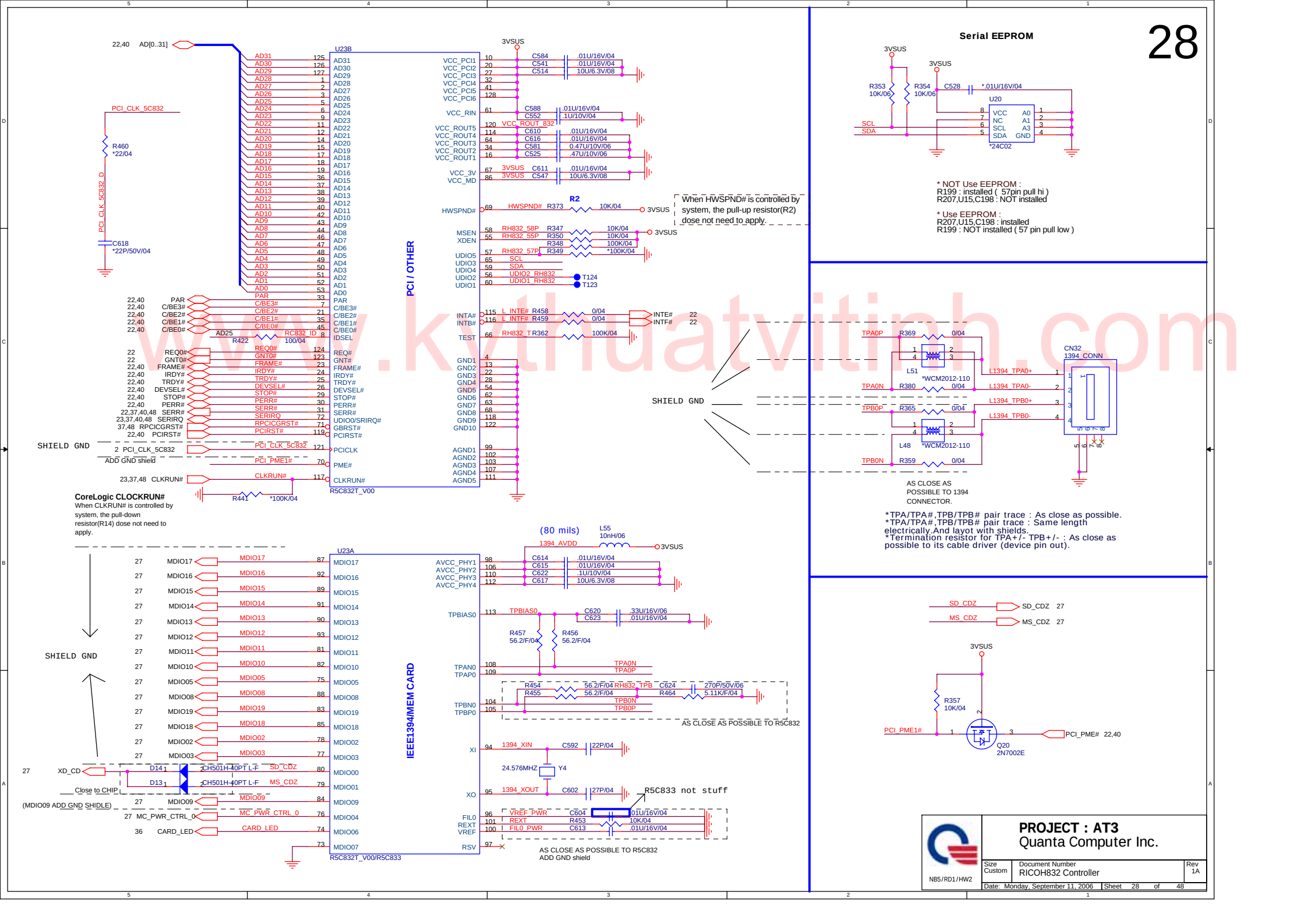
moden cable sprig

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	CARD READER/HOLE	1A

Date: Monday, September 11, 2006 Sheet 27 of 48



Serial EEPROM

* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)

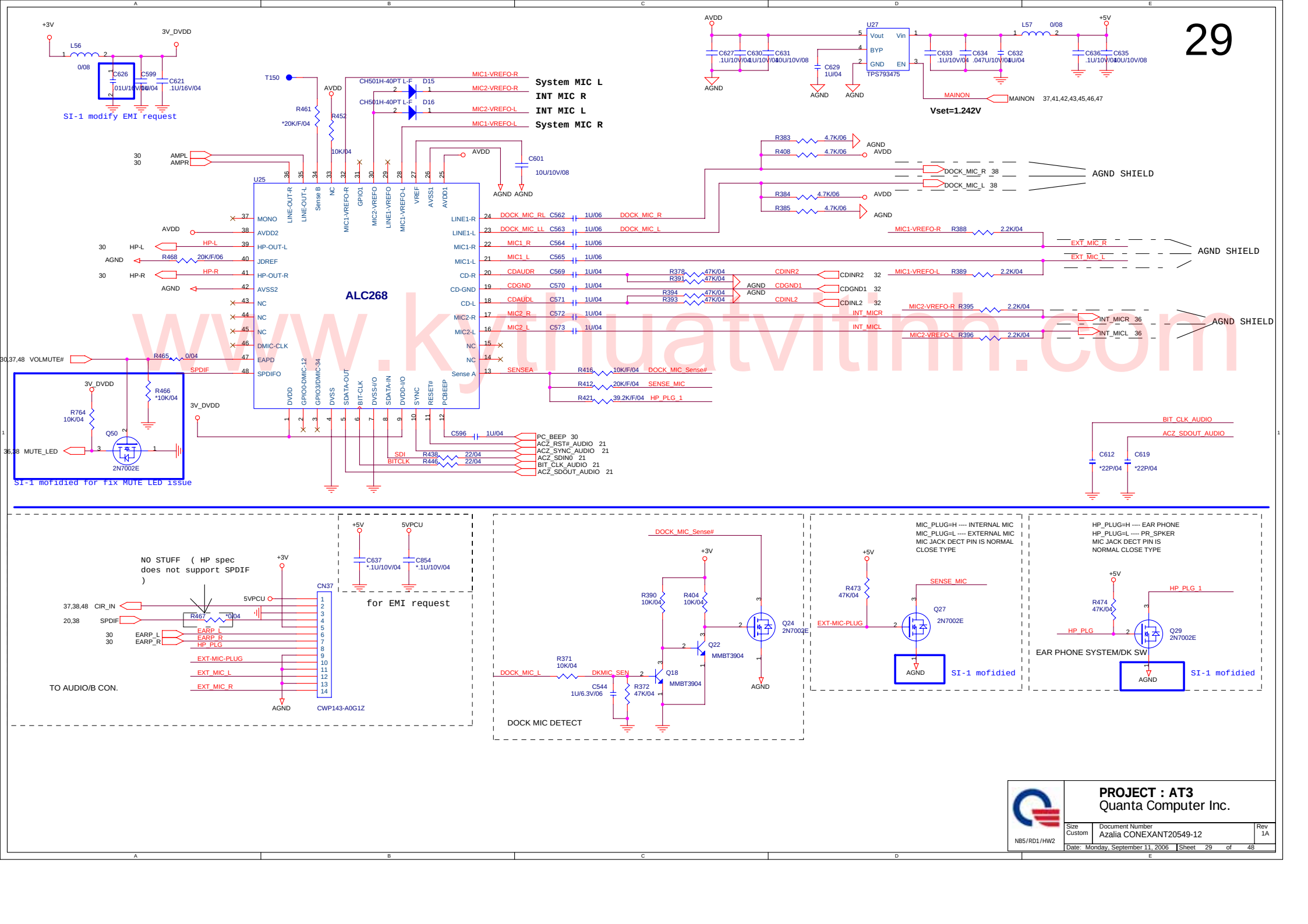
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RICOH832 Controller	1A

NB5/RD1/HW2

Date: Monday, September 11, 2006 Sheet 28 of 48



PROJECT : AT3
Quanta Computer Inc.

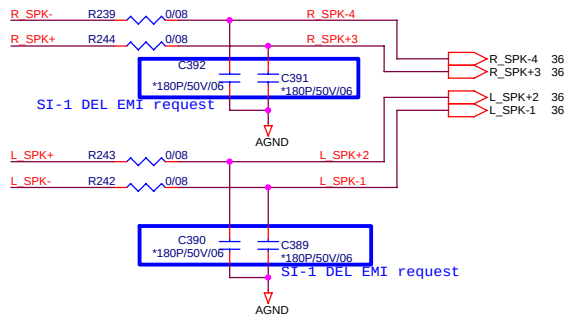
Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	1A

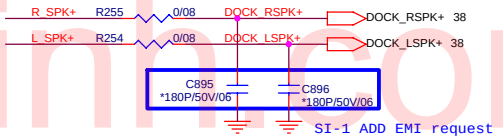
NB5/RD1/HW2

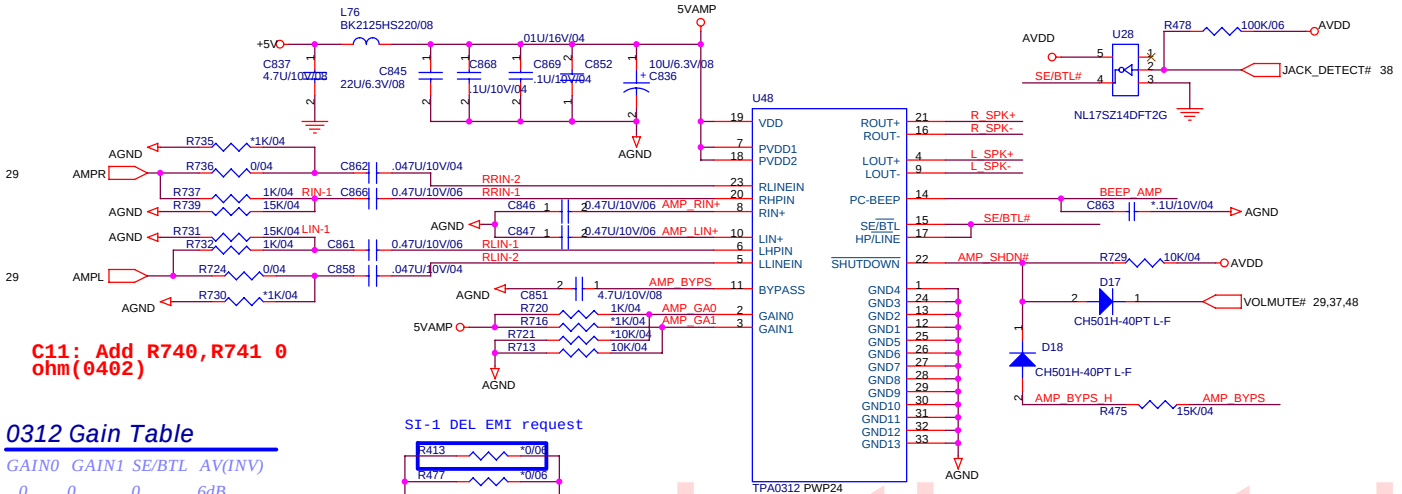
Date: Monday, September 11, 2006 Sheet 29 of 48

AUDIO AMPLIFIER

INT. SPEAKER

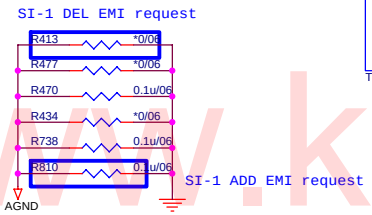




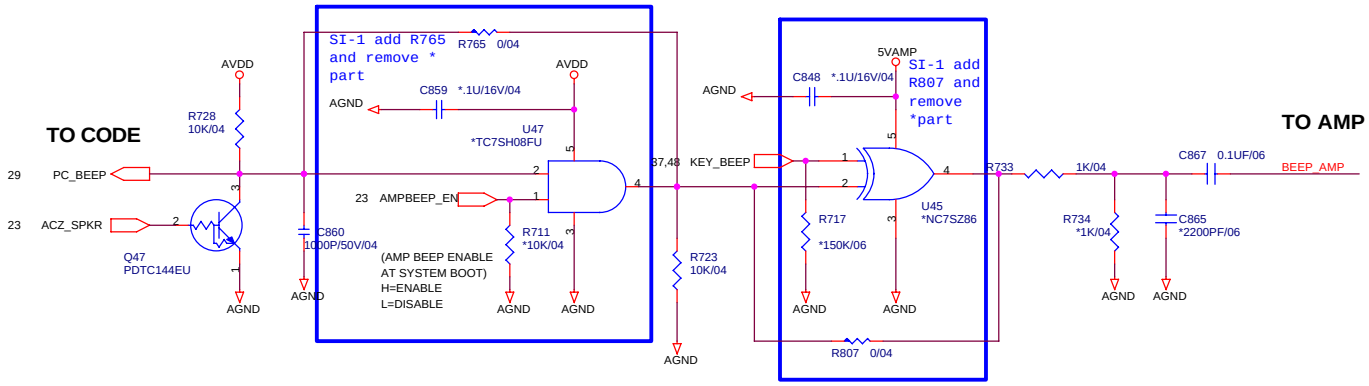


0312 Gain Table

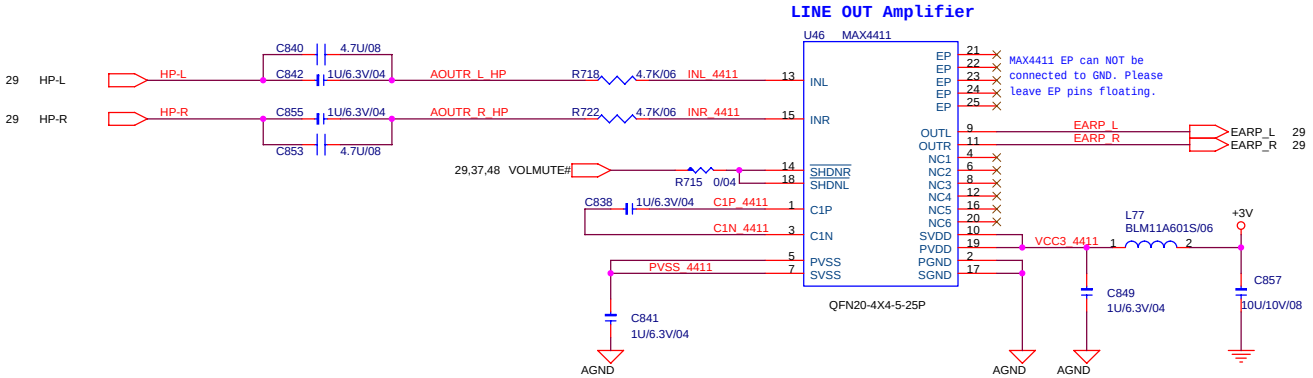
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



PCSPK BEEP



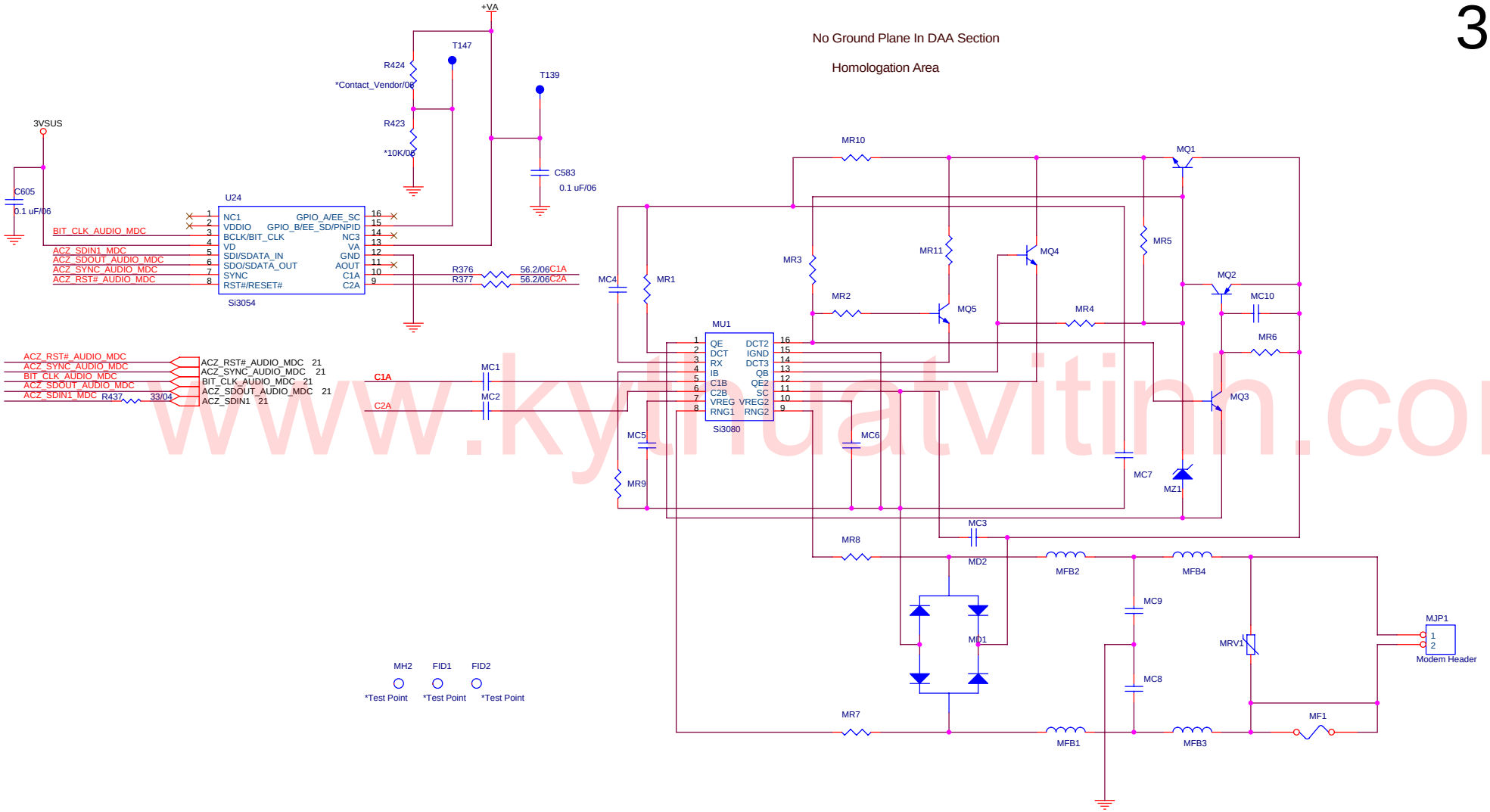
LINE OUT Amplifier



PROJECT : AT3	Quanta Computer Inc.
Size: Custom	Document Number: JACK/AMP_TAP0312
Rev: 1A	
NB5/RD1/HW2	Date: Monday, September 11, 2006 Sheet 30 of 48

No Ground Plane In DAA Section

Homologation Area



DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

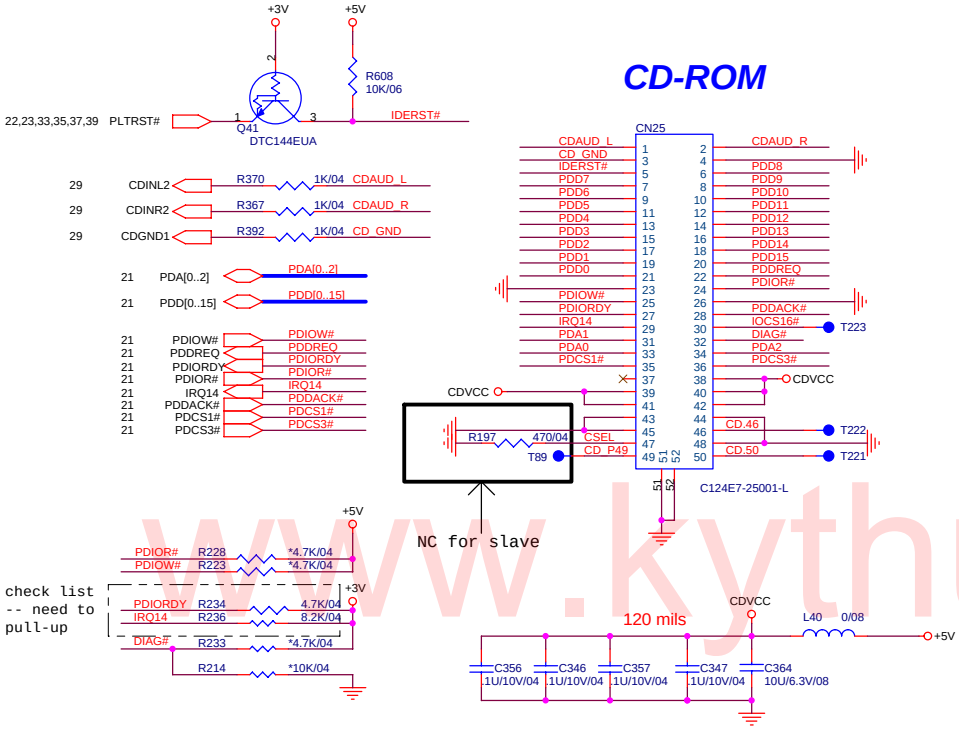
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(DAA)	1A

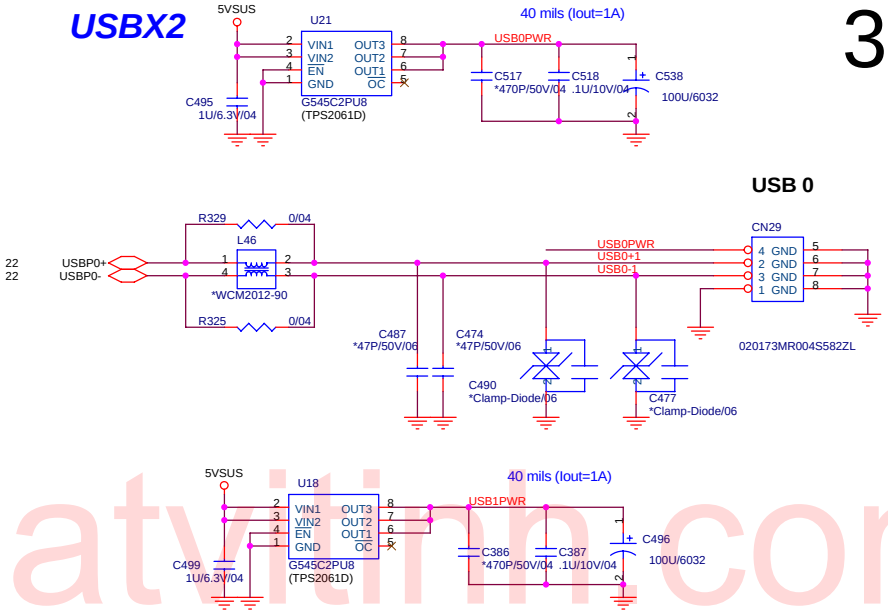
NB5/RD1/HW2

Date: Monday, September 11, 2006 Sheet 31 of 48

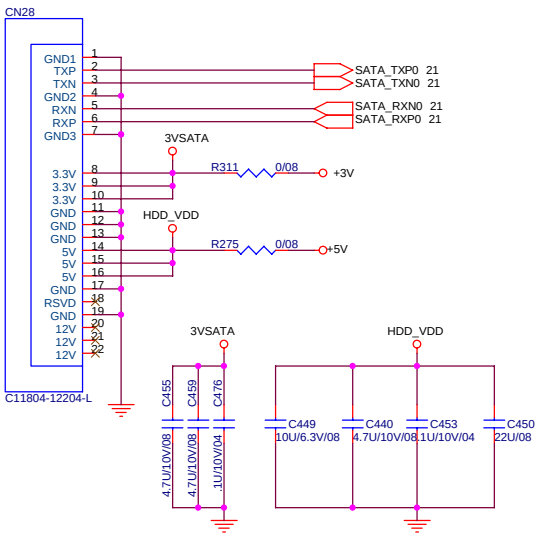
CD-ROM



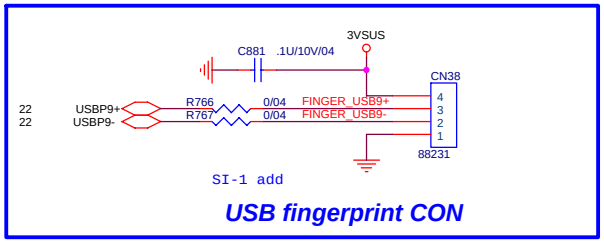
USBX2



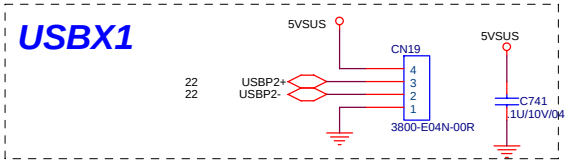
SATA_1 CONNECTOR



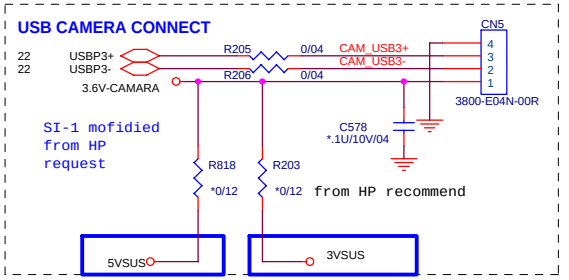
USB fingerprint CON

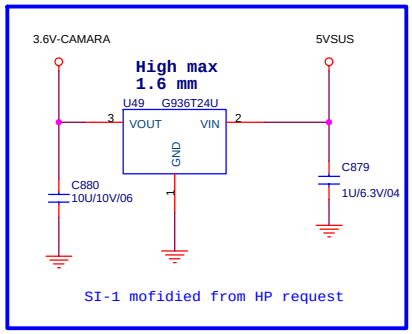


USBX1



USB CAMERA CONNECT





PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A
NB5/RD1/HW2	Date: Monday, September 11, 2006	Sheet 32 of 48

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix
10/100 LAN LED issue

R345 0/04

for 93C56 used. NC if 93C46 is used.

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

U19 RTL8111B/8111C/8101E

U22 93C46-3GR

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

BLOCK A is only for RTL8101E application.

Block A

RJ45

SI-1 modified to fix giga LAN LED issue

Remove R70 for 8111B and 8111C

U14 NS892403/2404

NS892403:GIGABIT

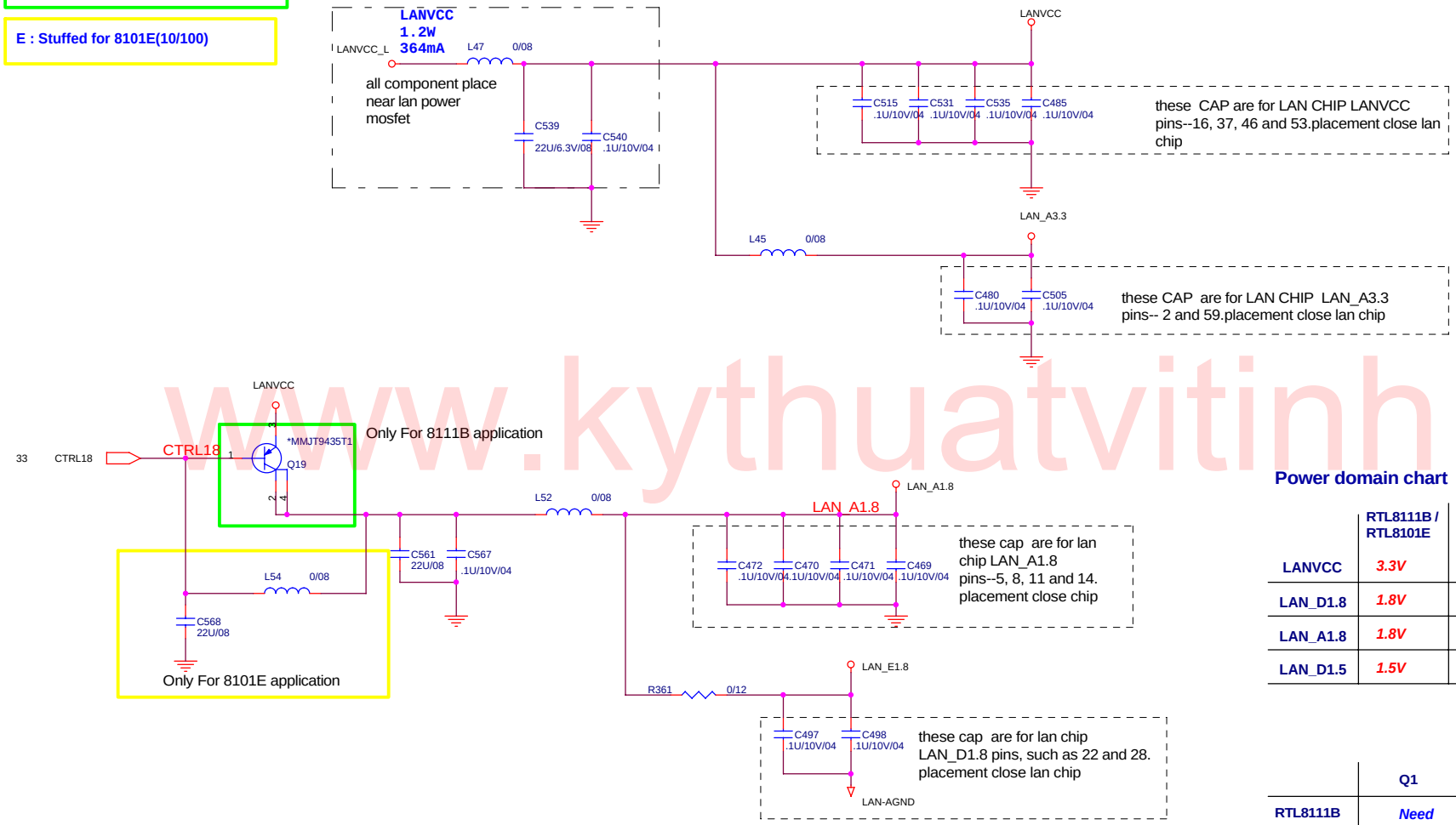
NS892405:10/100

close U6

NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.	
Size: Custom	Document Number: RTL8111B/8111C/8101E	Rev: 1A
Date: Monday, September 11, 2006	Sheet 33 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E	
LANVCC	3.3V	
LAN_D1.8	1.8V	
LAN_A1.8	1.8V	
LAN_D1.5	1.5V	

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

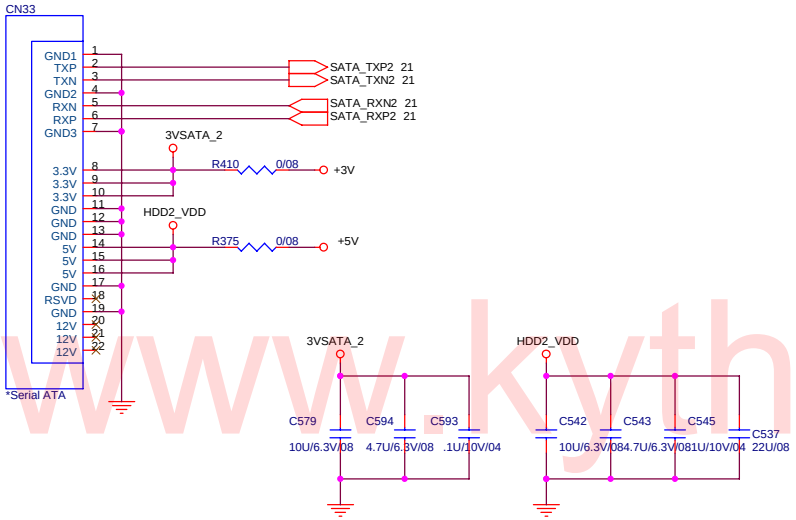
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

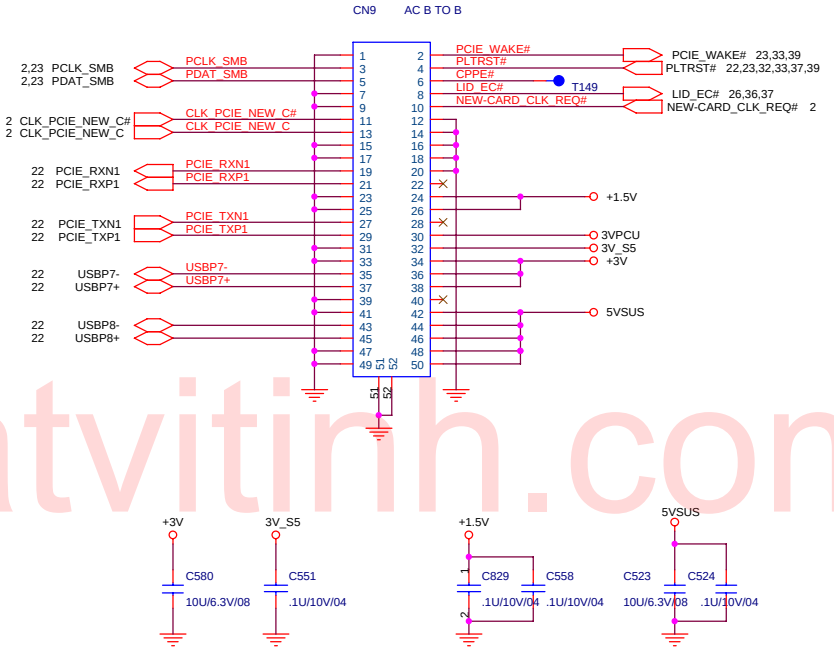
NB5/RD1/HW2

Date: Monday, September 11, 2006 Sheet 34 of 48

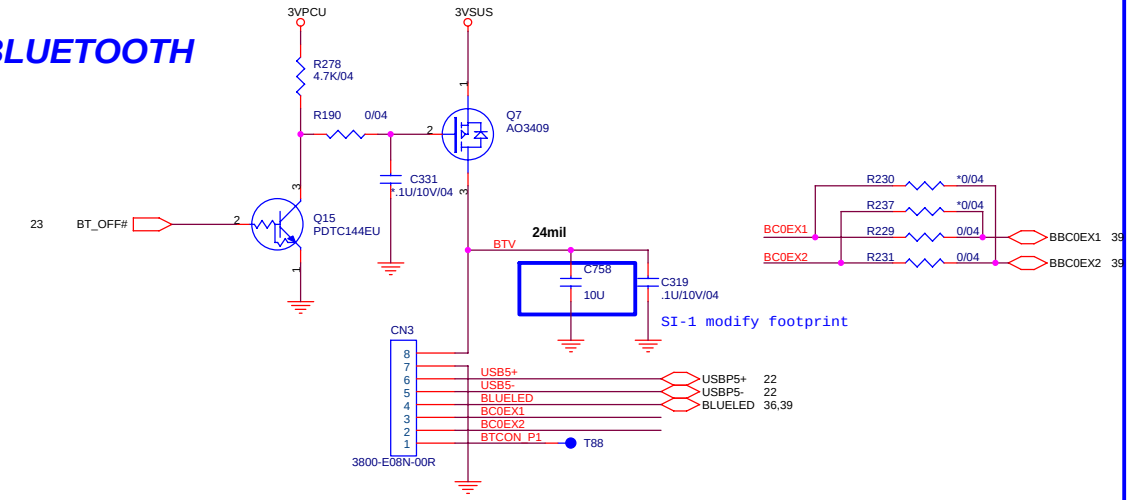
SATA_2 CONNECTOR
For 17"W Second HDD

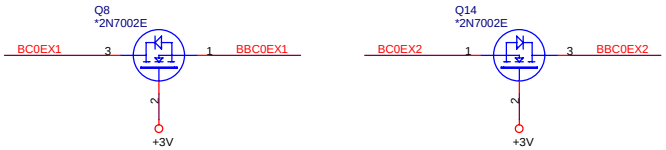


NEWCARD



BLUETOOTH



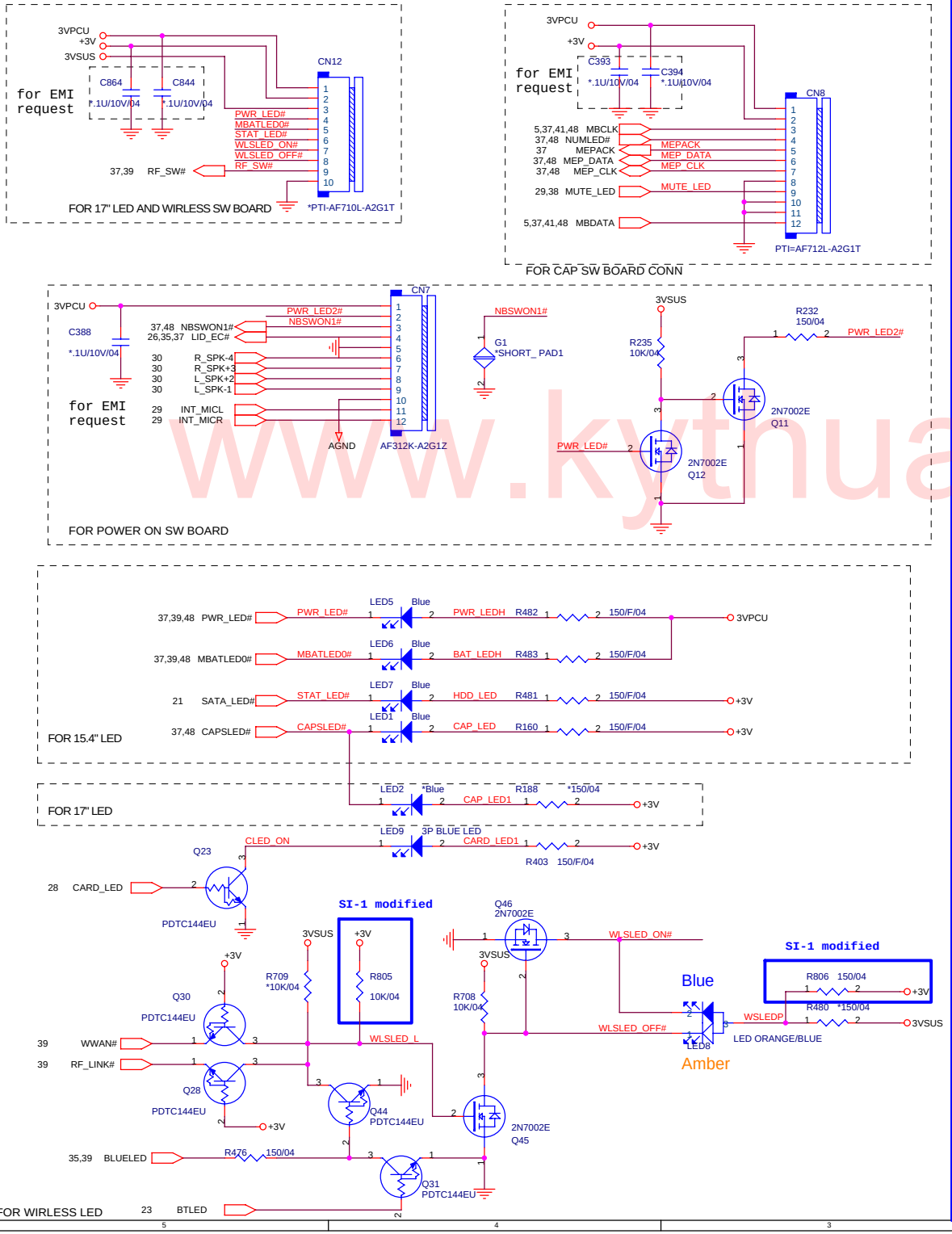


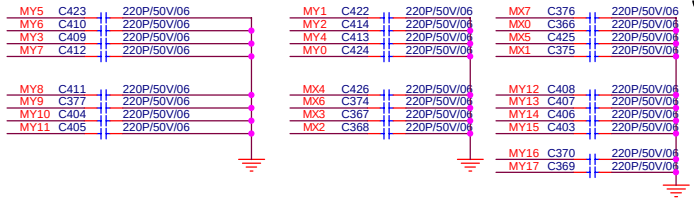
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	1A

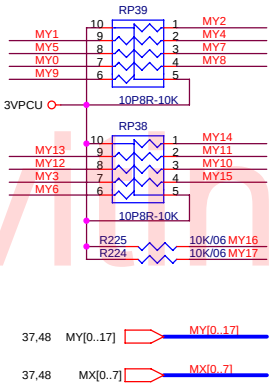
NB5/RD1/HW2

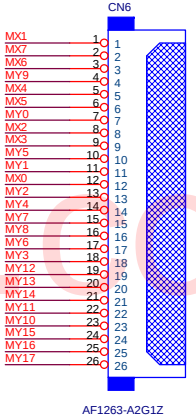
Date: Monday, September 11, 2006 | Sheet 35 of 48

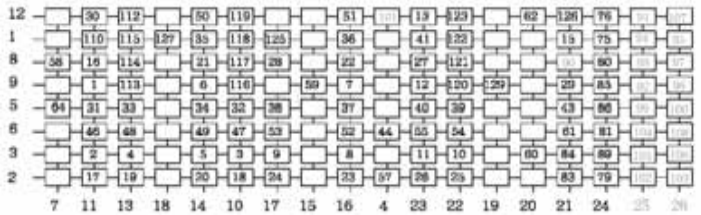




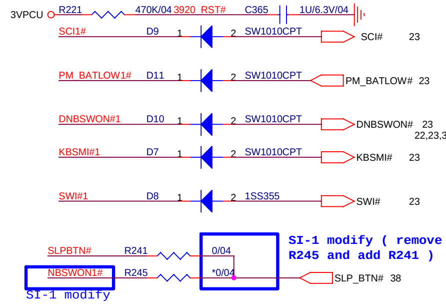
KEYBOARD PULL-UP



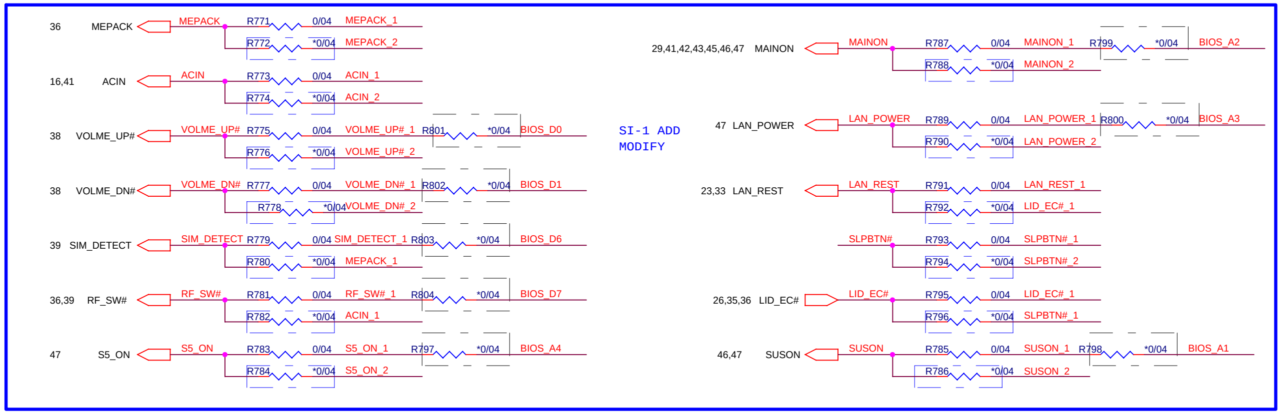




NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: LED/KEYBOARD/SW	Rev: 1A
Date: Monday, September 11, 2006	Sheet 36 of 48	

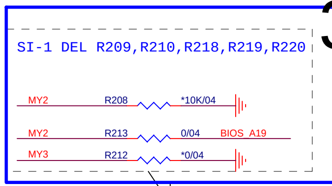


PIN NAME	USE KB3920 ISA_BUS BIOS	USE KB3920/KB3926 SPI BIOS
MEPACK	R772	R771
ACIN	R774	R773
VOLME_UP#	R776 R801	R775
VOLME_DN#	R778 R802	R777
SIM_DETECT	R780 R803	R779
RF_SW#	R782 R804	R781
S5_ON	R784 R797	R783
SUSON	R786 R798	R785
MAINON	R788 R799	R787
LAN_POWER	R790 R800	R789
LAN_REST	R792	R791
LID_EC#	R796	R795
SLPBTN#	R794	R793



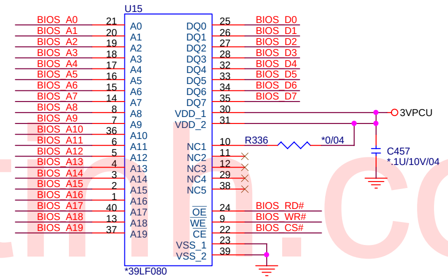
STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

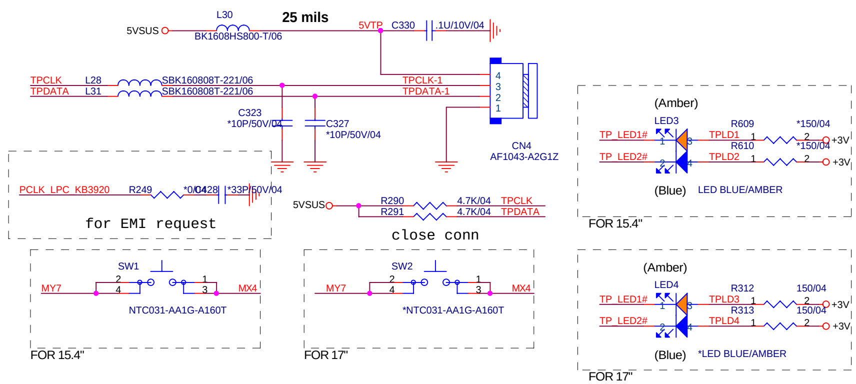


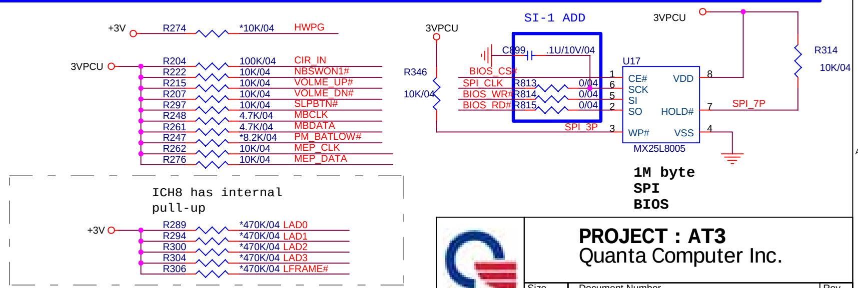
All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

BIOS 1M FLASH ROM



TOUCH PAD CONNECTOR





1M byte SPI BIOS

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3920/ROM/TP	1A

NB5/RD1/HW2

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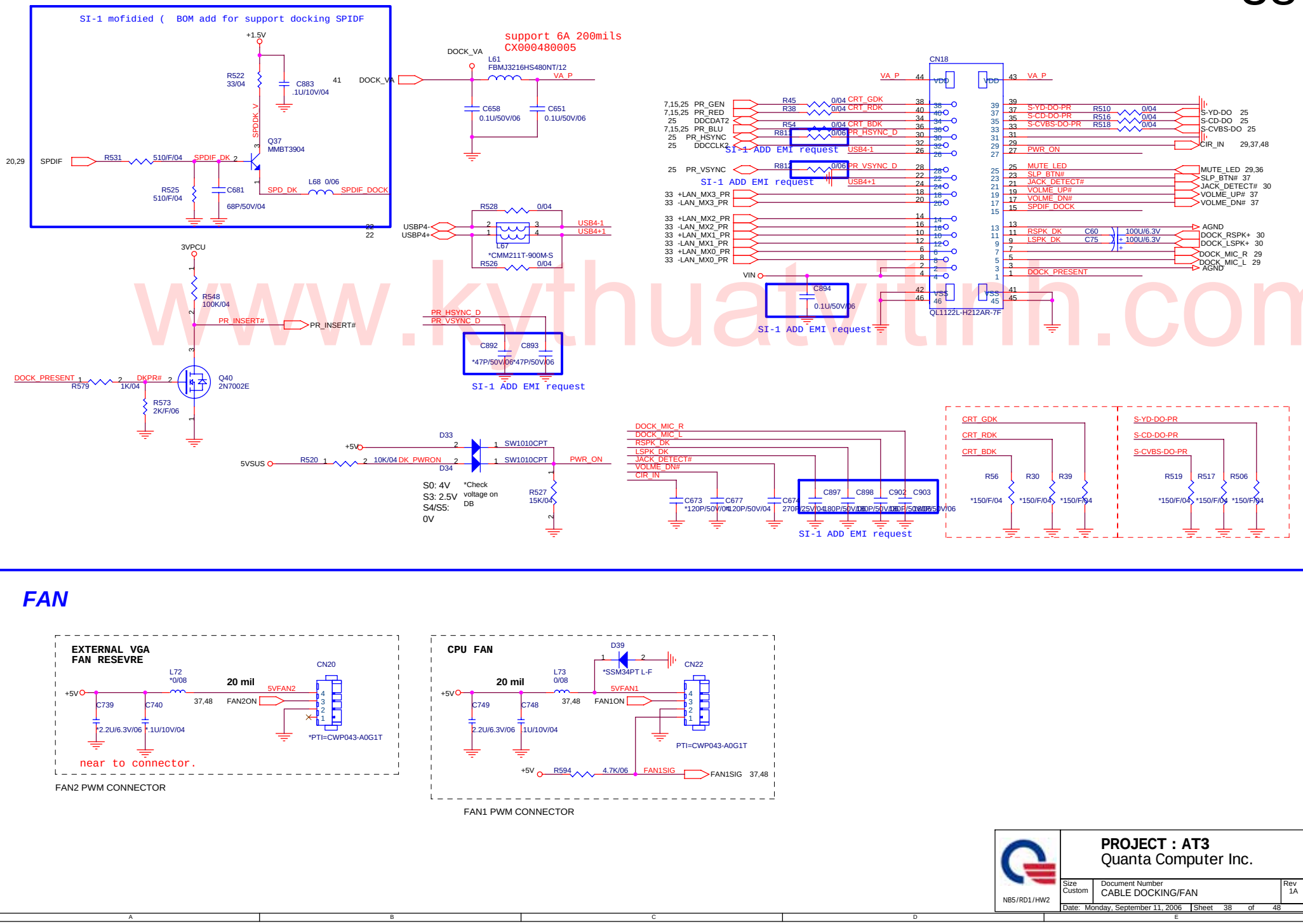
CABLE DOCK



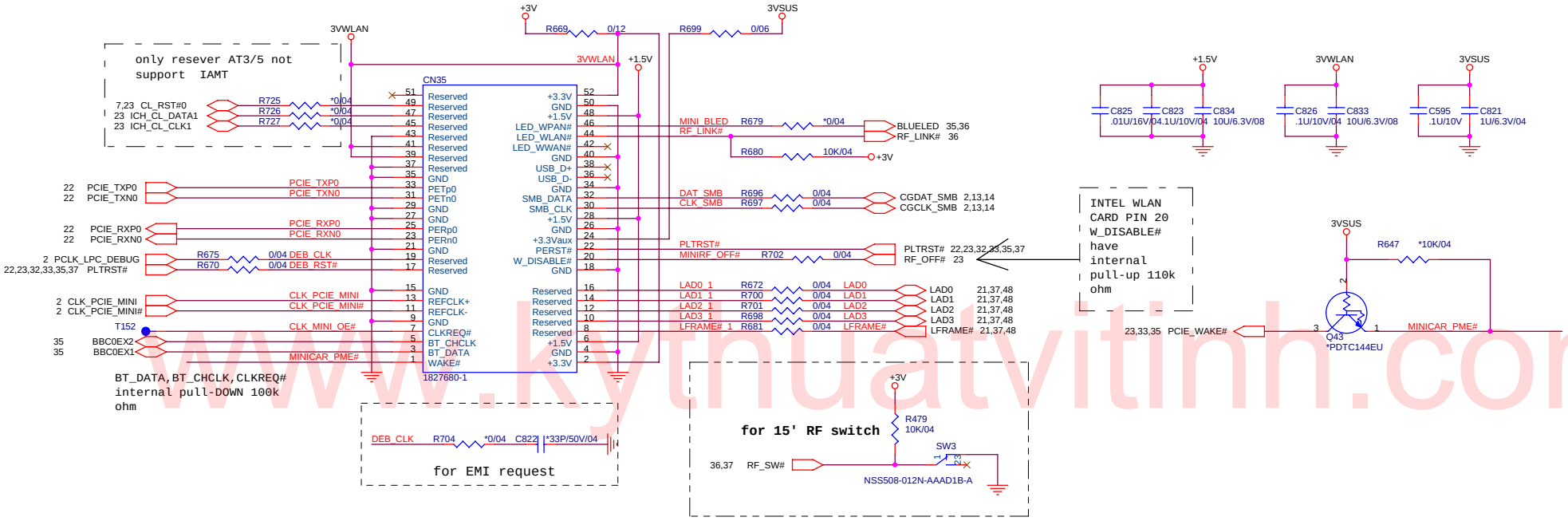
FAN

FAN2 PWM CONNECTOR

FAN1 PWM CONNECTOR

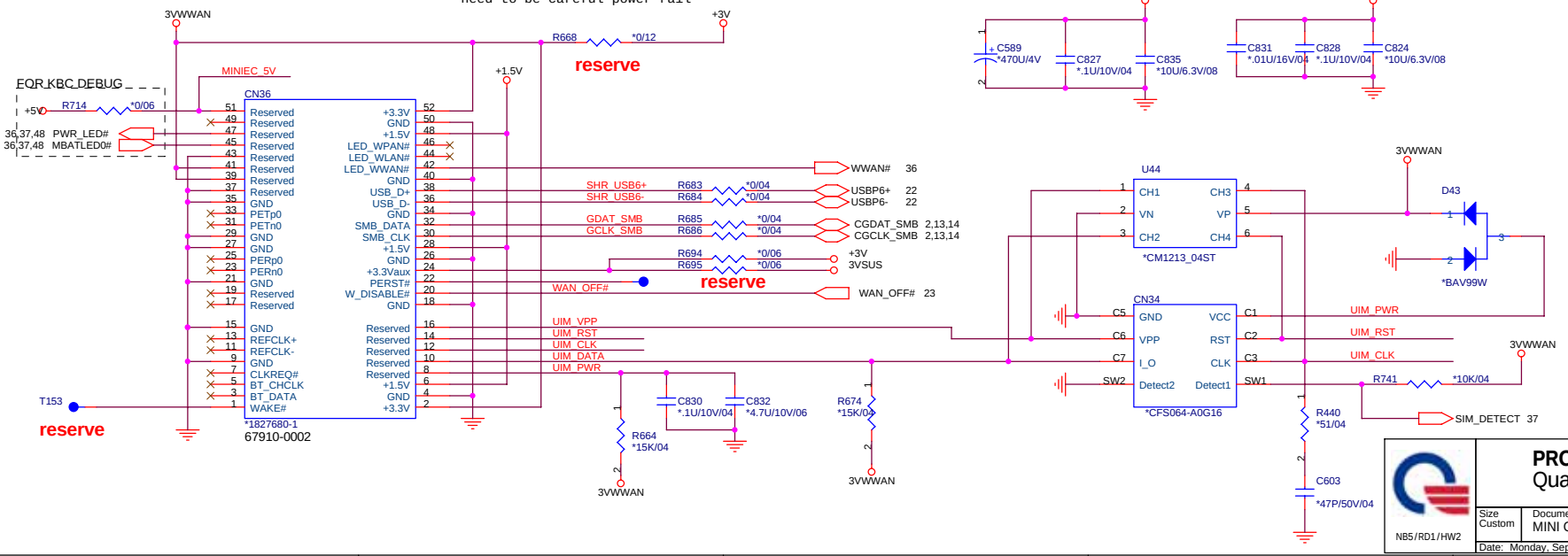
NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: CABLE DOCKING/FAN	Rev: 1A
Date: Monday, September 11, 2006	Sheet 38 of 48	

Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

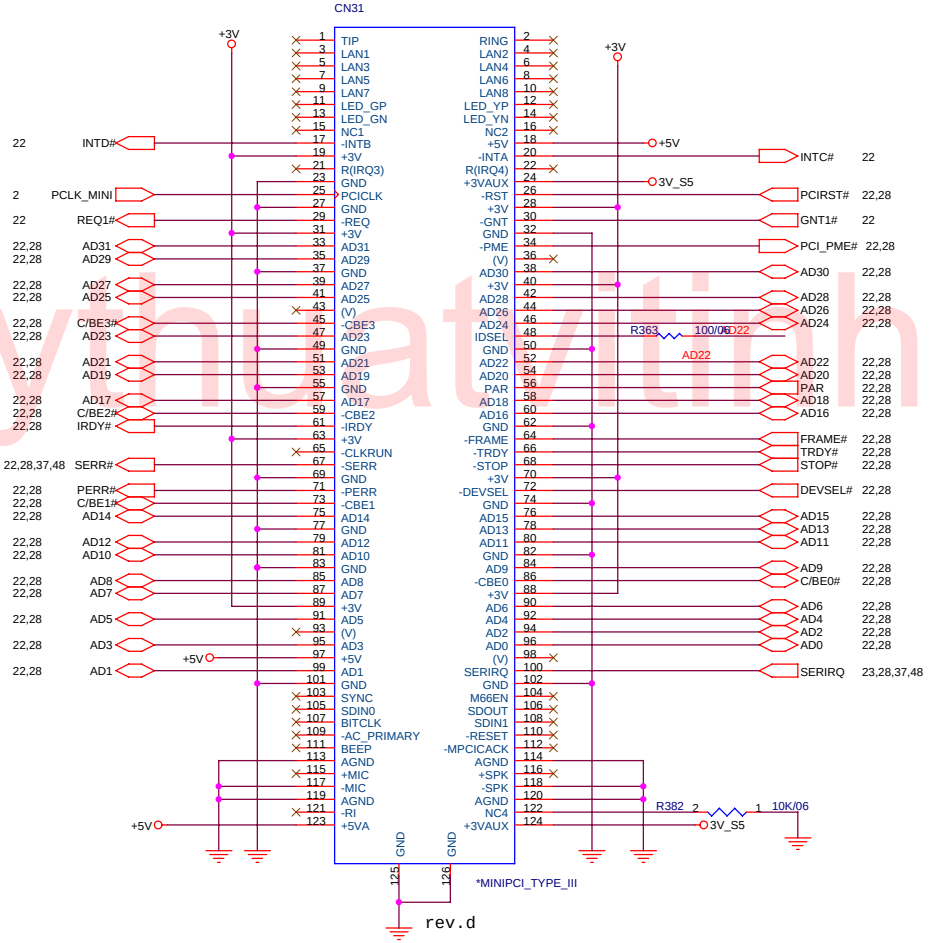
WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail



PROJECT : AT3		
Quanta Computer Inc.		
Size: Custom	Document Number: MINI CARD X2	Rev: 1A
NB5/RD1/HW2	Date: Monday, September 11, 2006	Sheet 39 of 48

MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI TYPE III SLOT	Rev: 1A
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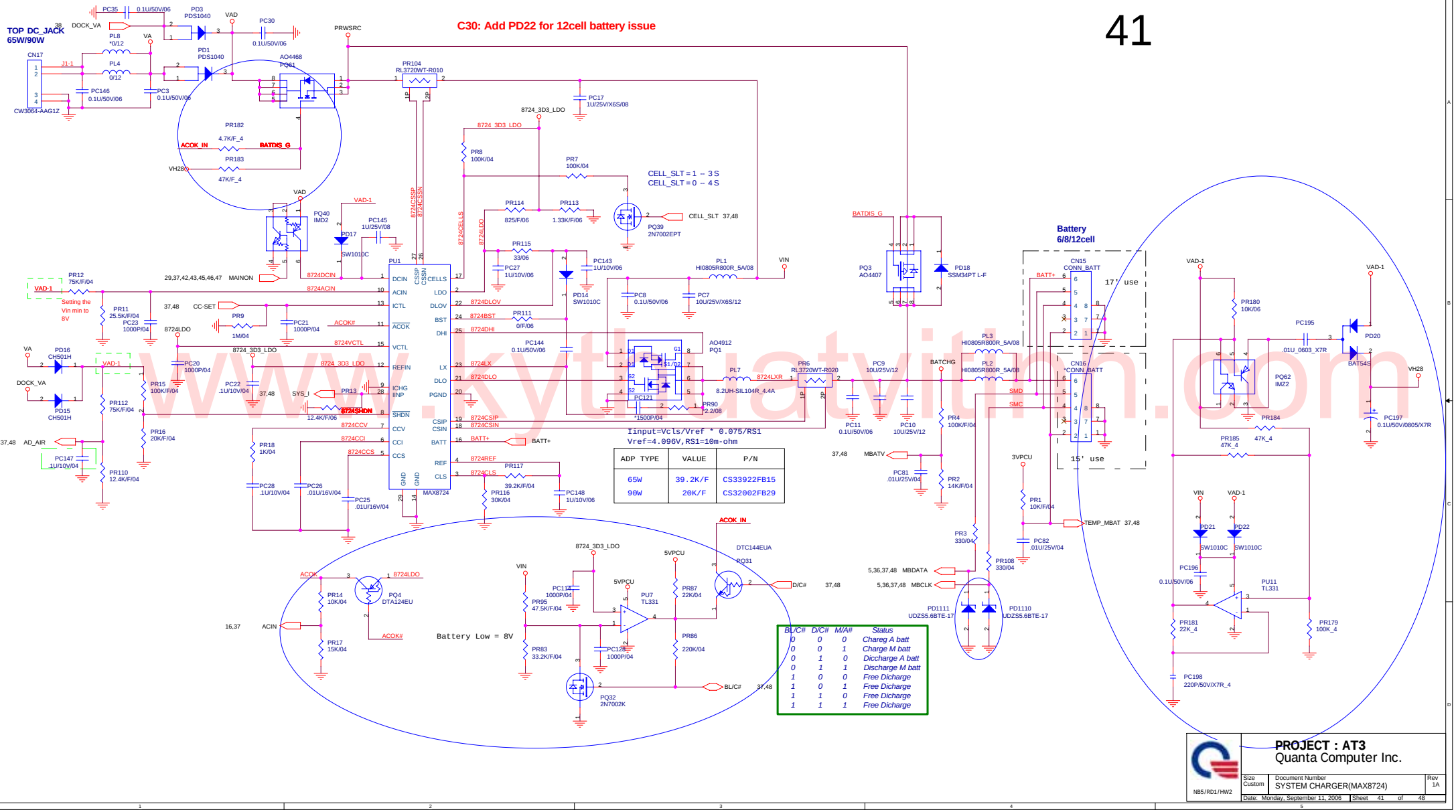
C30: Add PD22 for 12cell battery issue

TOP DC_JACK
65W/90W



PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM CHARGER(MAX8724)	1A

NB5/RD1/HW2

Date: Monday, September 11, 2006 Sheet 41 of 48

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

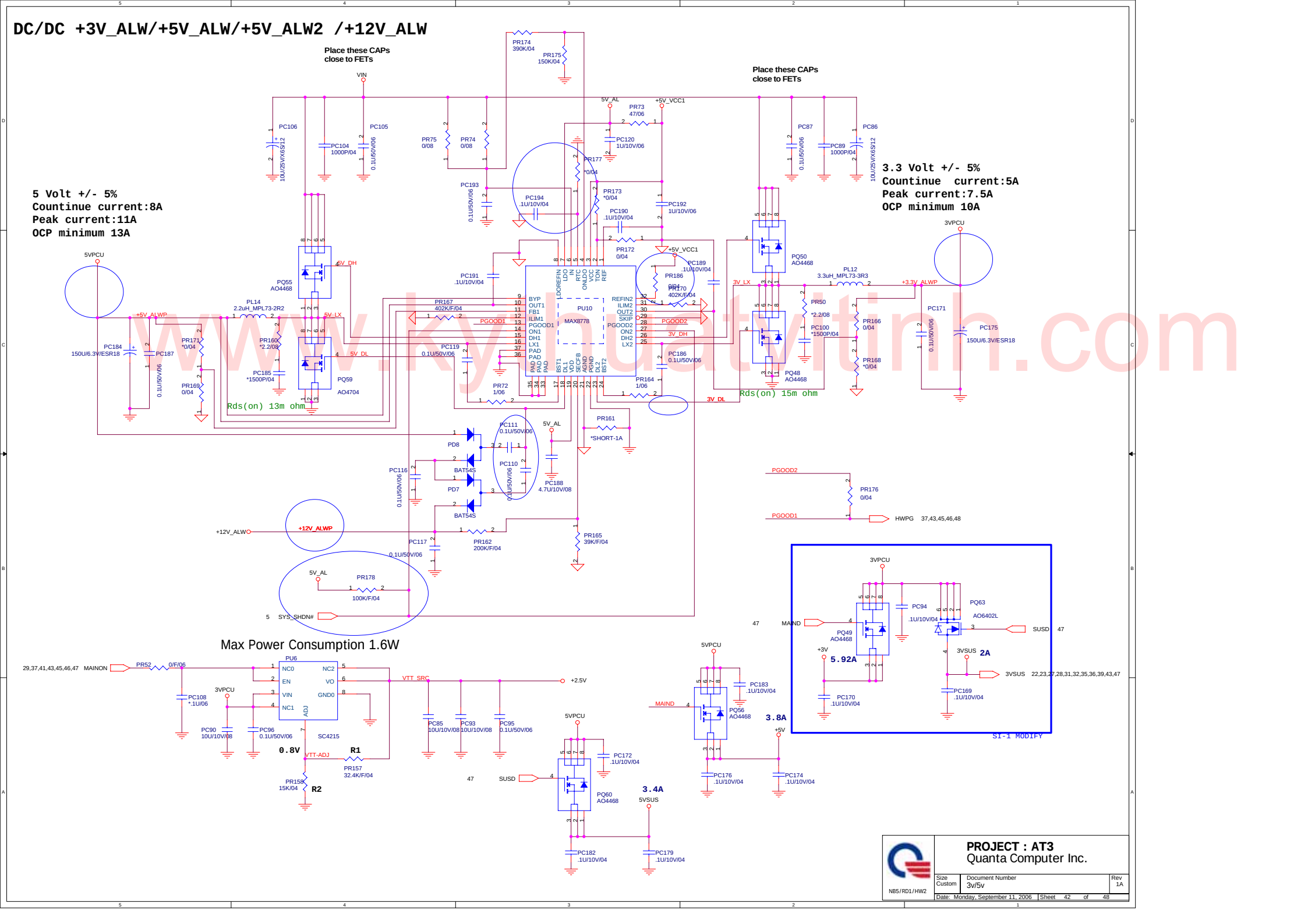
5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

Rds(on) 15m ohm

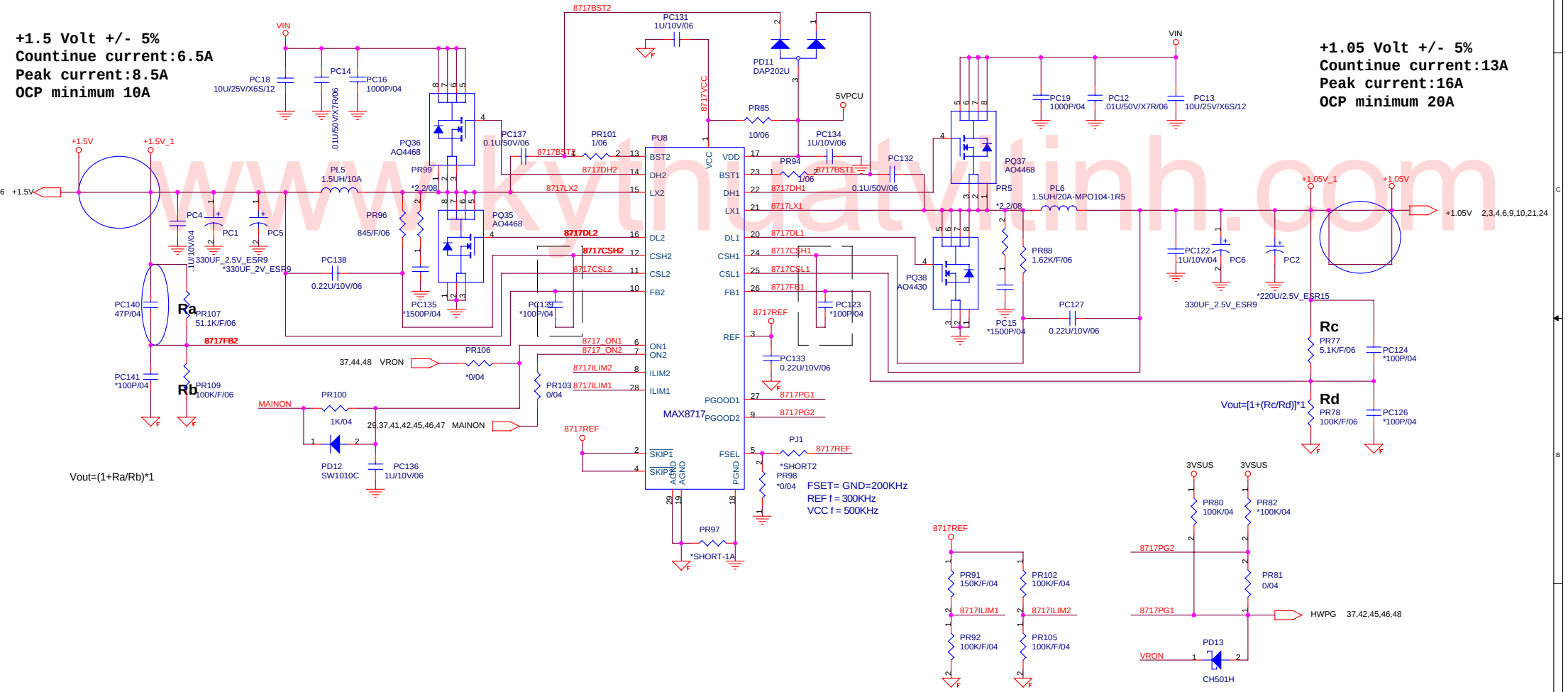
Max Power Consumption 1.6W



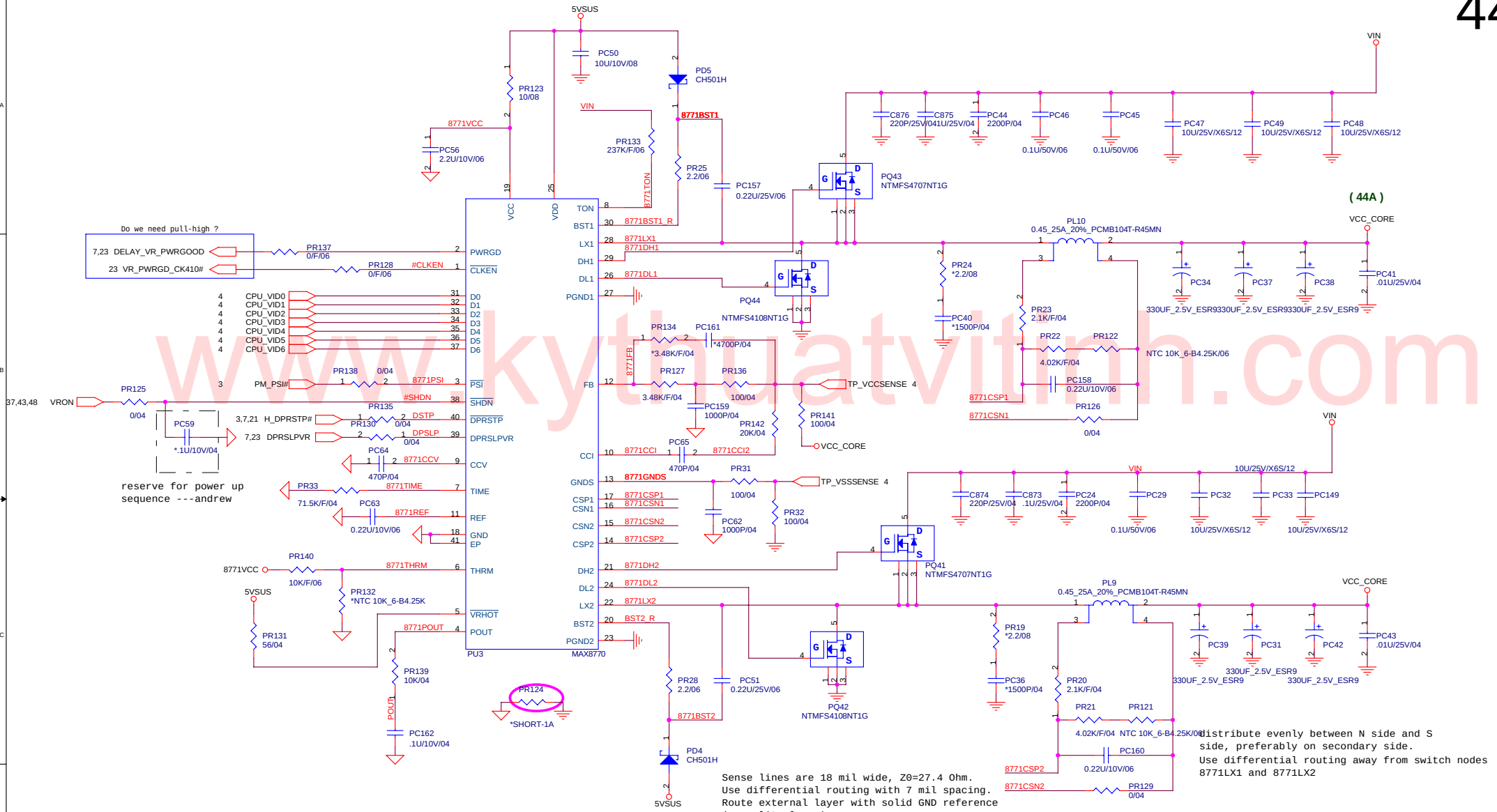
NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom Document Number: 3v/5v	Rev: 1A
	Date: Monday, September 11, 2006	Sheet 42 of 48

+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



PROJECT : AT3	
Quanta Computer Inc.	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)
Rev: 1A	
NB5/RD1/HW2	
Date: Monday, September 11, 2006	Sheet 43 of 48

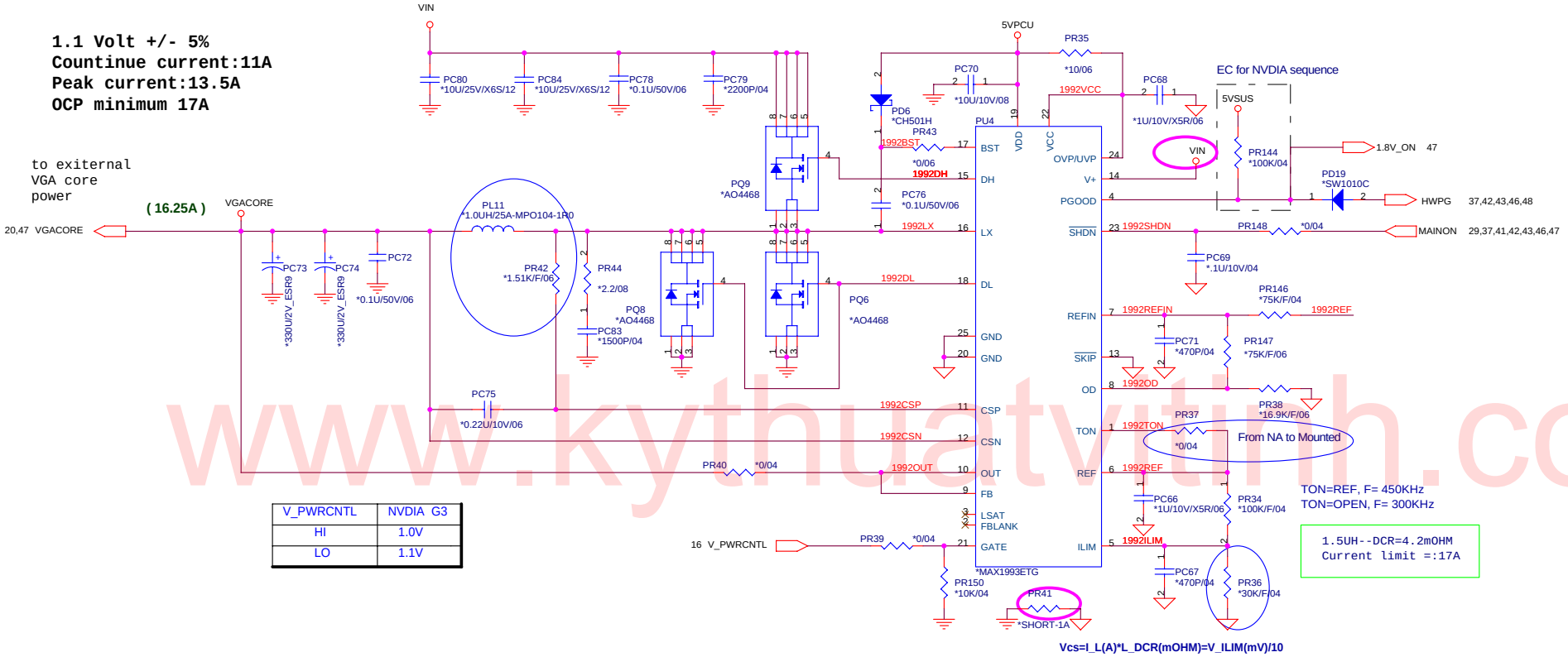


NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: CPU_CORE(MAX8771)	Rev: 1A
Date: Monday, September 11, 2006	Sheet 44 of 48	

1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

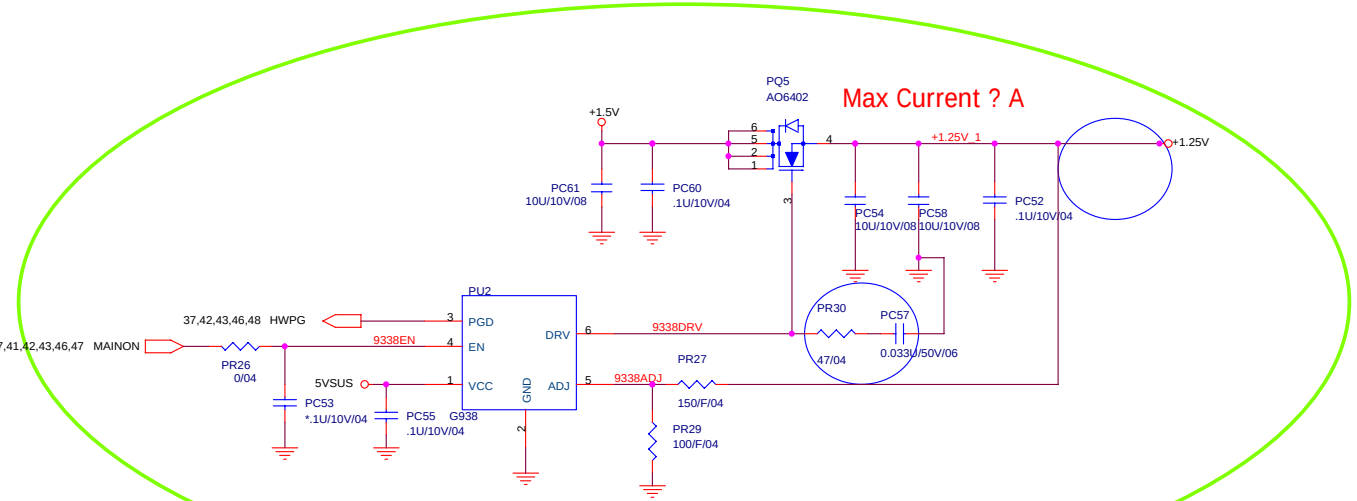
to exiternal
VGA core
power

(16.25A)



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10



Vout1=(1+R1/R2)*0.5

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGACORE (MAX1993)	1A

NB5/RD1/HW2

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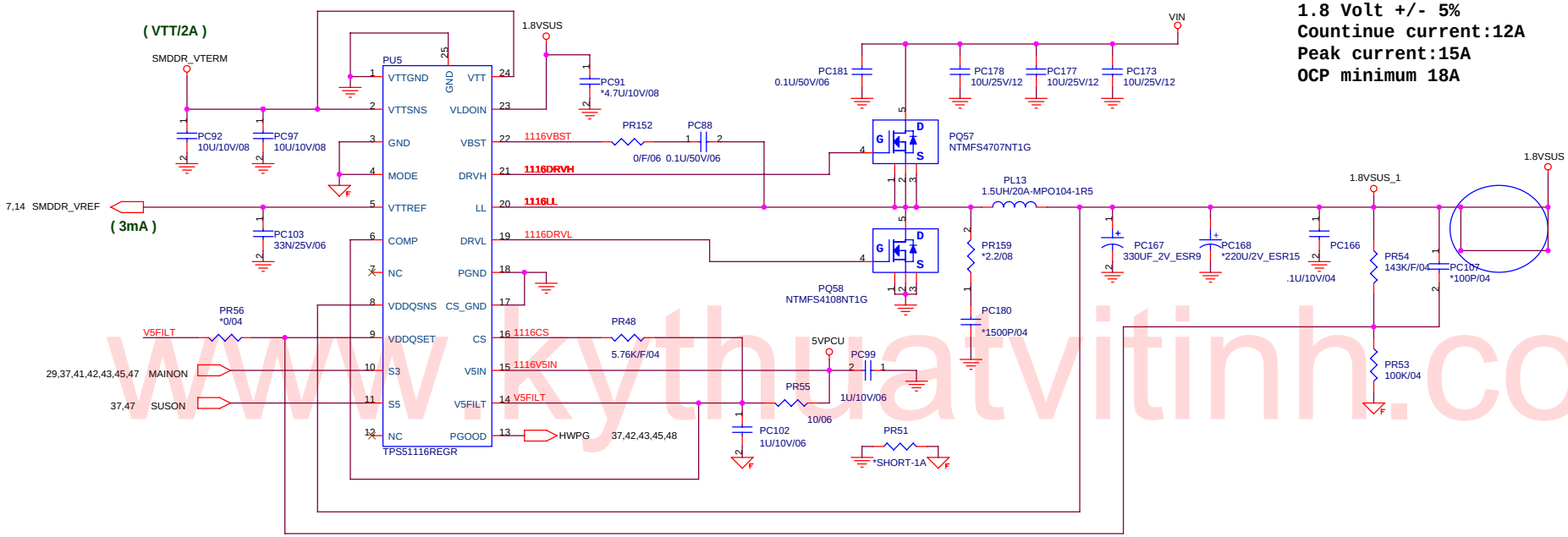
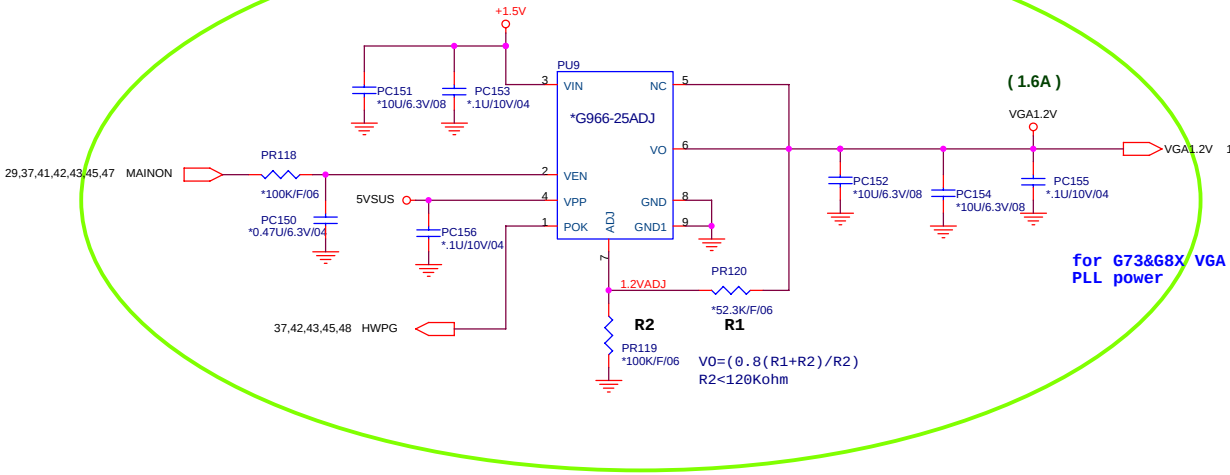
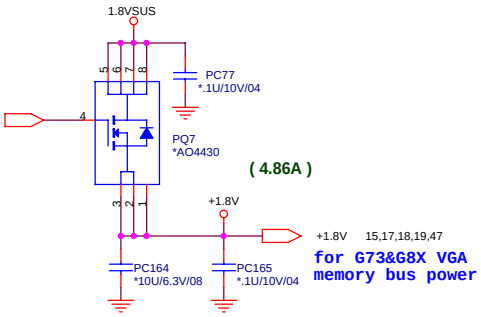
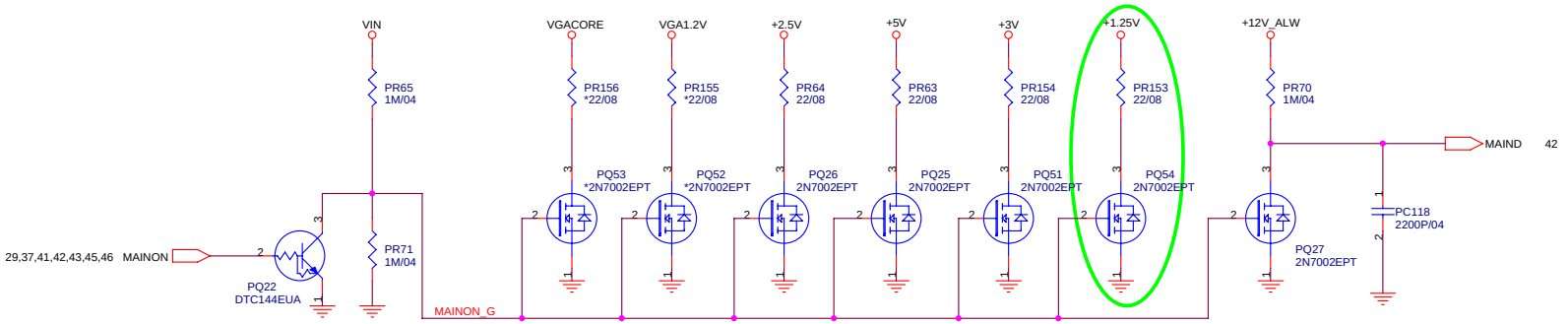


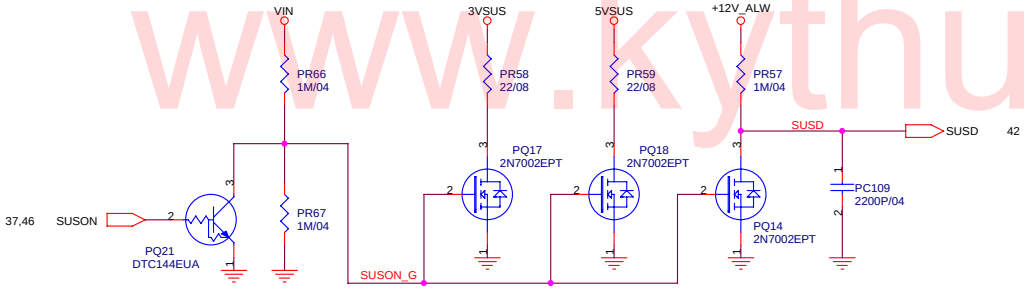


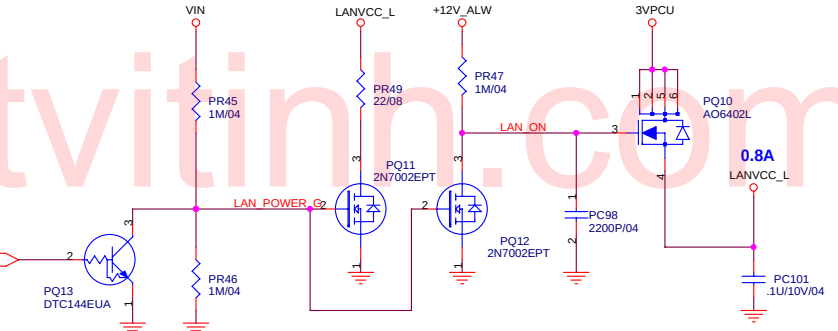


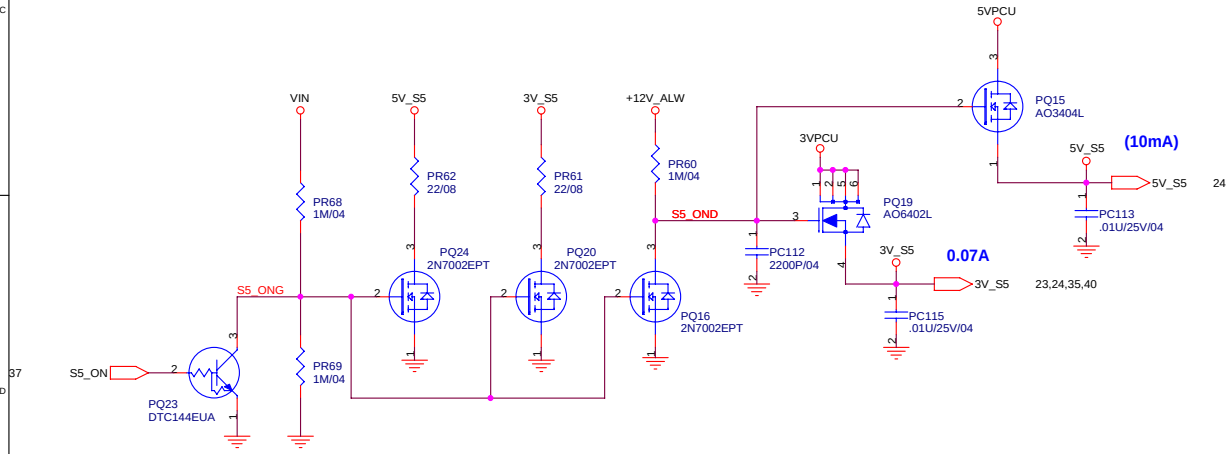
PROJECT : AT3
Quanta Computer Inc.

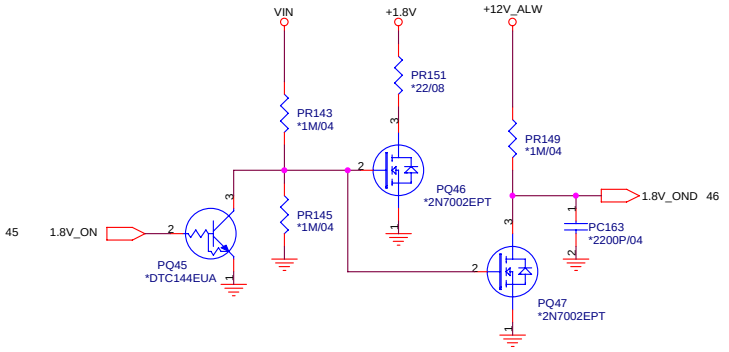
Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	1A
NB5/RD1/HW2	Date: Monday, September 11, 2006	Sheet 46 of 48



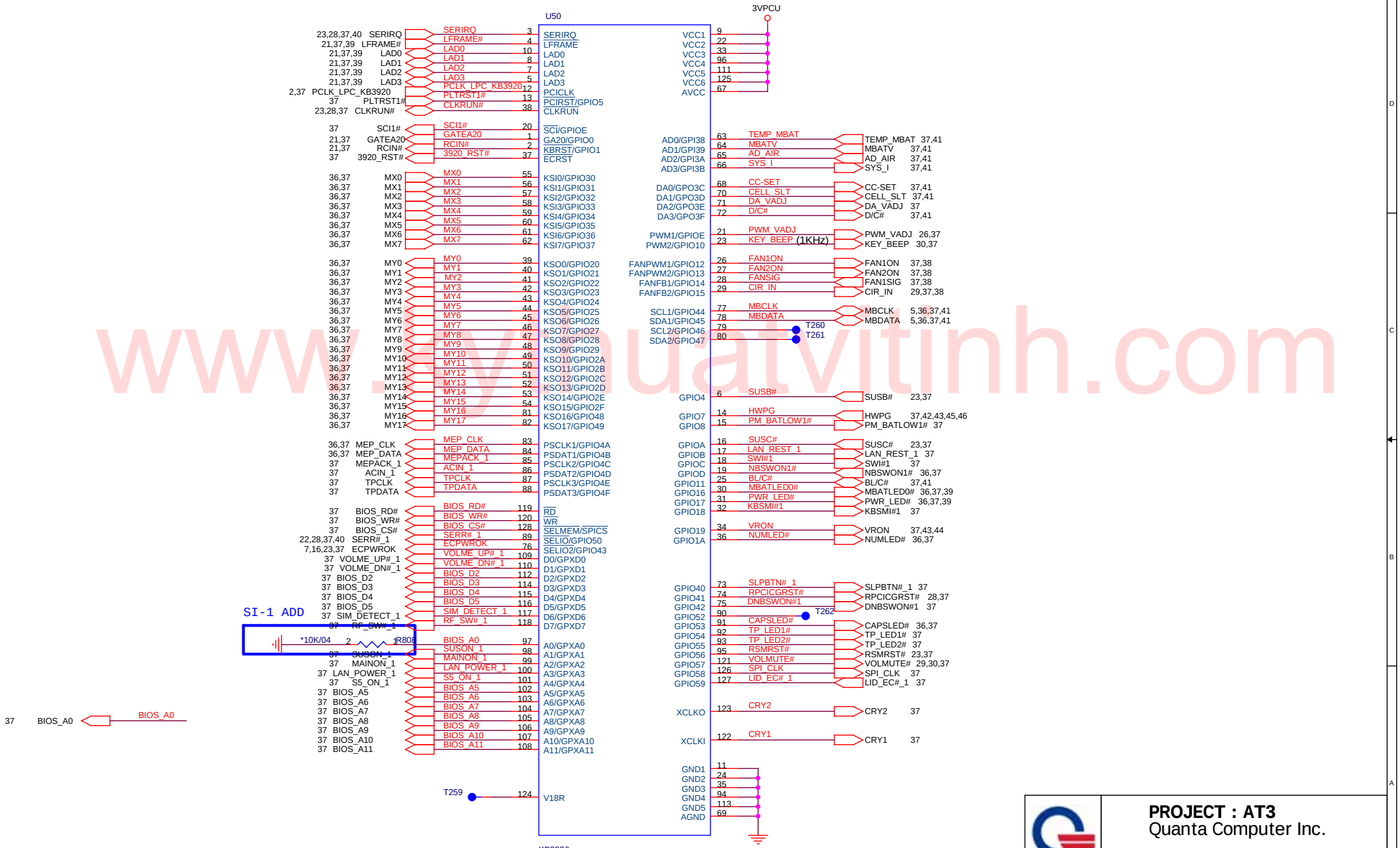








NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom Document Number: DISCHARGE	Rev: 1A
	Date: Monday, September 11, 2006	Sheet 47 of 48



PROJECT : AT3		
Quanta Computer Inc.		
Size: B	Document Number: KB3926	Rev: 1A
Date: Monday, September 11, 2006	Sheet 48 of 48	

NB5/RD1/HW2