

TABLE OF CONTENTS

MB

P01 : COVER SHEET
P02 : SYSTEM BLOCK DIAGRAM
P03 : POWER MAP
P04 : POWER SEQUENCY DIAGRAM
P05 : CLOCK MAP
P06 : SMBUS&I2C MAP
P07 : POWER SEQUENCE
P08 : DCIN/BATT
P09 : PWR_CHARGE
P10 : PWR_5V/3.3V
P11 : PWR_VTT
P12 : PWR_1.5V/0.75S
P13 : PWR_CPU_VCORE
P14 : PWR_OTHER
P15 : PWR_(Empty)
P16 : PWR_1.8VS
P17 : PWR_(Empty)
P18 : POWER SEQUENCY CHART
P19 : Penryn(HOST BUS)1/3
P20 : Penryn(HOST BUS)2/3
P21 : Penryn(Power/Gnd)3/3
P22 : Cantiga (HOST) 1/7
P23 : Cantiga (DMI) 2/7

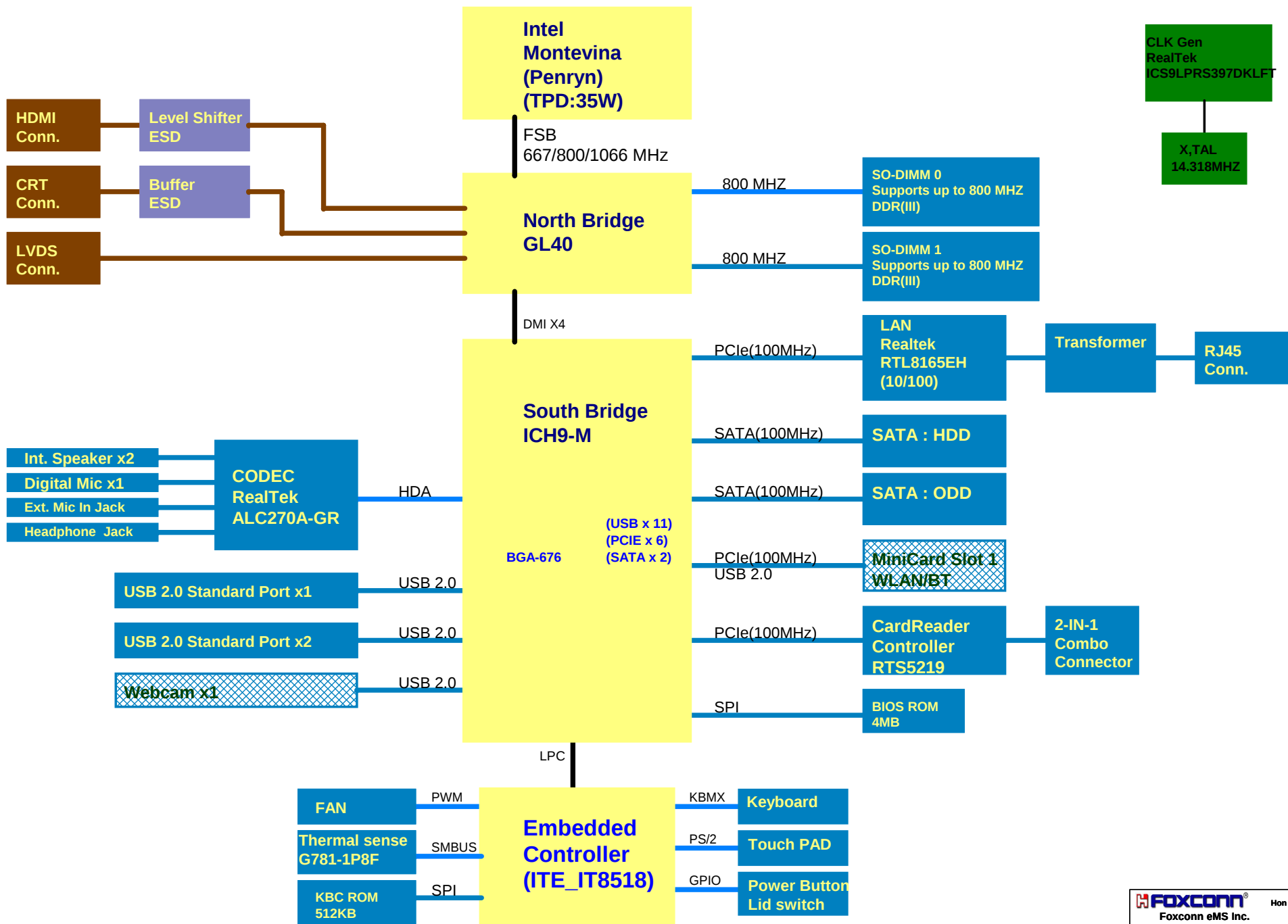
P24 : Cantiga (GRAPHIC) 3/7
P25 : Cantiga (DDR3) 4/7
P26 : Cantiga (POWER,VCC) 5/7
P27 : Cantiga (VCC CORE) 6/7
P28 : Cantiga (VSS) 7/7
P29 : ICH9-M (PCI/USB) 1/5
P30 : ICH9-M(LPC, IDE, SATA) 2/5
P31 : ICH9-M (GPIO) 3/5
P32 : ICH9-M (POWER) 4/5
P33 : ICH9-M (GND) 5/5
P34 : DDR3(S0-DIMM_0) 1/2
P35 : DDR3(S0-DIMM_1) 2/2
P36 : CLOCK GEN
P37 : EC+KBC (IT8518)
P38 : Audio(CODEC)
P39 : Audio(JACK/SPEAKER/MIC)
P40 : LAN (RTL8165EH)
P41 : Card Reader(RTL5219)
P42 : Mini PCIe&BT/PWRB/Control
P43 : USBX2/USB DB/SATA CONN
P44 : LVDS/Webcam
P45 : HDMI & CRT
P46 : Thermal/Fan/Stitch Cap

P. Leader	Check by	Design by

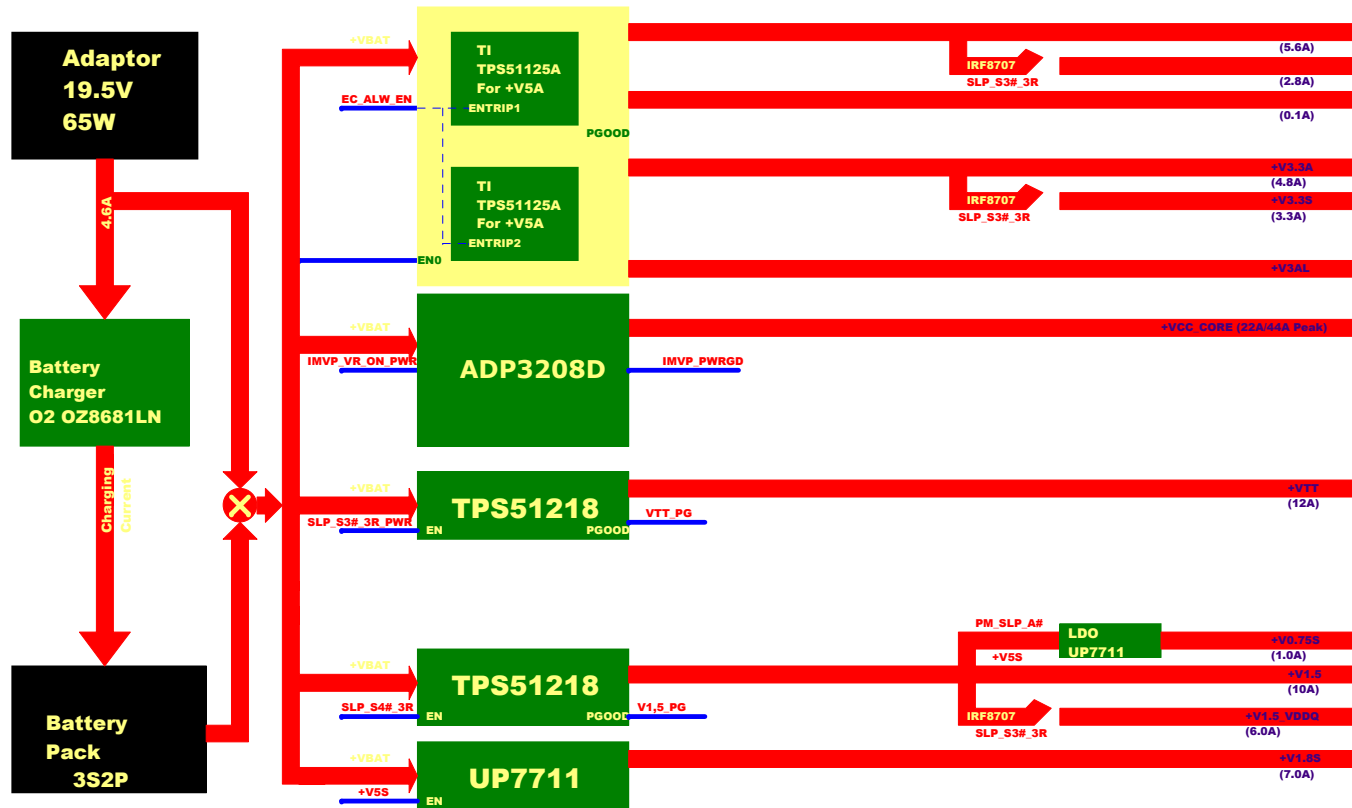
FOXCONN
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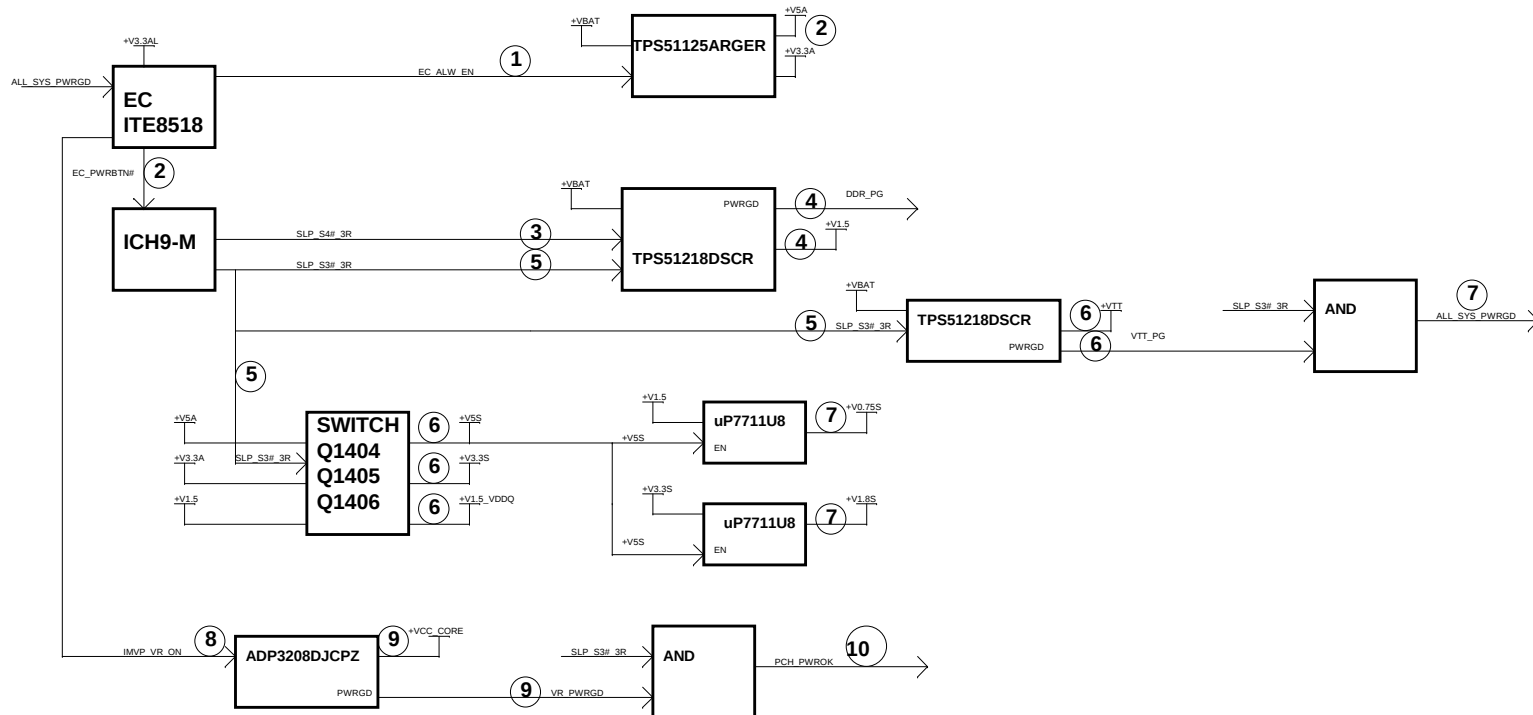
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111

Title		
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Size	Document Number	Rev
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Page Modified: Monday, January 24, 2011 08:43:01 (UTC/GMT) Sheet 1 of 46		



POWER MAP





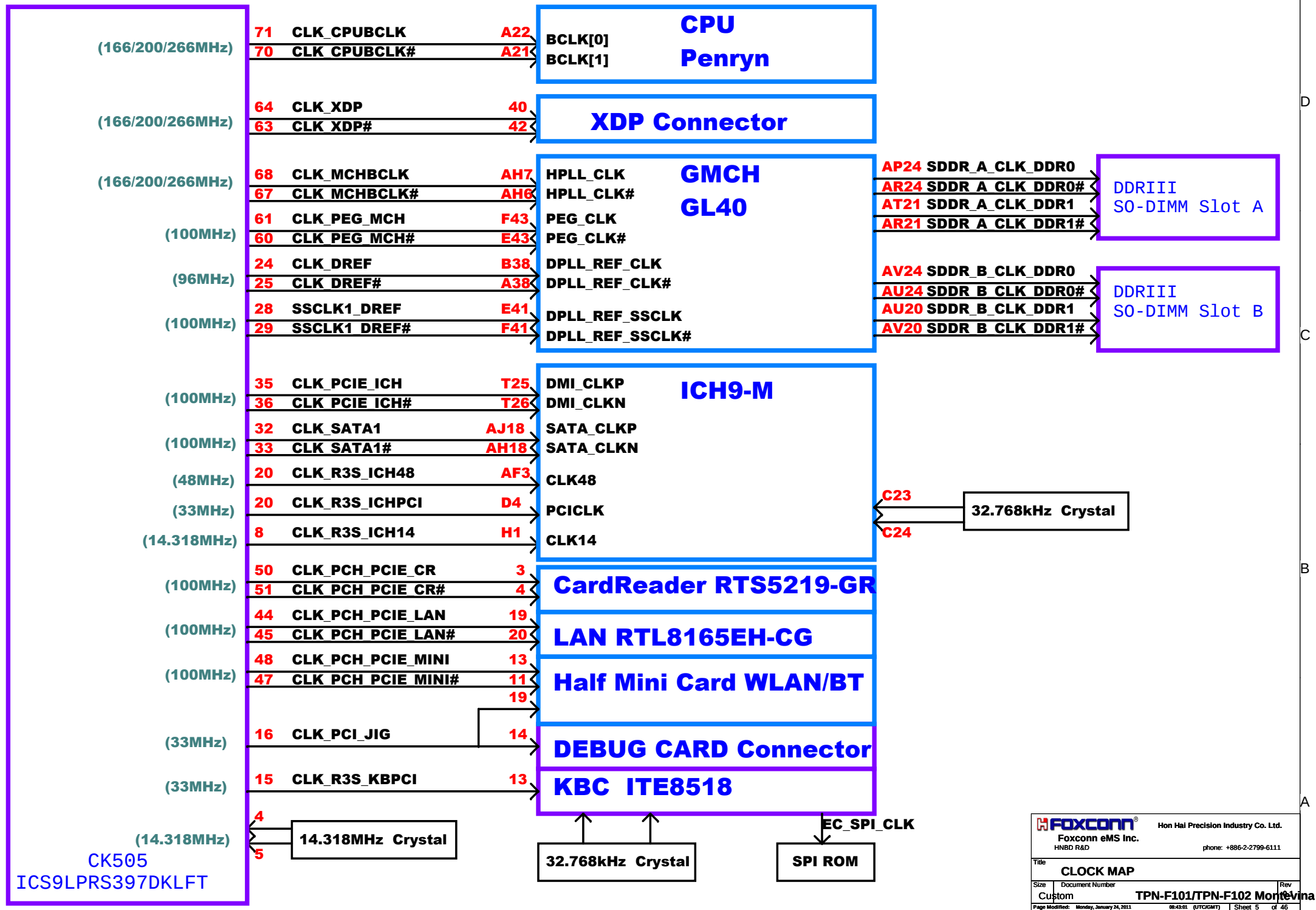
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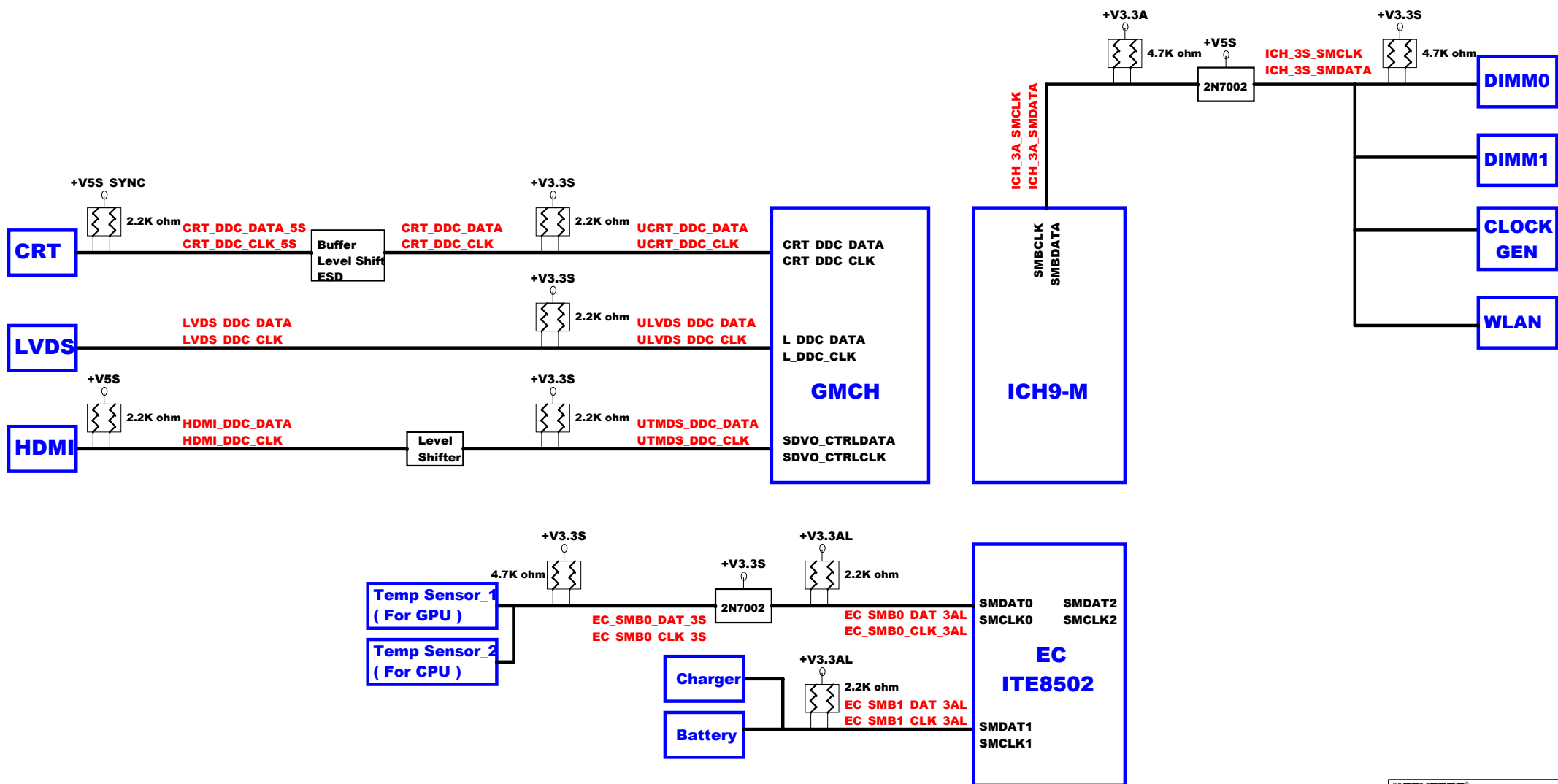
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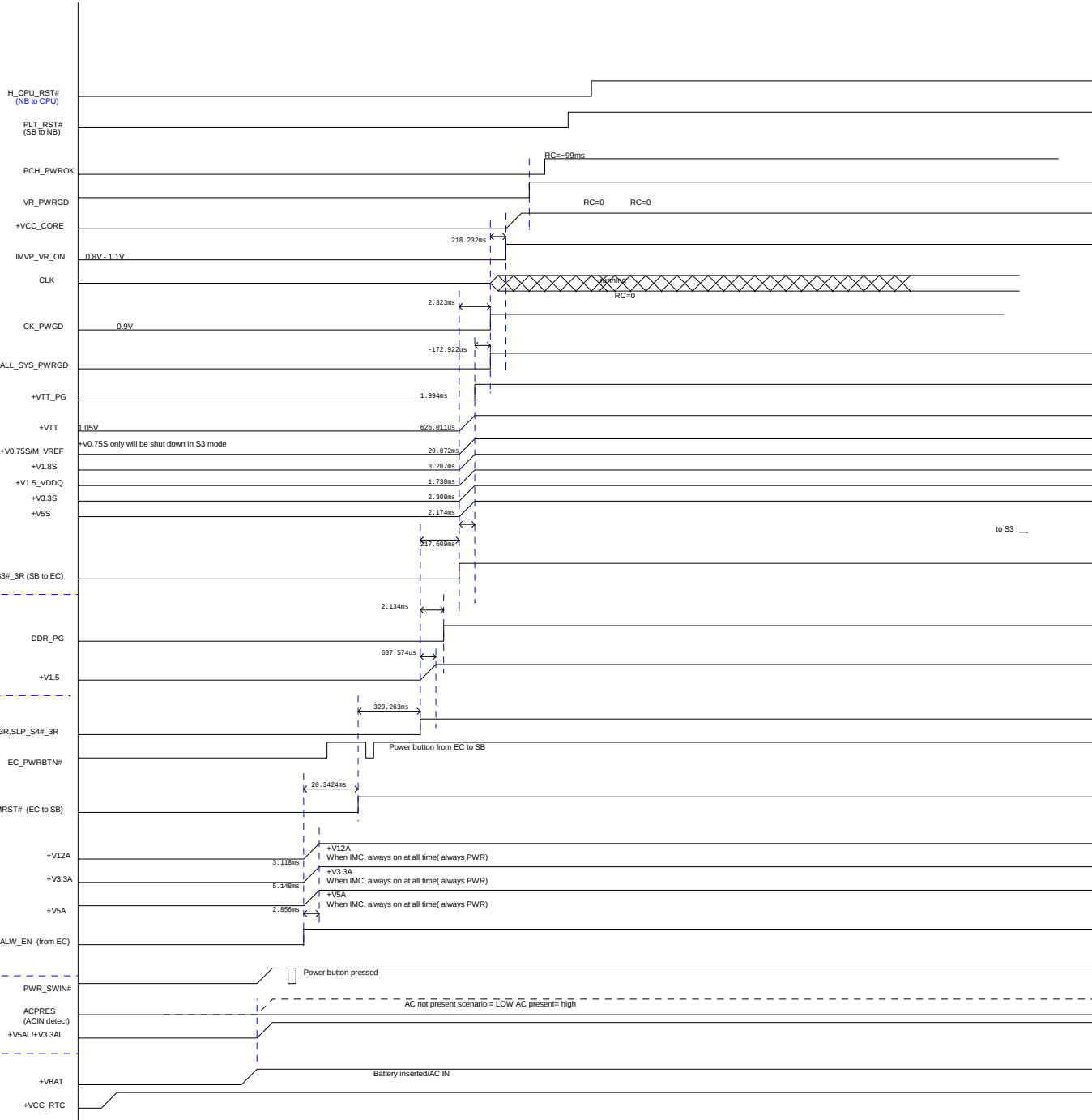
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 4, +V3.3S ramp before +V1.1S

ICH9-M:

- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before VCC_NB







Power on Sequence required:

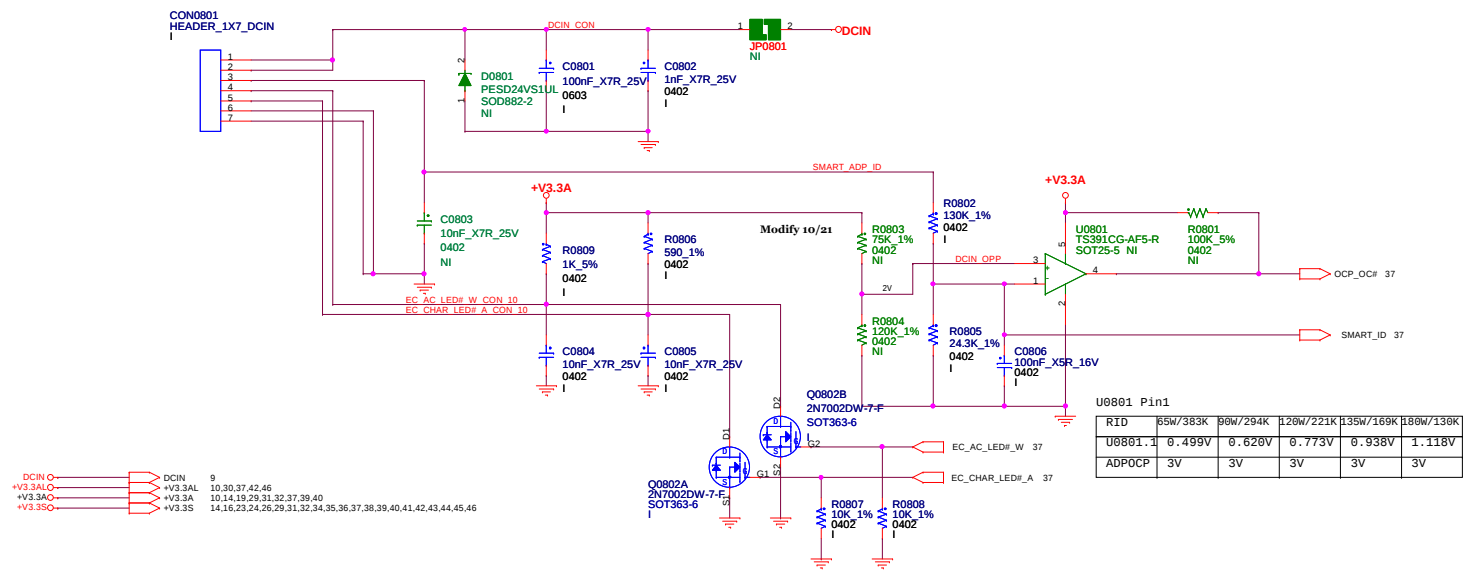
ICH9M:

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

GMCH:

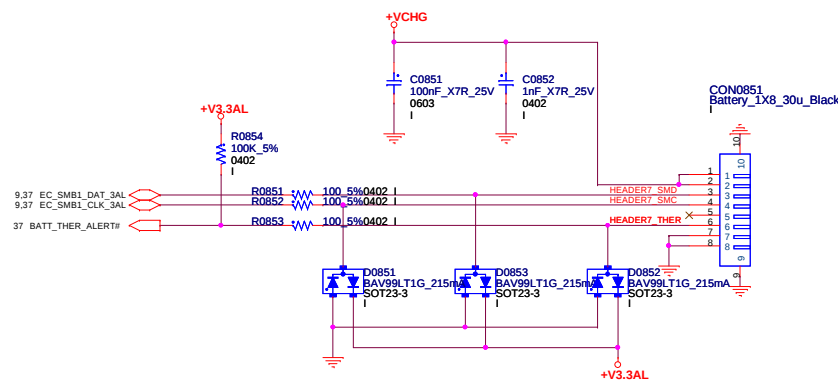
- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC_NB

DC_JACK WIRE to BOARD CONNECTOR

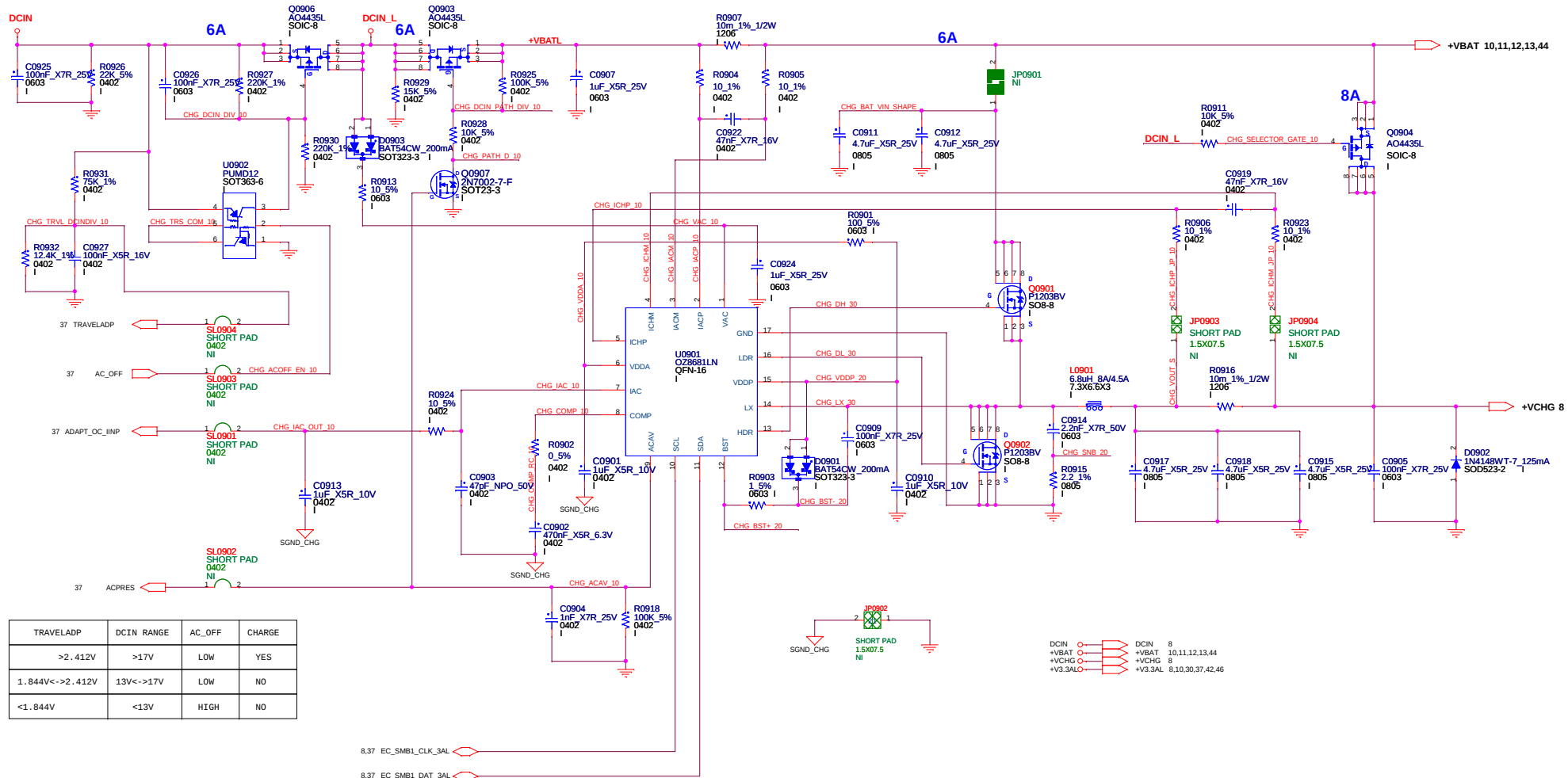


BATTERY CONNECTOR

2010.0914.0



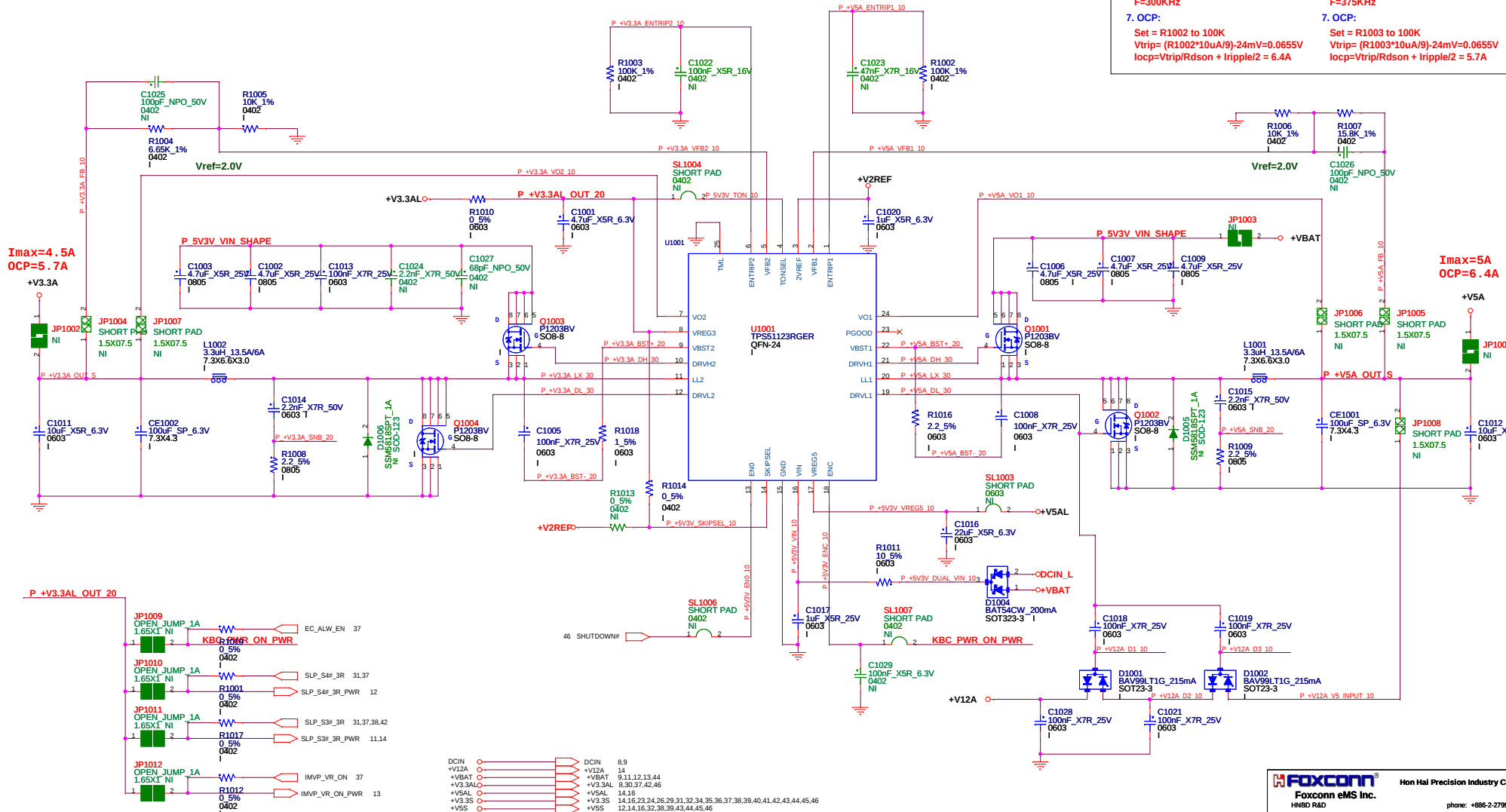
BATTERY CHARGER



+V5A / +V3.3A POWER SUPPLY

2010.1103.0

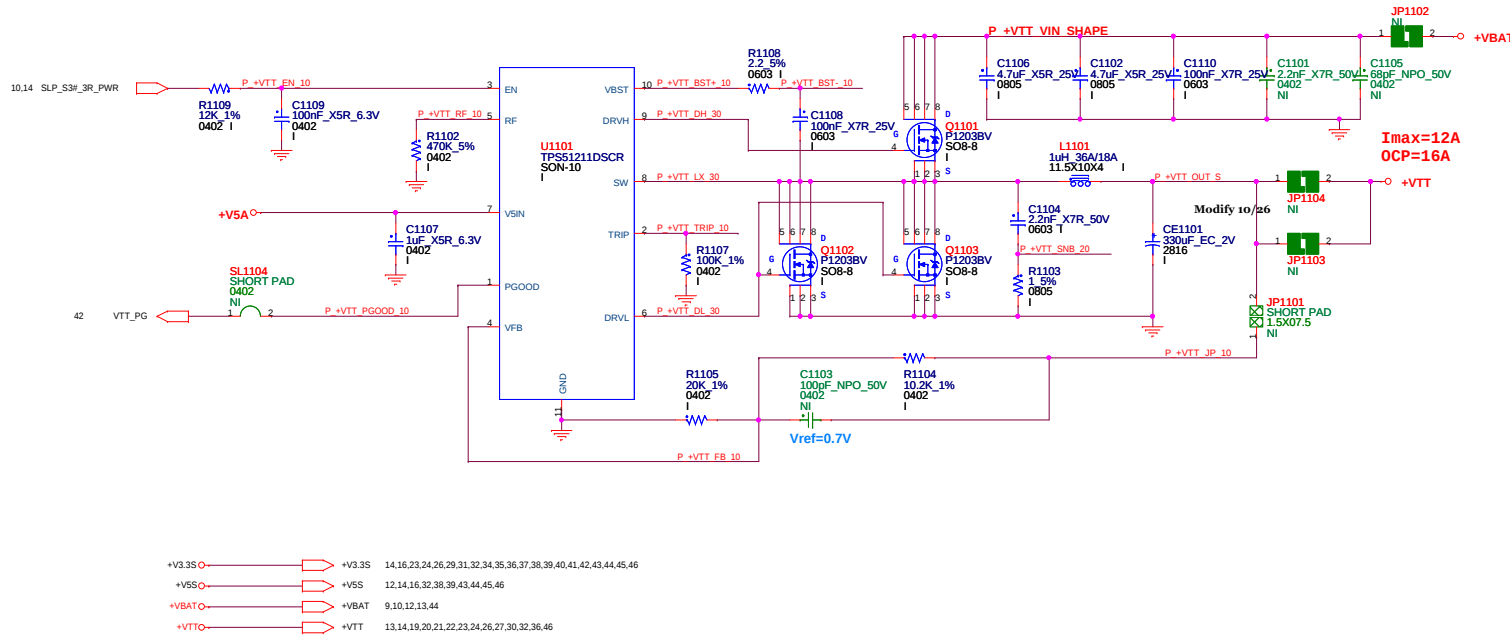
+V5A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 55.8mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^{\circ}C$) $I_{peak} = 88A$ (Pause $\geq 10us$) 6. Frequency: $F = 300KHz$ 7. OCP: Set = $R1002$ to $100K$ $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple}/2 = 6.4A$	+V3.3A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 33.15mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: L-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^{\circ}C$) $I_{peak} = 88A$ (Pause $\geq 10us$) 6. Frequency: $F = 375KHz$ 7. OCP: Set = $R1003$ to $100K$ $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple}/2 = 5.7A$
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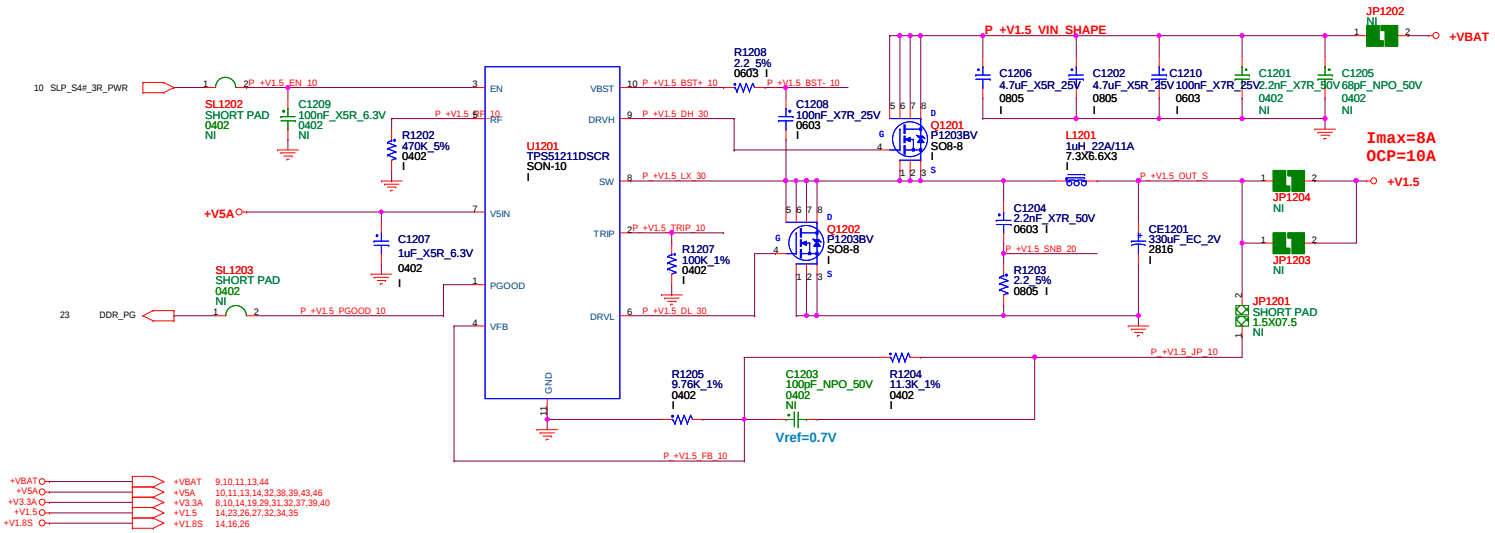
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 Size: Document Number
 C: **CHICAGO**
 Page Modified: Monday, January 24, 2011 09:06:38 (UTC+0800) Sheet 10 of 43
 Rev: **0.1**

+VTT POWER SUPPLY



- +VTT:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.86A$
 - Ripple Current:**
 $I_{rip} = 3.42A$
 - Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 30.78mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
 - MOSFET Spec:**
H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause $\approx 10\mu s$)
L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause $\approx 10\mu s$)
 - Frequency:**
 $F = 290KHz$ ($R_{0802} = 470K$)
 - OCP:**
 $Set = R_{0807} \text{ to } 100K$
 $V_{trip} = R_{0807} \cdot I_o \cdot A = 1V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 16A$

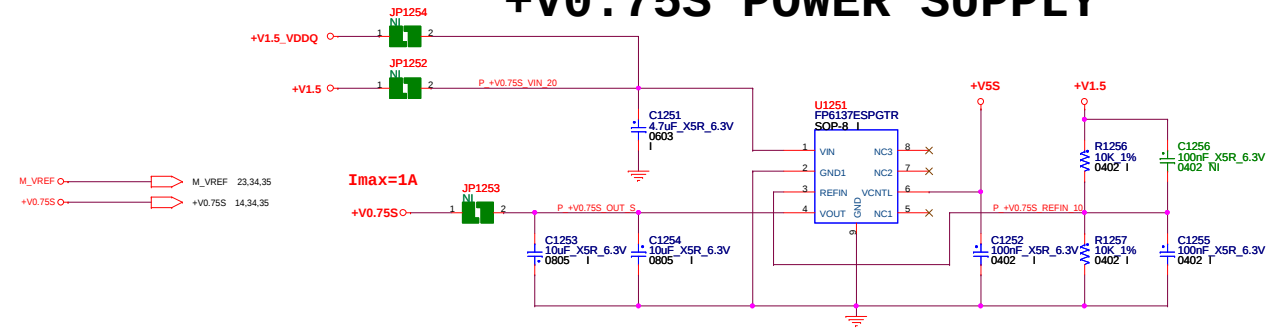
+V1.5 POWER SUPPLY



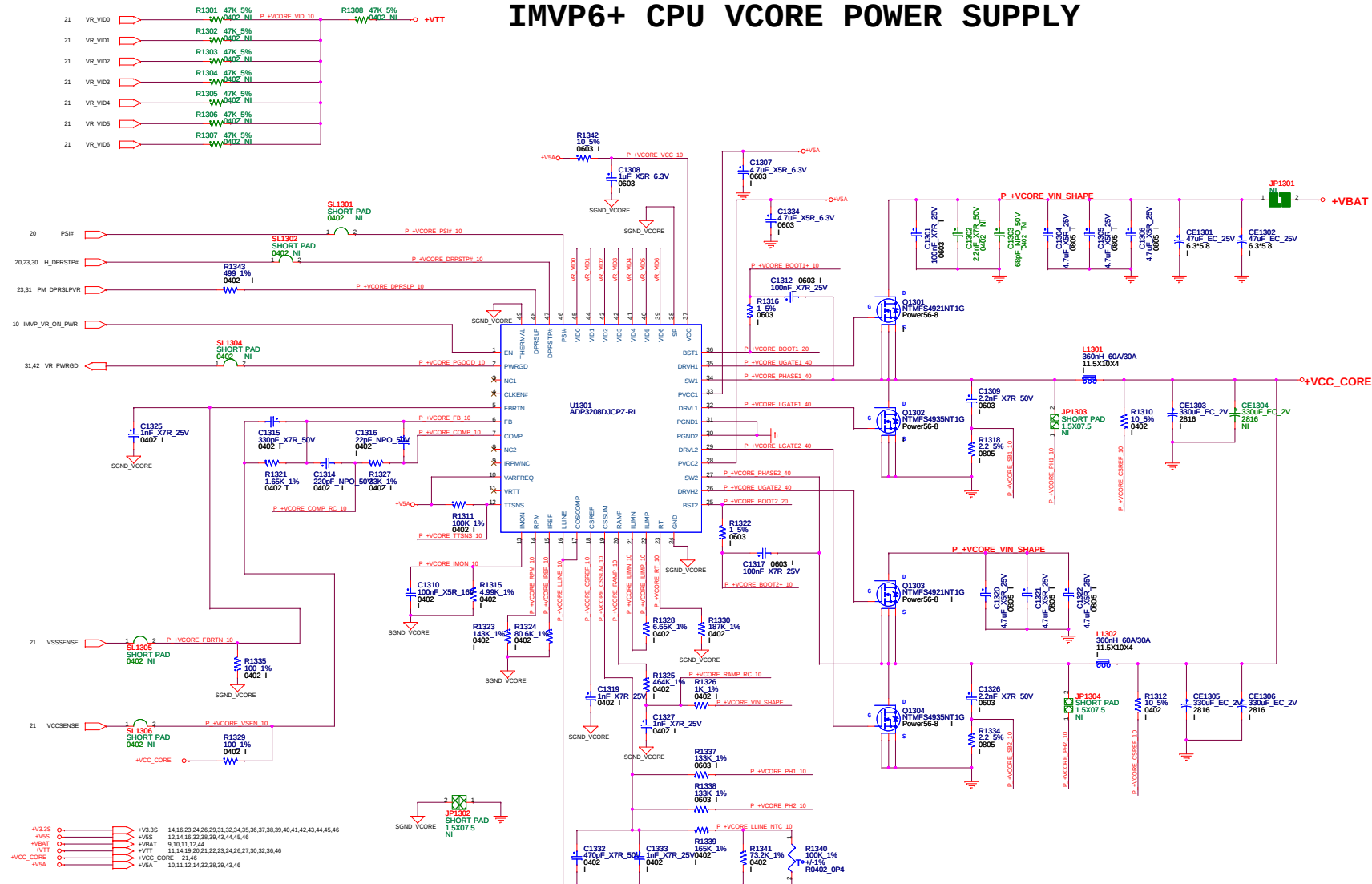
- +V1.5:**
 - I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.78A$
 - Ripple Current:**
 $I_{rip} = 3.34A$
 - Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 30.6mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
 - MOSFET Spec:**
 H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)

 L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 - Frequency:**
 $F = 290KHz$ ($R0902 = 470K$)
 - OCP:**
 Set = R0907 to 100K
 $V_{trip} = R0907 \cdot 10uA = 1V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple/2} = 9.5A$

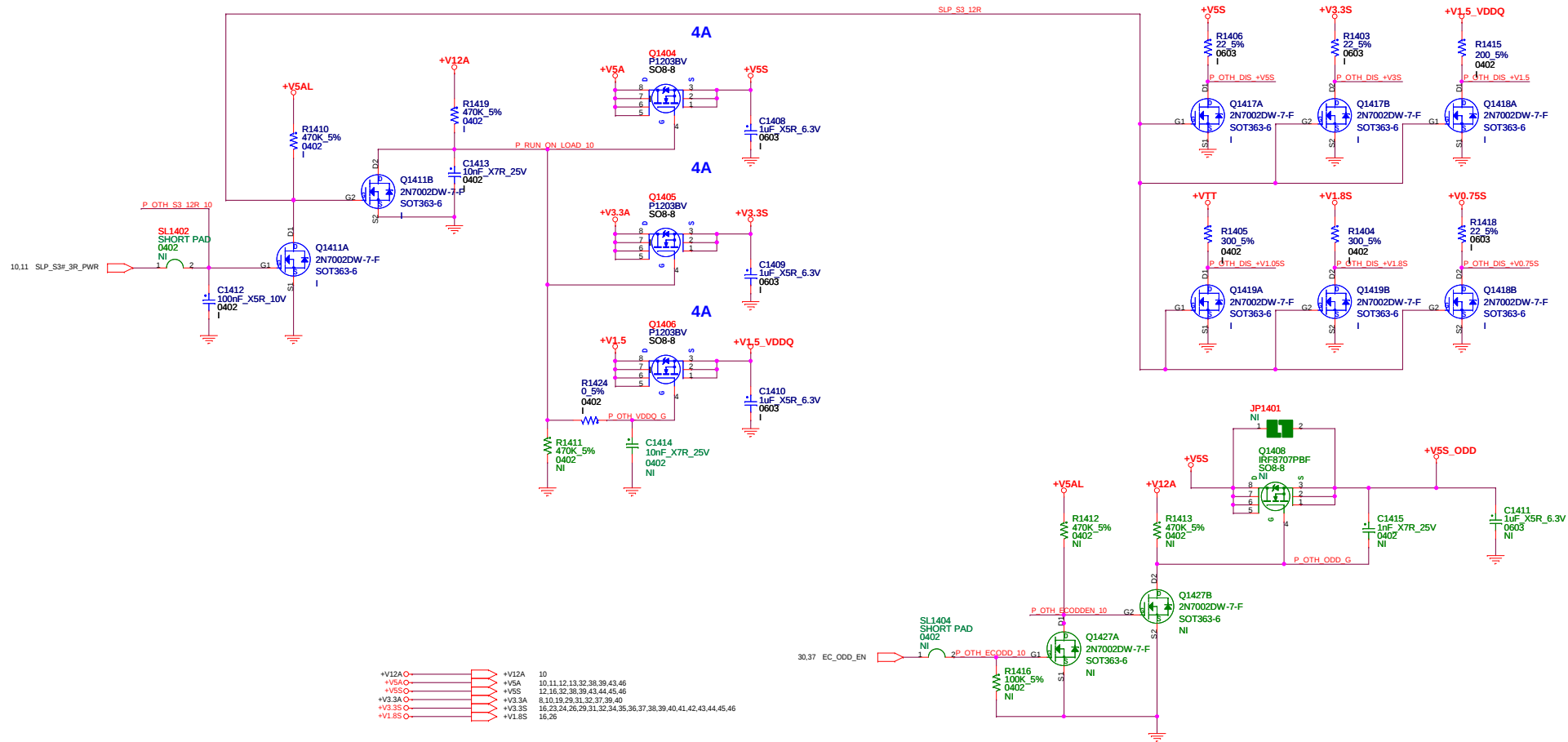
+V0.75S POWER SUPPLY

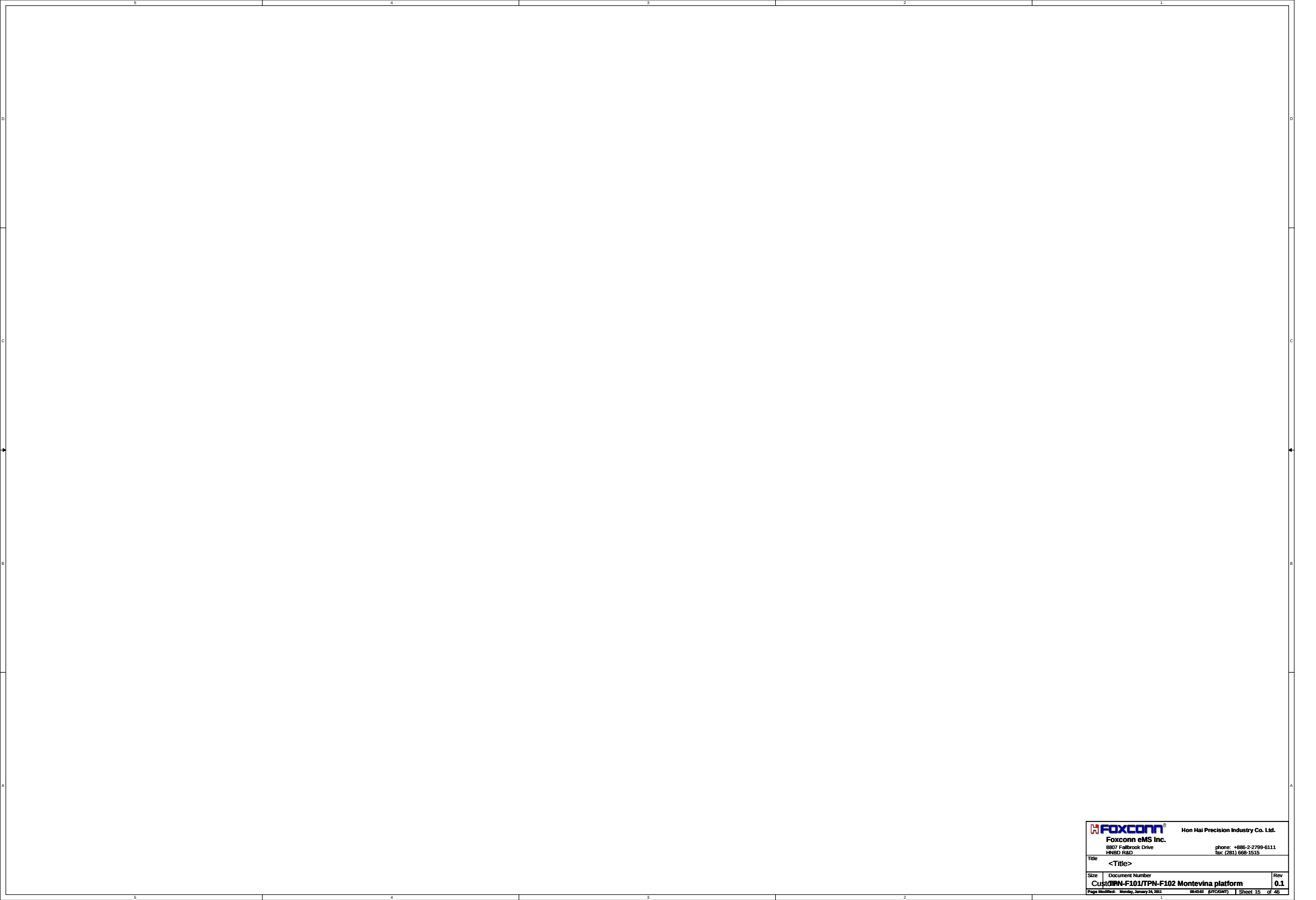


IMVP6+ CPU Vcore POWER SUPPLY

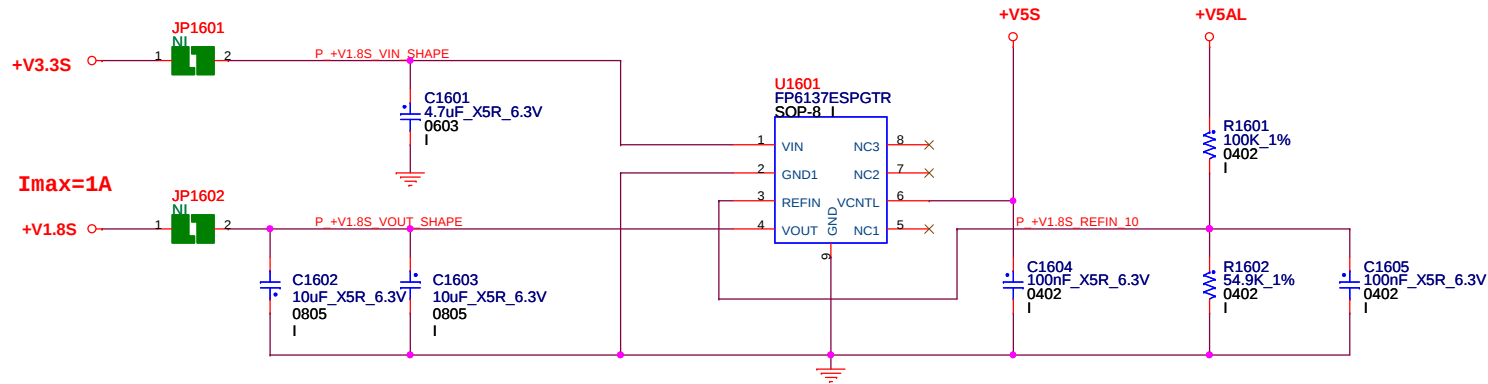


OTHER POWER / DISCHARGE CIRCUITS

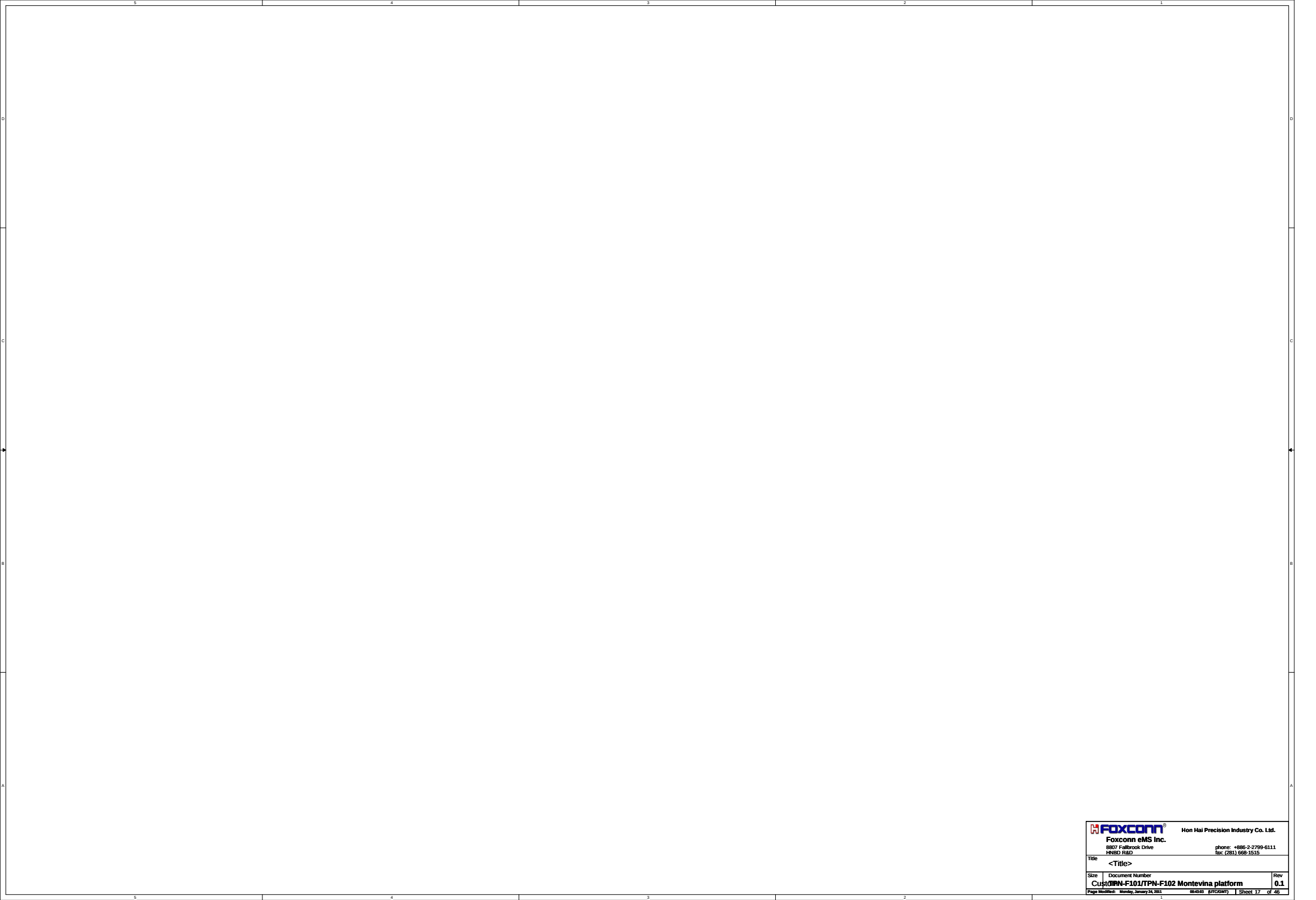




+V1.8S POWER SUPPLY



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Title		PWR_1.8VS	
Size	Document Number	Rev	
Customer	CHICAGO	0.1	
Page Modified: Monday, January 24, 2011		08:43:02 (UTC+GMT) Sheet 16 of 46	



Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKPIN	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	D56/3
+VCC_NB	PJ21/2
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	D87/2
+VDDR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	D57/1
+V1.8S	PJ2/1
+V3.3S	PC170
+V5S	PC175
+V1.2S	PQ41/D
SLP_S3H_3R	RS60
+V0.75S	PJ8/2
M_VREF	
+V1.5	PC182
SLP_S5H_3R	RS76
EC_PWRBTN#	D16/2
RSMRST#	RS61
+V1.1A	PJ23/2
+V3.3A	PC109
+V5A	PJ25
+V1.2A	PC169
EC_ALW_EN	PQ27/G
PWR_SWIN#	HEADER2/6
ACPRES	RS51
+V5AL	PC164
+V3.3AL	PJ24
M31ALDO	PC51
+VBAT	PJ19/2
+VCC_RTC	CS48

CPU MEM CTL & DDR3 SODIMM PWRS

CPU THM/SB/SCL1/2 SB_KB/SPI/LPC ROM PWRS

KBC is ready

KBC is powered by +V3.3AL

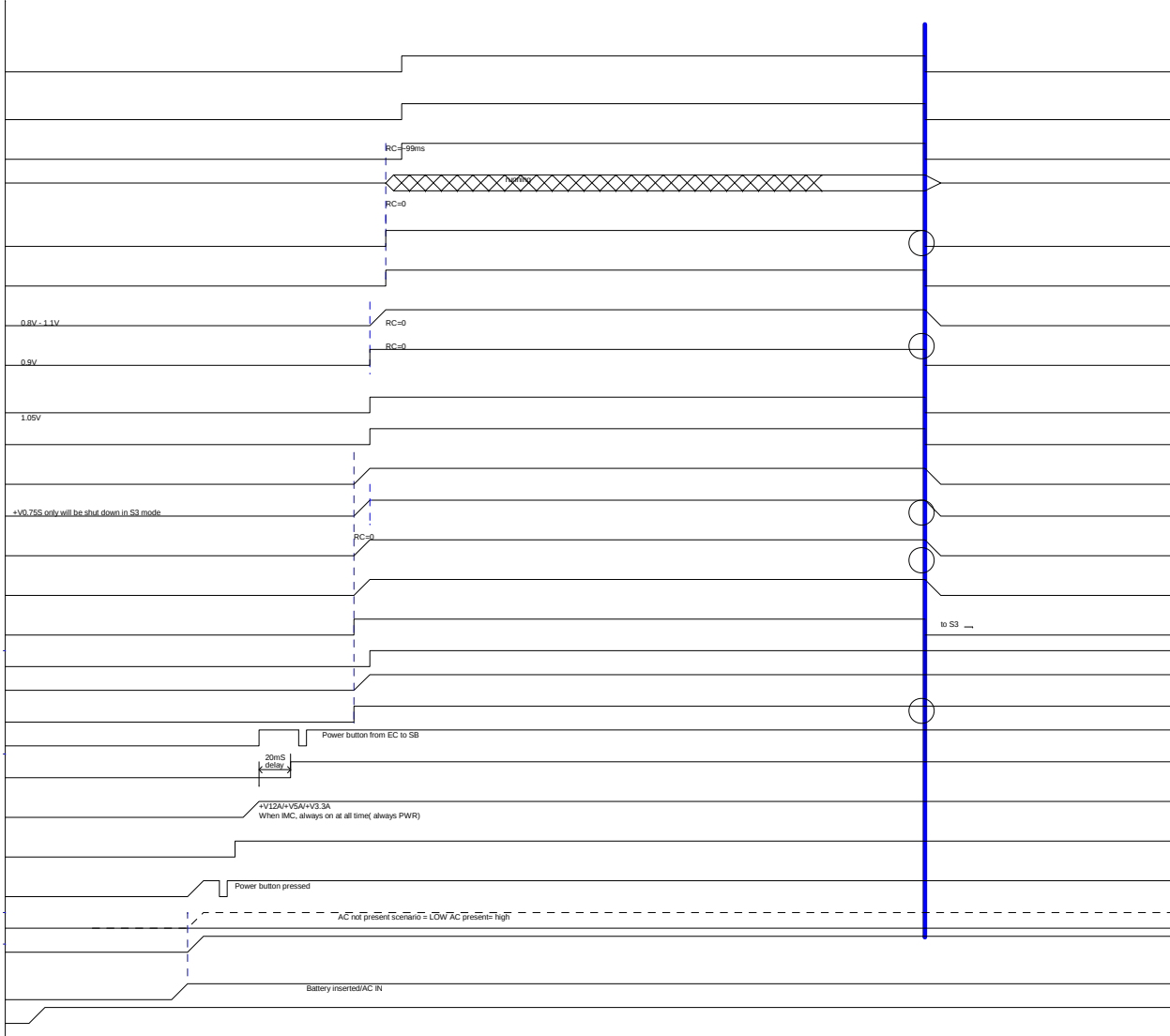
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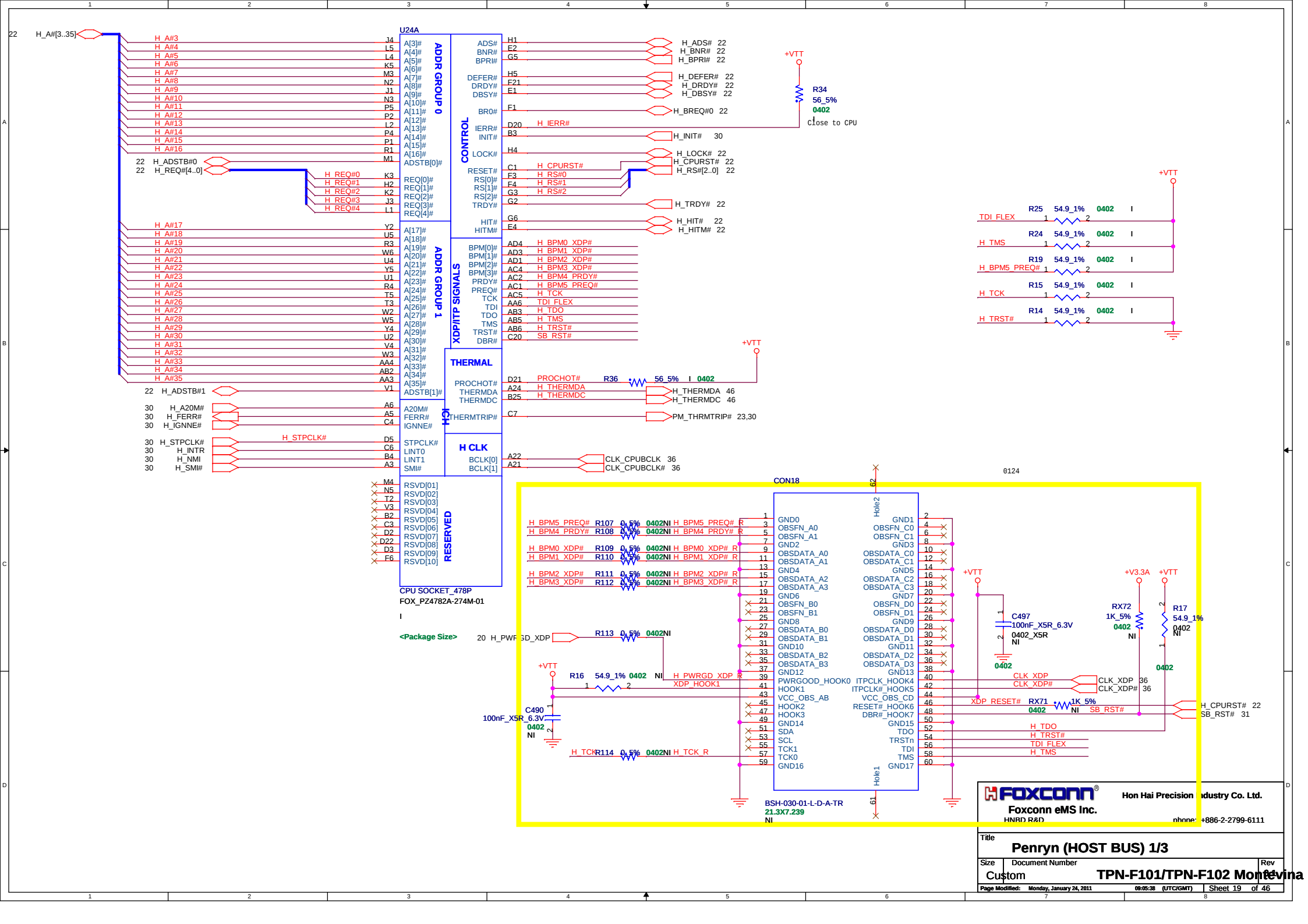
ICH9M:

1. +V3.3A ramp before +V1.1A
2. +V3.3S ramp before +V1.8S
3. +V1.8S ramp before +V1.1S
5. +V3.3A ramping down time > 300us
6. 50uS <= All power rails except +V3.3A <= 40mS
7. 100uS <= +V3.3A <= 40mS

GMCH:

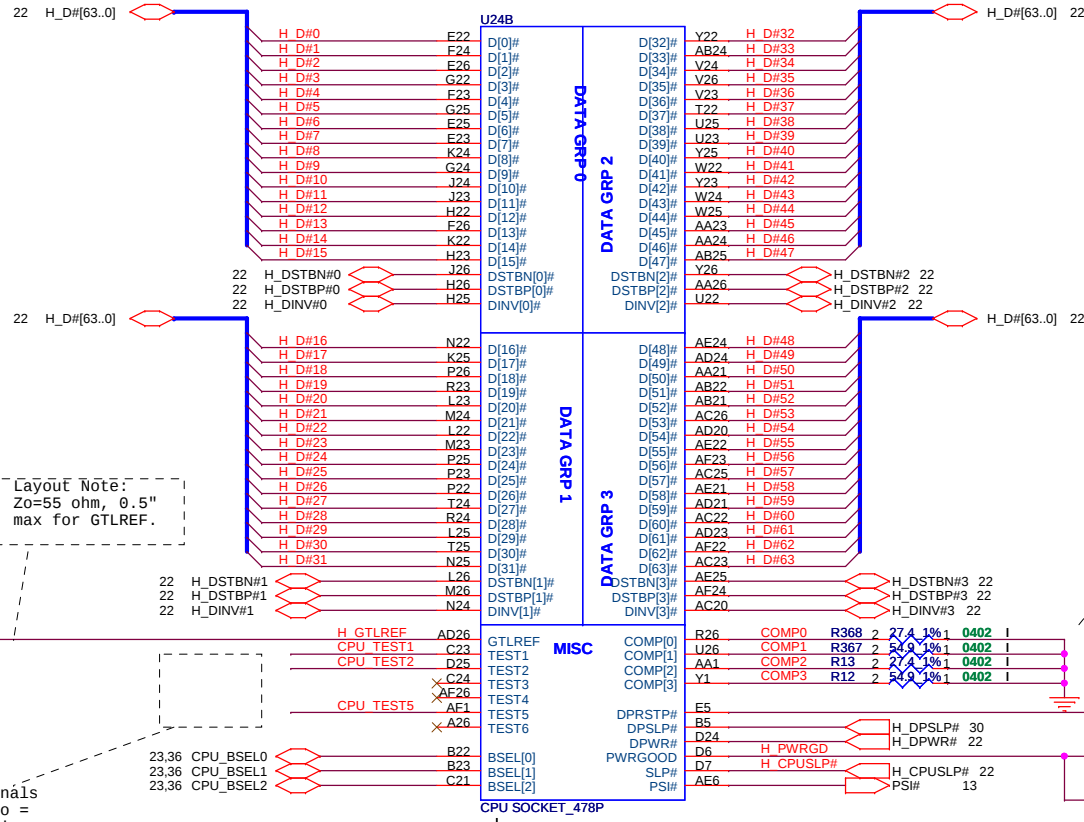
1. 0 < (+V3.3S) - (+V1.8S) < 2.1
2. +V1.8S ramp before +V1.1S
3. +V1.1S ramp before +VCC_NB



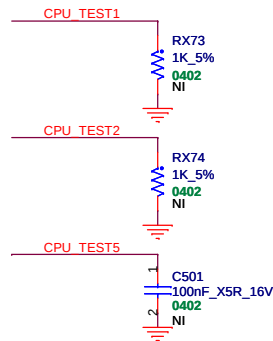


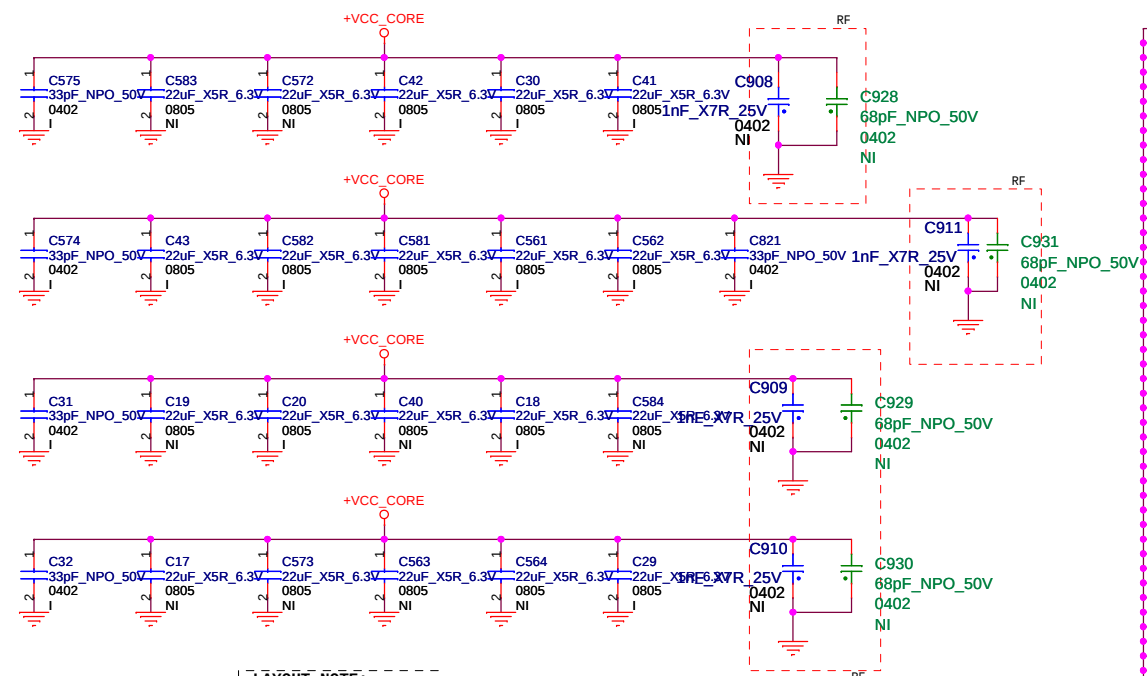
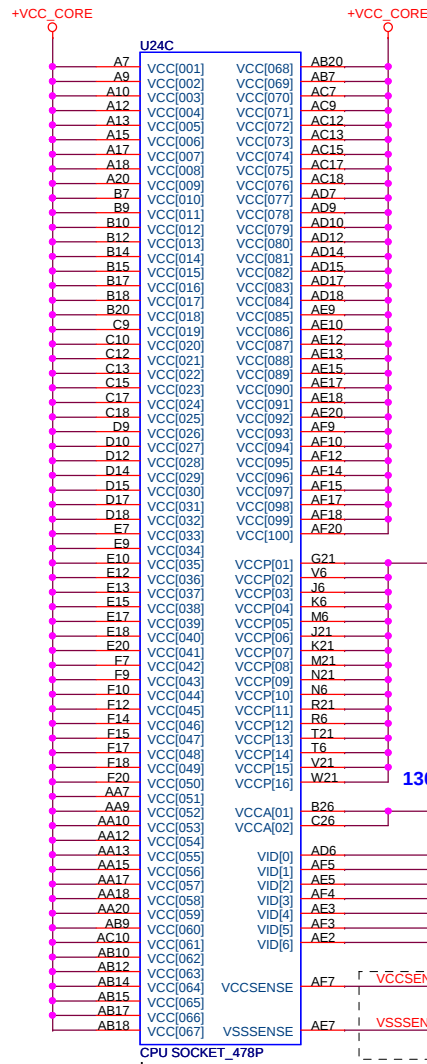
Place close to CPU

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

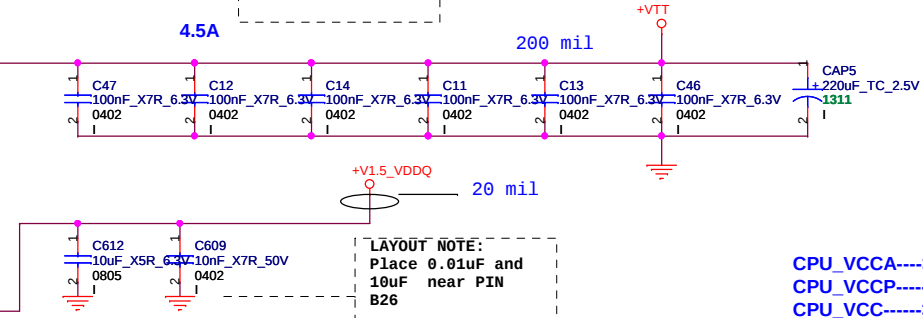


Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)





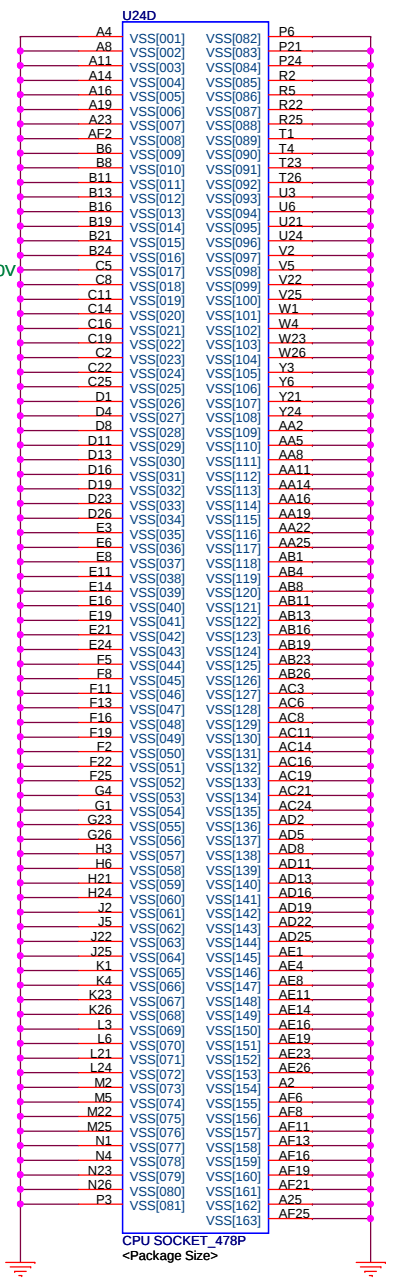
LAYOUT NOTE:
Place 0.1uF in
CPU center cavity
in 2 rows.



LAYOUT NOTE:
Place 0.01uF and
10uF near PIN
B26

CPU_VCCA---->0.13A
CPU_VCCP---->4.5A
CPU_VCC---->47A

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.



Outer width=18 mil spacing=7 mil
Inner width=14 mil spacing=7 mil
Length match < 25 mil



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Title

Penryn (POWER/GROUND) 3/3

Size

Document Number

Rev

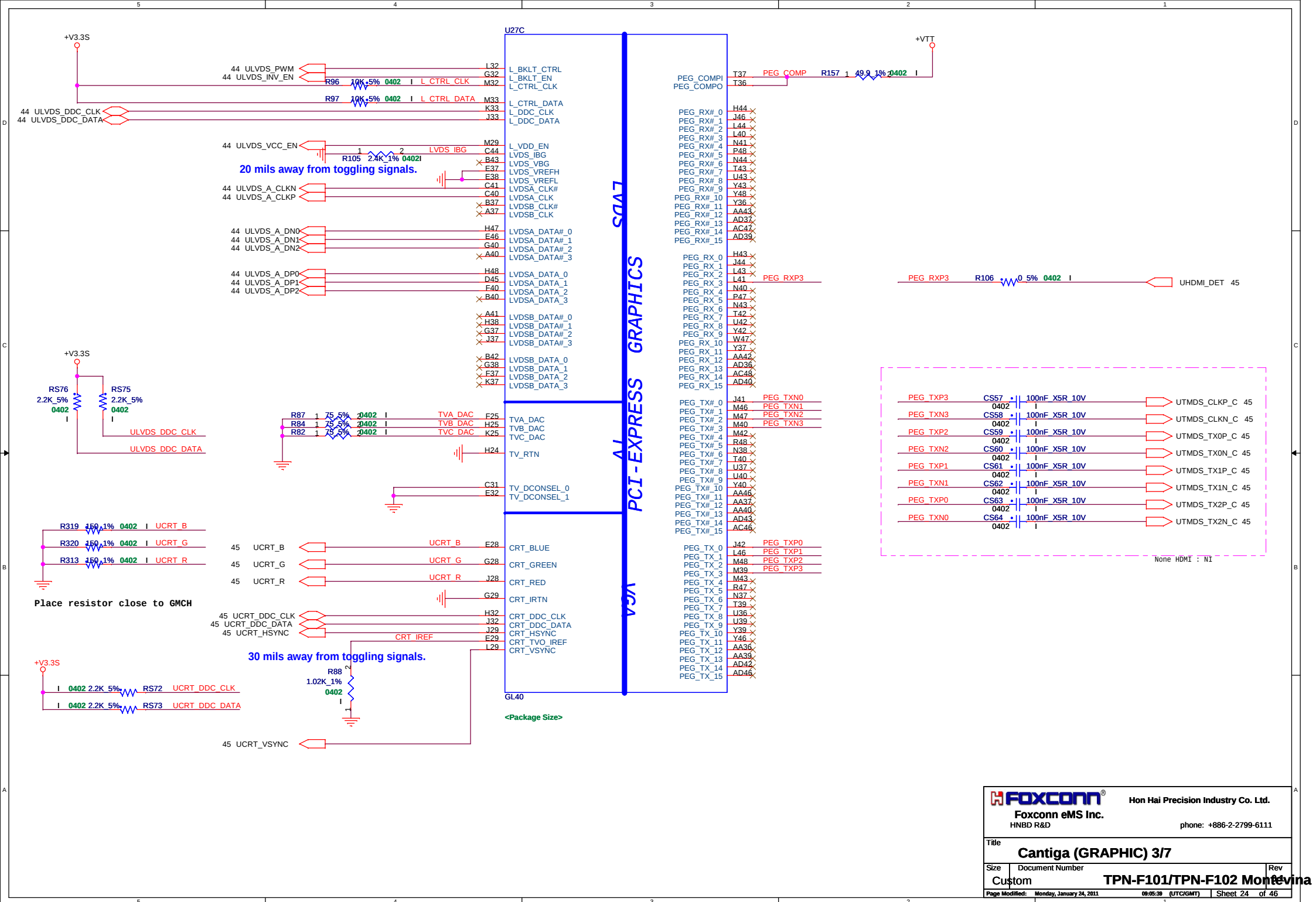
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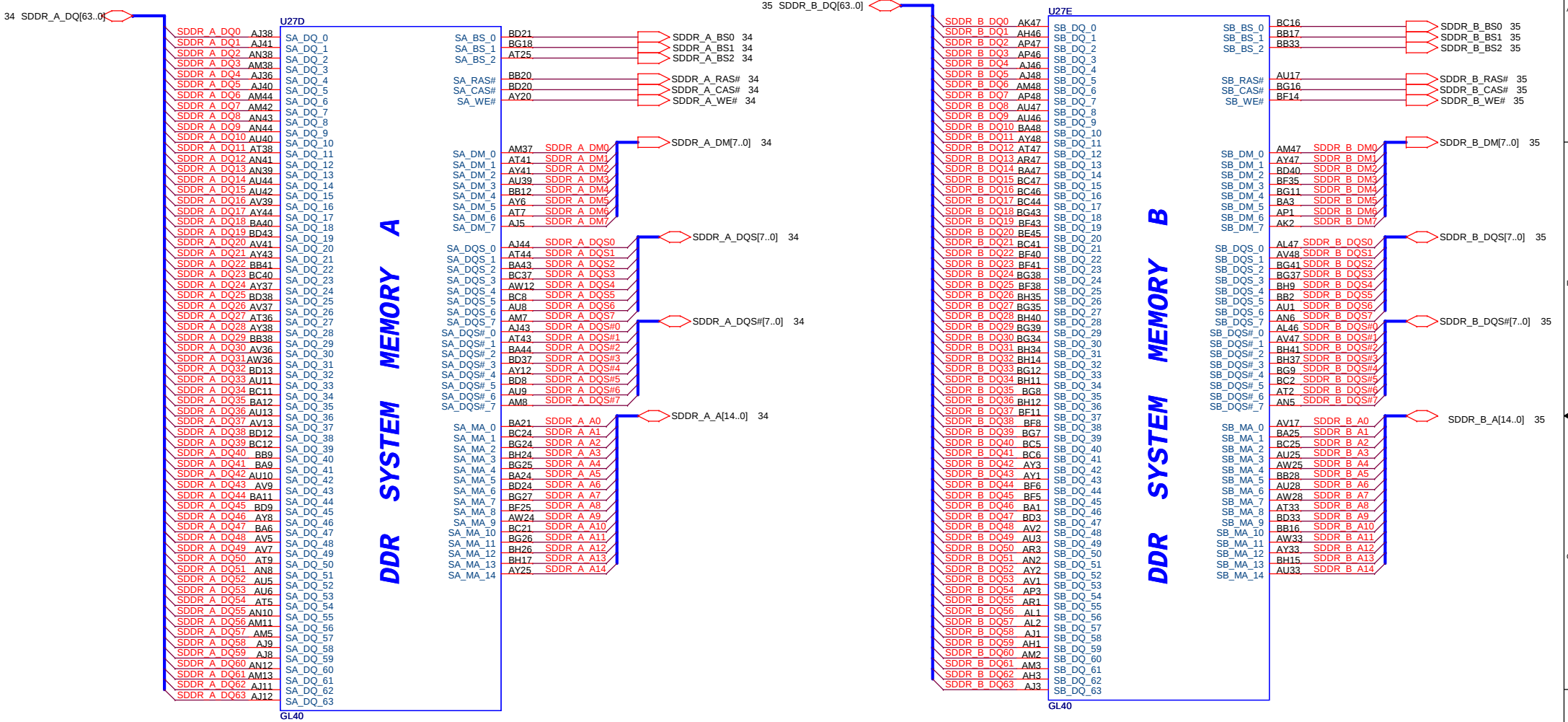
TPN-F101/TPN-F102 Montevina

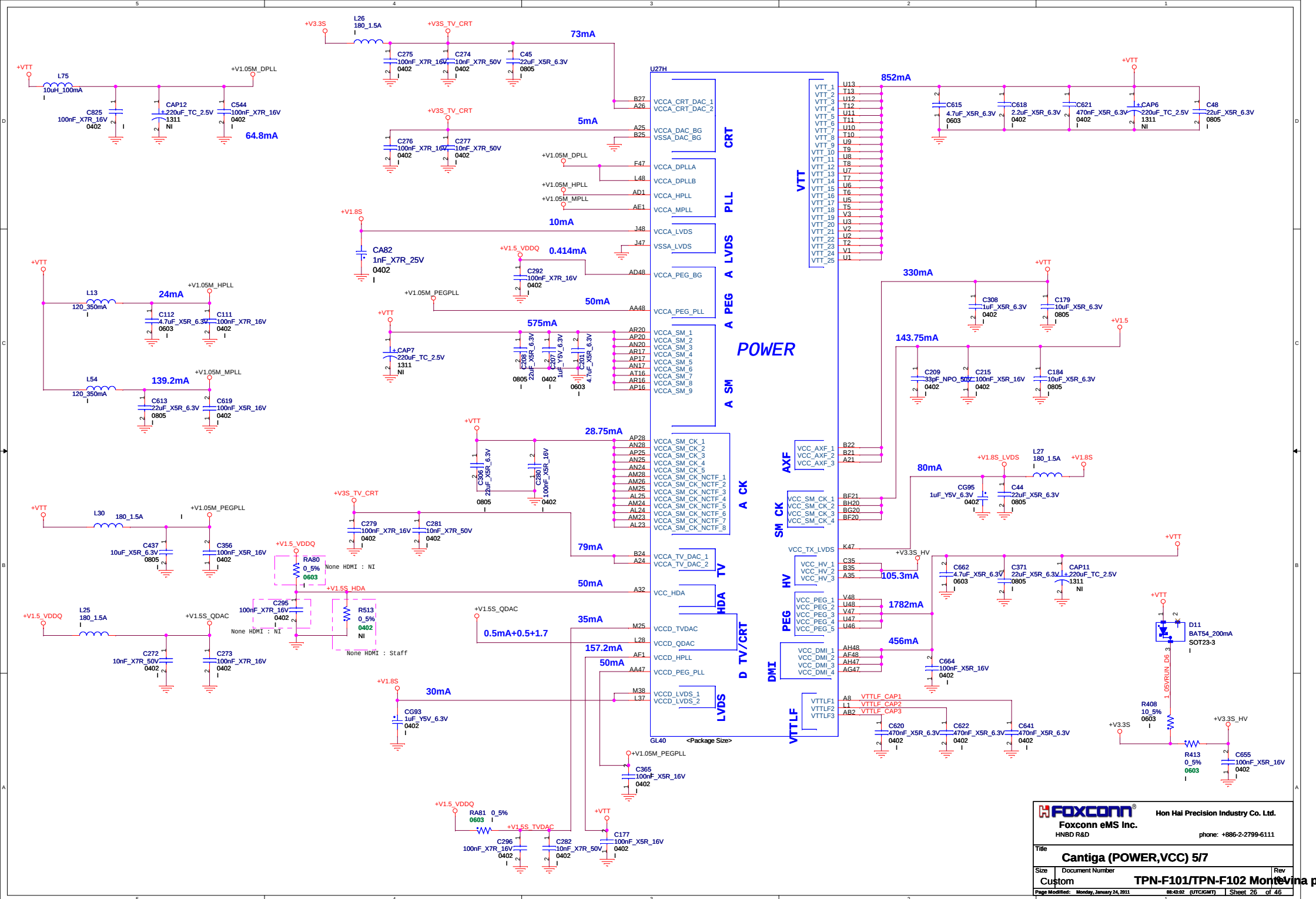
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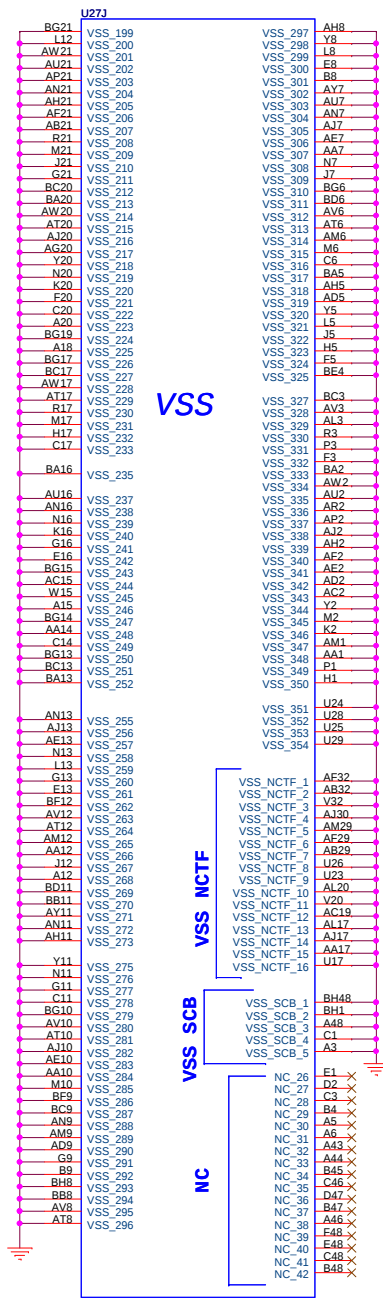
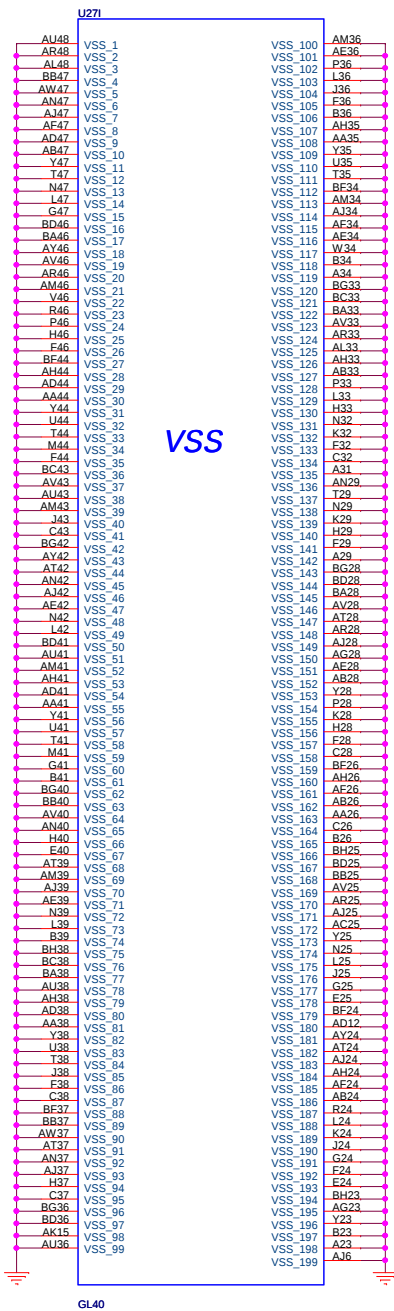
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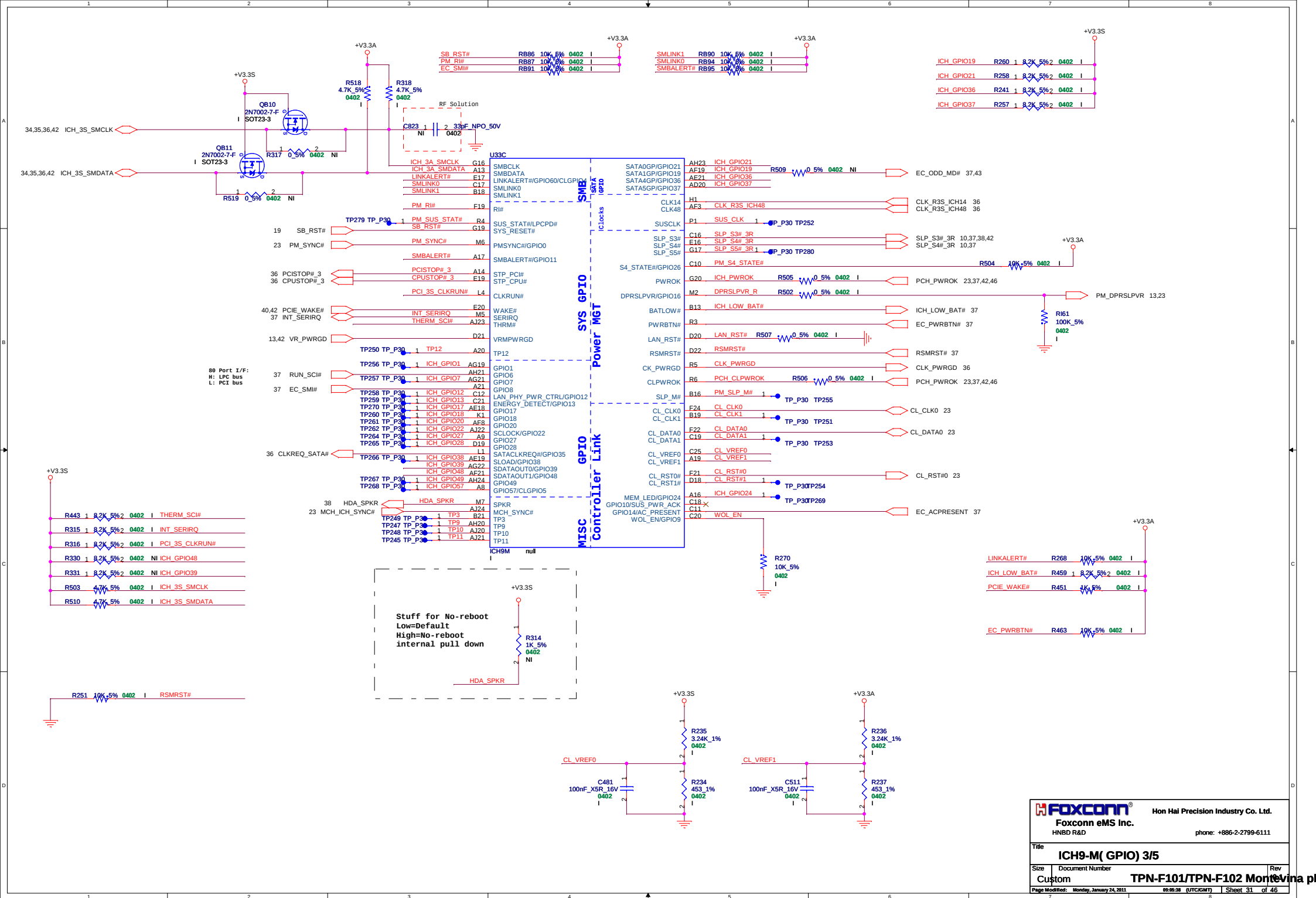
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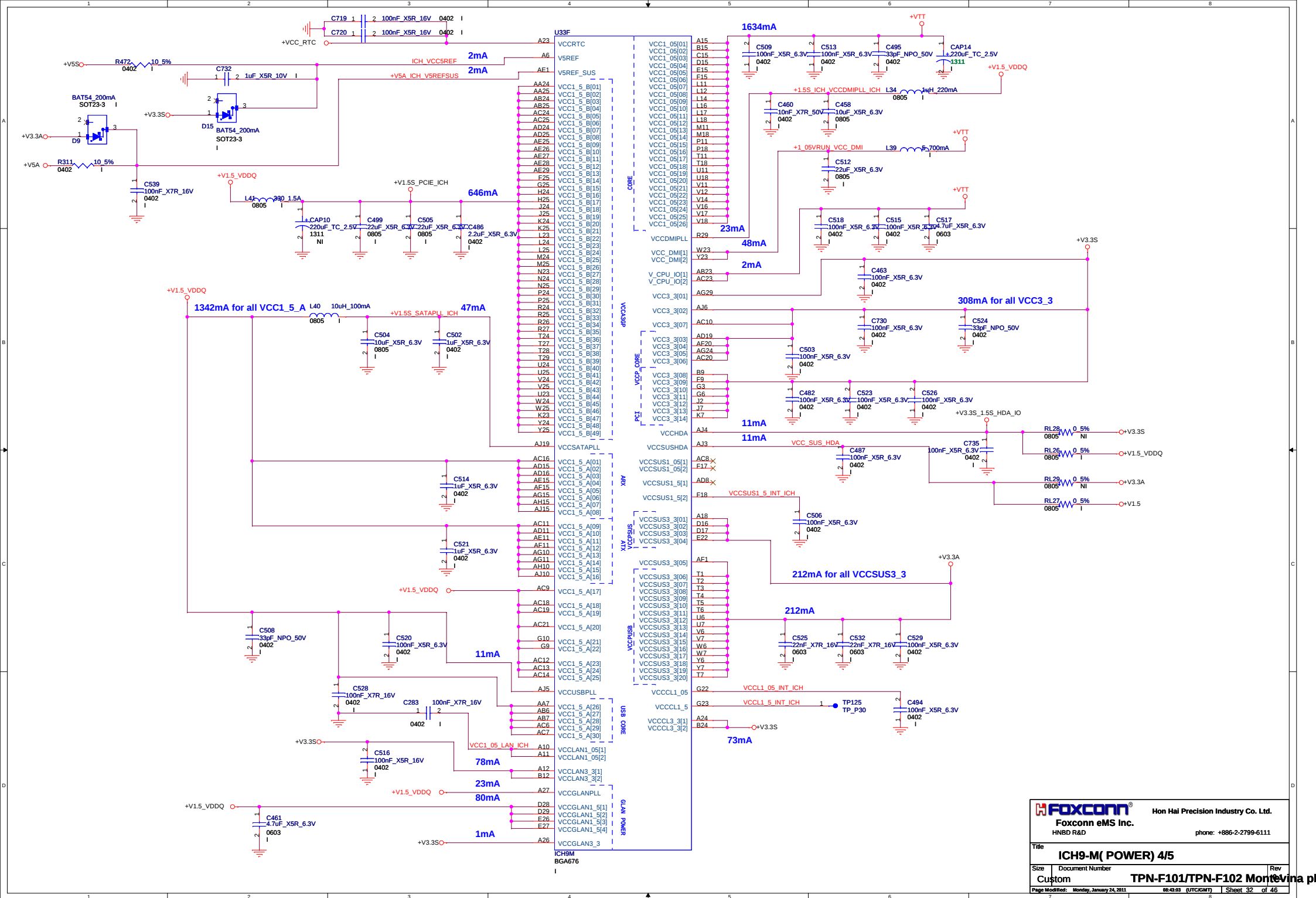


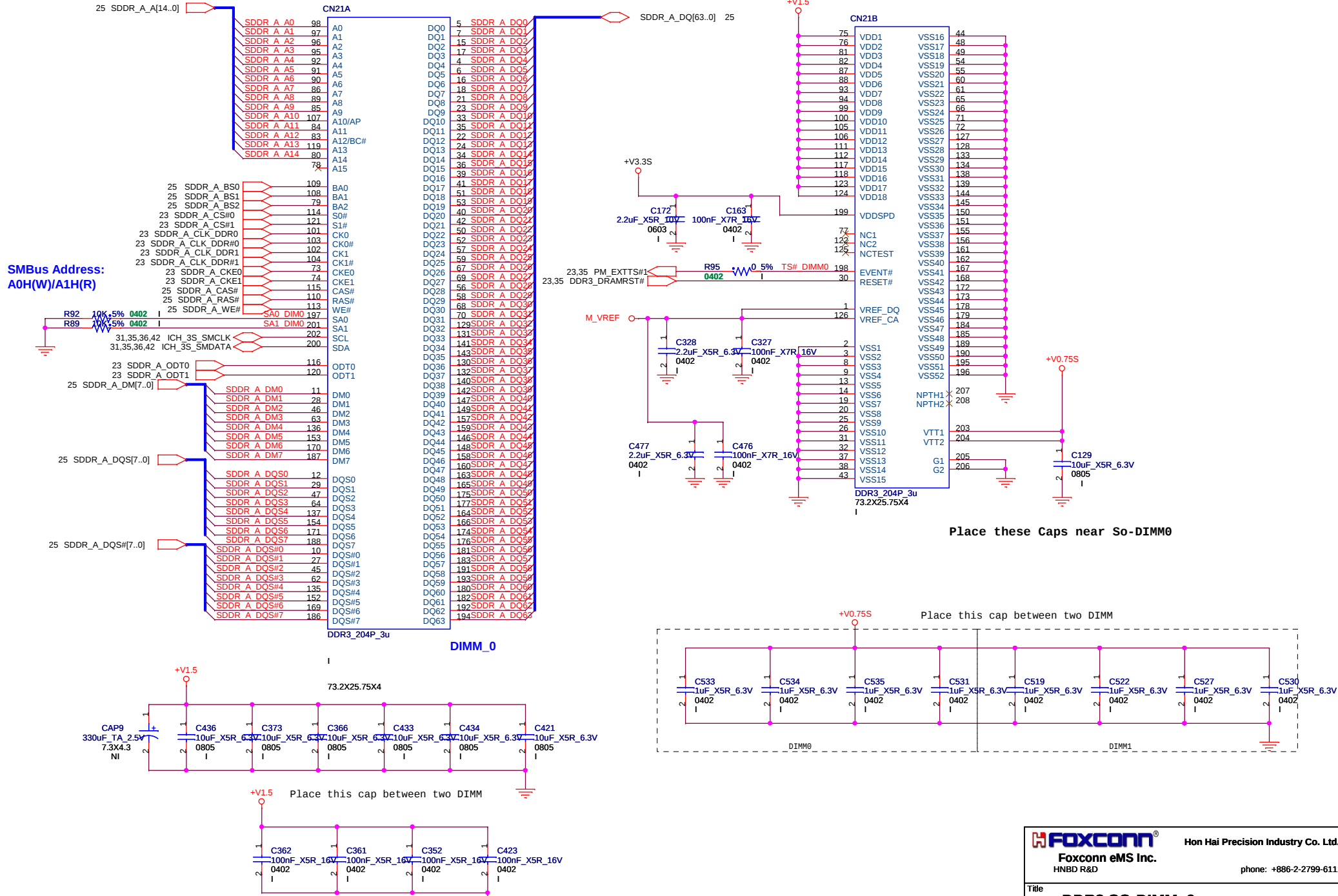


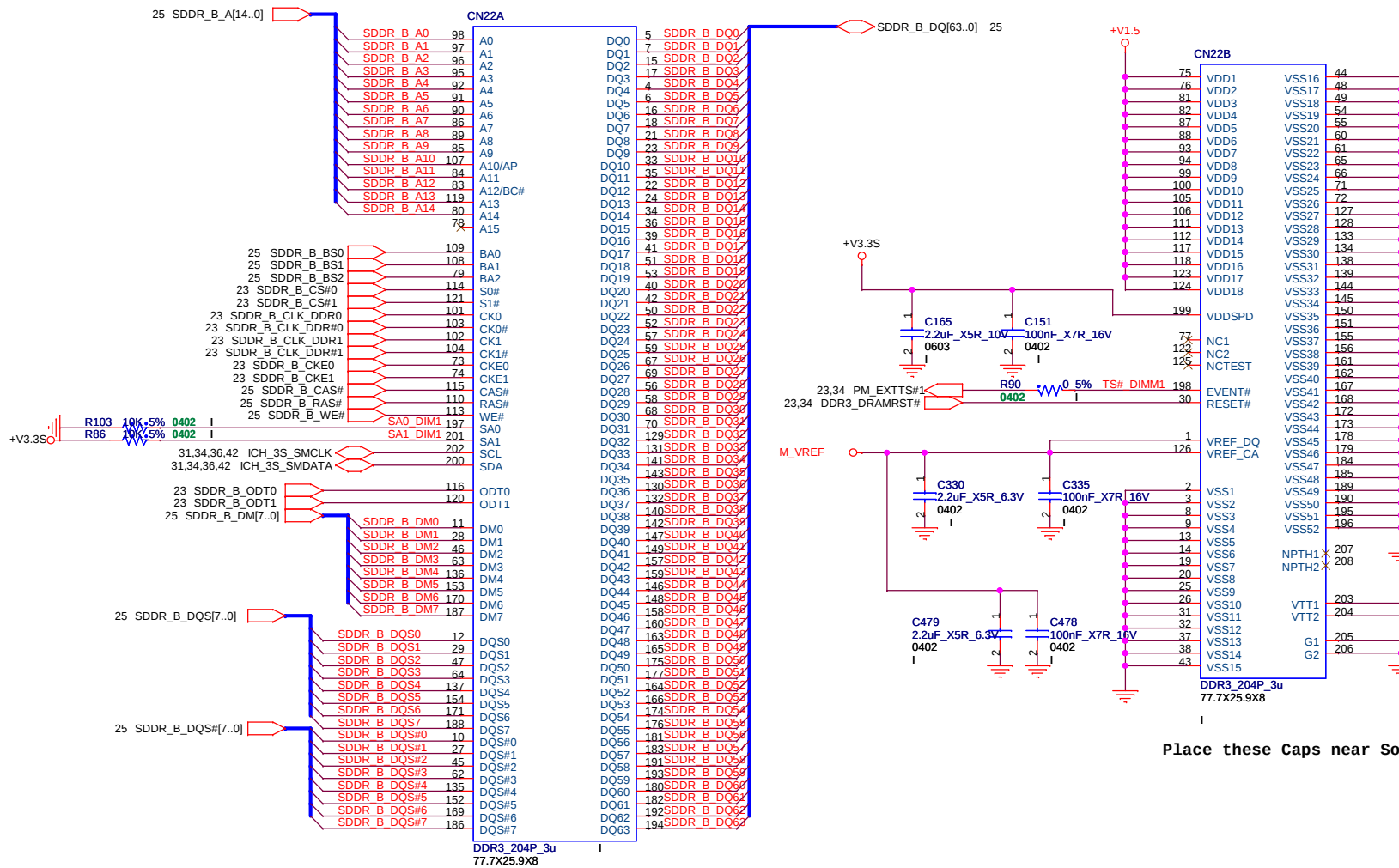




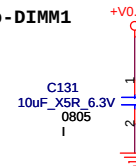


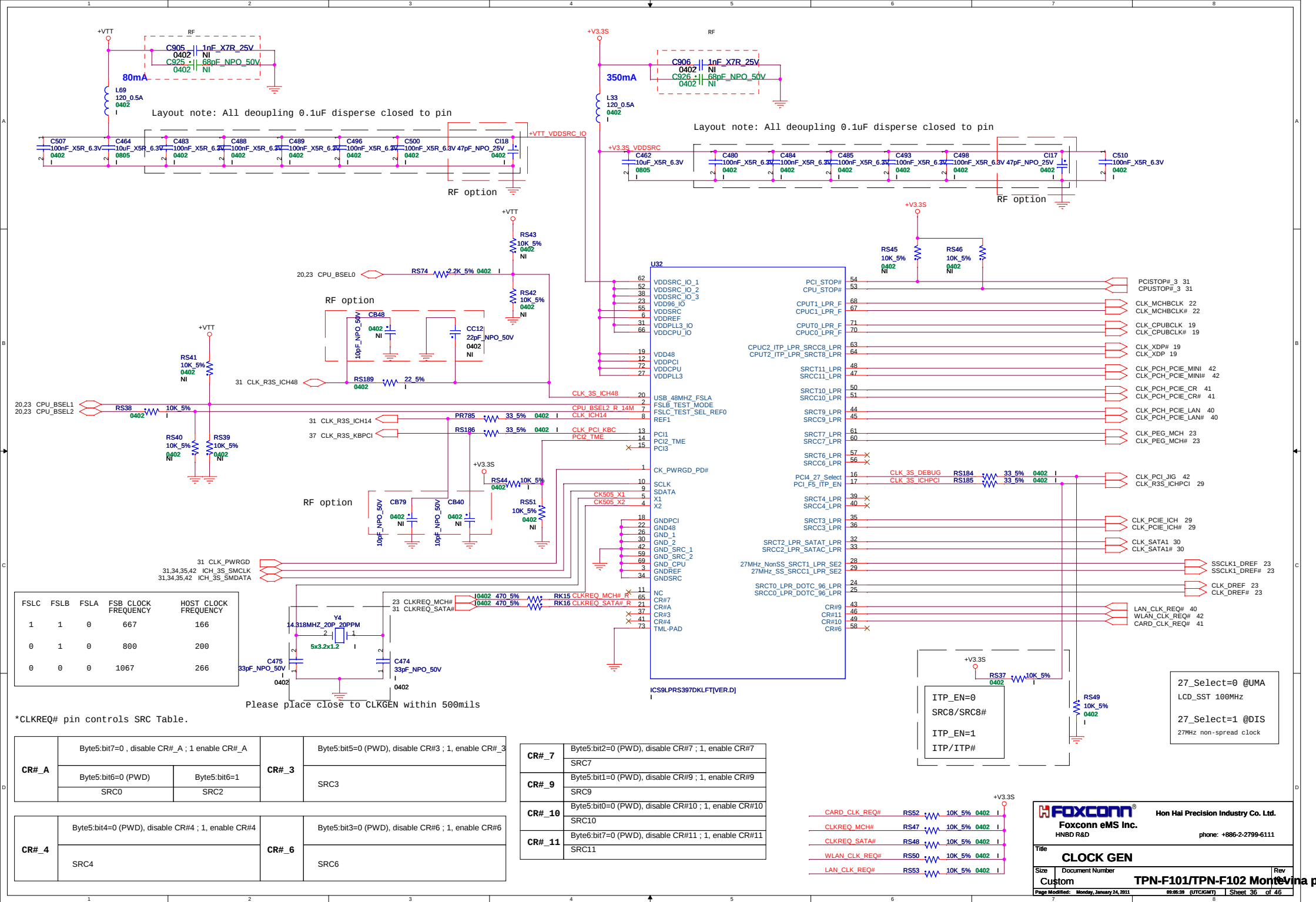


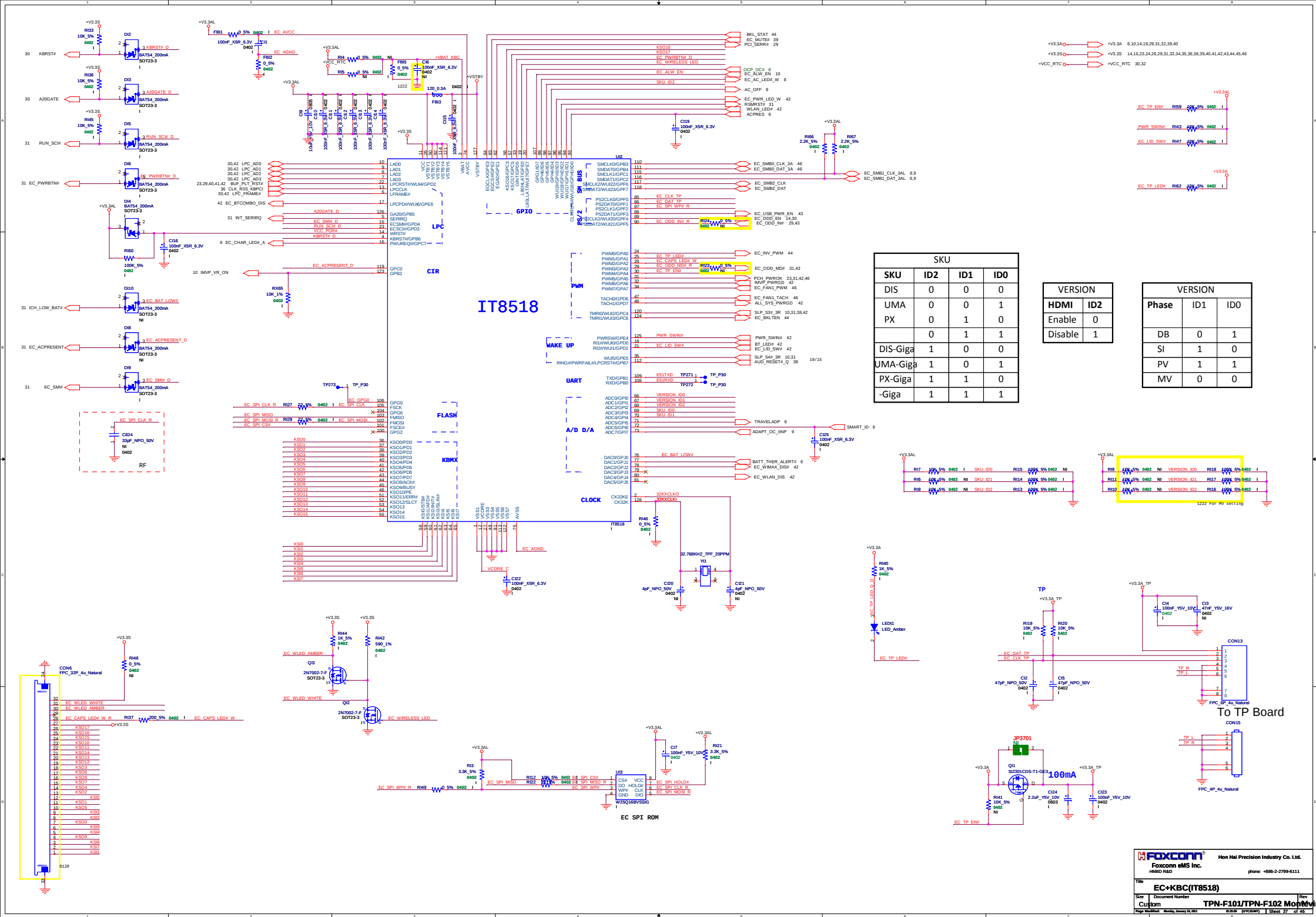


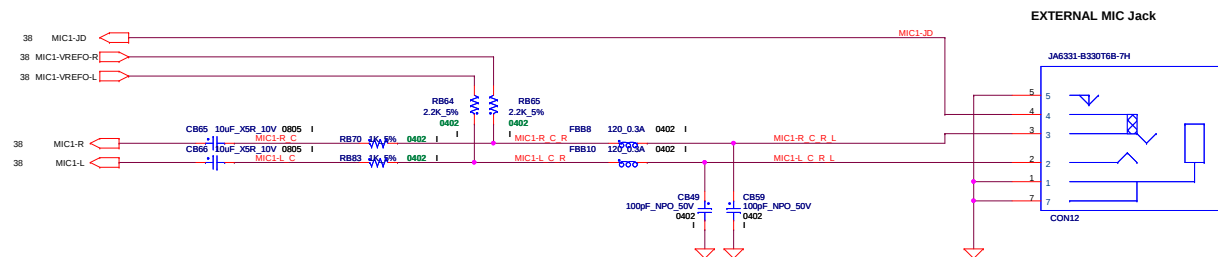
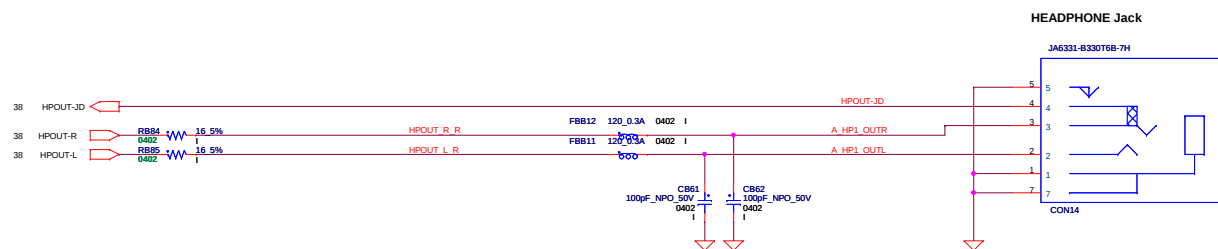
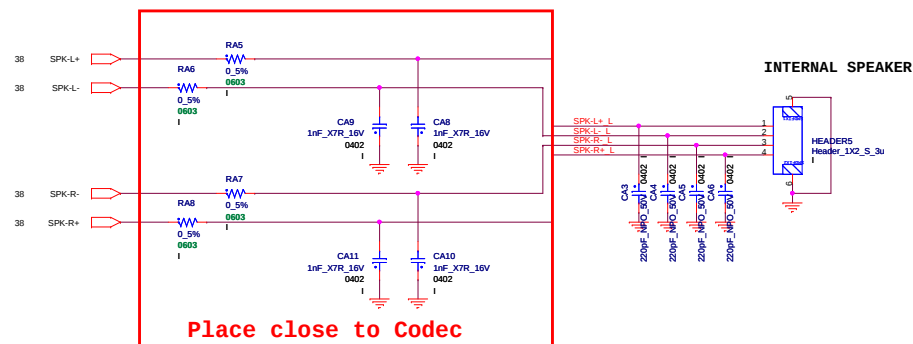
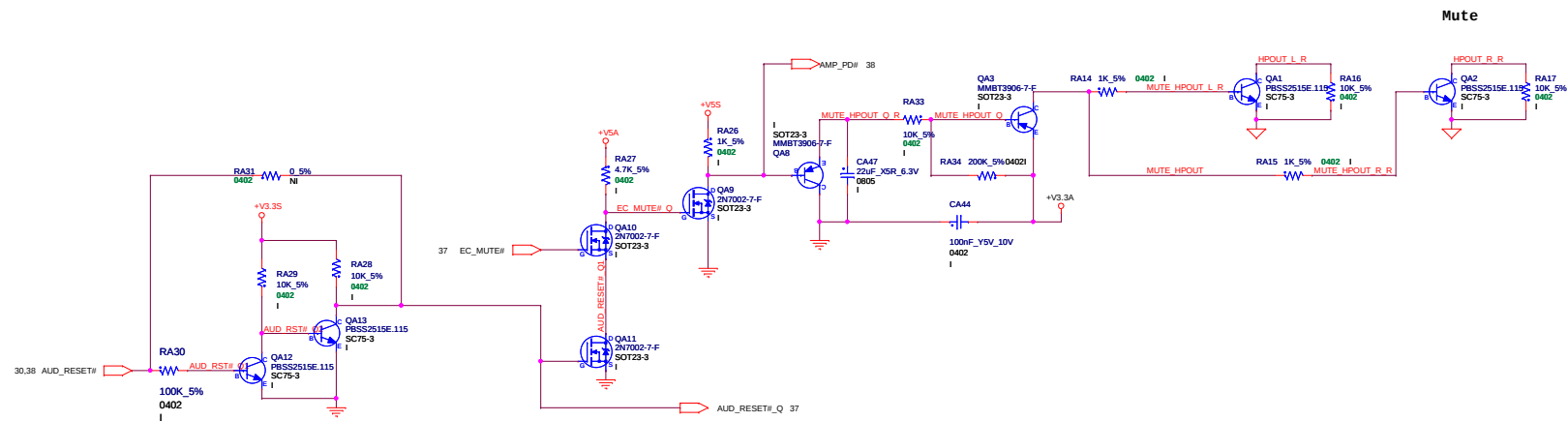


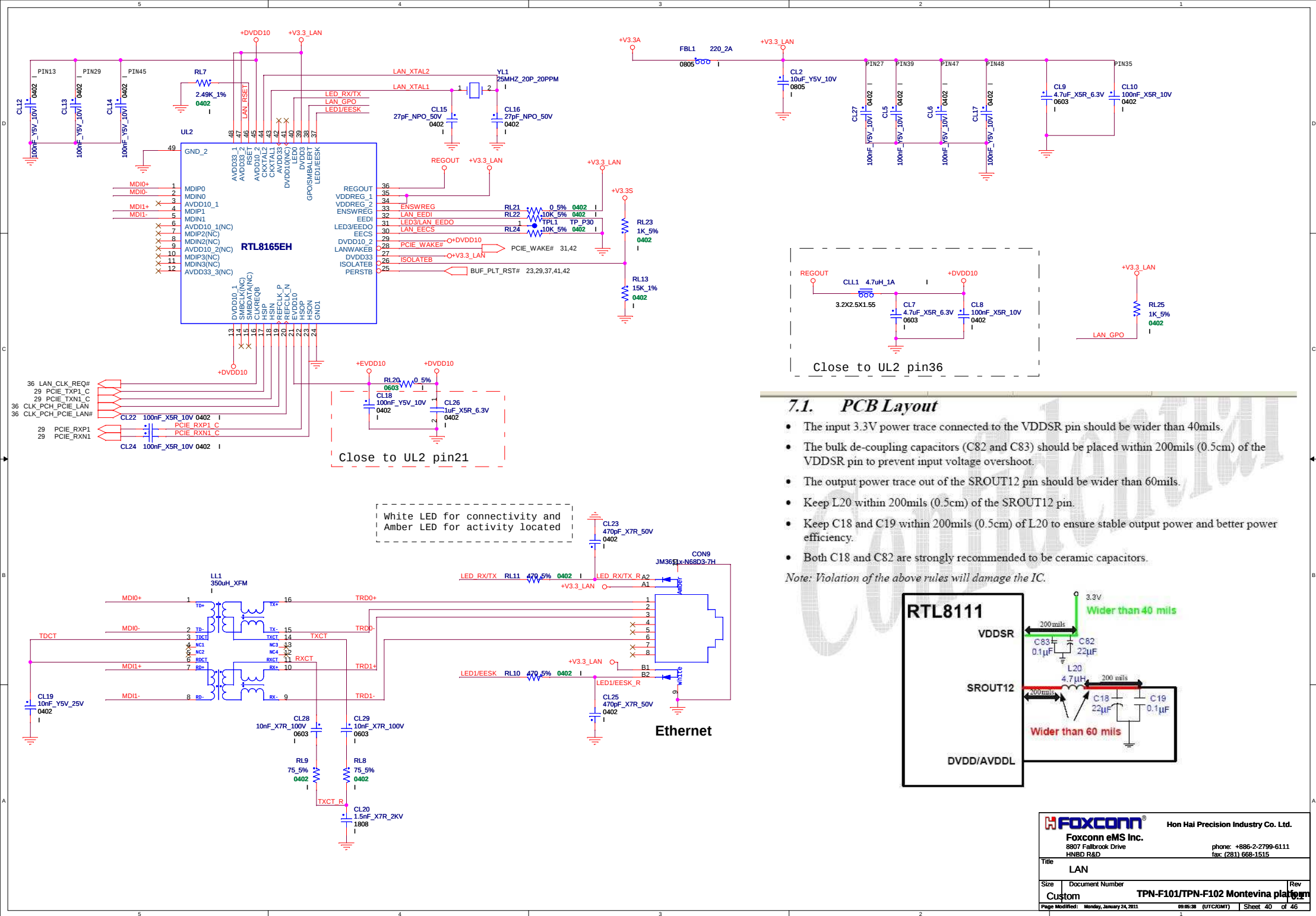
Place these Caps near So-DIMM1

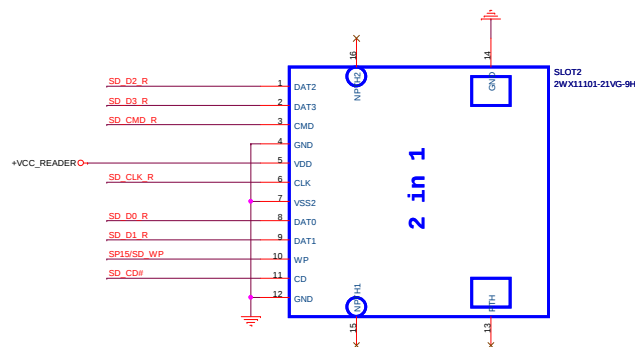
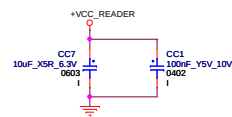
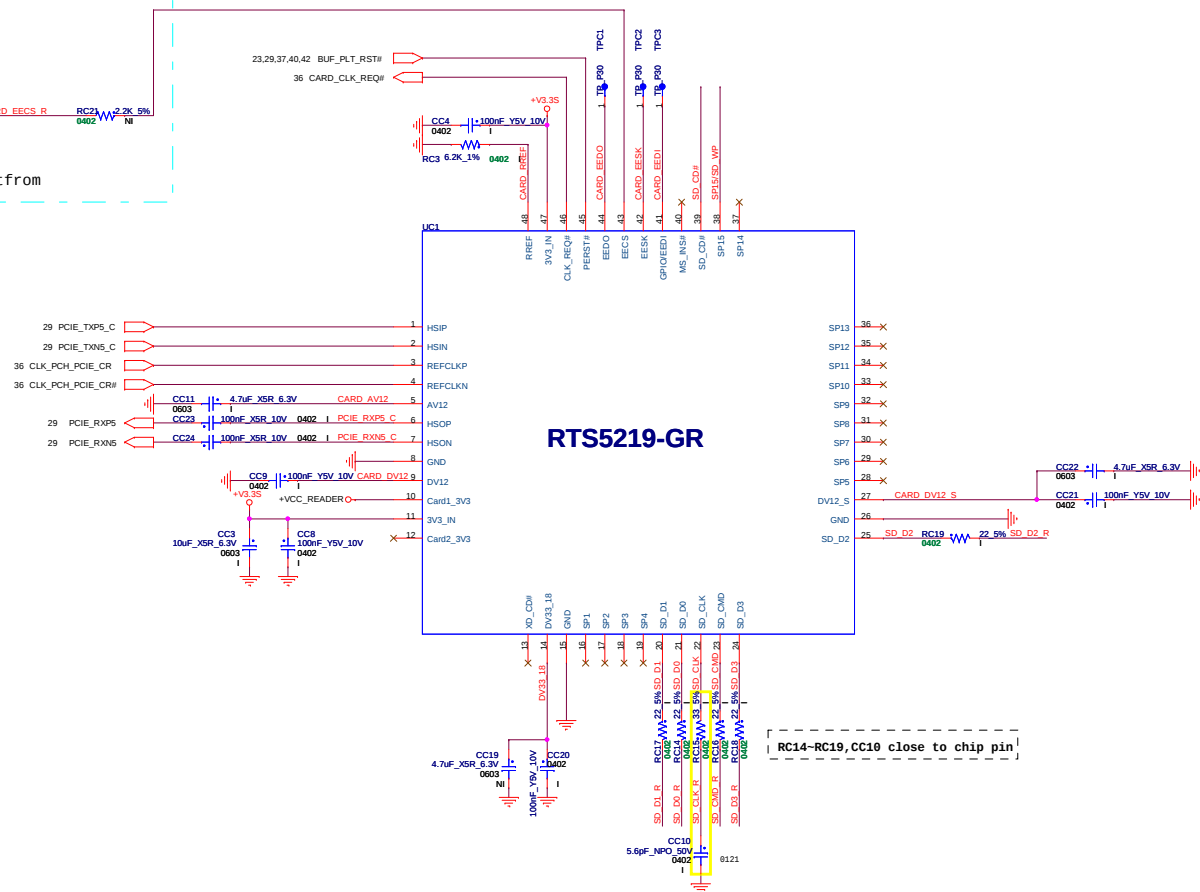
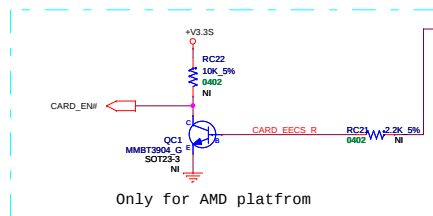


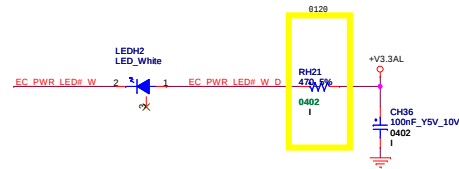






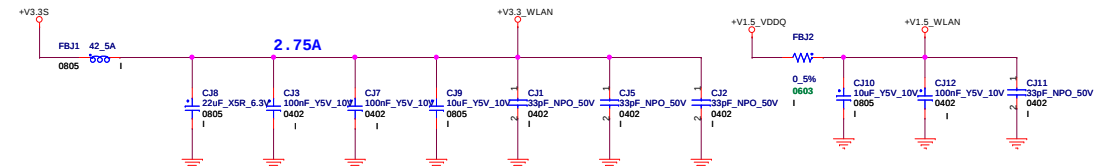
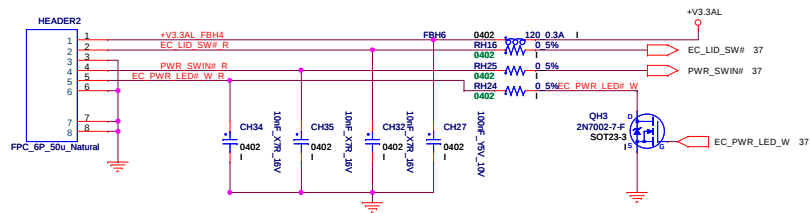




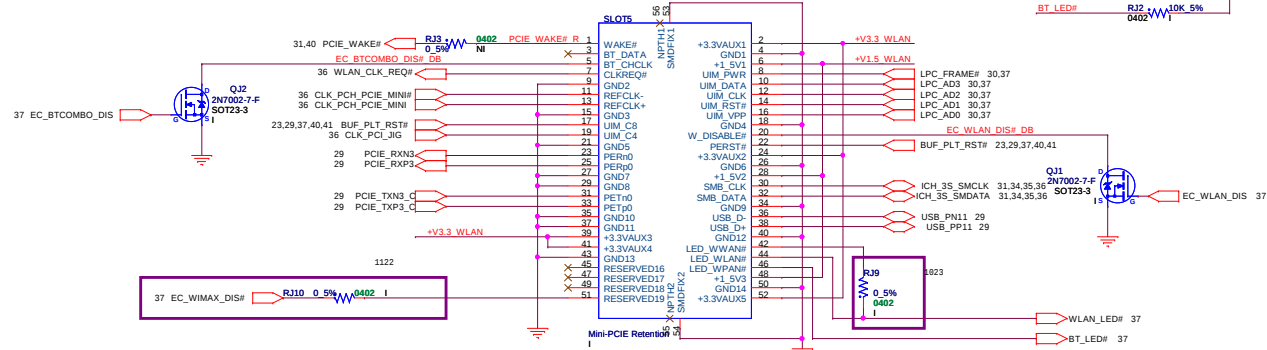


PWR LED

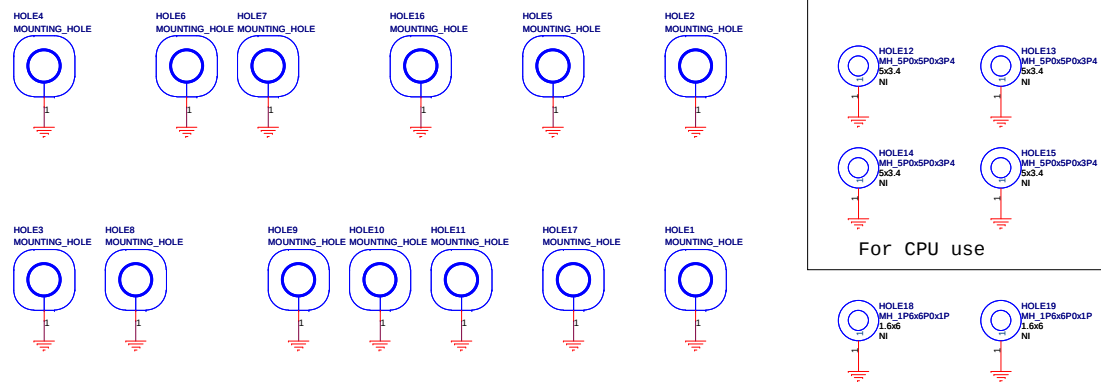
PWR Board CONN.



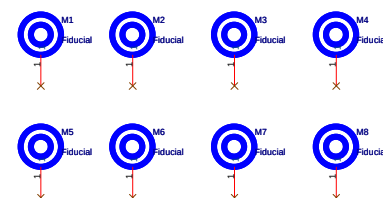
+1.5V=>0.5A Peak/0.375A Normal
+3.3Vaux=>2.75A Peak/1.1A Normal



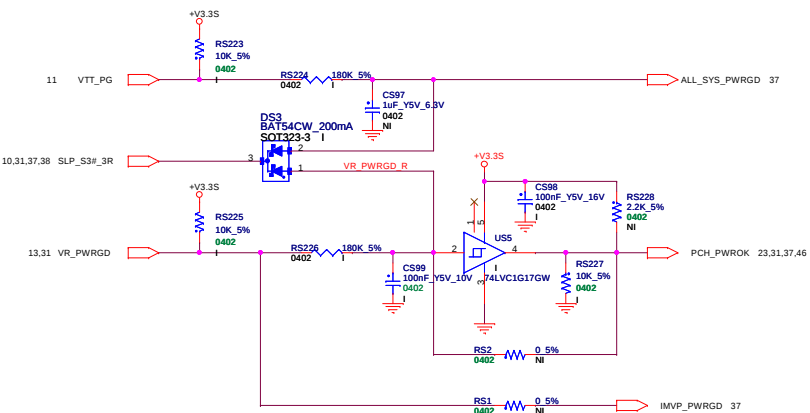
Half Mini Card for WLAN



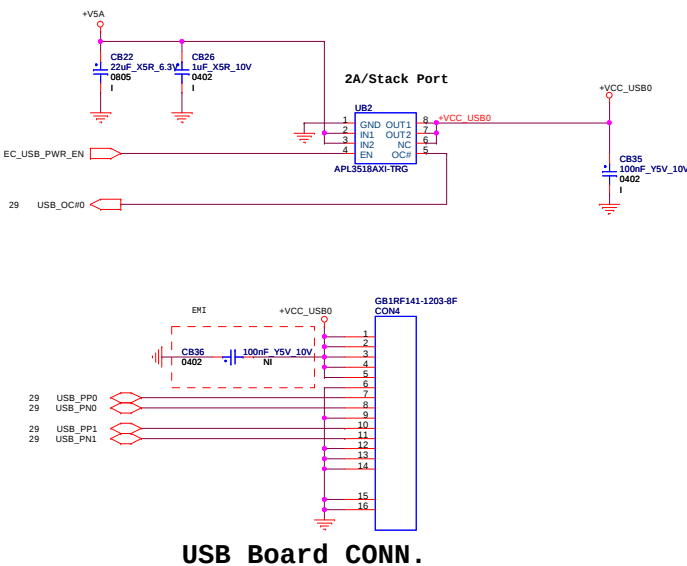
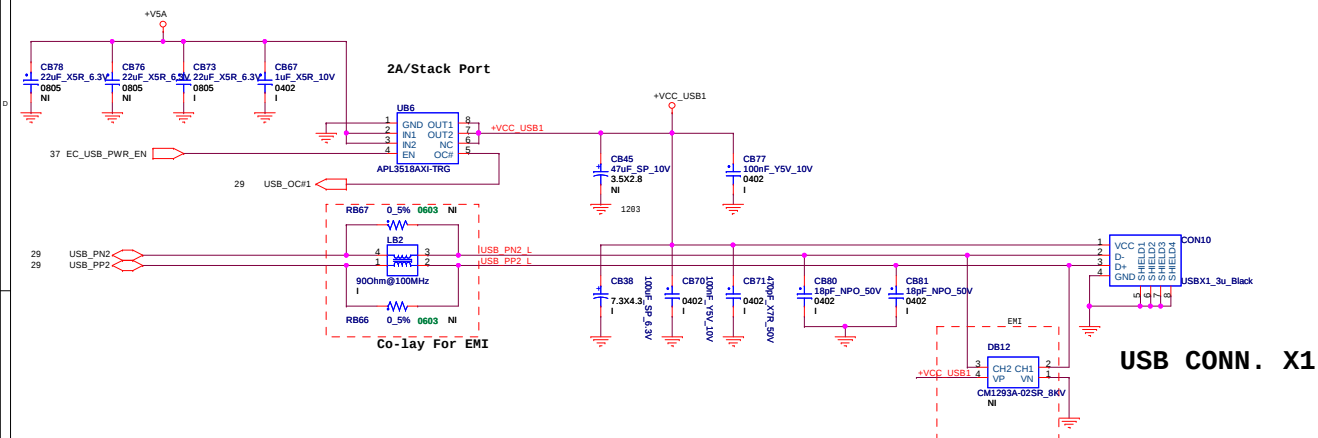
Mounting HOLE



Fiducial Mark



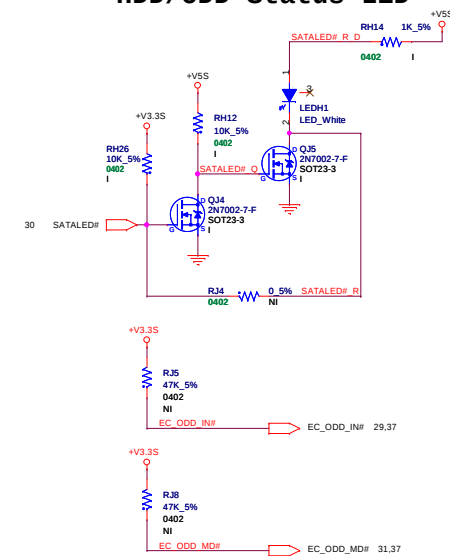
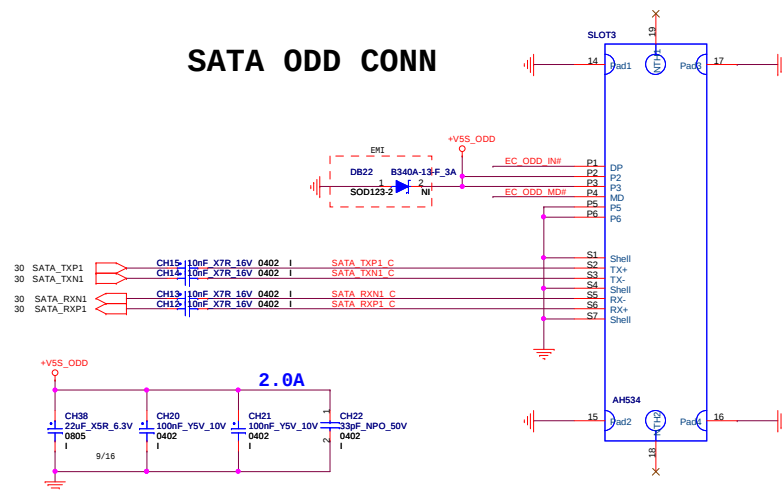
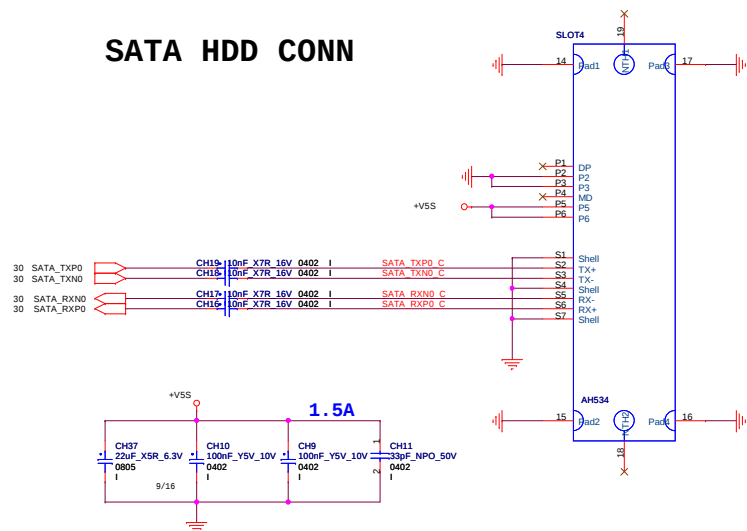
SEQUENCE CIRCUIT



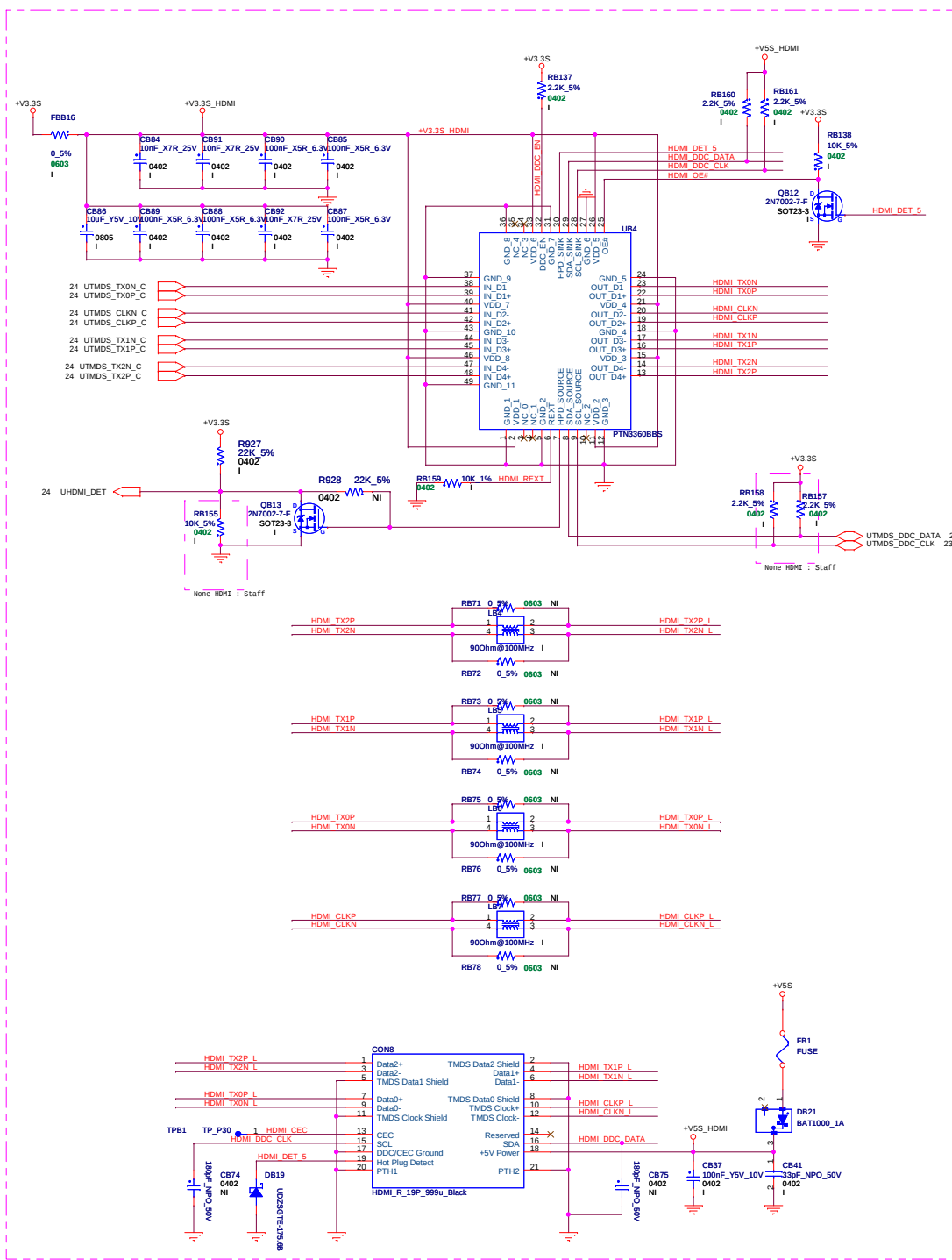
SATA HDD CONN

SATA ODD CONN

HDD/ODD Status LED

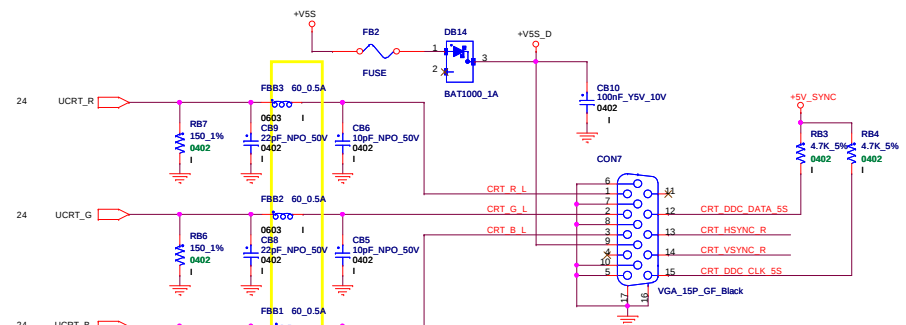
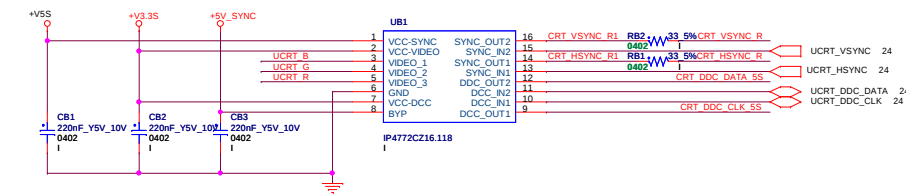


Power pin current
max. 1300 mA (less 2ms)



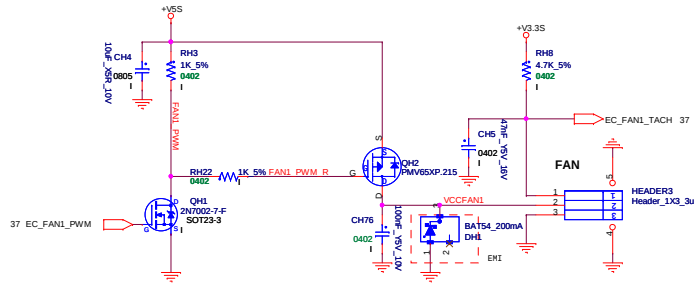
None HDMI : NI

CRT

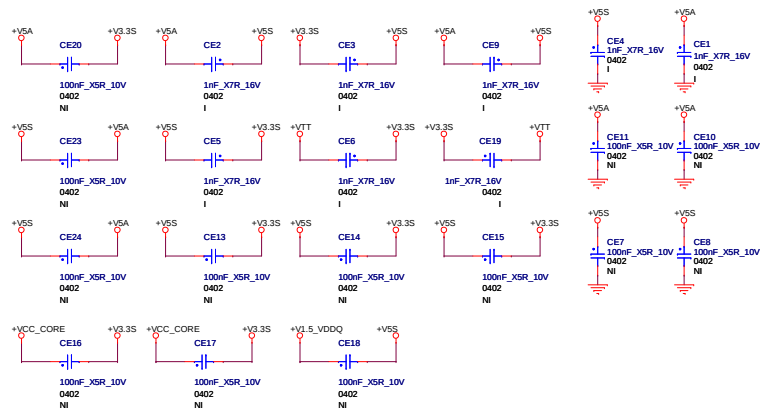
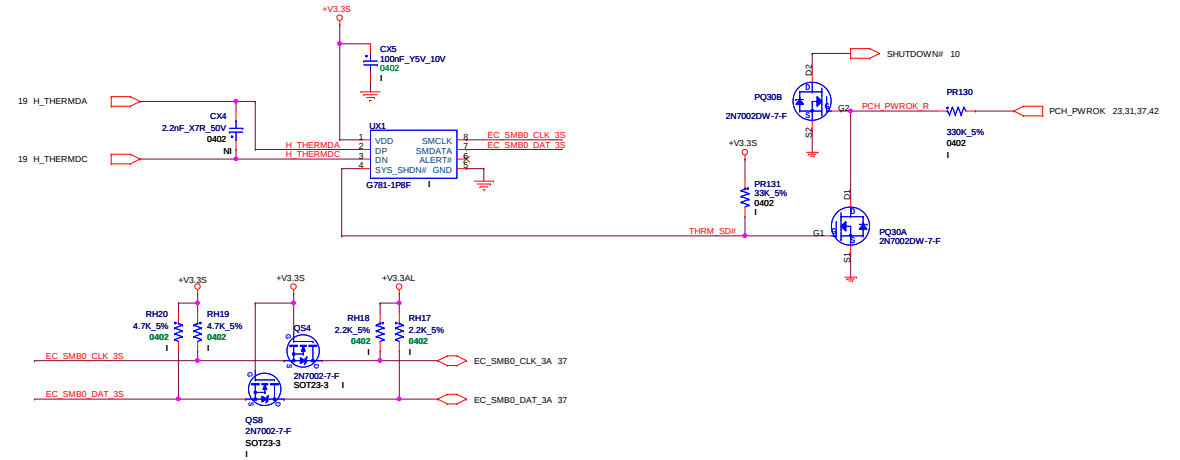


CRT CONNECTOR

FAN



THERMAL SENSOR



stitch cap

RF Solution