Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel Crestline_PM+ICH8-M core logic

IBT00 LA-3261P UMA

2007-03-28 REV:1A (MV2)

機密	等級	硬體二部
		產出人員
		產出日期
		解密日期

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Title: *Cover Sheet*

Size: Custom | Document Number: *LA-3261P UMA* | Rev: 0.4

Date: Wednesday, March 28, 2007 | Sheet 1 of 55

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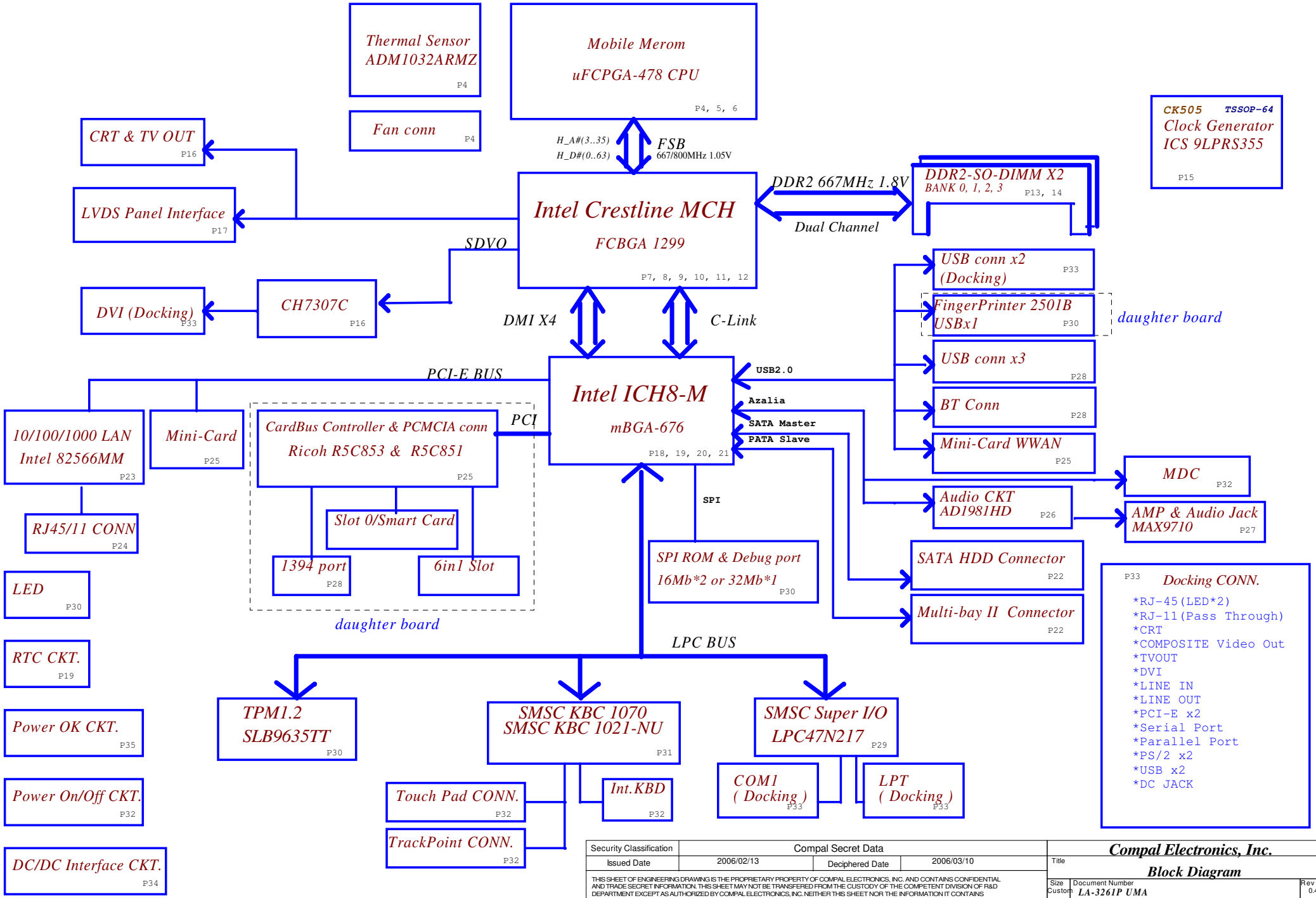
File Name : LA-3261P

Chimay UMA



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Title: Block Diagram

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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/ Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up0 (Right side)
1	Fingerprint
2	Reserve
3	WWAN
4	Walk-up1 (Left Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Reserve
8	Docking
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass strorage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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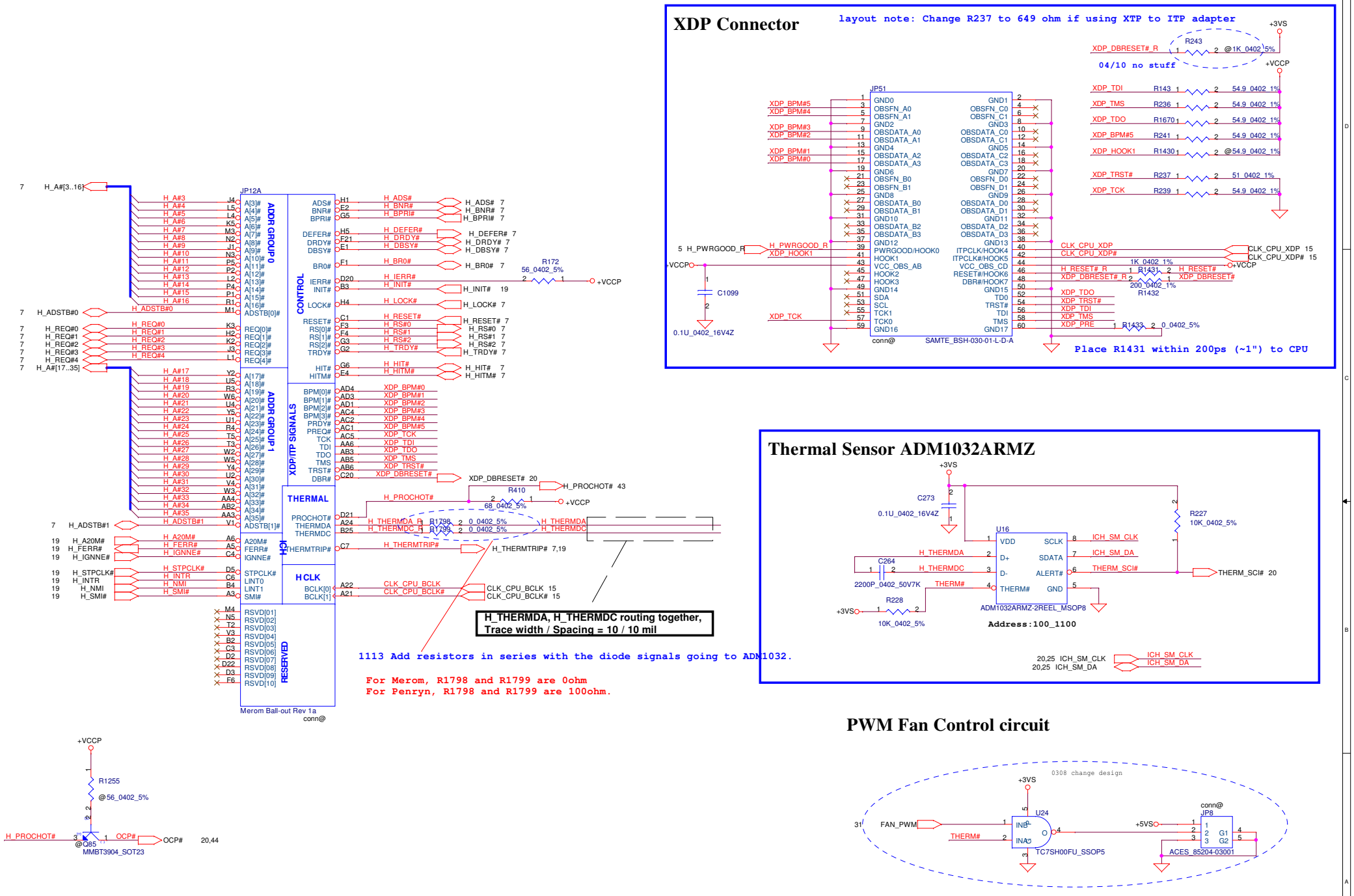

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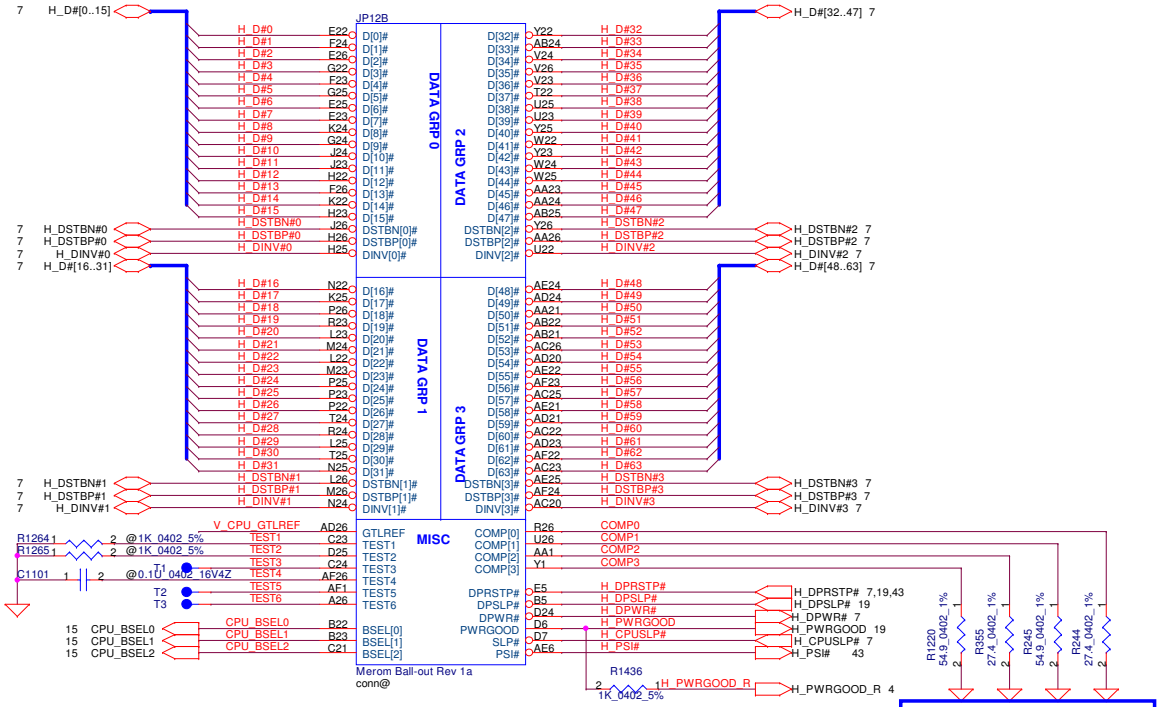
Title: Merom(1/3)-AGTL+/XDP

Size: Custom | Document Number: LA-3261P UMA | Rev: 0.4

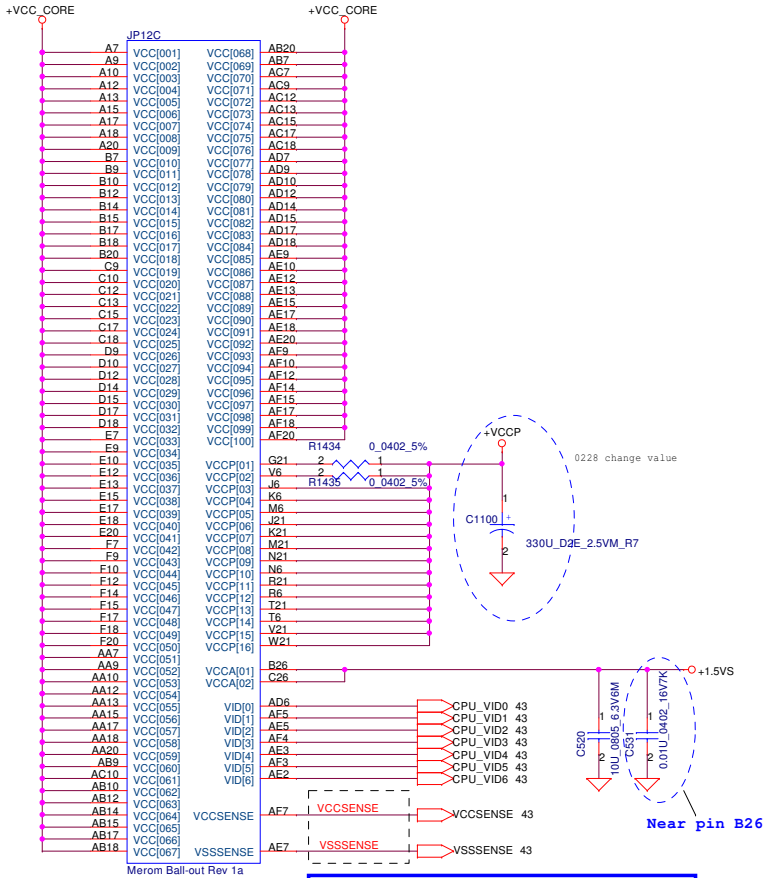
Date: Tuesday, March 27, 2007 | Sheet 4 of 55



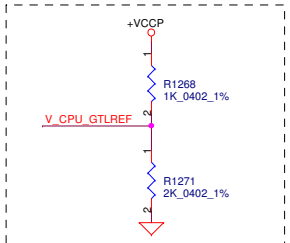
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

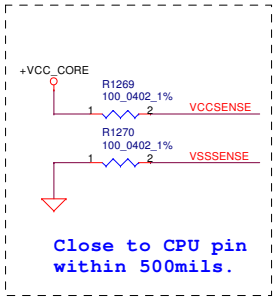
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

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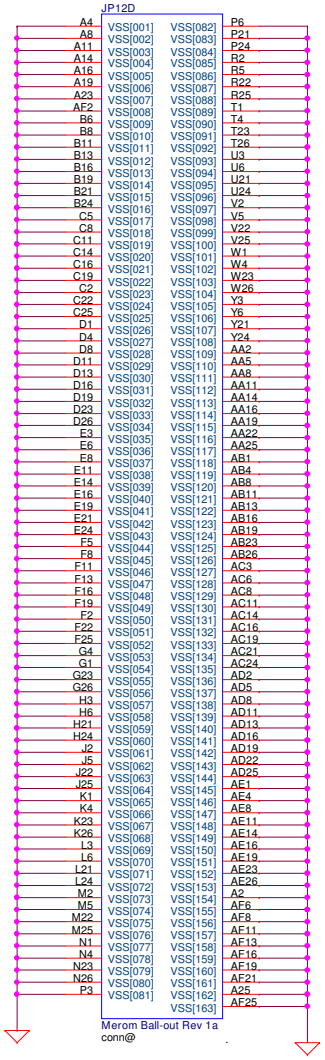
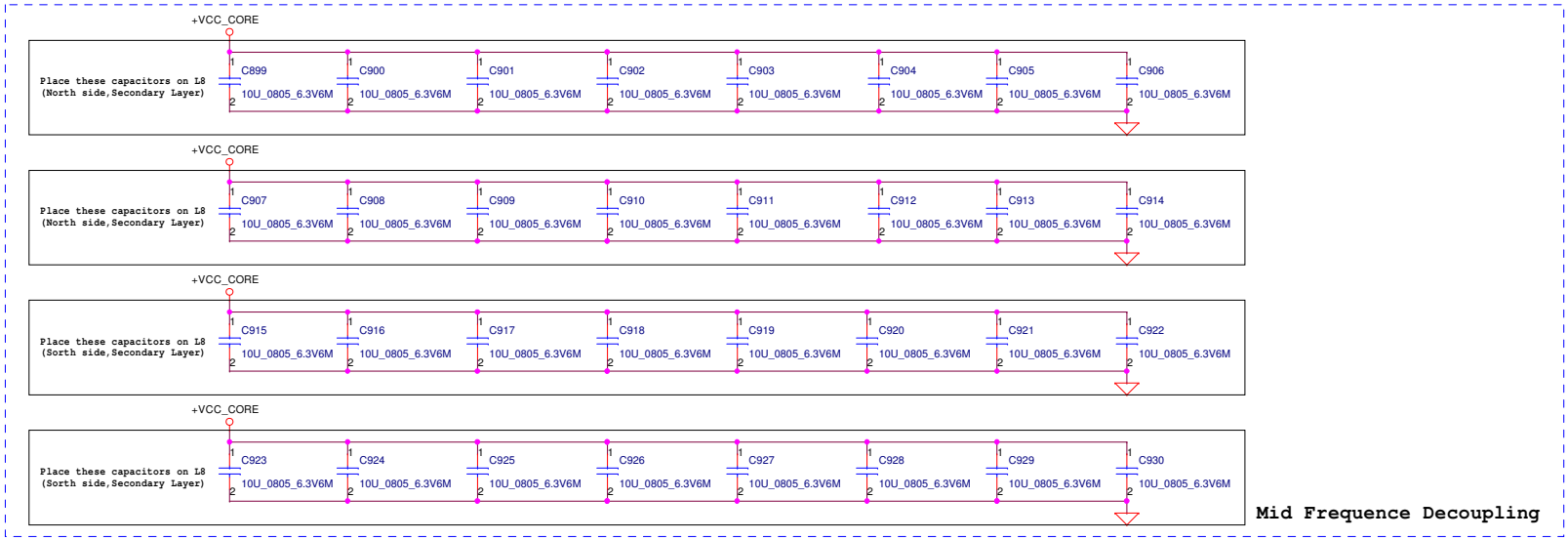
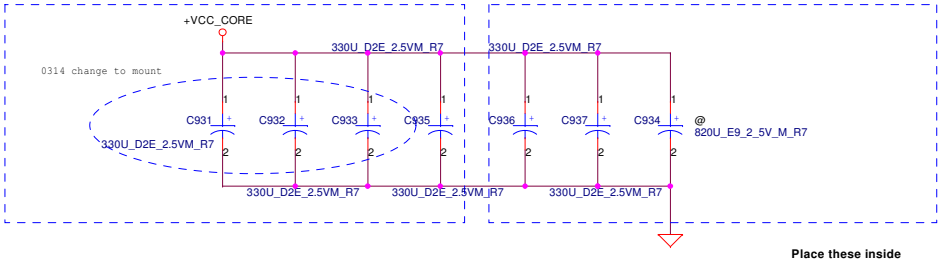
Date: Tuesday, March 27, 2007 | Sheet 5 of 55



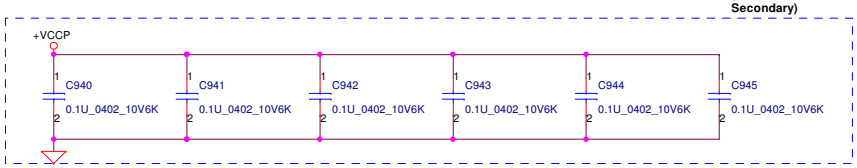


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Place these inside socket cavity on L8 (North side Secondary)



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Compal Electronics, Inc.

Title: **Merom(3/3)-GND&Bypass**

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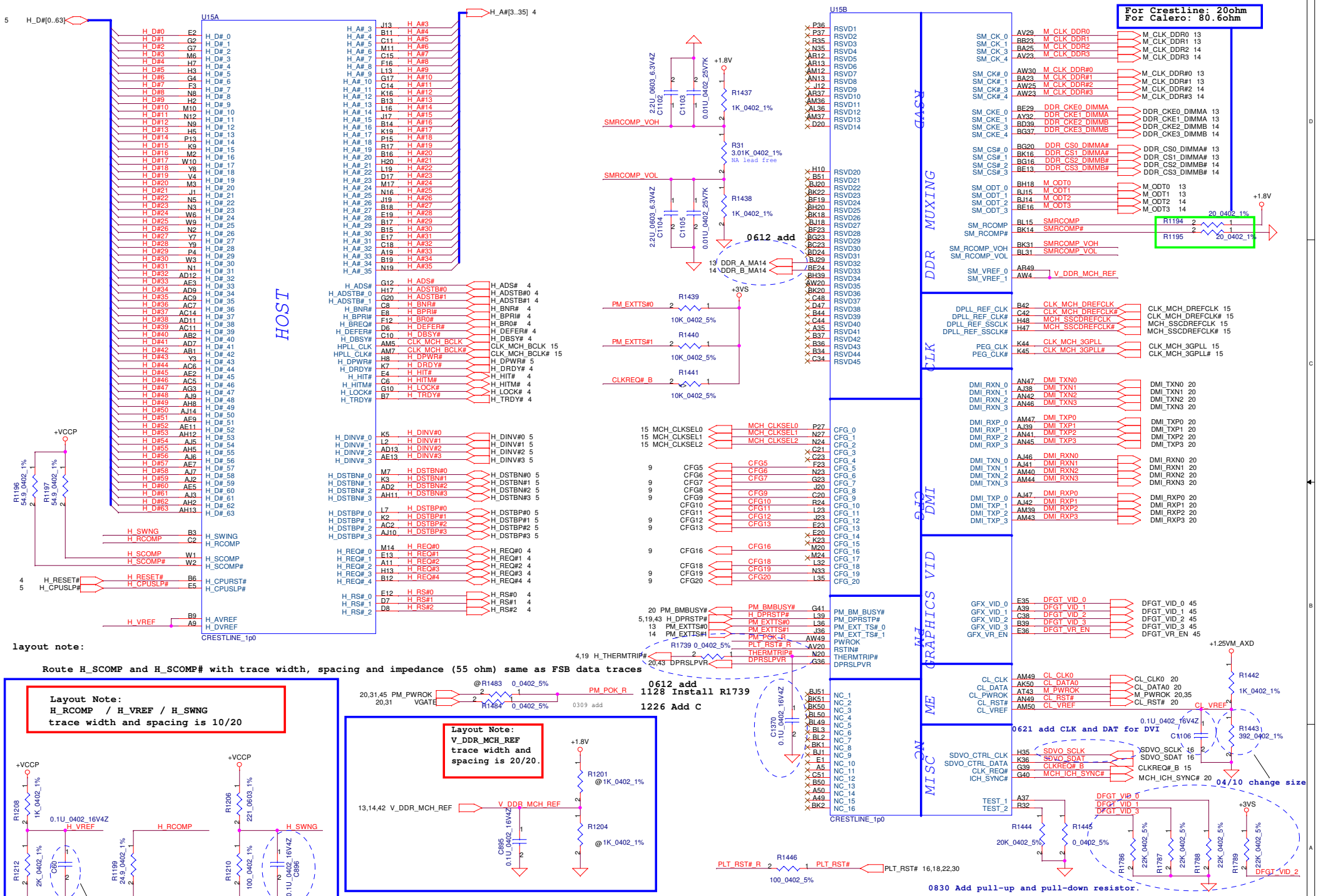

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Title: **CRESTLINE(1/6)-AGTL+/DMI/DDR2**

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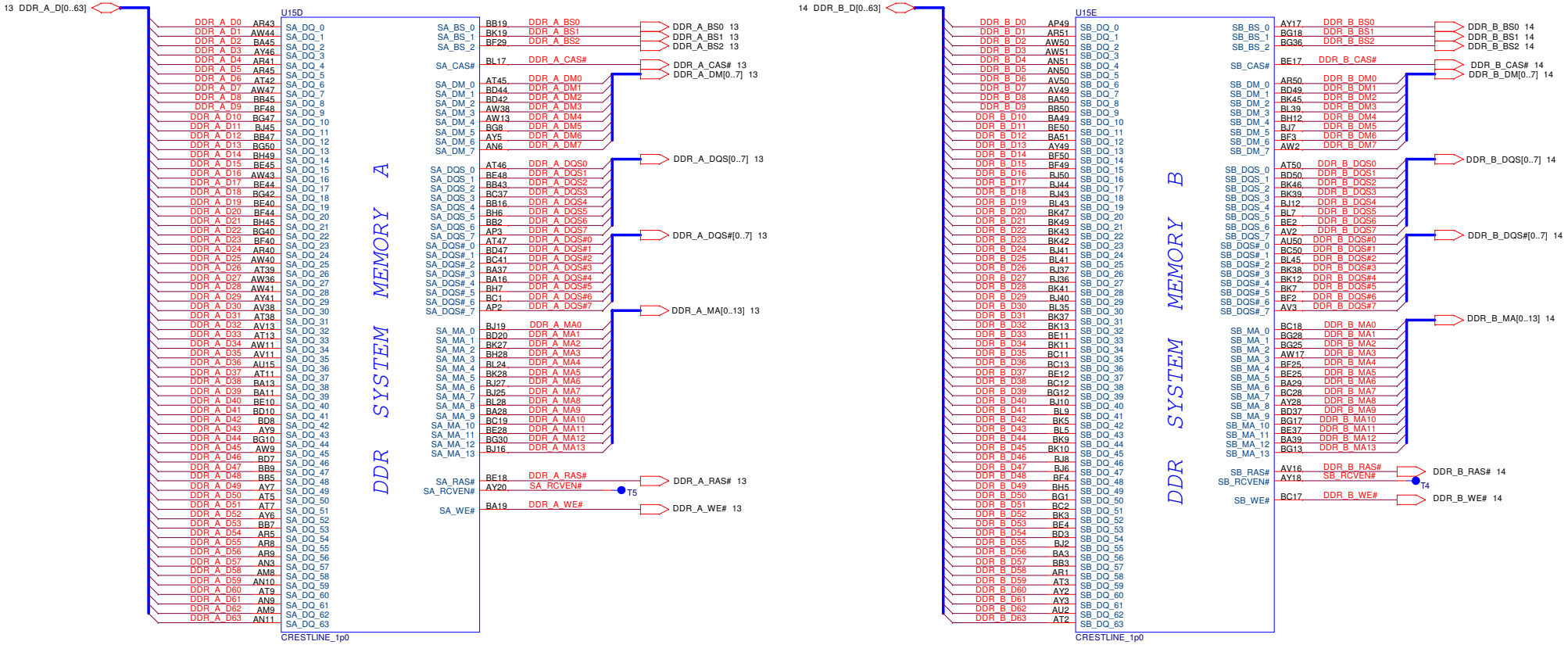
Date: Tuesday, March 27, 2007 | Sheet 7 of 55



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Compal Electronics, Inc.

Title: **CRESTLINE((2/6)-DDR2 A/B CH**

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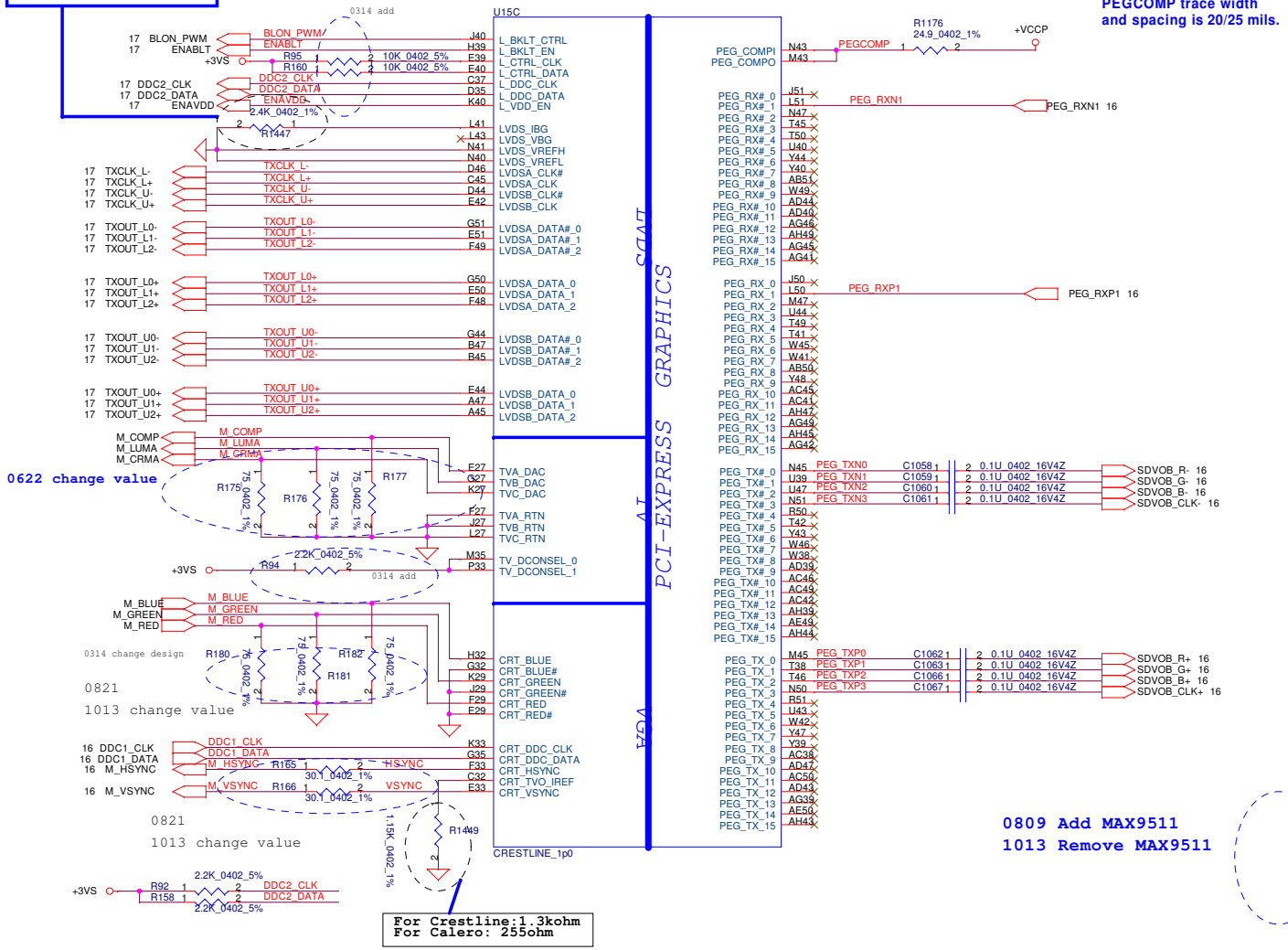
For Crestline:2.4kohm
For Calero: 1.5Kohm



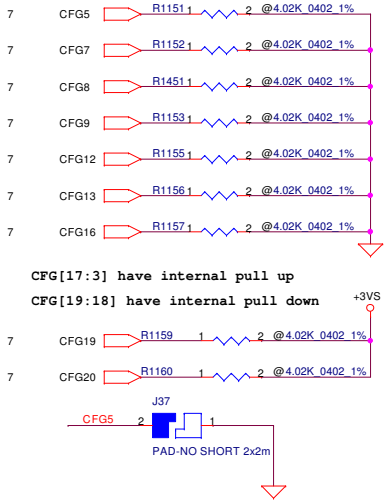
For Crestline:1.3kohm
For Calero: 255ohm

PEGCOMP trace width and spacing is 20/25 mils.

0809 Add MAX9511
1013 Remove MAX9511

Strap Pin Table

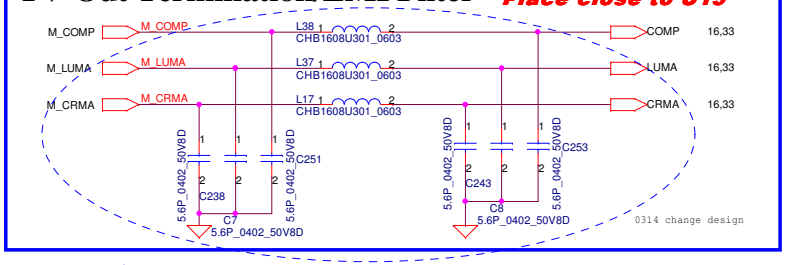
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

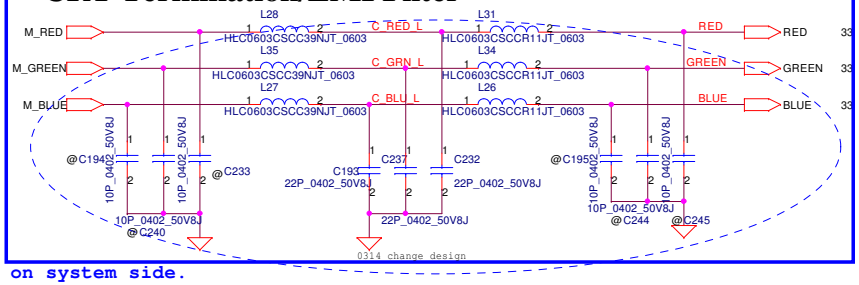
TV-Out Termination/EMI Filter

Place close to U15



CRT Termination/EMI Filter

Place Closed to U15



Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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Title: CRESTLINE((3/6)-VGA/LVDS/TV

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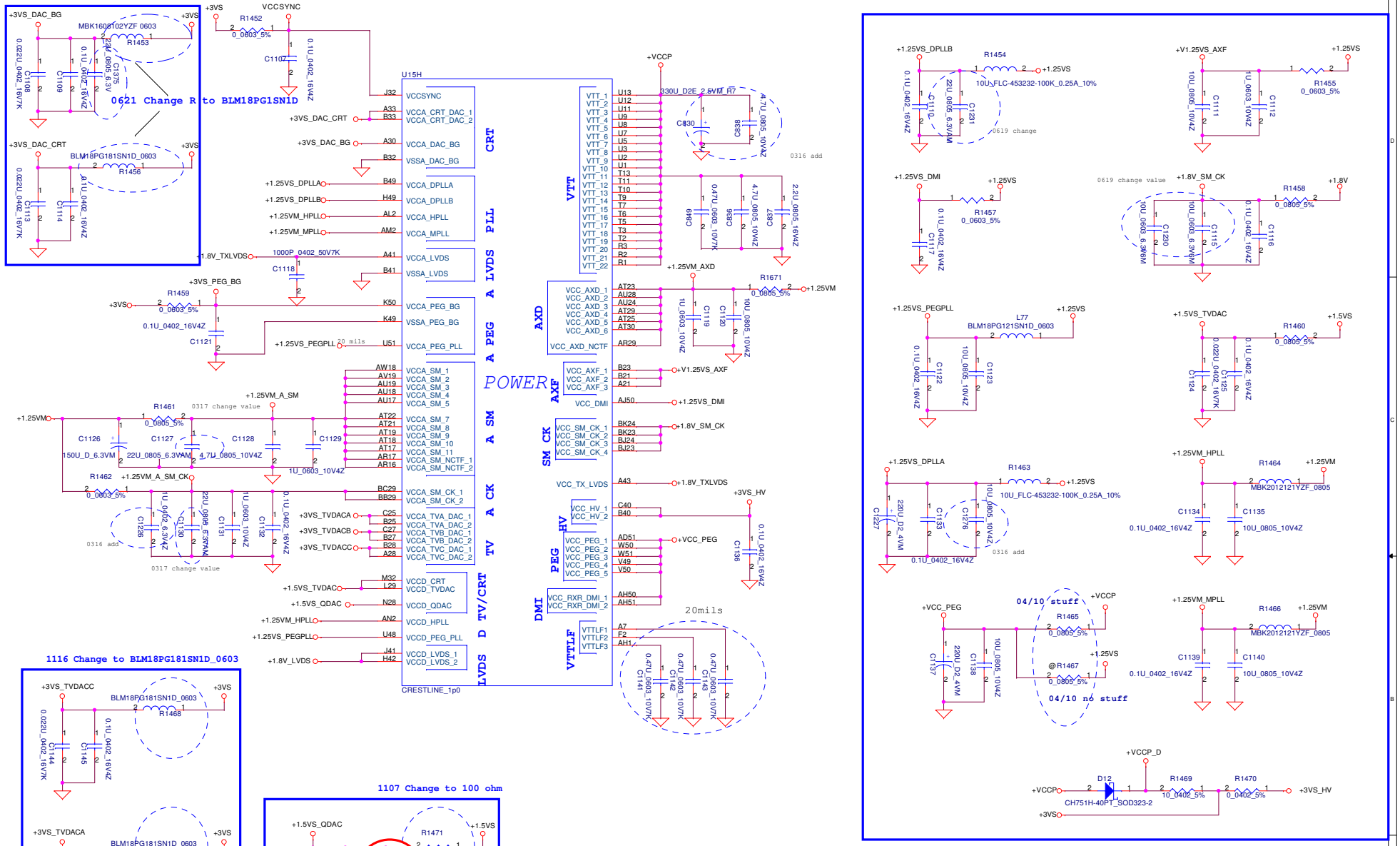

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Title: CRESTLINE(4/6)-PWR

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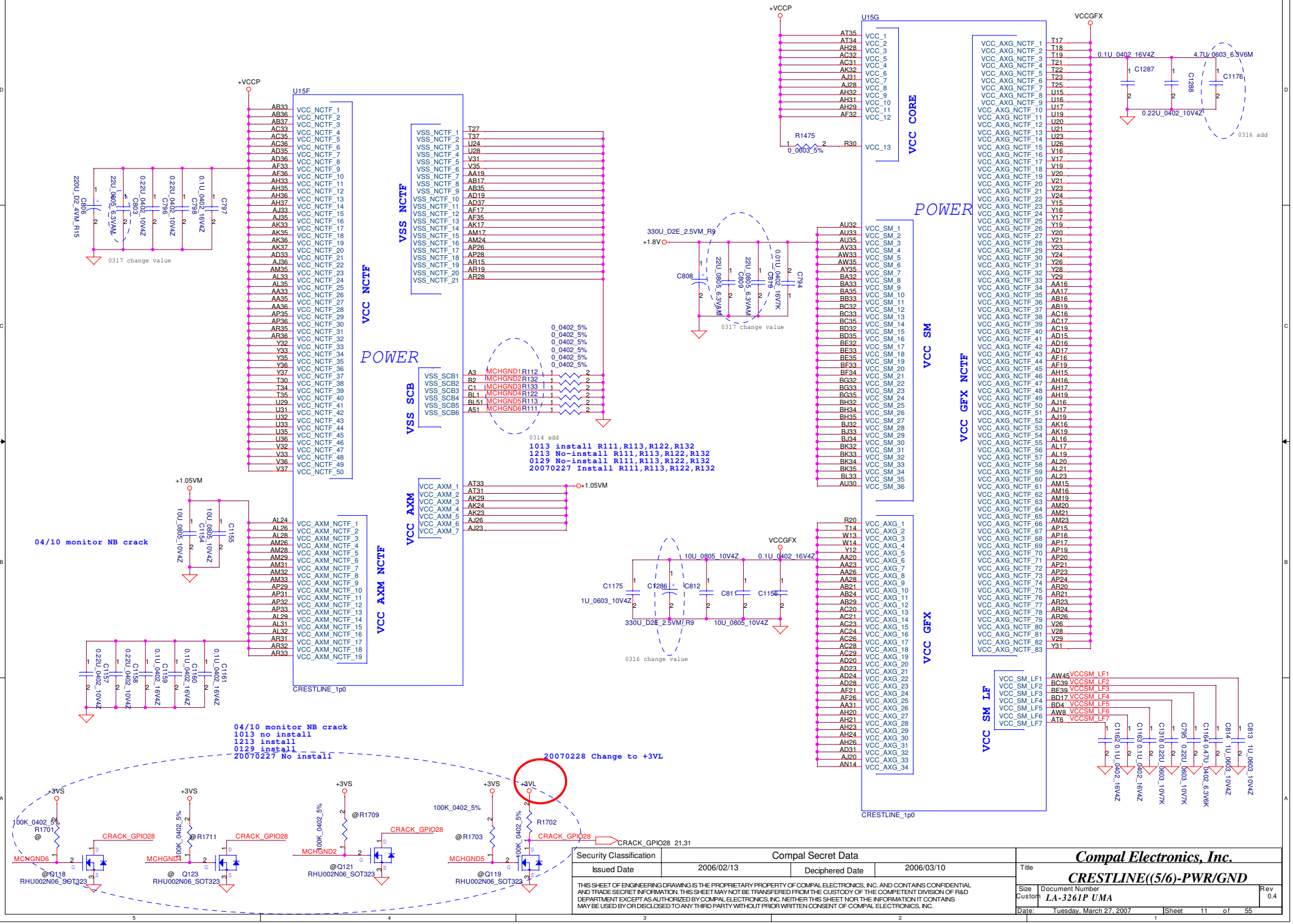

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Title: CRESTLINE((5/6)-PWR/GND

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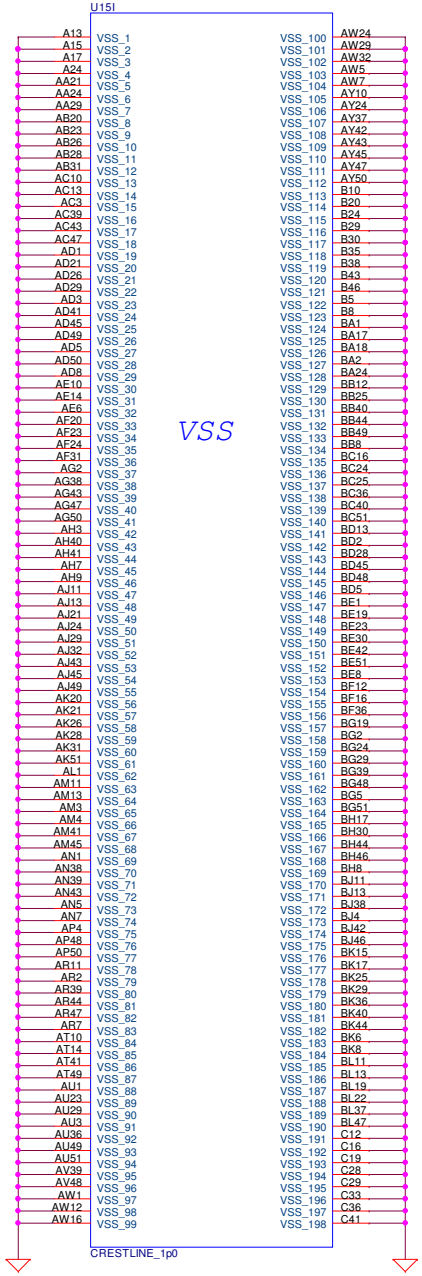

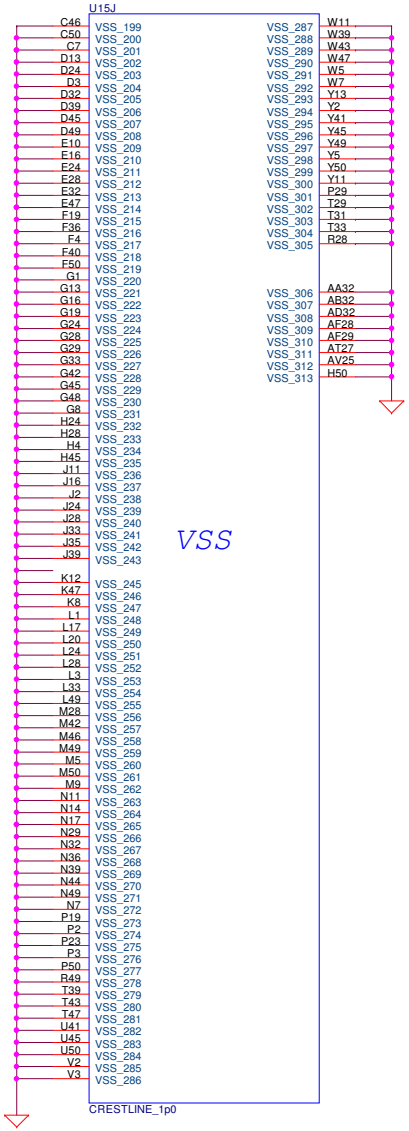

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Title: **CRESTLINE((6/6)-PWR/GND**

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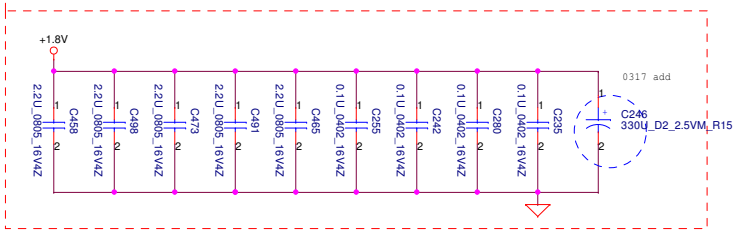
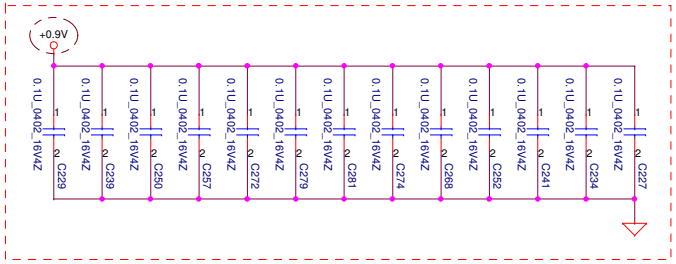
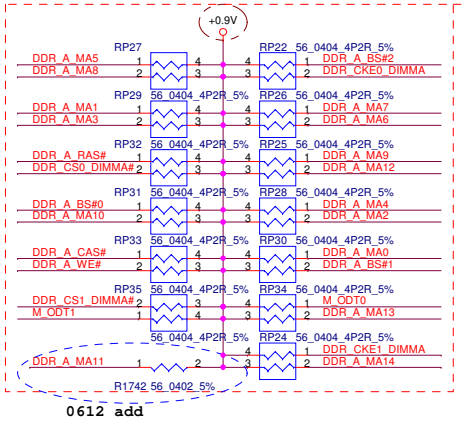
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
7,8 DDR_A_MA[0..14]

Layout Note:
Place near JP34

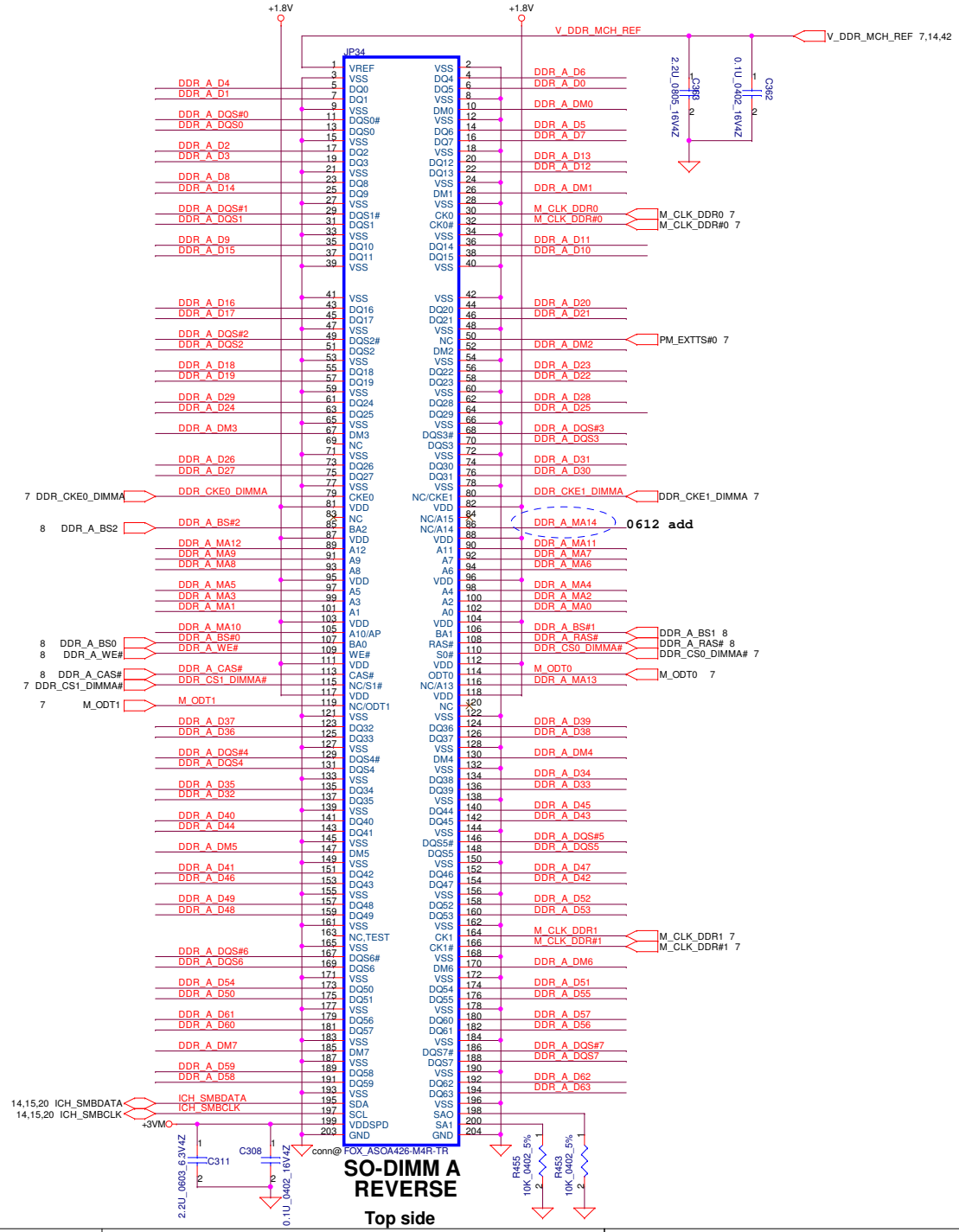


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

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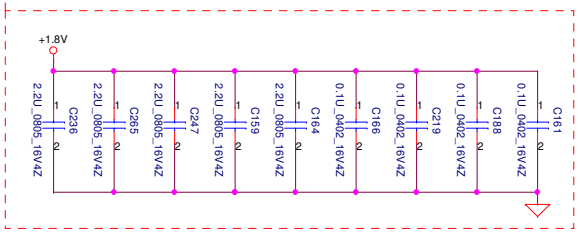
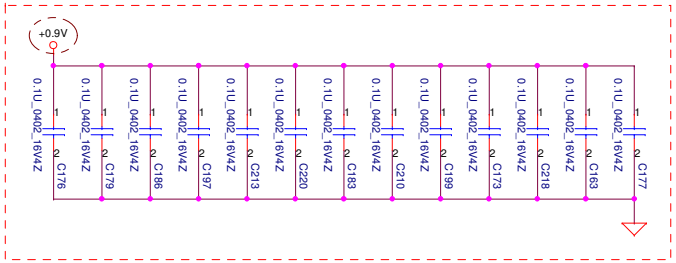
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
7,8 DDR_B_MA[0..14]

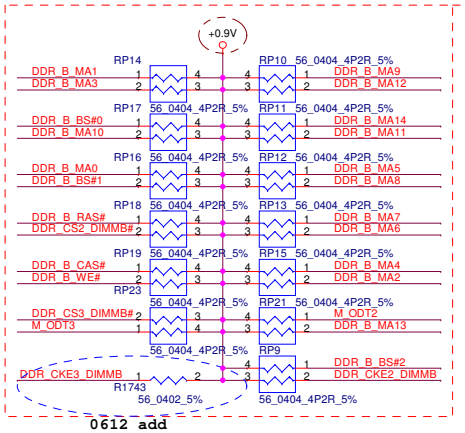
Layout Note:
Place near JP10



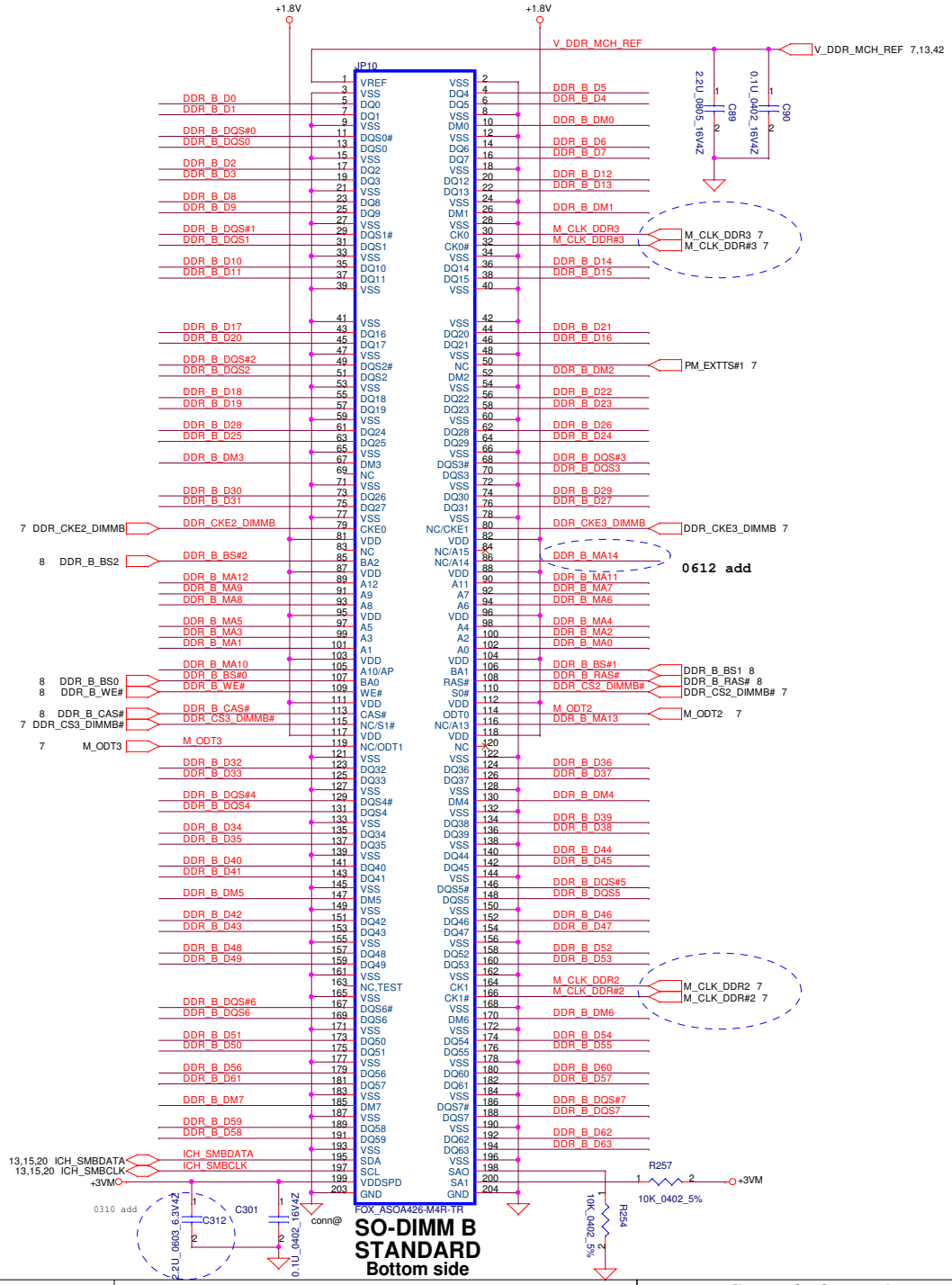
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"



0612 add



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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

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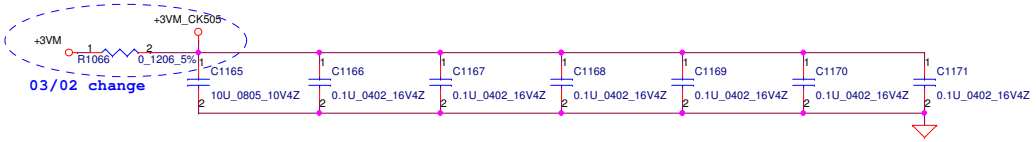
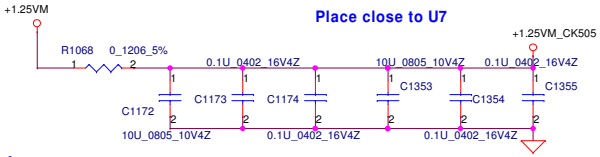
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107 R1135 R1083
*(Default)	No Stuff	R1074 R1086 R1098 R1113 R1128 R1139
667MHz	Stuff	R1086 R1139 R1135 R1074 R1139 R1135
	No Stuff	R1083 R1107 R1128 R1113 R1098
800MHz	Stuff	R1135 R1139
	No Stuff	R1083 R1086 R1098 R1128 R1074 R1107 R1113

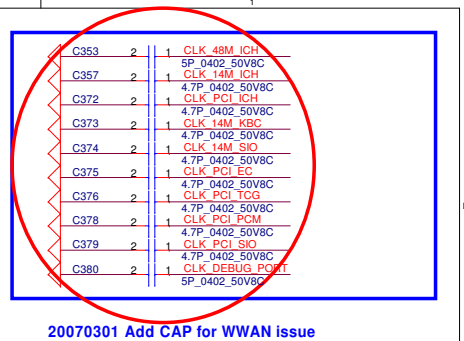


03/02 change

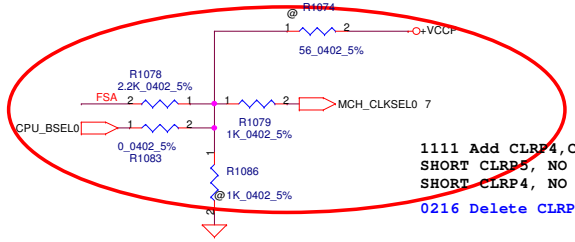


Place close to U7

03/02 change

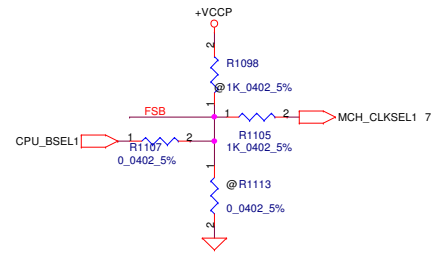


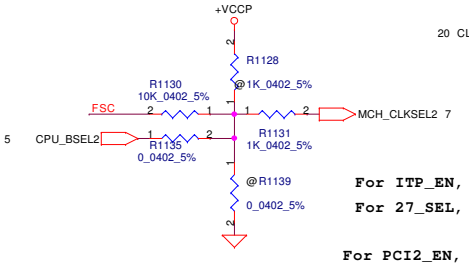
20070301 Add CAP for WWAN issue

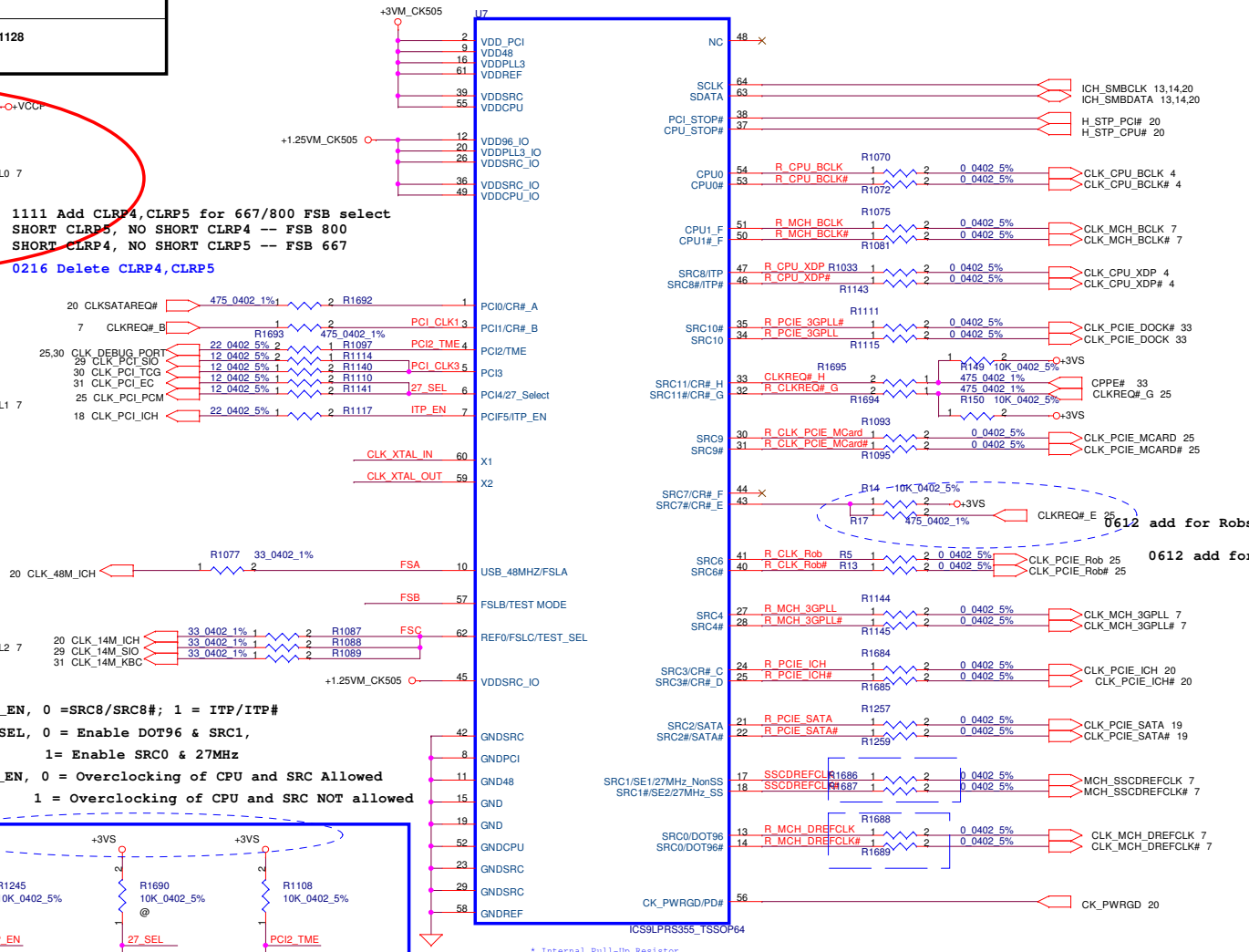


1111 Add CLRP4,CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- FSB 800
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

0216 Delete CLRP4,CLRP5





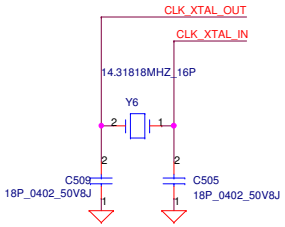


0612 add for Robson

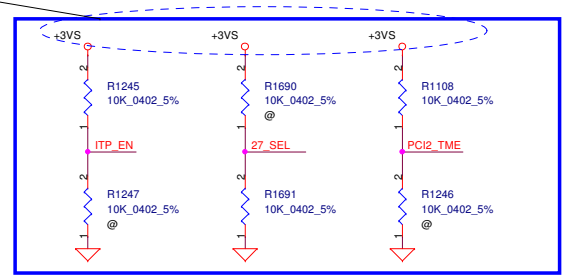
0612 add for Robson

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

0529 change power plane



Routing the trace at least 10mil



* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

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Compal Electronics, Inc.

Title: Clock generator

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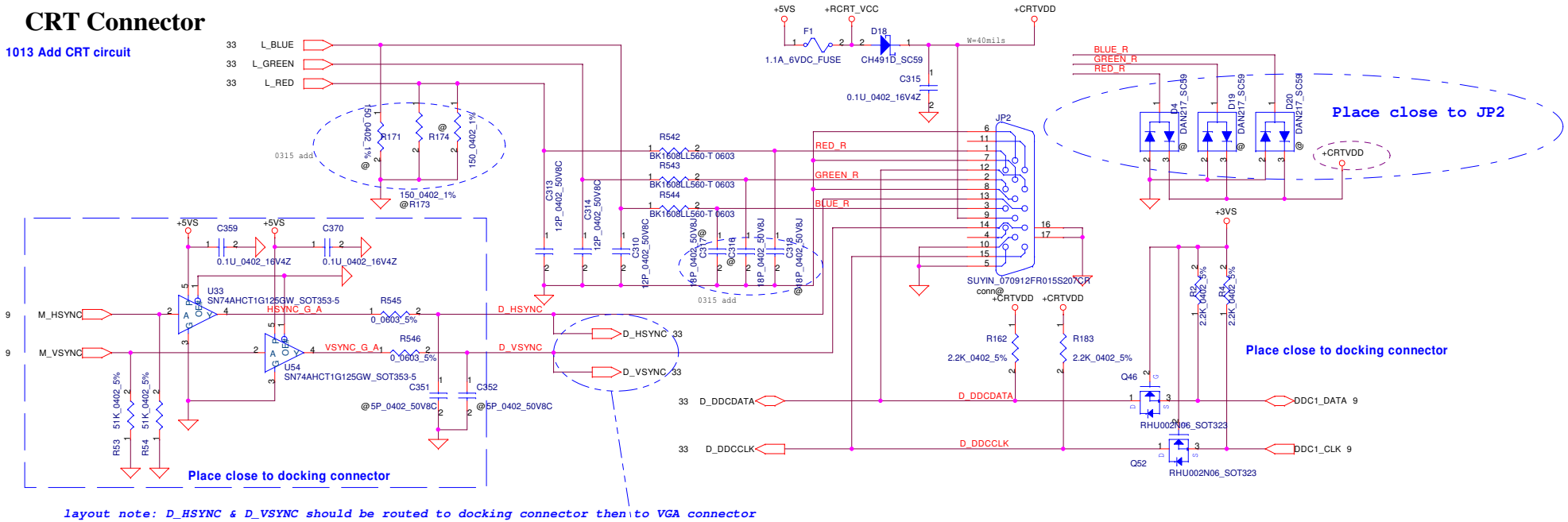
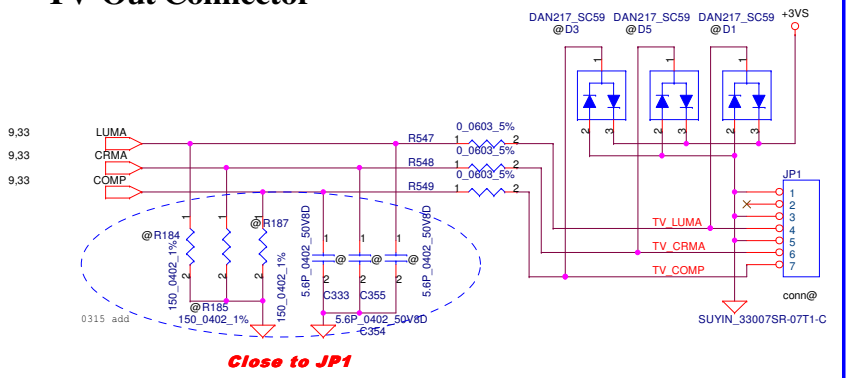
CRT Connector

1013 Add CRT circuit



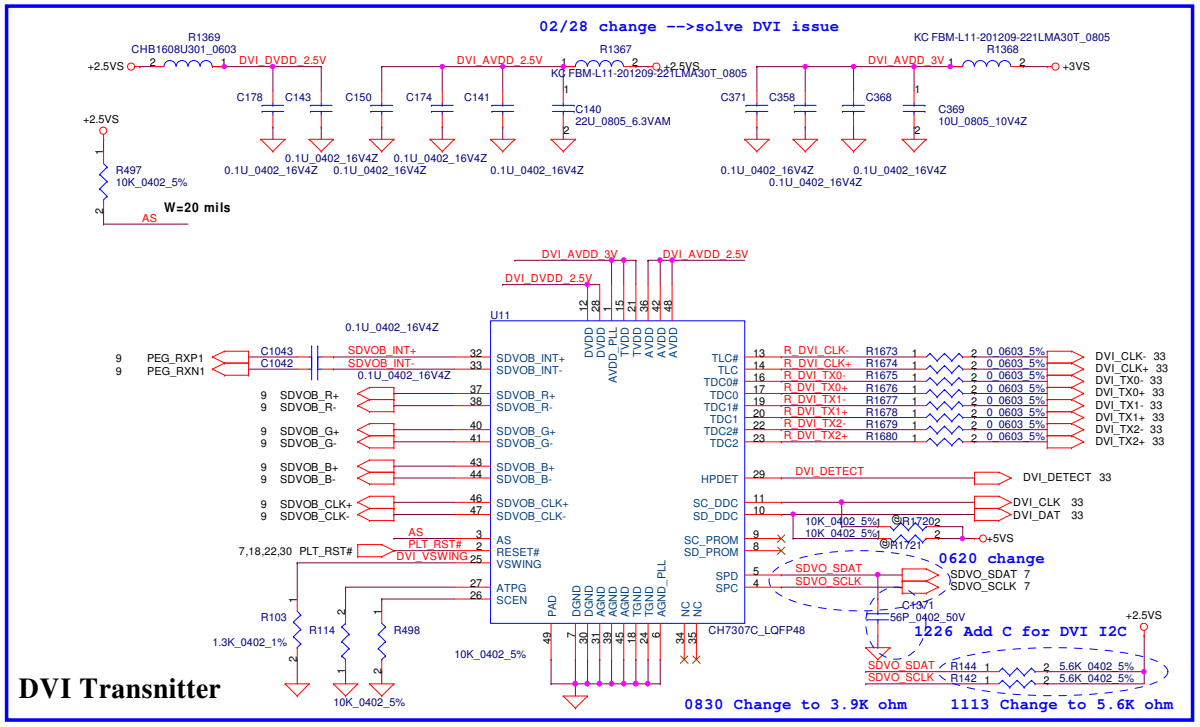
layout note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector

TV-Out Connector



layout note: TV-out signals should be routed to JP30 then to JP1

DVI Transnitter



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Compal Electronics, Inc.

Title: CRT & TVout Connector

Size: Document Number: LA-3261P UMA | Rev 0.4

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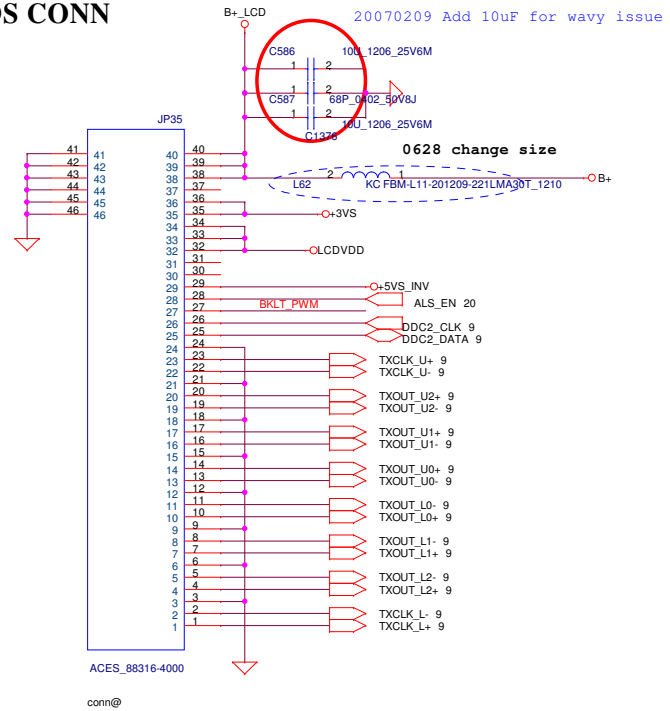
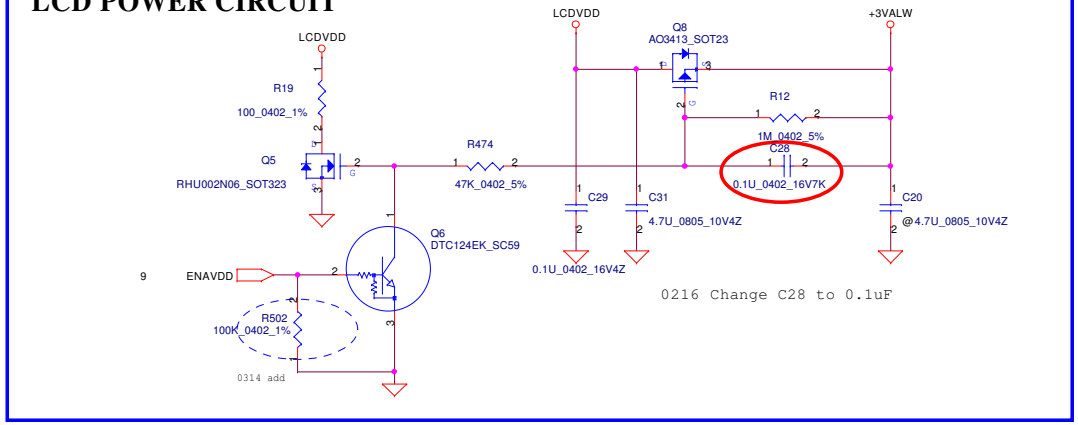
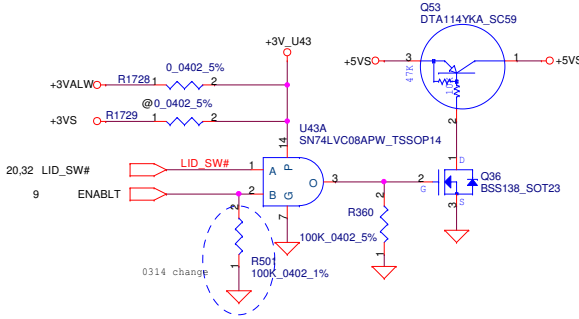
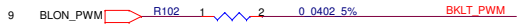
LVDS CONN



LCD POWER CIRCUIT







Support 3V inverter

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Compal Electronics, Inc.

Title: **LCD CONN.**

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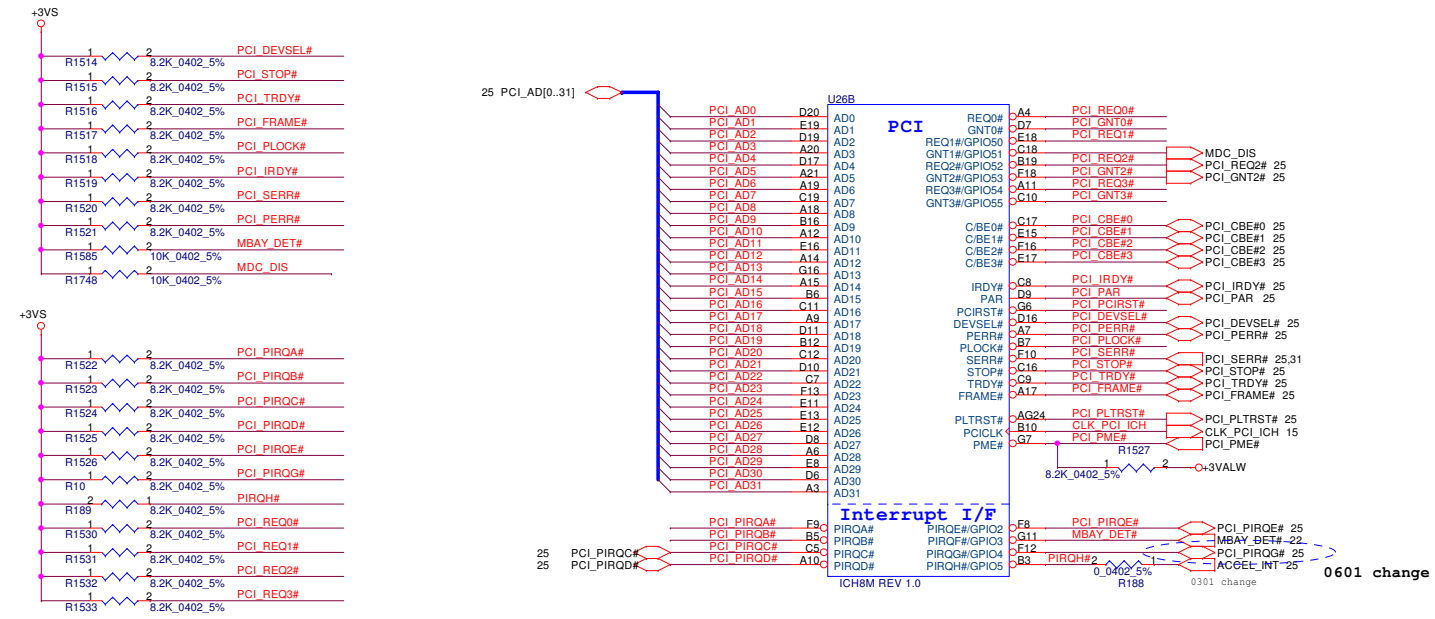
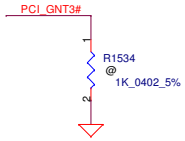
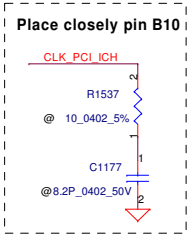
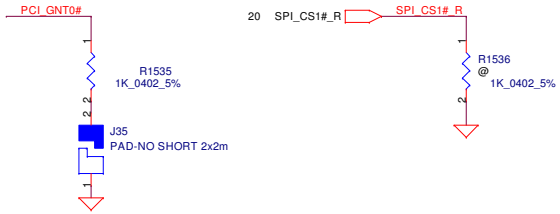


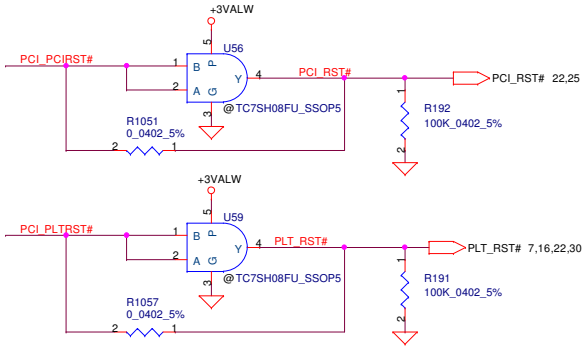


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC







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Compal Electronics, Inc.

Title: **ICH8(1/4)-PCI/INT**

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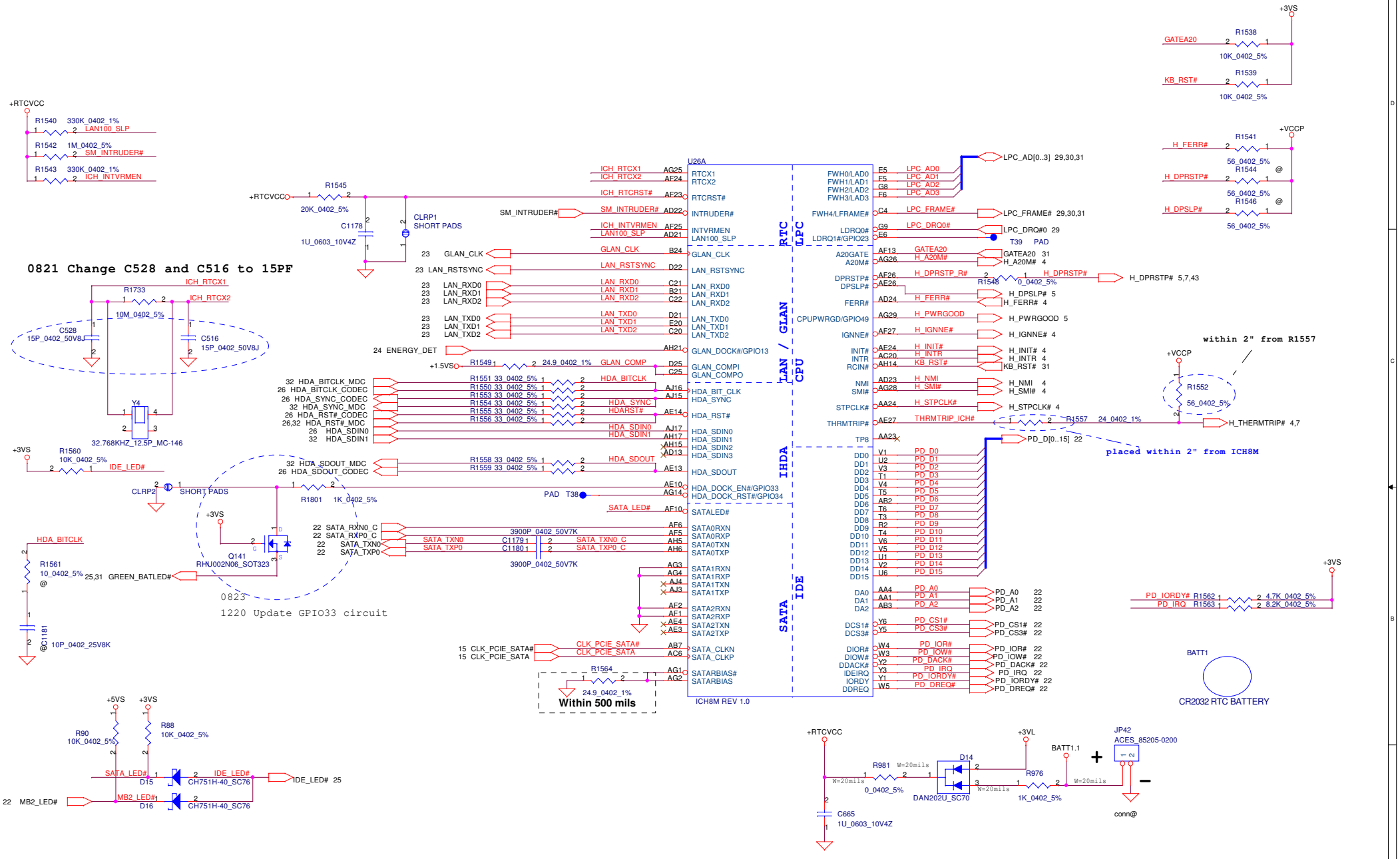

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Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-3261P UMA | Rev: 0.4

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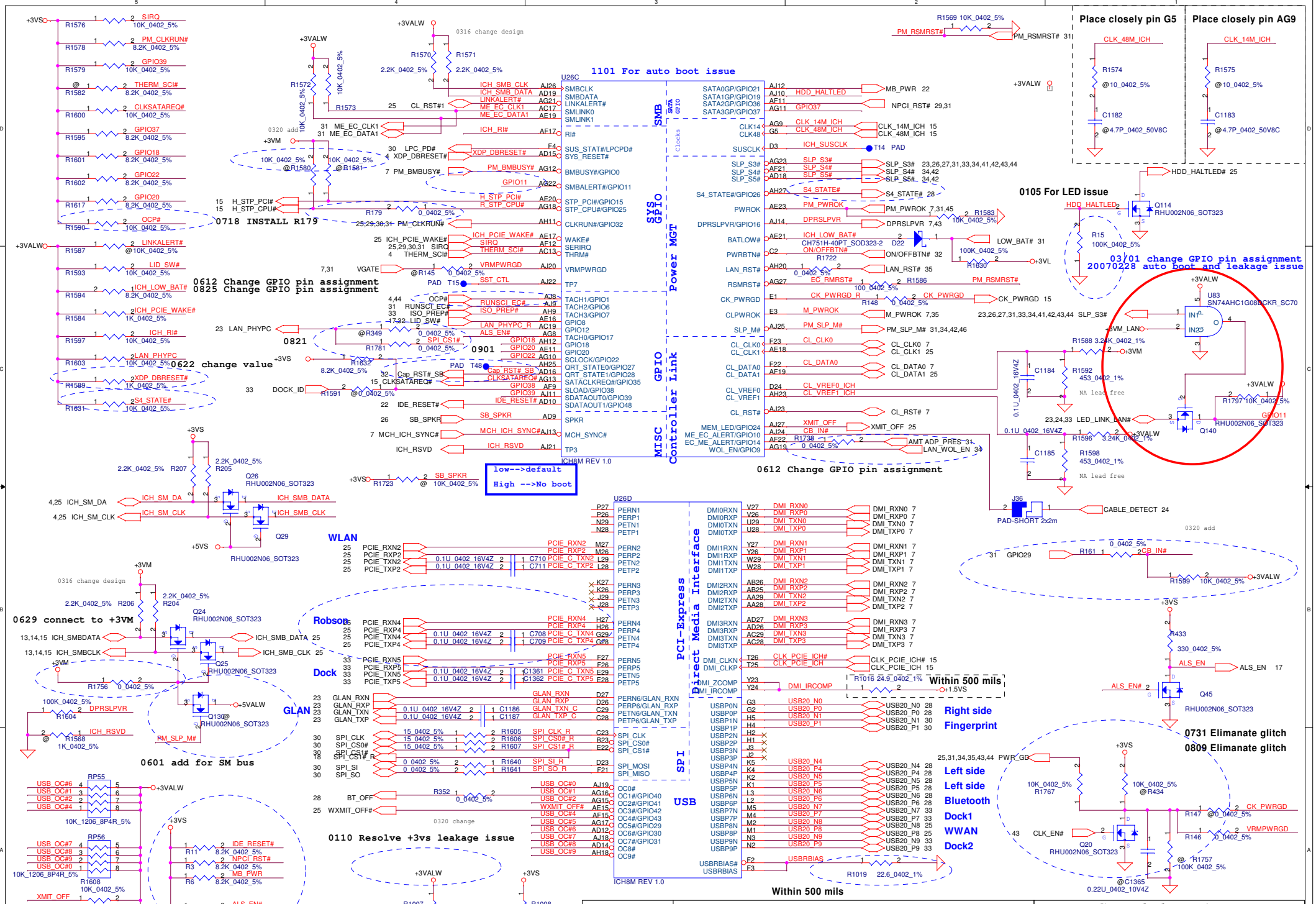

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Compal Electronics, Inc.

Title: ICH8(3/4)_PM,USB,GPIO

Size: Custom | Document Number: LA-3261P UMA | Rev: 0.4

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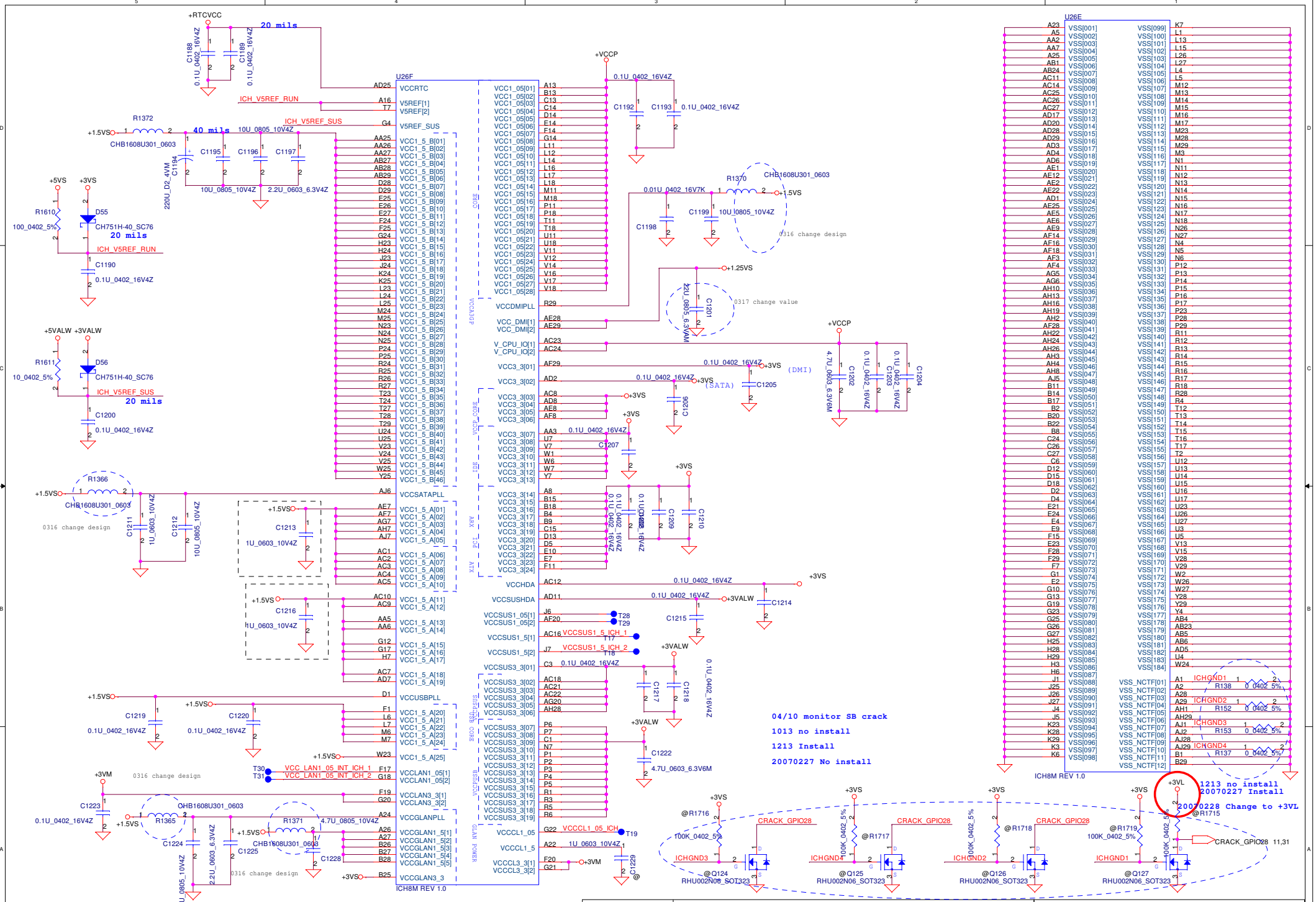

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Compal Electronics, Inc.

Title: **ICH8(4/4)_POWER&GND**

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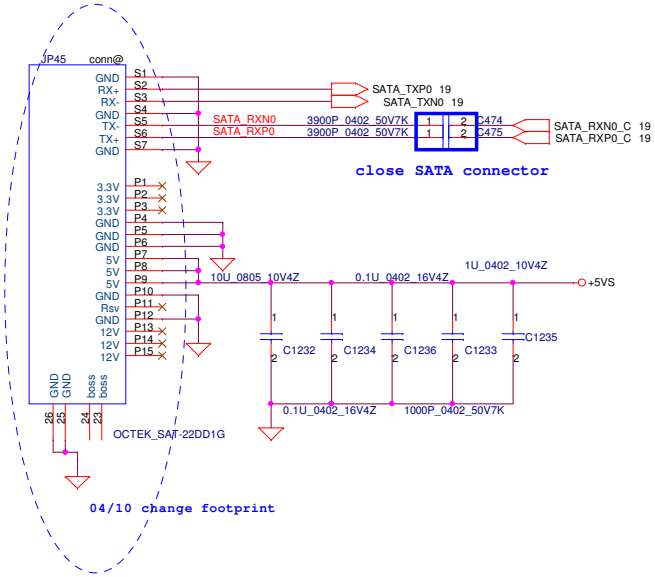
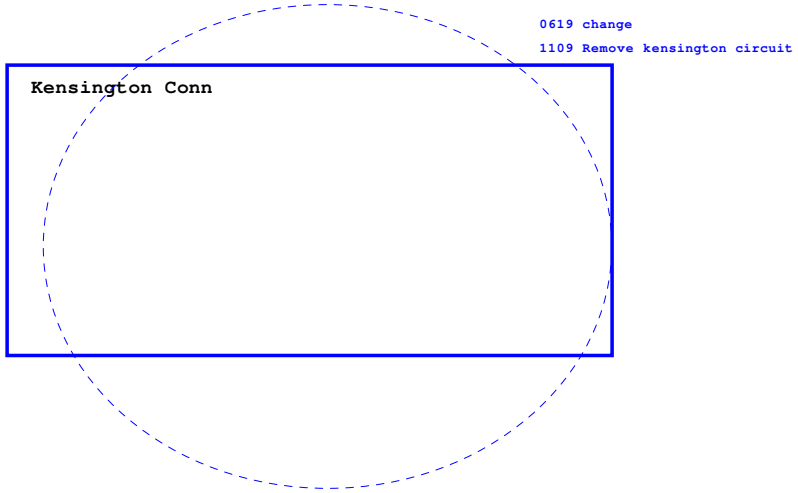
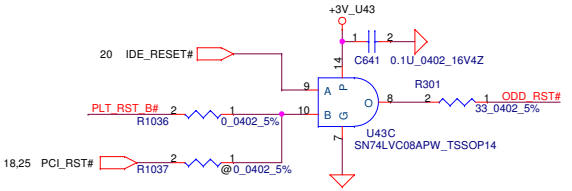
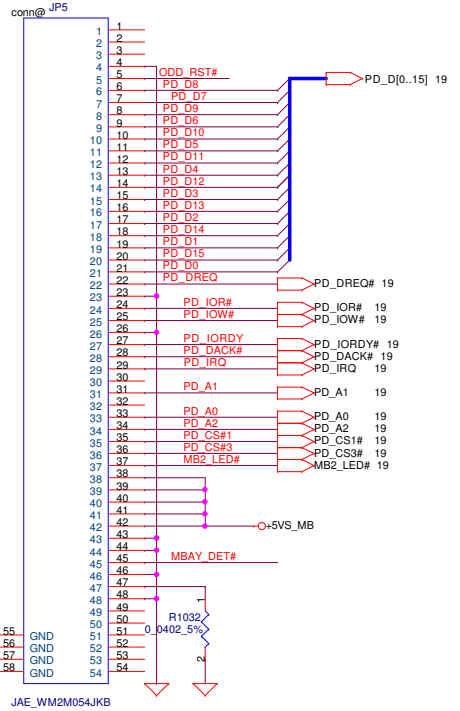
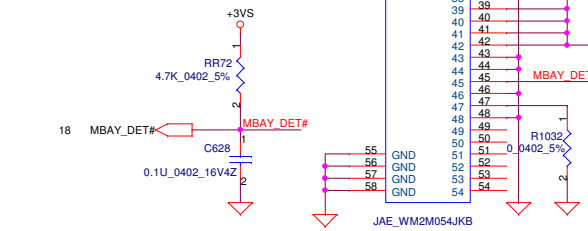
Multi Bay II connector

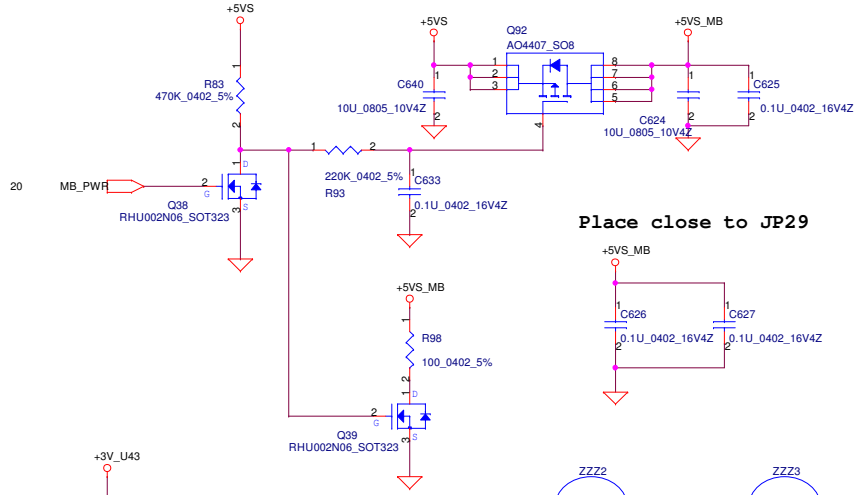


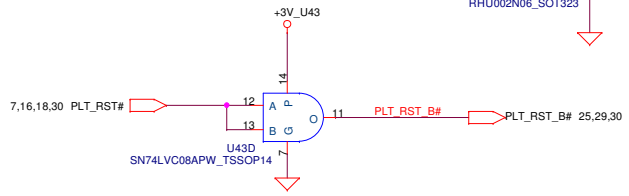












ZZZ2
Audio-wire

ZZZ3
PCB-MB

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Compal Electronics, Inc.

Title: **HDD & CDROM**

Size: Custom | Document Number: LA-3261P UMA | Rev: 0.4

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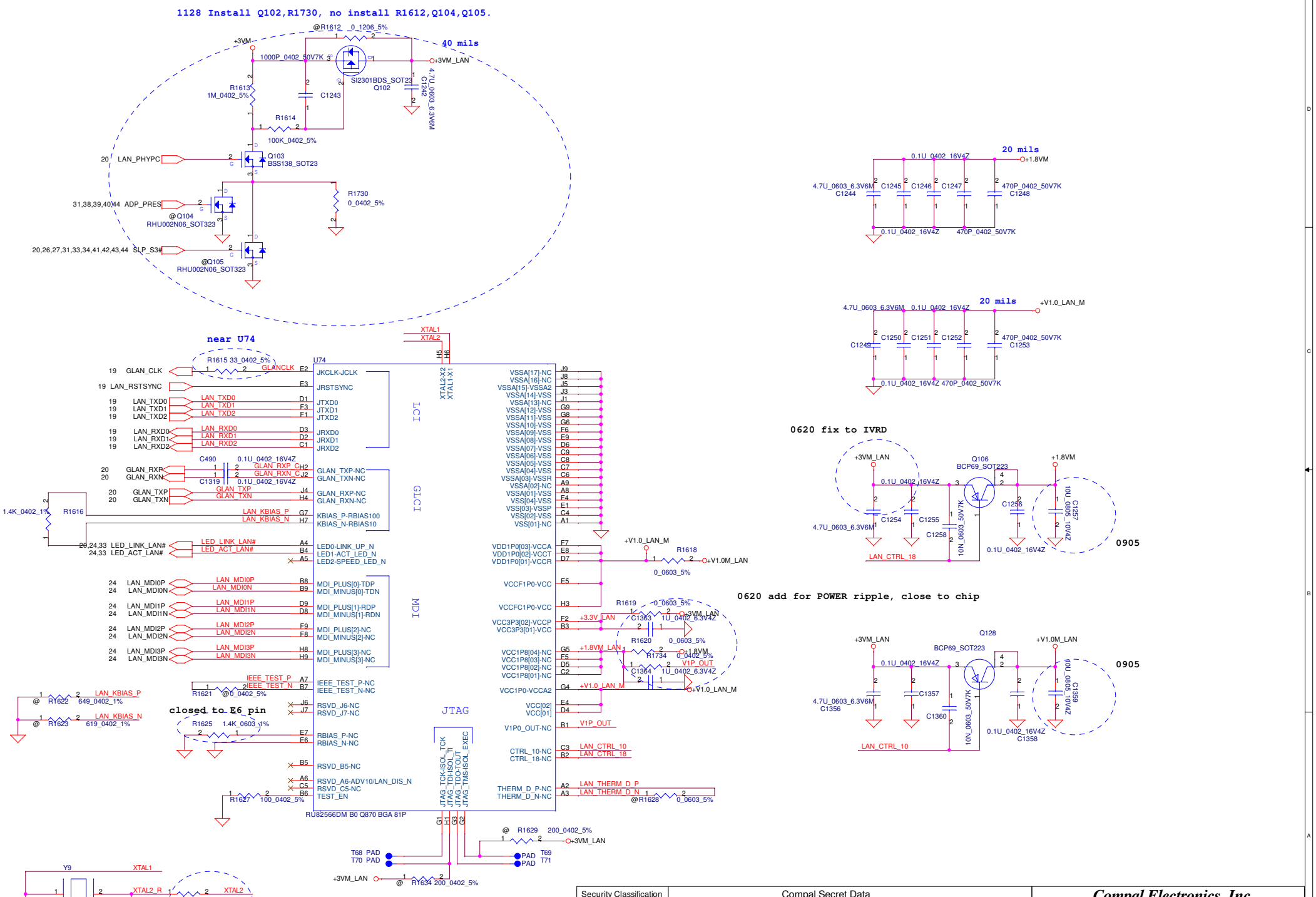

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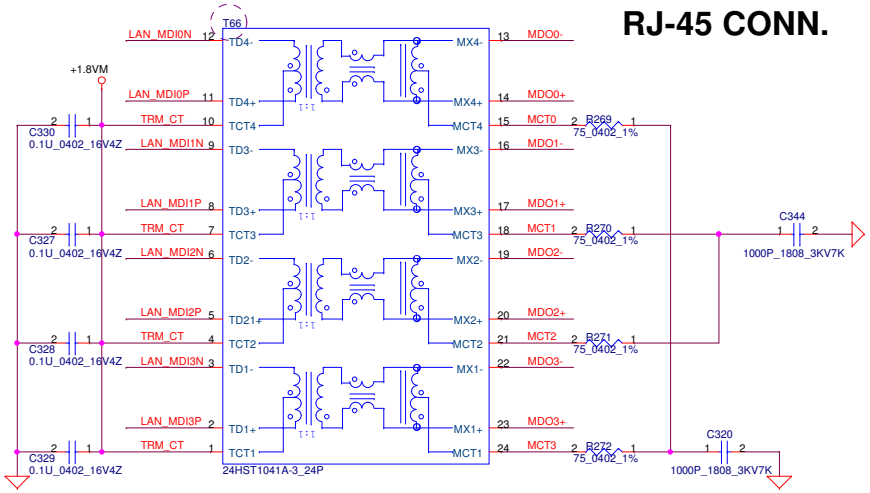
Compal Electronics, Inc.

Title: **Intel 82566 Nineveh**

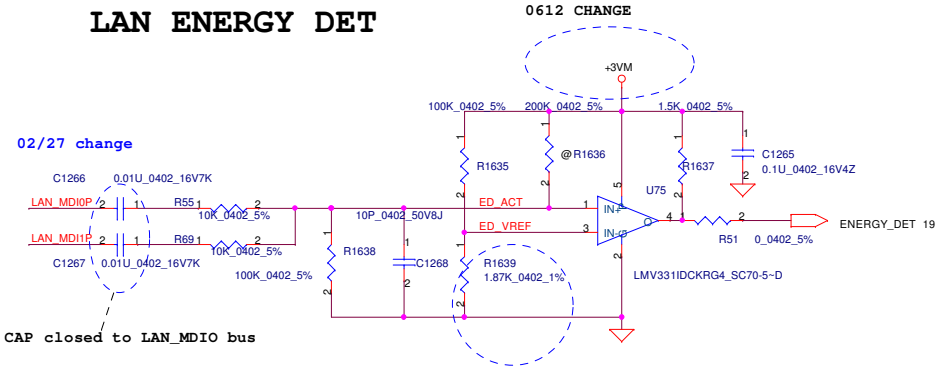
Size | Document Number: *LA-3261P UMA* | Rev 0.4

Date: Tuesday, March 27, 2007 | Sheet 23 of 55

RJ-45 CONN.

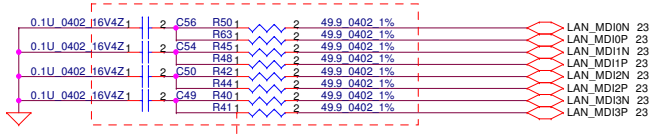


LAN ENERGY DET



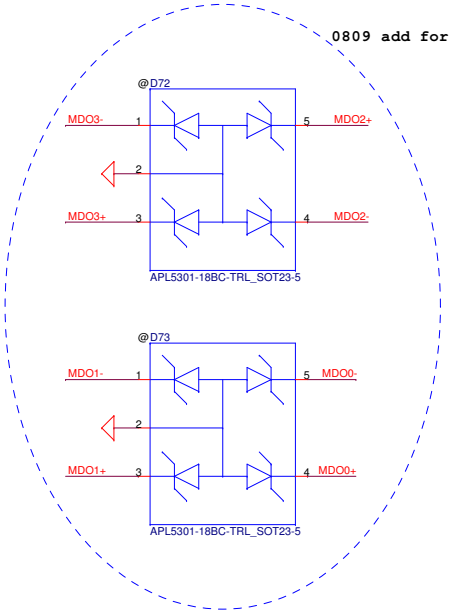
1113 Change R1639 to 1.4K based on Intel WW44

1116 Intel recommend

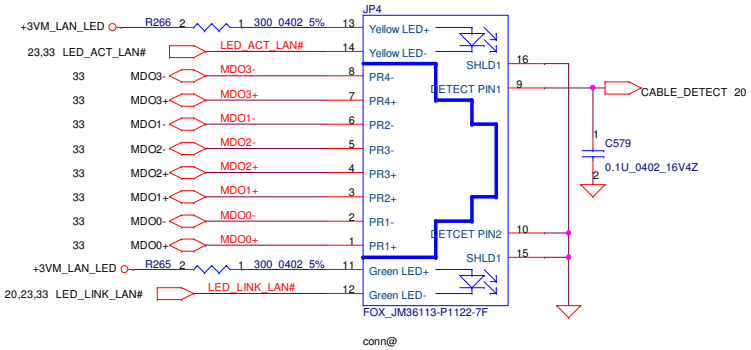


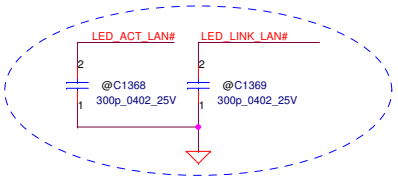
Layout Notice : Place termination as close as Intel 82566 as possible

0809 add for EMI request

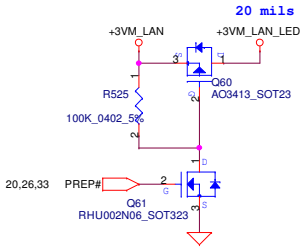


Note: MDO[3..0]+/- signals should route to JP4 first then to JP30.





1115 EMI REQUEST



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Issued Date	2006/02/13	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: **Magnetic & RJ45/RJ11**

Size | Document Number: *LA-3261P UMA* | Rev 0.4

Date: Tuesday, March 27, 2007 | Sheet 24 of 55

B/B connector with PCI / LED / FIR / SC interface

0620 Update ROBSON SCHEMATIC
0824 add 1394 signals
0830 Change 1394 signals

JP13 — ACES_88394-1A71

Pin	Signal	Pin	Signal
28 XTPA0-	XTPA0-	2	XTPB0- 28
28 XTPA0+	XTPA0+	4	XTPB0+ 28
15 CLK_PCIE_Rob#	CLK_PCIE_Rob#	6	PCI_PIRQG#
15 CLK_PCIE_Rob	CLK_PCIE_Rob	8	PCI_PIRQD# 18
20 PCIE_RXN4	PCIE_RXN4 (R37 0_0402_5%)	10	PCI_REQ2# 18
20 PCIE_RXP4	PCIE_RXP4 (R36 0_0402_5%)	12	PCI_PLTRST# 18
20 PCIE_TXN4	PCIE_TXN4	14	CLKREQ#_E 15
20 PCIE_TXP4	PCIE_TXP4	16	PCI_PIRQE# 18
15 CLK_PCI_PCM	CLK_PCI_PCM	18	PCI_PIRQC# 18
	PCI_AD31	20	PCI_RST# 18,22
	PCI_AD29	22	PCI_GNT2# 18
	PCI_AD27	24	SIRQ 20,29,30,31
	PCI_AD25	26	PWR_GD 20,31,34,35,43,44
18 PCI_CBE#3	PCI_CBE#3	28	PCI_AD30
	PCI_AD23	30	PCI_AD28
	PCI_AD21	32	PCI_AD26
	PCI_AD19	34	PCI_AD24
	PCI_AD17	36	PCM_SPK
18 PCI_CBE#2	PCI_CBE#2	38	PCI_AD22 PCM_SPK 26
18 PCI_IRDY#	PCI_IRDY#	40	PCI_AD20
20,29,30,31 PM_CLKRUN#	PM_CLKRUN#	42	PCI_PAR
18,31 PCI_SERR#	PCI_SERR#	44	PCI_AD18 PCI_PAR 18
18 PCI_PERR#	PCI_PERR#	46	PCI_AD16
18 PCI_CBE#1	PCI_CBE#1	48	PCI_FRAME#
	PCI_AD14	50	PCI_TRDY# PCI_FRAME# 18
	PCI_AD12	52	PCI_STOP# PCI_TRDY# 18
	PCI_AD10	54	PCI_DEVSEL# PCI_STOP# 18
	PCI_AD8	56	PCI_AD15 PCI_DEVSEL# 18
	PCI_AD7	58	
	PCI_AD5	60	PCI_AD13
	PCI_AD3	62	PCI_AD11
	PCI_AD1	64	PCI_AD9
		66	PCI_CBE#0 PCI_CBE#0 18
		68	PCI_AD6
		70	PCI_AD4
		72	PCI_AD2
		74	PCI_AD0
20 HDD_HALTLED#	HDD_HALTLED#	76	
+3VL		78	
30,32 WL_BLUE_LED#	WL_BLUE_LED#	80	IRRX
19,31 GREEN_BATLED#	GREEN_BATLED#	82	IRTXOUT
31 AMBER_BATLED#	AMBER_BATLED#	84	IRMODE
31,32,33 LED_STB#	LED_STB#	86	
19 IDE_LED#	IDE_LED#	88	SC_CD#
		90	
+1.5VS		92	SC_CLK
+3VS		94	SC_RST
		96	
+5VS		98	SC_DATA
		100	
		101 GND	GND 102

IRRX 29; IRTXOUT 29; IRMODE 29; SC_CLK 28; SC_RST 28; SC_DATA 28; +3VS; +SC_PWR

PCI_AD[0..31] — PCI_AD[0..31] 18

0622 change to support AMT

0731 Install R1383 and no install R1382, do not support wake on WWAN card

Mini-Express Card---WLAN

0824 Add +1.5VS_WLAN
0811 Isolate SLOT power from SYSTEM power.

0.1U_0402_16V4Z C538; C542 4.7U_0805_10V4Z; +3VS_WLAN
0.01U_0402_16V7K C293; C294; C533 4.7U_0805_10V4Z; +1.5VS_WLAN; 0.1U_0402_16V4Z
C954 0.1U_0402_16V4Z; +3VALW; +3VS; R1778 0_1206_5%; +3VS_WLAN
+1.5VS; R1785 0_1206_5%; +1.5VS_WLAN

0821 Install R1364

JP44 conn@ — MOLEX 67910-0002 52P

Pin	Signal	Pin	Signal
20 ICH_PCIE_WAKE#	ICH_PCIE_WAKE#	1	+3VS_WLAN
28 CH_DATA	CH_DATA	3	+1.5VS_WLAN
28 CH_CLK	CH_CLK	5	
15 CLKREQ#_G	CLKREQD#_MC (R1336 0_0402_5%)	7	
15 CLK_PCIE_MCARD#	CLK_PCIE_MCARD#	9	
15 CLK_PCIE_MCARD	CLK_PCIE_MCARD	11	
		13	
15,30 CLK_DEBUG_PORT		15	
20 PCIE_RXN2	PCIE_RXN2 (R1348 0_0402_5%)	17	
20 PCIE_RXP2	PCIE_RXP2 (R1349 0_0402_5%)	19	
20 PCIE_TXN2	PCIE_TXN2	21	
20 PCIE_TXP2	PCIE_TXP2	23	
20 CL_CLK1	R197 0_0402_5%	25	
20 CL_DATA1	R195 0_0402_5%	27	
20 CL_RST#1	R194 0_0402_5%	29	
		31	
		33	
		35	
		37	
		39	WW_LED#1R; WL_LED#; WP_LED#1R
		41	
		43	
		45	
		47	
		49	
		51	
		53 GND1	GND2 54

2 PCIE_C_RXN2; 2 PCIE_C_RXP2; 2 WW_LED#; 2 WP_LED#

2 XMIT_OFF#; 1 PLT_RST_B# 22,29,30; R1363 0_0402_5% +3VALW; R1364 0_0402_5% +3VM; ICH_SMB_CLK 20; ICH_SMB_DATA 20; WW_LED# 30; WL_LED# 30; WP_LED# 30

0906 Remove debug resistors
0906 Remove debug resistors
0906 Remove debug resistors
0821 Change +3VS to +3VS_WLAN
0612 change power plane
0627 Add 0 ohm on PIN 42,46
@R1754 0_0402_5%; @R1755 0_0402_5%

0627 PIN37,43 connected to GND
PIN39,41 connected to +3VS

0811 No install R1418,R1358,R1359,R1360

0906 Remove debug resistors

+3VALW; R517 @100K_0402_5%; R516 @10K_0402_5%; XMIT_OFF#
20 XMIT_OFF# — D74 CH751H-40_SC76; Q58 @RHU002N06_SOT323; R1422 0_0402_5%

0811 HP request

Mini-Express Card--WWAN

0811 Isolate SLOT power from SYSTEM power.

+3VALW; C959 0.1U_0402_16V4Z; +3VS; R1779 0_1206_5%; +3VS_WWAN
0.01U_0402_16V7K C295; C540 4.7U_0805_10V4Z; C544 0.1U_0402_16V4Z; +3VS_WWAN

JP46 conn@ — MOLEX 67910-0002 52P

UIM_PWR; UIM_DATA; UIM_CLK; UIM_RST; UIM_VPP; M_WXMIT_OFF#; USB20_N8 20; USB20_P8 20; WW_LED# 30

@R1382 0_0402_5% +3VALW; R1383 0_0402_5% +3VS_WWAN; R1071 20_0603_5%; R1073 0_0603_5%

U72 — S DIO(BR) NUP4301MR6T1 TSOP-6

JP50 — TAITW_PMPAT6-06GLBS7N14N0

@D13 DAN217_SC59; C554 4.7U_0805_10V4Z; C960 0.1U_0402_16V4Z; @R1780 10K_0402_5%

0821 Change +3VS to +3VS_WWAN
0811 Pins 37 and 43 connect to GND and remove +1.5VS

D66 CH751H-40_SC76; 20 WXMIT_OFF#; M_WXMIT_OFF#

0811 Reserve for SIM card does not meet rise time and a pull-up resistor is needed.
0116 Connected R1780.1 to UIM_PWR

0821 Delete SW1,C986,R521,D65,R200

ACCELEROMETER

+3VS; R1355 @0_0805_5%; +3VS_ACL; R1356 0_0603_5%; +3VS_ACL_IO
D64 CH751H-40_SC76

+3VS_ACL; C994; C995; C996 10U_0805_10V4Z; @0.01U_0402_16V7K; 0.1U_0402_16V4Z

0313 change design

U64 — LIS3LV02DL-TR _LGA16

Pin	Signal	Pin	Signal
18 ACCEL_INT	INT/RDY	1	GND 16
	SDD	2	RES 15
4,20 ICH_SM_DA	SDA/SDI/SPC	3	GND 14
+3VS_ACL_IO	VDD_IO	4	VDD 13
4,20 ICH_SM_CLK	SCL/SPC	5	RES 12
+3VS_ACL	CS	6	VDD 11
	NC	7	RES 10
	CK	8	GND 9

R1361 0_0402_5%; R1362 0_0402_5% +3VS_ACL; R1357 0_0402_5% +3VS_ACL_IO; R1359 10K_0402_5%; R1391 0_0402_5%

0619 Follow ST Demo circuit
0619 Follow ST Demo circuit
Must be placed in the center of the system.

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Issued Date	2005/05/26	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: Mini-Card/Mini-PCI/Accelerometer

Size: | Document Number: LA-3261P UMA | Rev: 0.4

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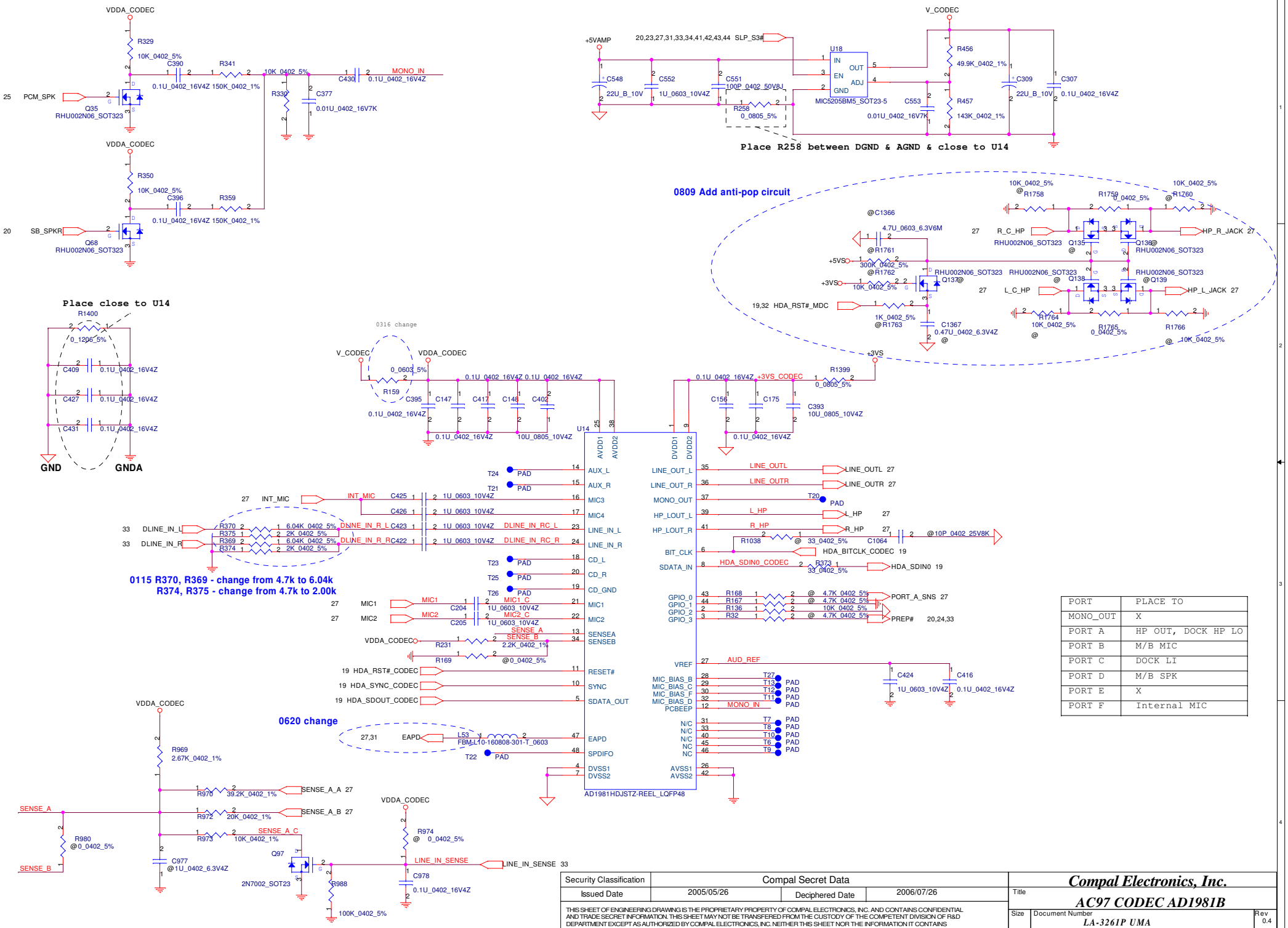

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

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Issued Date	2005/05/26	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: AC97 CODEC AD1981B

Size: Document Number: LA-3261P UMA | Rev: 0.4

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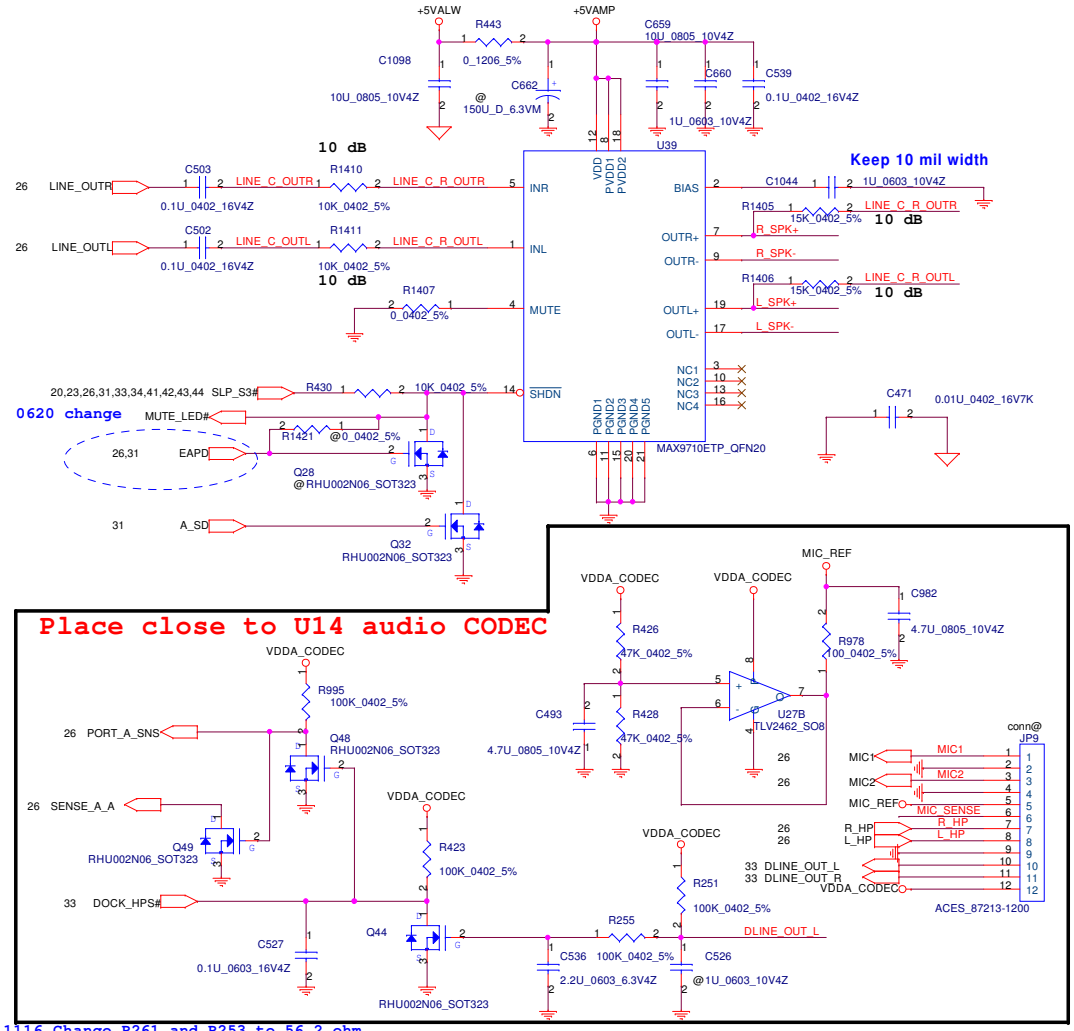
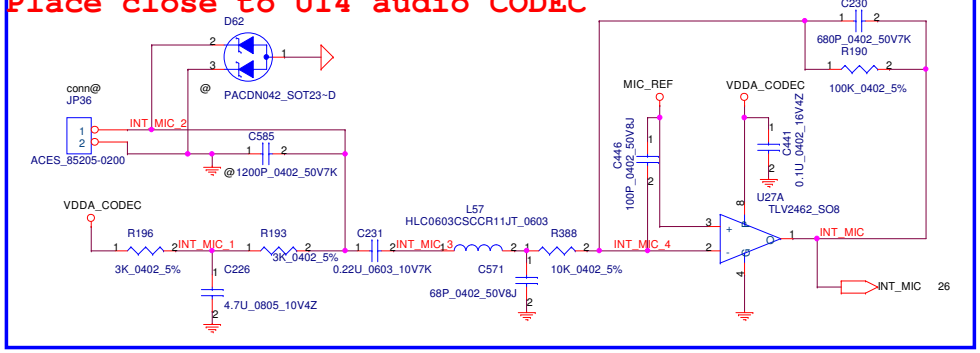
AMP. FOR INTERNAL SPEAKER



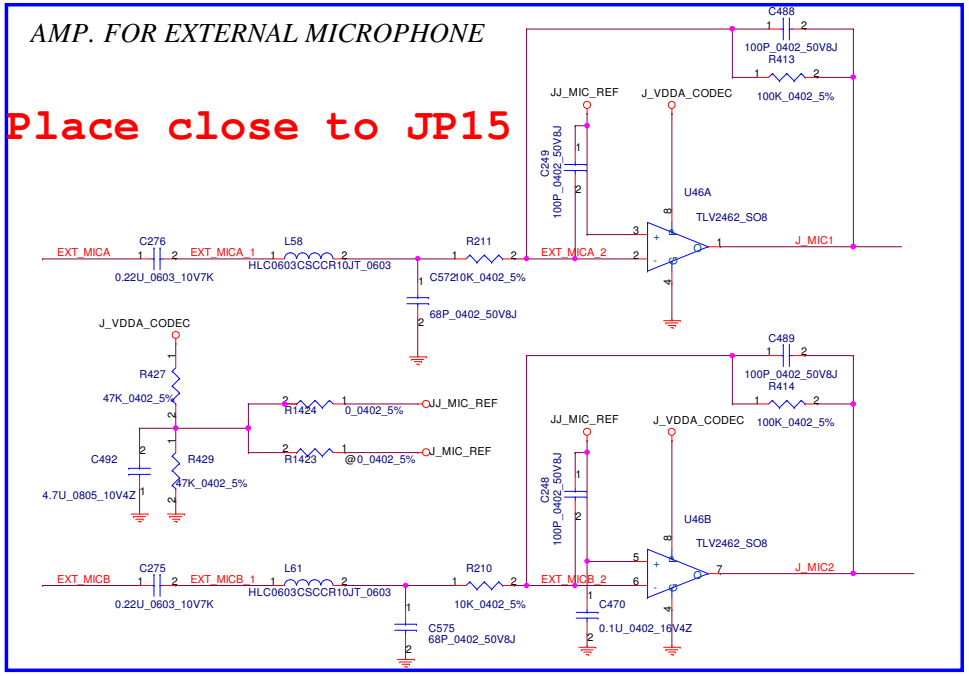
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC



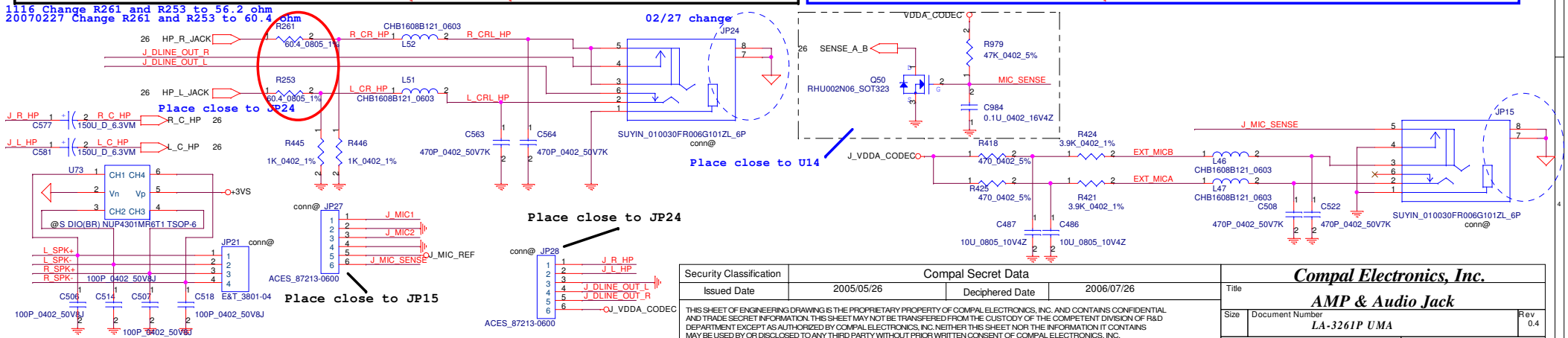
AMP. FOR EXTERNAL MICROPHONE

Place close to JP15



Place close to U14 audio CODEC

1116 Change R261 and R253 to 56.2 ohm
20070227 Change R261 and R253 to 60.4 ohm



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Compal Electronics, Inc.

Title: **AMP & Audio Jack**

Size	Document Number	Rev
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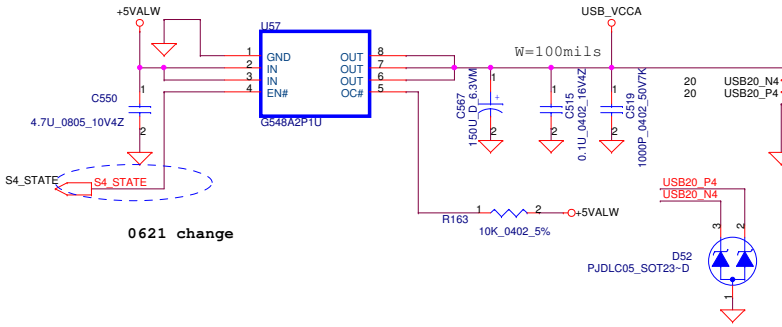
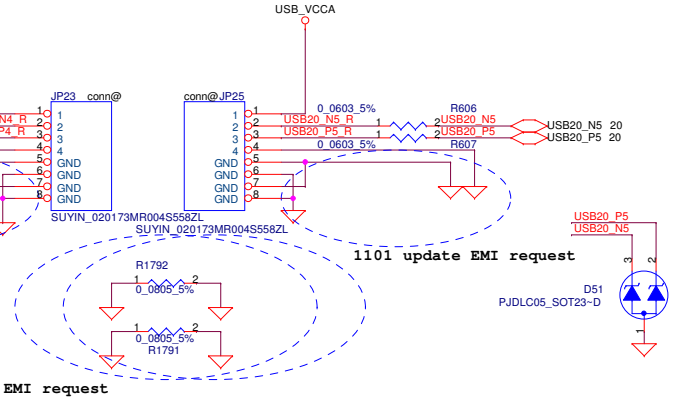
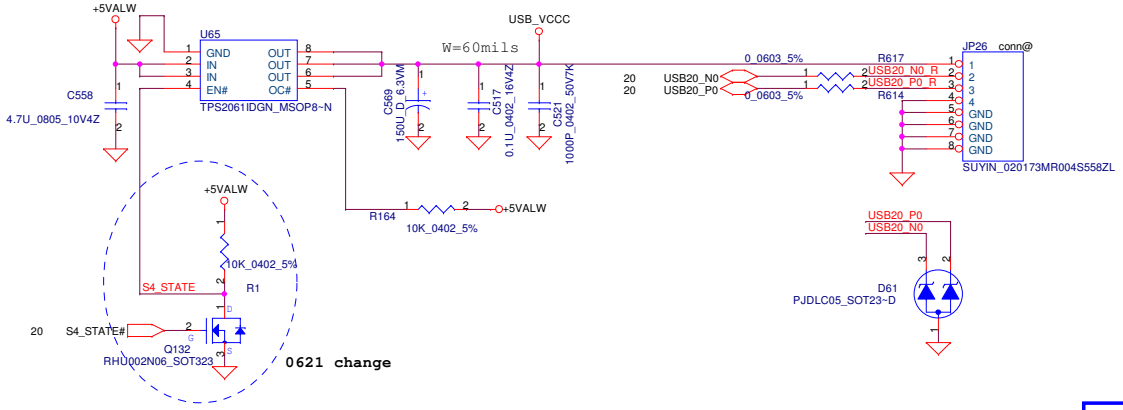
Left side USB CONNECTOR 0



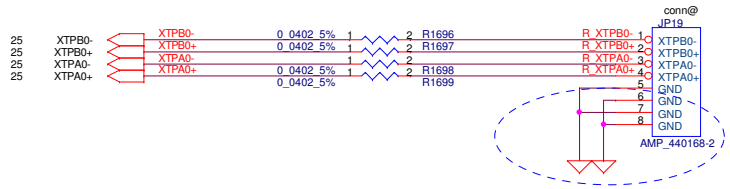
Left side USB CONNECTOR 1



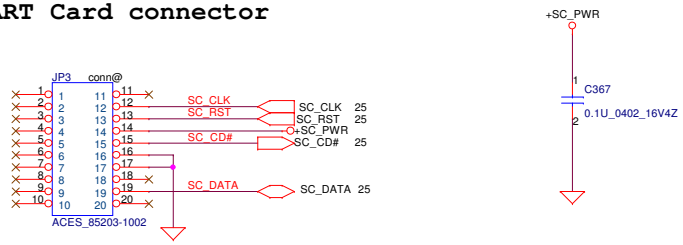
Right side USB CONNECTOR 0



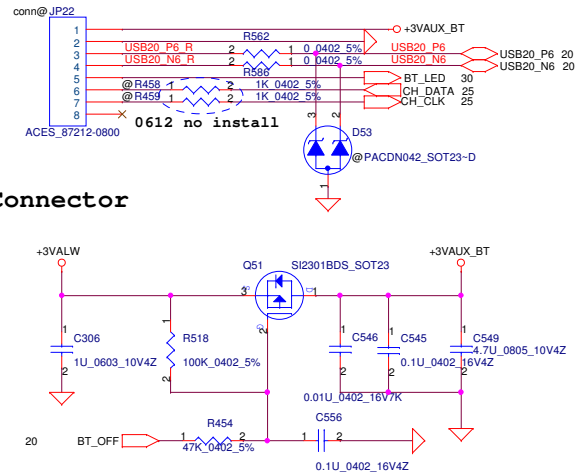
1394 connector



SMART Card connector



BT Connector



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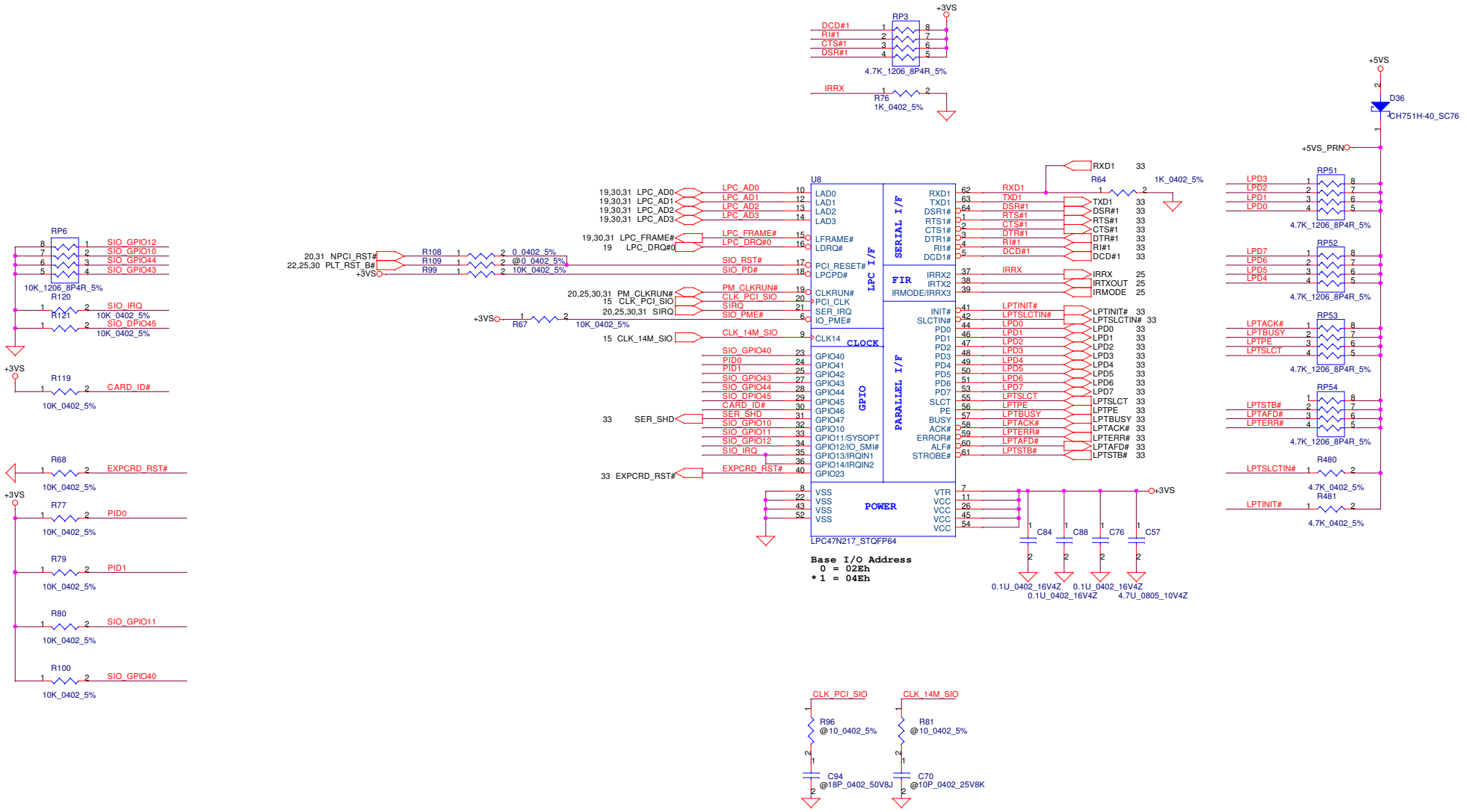
Compal Electronics, Inc.

Title: **USB & BT Connector**

Size: | Document Number: LA-3261P UMA | Rev: 0.4

Date: Tuesday, March 27, 2007 | Sheet 28 of 55



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Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217**

Size: | Document Number: *LA-3261P UMA* | Rev: 0.4

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BIOS ROM

0117 For SPI ROM debug

U66 — S IC FL 32K AT26DF321-SU SOP 8P 2.7V

SPI0 (32M*1)

U67 — SST25LF080A_SO8-200mil

SPI1 (16M*1)

0821 SPI1 no install
0906 SPI1 install
1116 SPI1 no install

0907 Add 0 ohm for SPI

Debug port

JP52 — ACES_87216-2404_24P, conn@

0629 Change Pin3 to Pin23, change Pin24 to GND

TPM1.2

U69 — SLB9635TT_TSSOP28

Base I/O Address
0 = 02Eh
1 = 04Eh

Mini-PCIE Card LED

BLUE

Finger printer

20070209 Add for FPR

JP38 — ACES_85205-0400, conn@

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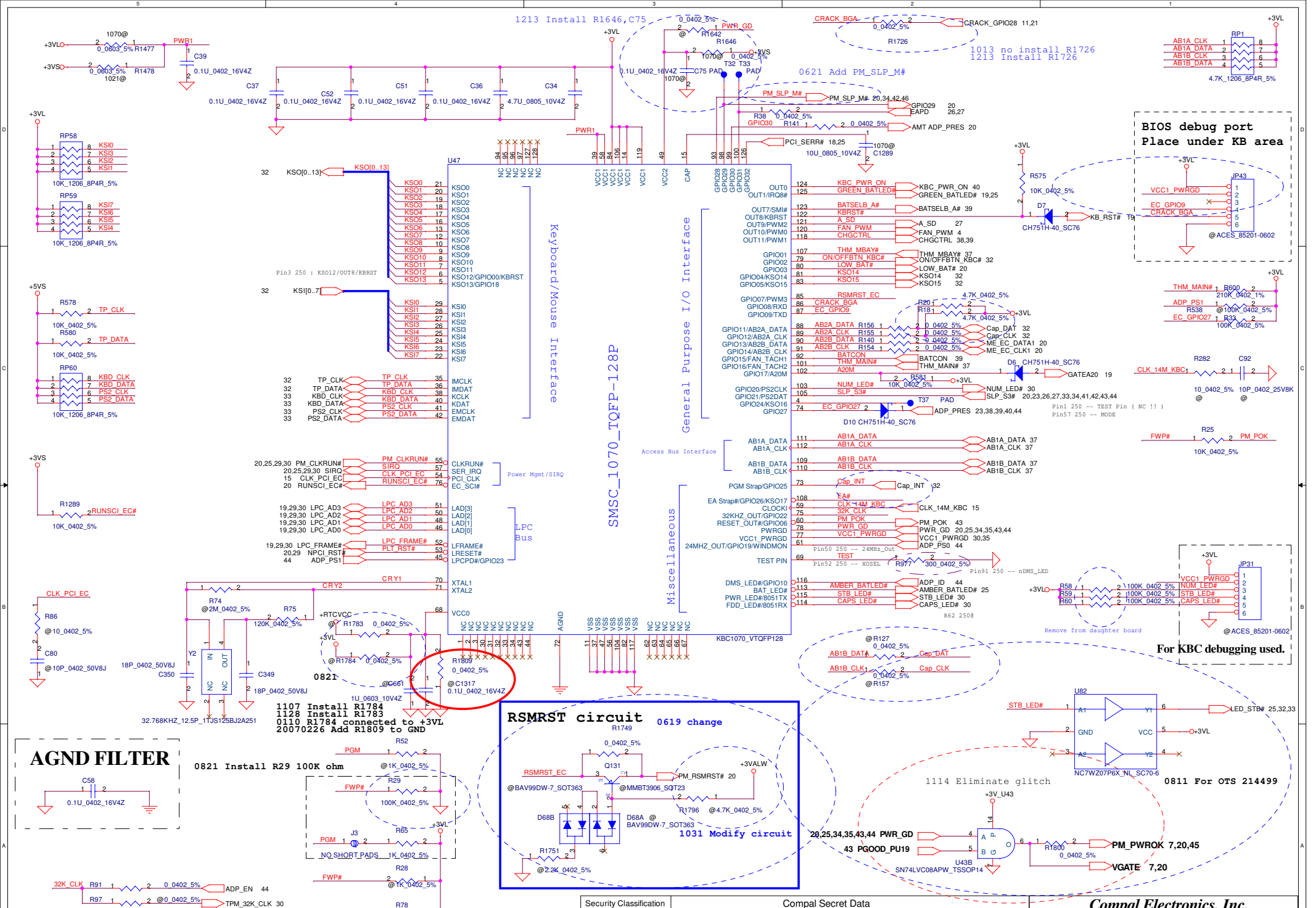
Compal Electronics, Inc.

Title: TCG/BIOS ROM/PS2/LED/SW

Size | Document Number: LA-3261P UMA | Rev 0.4

Date: Tuesday, March 27, 2007 | Sheet 30 of 55



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Title: LPC47N1021

Size: | Document Number: LA-3261P UMA | Rev: 0.4

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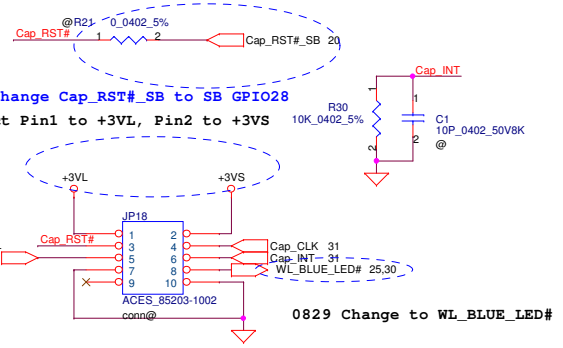
SWITCH BOARD.

0622 change

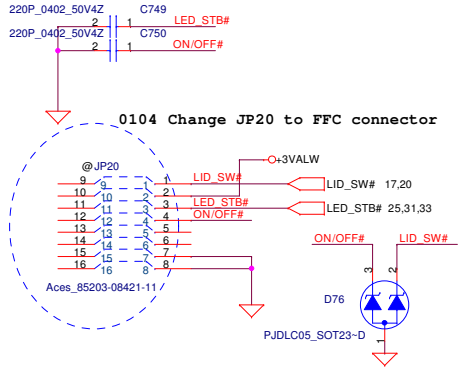


0901 Change Cap_RST#_SB to SB GPIO28

0809 Connect Pin1 to +3VL, Pin2 to +3VS

0829 Change to WL_BLUE_LED#

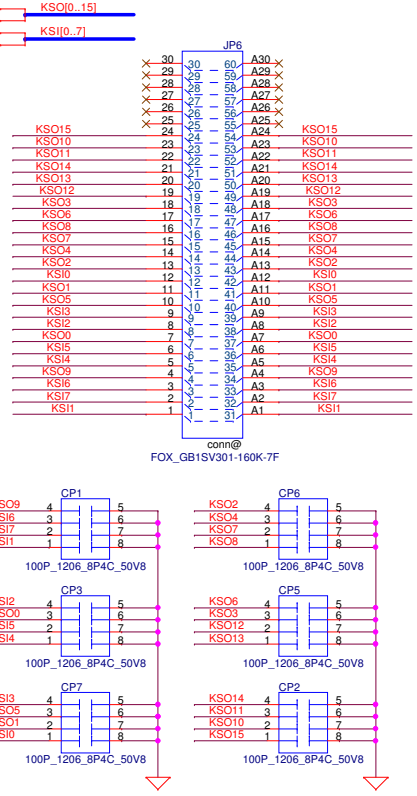
WL,Vol up,Vol down,Mute,Present button



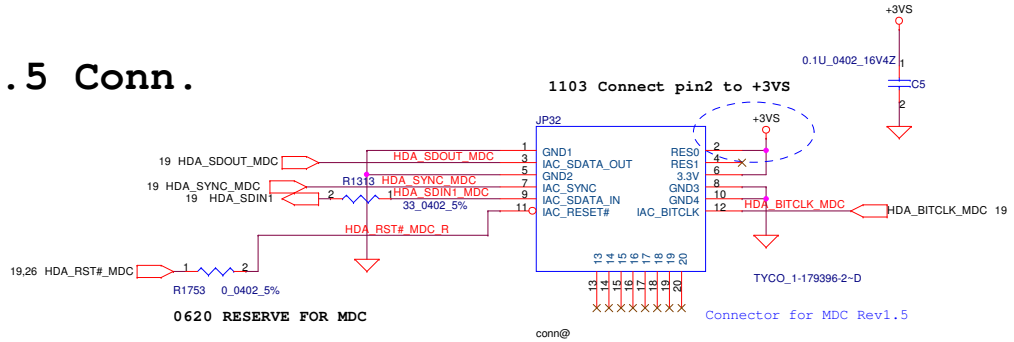
0104 Change JP20 to FFC connector

On/off ,information button

INT_KBD CONN.

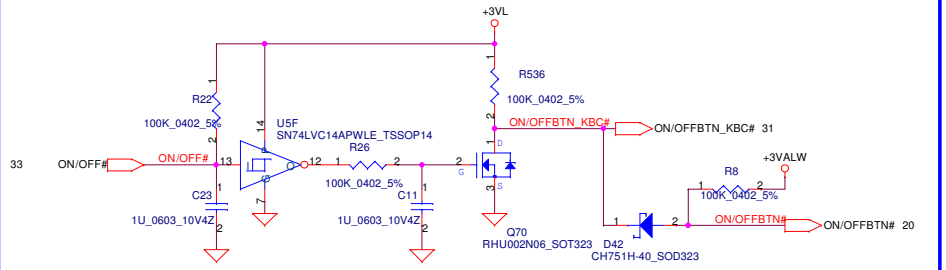


MDC 1.5 Conn.



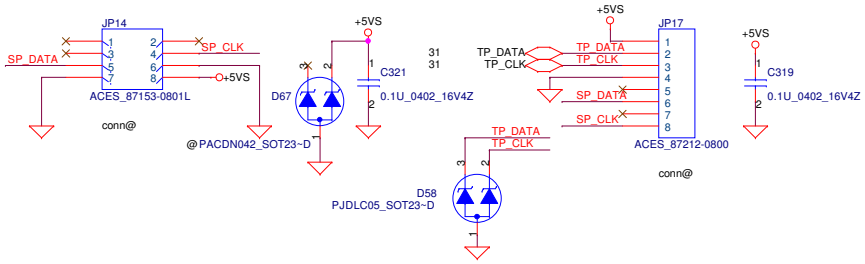
0620 RESERVE FOR MDC

Power button



TrackPoint CONN.

T/P BOARD.



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Compal Electronics, Inc.

Title: MDC/KBD/ON_OFF/LID

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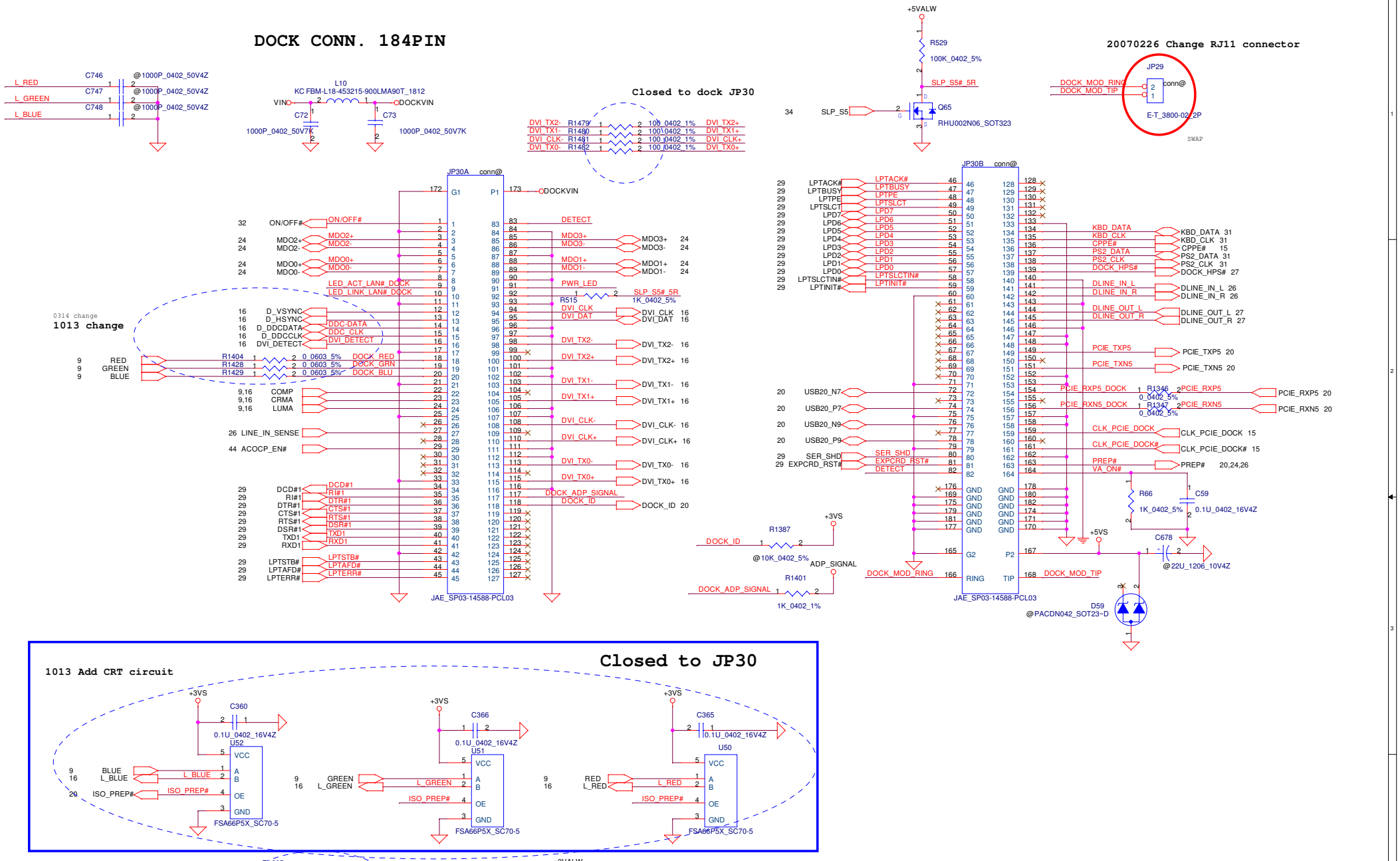
DOCK CONN. 184PIN



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Issued Date	2006/02/13	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: **Docking CONN.**

Size | Document Number: LA-3261P UMA | Rev: 0.4

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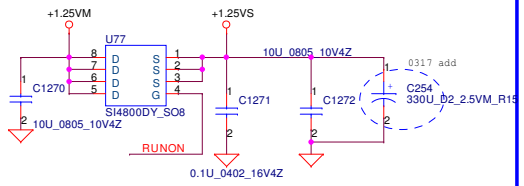
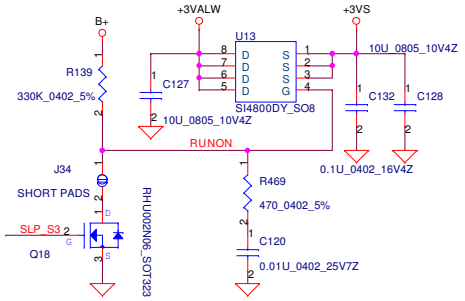
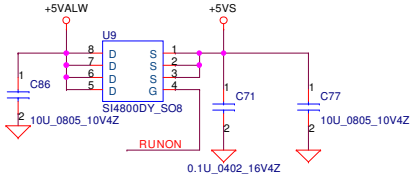
+1.25VM to +1.25VS Transfer



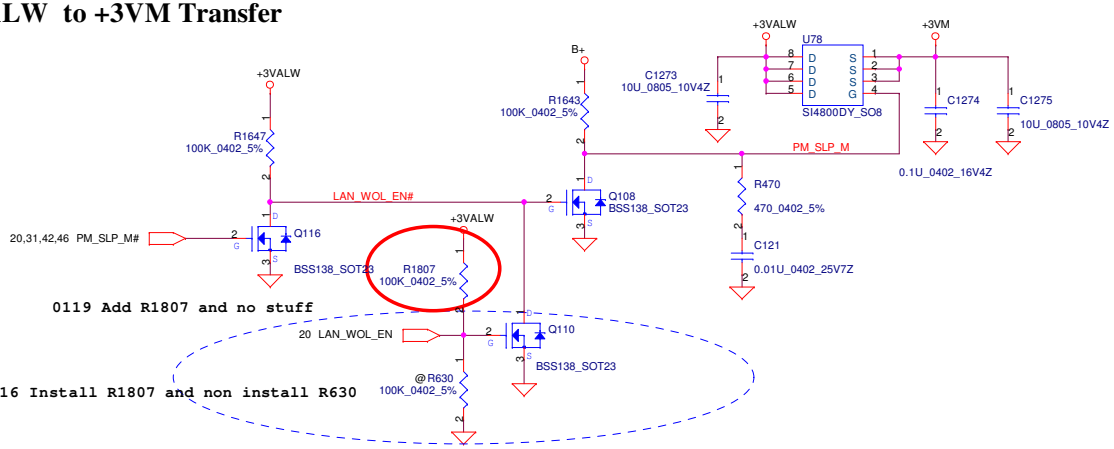
+3VALW to +3VS Transfer



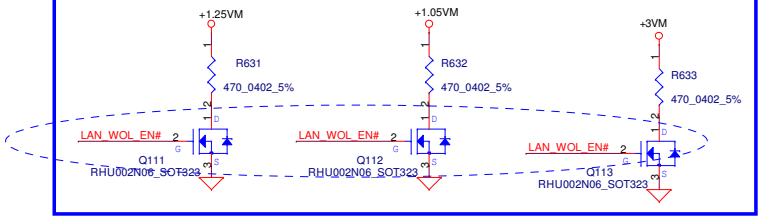
+5VALW to +5VS Transfer



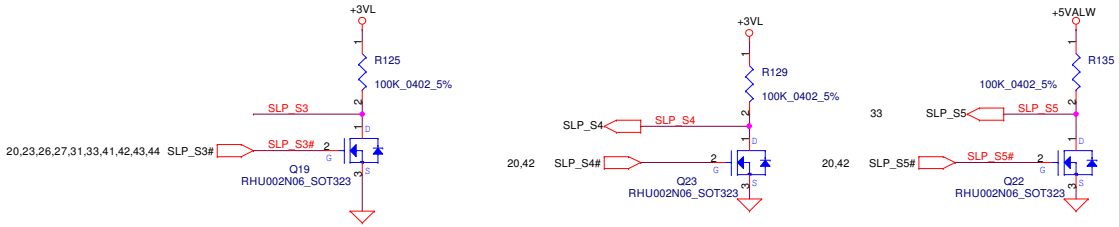
+3VALW to +3VM Transfer



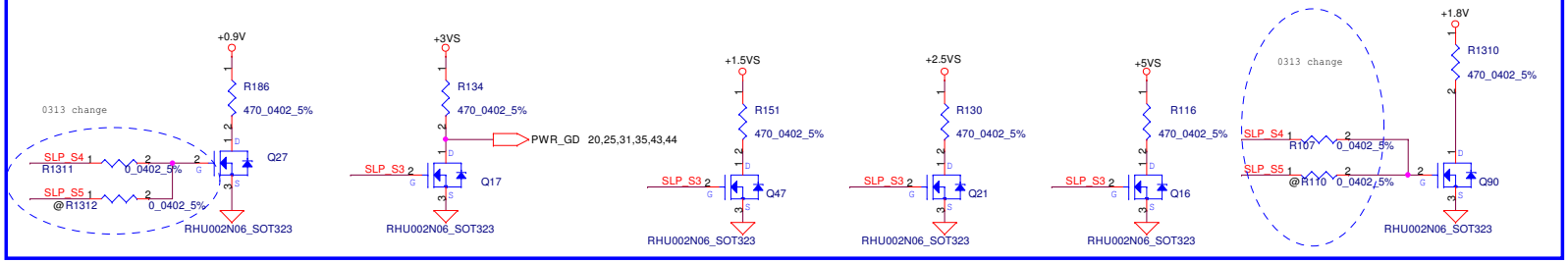
Discharge circuit-2 for V-M

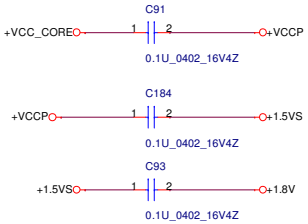


0718 Change net from PM_SLP_M# to LAN_WOL_EN#



Discharge circuit-1





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Compal Electronics, Inc.

Title: **DC/DC Circuits**

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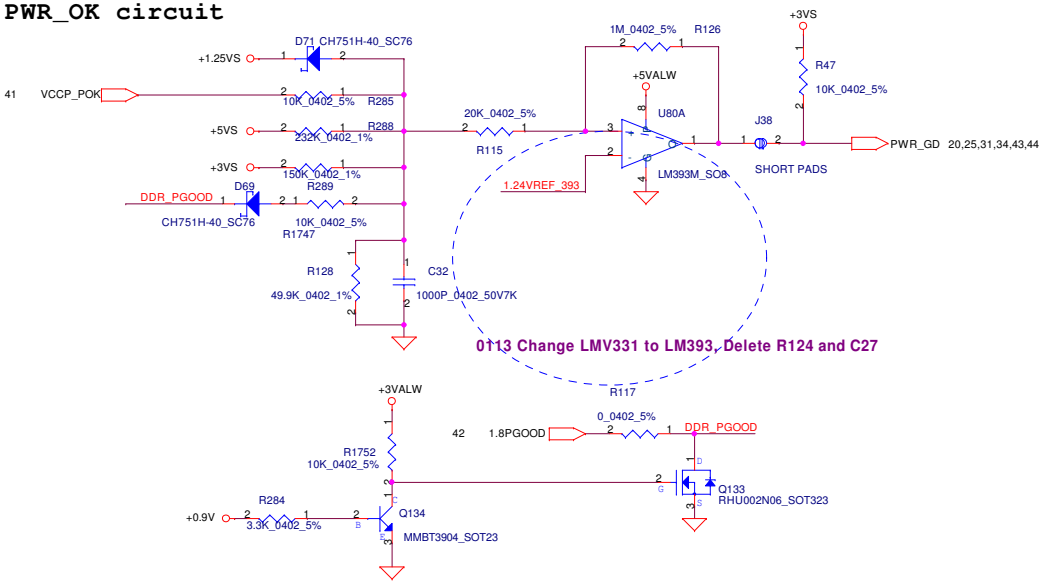
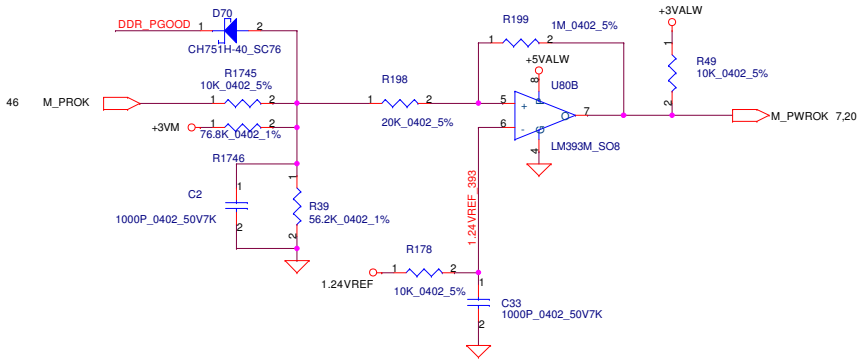
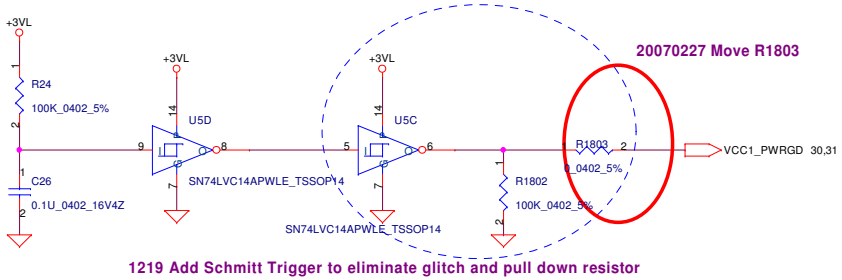
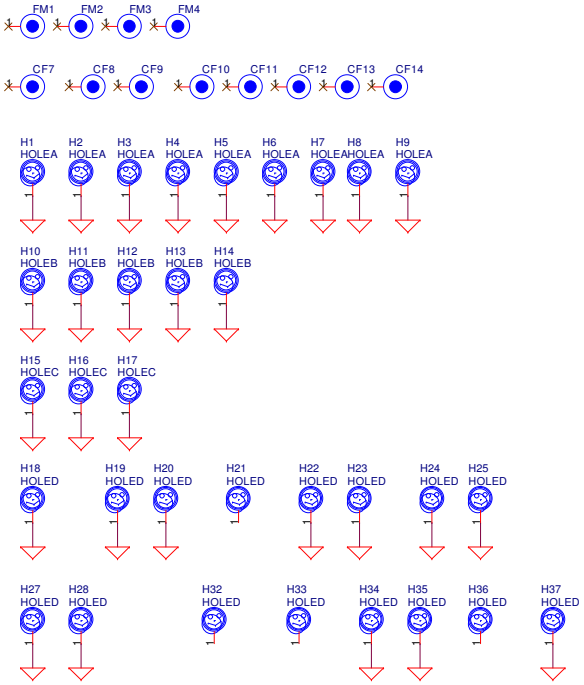
PWR_OK circuit



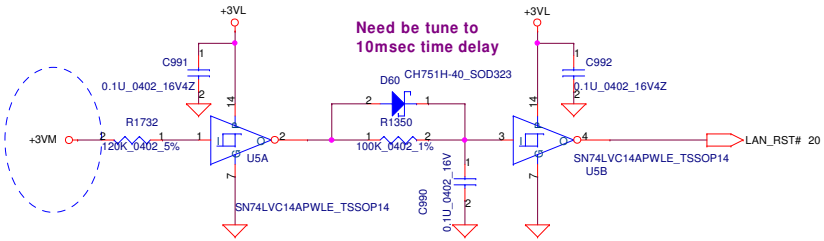


KBC PWR_OK circuit





LAN_RST circuit



1113 Tie R1732.2 to 3VM instead of 3VM_LAN

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Issued Date	2005/05/26	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: POK CKT

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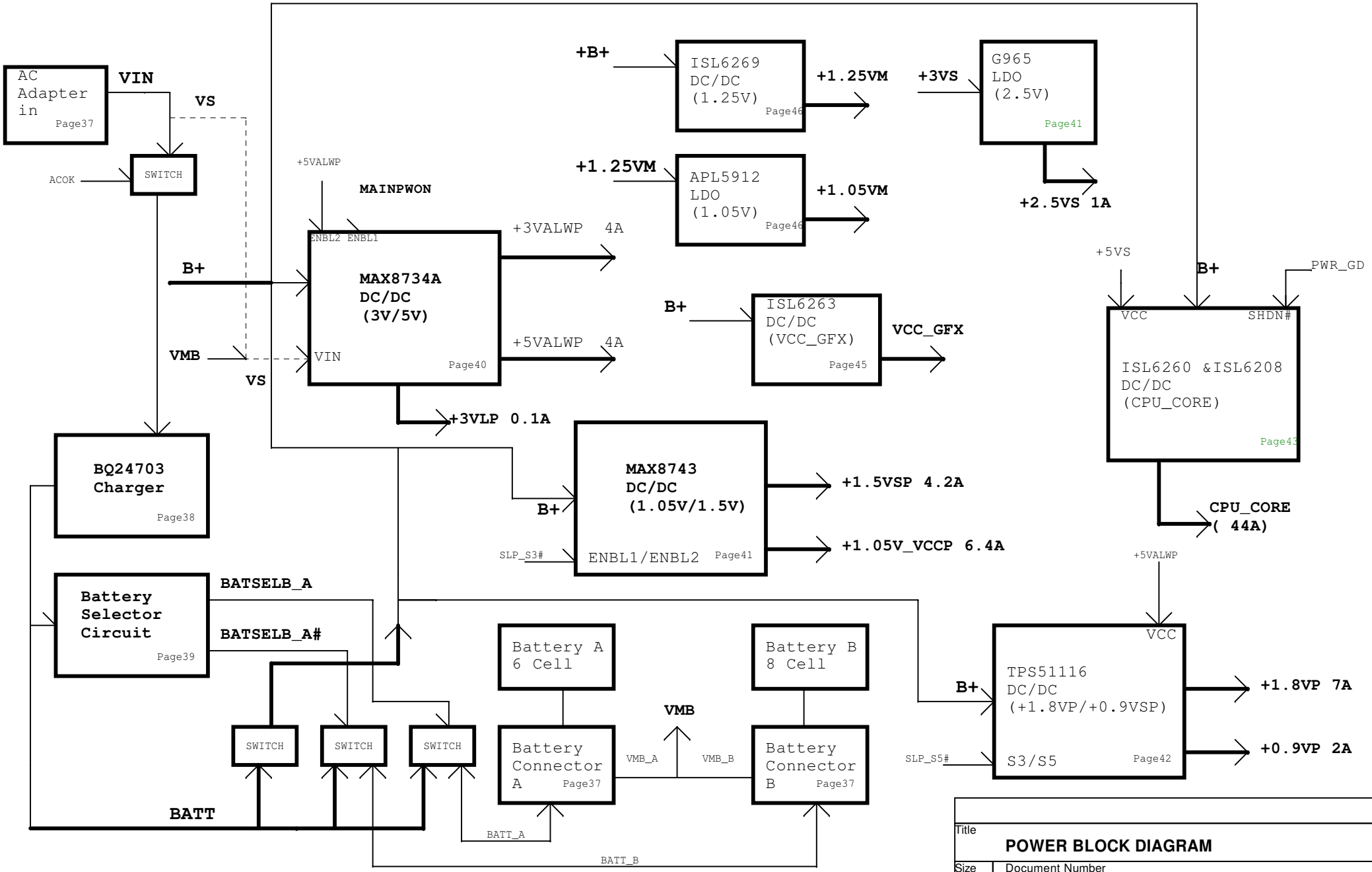

Title

POWER BLOCK DIAGRAM

Size	Document Number	Rev

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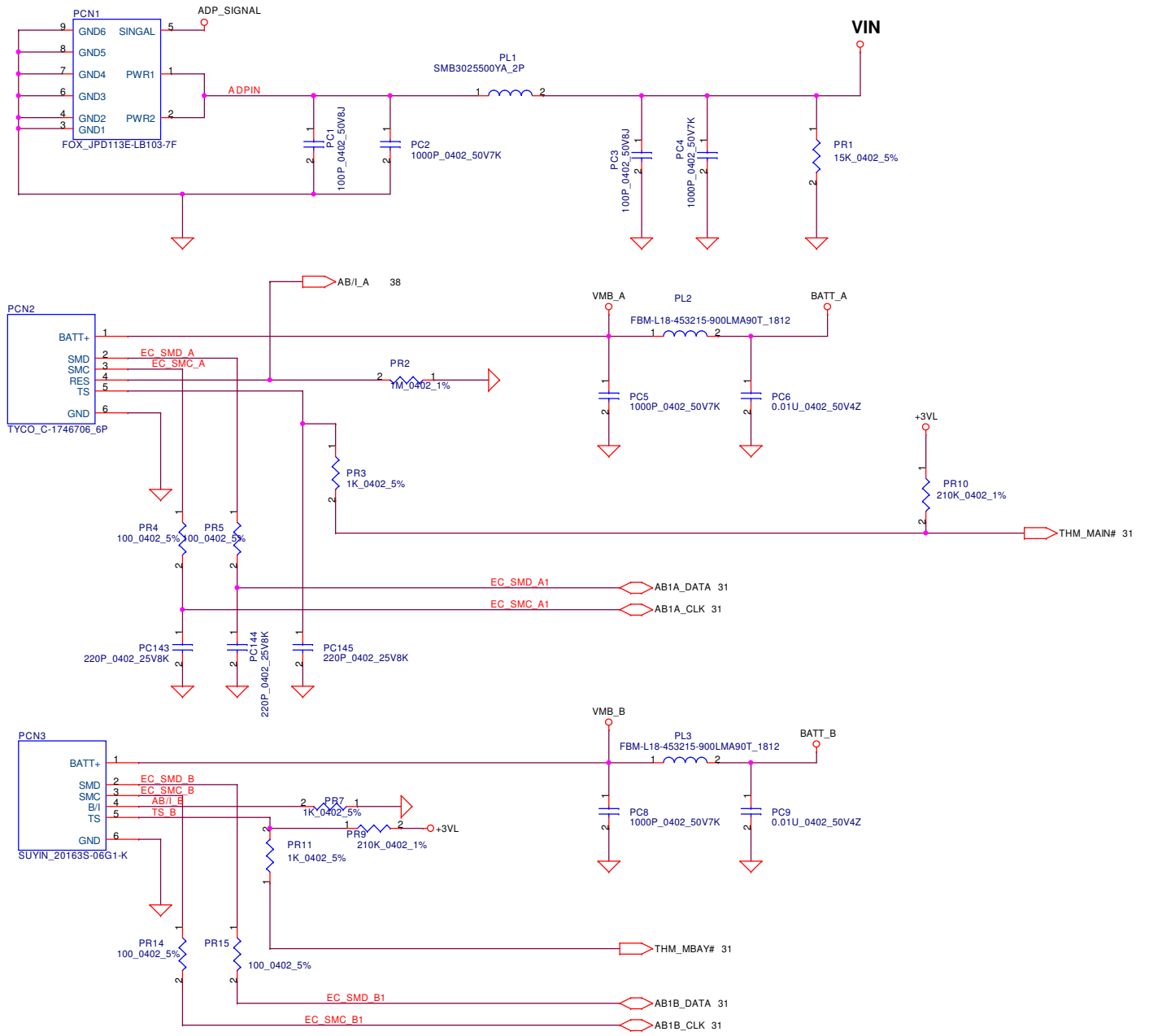

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Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: *LA-3261P UMA* | Rev

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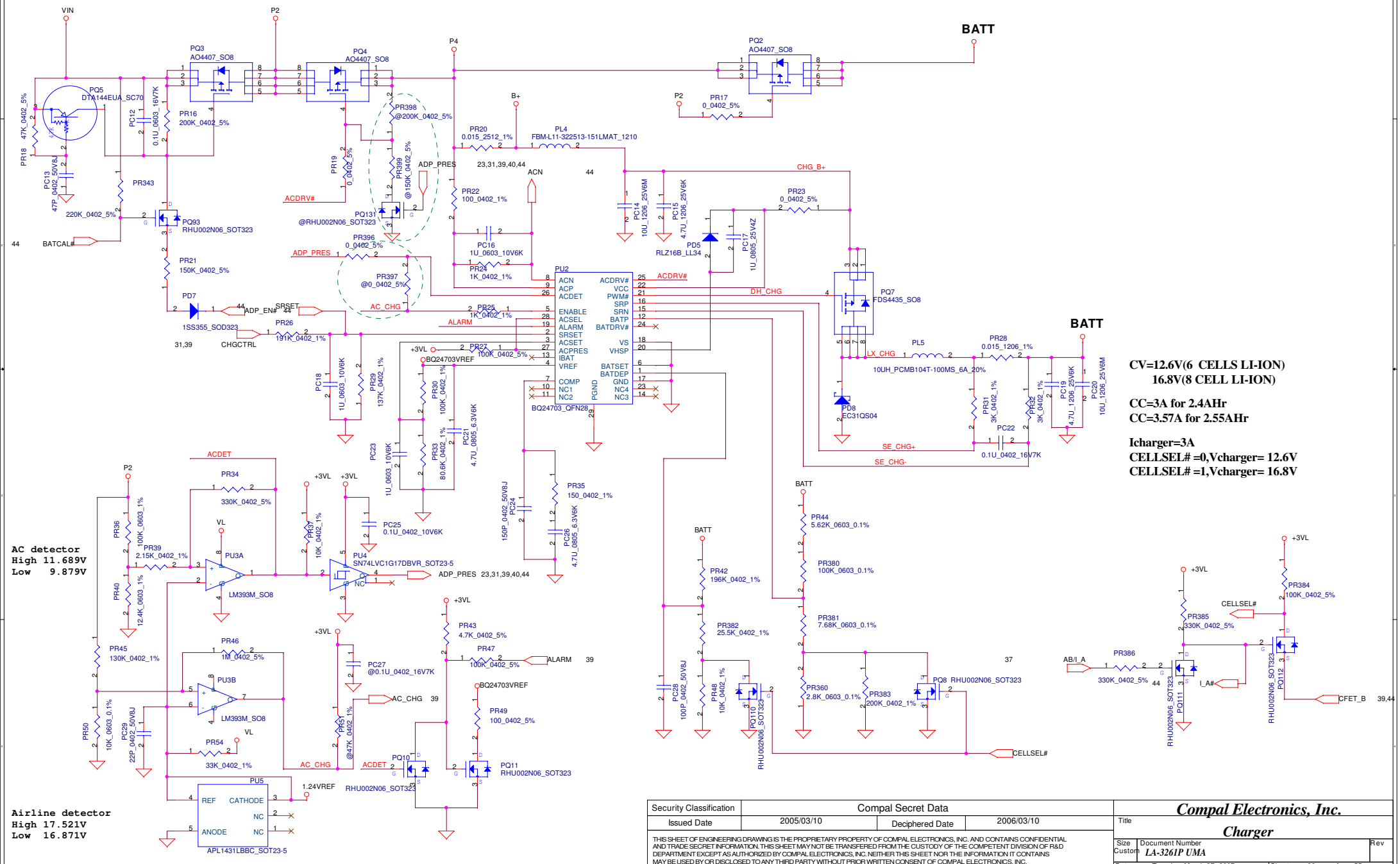

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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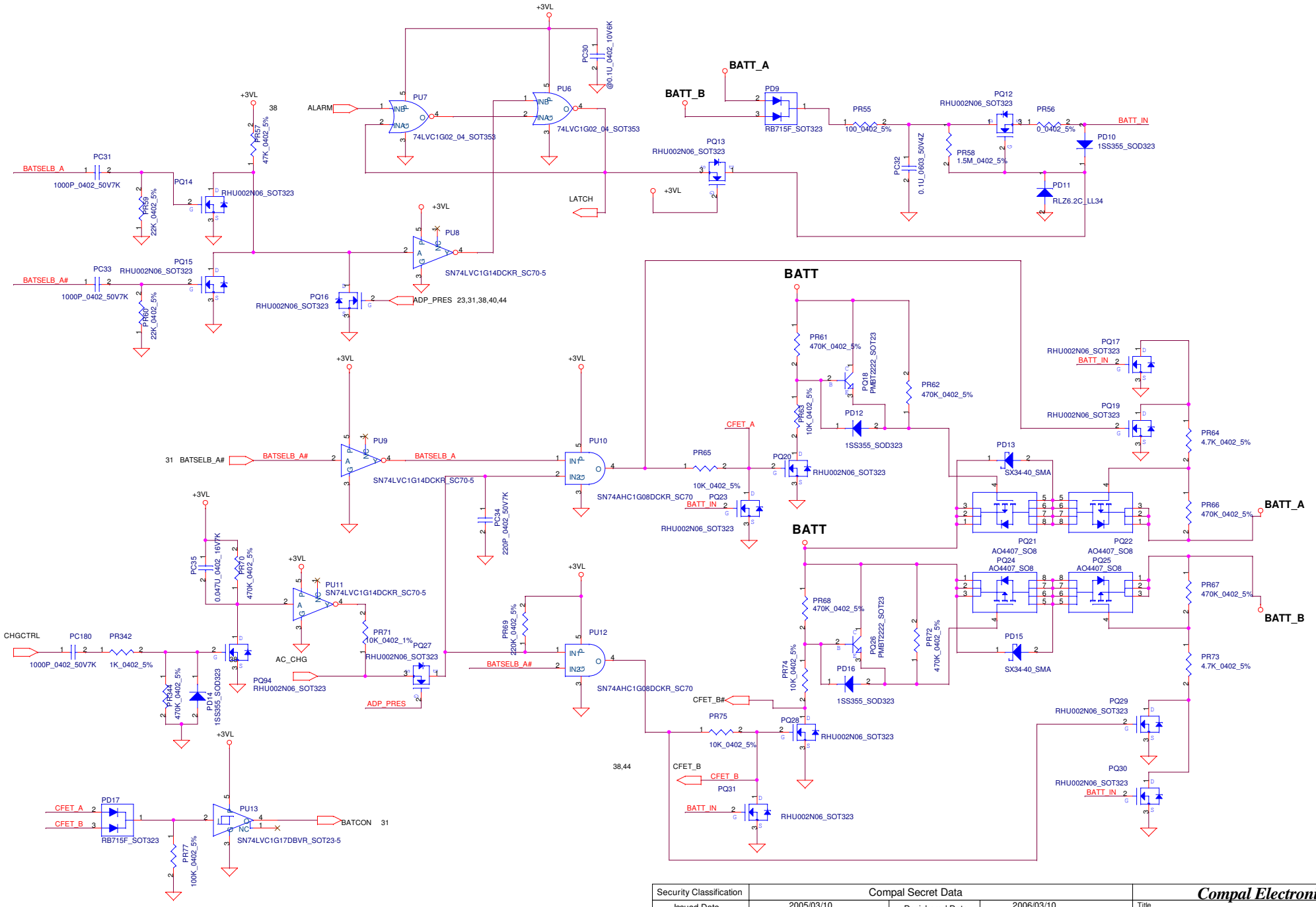
Compal Electronics, Inc.

Title: **Charger**

Size: Custom | Document Number: *LA-3261P UMA* | Rev

Date: Tuesday, March 27, 2007 | Sheet 38 of 55



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Compal Electronics, Inc.

Title: **Battery selector**

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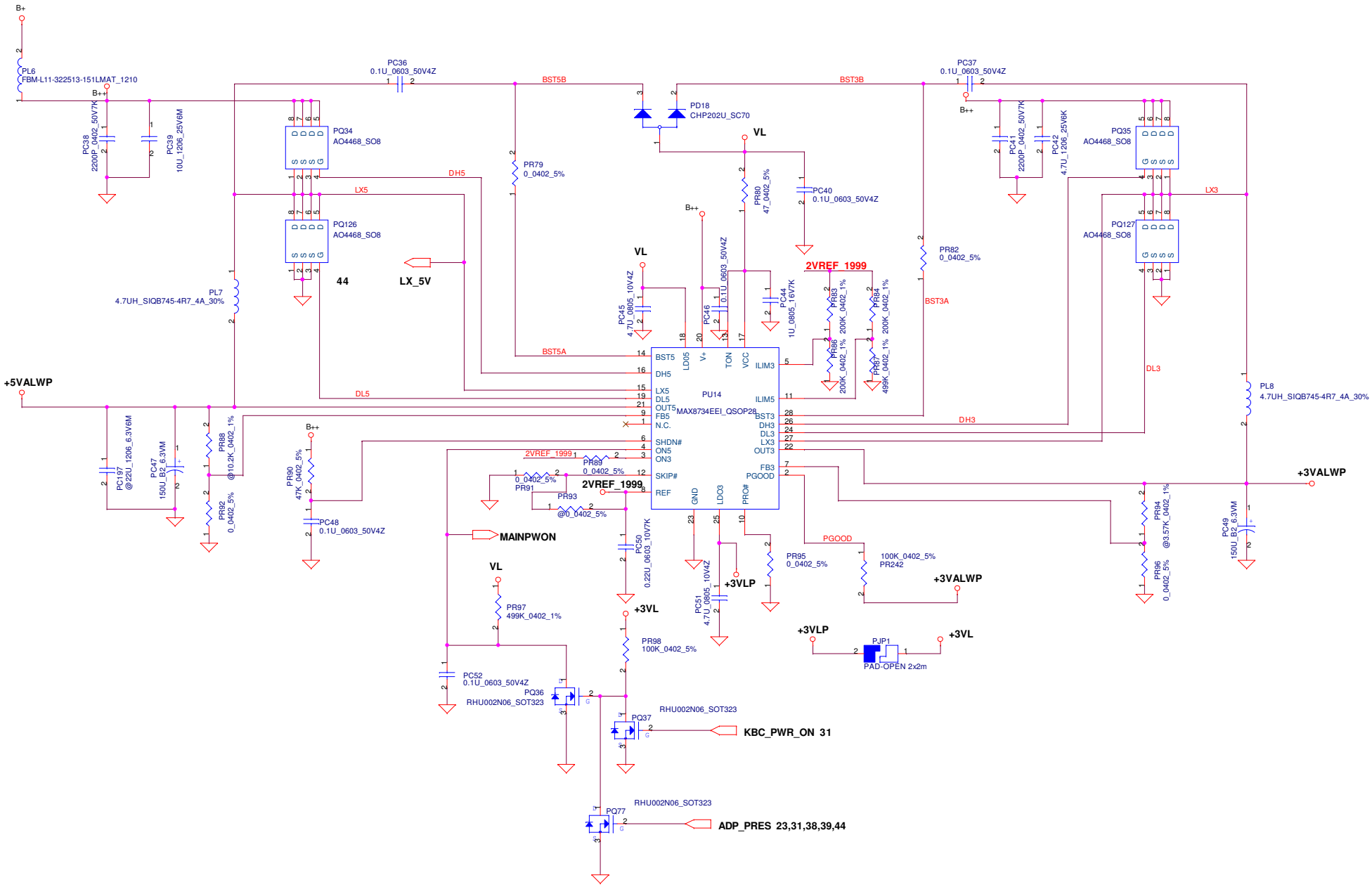
+3.3V/+5V



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Issued Date	2005/03/01	Deciphered Date	2006/03/01

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Title: 3.3V / 5V

Size: B | Document Number: LA-3261P UMA | Rev: 0.1

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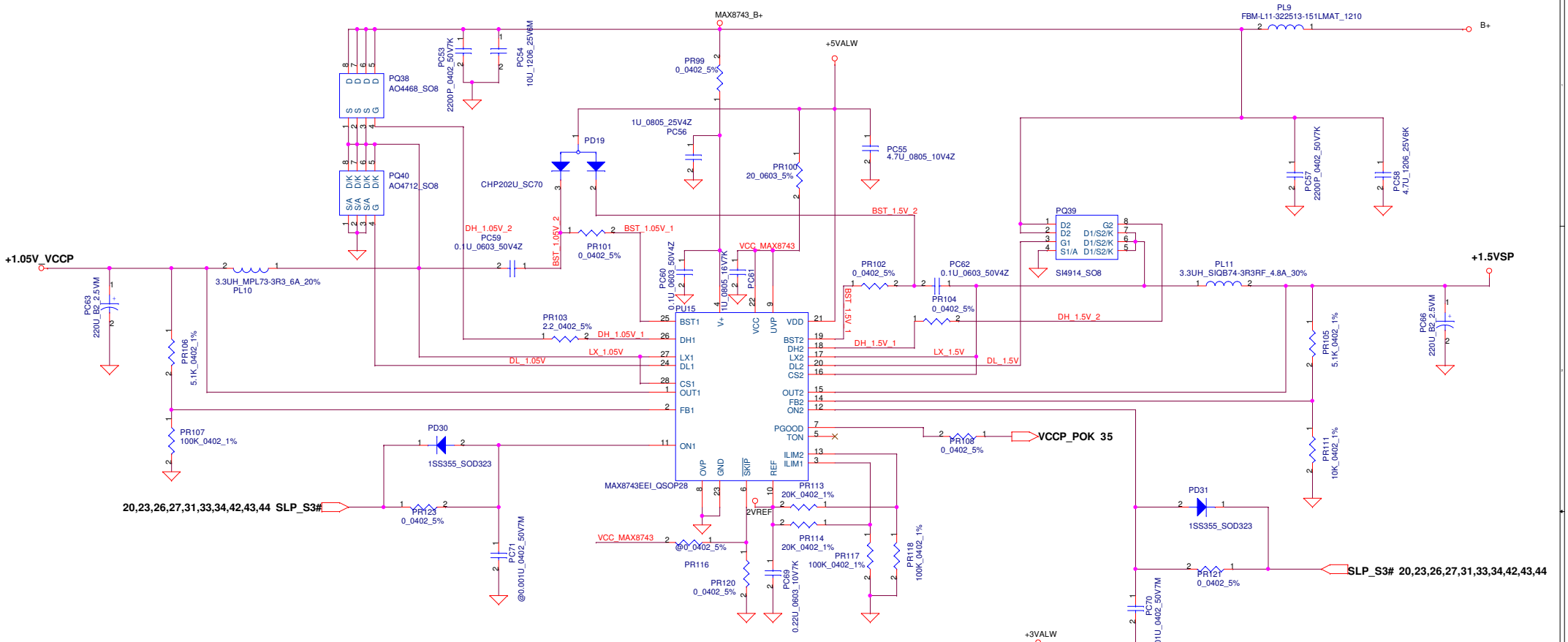
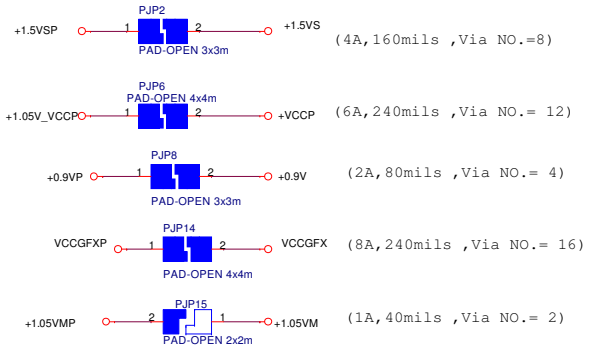
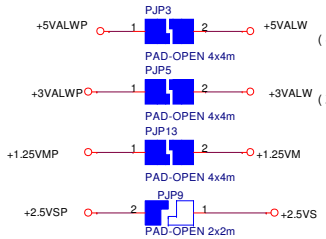


1.5VSP/ +1.05V_VCCP/+2.5V





Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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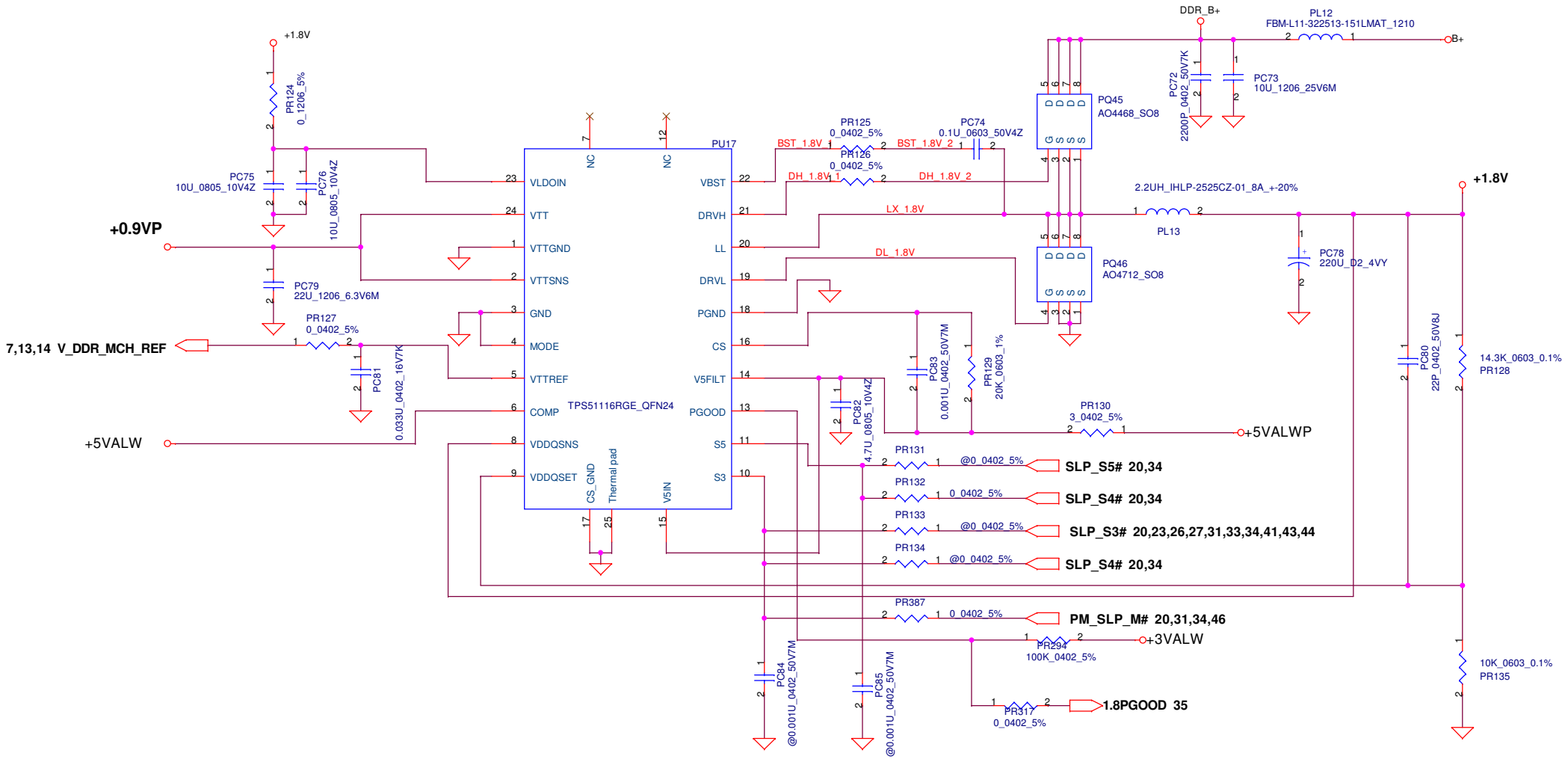
Compal Electronics, Inc.

Title: **2.5VALW/1.5VS/1.05VCCP**

Size: Custom | Document Number: *LA-3261P UMA* | Rev

Date: Tuesday, March 27, 2007 | Sheet 41 of 55



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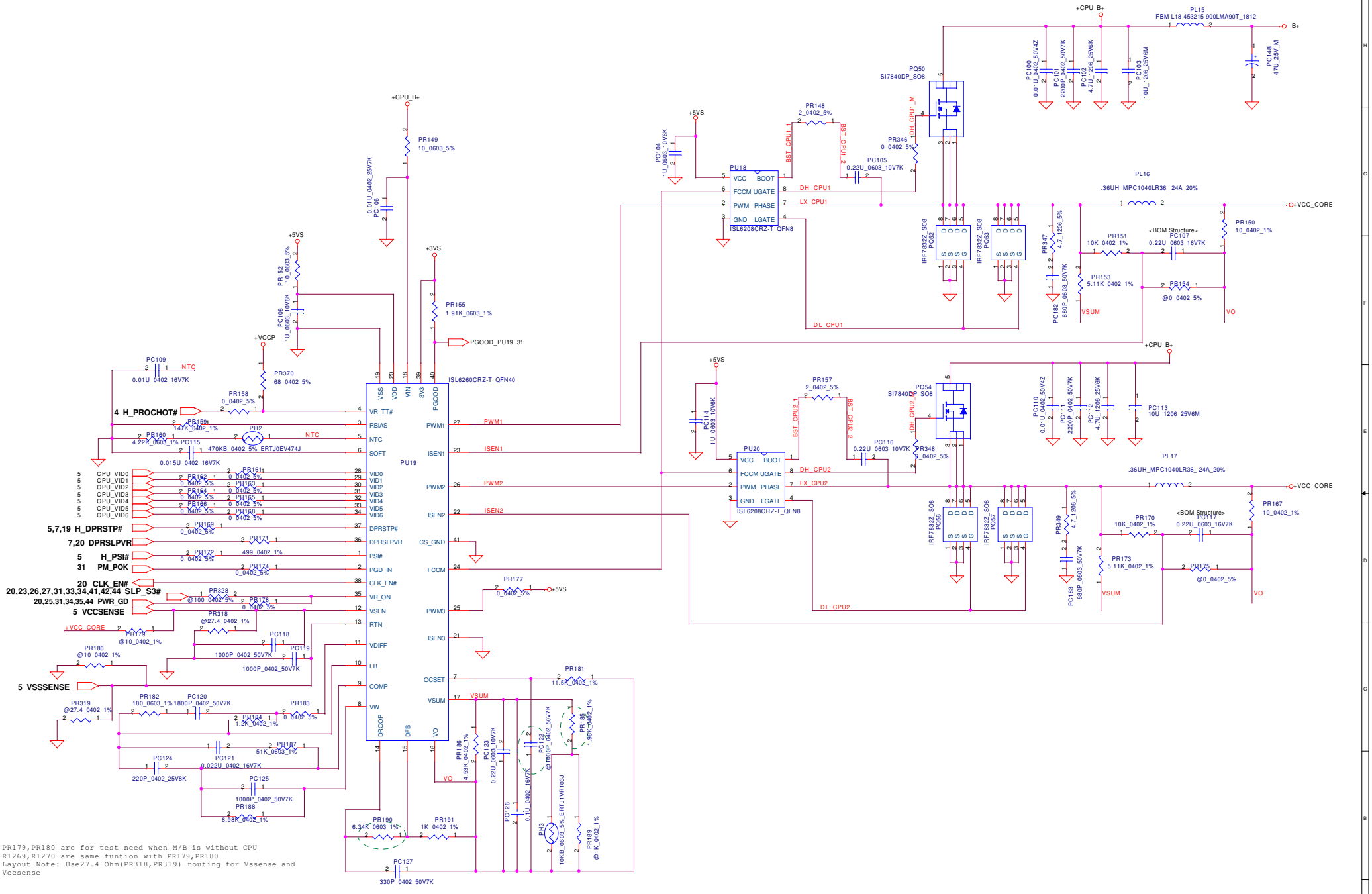
Compal Electronics, Inc.

Title: **1.8V/0.9VS**

Size: B | Document Number: LA-3261P UMA | Rev

Date: Tuesday, March 27, 2007 | Sheet 42 of 55



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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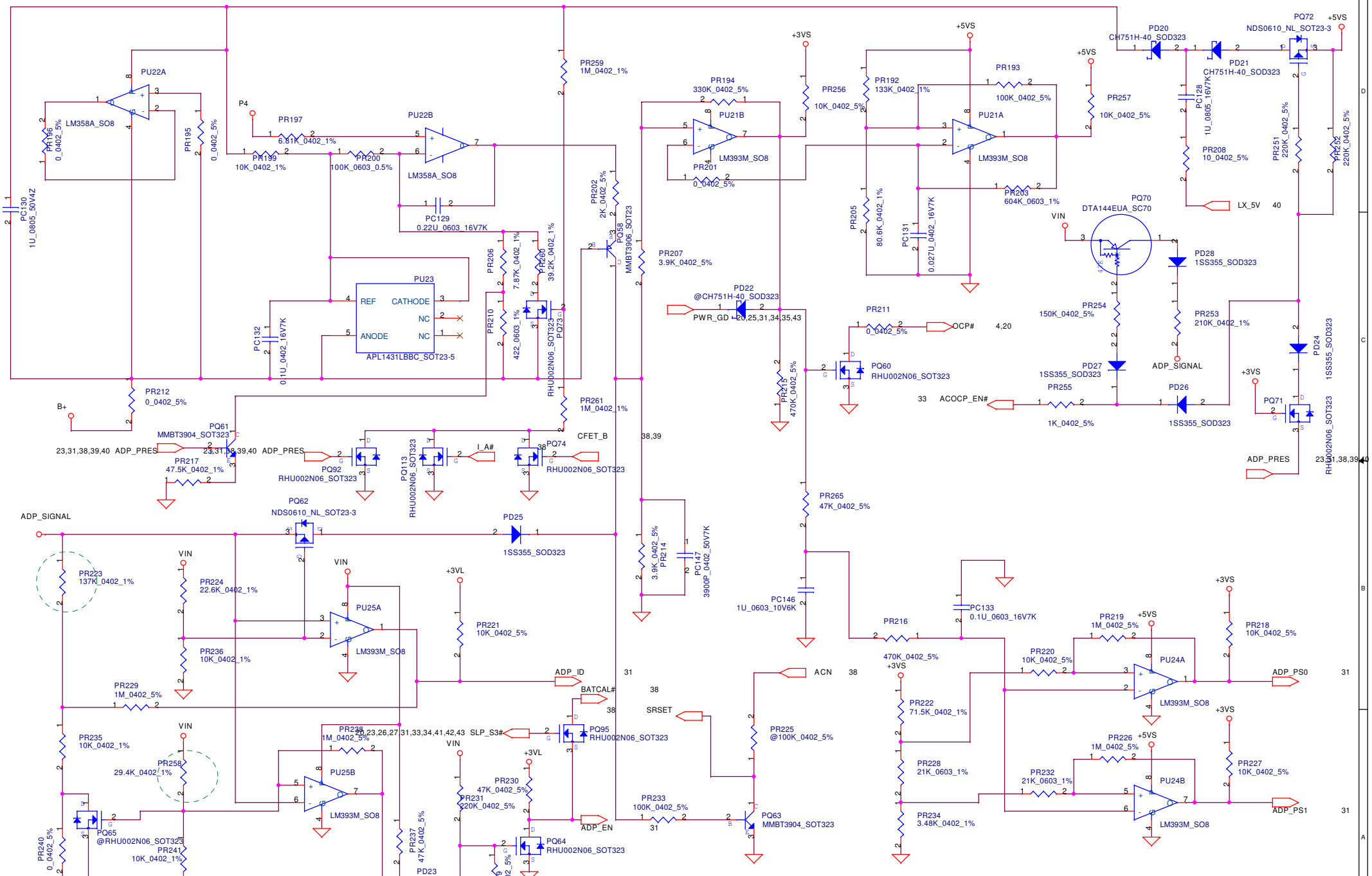
Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: **LA-3261P UMA** | Rev

Date: Tuesday, March 27, 2007 | Sheet 43 of 55



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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2005.8.20

Compal Electronics, Inc.

Title: **ADP_OCP**

Size: Custom | Document Number: LA-3261P UMA | Rev

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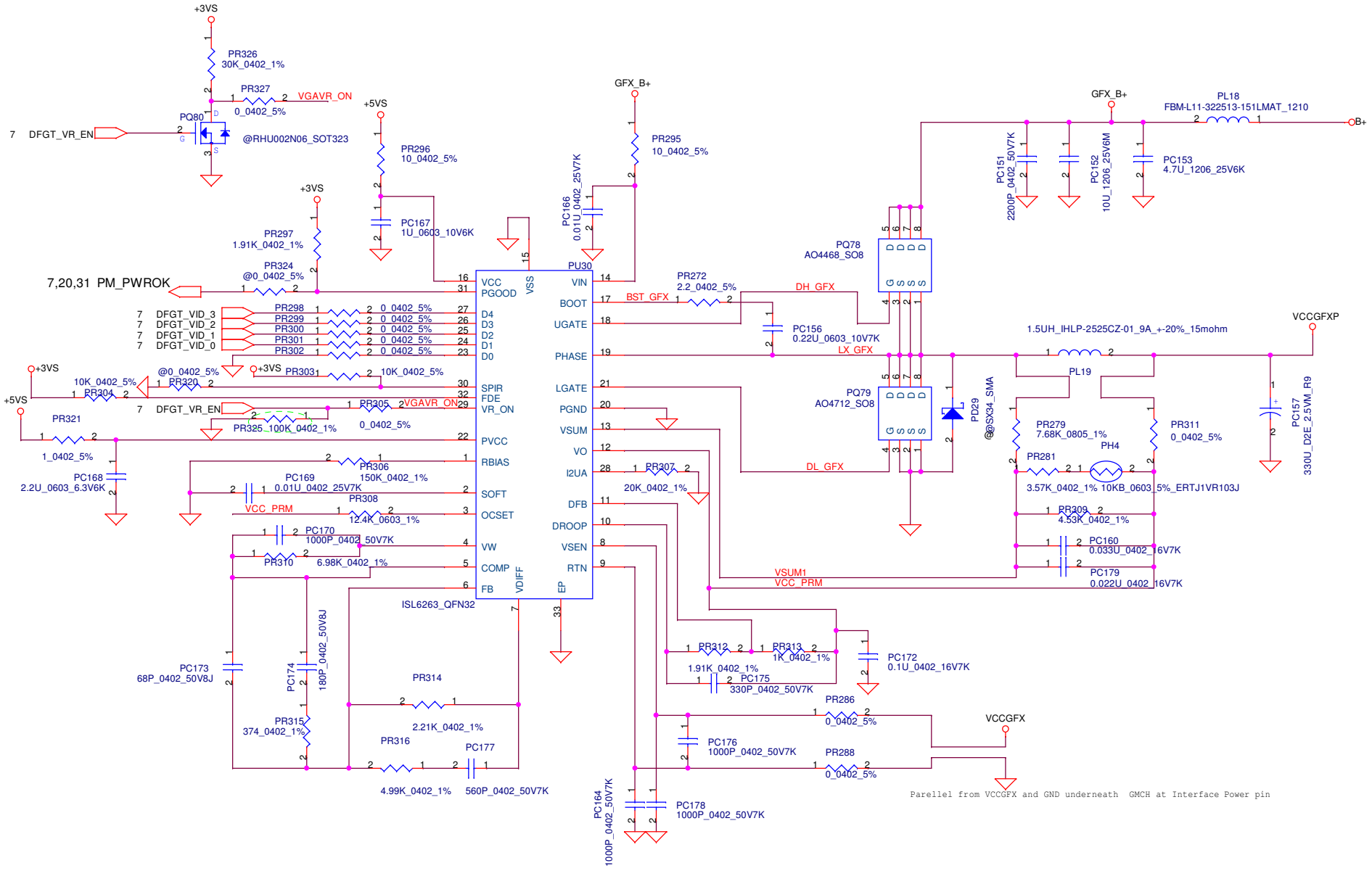

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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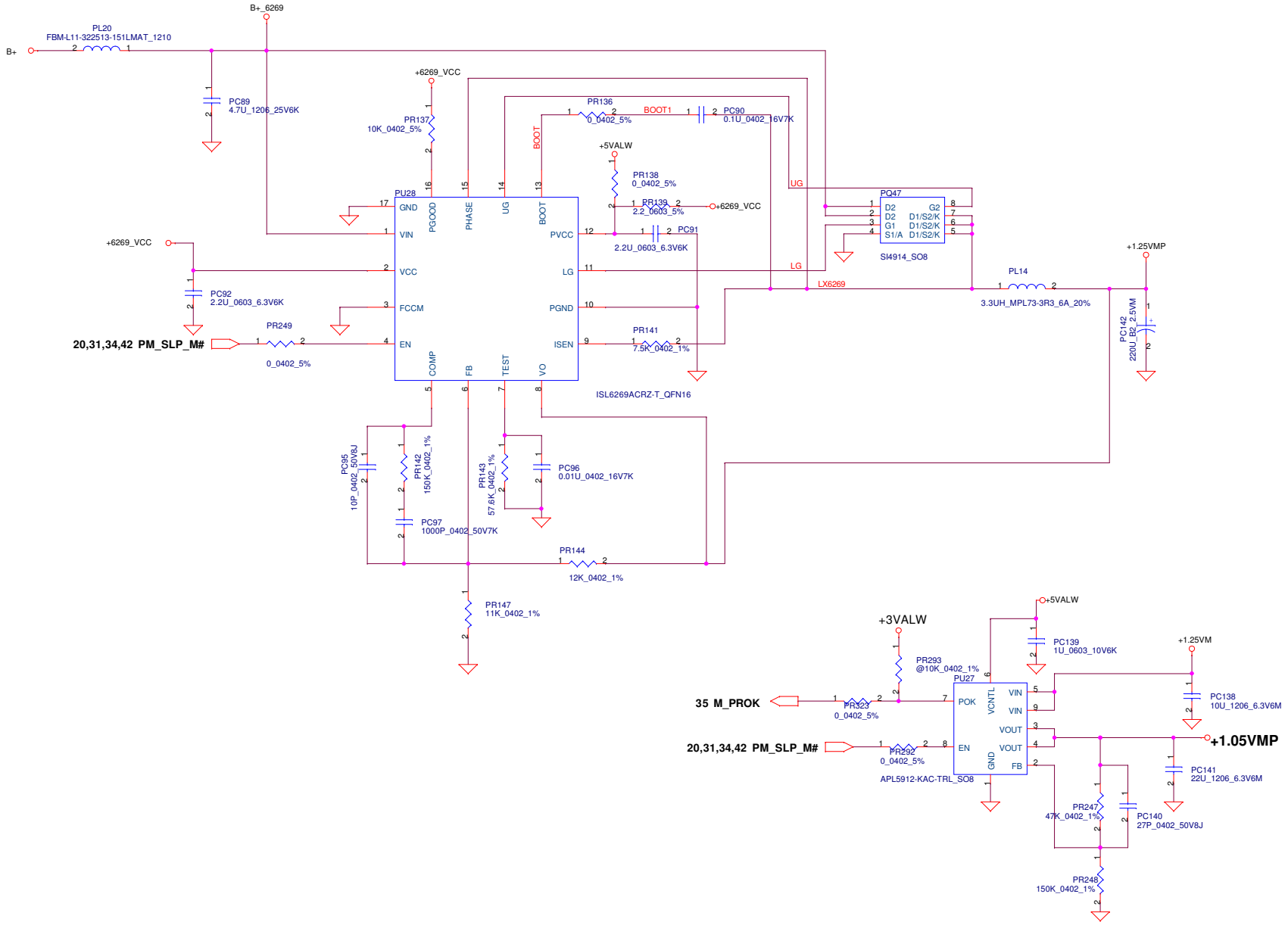
Compal Electronics, Inc.

Title: **VCCGFX**

Size: B | Document Number: LA-3261P UMA | Rev

Date: Tuesday, March 27, 2007 | Sheet 45 of 55



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **+1.25VMP/+1.05VMP**

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Version Change List (P. I. R. List) for Power Circuit (1)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Page42	1.8V/0.9V	3/9/2006	HP RL	Power Sequence	No install PR131 and install PR132 Change SLP_S5# at PR134.1 to SLP_S4# No install PR133 and install PR134 Add a 0 ohm resistor PR317 (no stuff) on M_PWROK	DB
2	Page45	VCCGFX	3/9/2006	Compal	MAX8776 VID table can't meet Intel VID SPEC	Change VCCGFX IC solution from MAX8776 to ISL6263	DB
3	Page43	CPU_CORE	3/10/2006	HP RL		Add 27.4 ohm pull-down (no stuff) on VCCSENSE & VSSSENSE near VR	DB
4	Page46	1.25VM/1.05VM	3/9/2006	HP RL	M_PWROK	Add a 0 ohm resistor PR323 (install) on M_PWROK change PR293 pin1 to +3VL	DB
5	Page46	1.25VM/1.05VM	4/10/2006	Compal	Correct 1.25VM voltage setting	Change PR144 to 12K and PR147 to 11K.	DB1-A
6	Page45	VCCGFX	4/10/2006	Compal	Power Sequence	Add a 0ohm PR324 (no stuff) on PM_PWROK	DB1-A
7	Page45	VCCGFX	4/24/2006	Compal	In S3 state, DFGT_VR_EN will no be actively driven, it is better to have a pull down resistor on DFGT_VR_EN.	Add a 30Kohm PR325	DB1-A
8	Page42	1.8V/0.9V	5/15/2006	HP MJ	Power Sequence	Change 1.5S to 1.8V in page 42 at pin 23 (VLDOIN)	DB1-B
~~9~~	~~Page46~~	~~1.25VM/1.05VM~~	~~5/15/2006~~	~~HP MJ~~	~~Power Good~~	~~Add PU34~~	~~DB2~~
10	Page38	Charge	5/15/2006	compal	For reducing charge temperture.	Change PL5 from 8.2uh MPL73-8R2 to 10UH_PCMB104T-100 Change PR28 from 0.015_2512 to 0.015_1206	DB2
11	Page43	CPU_CORE	6/5/2006	HP MJ	Power Sequence	investigate that SLP_S3# connect VR_ON and PM_POK connect PGD_IN	DB2
~~12~~	~~Page41~~	~~VCCP&1.5VS~~	~~6/5/2006~~	~~compal~~	~~Swap +1.05V_VCCP and +1.5VS location for improving power plane.~~	~~Change PR107 from 100k to 10K,PR111 from 10K to 100K.~~	~~DB2~~
13	Page37,38,44		6/22/2006	HP MJ	Chimay support for new battery cell chemistries	P38 : remove PR52, PR38, PR41,PR53, PQ9 P39 :remove PR262, PR263, PR264, PR76, PQ75, PQ76, PQ32 P37: Add PQ81~PQ91 PR329~PR341,PD32~PD36 P38 :Add PD37 P44 :Add PQ92,PD38,PD39	DB2
14	Page41	2.5VALW/1.5VS /1.05VCCP	8/17/2006	HP MJ	For sequence fine tune	Add PC181 but not be installed	SI
15	Page43	CPU_CORE	8/17/2006	HP RL	Add 68ohm pull up to +VCCP at PU19.4 per Intel DG1.0 sec. 4.4.1.3 Figure 50	Add PR345 as 68ohm between +VCCP and PU19.4	SI
16	Page44	ADP_OCP	11/08/2006	HP RL	Identify 65W adapter as full adapter	Change PR223 from 180K to 182K, PR258 from 29.4K to 22.6K	SI2
17	Page43	CPU_CORE	11/08/2006	compal	For EMI concern, add snabber	Add PR349 and PR347 as 4.7ohm, Add PC183 and PC182 as 680pF Change boost resistor (PR148 and PR157)from 0 to 2 ohm	SI2
18	Page38	Charge	11/08/2006	compal	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI2
19	Page42	1.8V/0.9V	11/13/2006	HP	Add PM_SLP_M# sequence	Add PR387	SI2

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Version Change List (P. I. R. List) for Power Circuit (2)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	Page43	CPU_CORE	2/28/2007	Compal	Fine tune CPU CORE solution	No install PC122 Change PR185 from 3K to 1.96K Change PR190 from 6.19K to 6.34K	MV
21	Page44	ADP_OCP	2/28/2007	HP	System identity	Change PR223 from 182K to 137K Change PR258 from 22.6K to 29.4K	MV
22	Page38	Charger	3/1/2007	Compal	Reserve circuit for testing Energy STAR	Reserve PR397, PR398, PR399 and PQ131 Add PR396 as 0 ohm.	MV

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Title: **PWR PIR Sheet (1)**

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
For DB1-B						
<2006.03.29>	1		Reserve resisters on Debug ports	30	Add R170, R201, R202 and CLRP3 jopen	0.2
	2	SATA footprint is wrong	SATA connector's PCB footprint is wrong	22	change to OCTEK_SAT-22DD1G_22P	0.2
<2006.04.10>	1		follow Intel suggestion for XDP_DBRESET#	4, 20	R243 no install and R1589 install (XDP_DBRESET#)	0.2
	2		Change component' s footprint for supply and layout easy	07	R1443 change from 0603 size to 0402	0.2
	3		+VCC_PEG should be 1.05V instead of 1.25V for Creatline	10	R1465 install and R1467 no install	0.2
	4		Monitor NB cracked pins	11	Add Q118, Q119, Q120, Q121, Q122, Q123, R1700, R1701, R1702 R1703, R1704, R1705, R1706, R1707, R1708, R1709, R1710, R1711	0.2
	5		Monitor SB cracked pins	21	Add Q124, Q125, Q126, Q127, R1716, R1712, R1713, R1717 R1718, R1714, R1719, R1715	0.2
	6	SPI BIOS can not flash.	For SPI BIOS flash issue	23	Delete Q102, R178 and Q115 Q102 pin1 short to pin3-->+3VM connect to +3VM_LAN PLT_RST# connect to PM_LAN_EN	0.2
<2006.04.21>	1		For LAN link status	18	change PCI_PIRQG to LED_LINK_LAN# and add R1727 0 ohm	0.2
	2		For LAN active status	23	Add LED_ACT_LAN# this net	0.2
	3		For ADP_PRES new design	20	add D68 and disconnect LED_LINK_LAN#	0.2
	4		For LAN net name	19	change net name from LAN_RST to LAN_RSTSYNC change net name from LANLINK_STATUS# to LED_LINK_LAN#	0.2
	5		For Compal Fan design	4	change Fan connector pin 1 and pin4	0.2
<2006.04.24>	1		For NIC RST	20 35	change net name from PM_LAN_EN to LAN_RST# Add a Resister R1722(0 ohm), R1732, R1731(no install) change net name from PGD_IN to LAN_RST# Install C991, C990, C992, D60, R1350 Adjust C990 and R1350 value to 0.1uF and 100K ohm.	0.2
For DB1-C						
<2006.05.15>	1	System can not power on	For RTC CLK	19	add R1733	0.3
	2	LAN can not work	For LAN function	23	modify LAN relative schematics	0.3
	3		For PWR OK	35	Change R124 pin2's voltage from 0.9v to 1.24VREF Change R1732 pin2's voltage from 3VM to 3VM_LAN	0.3

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
For DB2 <2006.05.29>	1		Add new feature (Kill switch)	22	Add R1736, jp53, R1737 and Q129	0.4
	2		modify CRACK_GPIO28 circuits	11 21	delete R1700, R1707, R1705-->NB delete R1712, R1713, R1714-->SB	0.4
	3		Change pull up for CK505 strapping	15	on R1108, R1690, R1245 from +3.3VM_CK505 to +3VS	0.4
	4		for LAN IVRI thermal protect and limit current.	23	add R1	0.4
	5		Add resisters for GPI pins floating	20	addR3, R6, R9, R11, R15	0.4
	6		Change KBC RST pin	31	change from PLT_RST# to NCPI_RST#	0.4
	7		Change to USB port assignments	28	Move Dock1 from USB8 to USB7 and move WWAN from USB3 to USB8	0.4
<2006.06.12>	1		New PCIE assignments	20	Updated Changes: PCIe - port1 = Free PCIe - port2 = WLAN PCIe - port3 = Free PCIe - port4 = Robson PCIe - port5 = Docking PCIe - port6 = Intel LOM is fixed at this location	
	2		Change SW design to Capsense SW.	32	Change SW Connector JP18 type and relative circuits	
	3		Add new feature (Robson)	15	Add R5, R13 on SRC6 and R14, R17 on CLKREQ_E#	
	4		Change GPIO pins	18 20	change GPIO4(SB) from LED_LINK_LAN# to PCI_PIRQG# change GPIO1(SB) from CB_PE# to LANLINK_STATUS#(i)	
	5		Change HP debug port power source	30	Add R1740, R1741 and connect to +3vs	
	6		Change KBC 1070 GPIO pins	31	CRACK_GPIO28 from GPIO28(KBC) to GPIO8(KBC) add R155, R156, R18, R20 and their signals connect to JP18 Add Cap_INT on GPIO25(KBC)	
	7		change WALN power source	25	change from +3valw to +3vM	
	8		Change U75 power source for LAN function	23	U75 should be powered by V3.3M instead of 1.8VM	
	9		Change USB power switch control pin	28	From S5 to S4_STATE# to control USB power	
	10		For support 2GB DIMMs	7 13, 14	BJ29 pin and BE24 pin (NB)connect to DDR DIMMA, B(A14 pin)	
	11		For Crestline sightings requires	7	add a 0ohm R1759 on pin N20(NB).	
<2006.06.14>	1		Modify PWROK circuits for All power source check	35	Change R1732 pin2's voltage from 3VM to 3VM_LAN	

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For DB2

	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.06.19>	1		Add Intel RSMRST circuit	31	Add R1749, R1750, R1751 and Q131, D68	0.4
	2		Change resister value meet G-vendor suggestion	25	change R1359, R1362 VALUE	0.4
	3		Kill switch design change	22	change R1736 pin2 contact to +RTCVCC	0.4
<2006.06.20>	1		Change PWR_OK circuit	35	delete R157 and PGD_IN net	0.4
	2		Reserve resister on HDA _RST#_MDC	32	Reserve R1753 0 ohm	0.4
	3		delete two components on Debug part 21	30	delete R1740, R1741	0.4
	4		Control Audio volume when boot	28	add EAPD link to KBC GPIO31	0.4
	5		Add new feature -->Robson	25	Add and change JP13 pin assignment for Robson	
	6		Fix LAN power circuit to IVRD	23	Delete R1 (0.68ohm), R1624, and install R1734	
	7		improve LAN Power ripple	23	Add C1364, C1363 on +3V_LAN and +1.8VM_LAN	
	8		improve DVI issue	16	Add SDVO_CLK/Data net name to NB SDVO_CLK/ Data pins	
<2006.06.21>	1		Change USB control signal	28	Change control signal name to S4_STATE and add Q132	
	2		Isolate power noise for NB	10	change R1453, R1456 from Resister to bead	
<2006.06.22>	1		Hold RESET to modem	32	Install R1753	
	2		Enable WLAN for AMT	25	Install R194, R195 and R197	
	3		Improve TV-out signals and fix TV garbage issue	10	change R175, R176, R177 from150 ohm to 75 ohm	
	4		follow Intel Demo circuit for XDP	28	Change pull up R1589 value for XDP_DBRESET# from 10K to 1K	
<2006.06.23>	1		Chnage Fan Connector pins' count	4	Chnage JP8 from 4pins to 3 pins.	
	2		delete MDC disable reserve part	32	delete U43B	
	3		Implement STB_LED# driver	31	add U43B	
	4		Modify power OK circuit	35	add Q134, Q133, R39, C2 Delete R286, R127, C30, R117, R35, R34, R118, U79	
	5		For Non-link part (INV_PWM from KBC to LCD)	17	delete R131	
	6		Delete Repeated function circuit	11	Delete D21,R520	
<2006.07.18>	1		For C-status	20	Install R179	0.5
	2		For discharge issue	34	Change discharge circuit net from PM_SLP_M# to LAN_WOL_EN#	0.5
	3		HP request	31	Install R155,R156 and un-install R127,R157	0.5
<2006.07.31>	1		Do not support wake on WWAN card	25	Install R1383 and no install R1382	0.5
<2006.08.09>	1		Add anti-pop circuit	26	Add anti-pop circuit	0.5
	2		Eliminate glitch	20	Add R1767, no install R434, C1365, R1757	0.5

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
	3		HP request	32	Connect JP18 pin1 to +3VL, pin2 to +3VS	0.5
	4		EMI request	24	Add D72 and D73 for EMI request	0.5
	5		Add MAX9511	9,16,33	Add MAX9511	0.5
<2006.08.11>	1		For OTS 214499	31	Add U82	0.5
	2		HP request	25	No install R1418,R1358,R1359,R1360	0.5
	3		HP request	25	JP44 PIN37,43 connected to GND JP44 PIN39,41 connected to +3VS	0.5
	4		HP request	25	Isolate SLOT power from SYSTEM power.	0.5
	5		HP request	25	Remove 1.5V from WWAN slot	0.5
	6		HP request	25	Install schottkey diode D74	0.5
	7		SIM I/O pull-up footprint is requested.	25	Add R1780 and no install	0.5
<2006.08.21>	1		HP request	25	change +3VS to +3VS_WLAN ,Change +3VS on R1383.2 to +3VS_WWAN Change +3VS on R1071.1 and R1703.1 to +3VS_WWAN	0.5
	2		HP request	9	Changes for MAX9511	0.5
	3		HP request	25	Remove SW1,C986,R521,D65,R200	0.5
	4		HP request	30	Need to connect SPI_HOLD#_0 and SPI_HOLD#_1 together.	0.5
	5		HP request	31	Item 191,192,193	0.5
	6		HP request	25	Install R1363 and NO INSTALL R1364	0.5
<2006.08.23>	1		HP request	19	Move D75 to SB and delete R1782	0.5
	2		HP request	25	Add 1394 signals on M/B	0.5
<2006.08.25>	1		HP request	25	Add a 0 ohm 0805 on 1.5VS to WLAN mini card connector	0.5
	2			20	Swap GPIO01 and GPIO11 connections.	0.5
<2006.08.29>	1		OTS issue	32	Change JP18 pin8 to WL_BLUE_LED#	0.5
<2006.08.30>	1			16	Change R142, R144 to 3.9K ohm	0.5

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
	3		Intel update	7	Add R1786,R1787,R1788,R1789	0.5
<2006.09.01>	1		HP request	32	Remove R23 and NPCI_RST# connection Remove PLT_RST# connection to R21.2 and connect GPIO28 from ICH8	0.5
<2006.09.04>	1		EMI request	28	Add R1790,R1791,R1792	0.5
<2006.09.06>	1		HP request	23	Change C1257 and C1359 to 10uF 0805	0.5
	2		HP request	25	Remove R1412,1413,1414,1415,1416,1417	0.5
	3		HP request	25	Remove R1418,1358,1353,1360	0.5
	4		HP request	30	Add 0 ohm for SPI, R1793,1794,1795	0.5
<2006.10.13>	1		HP request (MAX9511 issue)	9,16,33	Remove MAX9511 from CRT circuit	0.6
	2			11,21,31	No install BGA crack circuit	0.6
	3			32	Change KB connector	0.6
<2006.10.31>	1			31	Change RSMRST circuit, add R1796	0.6
<2006.11.01>	1		Auto power on issue	20	Auto power on issue(add Q140, R1797)	0.6
	2		1394 issue	28	Modify EMI request	0.6
<2006.11.03>	1		HP request	32	Connect JP32 pin2 to +3VS	0.6
<2006.11.07>	1		HP request	31	Install R1784, no install R1783	0.6
	2		Intel document	10	Change R1471 to 100 ohm	0.6
<2006.11.09>	1		Layout space	22	Remove kensinton circuit	0.6
<2006.11.11>	1		HP request	15	Add CLRP4 and CLRP5 for FSB 667/800 select	0.6
<2006.11.13>	1		HP request	35	Tie R1732.2 to 3VM instead of 3VM_LAN	0.6
	2		HP request	24	Change R1639 to 1.4K based on Intel WW44	0.6
	3		HP request	4	Add resistors in series with the diode signals going to ADM1032.	0.6
	4		HP request	31	Eliminate glitch circuit, install R1483 and no install R1484	0.6

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.11.16>	1		HP request	10	Change R1468, R1472, R1473 to bead	0.6
	2		HP request	24	Change R1639 to 1.87K ohm	0.6
	3		HP request	27	Change R261 and R253 to 56.2 ohms 1%.	0.6
<2006.11.28>	1		HP request	23	Install Q102,R1730, no install R1612,Q104,Q105.	0.6
	2		HP request	7	Install R1739	0.6
<2006.12.19>	1		HP request	35	Add Schmitt Trigger to eliminate glitch	0.7
	2		HP request	31	Install R1646,C75	0.7
	3		HP request	19	Update GPIO33 circuit	0.7
<2006.12.26>	1		HP request	7	Add C and no install	0.7
	2		Chrontel request	16	Add C for DVI I2C	0.7
<2007.01.02>	1		ME request	25	Change JP50 for rewrok	0.7
<2007.01.04>	1		Intel request	23	Add R1804	0.7
	2		ME request	32	Change JP20 to FFC connector	0.7
<2007.01.08>	1		EMI request	33	Add R1805,R1806 0 ohm, reserve C1372, C1373	0.7
<2007.01.10>	1		HP request	31	R1783 connected to +3VL	0.7
<2007.01.13>	1		Compal request	35	Change LMV331 to LM393, delete R124 and C27	0.7
<2007.01.15>	1		HP request	26	R370, R369 - change from 4.7k to 6.04k R374, R375 - change from 4.7k to 2.00k	0.7
<2007.01.16>	1		HP request	25	Connected R1780.2 to UIM_PWR	0.7
<2007.01.17>	1		HP request	30	Add pad for BIOS debug	0.7
<2007.01.19>	1		HP request	34	Add R1807 and no stuff	0.7
	2		CRT wavy issue	10	Add C1374 for CRT wavy issue	0.7
<2007.02.09>	1		CRT wavy issue	17	Add 10uFX2 for CRT wavy issue(C586, C1376)	0.9

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.02.09>	2		HP request	30	Add Q142 for FPR	0.9
<2007.02.16>	1		+3VM_LAN leakage	20	Add U83 for auto boot and leakage issue	0.9
	2		Compal request	15	Delete CLPR4, CLRP5	0.9
	3		HP request	34	Install R1807 and non install R630	0.9
	4		LVDS sequence issue	17	Change C28 to 0.1uF	0.9
	5		HP request	31	Add R1809 to GND	0.9
<2007.02.26>	1		Safety request	33	Change RJ11 connector	0.9
<2007.02.27>	1		HP request	27	Change R261 and R253 to 60.4 ohm	0.9
	2		HP request	35	Move R1803	0.9
<2007.02.28>	1		HP request	11,21	Change to +3VL	0.9
<2007.03.01>	1		HP request	10	CRT wavy issue -- add C1374	0.9
	2		HP request	15	Add CAP for WWAN issue	0.9

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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