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SI2

2009/09/10 REV :SI2-01

<Core Design>

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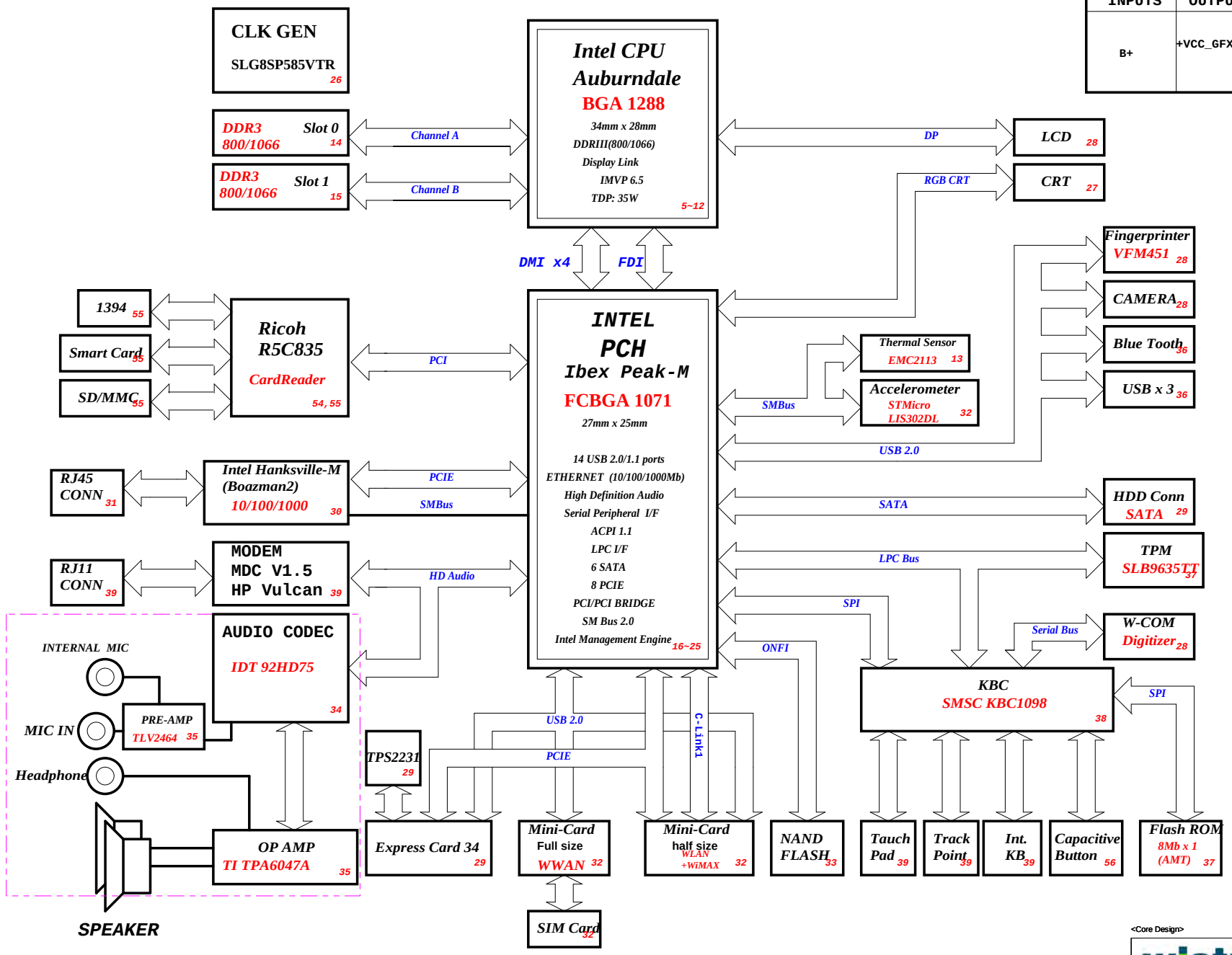
Title: *NORN 3.0*

Size	Document Number	Rev
A3	NORN 3.0	SE

Date: Thursday, September 10, 2009 Sheet 1 of 57

Norn3.0 BLOCK DIAGRAM



VGA
TPS51611

INPUTS	OUTPUTS
B+	+VCC_GFXCORE 15A 53

SYSTEM DC/DC
TPS51125

INPUTS	OUTPUTS
B+	+5VALW 5.5A +3VALW 6.5A 47

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
B+	+1.5V 9.5A +1.05VM_LAN 9A +VCCP 18A 48, 49

CHARGER
BQ24740

INPUTS	OUTPUTS
	BATT
BATT_A	18V 3.0A
BATT_B	5V 100mA 45

CPU DC/DC
TPS51621

INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 35A 50, 51

PCB LAYER

L1: Signal 1
L2: GND/VCC
L3: Signal 2
L4: GND/VCC
L5: Signal 3
L6: Signal 4
L7: VCC/GND
L8: Signal 5
L9: GND/VCC
L10: Signal 6

DOCK
CRT LINE IN LINE OUT USB*3 Ethernet ODD DP eSATA 40

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Title: Block Diagram
Size: Custom | Document Number: NORN 3.0 | Rev: SE
Date: Monday, August 17, 2009 | Sheet 2 of 57

Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+3VL VL	+3VALW +5VALW	+1.5V +0.75VS	+5VS +3VS +1.8VS +1.5VS +VCCP +1.05VS +VCC_CORE +VCC_GFXCORE	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	X	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	~~Floppy Disk~~
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up1 (Right Side)
1	Walk-up2 (Right Side)
2	Walk-up3 (Left Side)
3	Free
4	EXPRESS SLOT
5	Free
6	WLAN
7	Free
8	Bluetooth
9	WWAN
10	Fingerprint
11	Dock1 (HUB)
12	Webcam
13	Dock2 (IDE)

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Title: *Notes List*

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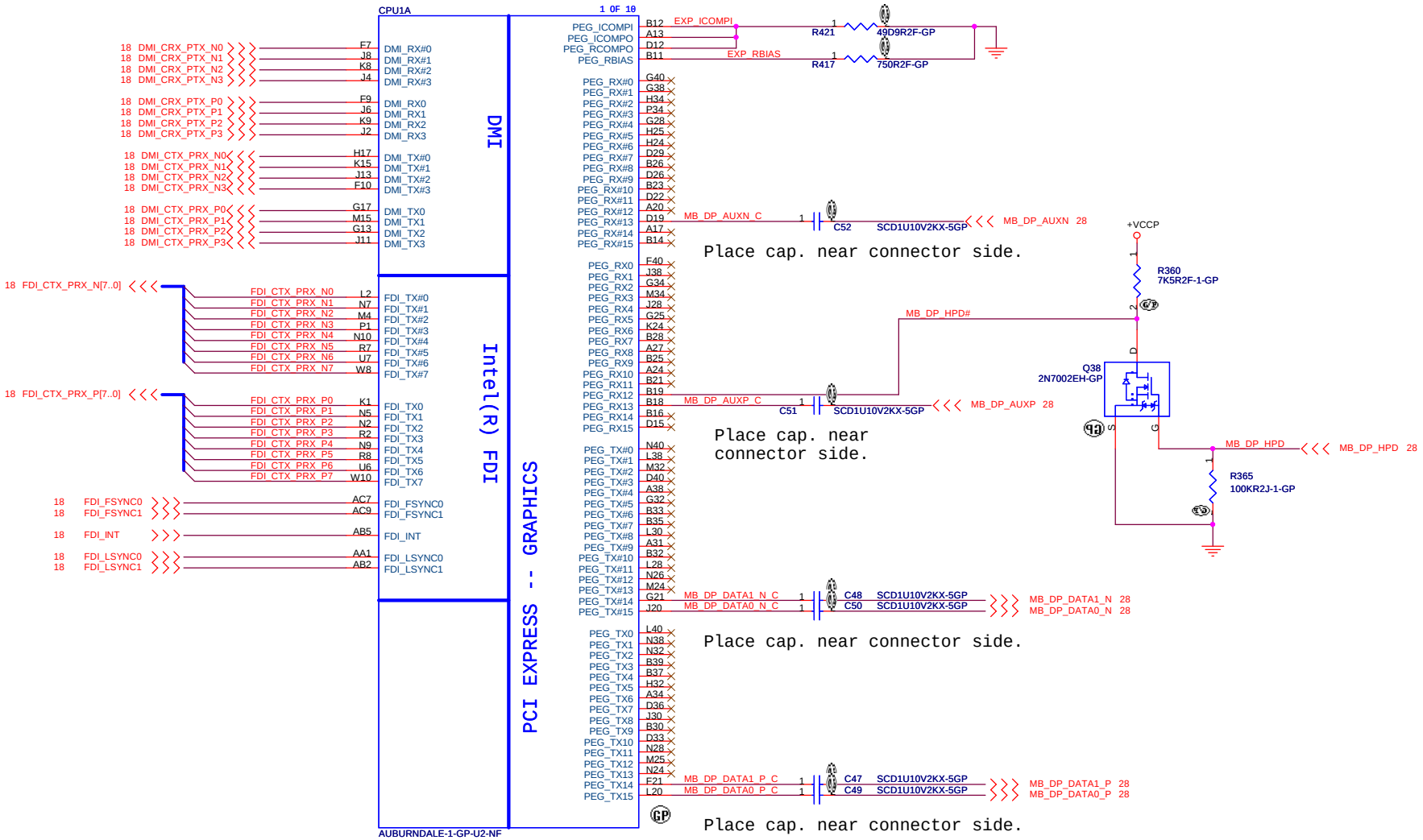
Date: Monday, August 17, 2009 | Sheet 4 of 57

trace lenth <0.5"



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Title: Auburndale(1/8)-DMI+PEG+FDI

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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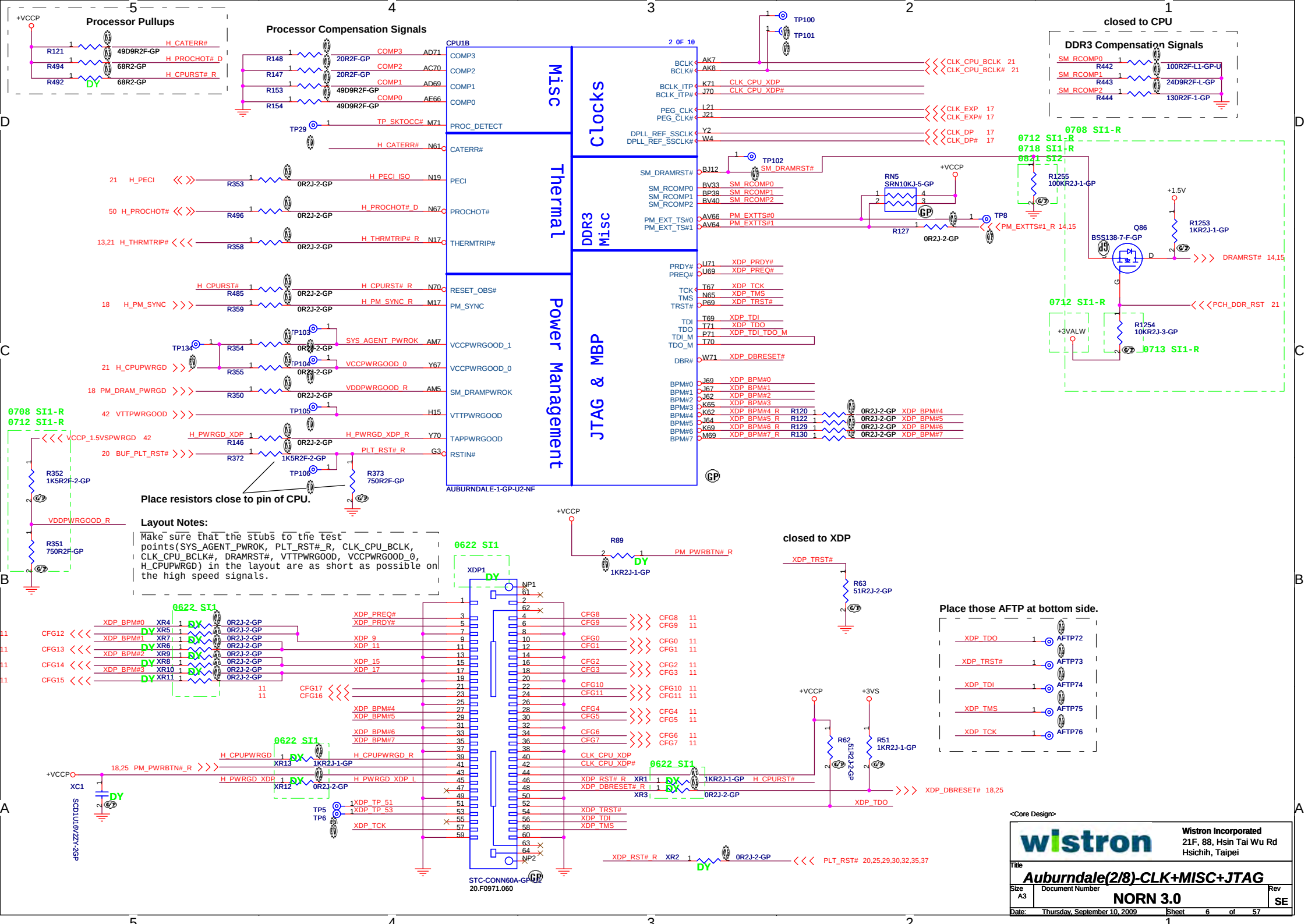
Processor Pullups
Processor Compensation Signals
CPU1B
Misc
Clocks
Thermal
DDR3 Misc
Power Management
JTAG & MBP
AUBURNDALE-1-GP-U2-NF
closed to CPU
DDR3 Compensation Signals
closed to XDP
Place resistors close to pin of CPU.
Layout Notes:
Make sure that the stubs to the test points(SYS_AGENT_PWROK, PLT_RST#_R, CLK_CPU_BCLK, CLK_CPU_BCLK#, DRAMRST#, VTTPWRGOOD, VCCPWRGOOD_0, H_CPUPWRGD) in the layout are as short as possible on the high speed signals.
Place those AFTP at bottom side.
STC-CONN60A-GP-12
20.F0971.060
SCD1U16V2ZY-2GP
<Core Design>
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Title
Auburndale(2/8)-CLK+MISC+JTAG
Size A3
Document Number
NORN 3.0
Rev SE
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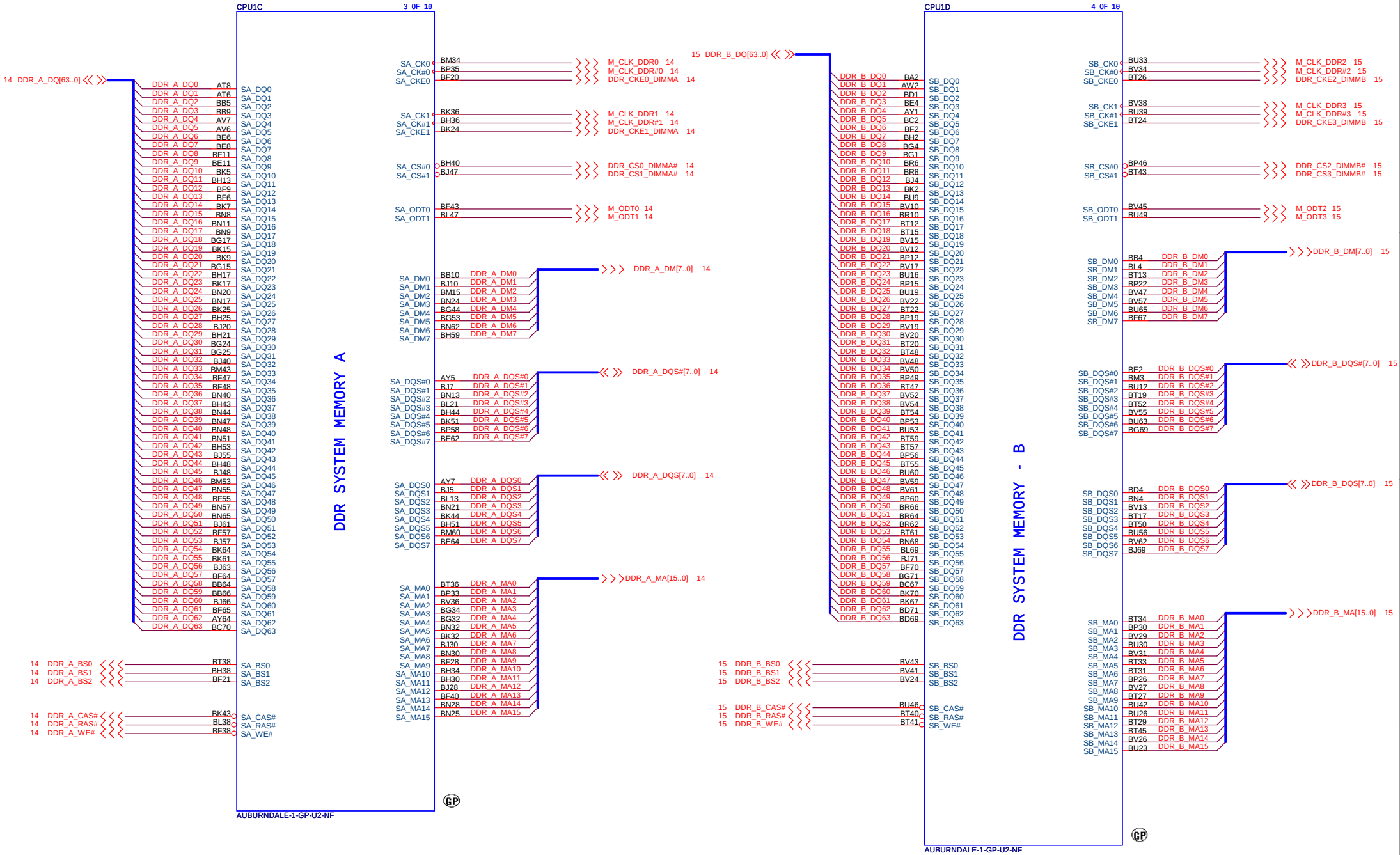

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Title: *Auburndale(3/8)-DDR3*

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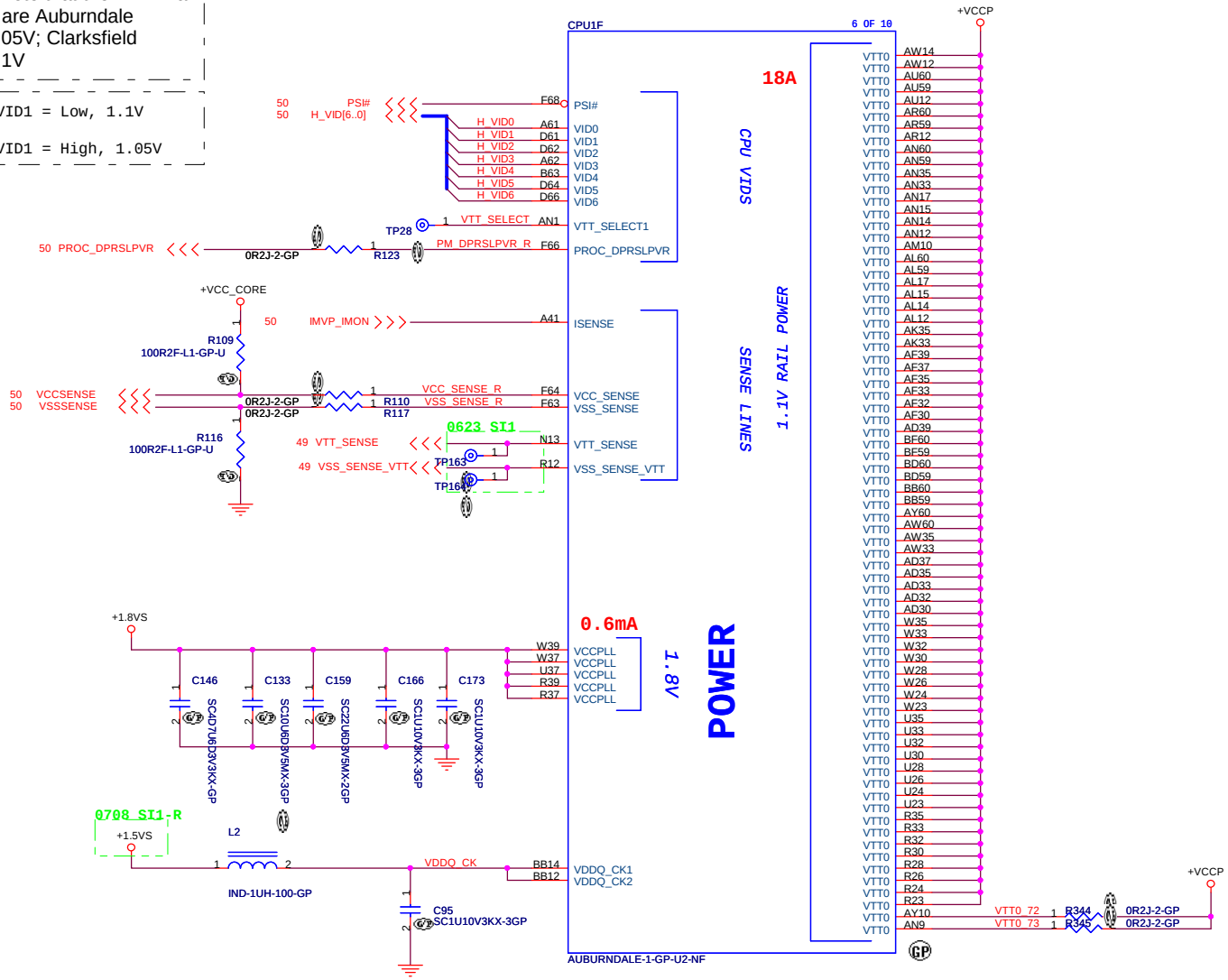
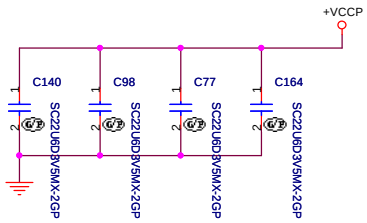
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V





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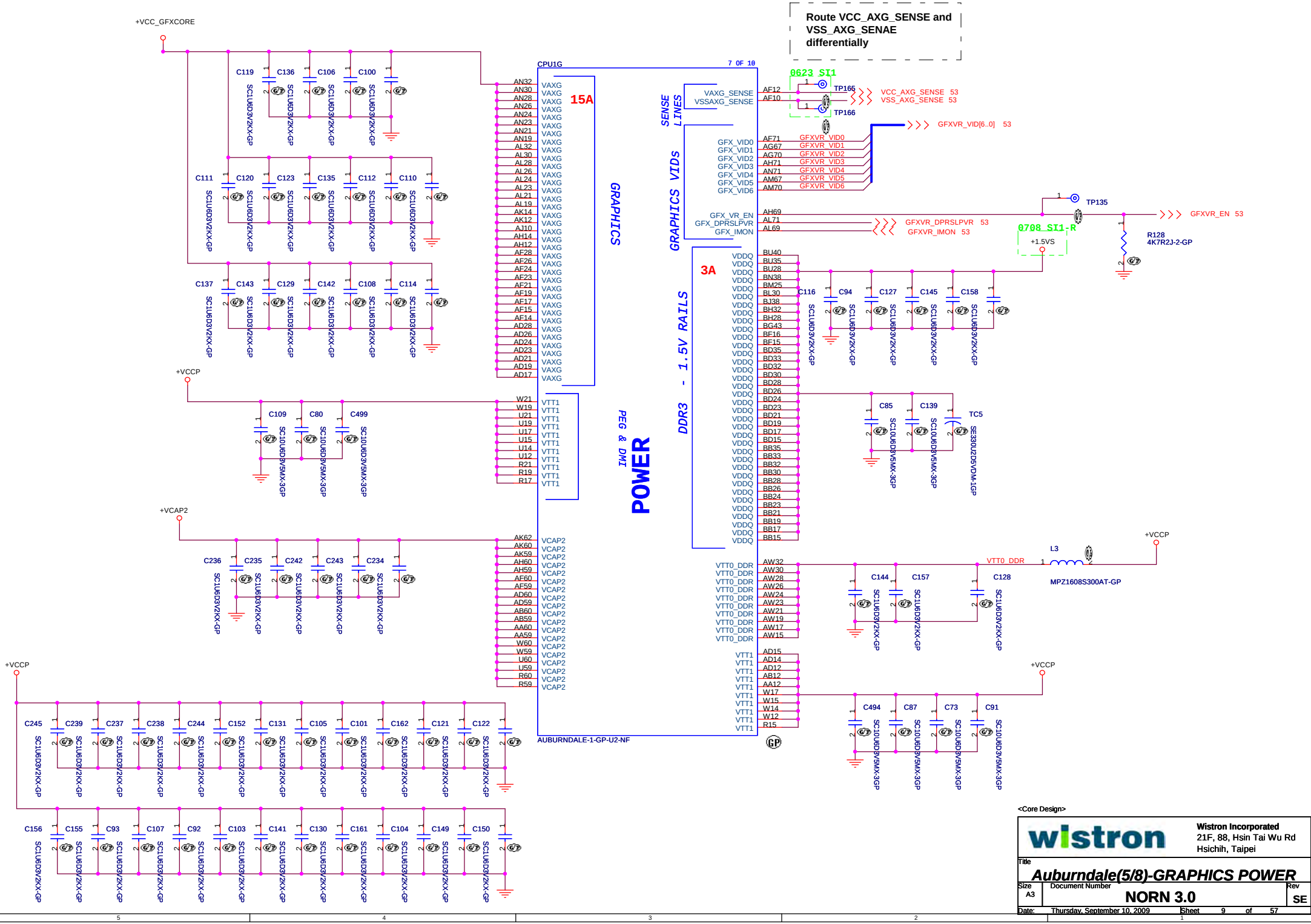
Title: Auburndale(4/8)-POWER

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 8 of 57


Route VCC_AXG_SENSE and VSS_AXG_SENAE differentially
+VCC_GFXCORE
CPU1G
7 OF 10
15A
3A
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
PEG & DMI
POWER
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 53
VSS_AXG_SENSE 53
GFXVR_VID[6..0] 53
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFXVR_DPRSLPVR 53
GFXVR_IMON 53
GFXVR_EN 53
0623_SI1
0708_SI1-R
+1.5VS
TP135
TP165
TP166
R128
4K7R2J-2-GP
+VCCP
+VCAP2
+VTT
VTT0_DDR
L3
MPZ1608S300AT-GP
AUBURNDALE-1-GP-U2-NF
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Title
Auburndale(5/8)-GRAPHICS POWER
Size A3
Document Number
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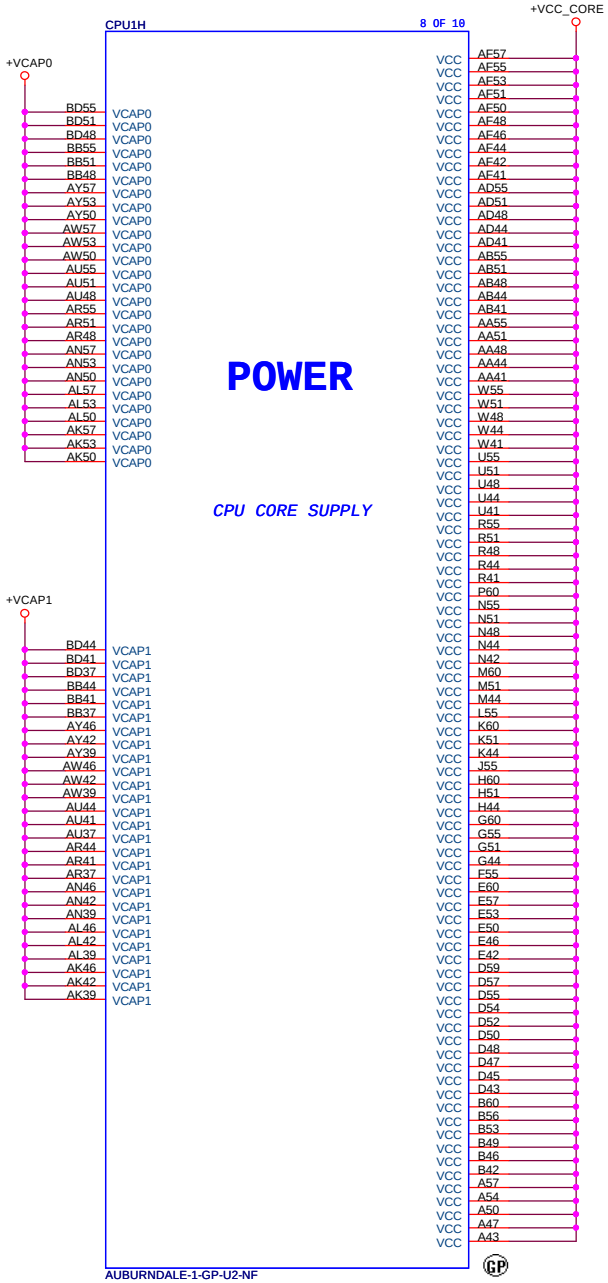
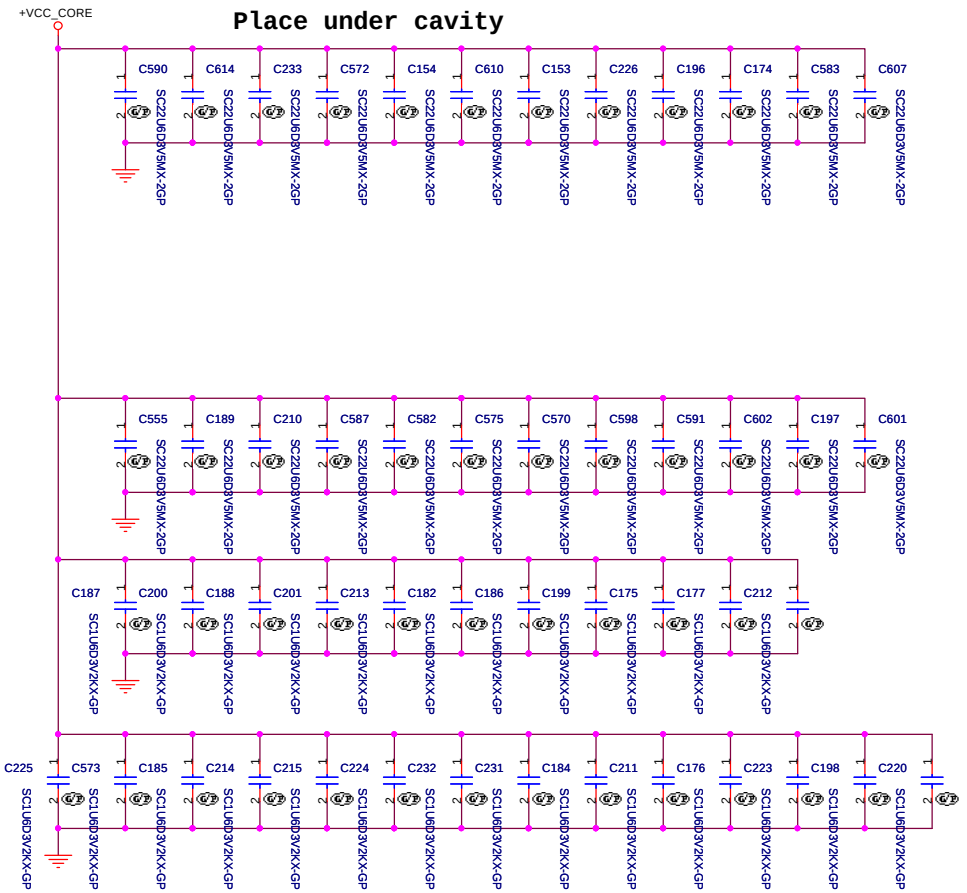
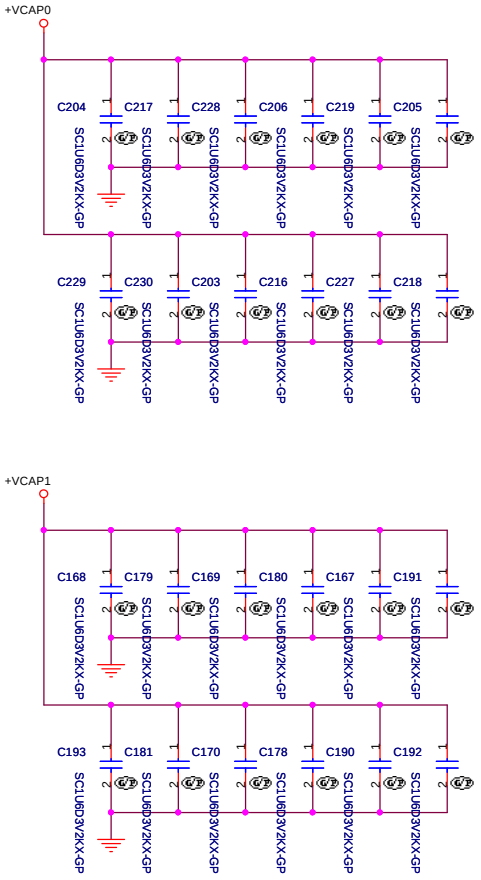

CPU1H
8 OF 10
+VCAP0
+VCAP1
+VCC_CORE
POWER
CPU CORE SUPPLY
AUBURNDALE-1-GP-U2-NF


+VCC_CORE
Place under cavity


+VCAP0
+VCAP1

CFG Straps for Processor

CFG0

DY R346 3K01R2F-3-GP

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3

DY R347 3K01R2F-3-GP

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4

0623 SI1 R348 3K3R2J-3-GP

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Only temporary for early CFD samples (rPGA/BGA)

CFG7

DY R349 3K01R2F-3-GP

BGA Ball Cracking Prevention and Detection

+3VS R118 100KR2J-1-GP — VSS_NCTF2_R — 21,38 CRACK_BGA — U20 — 2N7002EDWH-GP 84.2N702.C3F 2nd = 84.DMN66.03F — R108 100KR2J-1-GP — VSS_NCTF6_R

+3VS R490 100KR2J-1-GP — VSS_NCTF1_R — CRACK_BGA — U88 — 2N7002EDWH-GP 84.2N702.C3F 2nd = 84.DMN66.03F — R504 100KR2J-1-GP — VSS_NCTF7_R

CPU1E 5 OF 10 — AUBURNDALE-1-GP-U2-NF

RESERVED

CFG0 AL4 CFG0; CFG1 AM2 CFG1; CFG2 AK1 CFG2; CFG3 AK2 CFG3; CFG4 AK4 CFG4; CFG5 AJ2 CFG5; CFG6 AT2 CFG6; CFG7 AG7 CFG7; CFG8 AF4 CFG8; CFG9 AG2 CFG9; CFG10 AH1 CFG10; CFG11 AC2 CFG11; CFG12 AC4 CFG12; CFG13 AE2 CFG13; CFG14 AD1 CFG14; CFG15 AF8 CFG15; CFG16 AF6 CFG16; CFG17 AB7 CFG17

TP3 RSVD_TP0 AU1 RSVD_TP0

T4 RSVD#T4; T2 RSVD#T2

R357 DY 0R2J-2-GP RSVD17; R356 DY 0R2J-2-GP RSVD18 — U1 RSVD#U1; V2 RSVD#V2

AV71 RSVD#AV71; AW70 RSVD#AW70

AY69 RSVD#AY69; BB69 RSVD#BB69

D8 RSVD#D8; B7 RSVD#B7

A10 RSVD#A10; B9 RSVD#B9

C5 RSVD_NCTF#C5; A6 RSVD_NCTF#A6

E3 RSVD_NCTF#E3; F1 RSVD_NCTF#F1

NCTF TEST PIN: A5,A68,A69,A71,C3,C71,E1,E71,BR1,BR71, BT1,BT71,BV1,BV3,BV5,BV68,BV69,BV71

W66 RSVD#W66; W64 RSVD#W64 — TP167 TP168

AC69 RSVD#AC69; AC71 RSVD#AC71 — TP169

AA71 RSVD#AA71; AA69 RSVD#AA69 — TP170

R66 RSVD#R66; R64 RSVD#R64

BT5 RSVD_NCTF#BT5; BR5 RSDV_NCTF#BR5 — TP171

BV6 RSDV_NCTF#BV6; BV8 RSDV_NCTF#BV8

AV69 RSVD#AV69; AK71 RSVD#AK71; AN69 RSVD#AN69; AP66 RSVD#AP66; AH66 RSVD#AH66; AK66 RSVD#AK66; AR71 RSVD#AR71; AM66 RSVD#AM66; AK69 RSVD#AK69; AU71 RSVD#AU71; AT70 RSVD#AT70; AR69 RSVD#AR69; AU69 RSVD#AU69; AT67 RSVD#AT67

AP2 RSVD_TP2; AN7 RSVD_TP1 — TP4 TP7

AV4 RSVD#AV4; AU2 RSVD#AU2

BE69 RSVD64; BE71 RSVD65 — R131 DY 0R2J-2-GP; R133 DY 0R2J-2-GP

BV71 DC_TEST#_BV71_69; BV69; BV68 DC_TEST#_BV68 — R491 0R2J-2-GP; BV5 DC_TEST#_BV5 — R381 0R2J-2-GP; BV3 DC_TEST_BT3_BV3; BV1 DC_TEST#_BV1_BT1; BT71 DC_TEST_BT69_71; BT69; BT3; BT1; BR71 VSS_NCTF2_R; BR1 VSS_NCTF6_R; E71 DC_TEST#_E71 — R493 0R2J-2-GP; E1; C71 DC_TEST#_C71_A71; C69 DC_TEST_C69_A69; C3 DC_TEST#_C3 — R374 0R2J-2-GP; A71; A69; A68 VSS_NCTF1_R; A5 VSS_NCTF7_R

NCTF_DC_TEST#BV71, NCTF_DC_TEST#BV69, NCTF_DC_TEST#BV68, NCTF_DC_TEST#BV5, NCTF_DC_TEST#BV3, NCTF_DC_TEST#BV1, NCTF_DC_TEST#BT71, DC_TEST_BT69, DC_TEST_BT3, NCTF_DC_TEST#BT1, NCTF_DC_TEST#BR71, NCTF_DC_TEST#BR1, NCTF_DC_TEST#E71, NCTF_DC_TEST#E1, NCTF_DC_TEST#C71, DC_TEST_C69, NCTF_DC_TEST#C3, NCTF_DC_TEST#A71, NCTF_DC_TEST#A69, NCTF_DC_TEST#A68, NCTF_DC_TEST#A5

DC_TEST#_C71_A71 — TP31; DC_TEST_BT69_71 — TP30; DC_TEST#_BV5 — TP26; DC_TEST#_C3 — TP27

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Title: Auburndale(7/8)-RESERVED

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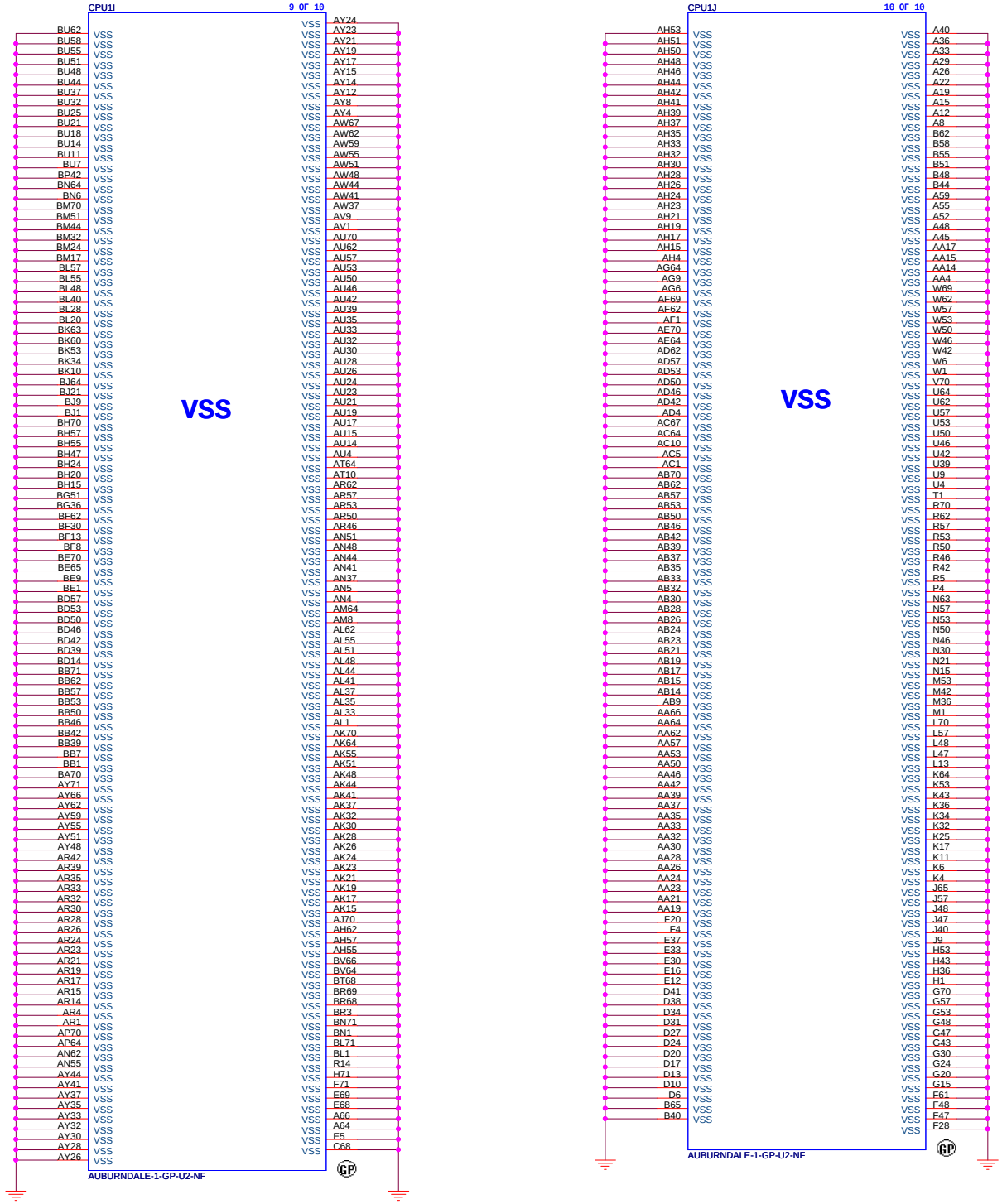

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Title

Auburndale(8/8)-VSS

Size	Document Number	Rev
Custom	NORN 3.0	SE

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CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

H_THERMDA
C290
SC2200P50V2KX-2GP
H_THERMDC

REMOTE2-
Q10
MMBT3904WT1G-1-GP
84.M3904.D11
2nd = 84.03904.Y11
C202
SC2200P50V2KX-2GP
REMOTE2+

AMBIENT TEMP: Q24 used for GPU

REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing. Lacate Cap near thermal diode .

4 WIRE PWM Fan Control circuit

+5VS
D10
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.F1F
DY
C291
SCD1U16V2ZY-2GP
R516
10KR2J-3-GP
FAN1
MLX-CON4-28-GP
20.F1035.004

+3VS
R166
10KR2J-3-GP
6,21 H_THRMTRIP#
R173
0R2J-2-GP
SYS_SHDN#

+3VS
R159
68R2-GP
C289
SCD1U10V2KX-4GP
+3VS_THER
R1219
10KR2J-3-GP

0630 SI1
FAN_PWM-R
FAN_PWM-R 38
C292
SCD1U16V2KX-3GP

FAN_PWM
FAN_TACH
R515
0R2J-2-GP
FAN_PWM_C

RN12
+3VS
SRN10KJ-5-GP

U32
EMC2113-1-AP-TR-GP
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
PWM_IN
ADDR_SEL
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
21 THERM_SCI#
R165
0R2J-2-GP
SYS_SHDN#
THERM_SCI#_R
14,15,17,26,32 SMB_CLK_S3
14,15,17,26,32 SMB_DATA_S3
FAN_PWM-R
ADDR_SEL
FAN_TACH
FAN_PWM
TRIP_SET
R164
2K05R2F-GP
SHDN_SEL

+3VS
R170
15KR2J-1-GP
SHDN_SEL

+5VS
AFTP43
FAN_PWM_C
AFTP39
FAN_TACH
AFTP40
AFTP41

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Title: SMSC2113 Thermal Sensor
Size: A3
Document Number: NORN 3.0
Rev: SE
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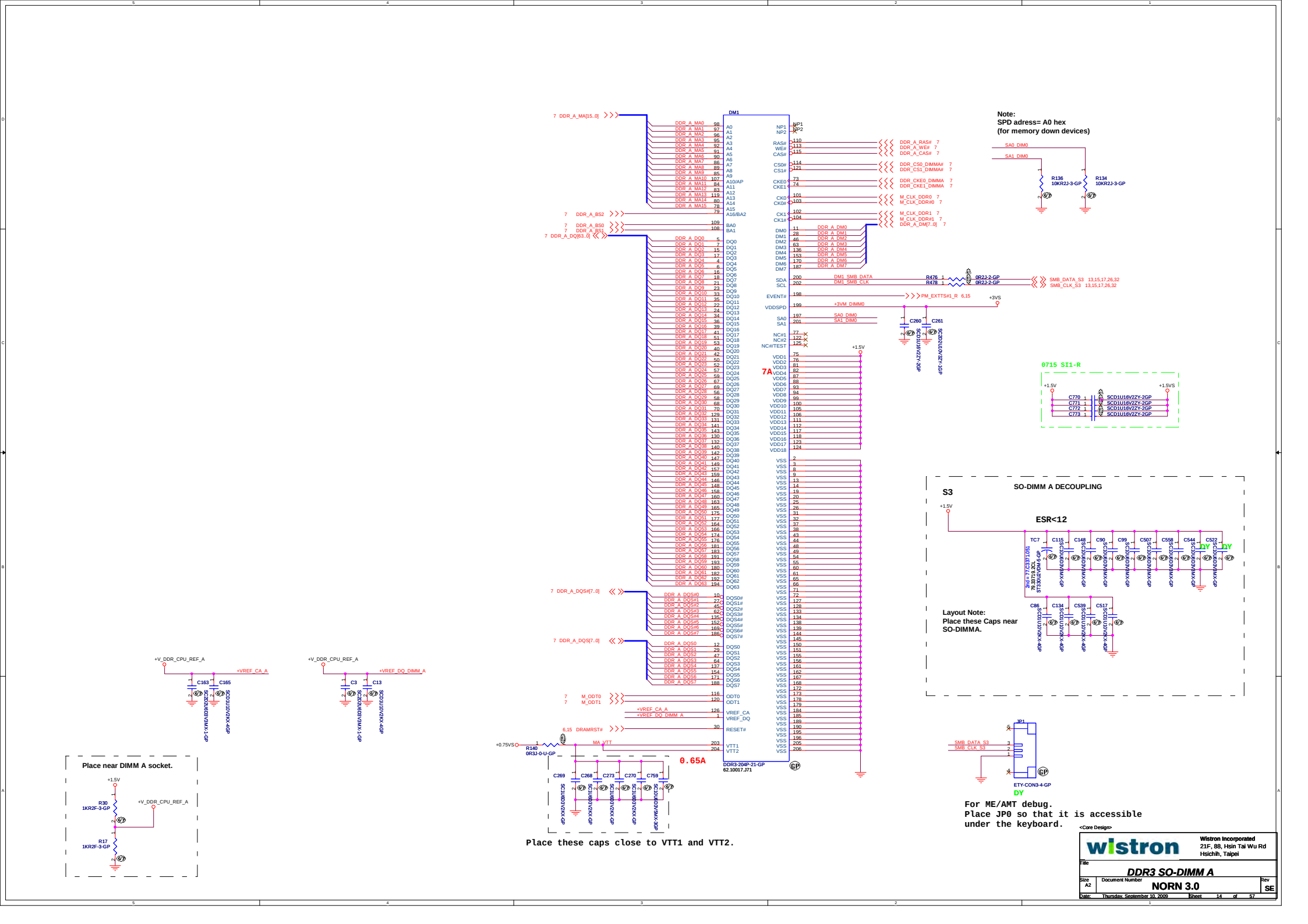
DM1
Note:
SPD adress= A0 hex
(for memory down devices)
SA0_DIM0
SA1_DIM0
R136 10KR2J-3-GP
R134 10KR2J-3-GP
0715 SI1-R
SO-DIMM A DECOUPLING
S3
ESR<12
Layout Note:
Place these Caps near
SO-DIMMA.
Place near DIMM A socket.
R30 1KR2F-3-GP
R17 1KR2F-3-GP
+V_DDR_CPU_REF_A
+VREF_CA_A
+VREF_DQ_DIMM_A
R140 0R3J-0-U-GP
0.65A
Place these caps close to VTT1 and VTT2.
DDR3-204P-21-GP
62.10017.J71
JP1
ETY-CON3-4-GP
DY
For ME/AMT debug.
Place JP0 so that it is accessible
under the keyboard.
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Hsichih, Taipei
DDR3 SO-DIMM A
NORN 3.0
Size A2
Rev SE
Date: Thursday, September 10, 2009
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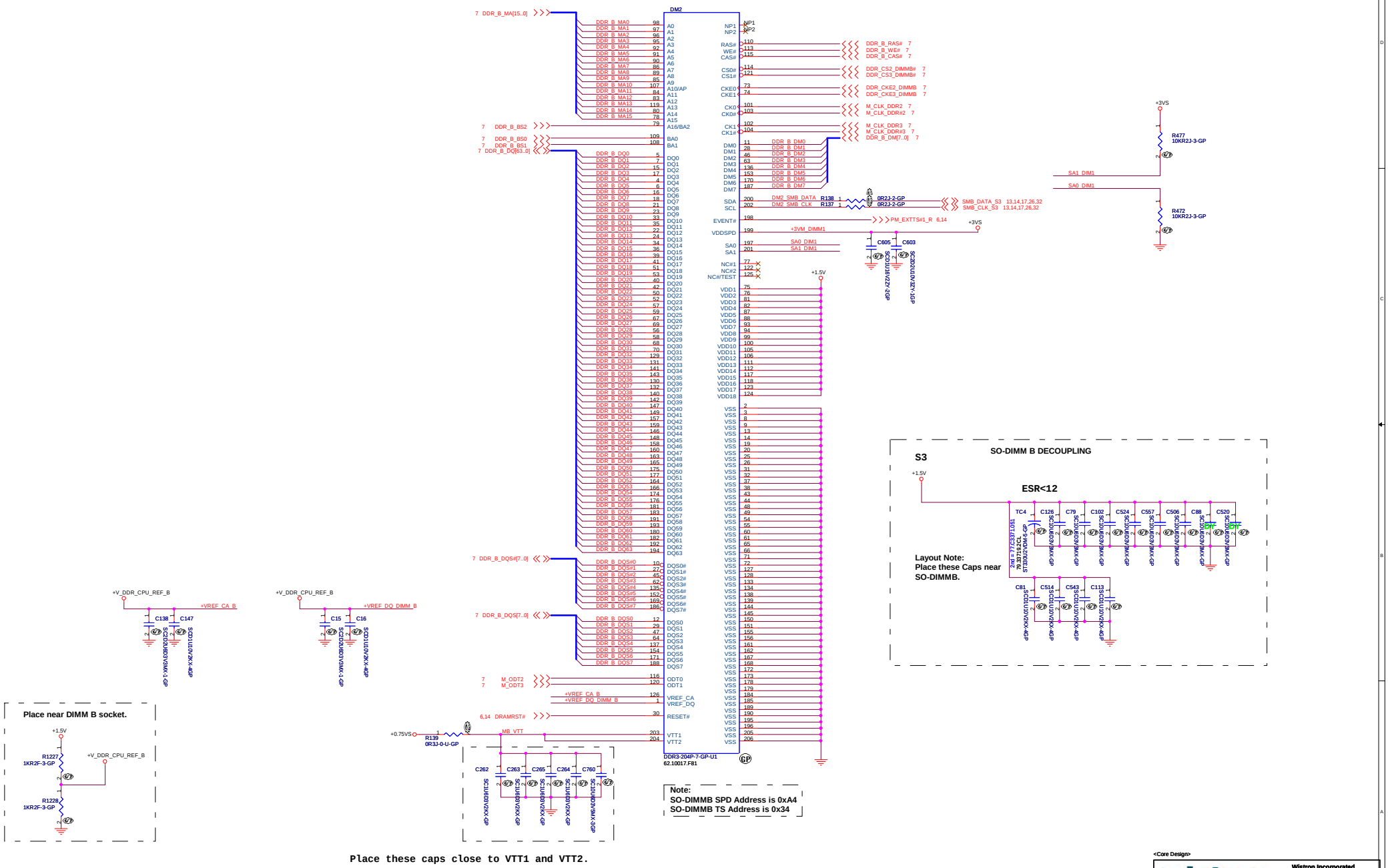

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Hsichih, Taipei

Title: DDR3 SO-DIMM B

Size: A2 | Document Number: NORN 3.0 | Rev: SE

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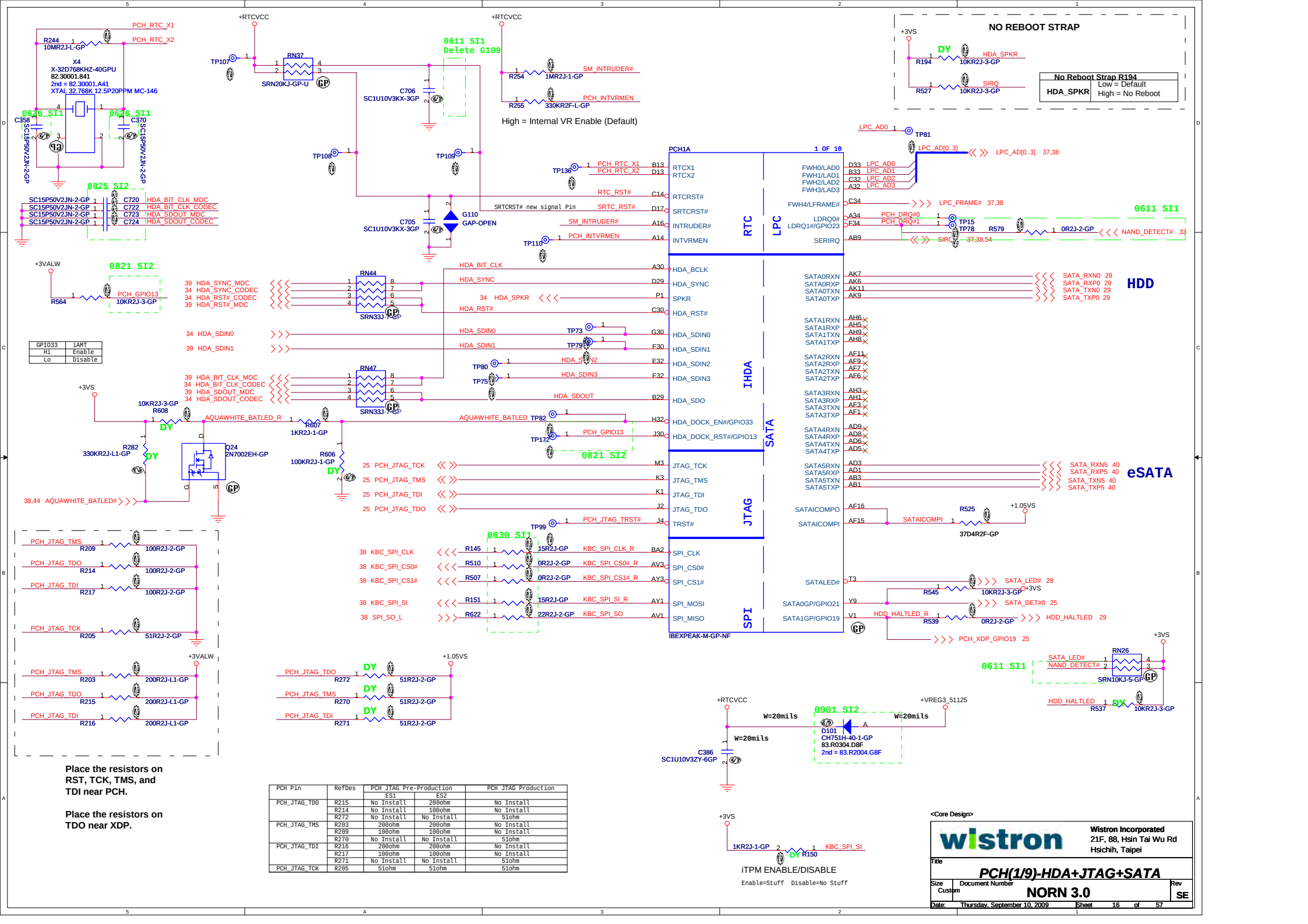
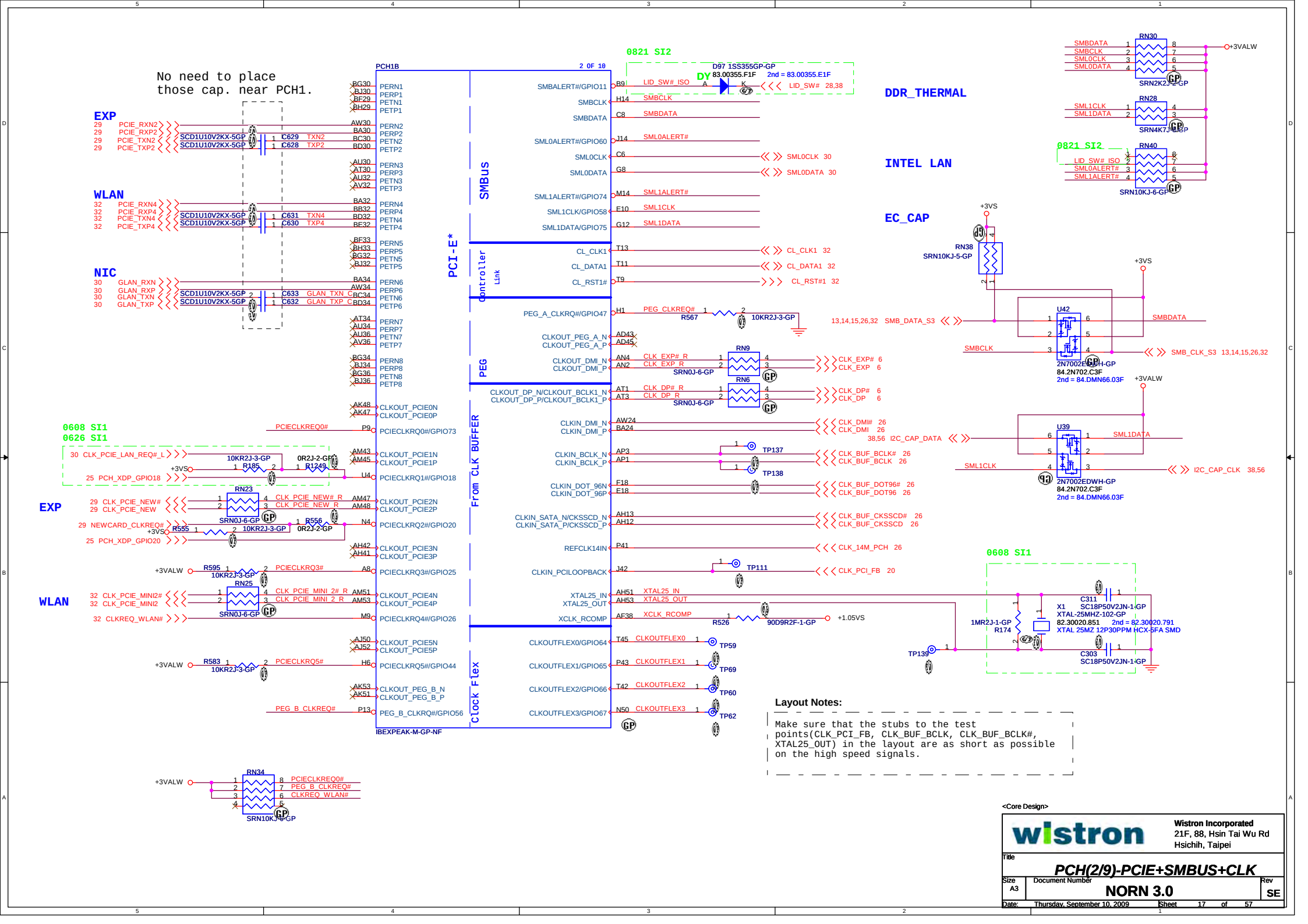


PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	
PCH_JTAG_TDO	R215	No Install	200ohm	No Install
	R214	No Install	100ohm	No Install
	R272	No Install	No Install	51ohm
PCH_JTAG_TMS	R203	200ohm	200ohm	No Install
	R209	100ohm	100ohm	No Install
	R270	No Install	No Install	51ohm
PCH_JTAG_TDI	R216	200ohm	200ohm	No Install
	R217	100ohm	100ohm	No Install
	R271	No Install	No Install	51ohm
PCH_JTAG_TCK	R205	51ohm	51ohm	51ohm


No need to place those cap. near PCH1.
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
0821 SI2
DDR_THERMAL
INTEL LAN
EC_CAP
EXP
WLAN
NIC
0608 SI1
0626 SI1
SRN2K2J-2-GP
SRN4K7J-4-GP
SRN10KJ-6-GP
SRN10KJ-5-GP
2N7002EDWH-GP
84.2N702.C3F
2nd = 84.DMN66.03F
IBEXPEAK-M-GP-NF
Layout Notes:
Make sure that the stubs to the test points(CLK_PCI_FB, CLK_BUF_BCLK, CLK_BUF_BCLK#, XTAL25_OUT) in the layout are as short as possible on the high speed signals.
<Core Design>
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Title
PCH(2/9)-PCIE+SMBUS+CLK
Size A3
Document Number
NORN 3.0
Rev SE
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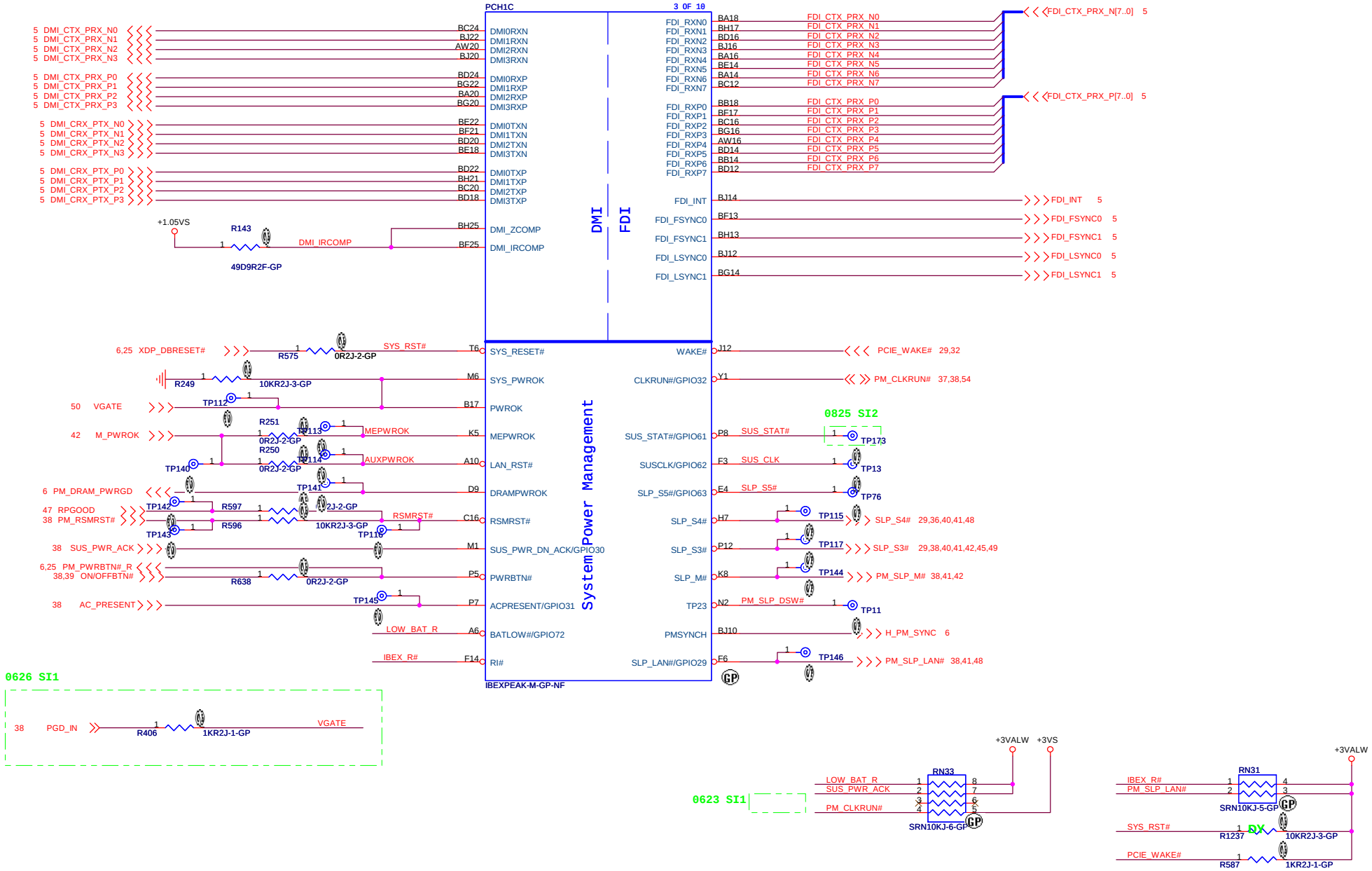

Title

PCH(3/9)-DMI+FDI+GPIO

Size	Document Number	Rev
A3	NORN 3.0	SE

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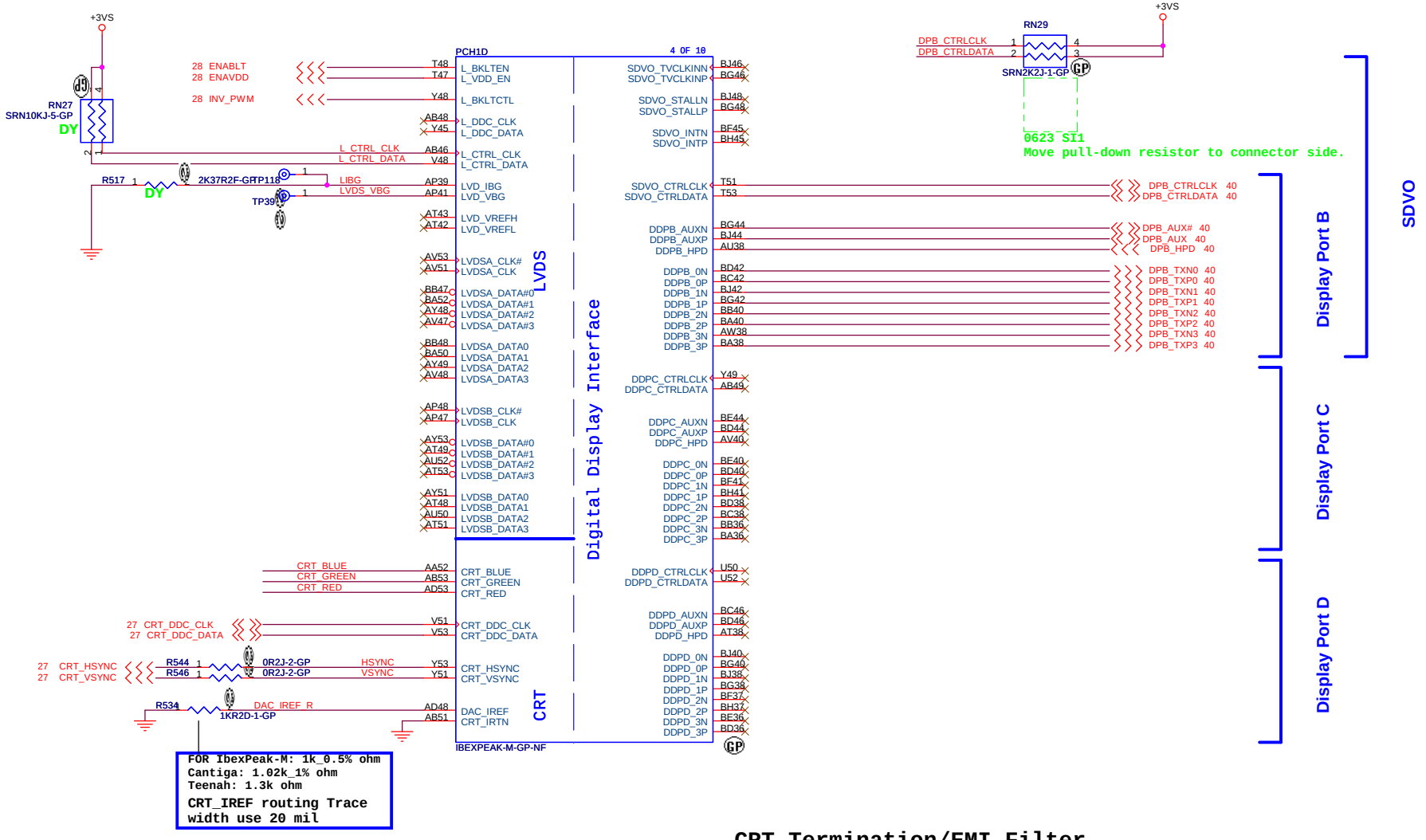
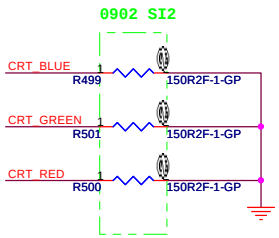
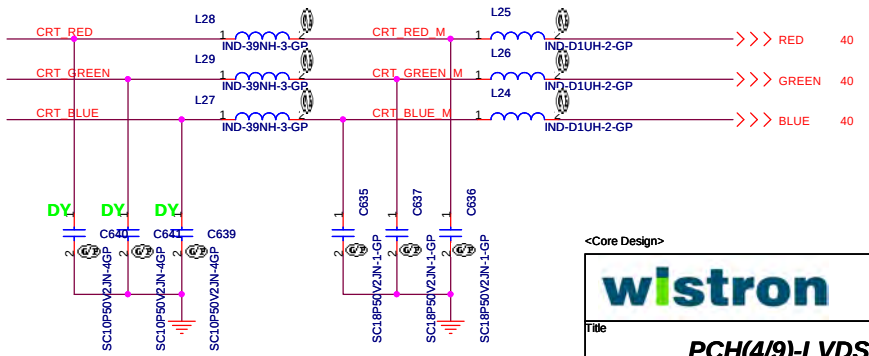


Place Close IbexPeak-M



CRT Termination/EMI Filter
T-Filter network should be placed near IbexPeak-M.



<Core Design>

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Title: PCH(4/9)-LVDS+DDI

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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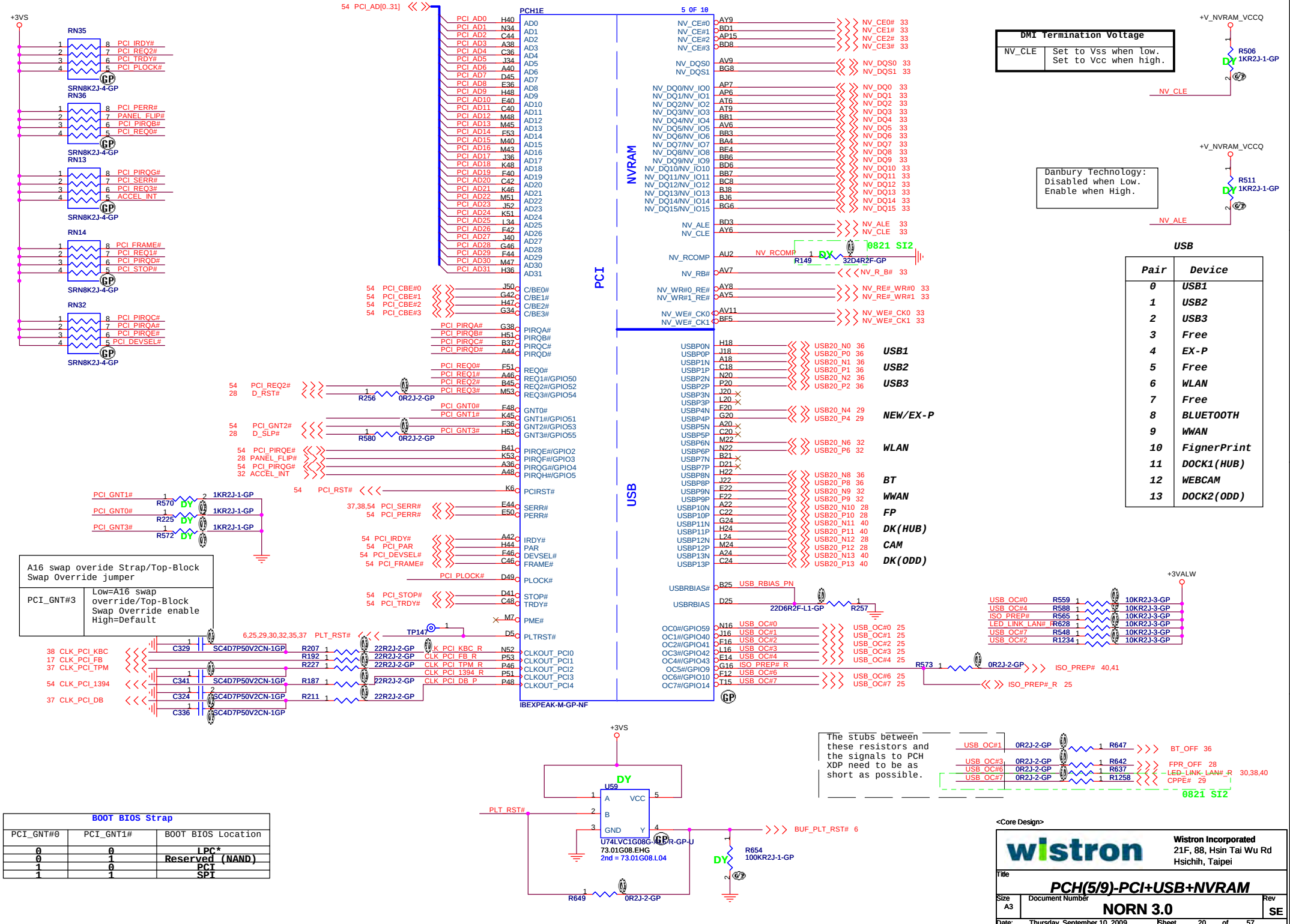
PCH1E
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
5 OF 10
RN35
SRN8K2J-4-GP
PCI_IRDY#
PCI_REQ2#
PCI_TRDY#
PCI_PLOCK#
RN36
PCI_PERR#
PANEL_FLIP#
PCI_PIRQB#
PCI_REQ0#
RN13
PCI_PIRQG#
PCI_SERR#
PCI_REQ3#
ACCEL_INT
RN14
PCI_FRAME#
PCI_REQ1#
PCI_PIRQD#
PCI_STOP#
RN32
PCI_PIRQC#
PCI_PIRQA#
PCI_PIRQE#
PCI_DEVSEL#
54 PCI_AD[0..31]
PCI_AD0 H40
PCI_AD1 N34
PCI_AD2 C44
PCI_AD3 A38
PCI_AD4 C36
PCI_AD5 J34
PCI_AD6 A40
PCI_AD7 D45
PCI_AD8 E36
PCI_AD9 H48
PCI_AD10 E40
PCI_AD11 C40
PCI_AD12 M48
PCI_AD13 M45
PCI_AD14 F53
PCI_AD15 M40
PCI_AD16 M43
PCI_AD17 J36
PCI_AD18 K48
PCI_AD19 F40
PCI_AD20 C42
PCI_AD21 K46
PCI_AD22 M51
PCI_AD23 J52
PCI_AD24 K51
PCI_AD25 L34
PCI_AD26 F42
PCI_AD27 J40
PCI_AD28 G46
PCI_AD29 F44
PCI_AD30 M47
PCI_AD31 H36
54 PCI_CBE#0 J50
54 PCI_CBE#1 G42
54 PCI_CBE#2 H47
54 PCI_CBE#3 G34
PCI_PIRQA# G38
PCI_PIRQB# H51
PCI_PIRQC# B37
PCI_PIRQD# A44
PCI_REQ0# F51
PCI_REQ1# A46
PCI_REQ2# B45
PCI_REQ3# M53
54 PCI_REQ2?
28 D_RST#
R256 0R2J-2-GP
PCI_GNT0# F48
PCI_GNT1# K45
54 PCI_GNT2#
28 D_SLP#
PCI_GNT3# F36
R580 0R2J-2-GP
54 PCI_PIRQE# B41
28 PANEL_FLIP# K53
54 PCI_PIRQG# A36
32 ACCEL_INT A48
54 PCI_RST# K6
37,38,54 PCI_SERR# E44
54 PCI_PERR# E50
54 PCI_IRDY# A42
54 PCI_PAR H44
54 PCI_DEVSEL# F46
54 PCI_FRAME# C46
PCI_PLOCK# D49
54 PCI_STOP# D41
54 PCI_TRDY# C48
PME# M7
6,25,29,30,32,35,37 PLT_RST#
TP147
D5
PCI_GNT1# R570 DY 1KR2J-1-GP
PCI_GNT0# R225 DY 1KR2J-1-GP
PCI_GNT3# R572 DY 1KR2J-1-GP
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT#3 Low=A16 swap override/Top-Block Swap Override enable High=Default
38 CLK_PCI_KBC C329 SC4D7P50V2CN-1GP R207 22R2J-2-GP CLK_PCI_KBC_R N52
17 CLK_PCI_FB R192 22R2J-2-GP CLK_PCI_FB_R P53
37 CLK_PCI_TPM R227 22R2J-2-GP CLK_PCI_TPM_R P46
54 CLK_PCI_1394 C341 SC4D7P50V2CN-1GP R187 22R2J-2-GP CLK_PCI_1394_R P51
37 CLK_PCI_DB C324 SC4D7P50V2CN-1GP R211 22R2J-2-GP CLK_PCI_DB_P P48
C336 SC4D7P50V2CN-1GP
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
NV_CE#0 AY9
NV_CE#1 BD1
NV_CE#2 AP15
NV_CE#3 BD8
NV_CE0# 33
NV_CE1# 33
NV_CE2# 33
NV_CE3# 33
NV_DQS0 AY9
NV_DQS1 BG8
NV_DQS0 33
NV_DQS1 33
NV_DQ0/NV_IO0 AP7
NV_DQ1/NV_IO1 AP6
NV_DQ2/NV_IO2 AT6
NV_DQ3/NV_IO3 AT9
NV_DQ4/NV_IO4 BB1
NV_DQ5/NV_IO5 AV6
NV_DQ6/NV_IO6 BR3
NV_DQ7/NV_IO7 BA4
NV_DQ8/NV_IO8 BF4
NV_DQ9/NV_IO9 BB6
NV_DQ10/NV_IO10 BD6
NV_DQ11/NV_IO11 BB7
NV_DQ12/NV_IO12 BC8
NV_DQ13/NV_IO13 BJ8
NV_DQ14/NV_IO14 BJ6
NV_DQ15/NV_IO15 BG6
NV_DQ0 33
NV_DQ1 33
NV_DQ2 33
NV_DQ3 33
NV_DQ4 33
NV_DQ5 33
NV_DQ6 33
NV_DQ7 33
NV_DQ8 33
NV_DQ9 33
NV_DQ10 33
NV_DQ11 33
NV_DQ12 33
NV_DQ13 33
NV_DQ14 33
NV_DQ15 33
NV_ALE BD3
NV_CLE AY6
NV_ALE 33
NV_CLE 33
NV_RCOMP AU2
NV_RCOMP R149 DY 32D4R2F-GP 0821 SI2
NV_RB# AV7
NV_R_B# 33
NV_WR#0_RE# AY8
NV_WR#1_RE# AY5
NV_RE#_WR#0 33
NV_RE#_WR#1 33
NV_WE#_CK0 AV11
NV_WE#_CK1 BF5
NV_WE#_CK0 33
NV_WE#_CK1 33
USBP0N H18
USBP0P J18
USBP1N A18
USBP1P C18
USBP2N N20
USBP2P P20
USBP3N J20
USBP3P L20
USBP4N F20
USBP4P G20
USBP5N A20
USBP5P C20
USBP6N M22
USBP6P N22
USBP7N B21
USBP7P D21
USBP8N H22
USBP8P J22
USBP9N E22
USBP9P F22
USBP10N A22
USBP10P C22
USBP11N G24
USBP11P H24
USBP12N L24
USBP12P M24
USBP13N A24
USBP13P C24
USB20_N0 36
USB20_P0 36
USB20_N1 36
USB20_P1 36
USB20_N2 36
USB20_P2 36
USB20_N4 29
USB20_P4 29
USB20_N6 32
USB20_P6 32
USB20_N8 36
USB20_P8 36
USB20_N9 32
USB20_P9 32
USB20_N10 28
USB20_P10 28
USB20_N11 40
USB20_P11 40
USB20_N12 28
USB20_P12 28
USB20_N13 40
USB20_P13 40
USB1
USB2
USB3
NEW/EX-P
WLAN
BT
WWAN
FP
DK(HUB)
CAM
DK(ODD)
USBRBIAS# B25 USB_RBIAS_PN
USBRBIAS D25
22D6R2F-L1-GP R257
OC0#/GPIO59 N16 USB_OC#0
OC1#/GPIO40 J16 USB_OC#1
OC2#/GPIO41 F16 USB_OC#2
OC3#/GPIO42 L16 USB_OC#3
OC4#/GPIO43 E14 USB_OC#4
OC5#/GPIO9 G16 ISO_PREP#_R
OC6#/GPIO10 F12 USB_OC#6
OC7#/GPIO14 T15 USB_OC#7
USB_OC#0 25
USB_OC#1 25
USB_OC#2 25
USB_OC#3 25
USB_OC#4 25
USB_OC#6 25
USB_OC#7 25
R573 0R2J-2-GP
ISO_PREP# 40,41
ISO_PREP#_R 25
+3VALW
USB_OC#0 R559 10KR2J-3-GP
USB_OC#4 R588 10KR2J-3-GP
ISO_PREP# R565 10KR2J-3-GP
LED_LINK_LAN#_R R628 10KR2J-3-GP
USB_OC#7 R548 10KR2J-3-GP
USB_OC#2 R1234 10KR2J-3-GP
DMI Termination Voltage
NV_CLE Set to Vss when low. Set to Vcc when high.
+V_NVRAM_VCCQ
R506 1KR2J-1-GP DY
NV_CLE
Danbury Technology:
Disabled when Low.
Enable when High.
+V_NVRAM_VCCQ
R511 1KR2J-1-GP DY
NV_ALE
USB
Pair Device
0 USB1
1 USB2
2 USB3
3 Free
4 EX-P
5 Free
6 WLAN
7 Free
8 BLUETOOTH
9 WWAN
10 FignerPrint
11 DOCK1(HUB)
12 WEBCAM
13 DOCK2(ODD)
+3VS
DY
U59
PLT_RST#
U74LVC1G08G-GP-R-GP-U
73.01G08.EHG
2nd = 73.01G08.L04
R649 0R2J-2-GP
R654 100KR2J-1-GP
BUF_PLT_RST# 6
The stubs between these resistors and the signals to PCH XDP need to be as short as possible.
USB_OC#1 0R2J-2-GP R647 BT_OFF 36
USB_OC#3 0R2J-2-GP R642 FPR_OFF 28
USB_OC#6 0R2J-2-GP R637 LED_LINK_LAN#_R 30,38,40
USB_OC#7 0R2J-2-GP R1258 CPPE# 29
0821 SI2
BOOT BIOS Strap
PCI_GNT#0 PCI_GNT1# BOOT BIOS Location
0 0 LPC*
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
<Core Design>
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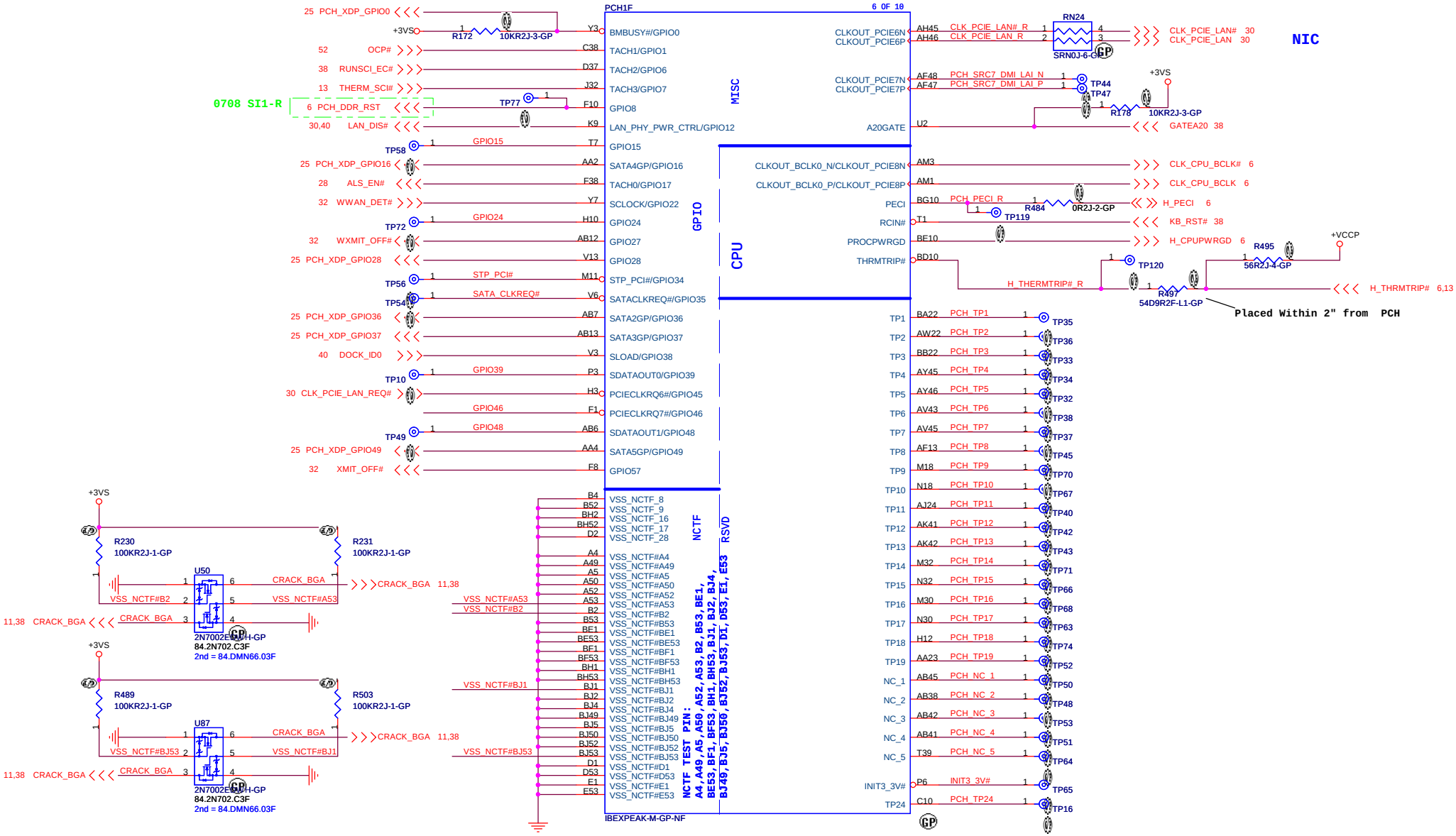
Hsichih, Taipei
Title
PCH(5/9)-PCI+USB+NVRAM
Size A3
Document Number NORN 3.0
Rev SE
Date: Thursday, September 10, 2009
Sheet 20 of 57



<Core Design>

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Title: PCH(6/9)-GPIO+VSS_NCTF+RSVD

Size	Document Number	Rev
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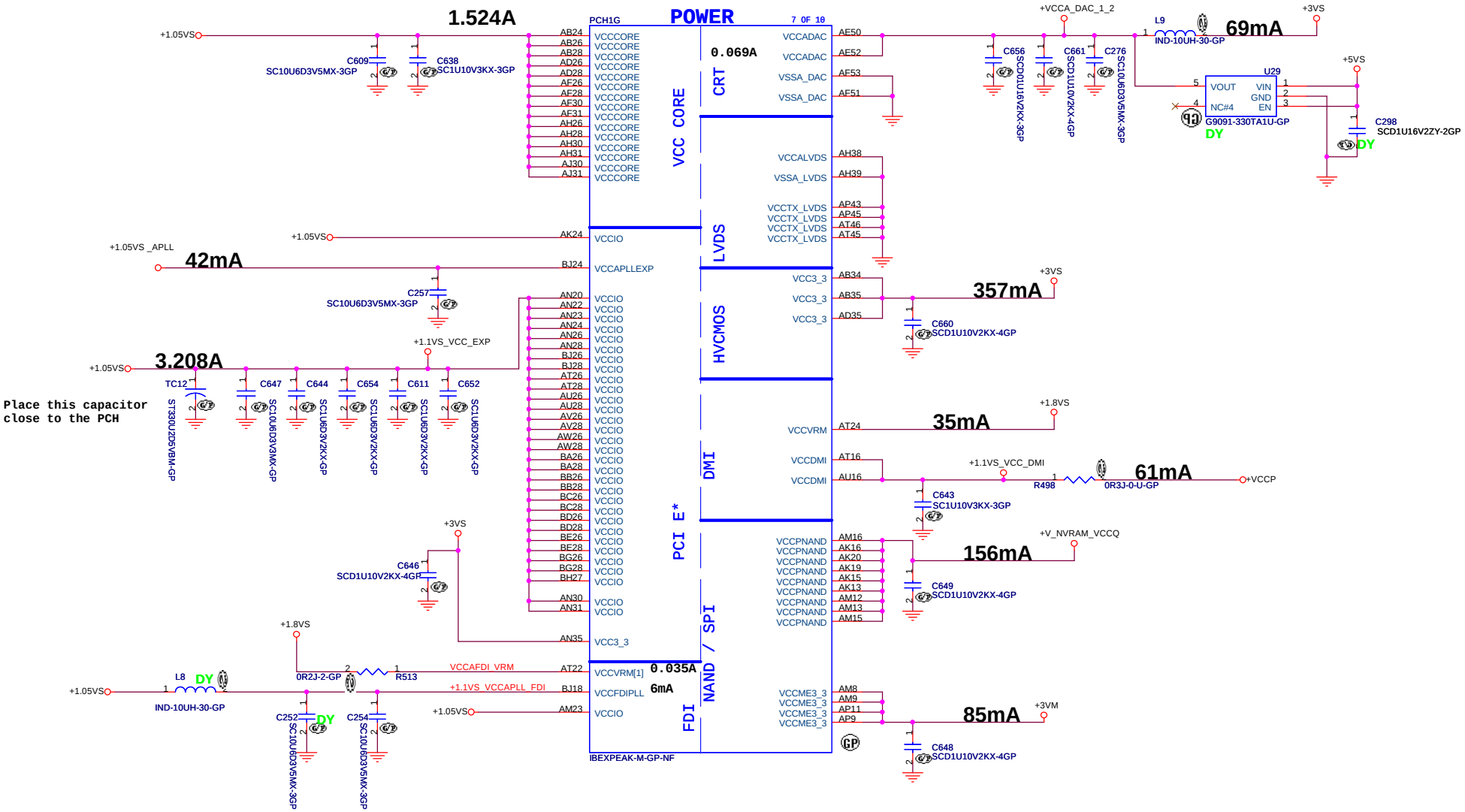

<Core Design>

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Title: PCH(7/9)-POWER

Size	Document Number	Rev
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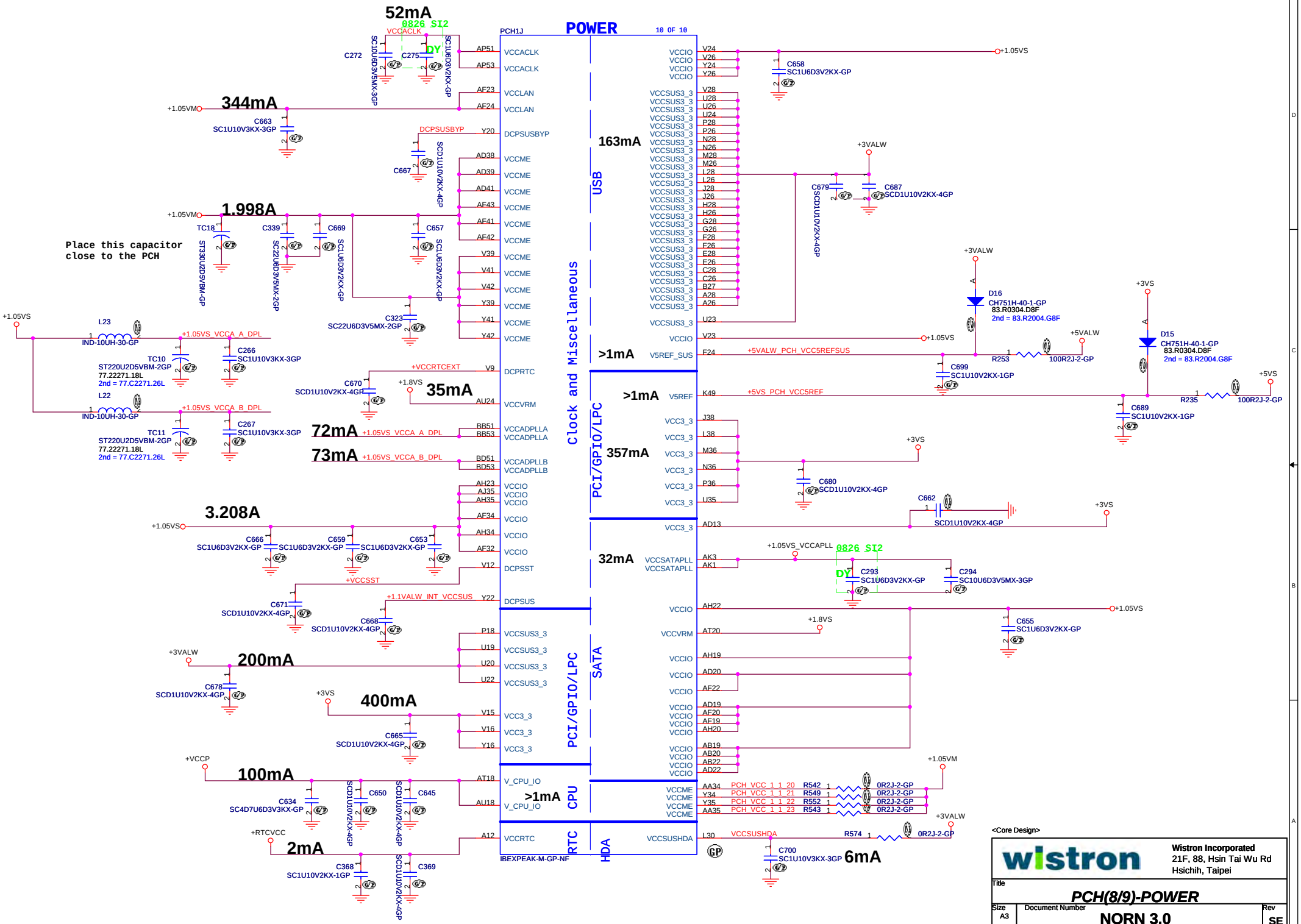
POWER
PCH1J
10 OF 10
52mA
0826 SI2
DY
344mA
1.998A
Place this capacitor close to the PCH
35mA
72mA
73mA
3.208A
200mA
400mA
100mA
2mA
163mA
>1mA
357mA
32mA
>1mA
6mA
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
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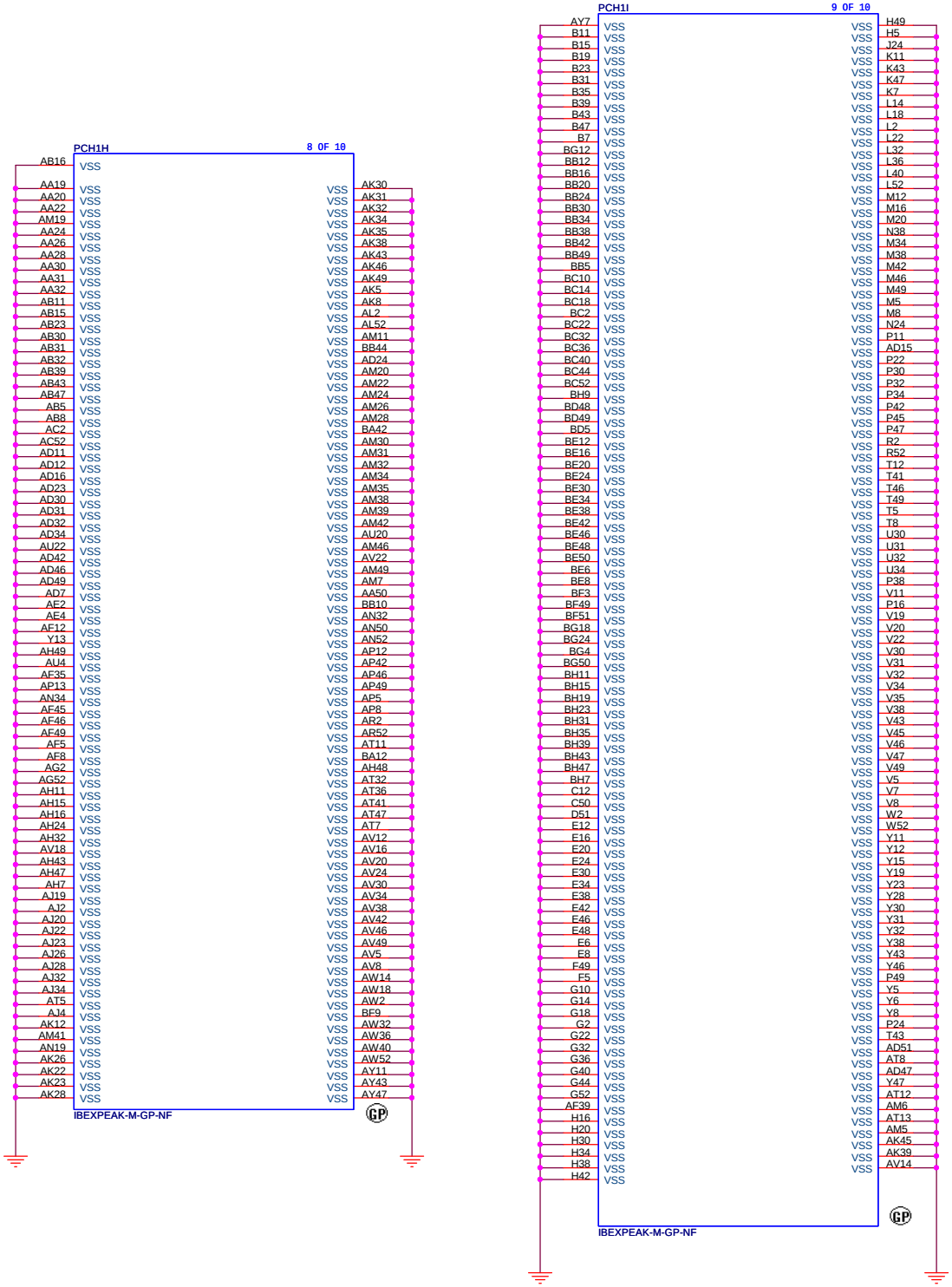
Hsichih, Taipei
PCH(8/9)-POWER
NORN 3.0
Size A3
Rev SE
Date: Wednesday, August 26, 2009
Sheet 23 of 57



<Core Design>

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Title: PCH(9/9)-GND

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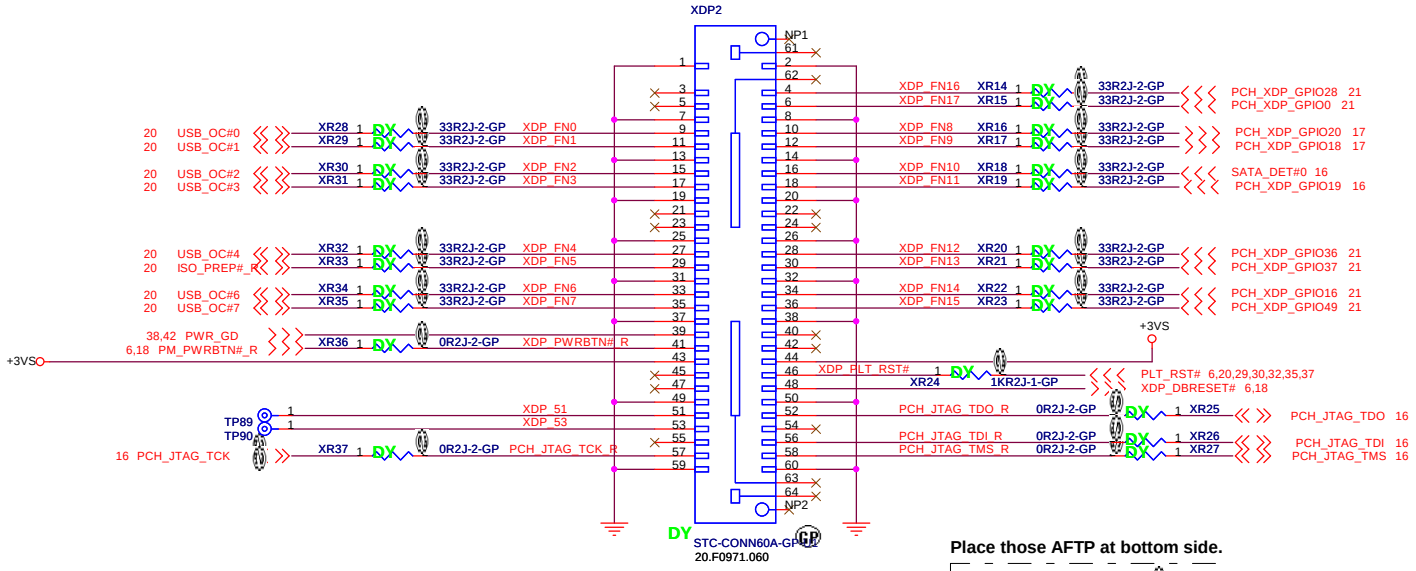
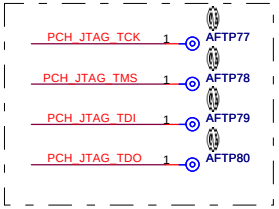
0626 SI1
Remove XDP2 and relative circuits.
0711 SI1-R
Add back.



Place those AFTP at bottom side.



<Core Design>

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Title: PCH XDP

Size	Document Number	Rev
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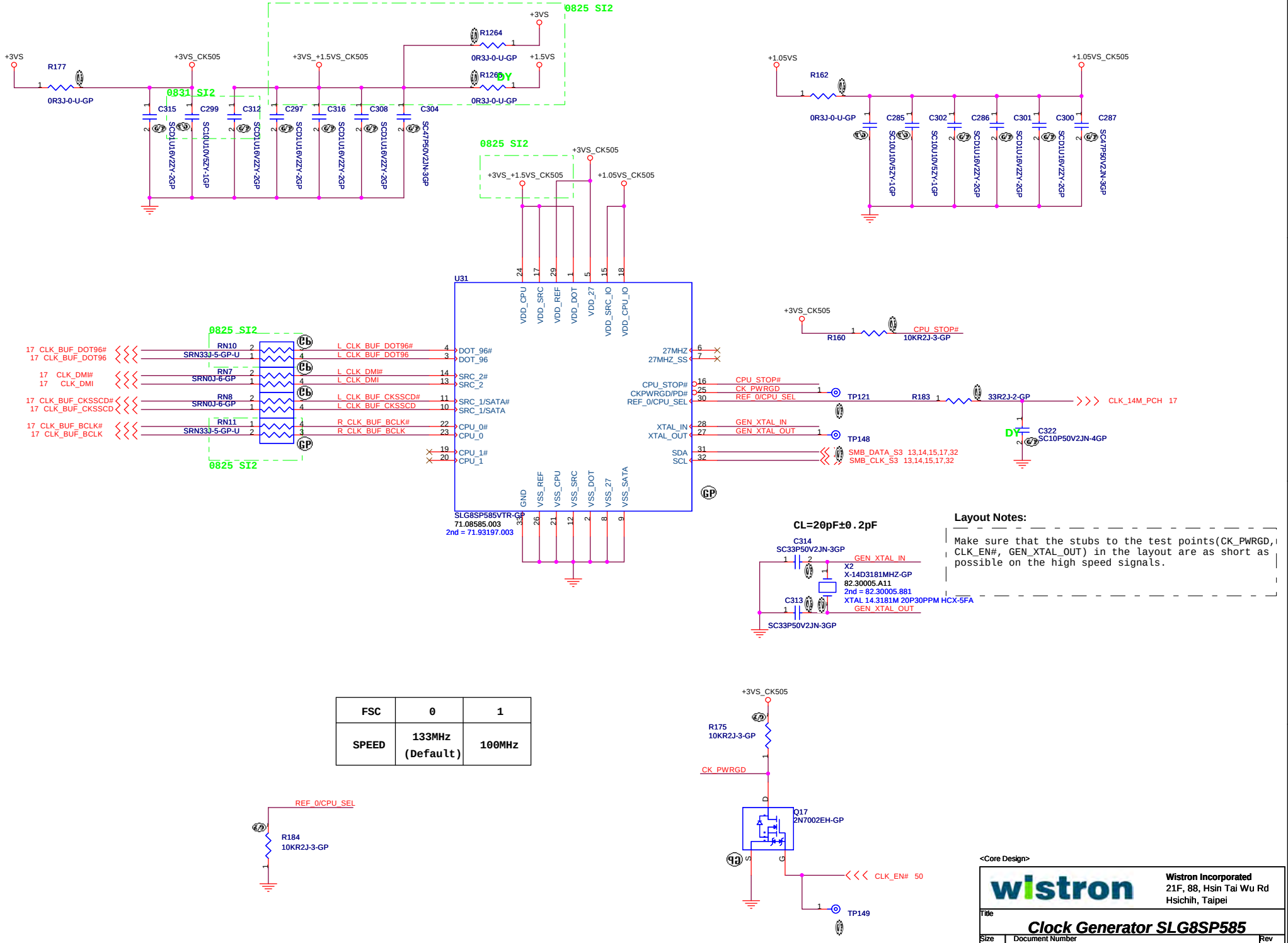

FSC	0	1
SPEED	133MHz (Default)	100MHz

<Core Design>

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Title: Clock Generator SLG8SP585

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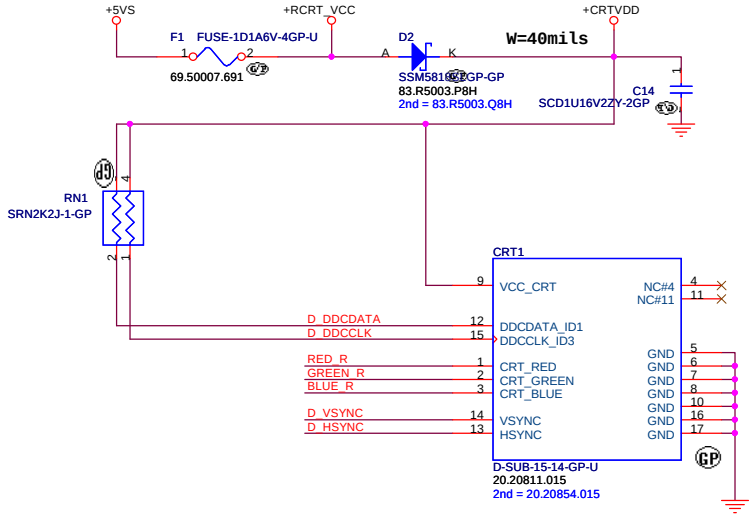
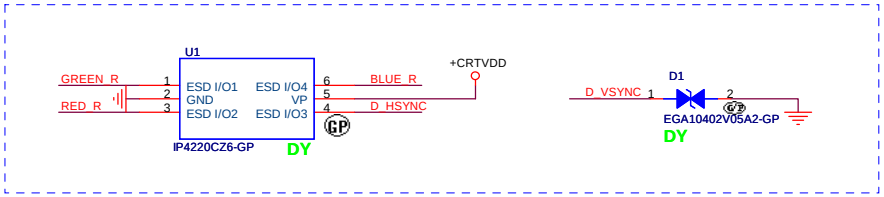
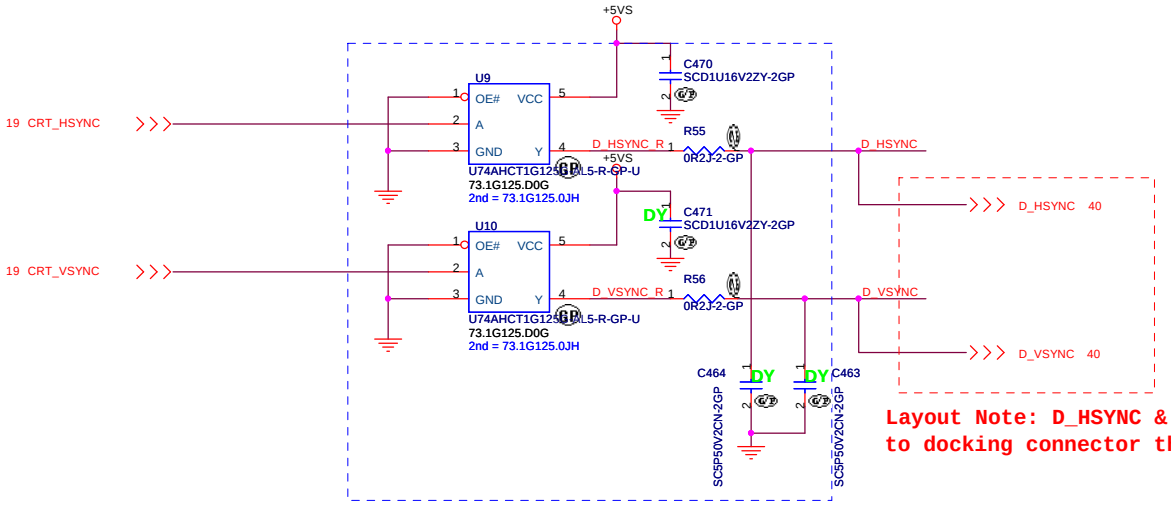
CRT connector



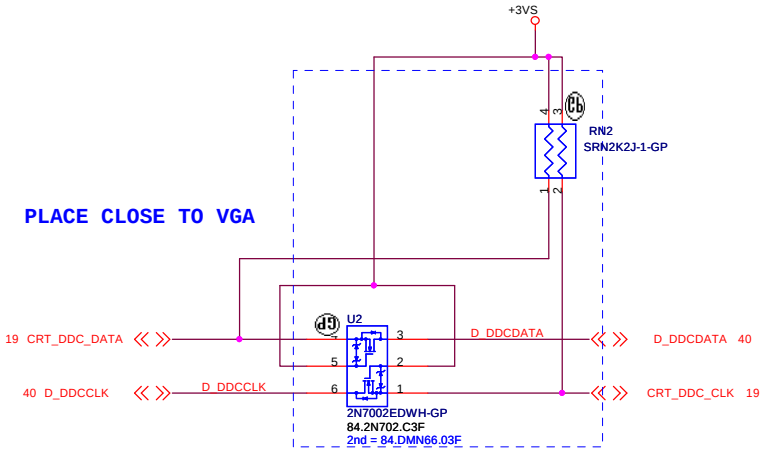


Place near the CRT connector



PLACE CLOSE TO VGA

Layout Note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector



<Core Design>

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Title: **CRT/TV CONNECTOR**

Size	Document Number	Rev
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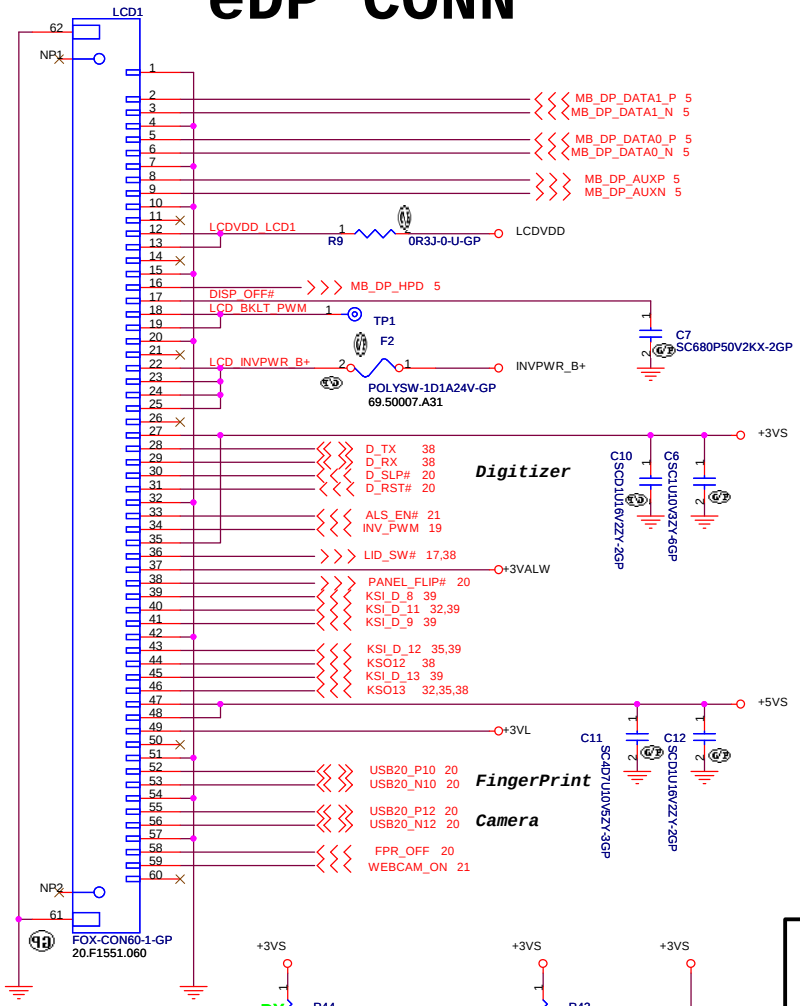
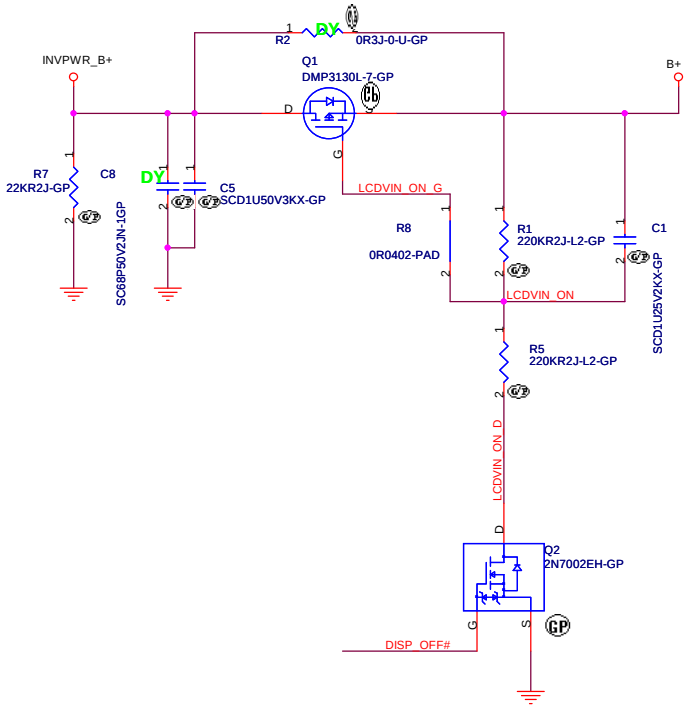
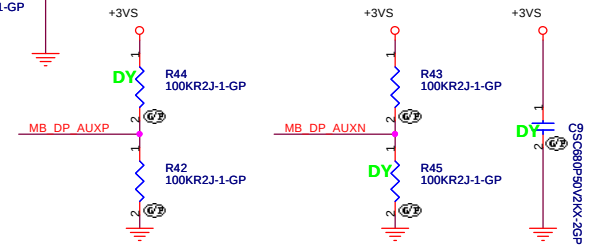
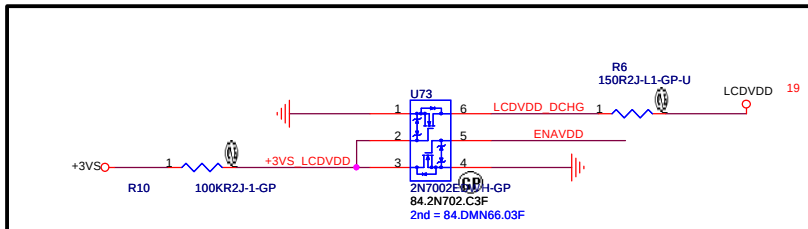
eDP CONN

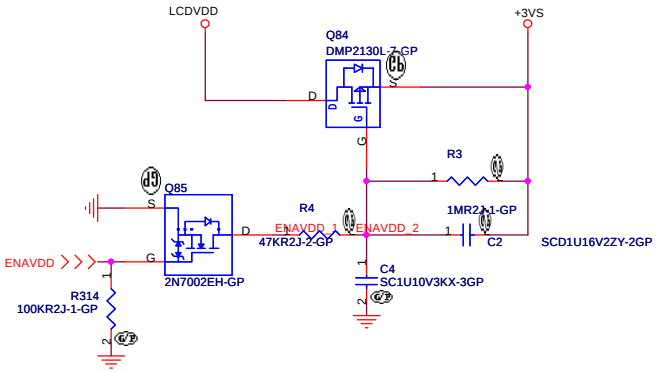


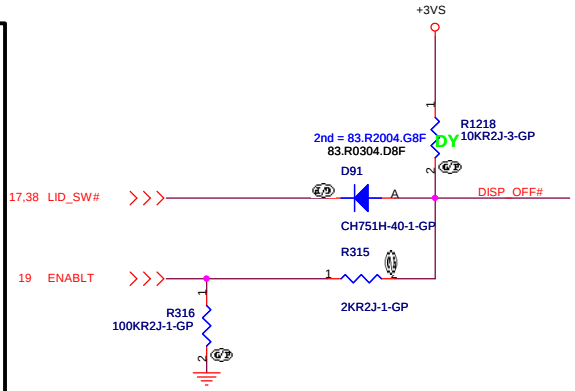




LCD POWER CIRCUIT







<core_design>

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Title	LCD CONN.	
Size A3	Document Number NORN 3.0	Rev SE
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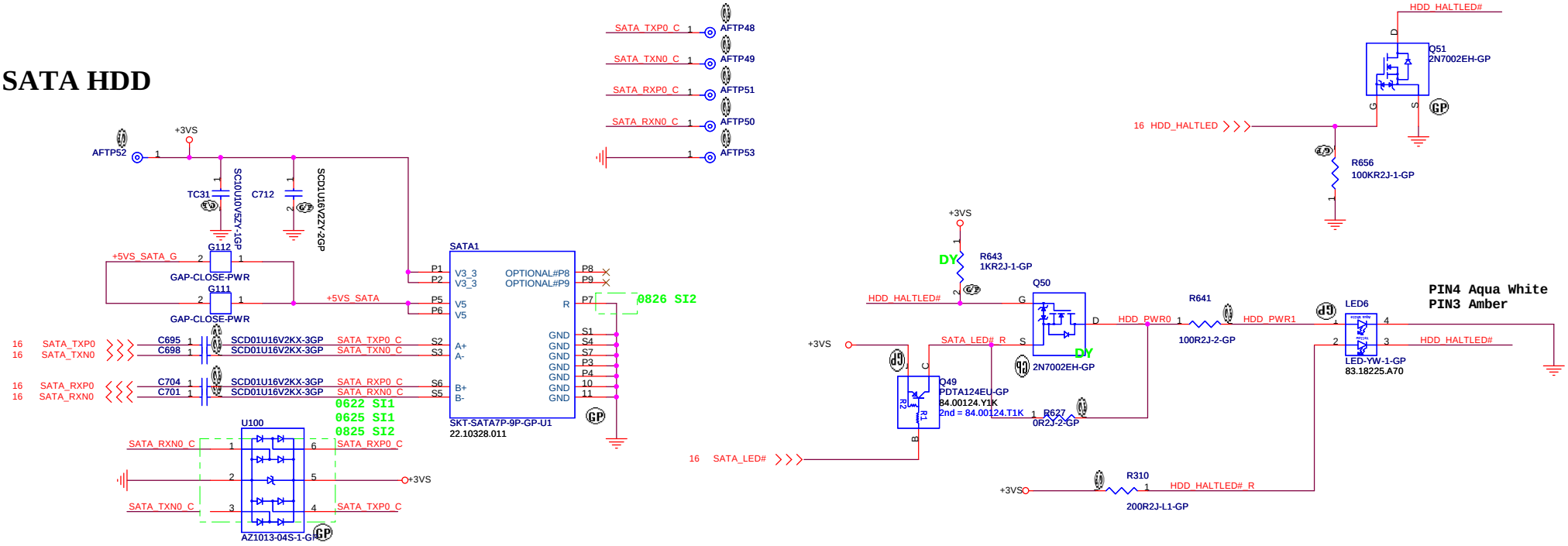
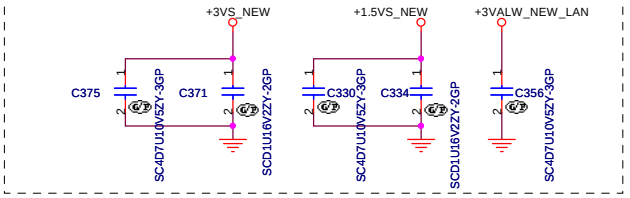
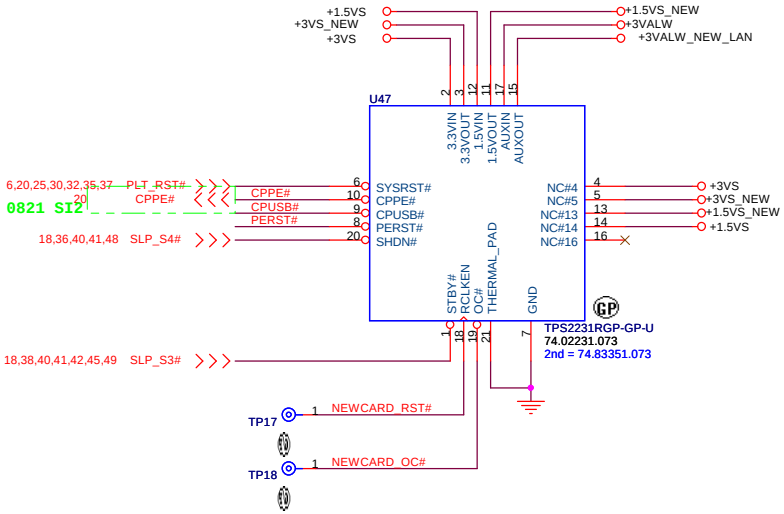
</core_design>

SATA HDD

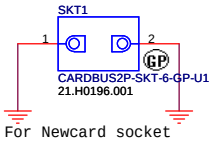


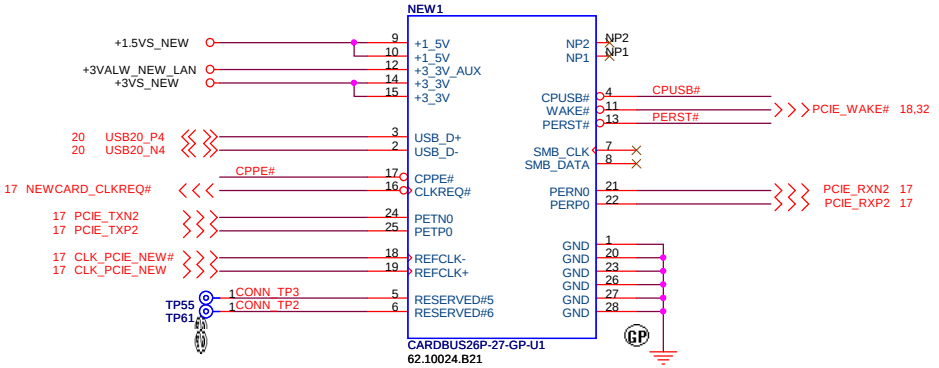
Place them Near to Connector





NEWCARD Connector





<Core Design>

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Hsichih, Taipei

Title: HDD /NEW CARD CONN.

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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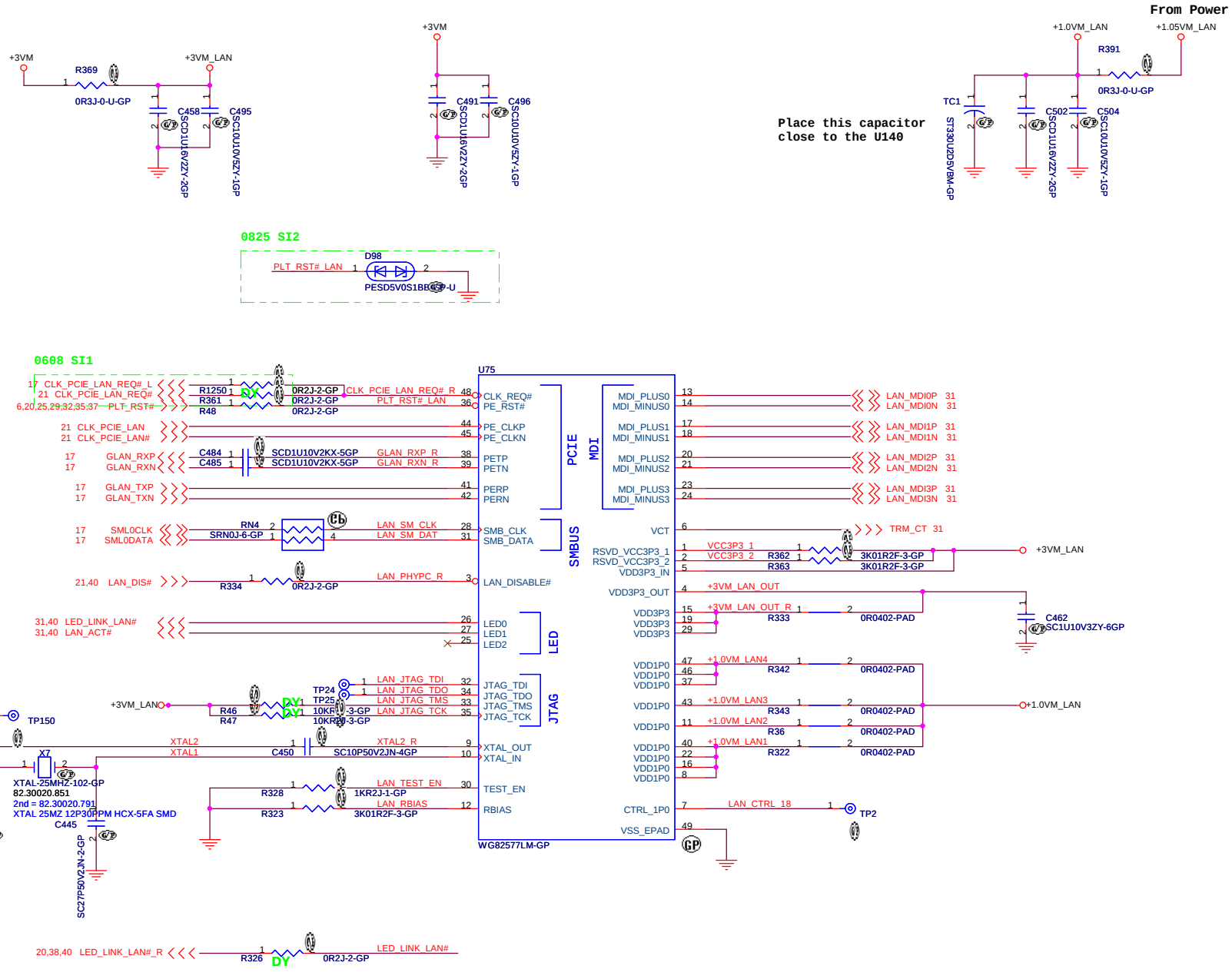

<Core Design>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Intel 82577 Bavoz

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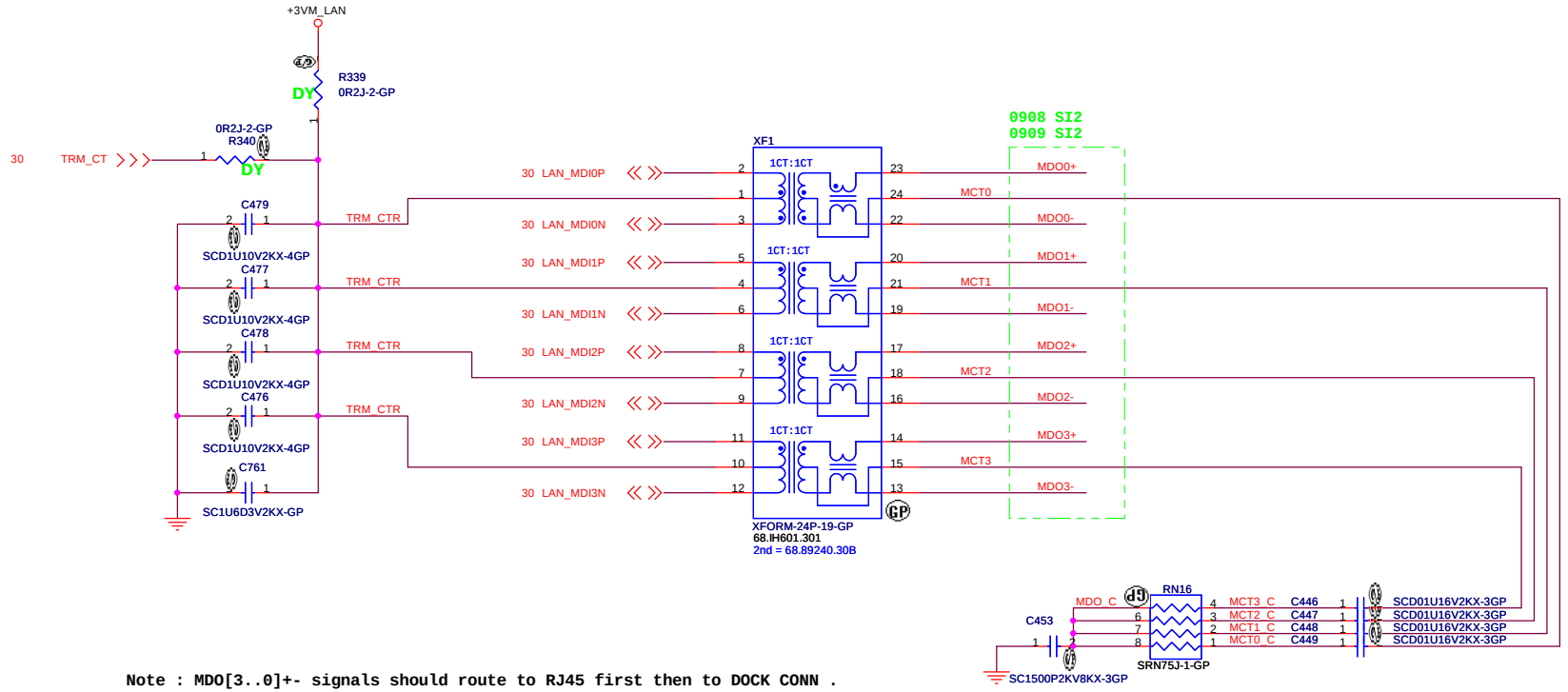
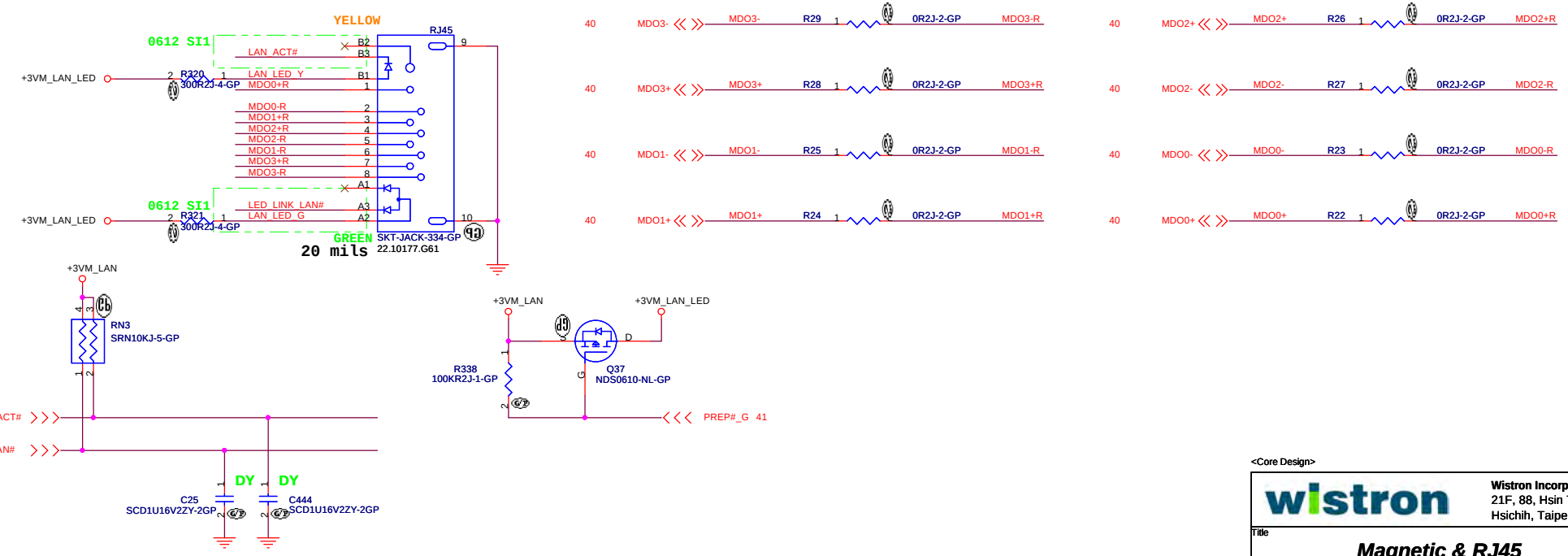


Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **Magnetic & RJ45**

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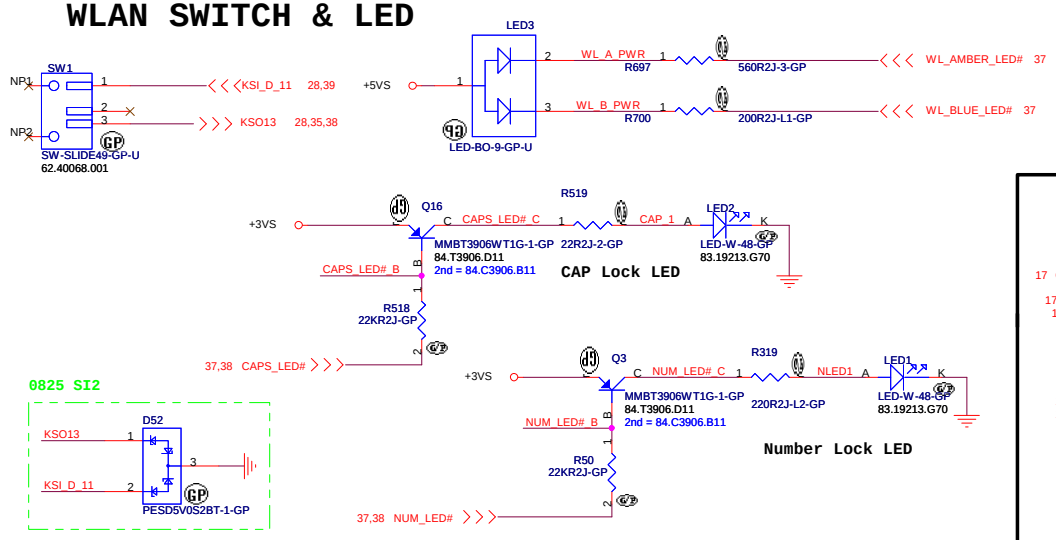
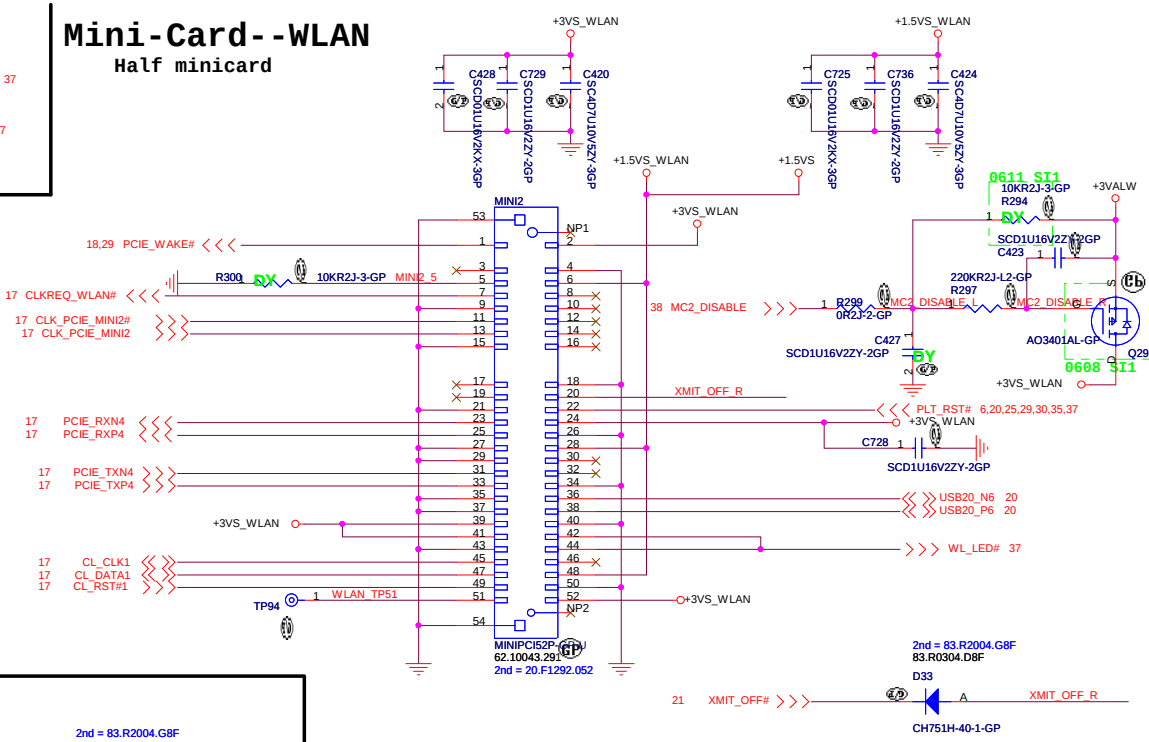
WLAN SWITCH & LED



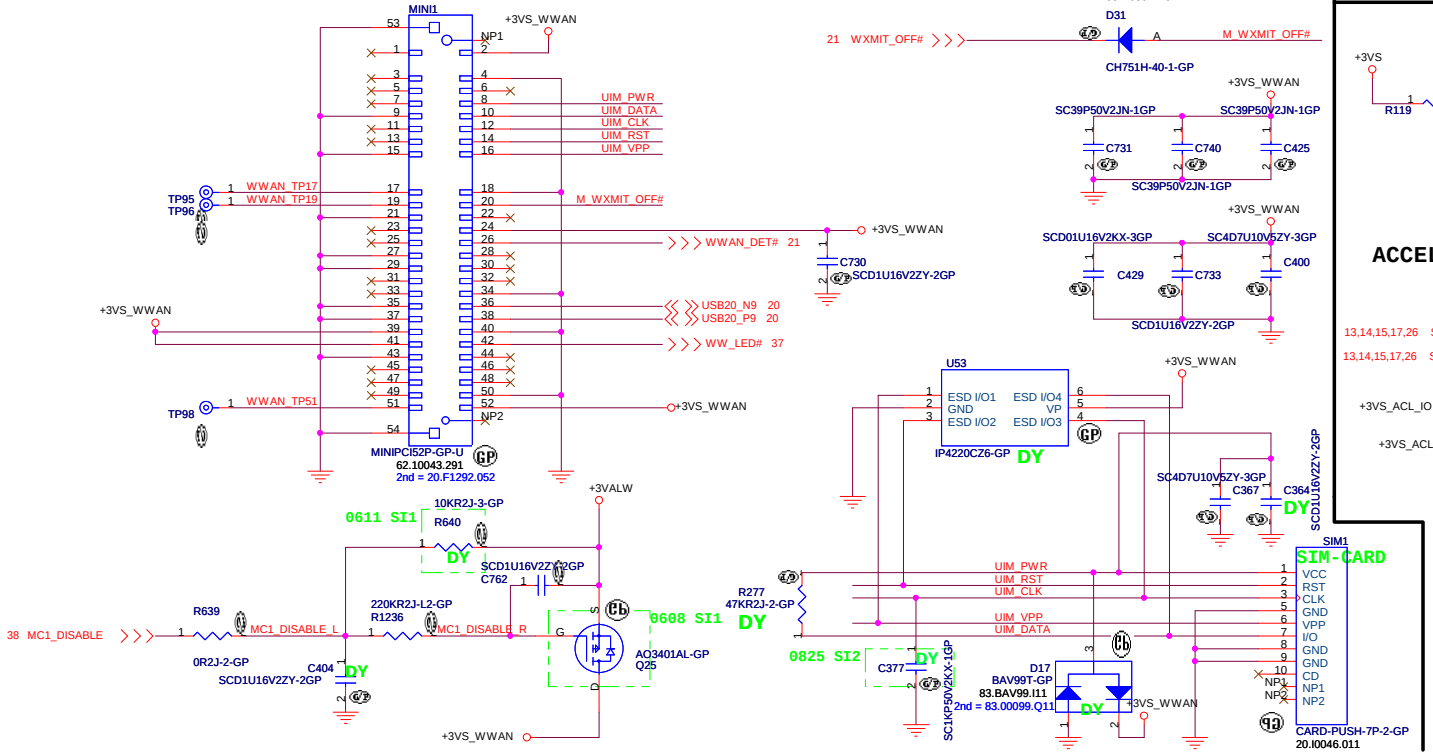
Mini-Card--WLAN

Half minicard

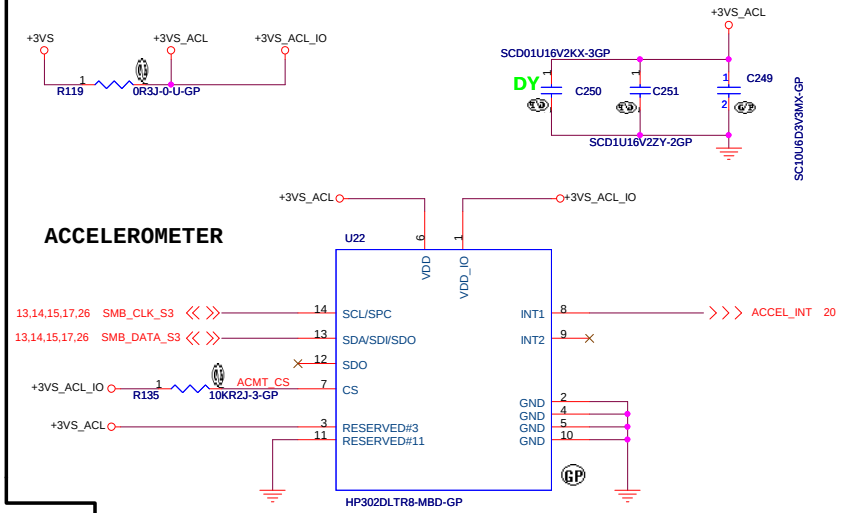


Mini-Card--WWAN

Full minicard



ACCELEROMETER



<Core Design>

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Title: Mini-Card/Accelerometer

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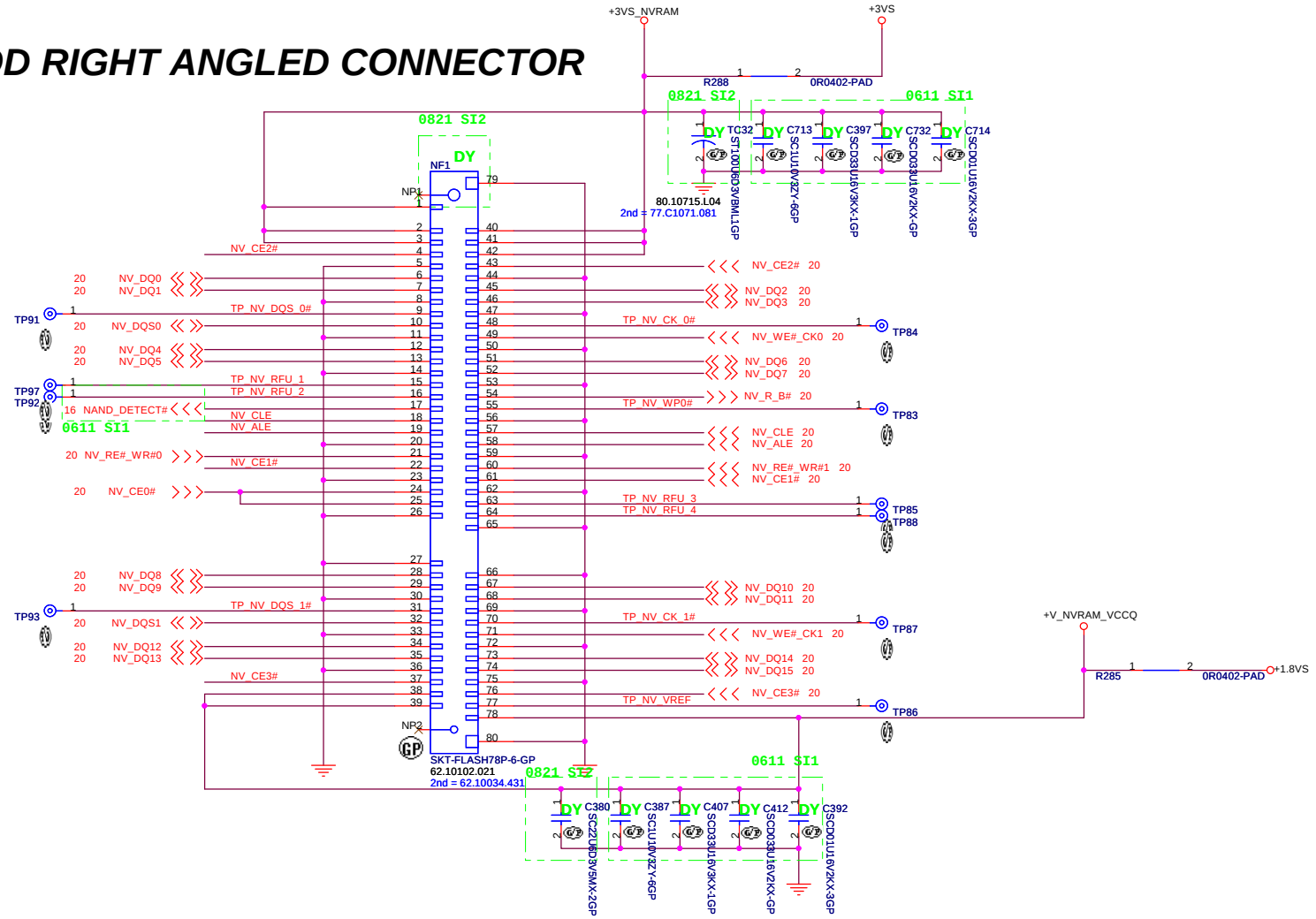
BRAIDWOOD RIGHT ANGLED CONNECTOR



<Core Design>

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Hsichih, Taipei

Title: NAND FLASH CONN

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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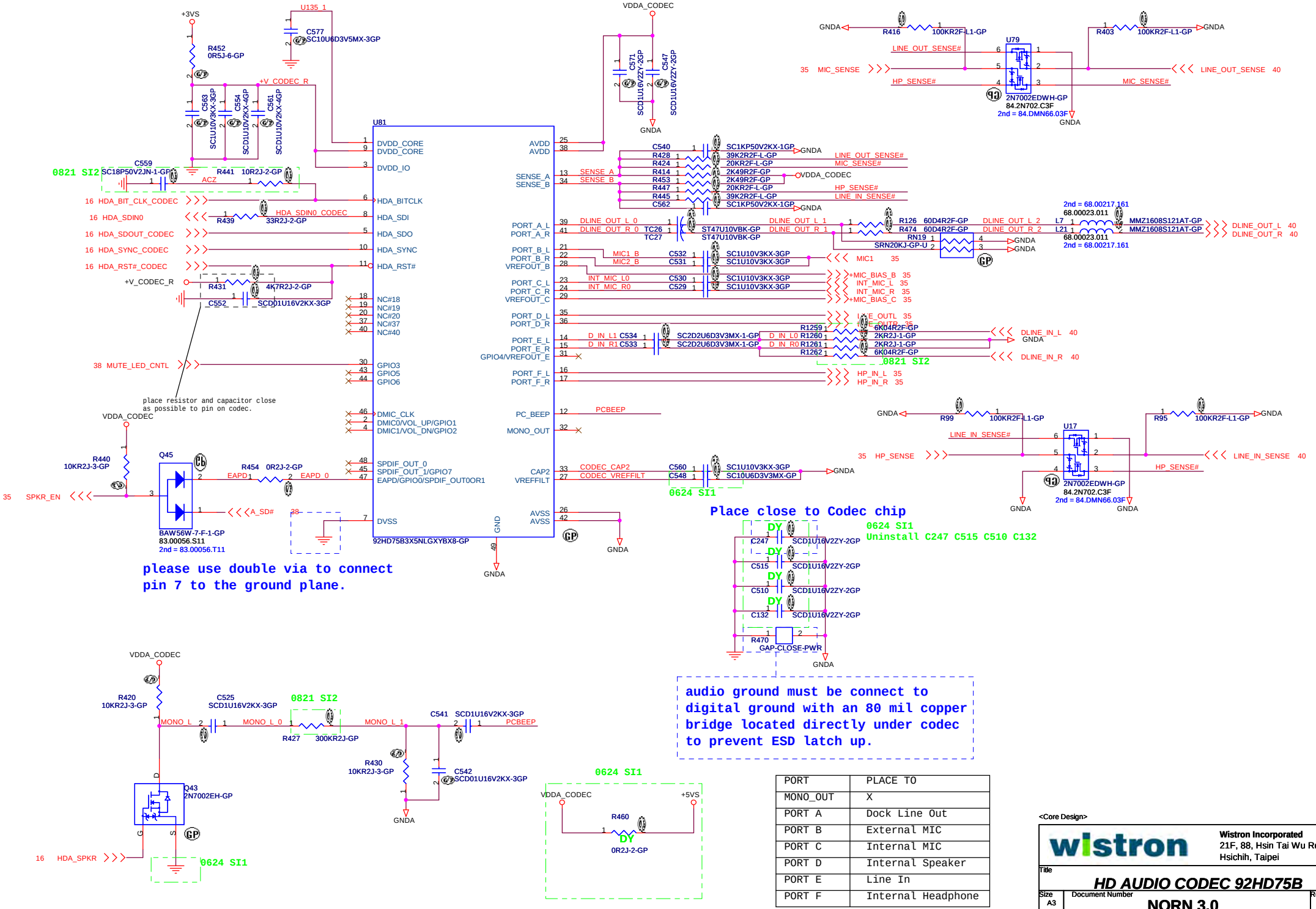

PORT	PLACE TO
MONO_OUT	X
PORT A	Dock Line Out
PORT B	External MIC
PORT C	Internal MIC
PORT D	Internal Speaker
PORT E	Line In
PORT F	Internal Headphone

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HD AUDIO CODEC 92HD75B

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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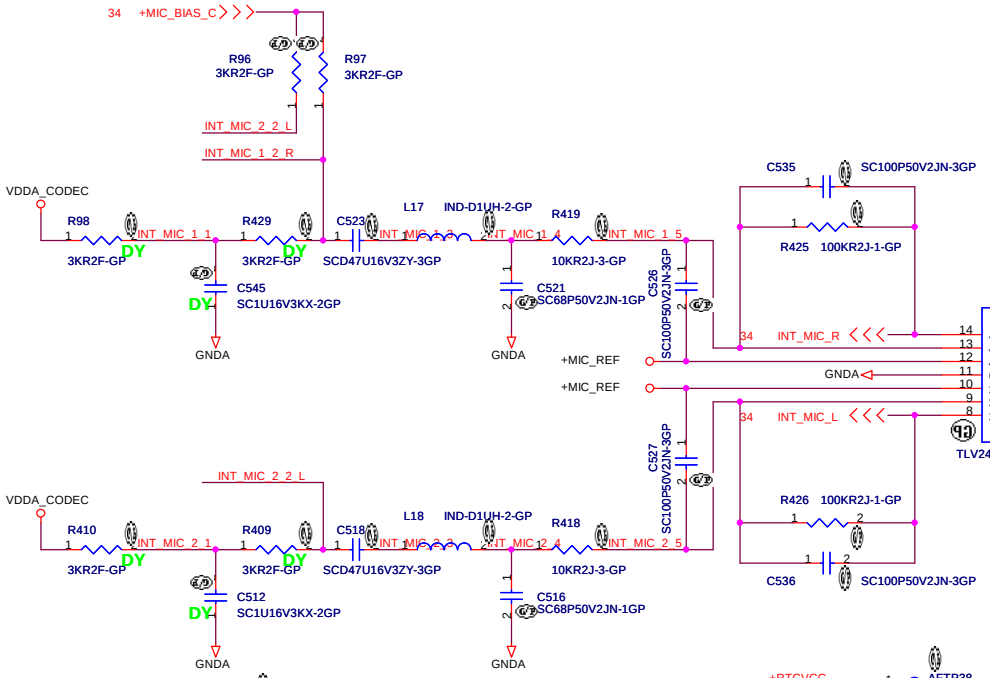
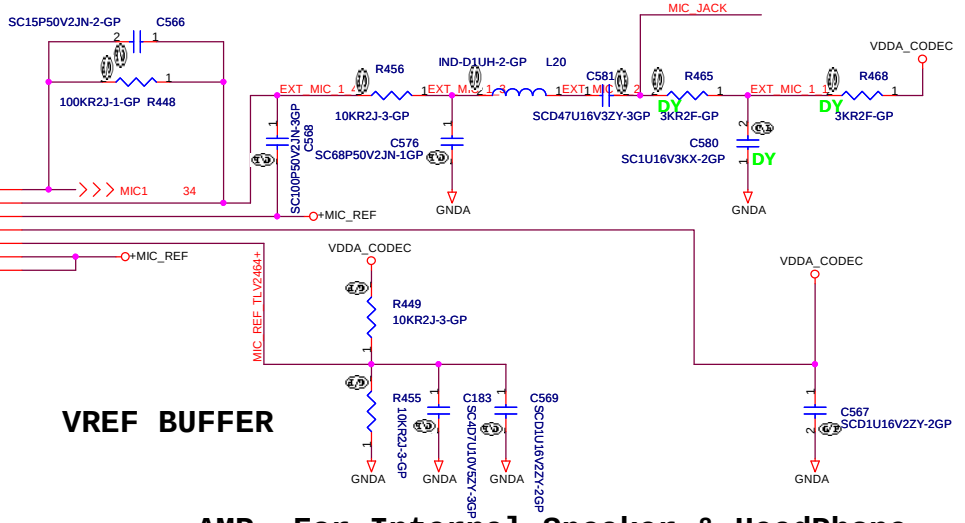
AMP. for Internal Microphone

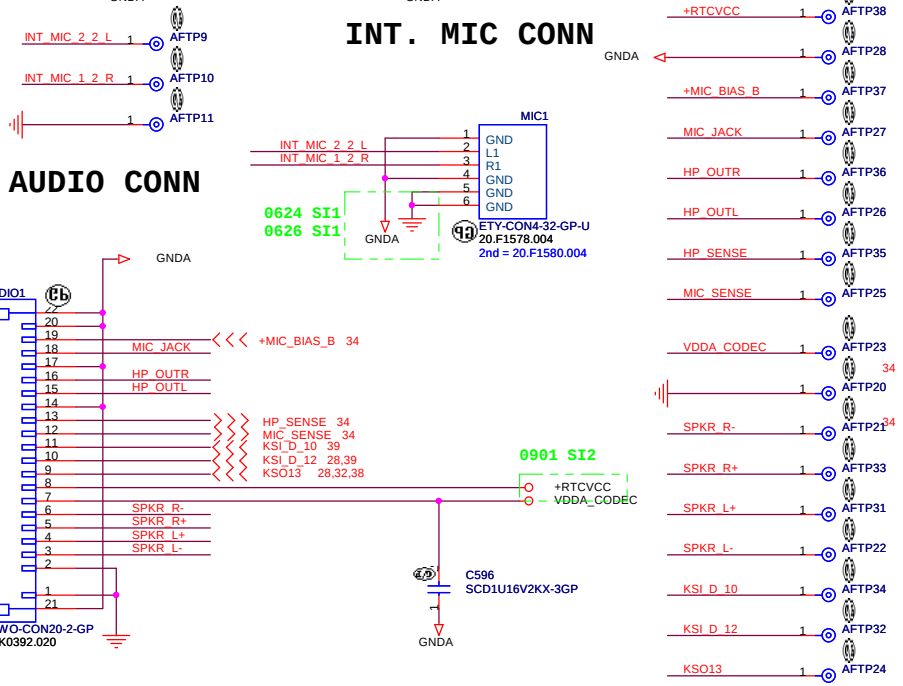


AMP. for External Microphone



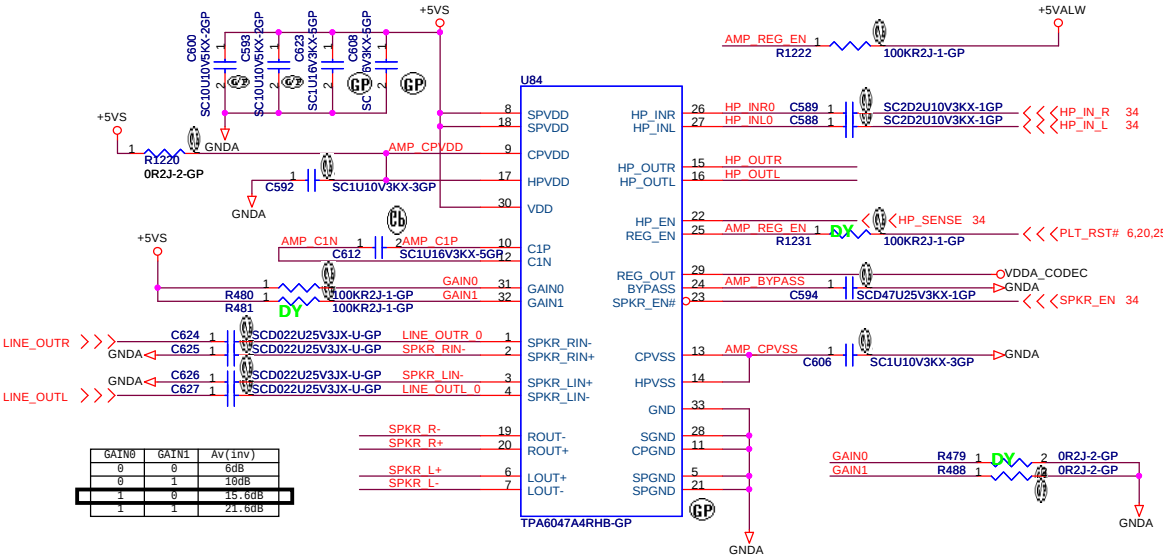
VREF BUFFER

INT. MIC CONN



AUDIO CONN

AMP. For Internal Speaker & HeadPhone.



GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

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Hsichih, Taipei

Title: *AMP & Audio Conn.*

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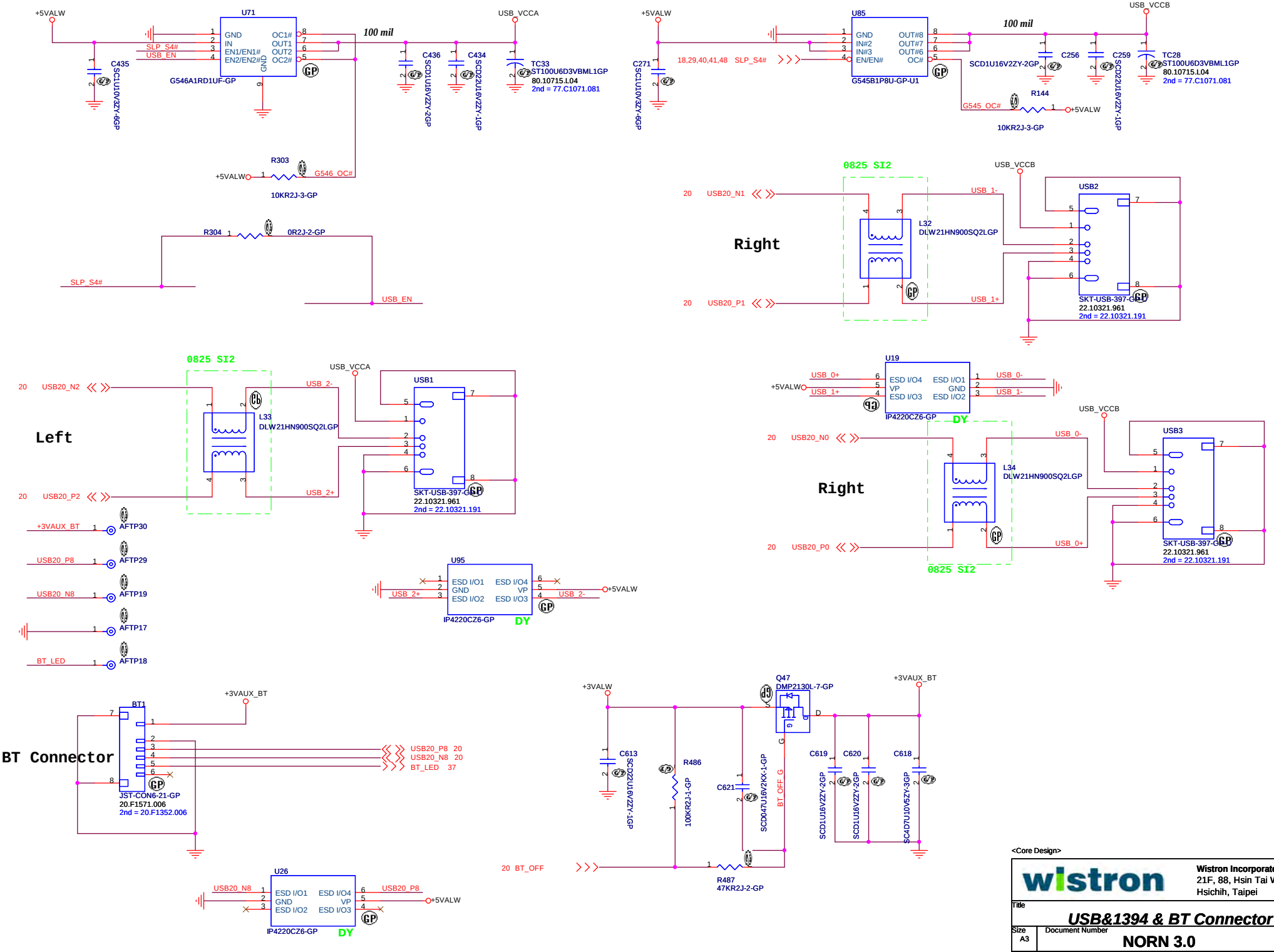

<Core Design>

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Hsichih, Taipei

Title: USB&1394 & BT Connector

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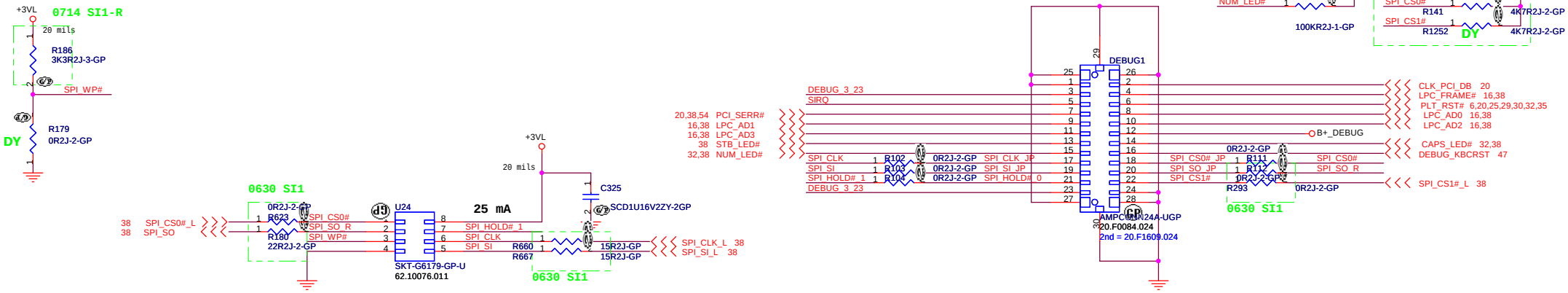
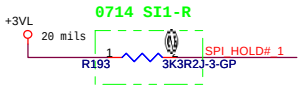
8Mb x 1

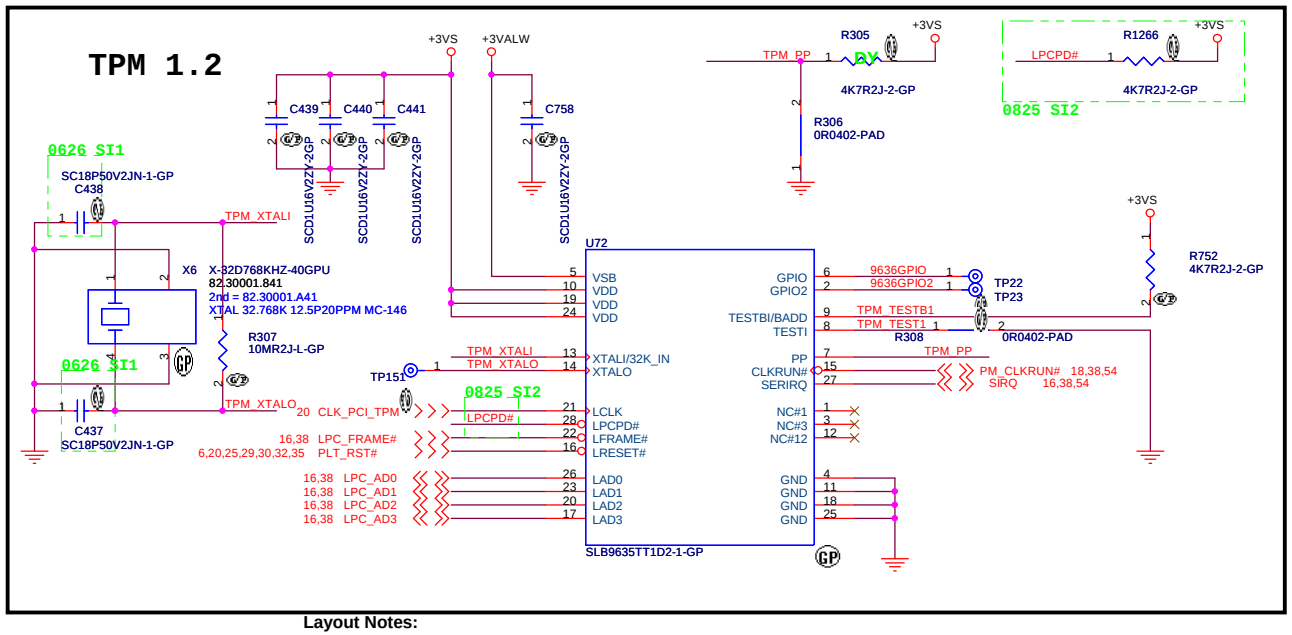
LPC Debug Port



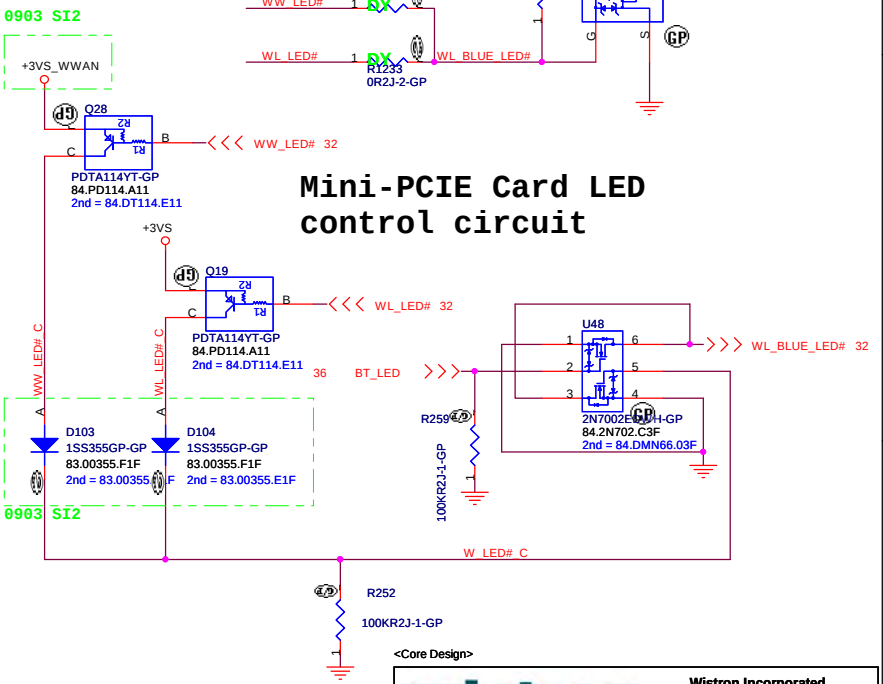
8M SPI
>72.25644.001 MX25L6445EM2I-10G 8-SOP
>72.25Q64.001 W25Q64BVSSIG SOIC-8



TPM 1.2



Mini-PCIE Card LED control circuit



Layout Notes:

Make sure that the stubs to the test points(TPM_XTALO) in the layout are as short as possible on the high speed signals.

<Core Design>

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Title: TPM/BIOS/24 DEBUG PORT

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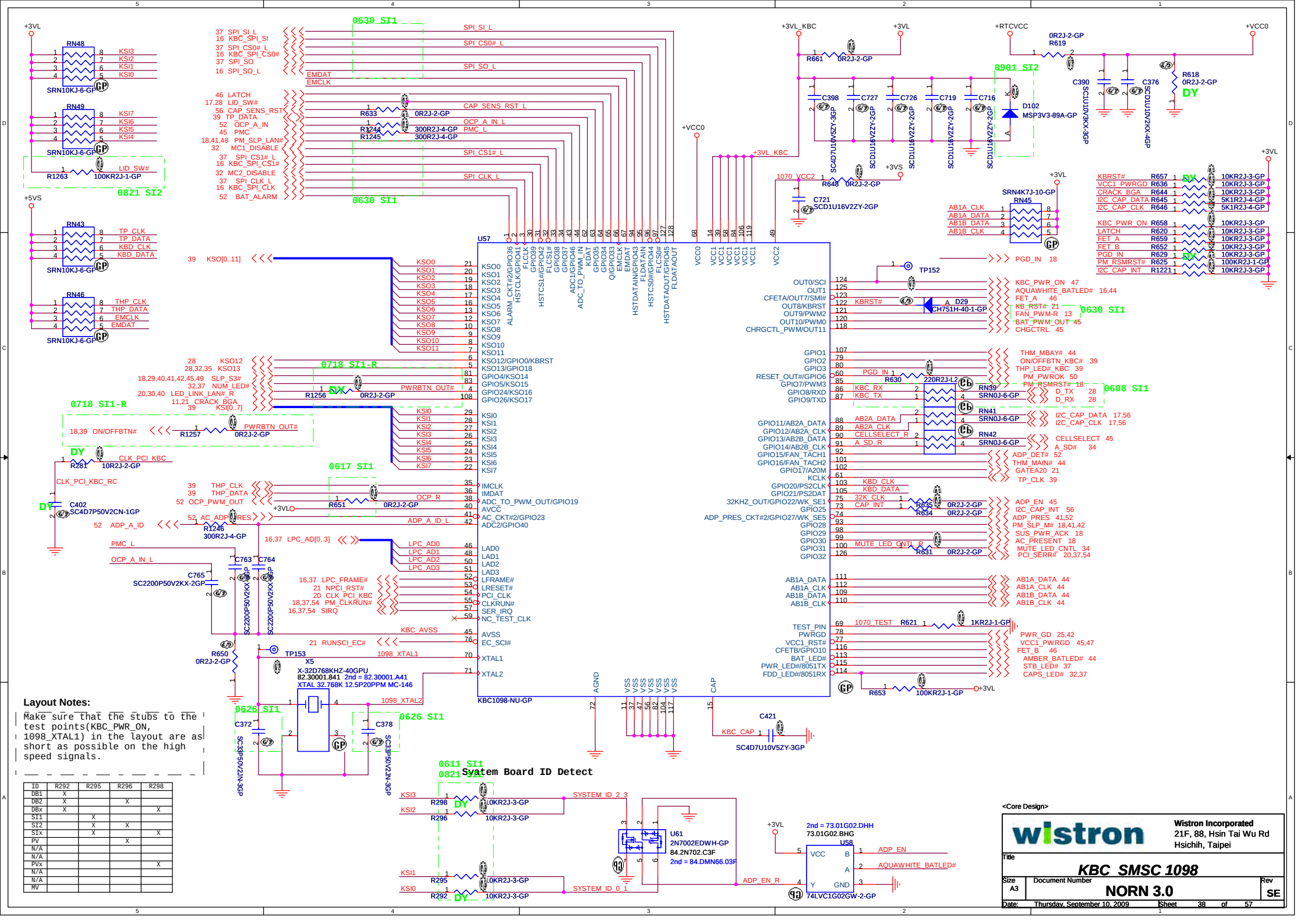
0630 SI1
0821 SI2
0718 SI1-R
0617 SI1
0901 SI2
0630 SI1
0608 SI1
0626 SI1
0611 SI1
0821 SI1
DY
U57
KBC1098-NU-GP
Layout Notes:
Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.
System Board ID Detect
ID R292 R295 R296 R298
DB1 X
DB2 X X
DBx X X
SI1 X
SI2 X X
SIx X X
PV X
N/A
N/A
PVx X
N/A
N/A
MV
<Core Design>
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Hsichih, Taipei
Title
KBC SMSC 1098
Size A3
Document Number
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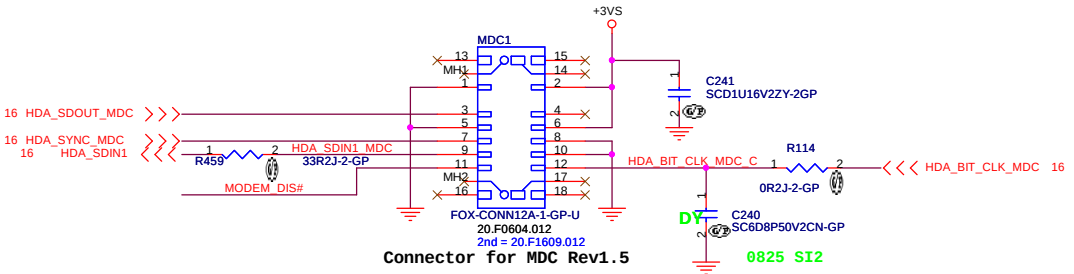
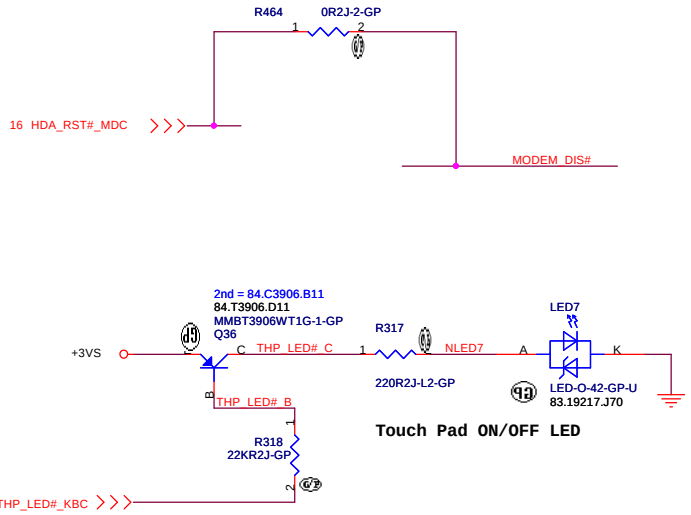
MDC 1.5 Conn.

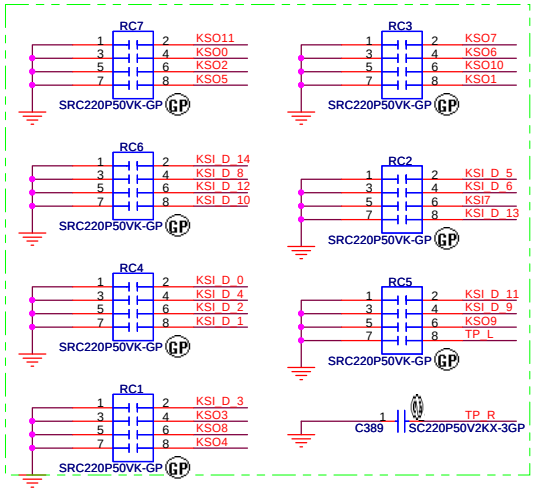


Connector for MDC Rev1.5



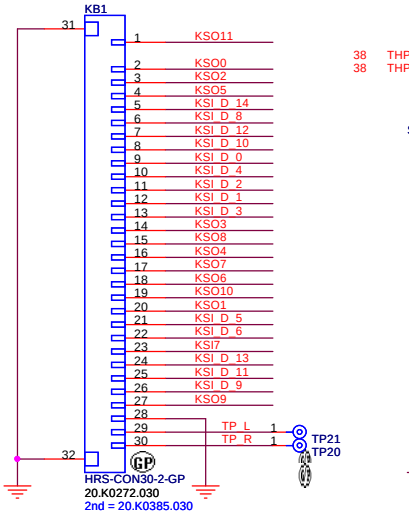
Touch Pad ON/OFF LED

0825 SI2

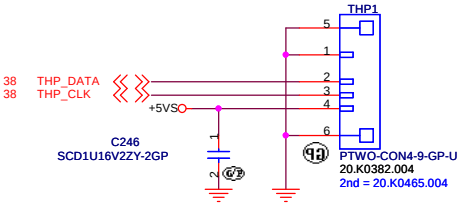


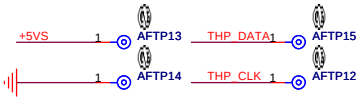
INT_KBD CONN.

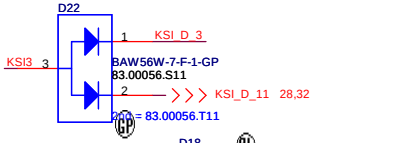
38 KSO[0..11] KSO[0..11]
38 KSI[0..7] KSI[0..7]

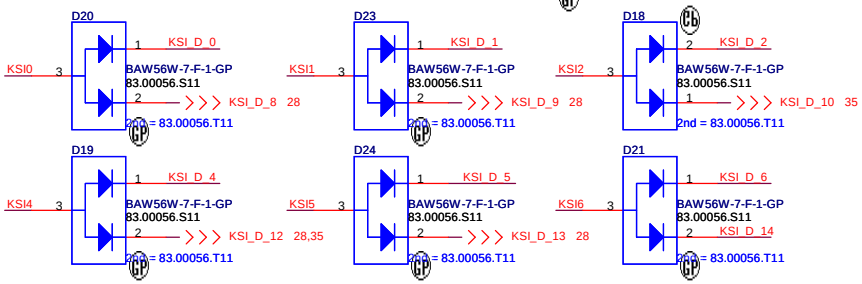


Touch_Pad CONN.

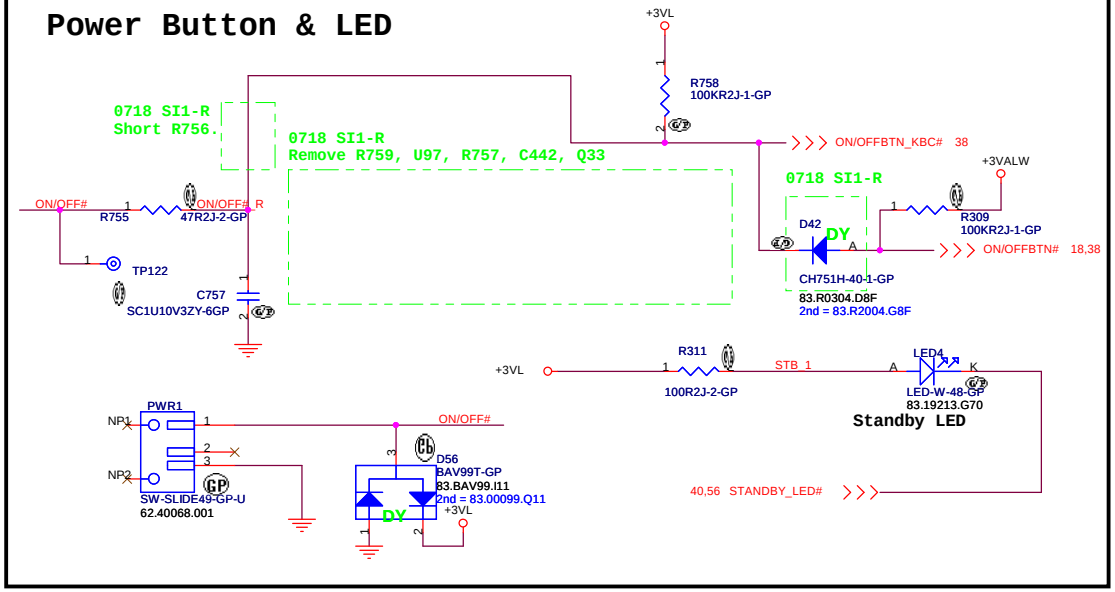




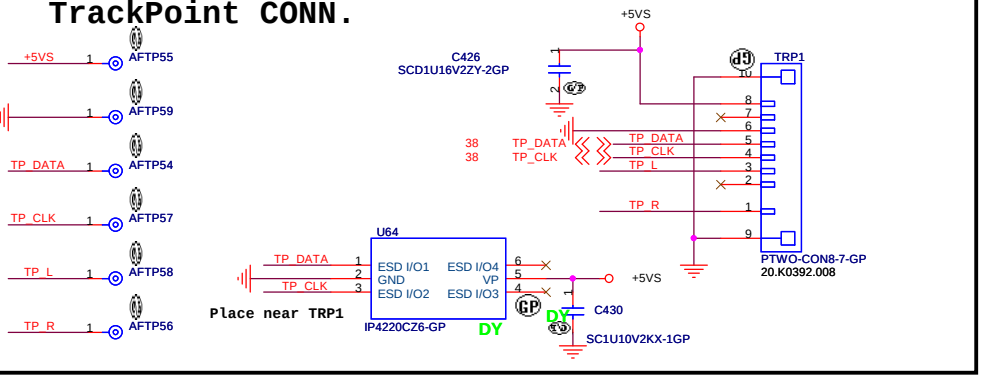


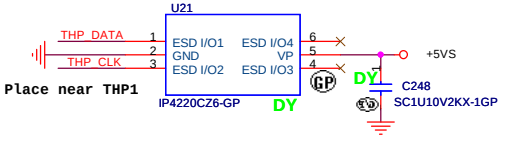


Power Button & LED



TrackPoint CONN.





<Core Design>

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Hsichih, Taipei

Title: MDC/KBD/ON OFF/T.P.

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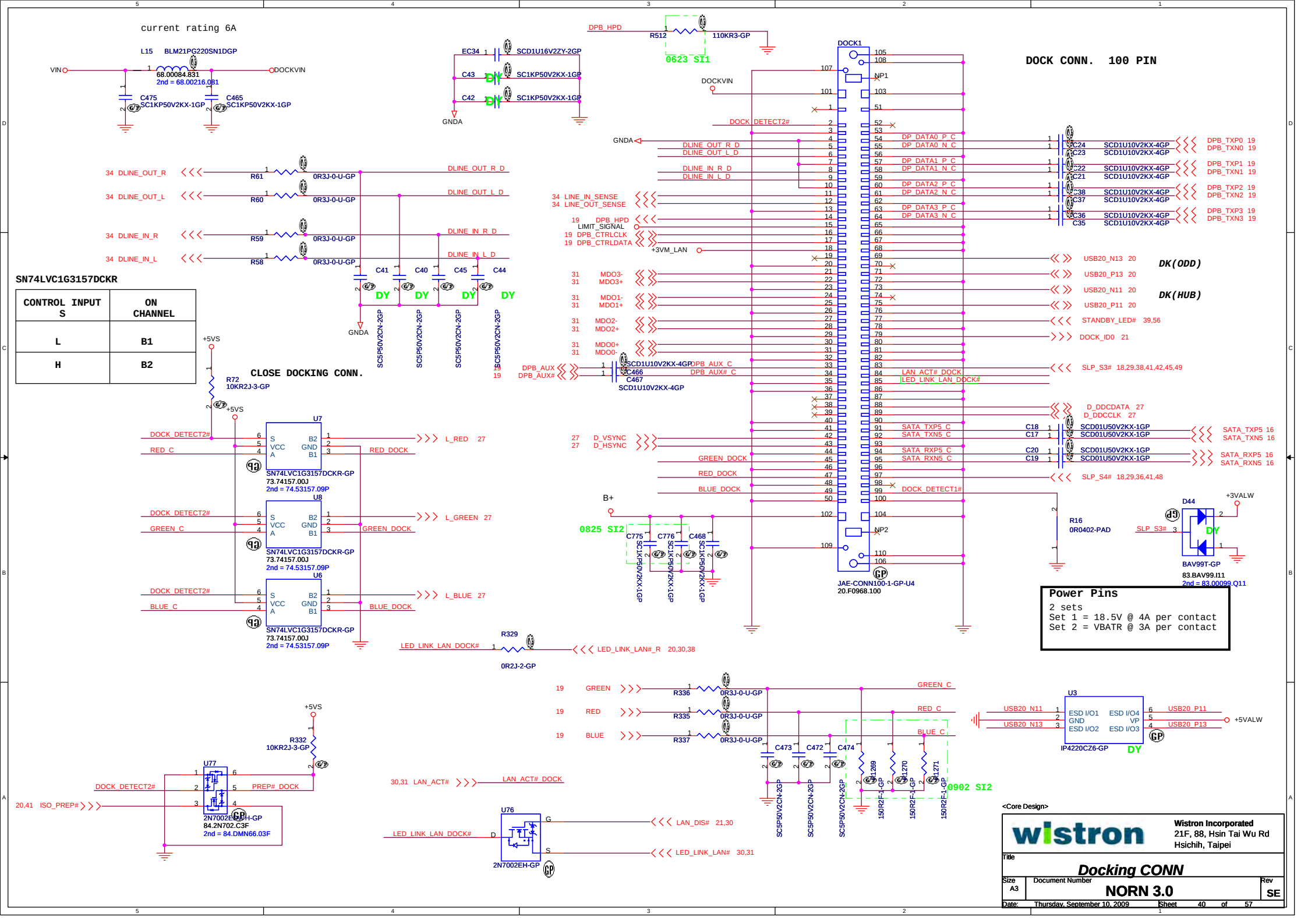
current rating 6A
L15 BLM21PG220SN1DGP
VIN
68.00084.831
2nd = 68.00216.031
DOCKVIN
C475 SC1KP50V2KX-1GP
C465 SC1KP50V2KX-1GP
EC34 SCD1U16V2ZY-2GP
C43 DY SC1KP50V2KX-1GP
C42 DY SC1KP50V2KX-1GP
GNDA
DPB_HPD
R512 110KR3-GP
0623 SI1
DOCK1
DOCK CONN. 100 PIN
JAE-CONN100-1-GP-U4
20.F0968.100
34 DLINE_OUT_R
34 DLINE_OUT_L
34 DLINE_IN_R
34 DLINE_IN_L
R61 0R3J-0-U-GP
R60 0R3J-0-U-GP
R59 0R3J-0-U-GP
R58 0R3J-0-U-GP
DLINE_OUT_R_D
DLINE_OUT_L_D
DLINE_IN_R_D
DLINE_IN_L_D
C41 DY SC5P50V2CN-2GP
C40 DY SC5P50V2CN-2GP
C45 DY SC5P50V2CN-2GP
C44 DY SC5P50V2CN-2GP
SN74LVC1G3157DCKR
CONTROL INPUT S
ON CHANNEL
L
B1
H
B2
CLOSE DOCKING CONN.
R72 10KR2J-3-GP
+5VS
U7
U8
U6
SN74LVC1G3157DCKR-GP
73.74157.00J
2nd = 74.53157.09P
DOCK_DETECT2#
RED_C
GREEN_C
BLUE_C
RED_DOCK
GREEN_DOCK
BLUE_DOCK
L_RED 27
L_GREEN 27
L_BLUE 27
LINE_IN_SENSE
LINE_OUT_SENSE
DPB_HPD
LIMIT_SIGNAL
DPB_CTRLCLK
DPB_CTRLDATA
+3VM_LAN
MDO3-
MDO3+
MDO1-
MDO1+
MDO2-
MDO2+
MDO0+
MDO0-
DPB_AUX
DPB_AUX#
C466 C467 SCD1U10V2KX-4GP
DPB_AUX_C
DPB_AUX#_C
D_VSYNC
D_HSYNC
B+
0825 SI2
C775 C776 C468 SC1KP50V2KX-1GP
DOCKVIN
NP1
NP2
DOCK_DETECT2#
DOCK_DETECT1#
DP_DATA0_P_C
DP_DATA0_N_C
DP_DATA1_P_C
DP_DATA1_N_C
DP_DATA2_P_C
DP_DATA2_N_C
DP_DATA3_P_C
DP_DATA3_N_C
C24 C23 SCD1U10V2KX-4GP
C22 C21 SCD1U10V2KX-4GP
C38 C37 SCD1U10V2KX-4GP
C36 C35 SCD1U10V2KX-4GP
DPB_TXP0 19
DPB_TXN0 19
DPB_TXP1 19
DPB_TXN1 19
DPB_TXP2 19
DPB_TXN2 19
DPB_TXP3 19
DPB_TXN3 19
USB20_N13 20
USB20_P13 20
USB20_N11 20
USB20_P11 20
DK(ODD)
DK(HUB)
STANDBY_LED# 39,56
DOCK_ID0 21
SLP_S3# 18,29,38,41,42,45,49
LAN_ACT# DOCK
LED_LINK_LAN_DOCK#
D_DDCDATA 27
D_DDCCLK 27
SATA_TXP5_C
SATA_TXN5_C
SATA_RXP5_C
SATA_RXN5_C
C18 C17 SCD01U50V2KX-1GP
C20 C19 SCD01U50V2KX-1GP
SATA_TXP5 16
SATA_TXN5 16
SATA_RXP5 16
SATA_RXN5 16
SLP_S4# 18,29,36,41,48
R16 0R0402-PAD
D44 BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
+3VALW
Power Pins
2 sets
Set 1 = 18.5V @ 4A per contact
Set 2 = VBATR @ 3A per contact
R329 0R2J-2-GP
LED_LINK_LAN_DOCK#
LED_LINK_LAN#_R 20,30,38
19 GREEN
19 RED
19 BLUE
R336 R335 R337 0R3J-0-U-GP
GREEN_C
RED_C
BLUE_C
C473 C472 C474 SC5P50V2CN-2GP
150R2F-1-GP
0902 SI2
U3
IP4220CZ6-GP
USB20_N11
USB20_N13
USB20_P11
USB20_P13
+5VALW
R332 10KR2J-3-GP
U77
2N7002EH-GP
84.2N702.C3F
2nd = 84.DMN66.03F
DOCK_DETECT2#
PREP#_DOCK
20,41 ISO_PREP#
30,31 LAN_ACT#
LAN_ACT# DOCK
U76
2N7002EH-GP
LED_LINK_LAN_DOCK#
LAN_DIS# 21,30
LED_LINK_LAN# 30,31
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wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Docking CONN
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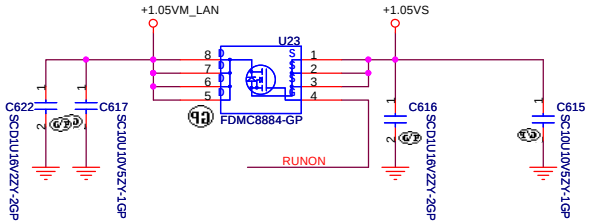
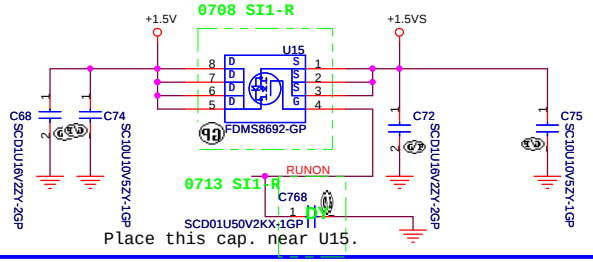
+1.05VM_LAN to +1.05VS Transfer

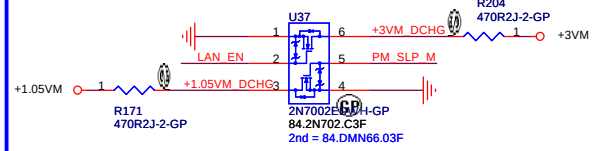


+1.5V to +1.5VS Transfer

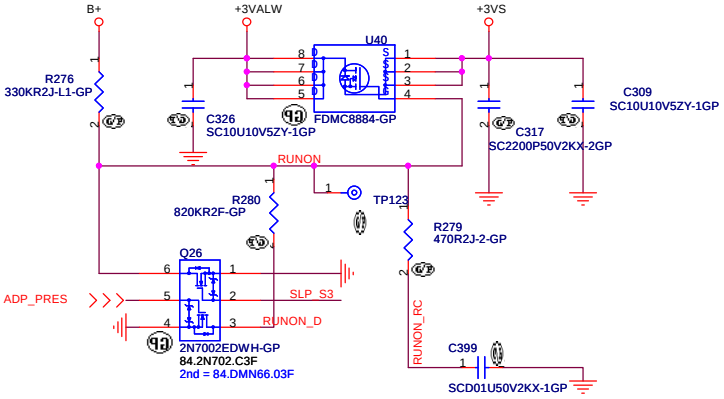


Place this cap. near U15.

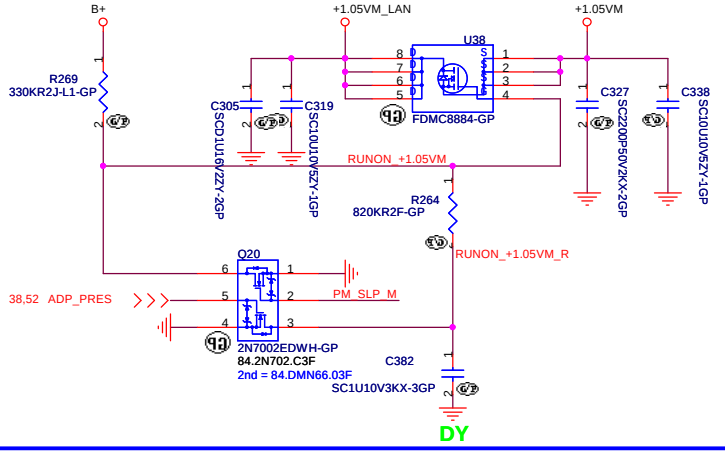
Discharge circuit-2 fot V-M



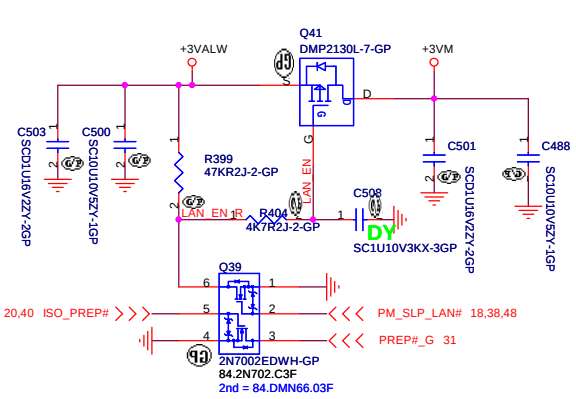
+3VALW to +3VS Transfer



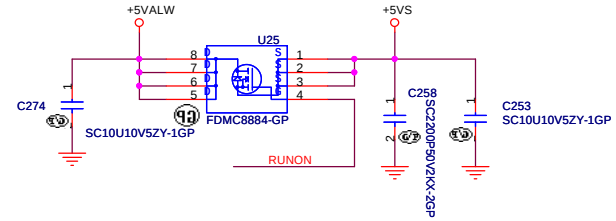
+1.05VM_LAN to +1.05VM Transfer

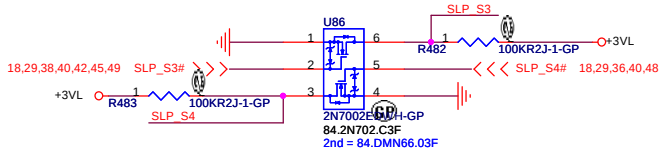


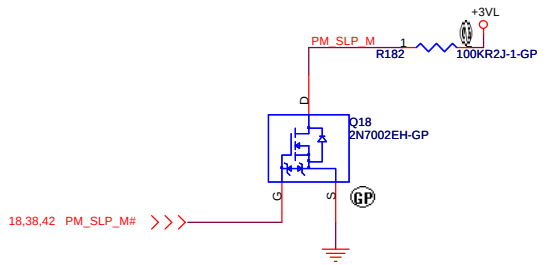
+3VALW to +3VM Transfer



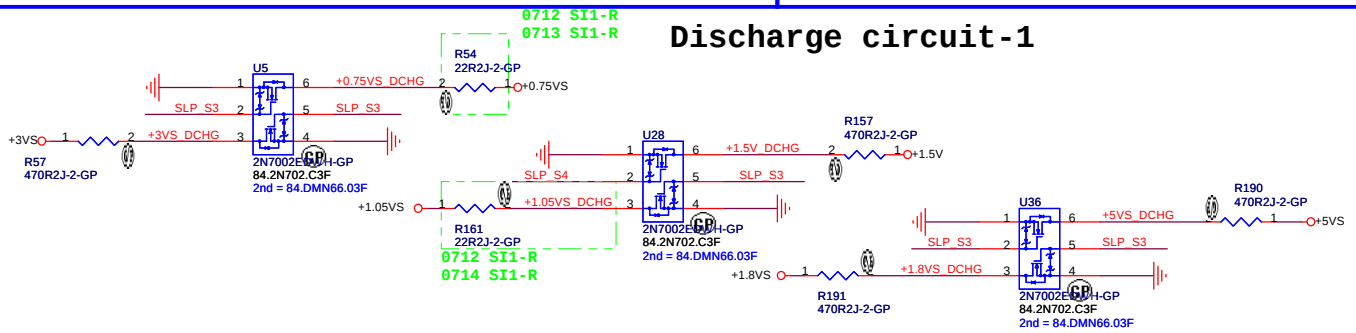
+5VALW to +5VS Transfer

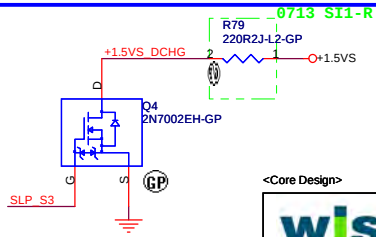






Discharge circuit-1





<Core Design>

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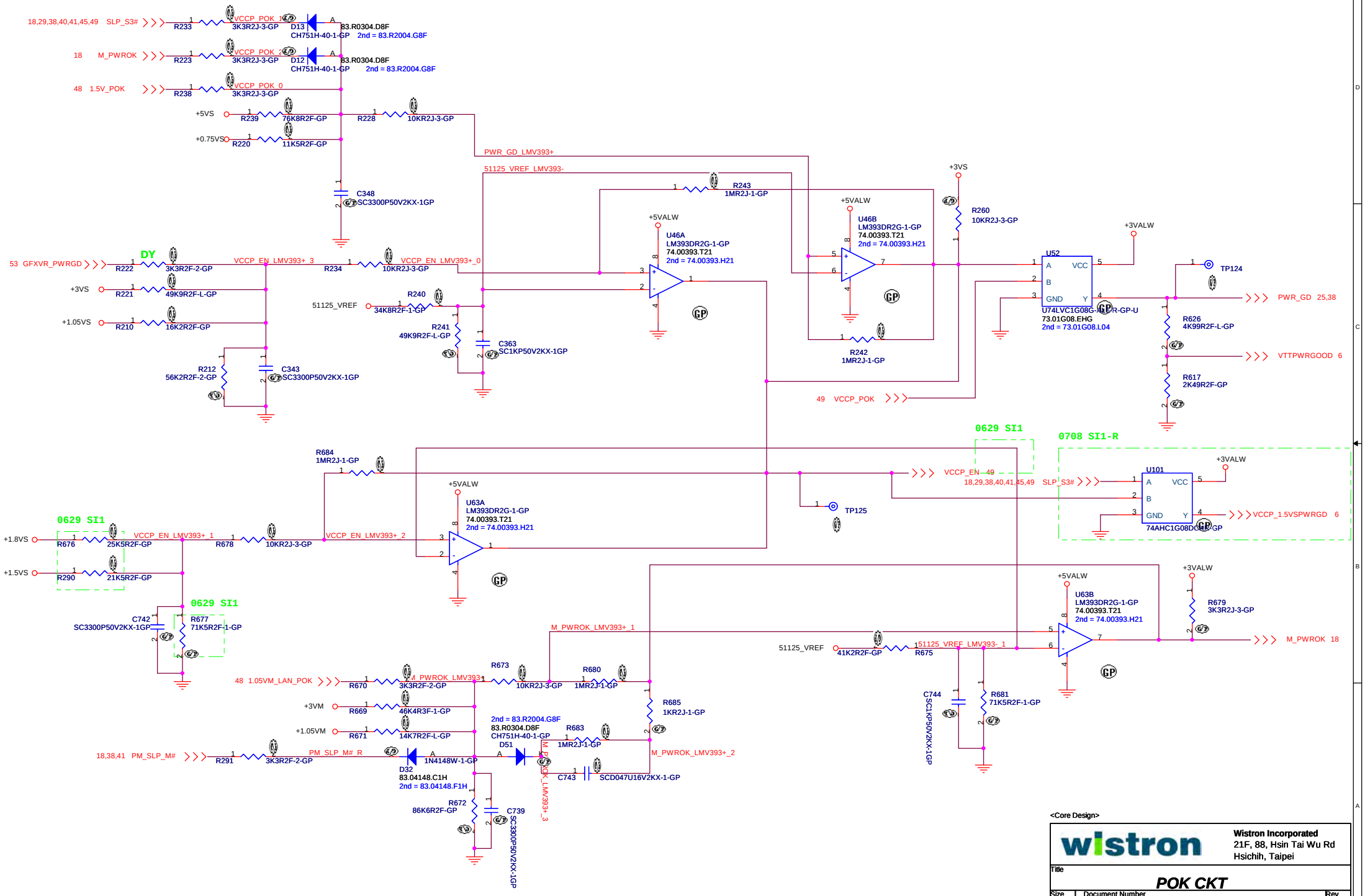
Hsichih, Taipei

Title: DC/DC Circuit

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 41 of 57



<Core Design>

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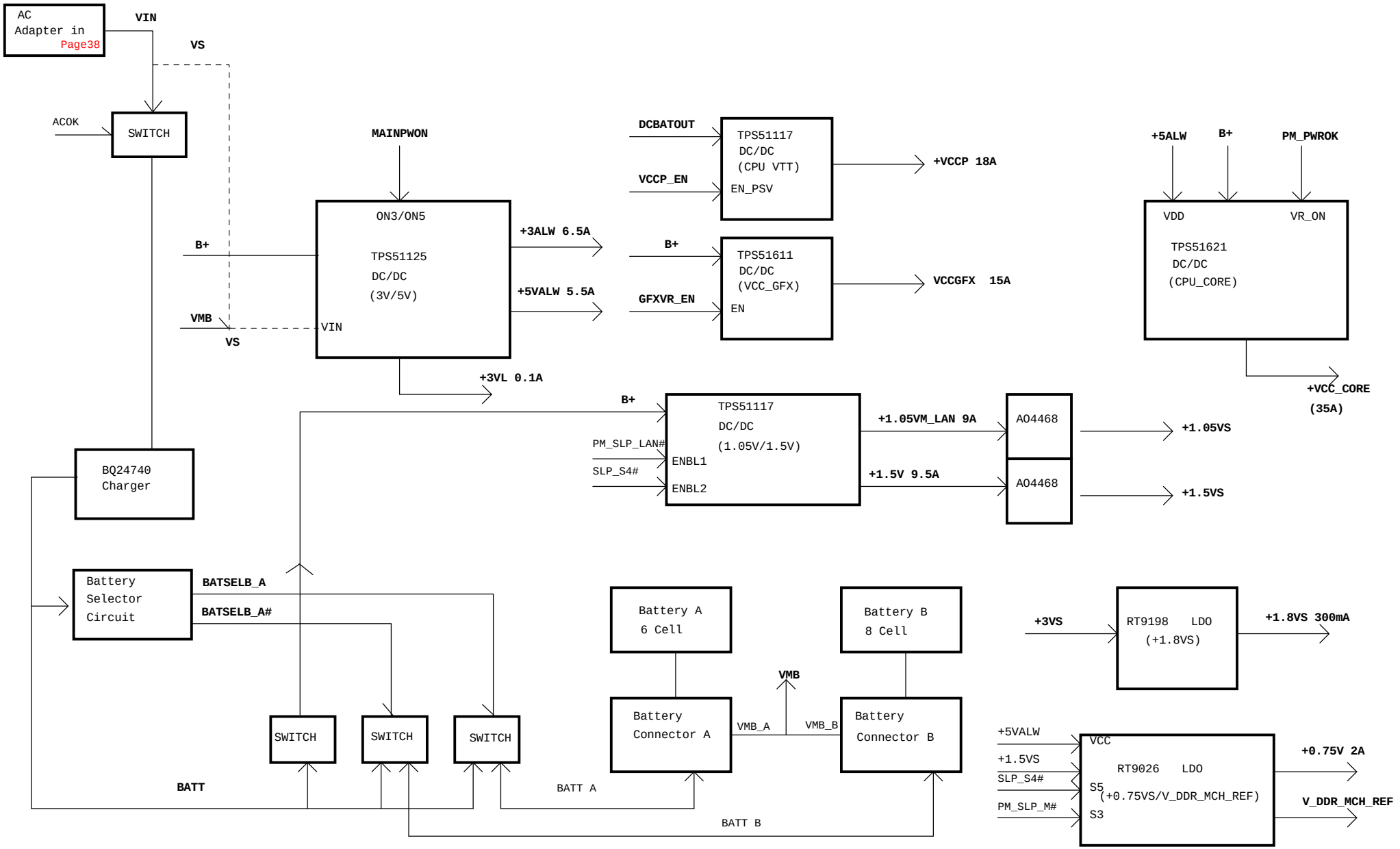
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: POK CKT

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 42 of 57



<Core Design>

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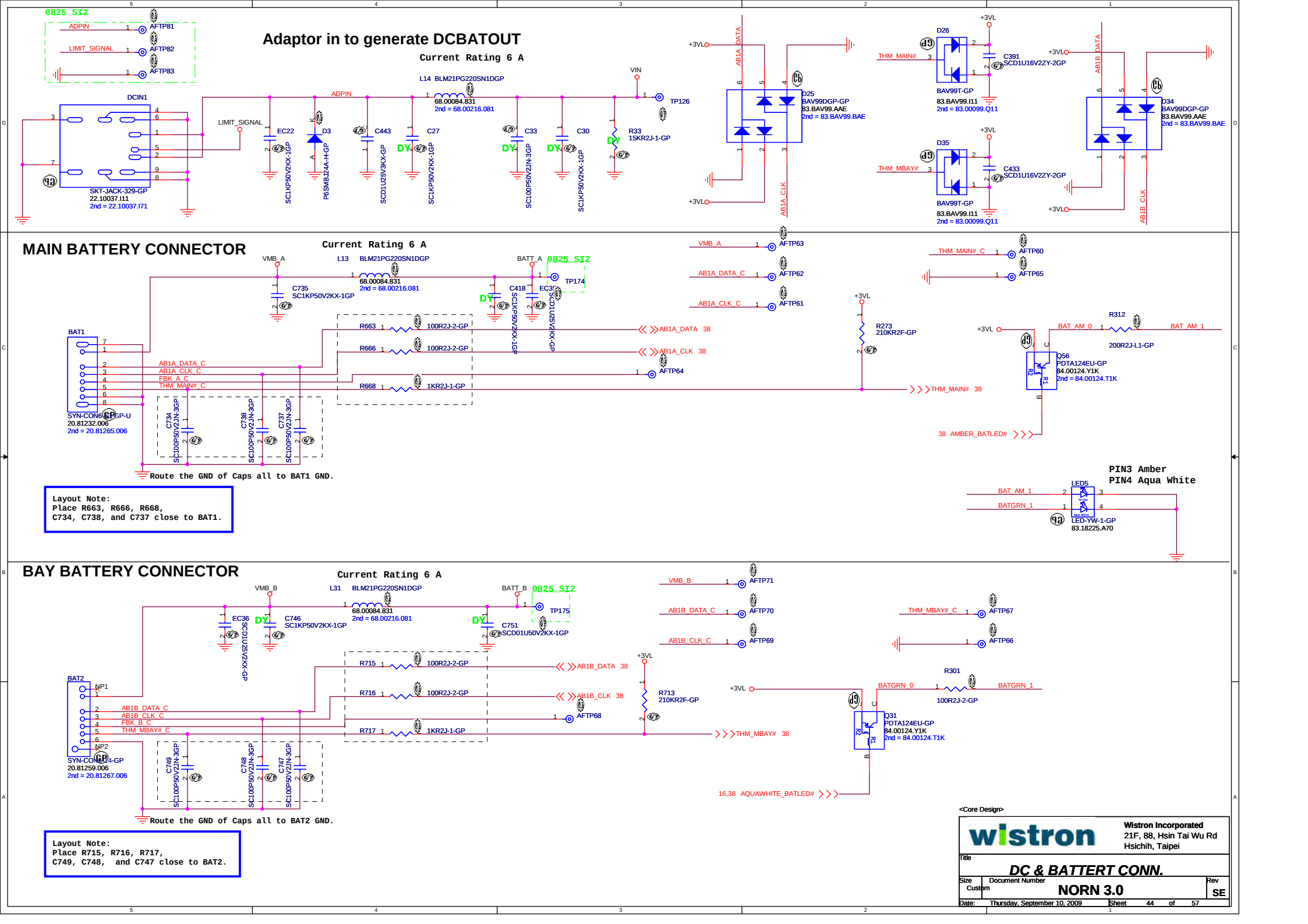
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

Power Block Diagram

Size	Document Number	Rev
A3	NORN 3.0	SE

Date: Monday, August 17, 2009 Sheet 43 of 57


0825_SI2
ADPIN
LIMIT_SIGNAL
AFTP81
AFTP82
AFTP83
Adaptor in to generate DCBATOUT
Current Rating 6 A
DCIN1
SKT-JACK-329-GP
22.10037.I11
2nd = 22.10037.I71
LIMIT_SIGNAL
EC22
SC1KP50V2KX-1GP
D3
P6SMBJ24A-H-GP
ADPIN
C443
SCD1U25V3KX-GP
C27
DY
SC1KP50V2KX-1GP
L14 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
C33
DY
SC100P50V2JN-3GP
C30
DY
SC1KP50V2KX-1GP
VIN
R33
15KR2J-1-GP
DY
TP126
+3VLO
AB1A_DATA
AB1A_CLK
D25
BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
D26
THM_MAIN#
BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
C391
SCD1U16V2ZY-2GP
+3VL
D35
THM_MBAY#
C433
SCD1U16V2ZY-2GP
AB1B_DATA
AB1B_CLK
D34
BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
MAIN BATTERY CONNECTOR
Current Rating 6 A
VMB_A
L13 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
C735
SC1KP50V2KX-1GP
BATT_A
0825_SI2
TP174
C418
DY
SC1KP50V2KX-1GP
EC35
SCD1U25V2KX-GP
VMB_A
AB1A_DATA_C
AB1A_CLK_C
AFTP63
AFTP62
AFTP61
THM_MAIN# C
AFTP60
AFTP65
BAT1
SYN-CON6-GP-U
20.81232.006
2nd = 20.81265.006
AB1A_DATA_C
AB1A_CLK_C
FBK_A_C
THM_MAIN# C
R663
100R2J-2-GP
R666
100R2J-2-GP
R668
1KR2J-1-GP
AB1A_DATA 38
AB1A_CLK 38
AFTP64
C734
C738
C737
SC100P50V2JN-3GP
Route the GND of Caps all to BAT1 GND.
R273
210KR2F-GP
THM_MAIN# 38
R312
BAT_AM_0
BAT_AM_1
200R2J-L1-GP
Q56
PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
38 AMBER_BATLED#
Layout Note:
Place R663, R666, R668,
C734, C738, and C737 close to BAT1.
PIN3 Amber
PIN4 Aqua White
LED5
BAT_AM_1
BATGRN_1
LED-YW-1-GP
83.18225.A70
BAY BATTERY CONNECTOR
Current Rating 6 A
VMB_B
L31 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
EC36
SCD1U25V2KX-GP
C746
DY
SC1KP50V2KX-1GP
BATT_B
0825_SI2
TP175
C751
DY
SCD01U50V2KX-1GP
VMB_B
AB1B_DATA_C
AB1B_CLK_C
AFTP71
AFTP70
AFTP69
THM_MBAY# C
AFTP67
AFTP66
BAT2
SYN-CON4-GP
20.81259.006
2nd = 20.81267.006
AB1B_DATA_C
AB1B_CLK_C
FBK_B_C
THM_MBAY# C
R715
100R2J-2-GP
R716
100R2J-2-GP
R717
1KR2J-1-GP
AB1B_DATA 38
AB1B_CLK 38
AFTP68
C749
C748
C747
SC100P50V2JN-3GP
Route the GND of Caps all to BAT2 GND.
R713
210KR2F-GP
THM_MBAY# 38
R301
BATGRN_0
BATGRN_1
100R2J-2-GP
Q31
PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
16,38 AQUAWHITE_BATLED#
Layout Note:
Place R715, R716, R717,
C749, C748, and C747 close to BAT2.
<Core Design>
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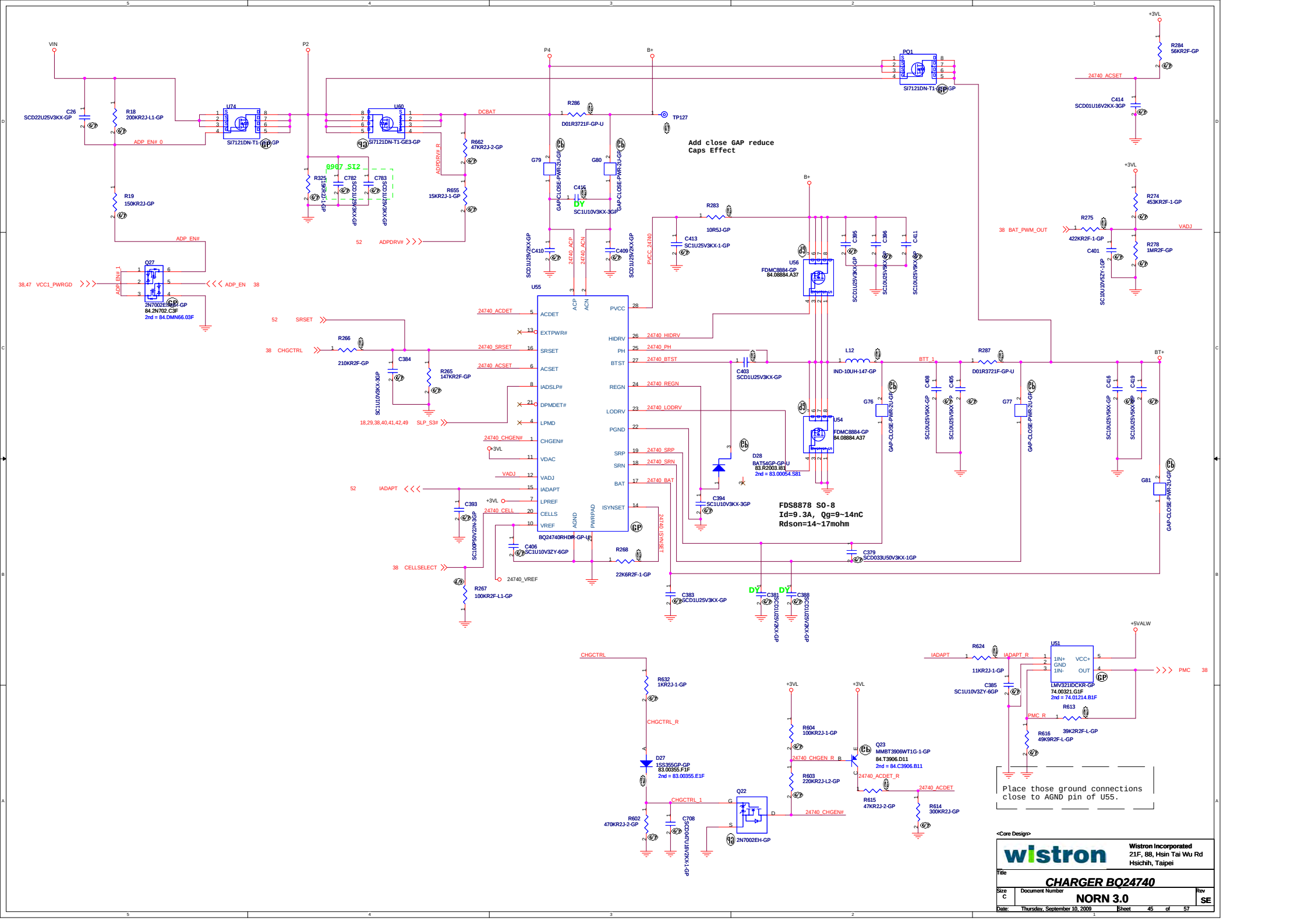
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
DC & BATTERT CONN.
Size
Custom
Document Number
NORN 3.0
Rev
SE
Date: Thursday, September 10, 2009
Sheet 44 of 57


VIN
P2
P4
B+
DCBAT
ADP_EN# 0
ADP_EN#
ADP_EN
38,47 VCC1_PWRGD
52 ADPDRV#
52 SRSET
38 CHGCTRL
18,29,38,40,41,42,49 SLP_S3#
52 IADAPT
38 CELLSELECT
24740_VREF
U55
BQ24740RHDR-GP-U5
FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm
Add close GAP reduce
Caps Effect
0907 SI2
+3VL
+5VALW
BT+
38 BAT_PWM_OUT
VADJ
PMC 38
CHGCTRL
CHGCTRL_R
CHGCTRL_1
24740_CHGEN_R
24740_CHGEN#
24740_ACDET_R
24740_ACDET
IADAPT_R
PMC_R
Place those ground connections
close to AGND pin of U55.
<Core Design>
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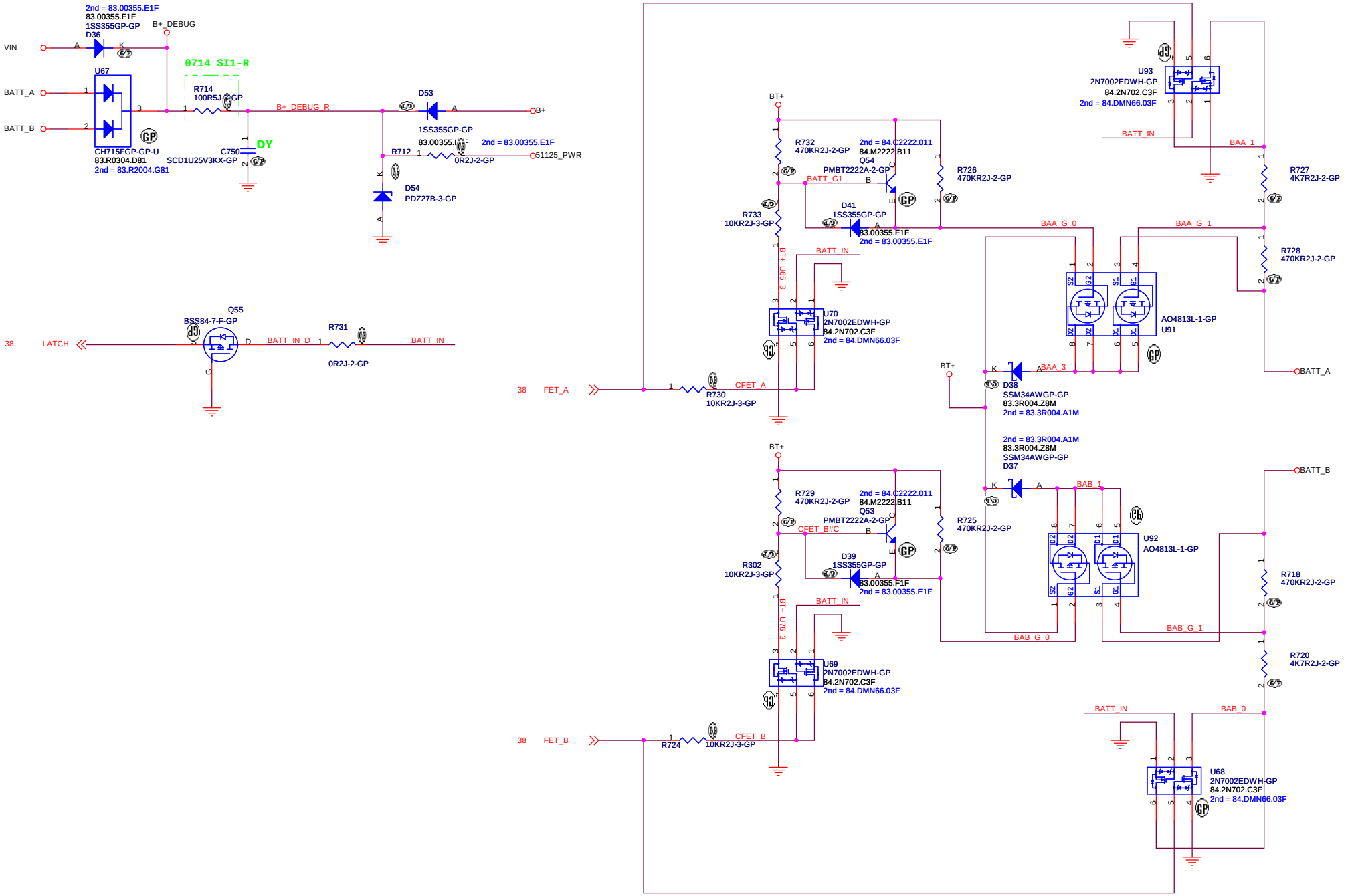
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CHARGER BQ24740
Size C
Document Number
NORN 3.0
Rev SE
Date: Thursday, September 10, 2009
Sheet 45 of 57



<Core Design>

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Hsichih, Taipei

Title

Battery Selector

Size	Document Number	Rev
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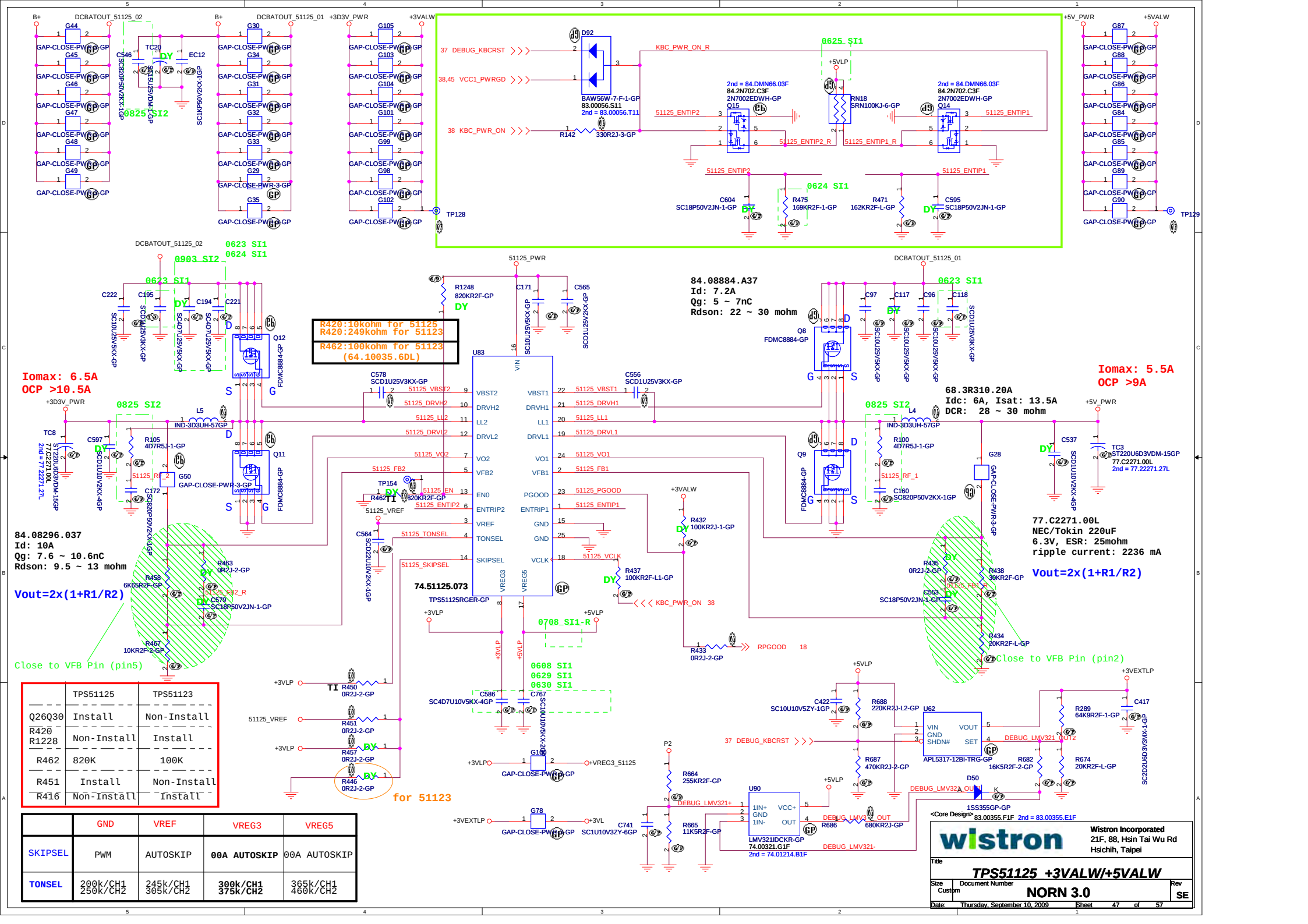
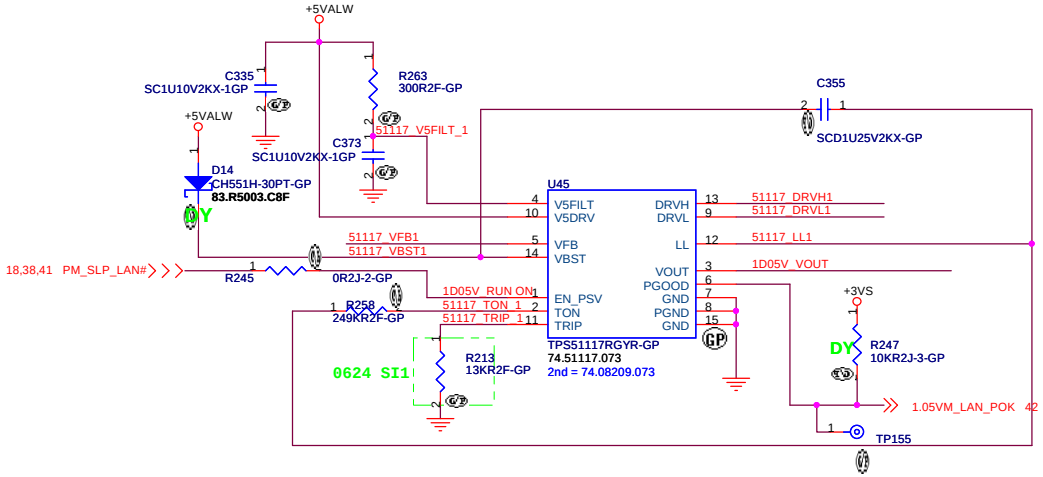
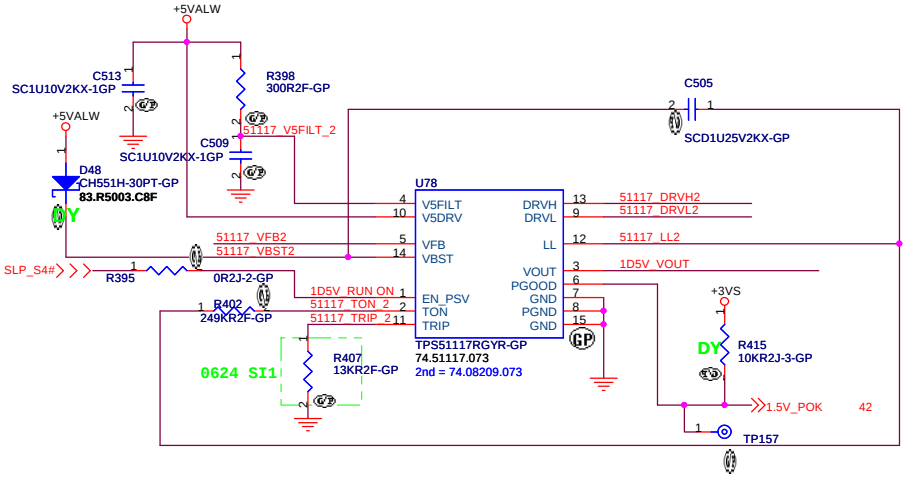
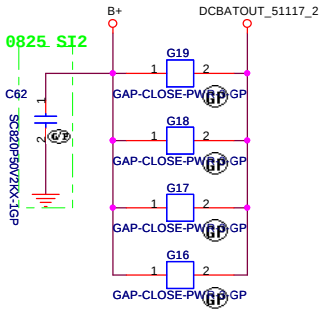


	TPS51125	TPS51123
Q26Q30	Install	Non-Install
R420 R1228	Non-Install	Install
R462	820K	100K
R451 R416	Install Non-Install	Non-Install Install

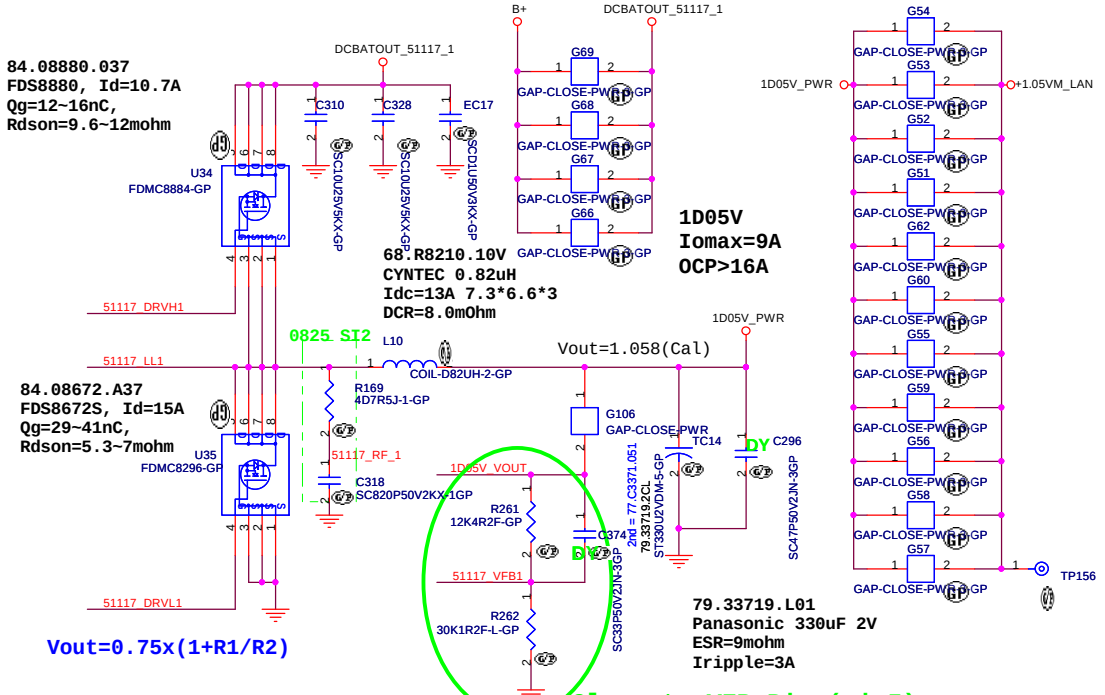
	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1** **375k/CH2**	365k/CH1 460k/CH2

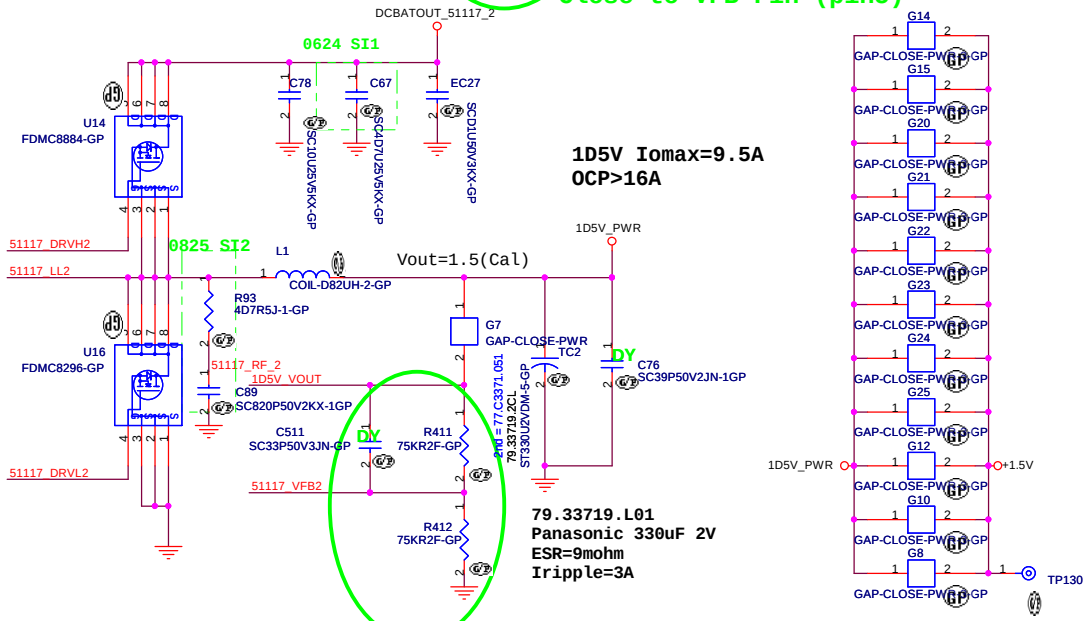






	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2





<Core Design>
wistron
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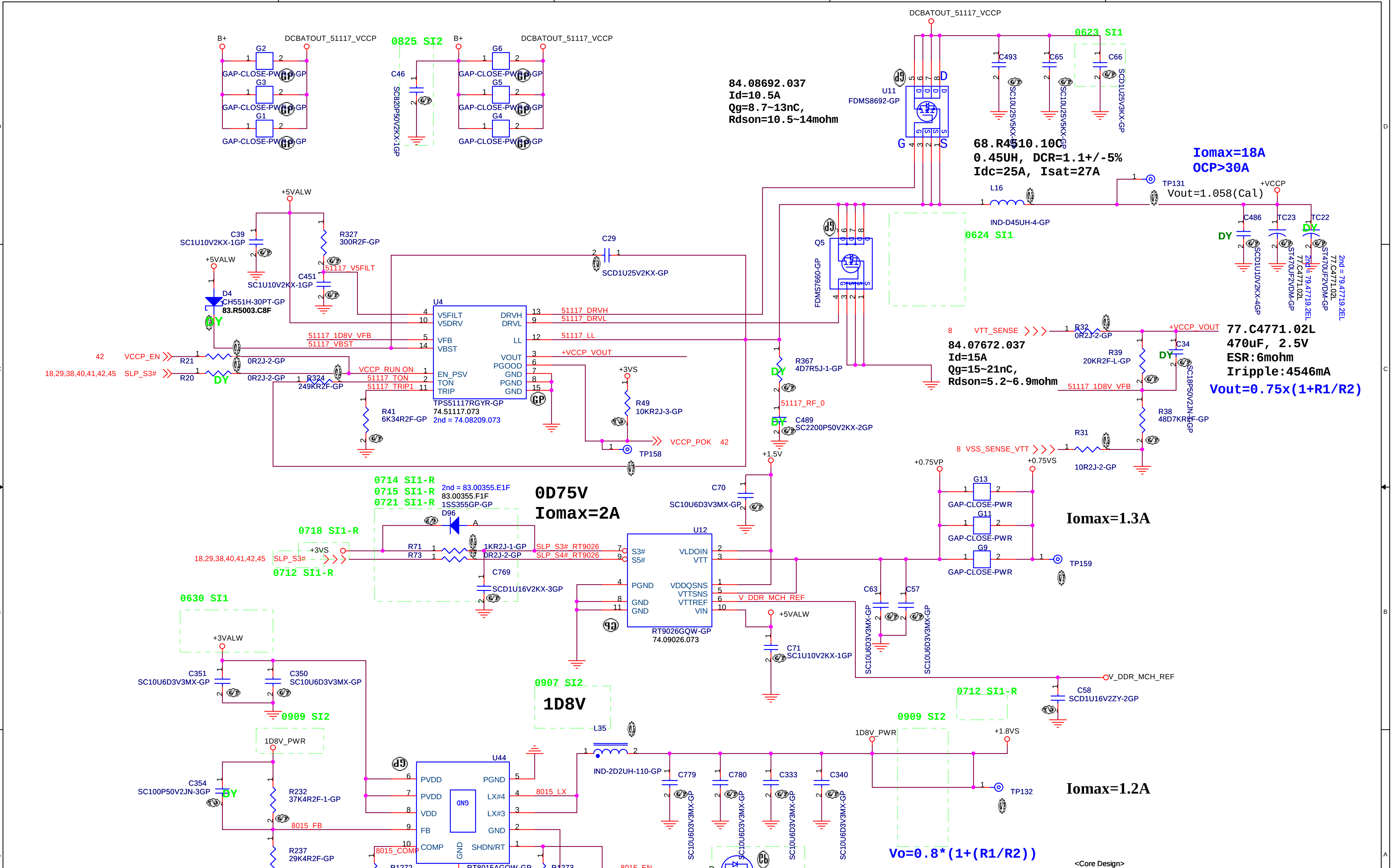
Hsichih, Taipei

Title: TPS51117_+1.05VM_LAN / +1.5V

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 48 of 57



DCBATOUT_51117_VCCP
B+
G2
G3
G1
GAP-CLOSE-PWR-GP
0825 SI2
C46
SC820P50V2KX-1GP
G6
G5
G4
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
U11
FDMS8692-GP
C493
C65
C66
0623 SI1
SC1U25V3KX-GP
SC10U25V5KX-GP
68.R4510.10C
0.45UH, DCR=1.1+/-5%
Idc=25A, Isat=27A
Iomax=18A
OCP>30A
TP131
Vout=1.058(Cal)
+VCCP
L16
IND-D45UH-4-GP
0624 SI1
C486
TC23
TC22
SCD1U10V2KX-4GP
ST470UF2VDM-GP
77.C4771.02L
2nd = 79.47719.2EL
+5VALW
C39
SC1U10V2KX-1GP
R327
300R2F-GP
C451
51117_V5FILT
C29
SCD1U25V2KX-GP
Q5
FDMS7660-GP
D4
CH551H-30PT-GP
83.R5003.C8F
DY
U4
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
TPS51117RGYR-GP
74.51117.073
2nd = 74.08209.073
51117_DRVH
51117_DRVL
51117_LL
+VCCP_VOUT
51117_1D8V_VFB
51117_VBST
VCCP_EN
R21
0R2J-2-GP
SLP_S3#
R20
R324
249KR2F-GP
VCCP_RUN ON
51117_TON
51117_TRIP1
R41
6K34R2F-GP
+3VS
R49
10KR2J-3-GP
VCCP_POK
TP158
R367
4D7R5J-1-GP
51117_RF_0
C489
SC2200P50V2KX-2GP
84.07672.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
VTT_SENSE
R32
0R2J-2-GP
+VCCP_VOUT
R39
20KR2F-L-GP
C34
SC18P50V2JN-GP
R38
48D7KR2F-GP
R31
10R2J-2-GP
VSS_SENSE_VTT
77.C4771.02L
470uF, 2.5V
ESR:6mohm
Iripple:4546mA
Vout=0.75x(1+R1/R2)
+1.5V
C70
SC10U6D3V3MX-GP
+0.75VP
+0.75VS
G13
G11
G9
GAP-CLOSE-PWR
TP159
Iomax=1.3A
0714 SI1-R
0715 SI1-R
0721 SI1-R
2nd = 83.00355.E1F
83.00355.F1F
1SS355GP-GP
D96
0D75V
Iomax=2A
0718 SI1-R
R71
R73
1KR2J-1-GP
0R2J-2-GP
SLP_S3#_RT9026
SLP_S4#_RT9026
0712 SI1-R
C769
SCD1U16V2KX-3GP
U12
S3#
S5#
VLDOIN
VTT
PGND
GND
VDDQSNS
VTTSNS
VTTREF
VIN
RT9026GQW-GP
74.09026.073
V_DDR_MCH_REF
C63
C57
SC10U6D3V3MX-GP
C71
SC1U10V2KX-1GP
C58
SCD1U16V2ZY-2GP
0630 SI1
+3VALW
C351
C350
SC10U6D3V3MX-GP
0909 SI2
0907 SI2
1D8V
L35
IND-2D2UH-110-GP
1D8V_PWR
+1.8VS
C779
C780
C333
C340
TP132
Iomax=1.2A
C354
SC100P50V2JN-3GP
R232
37K4R2F-1-GP
R237
29K4R2F-GP
8015_FB
U44
PVDD
VDD
FB
COMP
PGND
LX#4
LX#3
SHDN/RT
RT8015AGQW-GP
8015_LX
8015_COMP
R1272
30KR2F-GP
COMP_RC
C781
SC820P50V2KX-1GP
R1273
820KR2F-GP
8015_EN
Q87
BSS84-7-F-GP
0910 SI2
R1274
10KR2J-3-GP
Vo=0.8*(1+(R1/R2))

<Core Design>

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Hsichih, Taipei

Title: TPS51117_+VCCP/RT9026_+0.75VS/RT8015_+1.8VS

Size	Document Number	Rev
A3	NORN 3.0	SE

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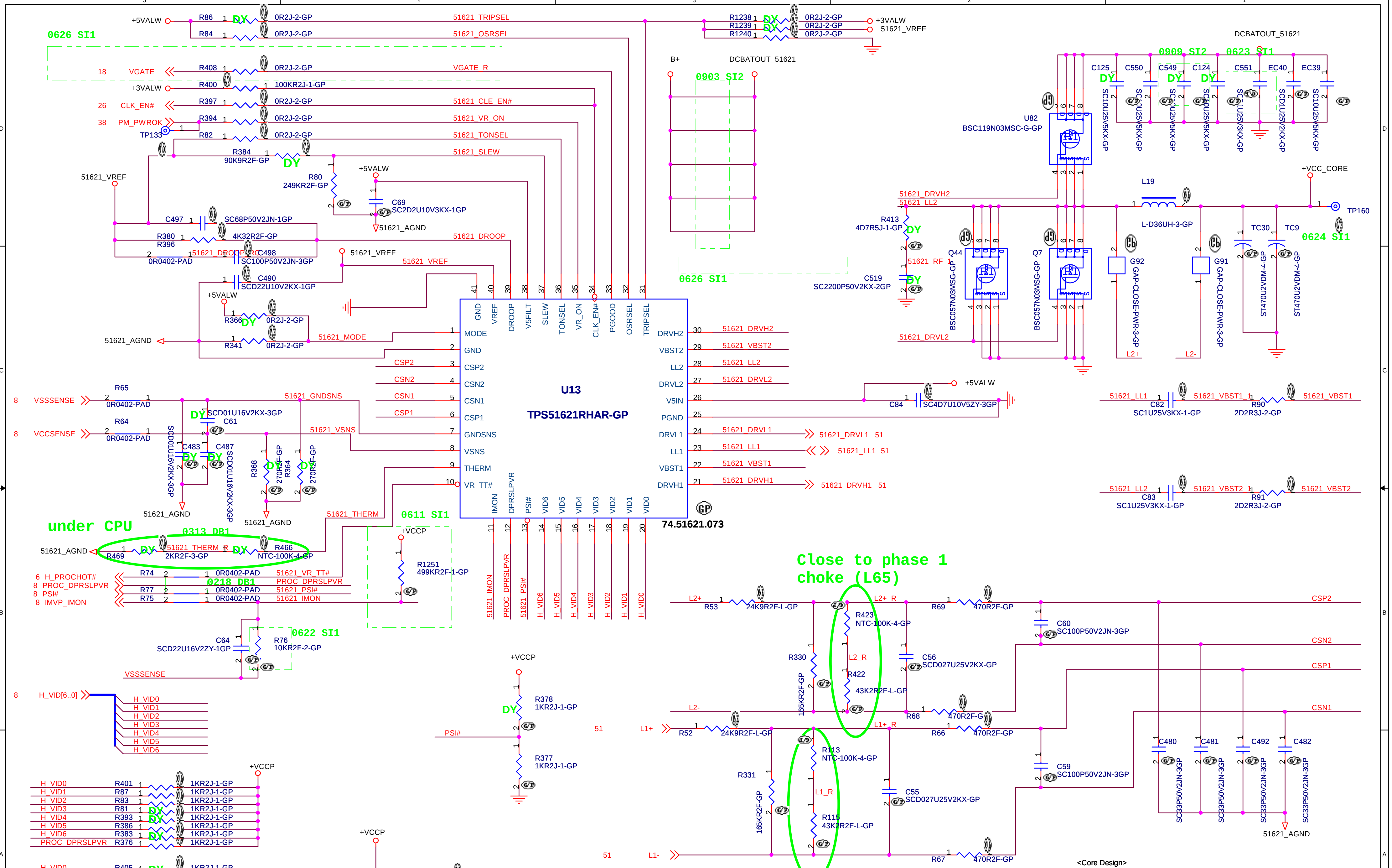

0626 SI1
0909 SI2
0623 SI1
0903 SI2
0624 SI1
0611 SI1
0313 DB1
0218 DB1
0622 SI1
under CPU
U13
TPS51621RHAR-GP
74.51621.073
MODE
GND
CSP2
CSN2
CSN1
CSP1
GNDSNS
VSNS
THERM
VR_TT#
VREF
DROOP
V5FILT
SLEW
TONSEL
VR_ON
CLK_EN#
PGOOD
OSRSEL
TRIPSEL
DRVH2
VBST2
LL2
DRVL2
V5IN
PGND
DRVL1
LL1
VBST1
DRVH1
IMON
DPRSLPVR
PSI#
VID6
VID5
VID4
VID3
VID2
VID1
VID0
51621_TRIPSEL
51621_OSRSEL
VGATE_R
51621_CLE_EN#
51621_VR_ON
51621_TONSEL
51621_SLEW
51621_DROOP
51621_VREF
51621_MODE
51621_GNDSNS
51621_VSNS
51621_THERM
51621_AGND
DCBATOUT_51621
+5VALW
+3VALW
+VCCP
+VCC_CORE
B+
18 VGATE
26 CLK_EN#
38 PM_PWROK
8 VSSSENSE
8 VCCSENSE
6 H_PROCHOT#
8 PROC_DPRSLPVR
8 PSI#
8 IMVP_IMON
8 H_VID[6..0]
U82 BSC119N03MSC-G-GP
Q44 BSC057N03MSG-GP
Q7 BSC057N03MSG-GP
L19 L-D36UH-3-GP
TP160
G92 GAP-CLOSE-PWR-3-GP
G91 GAP-CLOSE-PWR-3-GP
TC30 TC9 ST470U2VDM-4-GP
G82 GAP-CLOSE-PWR
51621_DRVL1 51
51621_LL1 51
51621_DRVH1 51
Close to phase 1 choke (L65)
Close to phase 2 choke (L67)
L2+
L2-
L1+
L1-
CSP2
CSN2
CSP1
CSN1
R53 24K9R2F-L-GP
R52 24K9R2F-L-GP
R423 NTC-100K-4-GP
R113 NTC-100K-4-GP
R422 43K2R2F-L-GP
R115 43K2R2F-L-GP
R330 165KR2F-GP
R331 165KR2F-GP
R69 470R2F-GP
R68 470R2F-GP
R66 470R2F-GP
R67 470R2F-GP
C60 SC100P50V2JN-3GP
C59 SC100P50V2JN-3GP
C56 SCD027U25V2KX-GP
C55 SCD027U25V2KX-GP
C480 C481 C492 C482 SC33P50V2JN-3GP
R378 1KR2J-1-GP
R377 1KR2J-1-GP
R70 68R2-GP
R1251 499KR2F-1-GP
R76 10KR2F-2-GP
C64 SCD22U16V2ZY-1GP
R469 2KR2F-3-GP
R466 NTC-100K-4-GP
C84 SC4D7U10V5ZY-3GP
C82 SC1U25V3KX-1-GP
C83 SC1U25V3KX-1-GP
R90 2D2R3J-2-GP
R91 2D2R3J-2-GP
R413 4D7R5J-1-GP
C519 SC2200P50V2KX-2GP
<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(1/2) TPS51621

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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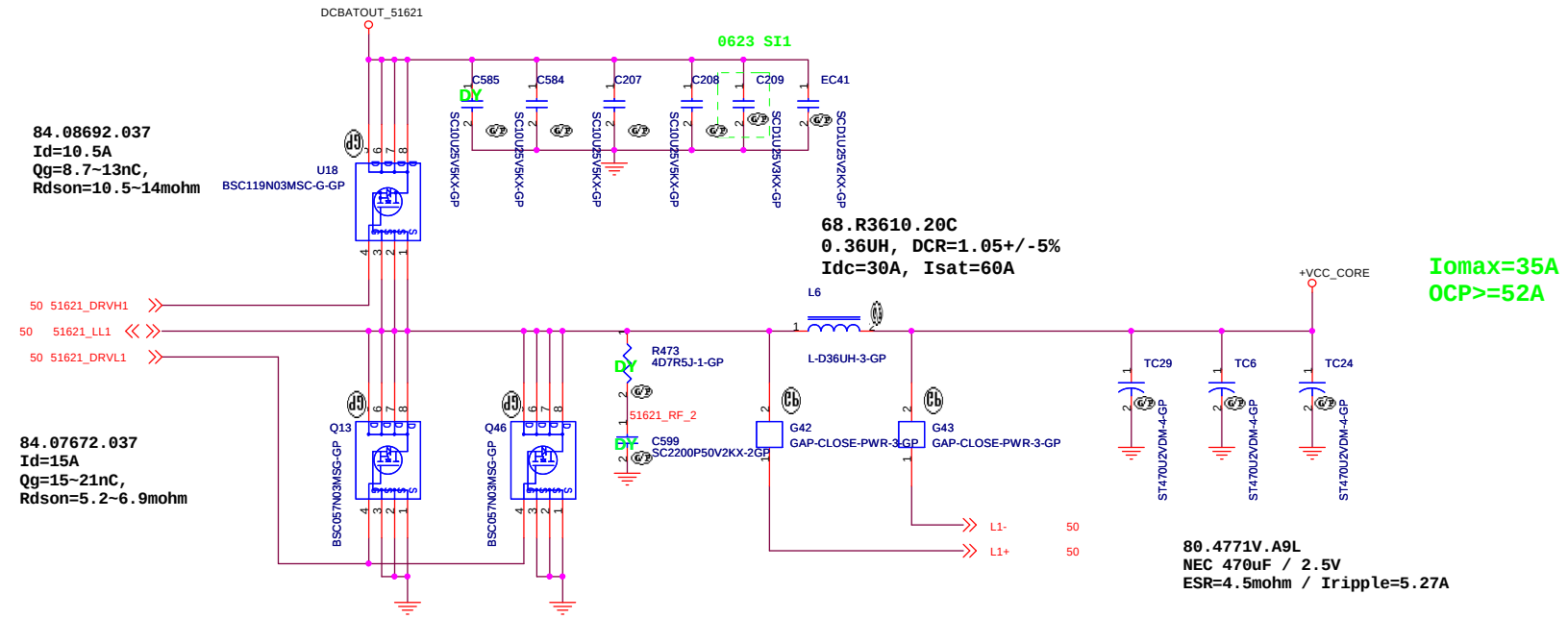

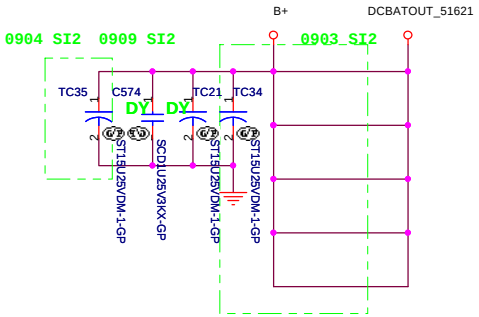

<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(2/2) TPS51621

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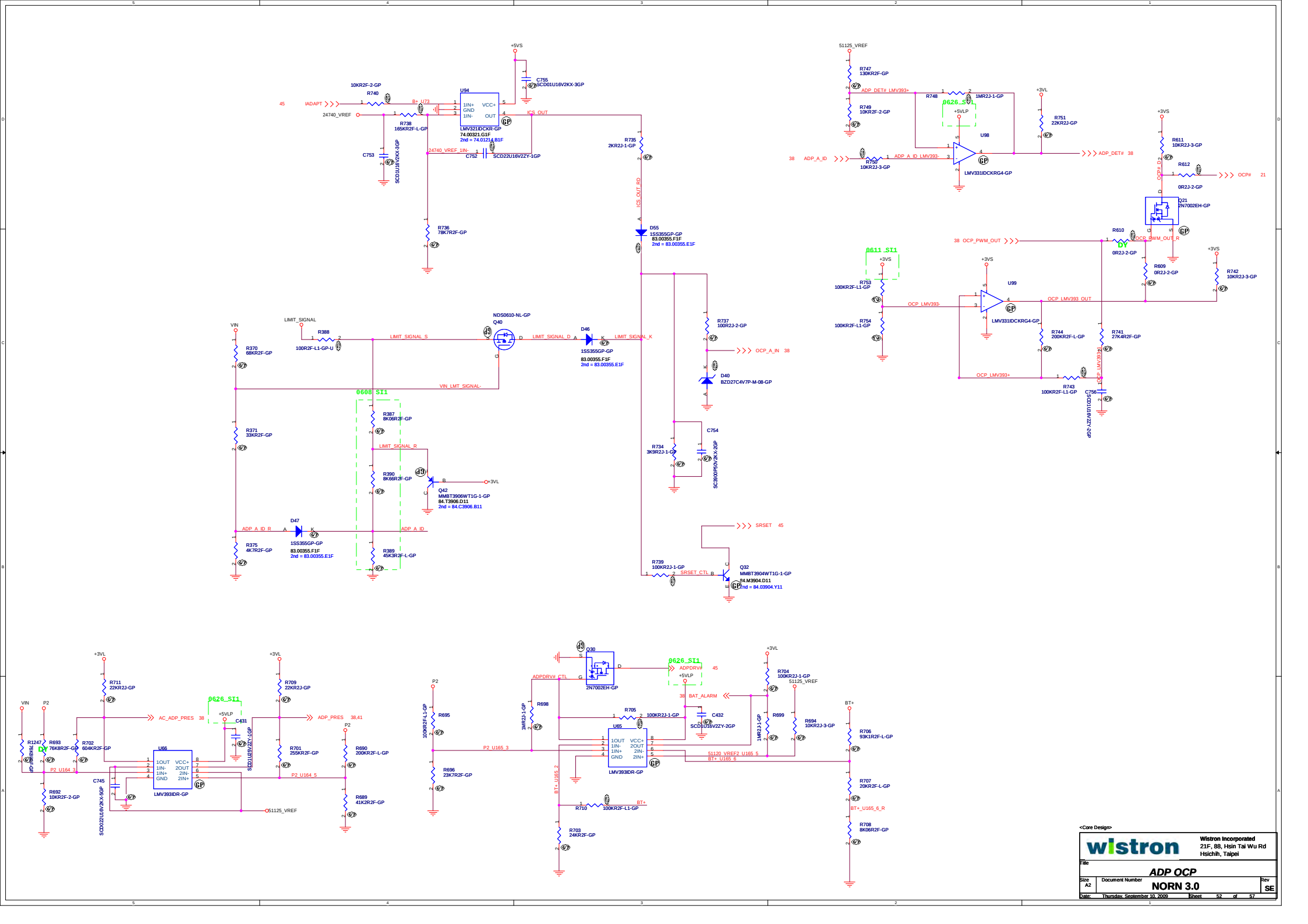
+5VS
C755
SCD01U16V2KX-3GP
10KR2F-2-GP
R740
45
IADAPT
24740_VREF
B+_U73
R738
165KR2F-L-GP
U94
1IN+
GND
1IN-
VCC+
OUT
LMV321IDCKR-GP
74.00321.G1F
2nd = 74.01214.B1F
ICS_OUT
C753
SCD1U16V2KX-3GP
24740_VREF_1IN-
C752
SCD22U16V2ZY-1GP
R735
2KR2J-1-GP
ICS_OUT_RD
R736
78K7R2F-GP
D55
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
51125_VREF
R747
130KR2F-GP
ADP_DET# LMV393+
R748
1MR2J-1-GP
0626_SI1
+5VLP
U98
R749
10KR2F-2-GP
+3VL
R751
22KR2J-GP
38
ADP_A_ID
R750
10KR2J-3-GP
ADP_A_ID LMV393-
LMV331IDCKRG4-GP
ADP_DET# 38
+3VS
R611
10KR2J-3-GP
OCP# 1/2
R612
OCP#
21
0R2J-2-GP
Q21
2N7002EH-GP
R610
OCP_PWM_OUT_R
38 OCP_PWM_OUT
DY
0R2J-2-GP
0611_SI1
R753
100KR2F-L1-GP
R754
100KR2F-L1-GP
OCP_LMV393-
U99
LMV331IDCKRG4-GP
OCP_LMV393_OUT
R609
0R2J-2-GP
R742
10KR2J-3-GP
R744
200KR2F-L-GP
R741
27K4R2F-GP
OCP_LMV393+
R743
100KR2F-L1-GP
C756
SCD1U16V2ZY-2GP
OCP_LMV393-
VIN
LIMIT_SIGNAL
R388
100R2F-L1-GP-U
LIMIT_SIGNAL_S
NDS0610-NL-GP
Q40
LIMIT_SIGNAL_D
D46
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
LIMIT_SIGNAL_K
R737
100R2J-2-GP
OCP_A_IN
38
R370
68KR2F-GP
VIN_LMT_SIGNAL-
D40
BZD27C4V7P-M-08-GP
0608_SI1
R387
8K06R2F-GP
R371
33KR2F-GP
LIMIT_SIGNAL_R
C754
R734
3K9R2J-1-GP
SC390DP50V2KX-3GP
R390
8K06R2F-GP
+3VL
Q42
MMBT3906WT1G-1-GP
84.T3906.D11
2nd = 84.C3906.B11
ADP_A_ID_R
D47
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
ADP_A_ID
R375
4K7R2F-GP
R389
45K3R2F-L-GP
SRSET
45
R739
100KR2J-1-GP
SRSET_CTL
Q32
MMBT3904WT1G-1-GP
84.M3904.D11
2nd = 84.03904.Y11
+3VL
R711
22KR2J-GP
R709
22KR2J-GP
0626_SI1
+5VLP
AC_ADP_PRES
38
ADP_PRES
38,41
C431
SCD1U25V2ZY-1GP
VIN
P2
R1247
10KR2J-1-GP
DY
R693
76KR2F-GP
R702
604KR2F-GP
P2_U164_3
U66
1OUT
1IN-
1IN+
GND
VCC+
2OUT
2IN-
2IN+
LMV393IDR-GP
R701
255KR2F-GP
P2_U164_5
R690
200KR2F-L-GP
R689
41K2R2F-GP
R692
10KR2F-2-GP
C745
SCD02U16V2KX-5GP
51125_VREF
P2
R695
10KR2F-L1-GP
R696
23K7R2F-GP
P2_U165_3
Q30
2N7002EH-GP
ADPDRV#_CTL
0626_SI1
ADPDRV#
45
+5VLP
38
BAT_ALARM
R698
1MR2J-1-GP
R705
100KR2J-1-GP
C432
SCD1U16V2ZY-2GP
U65
LMV393IDR-GP
R699
1MR2J-1-GP
R694
10KR2J-3-GP
51120_VREF2_U165_5
BT+_U165_6
BT+_U165_2
R710
100KR2F-L1-GP
BT+
R703
24KR2F-GP
+3VL
R704
100KR2J-1-GP
51125_VREF
BT+
R706
93K1R2F-L-GP
R707
20KR2F-L-GP
BT+_U165_6_R
R708
8K06R2F-GP
<Core Design>
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21F, 88, Hsin Tai Wu Rd
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Title
ADP OCP
Size
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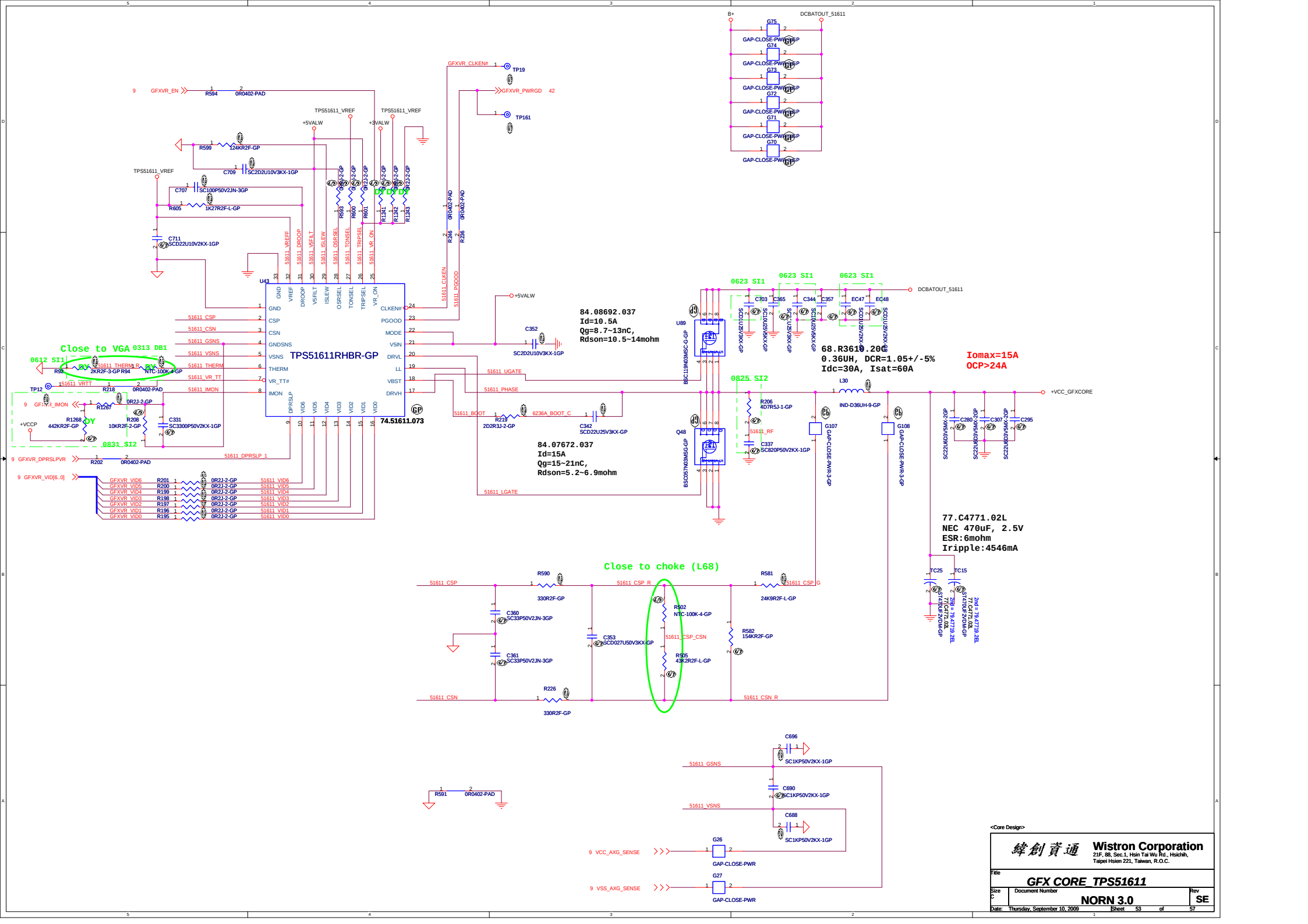

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Title: GFX CORE_TPS51611

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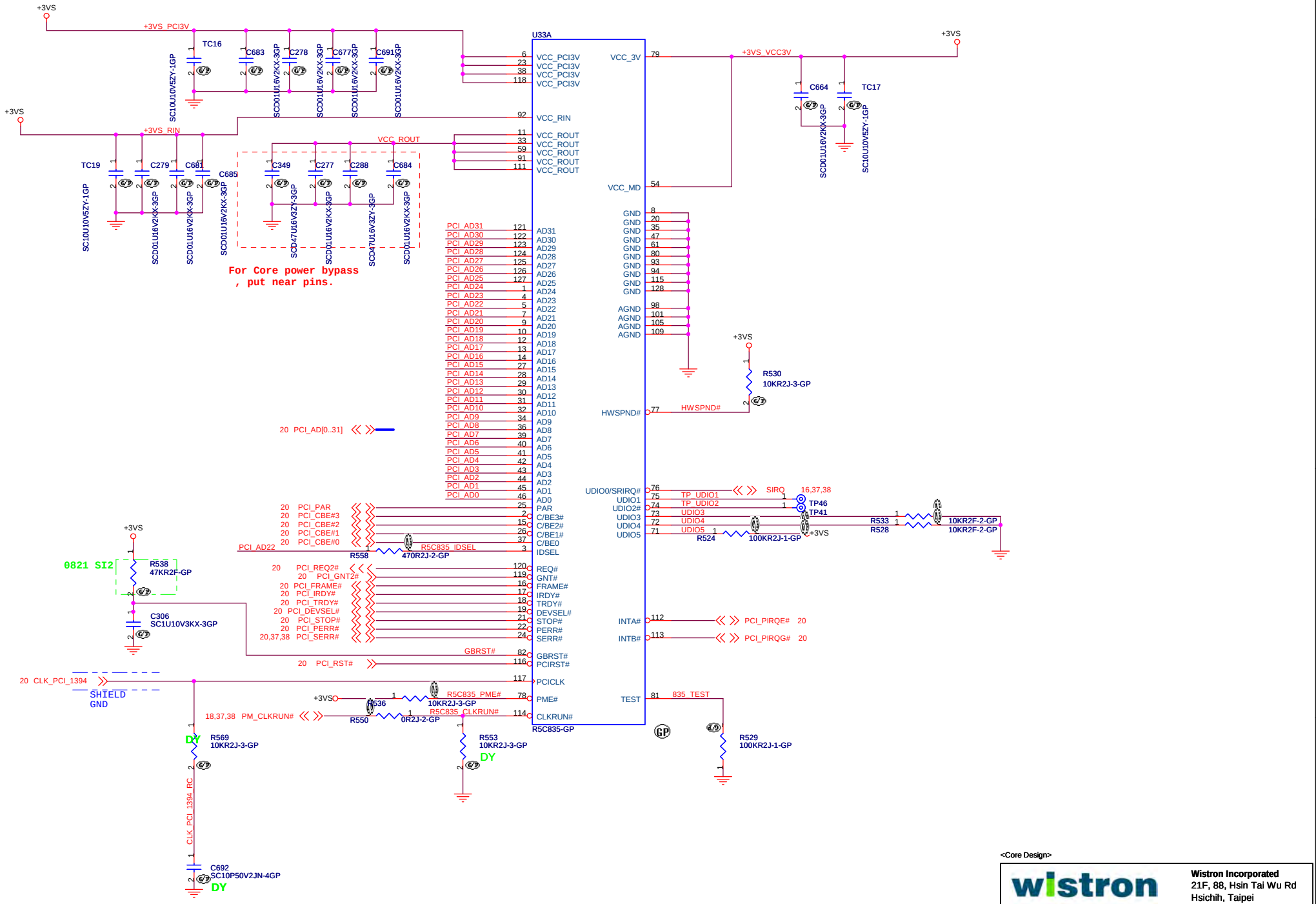
U33A
R5C835-GP
For Core power bypass , put near pins.
0821 SI2
SHIELD
GND
DY
20 CLK_PCI_1394
20 PCI_AD[0..31]
PCI_AD22
R5C835_IDSEL
R5C835_PME#
R5C835_CLKRUN#
18,37,38 PM_CLKRUN#
20 PCI_RST#
GBRST#
PCI_PIRQE# 20
PCI_PIRQG# 20
SIRQ 16,37,38
835_TEST
HWSPND#
CLK_PCI_1394_RC
<Core Design>
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
R5C835/PCI(1/2)
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Place C345 and C346, and X3 as close as possible.

Place R576 and C693 as close to R5C835 as possible.

Layout notes :
external parts for VREF, REXT and FIL0 as close as possible to R5C835.

Layout Notes:

Make sure that the stubs to the test points(1394_XO) in the layout are as short as possible on the high speed signals.

The shield GND is needed for SD_CLK(MDIO09). Also, the wide-width (more than 0.02inch) trace for MDIO09 should be used.

Place U41 within 2 inches of the card connector

40mil

For SD Card Power

Layout notes :
1394
GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND

CLOSE TO CHIP R5C835

SD_CLK need to 25mil

Place resistor close to CARD1

Layout Note: Add guard GND around SD_CLK
Change +3VS_CARD to 40mils

Please ensure that TPA+/- and TPB+/- are routed the same wire length.

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Title: R5C835/IEEE1394/SD/Smart(2/2)
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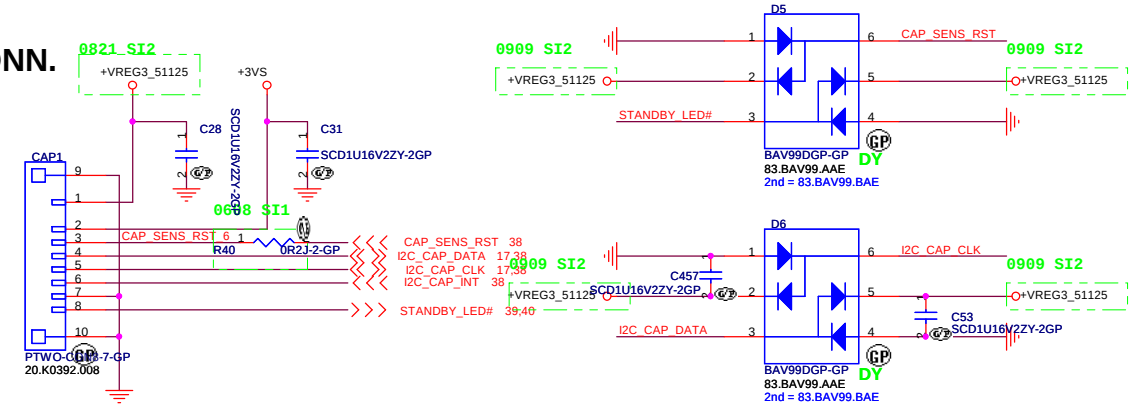
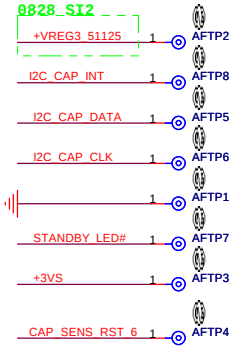
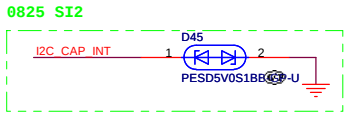
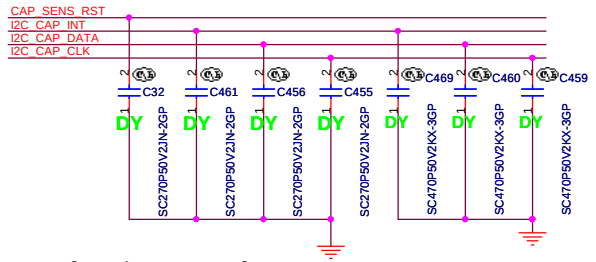
CAP BD CONN.





Vol up , Vol down , Mute ,Presentation





Place these 4 Caps close to CAP1.

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Title: CAP CONN.

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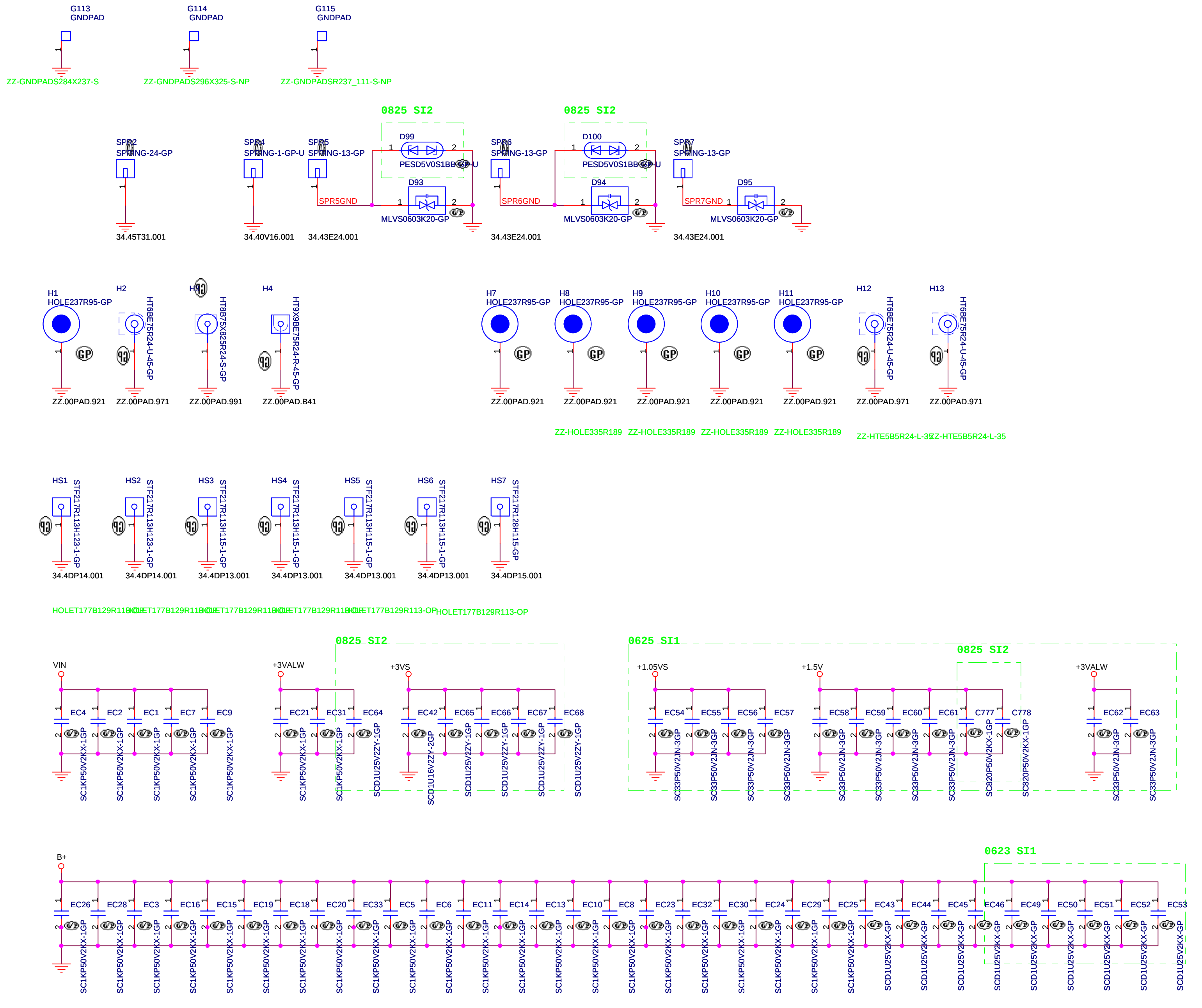

<Core Design>

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Title: **UNUSED PARTS/EMI Capacitors**

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