

Compal confidential

Schematics Document

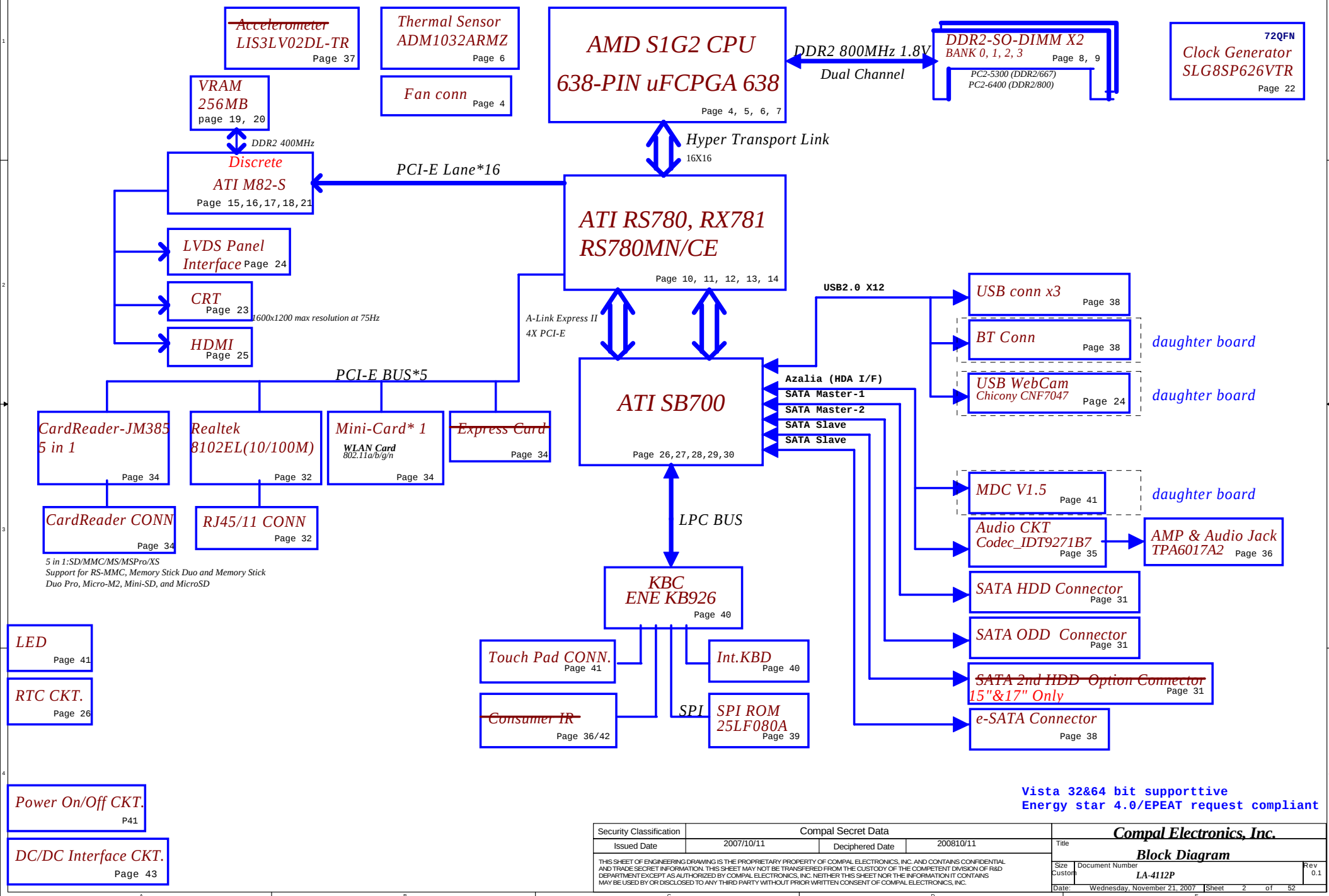
Mobile AMD S1G2 CPU with ATI
RX781(NB) & SB700(SB) core logic

2007-11-21

REV:0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc		
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OPP Rachman AMD 14" Discrete - LA-4112P



Vista 32&64 bit supporttve
Energy star 4.0/EPEAT request compliant

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Voltage Rails

0 MEANS ON X MEANS OFF

power plane State	+B +3VL +5VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_0 +CPU_CORE_1 +CPU_CORE_NB
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
ACCELEROMETER	3A	0 0 1 1 1 0 1 0

EC SM Bus1 address

EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	ADI1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b	ADI1032-1 VGA	98H	1001 100X b
CPU SIC interface	98H	1001 100X b			

SMBUS Control Table

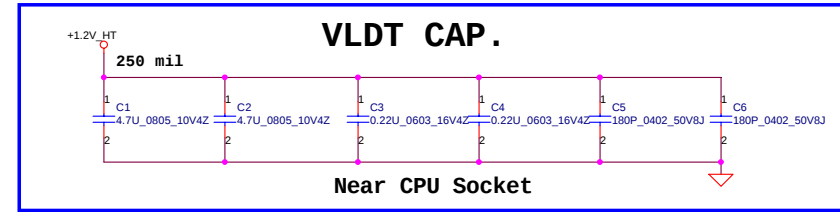
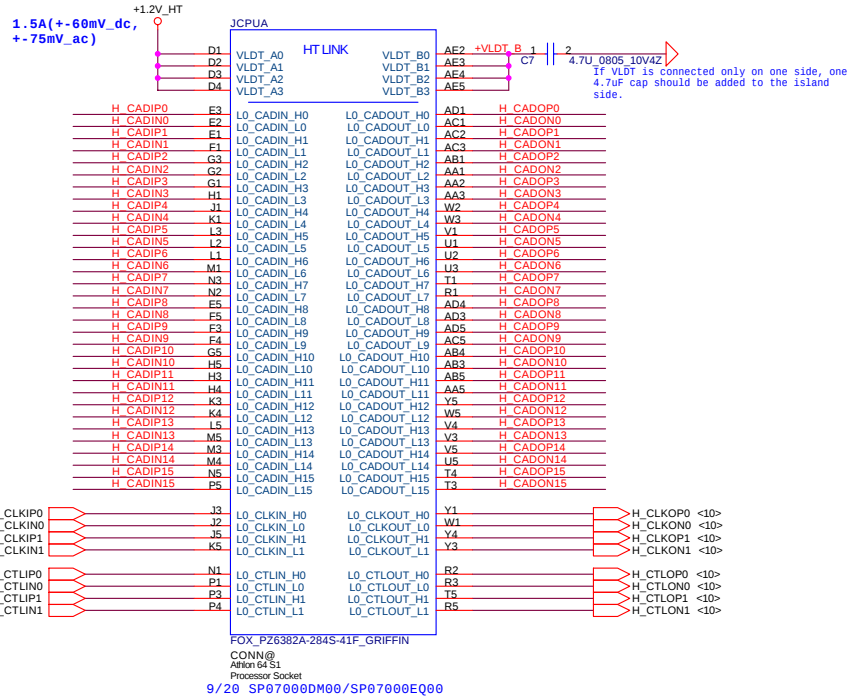
	SOURCE	THERMAL SENSOR VGA M82-SE ADM1032	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM 1 / 11	CLK CHIP	WL MINI_CARD Slot 1	LCD	HDMI	CRT	G-Sensor
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_CK2	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_DA2	KB926	V	X	X	V	X	X	X	X	X	X	X
SCL SDA	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
DDC4CLK DDC4DATA	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC3CLK DDC3DATA	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

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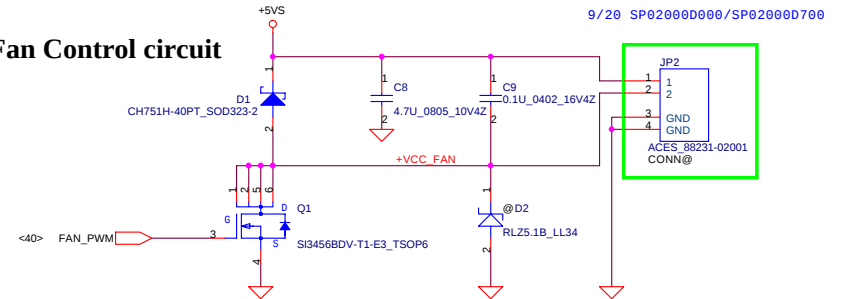
Notes List

<10> H_CADIP[0..15] H_CADIP[0..15]
<10> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <10>
H_CADON[0..15] H_CADON[0..15] <10>

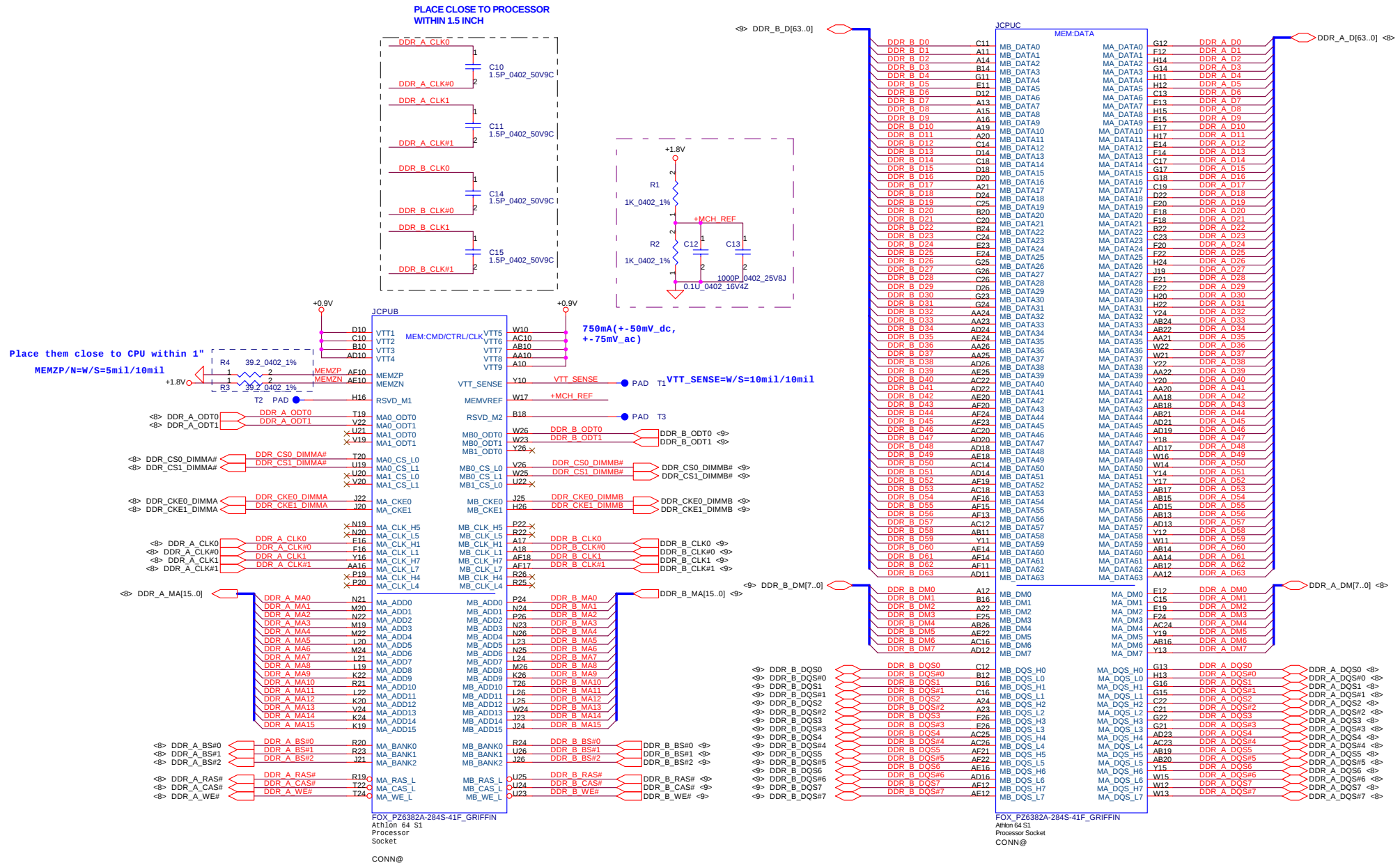


PWM Fan Control circuit

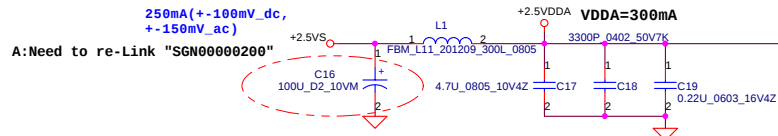


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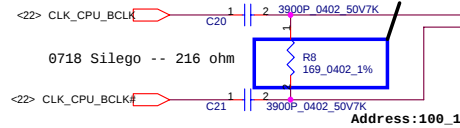
Processor DDR2 Memory Interface



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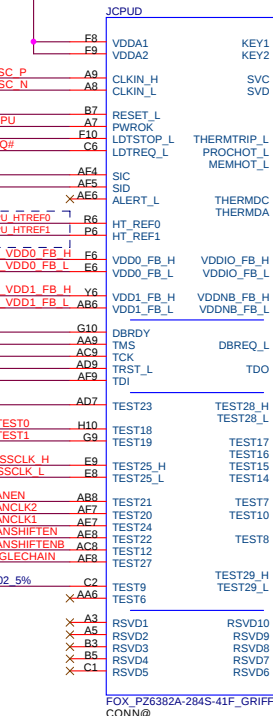
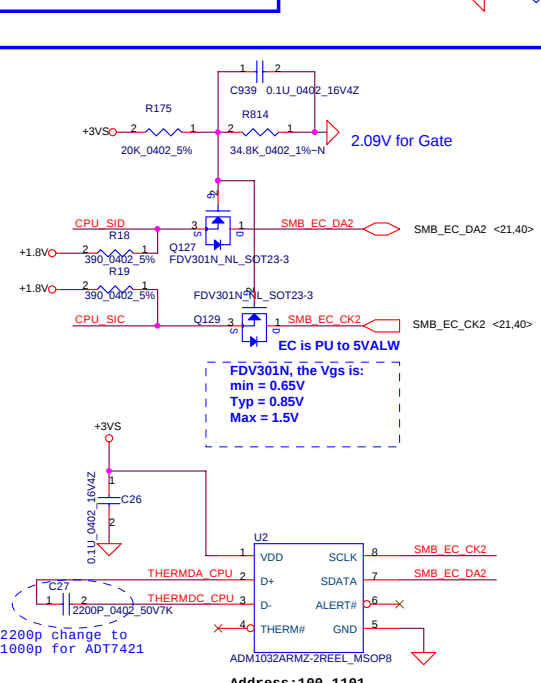
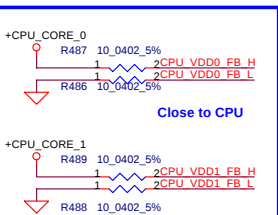
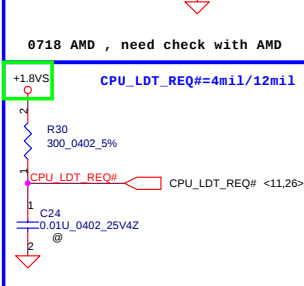
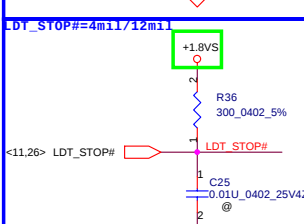
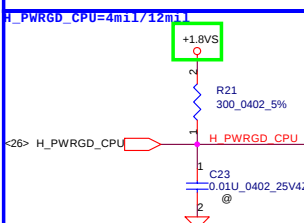
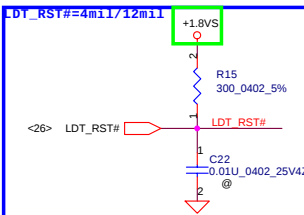
Place close to CPU with in 1.5"



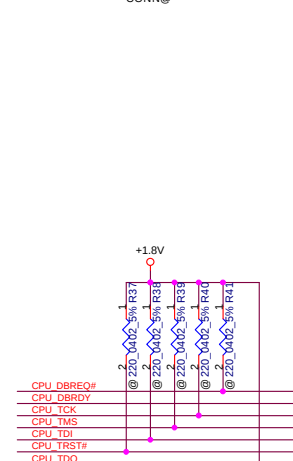
Address:100_1100

CPU_VDD0_FB_H/L(Differential pair)=10/5/5/5/10

CPU_VDD1_FB_H/L(Differential pair)=10/5/5/5/10

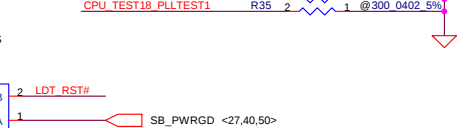
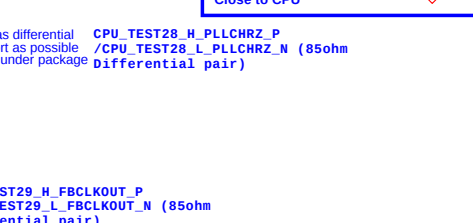
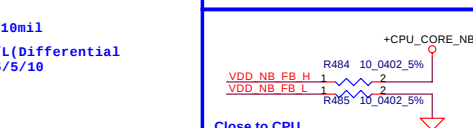
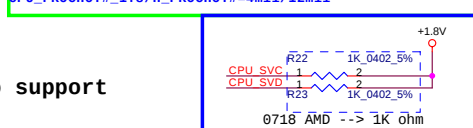
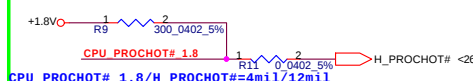
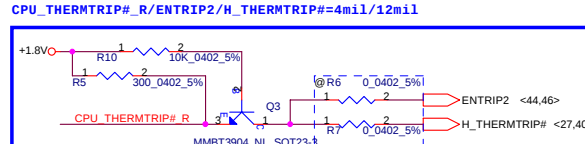
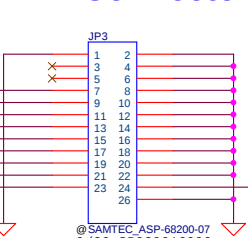


FOX_PZ6382A-284S-41F_GRIFFIN CONN@



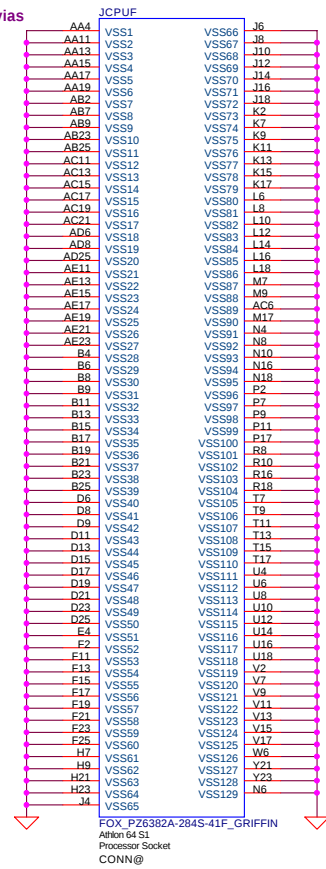
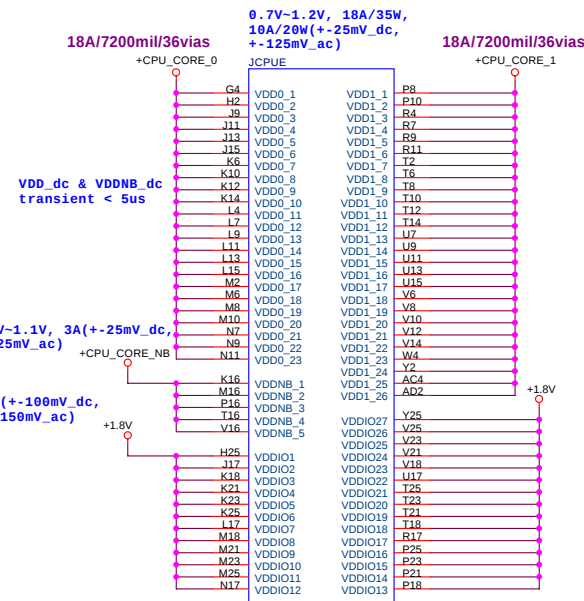
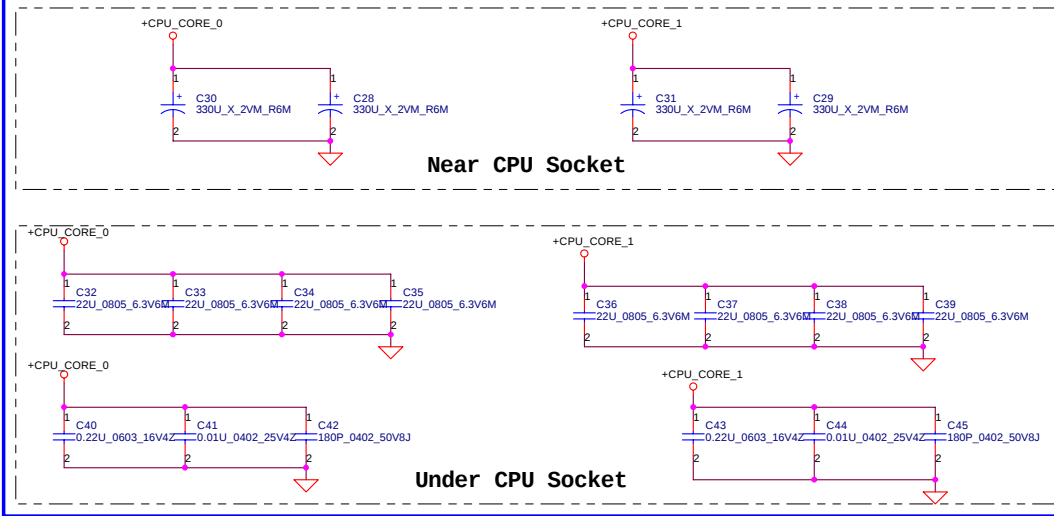
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

HDT Connector

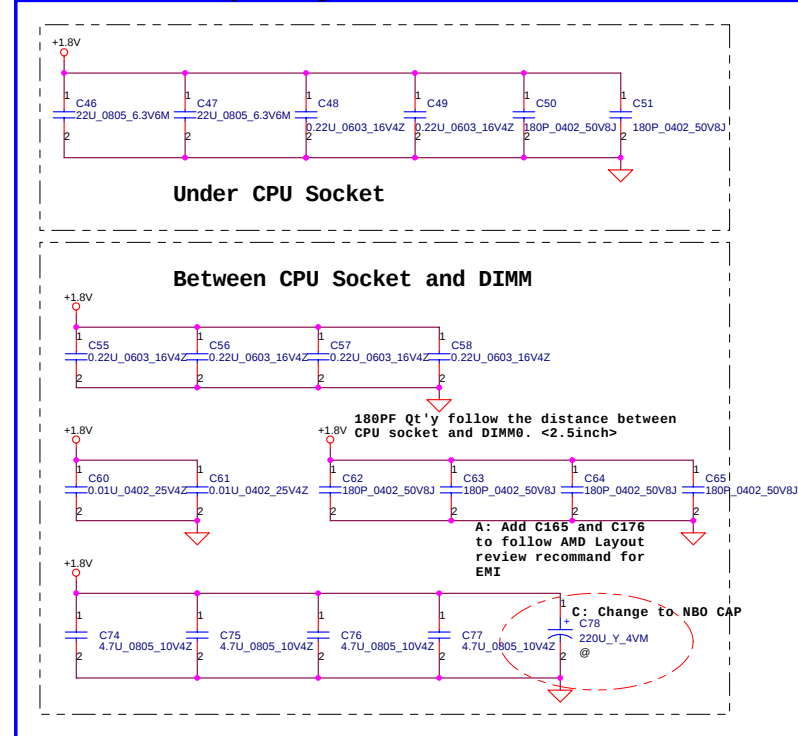


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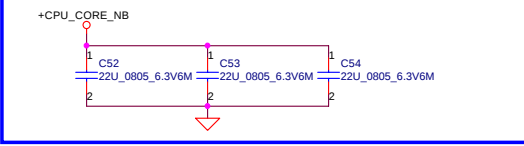
VDD(+CPU_CORE) decoupling.



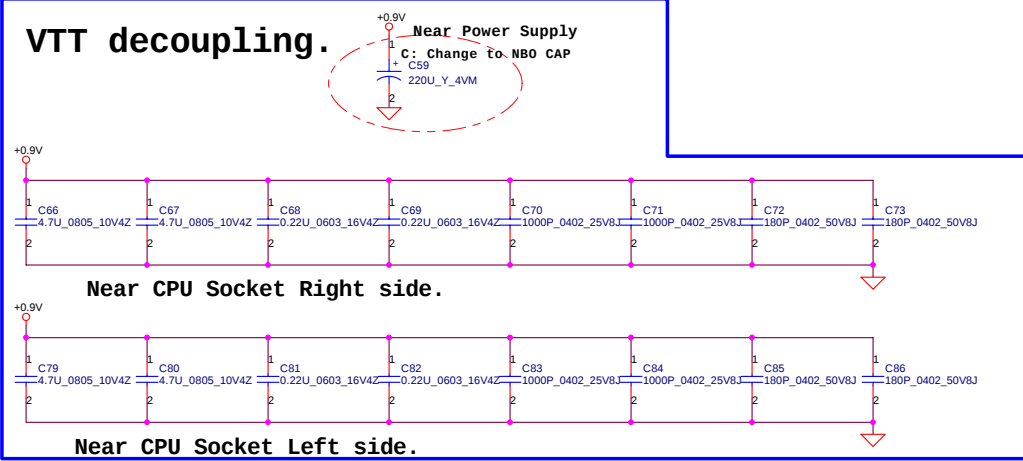
VDDIO decoupling.



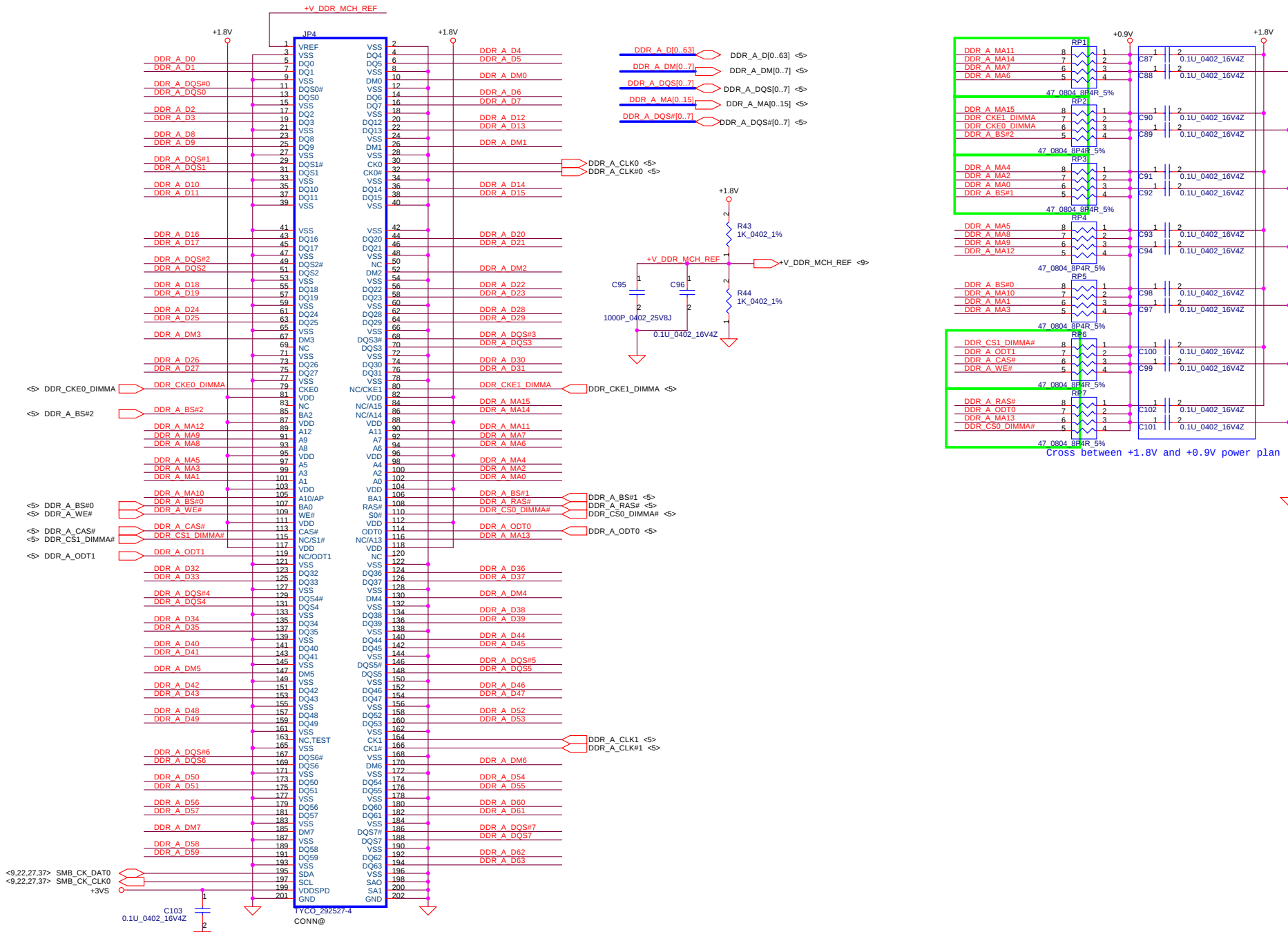
+CPU_CORE_NB decoupling.



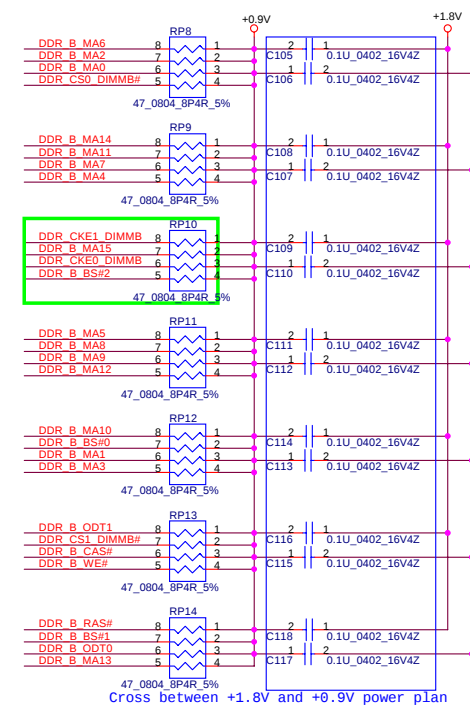
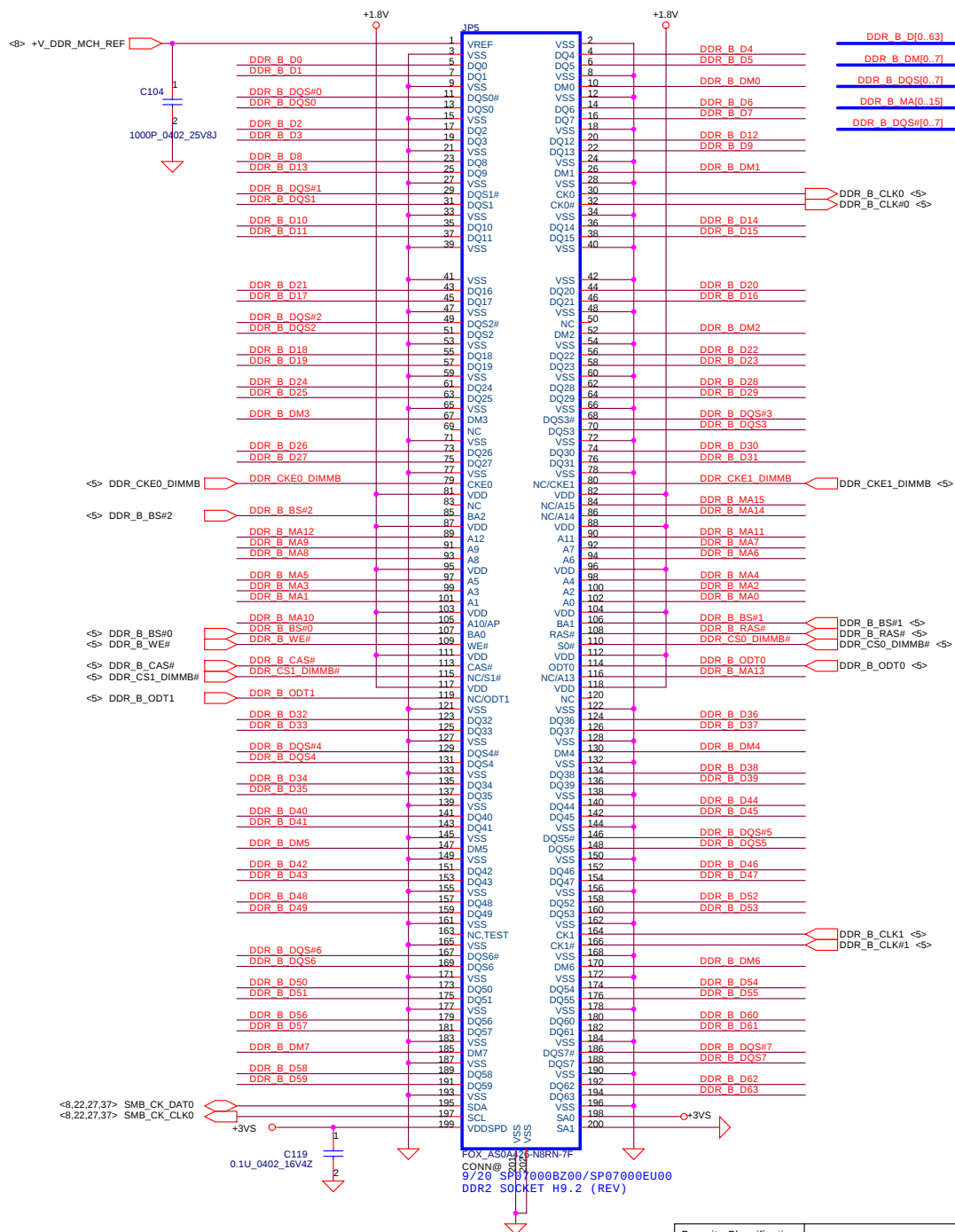
VTT decoupling.



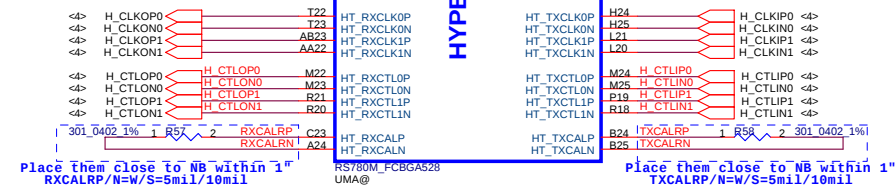
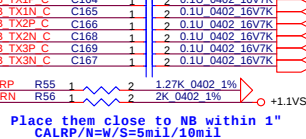
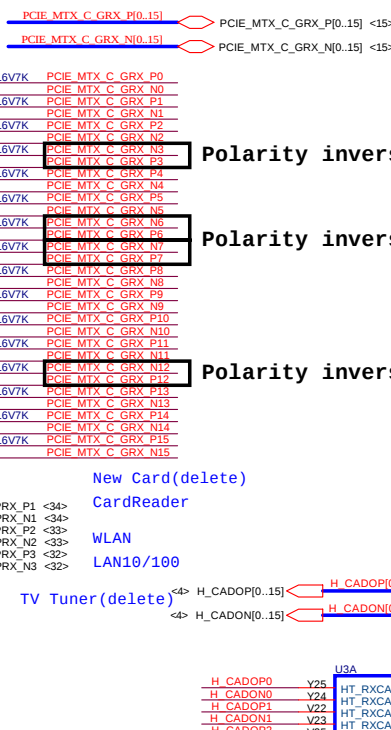
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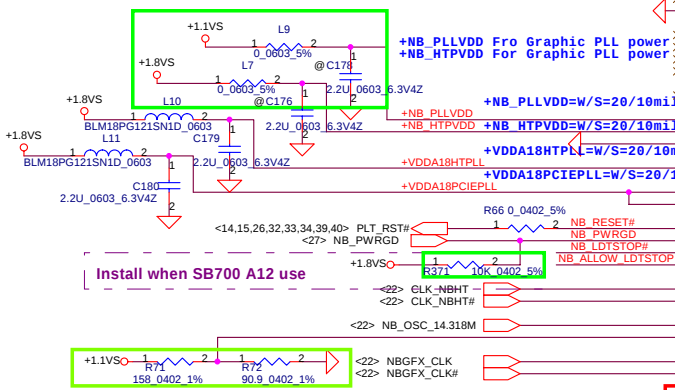
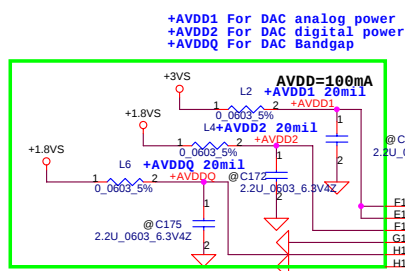
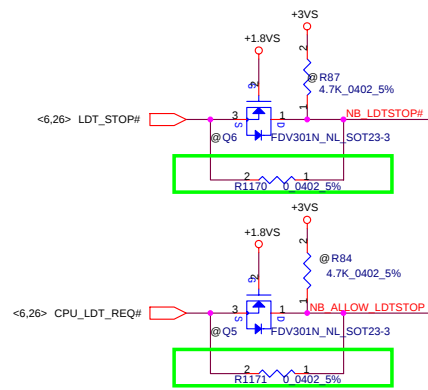
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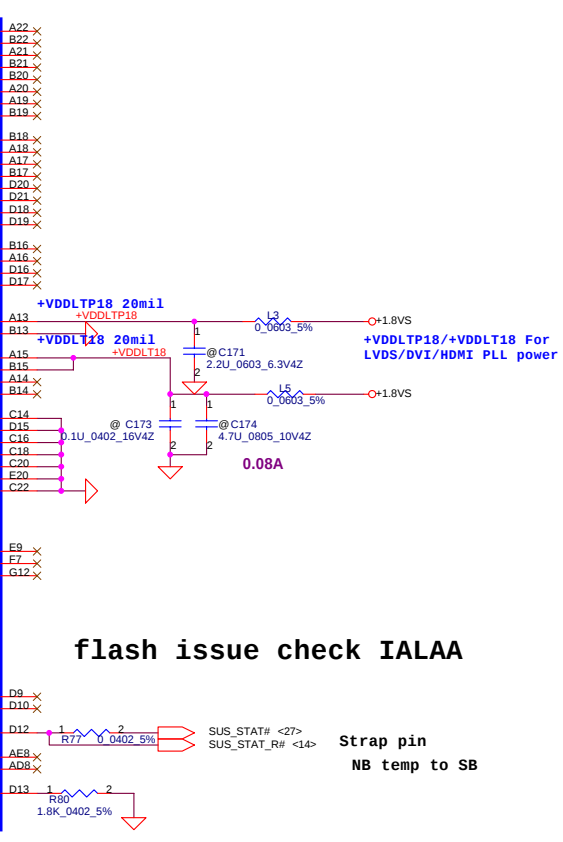
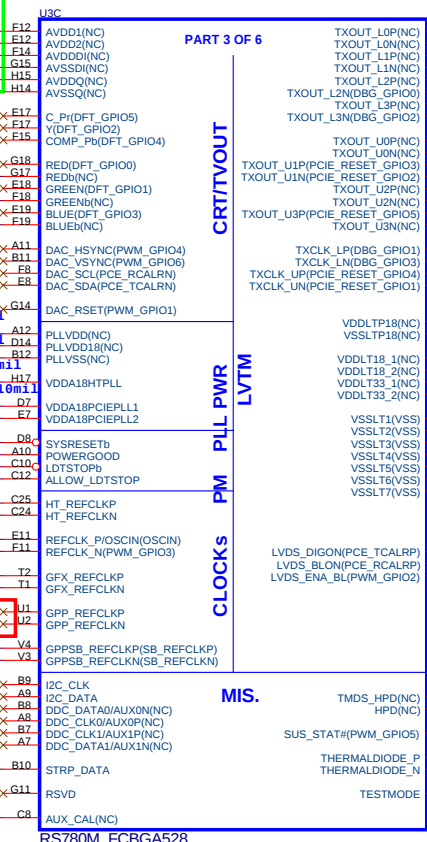
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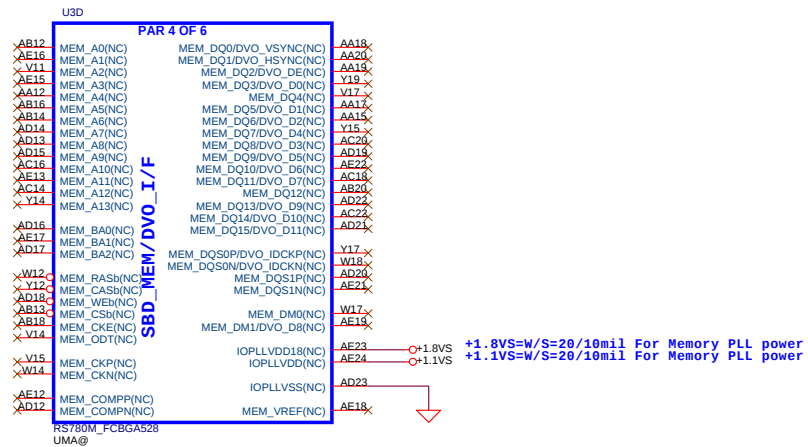
RS780: 158-? 1% series termination resistor and 90.9-? 1% resistor to GND to limit signal swing to 1.1 V. Also made provision for 0.5 * 1.1 V with a resistor divider at the REFCLK_N ball.



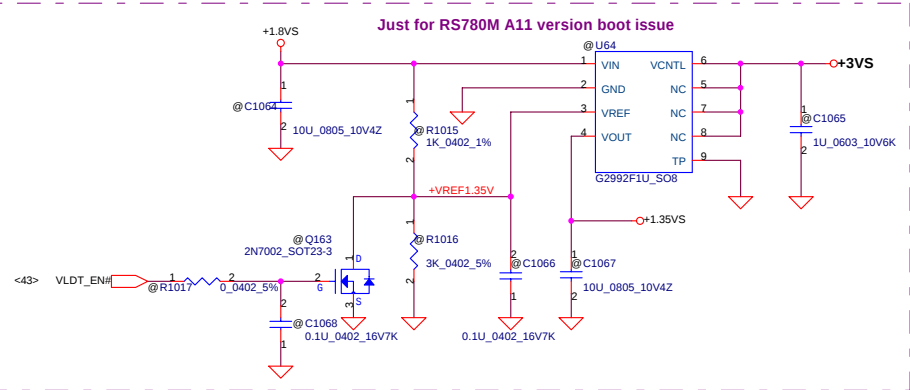
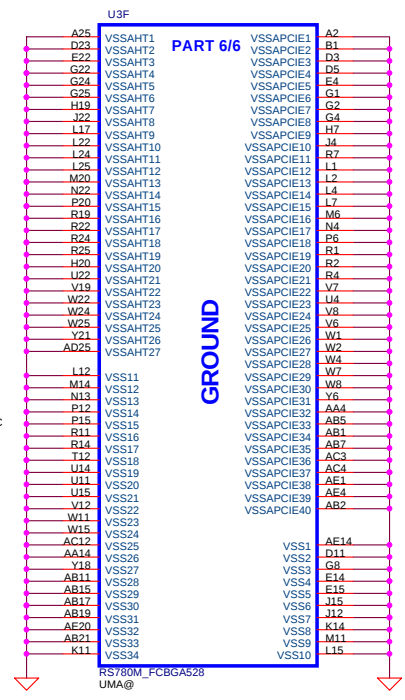
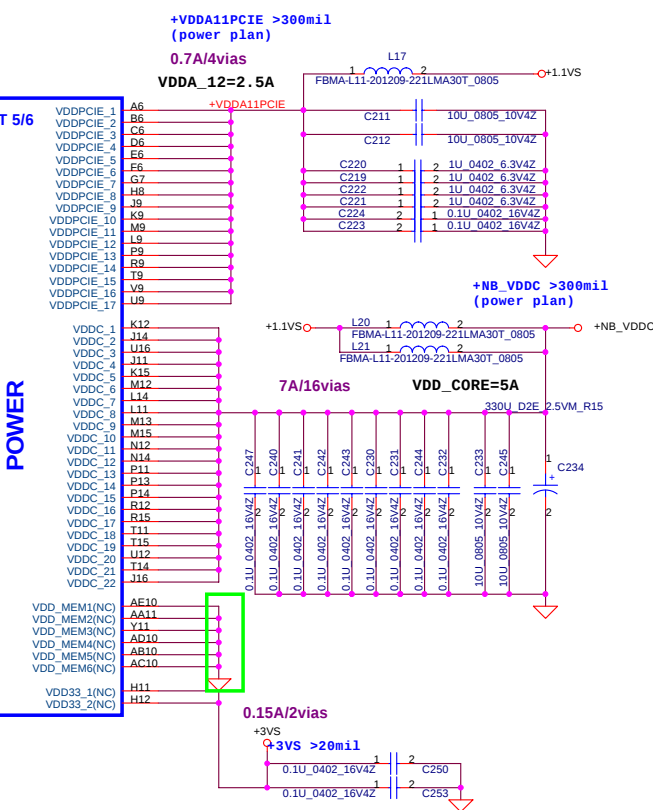
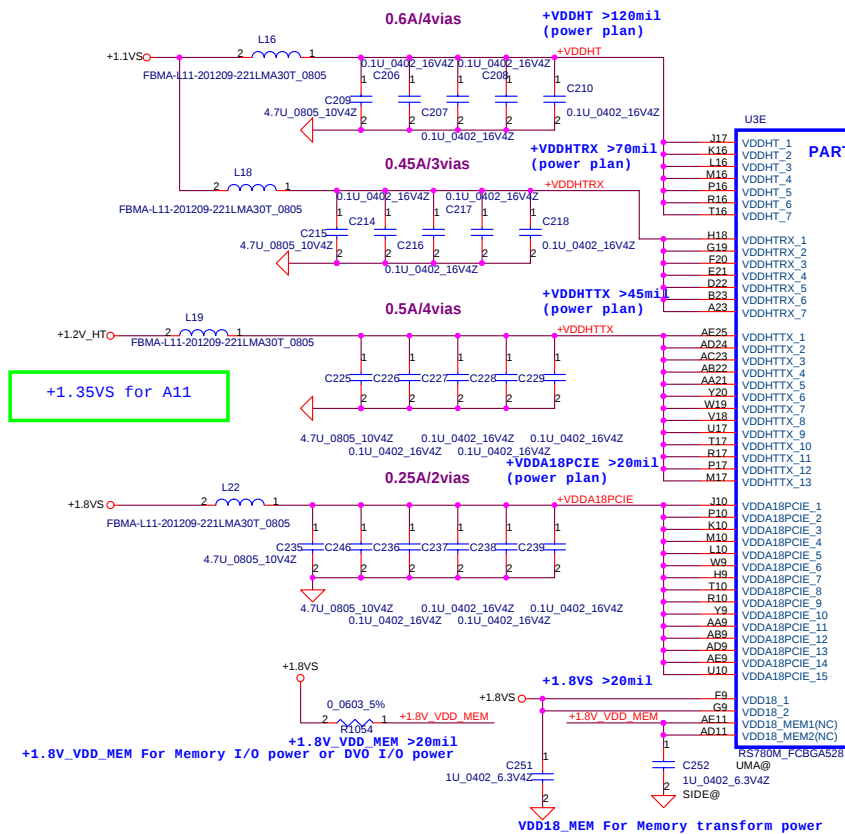
flash issue check IALAA

Strap pin
NB temp to SB

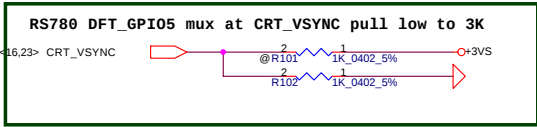
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				Sheet	13 of 52
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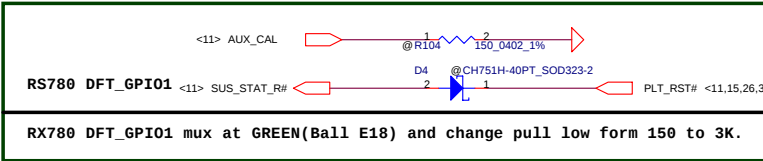
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.

1 : Disable (RS740) Enable (RX780, RS780)

0 : Enable (RS740) Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#



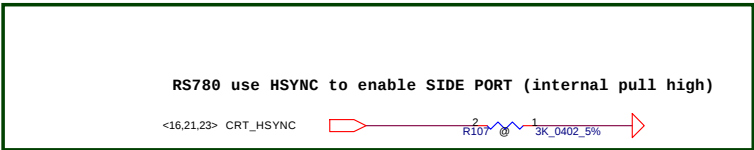
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPI01 RS780:SUS_STAT



DFT_GPIO0:STRAP_DEBUG_BUS_PCIE_ENABLED

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)

0 : Enable

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS740/RS780)

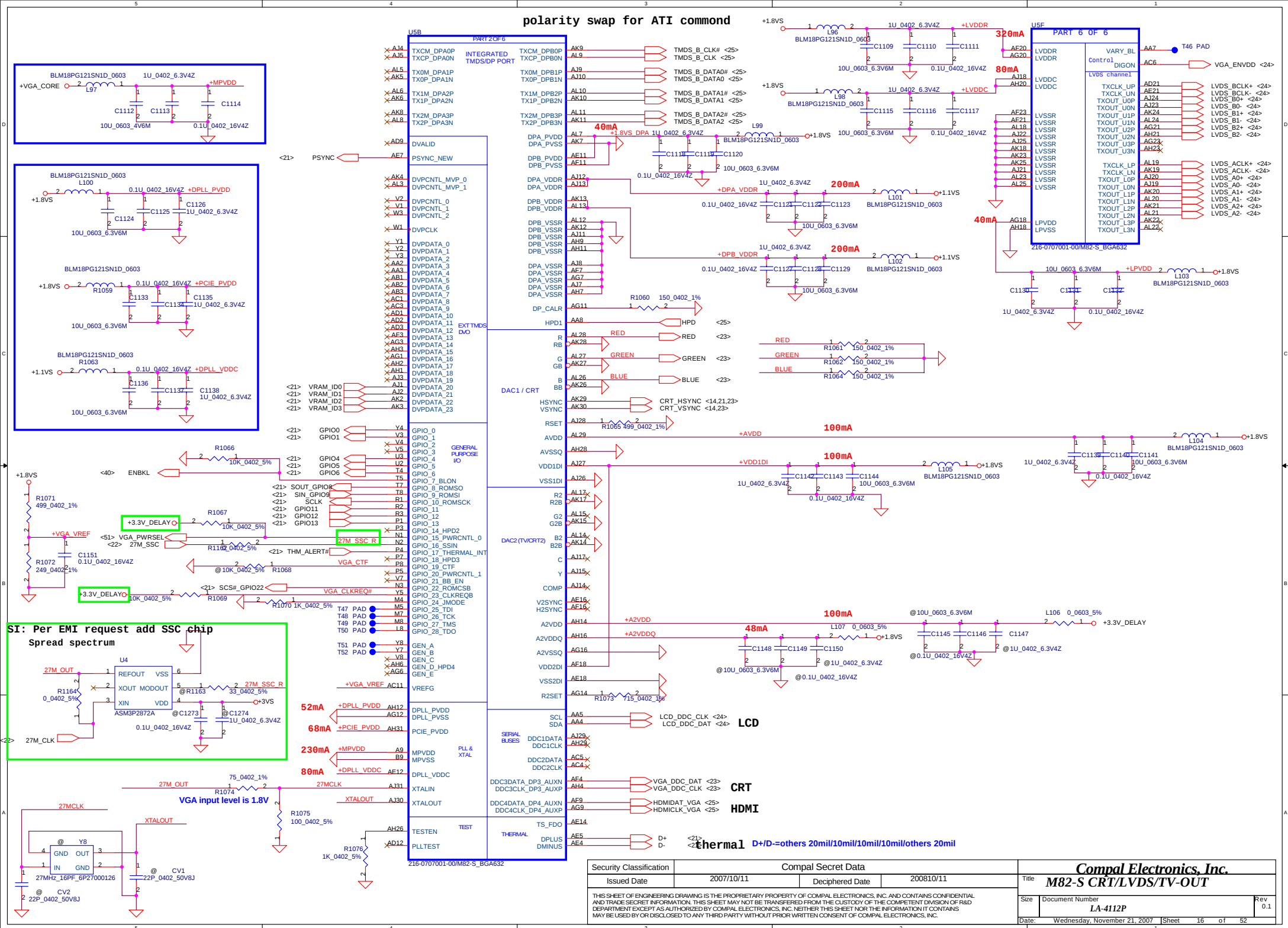
0 : Enable (RS740/RS780)

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				Custom	LA-4112P	0.1
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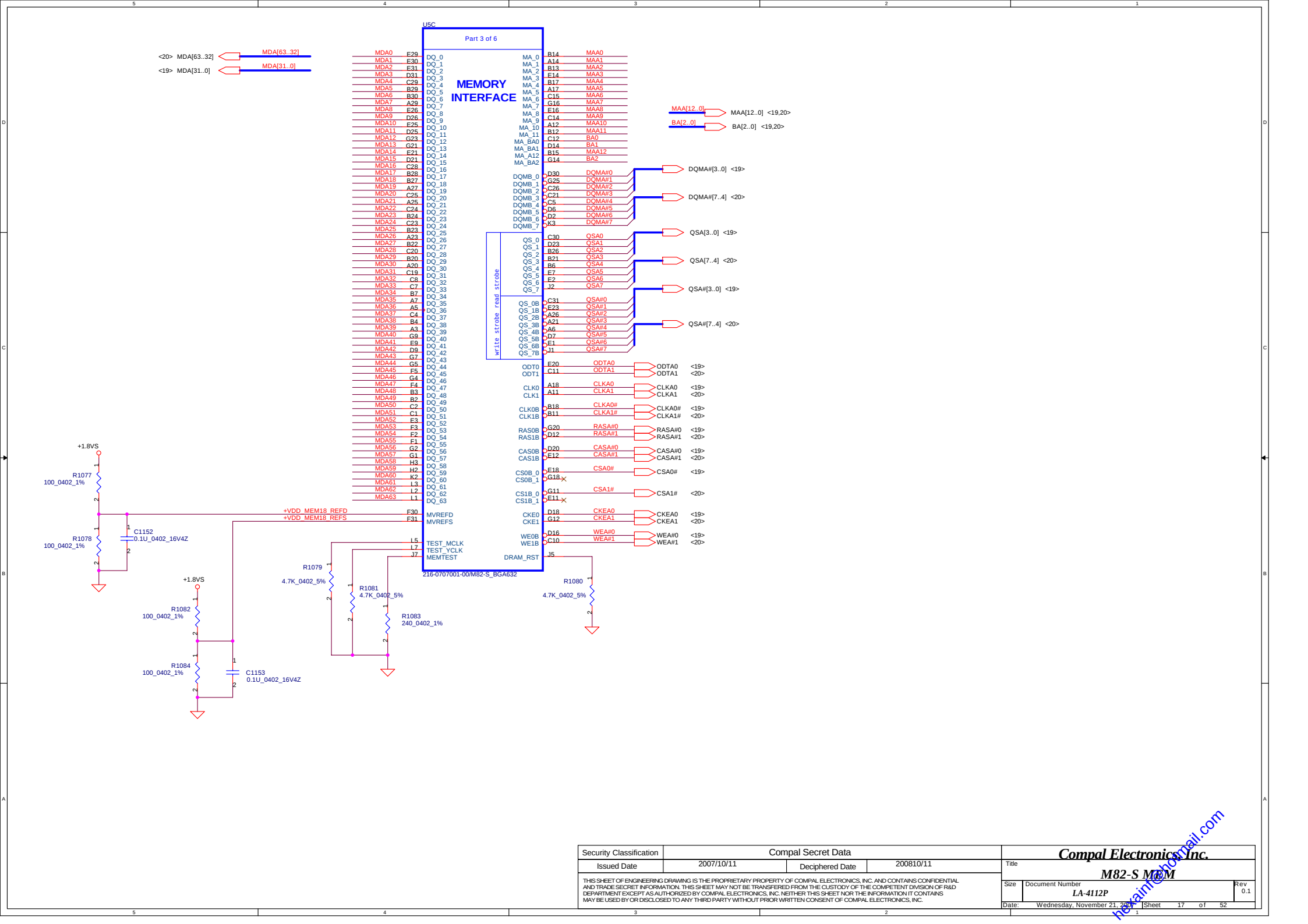


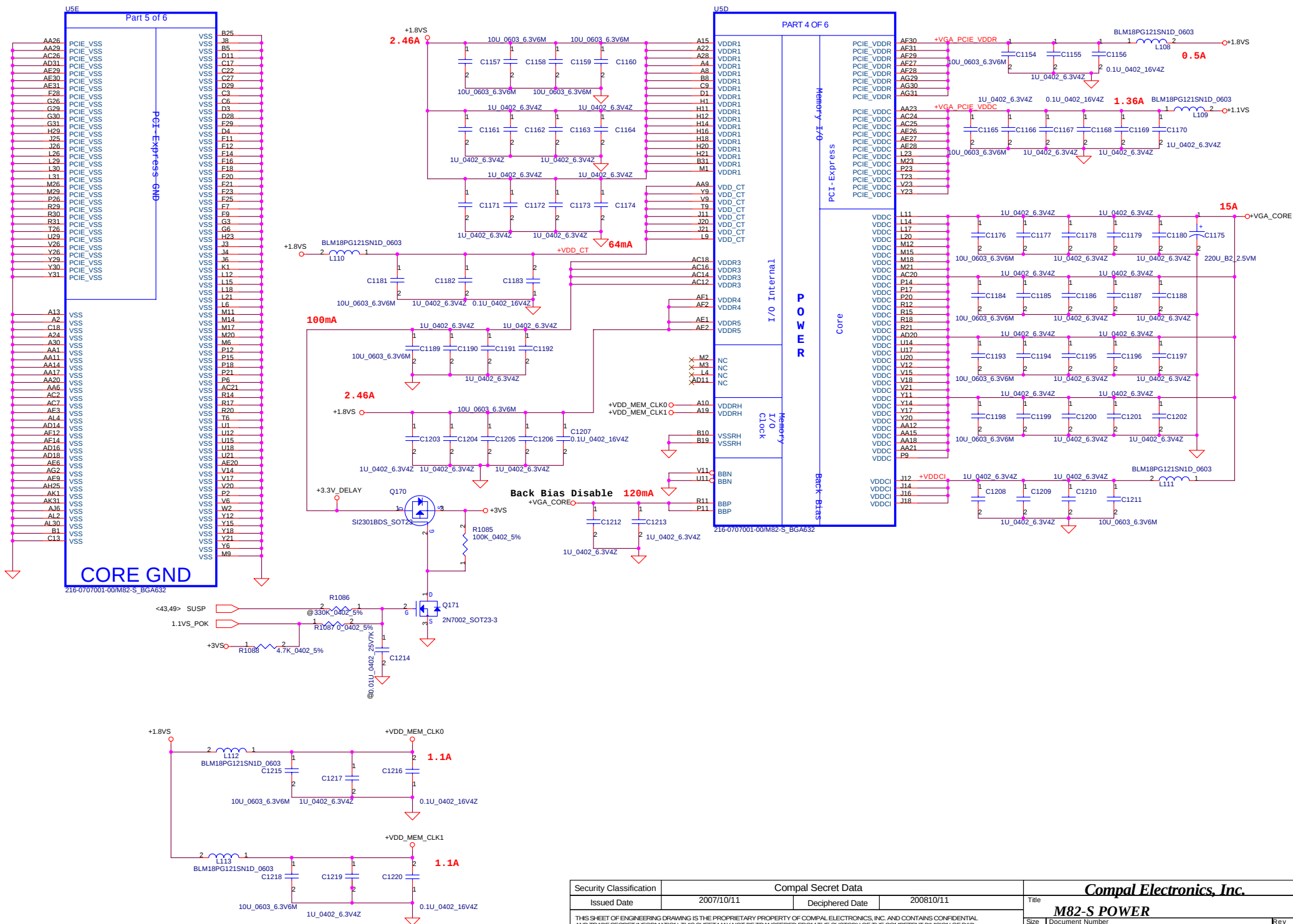
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				Document Number	0.1
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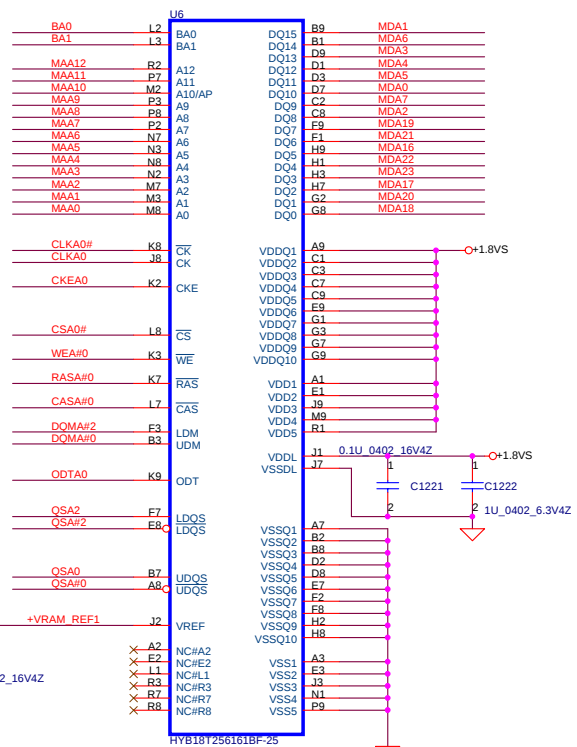
polarity swap for ATI command



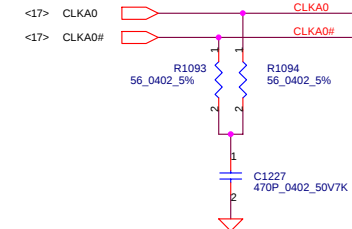
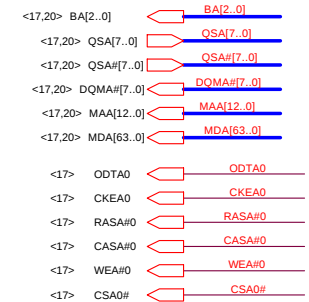
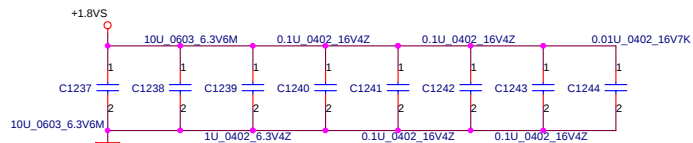
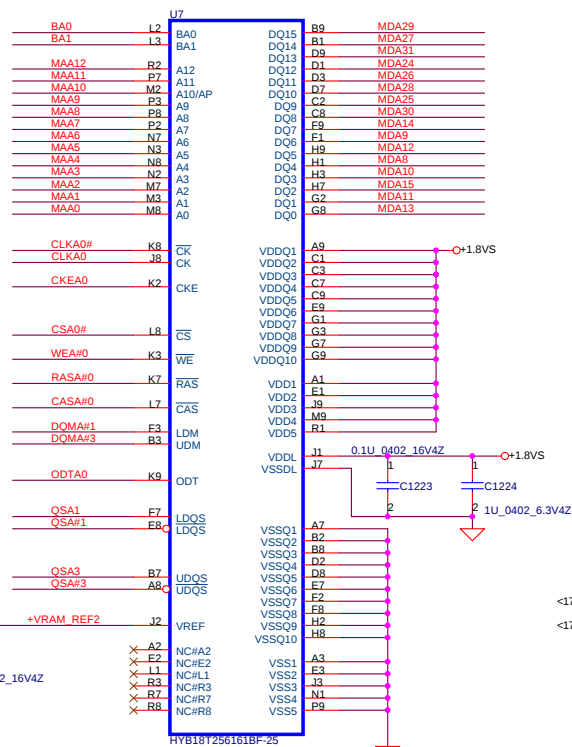
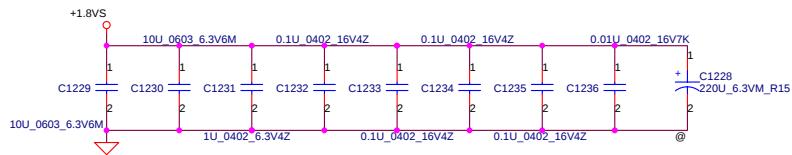
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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Title	
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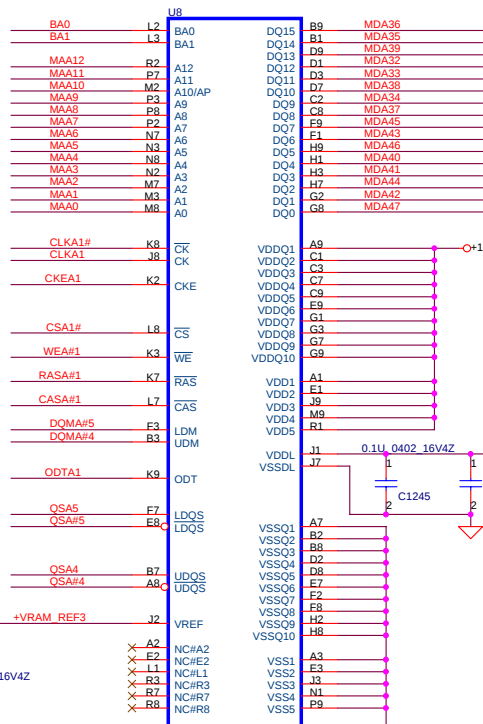




SA00002A200(HYNIX) S IC 16M16/500 HY5PS5616218FP-2L FBGA 84P 1.8V
 SA00002A500(QIMONDA) S IC D2 16M16/500 HYB18T256161BF-20 84P
 SA00000S810(QIMONDA) S IC D2 16M16/400 HYB18T256161BF-25 84P



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								M82-S VRAM					
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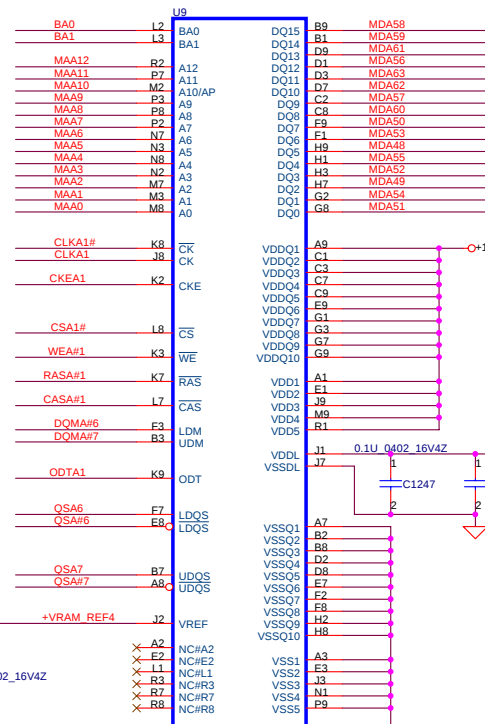
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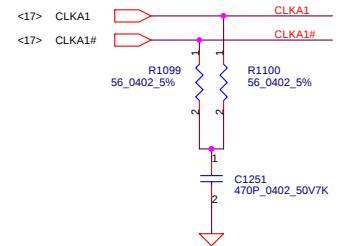
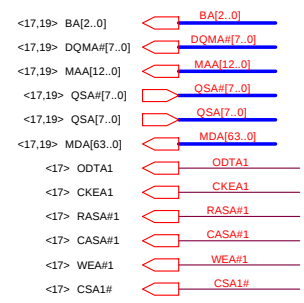
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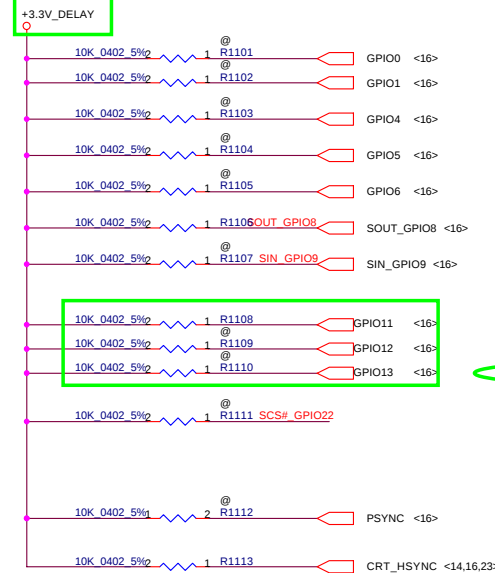
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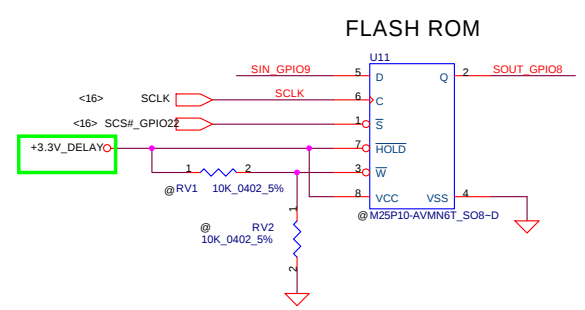
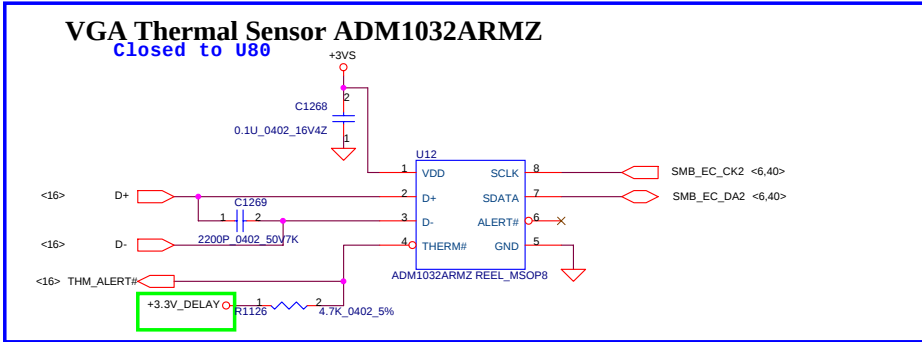
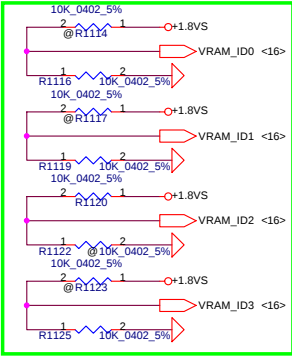


GPIO9 = 0 (BIOS_ROM_EN = 0)		
GPIO[13:11]	MEMORY SIZE	
0 0 0	128MB	
0 0 1	256MB	
0 1 0	64MB	
1 0 0	512MB	

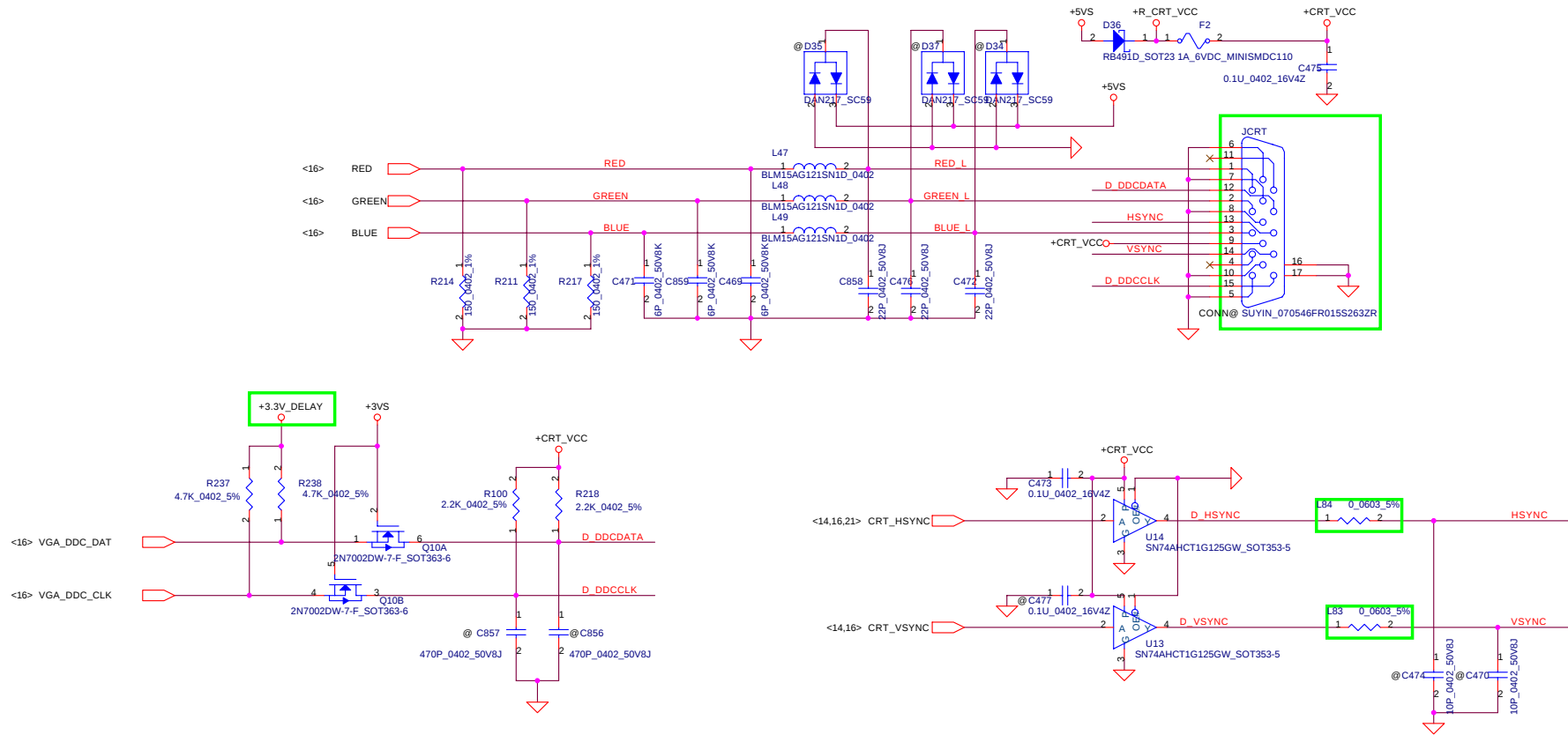
STRAPS	FN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED MBX
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
BIF_VGA_DIS	PSYNC	VGA ENABLED==0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1
VRAM_ID[3:0]	400MHz DVPDATA (23,22,21,20)		VRAM_ID 3,2,1,0
		Samsung 16Mx16 1.8V	0 0 0 0
		Samsung 32Mx16 1.8V	0 0 0 1
		Hynix 16Mx16 1.8V	0 0 1 0
		Hynix 32Mx16 1.8V	0 0 1 1
		Qimonda 32Mx16 1.8V	0 1 0 0
	500MHz DVPDATA (23,22,21,20)	Qimonda 32Mx16 1.8V	0 0 0 0
		Samsung 32Mx16 1.8V	0 0 0 1
		Hynix 16Mx16 1.8V	0 0 1 0
		Qimonda 16Mx16 1.8V	0 0 1 1
	Samsung 16Mx16 1.8V	0 1 0 0	

DB VRAM status			
400MHz DVPDATA (23,22,21,20)	Qimonda 32Mx16 1.8V	0 1 0 0	default
500MHz DVPDATA (23,22,21,20)	Hynix 32Mx16 1.8V	0 1 1 0	Options

ATI RESERVED CONFIGURATION STRAPS							
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESE							
GPIO2	GPIO3	GPIO5	GPIO6	DVALID	H2SYNC	V2SYNC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET							
GENERICC	GPIO21_BB_EN	GPIO_28_TDO					



CRT CONNECTOR

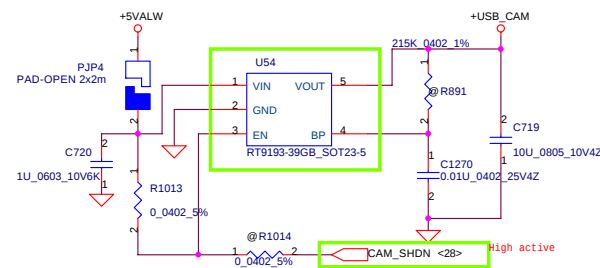
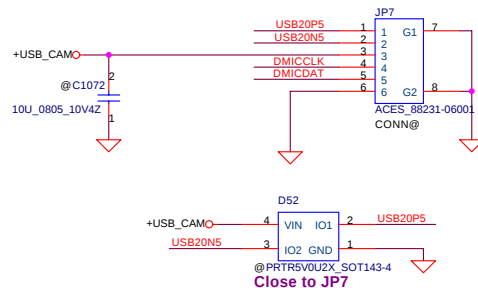


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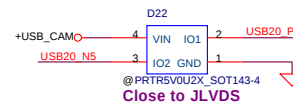
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CRT Connector

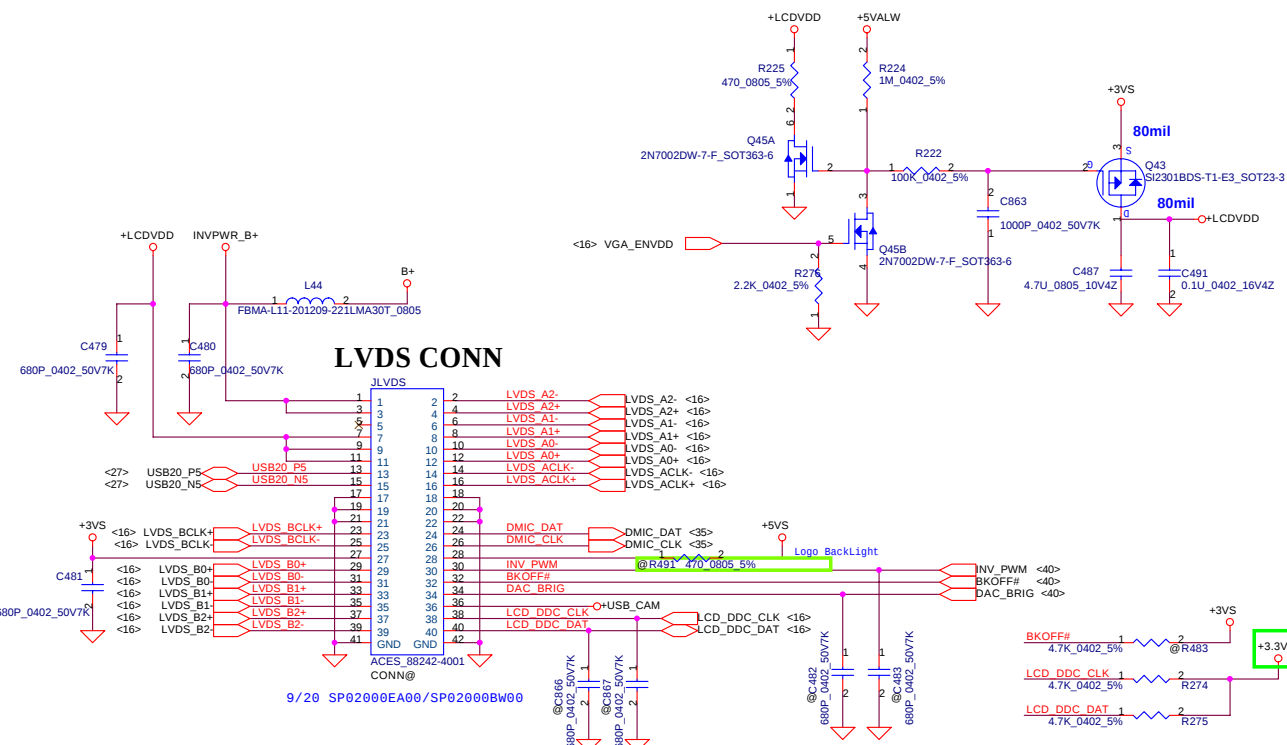
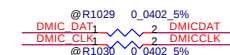
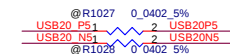
WebCam+Digital Mic



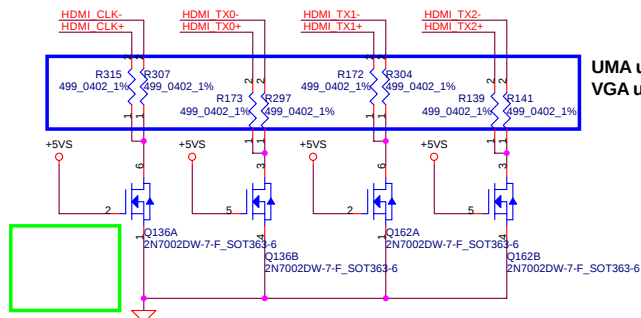
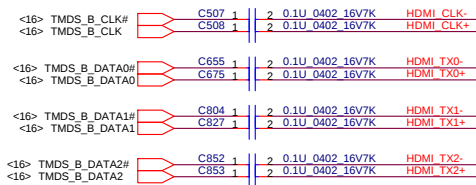
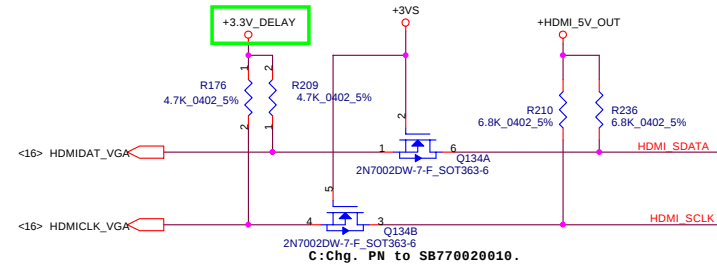
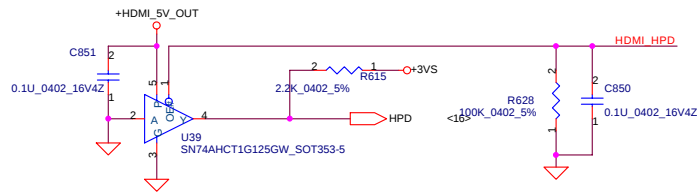
USB_VCCA is +3.9V, R892:100K; R891:215KKohm
G916 Vref=1.25V



Close to JLVDS

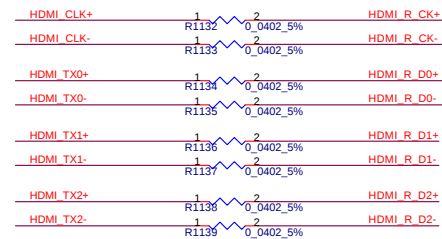


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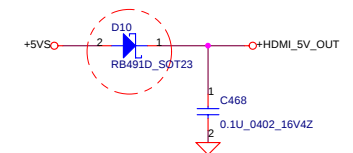


UMA use 750 ohm
VGA use 499 ohm

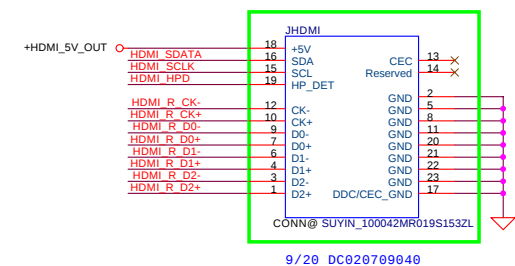
COMMON MODE CHOCK is SM070000K00 KING_WCM-2012-900T_4P



MP:Update D10 to meet HDMI.



HDMI Connector



9/20 DC020709040

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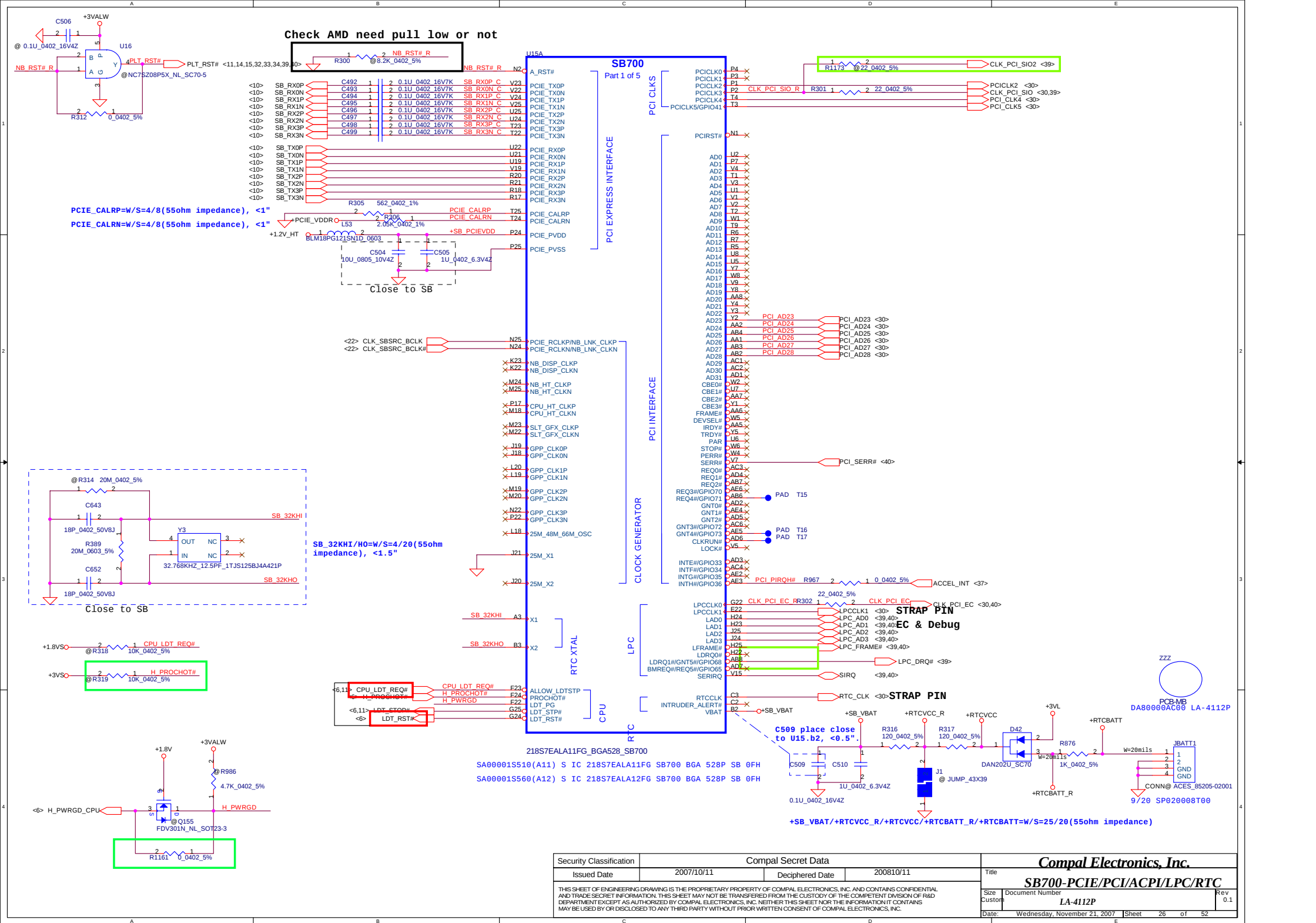
HDMI

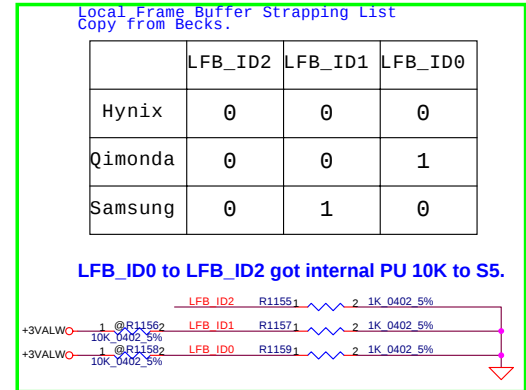
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Rev

0.1

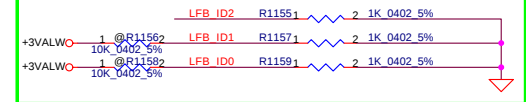
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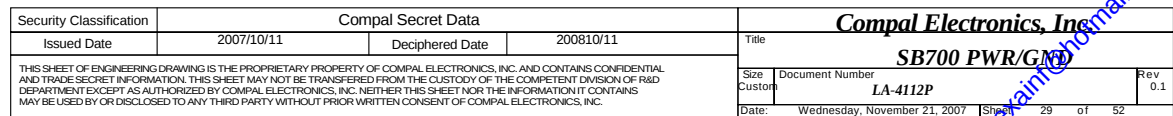




	LFB_ID2	LFB_ID1	LFB_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

LFB_ID0 to LFB_ID2 got internal PU 10K to S5.

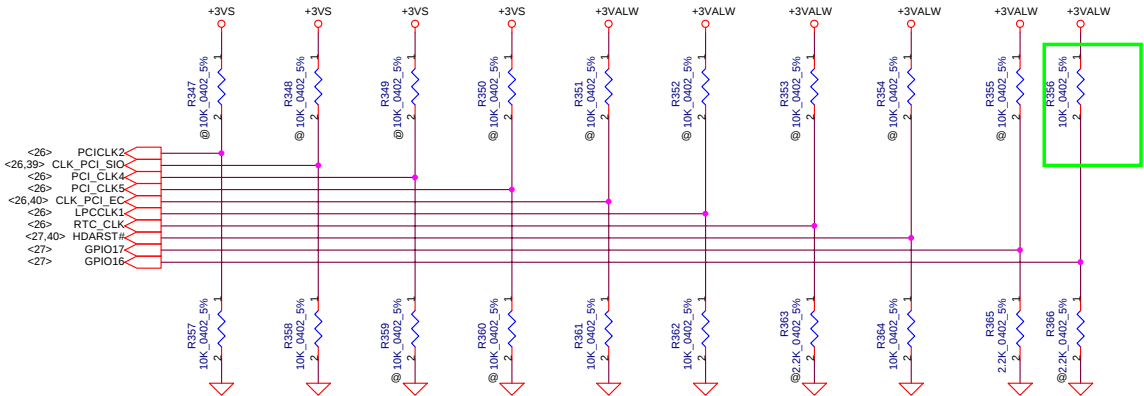




REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

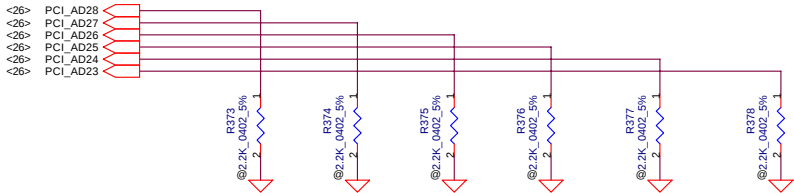
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



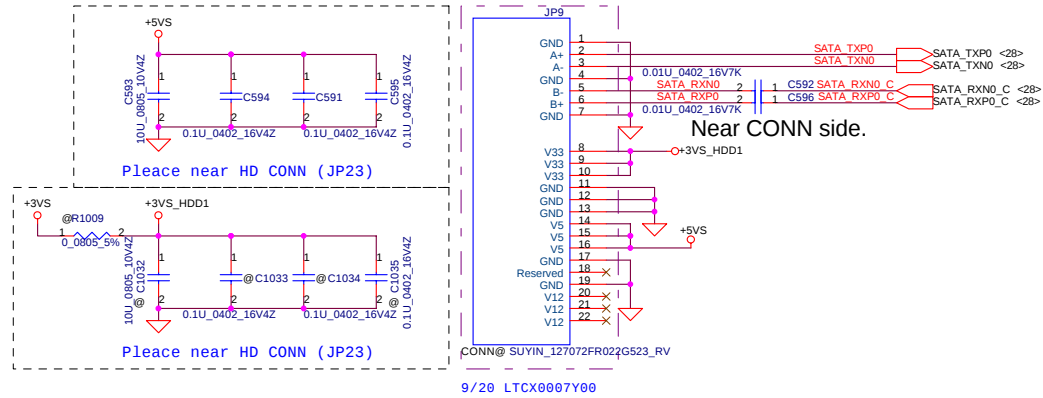
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

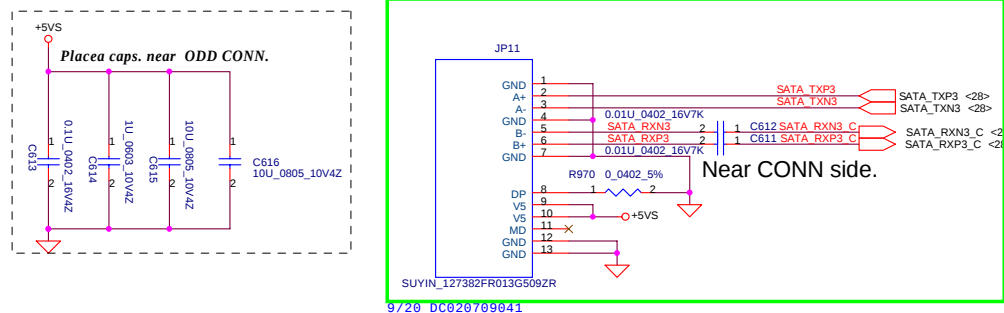


HDD Connector

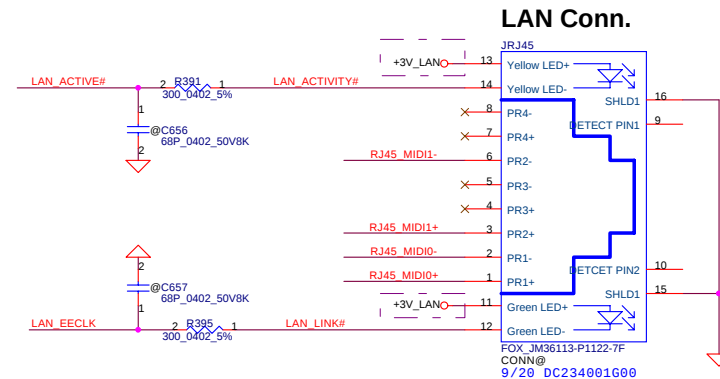
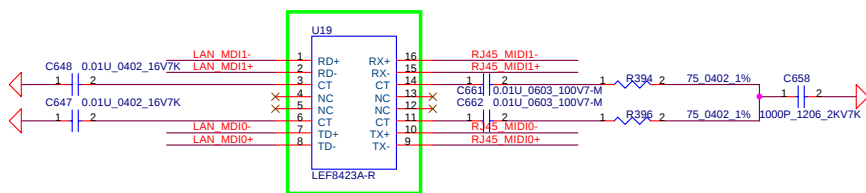
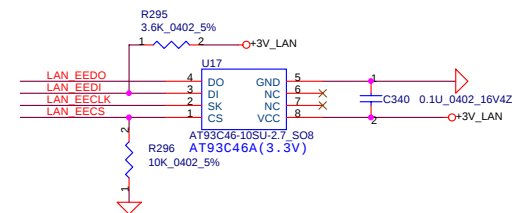
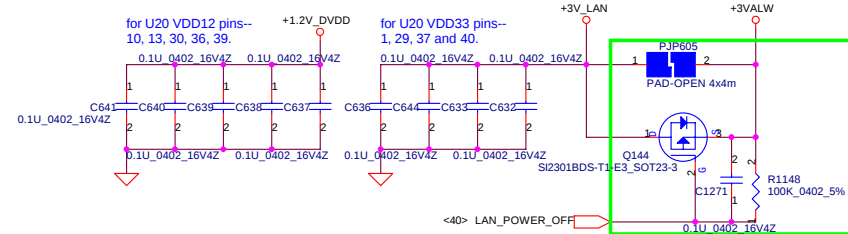
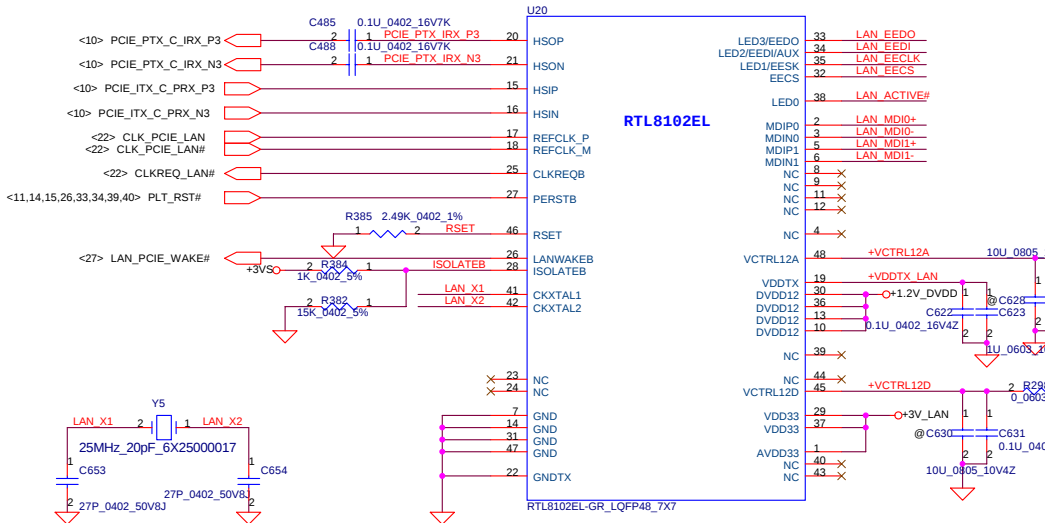


Multi-Bay Connector-option(deltet)

CD-ROM Connector



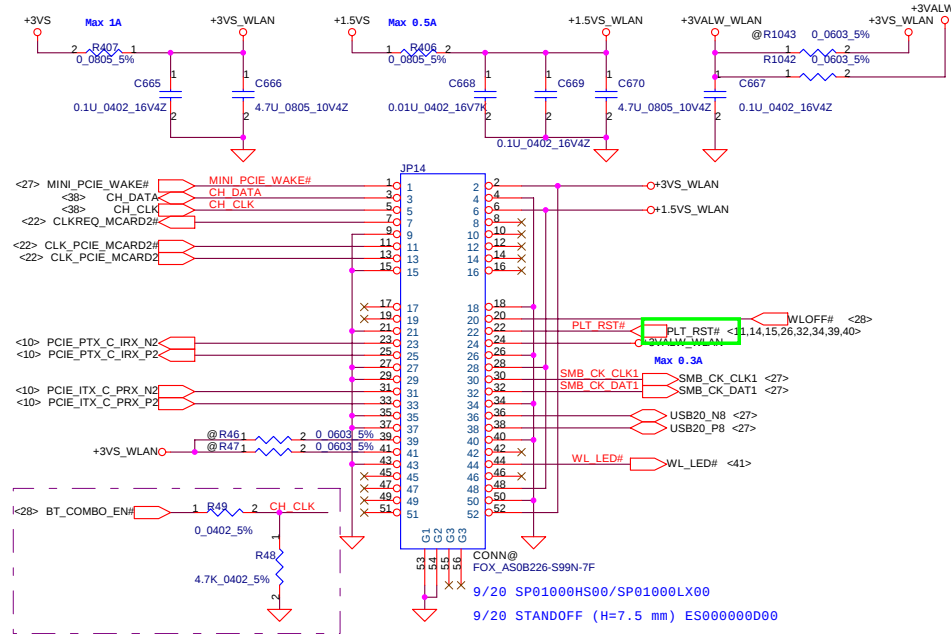
Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/11	Deciphered Date	200810/11	Compal Electronics, Inc.	
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				Custom	LA-4112P
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9/20 DC234001G00

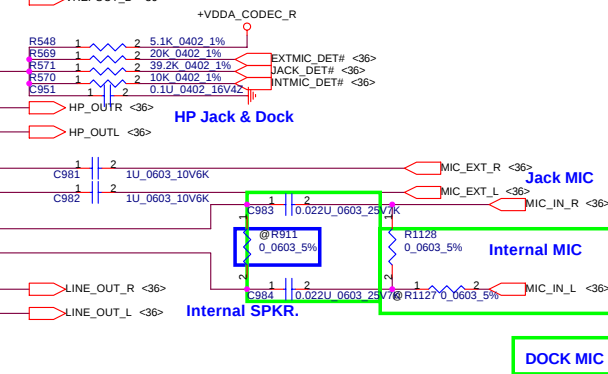
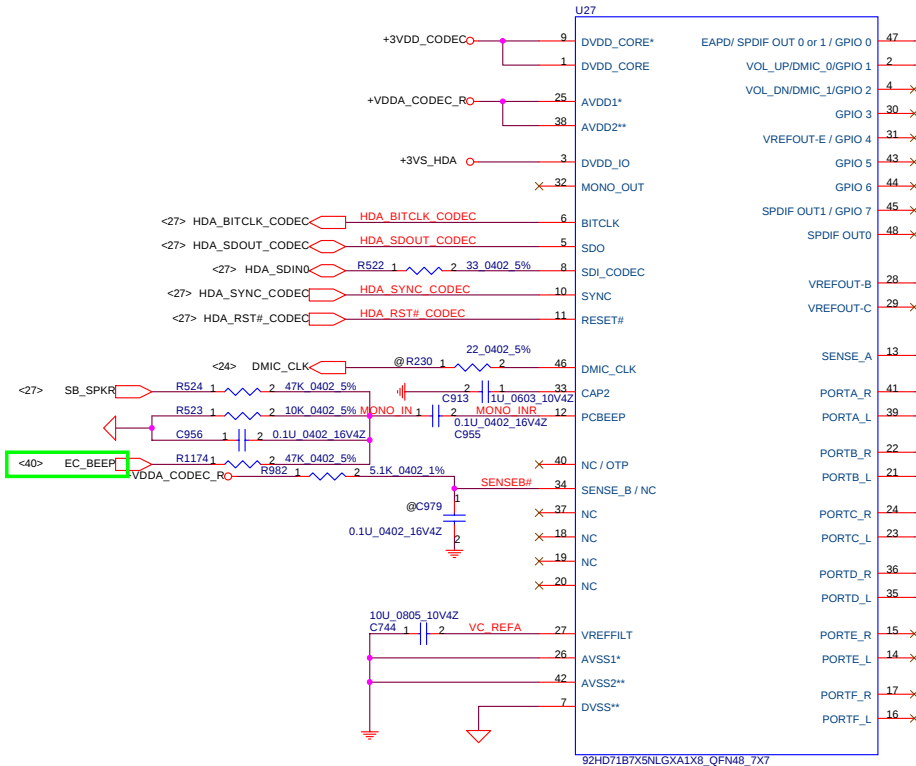
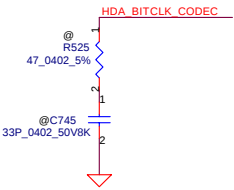
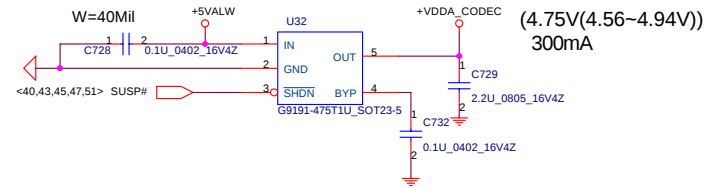
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				RealTek 8102EL 10/100				
				Size	Document Number		Rev	
				Custor	LA-4112P		0	
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Mini Card Slot 1---WLAN

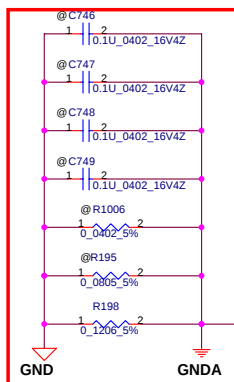


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				Size	Rev
				Custom	0.1
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CODEC POWER

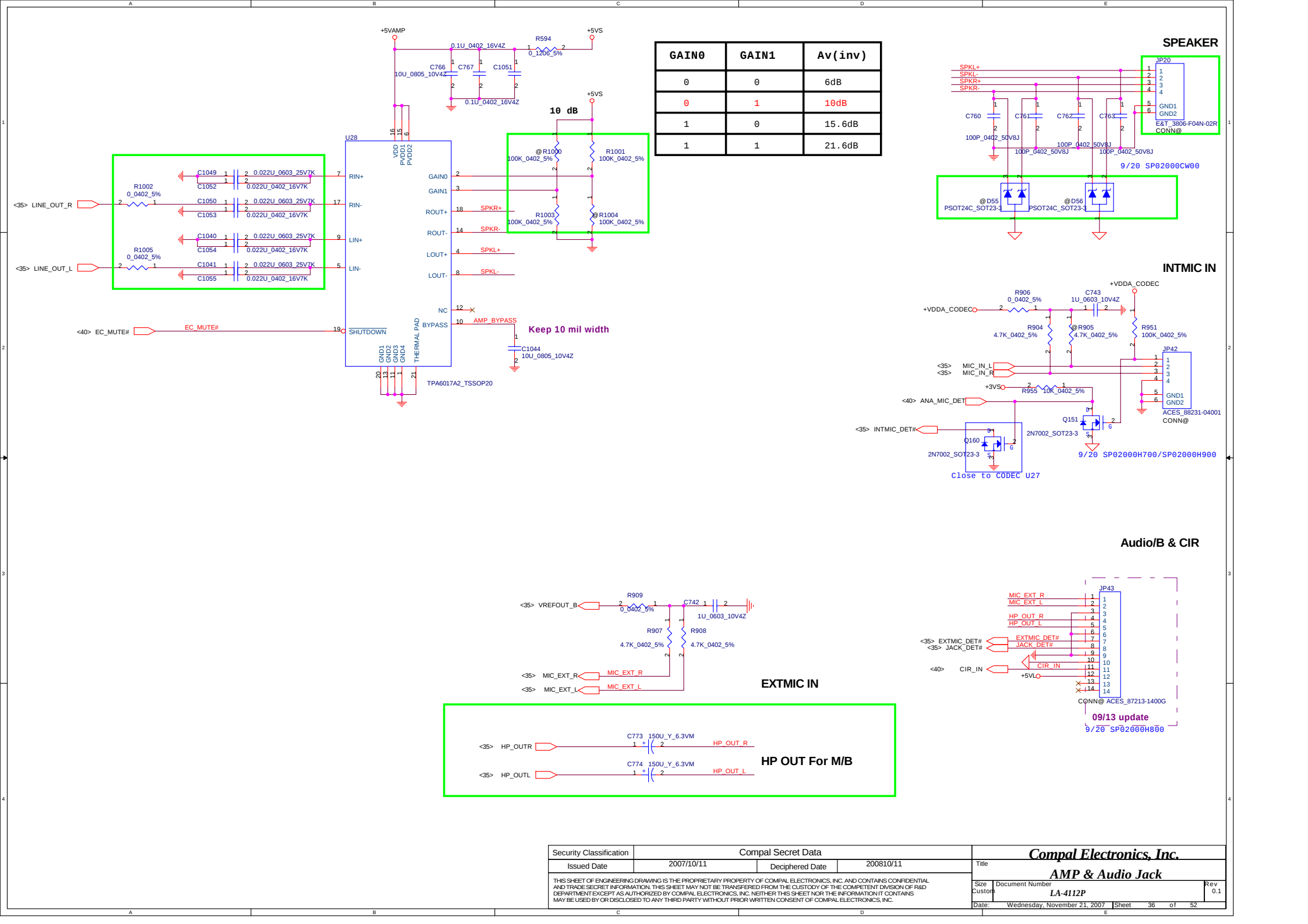


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.1K	H	5.1K

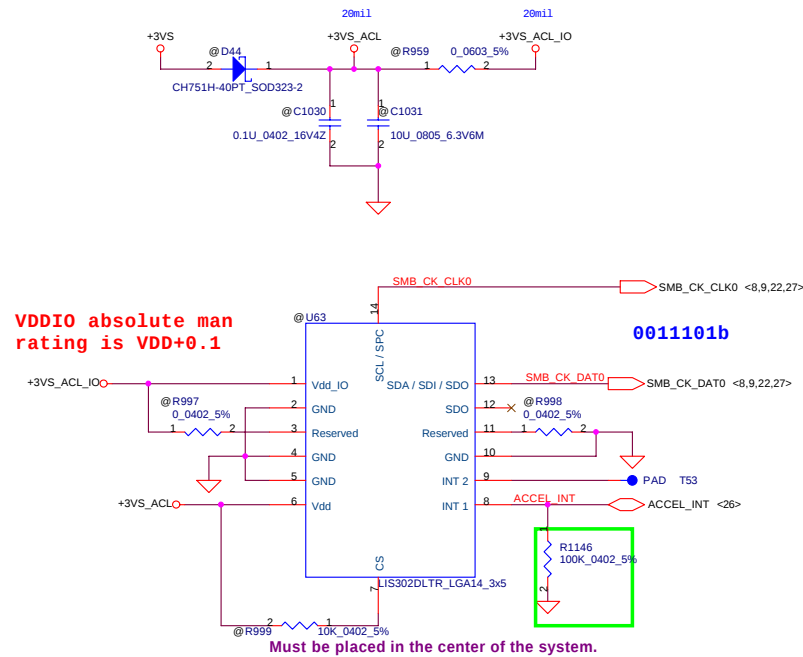


Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

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				Sheet	35 of 52
				Rev	0.1

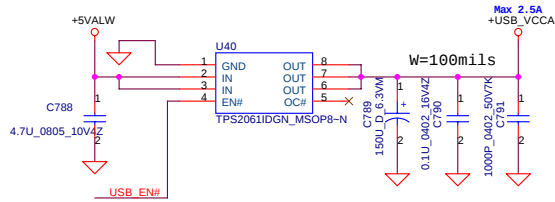


ACCELEROMETER

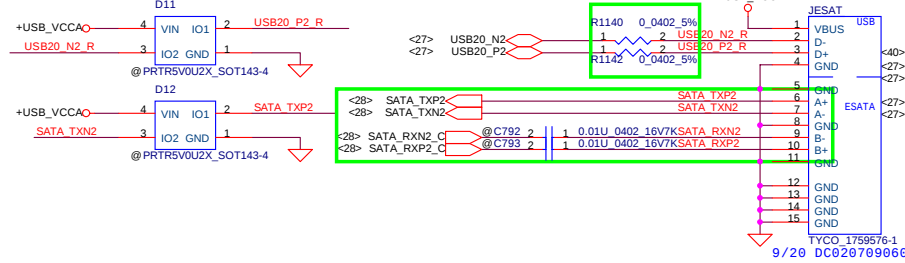


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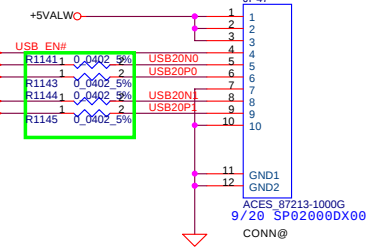
Left side USB CONNECTOR



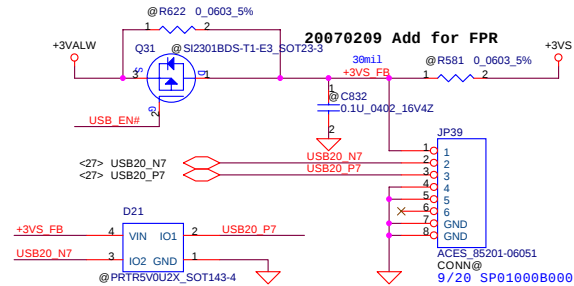
Left side ESATA5/USB2 combination Connector



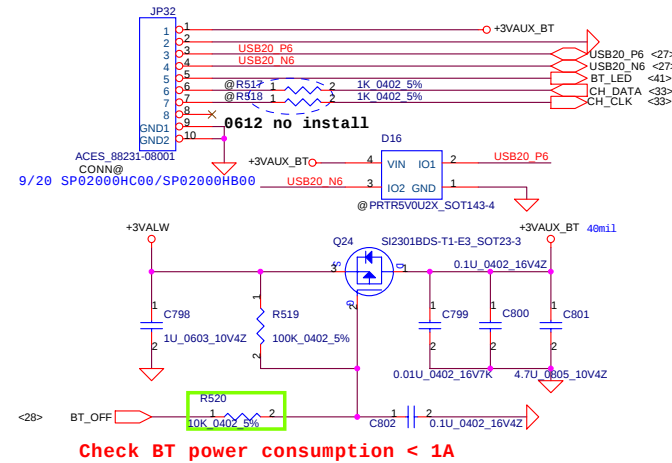
Right side USB 0&1 Board Conn



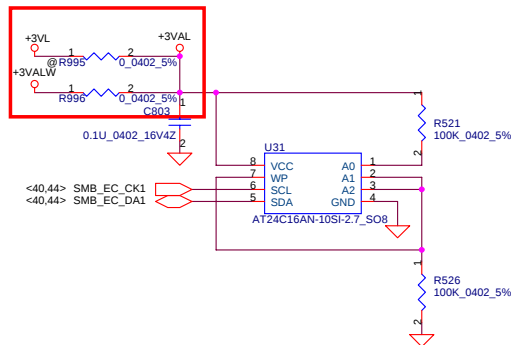
Finger printer



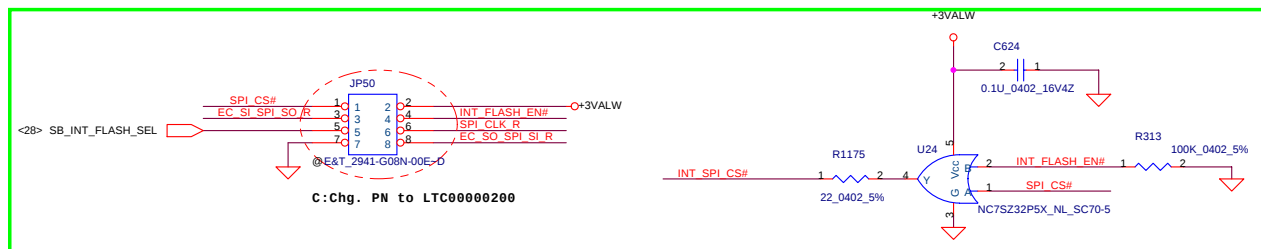
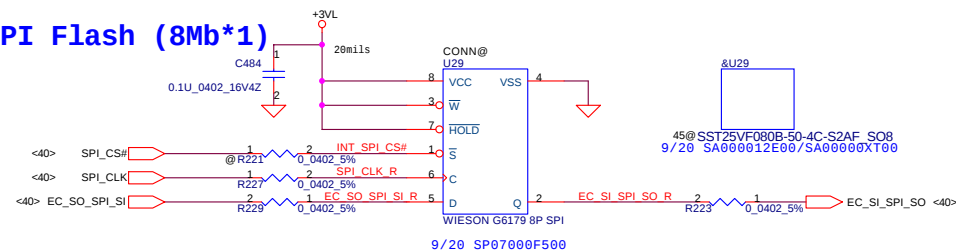
BT Connector



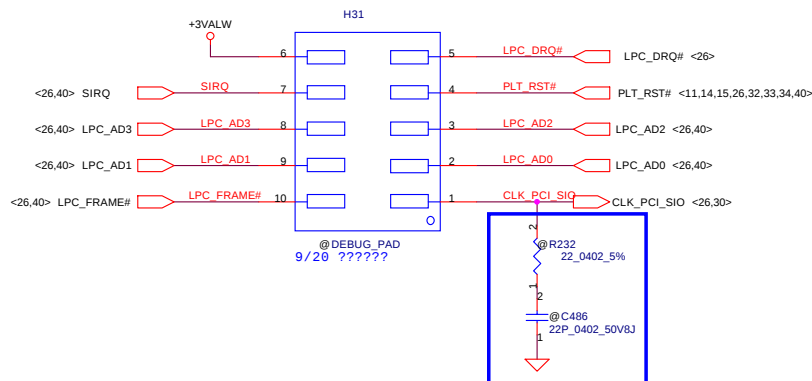
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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Compal Electronics, Inc.		
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				Date:	Wednesday, November 21, 2007	Sheet 38 of 52



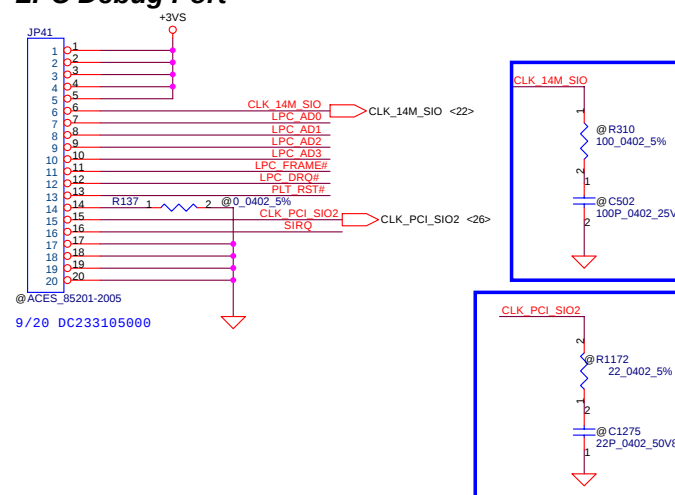
SPI Flash (8Mb*1)



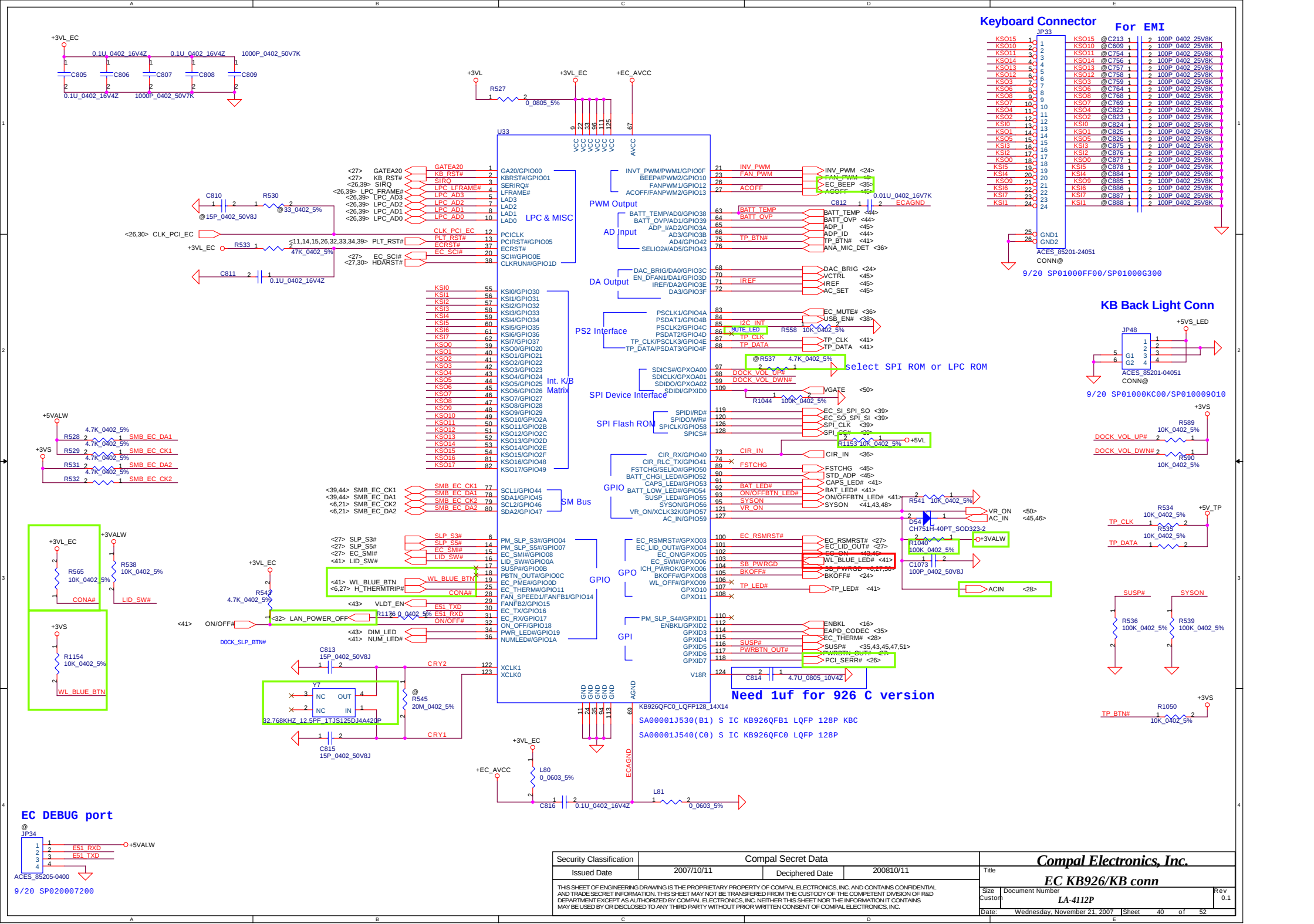
LPC Debug Port



LPC Debug Port



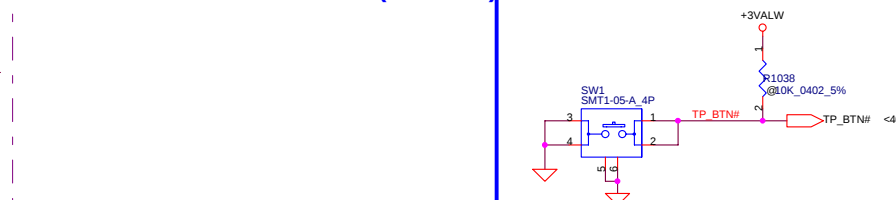
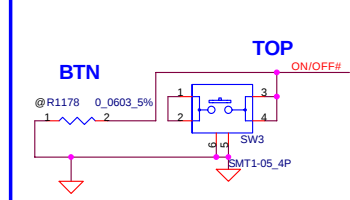
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						Size		Document Number		Rev	
						Custom		LA-4112P		0	
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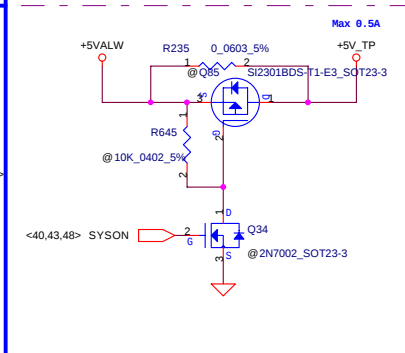
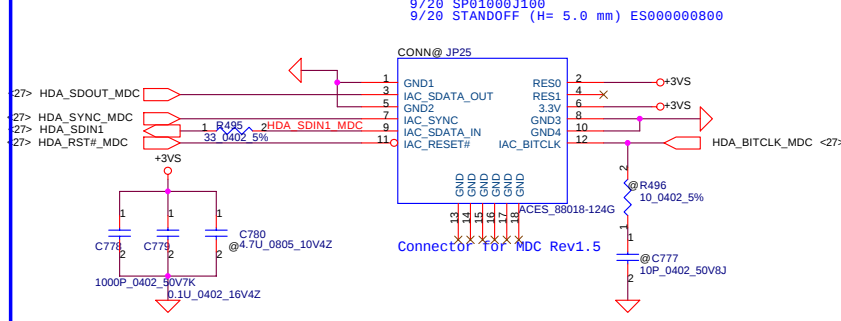
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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Title	EC KB926/KB conn	
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for debug only

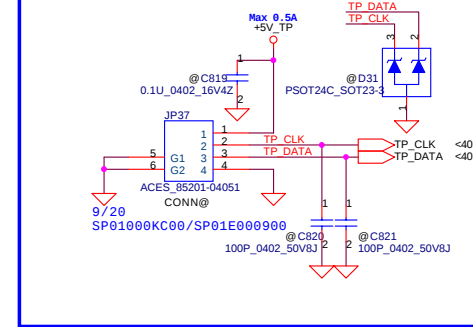
ON/OFF Button Connector(delete)TP ON/OFF



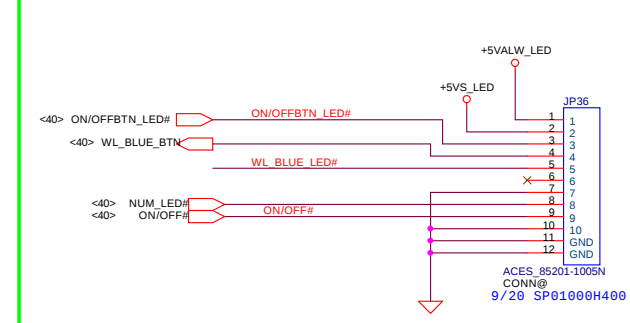
MDC 1.5 Conn.



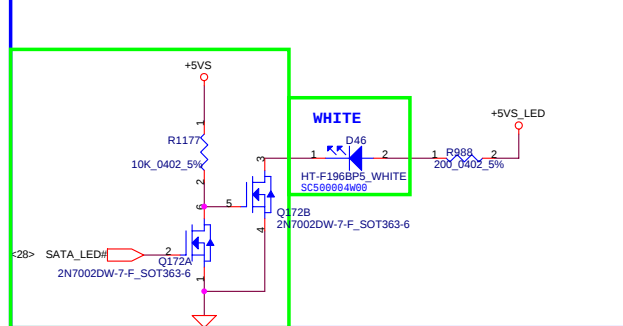
M/B TO TP/B



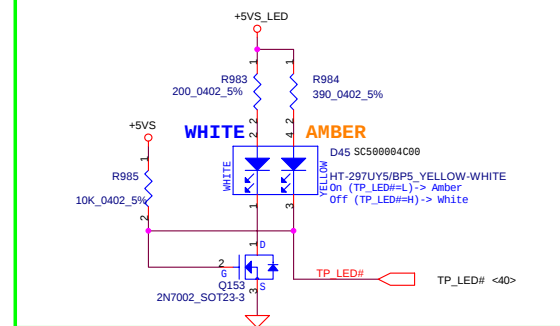
SWITCH BOARD.



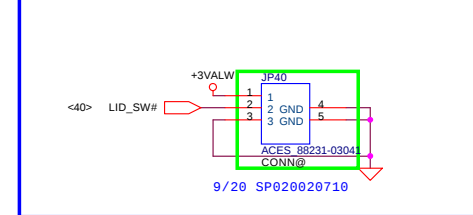
HDD LED



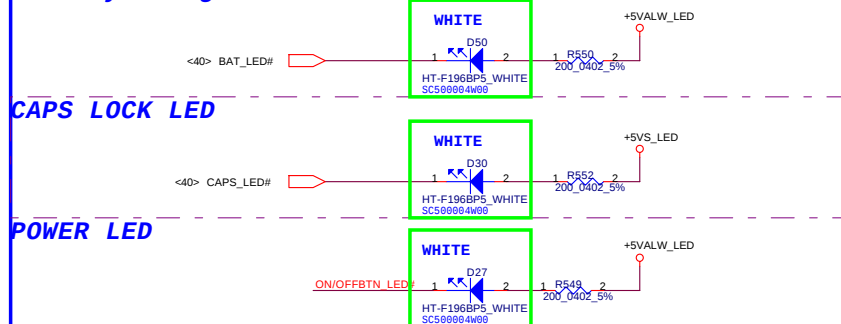
TouchPAD ON/OFF LED



Reed switch BOARD.



Battery Charge LED



White LED: VF=3V, IF = 10mA, Res = 200 ohm
Amber LED: VF=1.8V, IF = 8mA, Res = 390 ohm

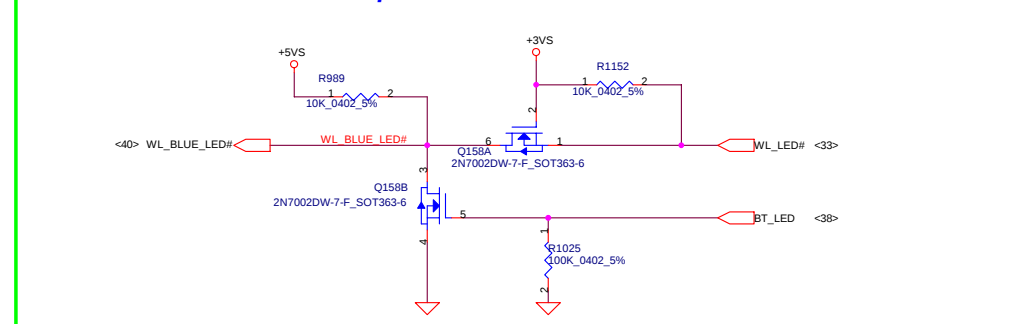
CAPS LOCK LED



POWER LED

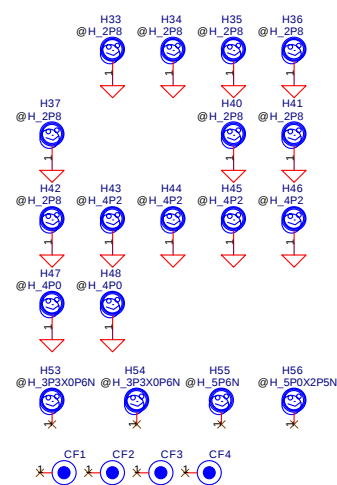


WLAN and BT LED inform pin to KBC



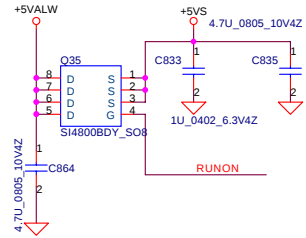
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H47, H48 -Stand off of MODEM on BOT Side

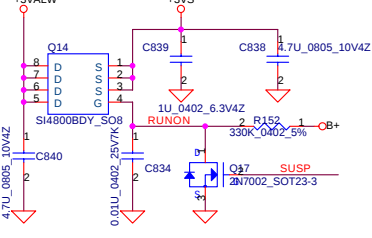


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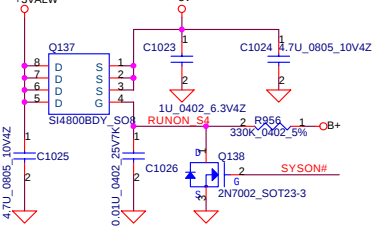
+5VALW TO +5VS



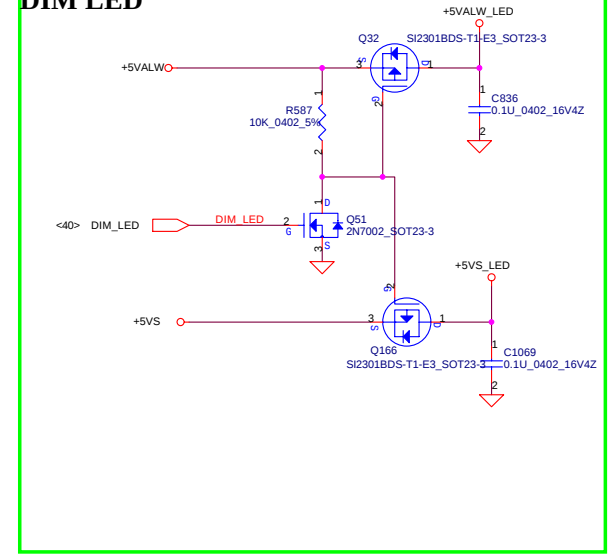
+3VALW TO +3VS



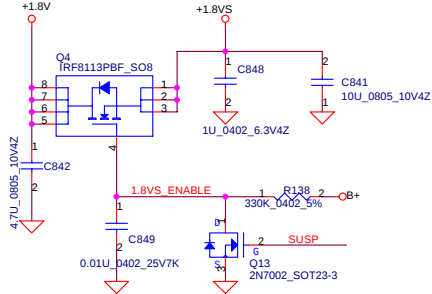
+3VALW TO +3V



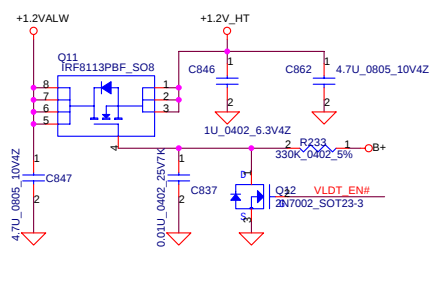
DIM LED



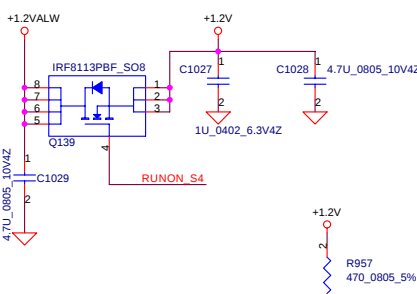
+1.8V TO +1.8VS



+1.2VALW TO +1.2V_HT

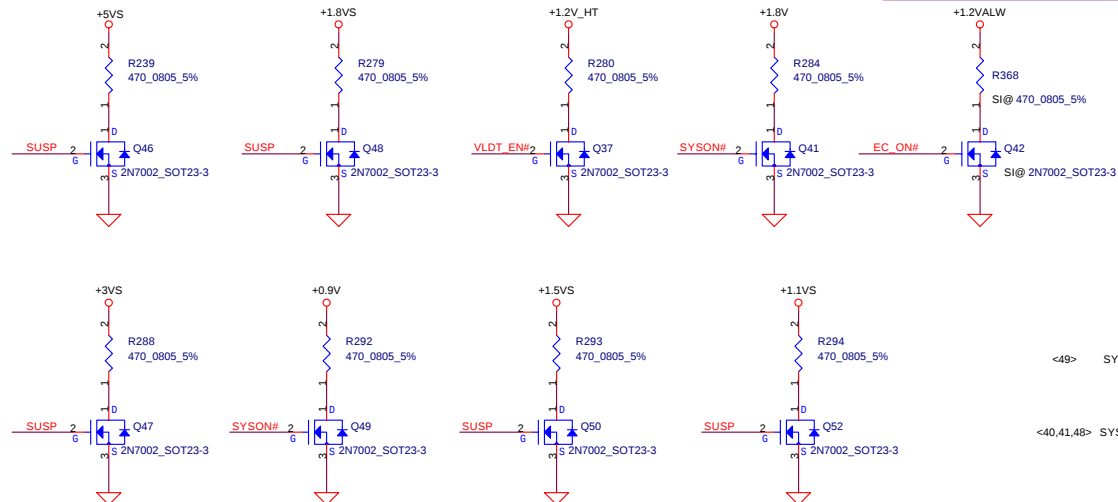


+1.2VALW TO +1.2V



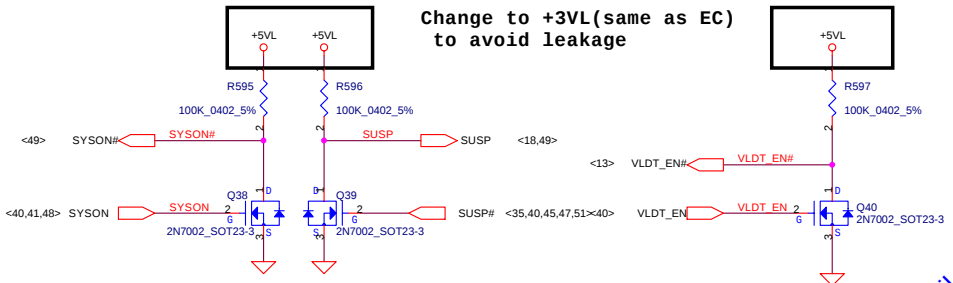
Reserve until SI-1 stage after SB
USB PHY power saving report

Discharge circuit



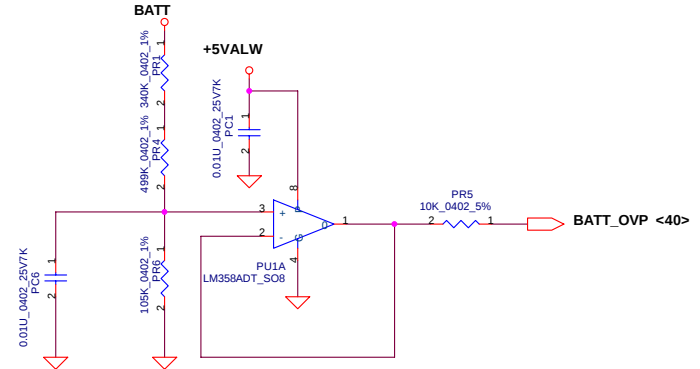
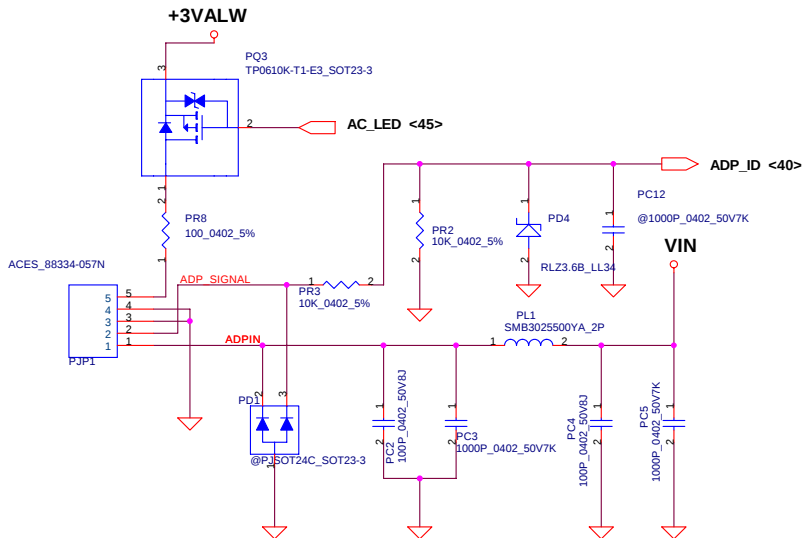
09/13 update (Del +V_DDR_MCH_REFF)

Change to +3VL(same as EC)
to avoid leakage

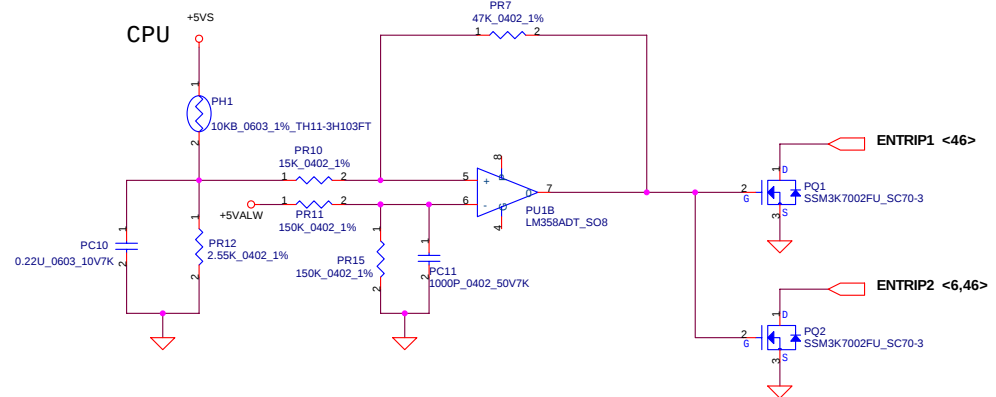
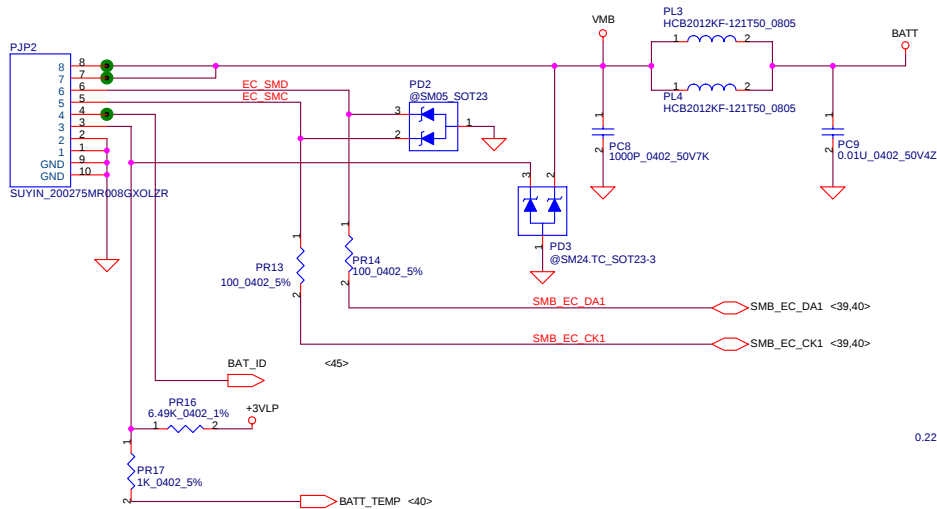


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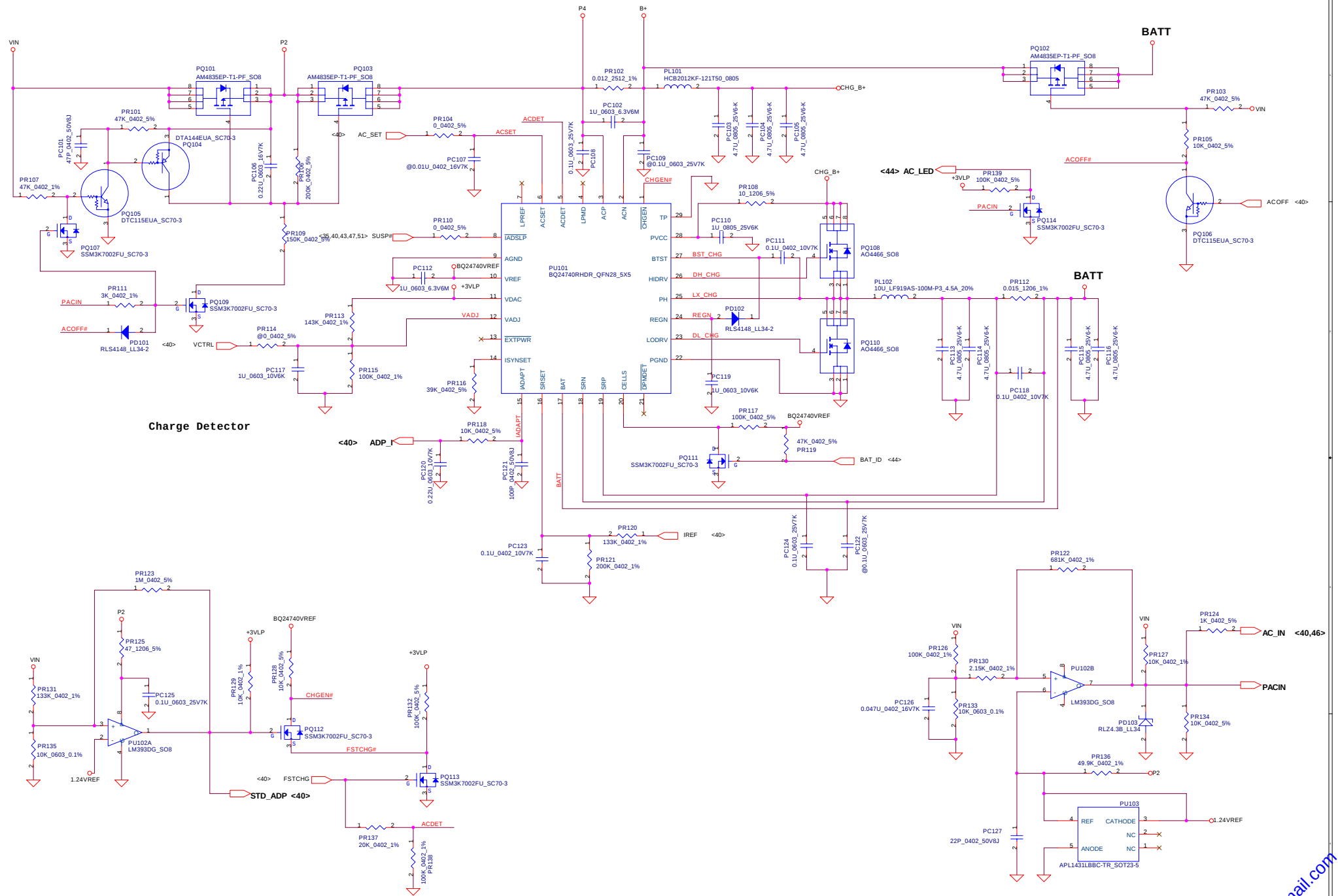
BATT1
45@CR2032 RTC BATTERY



PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C

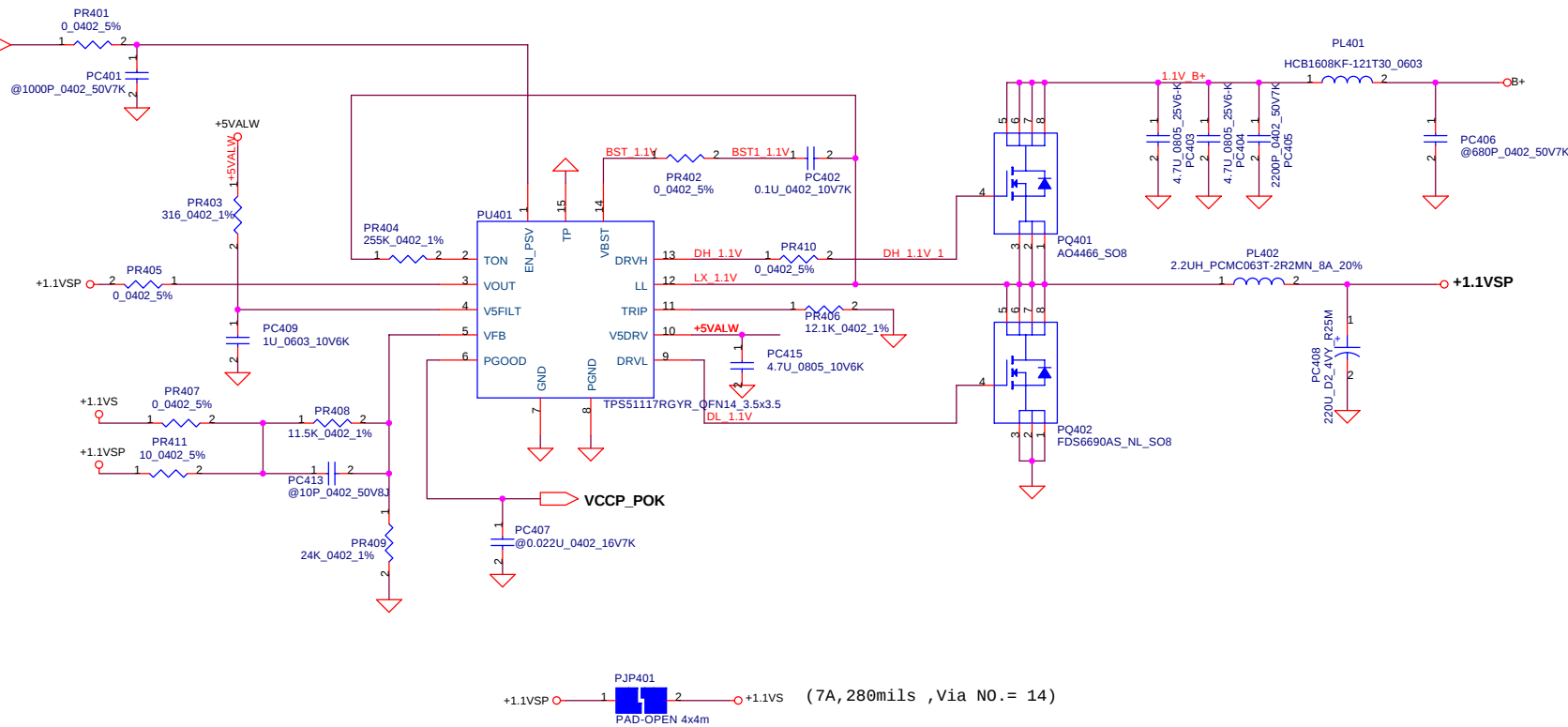


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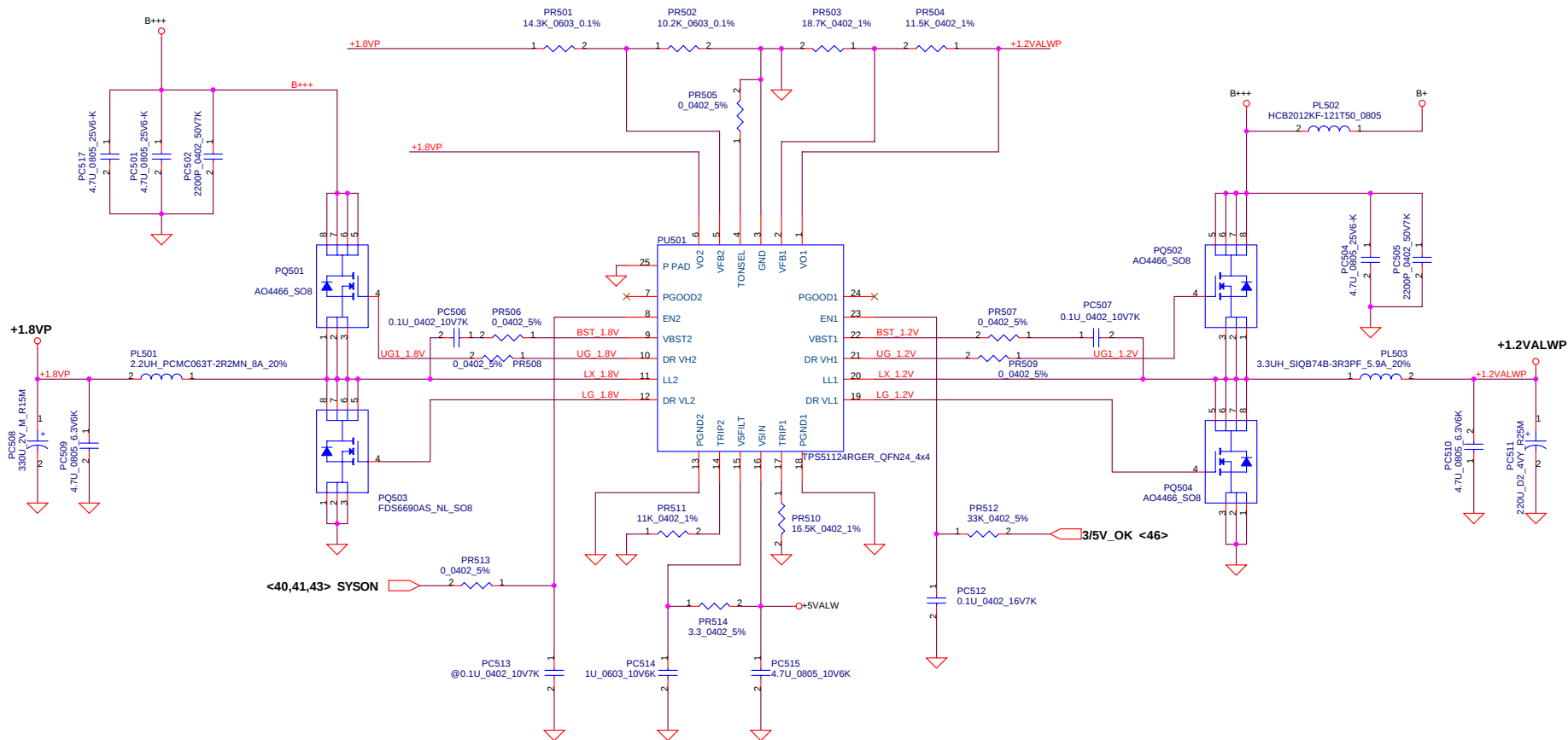


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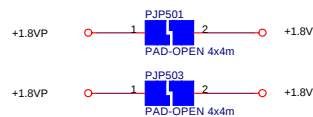
5,40,43,45,51> SUSP#



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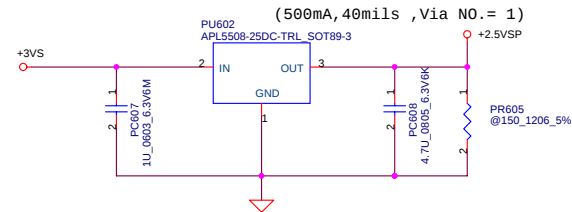
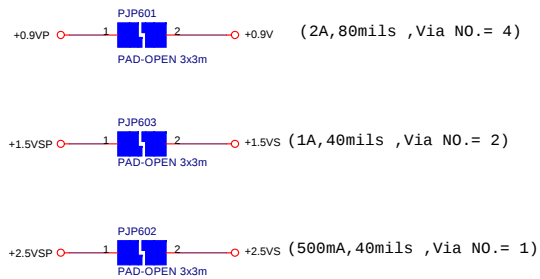
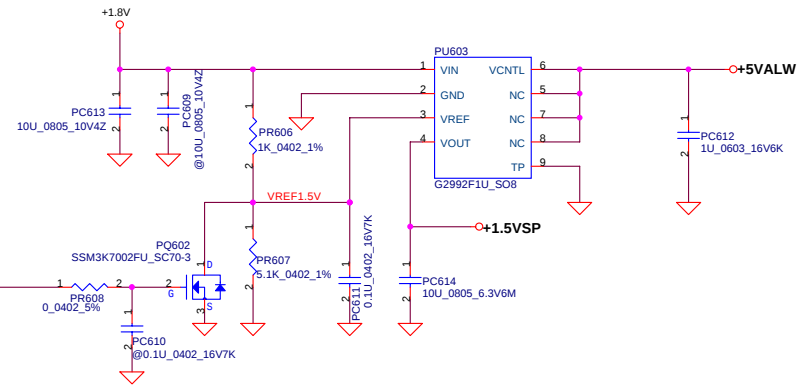
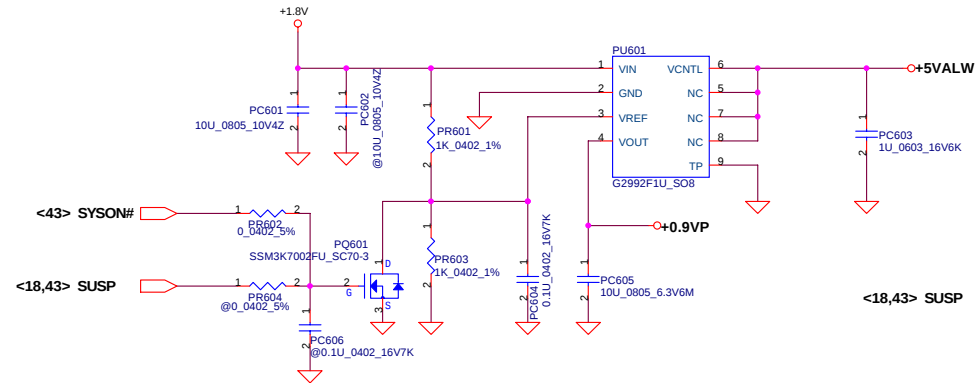
(8A,320mils ,Via N0.=16)



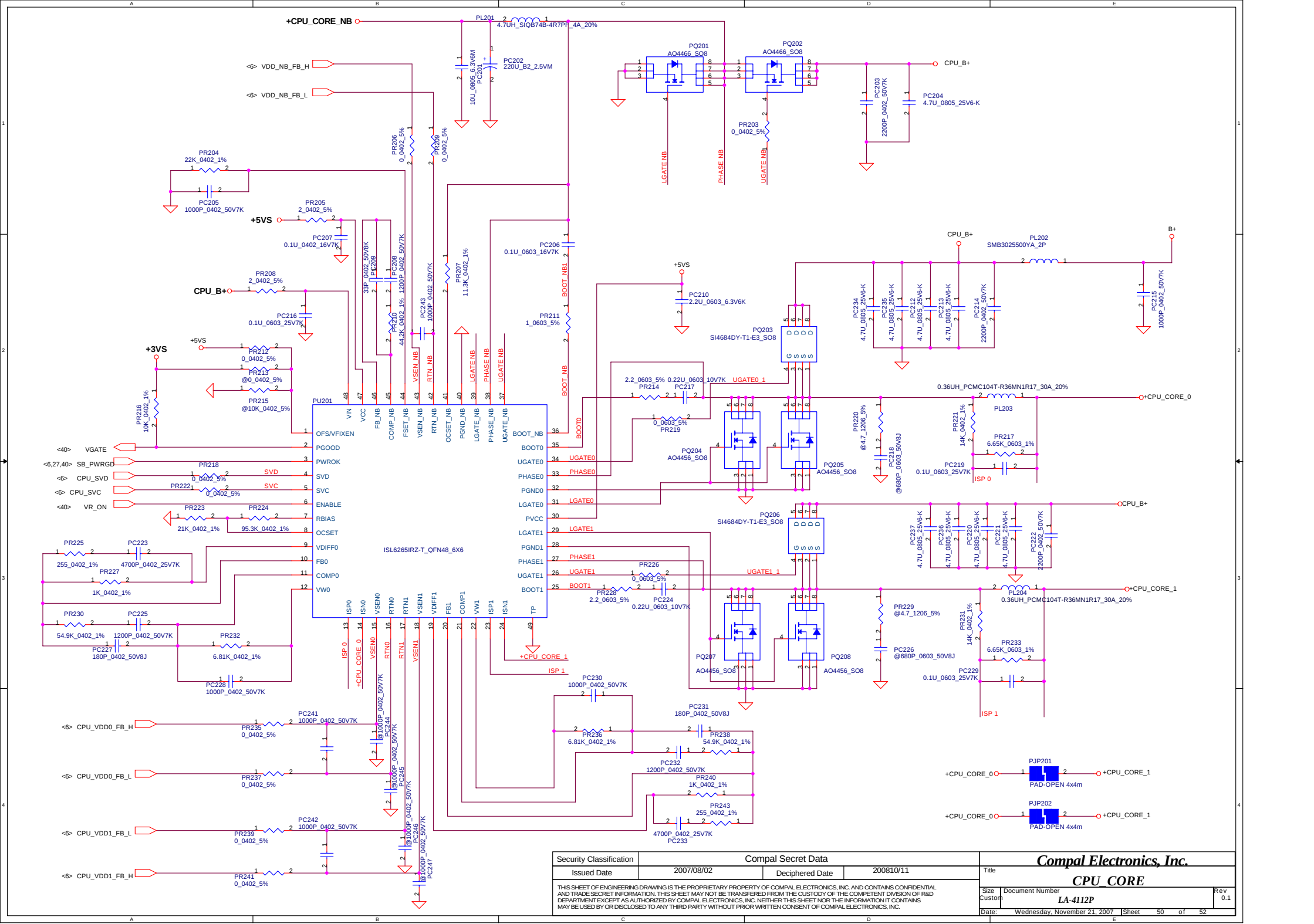
(4A,160mils ,Via N0.=8)

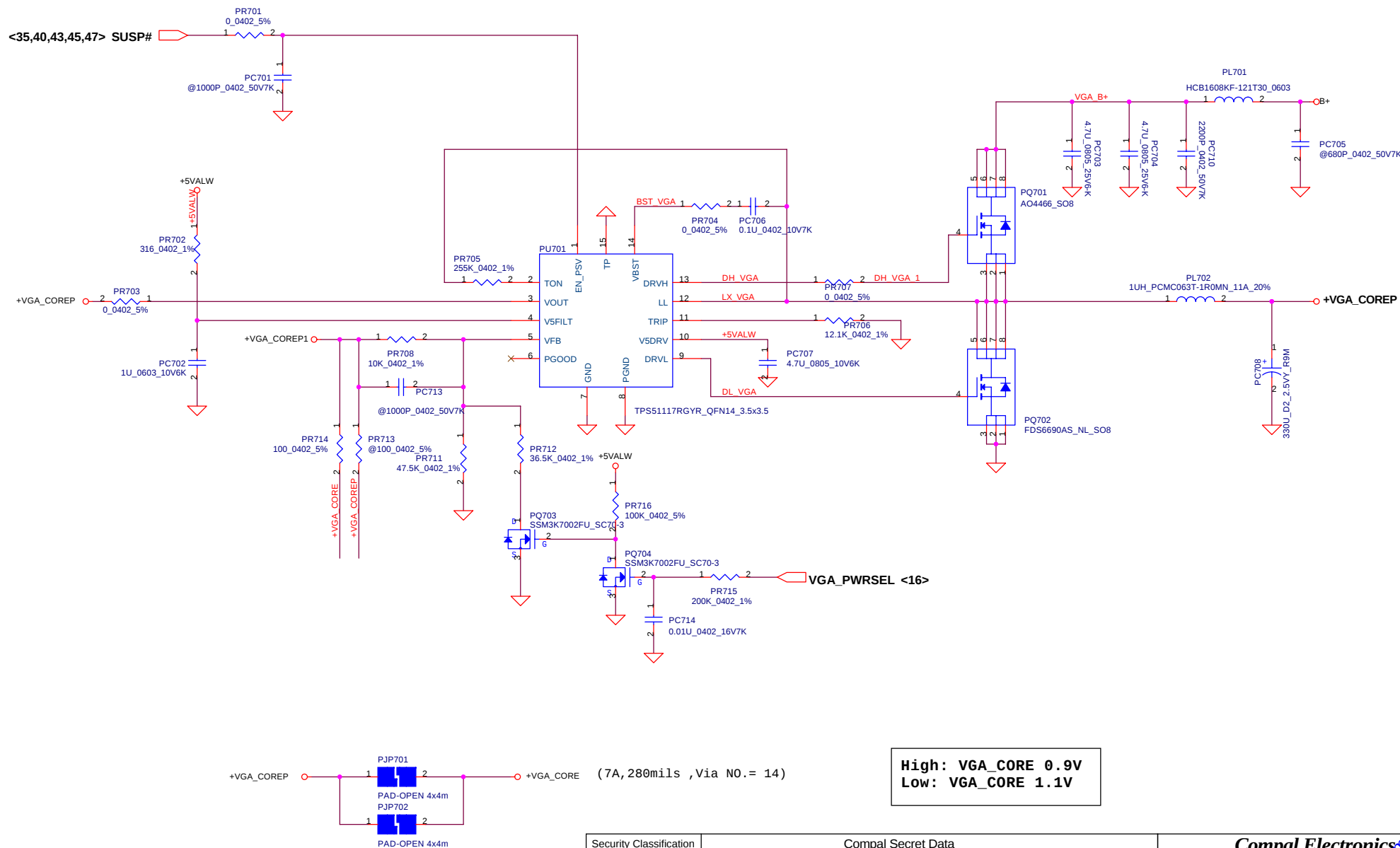


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