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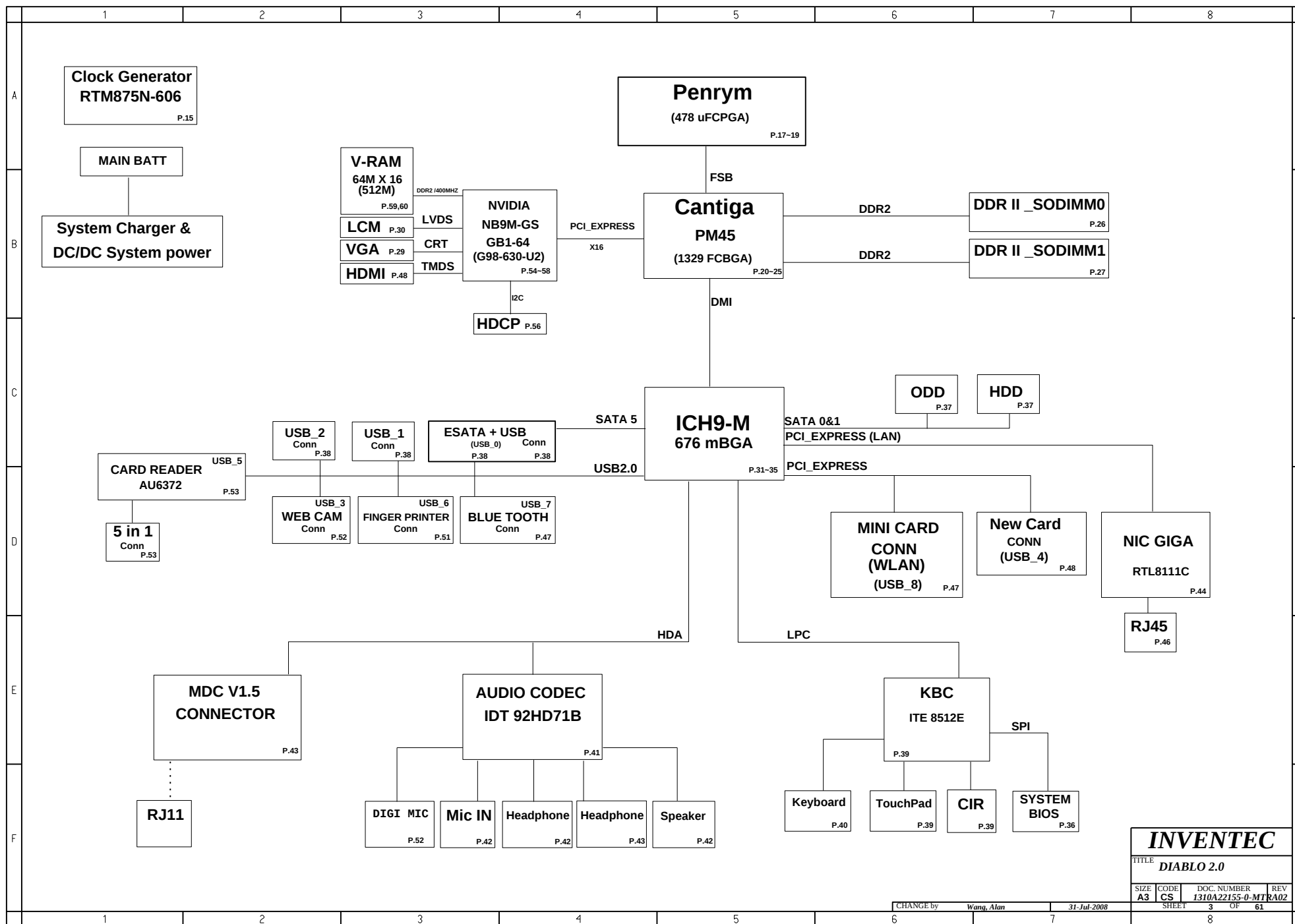
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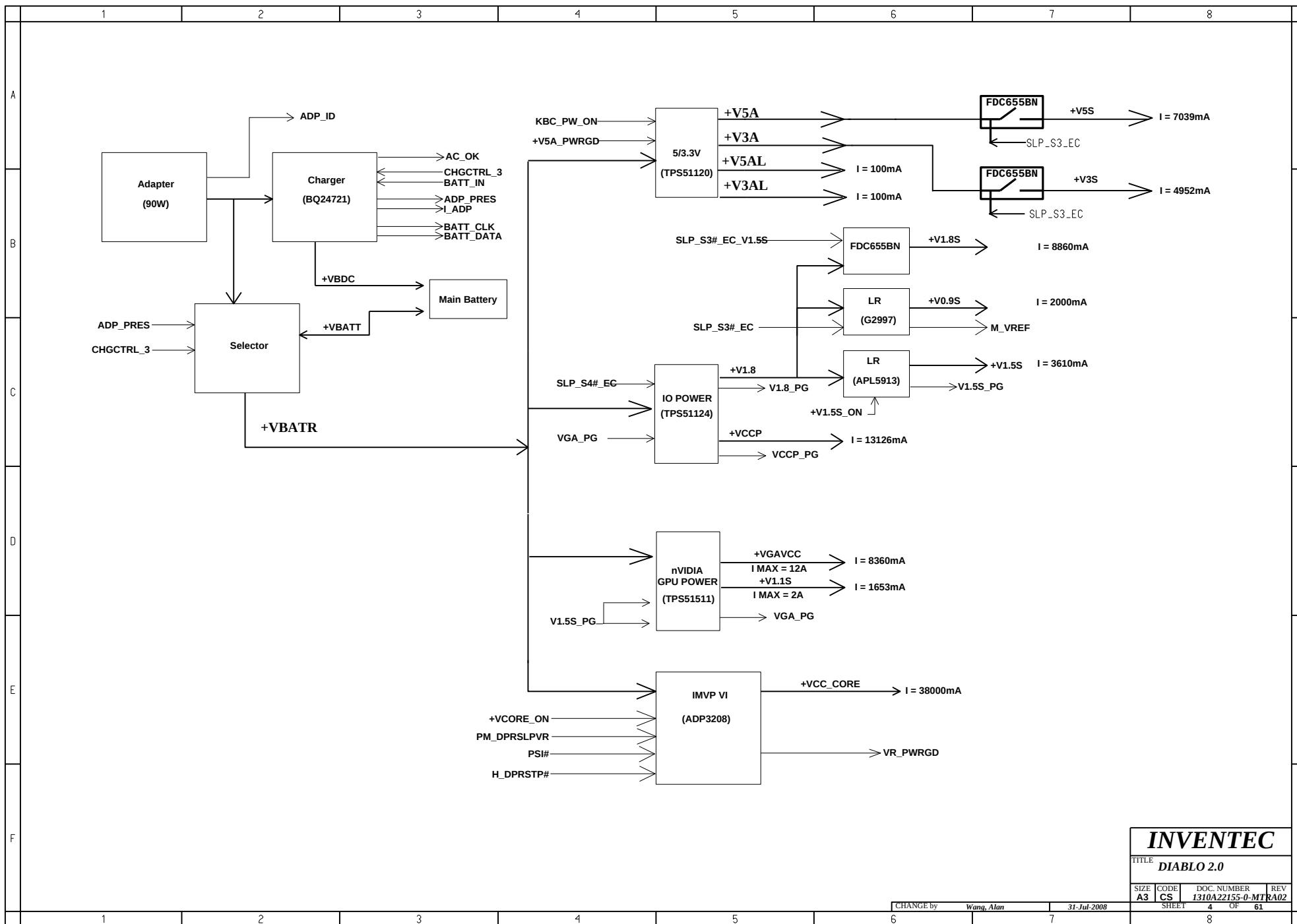
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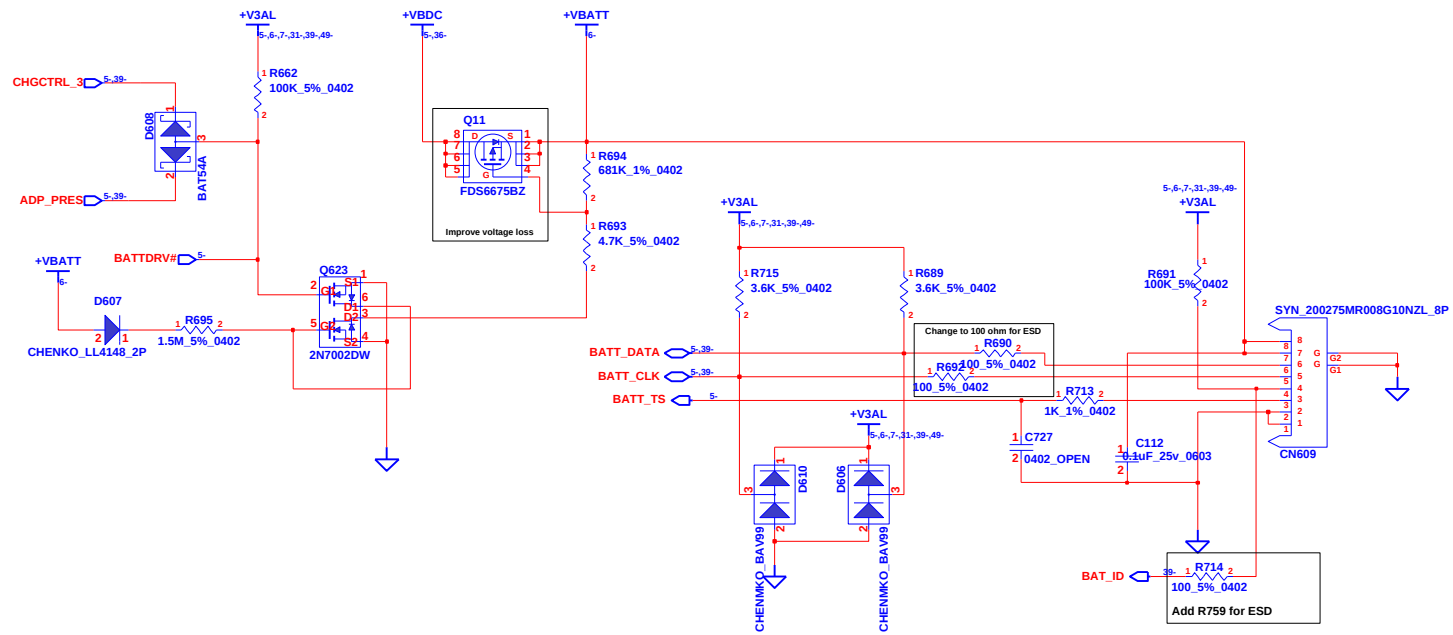
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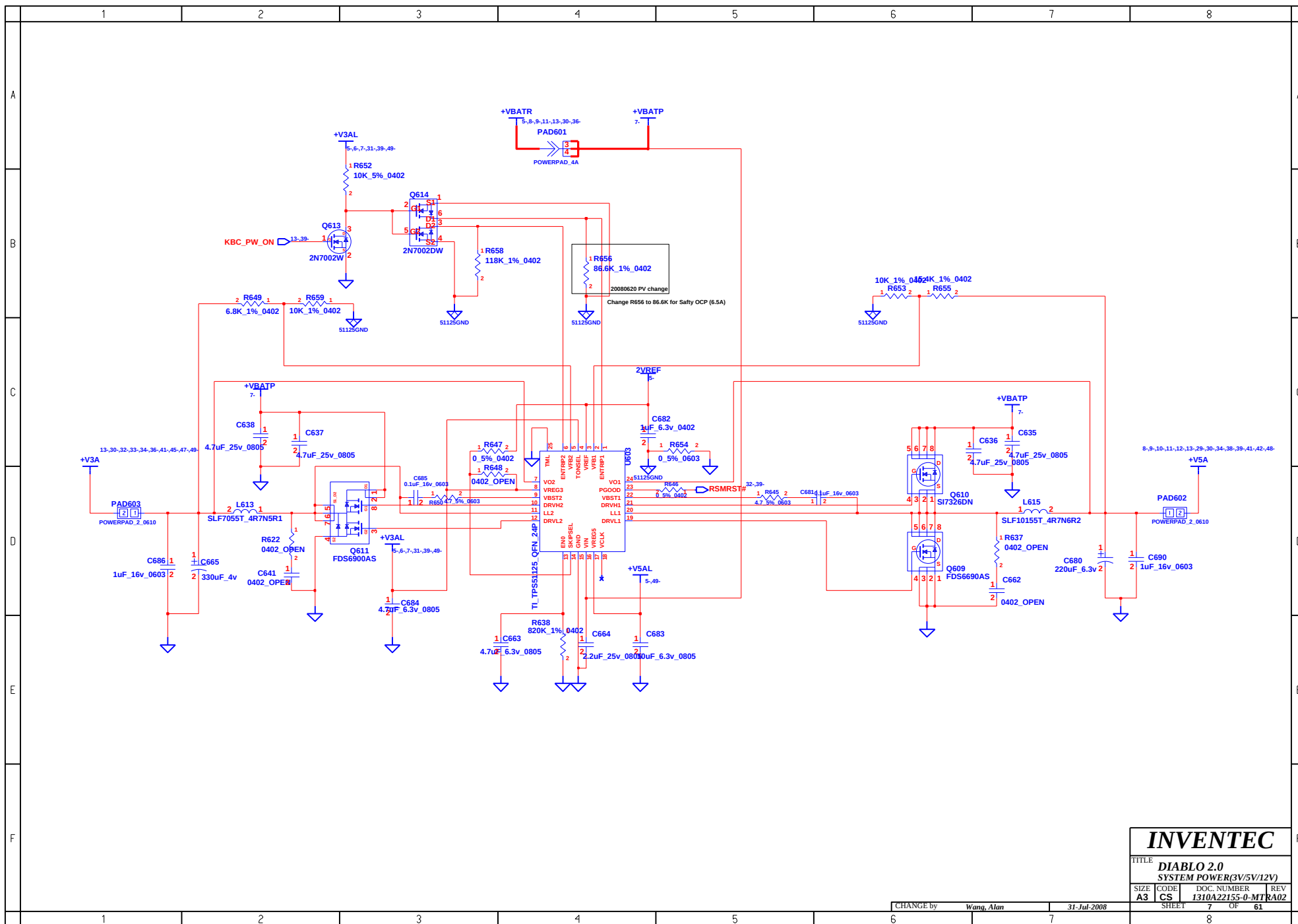


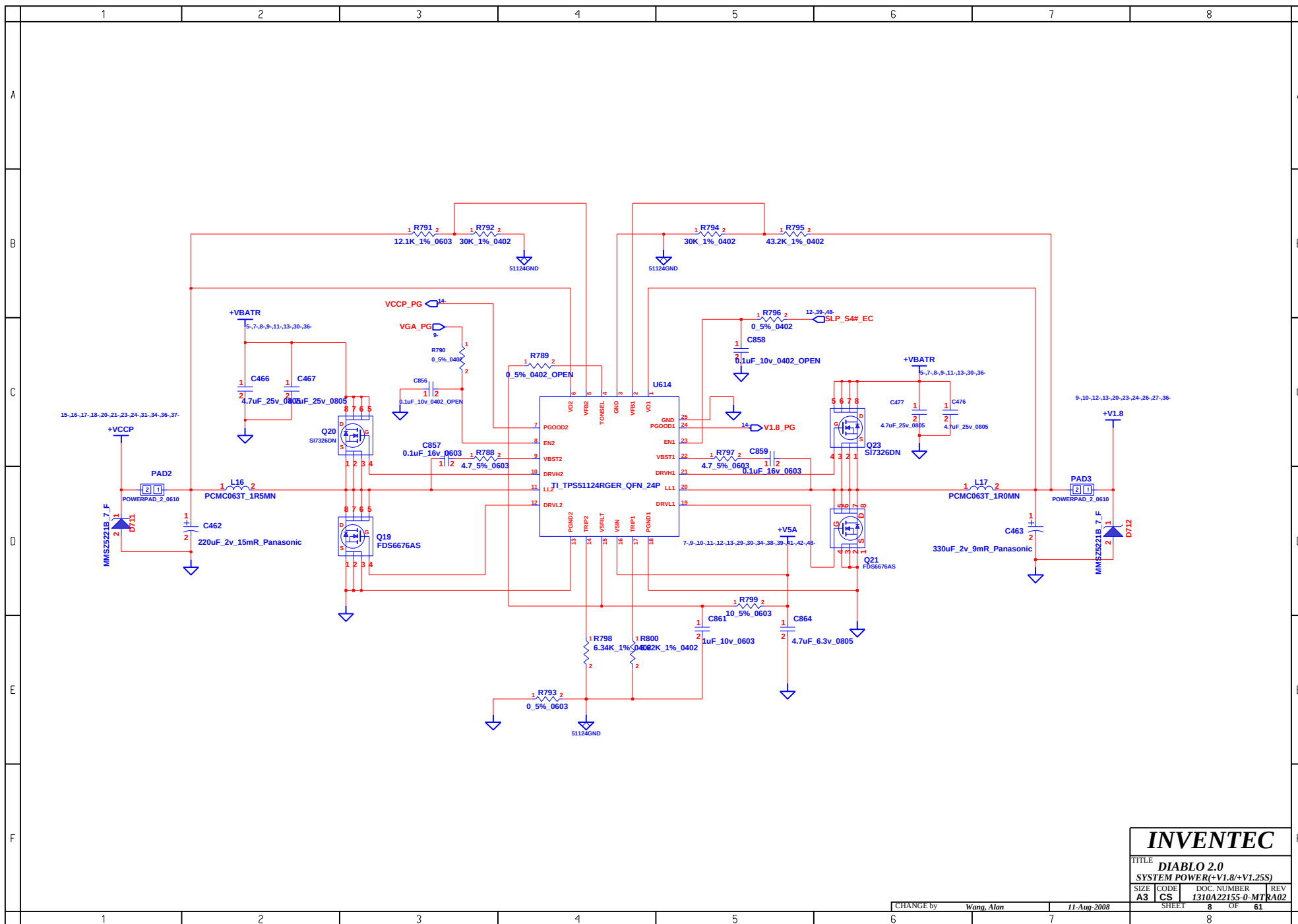
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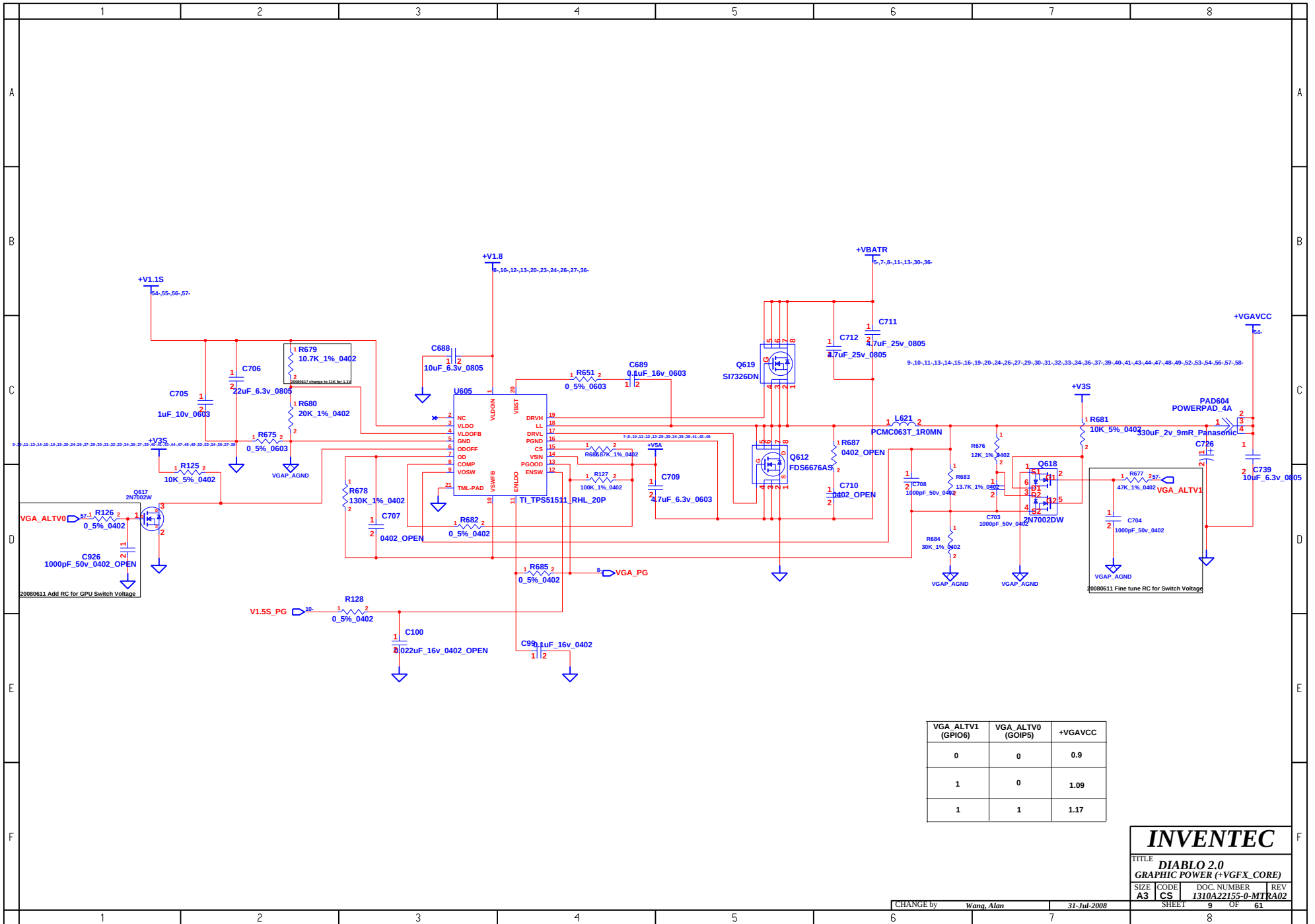
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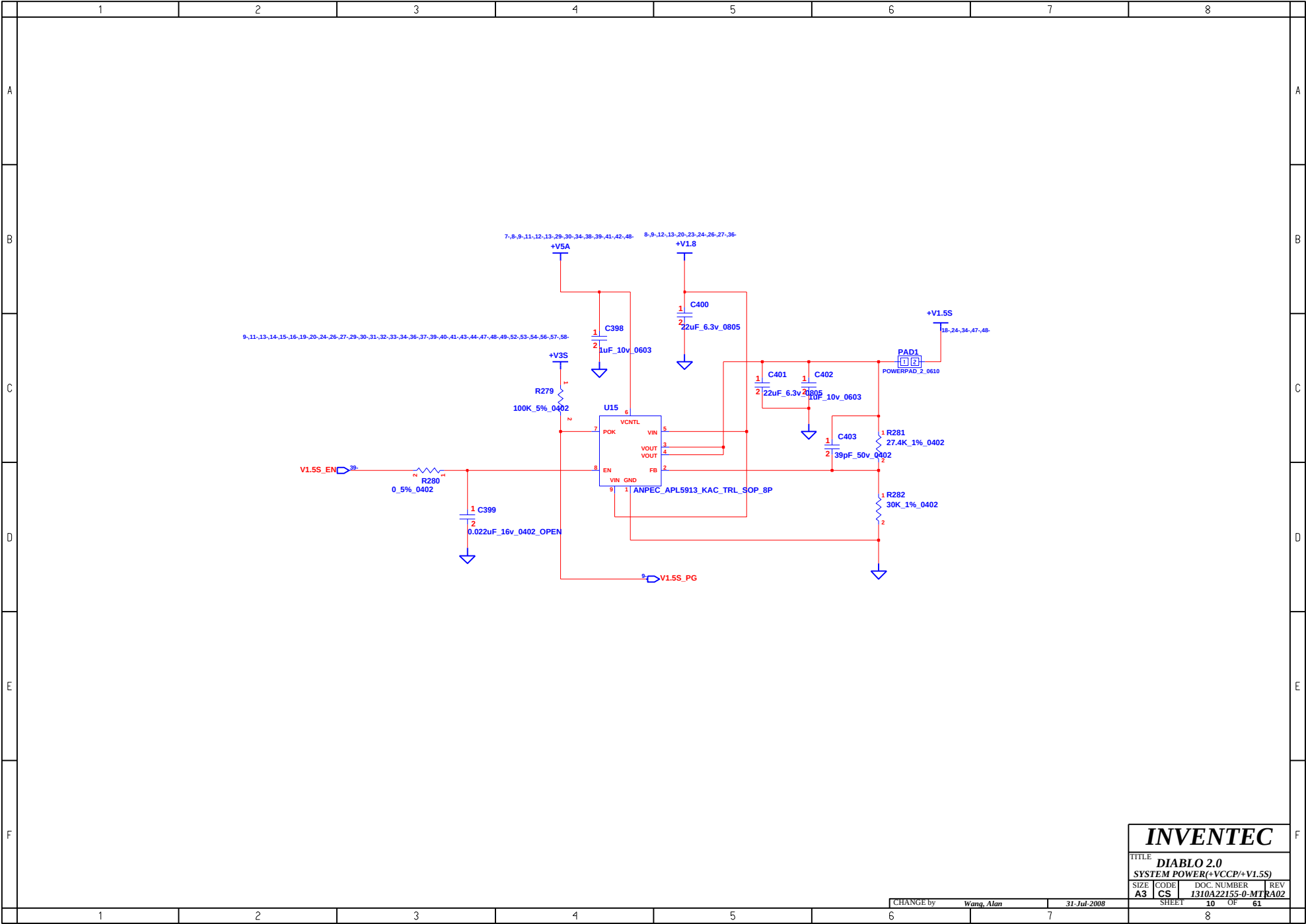
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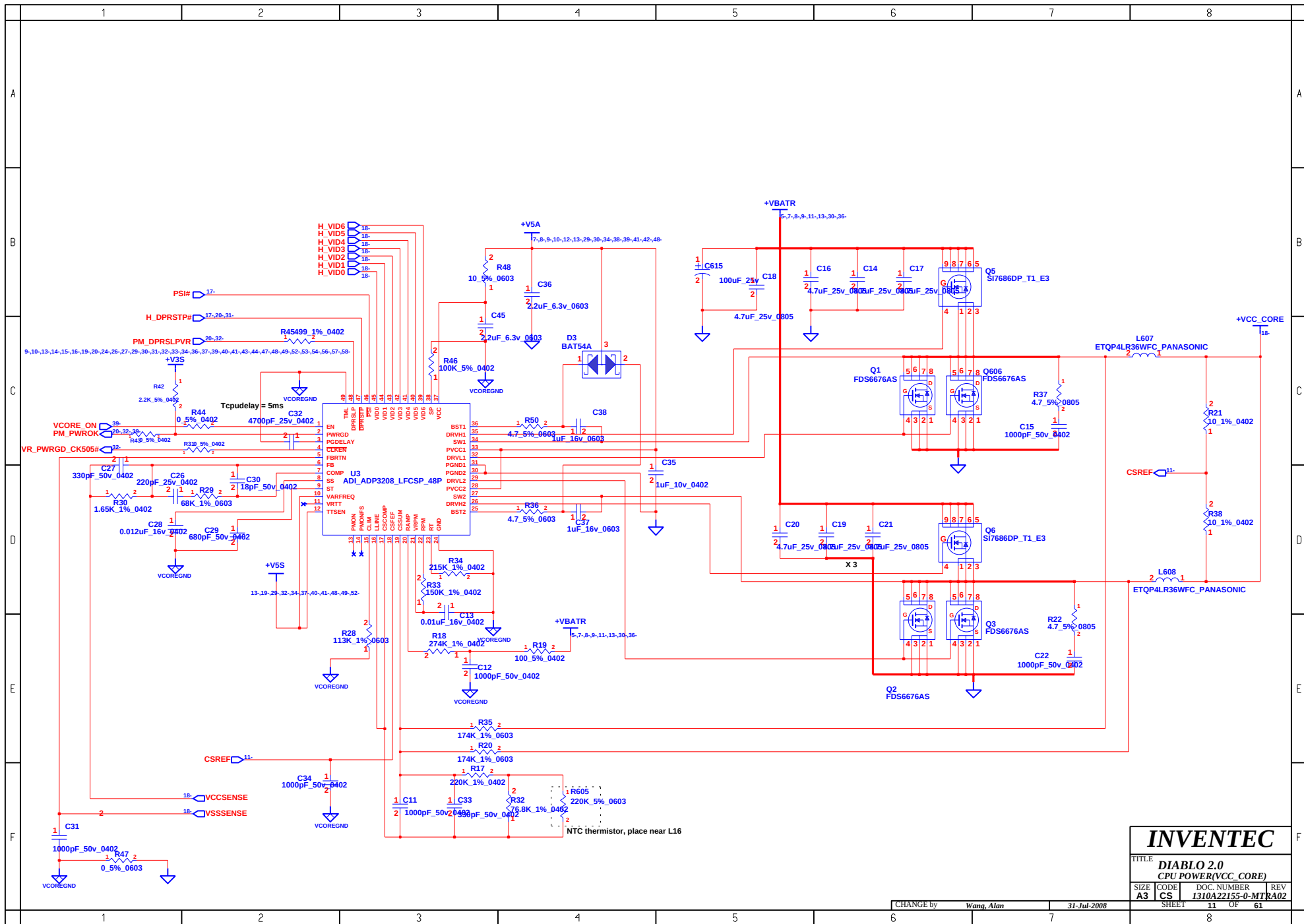
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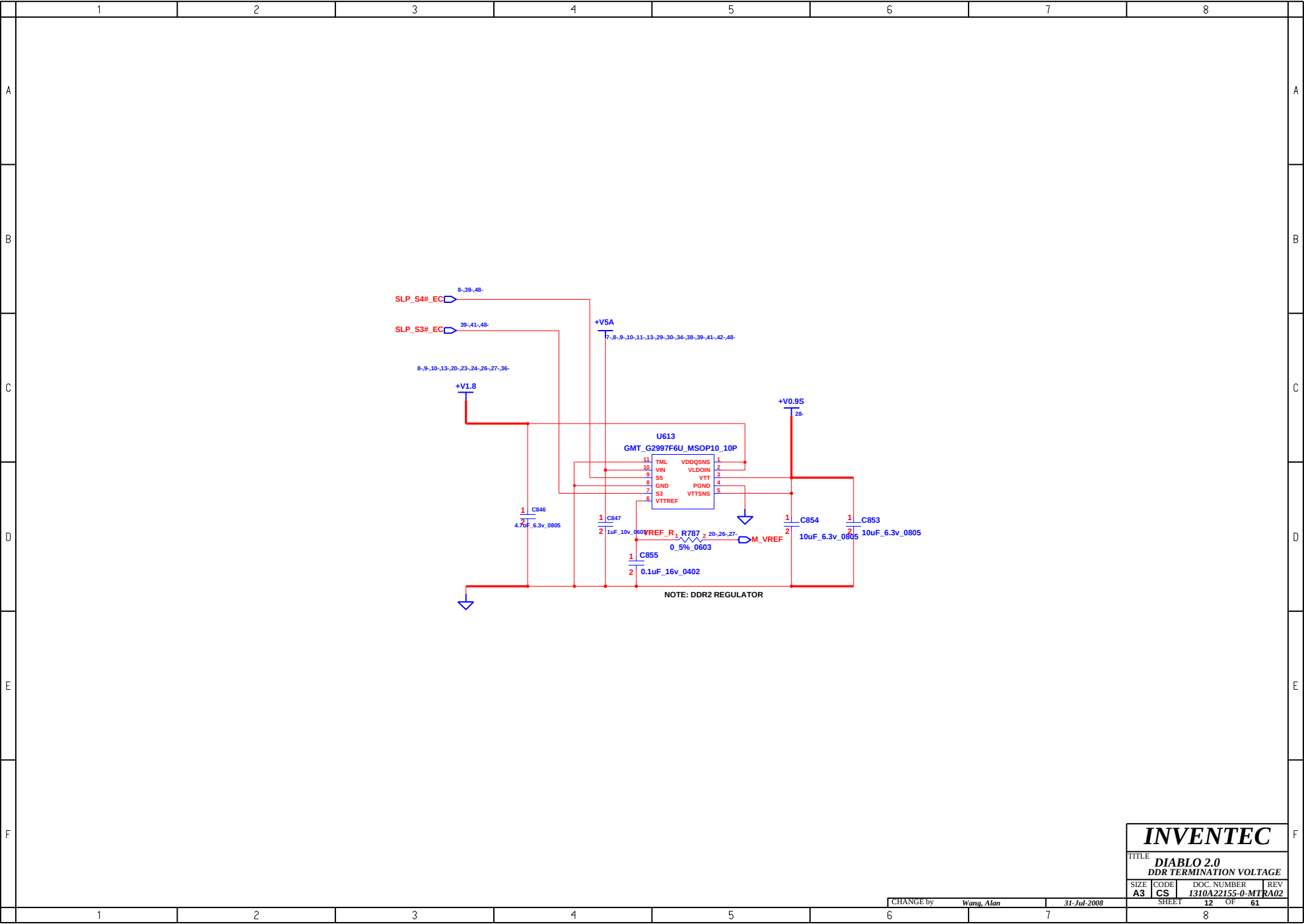
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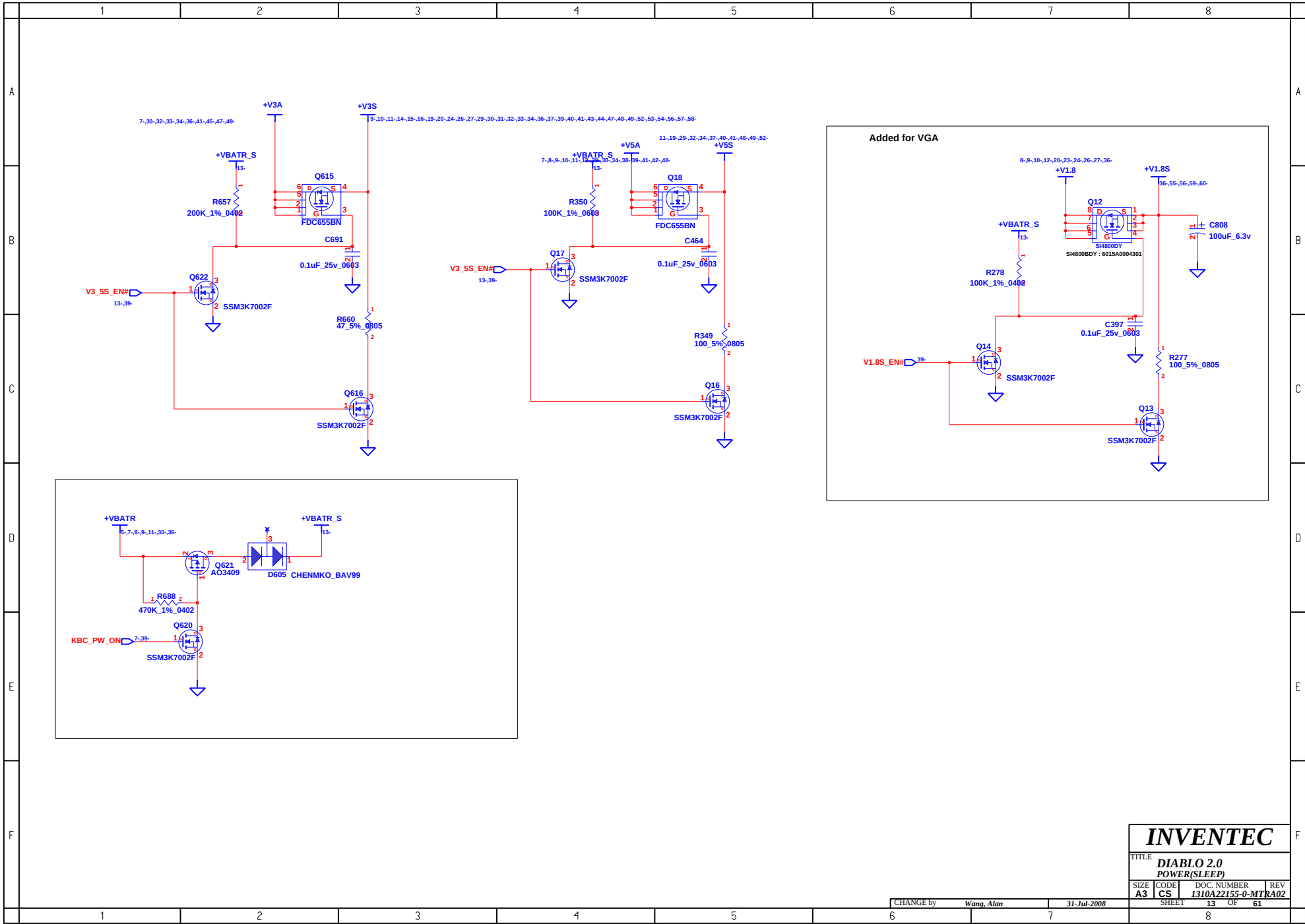
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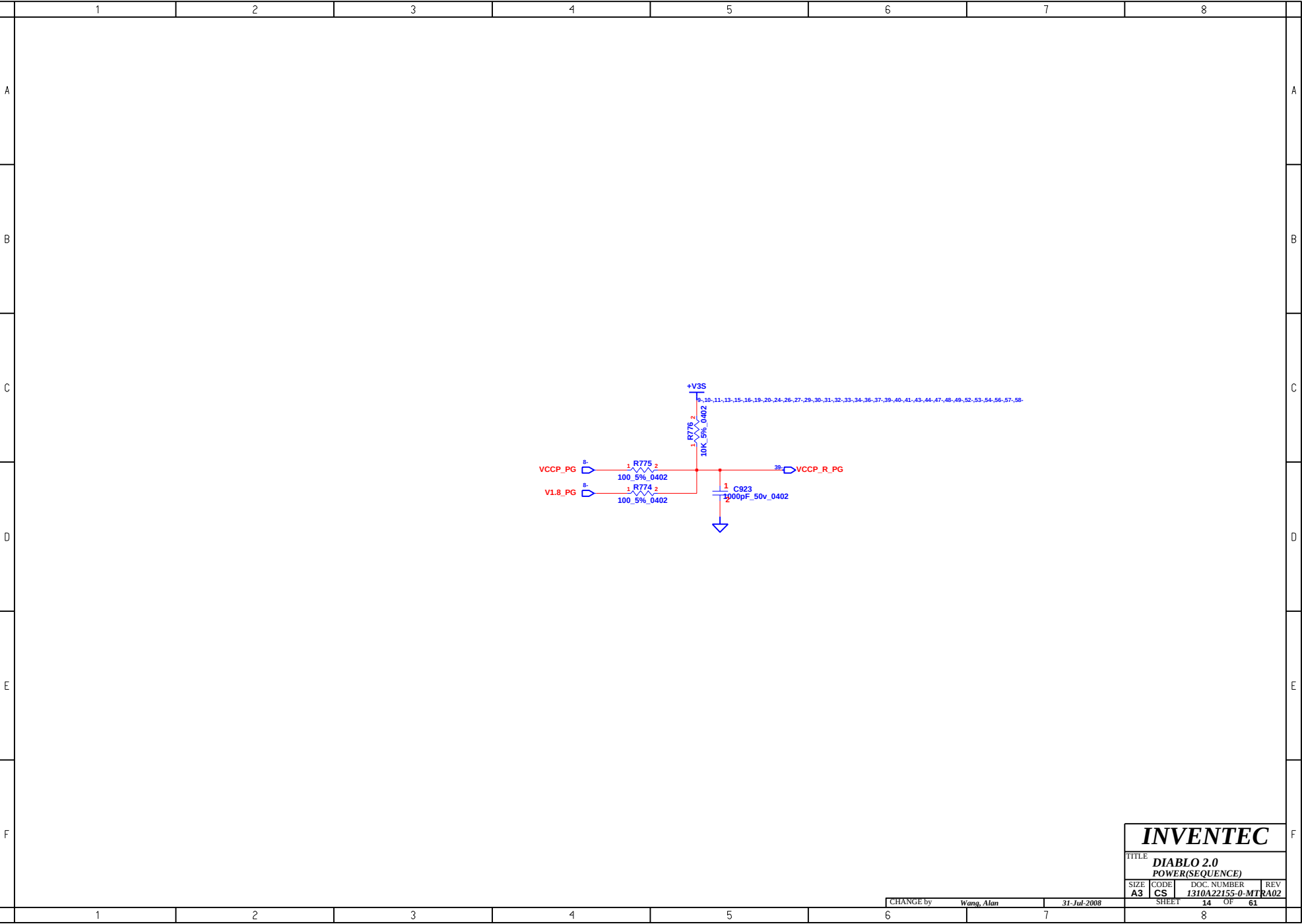
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POWER(SLEEP)			
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CHANGE by		31-Jul-2008	
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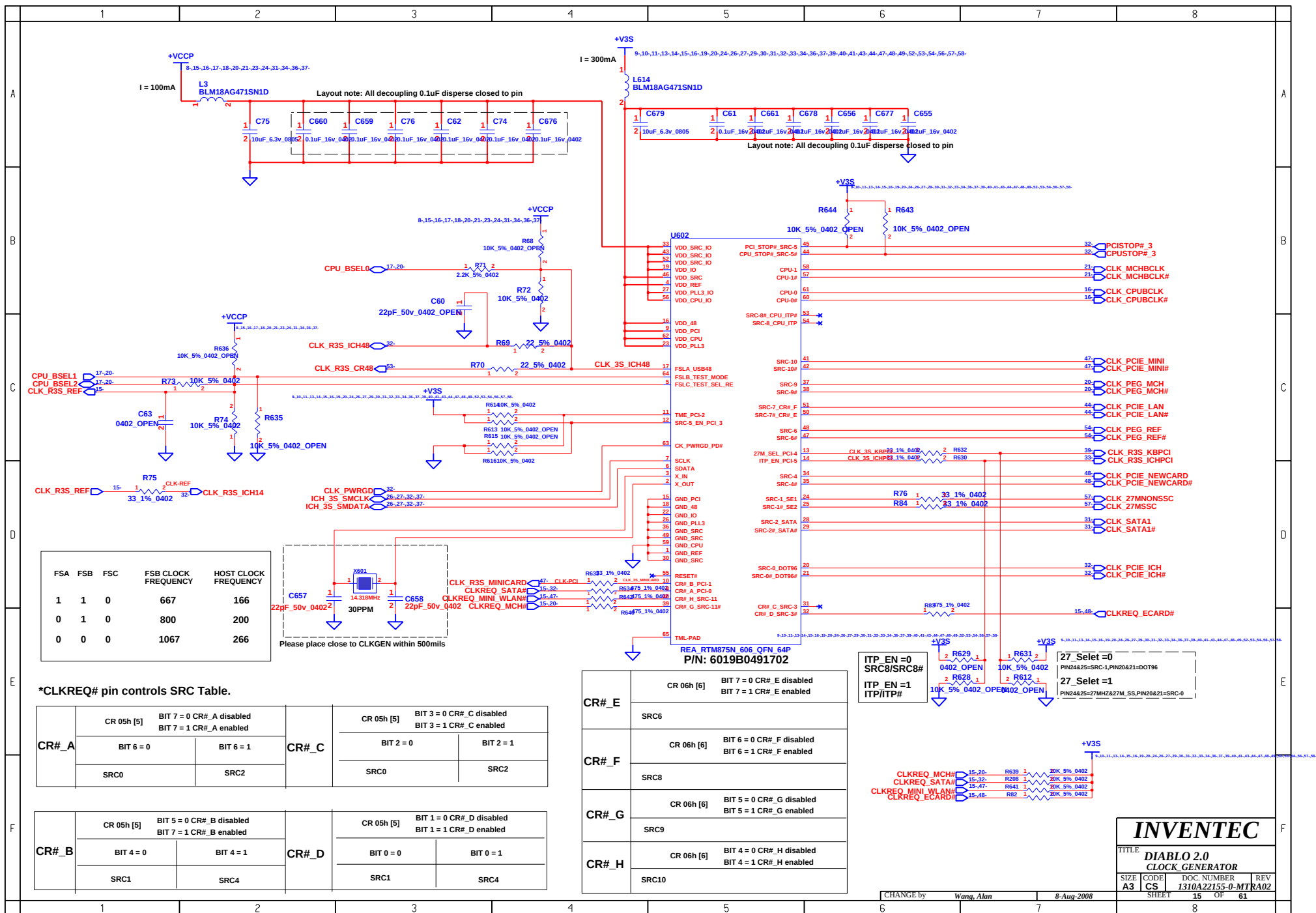
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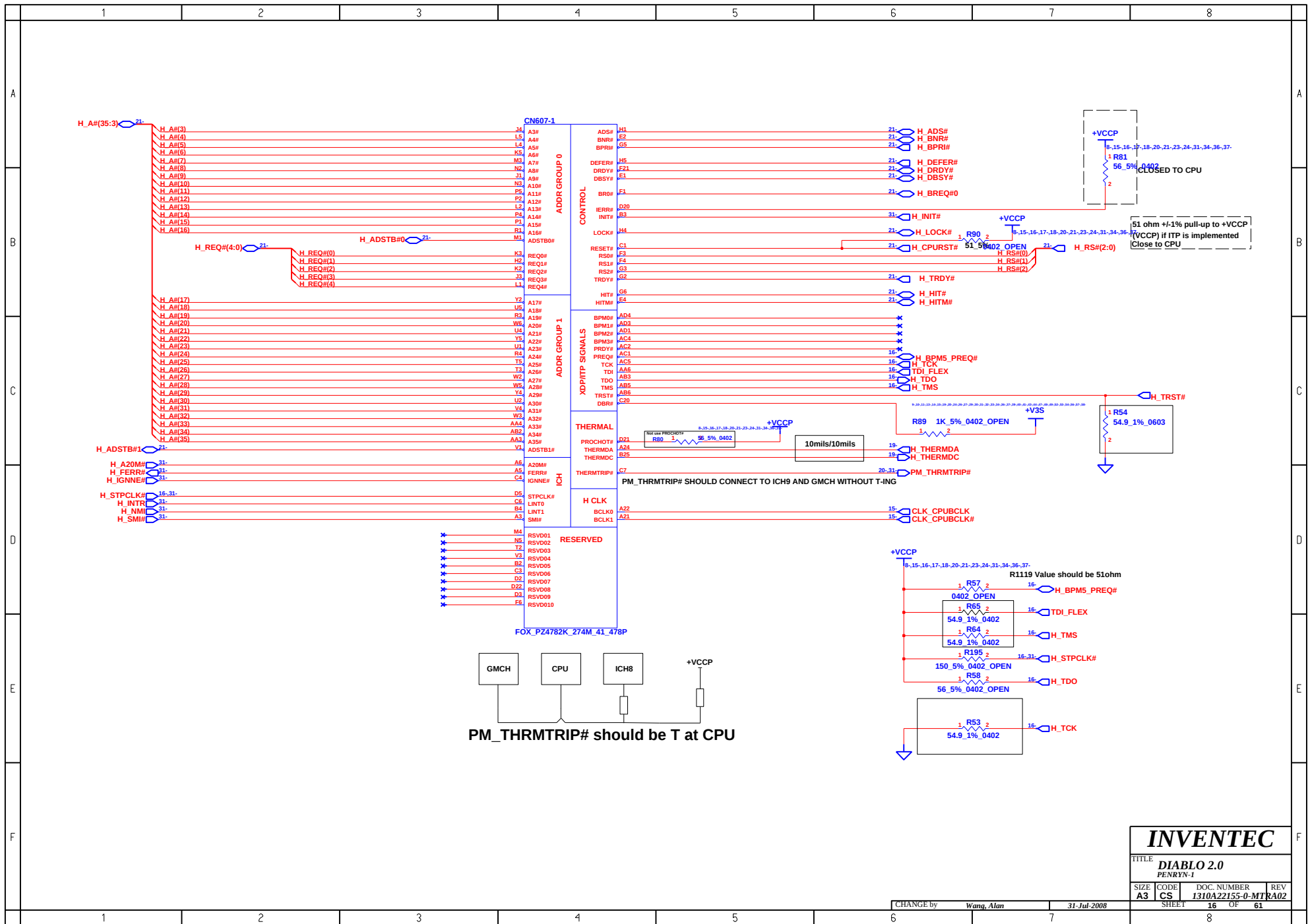
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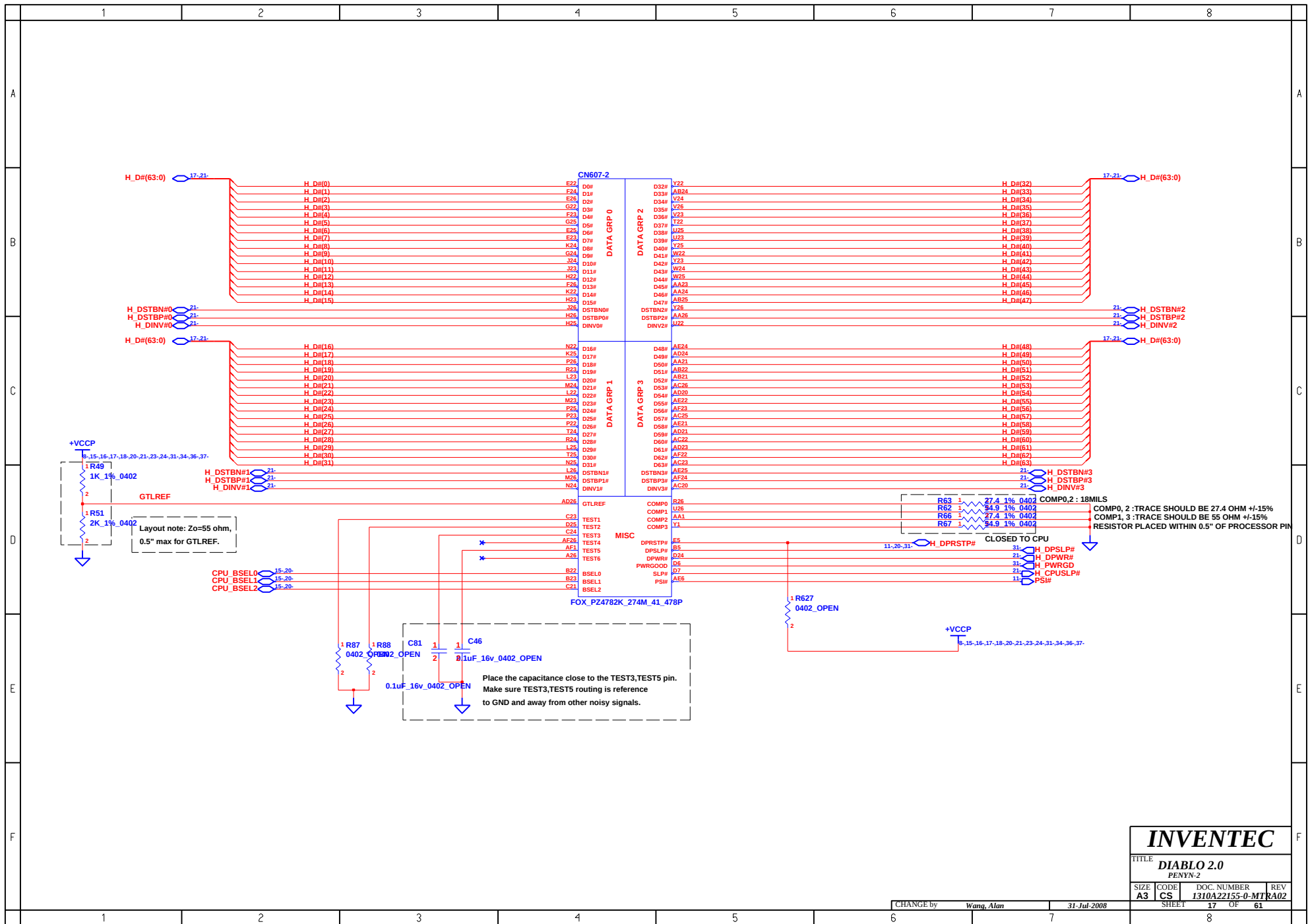
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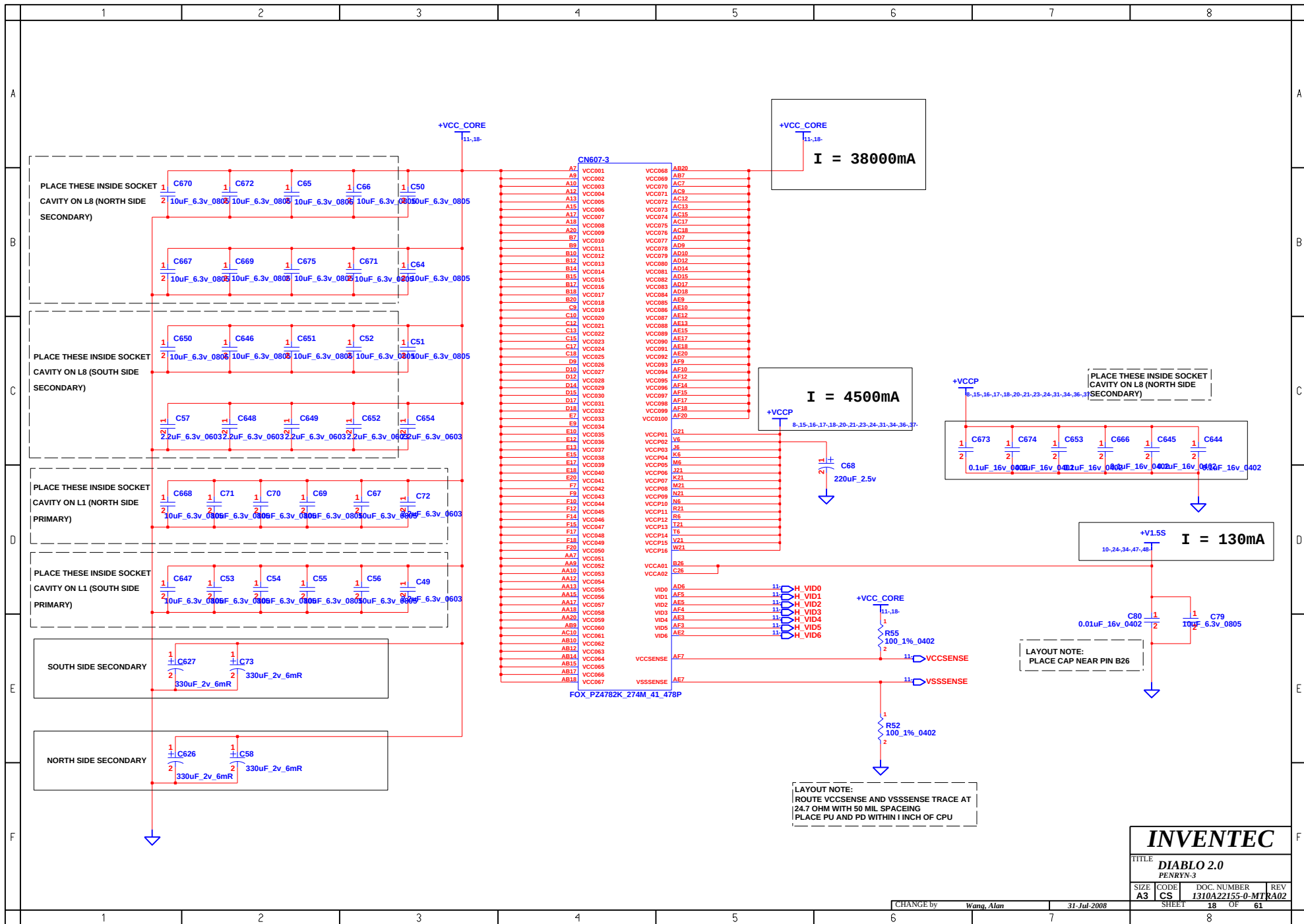


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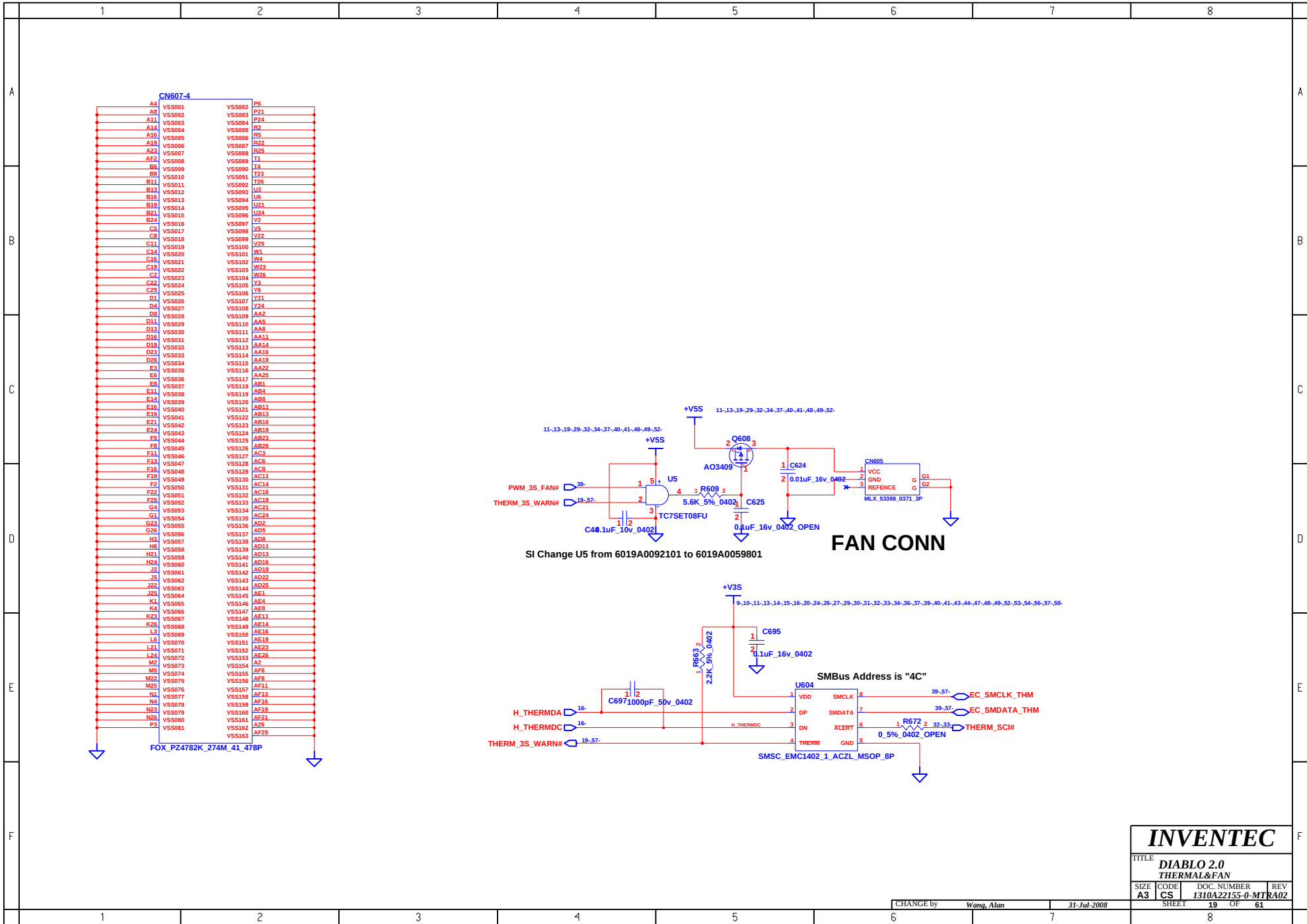
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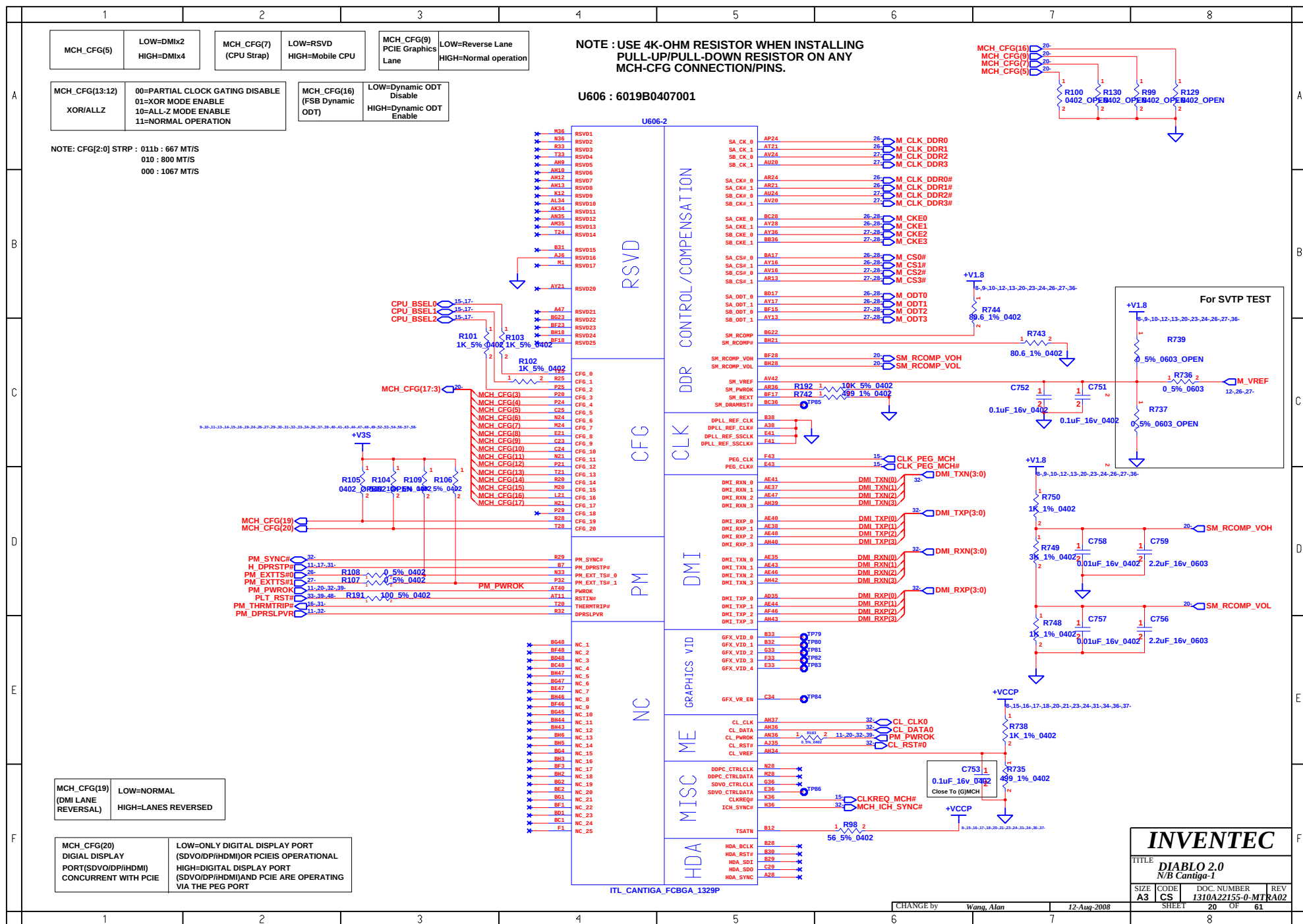
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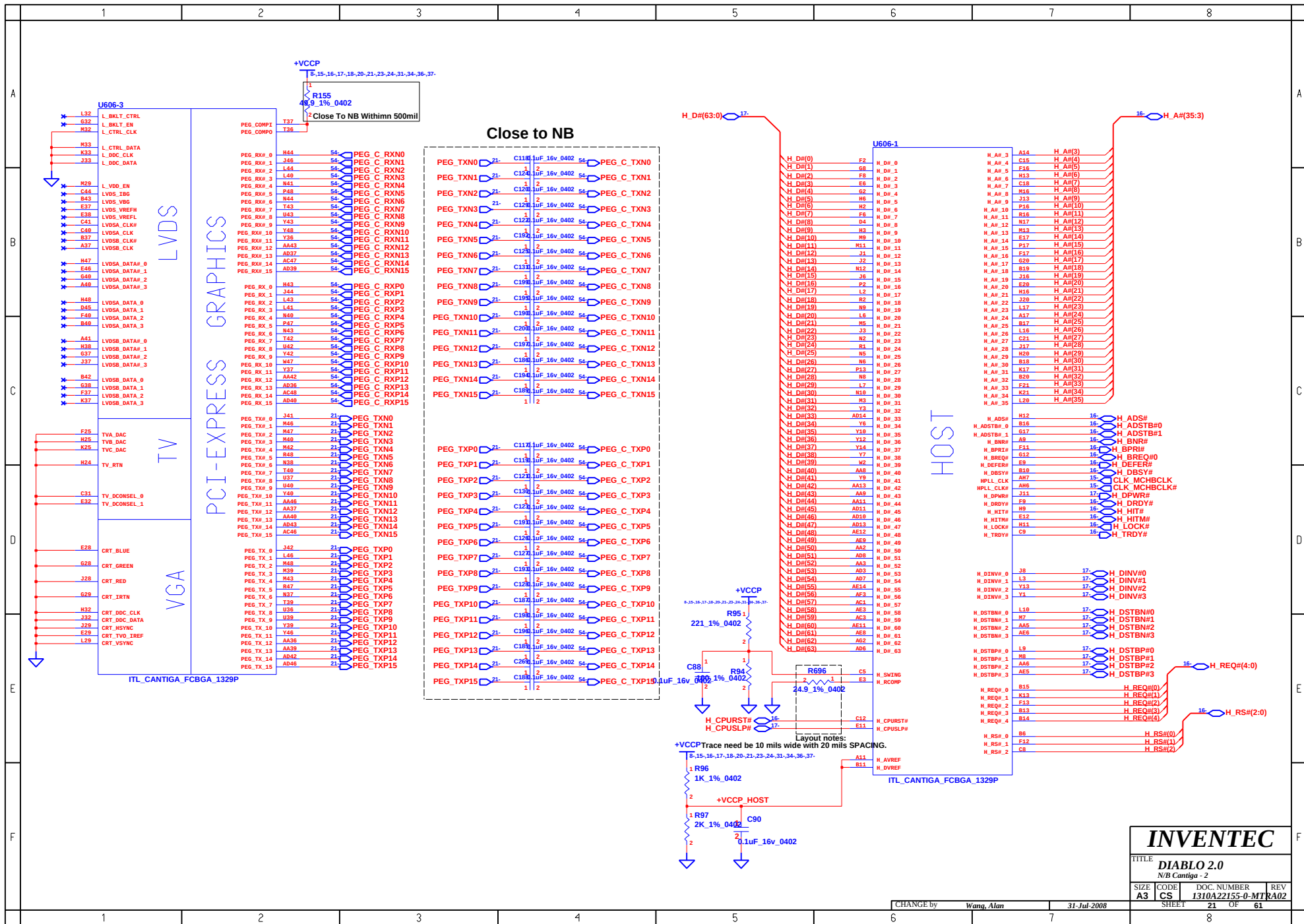
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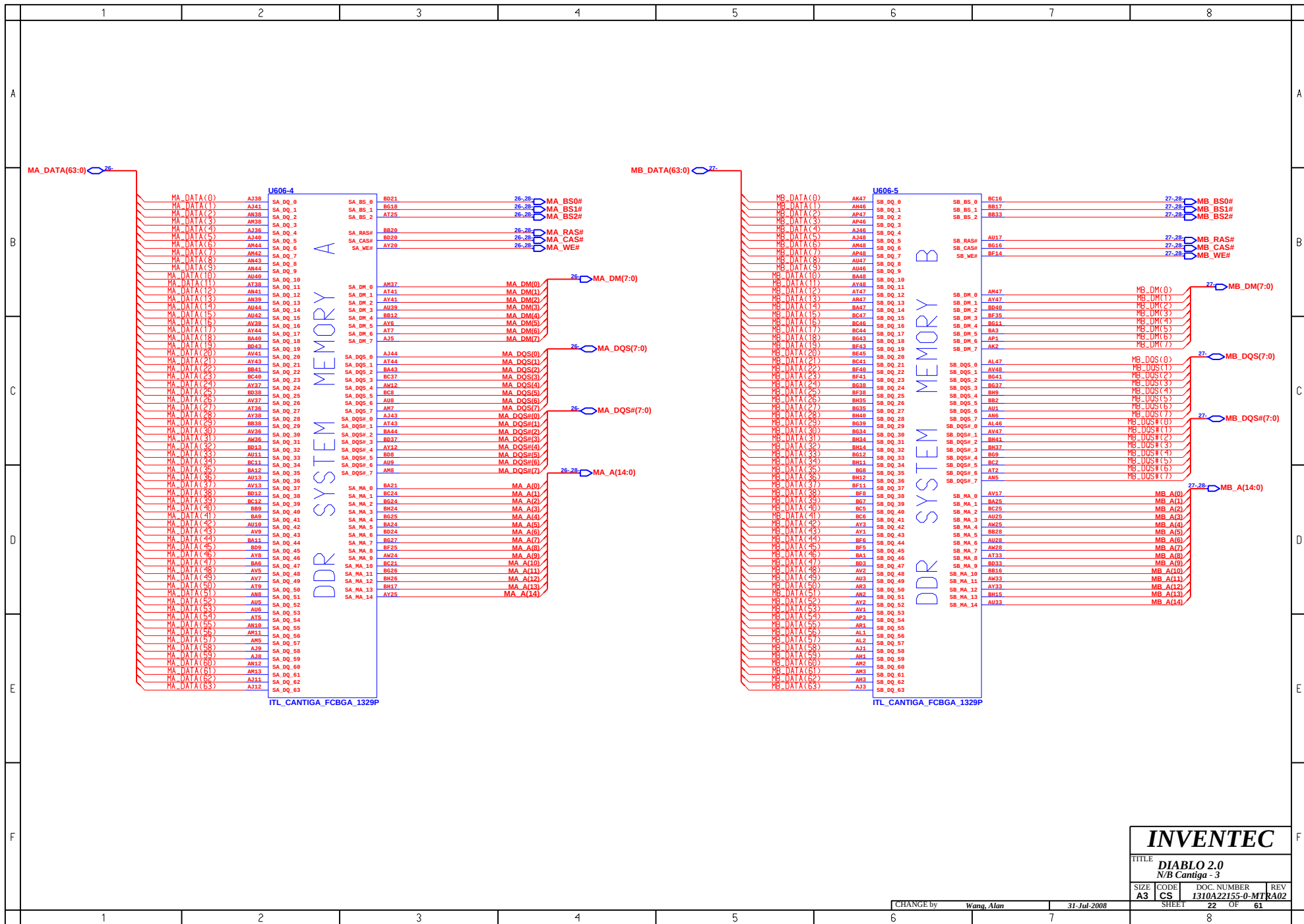


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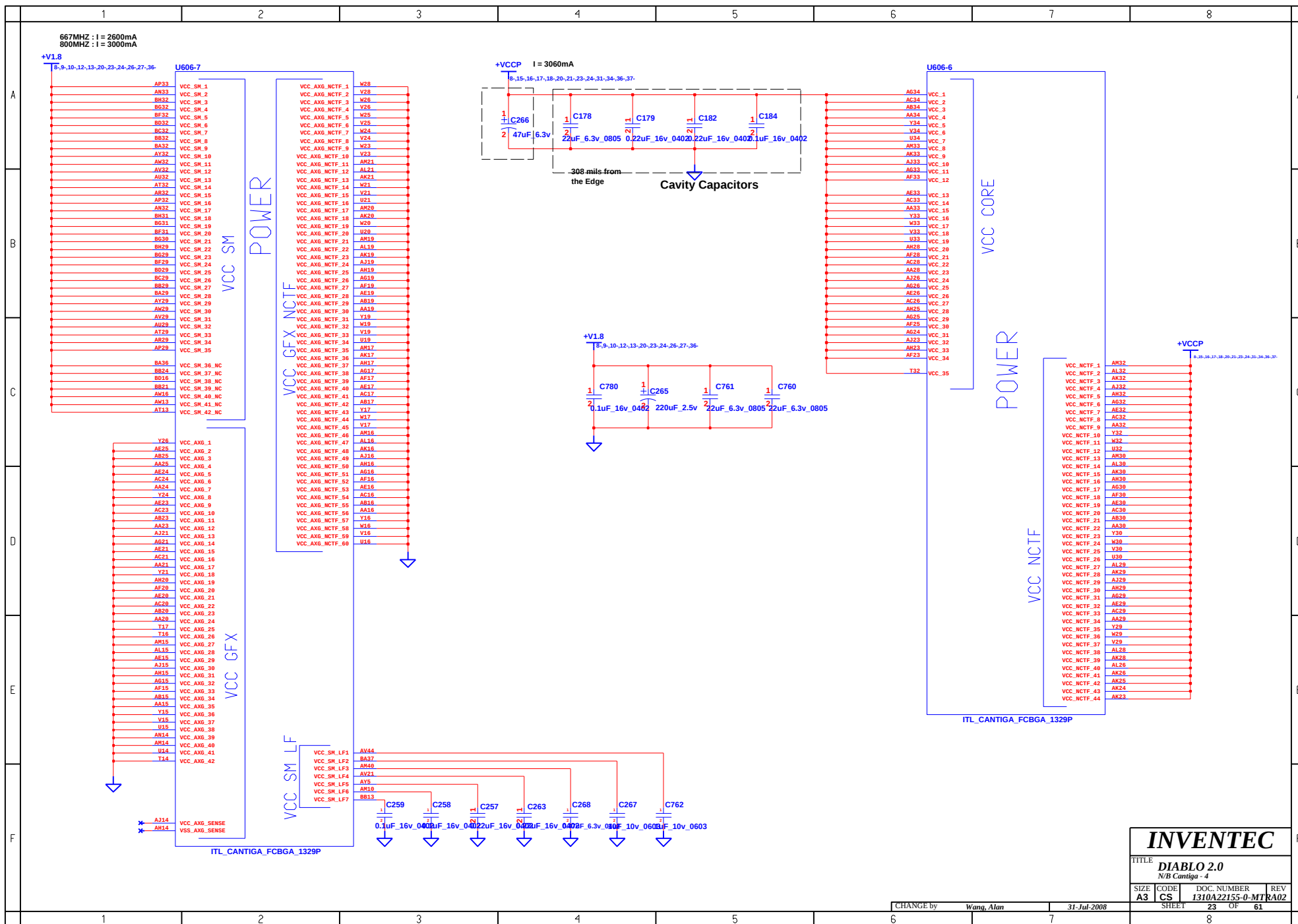
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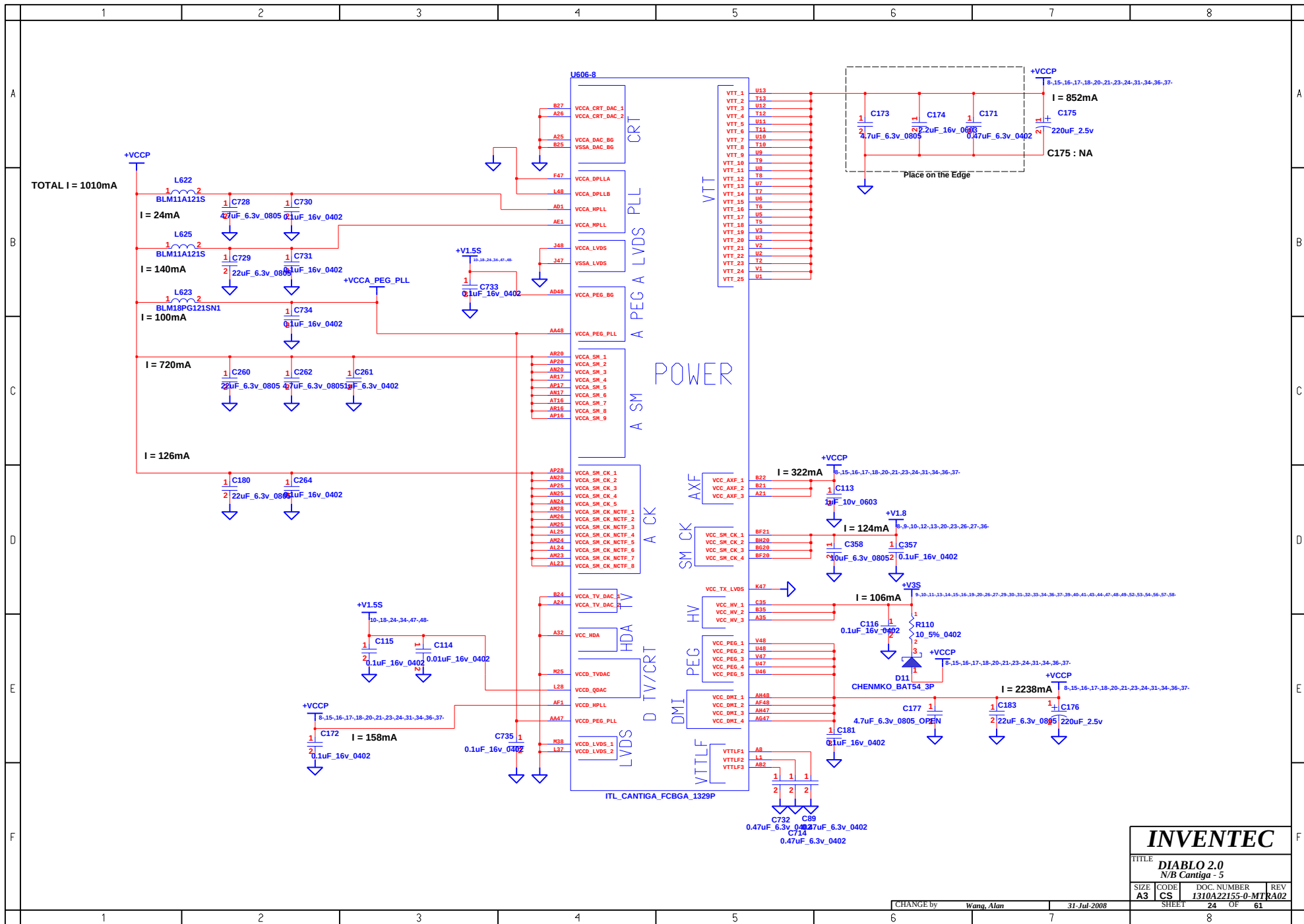
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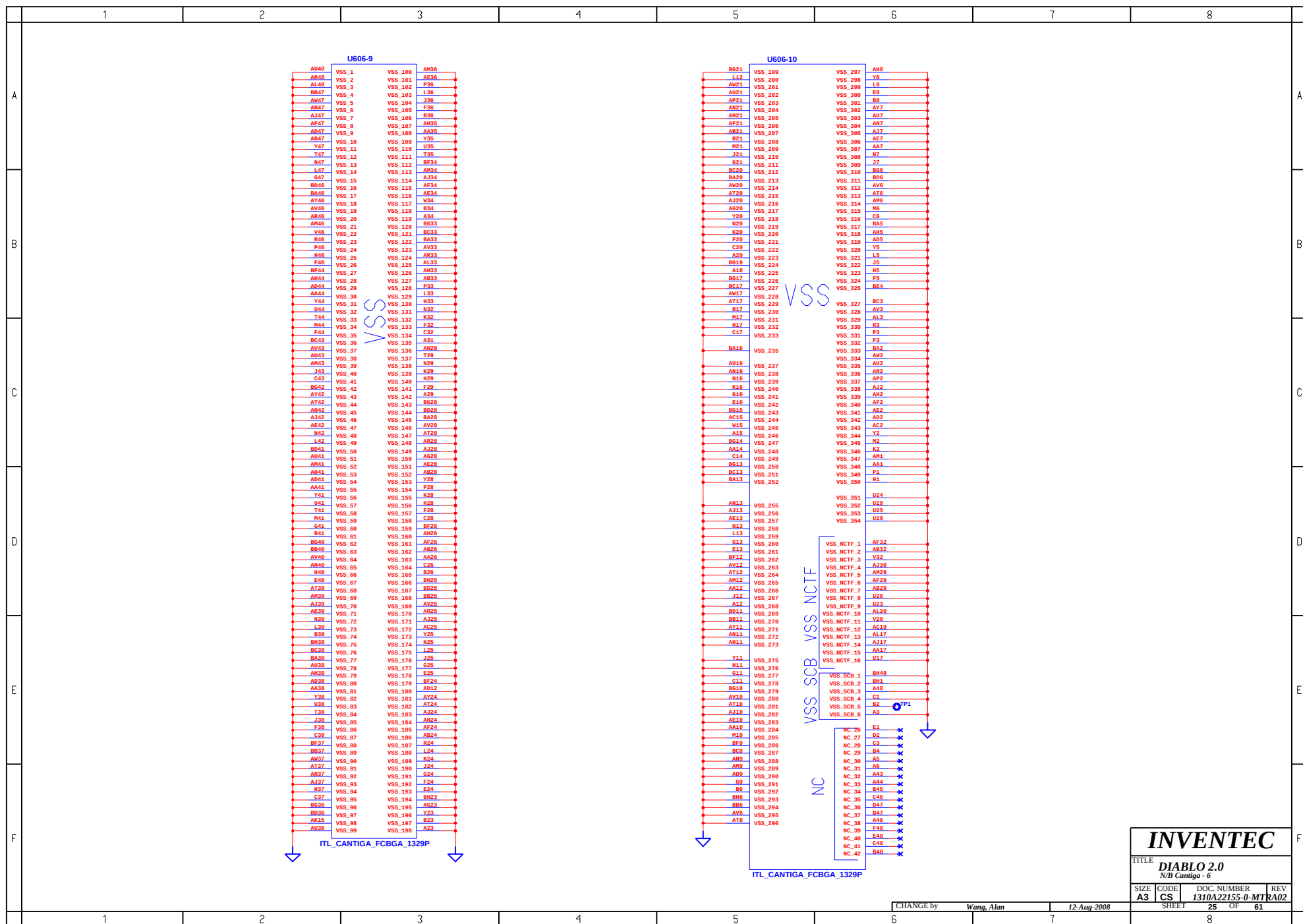
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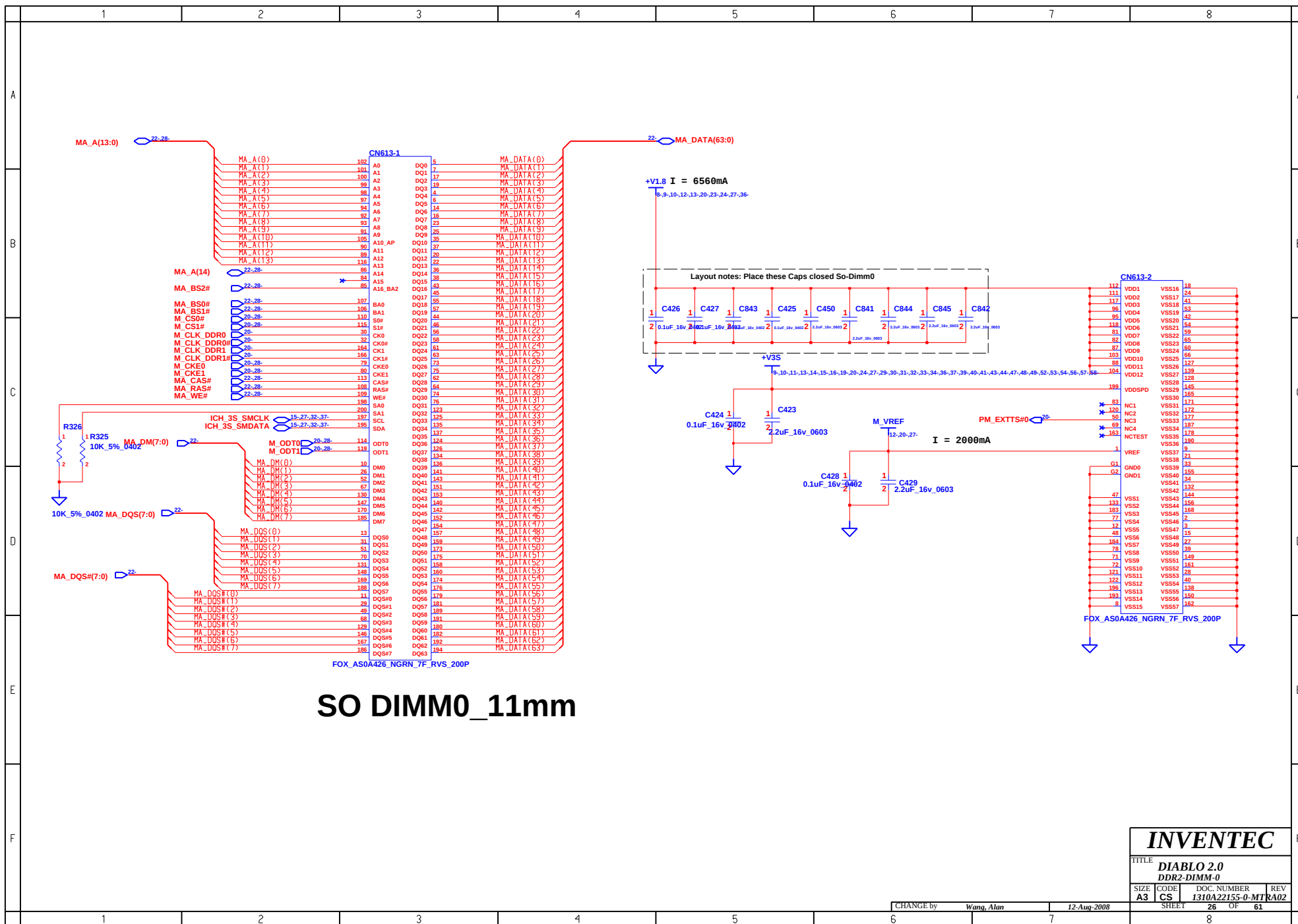
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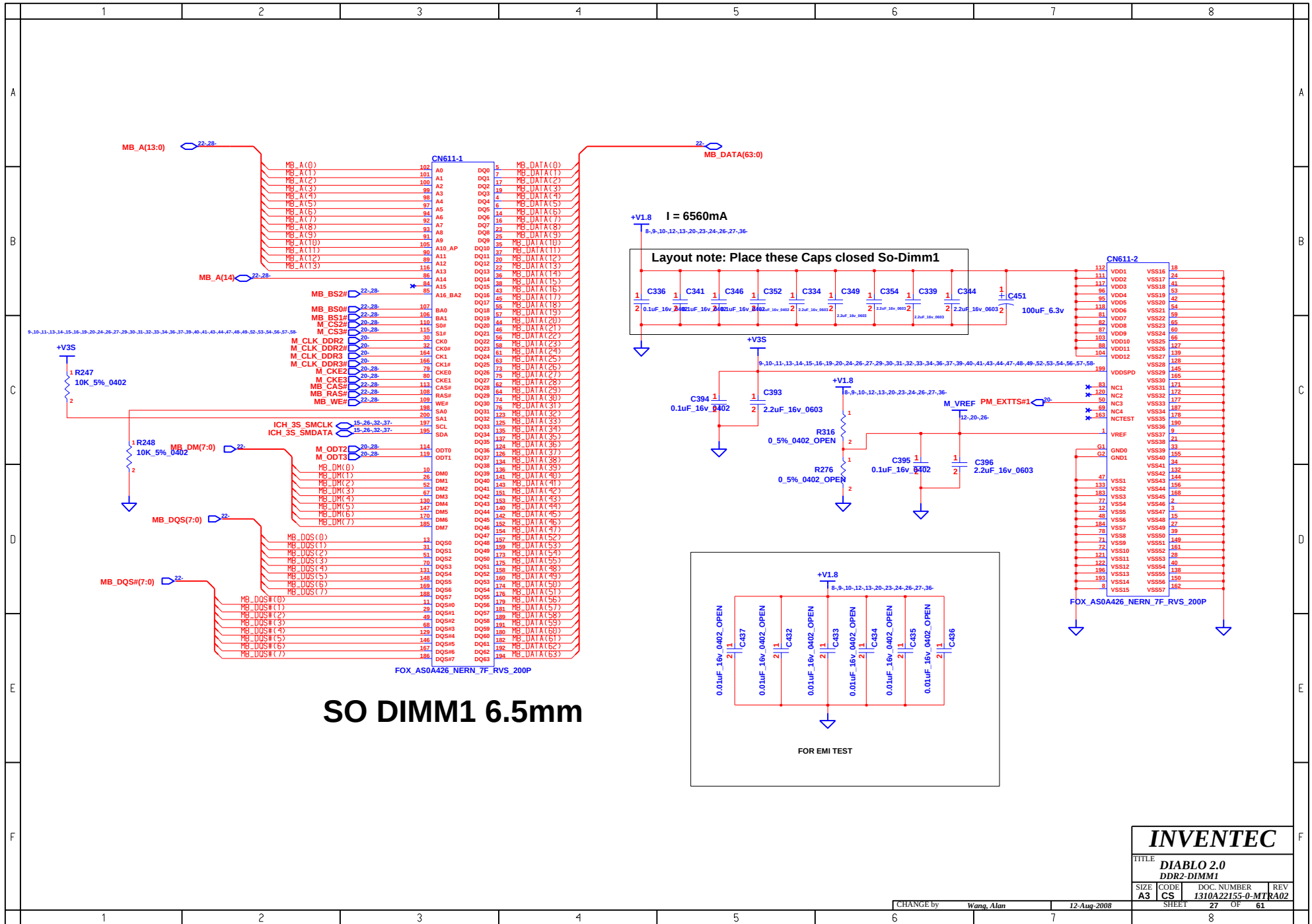
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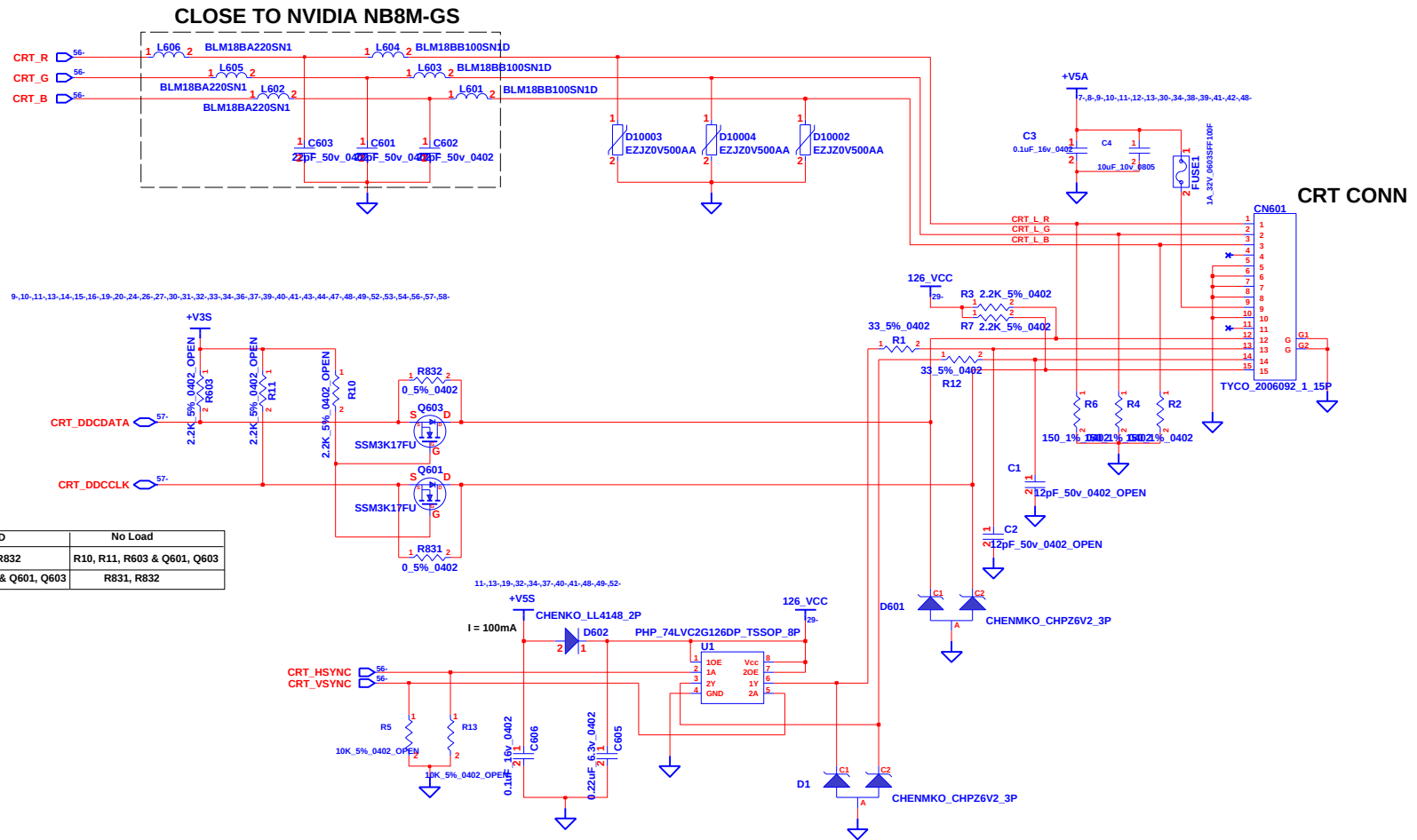




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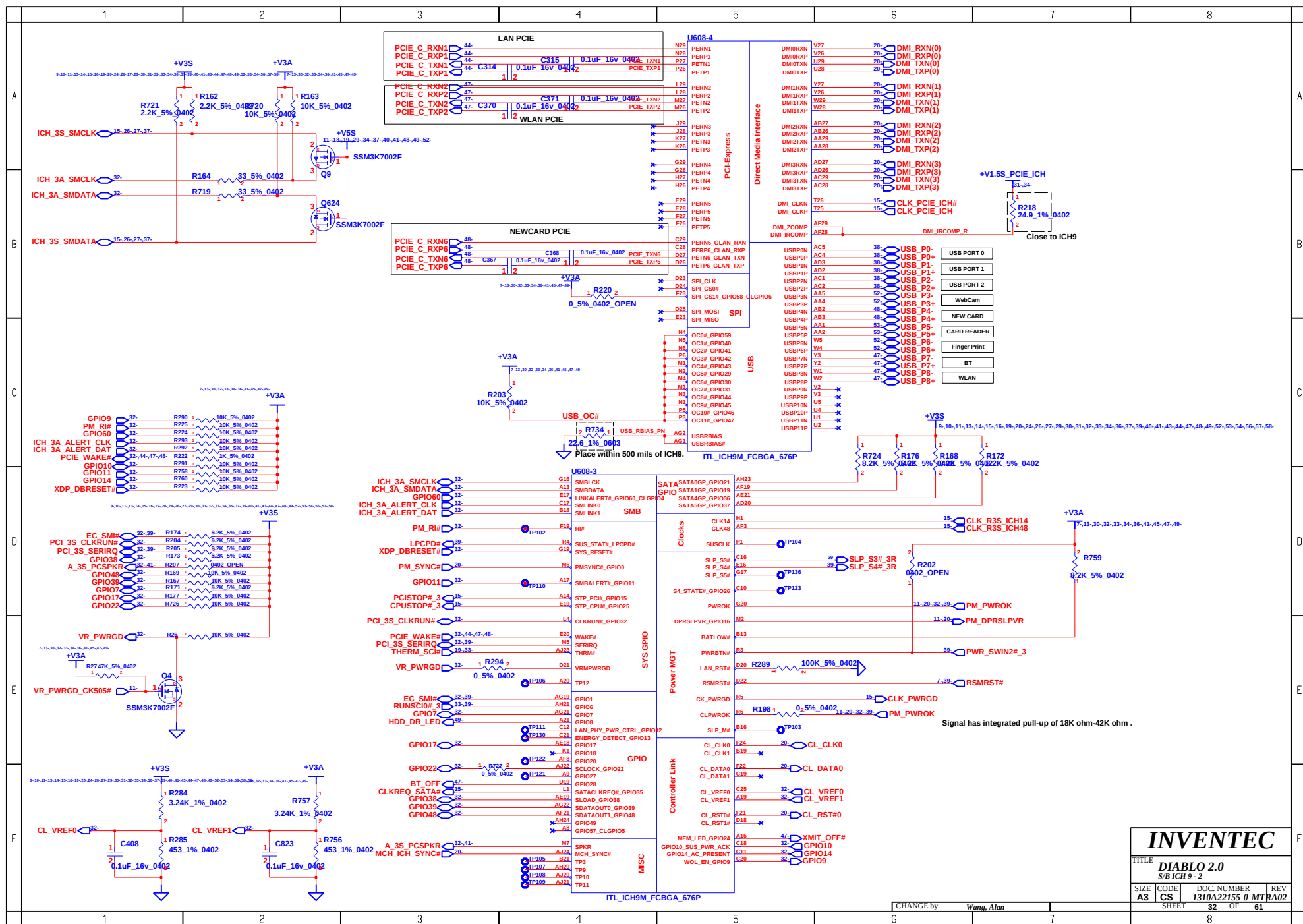
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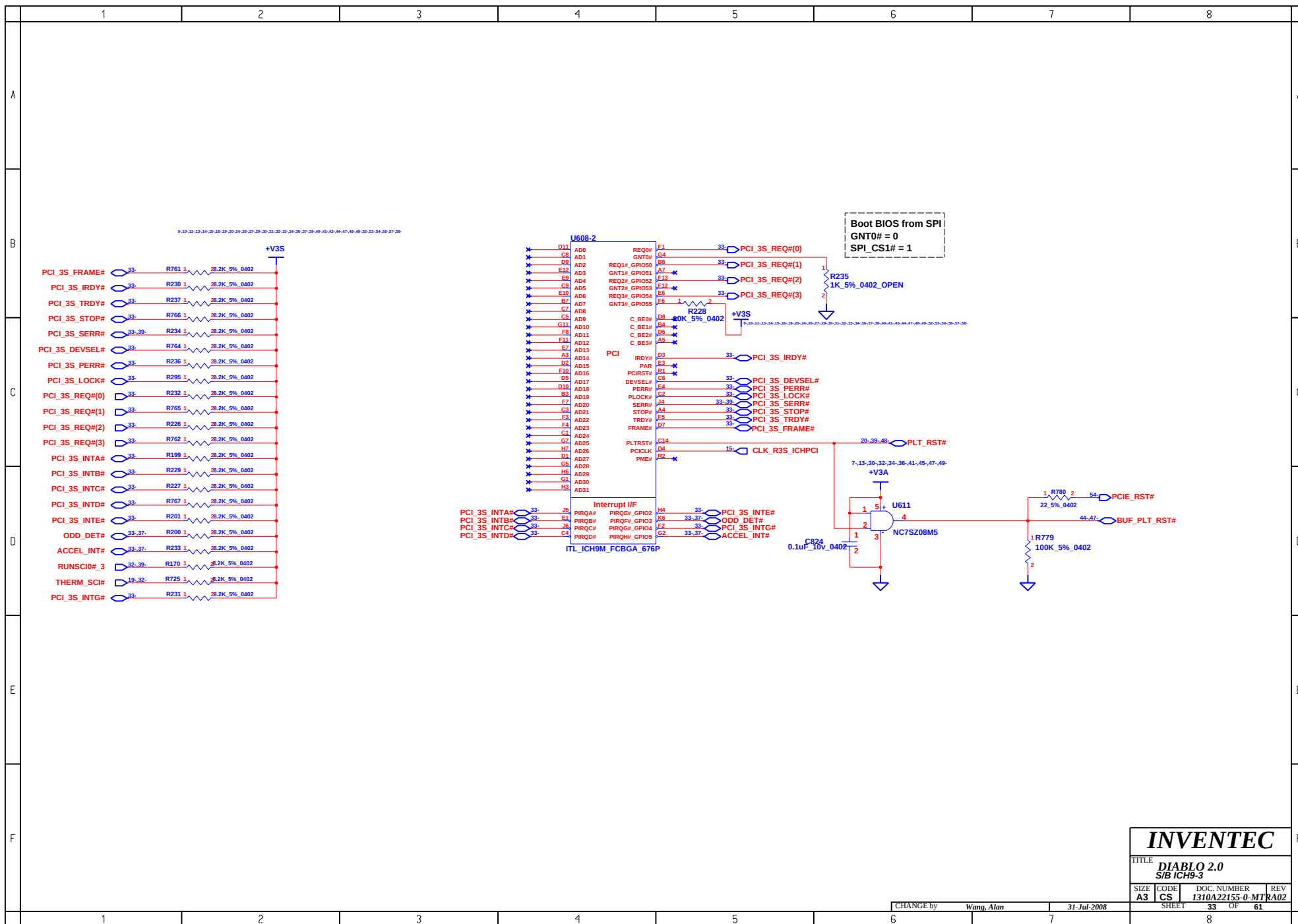


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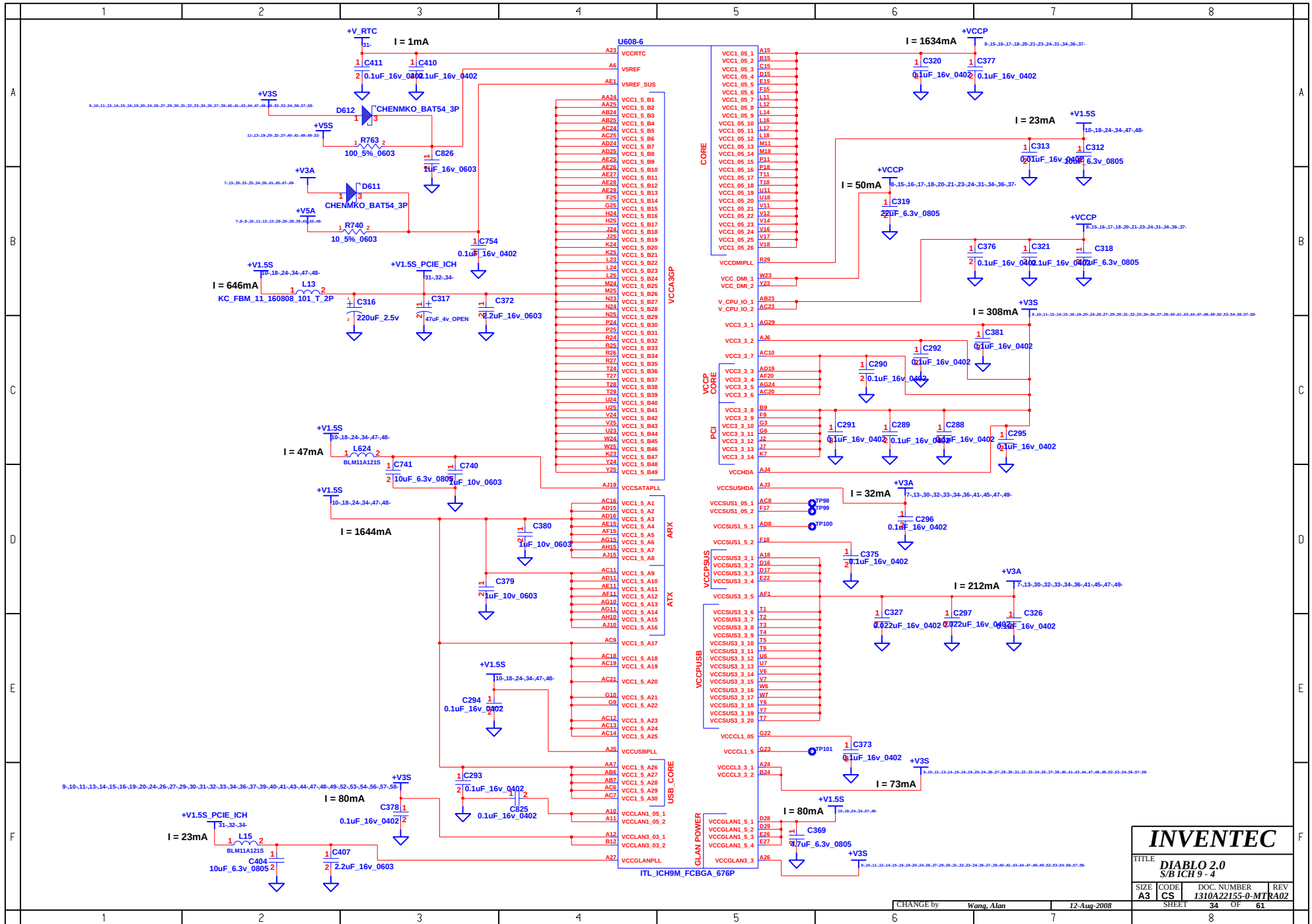
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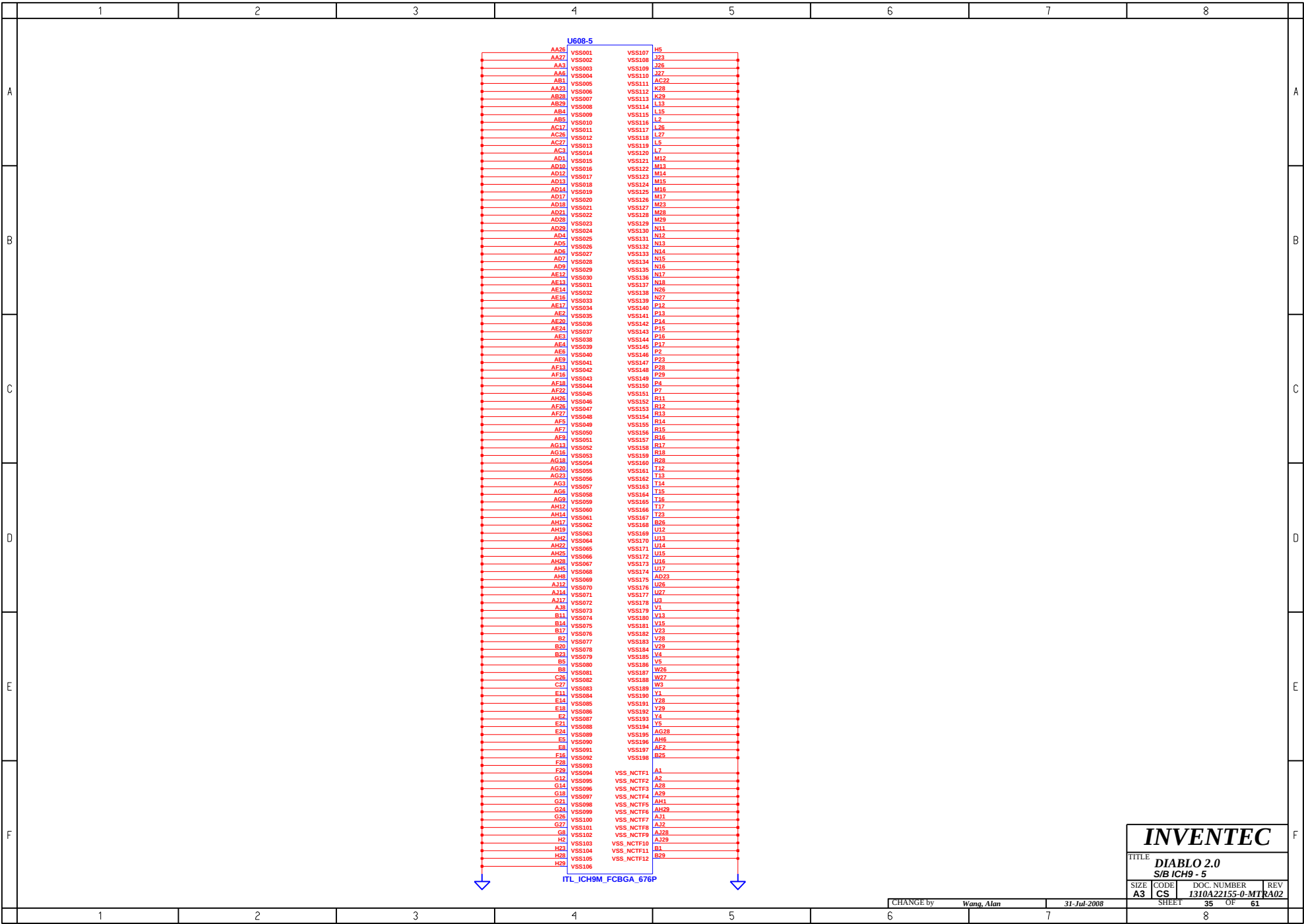


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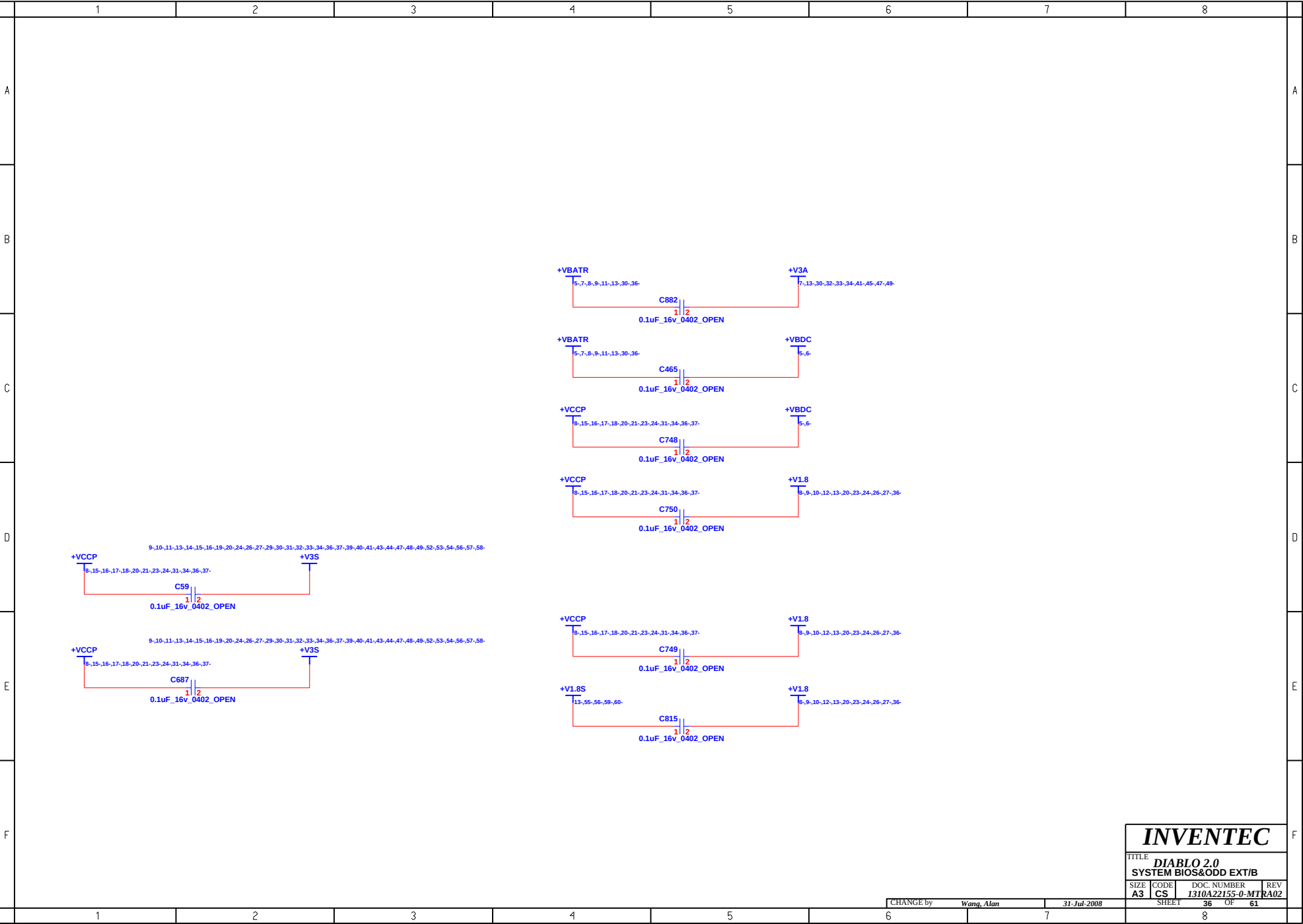
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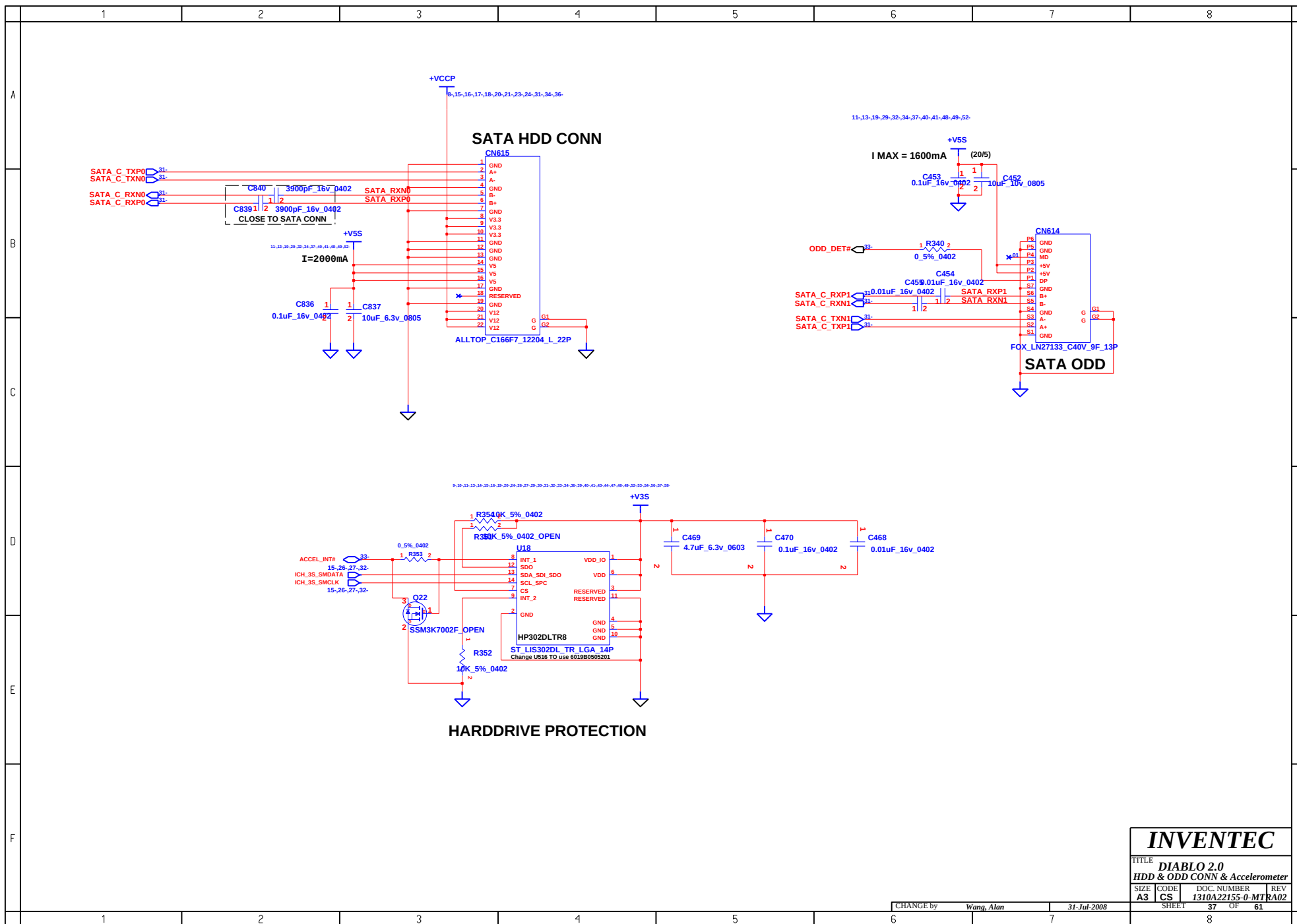
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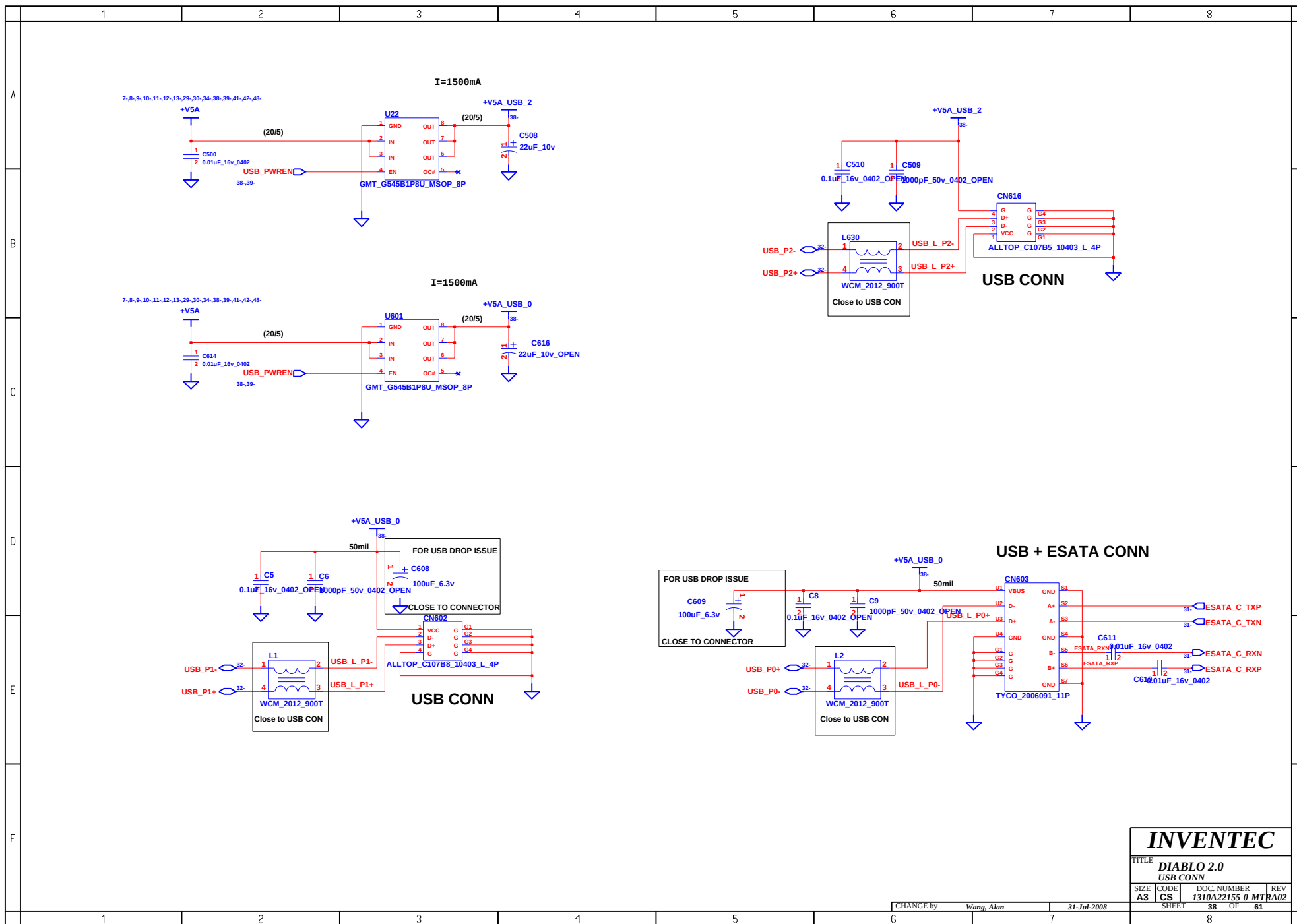
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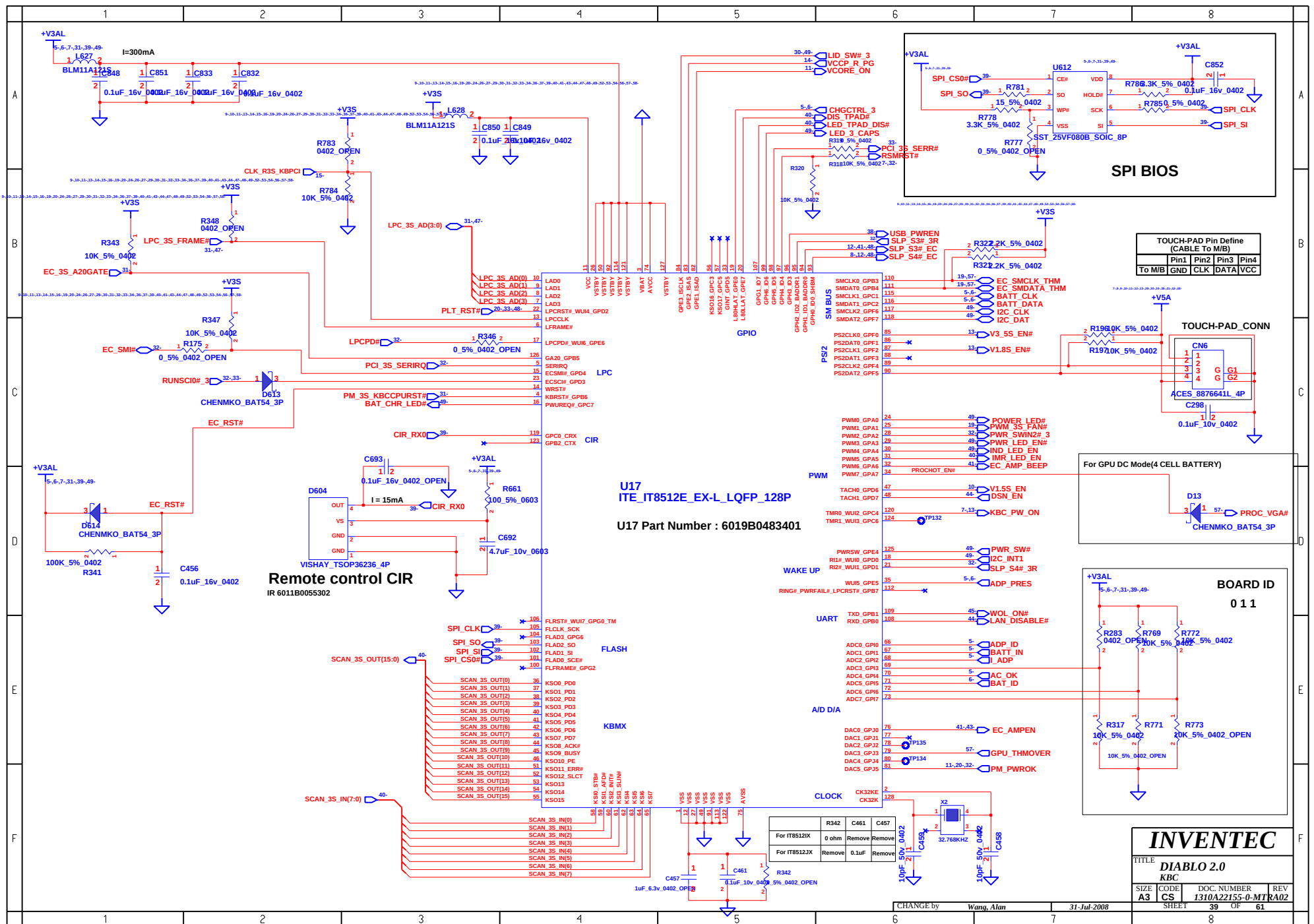
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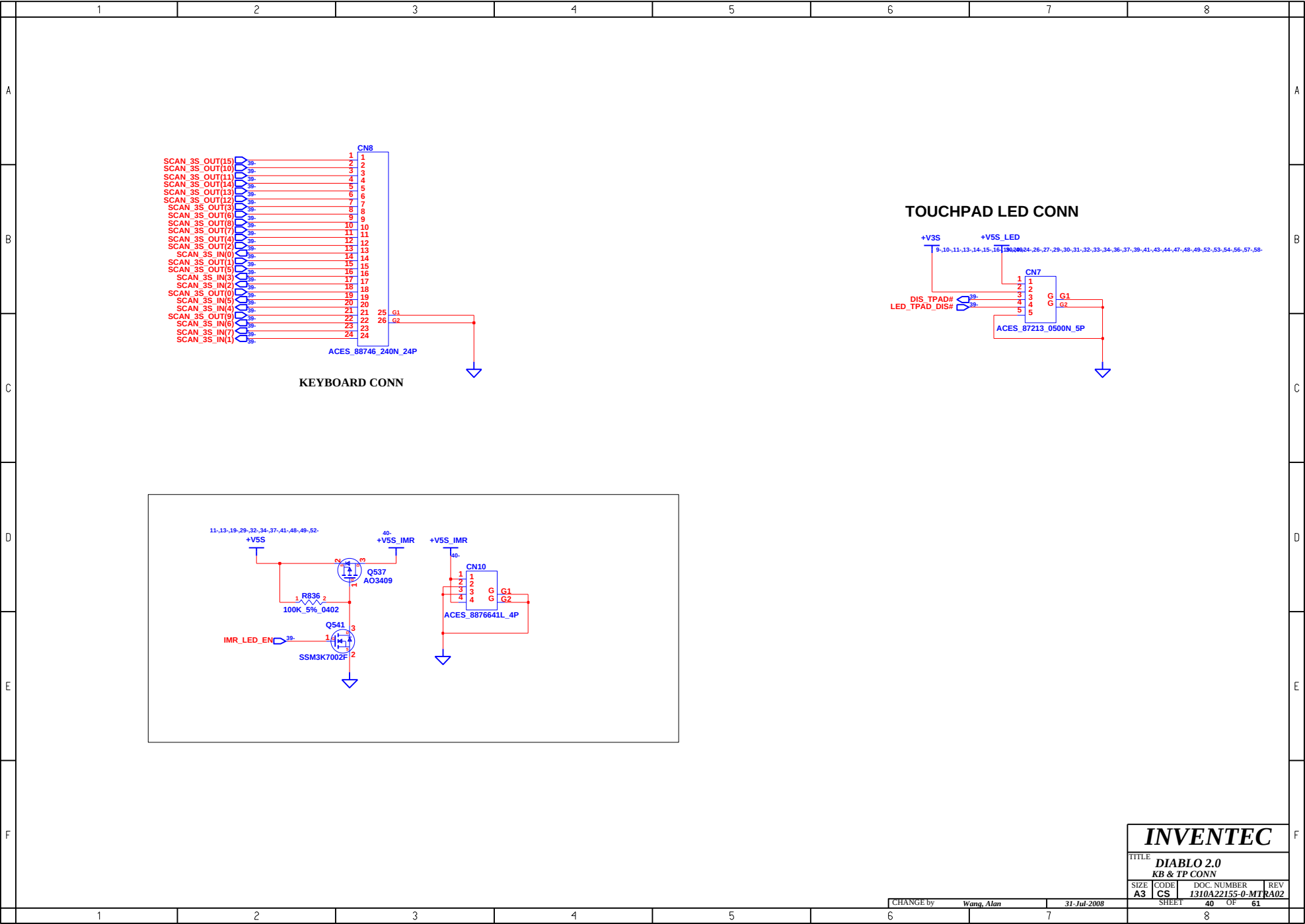
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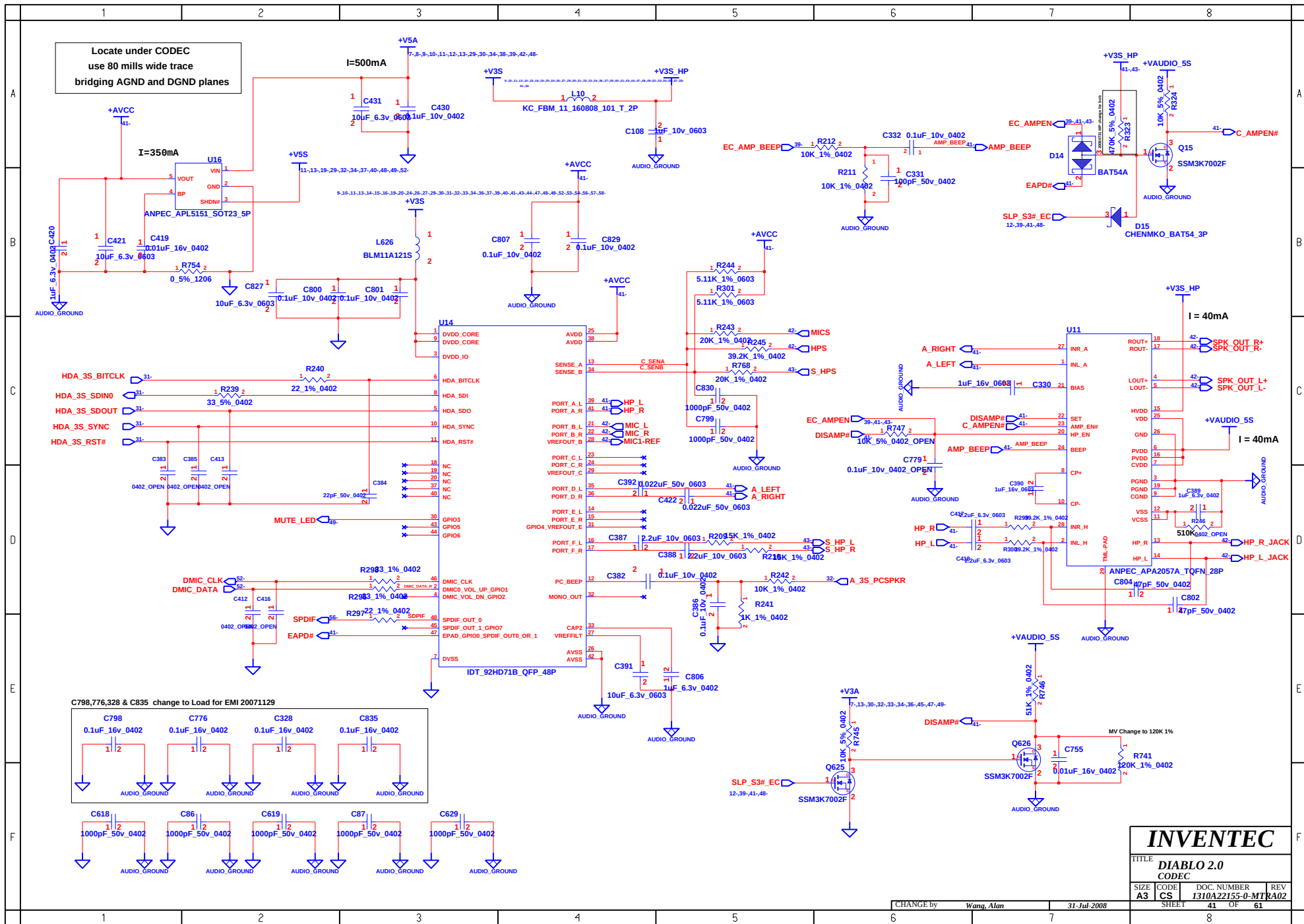
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A

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C

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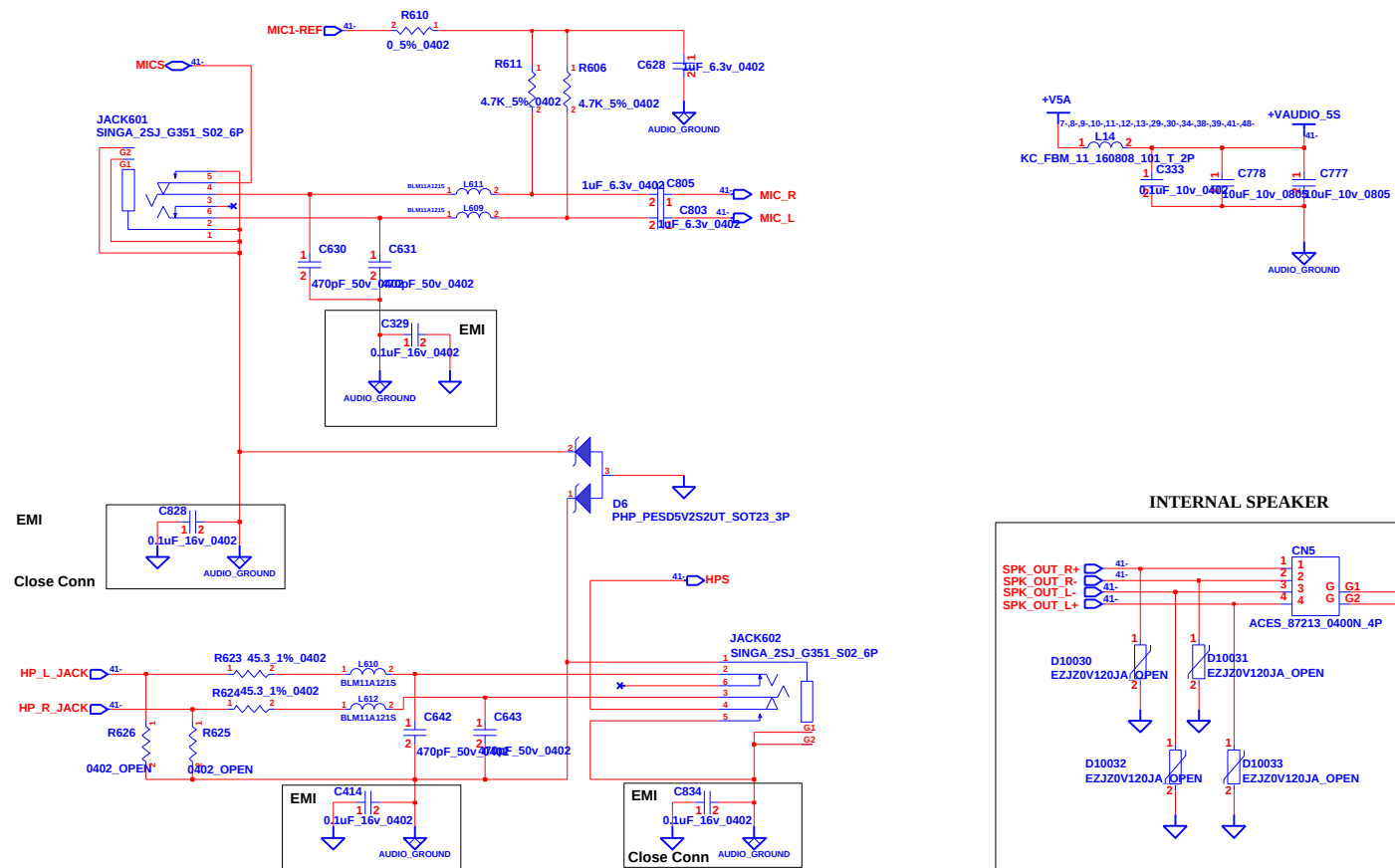
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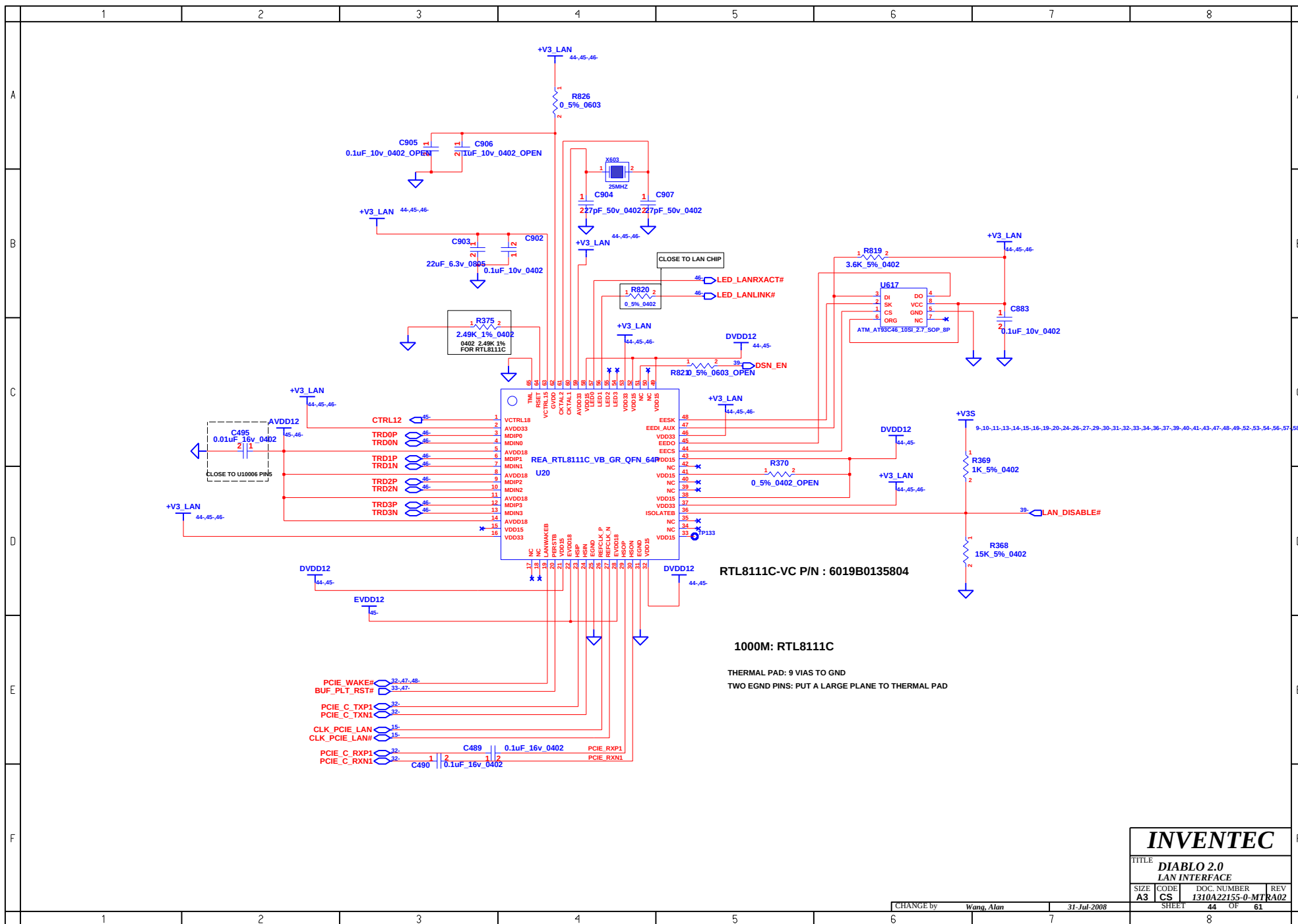
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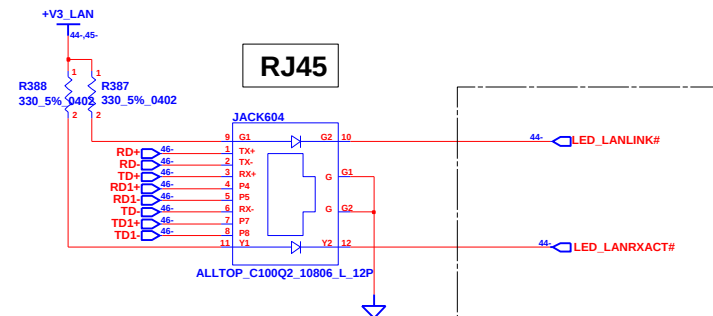
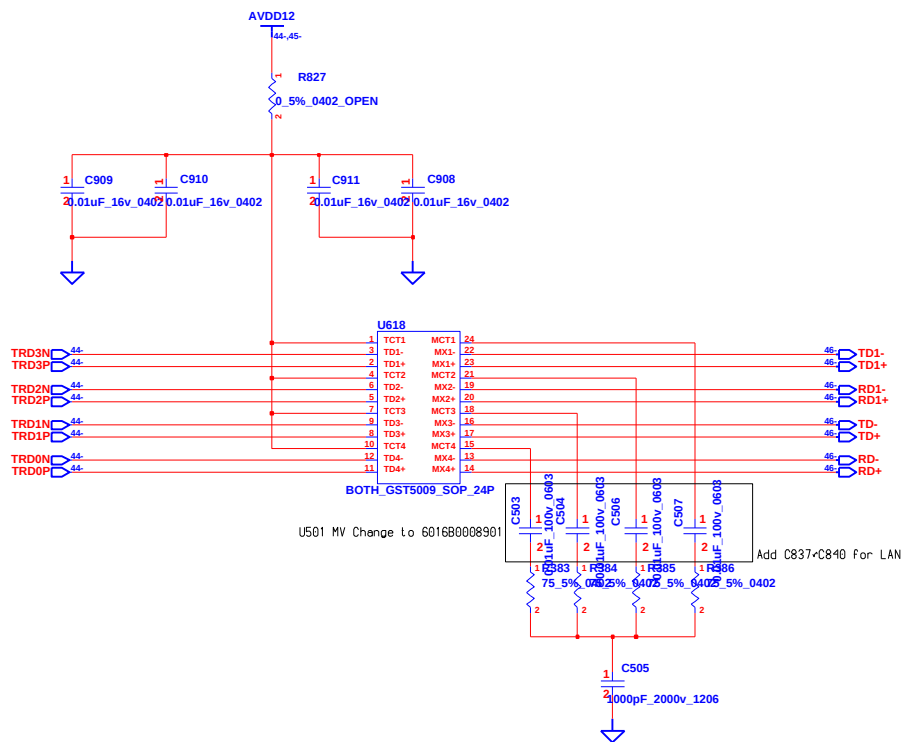


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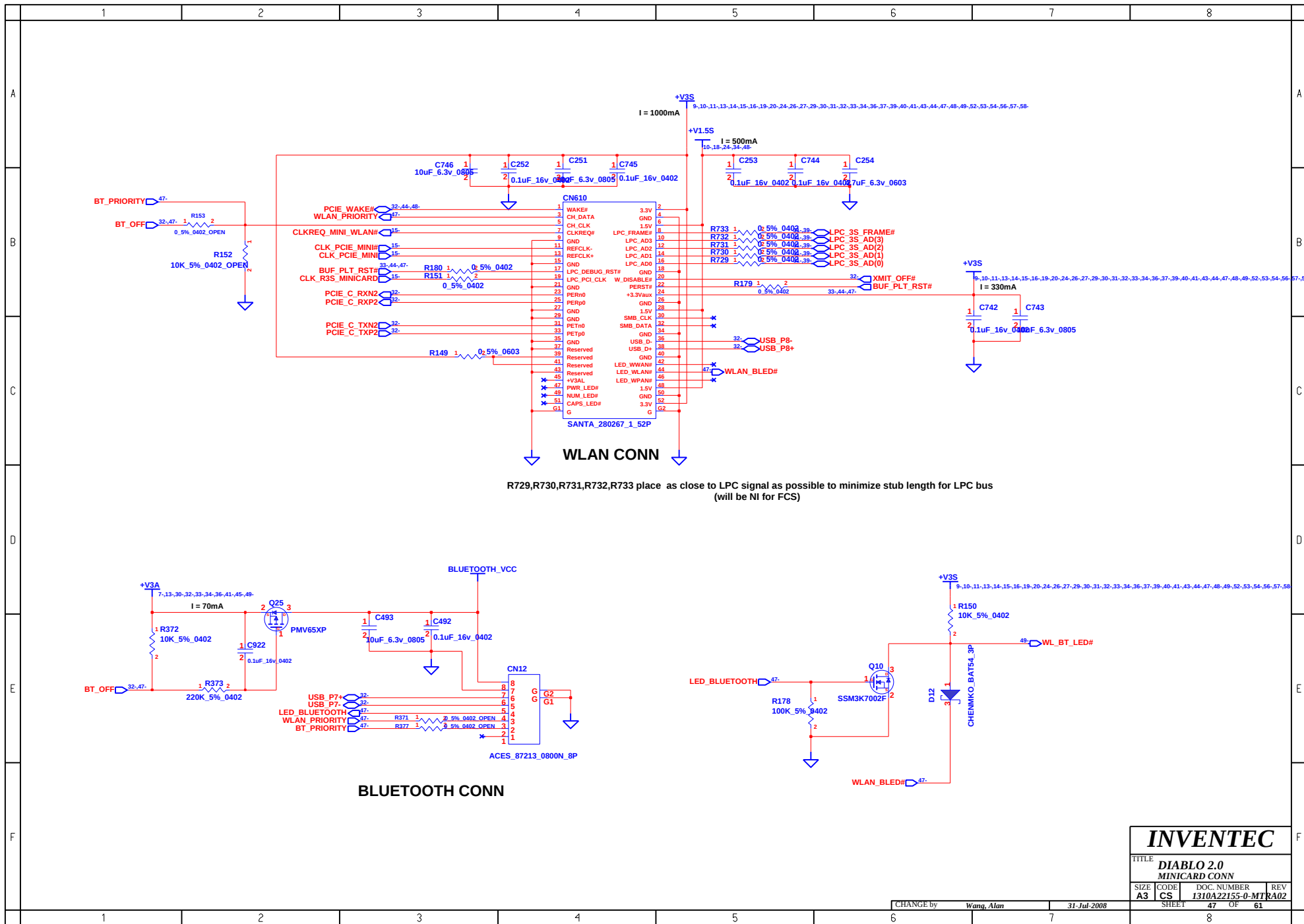
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LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

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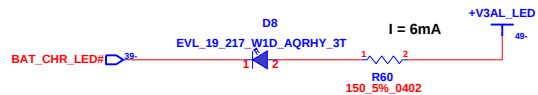


INVENTEC

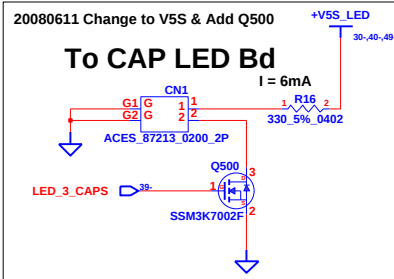
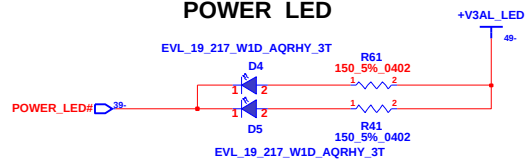
TITLE DIABLO 2.0 MINICARD CONN			
SIZE A3	CODE CS	DOC. NUMBER I310A22155-0-MT	REV RA02
CHANGE by Wang, Alan		31-Jul-2008	
SHEET 47		OF 61	

LED P/N: 6011B0072901

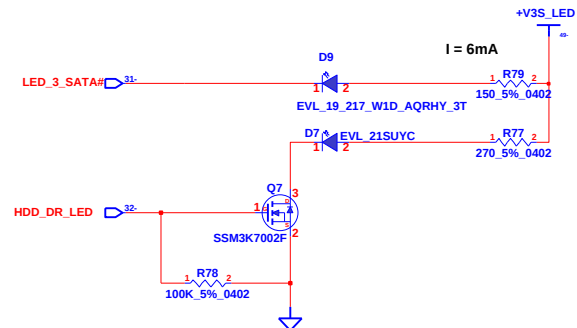
BATTERY-CHARGE LED



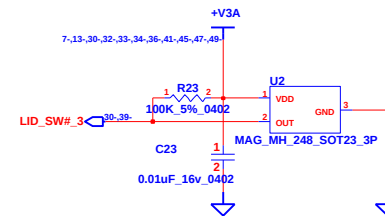
POWER LED



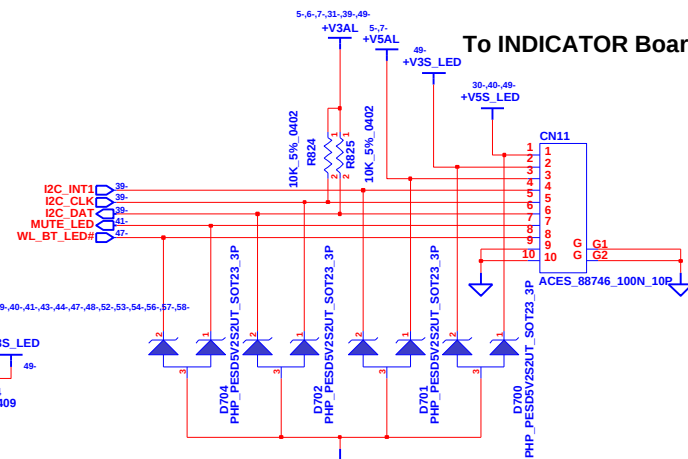
SATA LED & HDD-HALTED LED



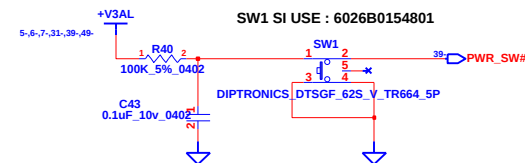
LID SWITCH



To INDICATOR Board



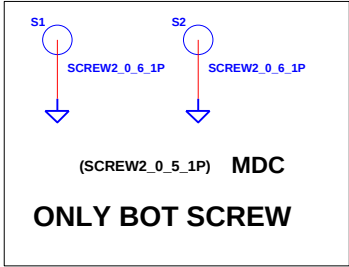
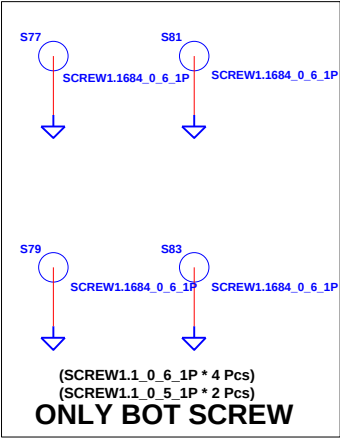
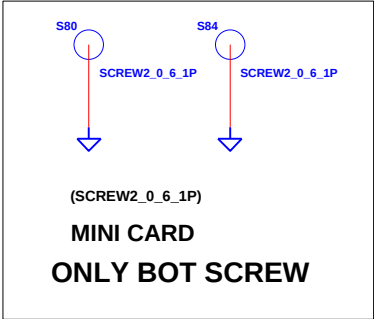
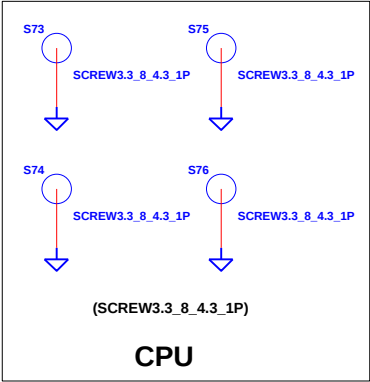
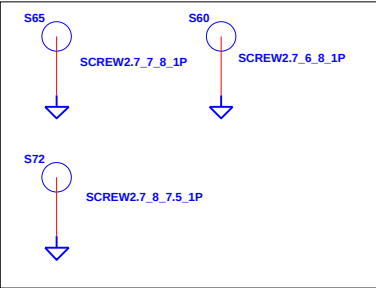
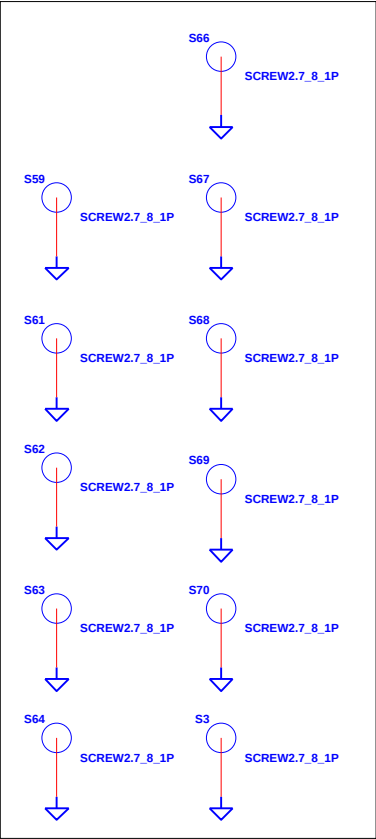
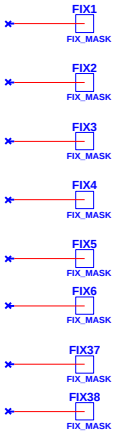
20080731 change to ESD Diode



POWER BUTTON

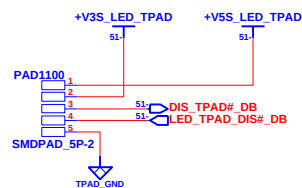
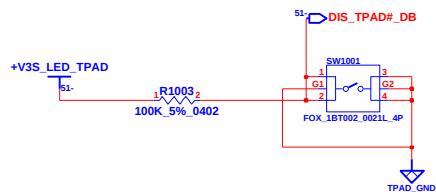
INVENTEC			
TITLE DIABLO 2.0 BUTTON & LED			
SIZE A3	CODE CS	DOC. NUMBER I310A22155-0-MT	REV RA02
CHANGE by Wang, Alan		31-Jul-2008	
SHEET 49		OF 61	

	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

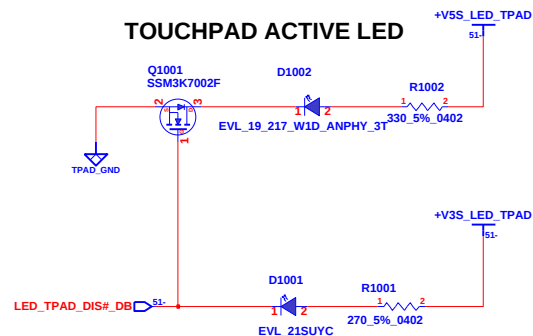


INVENTEC			
TITLE DIABLO 2.0 SCREW			
SIZE A3	CODE CS	DOC. NUMBER 1310A22155-0-MTR	REV A02
CHANGE by Wang, Alan		31-Jul-2008	
SHEET 50		OF 61	

TOUCHPAD-DISABLE BUTTOM_DB



TOUCHPAD ACTIVE LED



TouchPad Disable DB

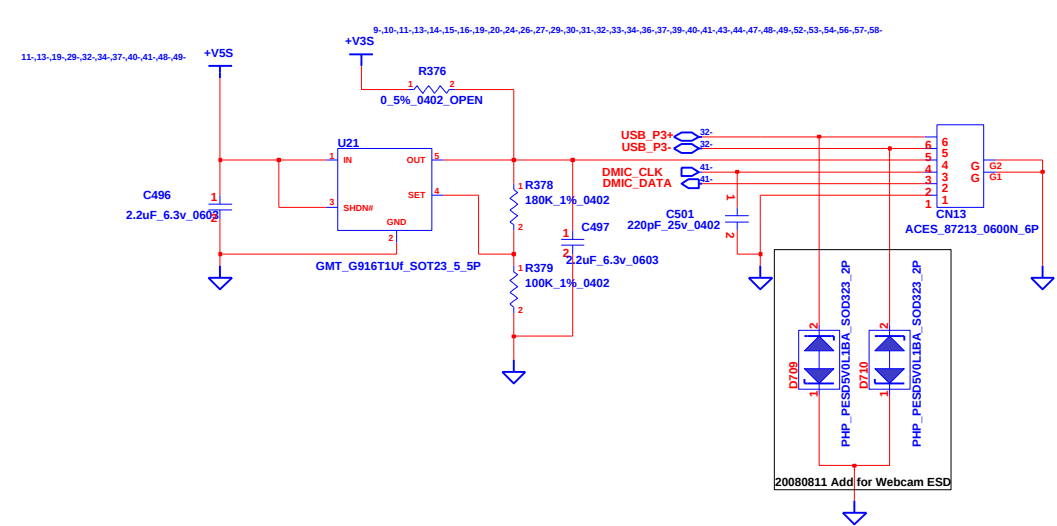
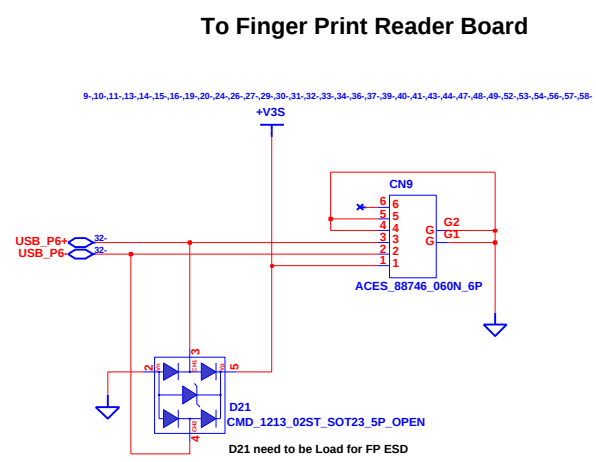
INVENTEC

TITLE
**DIABLO 2.0
FINGER PRINTER CONN.**

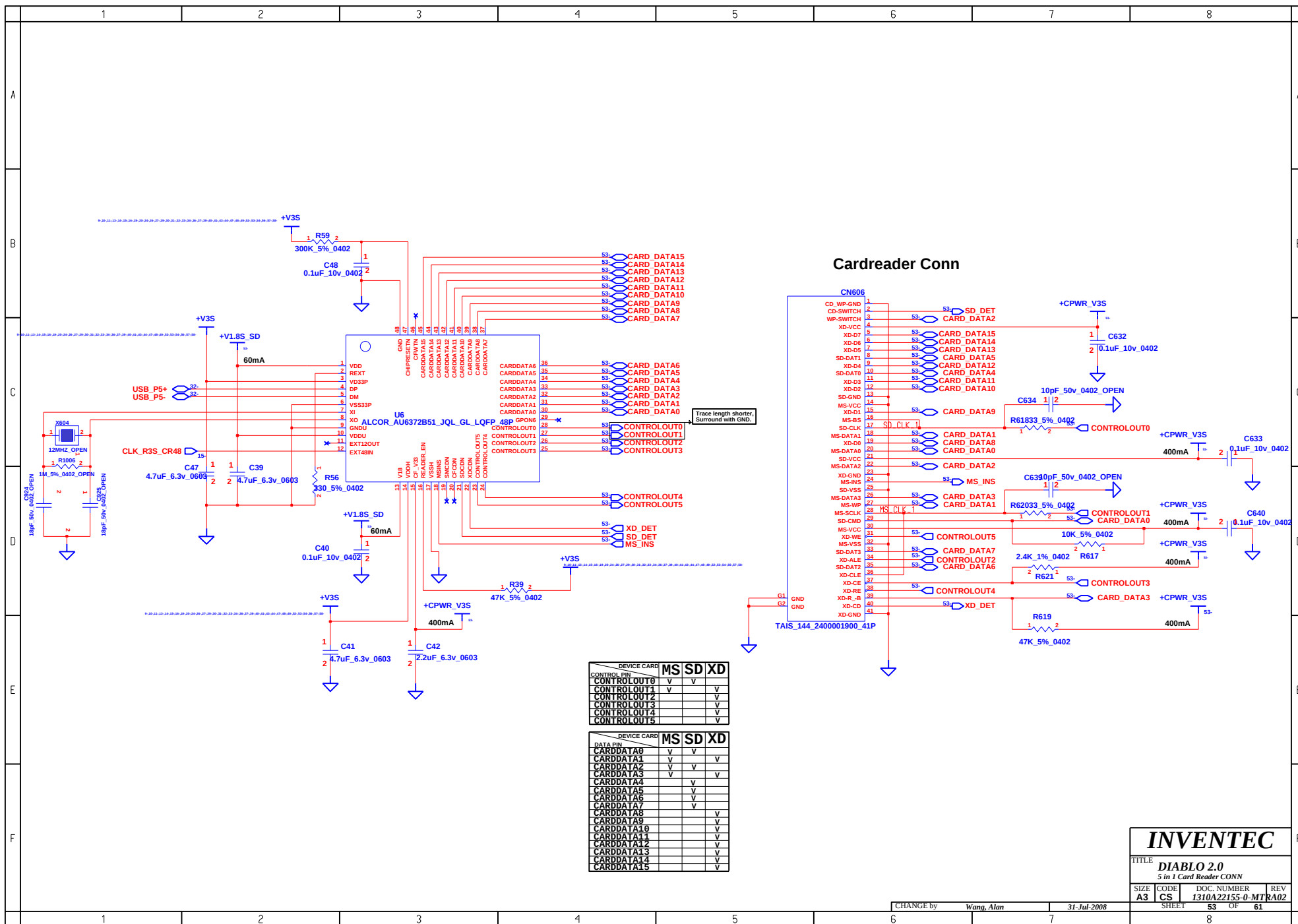
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22192-0-MT	RA02

CHANGE by Wang, Alan 31-Jul-2008

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Webcam CONN & DIGITAL MIC



DEVICE CARD			
CONTROL PIN	MS	SD	XD
CONTROL00	V	V	V
CONTROL01	V	V	V
CONTROL02	V	V	V
CONTROL03	V	V	V
CONTROL04	V	V	V
CONTROL05	V	V	V

DEVICE CARD			
DATA PIN	MS	SD	XD
CARD00	V	V	V
CARD01	V	V	V
CARD02	V	V	V
CARD03	V	V	V
CARD04	V	V	V
CARD05	V	V	V
CARD06	V	V	V
CARD07	V	V	V
CARD08	V	V	V
CARD09	V	V	V
CARD10	V	V	V
CARD11	V	V	V
CARD12	V	V	V
CARD13	V	V	V
CARD14	V	V	V
CARD15	V	V	V

INVENTEC

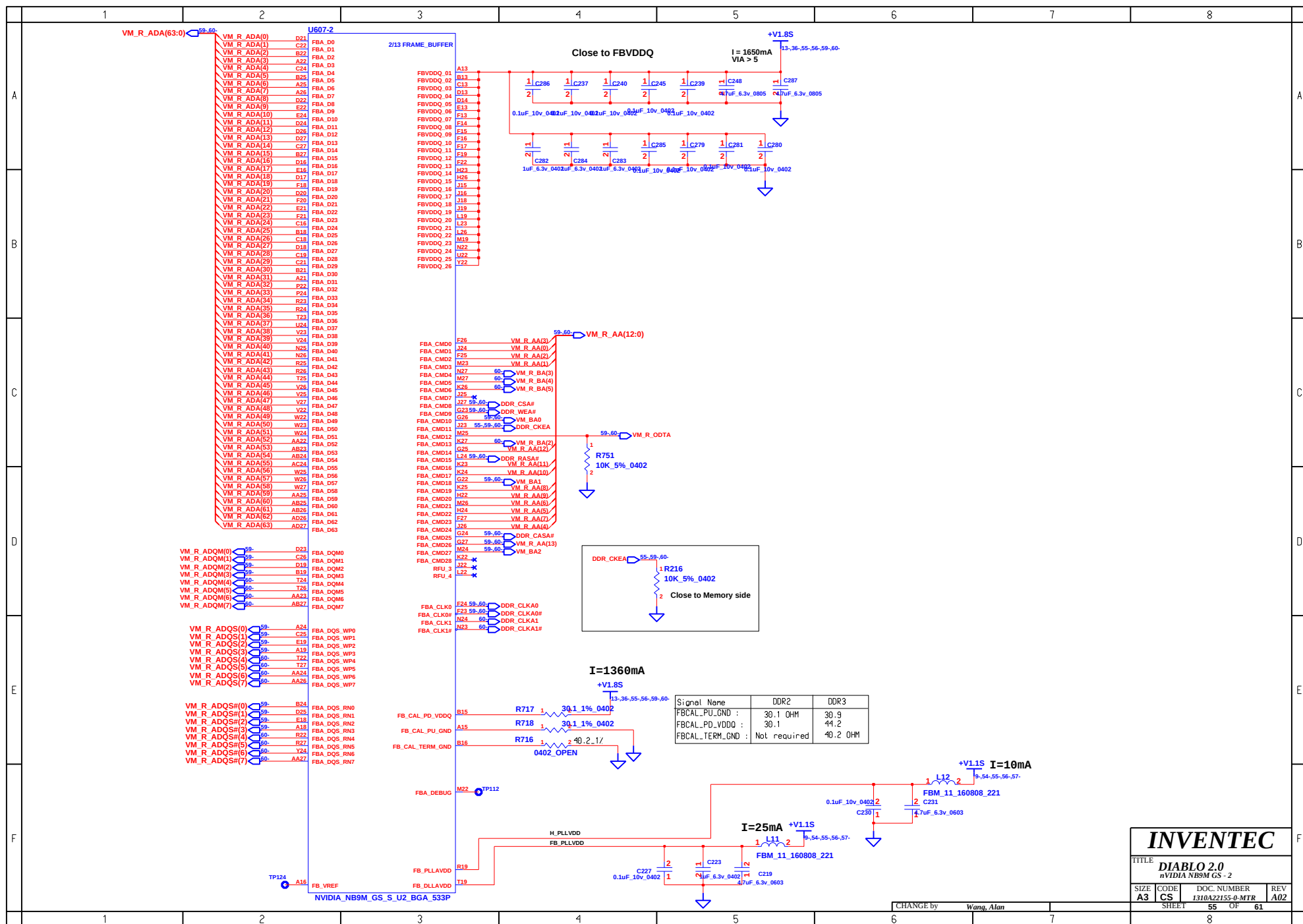
TITLE
DIABLO 2.0
5 in 1 Card Reader Conn

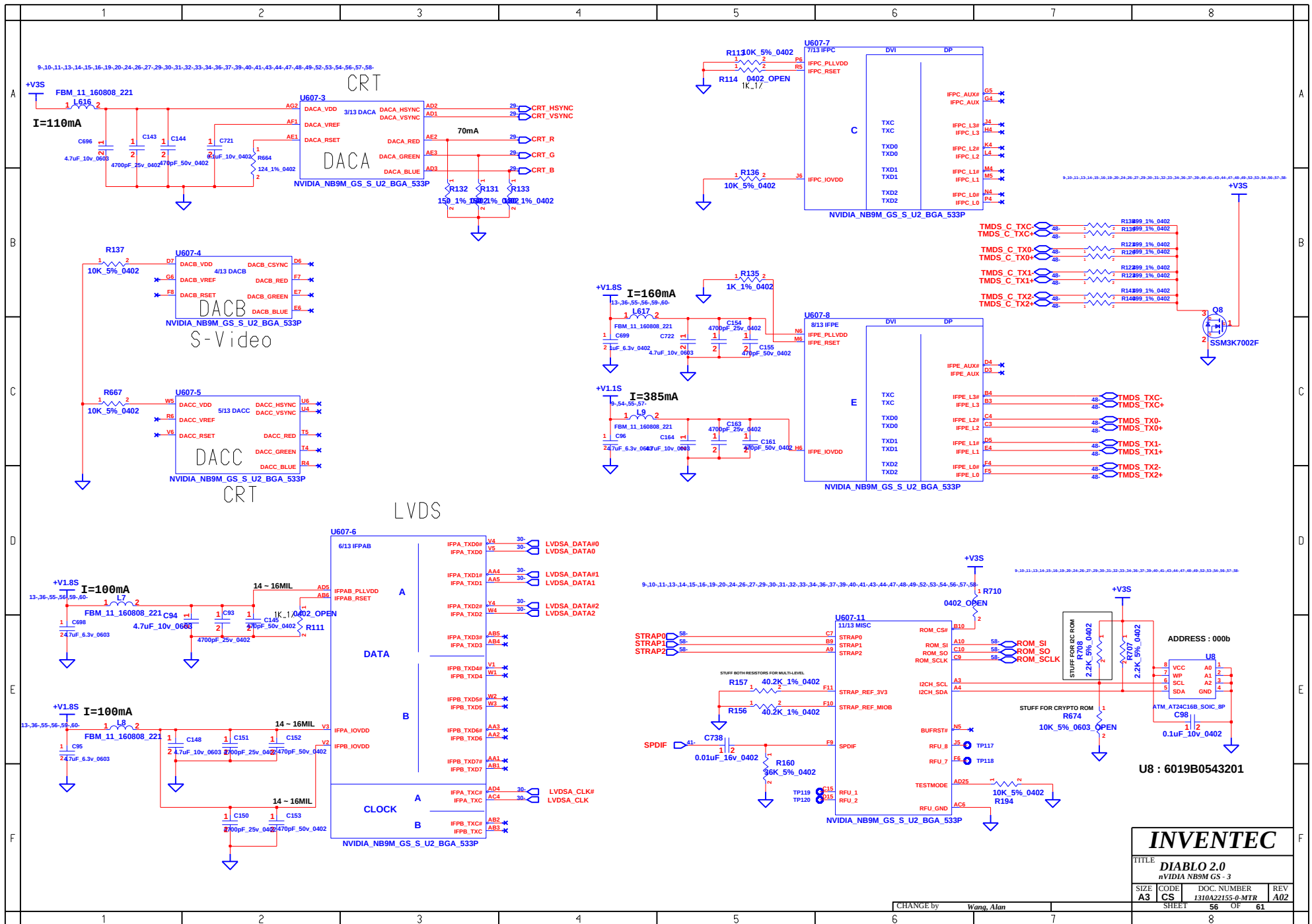
SIZE A3	CODE CS	DOC. NUMBER I310A22155-0-MT	REV RA02
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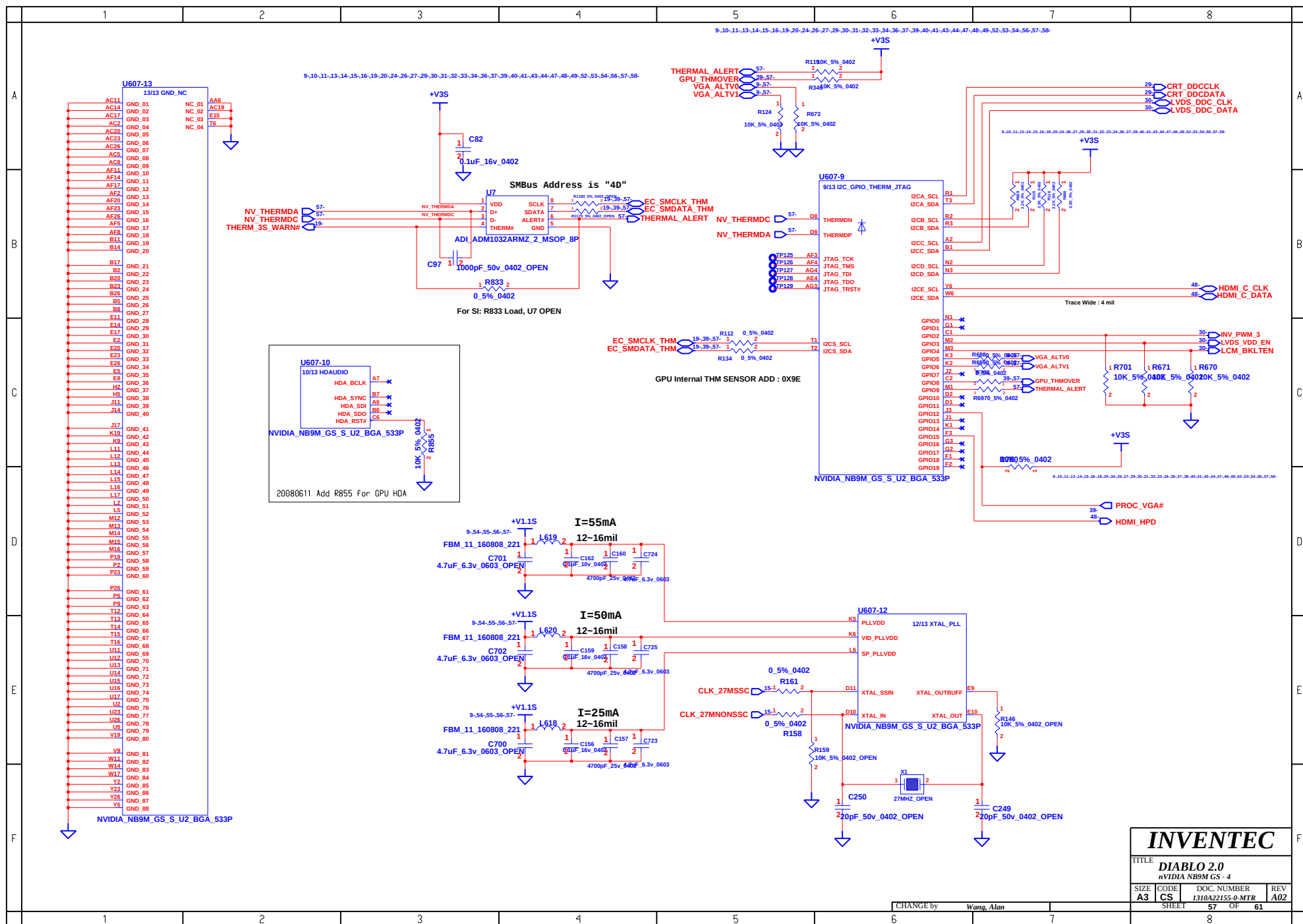
CHANGE by **Wang, Alan** 31-Jul-2008

SHEET **53** OF **61**

For dynamic load : V_{GA}VCC, F_BVDDQ & PEX_VDD ,two to three vias per amperer are recommended

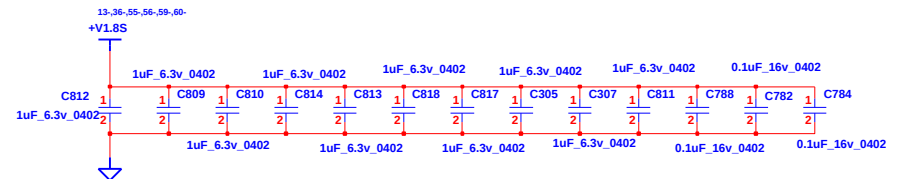
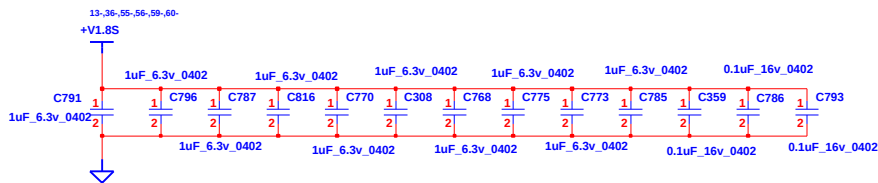
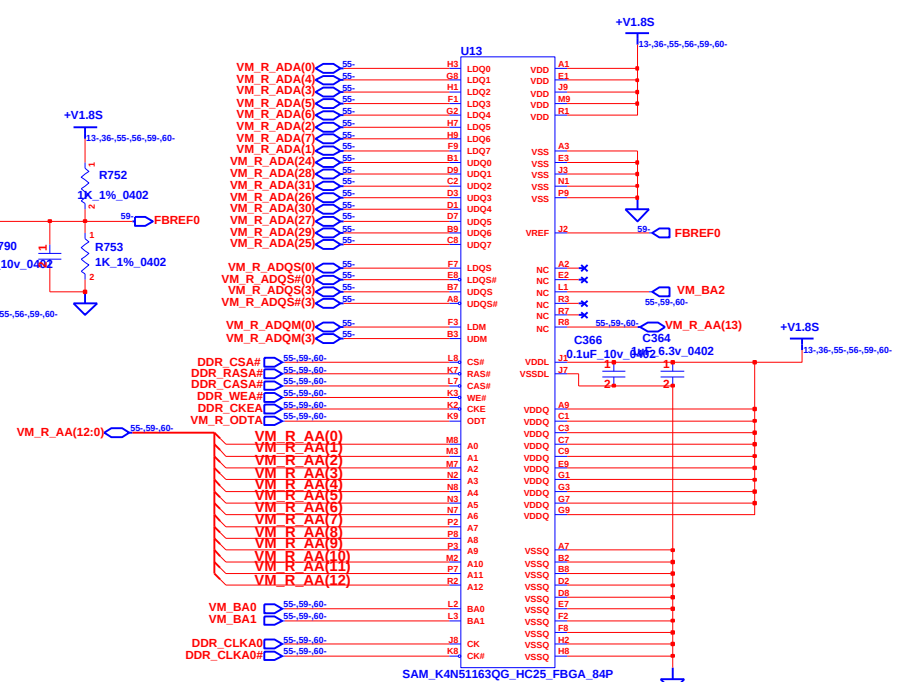
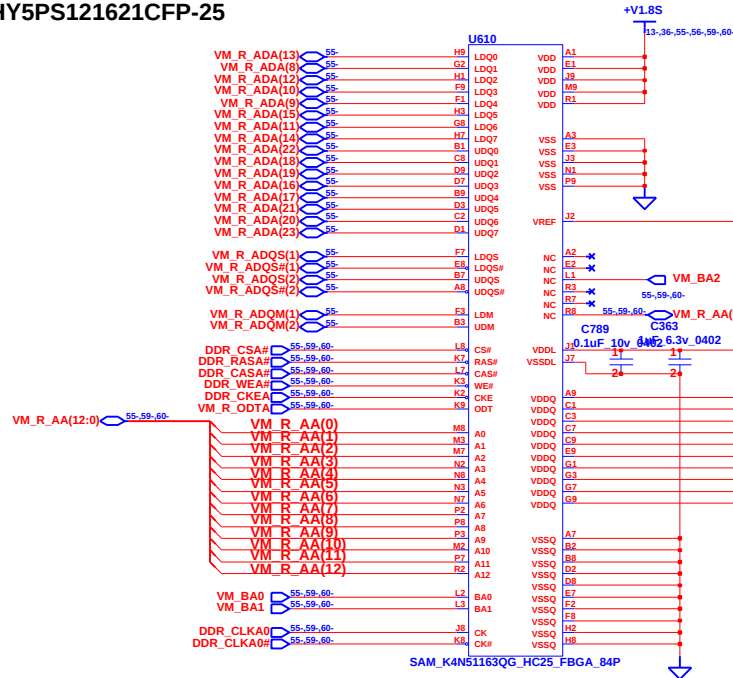






	1	2	3	4	5	6	7	8						
A	GB1 Family GPU Strap Options				GB1 Family GPU Strap Options (DIABLO 2.0) with Samsung GDDR2 64M X 16				A					
	Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Pin 2	Logical Strapping Pin 1	Logical Strapping Pin 0	Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Pin 2	Logical Strapping Pin 1	Logical Strapping Pin 0		
	ROM_SO	+V3S	XCLK_277	TVMODE [2]	TVMODE [1]	TVMODE [0]	ROM_SO	+V3S	1	1	1	0		
	ROM_SCLK	+V3S	PCI_DEVID [4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	ROM_SCLK	+V3S	0	0	1	0		
	ROM_SI	+V3S	RAMCFG [3]	RAMCFG [2]	RAMCFG [1]	RAMCFG [0]	ROM_SI	+V3S	0	0	0	1		
	STRAP2	+V3S	PCI_DEVID [3]	PCI_DEVID [2]	PCI_DEVID [1]	PCI_DEVID [0]	STRAP2	+V3S	1	0	0	1		
	STRAP1	+V3S	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]	STRAP1	+V3S	0	0	0	1		
	STRAP0	+V3S	USER [3]	USER [2]	USER [1]	USER [0]	STRAP0	+V3S	1	1	1	1		
B	Logical Strap Bit Mapping				NB9M-GS RAMCFG[3:0]				GB1 Family GPU Strap Options (DIABLO 2.0) with Hynix GDDR2 64M X 16				B	
	Resistor Values	Pull - up to VDD	Pull - down to GND	32M X 16 GDDR2	RAMCFG [3]	RAMCFG [2]	RAMCFG [1]	RAMCFG [0]	Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Pin 2	Logical Strapping Pin 1	Logical Strapping Pin 0
	5K ohm	1000	0000	Samsung	0	1	0	1	ROM_SO	+V3S	1	1	1	0
	10K ohm	1001	0001	Qimonda	0	1	1	0	ROM_SCLK	+V3S	0	0	1	0
	15K ohm	1010	0010	Hynix	0	1	1	1	ROM_SI	+V3S	0	0	0	0
	20K ohm	1011	0011	64M X 16 GDDR2	RAMCFG [3]	RAMCFG [2]	RAMCFG [1]	RAMCFG [0]	STRAP2	+V3S	1	0	0	1
	25K ohm	1100	0100	Samsung	0	0	0	1	STRAP1	+V3S	0	0	0	1
	30K ohm	1101	0101	Qimonda	0	0	1	0	STRAP0	+V3S	1	1	1	1
	35K ohm	1110	0110	Hynix	0	0	0	0						
	45K ohm	1111	0111											
C	9-10-11-13-14-15-16-19-20-24-26-27-29-30-31-32-33-34-36-37-39-40-41-43-44-47-48-49-52-53-54-56-57-58-10-11-13-14-15-16-19-20-24-26-27-29-30-31-32-33-34-36-37-39-40-41-43-44-47-48-49-52-53-54-56-57-58													C
D														D
E														E
F														F
	INVENTEC DIABLO 2.0 nVIDIA NB9M GS - 5 SIZE A3CODE CSDOC. NUMBER 1310A22155-0-MTRREV A02 CHANGE byWang, Alan SHEET 58 OF 61													
	1	2	3	4	5	6	7	8						

DIABLO 2.0 USE MEMORY RVL
SANSUNG K4N56163QG_HC25
HYNIX HY5PS121621CFP-25

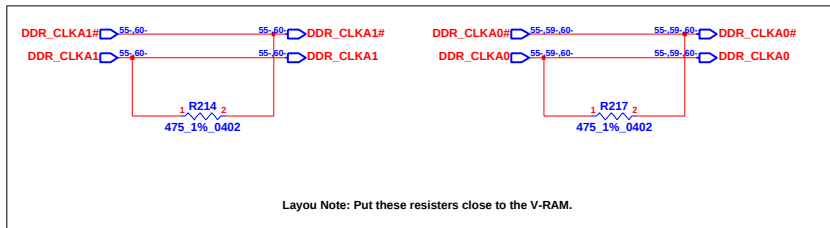
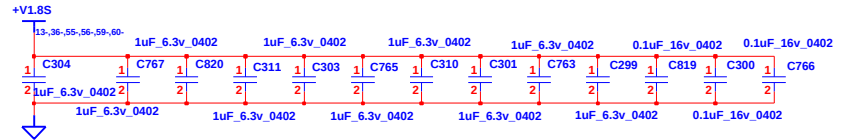
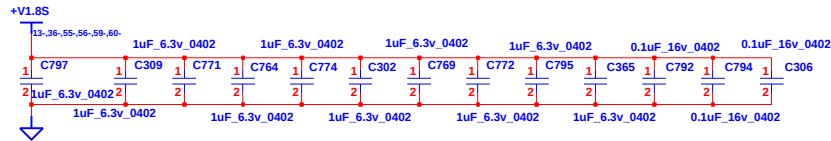
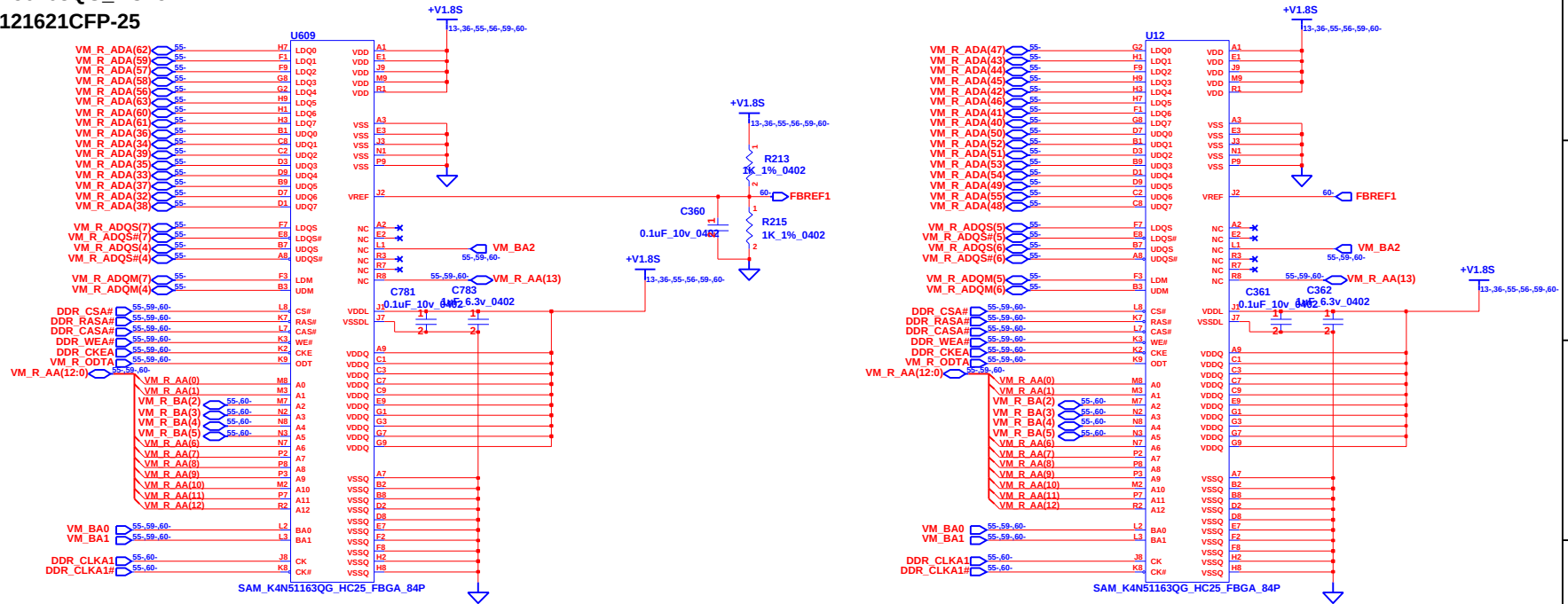


INVENTEC

TITLE DIABLO 2.0 VRAM (1/2)			
SIZE A3	CODE CS	DOC. NUMBER 1310A22155-0-MTR	REV A02
SHEET 59 OF 61			

CHANGE by Wang, Alan

DIABLO 2.0 USE MEMORY RVL
SANSUNG K4N56163QG_HC25
HYNIX HY5PS121621CFP-25



INVENTEC

TITLE		
DIABLO 2.0		
VRAM (2/2)		
SIZE	CODE	DOC. NUMBER
A3	CS	1310A22155-0-MTR
REV		A02
SHEET		60 OF 61

CHANGE by Wang, Alan