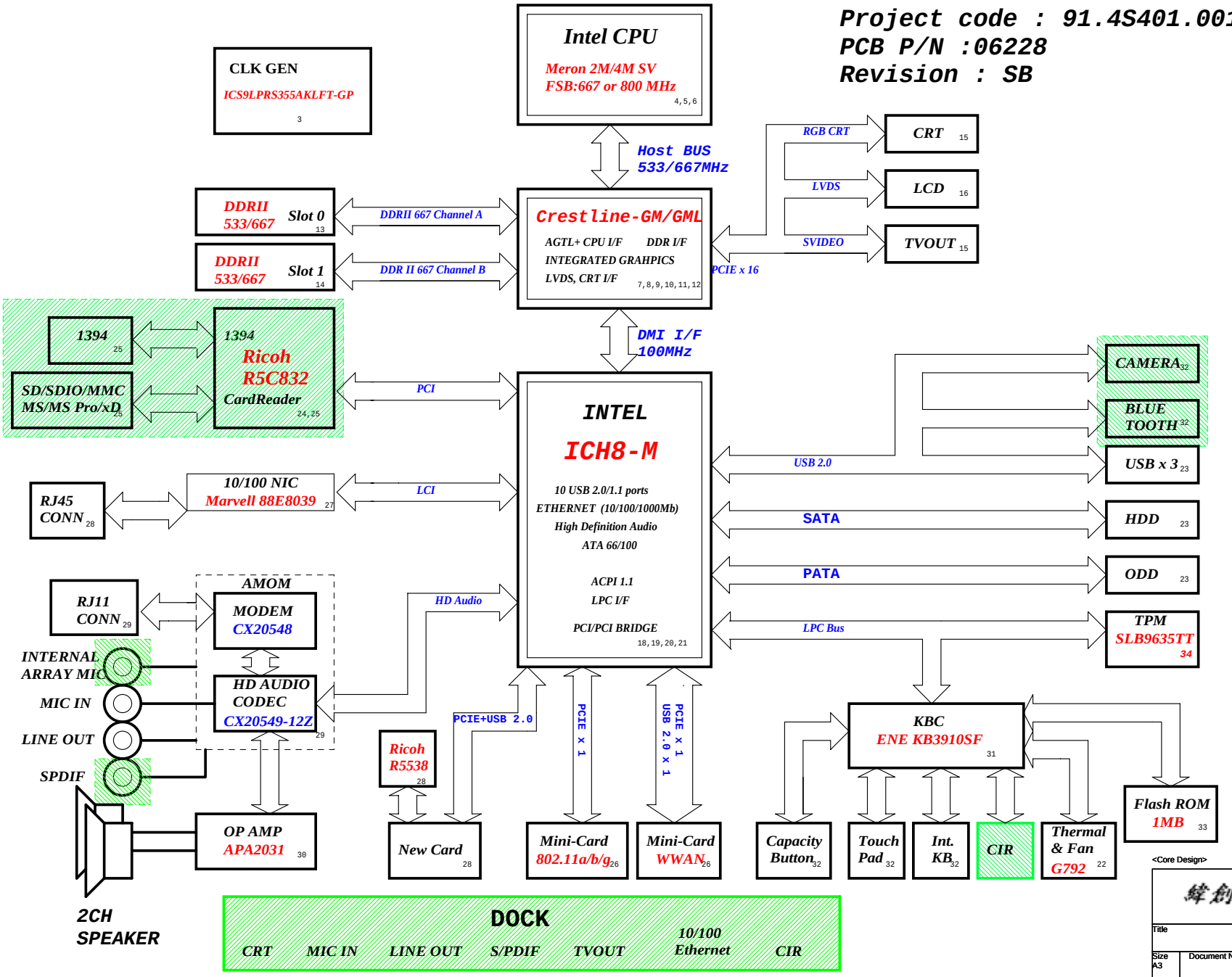
Pamirs UMA Block Diagram

Project code : 91.4S401.001
PCB P/N :06228
Revision : SB



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_AUX_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0 1D8V_S3

SYSTEM DC/DC ISL6269CRZ	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: Block Diagram
Size: A3 | Document Number: Pamirs | Rev: -3
Date: Friday, May 18, 2007 | Sheet 1 of 41

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	tp3	AZ_DOUT_ICH	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0		Normal Operation(default)
1	1		Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
low = A16 swap override enable	
high = default	

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

19,21	+RTCVCC
4,5,6,7,9,10,11,19,21,38,41	1D05V_S0
3,7,10,21,38	1D25V_S0
27	1D2V_LAN_S5
28	1D5V_NEW_S0
5,10,17,19,20,21,26,28,37,38,41	1D5V_S0
7,10,11,13,14,37,38,41	1D8V_S3
27,28	2D5V_LAN_S5
29,30	3D3V_AUD_S0
19,31,32,33,36,39,40	3D3V_AUX_S5
27,28	3D3V_LAN_S5
3,4,7,9,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,41	3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,41	3D3V_S5
22,29,31,34,36	5V_AUX_S5
16,23,32,33,34,36,37,38	5V_S3
15,16,17,20,21,22,23,26,29,30,31,32,33,34,35,41	5V_S0
16,21,34,37,38	5V_S5
17,39,40,41	AD+
16,17,34,35,36,37,38,39,41	DCBATOUT
13,14,38,41	DDR_VREF_S0
7,13,14,38	DDR_VREF_S3
22,31,33,39	KBC_3D3V_AUX
16	LCDVDD_S0
5,6,35	VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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Title: **Table of Content**

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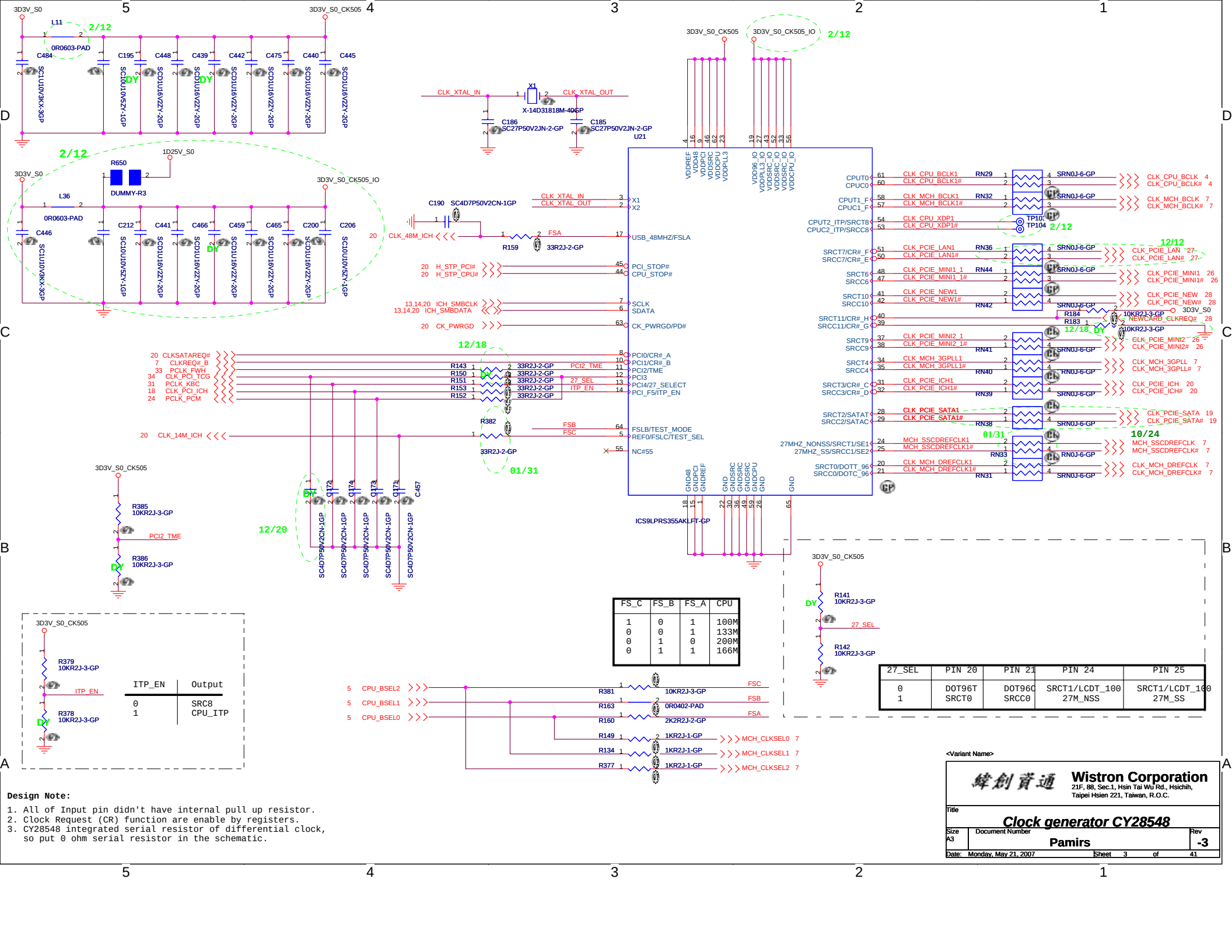

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

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Title: **Clock generator CY28548**

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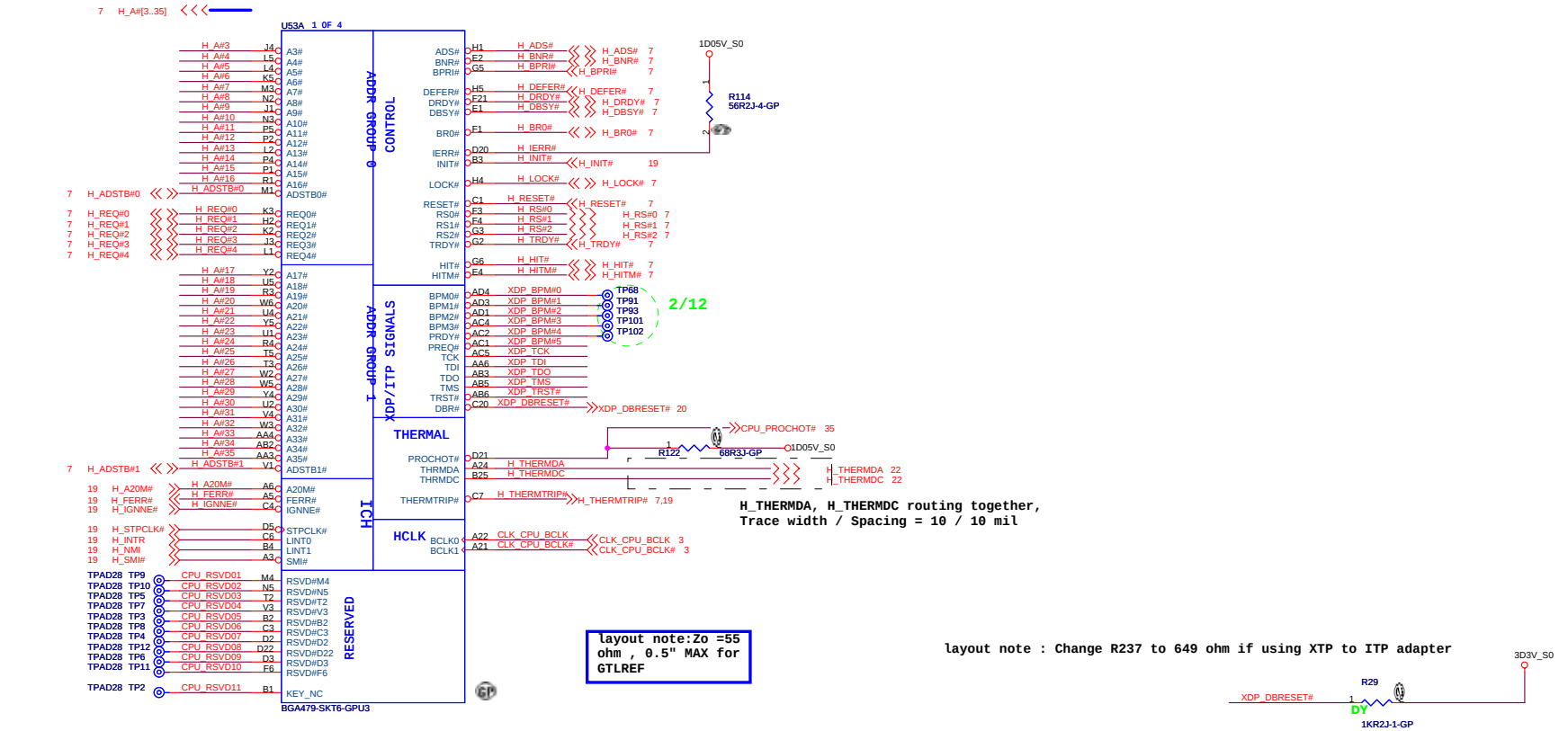
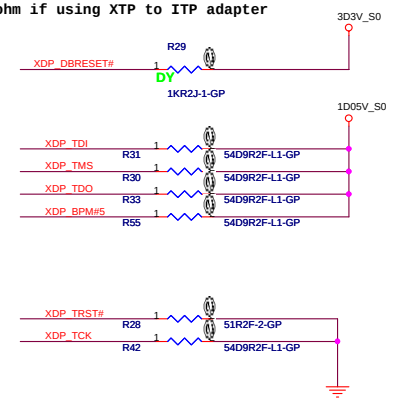
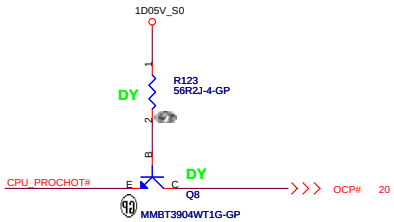


layout note : Change R237 to 649 ohm if using XTP to ITP adapter





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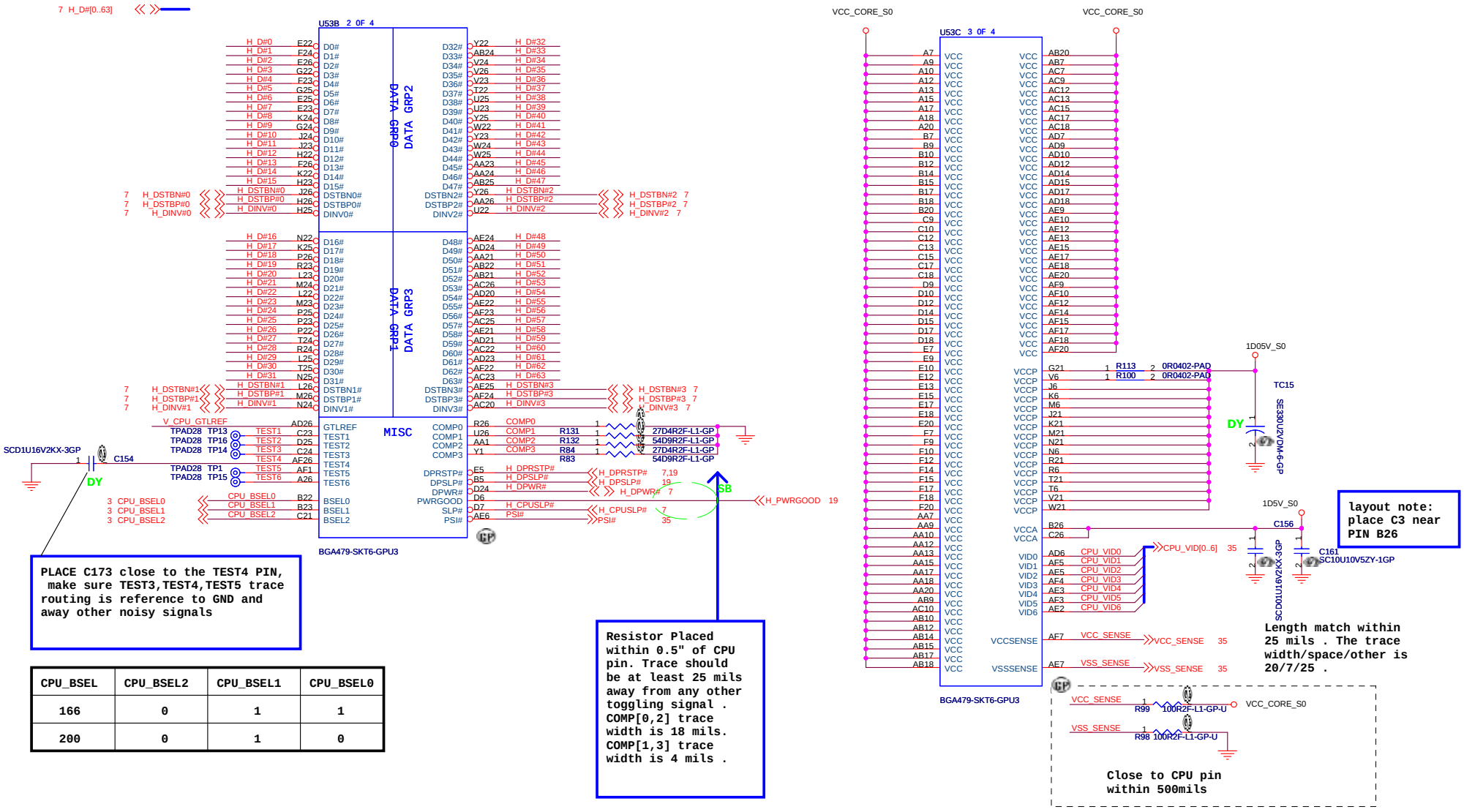
Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Pamirs | Rev: -3

Date: Wednesday, May 23, 2007 | Sheet 4 of 41



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Meron(2/3)-AGTL+/PWR

Size	Document Number	Rev
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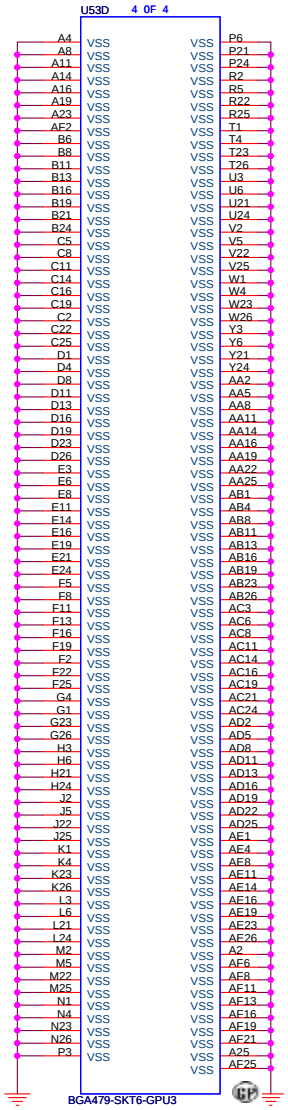
Date: Friday, May 18, 2007 Sheet 5 of 41



VCC_CORE_S0

3/5

Place these capacitors on L1
(North side ,Secondary Layer)

C111 C120 C127 C130 C135 C142 C146 C144 C828

SC10U10V5KX-2GP

VCC_CORE_S0

3/5

Place these capacitors on L1
(North side ,Secondary Layer)

C139 C131 C124 C145 C125 C136 C826 C117 C827

SC10U10V5KX-2GP

Mid Frequencd Decoupling

1D05V_S0

C107 C109 C108 C150 C149 C148

SCD1U16V2KX-3GP

Place these inside socket cavity on L1 (North side Secondary)

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Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Pamirs | Rev: -3

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

SB 0823

Layout Note :
Place C32 within 100 mils of NB

Layout Note :
Place C33 near
pin B3 of NB

0921 P/N CHANGE TO 71.CREST.M02

<Core Design>

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Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size	Document Number	Rev
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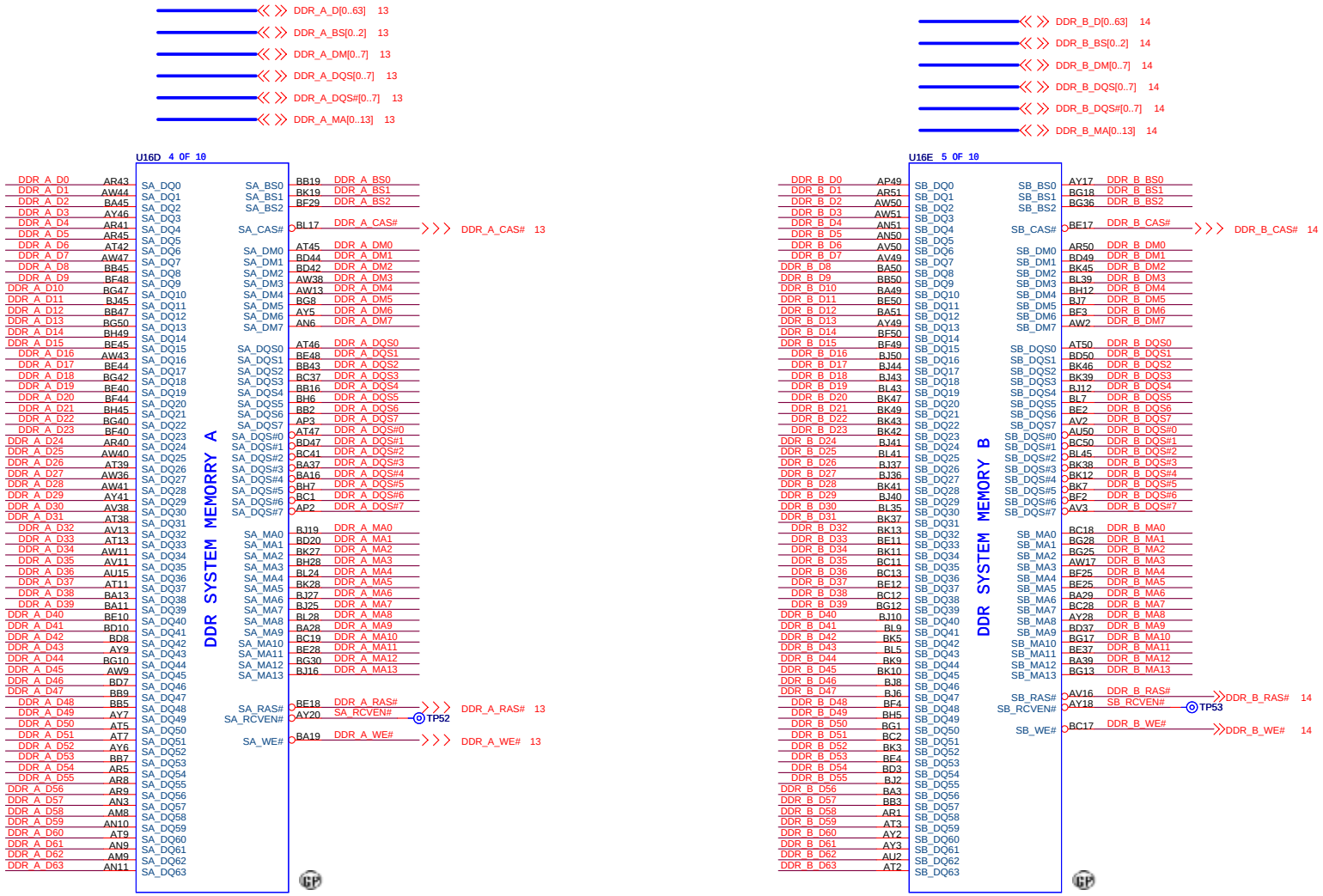

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Title
CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
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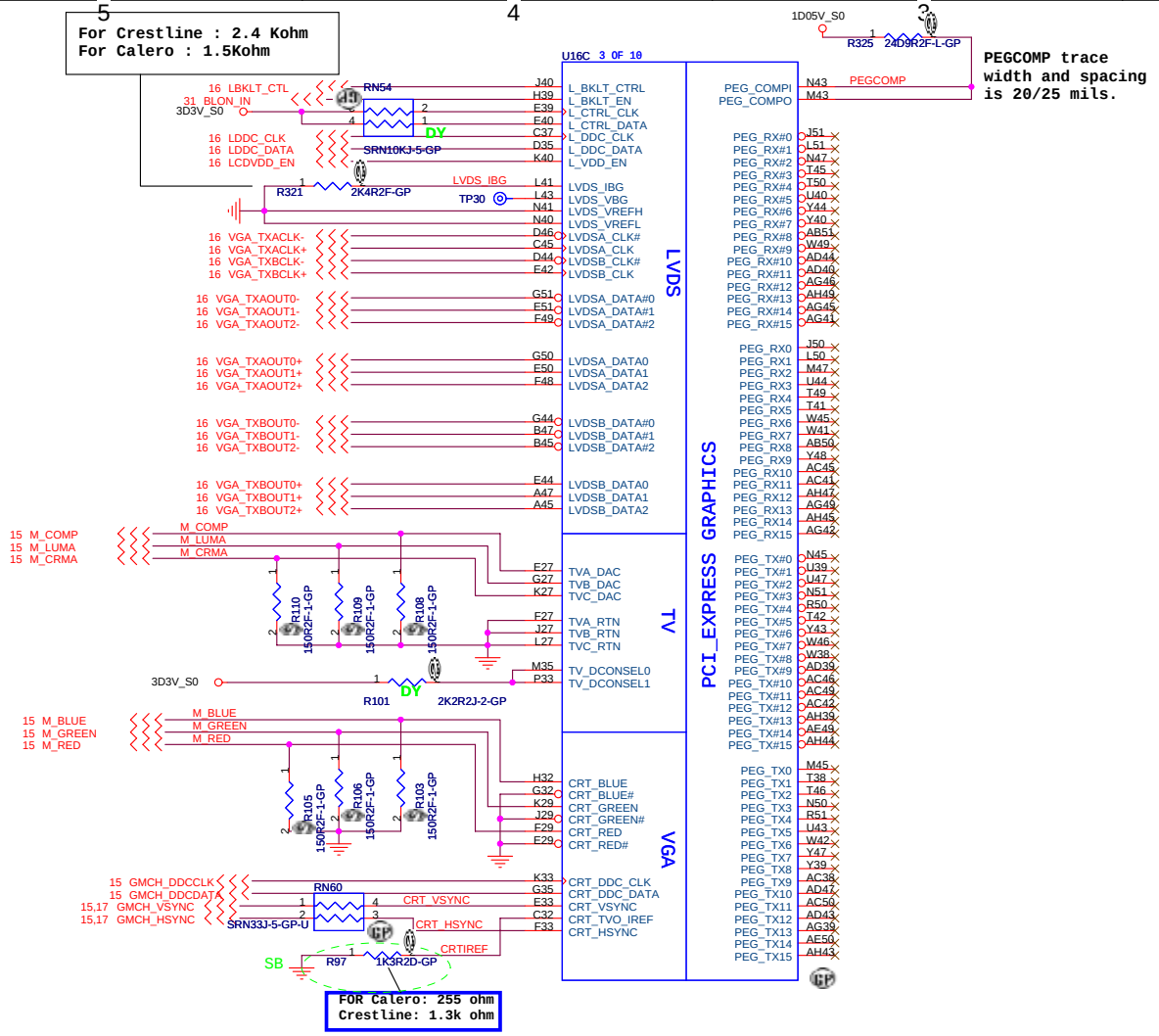

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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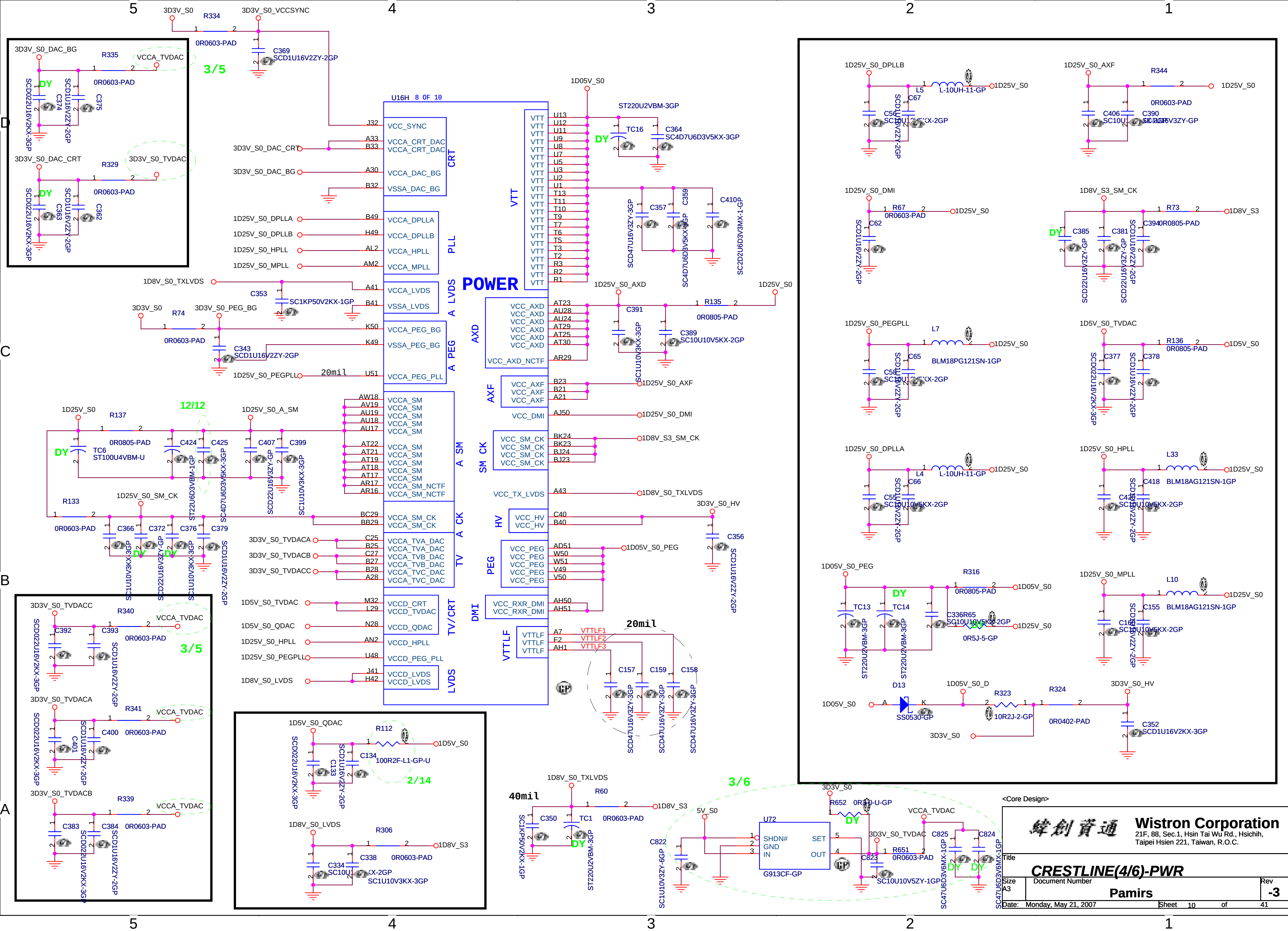
U16H 8 OF 10
POWER
VTT
CRT
PLL
A LVDS
A PEG
AXD
AXF
SM CK
A SM
A CK
HV
TV
PEG
DMI
TV/CRT
VTTLF
LVDS
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_NCTF
VCCA_SM_CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCC_AXD
VCC_AXD_NCTF
VCC_AXF
VCC_DMI
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_RXR_DMI
VTTLF
20mil
40mil
3/5
12/12
2/14
3/6
DY
3D3V_S0
3D3V_S0_VCCSYNC
1D05V_S0
1D25V_S0
1D8V_S3
1D5V_S0
5V_S0
U72
G913CF-GP
SHDN#
GND
IN
SET
OUT
D13
SS0530-GP
<Core Design>
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Title
CRESTLINE(4/6)-PWR
Size A3
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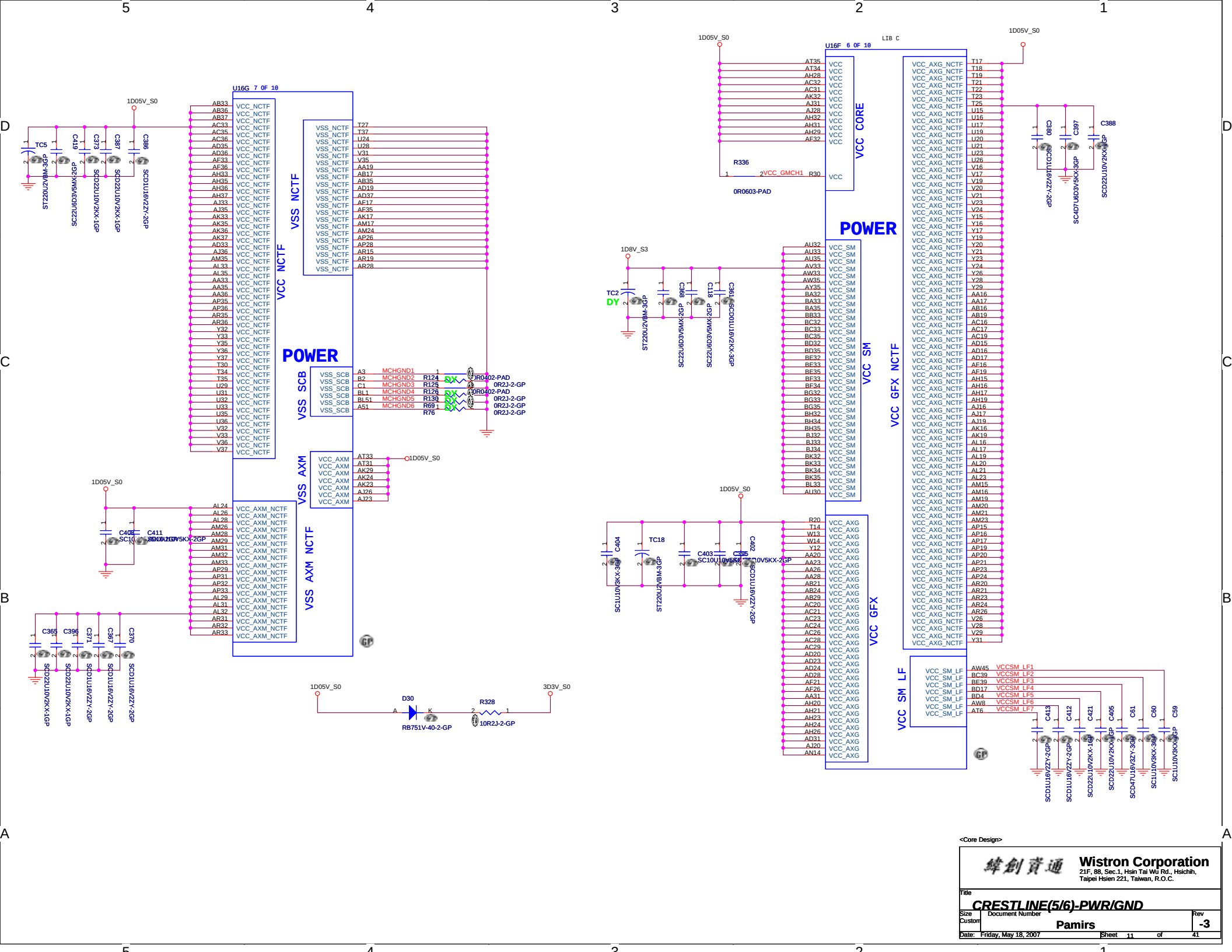
U16G 7 0F 10
VCC_NCTF
VSS_NCTF
VCC NCTF
VSS NCTF
POWER
VSS SCB
VSS AXM
VCC_AXM_NCTF
VSS AXM NCTF
1D05V_S0
U16F 6 0F 10
LIB C
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC_SM_LF
1D8V_S3
R336
0R0603-PAD
0R0402-PAD
0R2J-2-GP
D30
RB751V-40-2-GP
R328
10R2J-2-GP
3D3V_S0
<Core Design>
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Title
CRESTLINE(5/6)-PWR/GND
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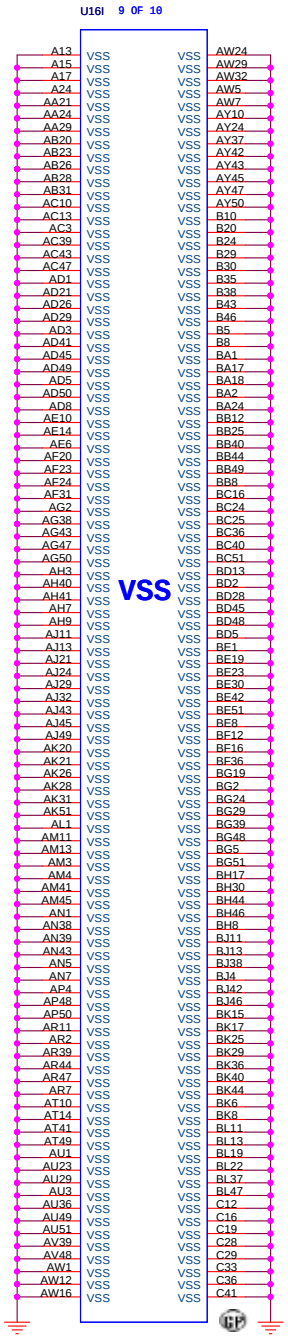

<Core Design>

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Title: ***CRESTLINE(6/6)-PWR/GND***

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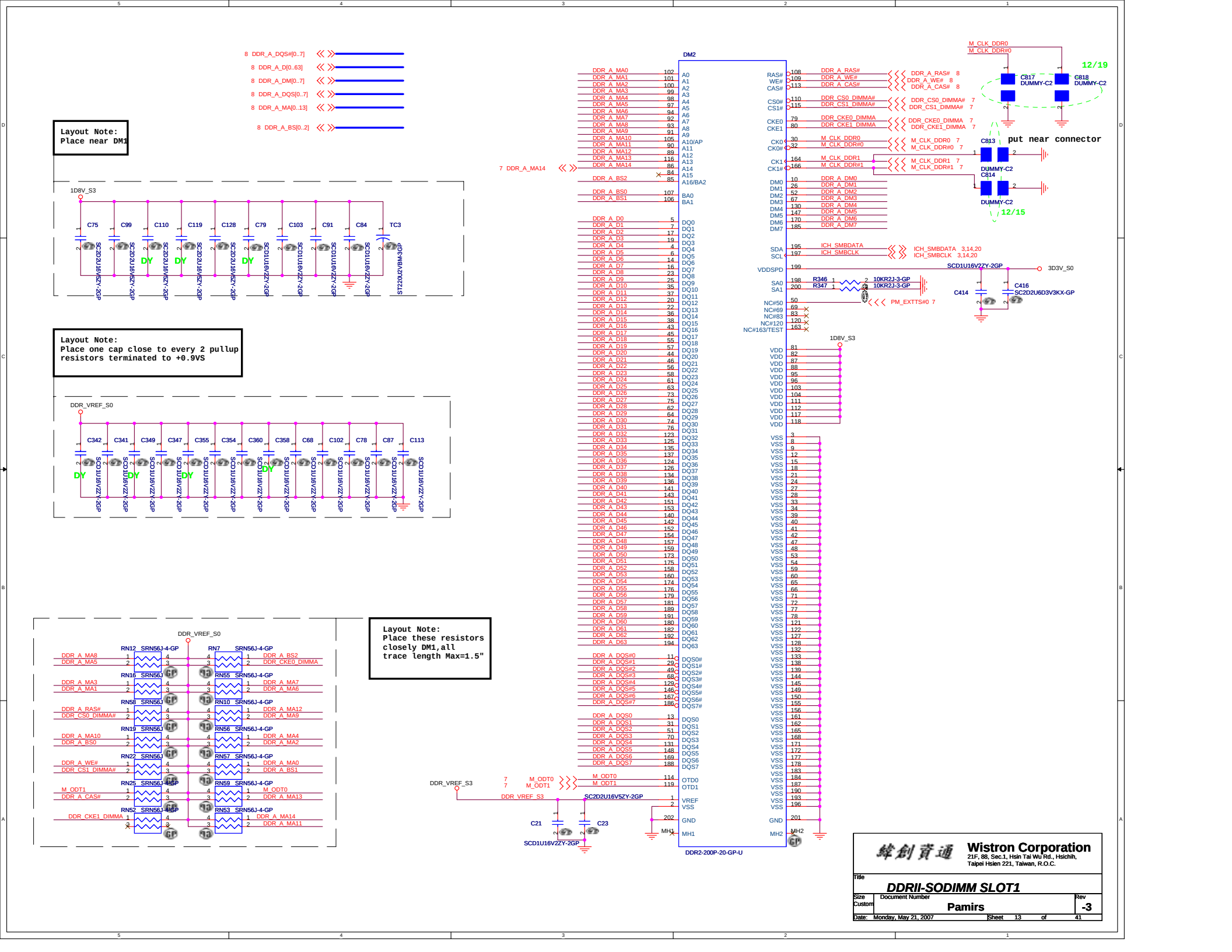
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C75 C99 C110 C119 C128 C79 C103 C91 C84 TC3
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C342 C341 C349 C347 C355 C354 C360 C358 C68 C102 C78 C87 C113
DY
DDR_VREF_S0
RN12 SRN56J-4-GP
RN7 SRN56J-4-GP
RN16 SRN56J-4-GP
RN55 SRN56J-4-GP
RN58 SRN56J-4-GP
RN10 SRN56J-4-GP
RN19 SRN56J-4-GP
RN56 SRN56J-4-GP
RN22 SRN56J-4-GP
RN57 SRN56J-4-GP
RN25 SRN56J-4-GP
RN59 SRN56J-4-GP
RN52 SRN56J-4-GP
RN53 SRN56J-4-GP
DDR_A_MA8 DDR_A_MA5 DDR_A_BS2 DDR_CKE0_DIMMA
DDR_A_MA3 DDR_A_MA1 DDR_A_MA7 DDR_A_MA6
DDR_A_RAS# DDR_CS0_DIMMA# DDR_A_MA12 DDR_A_MA9
DDR_A_MA10 DDR_A_BS0 DDR_A_MA4 DDR_A_MA2
DDR_A_WE# DDR_CS1_DIMMA# DDR_A_MA0 DDR_A_BS1
M_ODT1 DDR_A_CAS# M_ODT0 DDR_A_MA13
DDR_CKE1_DIMMA DDR_A_MA14 DDR_A_MA11
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C21 C23
SCD1U16V2ZY-2GP
DM2
DDR_A_MA0 DDR_A_MA1 DDR_A_MA2 DDR_A_MA3 DDR_A_MA4 DDR_A_MA5 DDR_A_MA6 DDR_A_MA7 DDR_A_MA8 DDR_A_MA9 DDR_A_MA10 DDR_A_MA11 DDR_A_MA12 DDR_A_MA13 DDR_A_MA14
DDR_A_BS2 DDR_A_BS0 DDR_A_BS1
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D4 DDR_A_D5 DDR_A_D6 DDR_A_D7 DDR_A_D8 DDR_A_D9 DDR_A_D10 DDR_A_D11 DDR_A_D12 DDR_A_D13 DDR_A_D14 DDR_A_D15 DDR_A_D16 DDR_A_D17 DDR_A_D18 DDR_A_D19 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27 DDR_A_D28 DDR_A_D29 DDR_A_D30 DDR_A_D31 DDR_A_D32 DDR_A_D33 DDR_A_D34 DDR_A_D35 DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D44 DDR_A_D45 DDR_A_D46 DDR_A_D47 DDR_A_D48 DDR_A_D49 DDR_A_D50 DDR_A_D51 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59 DDR_A_D60 DDR_A_D61 DDR_A_D62 DDR_A_D63
DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
M_ODT0 M_ODT1
DDR2-200P-20-GP-U
M_CLK_DDR0 M_CLK_DDR#0
12/19
C817 DUMMY-C2 C818 DUMMY-C2
C813 put near connector
DUMMY-C2 C814 DUMMY-C2
12/15
DDR_A_RAS# DDR_A_WE# DDR_A_CAS#
DDR_CS0_DIMMA# DDR_CS1_DIMMA#
DDR_CKE0_DIMMA DDR_CKE1_DIMMA
M_CLK_DDR1 M_CLK_DDR#1
DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7
ICH_SMBDATA ICH_SMBCLK
SCD1U16V2ZY-2GP 3D3V_S0
R346 R347 10KR2J-3-GP
C414 C416 SC2D2U6D3V3KX-GP
PM_EXTTS#0
1D8V_S3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
Pamirs
Rev -3
Date: Monday, May 21, 2007
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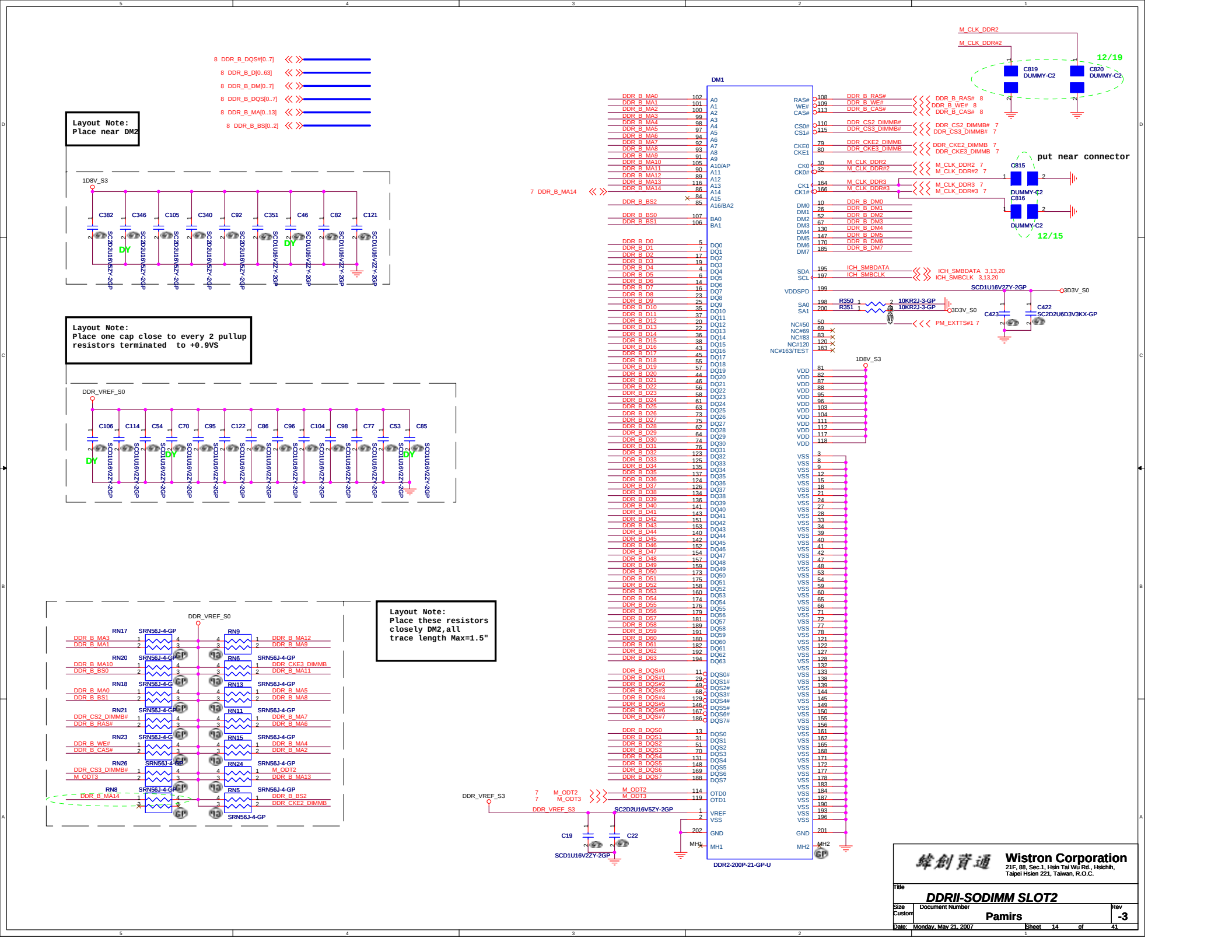
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
put near connector
12/19
12/15
DM1
DDR2-200P-21-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRII-SODIMM SLOT2
Pamirs
-3
Monday, May 21, 2007
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CRT I/F & CONNECTOR

0721

Layout Note:
Place these resistors close to the CRT-out connector

9 M_RED
9 M_GREEN
9 M_BLUE

L3 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

R7 150R2F-1-GP
R6 150R2F-1-GP
R5 150R2F-1-GP

C16 C13 C11 C14 C12 C10 SC10P50V2JN-4GP

CRT_R CRT_R 17
CRT_G CRT_G 17
CRT_B CRT_B 17

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0
C7 SCD01U16V2KX-3GP
F1 FUSE-1D1A6V-8GP
5V_S0
D4 RB751V-40-2-GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U1 20.20424.015
CRT_R CRT_G CRT_B
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON

C8 SC33P50V2JN-3GP DY
C9 SC33P50V2JN-3GP DY
C6 SC22P50V2JN-4GP
C5 SC22P50V2JN-4GP

D10 BAV99-7-F-GP
D12 BAV99-7-F-GP
DDC_DATA_CON
DDC_CLK_CON

U2 PACDN009MR-GP-U
GMCH_HSYNC
GMCH_VSYNC
CRT_R CRT_G CRT_B

5V_S0
C320 SCD1U16V2ZY-2GP
PR_INSERT 17

9,17 GMCH_HSYNC
9,17 GMCH_VSYNC

U5A U5B TSAHCT125PW-GP
HSYNC_5
VSYNC_5

RN4 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP

U1 2N7002DW-1-GP
9 GMCH_DDCDATA
17 DDC_CLK_CON
DDC_DATA_CON
DDC_CLK_CON
DDC_DATA_CON 17
GMCH_DDCCLK 9

5V @ ext. CRT side

TV OUT CONN

connector

9 M_CRMA
9 M_COMP
9 M_LUMA

L23 L24 L25 BLM18BB470SN1-GP

R271 R1 R2 150R2F-1-GP

C293 C292 C295 C294 C297 C296 SC10P50V2JN-4GP

0721

TV_CRMA 17
TV_COMP 17
TV_LUMA 17

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-18-GP
TV_LUMA
TV_CRMA
TV_COMP
LUMA CRMA COMP NC#2 NC#5 GND GND GND GND
22.10021.H31

D1 BAV99-7-F-GP
D3 BAV99-7-F-GP
D2 BAV99-7-F-GP
3D3V_S0
C1 SCD1U16V2ZY-2GP DY
C3 SCD1U16V2ZY-2GP DY
C2 SCD1U16V2ZY-2GP DY

<Core Design>

鋒創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Pamirs
Rev: -3
Date: Monday, May 21, 2007
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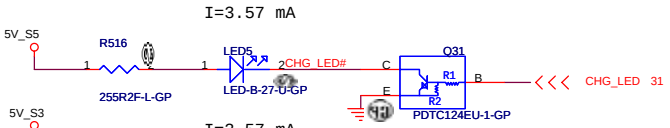
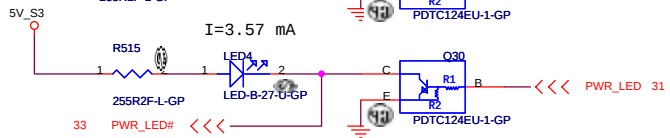
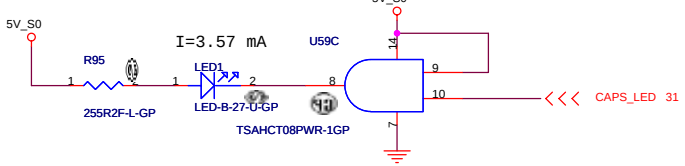
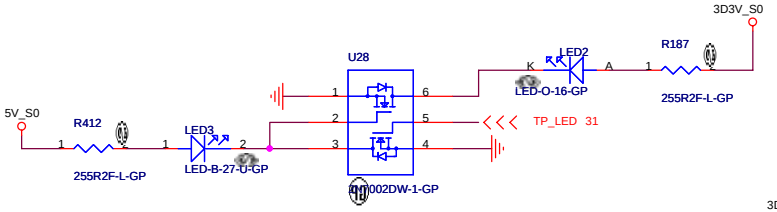
LED / INVERTER INTERFACE

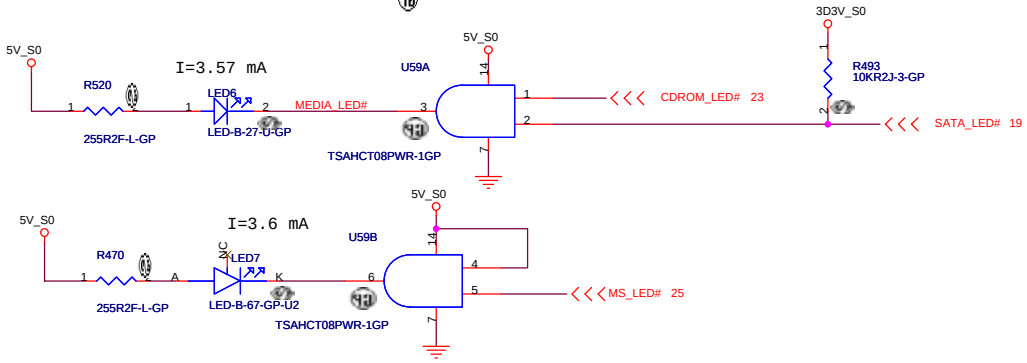
LCD/INV CONN

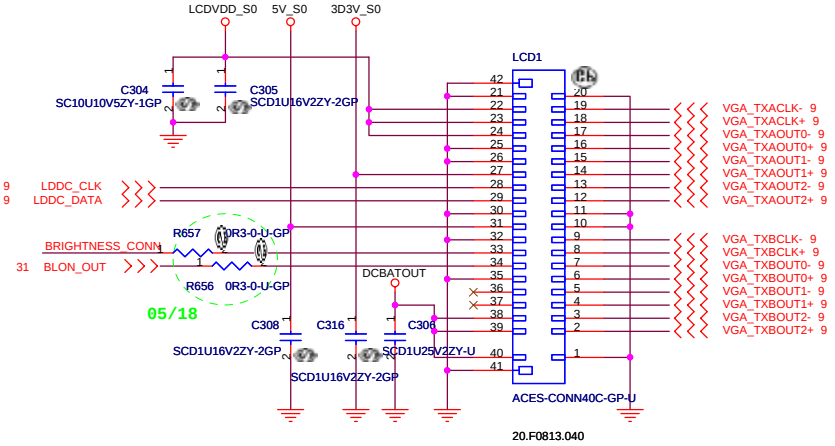


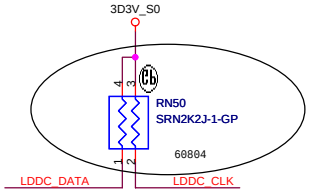


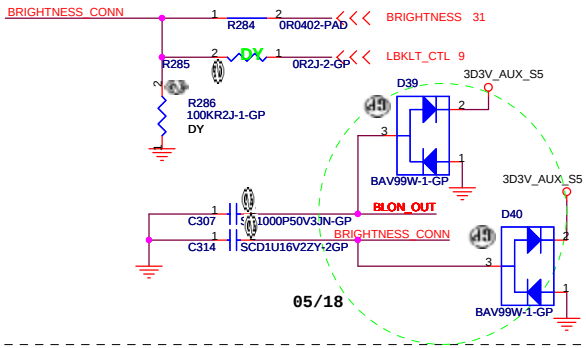


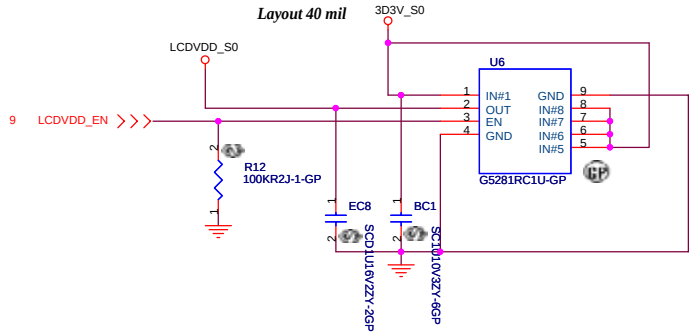


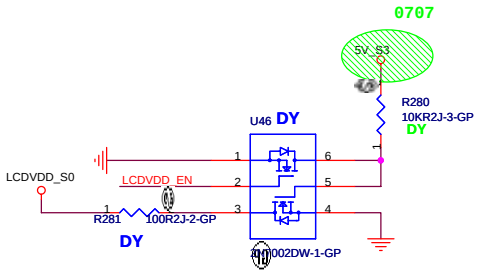












<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
Size: Custom	Document Number: Pamirs	Rev: -3
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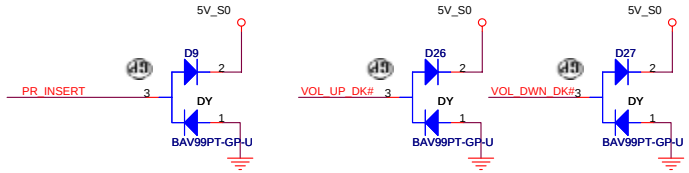
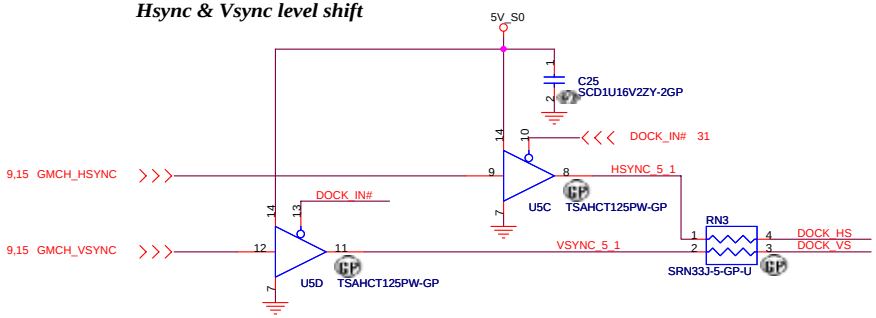
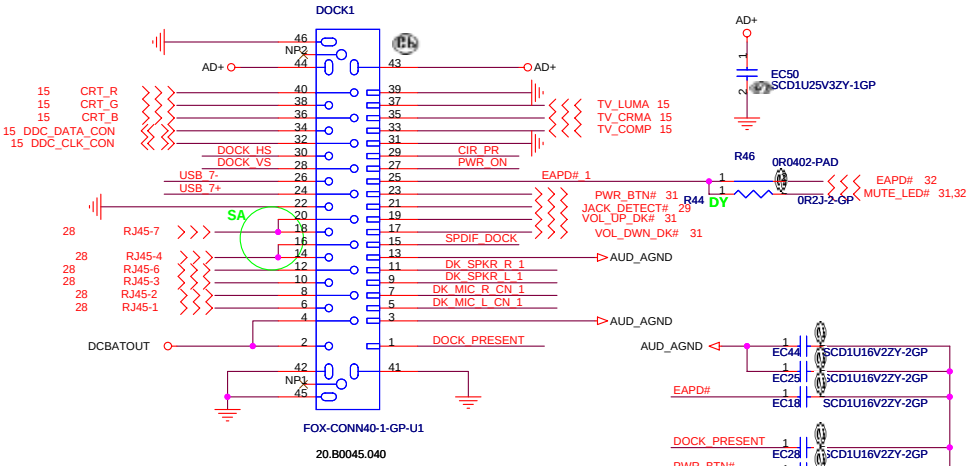
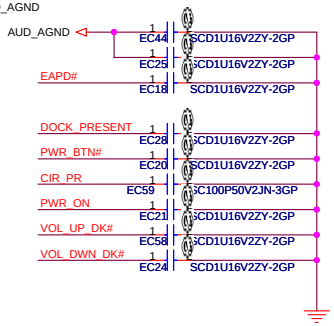
Docking Connector

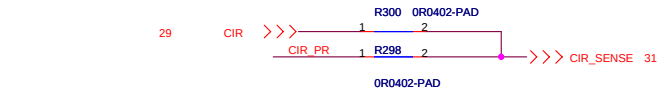


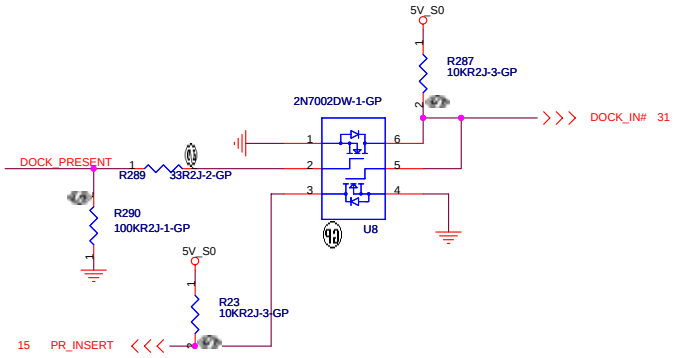
Hsync & Vsync level shift

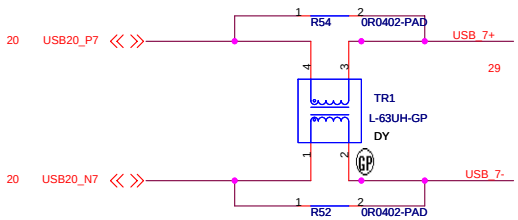


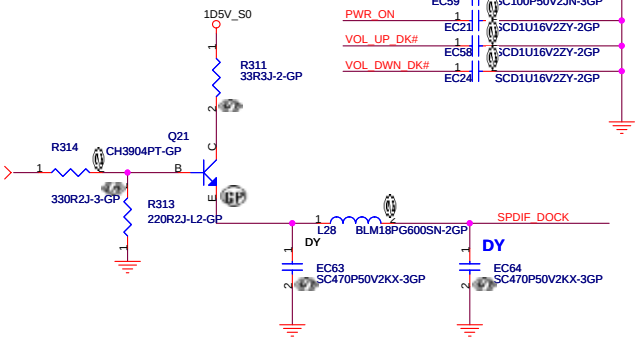


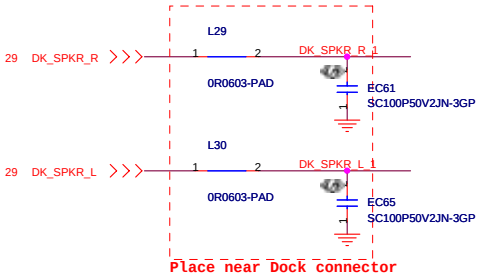


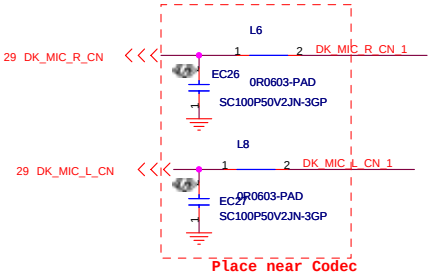


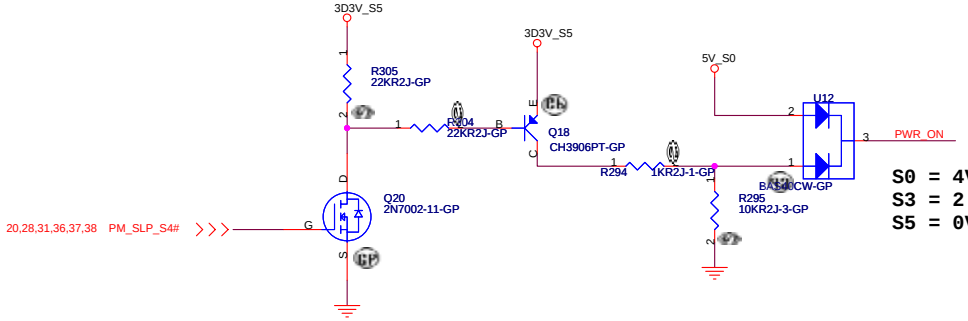












S0 = 4V
S3 = 2.5V
S5 = 0V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Board to board conn/ Docking

Size	Document Number	Rev
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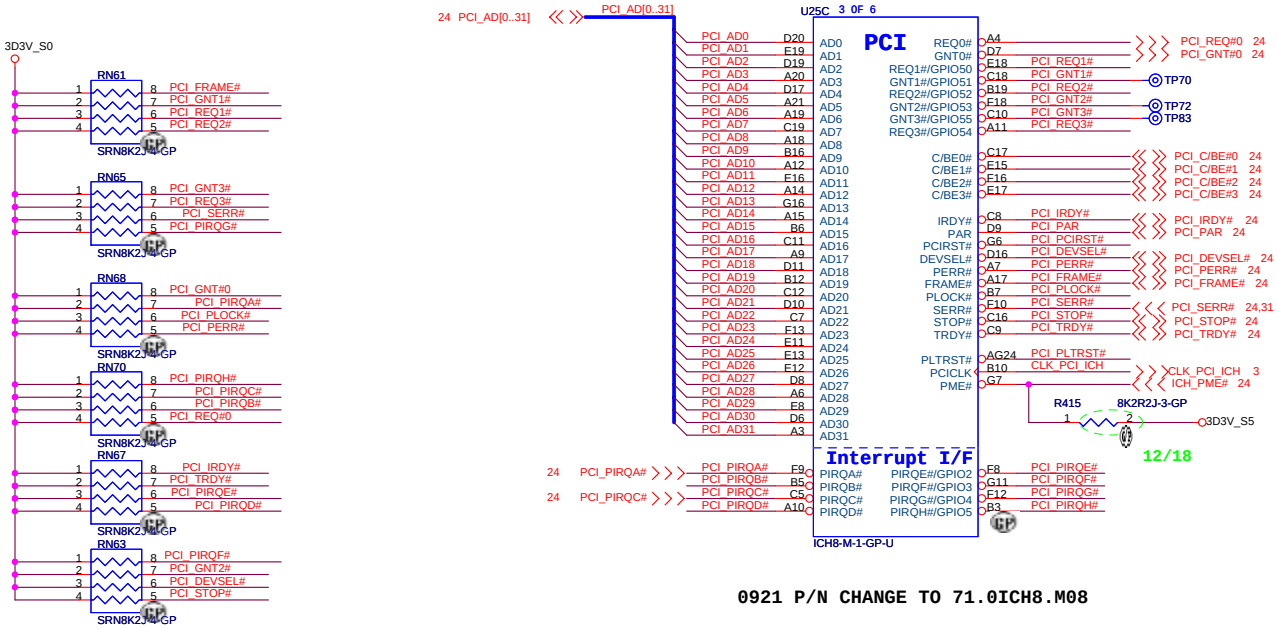
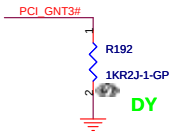
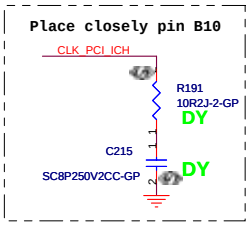


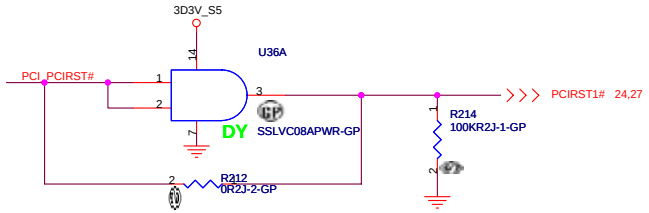
0921 P/N CHANGE TO 71.0ICH8.M08

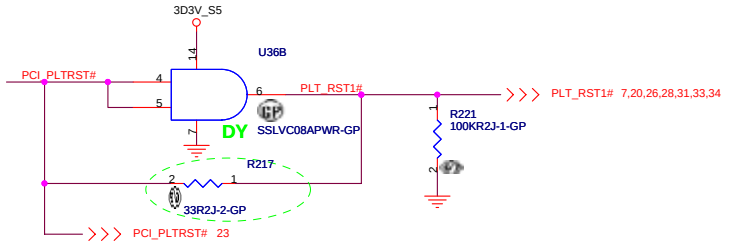


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size	Document Number	Rev
A3	Pamirs	-3

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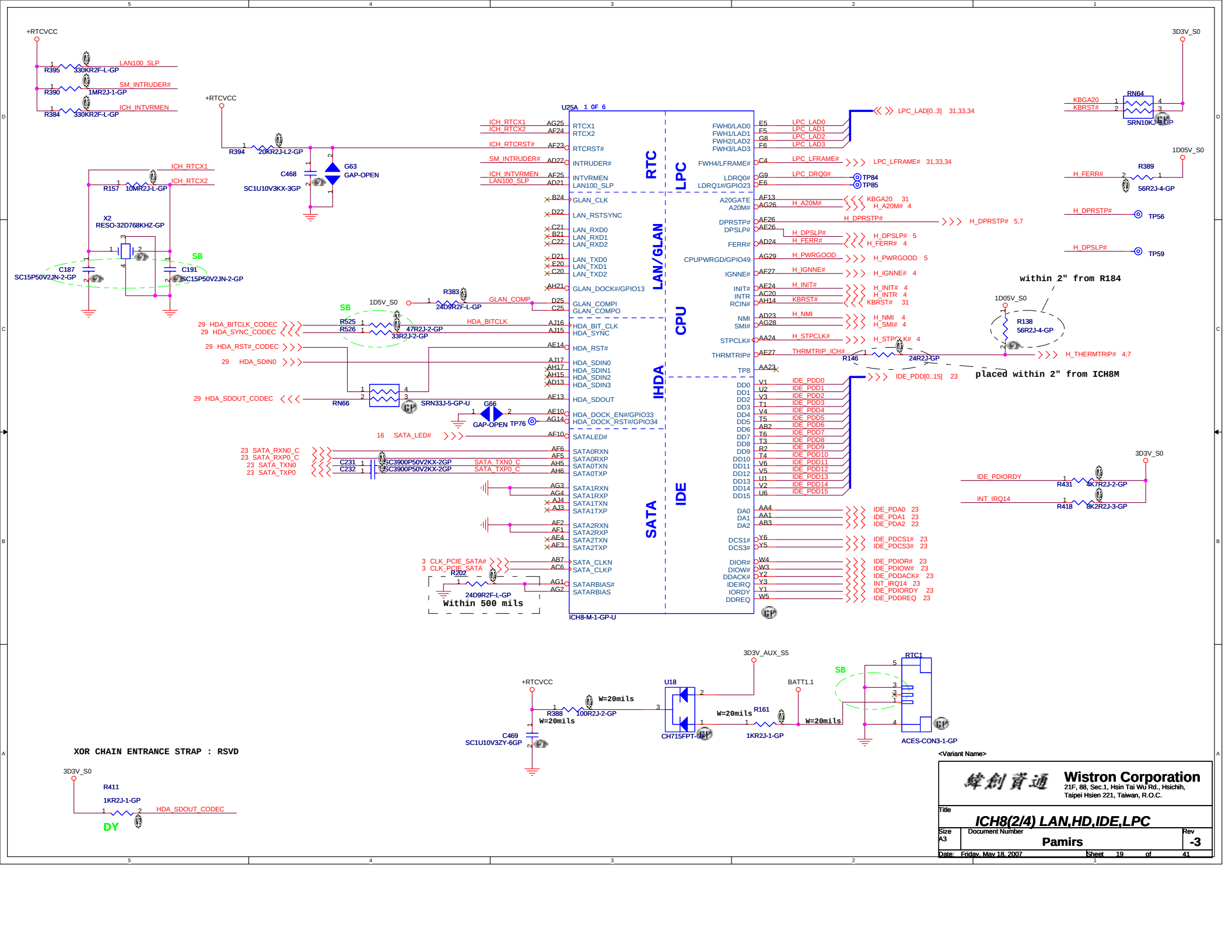
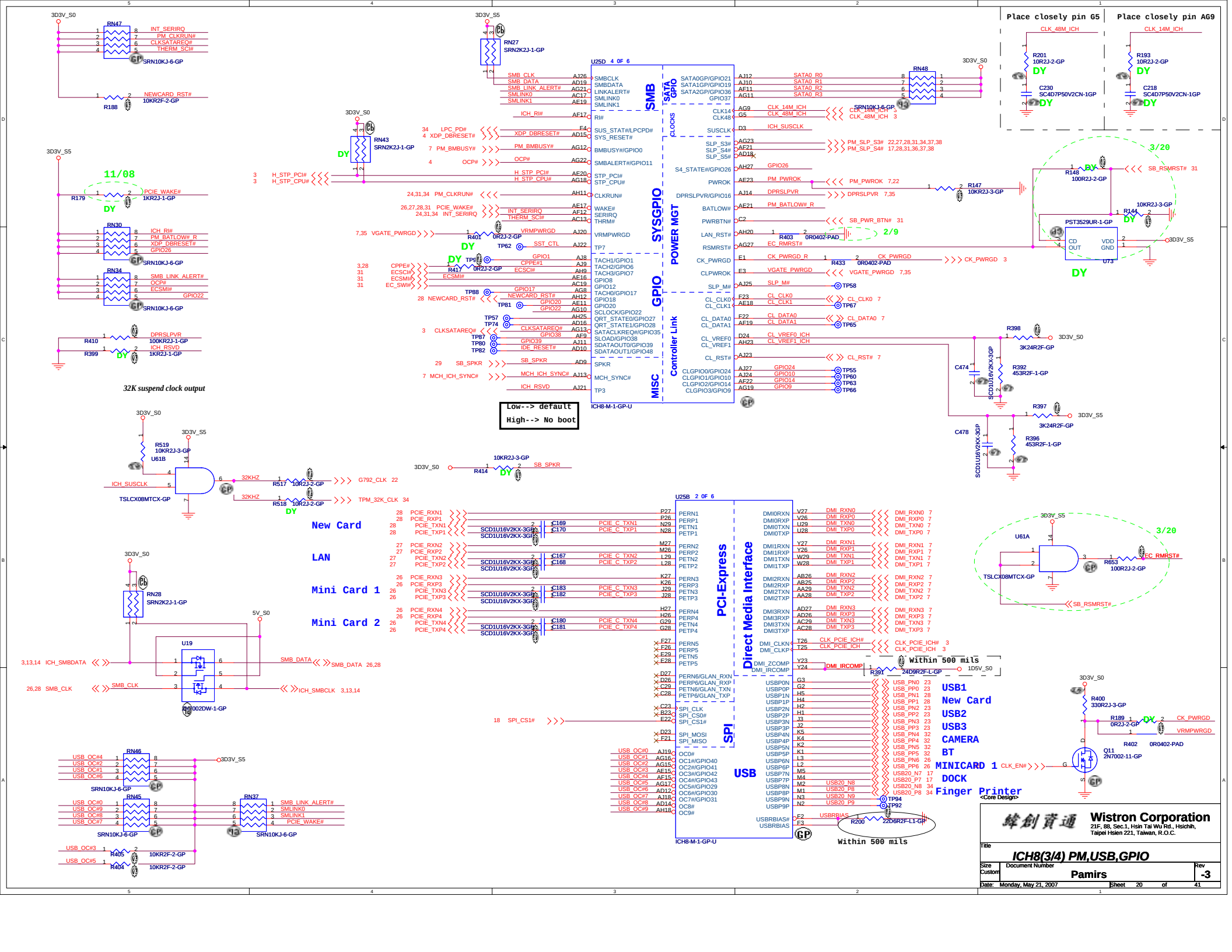
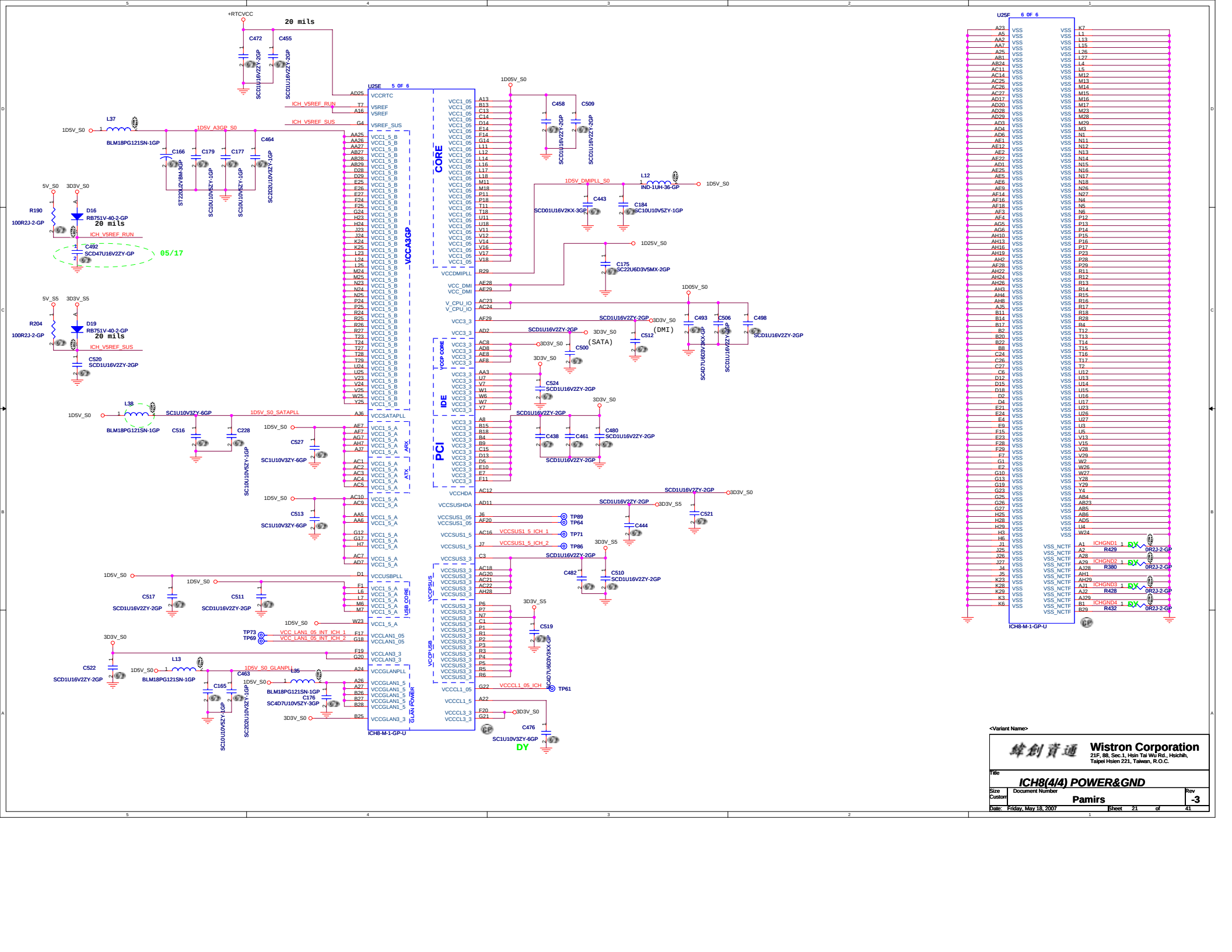
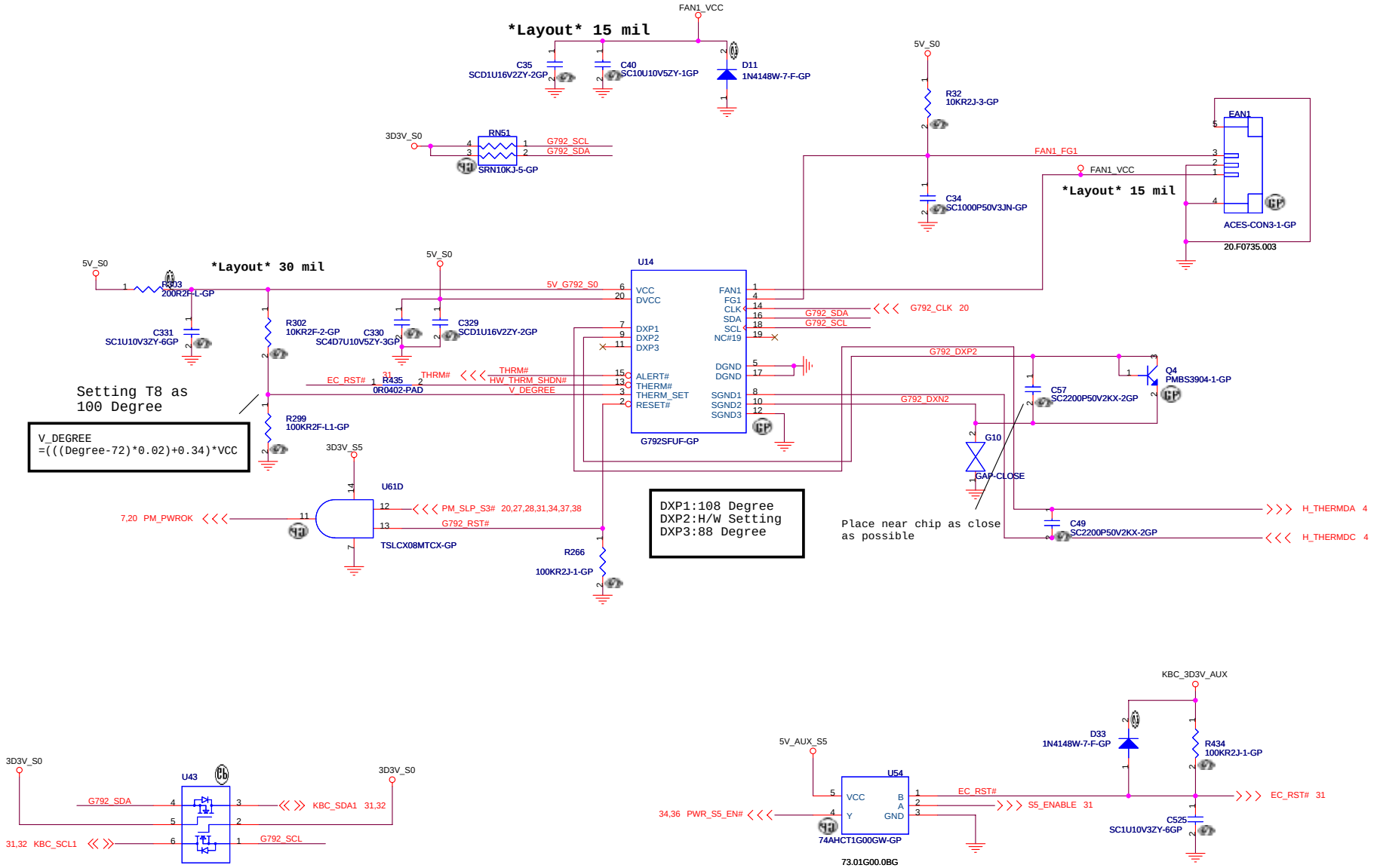

+RTCVCC
R395 330KR2F-L-GP
LAN100_SLP
R390 1MR2J-1-GP
SM_INTRUDER#
R384 330KR2F-L-GP
ICH_INTVRMEN
R394 20KR2J-L2-GP
G63 GAP-OPEN
C468 SC1U10V3KX-3GP
ICH_RTCX1
ICH_RTCX2
R157 10MR2J-L-GP
X2 RESO-32D768KHZ-GP
SB
C187 SC15P50V2JN-2-GP
C191 SC15P50V2JN-2-GP
U25A 1 0F 6
RTC
LPC
LAN/GLAN
CPU
IHDA
IDE
SATA
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH8-M-1-GP-U
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD[0..3] 31,33,34
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME# 31,33,34
LPC_DRQ0#
TP84
TP85
KBGA20 31
H_A20M# 4
H_DPRSTP# 5,7
H_DPSLP# 5
H_FERR# 4
H_PWRGOOD 5
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRST# 31
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP# 4,7
IDE_PDD[0..15] 23
IDE_PDA0 23
IDE_PDA1 23
IDE_PDA2 23
IDE_PDCS1# 23
IDE_PDCS3# 23
IDE_PDIOR# 23
IDE_PDIOW# 23
IDE_PDDACK# 23
INT_IRQ14 23
IDE_PDIORDY 23
IDE_PDDREQ 23
3D3V_S0
RN64 SRN10KJ-GP
KBGA20
KBRST#
1D05V_S0
R389 56R2J-4-GP
H_FERR#
H_DPRSTP#
TP56
H_DPSLP#
TP59
within 2" from R184
R138 56R2J-4-GP
R146 24R2J-GP
placed within 2" from ICH8M
R383 24D9R2F-L-GP
GLAN_COMP
R525 47R2J-2-GP
R526 33R2J-2-GP
HDA_BITCLK
29 HDA_BITCLK_CODEC
29 HDA_SYNC_CODEC
29 HDA_RST#_CODEC
29 HDA_SDIN0
29 HDA_SDOUT_CODEC
RN66 SRN33J-5-GP-U
G66 GAP-OPEN
TP76
16 SATA_LED#
23 SATA_RXN0_C
23 SATA_RXP0_C
23 SATA_TXN0
23 SATA_TXP0
C231 SC3900P50V2KX-2GP
C232 SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
3 CLK_PCIE_SATA#
3 CLK_PCIE_SATA
R202 24D9R2F-L-GP
Within 500 mils
IDE_PDIORDY
INT_IRQ14
R431 4K7R2J-2-GP
R418 8K2R2J-3-GP
3D3V_AUX_S5
BATT1.1
U18 CH715FPT-GP
R388 100R2J-2-GP
R161 1KR2J-1-GP
W=20mils
C469 SC1U10V3ZY-6GP
RTC1 ACES-CON3-1-GP
SB
XOR CHAIN ENTRANCE STRAP : RSVD
R411 1KR2J-1-GP
HDA_SDOUT_CODEC
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 19 of 41


Place closely pin G5
Place closely pin AG9
CLK_48M_ICH
CLK_14M_ICH
R201 10R2J-2-GP DY
C230 SC4D7P50V2CN-1GP DY
R193 10R2J-2-GP DY
C218 SC4D7P50V2CN-1GP DY
U25D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
CLGPIO3/GPIO9
ICH8-M-1-GP-U
Low--> default
High--> No boot
RN47 INT_SERIRQ PM_CLKRUN# CLKSATAREQ# THERM_SCI# SRN10KJ-6-GP
R188 10KR2F-2-GP NEWCARD_RST#
RN27 SRN2K2J-1-GP
RN43 SRN2K2J-1-GP DY
RN48 SRN10K1-6-GP
R179 1KR2J-1-GP PCIE_WAKE# DY
11/08
RN30 ICH_RI# PM_BATLOW#_R XDP_DBRESET# GPIO26 SRN10KJ-6-GP
RN34 SMB_LINK_ALERT# OCP# ECSMI# GPIO22 SRN10KJ-6-GP
R410 100KR2J-1-GP DPRSLPVR
R399 1KR2J-1-GP ICH_RSVD DY
32K suspend clock output
R401 0R2J-2-GP VGATE_PWRGD
R417 0R2J-2-GP CPPE#
R403 0R0402-PAD
R433 0R0402-PAD CK_PWRGD
R147 10KR2J-3-GP
R148 100R2J-2-GP DY SB_RSMRST# 31
R144 10KR2J-3-GP DY
PST3529UR-1-GP U73
3/20
2/9
R398 3K24R2F-GP
R397 3K24R2F-GP
C474 SCD1U16V2KX-3GP
C478 SCD1U16V2KX-3GP
R392 453R2F-1-GP
R396 453R2F-1-GP
R519 10KR2J-3-GP U61B TSLCX08MTCX-GP
R517 10KR2J-2-GP 32KHZ G792_CLK 22
R518 10KR2J-2-GP 32KHZ TPM_32K_CLK 34
R414 10KR2J-3-GP SB_SPKR
New Card
LAN
Mini Card 1
Mini Card 2
U25B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP DMI_ZCOMP DMI_IRCOMP
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBRBIAS USBRBIAS#
ICH8-M-1-GP-U
R391 24D9R2F-L-GP Within 500 mils
R200 22D6R2F-L1-GP Within 500 mils
U61A TSLCX08MTCX-GP R653 100R2J-2-GP EC_RMRST#
SB_RSMRST#
R400 330R2J-3-GP
R189 0R2J-2-GP DY CK_PWRGD
R402 0R0402-PAD VRMPWRGD
Q11 2N7002-11-GP
USB1
New Card
USB2
USB3
CAMERA
BT
MINICARD 1 CLK_EN#
DOCK
Finger Printer
RN46 SRN10KJ-6-GP
RN45 SRN10KJ-6-GP
RN37 SRN10KJ-6-GP
R405 10KR2F-2-GP USB_OC#3
R404 10KR2F-2-GP USB_OC#5
U19 M1002DW-1-GP
RN28 SRN2K2J-1-GP
SCD1U16V2KX-3GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(3/4) PM,USB,GPIO
Size Custom
Document Number Pamirs
Rev -3
Date: Monday, May 21, 2007
Sheet 20 of 41


+RTCVCC
20 mils
C472
C455
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
U25E 5 OF 6
VCCRTC
ICH_V5REF_RUN
VSREF
ICH_V5REF_SUS
VSREF_SUS
L37
1D5V_S0
BLM18PG121SN-1GP
1D5V_A3GP_S0
C166
C179
C177
C464
ST220U2V8M-3GP
SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
SC22D2U10V2Z1-1GP
5V_S0
3D3V_S0
R190
100R2J-2-GP
D16
RB751V-40-2-GP
20 mils
ICH_V5REF_RUN
C492
SCD47U16V2ZY-GP
05/17
5V_S5
3D3V_S5
R204
100R2J-2-GP
D19
RB751V-40-2-GP
20 mils
ICH_V5REF_SUS
C520
SCD1U16V2ZY-2GP
L38
1D5V_S0
BLM18PG121SN-1GP
SC1U10V3ZY-6GP
1D5V_S0_SATAPLL
C516
C228
SC10U10V5ZY-1GP
1D5V_S0
C527
SC1U10V3ZY-6GP
1D5V_S0
C513
SC1U10V3ZY-6GP
1D5V_S0
D1
C517
SCD1U16V2ZY-2GP
1D5V_S0
C511
SCD1U16V2ZY-2GP
1D5V_S0
TP73
TP69
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
3D3V_S0
L13
1D5V_S0
BLM18PG121SN-1GP
C522
SCD1U16V2ZY-2GP
1D5V_S0_GLANPLL
L35
C463
C165
SC10U10V5ZY-1GP
SC22D2U10V2ZY-1GP
1D5V_S0
BLM18PG121SN-1GP
C176
SC4D7U10V5ZY-3GP
3D3V_S0
CORE
VCCA3GP
IDE
PCI
VCCP_CORE
VCCP_USB
VCCP5U_S
USB_CORE
GLAN_POWER
ARX
ATX
VCC1_05
VCC3_3
VCCDMIPLL
VCC_DMI
V_CPU_IO
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCHDA
VCCUSBPLL
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3
ICH8-M-1-GP-U
1D05V_S0
C458
C509
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
1D5V_DMIPLL_S0
L12
IND-1UH-36-GP
1D5V_S0
C443
SCD01U16V2KX-3GP
C184
SC10U10V5ZY-1GP
1D25V_S0
C175
SC22U6D3V5MX-2GP
1D05V_S0
SCD1U16V2ZY-2GP
3D3V_S0
(SATA)
C500
C493
C506
C498
SCD1U16V2ZY-2GP
SC4D7U6D3V2KX-GP
SCD1U16V2ZY-2GP
(DMI)
C512
3D3V_S0
C524
SCD1U16V2ZY-2GP
3D3V_S0
SCD1U16V2ZY-2GP
C438
C461
C480
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S0
SCD1U16V2ZY-2GP
3D3V_S0
C444
C521
TP89
TP64
TP71
TP86
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
3D3V_S5
SCD1U16V2ZY-2GP
C482
C510
SCD1U16V2ZY-2GP
3D3V_S5
C519
SC4D7U6D3V3KX-GP
VCCCL1_05_ICH
TP61
3D3V_S0
C476
SC1U10V3ZY-6GP
DY
U25F 6 OF 6
VSS
VSS_NCTF
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R429
R380
R428
R432
0R2J-2-GP
ICH8-M-1-GP-U
<Variant Name>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Pamirs
Rev
-3
Date: Friday, May 18, 2007
Sheet 21 of 41



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

Size	Document Number	Rev
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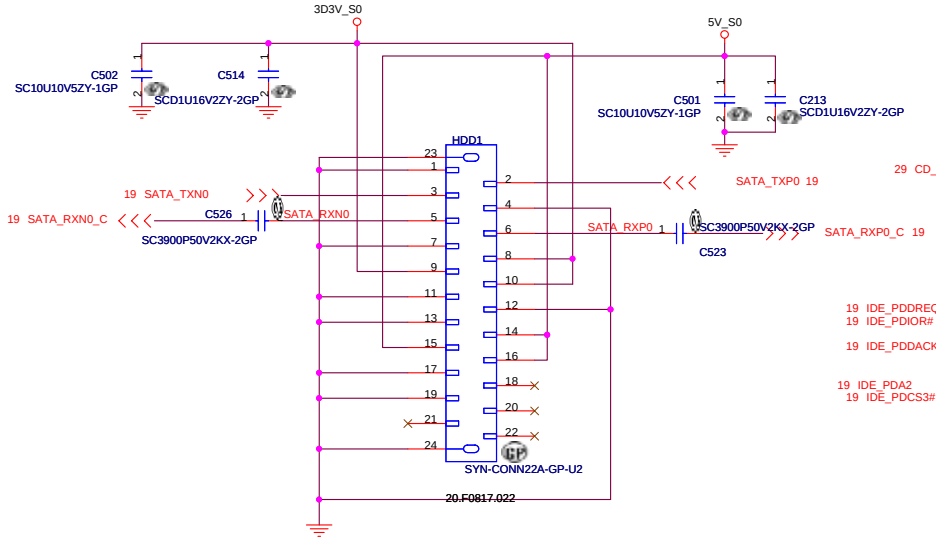
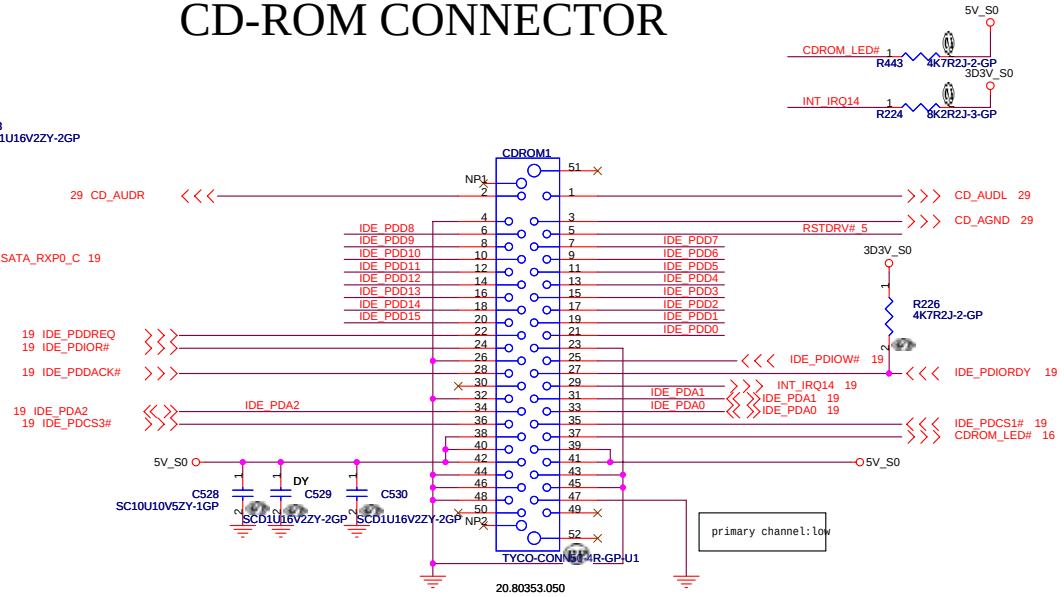
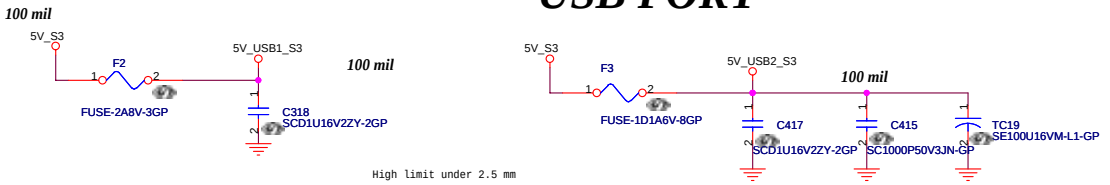
SATA HD Connector

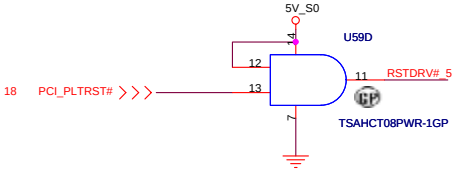


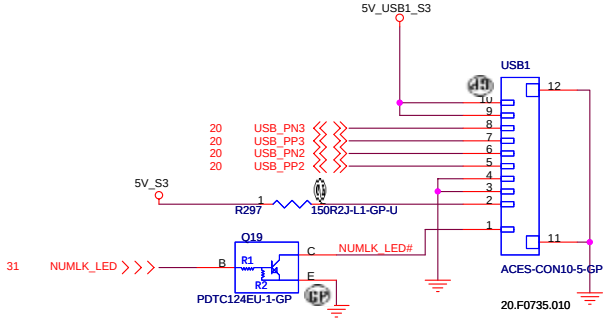
CD-ROM CONNECTOR

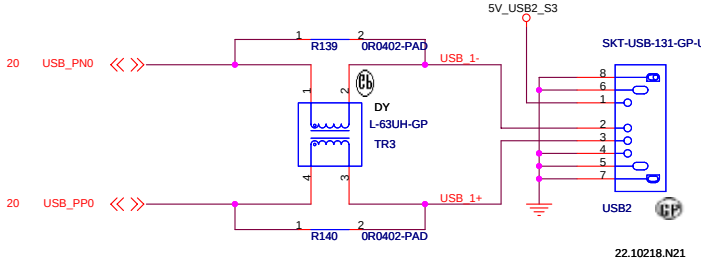


USB PORT









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HD/CDROM/USB***

Size	Document Number	Rev
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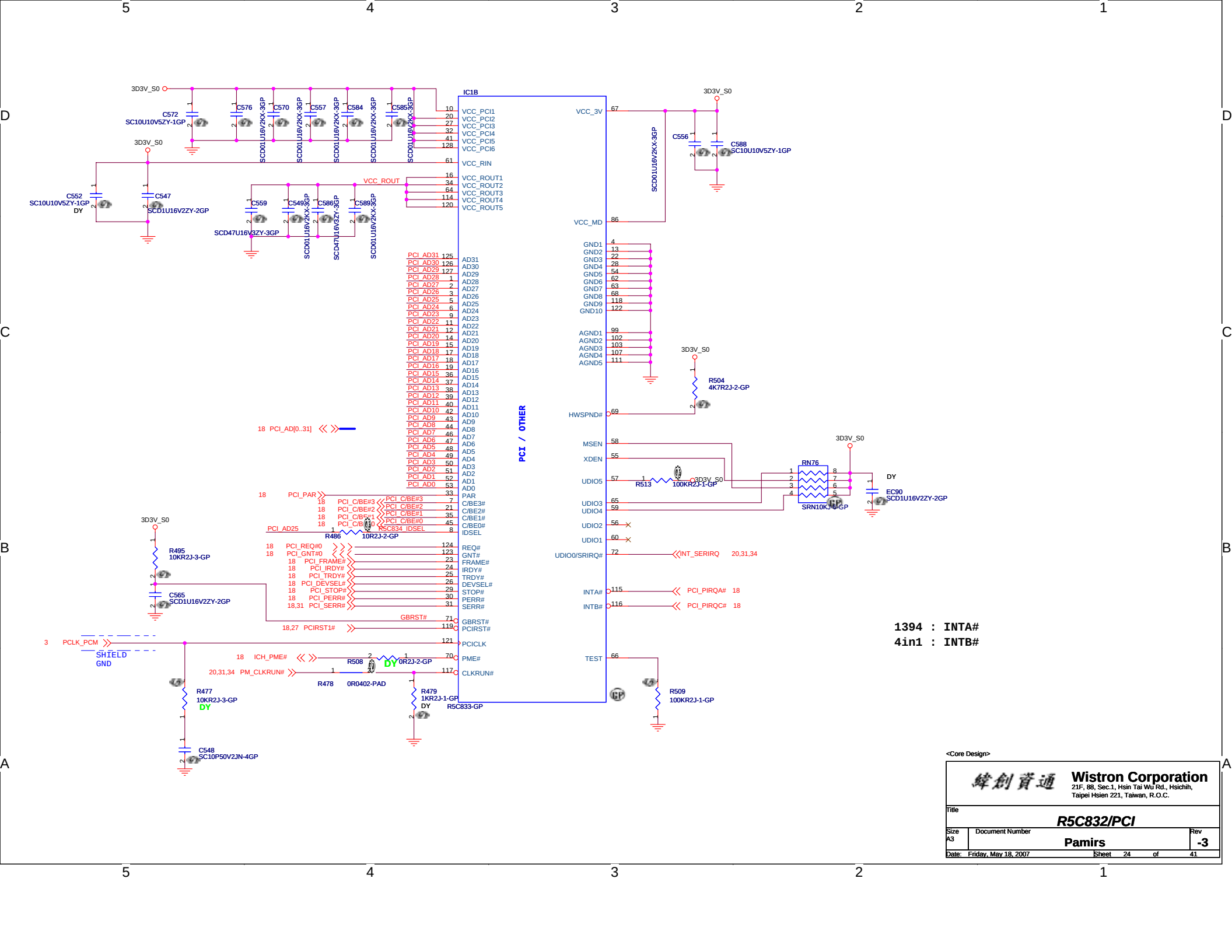
Date: Friday, May 18, 2007 Sheet 23 of 41



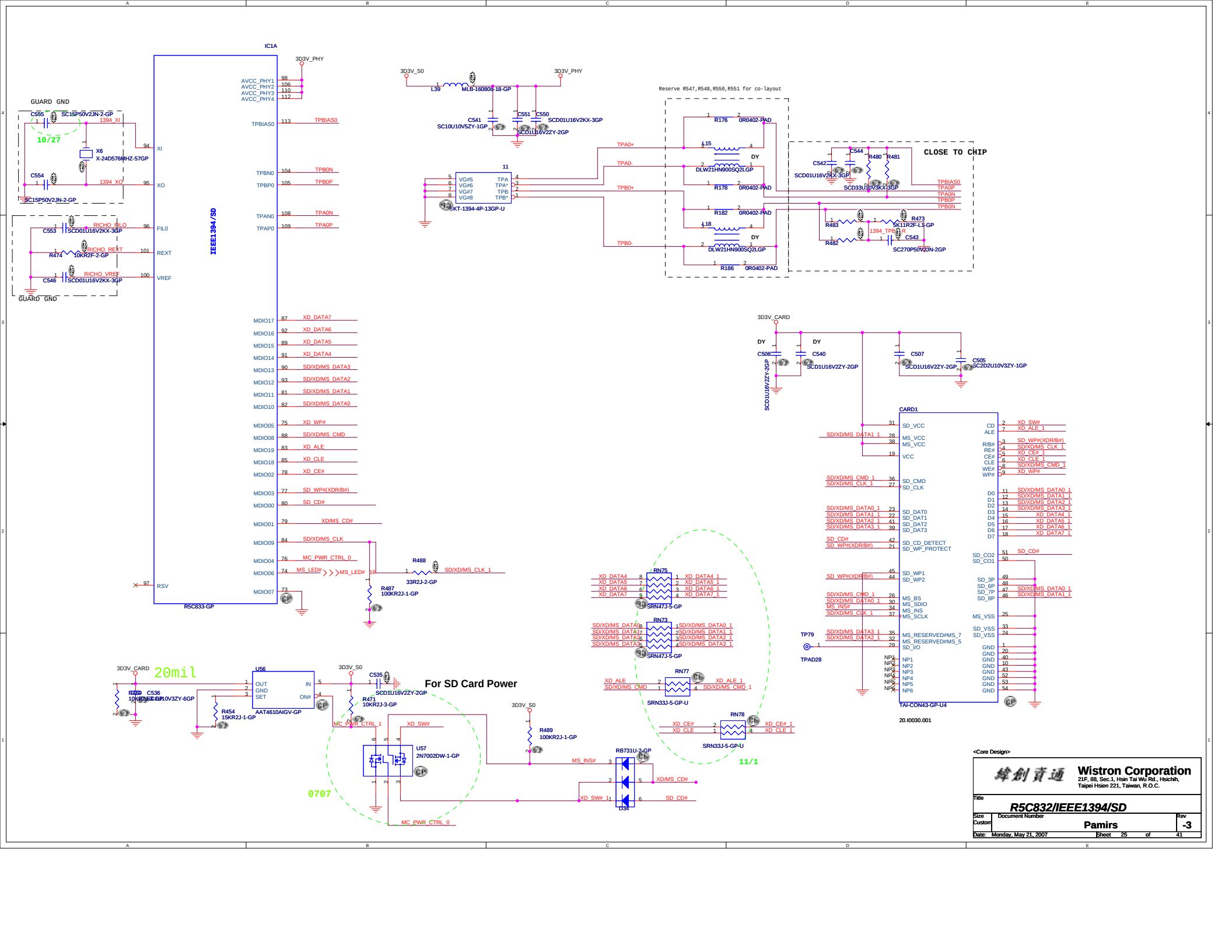
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

Size: A3 | Document Number: Pamirs | Rev: -3

Date: Friday, May 18, 2007 | Sheet 24 of 41



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

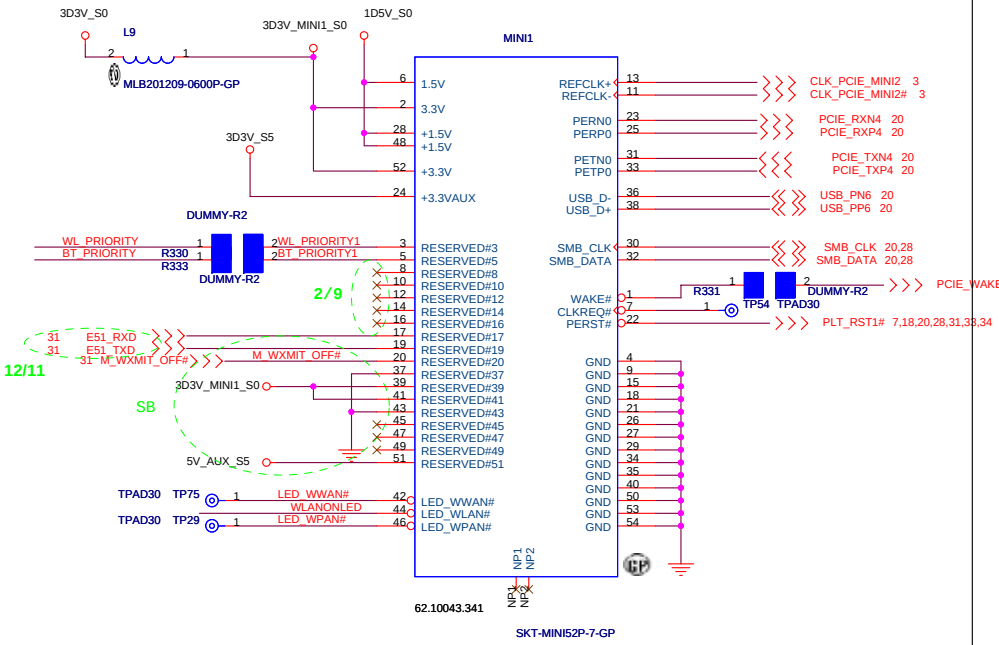
Title: R5C832/IEEE1394/SD

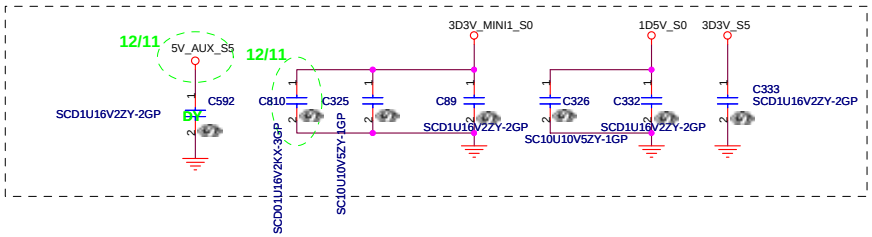
Size: Custom | Document Number: Pamirs | Rev: -3

Date: Monday, May 21, 2007 | Sheet 25 of 41

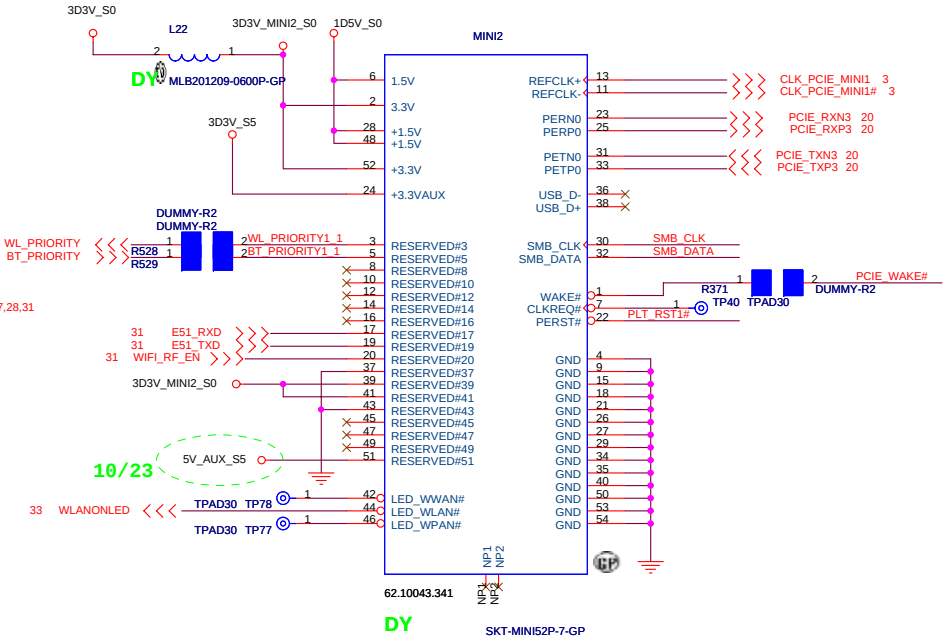
Mini Card Connector

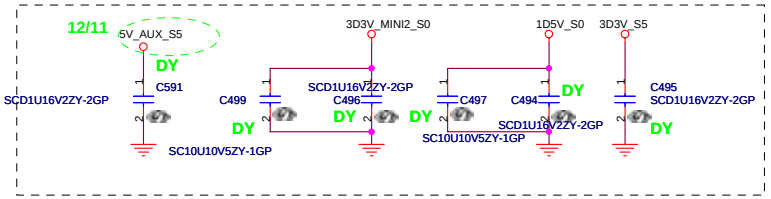
Mini Card Connector 1(WWAN)





Mini Card Connector 2(802.11a/b/g)





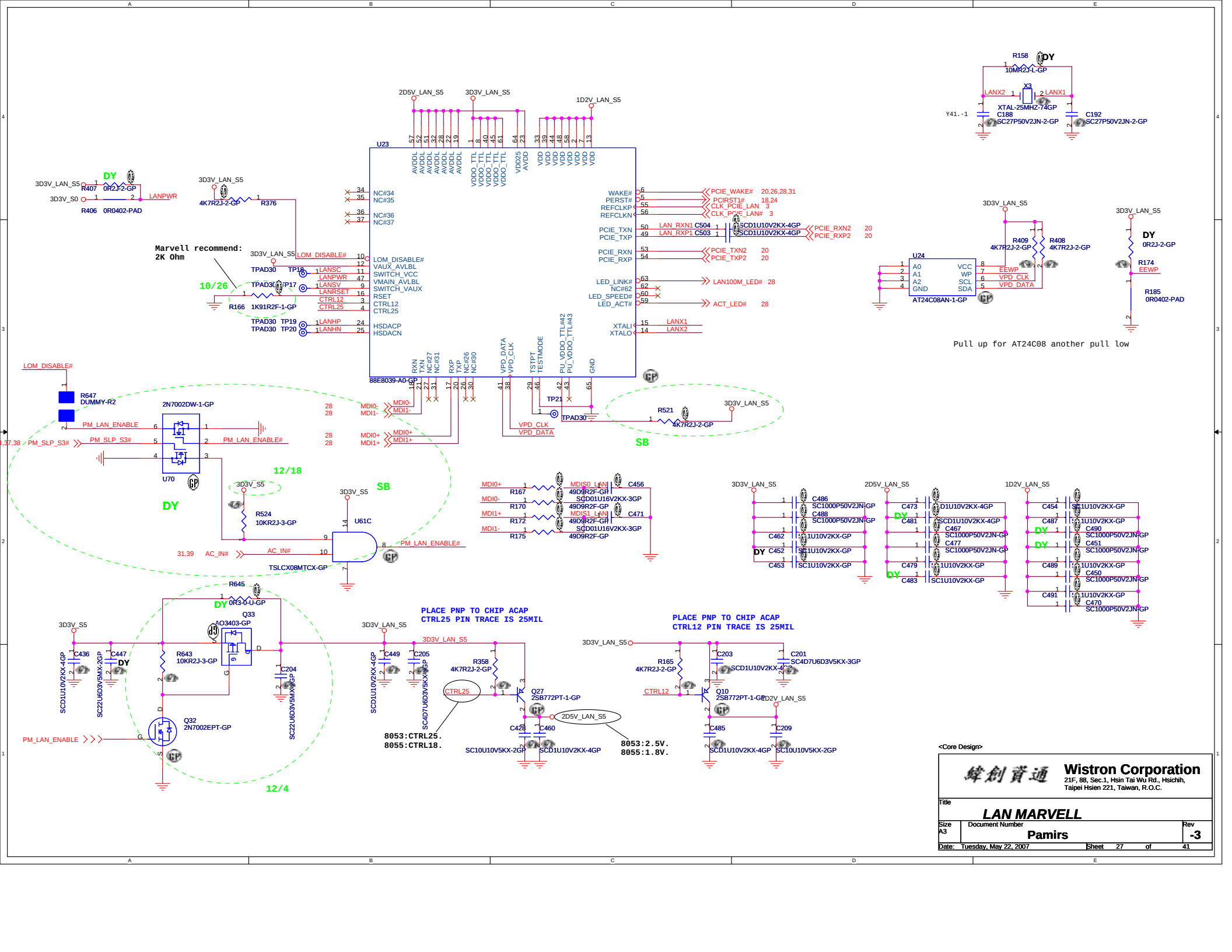
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size	Document Number	Rev
A3	Pamirs	-3

Date: Monday, May 21, 2007 Sheet 26 of 41



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN MARVELL**

Size	Document Number	Rev
A3	Pamirs	-3

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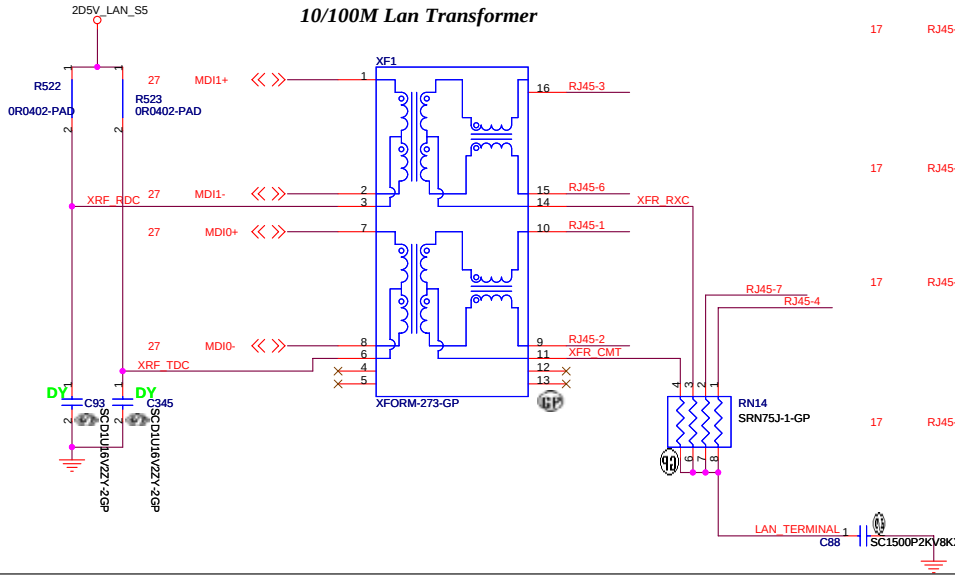
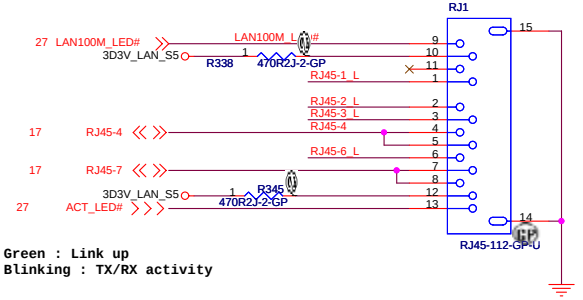


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

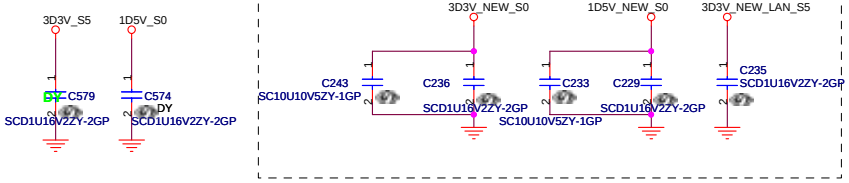


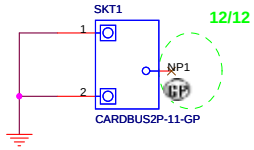
Green : Link up
Blinking : TX/RX activity

NEWCARD Connector

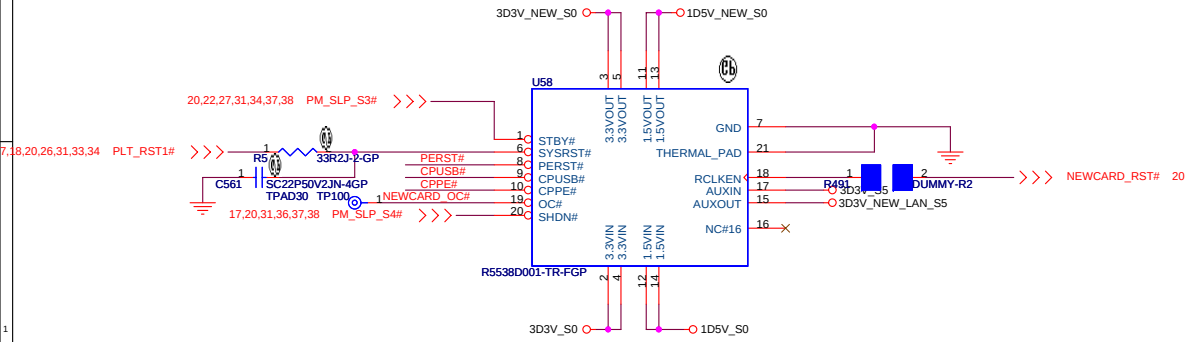
Place them Near to Chip

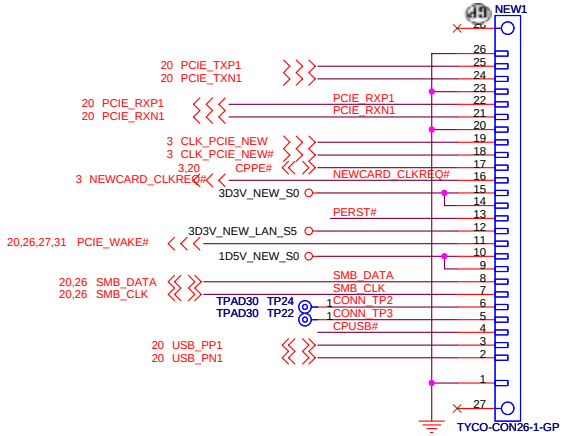
Place them Near to Connector

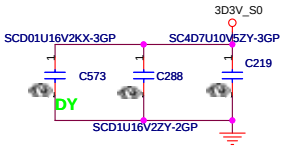




For Newcard socket







<Core Design>

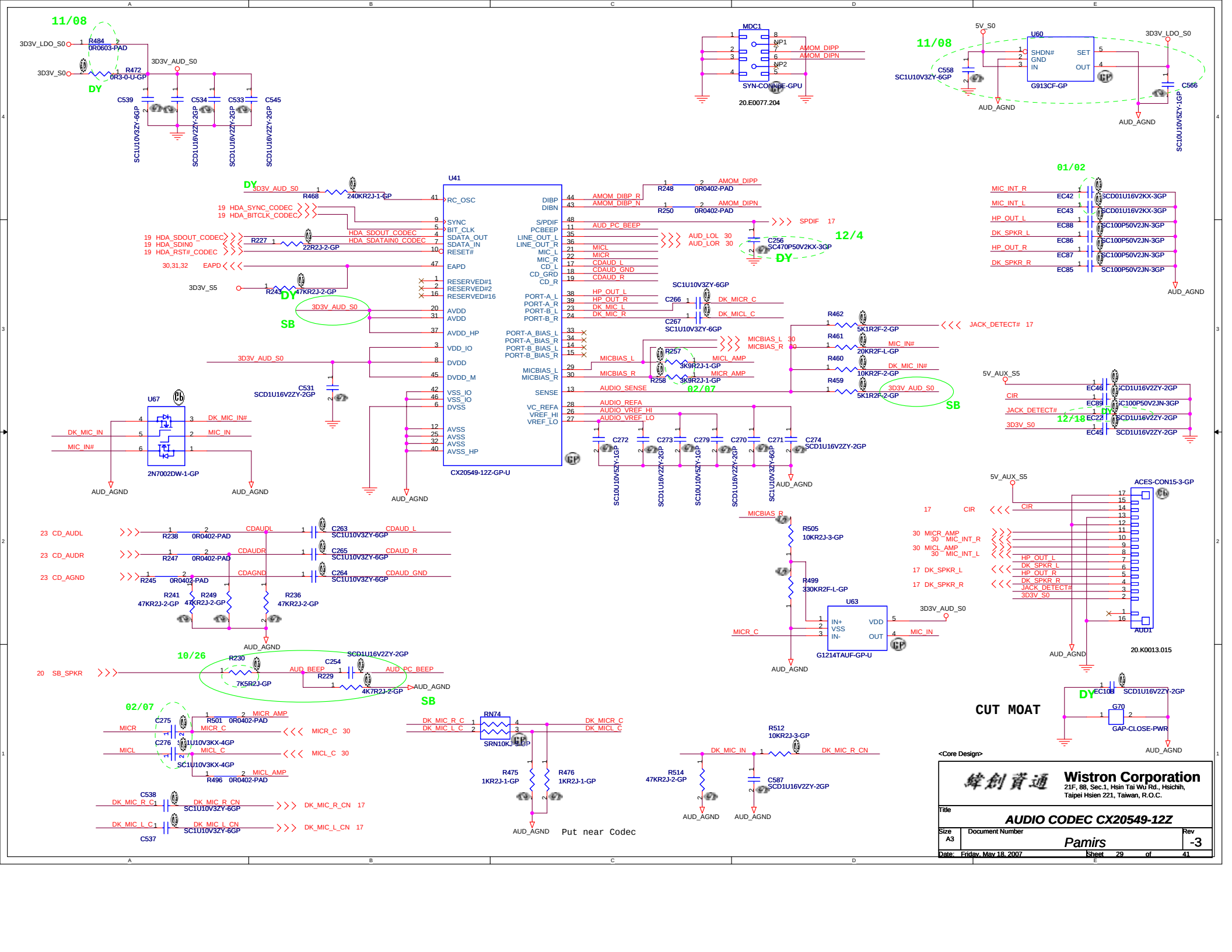
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

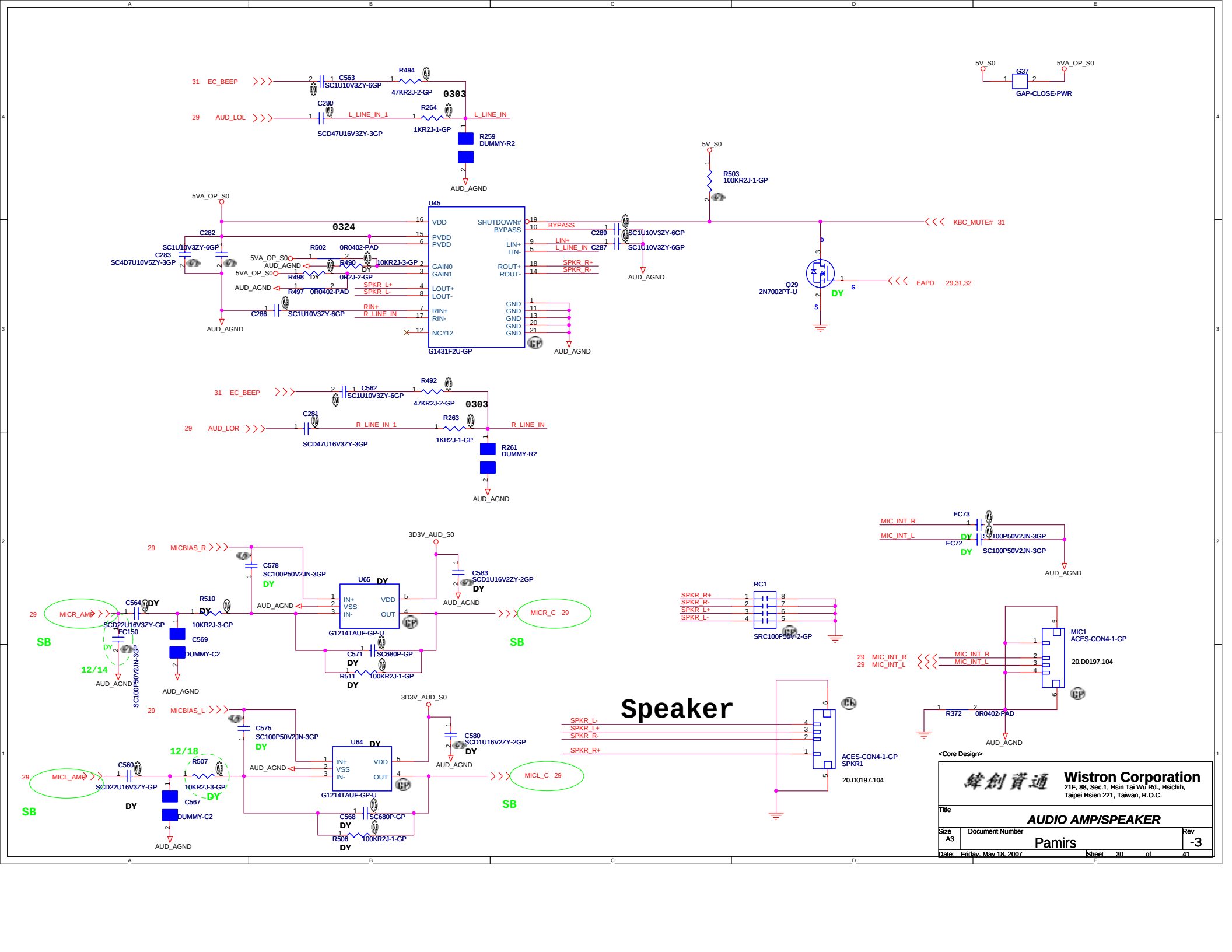
Title: LAN connector/NEW CARD/SIM

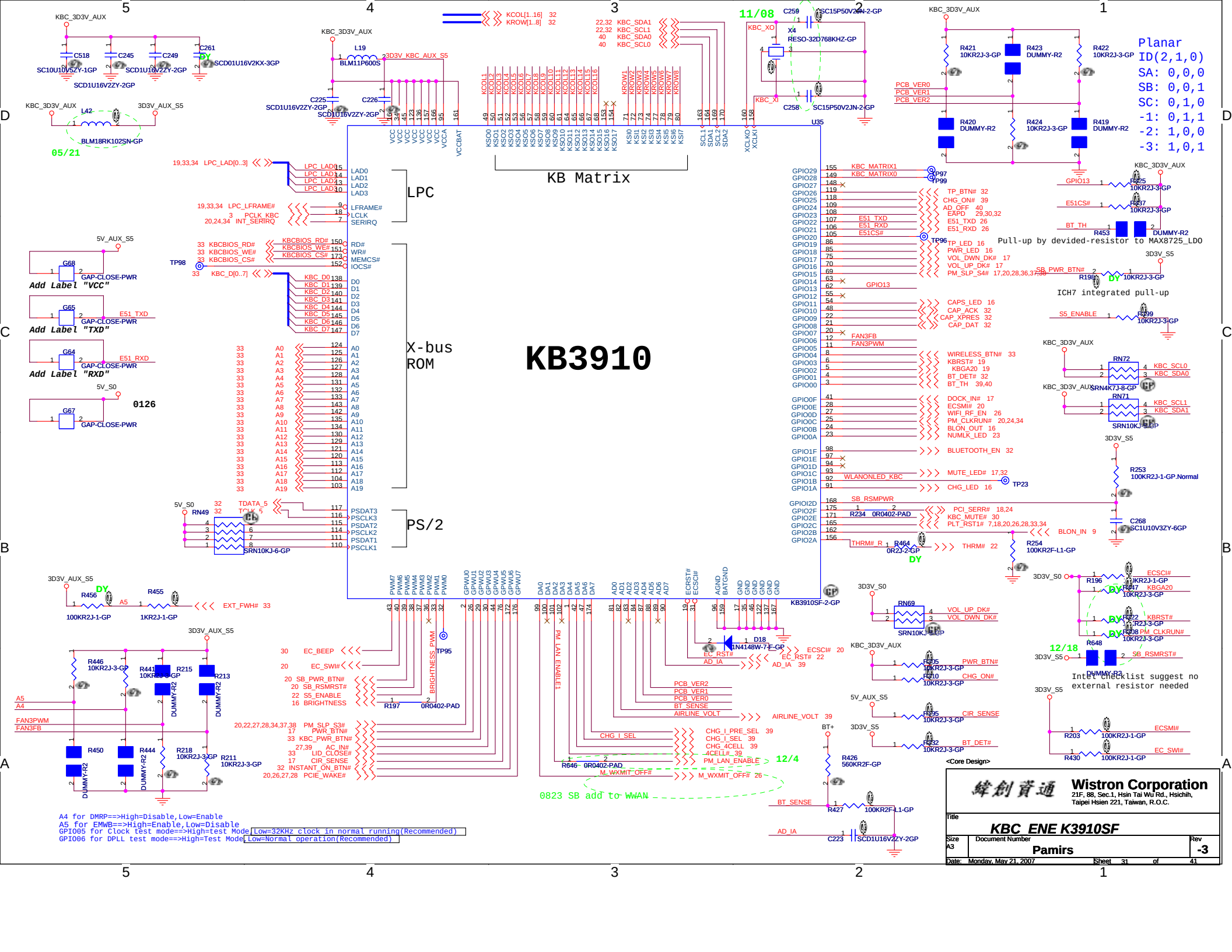
Size	Document Number	Rev
A3	Pamirs	-3

Date: Monday, May 21, 2007 Sheet 28 of 41

CLOSE TO TRANSFORMER


11/08
3D3V_LDO_S0
R484
0R0603-PAD
3D3V_S0
R472
0R3-0-U-GP
3D3V_AUD_S0
DY
C539
C534
C533
C545
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONNPE-GPU
20.E0077.204
11/08
5V_S0
U60
SHDN#
GND
IN
SET
OUT
G913CF-GP
3D3V_LDO_S0
C558
SC1U10V3ZY-6GP
C566
SC10U10V5ZY-1GP
AUD_AGND
AUD_AGND
01/02
MIC_INT_R
MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
EC42
EC43
EC88
EC86
EC87
EC85
SCD01U16V2KX-3GP
SCD01U16V2KX-3GP
SC100P50V2JN-3GP
SC100P50V2JN-3GP
SC100P50V2JN-3GP
SC100P50V2JN-3GP
AUD_AGND
DY
3D3V_AUD_S0
R468
240KR2J-1-GP
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC
19 HDA_SDOUT_CODEC
19 HDA_SDIN0
19 HDA_RST#_CODEC
R227
22R2J-2-GP
HDA_SDOUT_CODEC
HDA_SDATAIN0_CODEC
30,31,32 EAPD
3D3V_S5
R243
47KR2J-2-GP
DY
SB
3D3V_AUD_S0
U41
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
CX20549-12Z-GP-U
AMOM_DIBP_R
AMOM_DIBN_N
R248
0R0402-PAD
AMOM_DIPP
R250
0R0402-PAD
AMOM_DIPN
AUD_PC_BEEP
SPDIF 17
AUD_LOL 30
AUD_LOR 30
C256
SC470P50V2KX-3GP
12/4
DY
MICL
MICR
CDAUD_L
CDAUD_GND
CDAUD_R
HP_OUT_L
HP_OUT_R
DK_MIC_L
DK_MIC_R
SC1U10V3ZY-6GP
C266
DK_MICR_C
C267
SC1U10V3ZY-6GP
DK_MICL_C
R462
5K1R2F-2-GP
JACK_DETECT# 17
R461
20KR2F-L-GP
MIC_IN#
R460
10KR2F-2-GP
DK_MIC_IN#
R459
5K1R2F-2-GP
3D3V_AUD_S0
SB
MICBIAS_L 30
MICBIAS_R 30
R257
3K9R2J-1-GP
MICL_AMP
R258
3K9R2J-1-GP
MICR_AMP
02/07
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C272
C273
C279
C270
C271
C274
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SC1U10V3ZY-6GP
AUD_AGND
5V_AUX_S5
EC46
CIR
EC89
JACK_DETECT#
12/18
EC22
DY
3D3V_S0
EC45
SCD1U16V2ZY-2GP
SC100P50V2JN-3GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
C531
SCD1U16V2ZY-2GP
U67
DK_MIC_IN#
DK_MIC_IN
MIC_IN
MIC_IN#
2N7002DW-1-GP
AUD_AGND
AUD_AGND
AUD_AGND
23 CD_AUDL
23 CD_AUDR
23 CD_AGND
R238
0R0402-PAD
R247
0R0402-PAD
R245
0R0402-PAD
CDAUDL
CDAUDR
CDAGND
C263
SC1U10V3ZY-6GP
CDAUD_L
C265
SC1U10V3ZY-6GP
CDAUD_R
C264
SC1U10V3ZY-6GP
CDAUD_GND
R241
47KR2J-2-GP
R249
47KR2J-2-GP
R236
47KR2J-2-GP
AUD_AGND
MICBIAS_R
R505
10KR2J-3-GP
R499
330KR2F-L-GP
U63
IN+
VSS
IN-
VDD
OUT
MIC_IN
G1214TAUF-GP-U
MICR_C
3D3V_AUD_S0
AUD_AGND
5V_AUX_S5
ACES-CON15-3-GP
17 CIR
30 MICR_AMP
30 MICL_AMP
17 DK_SPKR_L
17 DK_SPKR_R
30 MIC_INT_R
30 MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
JACK_DETECT#
3D3V_S0
AUD1
AUD_AGND
20.K0013.015
10/26
20 SB_SPKR
R230
7K5R2J-GP
C254
SCD1U16V2ZY-2GP
AUD_BEEP
R229
4K7R2J-2-GP
AUD_PC_BEEP
AUD_AGND
SB
02/07
MICR
MICL
C275
C276
SC1U10V3KX-4GP
SC1U10V3KX-4GP
R501
0R0402-PAD
MICR_AMP
MICR_C
MICL_C
R496
0R0402-PAD
MICL_AMP
MICR_C 30
MICL_C 30
C538
C537
DK_MIC_R_C
DK_MIC_L_C
SC1U10V3ZY-6GP
SC1U10V3ZY-6GP
DK_MIC_R_CN
DK_MIC_L_CN
DK_MIC_R_CN 17
DK_MIC_L_CN 17
DK_MIC_R_C
DK_MIC_L_C
RN74
SRN10KJ-6GP
DK_MICR_C
DK_MICL_C
R475
1KR2J-1-GP
R476
1KR2J-1-GP
AUD_AGND
Put near Codec
R512
10KR2J-3-GP
DK_MIC_IN
DK_MIC_R_CN
R514
47KR2J-2-GP
C587
SCD1U16V2ZY-2GP
AUD_AGND
AUD_AGND
CUT MOAT
DY
EC108
SCD1U16V2ZY-2GP
G70
GAP-CLOSE-PWR
AUD_AGND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 29 of 41


31 EC_BEEP
C563
SC1U10V3ZY-6GP
R494
47KR2J-2-GP
0303
29 AUD_LOL
C290
L_LINE_IN_1
R264
1KR2J-1-GP
L_LINE_IN
R259
DUMMY-R2
AUD_AGND
5V_S0
G37
5VA_OP_S0
GAP-CLOSE-PWR
R503
100KR2J-1-GP
5VA_OP_S0
U45
0324
VDD
PVDD
PVDD
GAIN0
GAIN1
LOUT+
LOUT-
RIN+
RIN-
NC#12
SHUTDOWN#
BYPASS
LIN+
LIN-
ROUT+
ROUT-
GND
G1431F2U-GP
C282
SC1U10V3ZY-6GP
C283
SC4D7U10V5ZY-3GP
R502
0R0402-PAD
R490
10KR2J-3-GP
R498
0R2J-2-GP
R497
0R0402-PAD
C286
SC1U10V3ZY-6GP
SPKR_L+
SPKR_L-
RIN+
R_LINE_IN
C289
C287
SC1U10V3ZY-6GP
SPKR_R+
SPKR_R-
KBC_MUTE# 31
Q29
2N7002PT-U
EAPD 29,31,32
DY
31 EC_BEEP
C562
SC1U10V3ZY-6GP
R492
47KR2J-2-GP
0303
29 AUD_LOR
C281
R_LINE_IN_1
R263
1KR2J-1-GP
R_LINE_IN
R261
DUMMY-R2
AUD_AGND
3D3V_AUD_S0
29 MICBIAS_R
C578
SC100P50V2JN-3GP
U65
G1214TAUF-GP-U
IN+
VSS
IN-
VDD
OUT
C583
SCD1U16V2ZY-2GP
29 MICR_AMP
C564
SCD22U16V3ZY-GP
R510
10KR2J-3-GP
C569
DUMMY-C2
EC150
SC100P50V2JN-3GP
12/14
C571
SC680P-GP
R511
100KR2J-1-GP
MICR_C 29
SB
29 MICBIAS_L
C575
SC100P50V2JN-3GP
U64
G1214TAUF-GP-U
C580
SCD1U16V2ZY-2GP
29 MICL_AMP
C560
SCD22U16V3ZY-GP
R507
10KR2J-3-GP
C567
DUMMY-C2
12/18
C568
SC680P-GP
R506
100KR2J-1-GP
MICL_C 29
SB
DY
AUD_AGND
EC73
EC72
SC100P50V2JN-3GP
MIC_INT_R
MIC_INT_L
RC1
SRC100P50V-2-GP
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
MIC1
ACES-CON4-1-GP
20.D0197.104
R372
0R0402-PAD
Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
SPKR1
ACES-CON4-1-GP
20.D0197.104
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/SPEAKER
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 30 of 41


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U35
KB3910SF-2-GP
Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1
-2: 1,0,0
-3: 1,0,1
11/08
05/21
0126
12/4
12/18
0823 SB add to WWAN
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=Test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs
-3
Monday, May 21, 2007
31
41

CAMERA

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

KB1
ACES-CON24-2-GP
20.K0220.024

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

TPAD1
FOX-CON4-12-GP

Blue thumb

BT1
ACES-CON8-4-GP
20.F0772.008

11/09
(3.93V)
12/4

CAM1
20.D0197.105

Close to CN8

0717Change from S5

MAX 150mA

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
20.K0228.012

3/20
2/12

TOUCH-PAD SWITCH

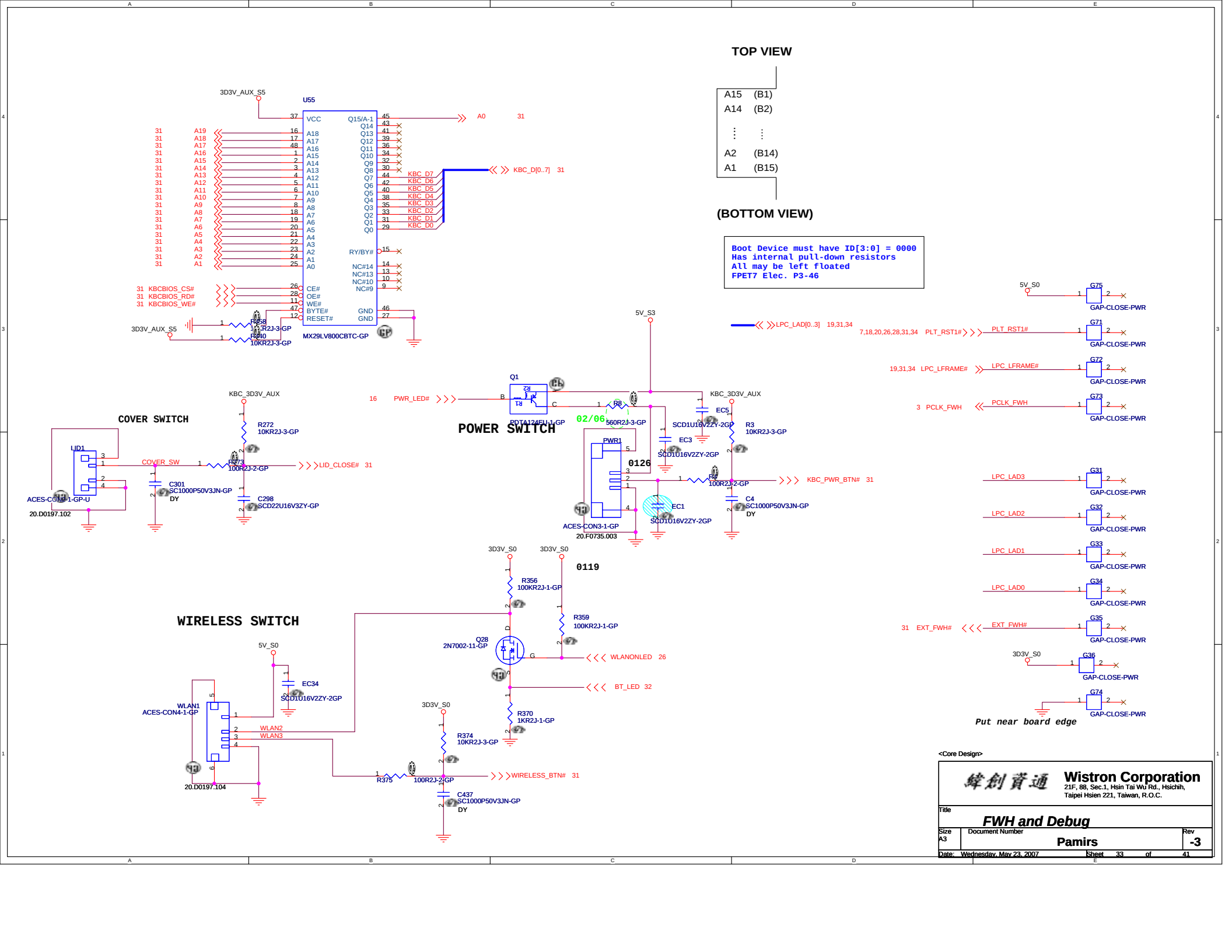
SW1
SW-TACT-68-GP-U
62.40009.451

RC6 SRC100P50V-2-GP
RC2 SRC100P50V-2-GP
RC5 SRC100P50V-2-GP
RC7 SRC100P50V-2-GP
RC3 SRC100P50V-2-GP
RC4 SRC100P50V-2-GP
for EMI

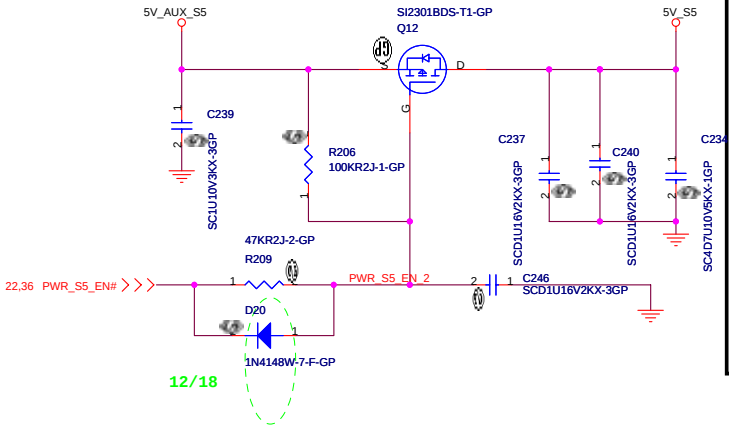
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

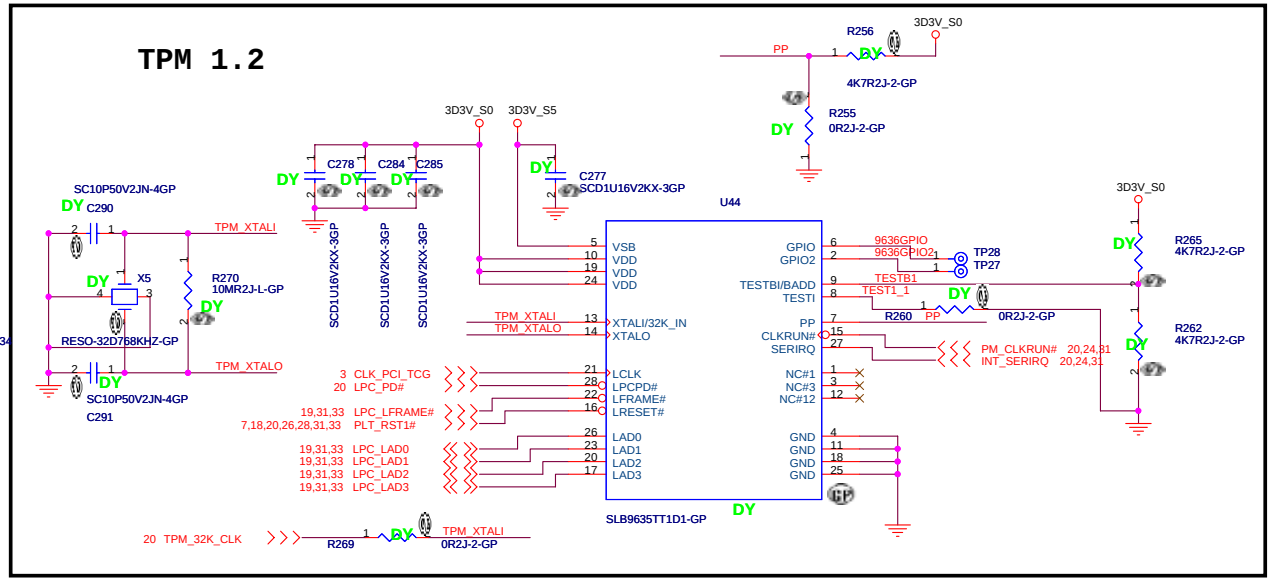
Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs
Rev: -3
Date: Monday, May 21, 2007
Sheet 32 of 41


TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
U55
MX29LV800CBTC-GP
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
02/06
0126
0119
Put near board edge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
FWH and Debug
Pamirs
-3
Wednesday, May 23, 2007
33 of 41

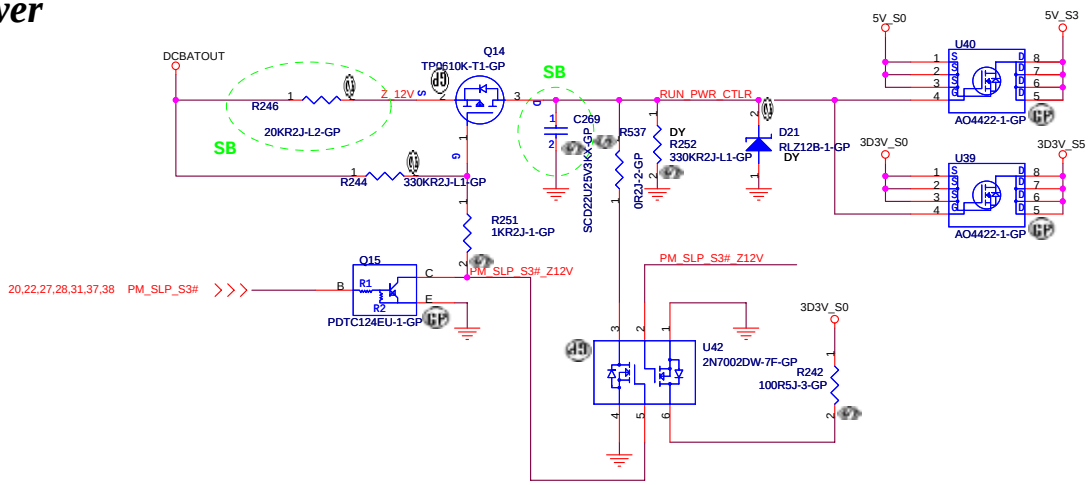
5V_AUX_S5 TO 5V_S5



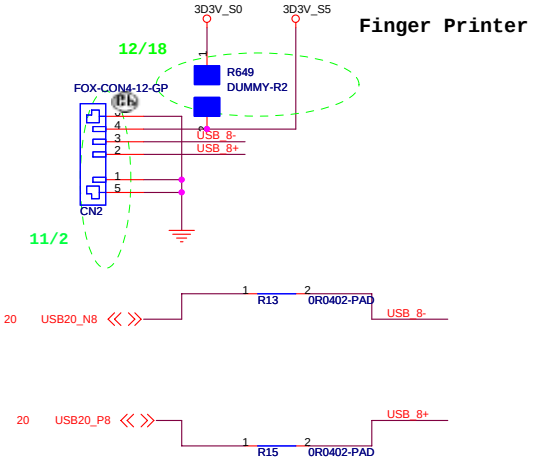
TPM 1.2



Run Power



Finger Printer



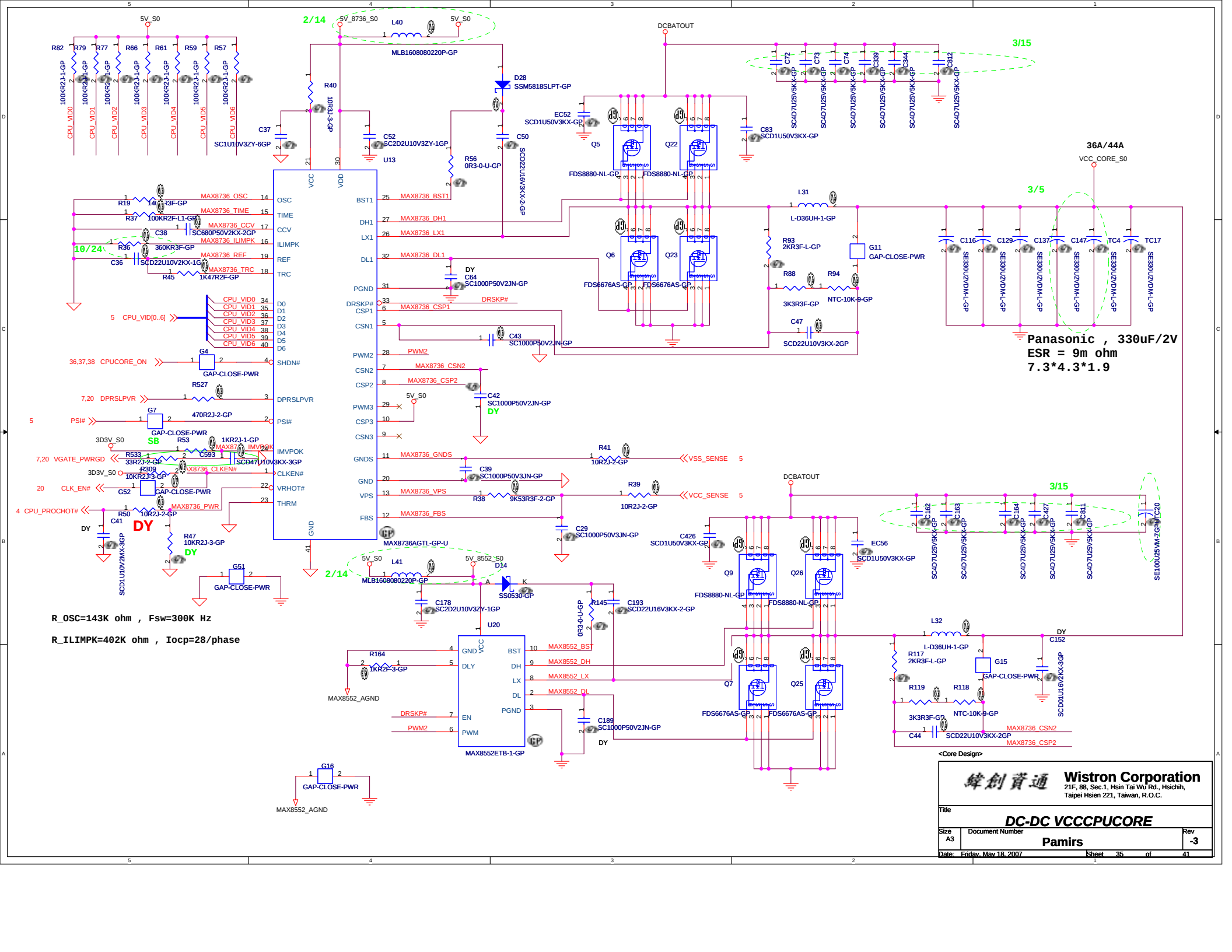
<Core Design>

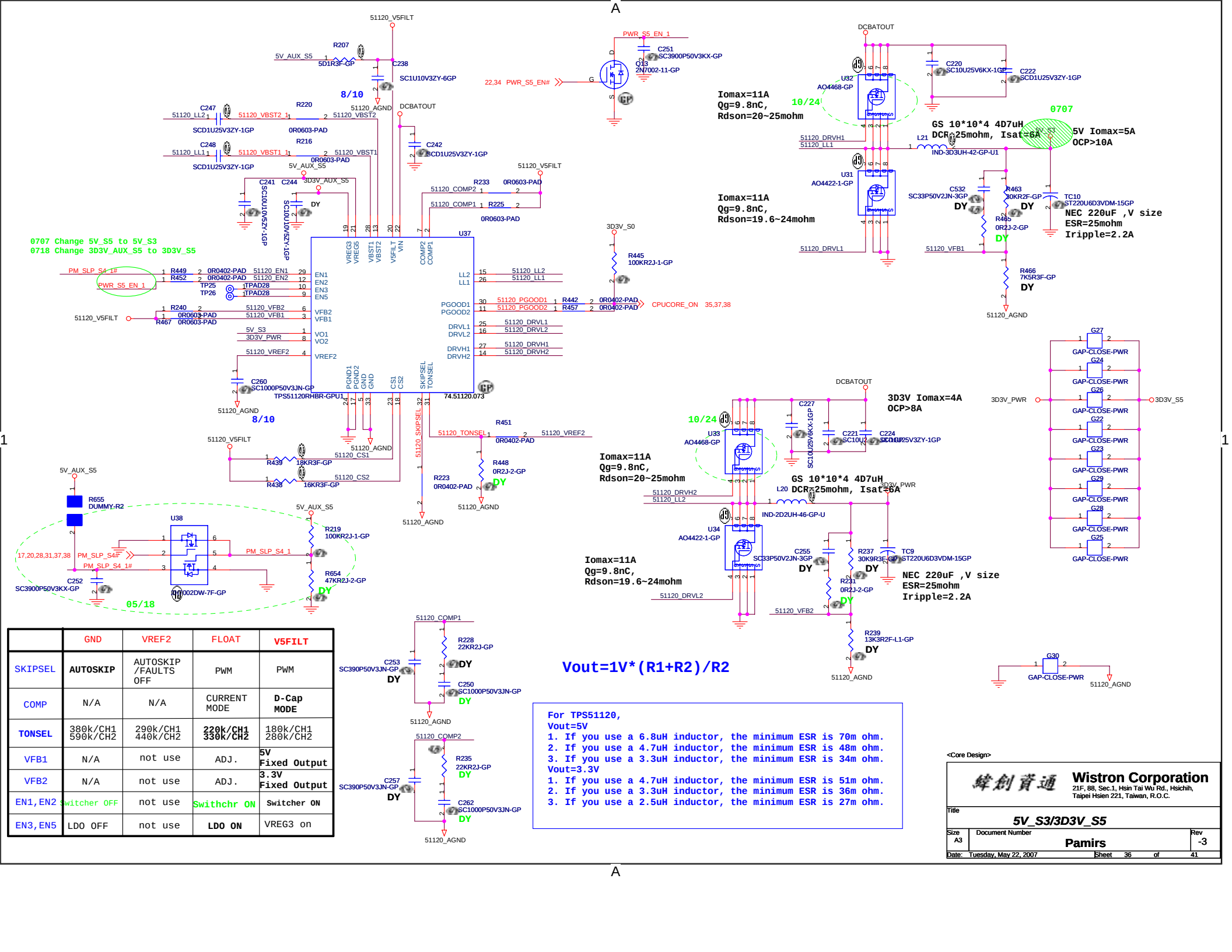
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size	Document Number	Rev
A3	Pamirs	-3

Date: Monday, May 21, 2007 Sheet 34 of 41


5V_S0
2/14
5V_8736_S0
L40
MLB1608080220P-GP
DCBATOUT
3/15
D28
SSM5818SLPT-GP
R82 R79 R77 R66 R61 R59 R57
100KR2J-1-GP
CPU_VID0 CPU_VID1 CPU_VID2 CPU_VID3 CPU_VID4 CPU_VID5 CPU_VID6
R40
10R3J-3-GP
C37
SC1U10V3ZY-6GP
C52
SC2D2U10V3ZY-1GP
U13
C50
SCD22U16V3KX-2-GP
R56
0R3-0-U-GP
EC52
SCD1U50V3KX-GP
Q5
Q22
FDS8880-NL-GP
C83
SCD1U50V3KX-GP
C72 C73 C74 C339 C344 C812
SC4D7U25V5KX-GP
36A/44A
VCC_CORE_S0
3/5
L31
L-D36UH-1-GP
R93
2KR3F-L-GP
G11
GAP-CLOSE-PWR
C116 C129 C137 C147 TC4 TC17
SE330U2V0M-L-GP
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R19
14K3R3F-GP
MAX8736_OSC
R37
100KR2F-L1-GP
MAX8736_TIME
C38
SC680P50V2KX-2GP
MAX8736_CCV
10/24
R36
360KR3F-GP
MAX8736_ILIMPK
C36
SCD22U10V2KX-1GP
MAX8736_REF
R45
1K47R2F-GP
MAX8736_TRC
OSC
TIME
CCV
ILIMPK
REF
TRC
VCC
VDD
BST1
DH1
LX1
DL1
PGND
DRSKP#
CSP1
CSN1
PWM2
CSN2
CSP2
PWM3
CSP3
CSN3
GNDS
GND
VPS
FBS
MAX8736_BST1
MAX8736_DH1
MAX8736_LX1
MAX8736_DL1
MAX8736_CSP1
MAX8736_CSN2
MAX8736_CSP2
MAX8736_GNDS
MAX8736_VPS
MAX8736_FBS
MAX8736AGTL-GP-U
Q6
Q23
FDS6676AS-GP
C64
SC1000P50V2JN-GP
DY
C43
SC1000P50V2JN-GP
C42
SC1000P50V2JN-GP
C39
SC1000P50V3JN-GP
C29
SC1000P50V3JN-GP
R38
9K53R3F-2-GP
R41
10R2J-2-GP
R39
10R2J-2-GP
VSS_SENSE
VCC_SENSE
R88
R94
3K3R3F-GP
NTC-10K-9-GP
C47
SCD22U10V3KX-2GP
CPU_VID[0..6]
CPU_VID0 CPU_VID1 CPU_VID2 CPU_VID3 CPU_VID4 CPU_VID5 CPU_VID6
D0 D1 D2 D3 D4 D5 D6
36,37,38 CPUCORE_ON
G4
GAP-CLOSE-PWR
SHDN#
R527
7,20 DPRSLPVR
DPRSLPVR
PSI#
G7
470R2J-2-GP
SB
3D3V_S0
R53
1KR2J-1-GP
MAX8736_IMVP0K
R533
33R2J-2-GP
SCD47U10V3KX-3GP
7,20 VGATE_PWRGD
R309
10KR2J-3-GP
MAX8736_CLKEN#
20 CLK_EN#
G52
GAP-CLOSE-PWR
IMVPOK
CLKEN#
VRHOT#
THRM
4 CPU_PROCHOT#
R50
10R2J-2-GP
MAX8736_PWR
C41
SCD1U10V2MX-3GP
R47
10KR2J-3-GP
G51
GAP-CLOSE-PWR
GND
5V_S0
L41
MLB1608080220P-GP
5V_8552_S0
D14
SS0530-GP
C178
SC2D2U10V3ZY-1GP
U20
R145
0R3-0-U-GP
C193
SCD22U16V3KX-2-GP
R164
1KR2F-3-GP
MAX8552_AGND
GND
VCC
DLY
BST
DH
LX
DL
PGND
EN
PWM
MAX8552_BST
MAX8552_DH
MAX8552_LX
MAX8552_DL
DRSKP#
PWM2
MAX8552ETB-1-GP
C189
SC1000P50V2JN-GP
Q9
Q26
Q7
Q25
FDS8880-NL-GP
FDS6676AS-GP
C426
SCD1U50V3KX-GP
EC56
SCD1U50V3KX-GP
C162 C163 C164 C427 C811
SC4D7U25V5KX-GP
SE100U25VM-7GPW-C20
L32
L-D36UH-1-GP
R117
2KR3F-L-GP
G15
GAP-CLOSE-PWR
R119
R118
3K3R3F-GP
NTC-10K-9-GP
C44
SCD22U10V3KX-2GP
C152
SCD01U16V2KX-3GP
G16
GAP-CLOSE-PWR
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC-DC VCCCPUCORE
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 35 of 41



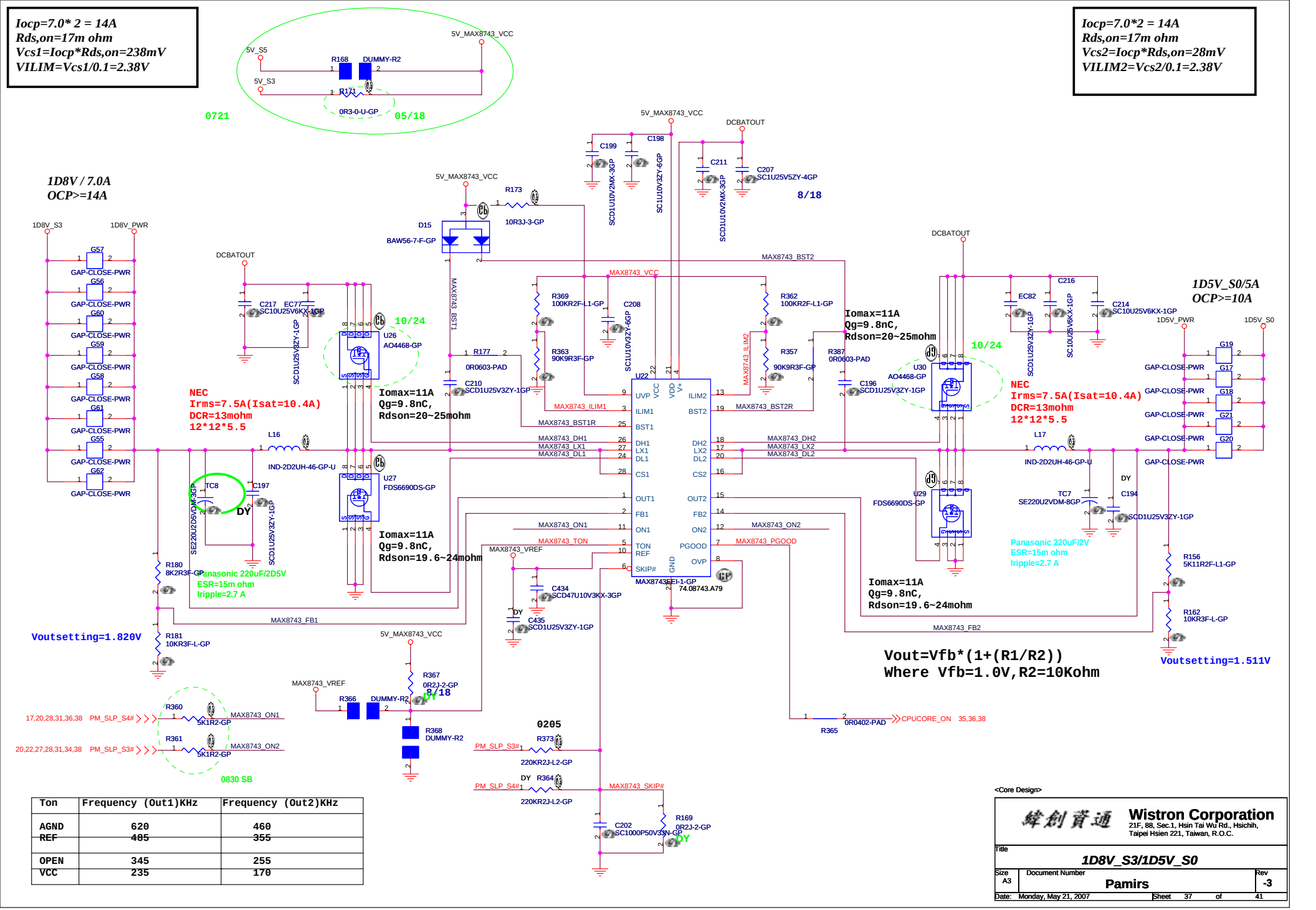
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V_S3/3D3V_S5**

Size: A3 | Document Number: **Pamirs** | Rev: -3

Date: Tuesday, May 22, 2007 | Sheet 36 of 41



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

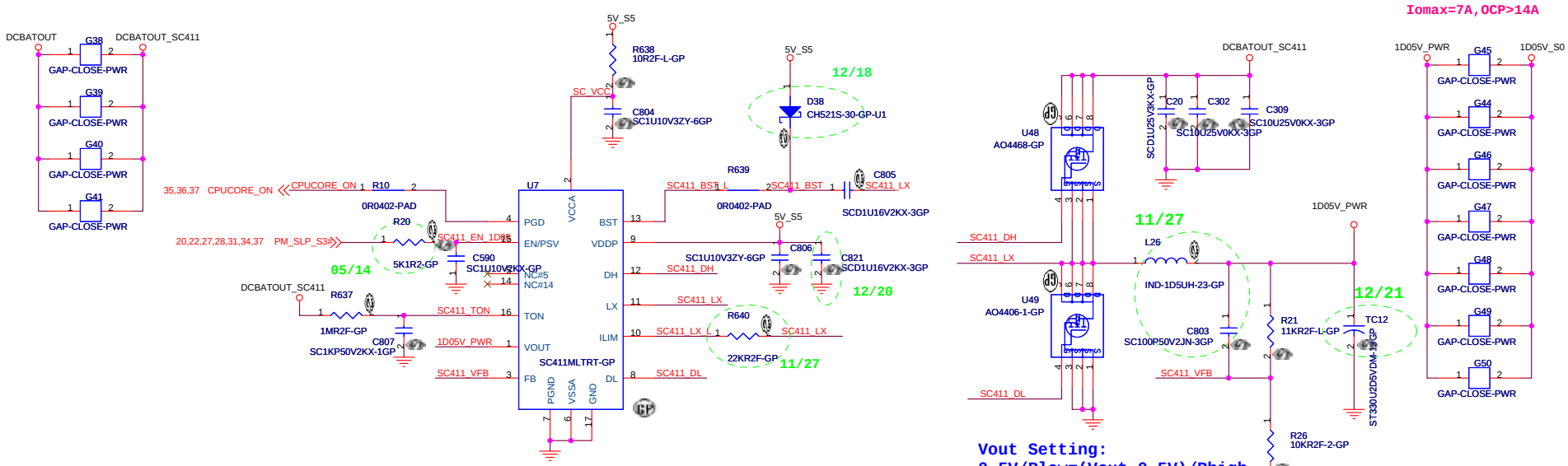
<Core Design>

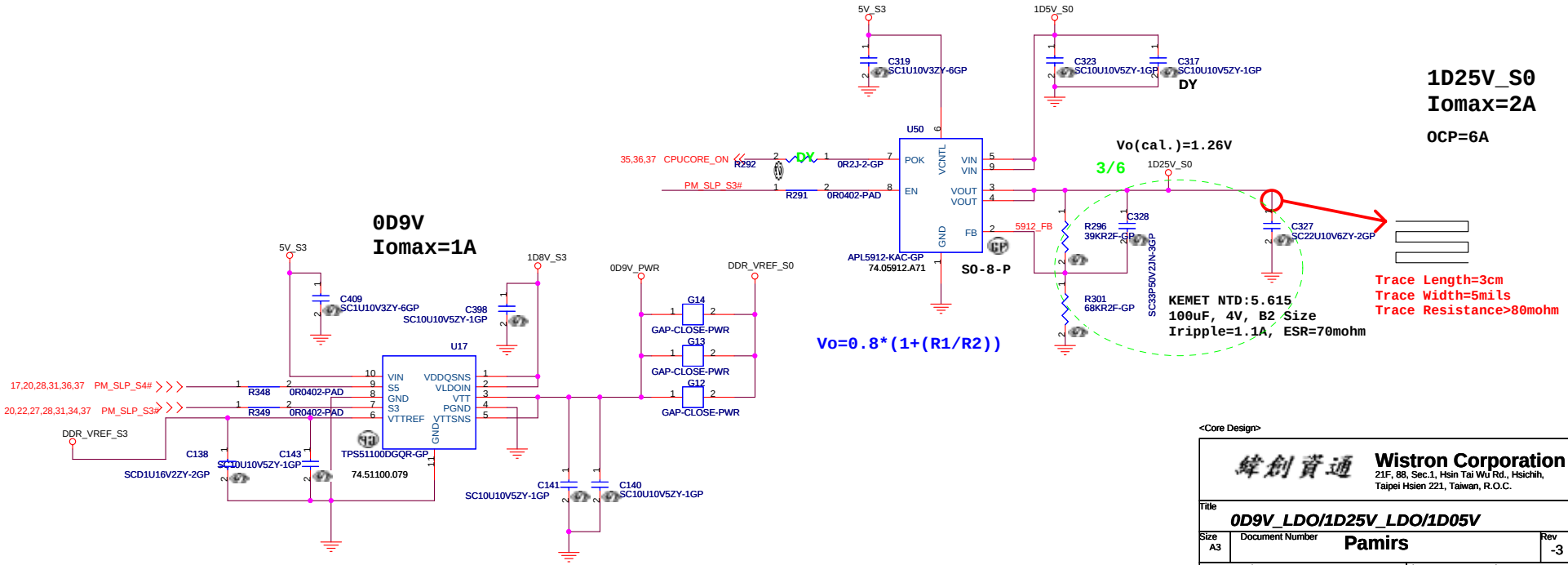
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S3/1D5V_S0

Size: A3 | Document Number: Pamirs | Rev: -3

Date: Monday, May 21, 2007 | Sheet 37 of 41





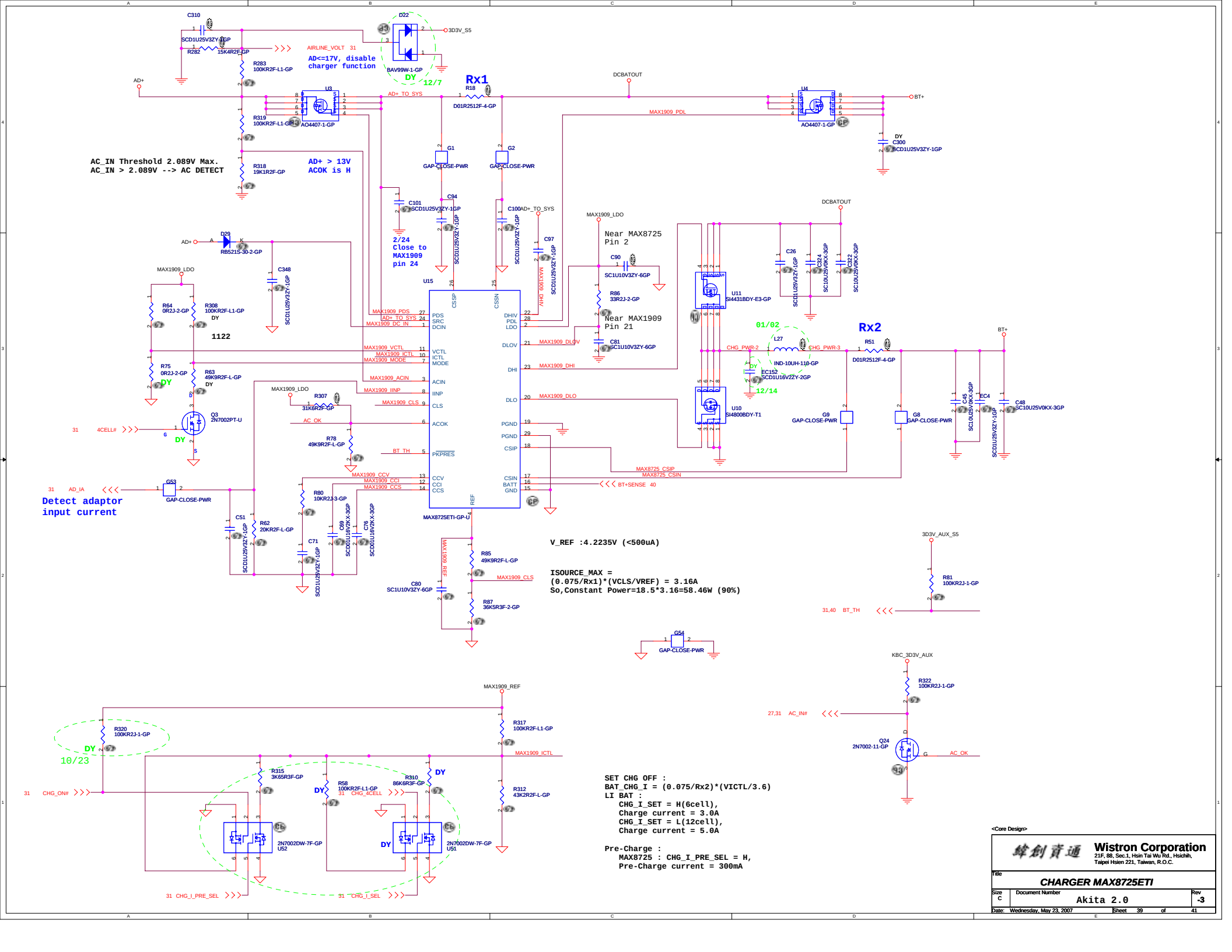
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D25V_LDO/1D05V

Size	Document Number	Rev
A3	Pamirs	-3

Date: Monday, May 21, 2007 Sheet 38 of 41


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable charger function
Rx1
Rx2
Near MAX8725 Pin 2
Near MAX1909 Pin 21
2/24 Close to MAX1909 pin 24
1122
01/02
12/14
12/7
10/23
Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
Wistron Corporation
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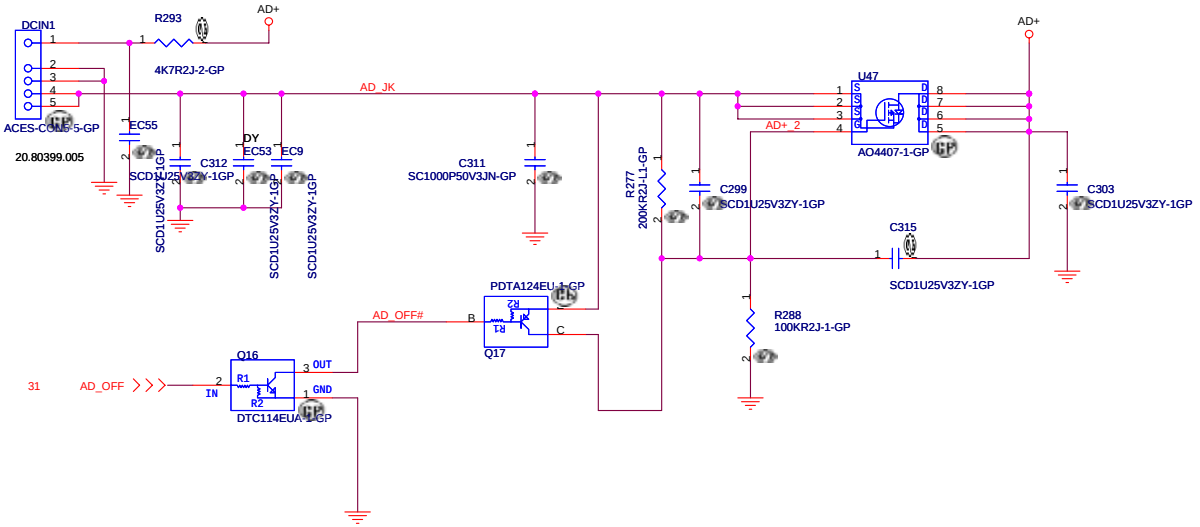
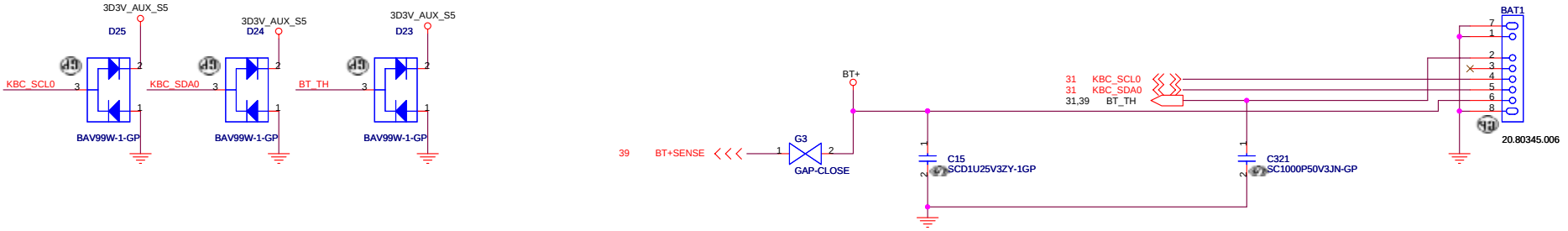
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Akita 2.0
Wednesday, May 23, 2007

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Title: AD/BATT CONN

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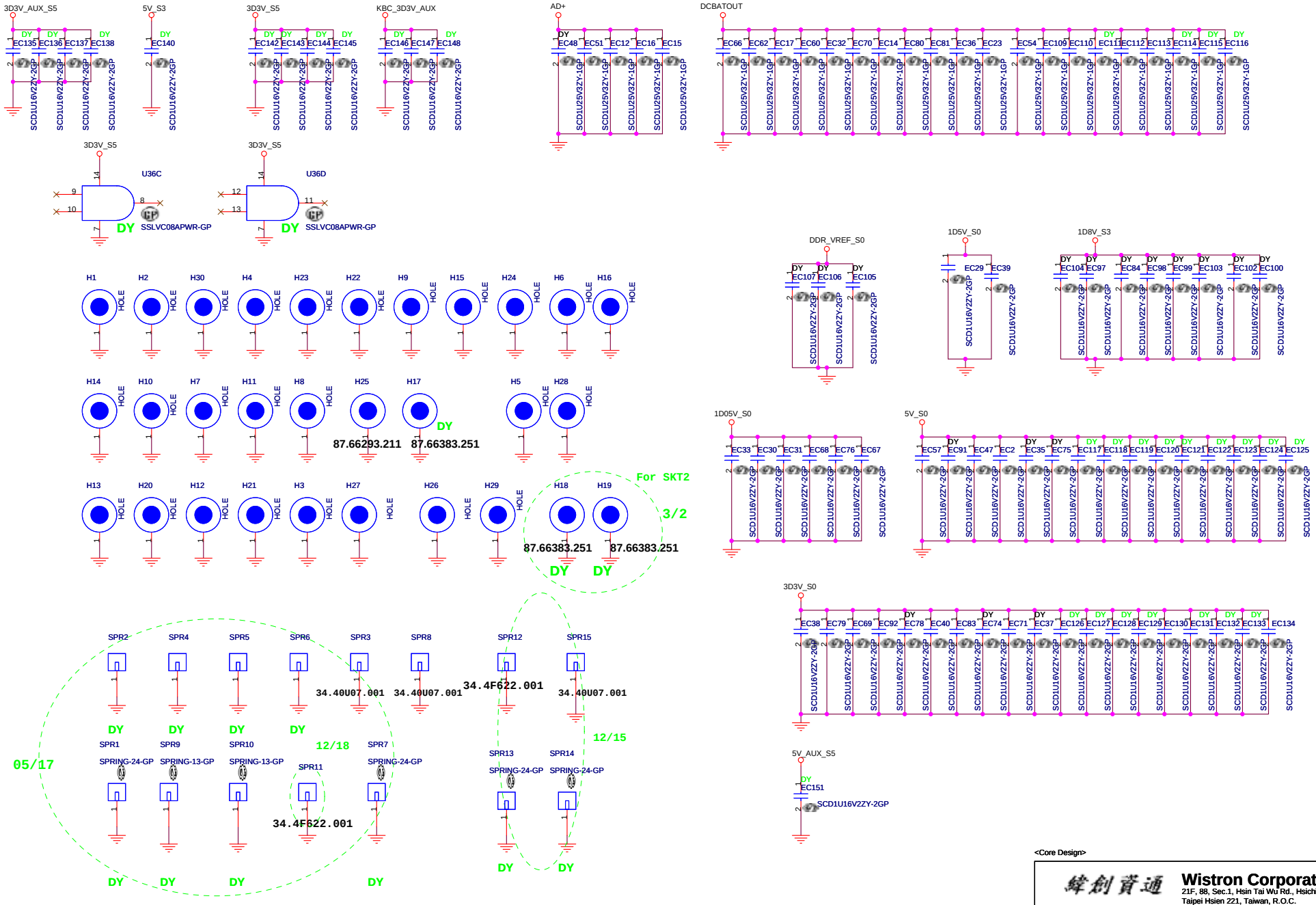

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Title: **MISC**

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