Compal confidential

Schematics Document
Mobile Merom uFCPGA with Satna Rosa Platform

2007-05-29
REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.		
Title	*Cover Sheet*	
Size: Custom	Document Number: *LA-3732P*	Rev: 1.0
Date: Monday, July 09, 2007	Sheet 1 of 42	

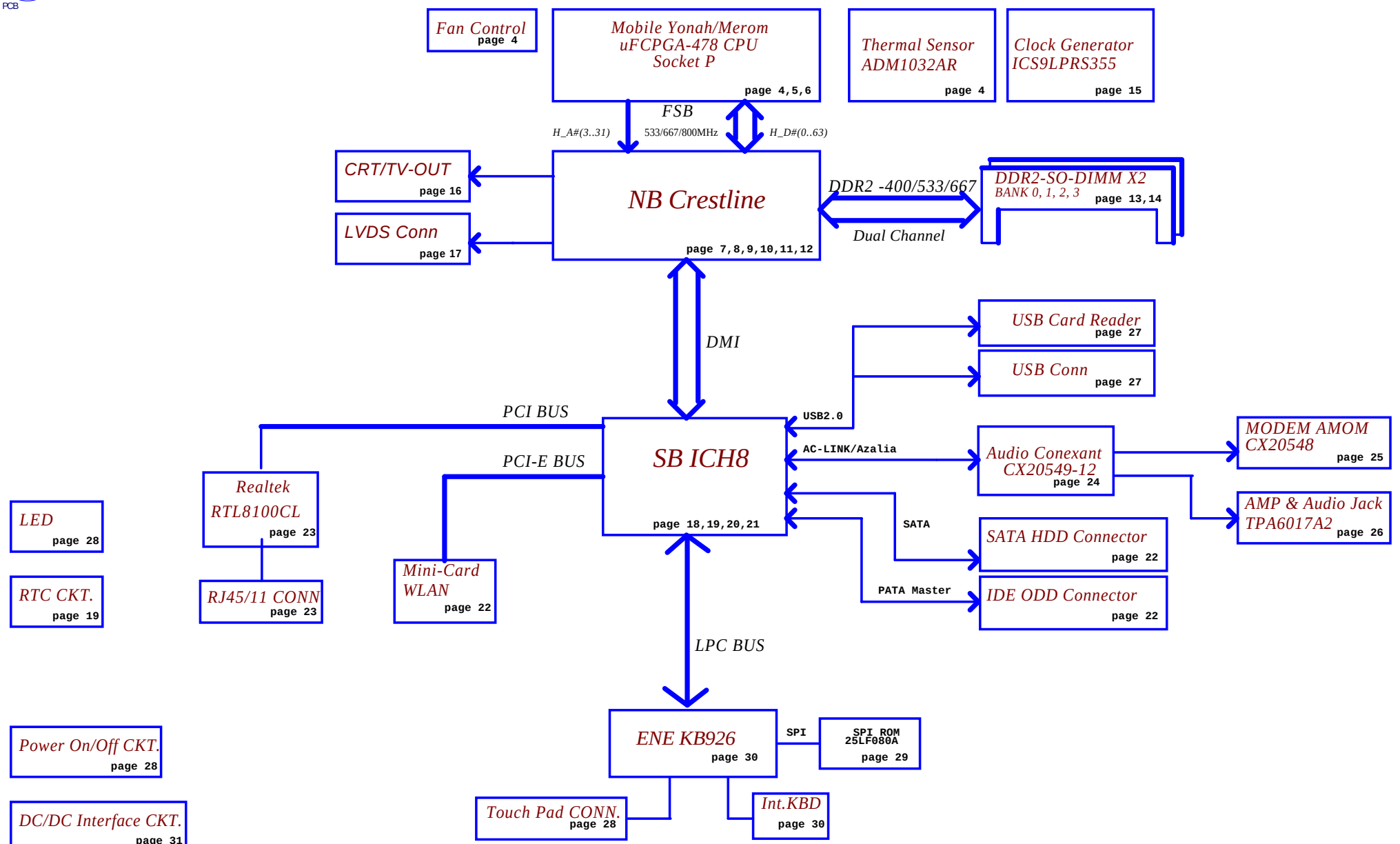
Compal confidential

File Name : LA-3732P

Spartan 1.0 (Merom +Crestline+ICH8)

ZZZ1

PCB



Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: Block Diagram

Size: Custom | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 2 of 42

Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

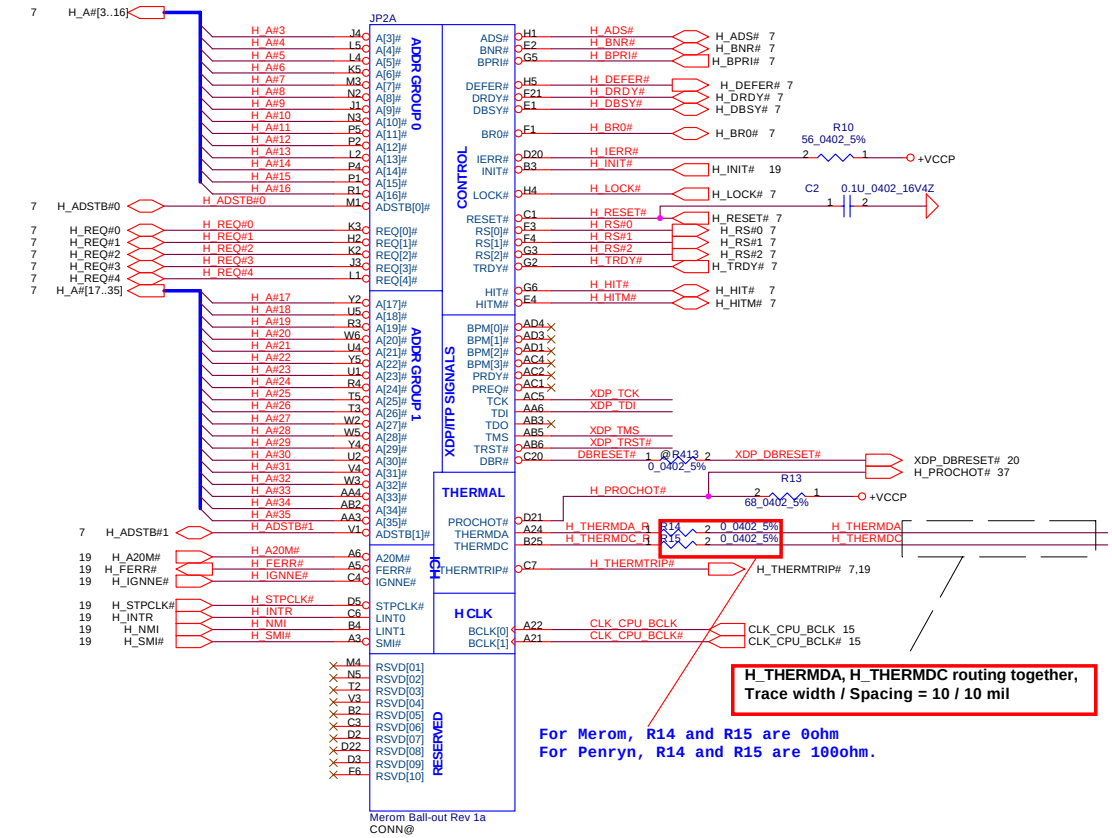
SOURCE \	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

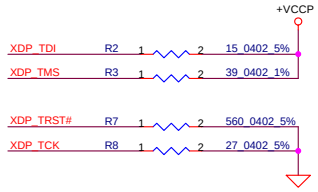
BOM: 43148632L01(965GM) & 43148632L02(960GML)

Jump-Short: PJP?

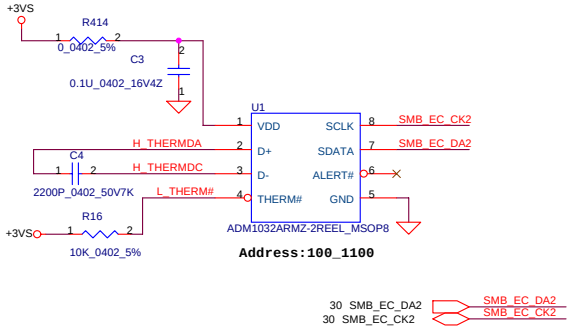
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: Notes List			
Size	Document Number: LA-3732P		Rev: 1.0
Date: Monday, July 09, 2007	Sheet 3 of 42		

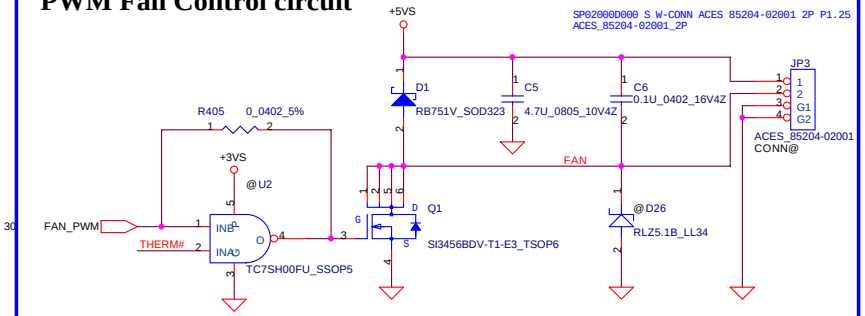




Thermal Sensor ADM1032ARMZ



PWM Fan Control circuit



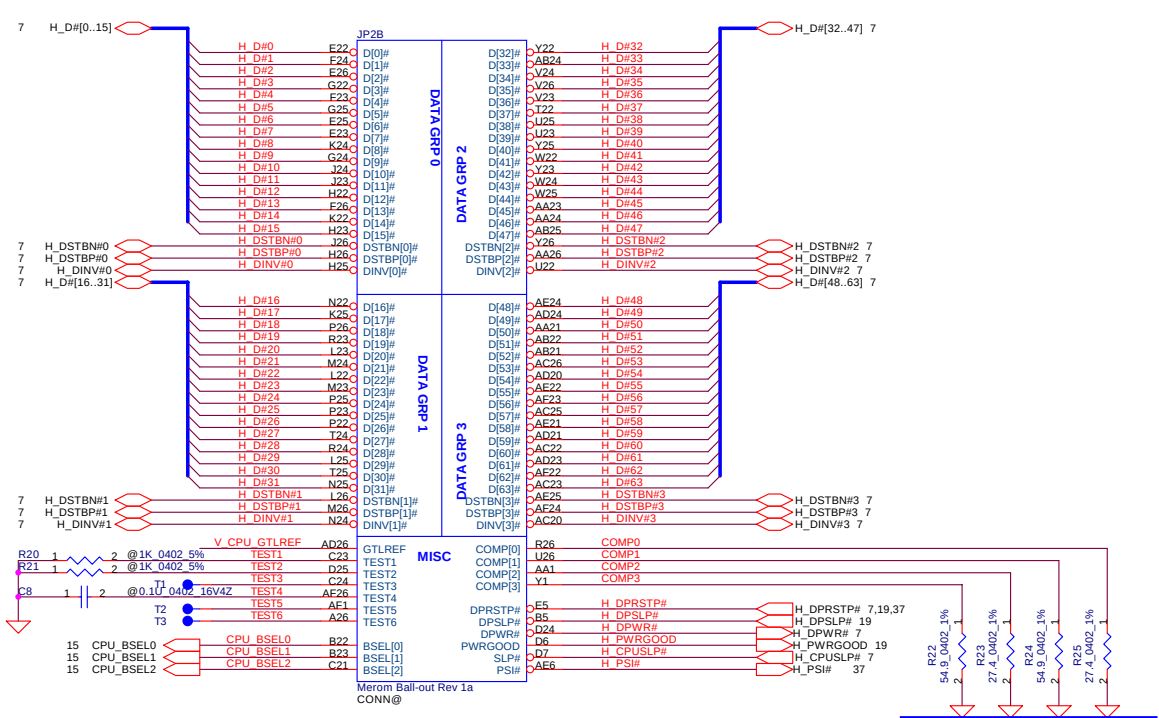
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Merom(1/3)-AGTL+/XDP

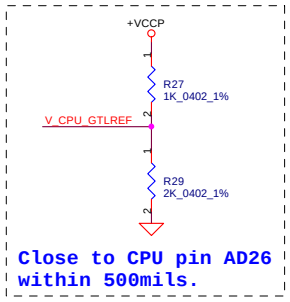
Size	Document Number	Rev
Custom	LA-3732P	1.0

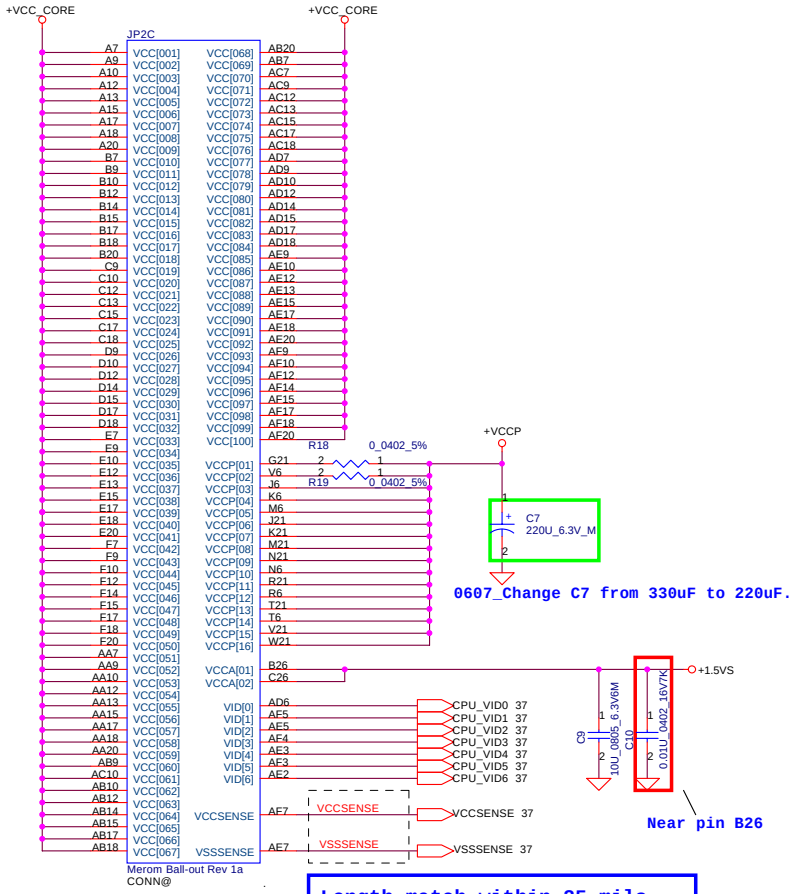
Date: Monday, July 09, 2007 Sheet 4 of 42

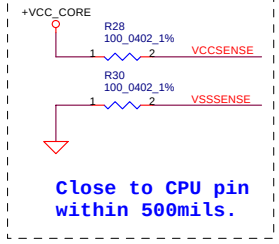


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0







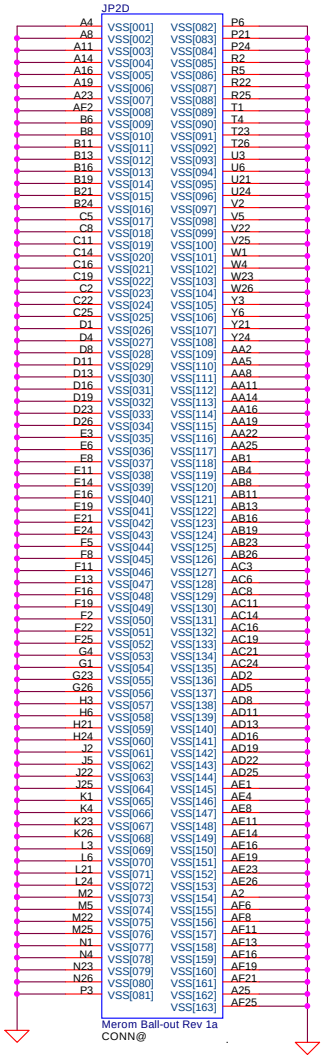
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

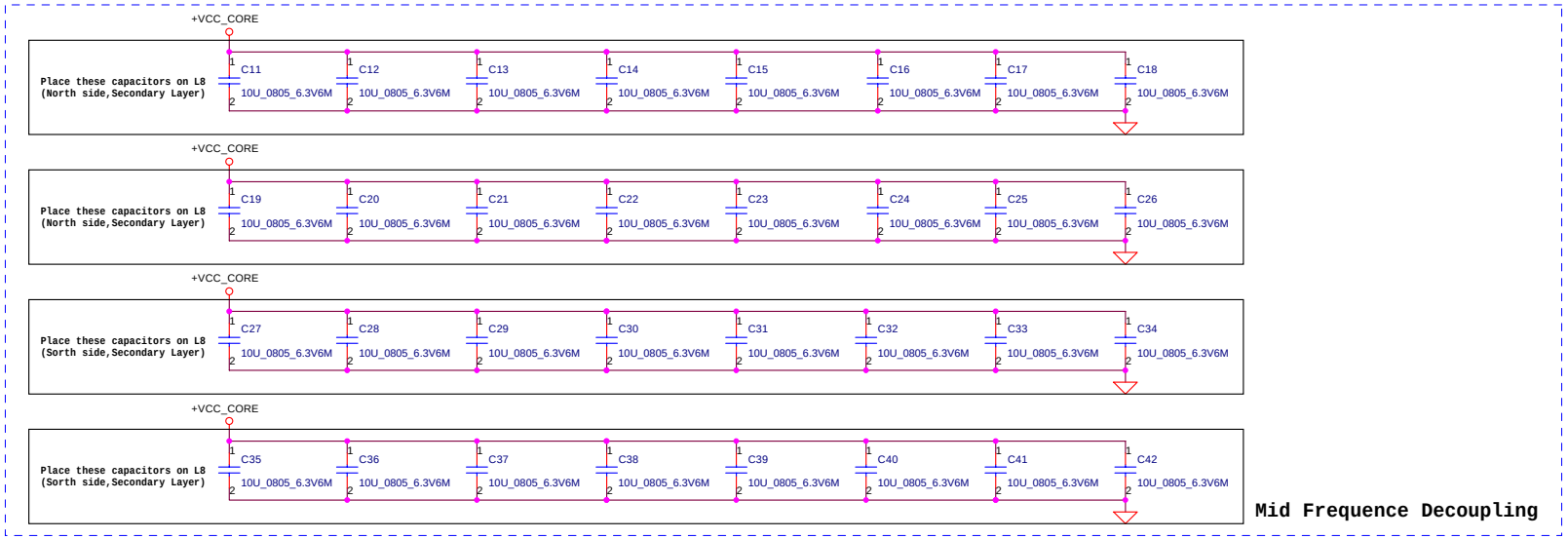
Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

Size	Document Number	Rev
Custom	LA-3732P	1.0

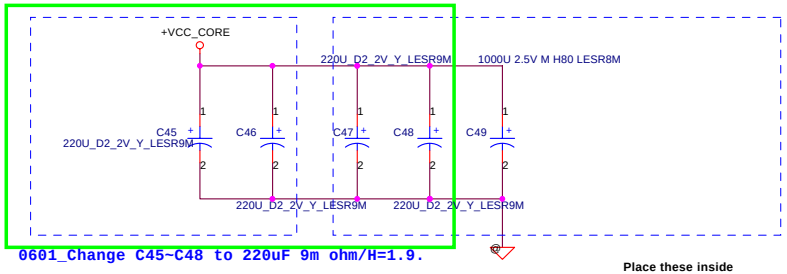
Date: Monday, July 09, 2007 | Sheet 5 of 42





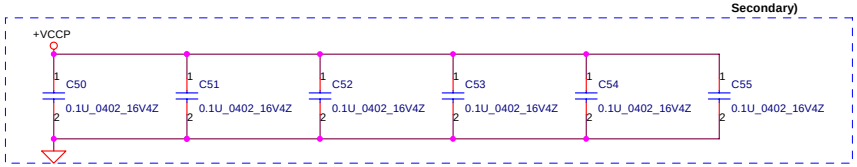
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



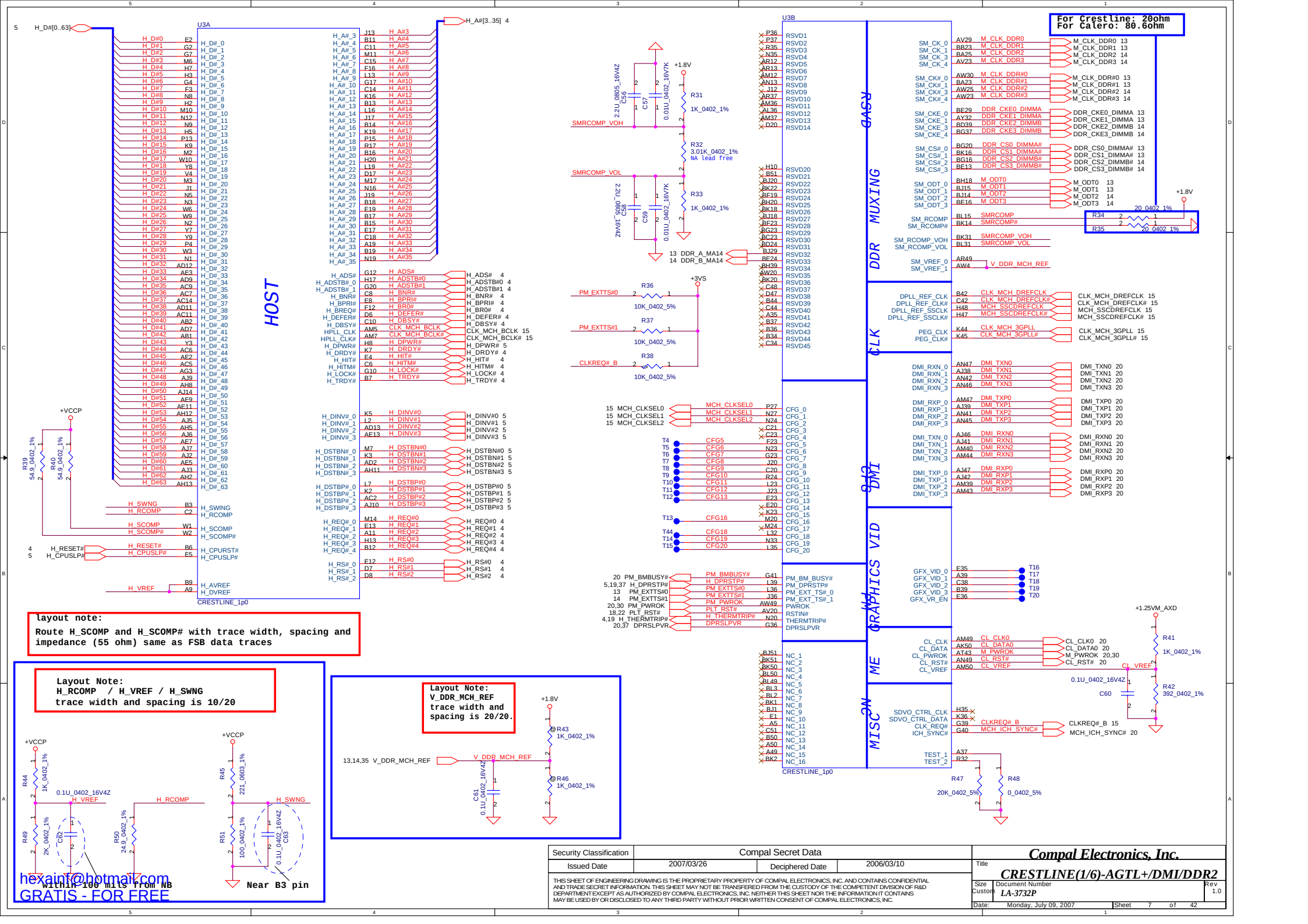
0601_Change C45~C48 to 220uF 9m ohm/H=1.9.

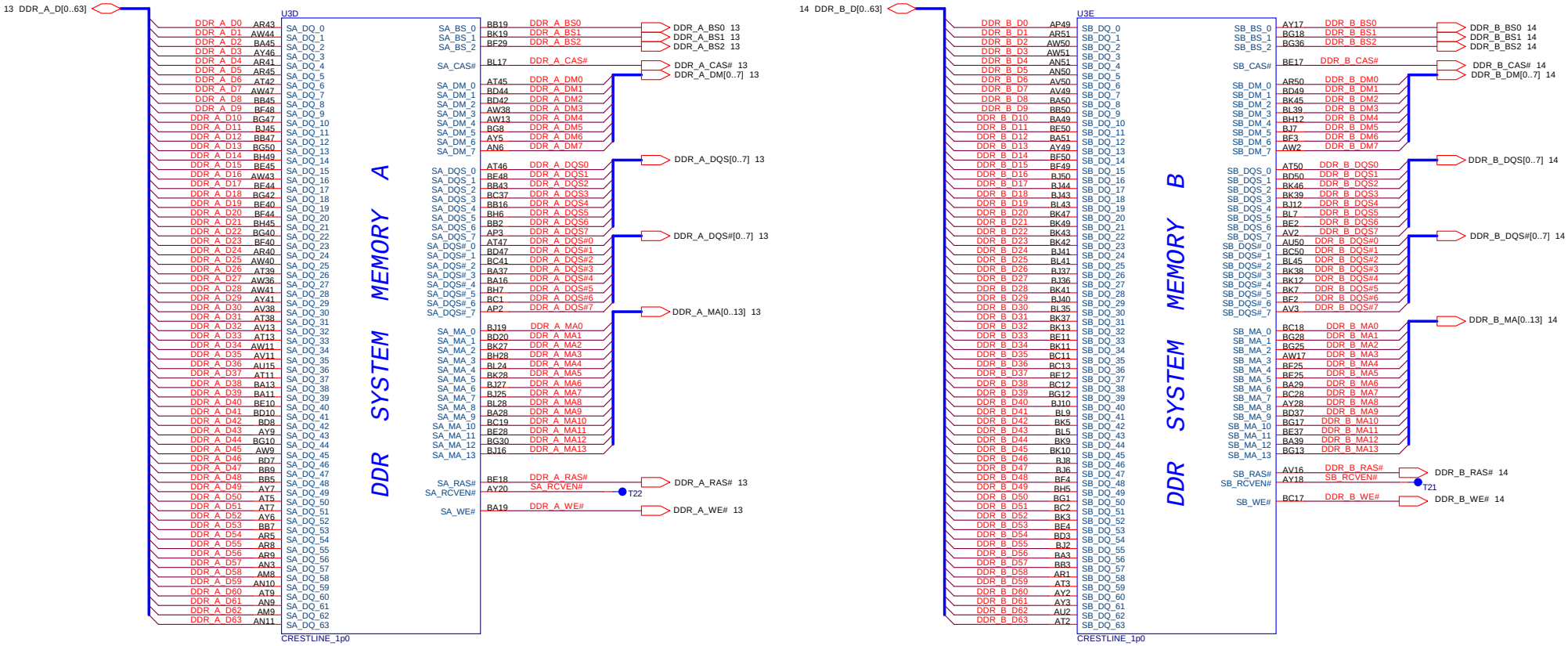
Place these inside socket cavity on L8 (North side Secondary)



Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	Merom(3/3)-GND&Bypass
Size: Custom	Document Number: LA-3732P
Rev	1.0
Date: Monday, July 09, 2007	Sheet 6 of 42


For Crestline: 20ohm
For Calero: 80.6ohm
HOST
CRESTLINE_1p0
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Within 100 mils from NB
Near B3 pin
Layout Note:
V_DDR_MCH_REF
trace width and spacing is 20/20.
hexainf@hotmail.com
GRATIS - FOR FREE
Security Classification
Compal Secret Data
Issued Date
2007/03/26
Deciphered Date
2006/03/10
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size
Custom
Document Number
LA-3732P
Rev
1.0
Date:
Monday, July 09, 2007
Sheet
7
of
42



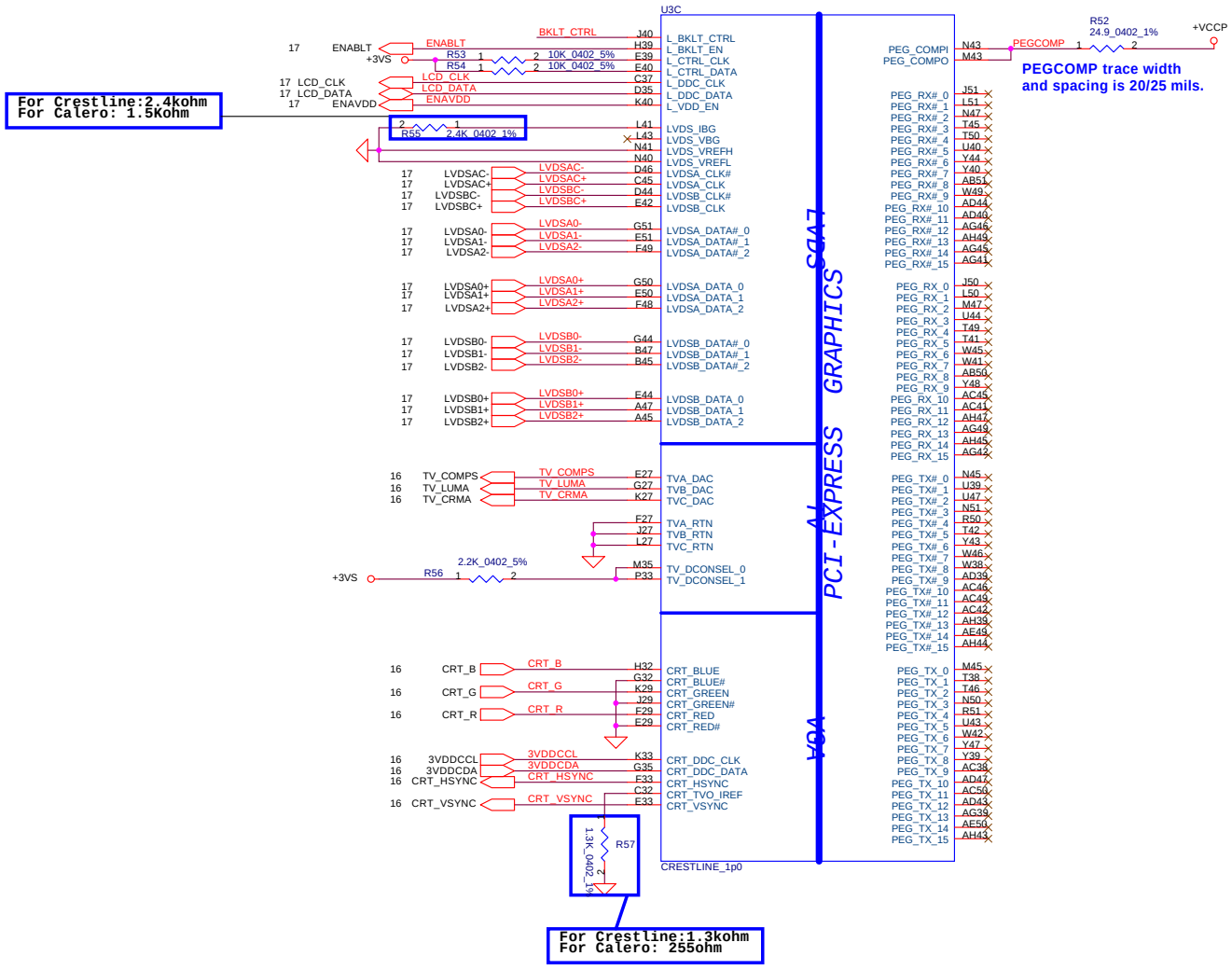
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CRESTLINE((2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	LA-3732P	1.0

Date: Monday, July 09, 2007 | Sheet 8 of 42



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

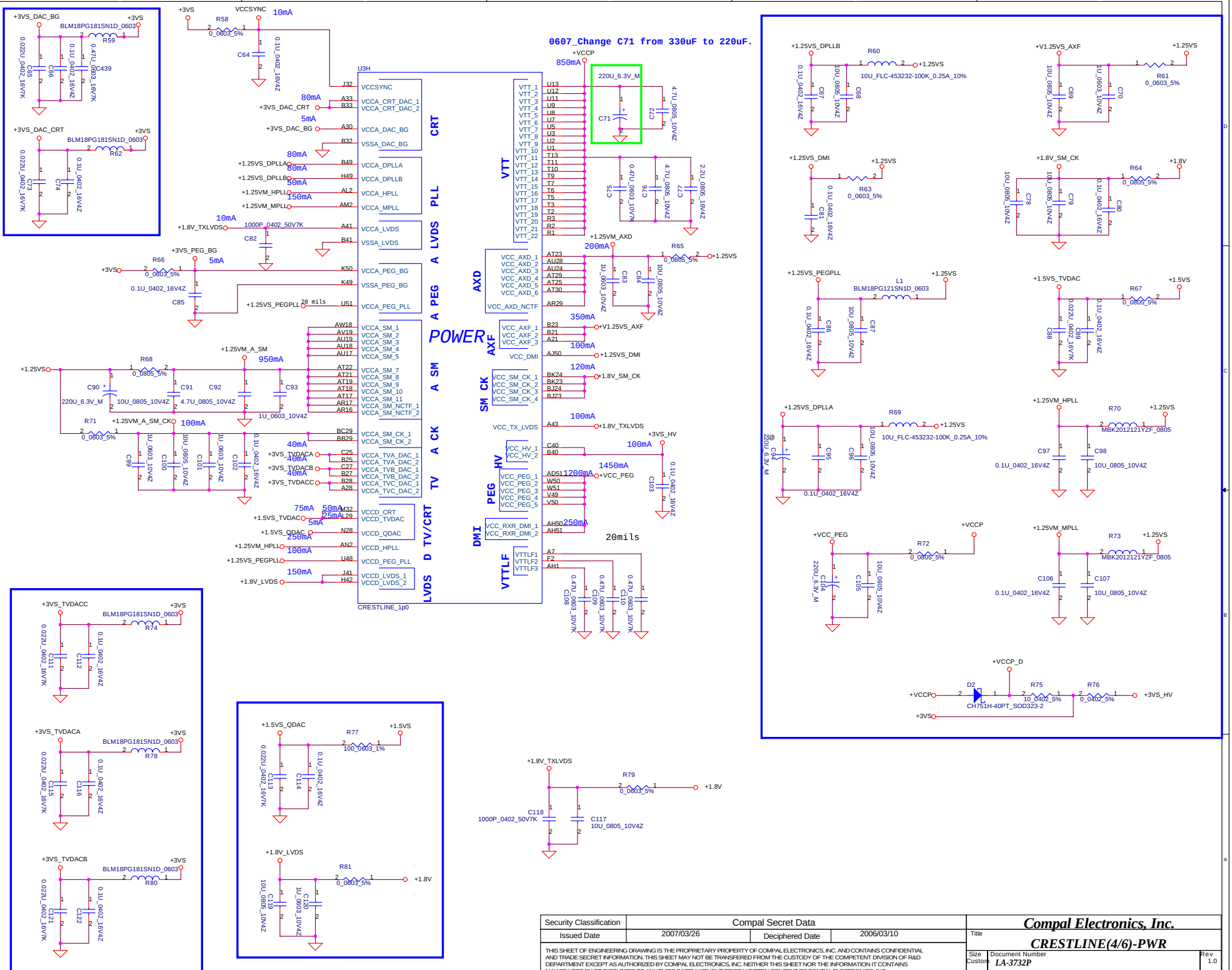
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: CRESTLINE((3/6)-VGA/LVDS/TV

Size: Custom	Document Number: LA-3732P	Rev: 1.0
Date: Monday, July 09, 2007	Sheet 9 of 42	



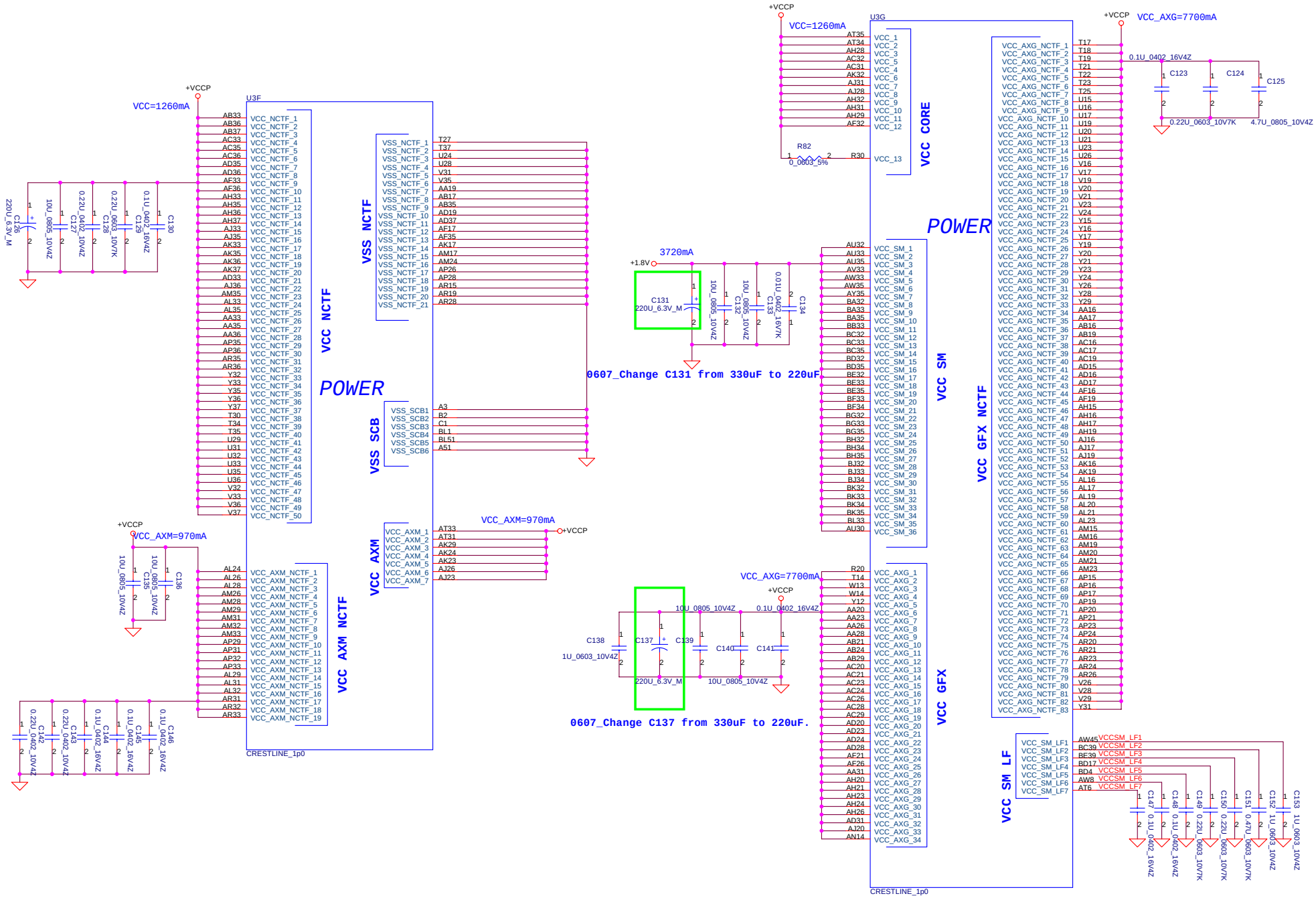
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CRESTLINE(4/6)-PWR**

Size	Document Number	Rev
Custom	LA-3732P	1.0

Date: Monday, July 09, 2007 Sheet 10 of 42



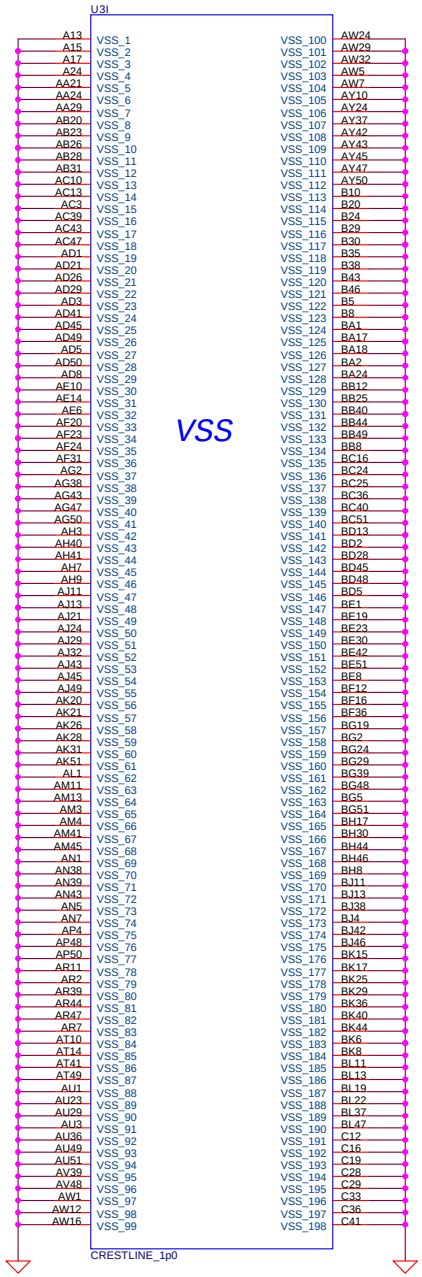
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

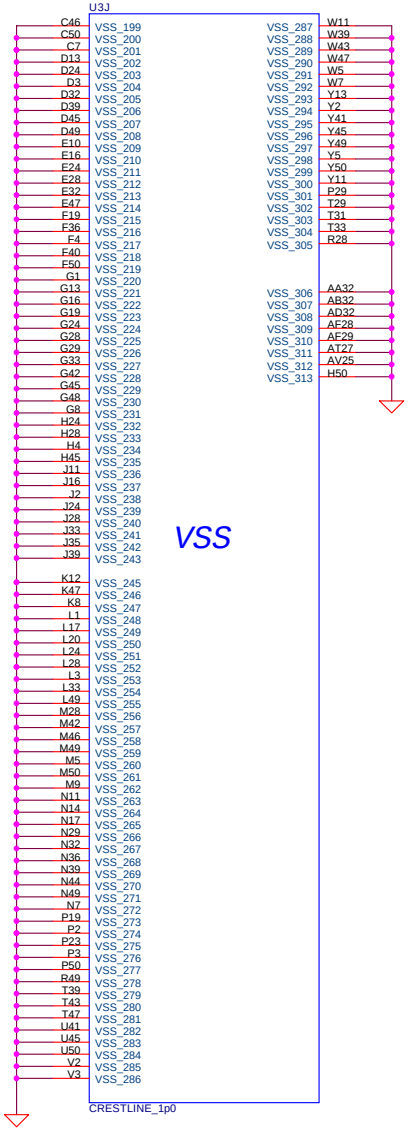
Compal Electronics, Inc.

Title: **CRESTLINE((5/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-3732P	1.0

Date: Monday, July 09, 2007 Sheet 11 of 42





Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

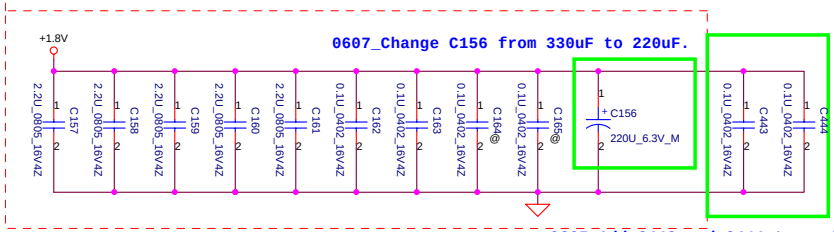
Title: **CRESTLINE((6/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-3732P	1.0

Date: Monday, July 09, 2007 | Sheet 12 of 42

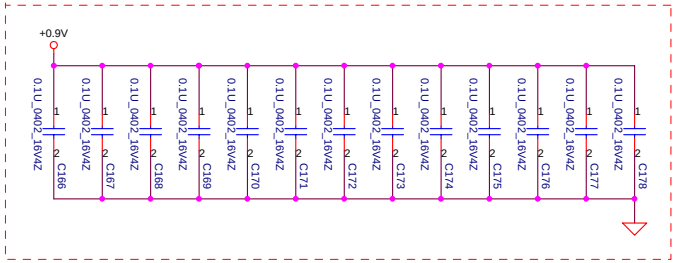
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
7,8 DDR_A_MA[0..14]

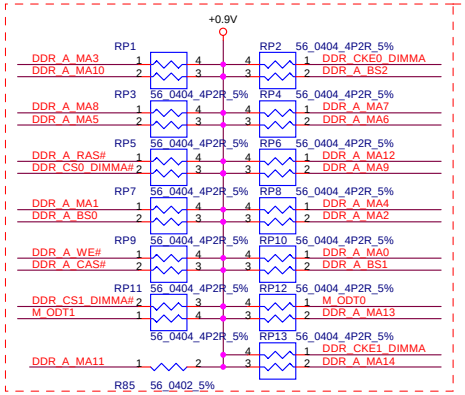
Layout Note:
Place near JP34



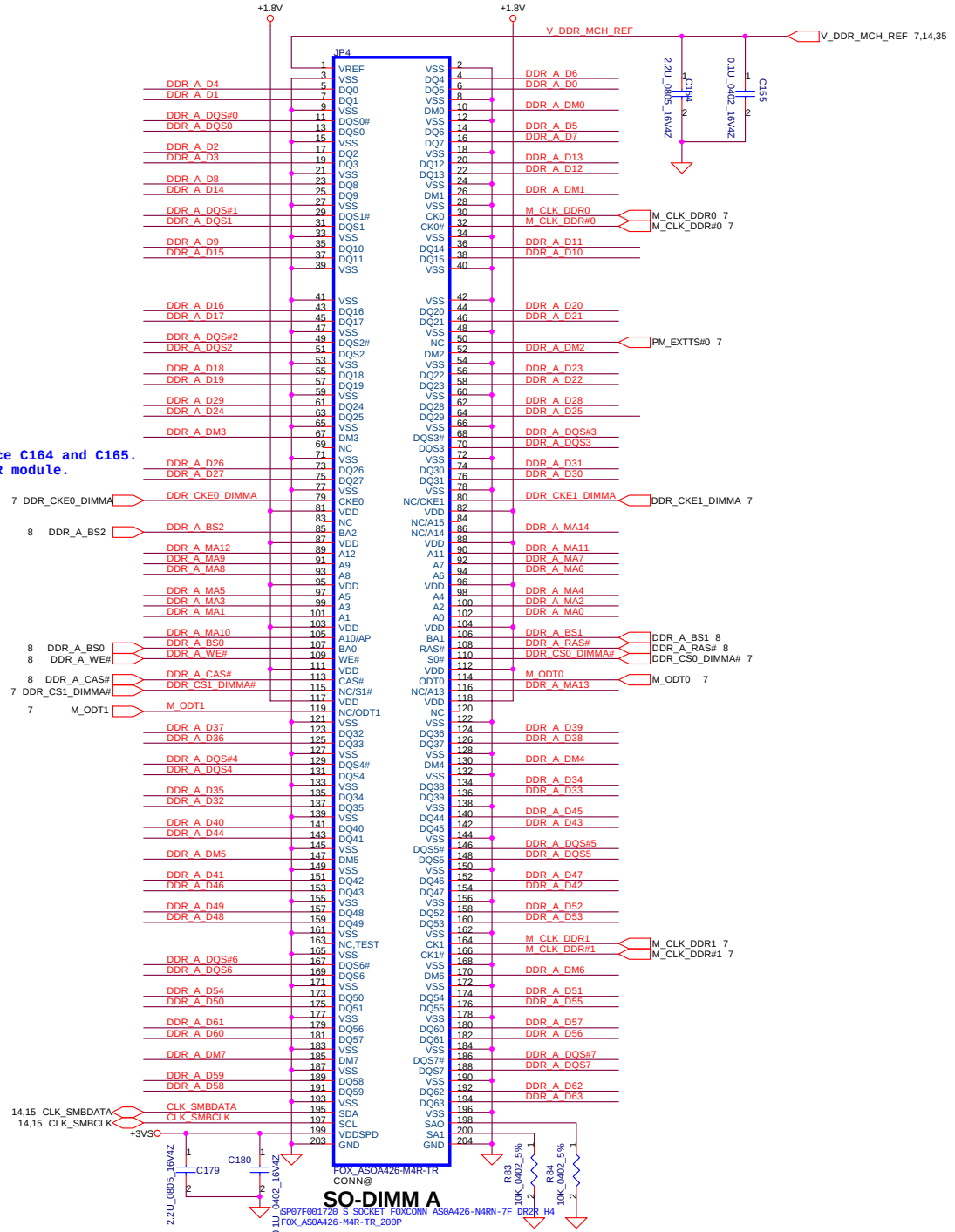
0605_Add C443 and C444 to replace C164 and C165.
To solve interfere with DDR module.

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

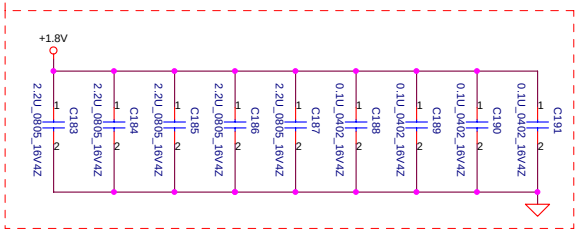
Title: **DDRII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-3732P	1.0

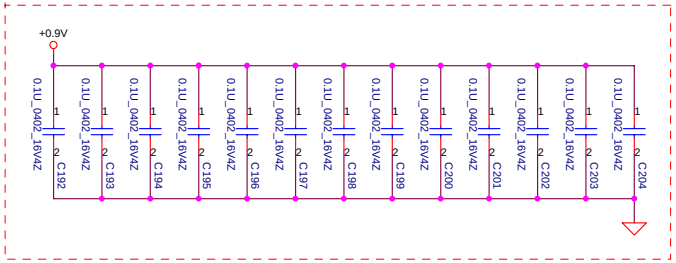
Date: Monday, July 09, 2007 Sheet 13 of 42

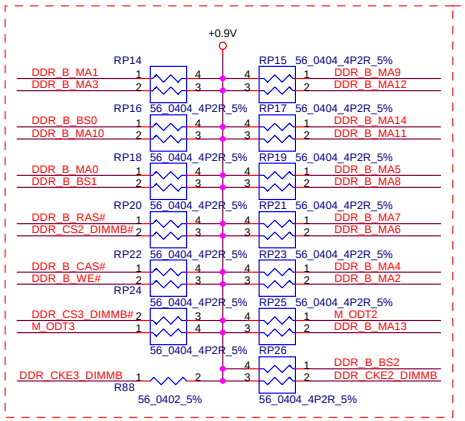
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
7,8 DDR_B_MA[0..14]

Layout Note:
Place near JP10

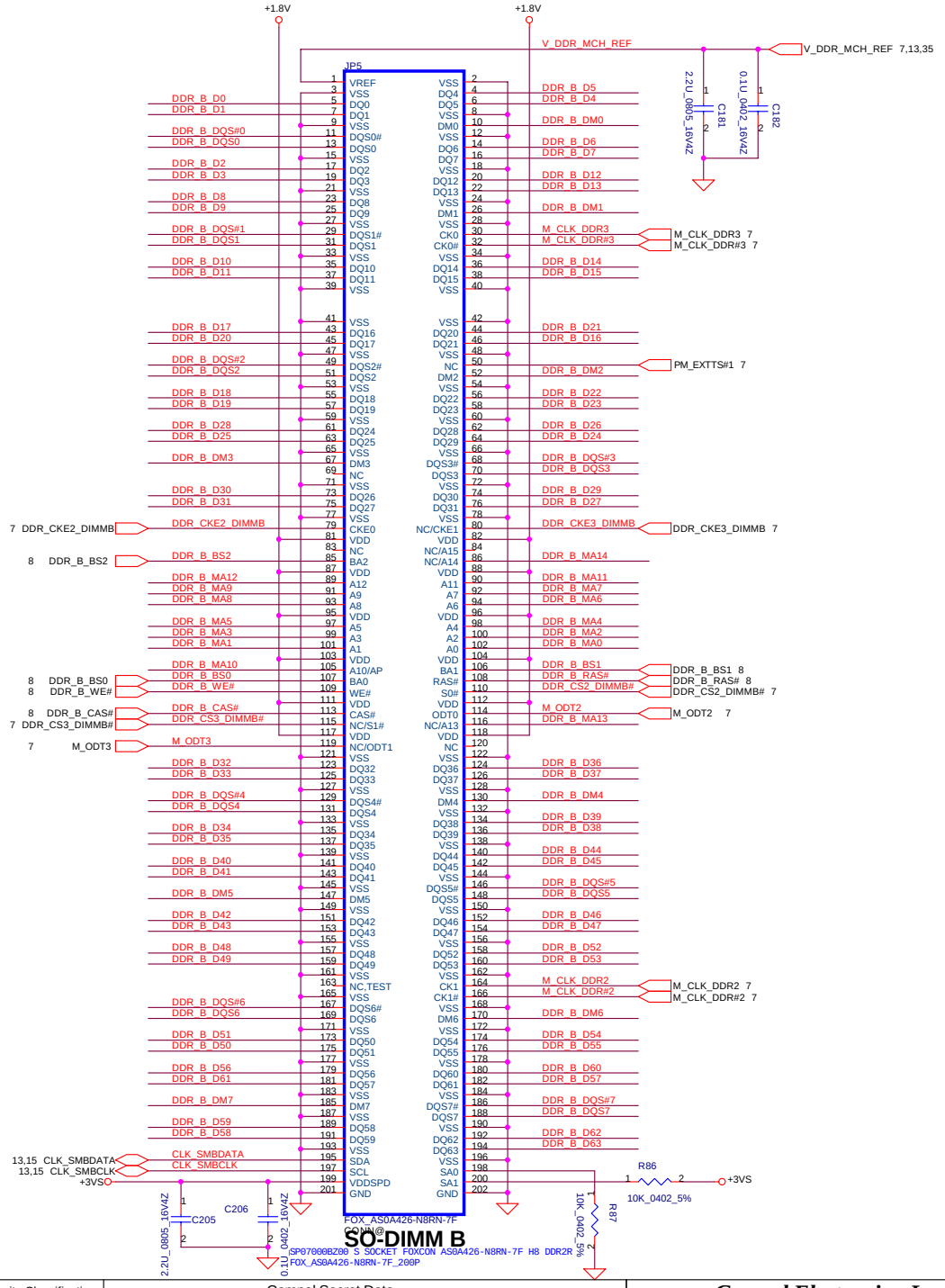


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"



Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-3732P	1.0
Date: Monday, July 09, 2007	Sheet 14 of 42	

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

CLRP4,CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- CPU option
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

Routing the trace at least 10mil

Place close to U4

SB, MINI PCI

For Layout request:
1. Change MINI_CLKREQ# from pin 32 to pin 43.
2. Change CLK_PCIE_MCARD from SRC9 to SRC6.

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

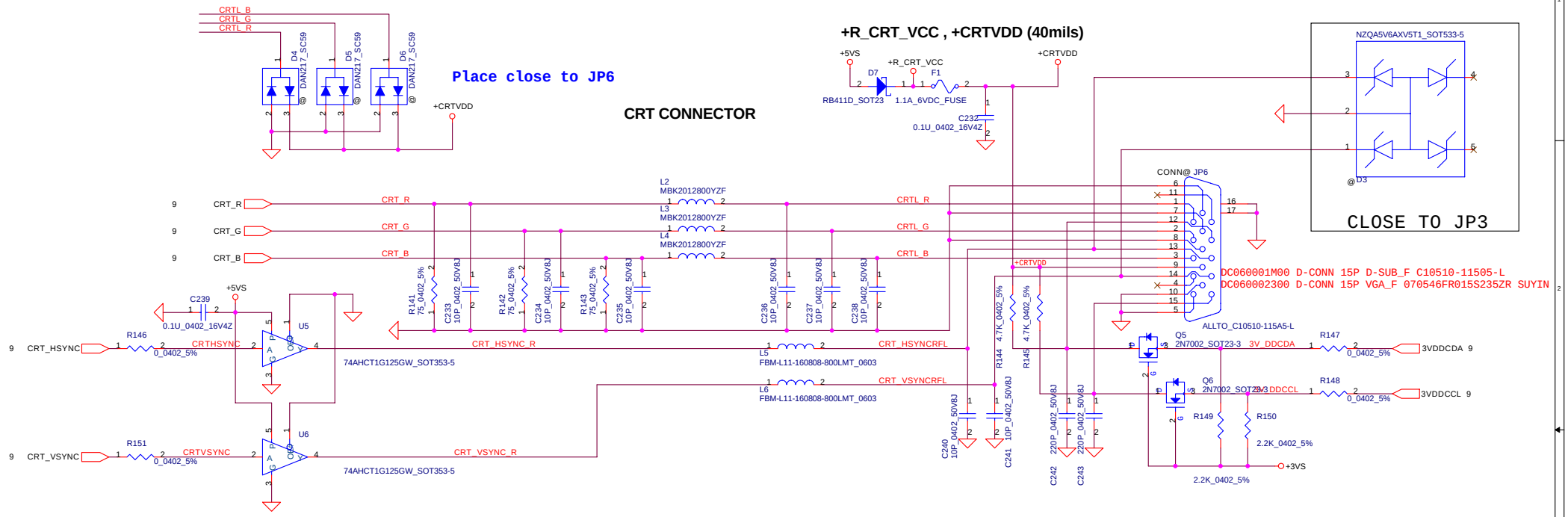
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

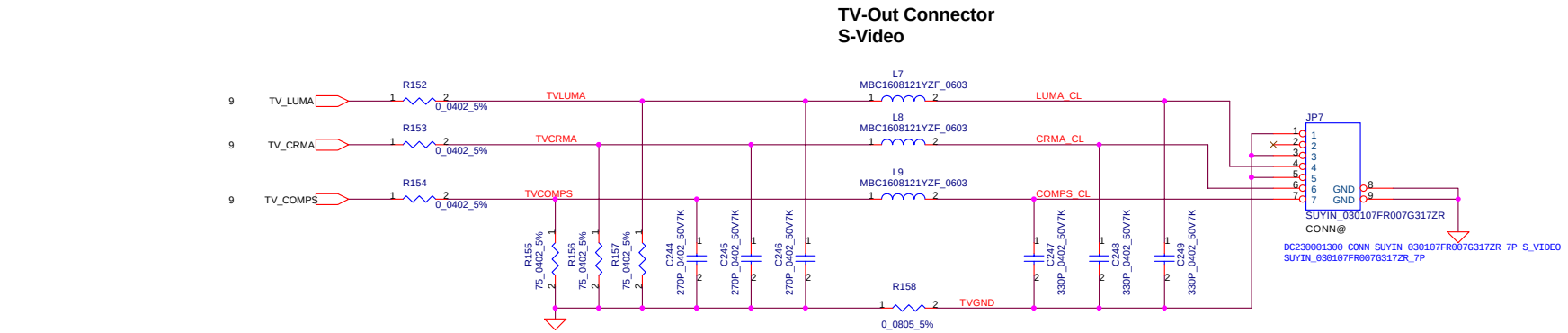
Compal Electronics, Inc.

Title: **Clock generator**

Size: | Document Number: **LA-3732P** | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 15 of 42





Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

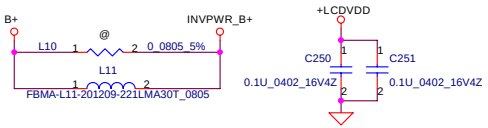
Compal Electronics, Inc.

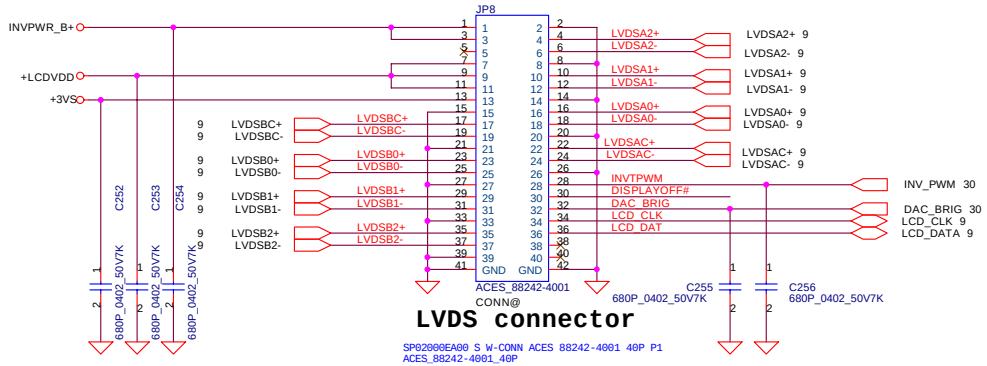
Title: **CRT & TVout Connector**

Size	Document Number	Rev
	LA-3732P	1.0

Date: Monday, July 09, 2007 | Sheet 16 of 42

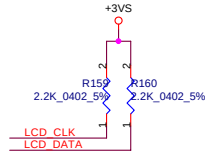
LVDS CONN

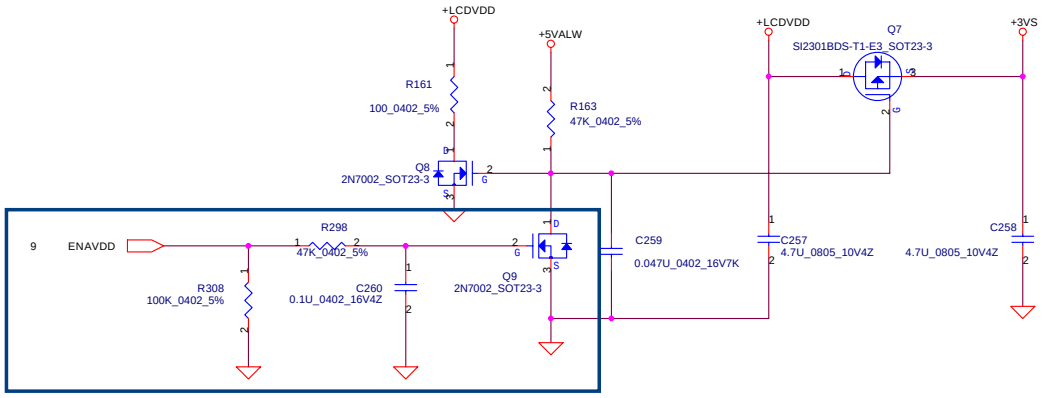




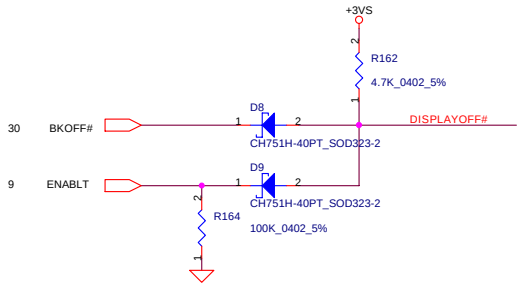
LVDS connector

SP02000EA00 S W-CONN ACES 88242-4001 40P P1
ACES_88242-4001_40P



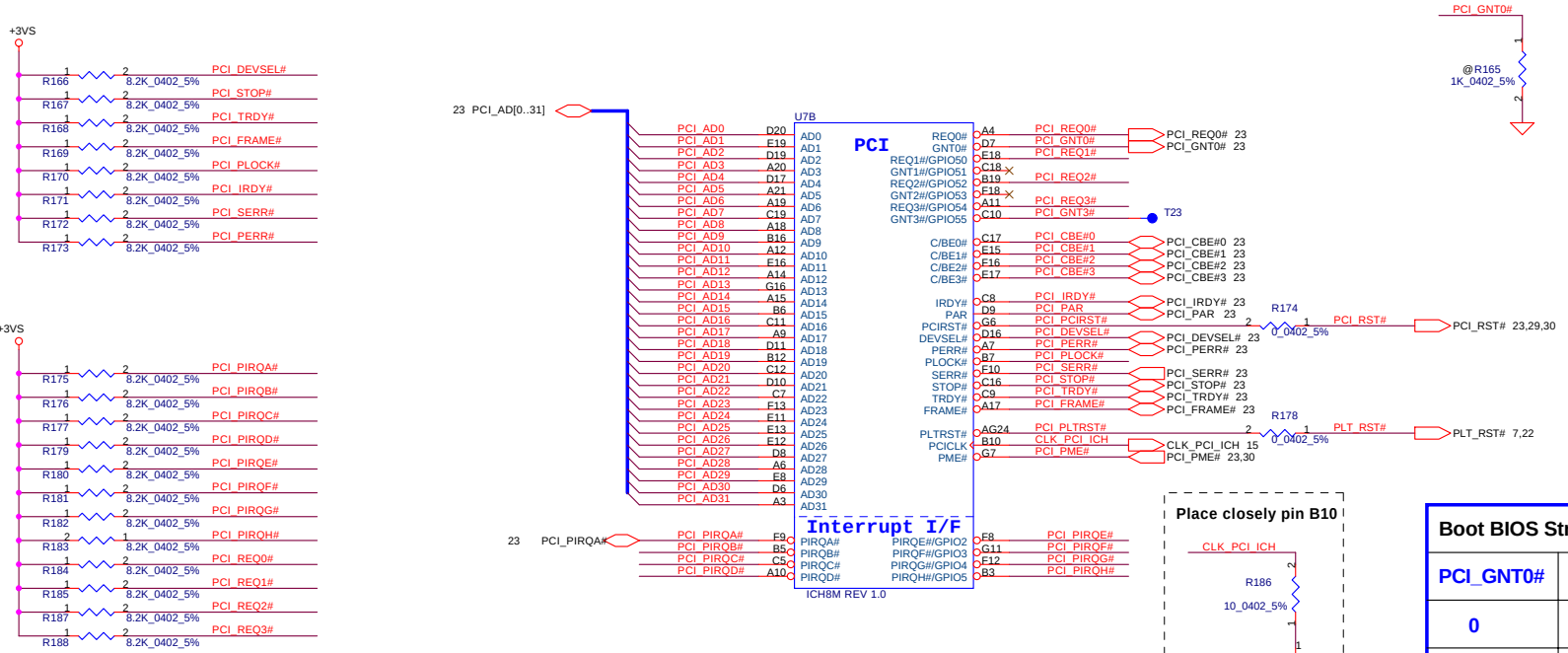


Avoid Panel display garbage after power on.



Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.		
Title	LCD CONN.	
Size	Document Number LA-3732P	Rev 1.0
Date: Monday, July 09, 2007	Sheet 17 of 42	



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enble High= Default

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

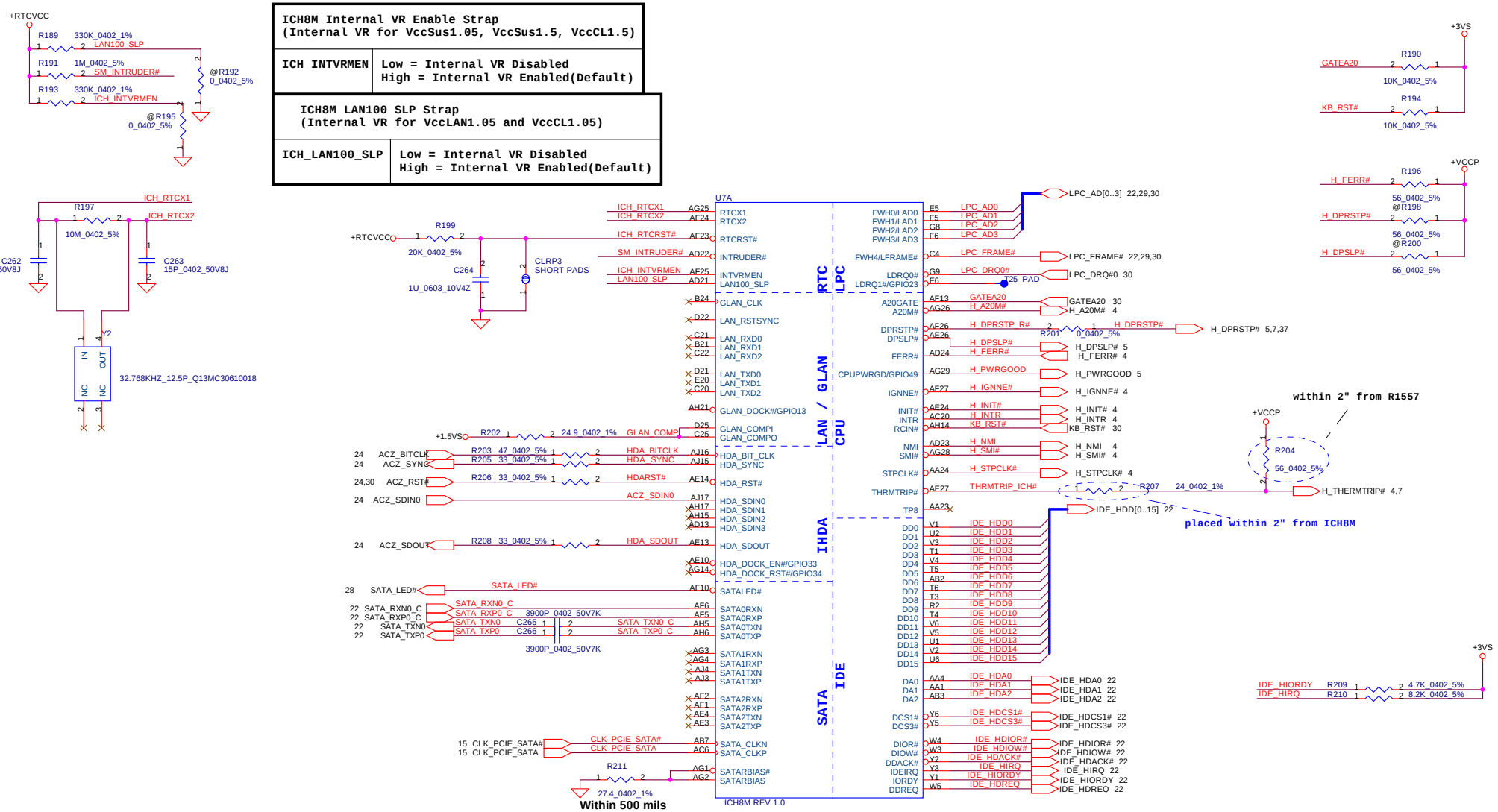
Title: ICH8(1/4)-PCI/INT

Size: | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 18 of 42

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



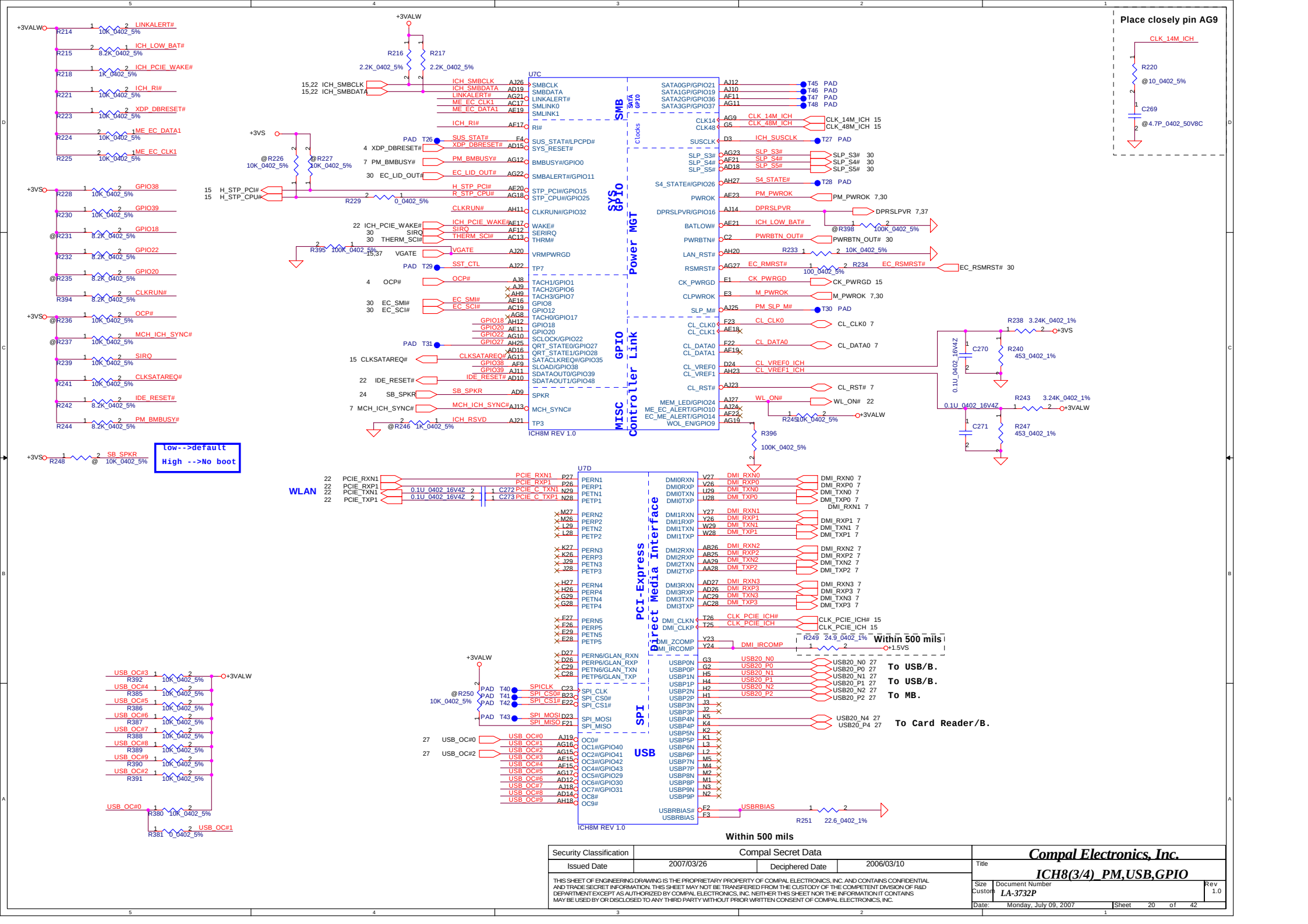
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size	Document Number	Rev
Custom	LA-3732P	1.0

Date: Monday, July 09, 2007 Sheet 19 of 42



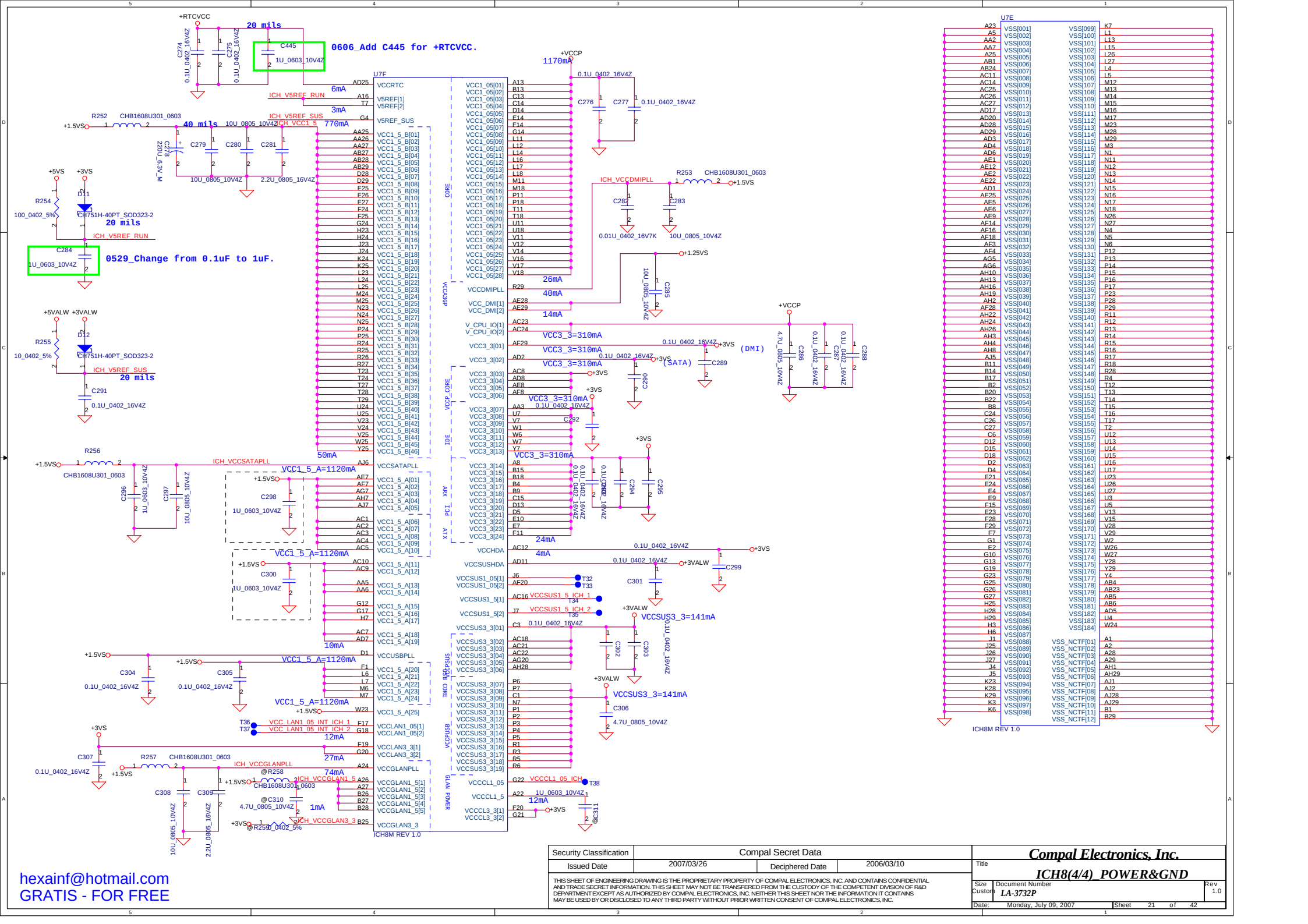
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH8(3/4)_PM,USB,GPIO**

Size	Document Number	Rev
Custom	LA-3732P	1.0

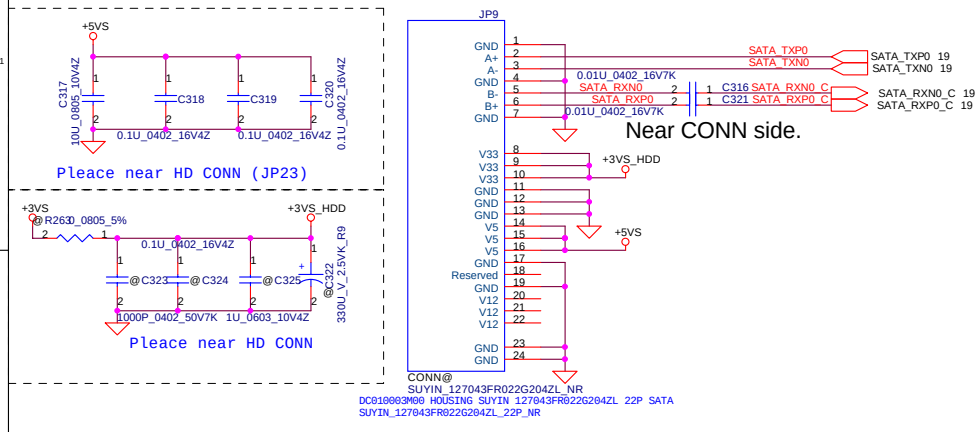
Date: Monday, July 09, 2007 | Sheet 20 of 42



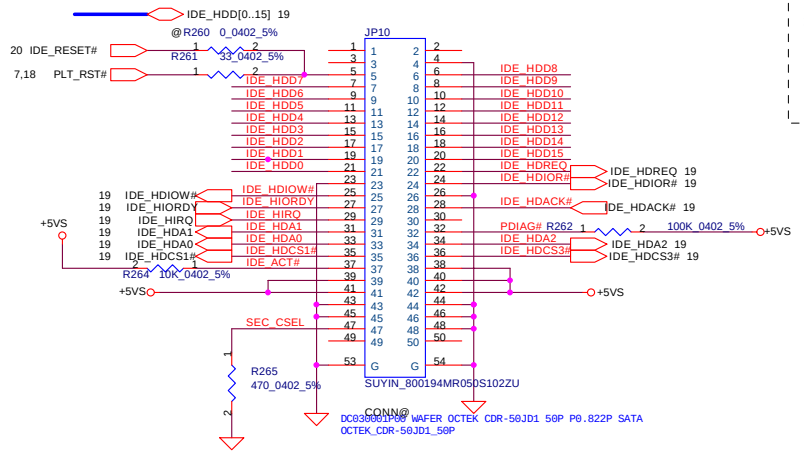
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

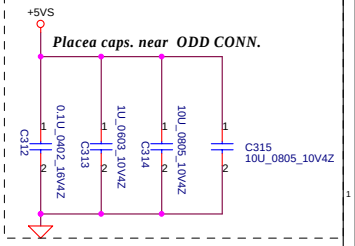
Compal Electronics, Inc.			
Title: ICH8(4/4)_POWER&GND			
Size: Custom	Document Number: LA-3732P		Rev: 1.0
Date: Monday, July 09, 2007	Sheet 21 of 42		

HDD Connector

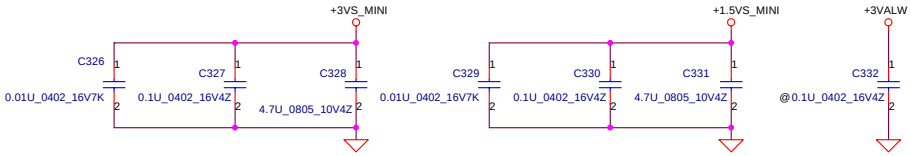


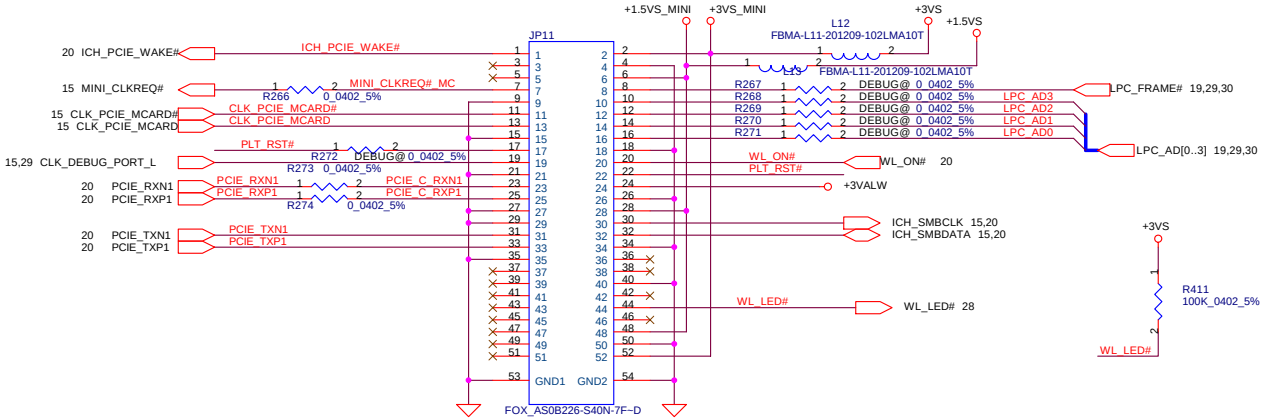
CD-ROM Connector





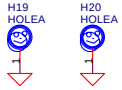
Mini-Express Card---WLAN





SP01000P700 S H-CONN ACES 88914-5204 52P P0.8

Mini Card STANDOFF



EC029000100 MINICARD_STANDOFF_8

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2007/08/29

Compal Electronics, Inc.

Title: **HDD/ODD/Mini Card CONN.**

Size	Document Number	Rev
	LA-3732P	1.0

Date: Monday, July 09, 2007 Sheet 22 of 42

Cloase to JP12.

0601_Add L21 and L22 For EMI request.

For EMI, locate close to LAN chip

0611_Reserve D27 and D28 For EMI request.

JM34F2*-N5125-7F
JM34F2A-M5125-7F

close to chip

close to magnetic

0310 Dammy by safty request.
Footprint can not match part number.

0601_For EMI request.

RJ11

PCI I/F

LAN I/F

Power

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2007/08/29

Compal Electronics, Inc.

Title: LAN-8100CL

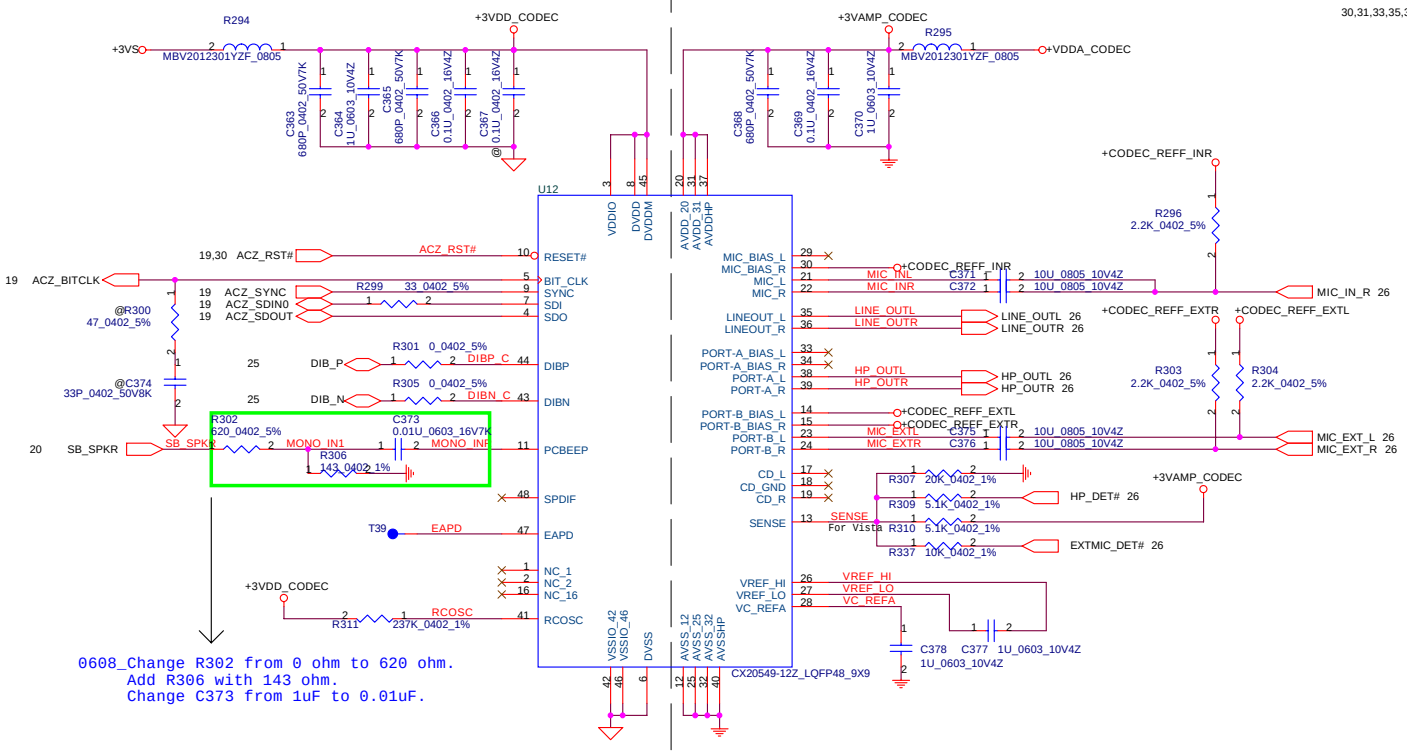
Size | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 23 of 42

AUDIO CODEC

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

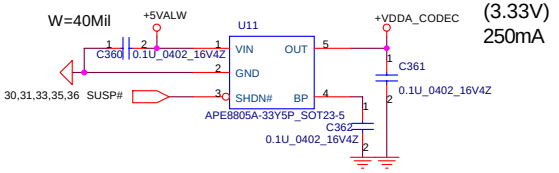
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

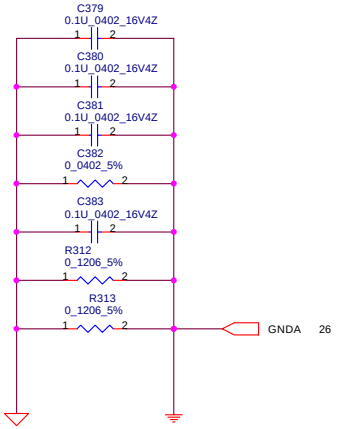


0608_Change R302 from 0 ohm to 620 ohm.
Add R306 with 143 ohm.
Change C373 from 1uF to 0.01uF.

DIGITAL **ANALOG**

CODEC POWER





HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0(LOW)	0(LOW)	OFF	ON	ON	Disable
0(LOW)	NC	OFF	ON	OFF	Disable
NC	0(LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

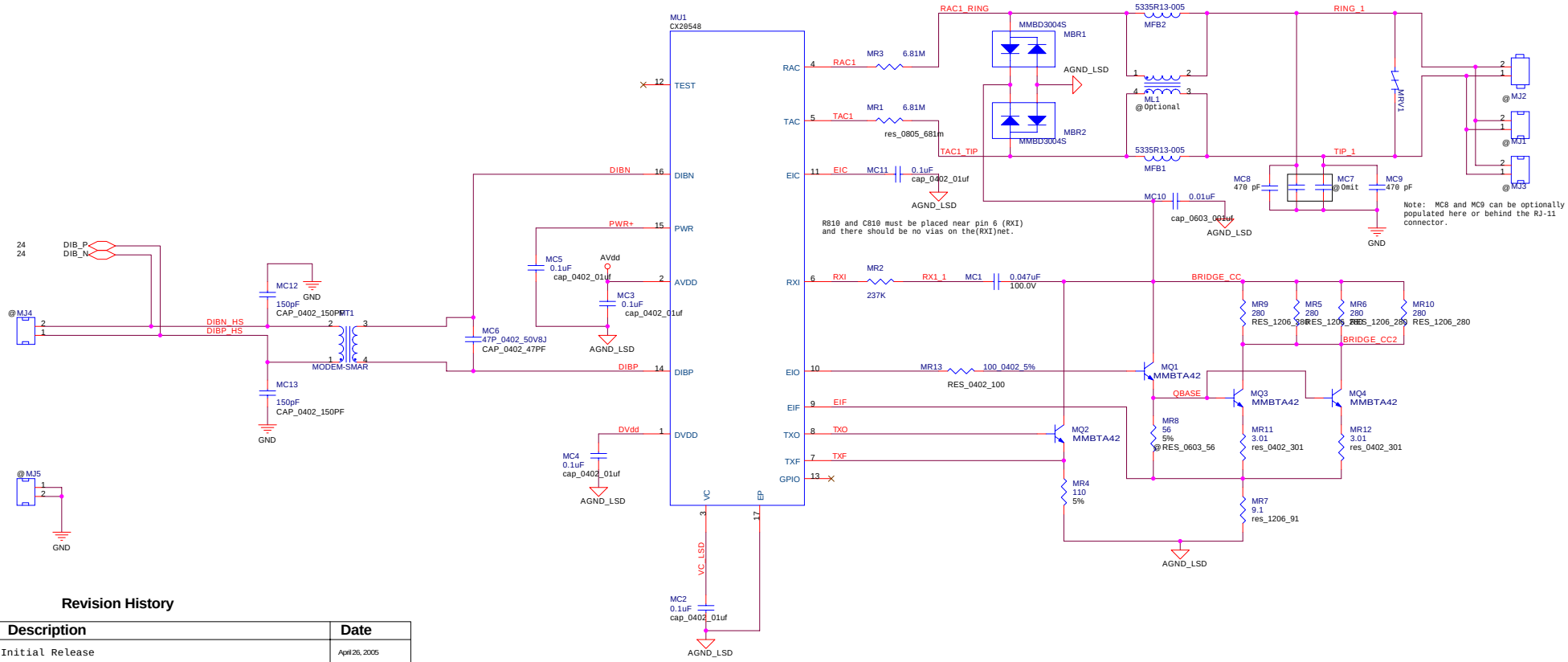
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: AMOM_codec

Size: Custom | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 24 of 42



Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

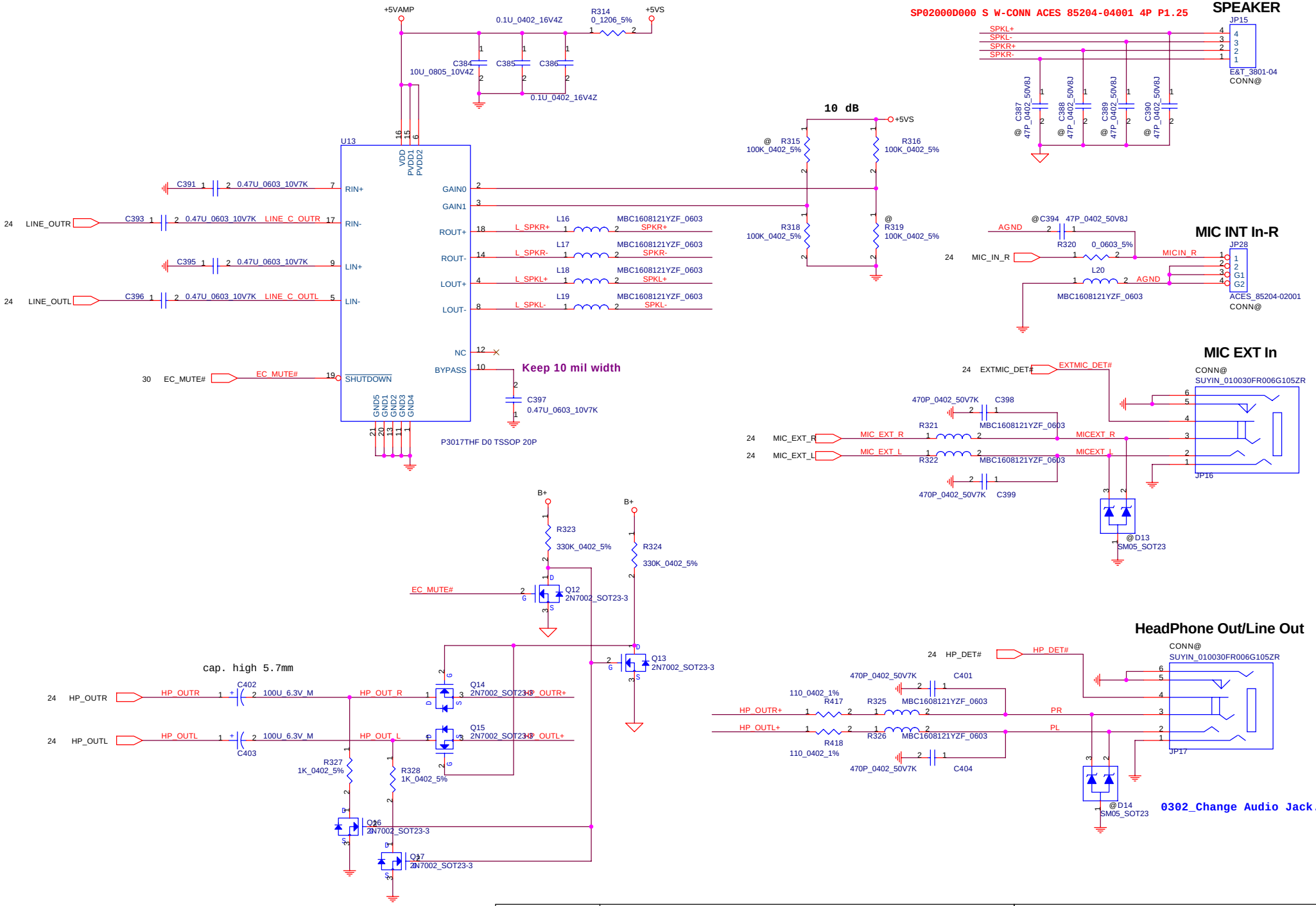
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2007/07/26

Compal Electronics, Inc.

Title: **AMOM-CX20548**

Size: | Document Number: **LA-3732P** | Rev: 1.0

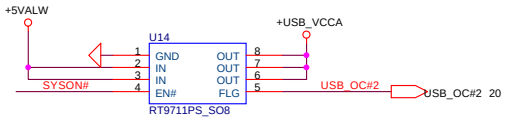
Date: Monday, July 09, 2007 | Sheet 25 of 42

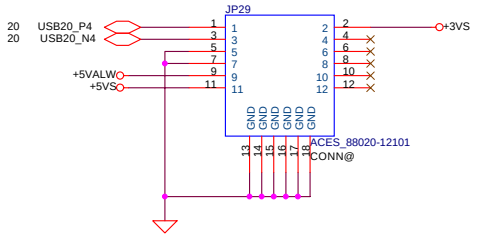


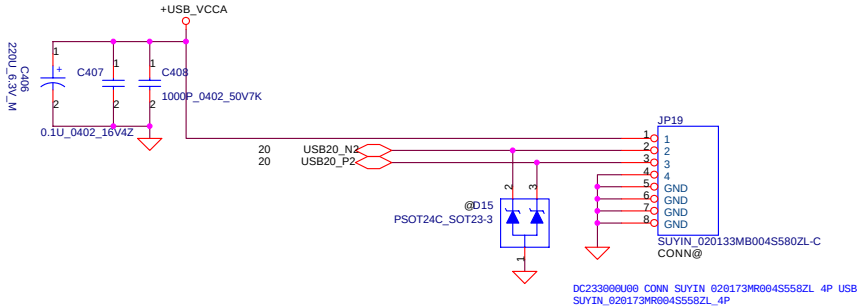
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2007/08/29

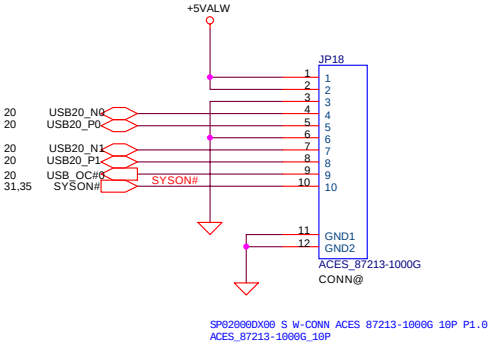
Compal Electronics, Inc.			
Title: AMP & Audio Jack			
Size	Document Number: LA-3732P		Rev: 1.0
Date: Monday, July 09, 2007		Sheet 26 of 42	

USB Port









Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

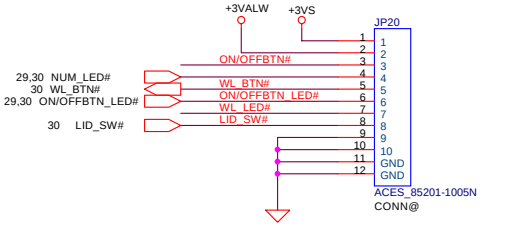
Compal Electronics, Inc.

Title: **USB CONN.**

Size | Document Number: **LA-3732P** | Rev: 1.0

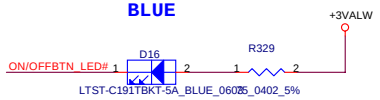
Date: Monday, July 09, 2007 | Sheet 27 of 42

M/BtoS/B



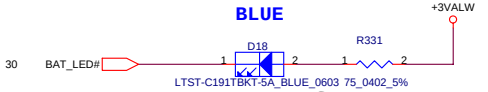
POWER LED(Left 1)

BLUE



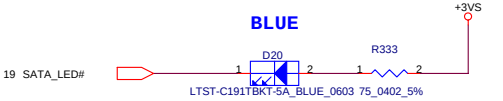
Battery Charge LED(Left 2)

BLUE

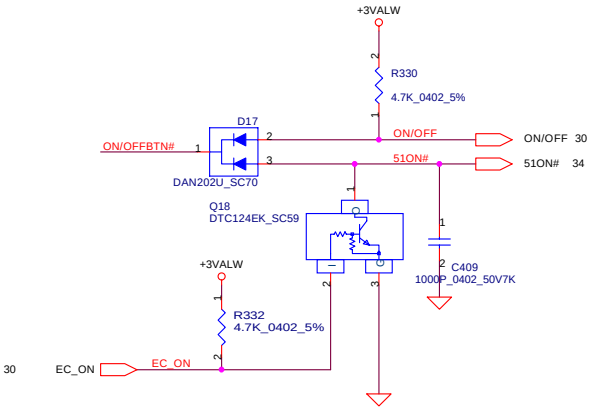


HDD LED(Left 3)

BLUE

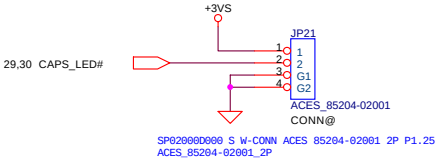


Power ON/OFF

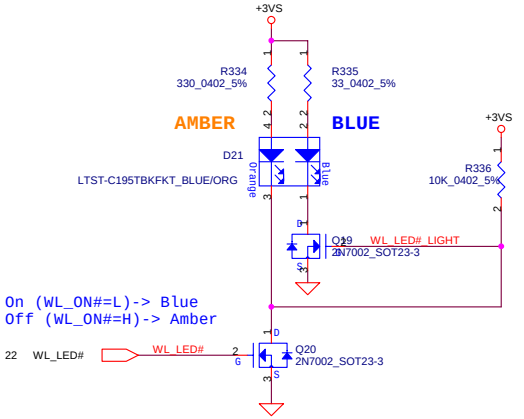


0426_Change all LED power source from 5V to 3V.

M/B to SB(Caps Lock LED)

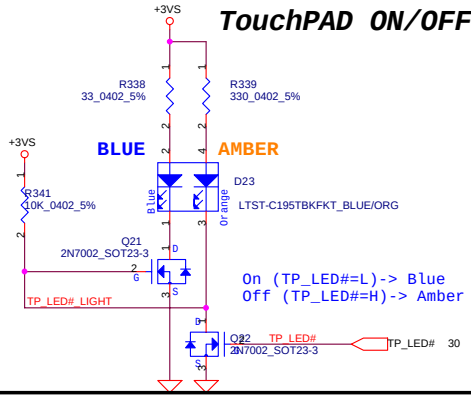


Wireless ON/OFF LED(Left 4)

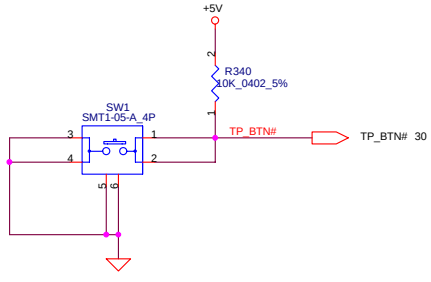


D21, D25, D23 Footprint can not match part number.

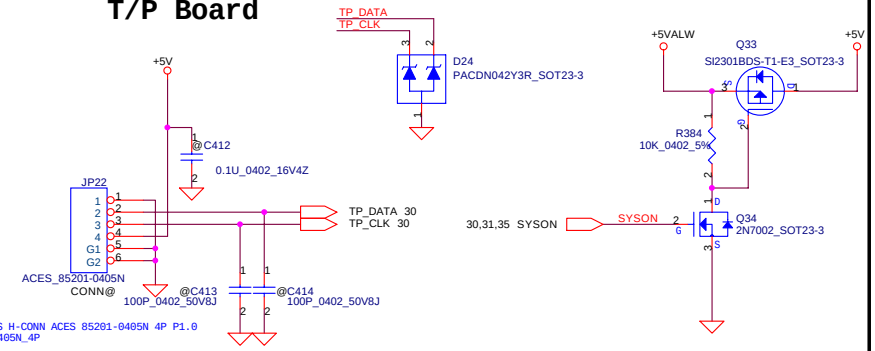
TouchPAD ON/OFF LED



TP ON/OFF



T/P Board



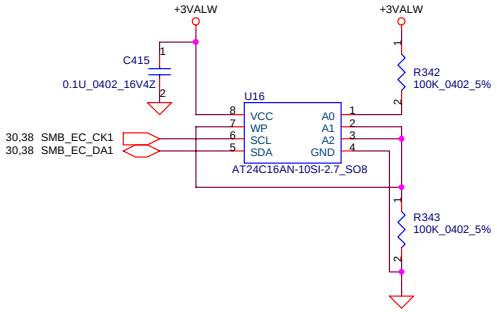
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

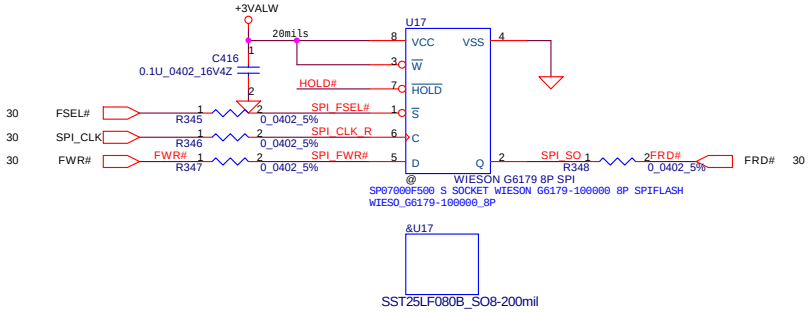
Title: LED/SW

Size	Document Number	Rev
	LA-3732P	1.0

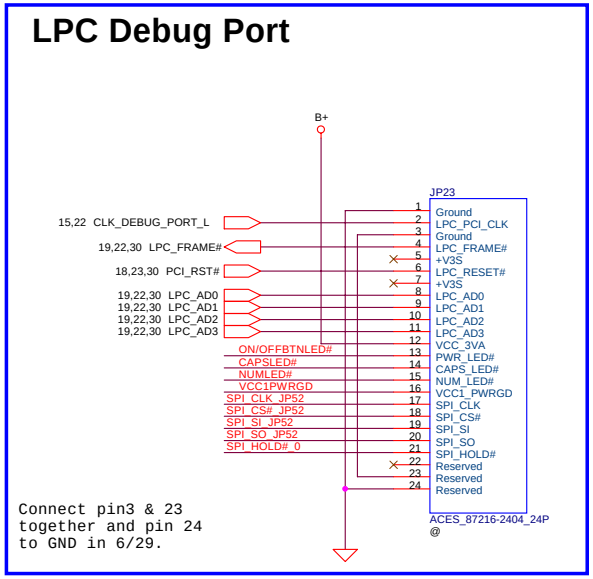
Date: Monday, July 09, 2007 Sheet 28 of 42

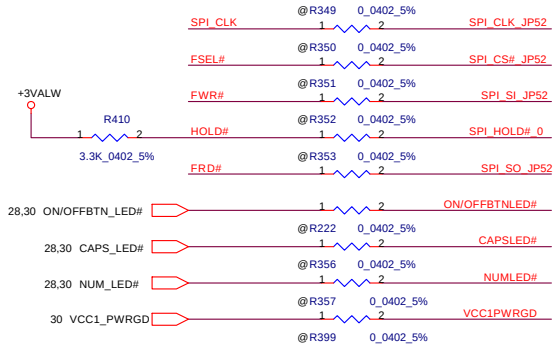


SPI ROM



LPC Debug Port





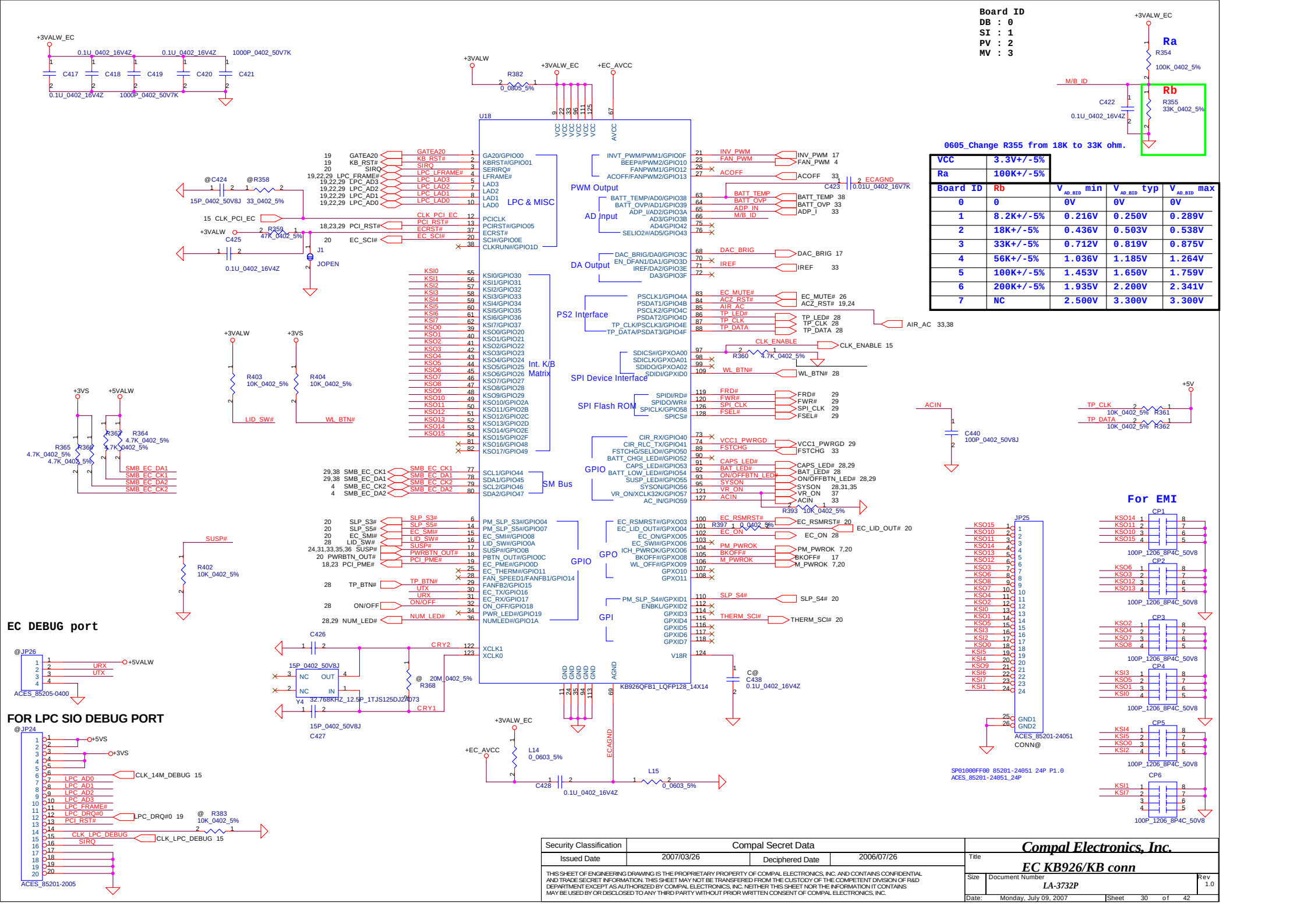
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

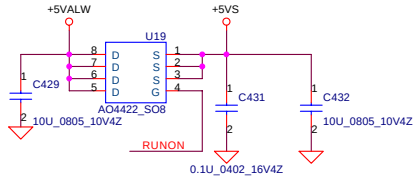
Title: **BIOS ROM**

Size	Document Number	Rev
	LA-3732P	1.0

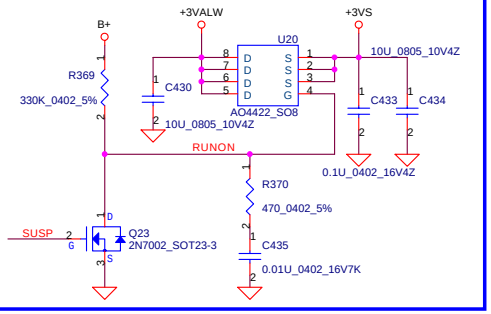
Date: Monday, July 09, 2007 Sheet 29 of 42

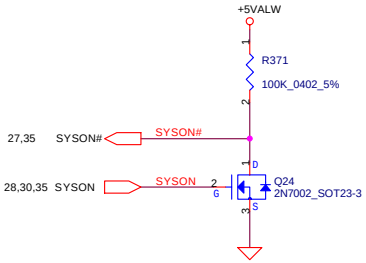

Board ID
DB : 0
SI : 1
PV : 2
MV : 3
Ra
R354
100K_0402_5%
Rb
R355
33K_0402_5%
C422
0.1U_0402_16V4Z
M/B_ID
0605_Change R355 from 18K to 33K ohm.
VCC 3.3V+/-5%
Ra 100K+/-5%
Board ID | Rb | V_AD_BID min | V_AD_BID typ | V_AD_BID max
0 | 0 | 0V | 0V | 0V
1 | 8.2K+/-5% | 0.216V | 0.250V | 0.289V
2 | 18K+/-5% | 0.436V | 0.503V | 0.538V
3 | 33K+/-5% | 0.712V | 0.819V | 0.875V
4 | 56K+/-5% | 1.036V | 1.185V | 1.264V
5 | 100K+/-5% | 1.453V | 1.650V | 1.759V
6 | 200K+/-5% | 1.935V | 2.200V | 2.341V
7 | NC | 2.500V | 3.300V | 3.300V
U18
KB926QFB1_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
EC DEBUG port
FOR LPC SIO DEBUG PORT
For EMI
ACES_85205-0400
ACES_85201-2005
ACES_85201-24051
CONN@
SP01000FF00 85201-24051 24P P1.0
ACES_85201-24_24P
Security Classification | Compal Secret Data
Issued Date | 2007/03/26 | Deciphered Date | 2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC KB926/KB conn
Size | Document Number | Rev
LA-3732P | 1.0
Date: Monday, July 09, 2007 | Sheet 30 of 42

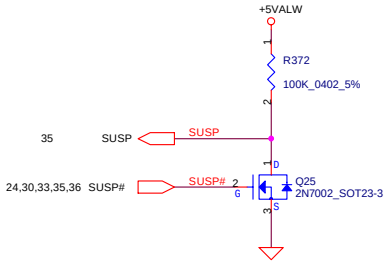
+5VALW to +5VS Transfer

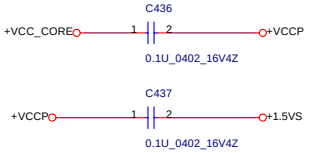


+3VALW to +3VS Transfer

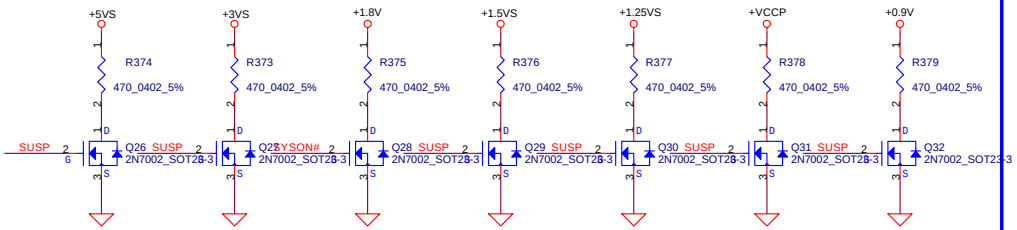


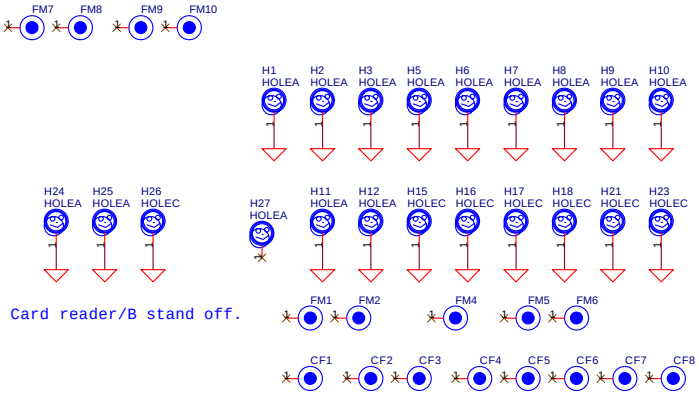






Discharge circuit





For Card reader/B stand off.

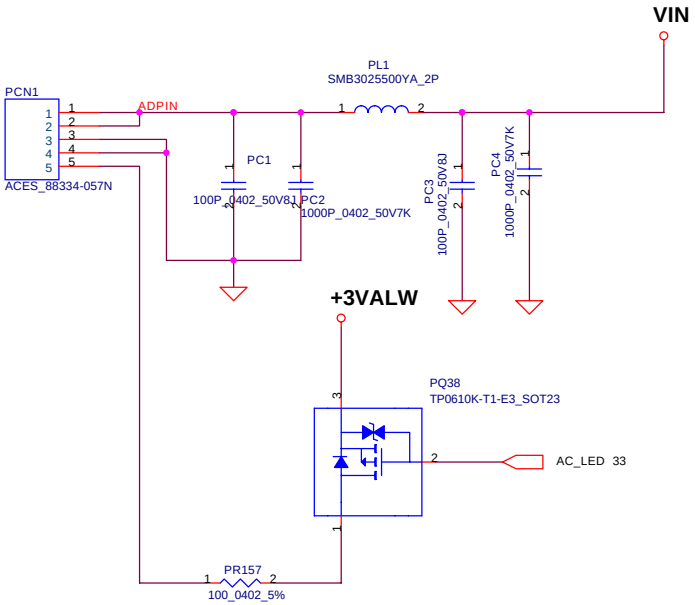
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size	Document Number	Rev
	LA-3732P	1.0

Date: Monday, July 09, 2007 | Sheet 31 of 42

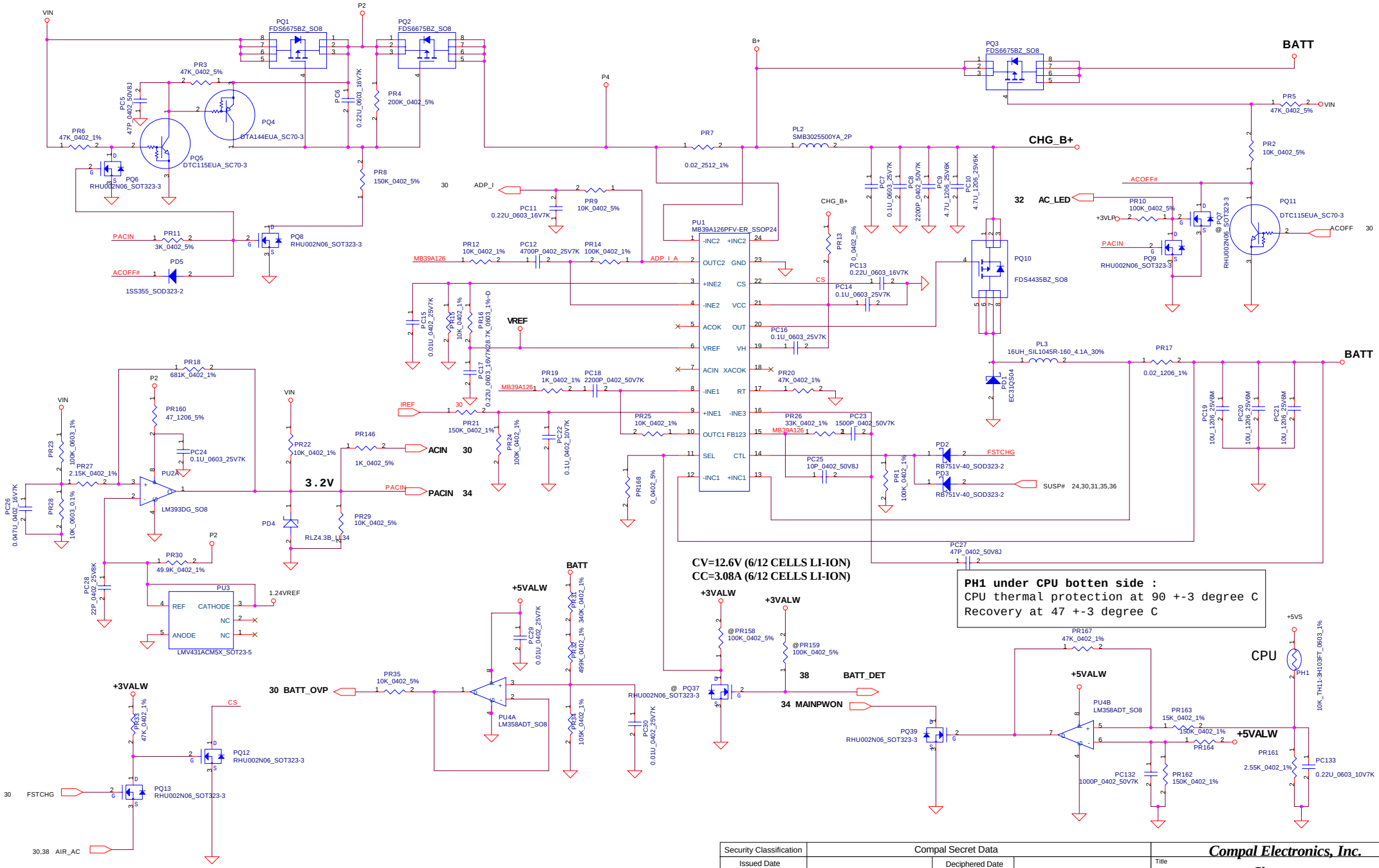


Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Title: **DC CONN**

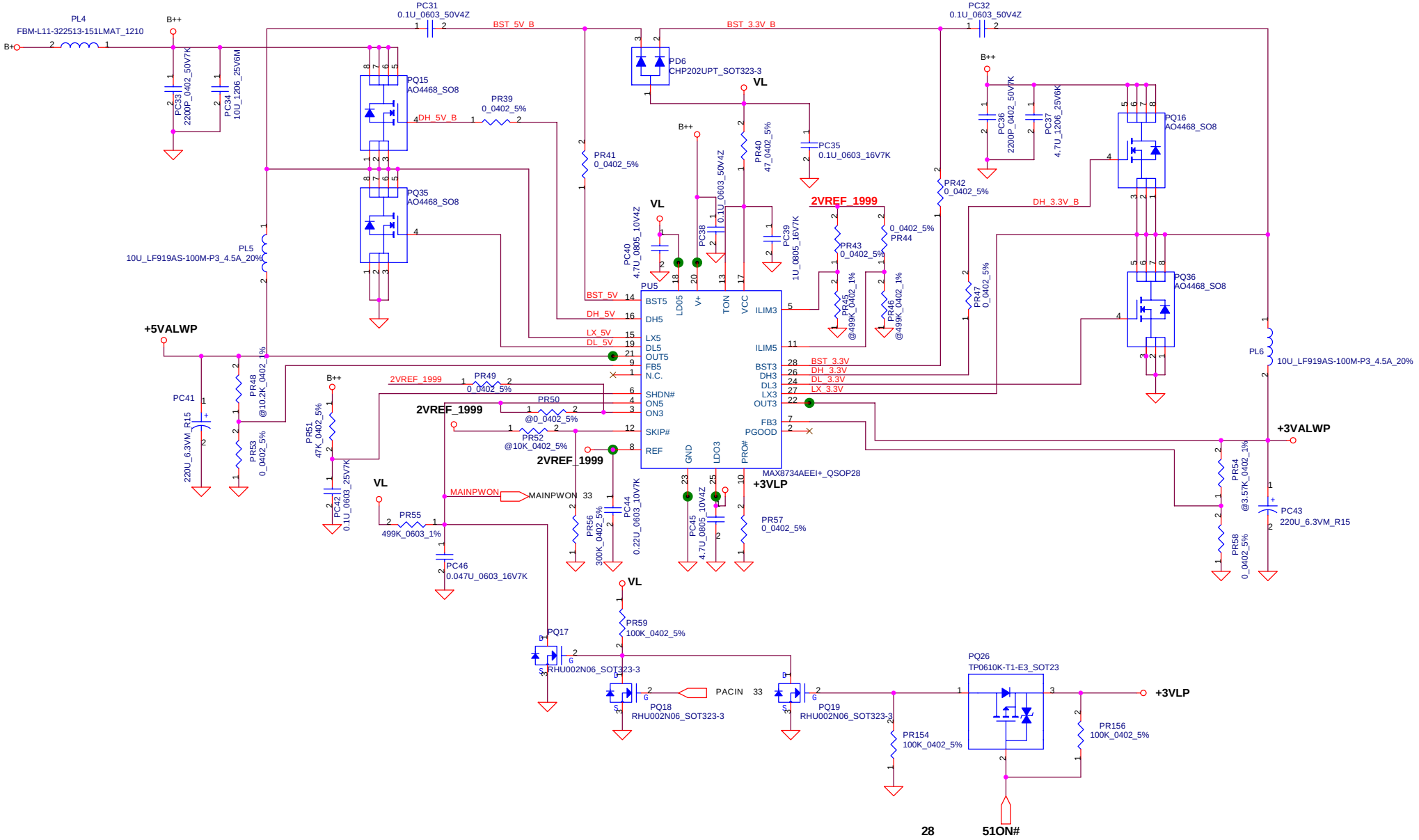
Size	Document Number	Rev
Custom	LA-3732P	

Date: Monday, July 09, 2007 Sheet 32 of 40



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.		
Title: Charger		
Size: Custom	Document Number	Rev
Date: Monday, July 09, 2007	Sheet 33 of 40	



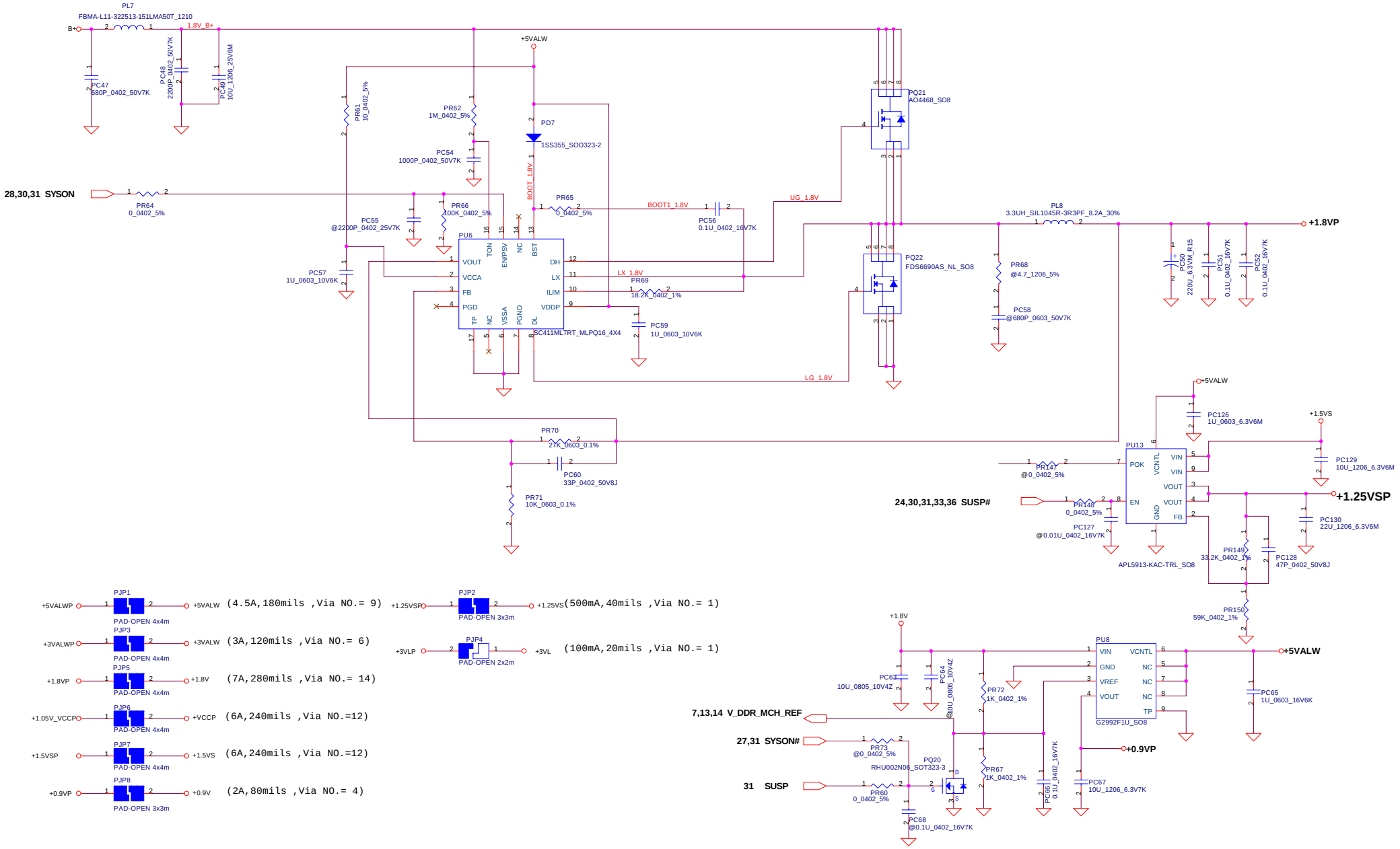
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **3.3VALWP / 5VALWP**

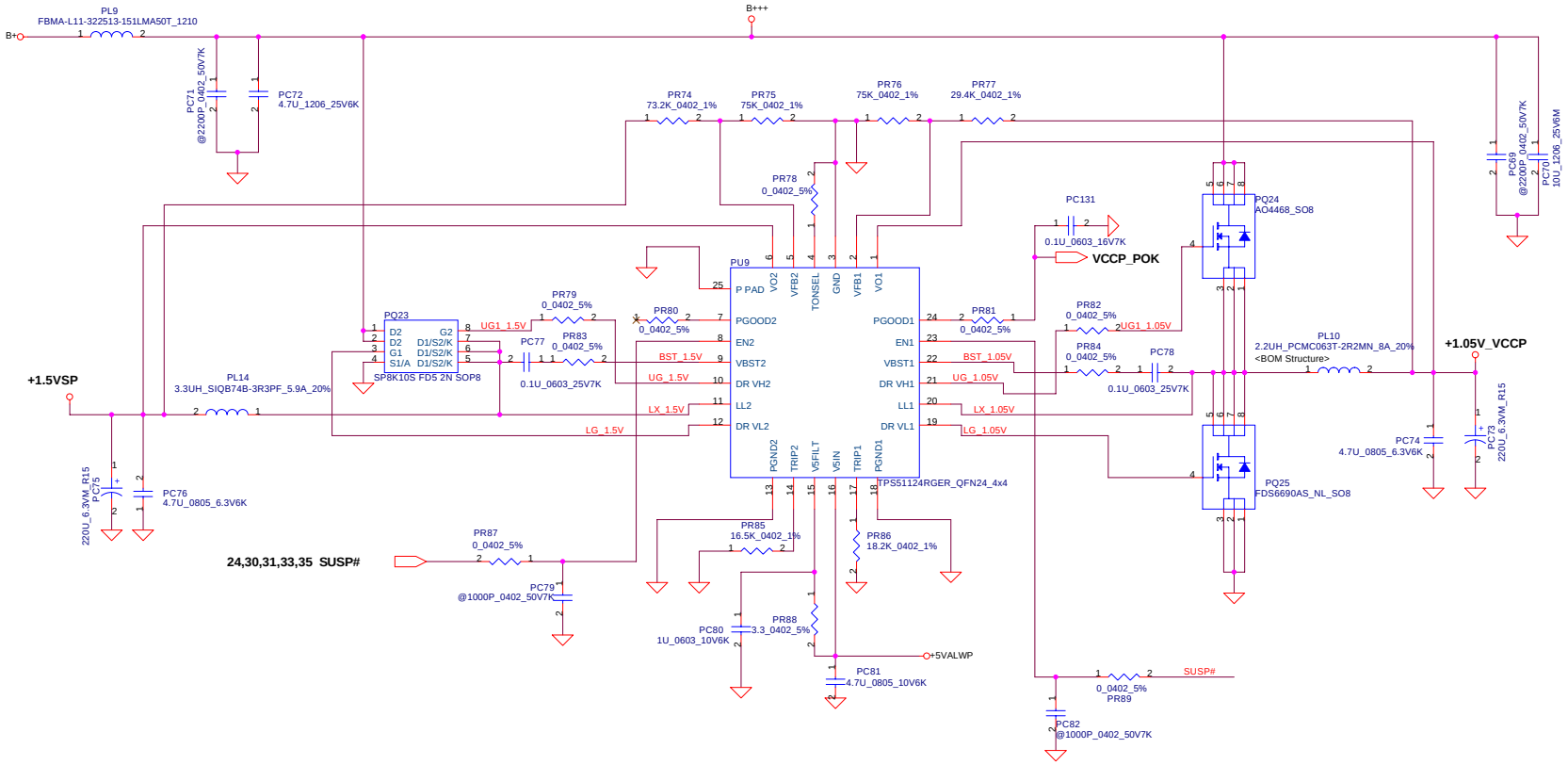
Size	Document Number	Rev

Date: Monday, July 09, 2007 Sheet 34 of 40



Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.			
Title	1.8VP/0.9VSP/2.5VSP		
Size	Document Number		Rev
	LA-3732P		0.2
Date:	Monday, July 09, 2007	Sheet	35 of 40



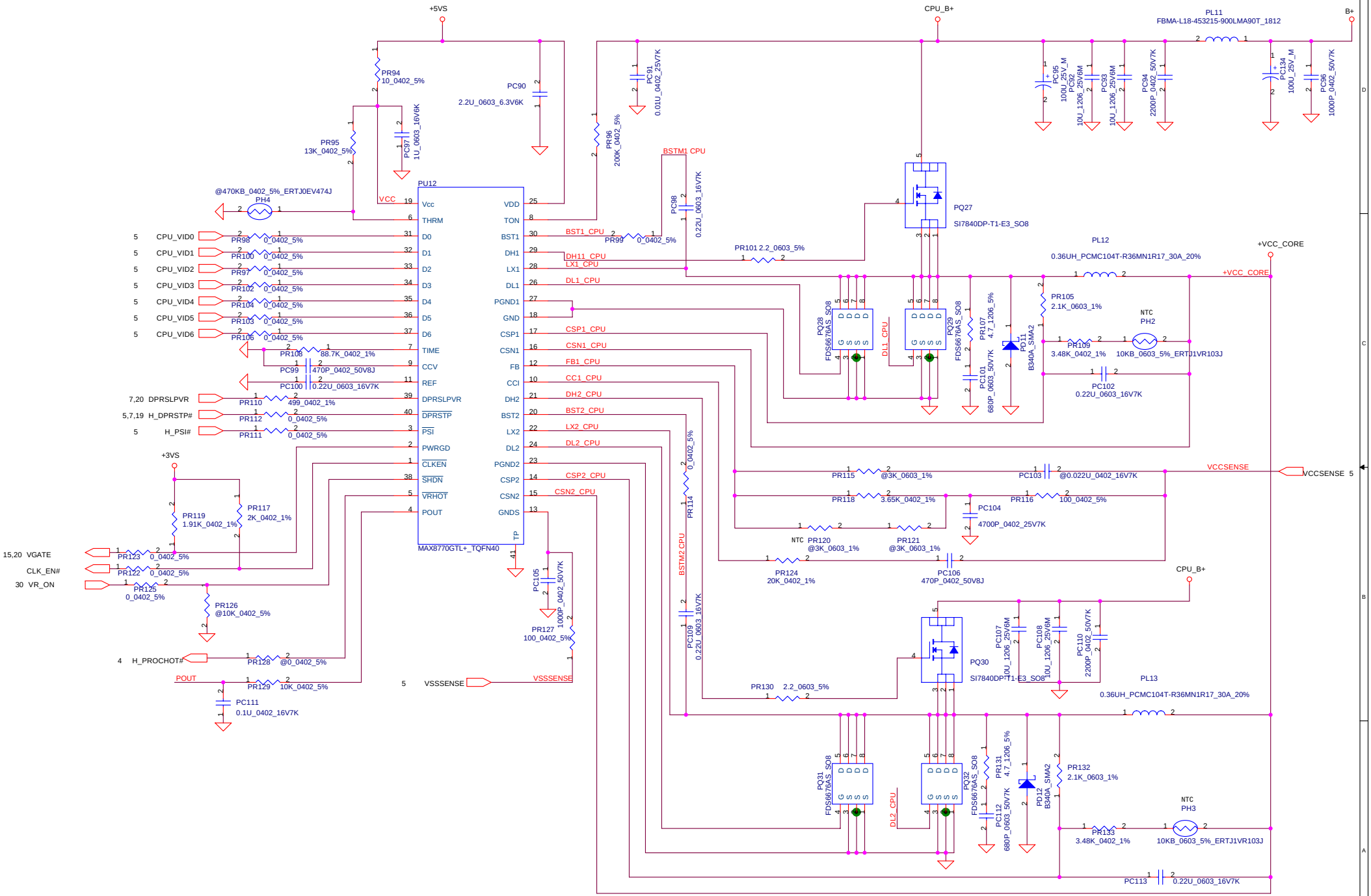
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **1.2V_VP/1.5VSP/1.05VP**

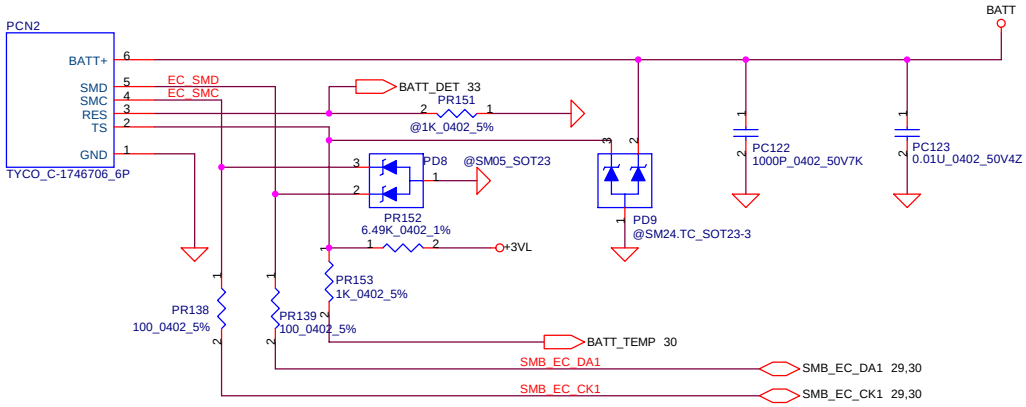
Size	Document Number	Rev
	LA-3732P	0.2

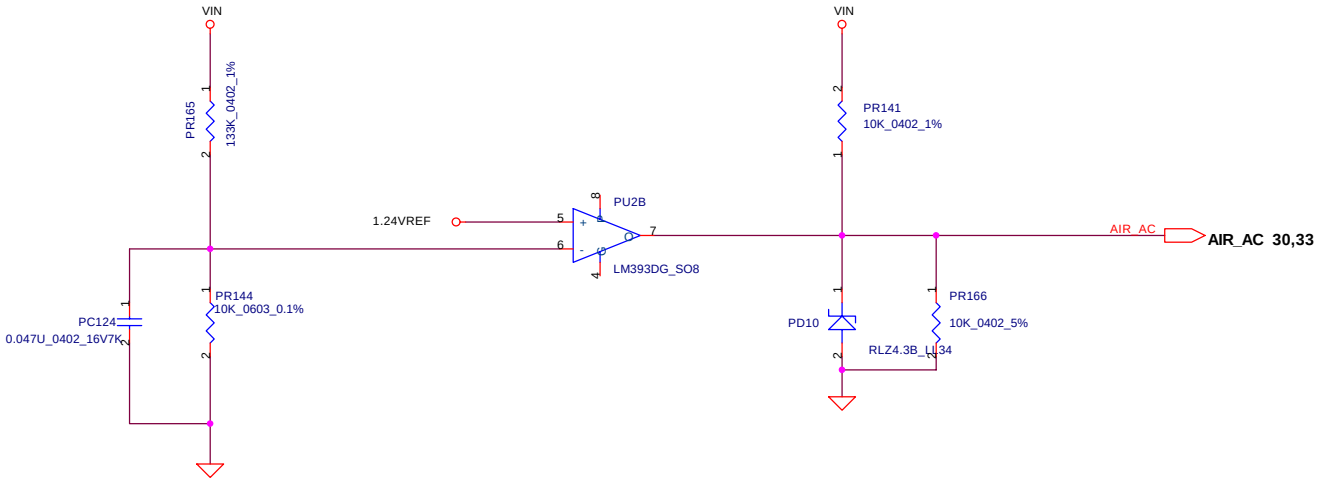
Date: Monday, July 09, 2007 | Sheet 36 of 40



Compal Electronics, Inc.

Title	+CPU_CORE	
Size	Document Number	Rev
Custom		0.2
Date: Monday, July 09, 2007	Sheet 37 of 40	





Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: *LA-3732P* | Rev:

Date: Monday, July 09, 2007 | Sheet 40 of 38

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW request.	35	Modify 1.25VSP enable signal from SLP_S3# to SUSP#.	2/13	
2	Change PR152 from 210K to 6.49K	38	Change PR152 from 210K to 6.49K	2/13	
3	Follow Volga 2.0 design.	37	Delete PC118,PC119,PC120,PC121,PR113,PR134.	3/6	
4	For layout concern.	37	Change PC95 location behind PL11.	3/8	
5	Prevent S3 leakage issue.	33	Change PD3 pin 2 connect from EC_ON to SUSP#	3/9	
6	Prevent LMV431 will oscillate.	33	Change PR30 from 75K to 51K.	3/9	
7	Prevent LMV431 will oscillate.	33	Change PC28 from 0.022u to 22P.	3/9	
8	EMI request add CPU core snabber and gate driver use 2.2_0603	34	Change PR101&PR130 from 0_0402 to 2.2_0603	3/12	
9	Modify DC in jack LED design for energy star.	35	Add PQ105.	3/12	
10	DFx request change PL1 type.	36	Change PL1 material type.	4/25	
11	Add Air line adapter circuit.	38		4/26	
12	Change CPU high side and add Schotty for EMI	37		6/7	
13	Remove PL15.	38	Remove PL15.	6/7	
14	Change PC22 from 1u_0603_6.3V to 0.1u_0402_10V	39		6/11	

Compal Electronics, Inc.
Title: Changed-List History-1
Size: Document Number: LA-3732P Rev: 0.2
Date: Monday, July 09, 2007 Sheet 39 of 40

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Change C117 from 220uF to 10uF.	10		2/8	DB --> SI
2	Remove R401.	19		2/5	DB --> SI
3	Change Crystal Y2 type (the same as Abita).	19		2/5	DB --> SI
4	Connect LAN_RST# from EC_RAMRST# to GND.	20		2/5	DB --> SI
5	Change ODD connector type.	22		2/13	DB --> SI
6	Change U11 power from +5VS to +5VALW.	24		2/12	DB --> SI
7	Change U11 enable signal from SLP_S3# to SUSP#.	24		2/8	DB --> SI
8	Reverse JP19 USB Connector and need to double check layout symbol.	27		2/12	DB --> SI
9	Change Power and Battery charge LED power from +3VALW to +5VALW.	28		2/8	DB --> SI
10	Change HDD LED power from +3VS to +5VS.	28		2/8	DB --> SI
11	Delete reserve component (D25 BSW2) for 14.1".	28		2/8	DB --> SI
12	Change R329, R333, R470 from 200 ohm to 470 ohm.	28		2/8	DB --> SI
13	Change R334, R339 from 200 ohm to 820 ohm.	28		2/8	DB --> SI
14	Add pull down resistor R402 (100k ohm) for SUSP#.	30		2/5	DB --> SI
15	Change C44, C49 type from DIP to SMD.	06		2/14	DB --> SI
16	Add R402 pull high resistor for LID_SW#.	30		2/14	DB --> SI
17	Add R403 pull high resistor for WL_BTN#.	30		2/14	DB --> SI
18	Delete D19.	28		2/16	DB --> SI
19	Change R300 from 10 ohm to 47 ohm and C374 from 10pF to 33pF.	24		2/16	DB --> SI
20	Delete JP27, R317, C392.	26		2/16	DB --> SI
21	Delete R297.	24		2/16	DB --> SI
22	Change RTC battery and connector.	19		2/26	DB --> SI
23	Change C413 and 414 package from 0603 to 0402.	28		2/26	DB --> SI
24	Add JP28 for USB card reader.	27		2/28	DB --> SI
25	Change R105 from 22 ohm to 0 ohm.	15		3/1	DB --> SI
26	Delete C49 and remount C46.	06		3/1	DB --> SI
27	Change JP16 and JP17 Audio Jack.	26		3/2	DB --> SI
28	Add R405.	04		3/6	DB --> SI
29	Change USB connector (JP19) type.	27		3/8	DB --> SI

Compal Electronics, Inc.

Title: HW Changed-List History-1

Size | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 40 of 42

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Connect R323.1 from B+ to +3VALW. (Cancel in 4/24)	26		4/9	SI --> PV
2	Add R406 between H_OUT_R and H_OUTR+, R407 between H_OUT_L and H_OUTL+	26		4/9	SI --> PV
3	Swap channel L and R.	26		4/9	SI --> PV
4	Add R408 and R409. (Cancel in 4/24)	26		4/9	SI --> PV
5	Reverse JP22 pin define.	28		4/10	SI --> PV
6	Change R360 from 10K to 4.7K ohm for KB926 C0 version.	31		4/10	SI --> PV
7	Reserve C438 for KB926 C0 version.	31		4/10	SI --> PV
8	Change C45~C48 to 9m ohm and reserve C49.	06		4/16	SI --> PV
9	Change R233 from 0 ohm to 10K ohm.	20		4/16	SI --> PV
10	Change R233 from 0 ohm to 10K ohm.	30		4/16	SI --> PV
11	Reverse JP15 pin define.	26		4/16	SI --> PV
12	Add pull high R410 (3.3K ohm) for HOLD#.	29		4/17	SI --> PV
13	Change R211 from 24.9 to 27.4 ohm.	19		4/17	SI --> PV
14	Add CP1~CP6 for EMI.	30		4/17	SI --> PV
15	Add R186 and C261 for EMI.	18		4/17	SI --> PV
16	Add R292 and C356 for EMI.	23		4/17	SI --> PV
17	Add D24 for EMI.	28		4/17	SI --> PV
18	Add C233, C234, C235 for EMI.	16		4/17	SI --> PV
19	Add R411 to pull high for WL_LED#.	22		4/17	SI --> PV
20	Remove XDP circuit for EMI request. Change R2 to 15 ohm R3 to 39 ohm R7 to 560 ohm R8 to 27 ohm	04		4/17	SI --> PV
21	Change R223 from 1K to 10K ohm when remove XDP.	20		4/17	SI --> PV
22	Add reserve resistor R412 for LPC debug port.	15		4/17	SI --> PV
23	Add C439 to avoid wavelike display.	10		4/20	SI --> PV
24	Change C262 and C263 from 15pF to 12pF.	19		4/23	SI --> PV
25	Per ENE request, change C426 and C427 from 10pF to 27pF from now.	30		4/23	SI --> PV
26	Reserve R300 and C374 for EMI request.	24		4/24	SI --> PV
27	Add C440 for AC_IN.	31		4/24	SI --> PV
28	Change R355 from 8.2K to 18K ohm.	31		4/25	SI --> PV
29	Add L16~19 for EMI request.	26		4/25	SI --> PV
30	Change C336~C338 from 22p to 10pF.	16		4/25	SI --> PV
31	Add R415 and R416 for thermal second solution.	04		4/25	SI --> PV
32	Change R320 from 0 ohm to bead. Add L20.	26		4/25	SI --> PV
33	Change R321 and R322 from 0 ohm to bead. Add C398 and C399.	26		4/25	SI --> PV
34	Add C401 and C404.	26		4/25	SI --> PV
35	Connect AIR_AC to U18 pin85 to support AIR adapter.	31		4/26	SI --> PV
36	Add C441.	15		4/26	SI --> PV
37	Add R417 and R418 to fine tune Headphone output voltage	26		4/26	SI --> PV
38	Delete R219 and C268 for EMI request.	20		4/26	SI --> PV

Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2007/02/28

Compal Electronics, Inc.

Title: **HW Changed-List History-1**

Size	Document Number	Rev
	LA-3732P	1.0

Date: Monday, July 09, 2007 Sheet 41 of 42

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Change C7, C71, C131, C137, C156 from 330uF to 220uF.	5, 10, 11, 13		6/7	PV --> MV
2	Change C45~C48 from 330uF/9m to 220uF/9m.	6		6/1	PV --> MV
3	Add C443 and C444 to replace C164 and C165, to solve interfere with DDR module.	13		6/5	PV --> MV
4	Add C442 for +3VL.	19		6/1	PV --> MV
5	Change C284 from 0.1uF to 1uF to meet intel guildline.	21		5/29	PV --> MV
6	Add C445 (1uF) for +RTCVCC.	21		6/6	PV --> MV
7	Add L21 and L22 for EMI request.	23		6/1	PV --> MV
8	Mount C357 and C358 for EMI request.	23		6/1	PV --> MV
9	Change R355 from 18K to 33K ohm.	30		6/5	PV --> MV
10	Change R302 from 0 ohm to 620 ohm. Add R306 with 143 ohm. Change C373 from 1uF to 0.01uF.	24		6/8	PV --> MV
11	Add D27 and D28 for EMI request.	23		6/11	PV --> MV

Compal Electronics, Inc.

Title: HW Changed-List History-1

Size | Document Number: LA-3732P | Rev: 1.0

Date: Monday, July 09, 2007 | Sheet 42 of 42