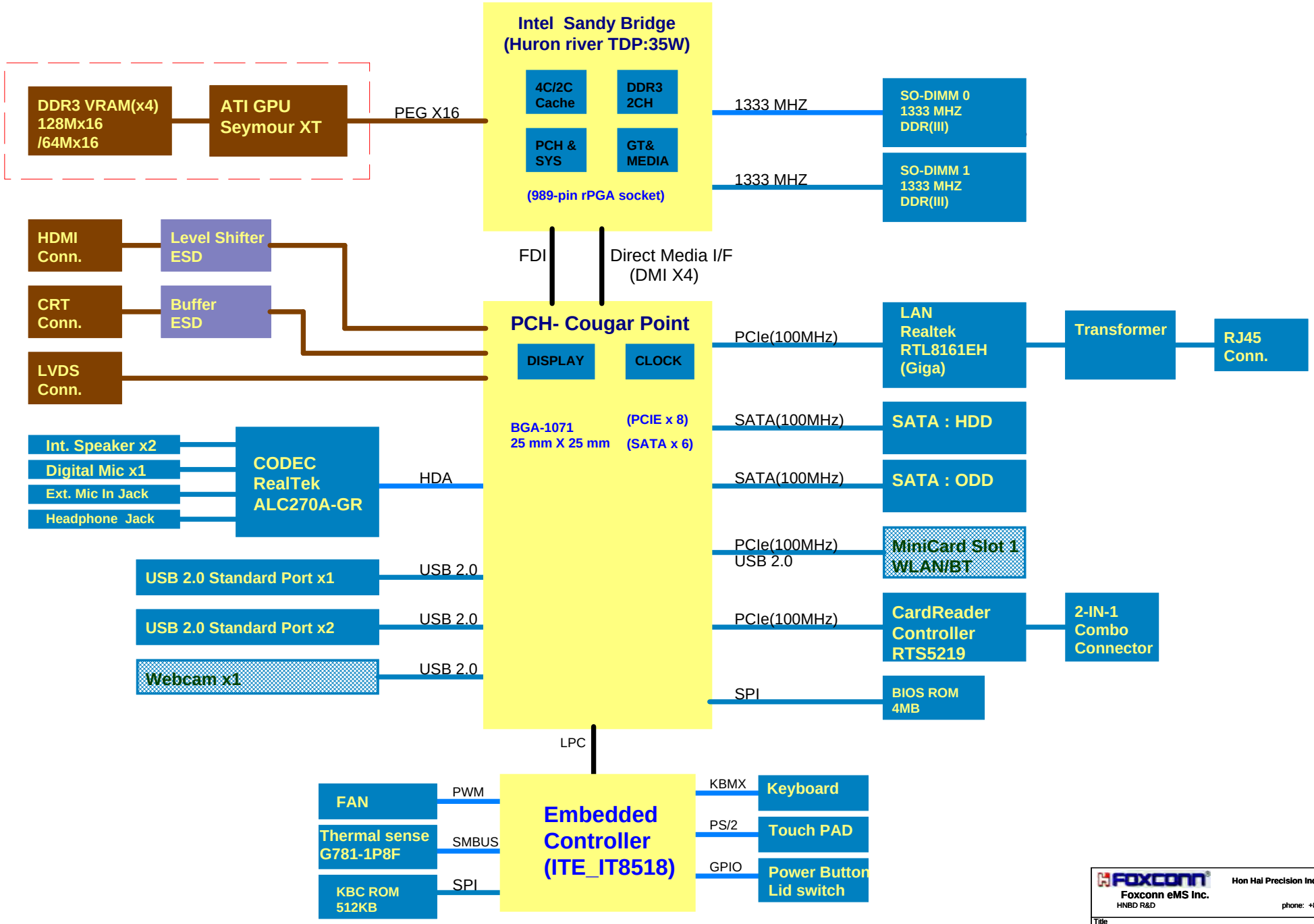

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Title: SYSTEM BLOCK DIAGRAM

Size	Document Number	Rev
Custom	CHICAGO	

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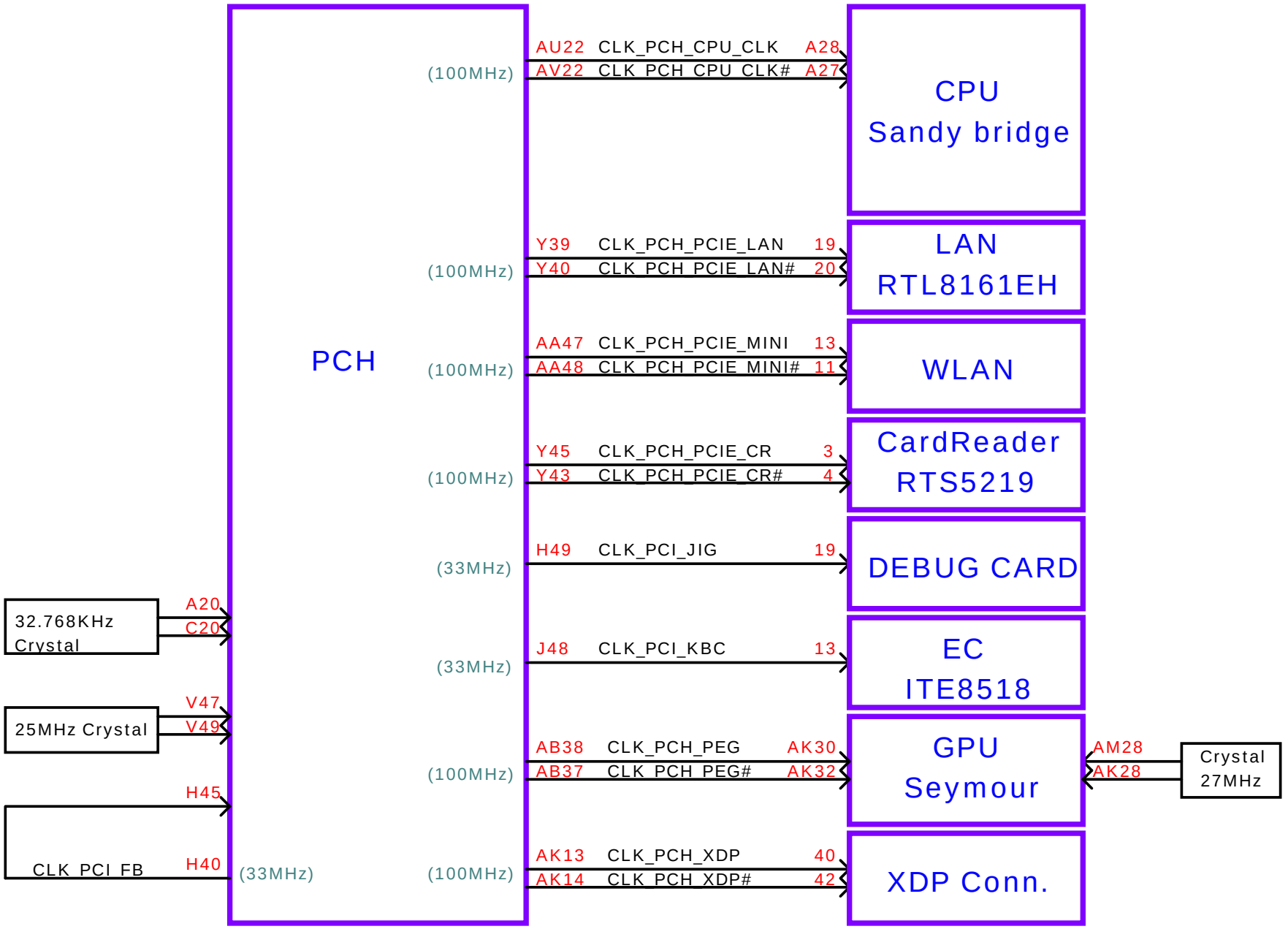

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Title: CLOCK MAP

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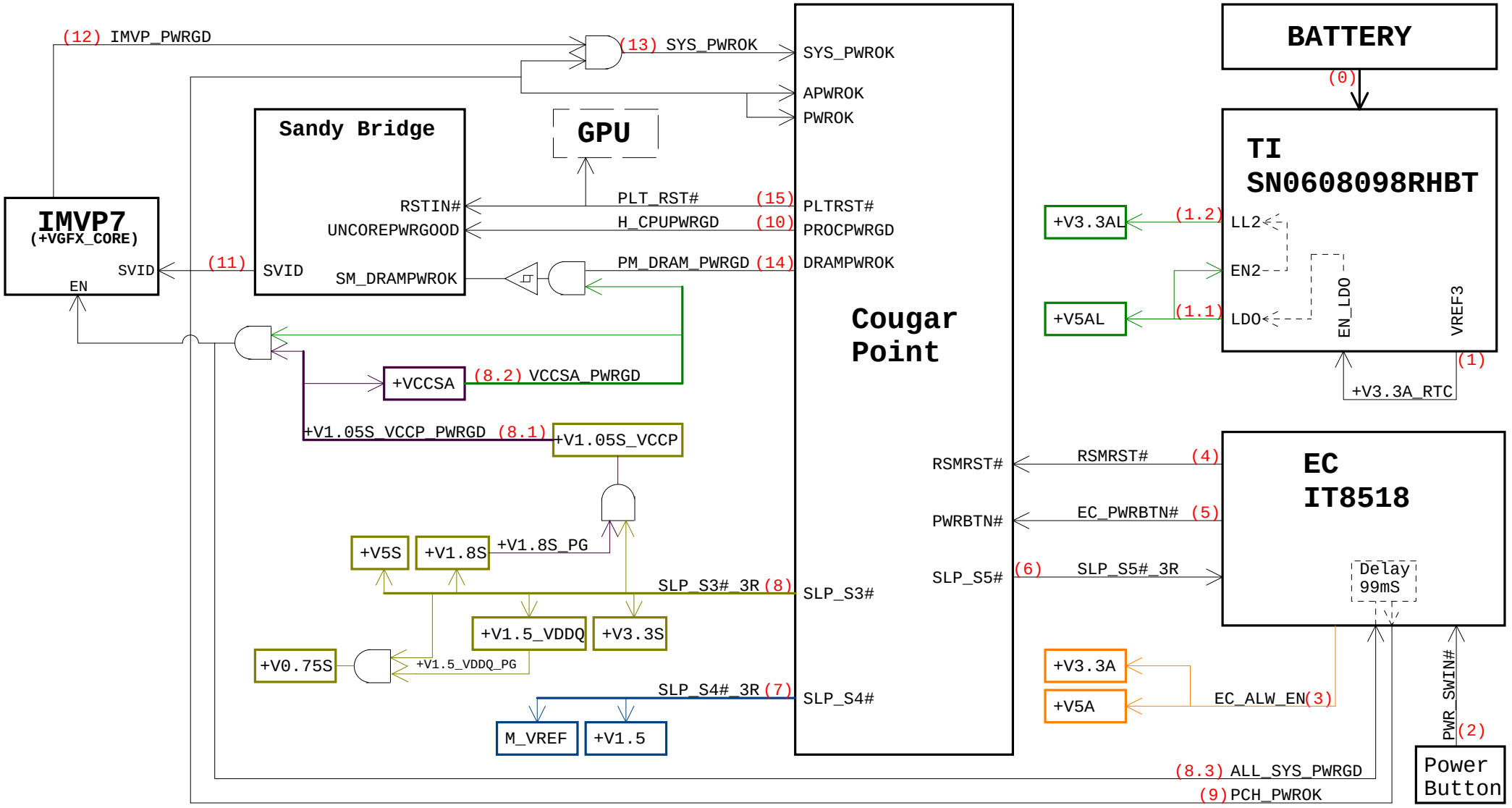

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Title: POWER SEQUENCY DIAGRAM

Size	Document Number	Rev
Custom	CHICAGO	MV

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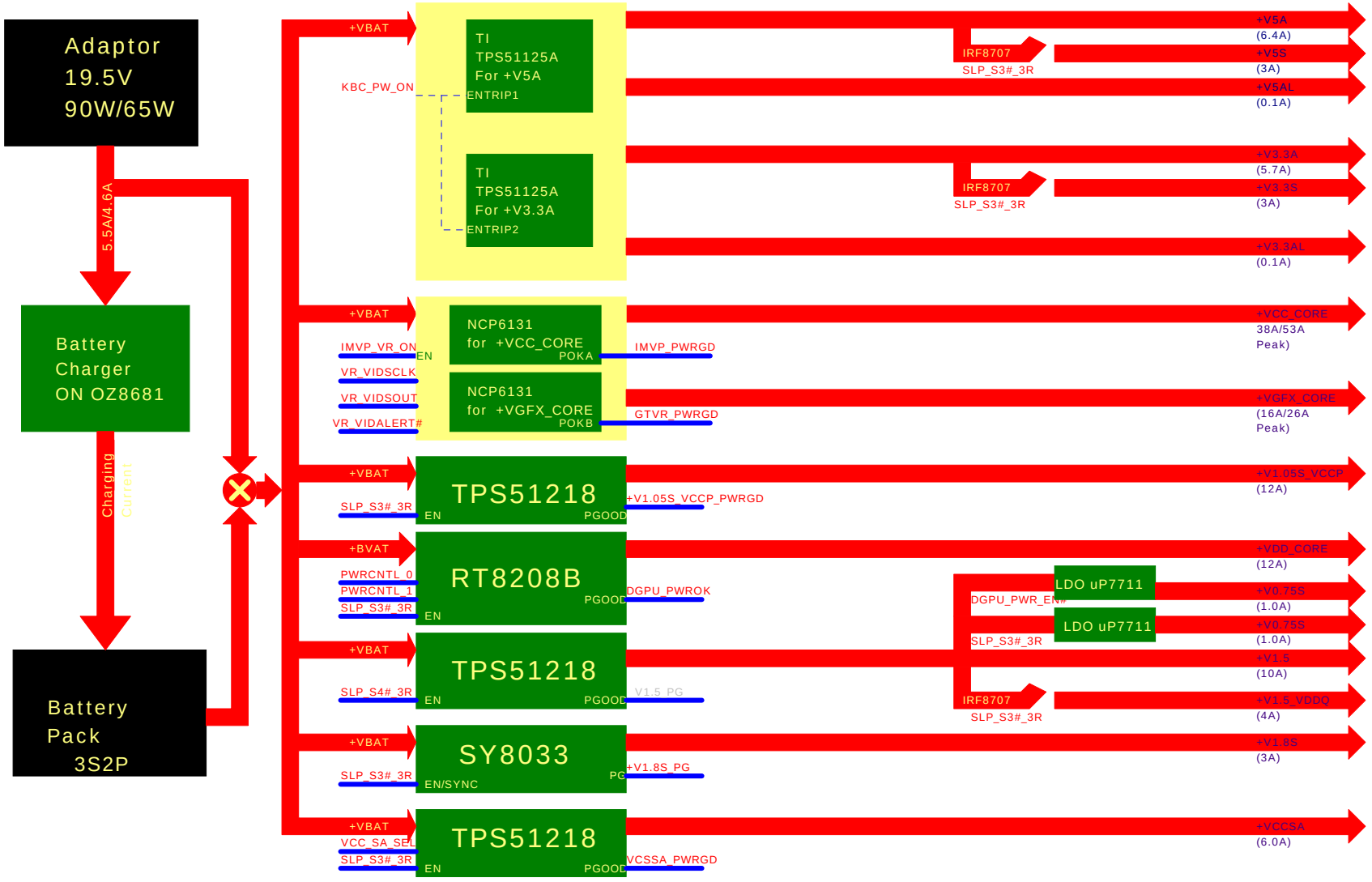
POWER MAP



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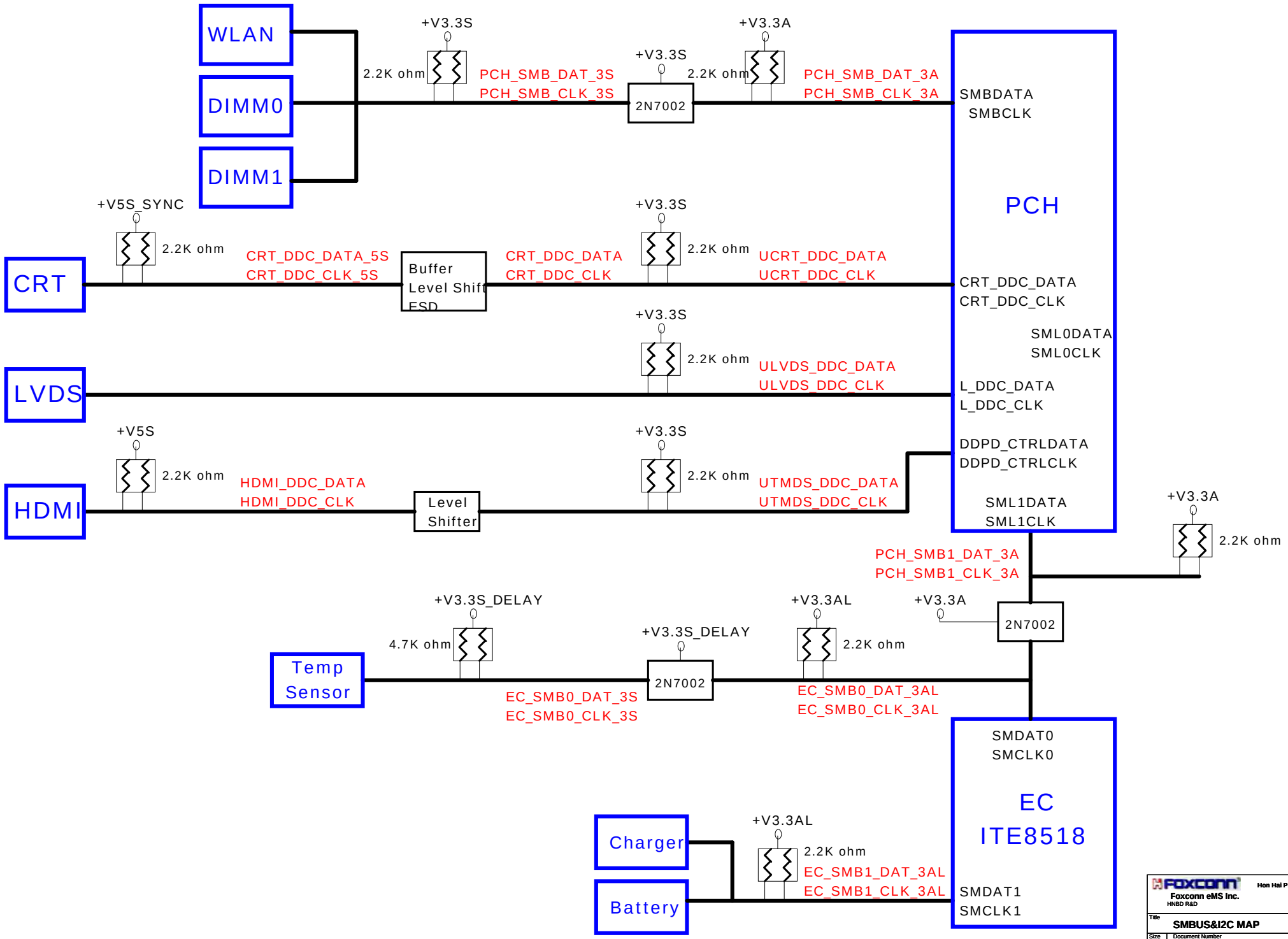
Title		
POWER MAP		
Size: C	Document Number: CHICAGO	Rev: MV
Page Modified: Tuesday, March 08, 2011 08:28:57 (UTC/GMT)		Sheet 5 of 43



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Title: SMBUS&I2C MAP

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Title: BLANK	
Size: A	Document Number: CHICAGO — Rev: MV
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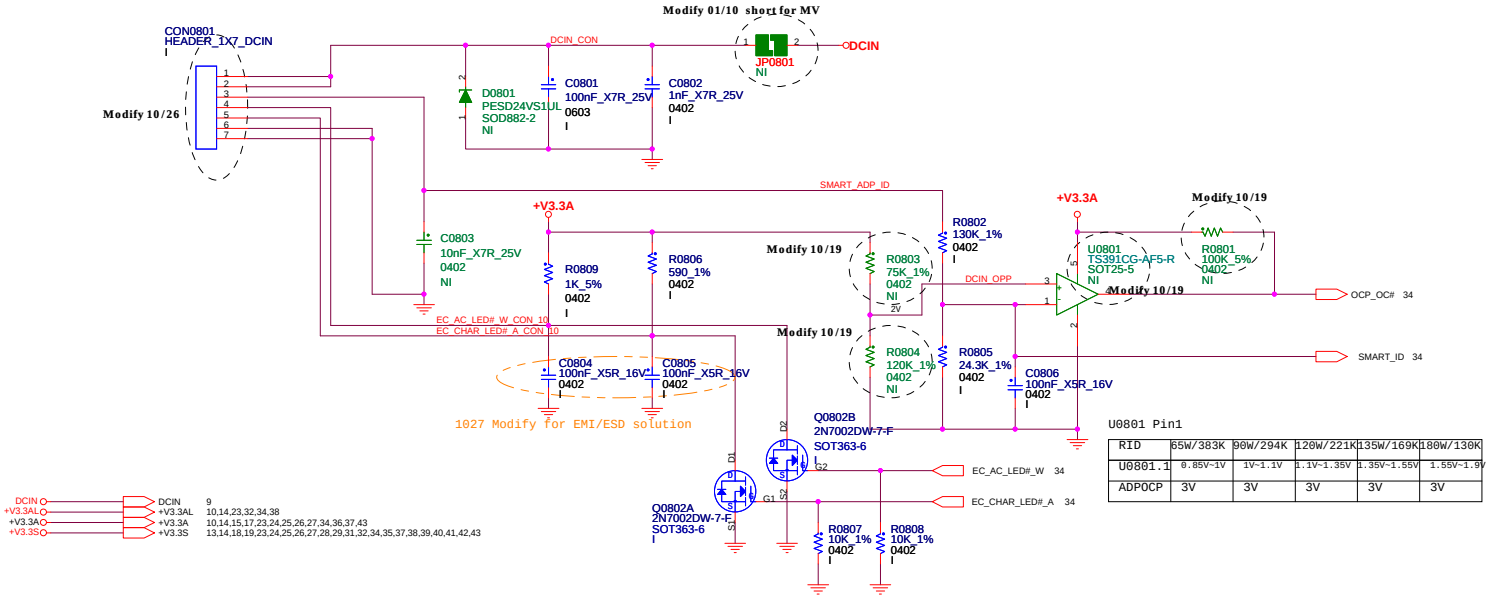
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

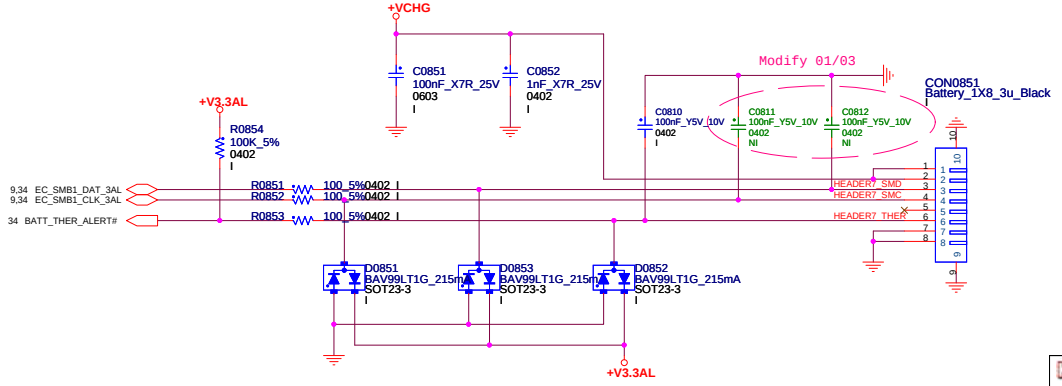


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.85V~1V	1V~1.1V	1.1V~1.35V	1.35V~1.55V	1.55V~1.9V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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Title: DCIN/BATTERY

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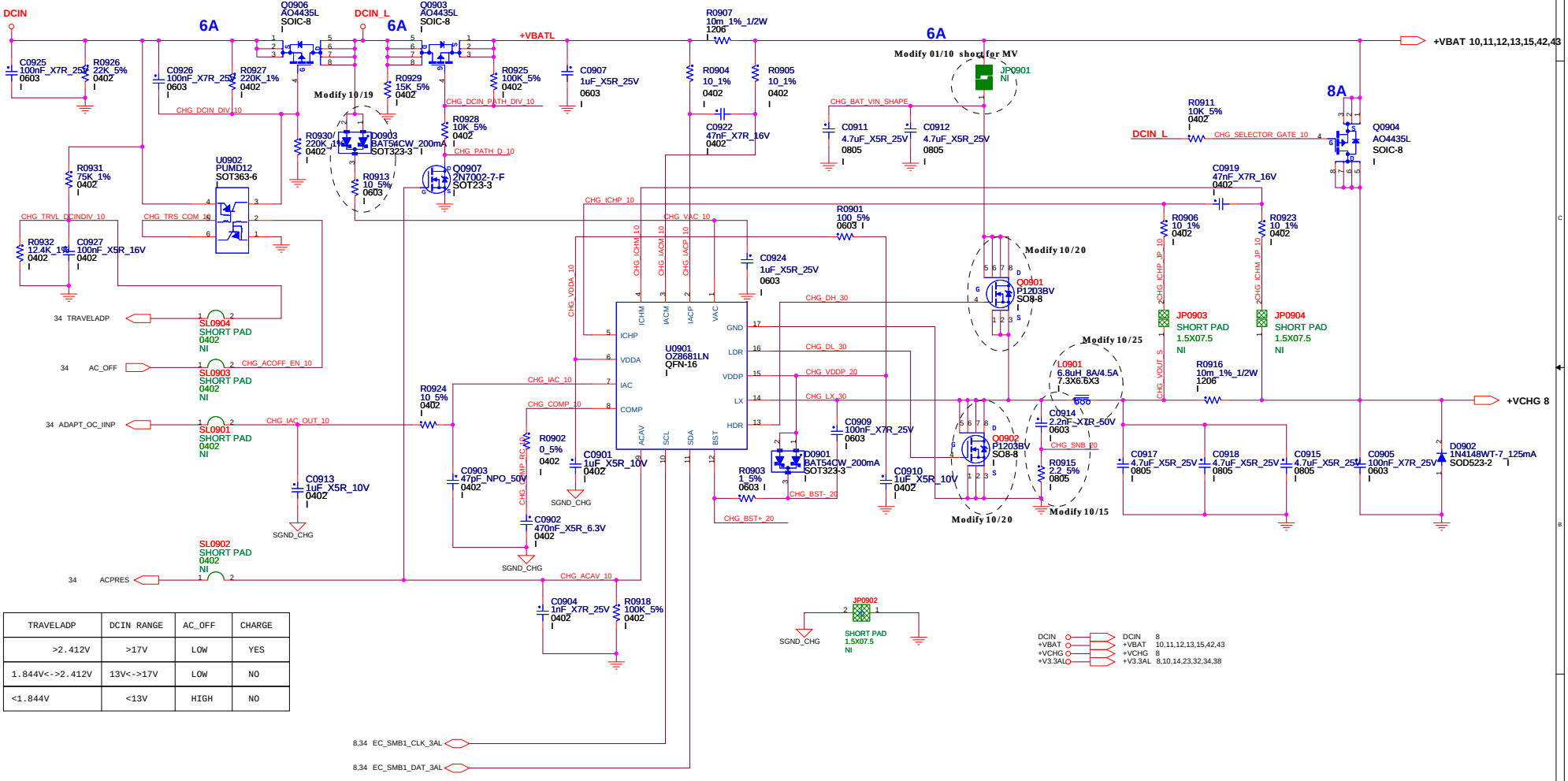
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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Title: PWR_Charger

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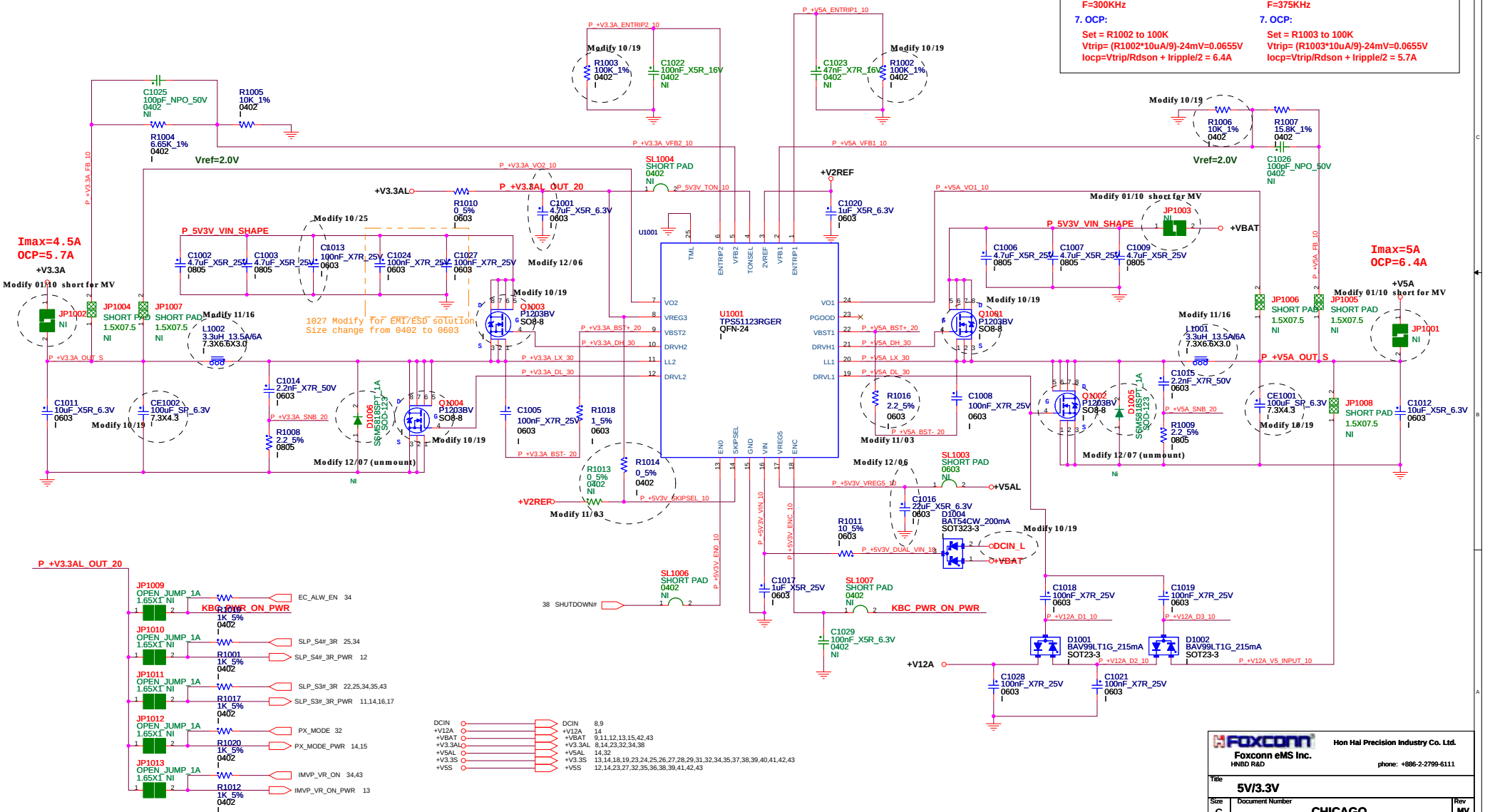
+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current:	1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=3.7A	Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:	2.Ripple Current:
Irip=3.72A	Irip=2.21A
3. Ripple Voltage:	3.Ripple Voltage:
ESR/1=15mohm	ESR/1=15mohm
Vrip=55.8mV	Vrip=33.15mV
4. Inductor Spec:	4.Inductor Spec:
Isat=13.5A	Isat=13.5A
Idc=6A	Idc=6A
DCR=30mohm	DCR=30mohm
5.MOSFET Spec:	
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)
6. Frequency:	6. Frequency:
F=300KHz	F=375KHz
7. OCP:	7. OCP:
Set = R1002 to 100K	Set = R1003 to 100K
Vtrip= (R1002*10uA/9)-24mV=0.0655V	Vtrip= (R1003*10uA/9)-24mV=0.0655V
Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



DCIN	DCIN	8,9
+V12A	+V12A	14
+VBAT	+VBAT	9,11,12,13,15,42,43
+V3.3AL	+V3.3AL	8,14,23,32,34,38
+V5AL	+V5AL	14,32
+V3.3S	+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V5S	+V5S	12,14,23,27,32,35,36,38,39,41,42,43

JP1009	EC_ALW_EN	34
JP1010	SLP_S4#_3R	25,34
	SLP_S4#_3R_PWR	12
JP1011	SLP_S3#_3R	22,25,34,35,43
	SLP_S3#_3R_PWR	11,14,16,17
JP1012	PX_MODE	32
	PX_MODE_PWR	14,15
JP1013	IMVP_VR_ON	34,43
	IMVP_VR_ON_PWR	13

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Title	5V/3.3V
Size C	Document Number CHICAGO
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+VTT POWER SUPPLY

2010.1103.0

+V1.05S_VCCP:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.24A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

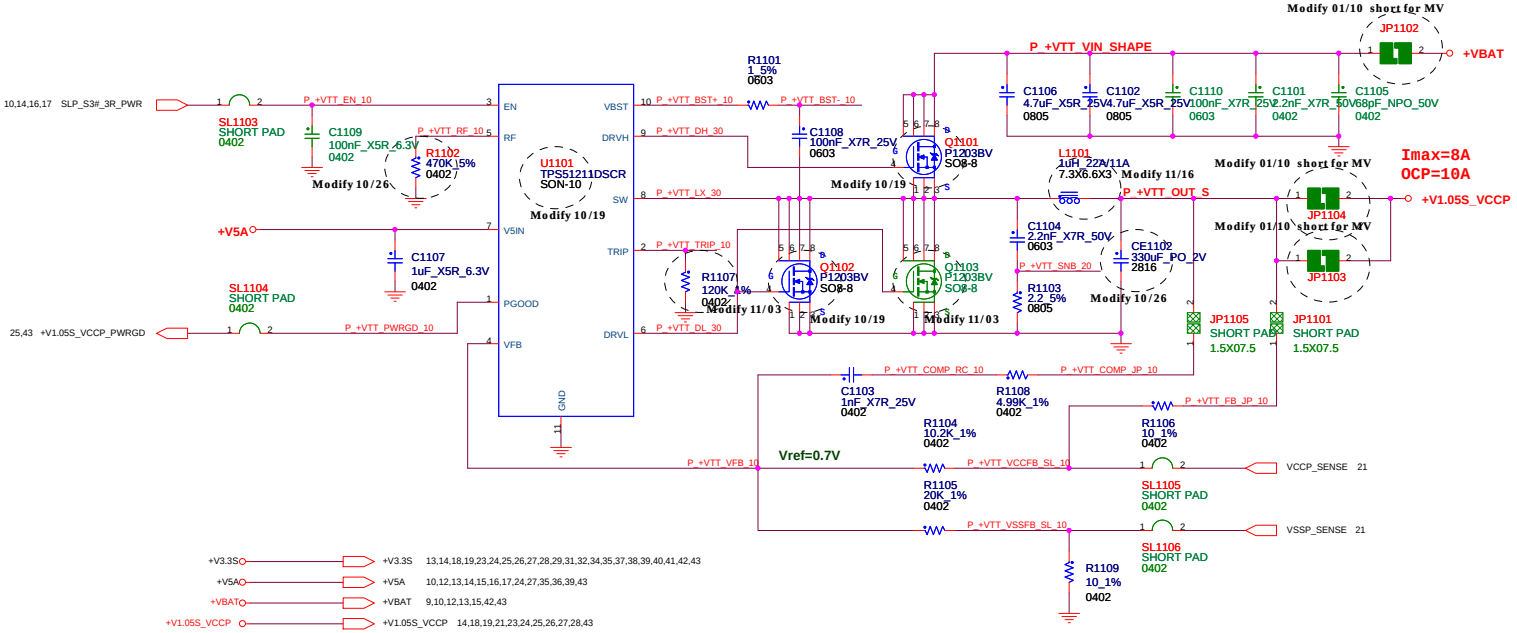
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:

F=290KHz (R1102=0ohm)

7. OCP:

Set = R1107 to 120K
Vtrip= R1107*10uA=1.2V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A



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Title: +VTT		
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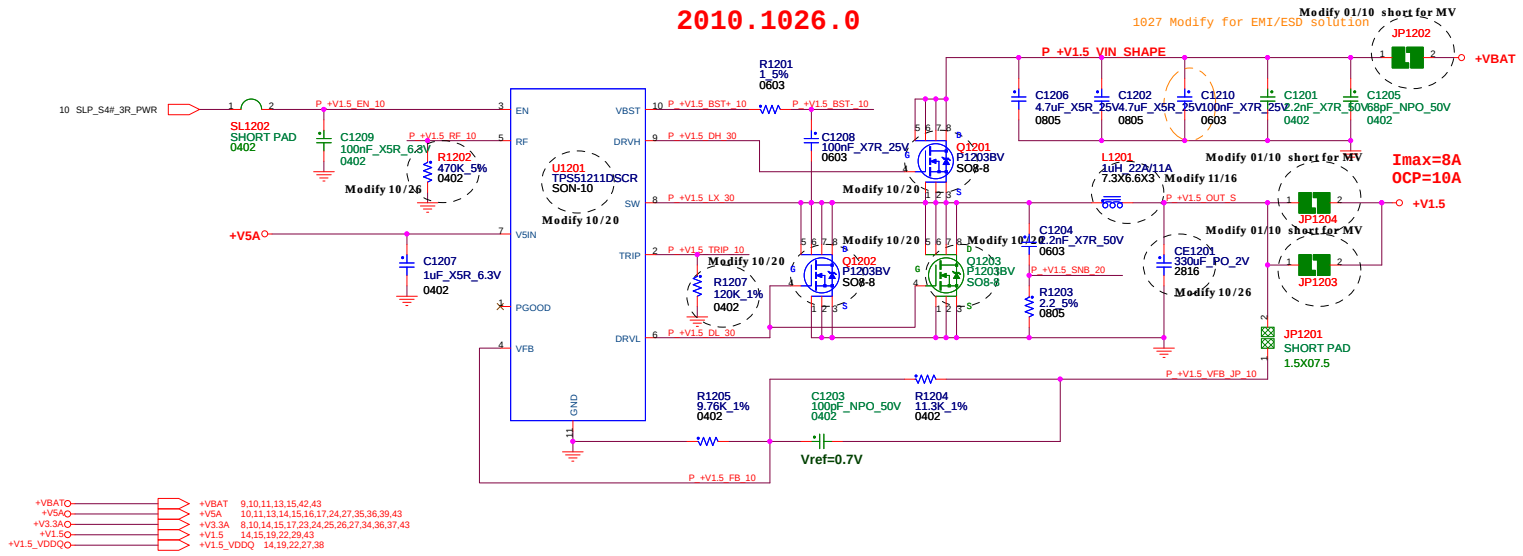
+V1.5 POWER SUPPLY

2010.1026.0



+V1.5:

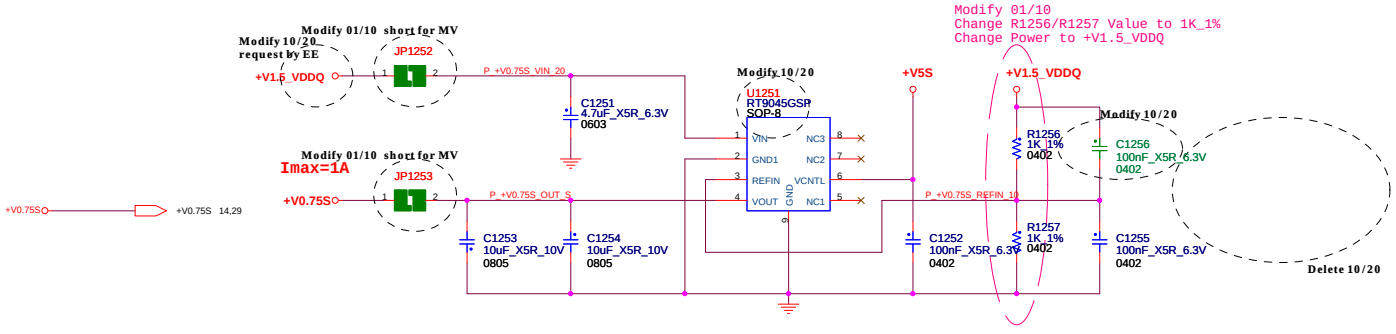
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
   Irip=3.34A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.6mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:
   F=290KHz (R0902=0ohm)
7. OCP:
   Set = R1207 to 120K
   Vtrip= R1207*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

+V0.75S POWER SUPPLY

2010.1026.0



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Title	1.5VDDR3/0.75V
Size: C	Document Number: CHICAGO
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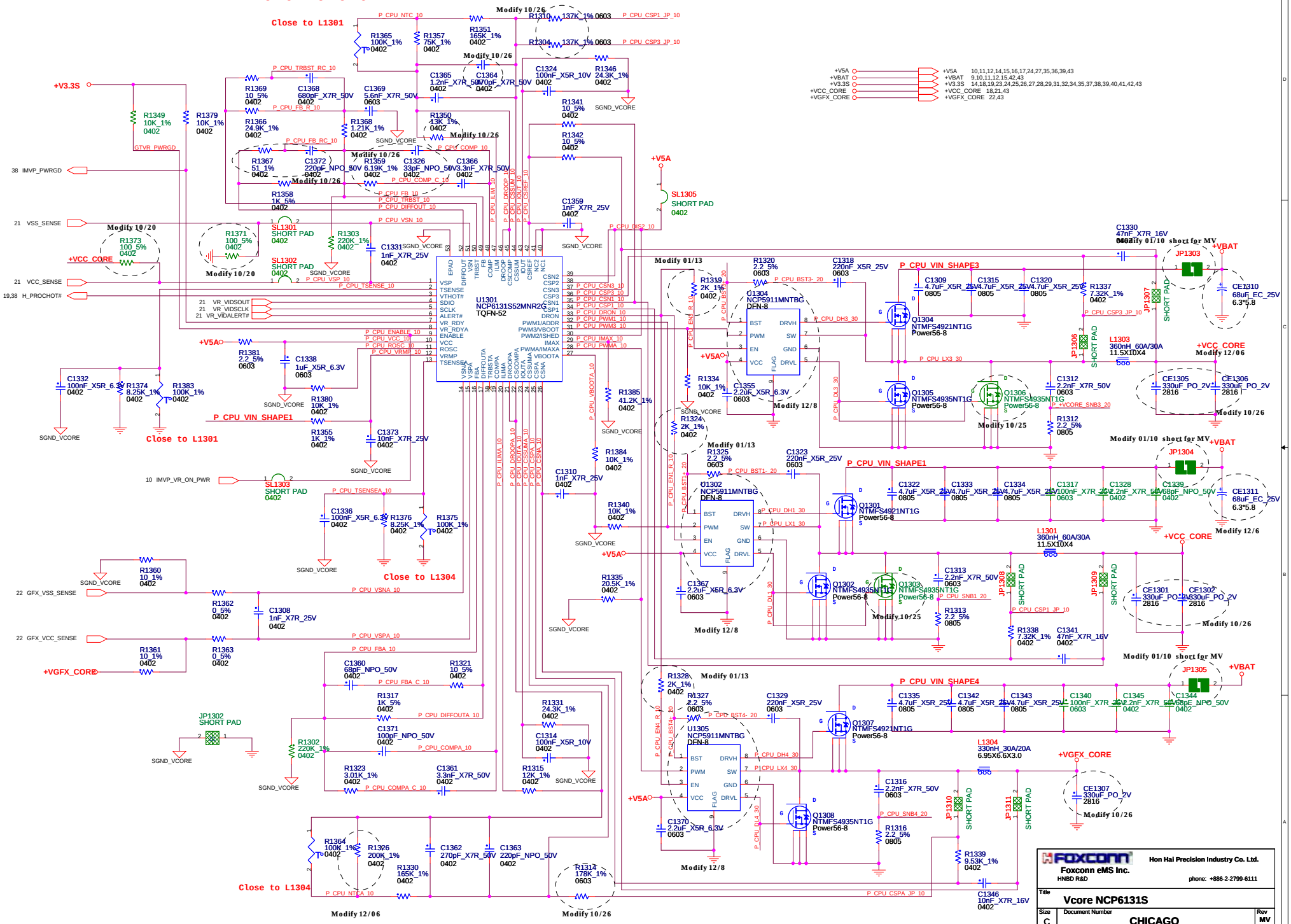
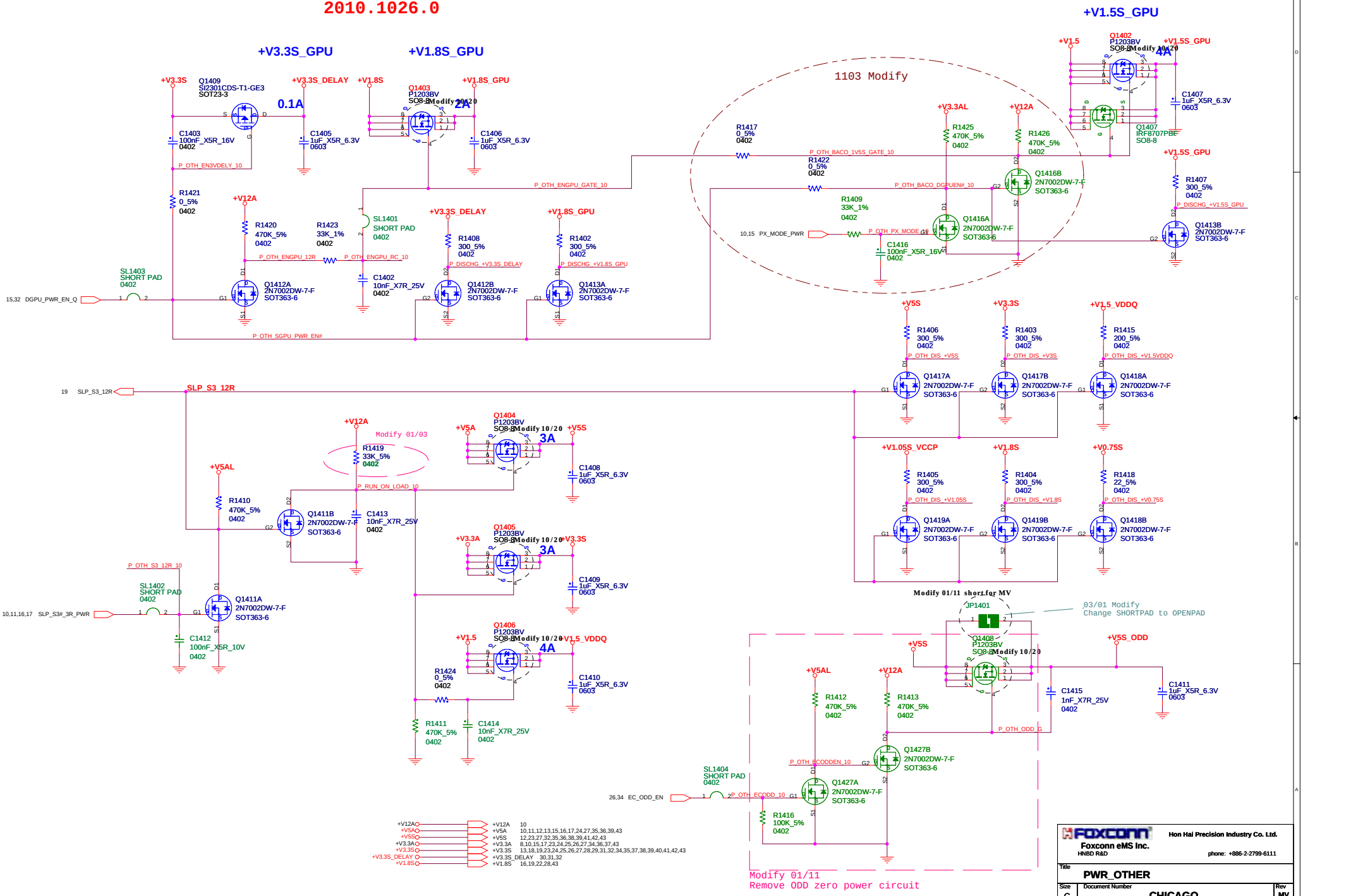
IMVP7 CPU VCORE POWER SUPPLY

2010.1026.0



OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



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Title: PWR_OTHER

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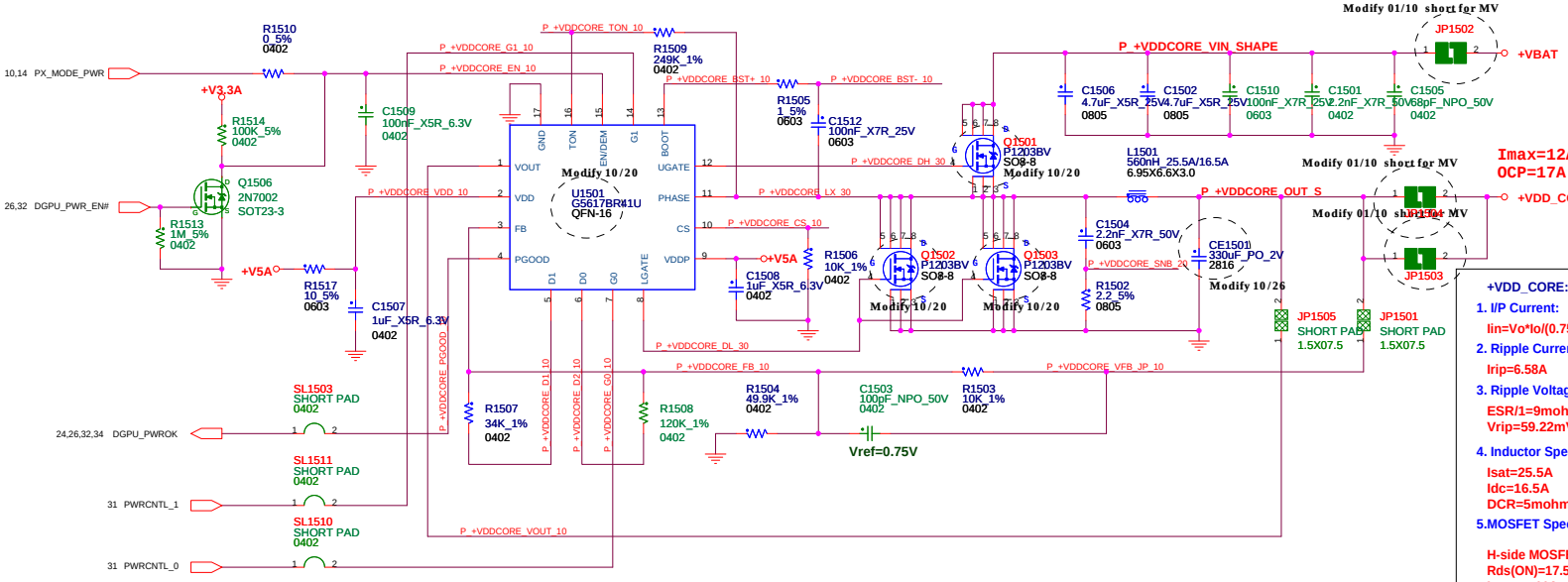
+VDD_CORE POWER SUPPLY

2010.1026.0



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.48A

2. Ripple Current:

Irip=6.58A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=59.22mV

4. Inductor Spec:

Isat=25.5A
Idc=16.5A
DCR=5mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF		L-side MOSFET: IRF8707PBF	
Rds(ON)=17.5mohm (Vgs=4.5 V)		Rds(ON)=17.5mohm (Vgs=4.5 V)	
I cont = 11A	(T =25 ℃)	I cont = 11A	(T =25 ℃)
I peak = 88A	(Pause =10 us)	I peak = 88A	(Pause =10 us)

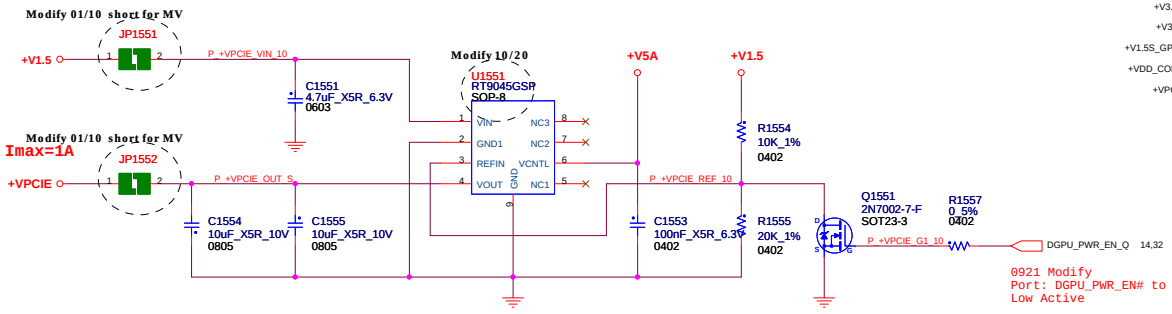
6. Frequency:

TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns
F=VOUT/(VIN*TON)=286KHz

7. OCP:

Set = R1506 to 10K
Vtrip= R1206*10uA=0.1V
Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY



0921 Modify
Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
Low Active

+VBAT	+VBAT	9,10,11,12,13,42,43
+V5A	+V5A	10,11,12,13,14,16,17,24,27,35,36,39,43
+V3.3A	+V3.3A	8,10,14,17,23,24,25,26,27,34,36,37,43
+V3.3S	+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.5S_GPU	+V1.5S_GPU	14,30,32,33,43
+VDD_CORE	+VDD_CORE	32,43
+VPCIE	+VPCIE	30,31,32,43

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Title: VATVDD/+VPCIE

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+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.44A

2. Ripple Current:

Irip=0.53A

3. Ripple Voltage:

ESR/3=3.3mohm
Vrip=1.75mV

4. Inductor Spec:

Isat=14A
Idc=8A
DCR=20mohm

5.MOSFET Spec:

H-side P-MOSFET: Rds(ON)=110mohm (Vgs=4.5 V)

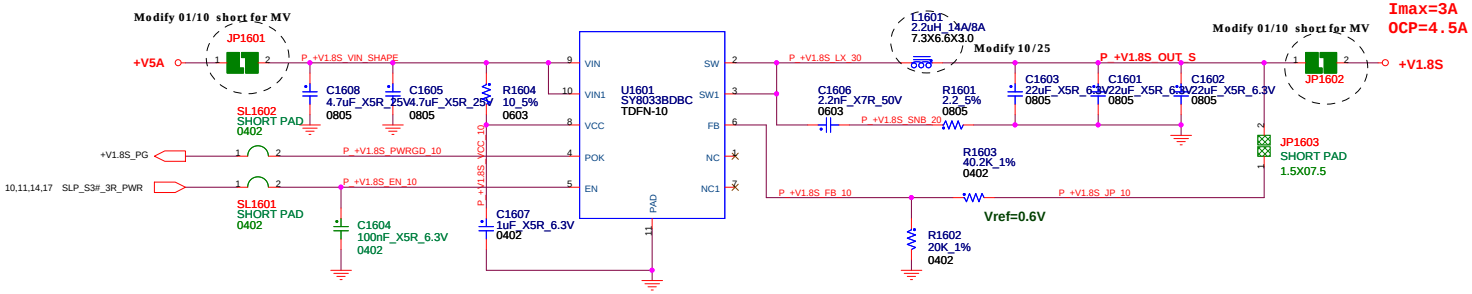
L-side N-MOSFET: Rds(ON)=75mohm (Vgs=4.5 V)

6. Frequency:

F=1MHz (min=800KHz, max=1.2MHz)

7. OCP:

Iocp=4A(min)/4.5A(typ)/5A(max)



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Title: +1.8VS		
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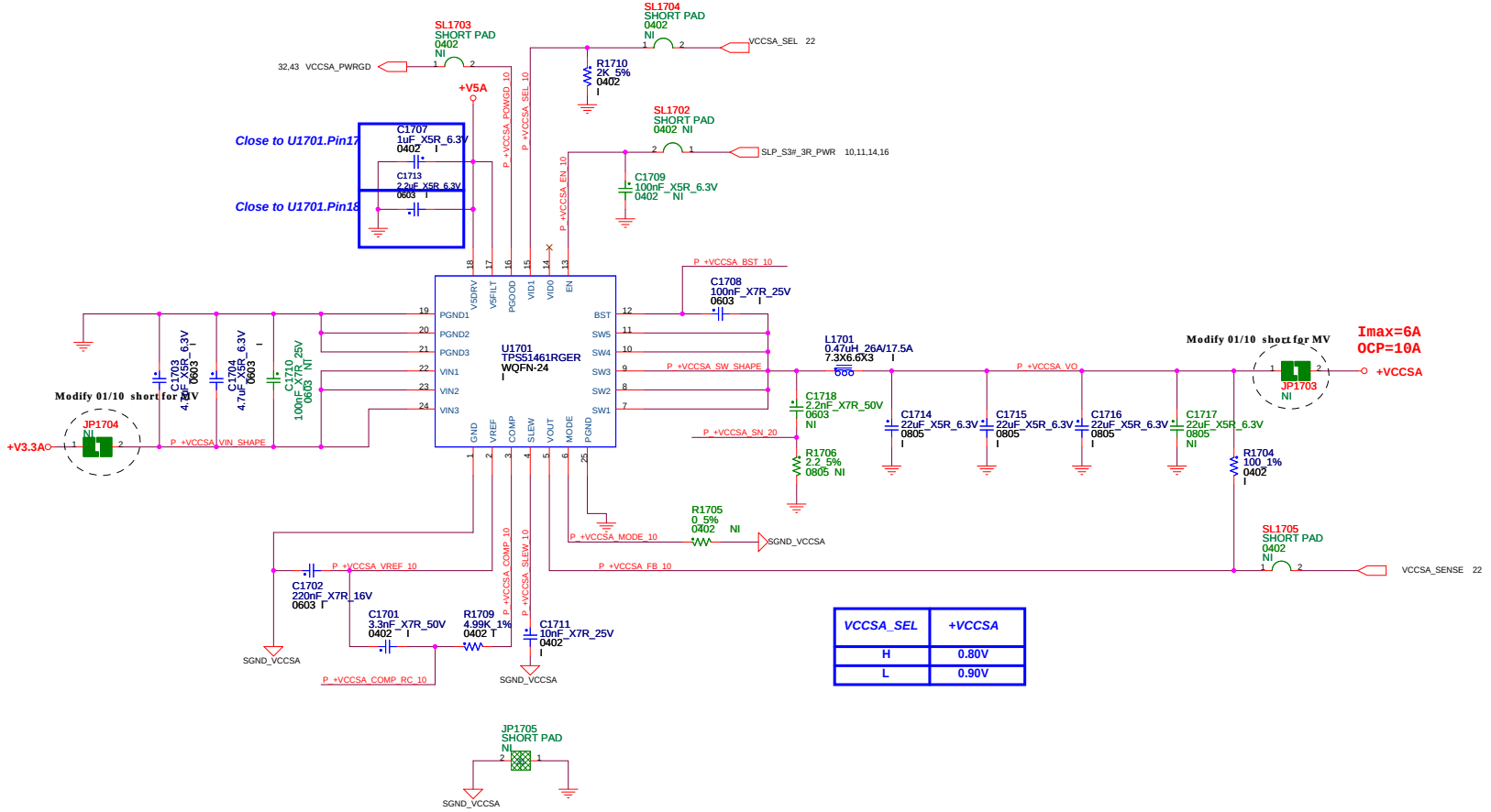
+VCCSA POWER SUPPLY

2010.1026.0

+VCCSA:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.18A
2. Ripple Current:
   Irip=1.39A
3. Ripple Voltage:
   ESR/4=1mohm
   Vrip=1.39mV
4. Inductor Spec:
   Isat=26A
   Idc=17.5A
   DCR=4.2mohm
5. MOSFET Spec:
6. Frequency:
   F=1MHz (R1705=Open)
7. OCP:
   Min : 6A / Typ : 7.5A



VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

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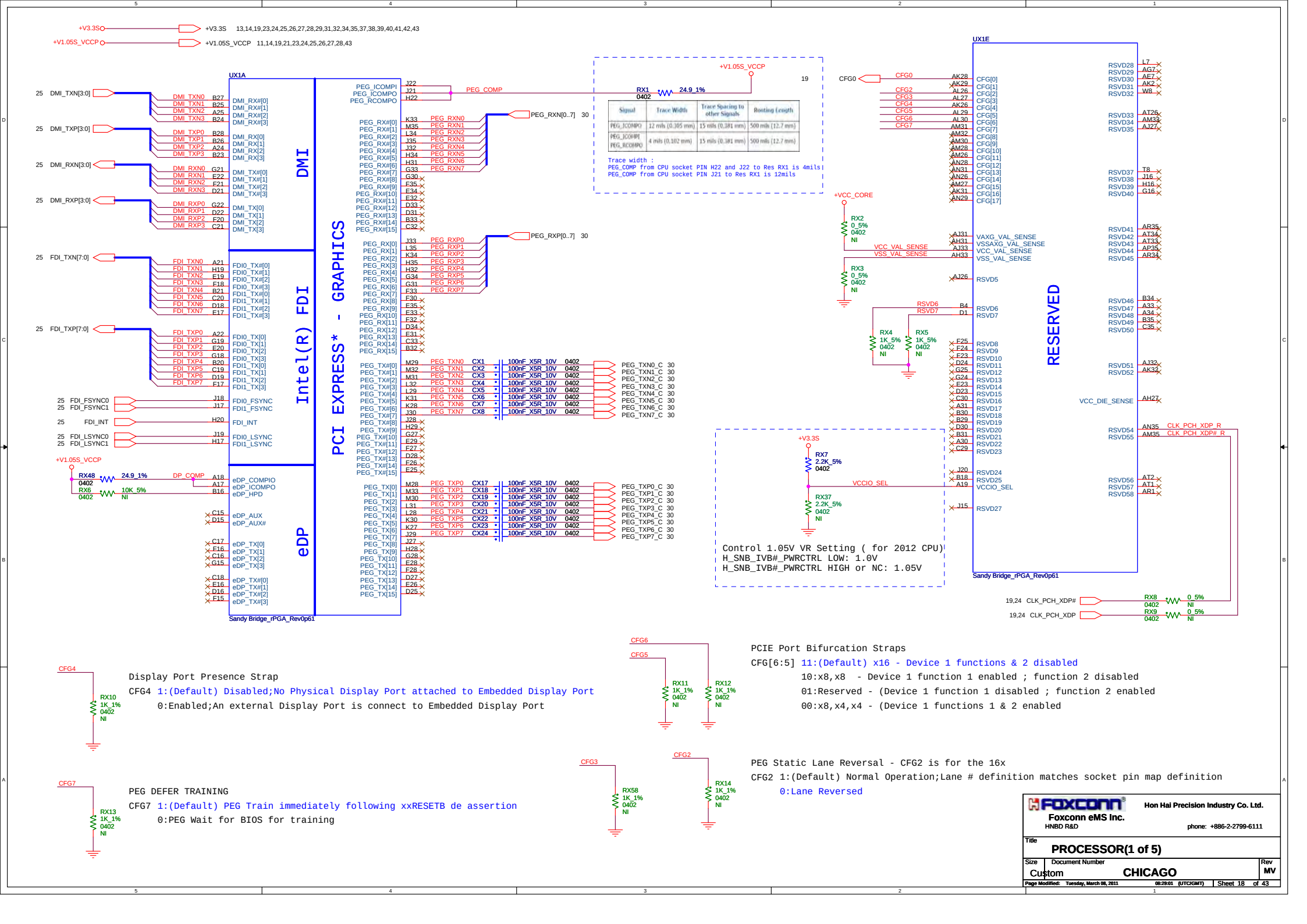
+V3.3S +V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43
UX1A
DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP
Sandy Bridge_rPGA_Rev0p61
Trace width :
PEG_COMP from CPU socket PIN H22 and J22 to Res RX1 is 4mils
PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils
Control 1.05V VR Setting (for 2012 CPU)
H_SNB_IVB#_PWRCTRL LOW: 1.0V
H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V
UX1E
RESERVED
Sandy Bridge_rPGA_Rev0p61
Display Port Presence Strap
CFG4 1:(Default) Disabled;No Physical Display Port attached to Embedded Display Port
0:Enabled;An external Display Port is connect to Embedded Display Port
PEG DEFER TRAINING
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
0:PEG Wait for BIOS for training
PCIE Port Bifurcation Straps
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled
PEG Static Lane Reversal - CFG2 is for the 16x
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
0:Lane Reversed
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PROCESSOR(1 of 5)
Custom
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+V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,22,27,38
+V1.8S +V1.8S 14,16,22,28,43
+V1.5 +V1.5 12,14,15,22,29,43

UX1B

MISC
26 H_SNB_IVB# — C26 PROC_SELECT# (RX15 2.2K_5% 0402 to +V1.8S)
AN34 SKTOCC#

THERMAL
TP_P30 TP1 — 1 H_CATERR# — AL33 CATERR#
26,34 H_PECI — AN33 PECI
13,38 H_PROCHOT# — H_PROCHOT# — RX20 56_5% 0402 — H_PROCHOT# R — AL32 PROCHOT#
(+V1.05S_VCCP — RX18 62_5% 0402 — H_PROCHOT#; CX33 43pF_X7R_50V 0402 — Close to VR)
26 H_THRMTRIP# — AN32 THERMTRIP#

PWR MANAGEMENT
25 H_PM_SYNC — AM34 PM_SYNC
26 H_CPUPWRGD — H_CPUPWRGD — AP33 UNCOREPWRGOOD
(CX125 100nF_X5R_10V 0402; RX27 10K_5% 0402 SM_DRAMPWROK — V8 SM_DRAMPWROK)
BUF_PLT_RST# R — AR33 RESET#

CLOCKS
BCLK A28 / BCLK# A27 — CLK_PCH_CPU_CLK 24 / CLK_PCH_CPU_CLK# 24 (100MHz)
DPLL_REF_CLK A16 / DPLL_REF_CLK# A15 — 0402 RX71 1K_5% / 0402 RX72 1K_5% — +V1.05S_VCCP

DDR3 MISC
SM_DRAMRST# R8 — SM_DRAMRST#
SM_RCOMP[0] AK1 — SM_RCOMP0 RX22 140_1% 0402
SM_RCOMP[1] A5 — SM_RCOMP1 RX23 25.5_1% 0402
SM_RCOMP[2] A4 — SM_RCOMP2 RX24 200_1% 0402

JTAG & BPM
PRDY# AP29 — XDP_PRDY#
PREQ# AP27 — XDP_PREQ#
TCK AR26 — XDP_TCK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBR# — RX26 1K_5% 0402 NI +V3.3S; RX69 0_5% 0402 NI — SB_RST# 25
BPM#[0] AT28 — XDP_OBS0
BPM#[1] AR29 — XDP_OBS1
BPM#[2] AR30 — XDP_OBS2
BPM#[3] AT30 — XDP_OBS3
BPM#[4] AP32 — XDP_OBS4
BPM#[5] AR31 — XDP_OBS5
BPM#[6] AT31 — XDP_OBS6
BPM#[7] AR32 — XDP_OBS7

Sandy Bridge_rPGA_Rev0p61

(+V1.05S_VCCP — RX16 0_5% 0402 NI — SM_DRAMRST# Q — QX1 2N7002-7-F SOT23-3 — RX21 4.99K_1% 0402 — CX34 47nF_X7R_16V 0402)
+V1.5 — RX17 1K_5% 0402 — RX19 1K_5% 0402 — DDR3_DRAMRST# 29
RX25 0_5% 0402 — DRAMRST_CNTRL 22,24

PU/PD for JTAG signals
+V1.05S_VCCP
XDP_TDO — RX28 51_5% 0402
XDP_TMS — RX29 51_5% 0402
XDP_TDI — RX30 51_5% 0402
XDP_PREQ# — RX32 51_5% 0402 NI
XDP_TCK — RX33 51_5% 0402
XDP_TRST# — RX35 51_5% 0402

+V3.3S — RX36 200_1% 0402
RX31 0_5% 0402 NI — SM_DRAMPWROK_R
+V3.3S — CX126 100nF_Y5V_10V 0402
+V1.5_VDDQ — CX129 1uF_Y5V_6.3V 0402 — RX34 200_1% 0402
25 PM_DRAM_PWRGD
34,43 ALL_SYS_PWRGD
UX4 74LVC2G07GW.125 (1A, 2A, GND, 1Y, 2Y, VCC)
RX38 130_1% 0402 — SM_DRAMPWROK
RX75 39_5% 0603 NI
QX4 2N7002-7-F SOT23-3 NI — SLP_S3_12R 14

HEADER1
XDP_PREQ# / XDP_PRDY#
XDP_OBS0 / XDP_OBS1
XDP_OBS2 / XDP_OBS3
XDP_OBS4 / XDP_OBS5
XDP_OBS6 / XDP_OBS7
H_CPUPWRGD — RX39 1K_5% 0402 NI — XDP_H_CPUPWRGD
25,34 EC_PWRBTN# — RX40 1K_5% 0402 NI — XDP_HOOK2
+V1.05S_VCCP
18 CFG0
25,43 SYS_PWROK
CX37 100nF_X5R_6.3V 0402 NI
XDP_TCK
CLK_PCH_XDP 18,24
CLK_PCH_XDP# 18,24
XDP_RST# — RX41 1K_5% 0402 NI — +V1.05S_VCCP — BUF_PLT_RST# 26,34,37,38,40
XDP_DBR#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
BSH-030-01-L-D-A-TR NI

RX70 1.5K_1%
+V3.3S — CX36 100nF_Y5V_10V 0402 NI
+V1.05S_VCCP — RX42 75_1% 0402 NI
26,34,37,38,40 BUF_PLT_RST# — BUFO_CPU_RST# — RX43 43_1% 0402 — BUF_PLT_RST# R
RX44 750_1% 0402
UX3 74LVC1G07GW.125 SOT353-5 NI

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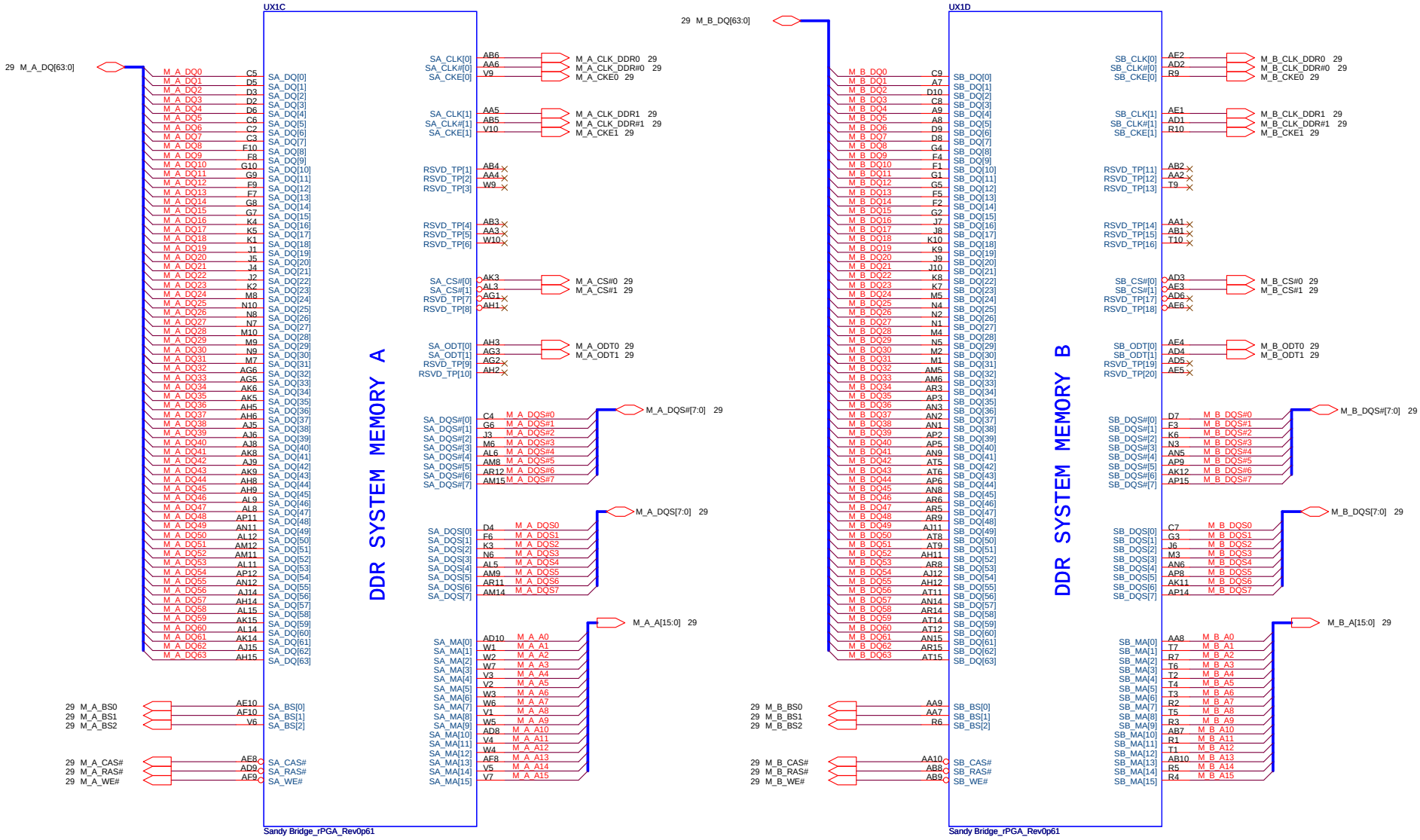

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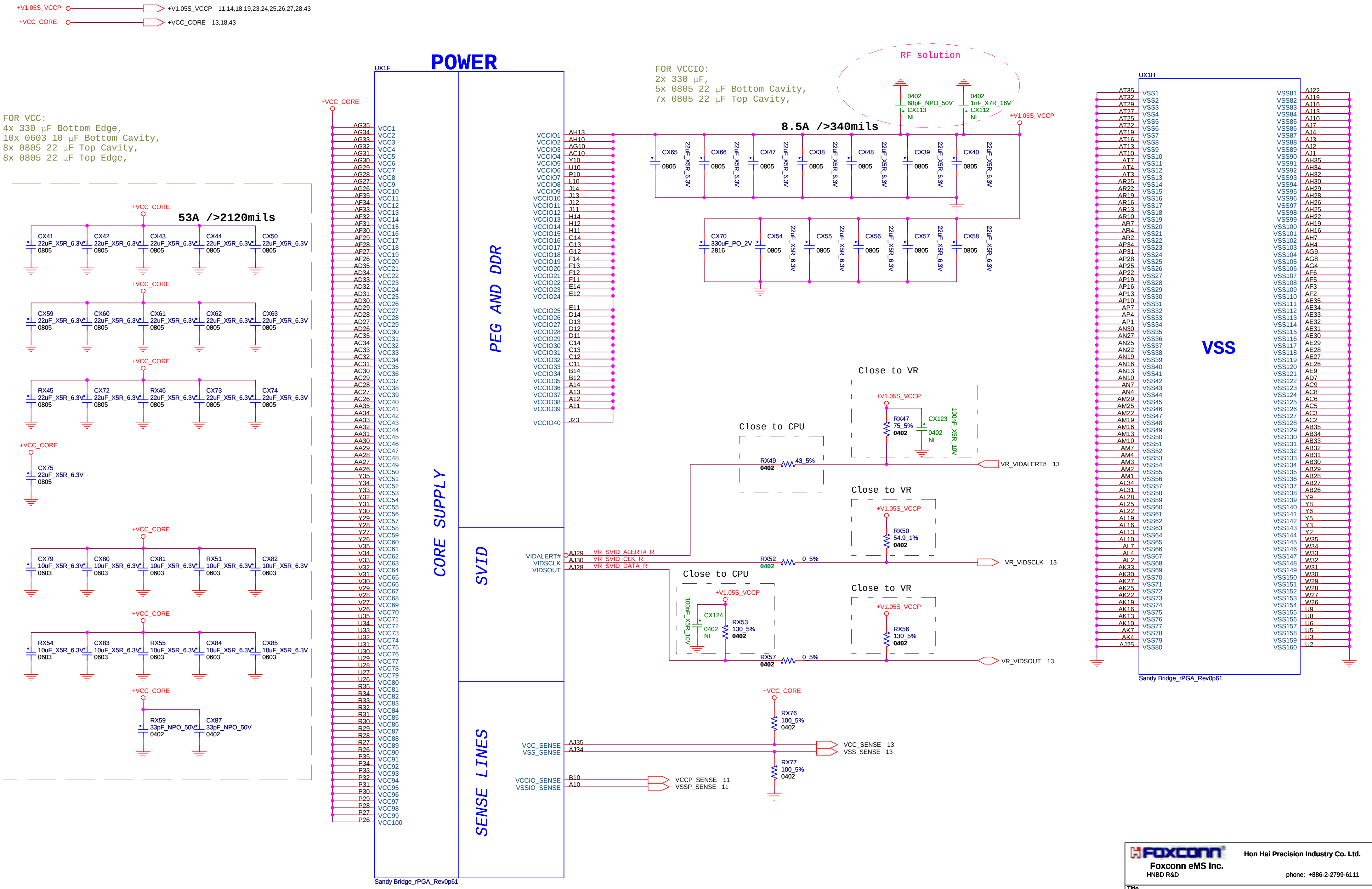

+V1.05S_VCCP
+V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43
+VCC_CORE
+VCC_CORE 13,18,43
FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,
53A />2120mils
CX41 22uF_X5R_6.3V 0805
CX42 22uF_X5R_6.3V 0805
CX43 22uF_X5R_6.3V 0805
CX44 22uF_X5R_6.3V 0805
CX50 22uF_X5R_6.3V 0805
CX59 22uF_X5R_6.3V 0805
CX60 22uF_X5R_6.3V 0805
CX61 22uF_X5R_6.3V 0805
CX62 22uF_X5R_6.3V 0805
CX63 22uF_X5R_6.3V 0805
RX45 22uF_X5R_6.3V 0805
CX72 22uF_X5R_6.3V 0805
RX46 22uF_X5R_6.3V 0805
CX73 22uF_X5R_6.3V 0805
CX74 22uF_X5R_6.3V 0805
CX75 22uF_X5R_6.3V 0805
CX79 10uF_X5R_6.3V 0603
CX80 10uF_X5R_6.3V 0603
CX81 10uF_X5R_6.3V 0603
RX51 10uF_X5R_6.3V 0603
CX82 10uF_X5R_6.3V 0603
RX54 10uF_X5R_6.3V 0603
CX83 10uF_X5R_6.3V 0603
RX55 10uF_X5R_6.3V 0603
CX84 10uF_X5R_6.3V 0603
CX85 10uF_X5R_6.3V 0603
RX59 33pF_NPO_50V 0402
CX87 33pF_NPO_50V 0402
POWER
UX1F
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
Sandy Bridge_rPGA_Rev0p61
FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,
RF solution
0402 68pF_NPO_50V CX113 NI
0402 1nF_X7R_16V CX112 NI
8.5A />340mils
CX65 0805 22uF_X5R_6.3V
CX66 0805 22uF_X5R_6.3V
CX47 0805 22uF_X5R_6.3V
CX38 0805 22uF_X5R_6.3V
CX48 0805 22uF_X5R_6.3V
CX39 0805 22uF_X5R_6.3V
CX40 0805 22uF_X5R_6.3V
CX70 330uF_PO_2V 2816
CX54 0805 22uF_X5R_6.3V
CX55 0805 22uF_X5R_6.3V
CX56 0805 22uF_X5R_6.3V
CX57 0805 22uF_X5R_6.3V
CX58 0805 22uF_X5R_6.3V
VIDALERT# AJ29 VR_SVID_ALERT#_R
VIDSCLK AJ30 VR_SVID_CLK_R
VIDSOUT AJ28 VR_SVID_DATA_R
Close to VR
RX47 75_5% 0402
CX123 0402 NI 100nF_X5R_10V
Close to CPU
RX49 0402 43_5%
VR_VIDALERT# 13
RX50 54.9_1% 0402
RX52 0402 0_5%
VR_VIDSCLK 13
CX124 0402 NI 100nF_X5R_10V
RX53 130_5% 0402
RX56 130_5% 0402
RX57 0402 0_5%
VR_VIDSOUT 13
VCC_SENSE AJ35
VSS_SENSE AJ34
RX76 100_5% 0402
RX77 100_5% 0402
VCC_SENSE 13
VSS_SENSE 13
VCCIO_SENSE B10
VSSIO_SENSE A10
VCCP_SENSE 11
VSSP_SENSE 11
UX1H
VSS

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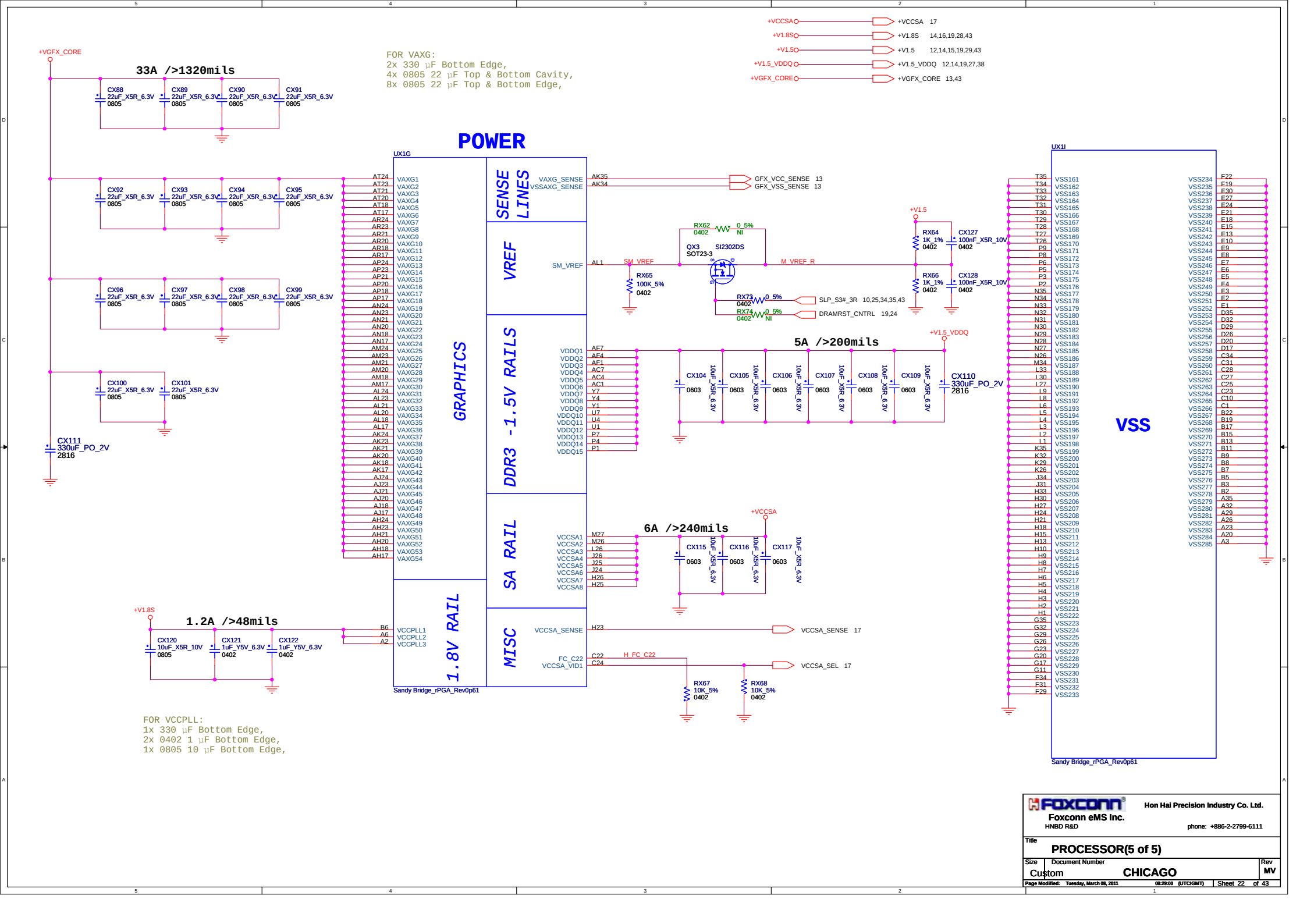
+VCCSA 17
+V1.8S 14,16,19,28,43
+V1.5 12,14,15,19,29,43
+V1.5_VDDQ 12,14,19,27,38
+VGFX_CORE 13,43
+VGFX_CORE
33A />1320mils
CX88 22uF_X5R_6.3V 0805
CX89 22uF_X5R_6.3V 0805
CX90 22uF_X5R_6.3V 0805
CX91 22uF_X5R_6.3V 0805
CX92 22uF_X5R_6.3V 0805
CX93 22uF_X5R_6.3V 0805
CX94 22uF_X5R_6.3V 0805
CX95 22uF_X5R_6.3V 0805
CX96 22uF_X5R_6.3V 0805
CX97 22uF_X5R_6.3V 0805
CX98 22uF_X5R_6.3V 0805
CX99 22uF_X5R_6.3V 0805
CX100 22uF_X5R_6.3V 0805
CX101 22uF_X5R_6.3V 0805
CX111 330uF_PO_2V 2816
FOR VAXG:
2x 330 µF Bottom Edge,
4x 0805 22 µF Top & Bottom Cavity,
8x 0805 22 µF Top & Bottom Edge,
POWER
UX1G
SENSE LINES
VREF
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
VAXG_SENSE
VSSAXG_SENSE
GFX_VCC_SENSE 13
GFX_VSS_SENSE 13
SM_VREF
RX62 0402 0_5% NI
QX3 SI2302DS SOT23-3
M_VREF_R
RX65 100K_5% 0402
RX73 0402 0_5%
RX74 0402 0_5% NI
SLP_S3#_3R 10,25,34,35,43
DRAMRST_CNTRL 19,24
+V1.5
RX64 1K_1% 0402
RX66 1K_1% 0402
CX127 100nF_X5R_10V 0402
CX128 100nF_X5R_10V 0402
+V1.5_VDDQ
5A />200mils
CX104 0603 10uF_X5R_6.3V
CX105 0603 10uF_X5R_6.3V
CX106 0603 10uF_X5R_6.3V
CX107 0603 10uF_X5R_6.3V
CX108 0603 10uF_X5R_6.3V
CX109 0603 10uF_X5R_6.3V
CX110 330uF_PO_2V 2816
+VCCSA
6A />240mils
CX115 0603 10uF_X5R_6.3V
CX116 0603 10uF_X5R_6.3V
CX117 0603 10uF_X5R_6.3V
+V1.8S
1.2A />48mils
CX120 10uF_X5R_10V 0805
CX121 1uF_Y5V_6.3V 0402
CX122 1uF_Y5V_6.3V 0402
VCCSA_SENSE
VCCSA_SENSE 17
FC_C22
H_FC_C22
VCCSA_VID1
VCCSA_SEL 17
RX67 10K_5% 0402
RX68 10K_5% 0402
Sandy Bridge_rPGA_Rev0p61
FOR VCCPLL:
1x 330 µF Bottom Edge,
2x 0402 1 µF Bottom Edge,
1x 0805 10 µF Bottom Edge,
UX1I
VSS
Sandy Bridge_rPGA_Rev0p61
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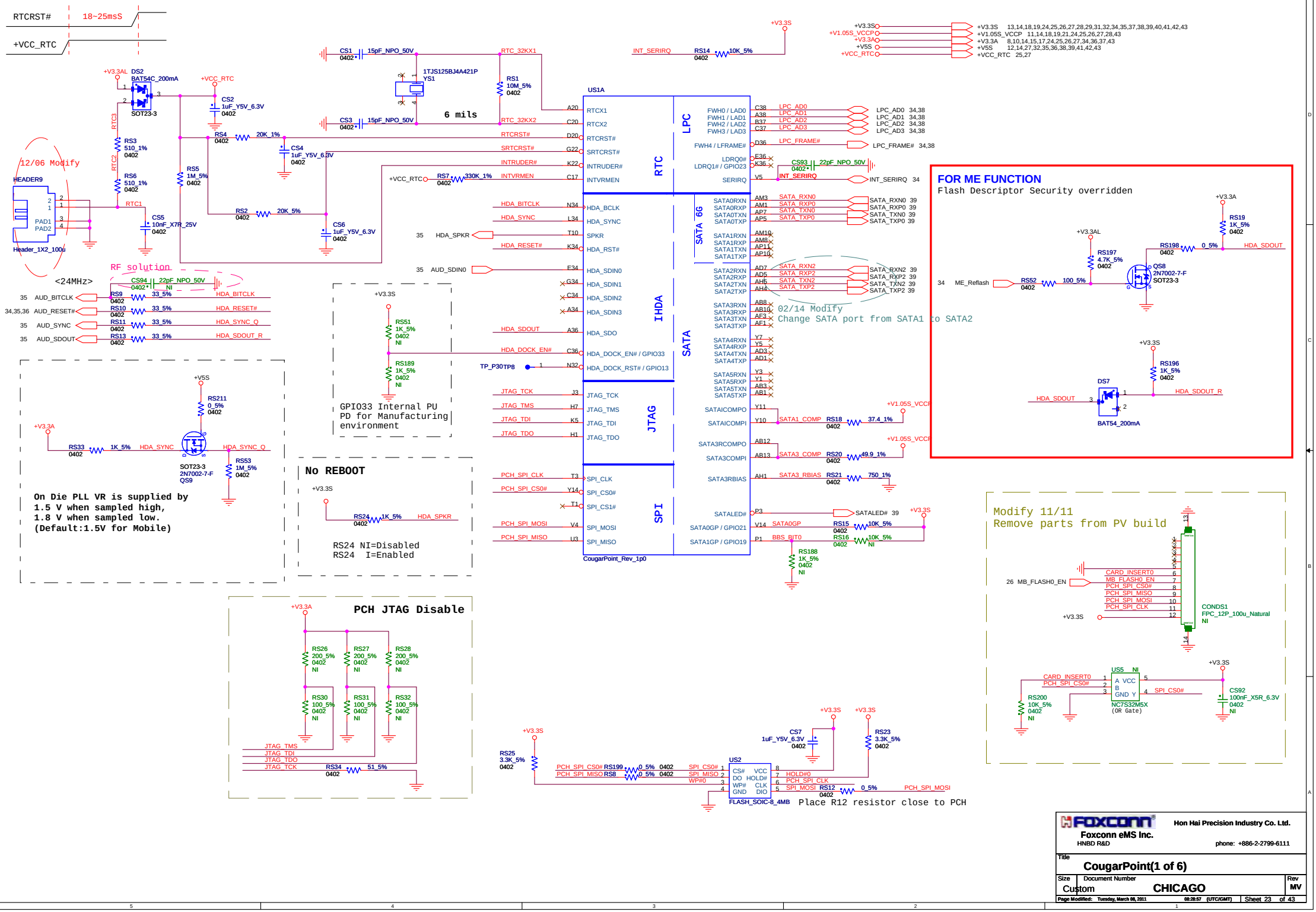

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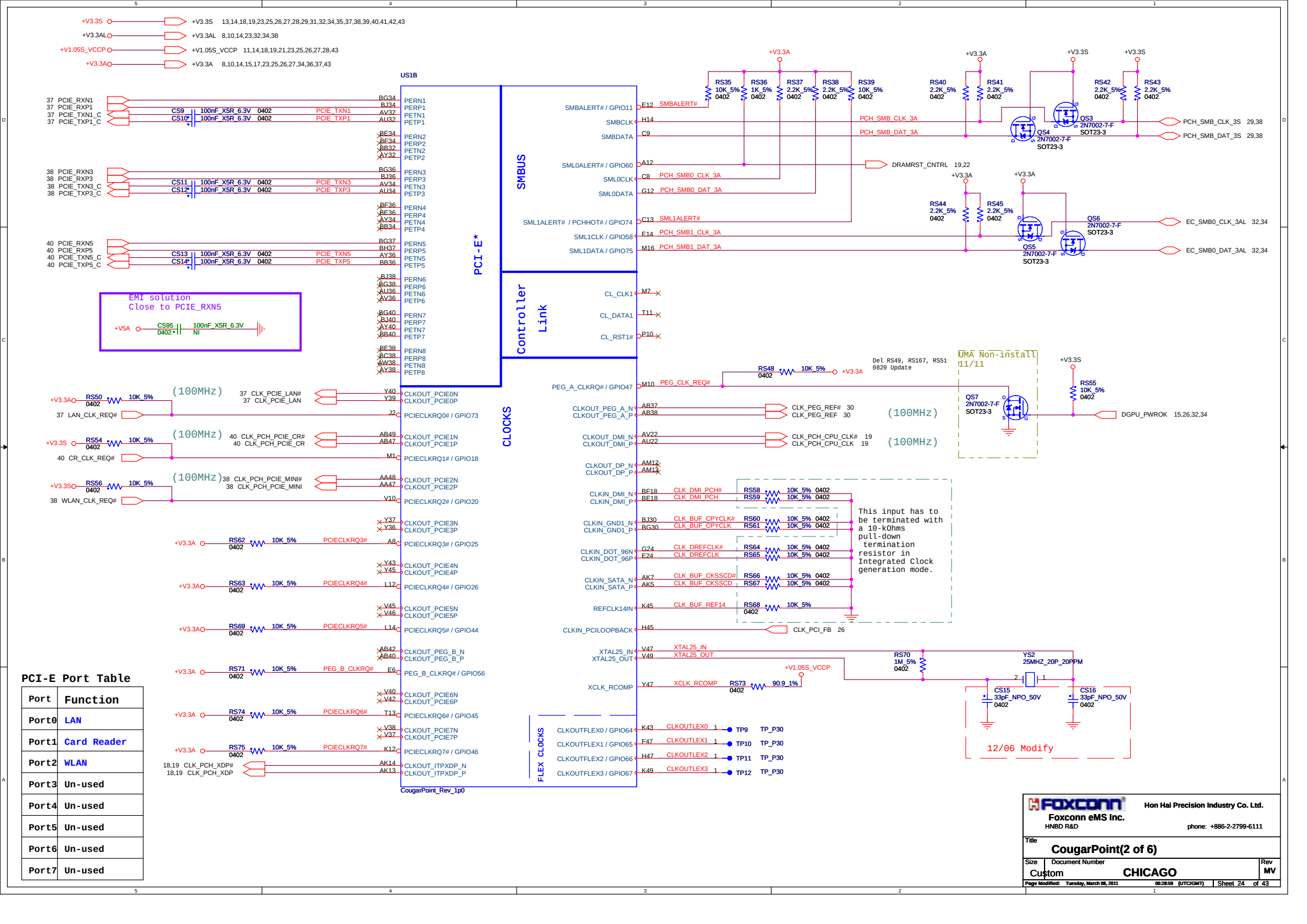

PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used

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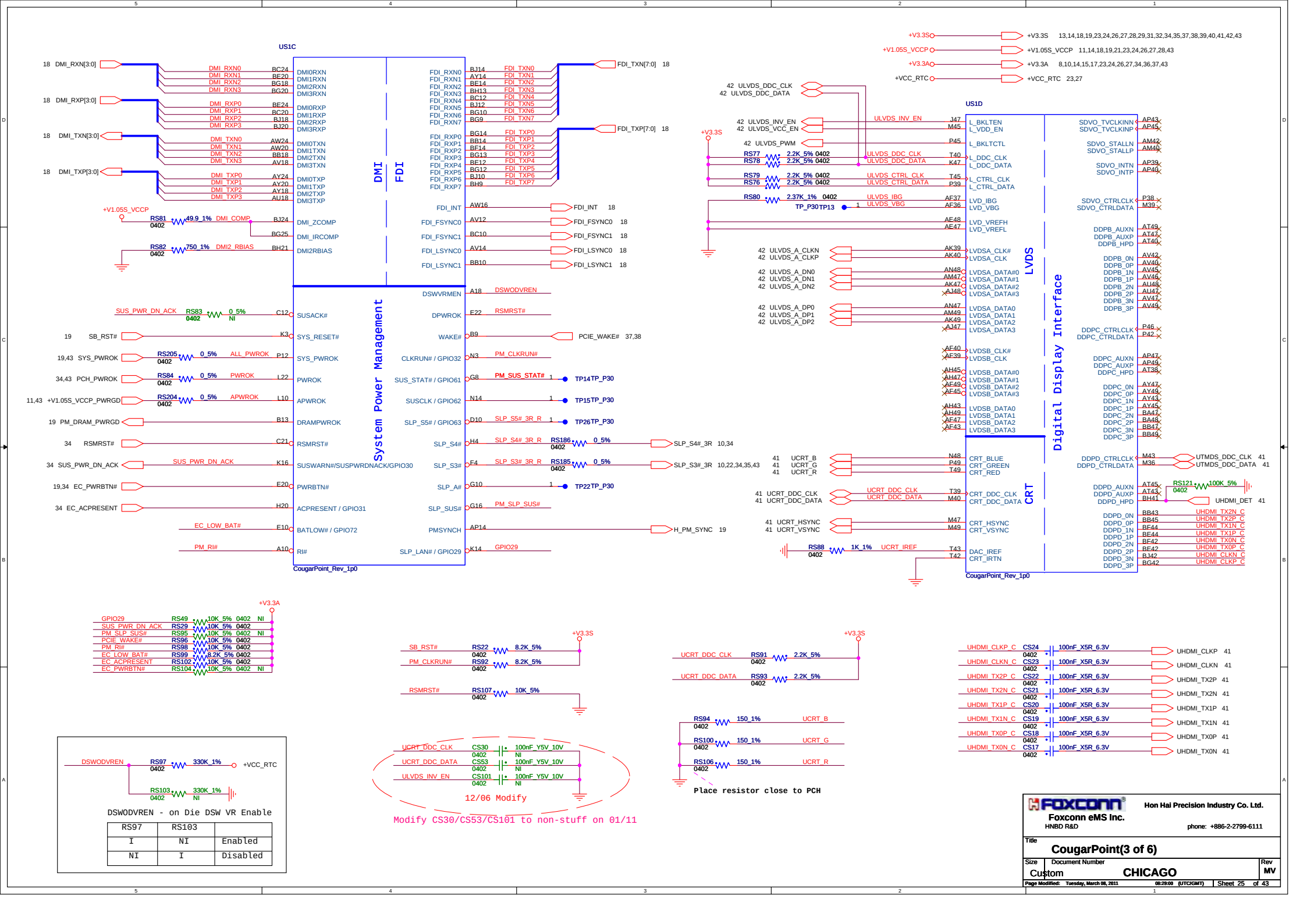
US1C
DMI
FDI
System Power Management
CougarPoint_Rev_1p0
US1D
LVDS
Digital Display Interface
CRT
CougarPoint_Rev_1p0
+V3.3S 13,14,18,19,23,24,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,18,19,21,23,24,26,27,28,43
+V3.3A 8,10,14,15,17,23,24,26,27,34,36,37,43
+VCC_RTC 23,27
DSWODVREN - on Die DSW VR Enable
RS97 RS103
I NI Enabled
NI I Disabled
12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11
Place resistor close to PCH
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Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

RS108 0402 1K_5% NI BBS_BIT1

+V3.3S

RS111 0402 8.2K_5% INT_PIRQA#
RS113 0402 8.2K_5% INT_PIRQB#
RS115 0402 8.2K_5% INT_PIRQC#
RS117 0402 8.2K_5% INT_PIRQD#
RS118 0402 8.2K_5% DGPU_HOLD_RST#
RS119 0402 8.2K_5% NI DGPU_DDC_SELECT#
RS120 0402 8.2K_5% DGPU_PWR_EN#
RS122 0402 8.2K_5% SB_ODD_MD#
RS123 0402 8.2K_5% SATA_ODD_DA#
RS124 0402 8.2K_5% INT_PIRQG#
RS125 0402 8.2K_5% INT_PIRQH#

RS126 0402 100K_5% NI PLT_RST#

Del RS121 8.2Kohm to +V3.3S
0820 Update

US1E

RSVD: TP1–TP20, TP21–TP24, TP25–TP40

PCI: PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1# / GPIO50, REQ2# / GPIO52, REQ3# / GPIO54, GNT1# / GPIO51, GNT2# / GPIO53, GNT3# / GPIO55, PIRQE# / GPIO2, PIRQF# / GPIO3, PIRQG# / GPIO4, PIRQH# / GPIO5, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

USB: USBP0N/P, USBP1N/P, USBP2N/P, USBP3N/P, USBP4N/P, USBP5N/P, USBP6N/P, USBP7N/P, USBP8N/P, USBP9N/P, USBP10N/P, USBP11N/P, USBP12N/P, USBP13N/P, USBRBIAS, USBRBIAS#, OC0# / GPIO59, OC1# / GPIO40, OC2# / GPIO41, OC3# / GPIO42, OC4# / GPIO43, OC5# / GPIO9, OC6# / GPIO10, OC7# / GPIO14

CougarPoint_Rev_1p0

30 DGPU_HOLD_RST# — DGPU_HOLD_RST# RS46 0402 0_5% — 12/06 Modify
15,32 DGPU_PWR_EN# — DGPU_PWR_EN#
TP_P30 TP17 — DGPU_PWM_SELECT#, DGPU_DDC_SELECT#
39 SB_ODD_MD# — SB_ODD_MD#, SATA_ODD_DA#
INT_PIRQG#, INT_PIRQH#
TP_P30 TP18 — PCI_PME#
30 PLT_RST# — PLT_RST#
38 CLK_PCI_JIG — RS134 0402 22_5% TP_P30 TP19 CLK_PCI_JIG_R
34 CLK_PCI_KBC — RS135 0402 22_5% TP_P30 TP20 CLK_PCI_KBC_R
24 CLK_PCI_FB — RS136 0402 22_5% CLK_PCI_FB_R

USB_PN0–PN2 39, USB_PP0–PP2 39, USB_PN10–PN11 42, USB_PP10–PP11 42, USB_PP1 39, USB_PN1 39, USB_PP11 38, USB_PN11 38

USBRBIAS — RS131 0402 22.6_1%

USB_OC#0 39, USB_OC#1 39

US1F

GPIO: BMBUSY# / GPIO0, TACH1 / GPIO1, TACH2 / GPIO6, TACH3 / GPIO7, GPIO8, LAN_PHY_PWR_CTRL / GPIO12, GPIO15, SATA4GP / GPIO16, TACH0 / GPIO17, SCLOCK / GPIO22, GPIO24 / MEM_LED, GPIO27, GPIO28, STP_PCI# / GPIO34, GPIO35, SATA2GP / GPIO36, SATA3GP / GPIO37, SLOAD / GPIO38, SDATAOUT0 / GPIO39, SDATAOUT1 / GPIO48, SATA5GP / GPIO49, GPIO57, TACH4 / GPIO68, TACH5 / GPIO69, TACH6 / GPIO70, TACH7 / GPIO71

CPU/MISC: A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, DF_TVS, TS_VSS1–4, NC_1

NCTF: VSS_NCTF_1–14, VSS_NCTF_15–32

CougarPoint_Rev_1p0

34 PCI_SERR# — RS17 0402 0_5% GPIO0
34 EC_SMI#
DGPU_HPD_INTR#
34 RUN_SCI#
TP_P30 TP25 — 1
GPIO12
23 MB_FLASH0_EN
GPIO16
15,24,32,34 DGPU_PWROK — DGPU_PWROK
GPIO22
TP_P30 TP16 — 1
GPIO24
GPIO27
GPIO28
GPIO34
GPIO35
SB_ODD_IN# Q
GPIO37
MFG_MODE
GFX_DET
GPIO48
GPIO49
GPIO57

RS127 10K_5% 0402

C40 RS201 0402 0_5% EC_ODD_EN 14,34
B41 GPIO69
C41 GPIO70
A40 GPIO71
RS109 10K_5% 0402

P4 A20GATE 34
AU16 H_PECI_R RS110 0402 0_5% NI H_PECI 19,34
P5 KBRST# 34
AY11 H_CPUPWRGD 19
AY10 H_THRMTRIP# R RS112 0402 390_1% H_THRMTRIP# 19
T14 RS114 0402 56_5% NI +V1.05S_VCCP
AY1 H_SNB_IVB# R RS116 0402 1K_5% H_SNB_IVB# 19

AH8, AK11, AH10, AK10

P37

+V3.3A

RS132 0402 10K_5% GPIO28
RS130 0402 1K_5% NI

RS195 0402 10K_5% GPIO24
RS137 0402 10K_5% GPIO12
RS138 0402 1K_5% MB_FLASH0_EN

+V3.3S

RS139 0402 10K_5% GPIO70
RS140 0402 10K_5% GPIO71
RS141 0402 10K_5% GPIO0
RS142 0402 10K_5% EC_SMI#
RS146 0402 10K_5% DGPU_HPD_INTR#
RS154 0402 10K_5% MFG_MODE
RS158 0402 10K_5% GFX_DET
RS159 0402 10K_5% GPIO16
RS160 0402 10K_5% GPIO49
RS161 0402 10K_5% GPIO22
RS162 0402 10K_5% GPIO34
RS163 0402 10K_5% GPIO48
RS133 0402 220K_5% GPIO37

GPIO27 RS143 0402 10K_5%
GPIO35 RS148 0402 1K_5% NI
DGPU_PWROK RS155 0402 100K_5% NI

PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

+V3.3S — +V3.3S 13,14,18,19,23,24,25,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V3.3A — +V3.3A 8,10,14,15,17,23,24,25,27,34,36,37,43

+V3.3S
US4 74LVC1G17GW.125
19,34,37,38,40 BUF_PLT_RST# — RS152 100K_5% 0402 — PLT_RST#

USB_OC#0 — 0402 10K_5% RS144
USB_OC#1 — 0402 10K_5% RS145
USB_OC#2 — 0402 10K_5% RS147
+V3.3A

12/06 Modify
DGPU_HOLD_RST# — CS102 0402 100nF_Y5V_10V NI
SB_ODD_MD# — CS103 0402 100nF_Y5V_10V NI

Modify CS102/CS103 to non-stuff on 01/11

+V3.3S
QS10 2N7002-7-F SOT23-3 NI
RS164 220K_5% 0402
39 SB_ODD_IN# — SB_ODD_IN# Q
PLT_RST#

02/24 Modify
same as the PV build

USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

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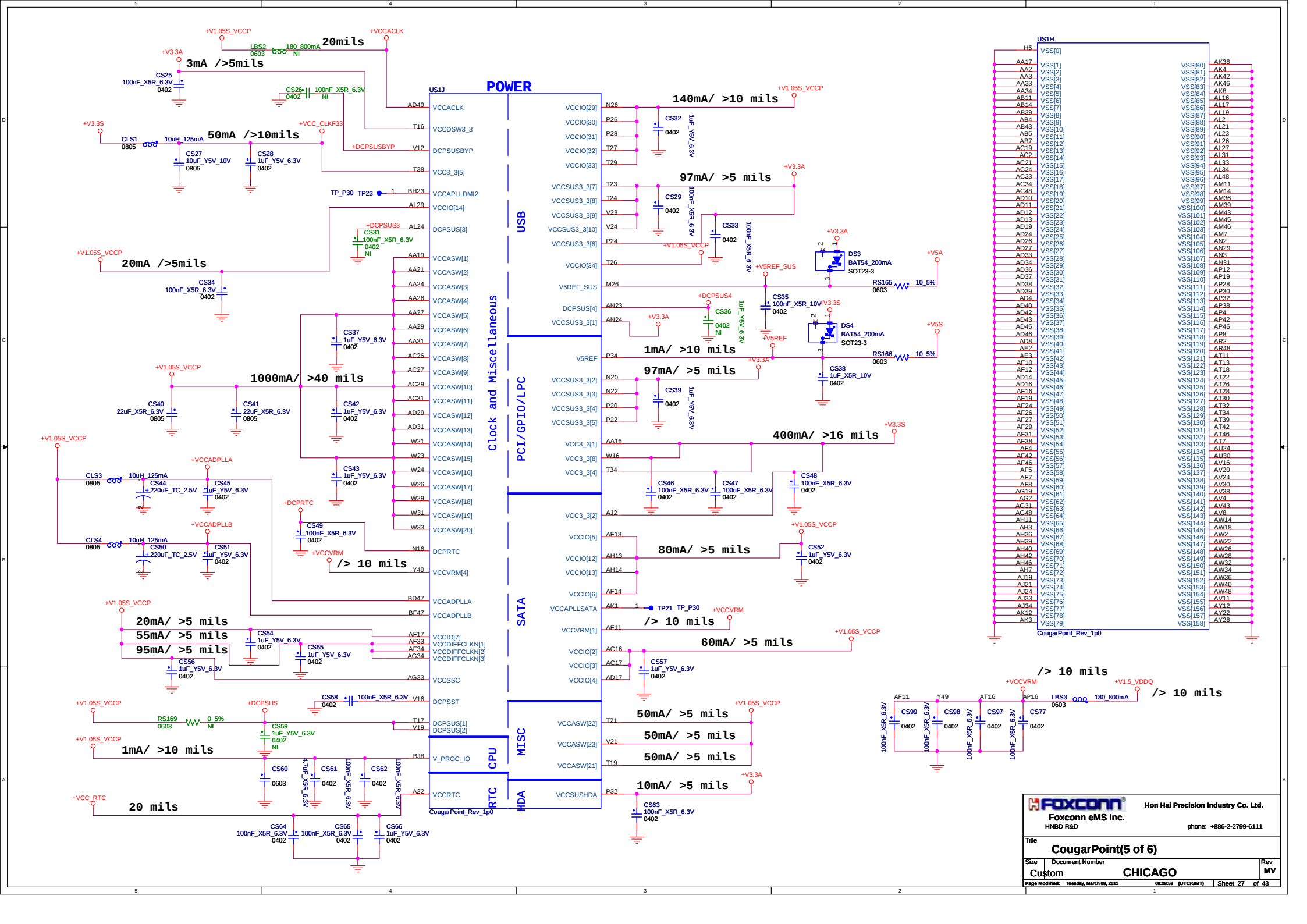
POWER
US1J
CougarPoint_Rev_1p0
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
20mils
3mA />5mils
50mA />10mils
20mA />5mils
1000mA/ >40 mils
1mA/ >10 mils
20mA/ >5 mils
55mA/ >5 mils
95mA/ >5 mils
20 mils
140mA/ >10 mils
97mA/ >5 mils
1mA/ >10 mils
97mA/ >5 mils
400mA/ >16 mils
80mA/ >5 mils
/> 10 mils
60mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
10mA/ >5 mils
/> 10 mils
/> 10 mils
US1H
CougarPoint_Rev_1p0
Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBD R&D
phone: +886-2-2799-6111
Title
CougarPoint(5 of 6)
Size
Custom
Document Number
CHICAGO
Rev
MV
Page Modified: Tuesday, March 08, 2011 08:28:58 (UTC/GMT)
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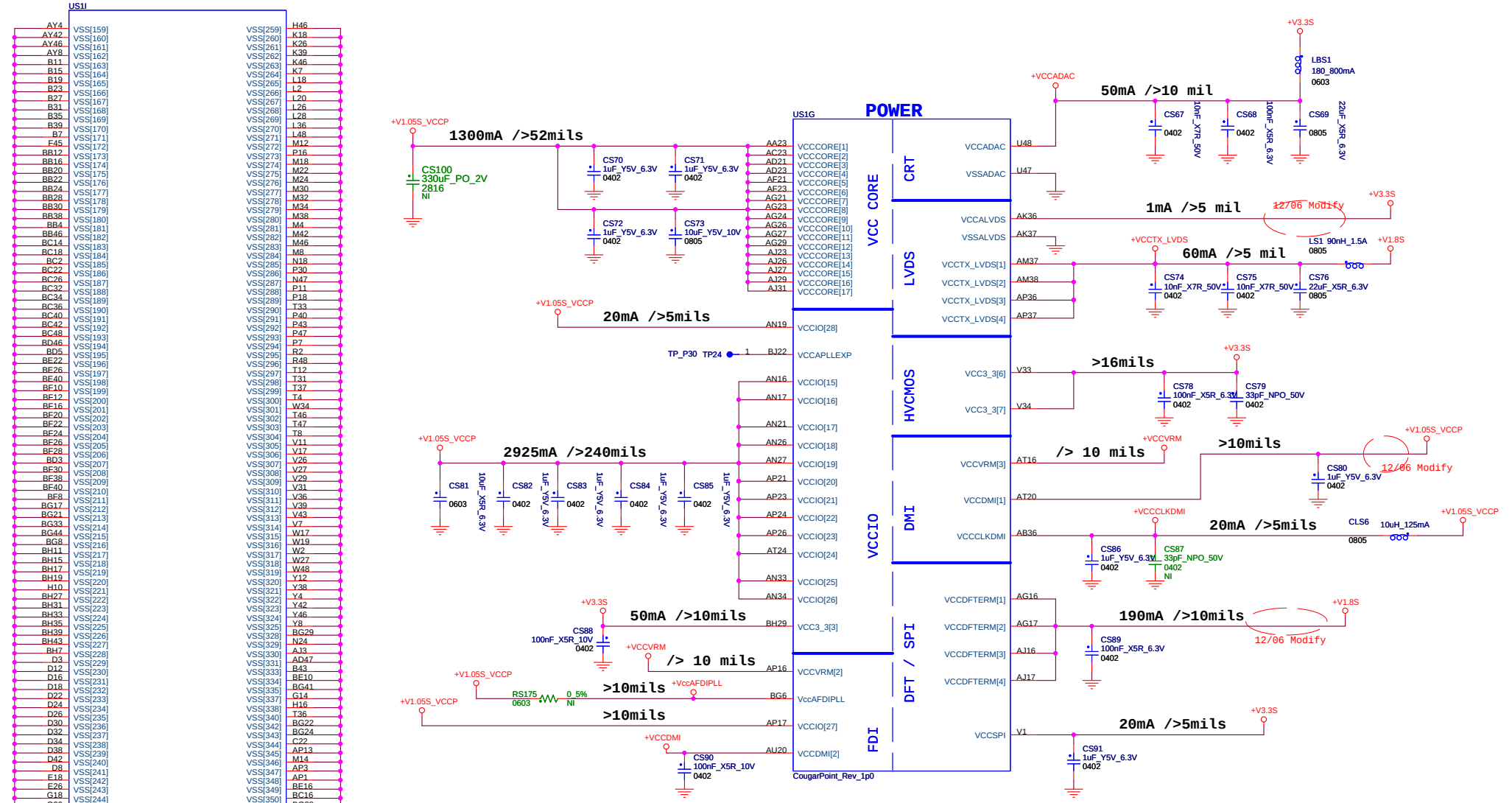
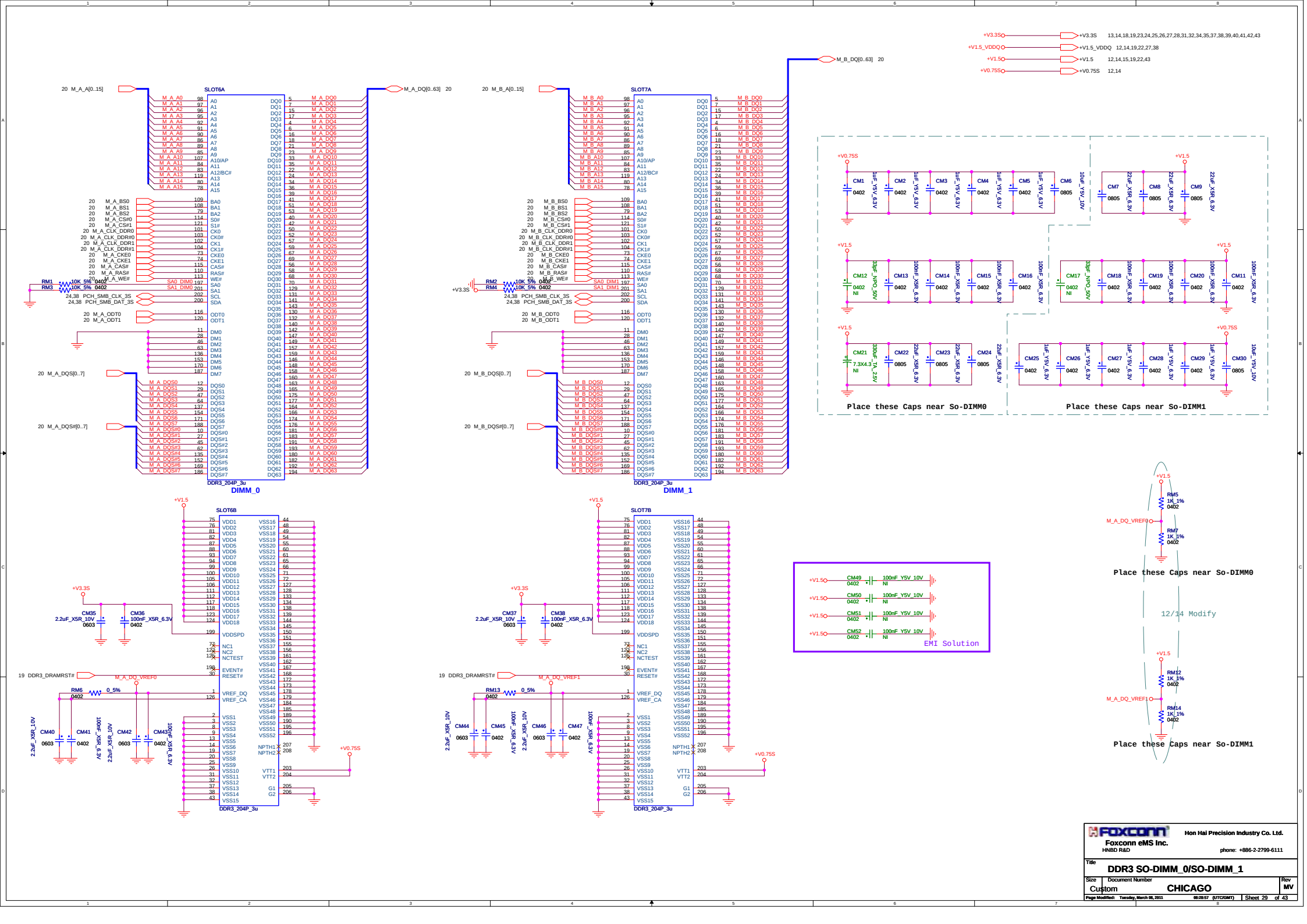


Hon Hai Precision Industry Co. Ltd.	Foxconn eMS Inc.
HNBD R&D	phone: +886-2-2799-6111
Title	CougarPoint(6 of 6)
Size: Custom	Document Number: CHICAGO
Rev: MV	
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)	Sheet 28 of 43


+V3.3S +V3.3S 13,14,18,19,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41,42,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,19,22,27,38
+V1.5 +V1.5 12,14,15,19,22,43
+V0.75S +V0.75S 12,14
M_B_DQ[0..63] 20
SLOT6A
20 M_A_A[0..15]
M_A_DQ[0..63] 20
20 M_A_BS0
20 M_A_BS1
20 M_A_BS2
20 M_A_CS#0
20 M_A_CS#1
20 M_A_CLK_DDR0
20 M_A_CLK_DDR#0
20 M_A_CLK_DDR1
20 M_A_CLK_DDR#1
20 M_A_CKE0
20 M_A_CKE1
20 M_A_CAS#
20 M_A_RAS#
20 M_A_WE#
RM1 10K_5% 0402
RM3 10K_5% 0402
24,38 PCH_SMB_CLK_3S
24,38 PCH_SMB_DAT_3S
20 M_A_ODT0
20 M_A_ODT1
20 M_A_DQS[0..7]
20 M_A_DQS#[0..7]
DDR3_204P_3u
DIMM_0
SLOT7A
20 M_B_A[0..15]
20 M_B_BS0
20 M_B_BS1
20 M_B_BS2
20 M_B_CS#0
20 M_B_CS#1
20 M_B_CLK_DDR0
20 M_B_CLK_DDR#0
20 M_B_CLK_DDR1
20 M_B_CLK_DDR#1
20 M_B_CKE0
20 M_B_CKE1
20 M_B_CAS#
20 M_B_RAS#
20 M_B_WE#
RM2 10K_5% 0402
RM4 10K_5% 0402
+V3.3S
24,38 PCH_SMB_CLK_3S
24,38 PCH_SMB_DAT_3S
20 M_B_ODT0
20 M_B_ODT1
20 M_B_DQS[0..7]
20 M_B_DQS#[0..7]
DDR3_204P_3u
DIMM_1
Place these Caps near So-DIMM0
Place these Caps near So-DIMM1
SLOT6B
+V1.5
+V3.3S
CM35 2.2uF_X5R_10V 0603
CM36 100nF_X5R_6.3V 0402
19 DDR3_DRAMRST#
M_A_DQ_VREF0
RM6 0_5%
CM40 2.2uF_X5R_10V 0603
CM41 100nF_X5R_6.3V 0402
CM42 2.2uF_X5R_10V 0603
CM43 100nF_X5R_6.3V 0402
+V0.75S
DDR3_204P_3u
SLOT7B
+V1.5
+V3.3S
CM37 2.2uF_X5R_10V 0603
CM38 100nF_X5R_6.3V 0402
19 DDR3_DRAMRST#
M_A_DQ_VREF1
RM13 0_5%
CM44 2.2uF_X5R_10V 0603
CM45 100nF_X5R_6.3V 0402
CM46 2.2uF_X5R_10V 0603
CM47 100nF_X5R_6.3V 0402
+V0.75S
DDR3_204P_3u
EMI Solution
+V1.5
CM49 0402 100nF_Y5V_10V NI
CM50 0402 100nF_Y5V_10V NI
CM51 0402 100nF_Y5V_10V NI
CM52 0402 100nF_Y5V_10V NI
+V1.5
RM5 1K_1% 0402
M_A_DQ_VREF0
RM7 1K_1% 0402
Place these Caps near So-DIMM0
12/14 Modify
+V1.5
RM12 1K_1% 0402
M_A_DQ_VREF1
RM14 1K_1% 0402
Place these Caps near So-DIMM1
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Foxconn eMS Inc.
HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
Title
DDR3 SO-DIMM_0/SO-DIMM_1
Size
Custom
Document Number
CHICAGO
Rev
MV
Page Modified: Tuesday, March 08, 2011 08:28:57 (UTC/GMT)
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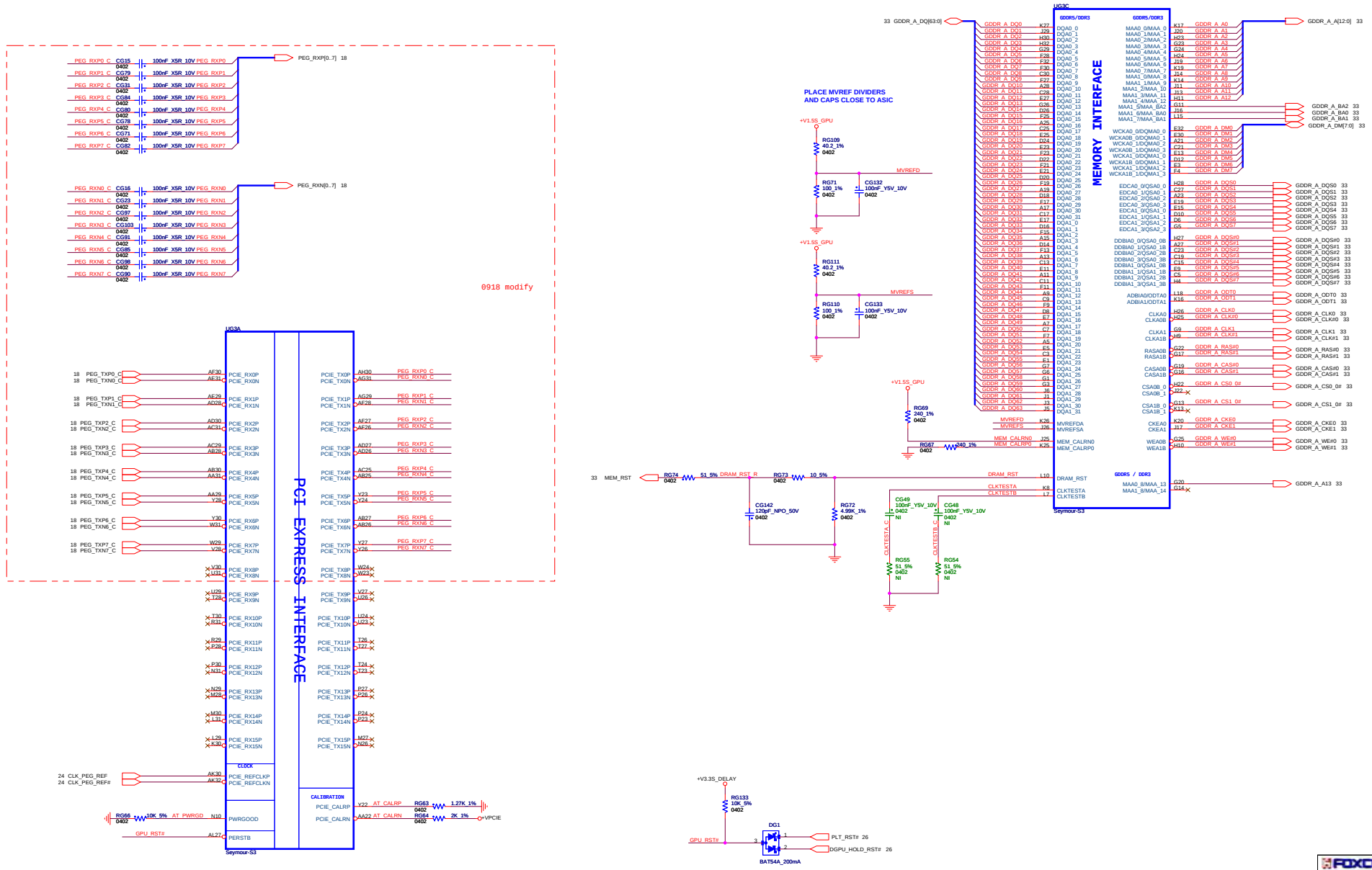
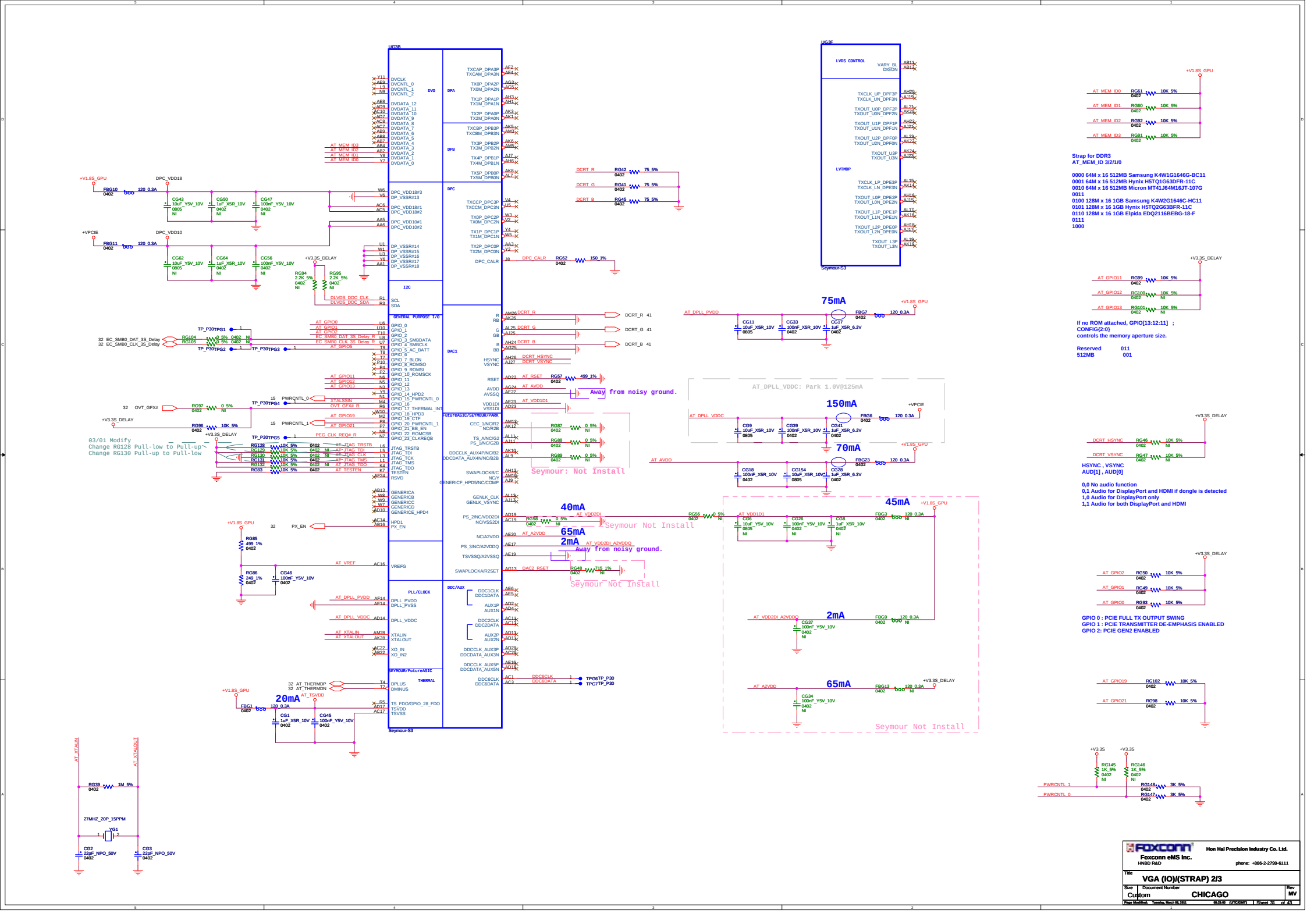


Foxconn eMS Inc. HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111		
Title: VGA_S3 (PCI-E) 1/3			
Size: Custom	Document Number: CHICAGO	Rev: MV	
Page Modified: Tuesday, March 09, 2021 08:29:35 (UTC/GMT)		Sheet 30 of 43	


UG3B
UG3F
LVDS CONTROL
LVTMDP
Seymour-S3
DVO
DPA
DPB
DPC
I2C
GENERAL PURPOSE I/O
DAC1
FutureASIC/SEYMOUR/P2RC
DDC/AUX
PLL/CLOCK
THERMAL
SEYMOUR/FutureASIC
+V1.8S_GPU
+V3.3S_DELAY
+VPCIE
DPC_VDD18
DPC_VDD10
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
Away from noisy ground.
Seymour: Not Install
Seymour Not Install
AT_DPLL_VDDC: Park 1.0V@125mA
Strap for DDR3
AT_MEM_ID 3/2/1/0
0000 64M x 16 512MB Samsung K4W1G1646G-BC11
0001 64M x 16 512MB Hynix H5TQ1G63DFR-11C
0010 64M x 16 512MB Micron MT41J64M16JT-107G
0011
0100 128M x 16 1GB Samsung K4W2G1646C-HC11
0101 128M x 16 1GB Hynix H5TQ2G63BFR-11C
0110 128M x 16 1GB Elpida EDQ2116BEBG-18-F
0111
1000
If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.
Reserved 011
512MB 001
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
03/01 Modify
Change RG128 Pull-low to Pull-up
Change RG130 Pull-up to Pull-low
27MHZ_20P_15PPM
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Title
VGA (IO)/(STRAP) 2/3
Size
Custom
Document Number
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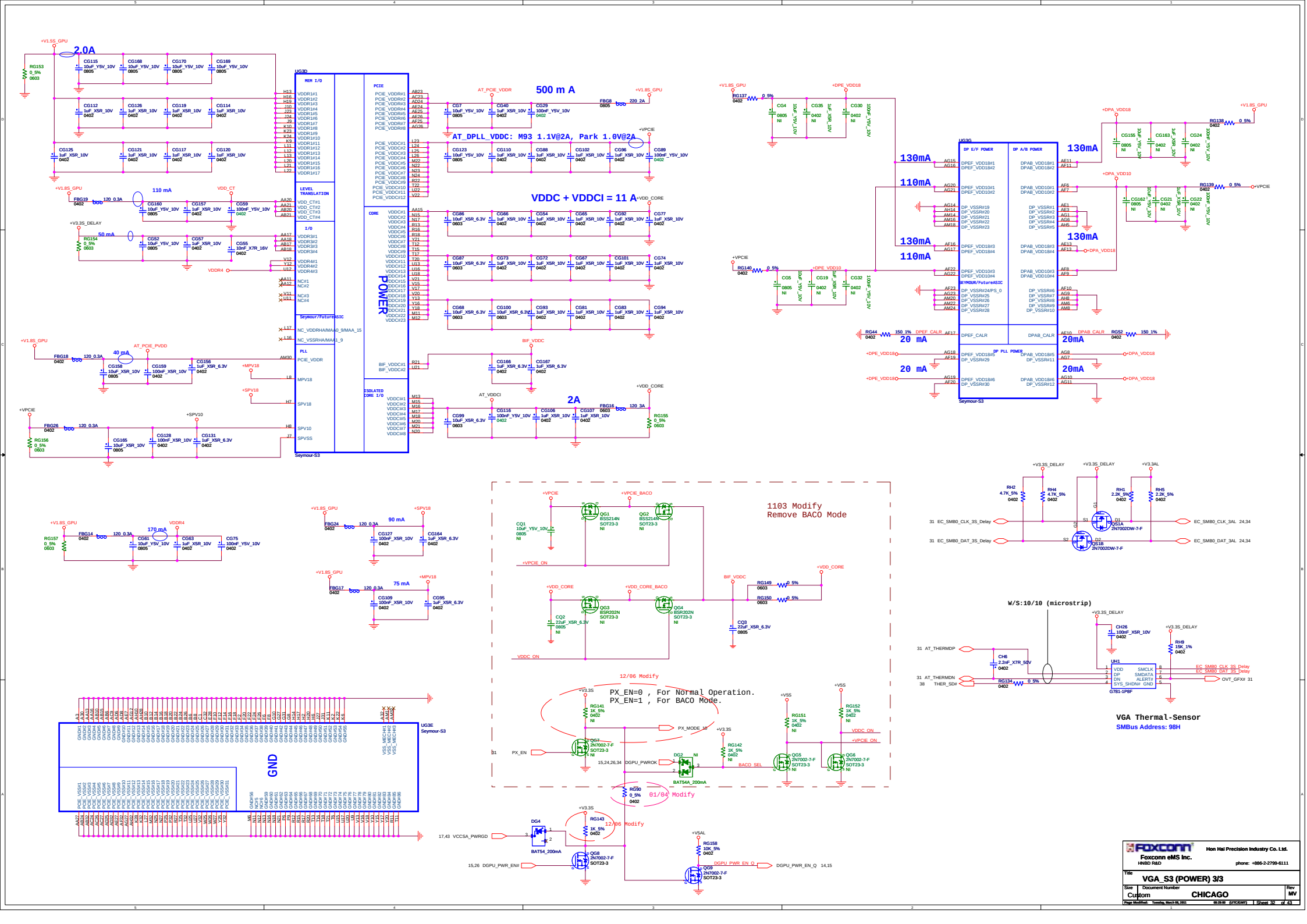
2.0A
500 m A
AT_DPLL_VDDC: M93 1.1V@2A, Park 1.0V@2A
VDDC + VDDCI = 11 A
2A
110 mA
50 mA
40 mA
90 mA
75 mA
170 mA
20 mA
130mA
110mA
1103 Modify
Remove BACO Mode
12/06 Modify
01/04 Modify
PX_EN=0 , For Normal Operation.
PX_EN=1 , For BACO Mode.
W/S:10/10 (microstrip)
VGA Thermal-Sensor
SMBus Address: 98H
UG3D
Seymour-S3
UG3E
UG3G
GND
POWER
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HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
VGA_S3 (POWER) 3/3
CHICAGO
Custom
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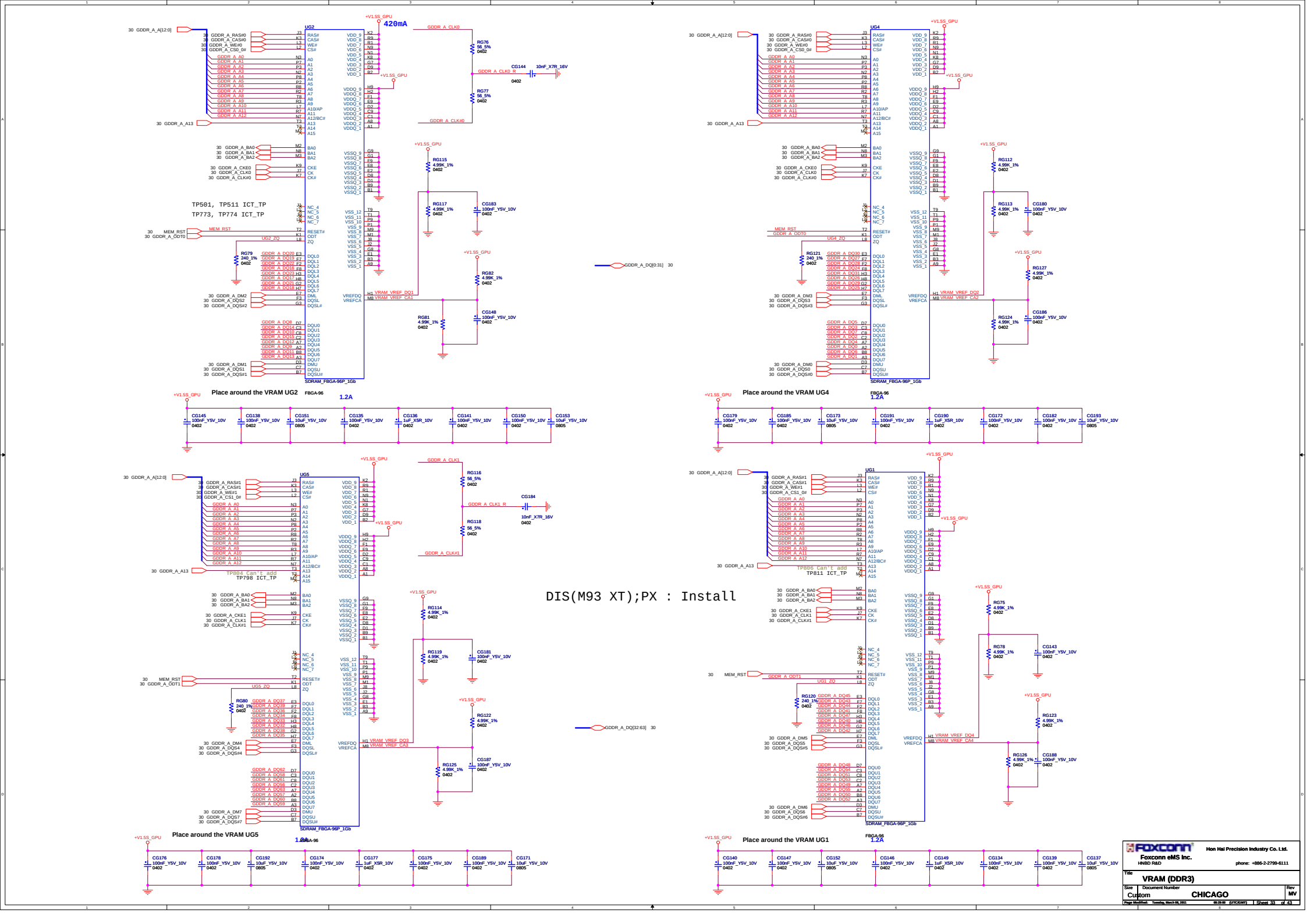
UG2
420mA
+V1.5S_GPU
GDDR_A_CLK0
GDDR_A_CLK0_R
GDDR_A_CLK#0
RG76 56_5% 0402
RG77 56_5% 0402
CG144 10nF_X7R_16V 0402
RG115 4.99K_1% 0402
RG117 4.99K_1% 0402
CG183 100nF_Y5V_10V 0402
RG82 4.99K_1% 0402
RG81 4.99K_1% 0402
CG148 100nF_Y5V_10V 0402
TP501, TP511 ICT_TP
TP773, TP774 ICT_TP
MEM_RST
UG2_ZQ
RG79 240_1% 0402
SDRAM_FBGA-96P_1Gb
Place around the VRAM UG2
FBGA-96
1.2A
UG4
RG112 4.99K_1% 0402
RG113 4.99K_1% 0402
CG180 100nF_Y5V_10V 0402
RG127 4.99K_1% 0402
RG124 4.99K_1% 0402
CG186 100nF_Y5V_10V 0402
UG4_ZQ
RG121 240_1% 0402
Place around the VRAM UG4
CG145 100nF_Y5V_10V 0402
CG138 100nF_Y5V_10V 0402
CG151 10uF_Y5V_10V 0805
CG135 100nF_Y5V_10V 0402
CG136 1uF_X5R_10V 0402
CG141 100nF_Y5V_10V 0402
CG150 100nF_Y5V_10V 0402
CG153 10uF_Y5V_10V 0805
CG179 100nF_Y5V_10V 0402
CG185 100nF_Y5V_10V 0402
CG173 10uF_Y5V_10V 0805
CG191 100nF_Y5V_10V 0402
CG190 1uF_X5R_10V 0402
CG172 100nF_Y5V_10V 0402
CG182 100nF_Y5V_10V 0402
CG192 10uF_Y5V_10V 0805
UG5
GDDR_A_CLK1
GDDR_A_CLK1_R
GDDR_A_CLK#1
RG116 56_5% 0402
RG118 56_5% 0402
CG184 10nF_X7R_16V 0402
TP798 ICT_TP
RG114 4.99K_1% 0402
RG119 4.99K_1% 0402
CG181 100nF_Y5V_10V 0402
RG122 4.99K_1% 0402
RG125 4.99K_1% 0402
CG187 100nF_Y5V_10V 0402
UG5_ZQ
RG80 240_1% 0402
Place around the VRAM UG5
CG176 100nF_Y5V_10V 0402
CG178 100nF_Y5V_10V 0402
CG192 10uF_Y5V_10V 0805
CG174 100nF_Y5V_10V 0402
CG177 1uF_X5R_10V 0402
CG175 100nF_Y5V_10V 0402
CG189 100nF_Y5V_10V 0402
CG171 10uF_Y5V_10V 0805
UG1
TP811 ICT_TP
RG75 4.99K_1% 0402
RG78 4.99K_1% 0402
CG143 100nF_Y5V_10V 0402
RG123 4.99K_1% 0402
RG126 4.99K_1% 0402
CG188 100nF_Y5V_10V 0402
UG1_ZQ
RG120 240_1% 0402
Place around the VRAM UG1
CG140 100nF_Y5V_10V 0402
CG147 100nF_Y5V_10V 0402
CG152 10uF_Y5V_10V 0805
CG146 100nF_Y5V_10V 0402
CG149 1uF_X5R_10V 0402
CG134 100nF_Y5V_10V 0402
CG139 100nF_Y5V_10V 0402
CG137 10uF_Y5V_10V 0805
DIS(M93 XT);PX : Install
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Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
Title
VRAM (DDR3)
Size
Custom
Document Number
CHICAGO
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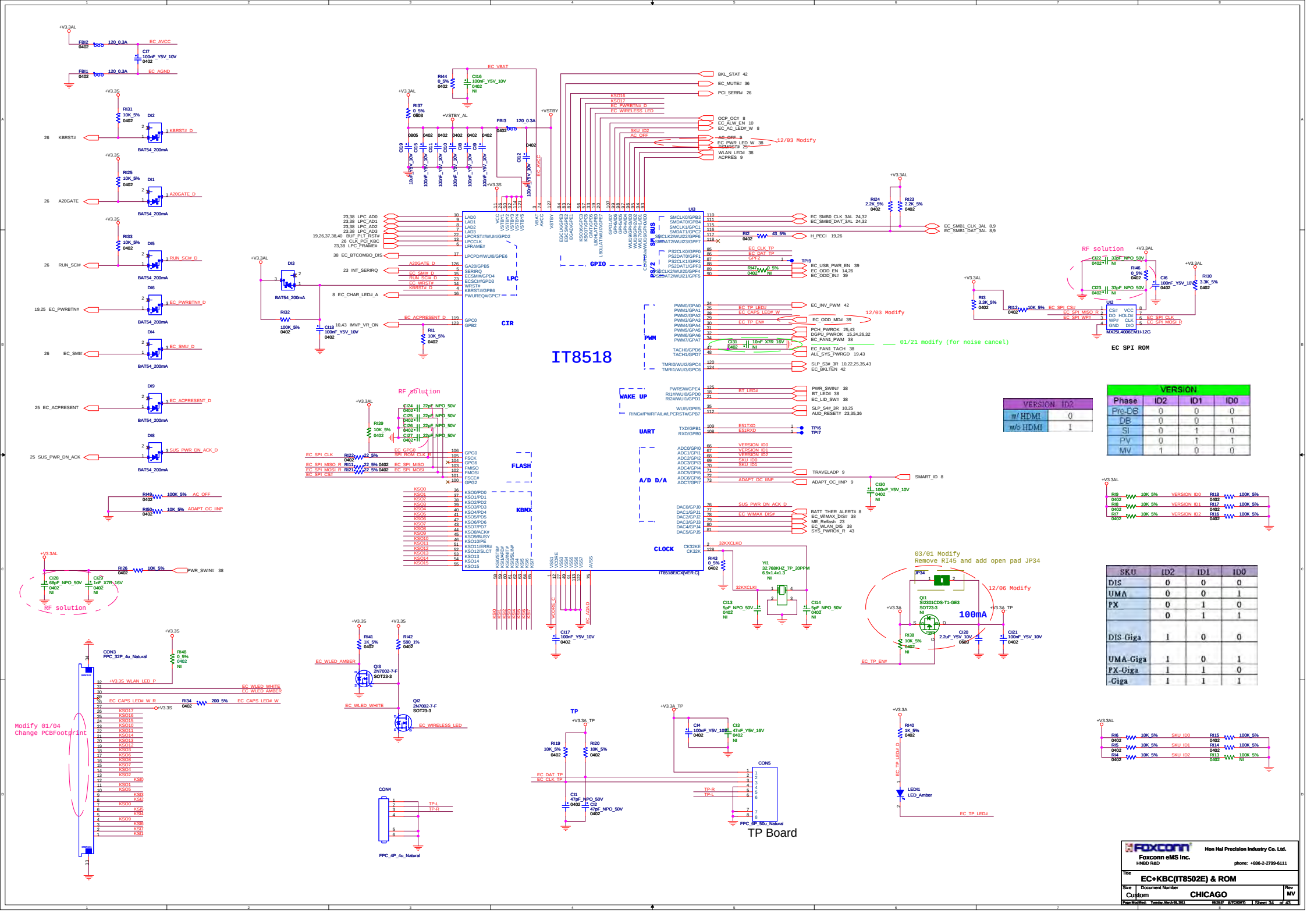
IT8518
IT8518E/CX[VER.C]
LPC
CIR
FLASH
KBMX
GPIO
SMB
PWM
WAKE UP
UART
A/D D/A
CLOCK
RF solution
03/01 Modify
Remove RI45 and add open pad JP34
12/06 Modify
12/03 Modify
01/21 modify (for noise cancel)
100mA
Modify 01/04
Change PCBFootprint
TP Board
EC SPI ROM
VERSION
Phase ID2 ID1 ID0
Pre-DB 0 0 0
DB 0 0 1
SI 0 1 0
PV 0 1 1
MV 1 0 0
VERSION_ID2
w/ HDMI 0
w/o HDMI 1
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
Foxconn
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HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
Title
EC+KBC(IT8502E) & ROM
Size
Custom
Document Number
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MV
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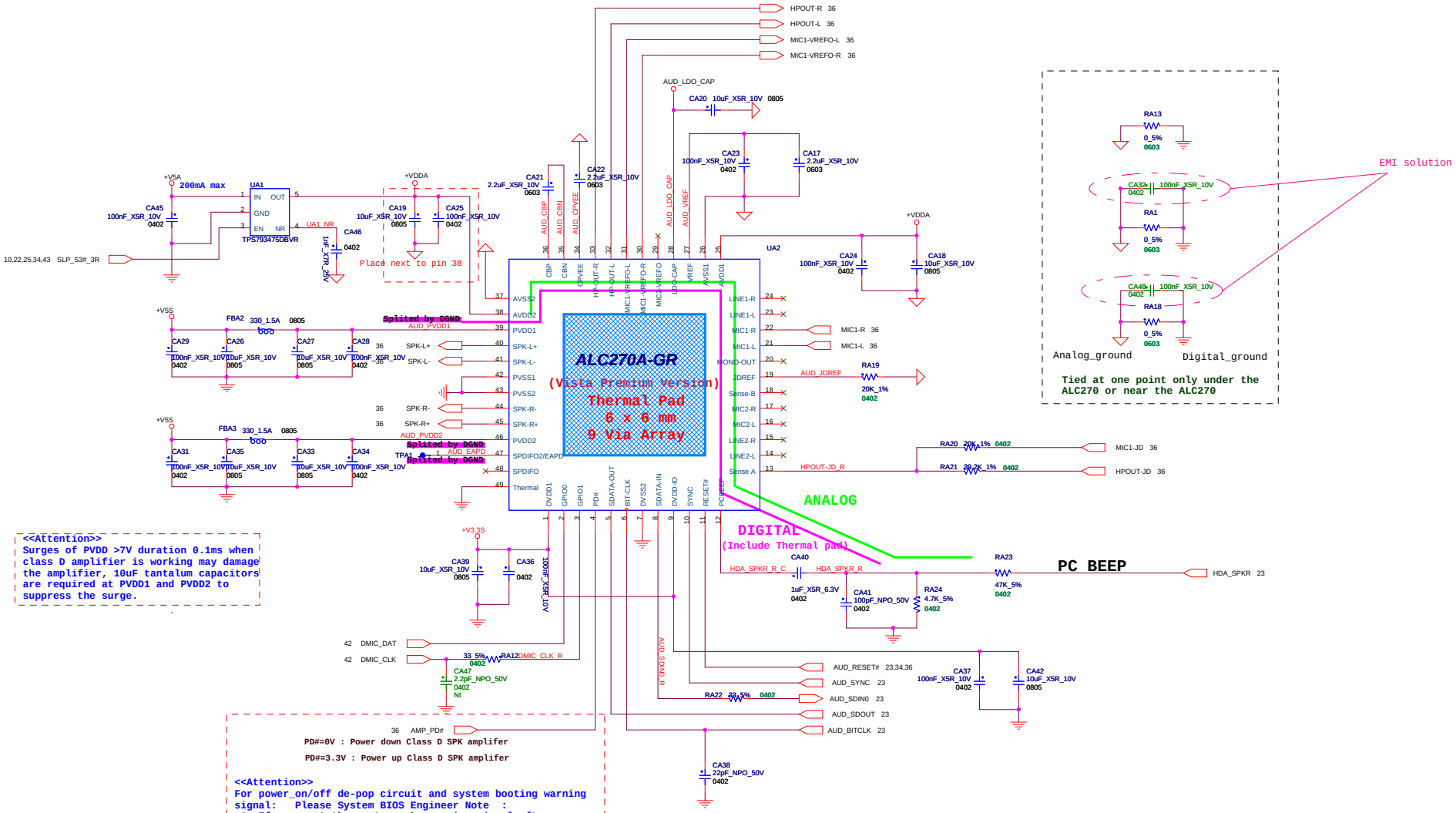

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Title: Audio (CODEC_ALC270A)		
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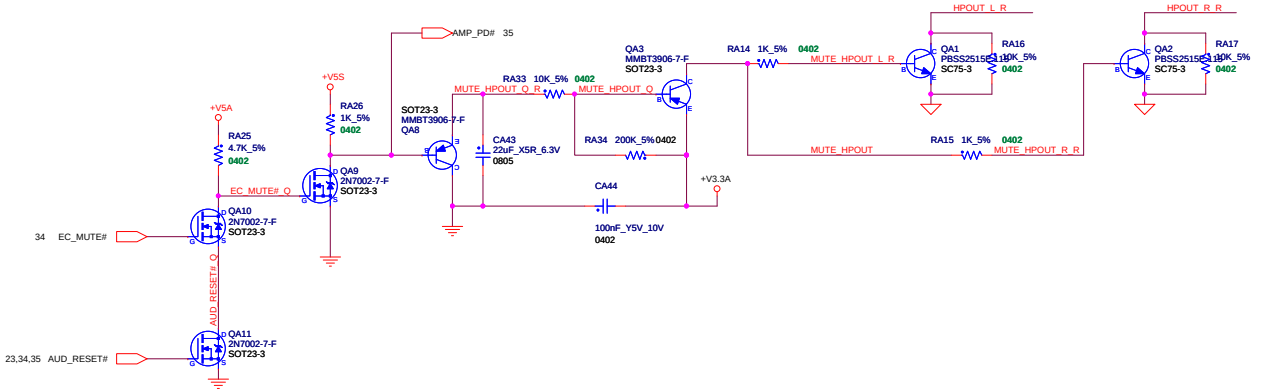
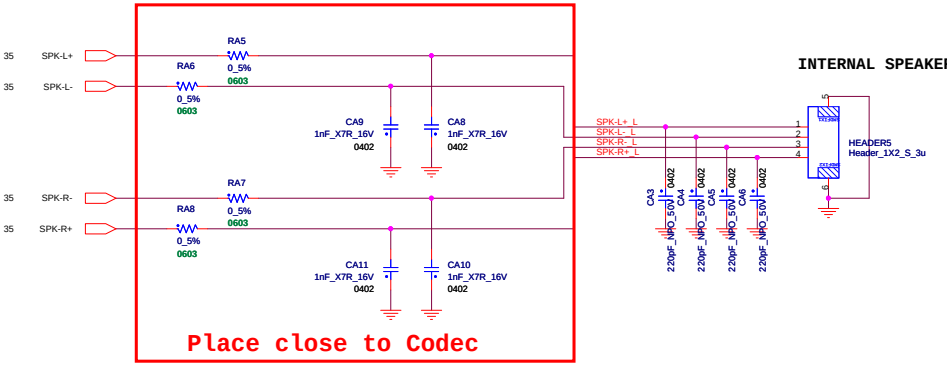
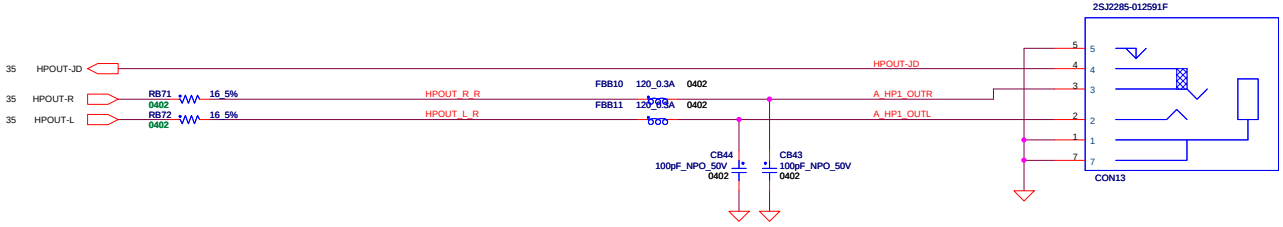
Mute



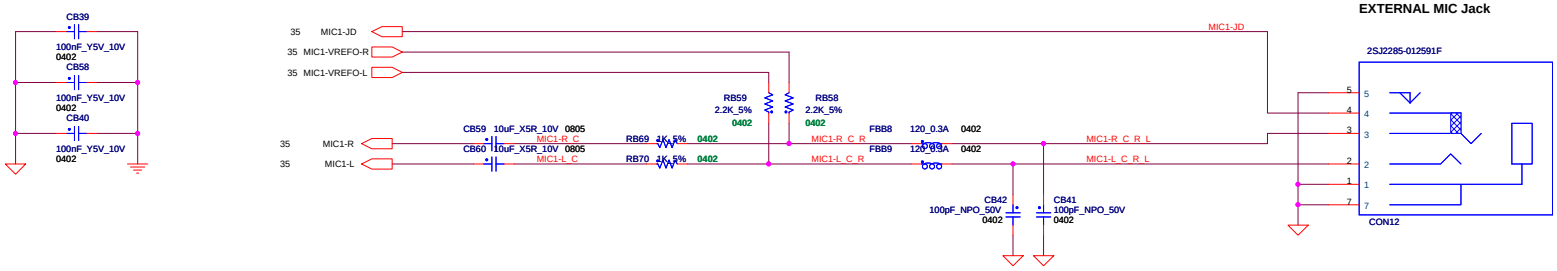
INTERNAL SPEAKER



HEADPHONE Jack



EXTERNAL MIC Jack



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HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111

Title: Audio (JACK+AMP+SPK+Mute)

Size: Custom | Document Number: CHICAGO | Rev: MV

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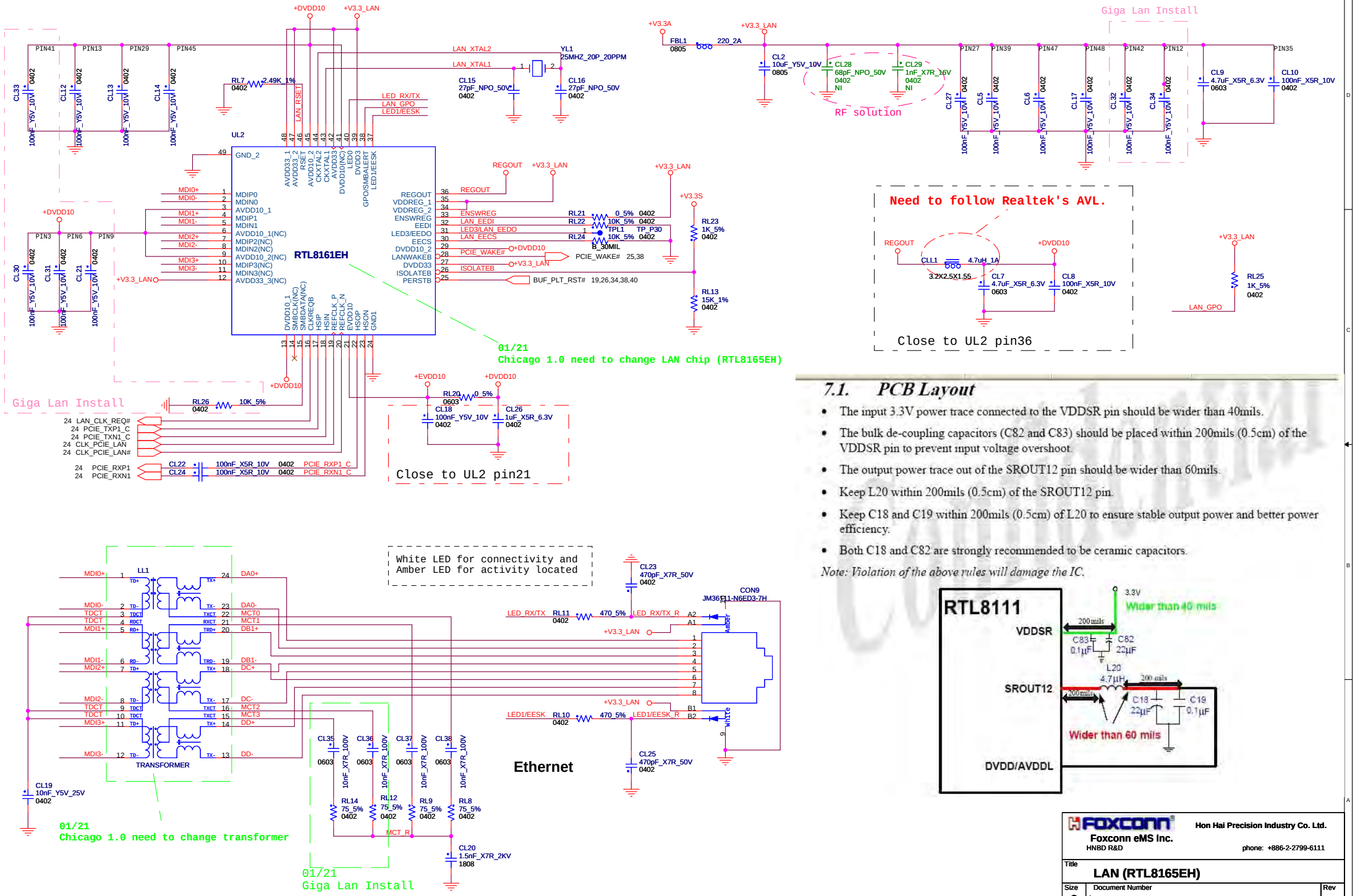

7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.

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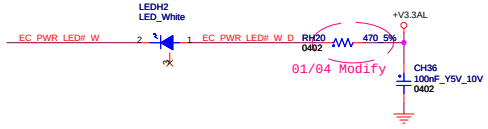
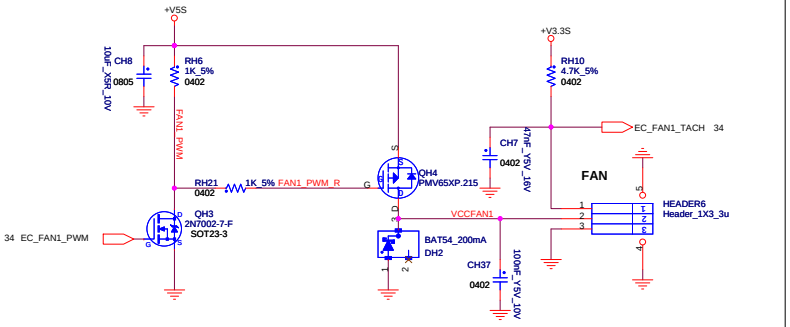
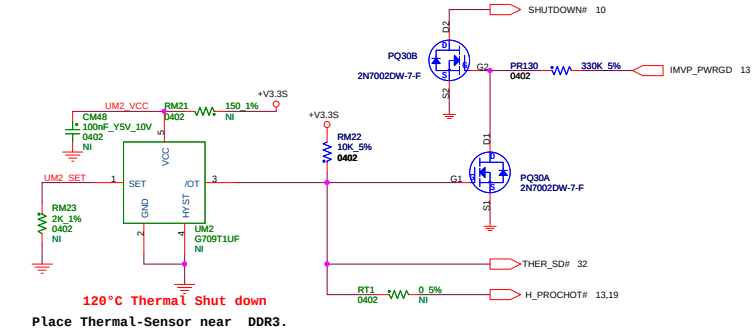
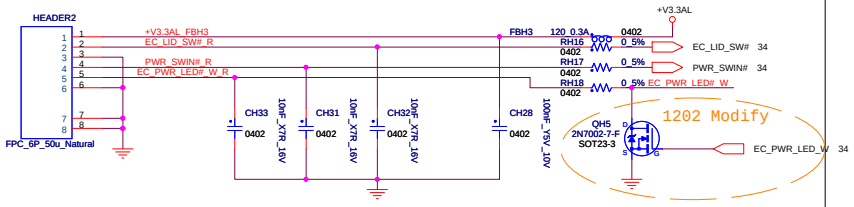
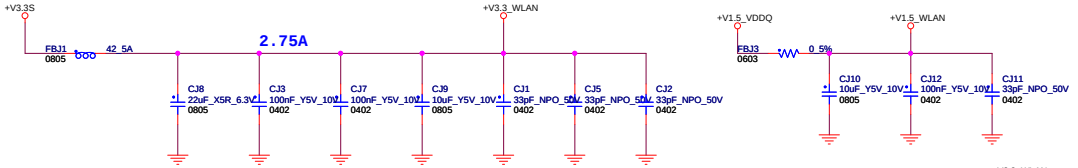


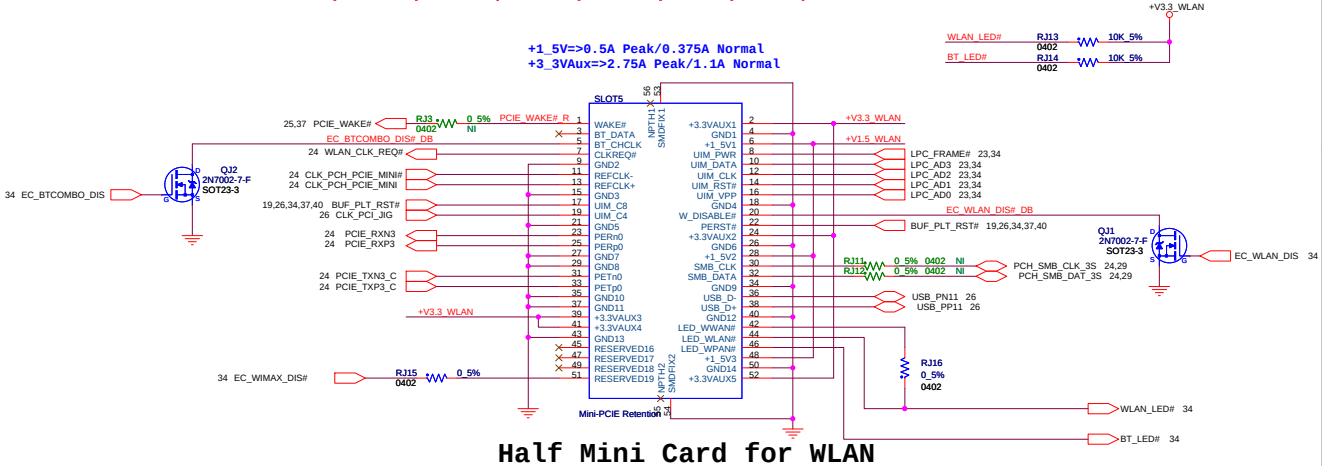




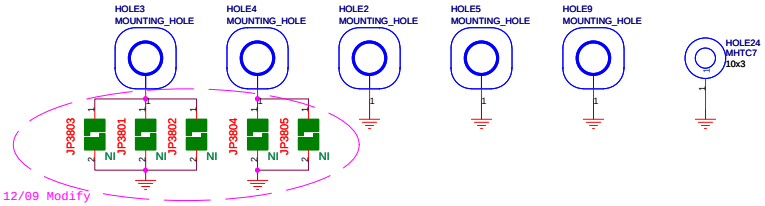
PWR Board CONN.

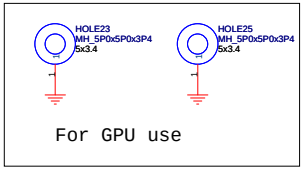


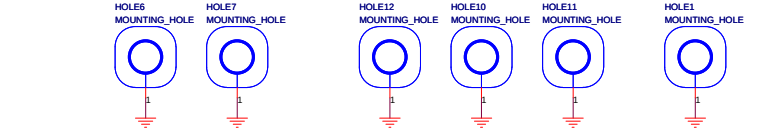


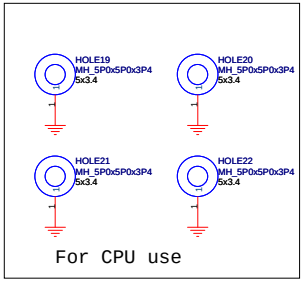


Half Mini Card for WLAN



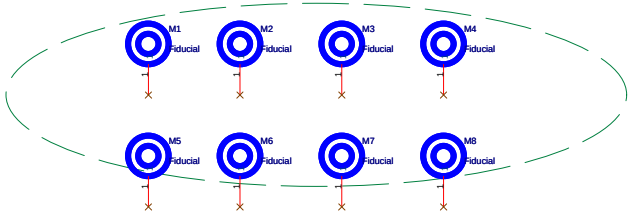






Mounting HOLE

02/09 Modify
Change PCBfootprint from FIDUCIAL_1P_3P_B to FIDUCIAL_MARK



Fiducial Mark

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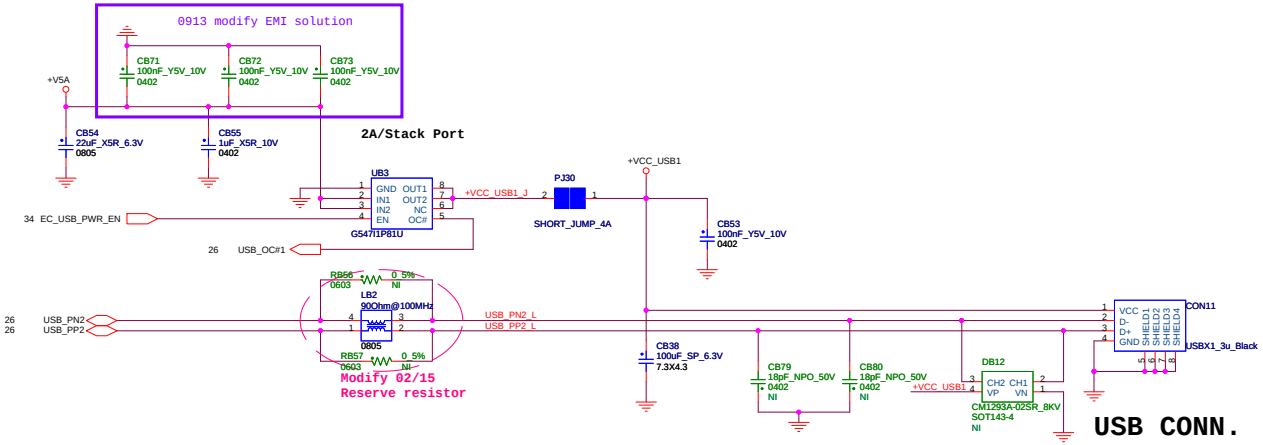
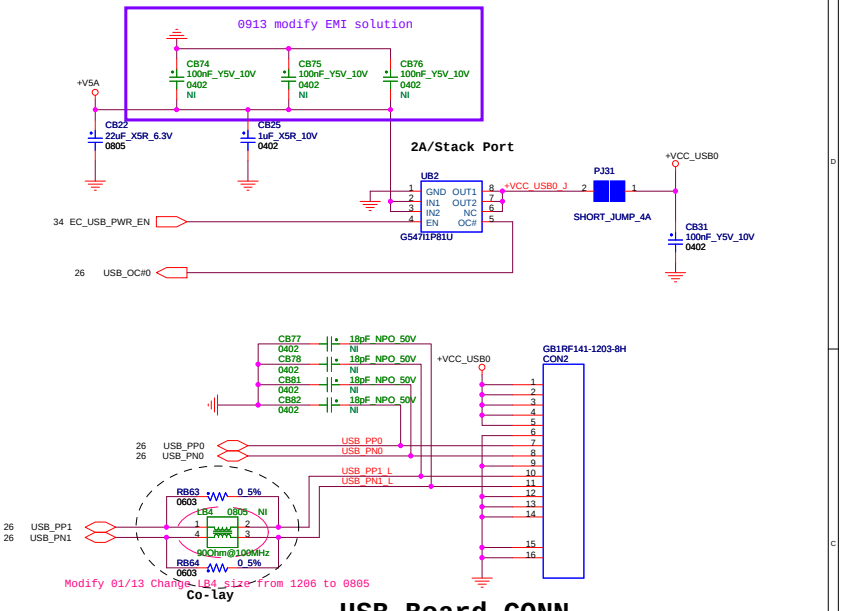
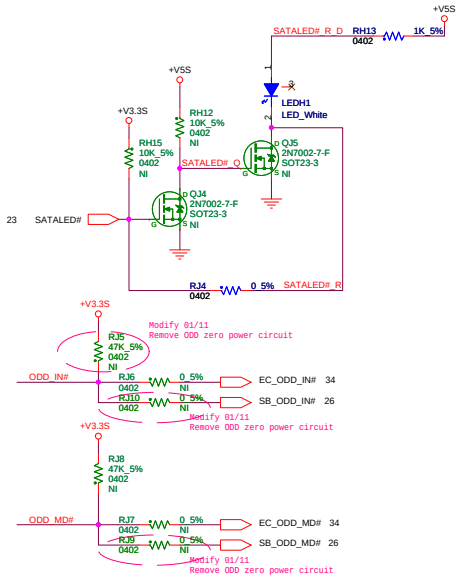


USB CONN.

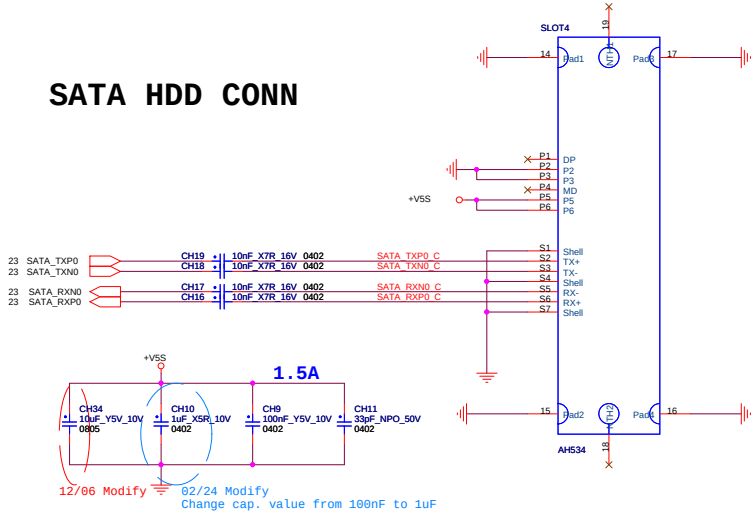


USB Board CONN.

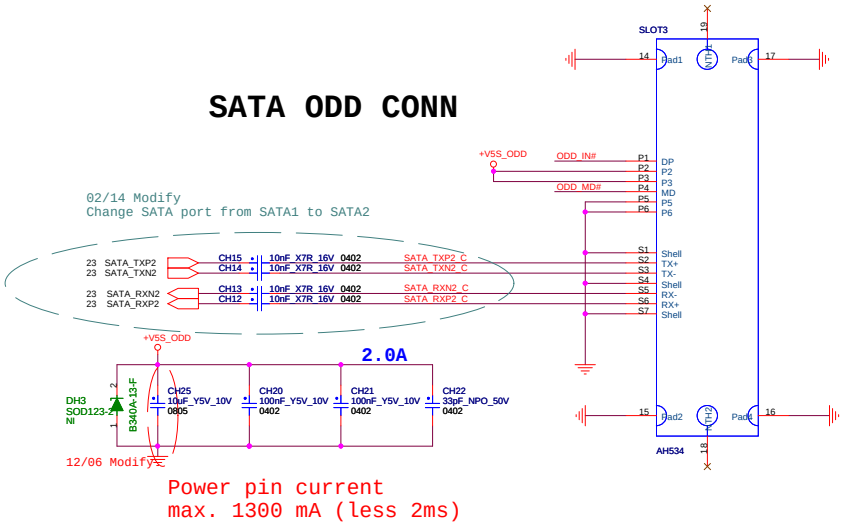
HDD/ODD Status LED



SATA HDD CONN



SATA ODD CONN



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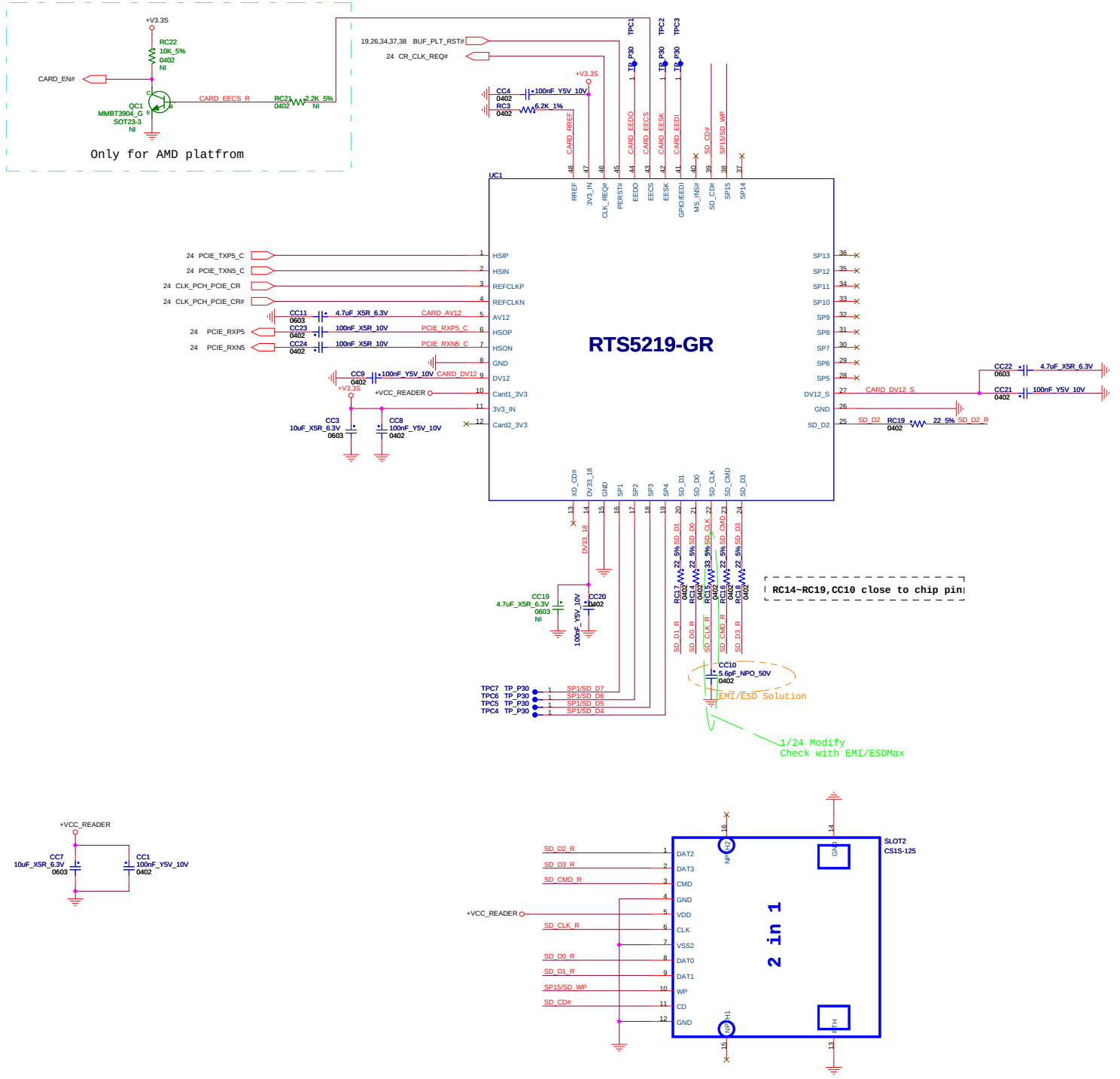

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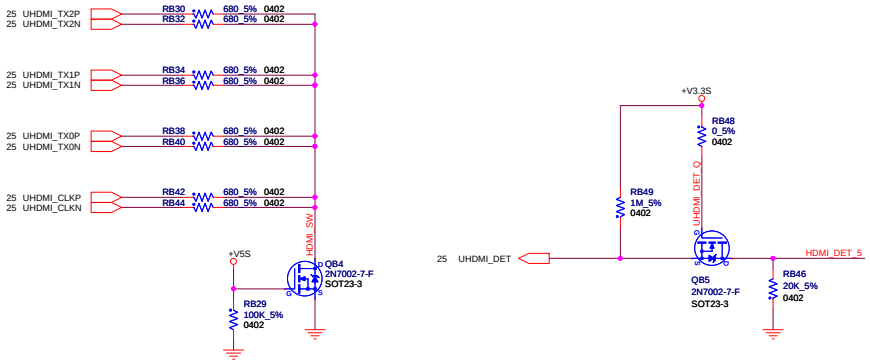
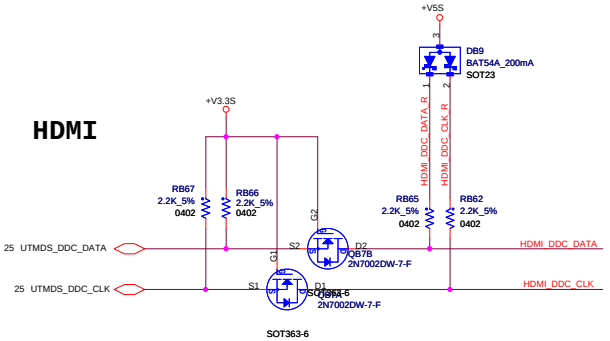
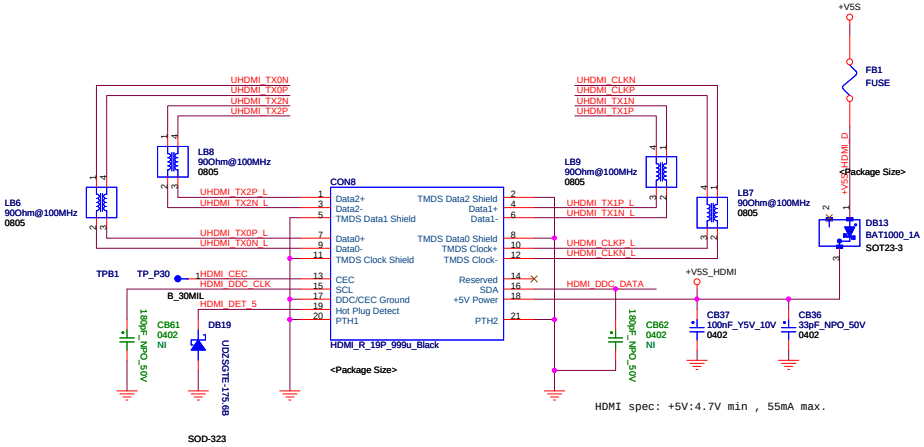


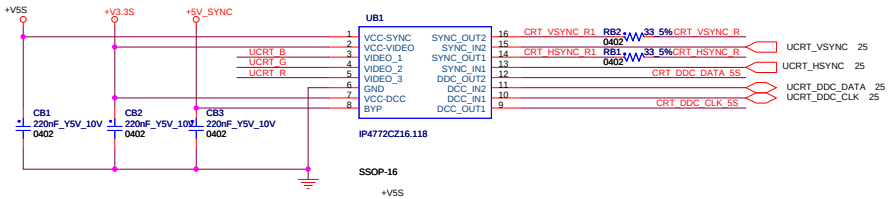
HDMI

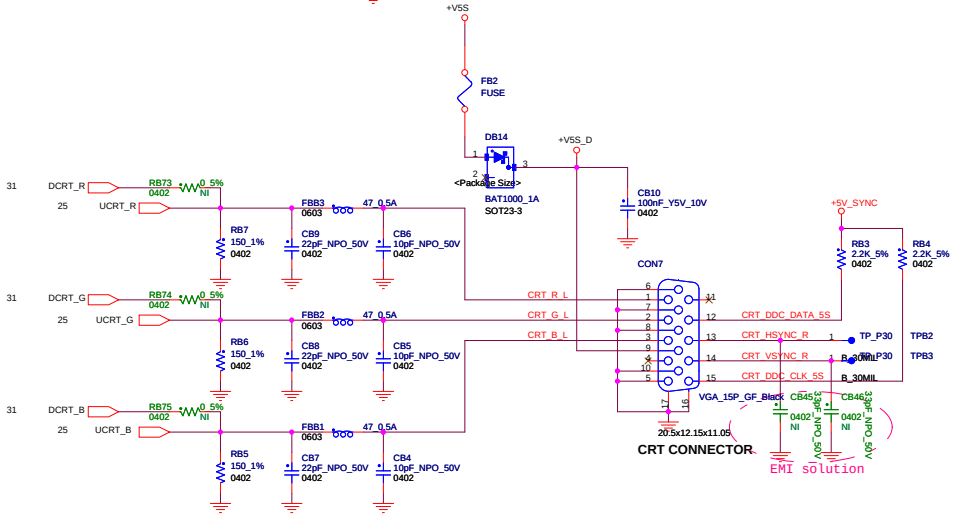




HDMI spec: +5V:4.7V min , 55mA max.

CRT





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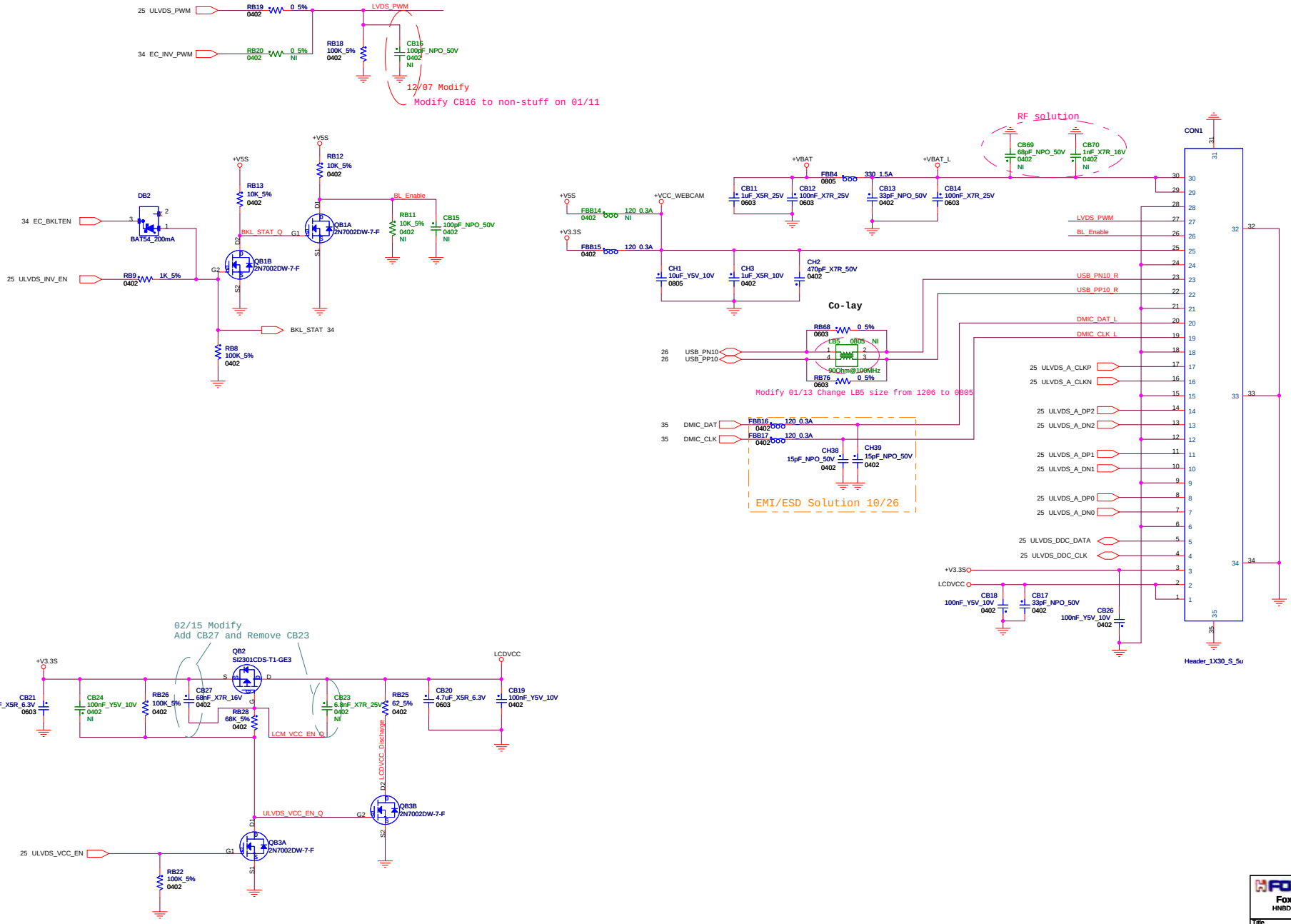

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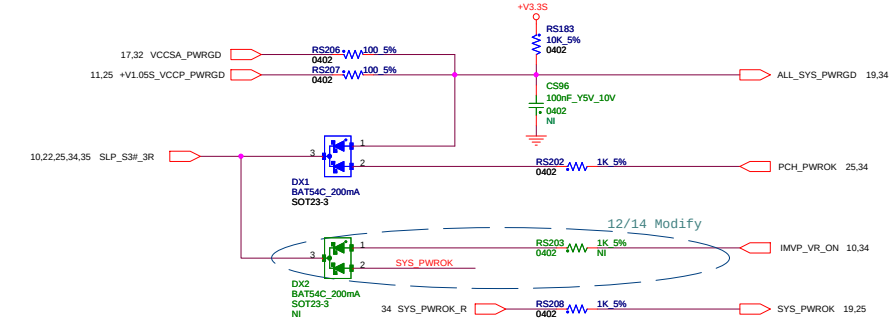
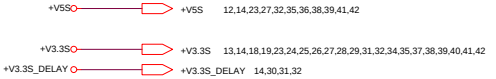
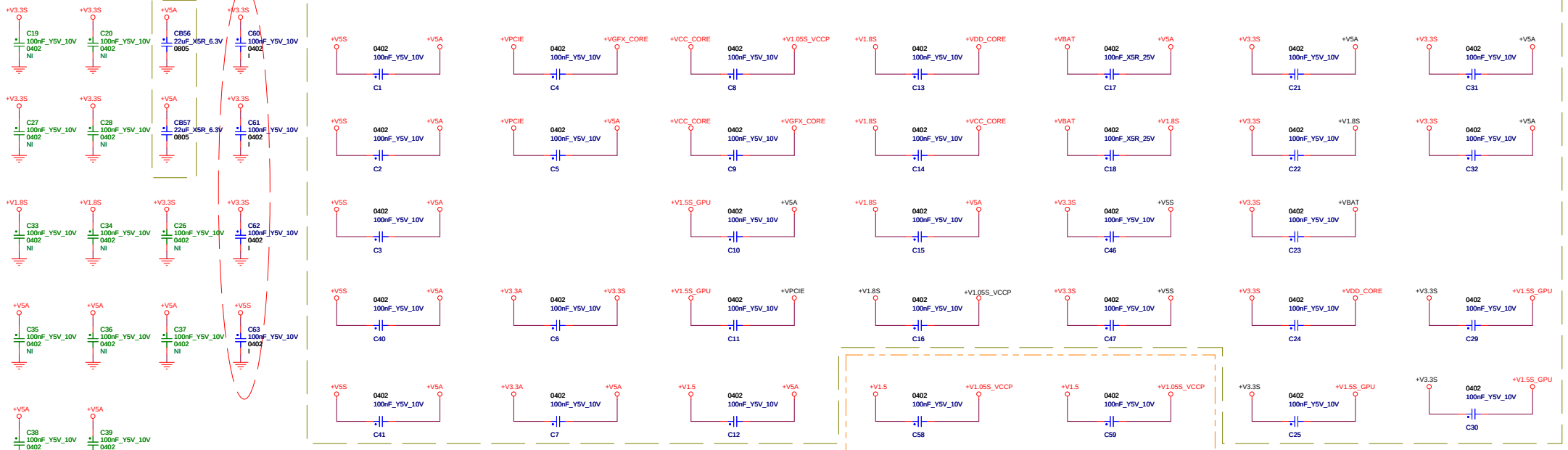




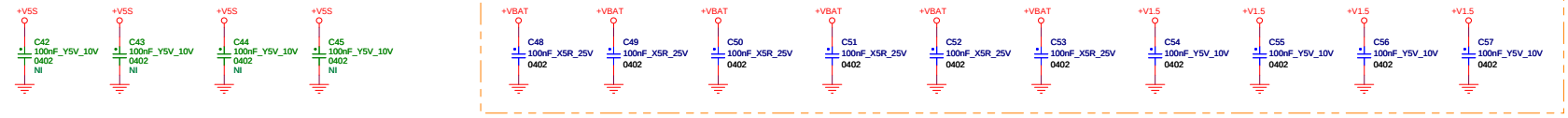
12/07 Modify

1117 Modify

Modify 11/11



EMI/ESD Solution 10/26



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