PROJECT : CHICAGO (For Intel Huron River Platform)

P. Leader	Check by	Design by

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Title: **Index Page**

Size	Document Number	Rev
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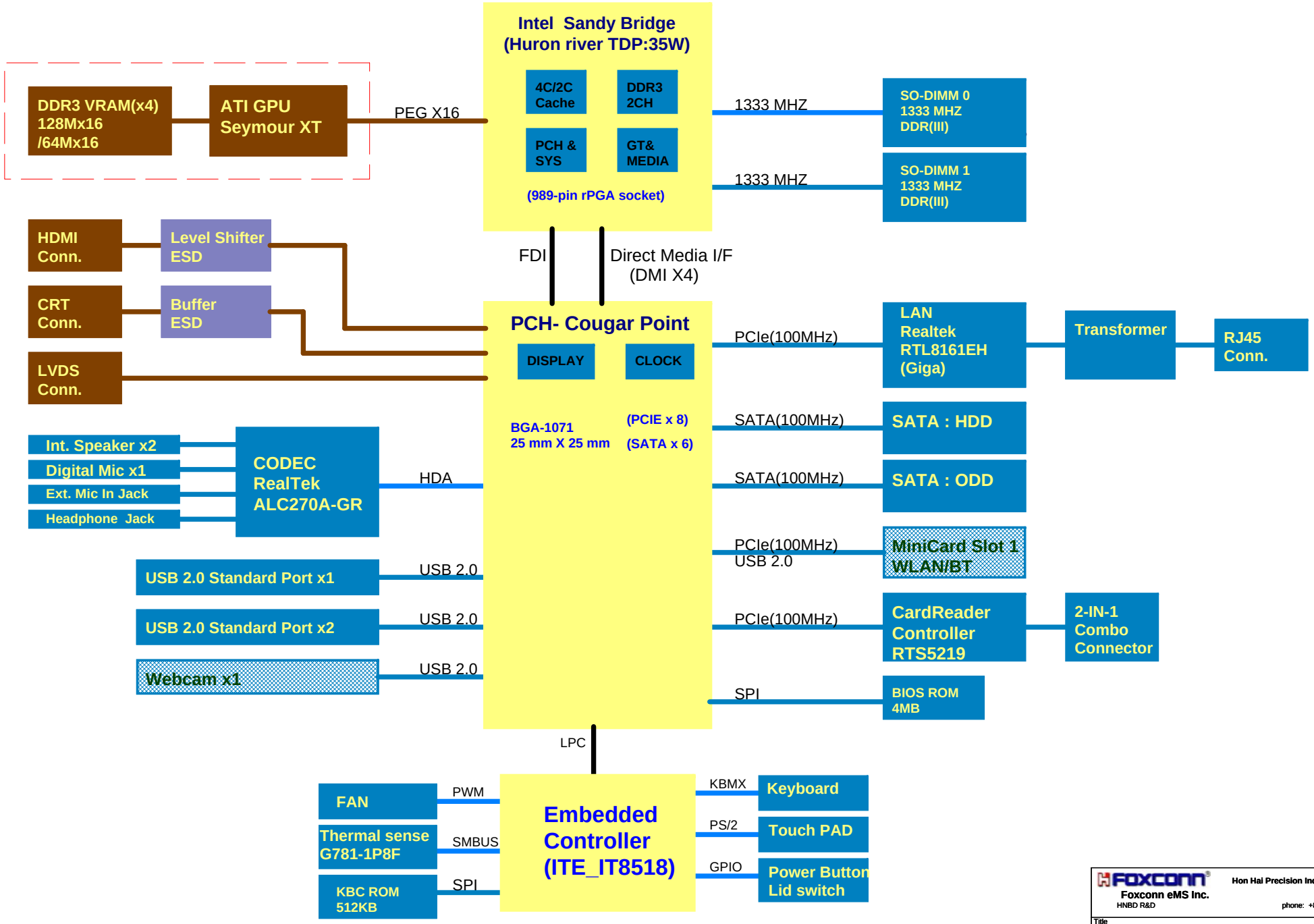

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Title: SYSTEM BLOCK DIAGRAM

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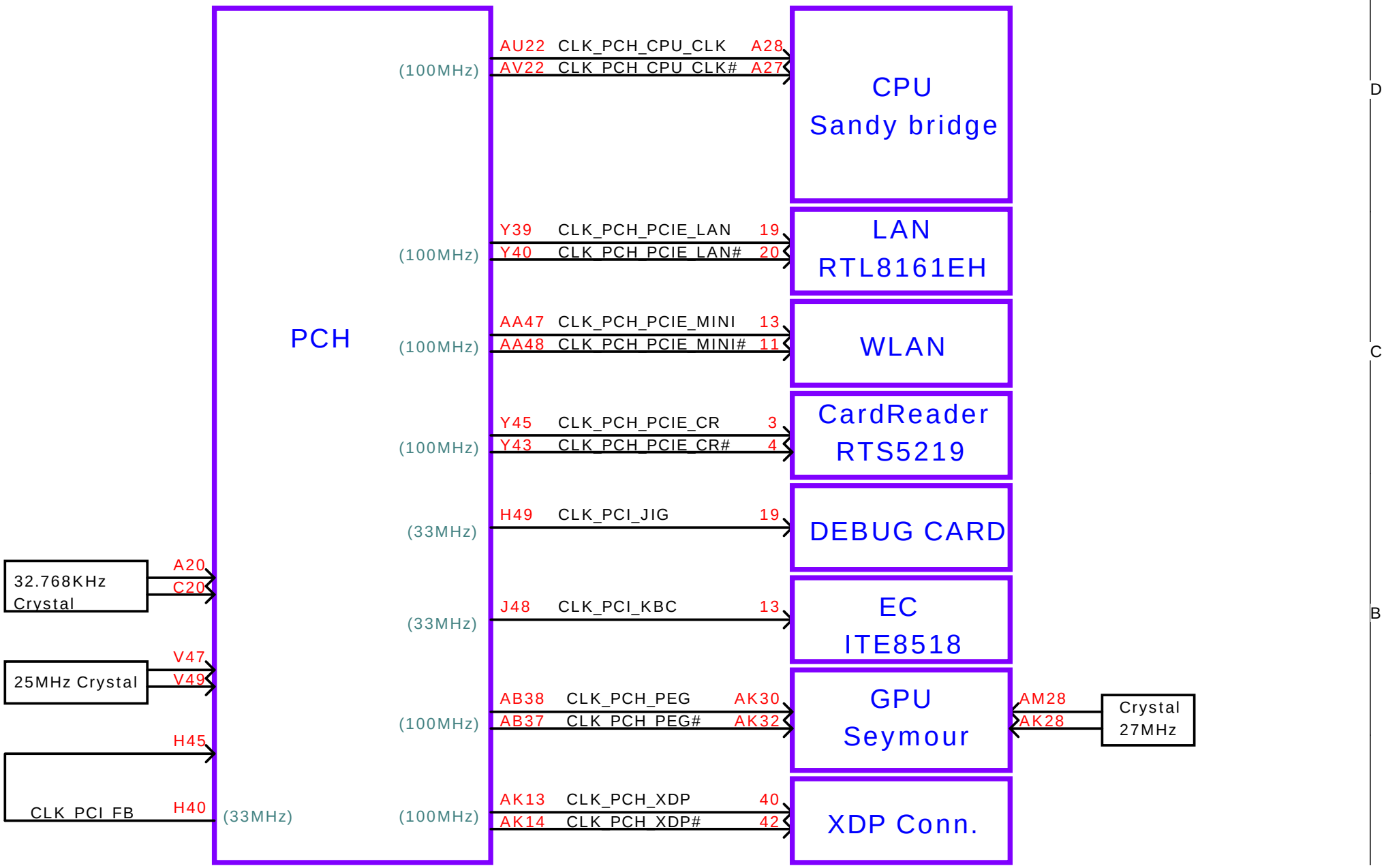

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Title: CLOCK MAP

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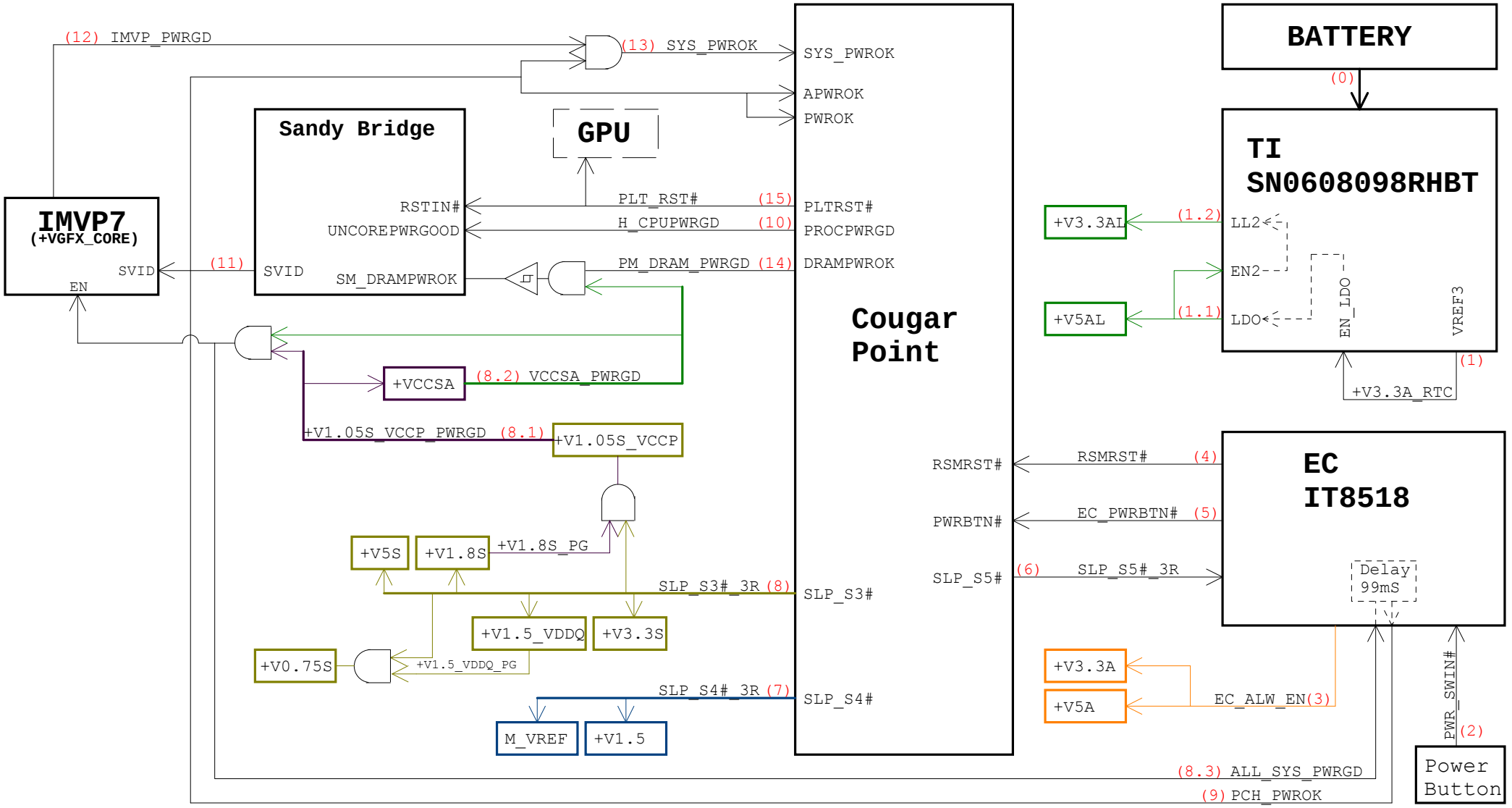

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Title: POWER SEQUENCY DIAGRAM

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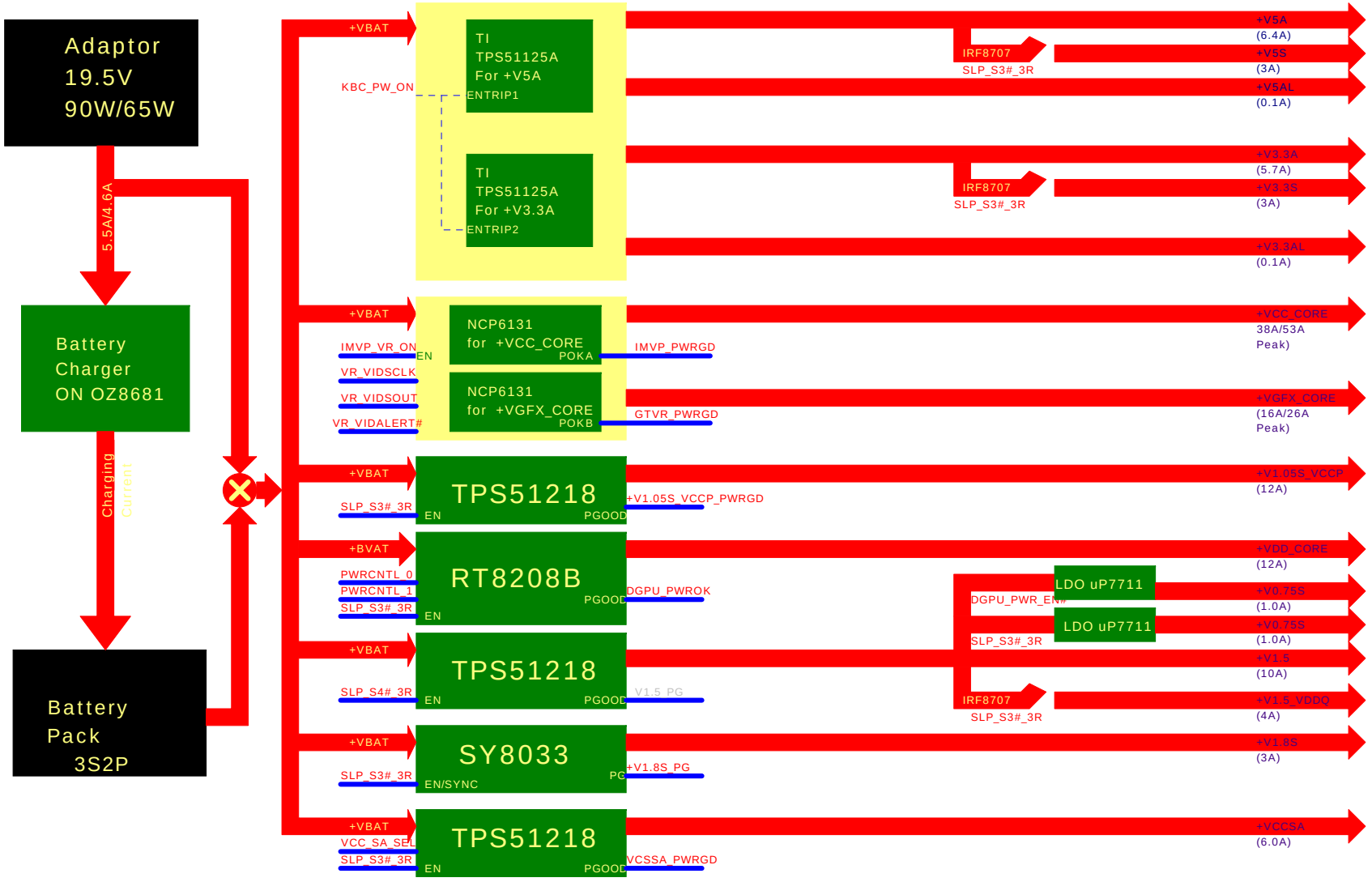
POWER MAP



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Title		
POWER MAP		
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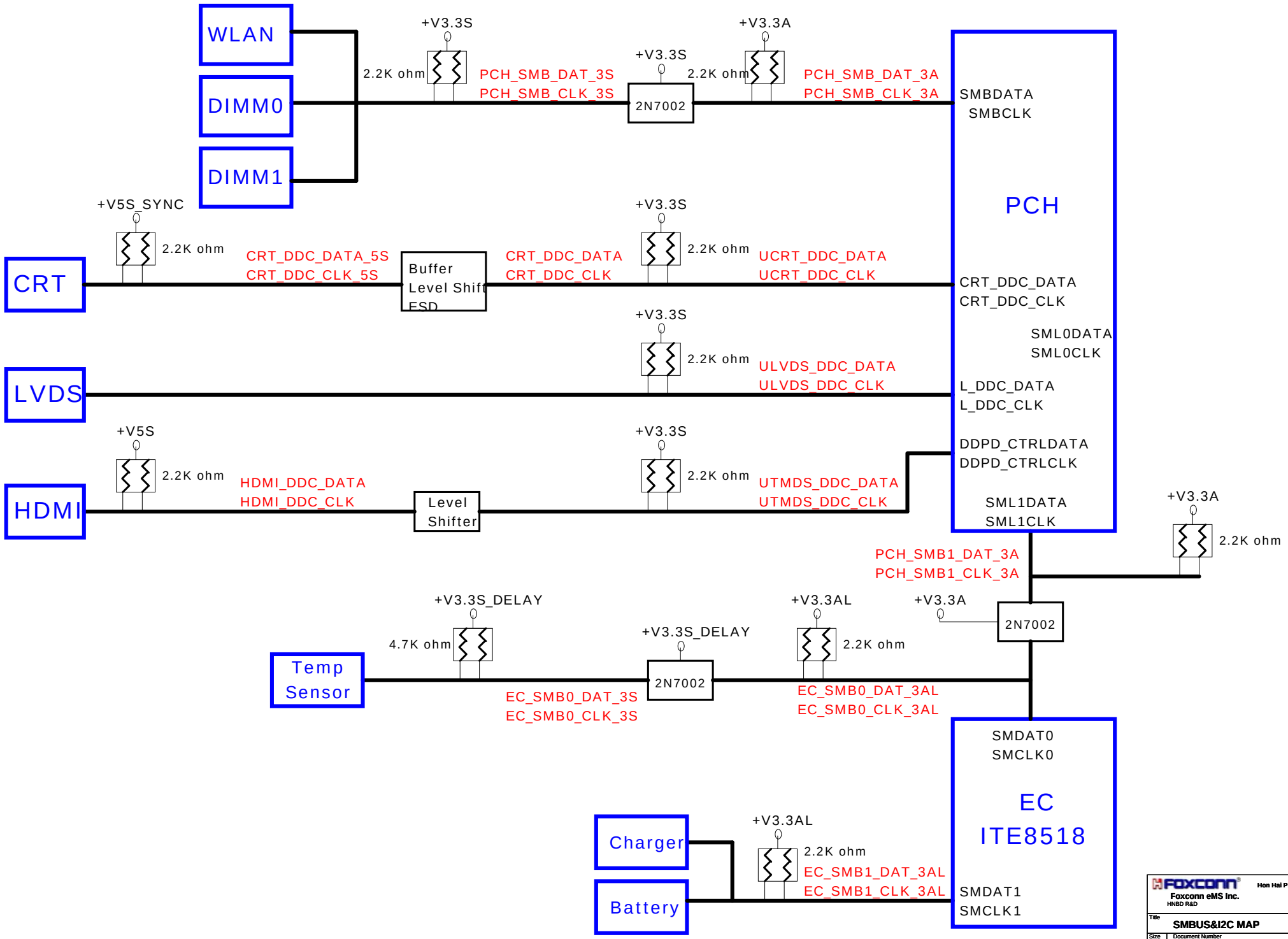

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Title: SMBUS&I2C MAP

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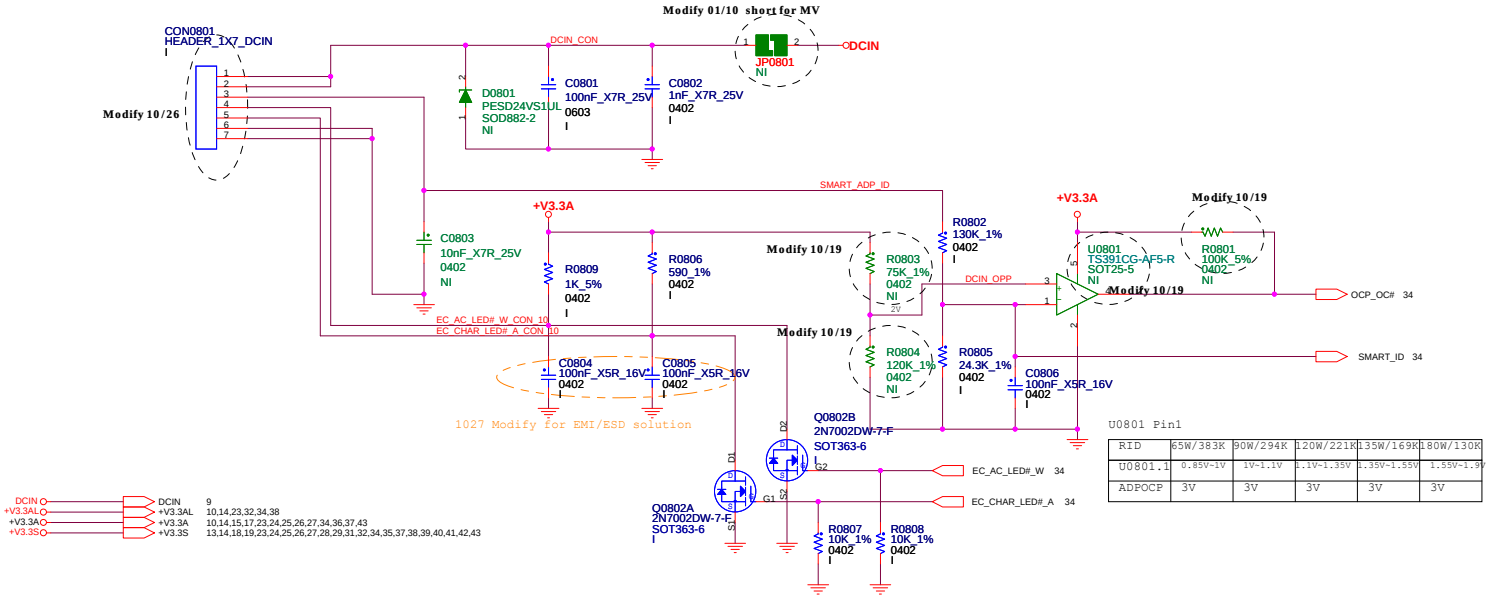
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

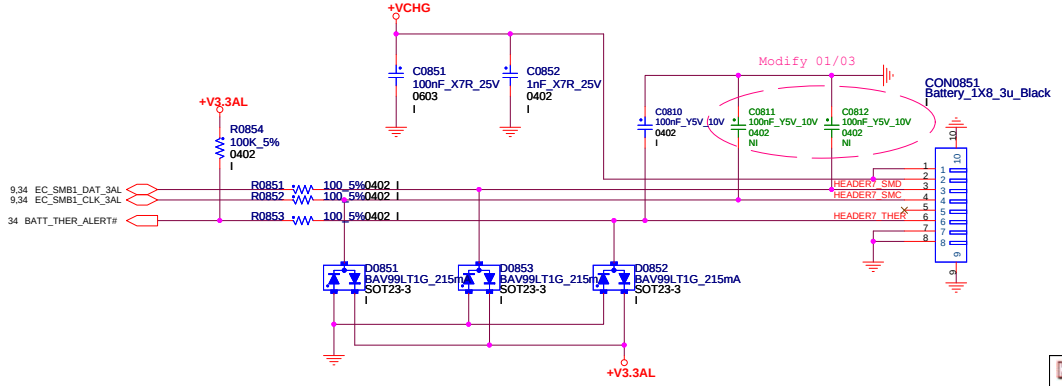


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.85V~1V	1V~1.1V	1.1V~1.35V	1.35V~1.55V	1.55V~1.9V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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Size	Document Number: CHICAGO		Rev: MV
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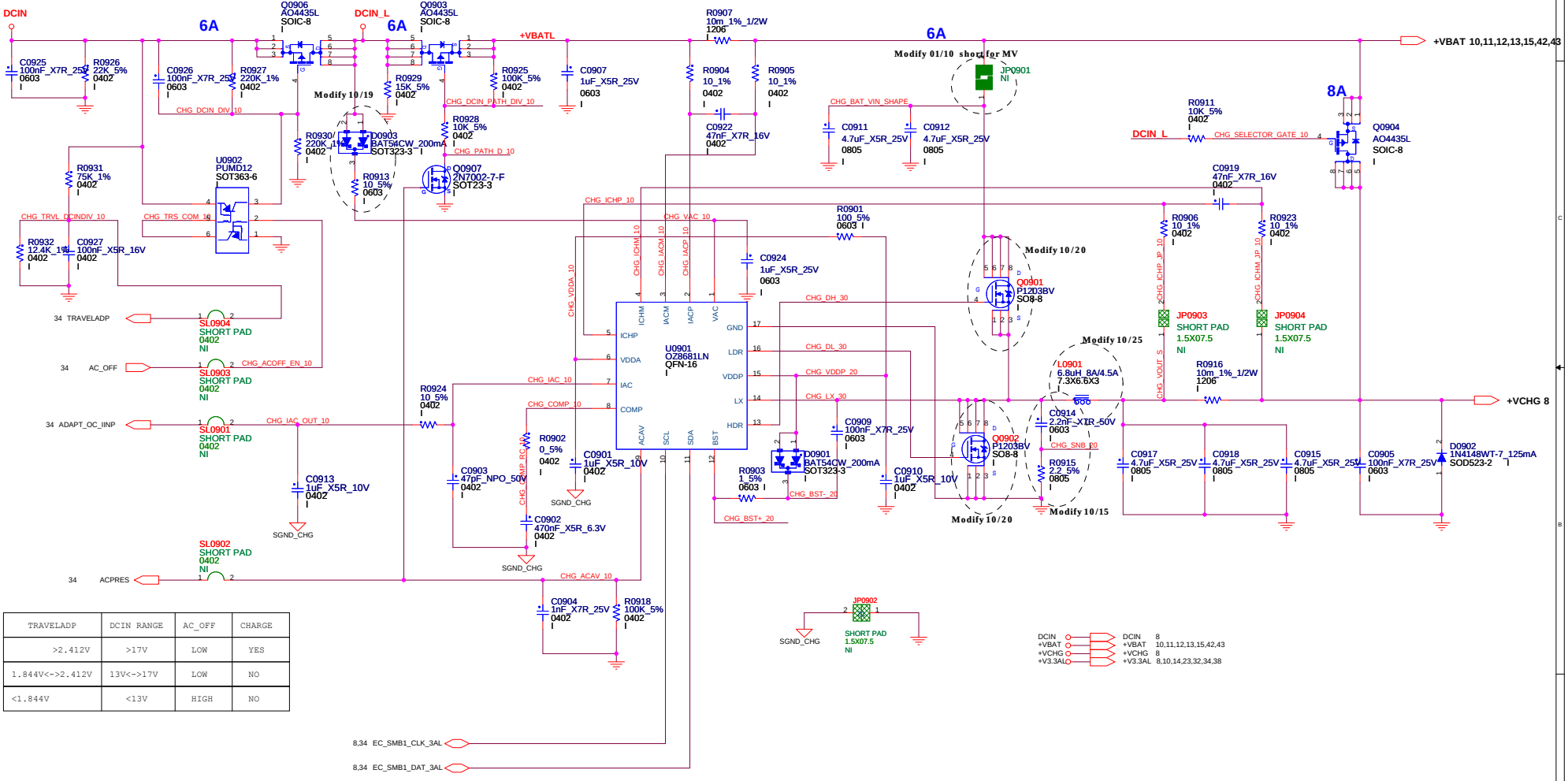
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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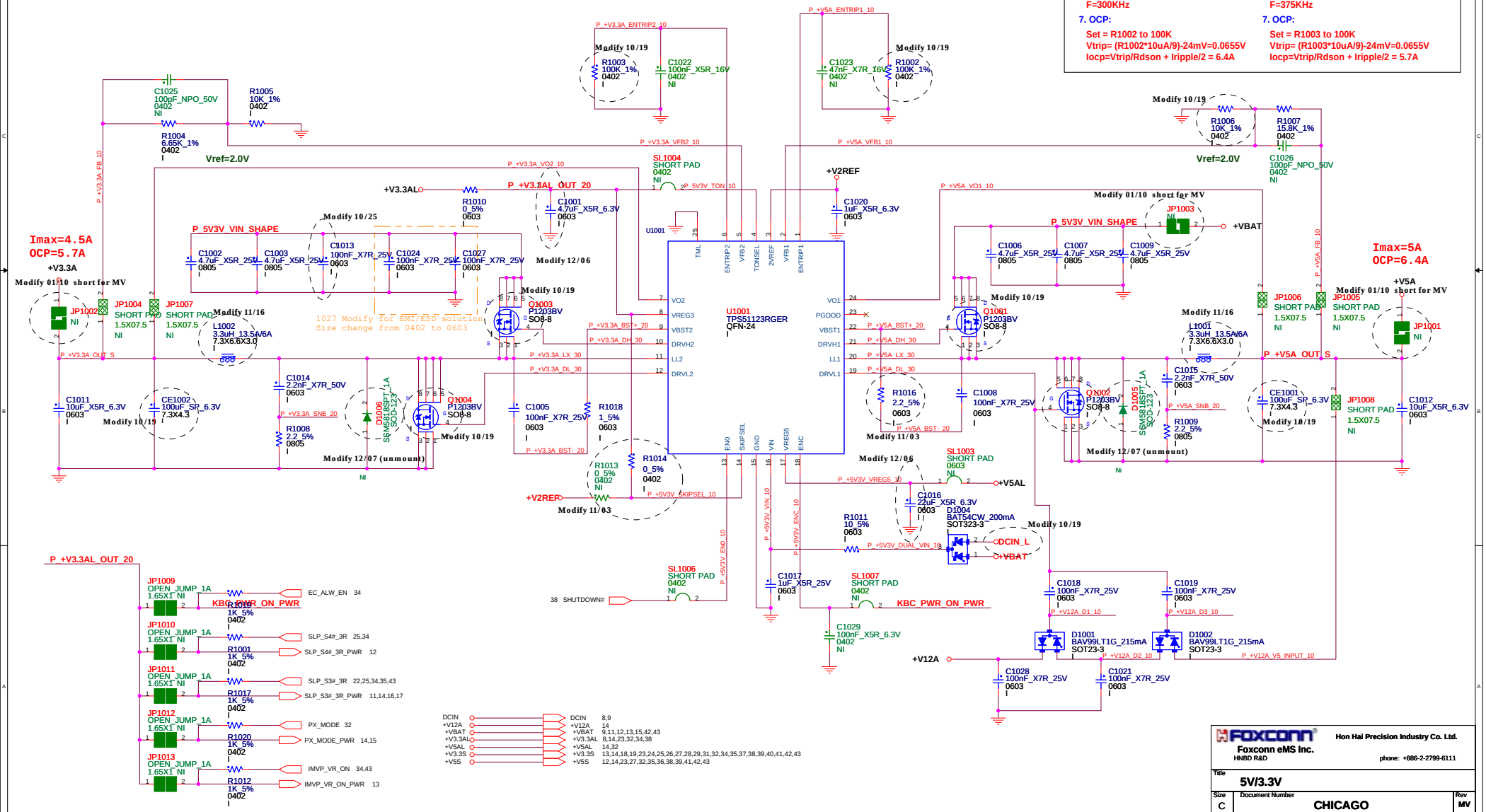
+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current:	1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=3.7A	Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:	2.Ripple Current:
Irip=3.72A	Irip=2.21A
3. Ripple Voltage:	3.Ripple Voltage:
ESR/1=15mohm Vrip=55.8mV	ESR/1=15mohm Vrip=33.15mV
4. Inductor Spec:	4.Inductor Spec:
Isat=13.5A Idc=6A DCR=30mohm	Isat=13.5A Idc=6A DCR=30mohm
5.MOSFET Spec:	
H-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)	L-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)
6. Frequency:	6. Frequency:
F=300KHz	F=375KHz
7. OCP:	7. OCP:
Set = R1002 to 100K Vtrip= (R1002*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	Set = R1003 to 100K Vtrip= (R1003*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



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Title: 5V/3.3V		
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+VTT POWER SUPPLY

2010.1103.0

+V1.05S_VCCP:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.24A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

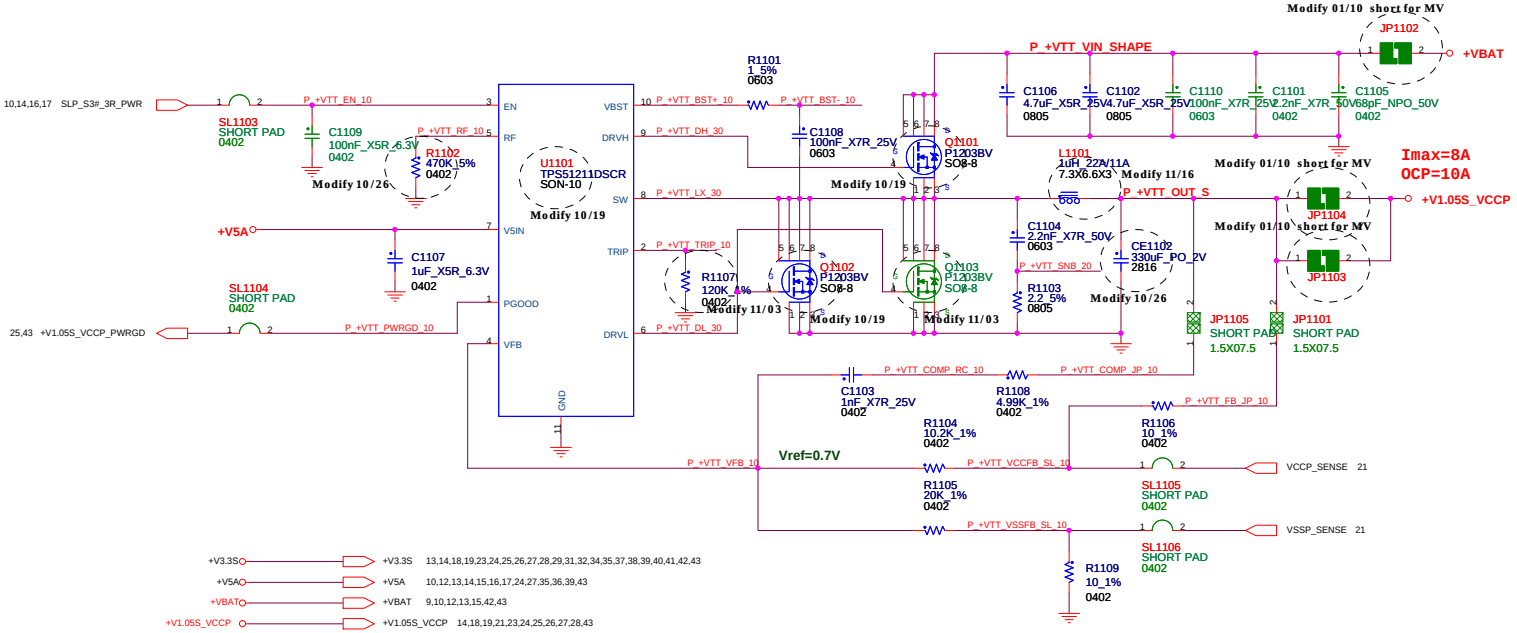
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:

F=290KHz (R1102=0ohm)

7. OCP:

Set = R1107 to 120K
Vtrip= R1107*10uA=1.2V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A



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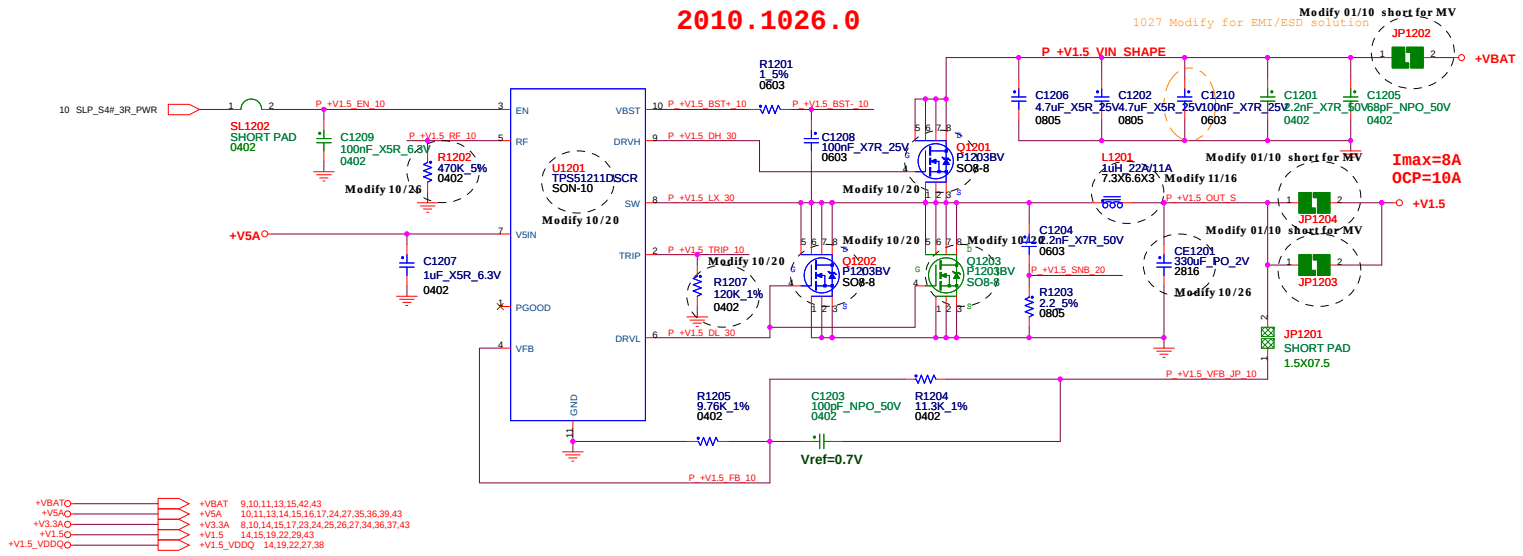
+V1.5 POWER SUPPLY

2010.1026.0



+V1.5:

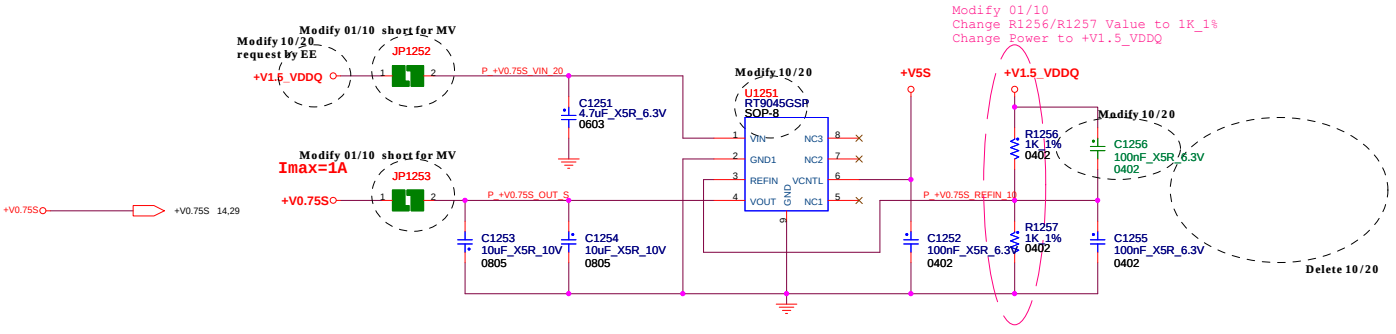
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
   Irip=3.34A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.6mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:
   F=290KHz (R0902=0ohm)
7. OCP:
   Set = R1207 to 120K
   Vtrip= R1207*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

+V0.75S POWER SUPPLY

2010.1026.0



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Title: 1.5VDDR3/0.75V		
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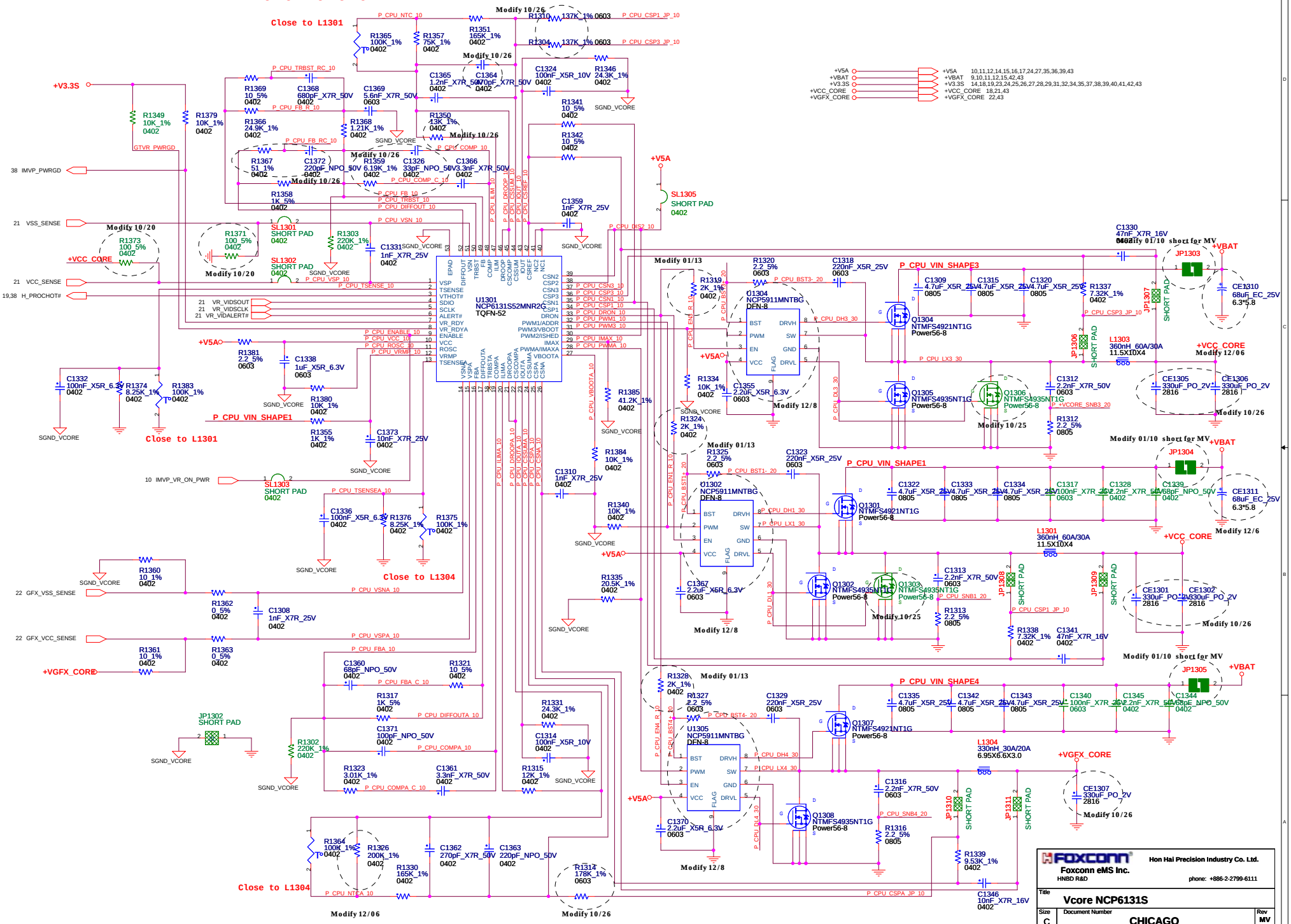
IMVP7 CPU VCORE POWER SUPPLY

2010.1026.0



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Title: Vcore NCP6131S

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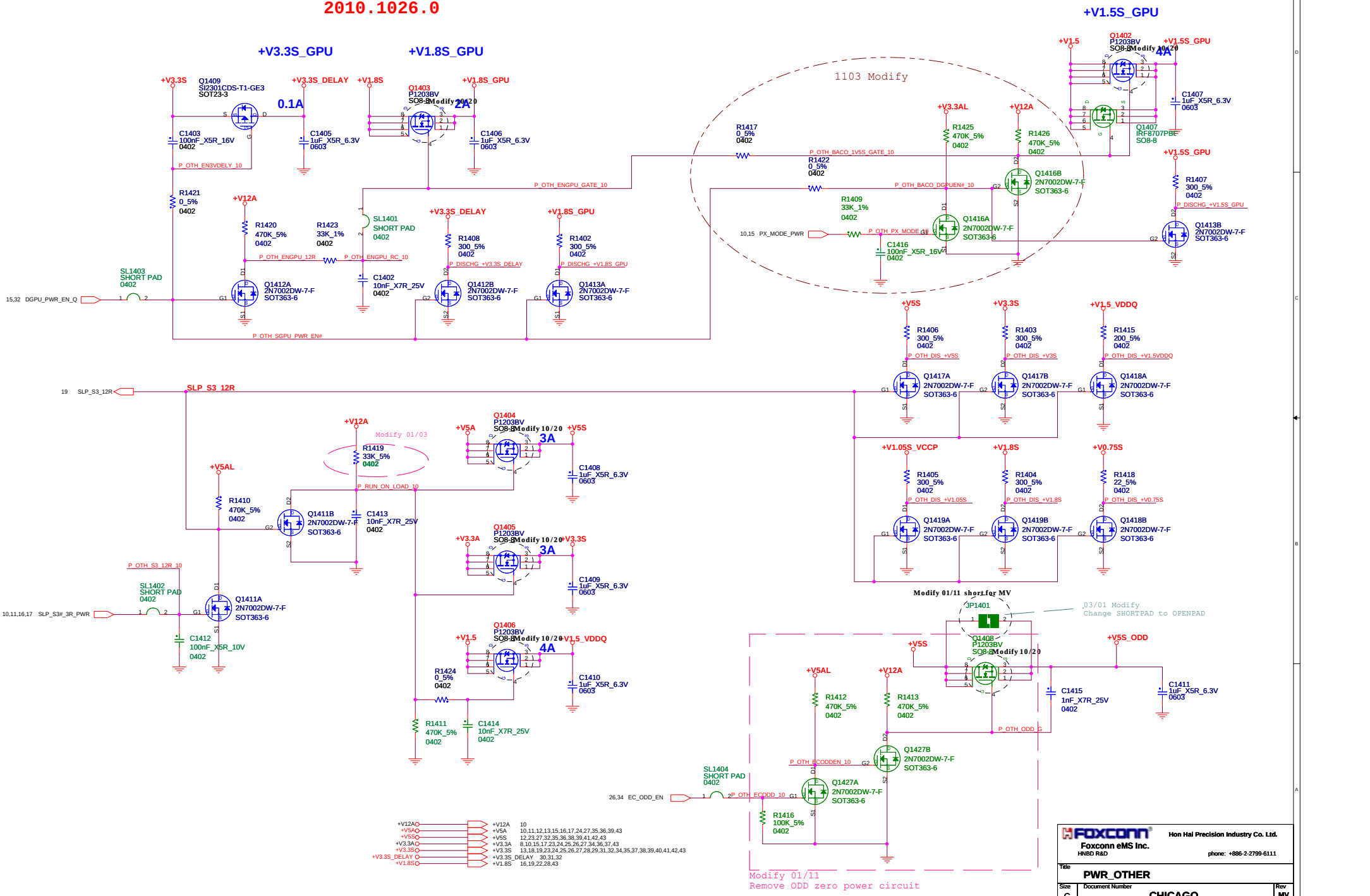
OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



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Title	PWR_OTHER
Size: C	Document Number: CHICAGO
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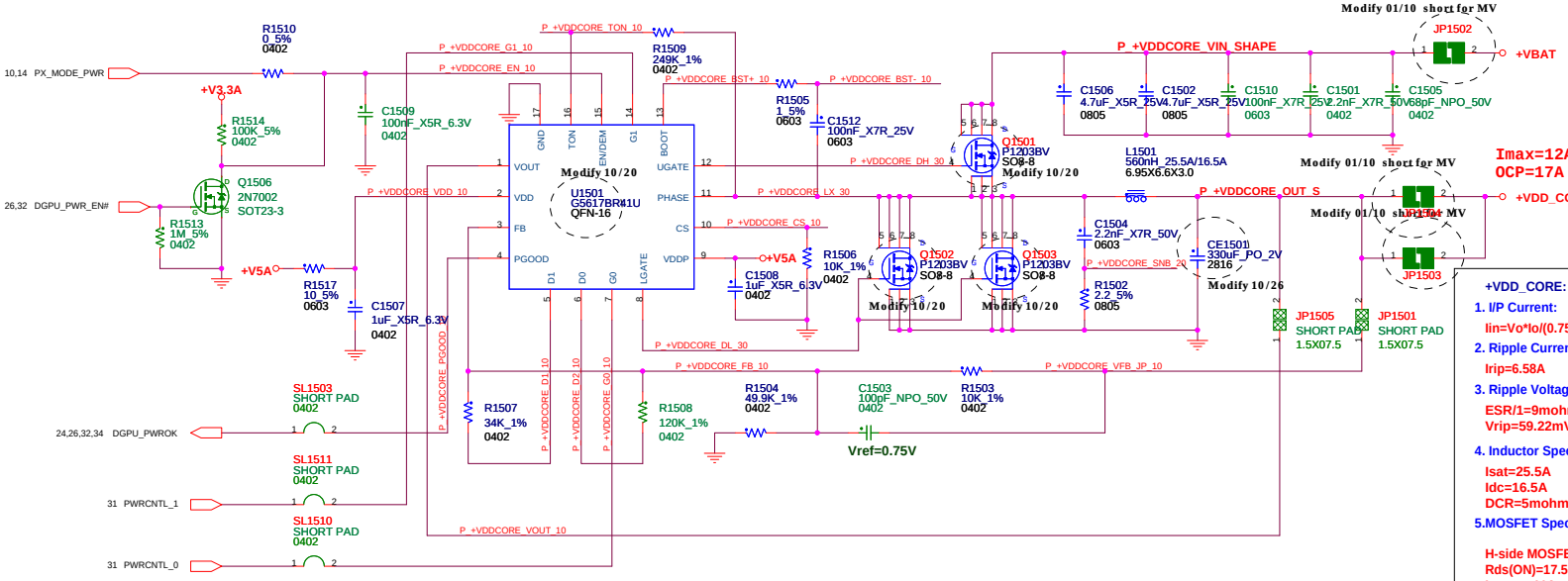
+VDD_CORE POWER SUPPLY

2010.1026.0



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.48A

2. Ripple Current:

Irip=6.58A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=59.22mV

4. Inductor Spec:

Isat=25.5A
Idc=16.5A
DCR=5mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

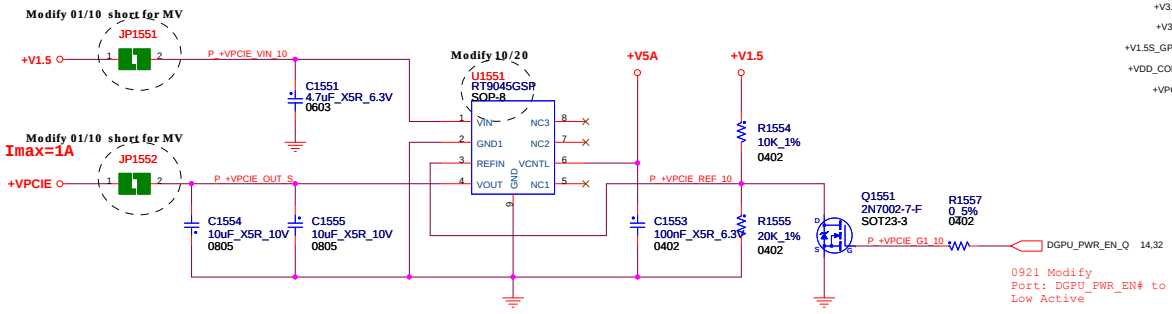
6. Frequency:

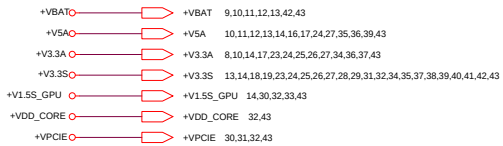
TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns
F=VOUT/(VIN*TON)=286KHz

7. OCP:

Set = R1506 to 10K
Vtrip= R1206*10uA=0.1V
Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY





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Title: VATVDD/+VPCIE

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+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.44A

2. Ripple Current:

Irip=0.53A

3. Ripple Voltage:

ESR/3=3.3mohm
Vrip=1.75mV

4. Inductor Spec:

Isat=14A
Idc=8A
DCR=20mohm

5.MOSFET Spec:

H-side P-MOSFET: Rds(ON)=110mohm (Vgs=4.5 V)

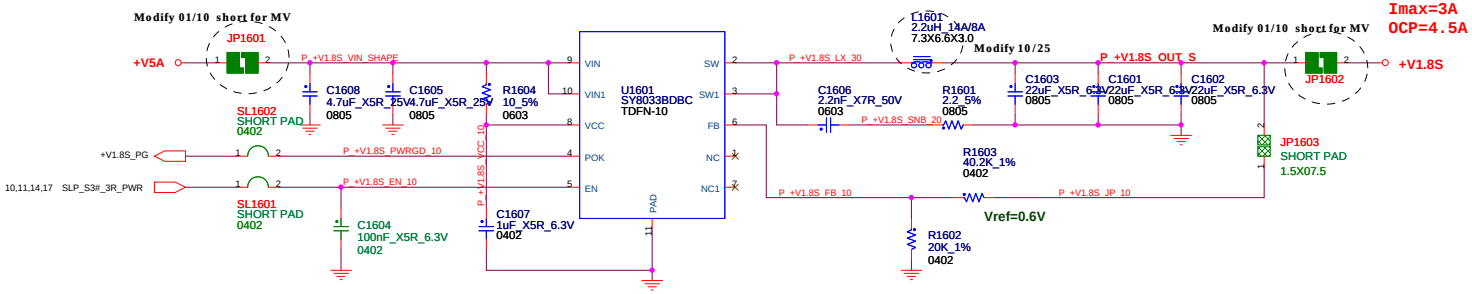
L-side N-MOSFET: Rds(ON)=75mohm (Vgs=4.5 V)

6. Frequency:

F=1MHz (min=800KHz, max=1.2MHz)

7. OCP:

Iocp=4A(min)/4.5A(typ)/5A(max)



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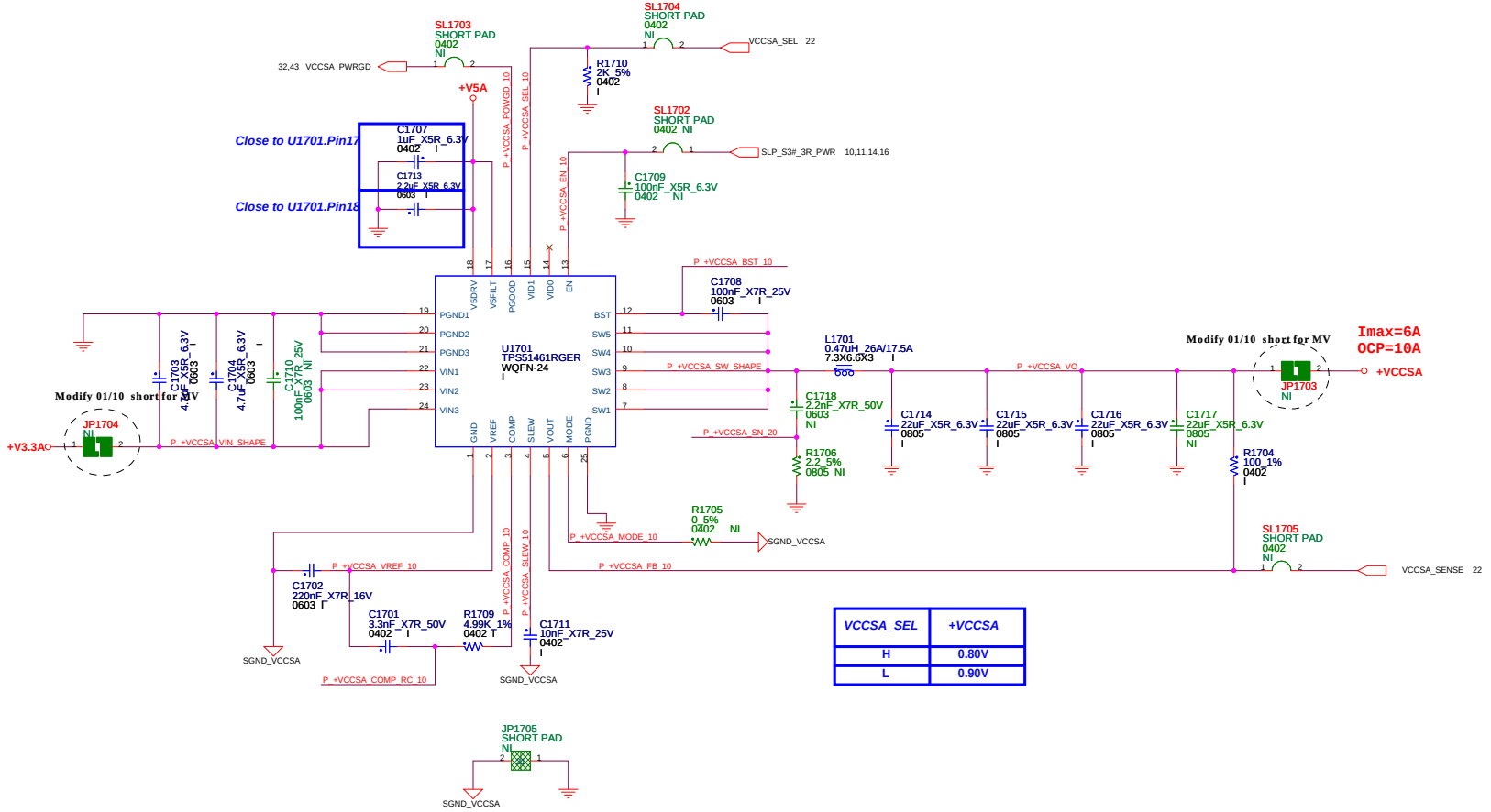
+VCCSA POWER SUPPLY

2010.1026.0

+VCCSA:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.18A
2. Ripple Current:
   Irip=1.39A
3. Ripple Voltage:
   ESR/4=1mohm
   Vrip=1.39mV
4. Inductor Spec:
   Isat=26A
   Idc=17.5A
   DCR=4.2mohm
5. MOSFET Spec:
6. Frequency:
   F=1MHz (R1705=Open)
7. OCP:
   Min : 6A / Typ : 7.5A



VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

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+V3.3S +V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43

+V1.05S_VCCP +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43

UX1A

DMI_TXN[3:0] DMI_TXN0 B27, DMI_TXN1 B25, DMI_TXN2 A25, DMI_TXN3 B24 → DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]

DMI_TXP[3:0] DMI_TXP0 B28, DMI_TXP1 B26, DMI_TXP2 A24, DMI_TXP3 B23 → DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]

DMI_RXN[3:0] DMI_RXN0 G21, DMI_RXN1 E22, DMI_RXN2 F21, DMI_RXN3 D21 → DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]

DMI_RXP[3:0] DMI_RXP0 G22, DMI_RXP1 D22, DMI_RXP2 F20, DMI_RXP3 C21 → DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

DMI

FDI_TXN[7:0] FDI_TXN0 A21, FDI_TXN1 H19, FDI_TXN2 E19, FDI_TXN3 F18, FDI_TXN4 B21, FDI_TXN5 C20, FDI_TXN6 D18, FDI_TXN7 E17 → FDI0_TX#[0] FDI0_TX#[1] FDI0_TX#[2] FDI0_TX#[3] FDI1_TX#[0] FDI1_TX#[1] FDI1_TX#[2] FDI1_TX#[3]

FDI_TXP[7:0] FDI_TXP0 A22, FDI_TXP1 G19, FDI_TXP2 E20, FDI_TXP3 G18, FDI_TXP4 B20, FDI_TXP5 C19, FDI_TXP6 D19, FDI_TXP7 E17 → FDI0_TX[0] FDI0_TX[1] FDI0_TX[2] FDI0_TX[3] FDI1_TX[0] FDI1_TX[1] FDI1_TX[2] FDI1_TX[3]

FDI_FSYNC0 J18 → FDI0_FSYNC

FDI_FSYNC1 J17 → FDI1_FSYNC

FDI_INT H20 → FDI_INT

FDI_LSYNC0 J19 → FDI0_LSYNC

FDI_LSYNC1 H17 → FDI1_LSYNC

Intel(R) FDI

+V1.05S_VCCP

RX48 0402 24.9_1% DP_COMP → A18

RX6 0402 10K_5% NI → A17

eDP_COMPIO A18, eDP_ICOMPO A17, eDP_HPD B16

eDP_AUX C15, eDP_AUX# D15

eDP_TX[0] C17, eDP_TX[1] F16, eDP_TX[2] C16, eDP_TX[3] G15

eDP_TX#[0] C18, eDP_TX#[1] E16, eDP_TX#[2] D16, eDP_TX#[3] F15

eDP

Sandy Bridge_rPGA_Rev0p61

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22, PEG_ICOMPO J21, PEG_RCOMPO H22 → PEG_COMP

RX1 0402 24.9_1%

Signal	Trace Width	Trace Spacing to other Signals	Routing Length
PEG_ICOMPO	12 mils (0.305 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)
PEG_ICOMPI PEG_RCOMPO	4 mils (0.102 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)

Trace width :
PEG_COMP from CPU socket PIN H22 and J22 to Res RX1 is 4mils
PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils

PEG_RX#[0] K33, PEG_RX#[1] M35, PEG_RX#[2] L34, PEG_RX#[3] J35, PEG_RX#[4] J32, PEG_RX#[5] H34, PEG_RX#[6] H31, PEG_RX#[7] G33, PEG_RX#[8] G30, PEG_RX#[9] F35, PEG_RX#[10] E34, PEG_RX#[11] E32, PEG_RX#[12] D33, PEG_RX#[13] D31, PEG_RX#[14] B33, PEG_RX#[15] C32 → PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 → PEG_RXN[0..7] 30

PEG_RX[0] J33, PEG_RX[1] L35, PEG_RX[2] K34, PEG_RX[3] H35, PEG_RX[4] H32, PEG_RX[5] G34, PEG_RX[6] G31, PEG_RX[7] F33, PEG_RX[8] F30, PEG_RX[9] E35, PEG_RX[10] E33, PEG_RX[11] F32, PEG_RX[12] D34, PEG_RX[13] E31, PEG_RX[14] C33, PEG_RX[15] B32 → PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 → PEG_RXP[0..7] 30

PEG_TX#[0] M29, PEG_TX#[1] M32, PEG_TX#[2] M31, PEG_TX#[3] L32, PEG_TX#[4] L29, PEG_TX#[5] K31, PEG_TX#[6] K28, PEG_TX#[7] J30, PEG_TX#[8] J28, PEG_TX#[9] H29, PEG_TX#[10] G27, PEG_TX#[11] E29, PEG_TX#[12] F27, PEG_TX#[13] D28, PEG_TX#[14] F26, PEG_TX#[15] E25 → PEG_TXN0 CX1, PEG_TXN1 CX2, PEG_TXN2 CX3, PEG_TXN3 CX4, PEG_TXN4 CX5, PEG_TXN5 CX6, PEG_TXN6 CX7, PEG_TXN7 CX8 → 100nF_X5R_10V 0402 → PEG_TXN0_C … PEG_TXN7_C 30

PEG_TX[0] M28, PEG_TX[1] M33, PEG_TX[2] M30, PEG_TX[3] L31, PEG_TX[4] L28, PEG_TX[5] K30, PEG_TX[6] K27, PEG_TX[7] J29, PEG_TX[8] J27, PEG_TX[9] H28, PEG_TX[10] G28, PEG_TX[11] E28, PEG_TX[12] F28, PEG_TX[13] D27, PEG_TX[14] E26, PEG_TX[15] D25 → PEG_TXP0 CX17, PEG_TXP1 CX18, PEG_TXP2 CX19, PEG_TXP3 CX20, PEG_TXP4 CX21, PEG_TXP5 CX22, PEG_TXP6 CX23, PEG_TXP7 CX24 → 100nF_X5R_10V 0402 → PEG_TXP0_C … PEG_TXP7_C 30

UX1E

CFG0 → CFG[0] AK28, CFG[1] AK29, CFG[2] AL26, CFG[3] AL27, CFG[4] AK26, CFG[5] AL29, CFG[6] AL30, CFG[7] AM31, CFG[8] AM32, CFG[9] AM30, CFG[10] AM28, CFG[11] AM26, CFG[12] AN28, CFG[13] AN31, CFG[14] AN26, CFG[15] AM27, CFG[16] AK31, CFG[17] AN29

+VCC_CORE

RX2 0_5% 0402 NI

VCC_VAL_SENSE AJ31, VSS_VAL_SENSE AH31 → VAXG_VAL_SENSE, VSSAXG_VAL_SENSE

RX3 0_5% 0402 NI

VCC_VAL_SENSE AJ33, VSS_VAL_SENSE AH33

AJ26 RSVD5

RSVD6 B4, RSVD7 D1 → RSVD6, RSVD7

RX4 1K_5% 0402 NI

RX5 1K_5% 0402 NI

RSVD8 E25, RSVD9 F24, RSVD10 F23, RSVD11 D24, RSVD12 G25, RSVD13 G24, RSVD14 F23, RSVD15 D23, RSVD16 C30, RSVD17 A31, RSVD18 B30, RSVD19 B29, RSVD20 D30, RSVD21 B31, RSVD22 A30, RSVD23 C29

J20 RSVD24, B18 RSVD25, A19 VCCIO_SEL

J15 RSVD27

RESERVED

RSVD28 L7, RSVD29 AG7, RSVD30 AE7, RSVD31 AK2, RSVD32 W8

RSVD33 AT26, RSVD34 AM33, RSVD35 AJ27

RSVD37 T8, RSVD38 J16, RSVD39 H16, RSVD40 G16

RSVD41 AR35, RSVD42 AT34, RSVD43 AT33, RSVD44 AP35, RSVD45 AR34

RSVD46 B34, RSVD47 A33, RSVD48 A34, RSVD49 B35, RSVD50 C35

RSVD51 AJ32, RSVD52 AK32

VCC_DIE_SENSE AH27

RSVD54 AN35, RSVD55 AM35

CLK_PCH_XDP_R

CLK_PCH_XDP#_R

RSVD56 AT2, RSVD57 AT1, RSVD58 AR1

Sandy Bridge_rPGA_Rev0p61

19,24 CLK_PCH_XDP# → RX8 0402 0_5% NI

19,24 CLK_PCH_XDP → RX9 0402 0_5% NI

+V3.3S

RX7 2.2K_5% 0402

VCCIO_SEL

RX37 2.2K_5% 0402 NI

Control 1.05V VR Setting (for 2012 CPU)
H_SNB_IVB#_PWRCTRL LOW: 1.0V
H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V

CFG4

RX10 1K_1% 0402 NI

Display Port Presence Strap

CFG4 1:(Default) Disabled;No Physical Display Port attached to Embedded Display Port

0:Enabled;An external Display Port is connect to Embedded Display Port

CFG7

RX13 1K_1% 0402 NI

PEG DEFER TRAINING

CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion

0:PEG Wait for BIOS for training

CFG6

CFG5

RX11 1K_1% 0402 NI

RX12 1K_1% 0402 NI

PCIE Port Bifurcation Straps

CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled

10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled

01:Reserved - (Device 1 function 1 disabled ; function 2 enabled

00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled

CFG3

RX58 1K_1% 0402 NI

CFG2

RX14 1K_1% 0402 NI

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition

0:Lane Reversed

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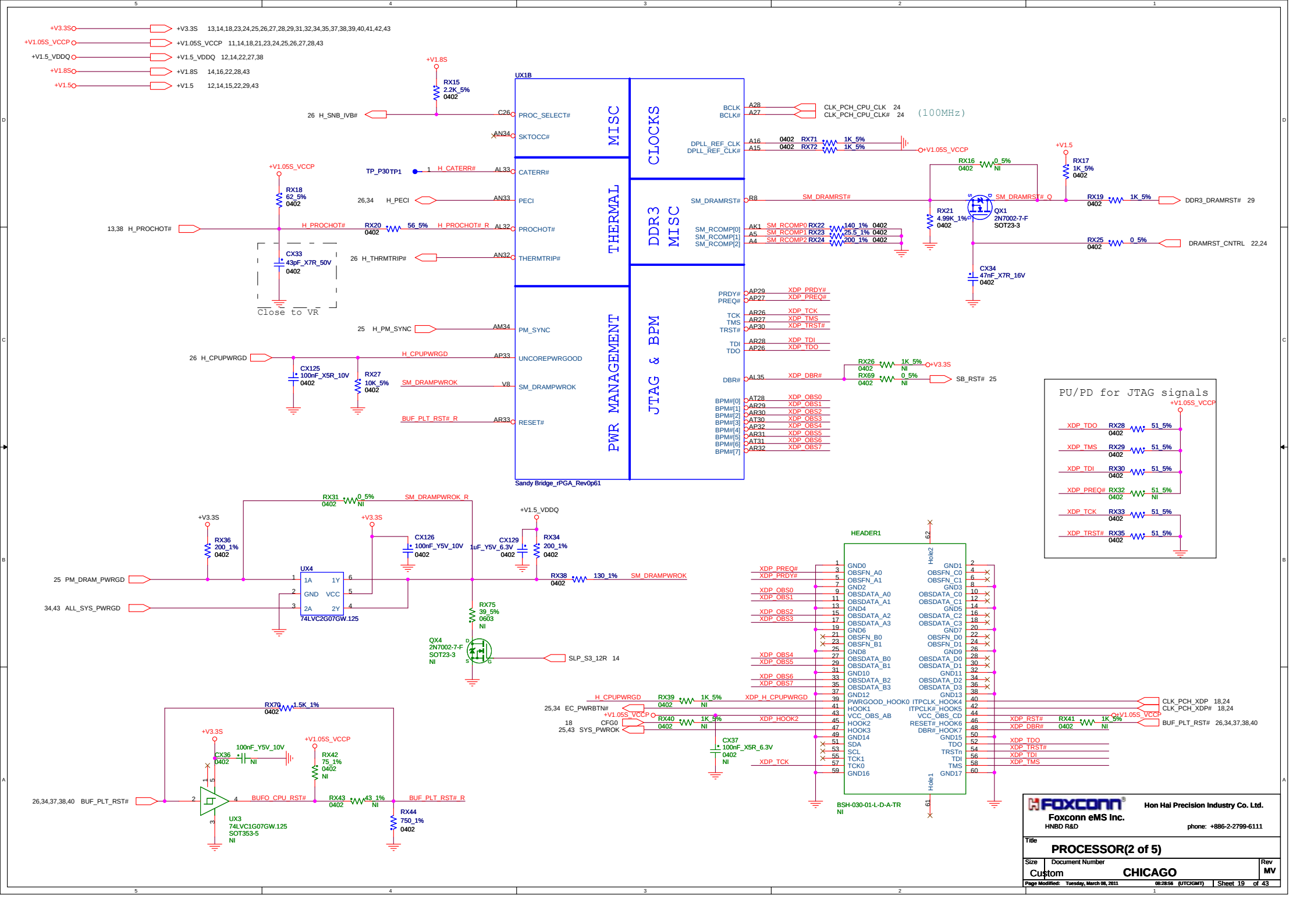
+V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
+V1.5_VDDQ 12,14,22,27,38
+V1.8S 14,16,22,28,43
+V1.5 12,14,15,22,29,43
UX1B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PROC_SELECT#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
Sandy Bridge_rPGA_Rev0p61
CLK_PCH_CPU_CLK 24
CLK_PCH_CPU_CLK# 24
(100MHz)
DDR3_DRAMRST# 29
DRAMRST_CNTRL 22,24
SB_RST# 25
Close to VR
PU/PD for JTAG signals
HEADER1
BSH-030-01-L-D-A-TR
CLK_PCH_XDP 18,24
CLK_PCH_XDP# 18,24
BUF_PLT_RST# 26,34,37,38,40
SLP_S3_12R 14
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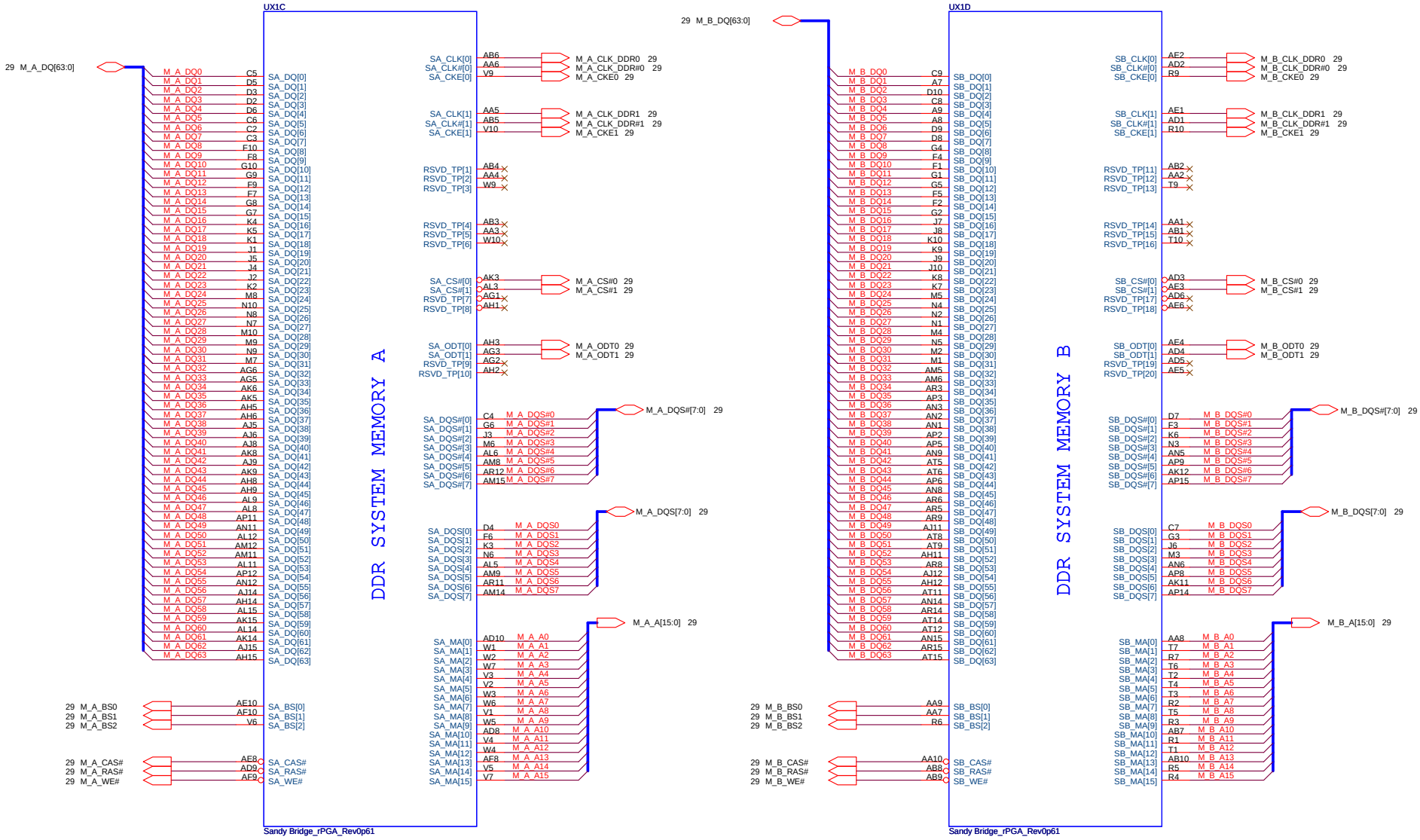

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+V1.05S_VCCP +V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43

+VCC_CORE +VCC_CORE 13,18,43

POWER

FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,

+VCC_CORE

53A />2120mils

CX41 22uF_X5R_6.3V 0805
CX42 22uF_X5R_6.3V 0805
CX43 22uF_X5R_6.3V 0805
CX44 22uF_X5R_6.3V 0805
CX50 22uF_X5R_6.3V 0805

CX59 22uF_X5R_6.3V 0805
CX60 22uF_X5R_6.3V 0805
CX61 22uF_X5R_6.3V 0805
CX62 22uF_X5R_6.3V 0805
CX63 22uF_X5R_6.3V 0805

RX45 22uF_X5R_6.3V 0805
CX72 22uF_X5R_6.3V 0805
RX46 22uF_X5R_6.3V 0805
CX73 22uF_X5R_6.3V 0805
CX74 22uF_X5R_6.3V 0805

CX75 22uF_X5R_6.3V 0805

CX79 10uF_X5R_6.3V 0603
CX80 10uF_X5R_6.3V 0603
CX81 10uF_X5R_6.3V 0603
RX51 10uF_X5R_6.3V 0603
CX82 10uF_X5R_6.3V 0603

RX54 10uF_X5R_6.3V 0603
CX83 10uF_X5R_6.3V 0603
RX55 10uF_X5R_6.3V 0603
CX84 10uF_X5R_6.3V 0603
CX85 10uF_X5R_6.3V 0603

RX59 33pF_NPO_50V 0402
CX87 33pF_NPO_50V 0402

UX1F

PEG AND DDR

+VCC_CORE

AG35 VCC1, AG34 VCC2, AG33 VCC3, AG32 VCC4, AG31 VCC5, AG30 VCC6, AG29 VCC7, AG28 VCC8, AG27 VCC9, AG26 VCC10, AF35 VCC11, AF34 VCC12, AF33 VCC13, AF32 VCC14, AF31 VCC15, AF30 VCC16, AF29 VCC17, AF28 VCC18, AF27 VCC19, AF26 VCC20, AD35 VCC21, AD34 VCC22, AD33 VCC23, AD32 VCC24, AD31 VCC25, AD30 VCC26, AD29 VCC27, AD28 VCC28, AD27 VCC29, AD26 VCC30, AC35 VCC31, AC34 VCC32, AC33 VCC33, AC32 VCC34, AC31 VCC35, AC30 VCC36, AC29 VCC37, AC28 VCC38, AC27 VCC39, AC26 VCC40, AA35 VCC41, AA34 VCC42, AA33 VCC43, AA32 VCC44, AA31 VCC45, AA30 VCC46, AA29 VCC47, AA28 VCC48, AA27 VCC49, AA26 VCC50, Y35 VCC51, Y34 VCC52, Y33 VCC53, Y32 VCC54, Y31 VCC55, Y30 VCC56, Y29 VCC57, Y28 VCC58, Y27 VCC59, Y26 VCC60, V35 VCC61, V34 VCC62, V33 VCC63, V32 VCC64, V31 VCC65, V30 VCC66, V29 VCC67, V28 VCC68, V27 VCC69, V26 VCC70, U35 VCC71, U34 VCC72, U33 VCC73, U32 VCC74, U31 VCC75, U30 VCC76, U29 VCC77, U28 VCC78, U27 VCC79, U26 VCC80, R35 VCC81, R34 VCC82, R33 VCC83, R32 VCC84, R31 VCC85, R30 VCC86, R29 VCC87, R28 VCC88, R27 VCC89, R26 VCC90, P35 VCC91, P34 VCC92, P33 VCC93, P32 VCC94, P31 VCC95, P30 VCC96, P29 VCC97, P28 VCC98, P27 VCC99, P26 VCC100

CORE SUPPLY

FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,

RF solution

0402 68pF_NPO_50V CX113 NI
0402 1nF_X7R_16V CX112 NI

+V1.05S_VCCP

8.5A />340mils

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

CX65 22uF_X5R_6.3V 0805
CX66 22uF_X5R_6.3V 0805
CX47 22uF_X5R_6.3V 0805
CX38 22uF_X5R_6.3V 0805
CX48 22uF_X5R_6.3V 0805
CX39 22uF_X5R_6.3V 0805
CX40 22uF_X5R_6.3V 0805

CX70 330uF_PO_2V 2816
CX54 22uF_X5R_6.3V 0805
CX55 22uF_X5R_6.3V 0805
CX56 22uF_X5R_6.3V 0805
CX57 22uF_X5R_6.3V 0805
CX58 22uF_X5R_6.3V 0805

SVID

VIDALERT# AJ29 VR_SVID_ALERT#_R
VIDSCLK AJ30 VR_SVID_CLK_R
VIDSOUT AJ28 VR_SVID_DATA_R

Close to VR
+V1.05S_VCCP
RX47 75_5% 0402
CX123 100nF_X5R_10V 0402 NI
Close to CPU
RX49 0402 43_5%
VR_VIDALERT# 13

Close to VR
+V1.05S_VCCP
RX50 54.9_1% 0402
Close to CPU
RX52 0402 0_5%
VR_VIDSCLK 13

Close to CPU
+V1.05S_VCCP
CX124 100nF_X5R_10V 0402 NI
RX53 130_5% 0402
Close to VR
+V1.05S_VCCP
RX56 130_5% 0402
RX57 0402 0_5%
VR_VIDSOUT 13

SENSE LINES

+VCC_CORE
RX76 100_5% 0402
RX77 100_5% 0402

VCC_SENSE AJ35
VSS_SENSE AJ34
VCC_SENSE 13
VSS_SENSE 13

VCCIO_SENSE B10
VSSIO_SENSE A10
VCCP_SENSE 11
VSSP_SENSE 11

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UX1H

VSS

AT35 VSS1, AT32 VSS2, AT29 VSS3, AT27 VSS4, AT25 VSS5, AT22 VSS6, AT19 VSS7, AT16 VSS8, AT13 VSS9, AT10 VSS10, AT7 VSS11, AT4 VSS12, AT3 VSS13, AR25 VSS14, AR22 VSS15, AR19 VSS16, AR16 VSS17, AR13 VSS18, AR10 VSS19, AR7 VSS20, AR4 VSS21, AR2 VSS22, AP34 VSS23, AP31 VSS24, AP28 VSS25, AP25 VSS26, AP22 VSS27, AP19 VSS28, AP16 VSS29, AP13 VSS30, AP10 VSS31, AP7 VSS32, AP4 VSS33, AP1 VSS34, AN30 VSS35, AN27 VSS36, AN25 VSS37, AN22 VSS38, AN19 VSS39, AN16 VSS40, AN13 VSS41, AN10 VSS42, AN7 VSS43, AN4 VSS44, AM29 VSS45, AM25 VSS46, AM22 VSS47, AM19 VSS48, AM16 VSS49, AM13 VSS50, AM10 VSS51, AM7 VSS52, AM4 VSS53, AM3 VSS54, AM2 VSS55, AM1 VSS56, AL34 VSS57, AL31 VSS58, AL28 VSS59, AL25 VSS60, AL22 VSS61, AL19 VSS62, AL16 VSS63, AL13 VSS64, AL10 VSS65, AL7 VSS66, AL4 VSS67, AL2 VSS68, AK33 VSS69, AK30 VSS70, AK27 VSS71, AK25 VSS72, AK22 VSS73, AK19 VSS74, AK16 VSS75, AK13 VSS76, AK10 VSS77, AK7 VSS78, AK4 VSS79, AJ25 VSS80

VSS81 AJ22, VSS82 AJ19, VSS83 AJ16, VSS84 AJ13, VSS85 AJ10, VSS86 AJ7, VSS87 AJ4, VSS88 AJ3, VSS89 AJ2, VSS90 AJ1, VSS91 AH35, VSS92 AH34, VSS93 AH32, VSS94 AH30, VSS95 AH29, VSS96 AH28, VSS97 AH26, VSS98 AH25, VSS99 AH22, VSS100 AH19, VSS101 AH16, VSS102 AH7, VSS103 AH4, VSS104 AG9, VSS105 AG8, VSS106 AG4, VSS107 AF6, VSS108 AF5, VSS109 AF3, VSS110 AF2, VSS111 AE35, VSS112 AE34, VSS113 AE33, VSS114 AE32, VSS115 AE31, VSS116 AE30, VSS117 AE29, VSS118 AE28, VSS119 AE27, VSS120 AE26, VSS121 AE9, VSS122 AD7, VSS123 AC9, VSS124 AC8, VSS125 AC6, VSS126 AC5, VSS127 AC3, VSS128 AC2, VSS129 AB35, VSS130 AB34, VSS131 AB33, VSS132 AB32, VSS133 AB31, VSS134 AB30, VSS135 AB29, VSS136 AB28, VSS137 AB27, VSS138 AB26, VSS139 Y9, VSS140 Y8, VSS141 Y6, VSS142 Y5, VSS143 Y3, VSS144 Y2, VSS145 W35, VSS146 W34, VSS147 W33, VSS148 W32, VSS149 W31, VSS150 W30, VSS151 W29, VSS152 W28, VSS153 W27, VSS154 W26, VSS155 U9, VSS156 U8, VSS157 U6, VSS158 U5, VSS159 U3, VSS160 U2

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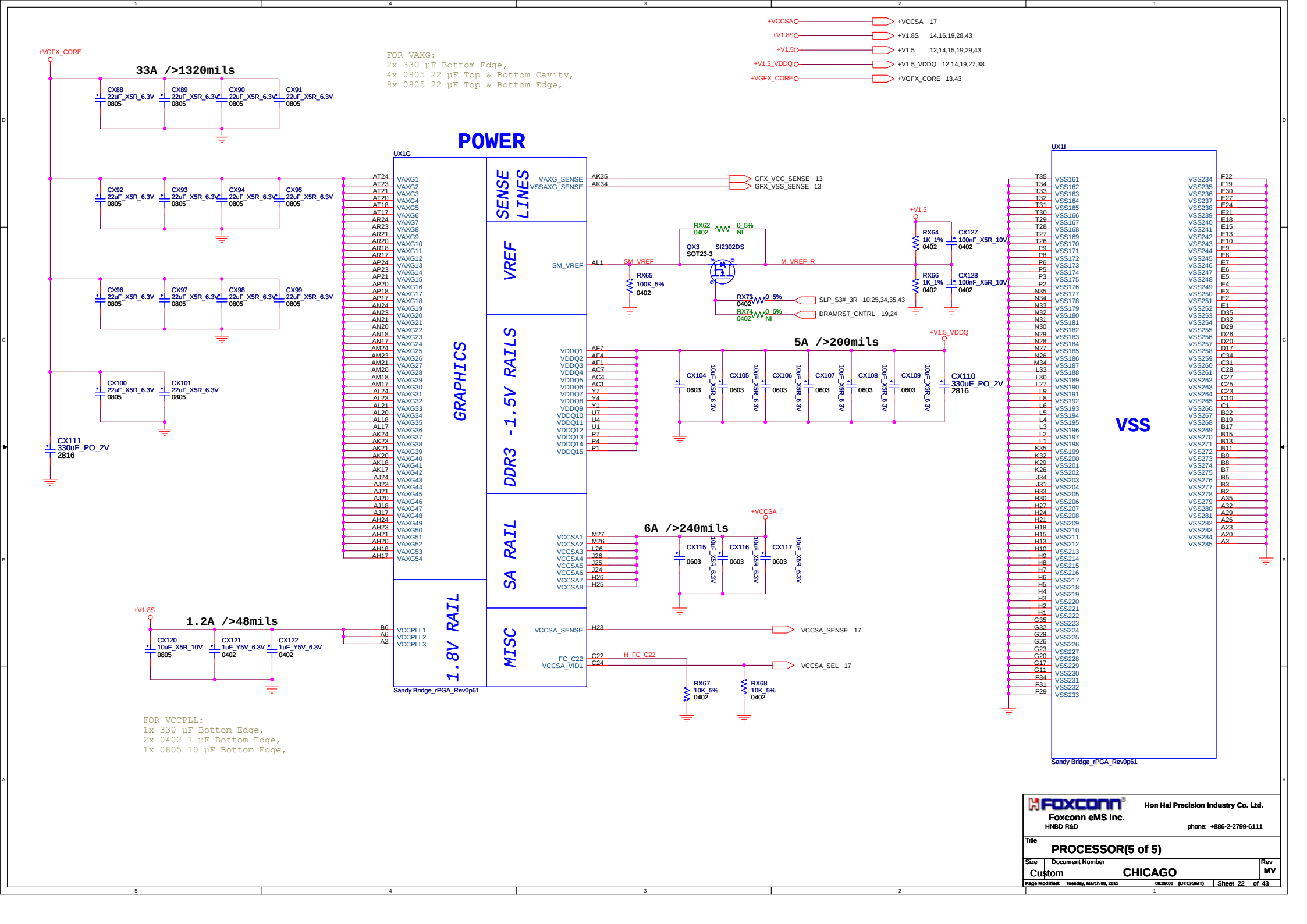
+VCCSA 17
+V1.8S 14,16,19,28,43
+V1.5 12,14,15,19,29,43
+V1.5_VDDQ 12,14,19,27,38
+VGFX_CORE 13,43
+VGFX_CORE
33A />1320mils
CX88 22uF_X5R_6.3V 0805
CX89 22uF_X5R_6.3V 0805
CX90 22uF_X5R_6.3V 0805
CX91 22uF_X5R_6.3V 0805
CX92 22uF_X5R_6.3V 0805
CX93 22uF_X5R_6.3V 0805
CX94 22uF_X5R_6.3V 0805
CX95 22uF_X5R_6.3V 0805
CX96 22uF_X5R_6.3V 0805
CX97 22uF_X5R_6.3V 0805
CX98 22uF_X5R_6.3V 0805
CX99 22uF_X5R_6.3V 0805
CX100 22uF_X5R_6.3V 0805
CX101 22uF_X5R_6.3V 0805
CX111 330uF_PO_2V 2816
FOR VAXG:
2x 330 µF Bottom Edge,
4x 0805 22 µF Top & Bottom Cavity,
8x 0805 22 µF Top & Bottom Edge,
POWER
UX1G
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AK35
AK34
GFX_VCC_SENSE 13
GFX_VSS_SENSE 13
VREF
SM_VREF
AL1
RX62 0_5% 0402 NI
QX3 SI2302DS SOT23-3
RX65 100K_5% 0402
RX73 0_5% 0402
RX74 0_5% 0402 NI
SLP_S3#_3R 10,25,34,35,43
DRAMRST_CNTRL 19,24
+V1.5
RX64 1K_1% 0402
RX66 1K_1% 0402
CX127 100nF_X5R_10V 0402
CX128 100nF_X5R_10V 0402
GRAPHICS
DDR3 -1.5V RAILS
5A />200mils
+V1.5_VDDQ
CX104 CX105 CX106 CX107 CX108 CX109 10uF_X5R_6.3V 0603
CX110 330uF_PO_2V 2816
SA RAIL
6A />240mils
+VCCSA
CX115 CX116 CX117 10uF_X5R_6.3V 0603
MISC
VCCSA_SENSE
VCCSA_SENSE 17
VCCSA_VID1
VCCSA_SEL 17
RX67 10K_5% 0402
RX68 10K_5% 0402
1.8V RAIL
+V1.8S
1.2A />48mils
CX120 10uF_X5R_10V 0805
CX121 1uF_Y5V_6.3V 0402
CX122 1uF_Y5V_6.3V 0402
VCCPLL1
VCCPLL2
VCCPLL3
Sandy Bridge_rPGA_Rev0p61
FOR VCCPLL:
1x 330 µF Bottom Edge,
2x 0402 1 µF Bottom Edge,
1x 0805 10 µF Bottom Edge,
UX1I
VSS
Sandy Bridge_rPGA_Rev0p61
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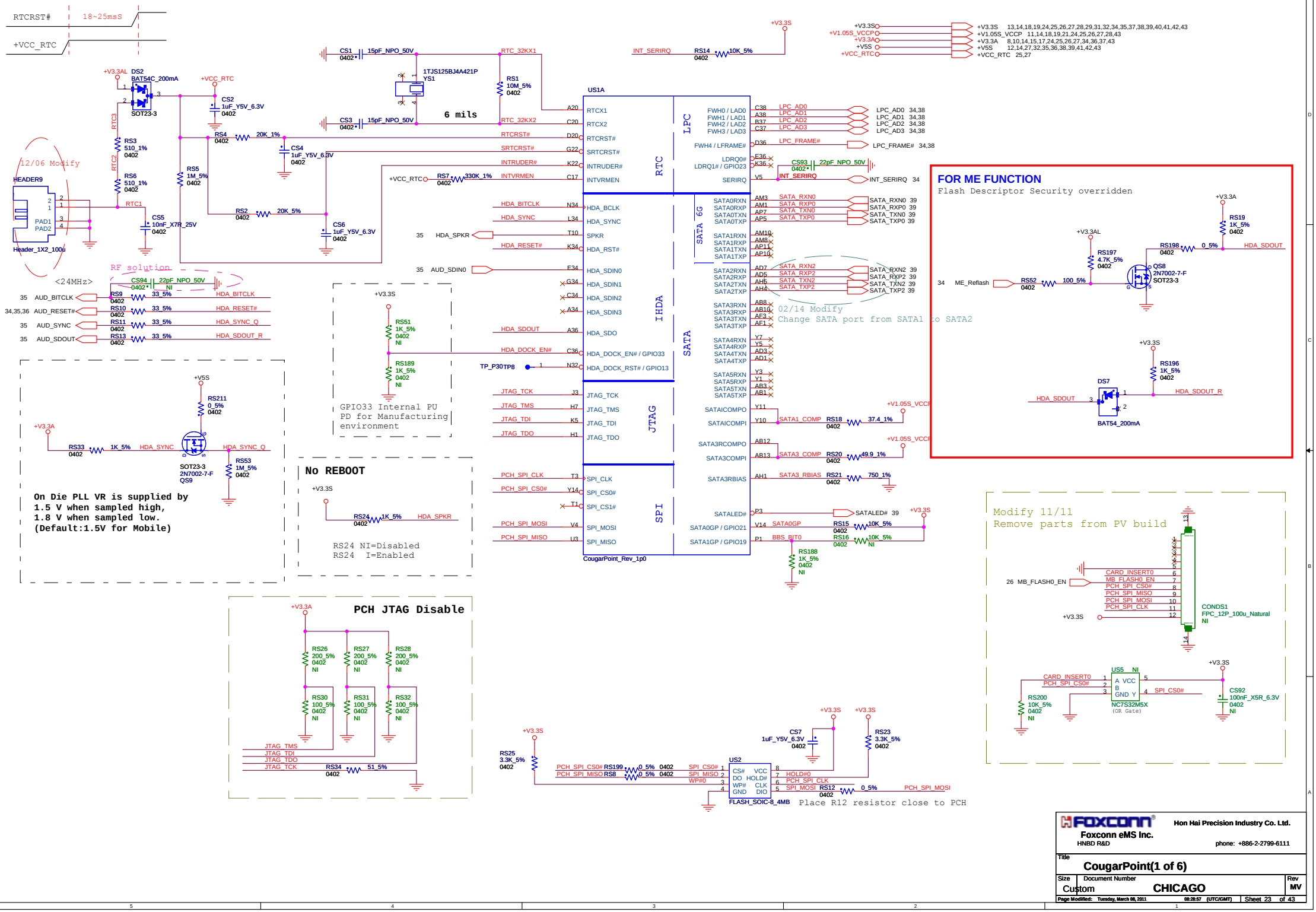

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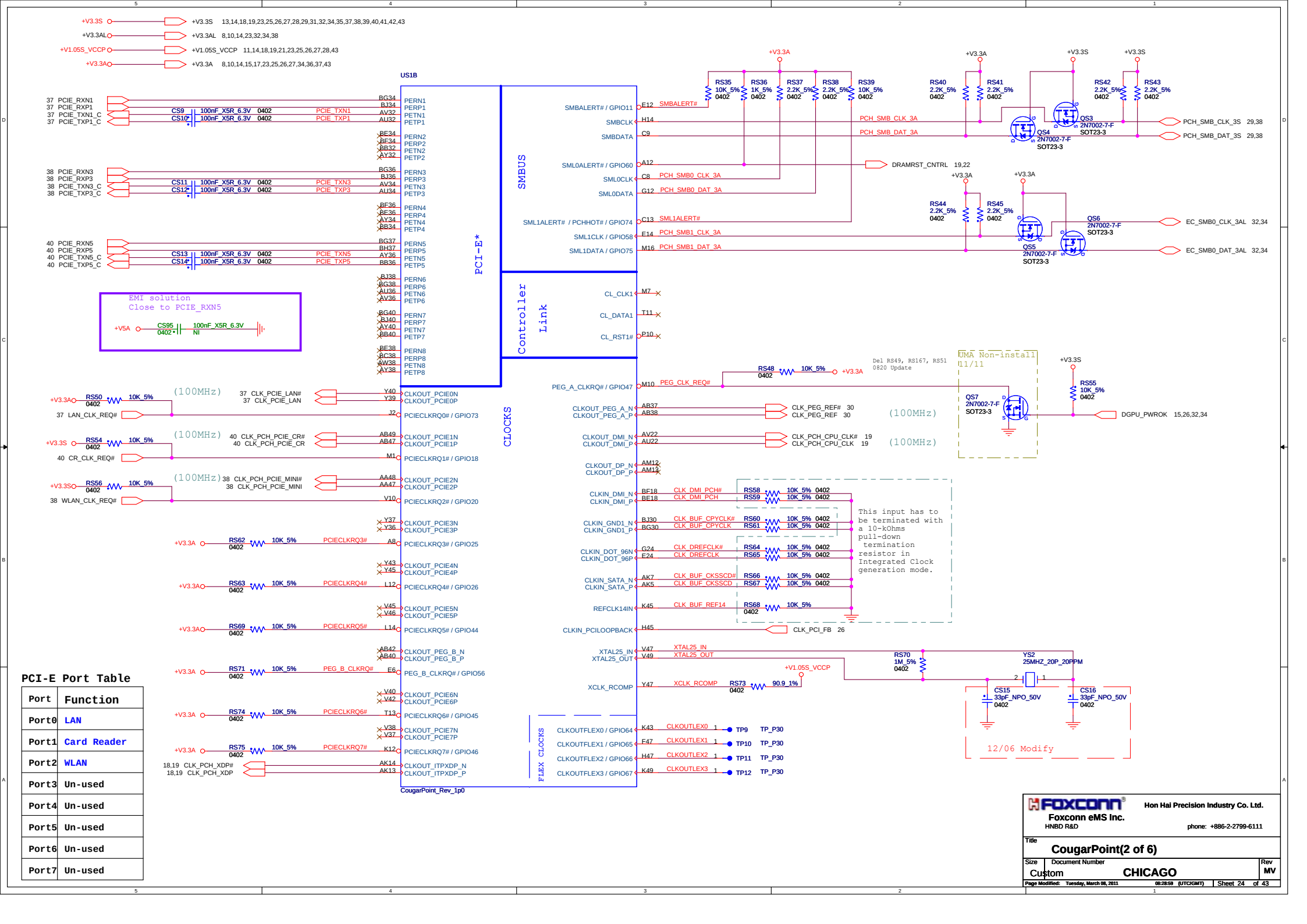

PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used

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Title: CougarPoint(2 of 6)

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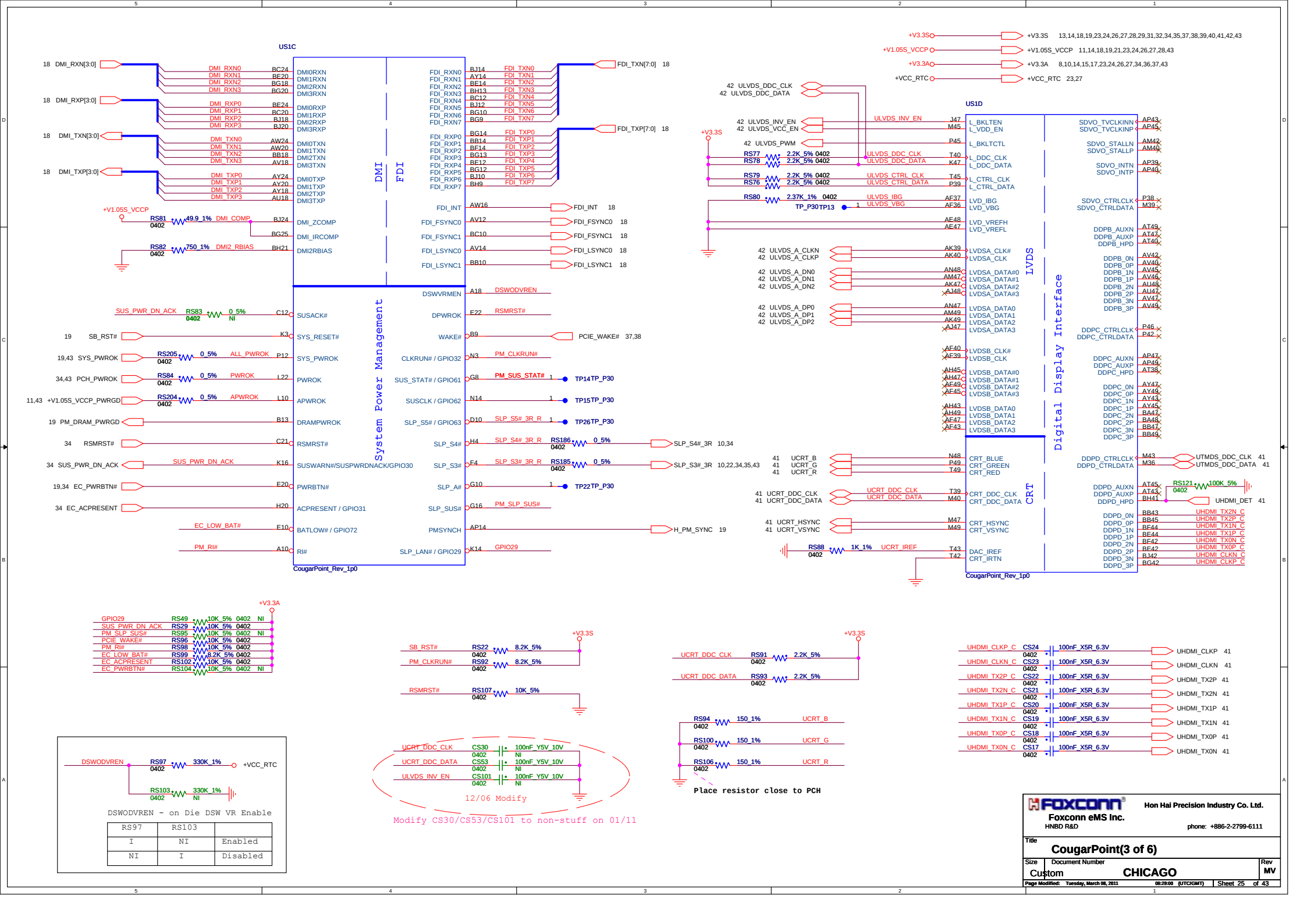
US1C
DMI
FDI
System Power Management
CougarPoint_Rev_1p0
US1D
LVDS
Digital Display Interface
CRT
CougarPoint_Rev_1p0
+V3.3S 13,14,18,19,23,24,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,18,19,21,23,24,26,27,28,43
+V3.3A 8,10,14,15,17,23,24,26,27,34,36,37,43
+VCC_RTC 23,27
DSWODVREN - on Die DSW VR Enable
RS97 RS103
I NI Enabled
NI I Disabled
12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11
Place resistor close to PCH
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CougarPoint(3 of 6)
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Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

Del RS121 8.2Kohm to +V3.3S
0820 Update

12/06 Modify

Modify CS102/CS103 to non-stuff on 01/11

02/24 Modify
same as the PV build

CougarPoint_Rev_1p0

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Title: CougarPoint(4 of 6)
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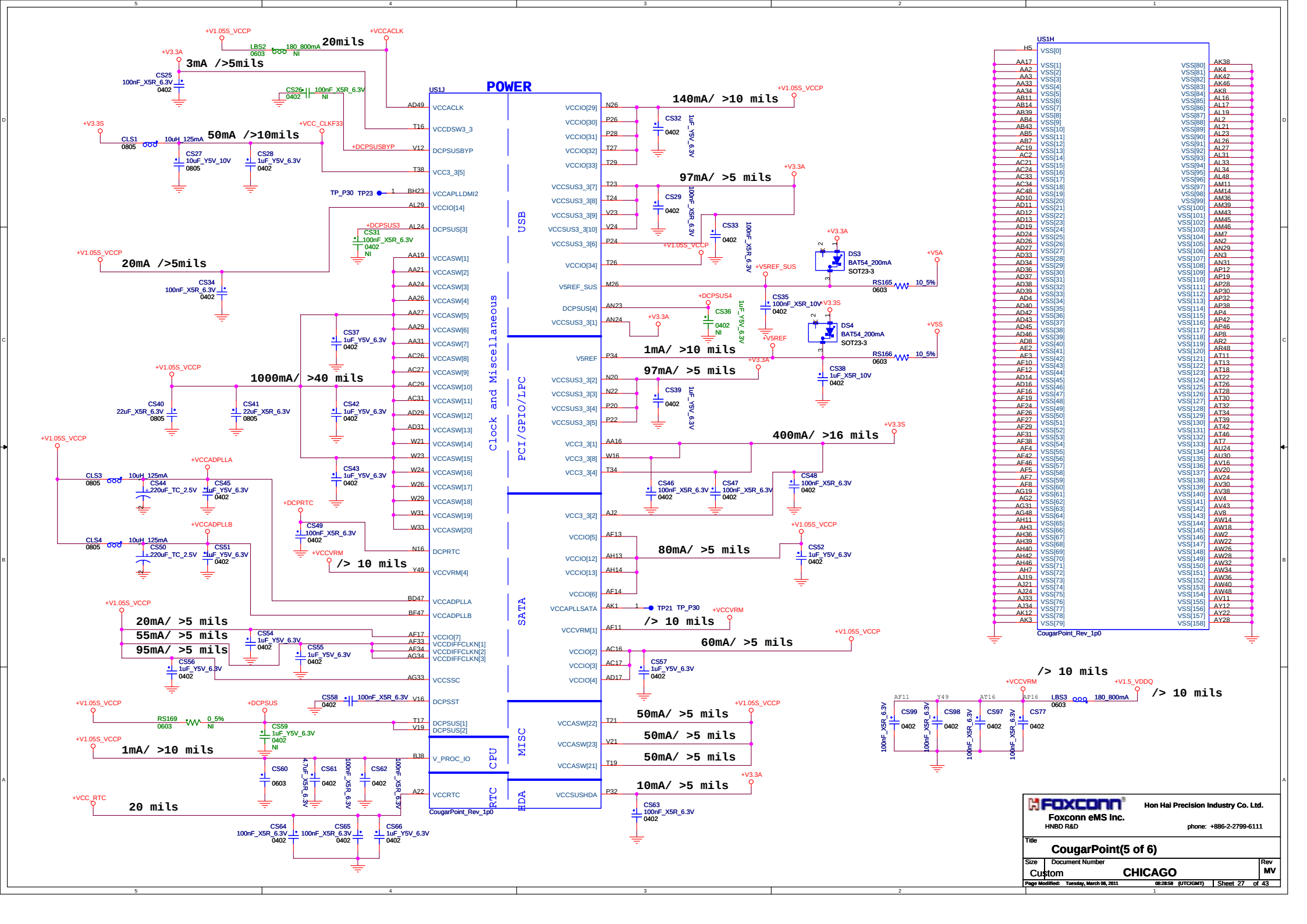
POWER
US1J
CougarPoint_Rev_1p0
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
20mils
3mA />5mils
50mA />10mils
20mA />5mils
1000mA/ >40 mils
20mA/ >5mils
55mA/ >5 mils
95mA/ >5 mils
1mA/ >10 mils
20 mils
140mA/ >10 mils
97mA/ >5 mils
1mA/ >10 mils
97mA/ >5 mils
400mA/ >16 mils
80mA/ >5 mils
/> 10 mils
60mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
10mA/ >5 mils
/> 10 mils
/> 10 mils
US1H
CougarPoint_Rev_1p0
Foxconn
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Foxconn eMS Inc.
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phone: +886-2-2799-6111
Title
CougarPoint(5 of 6)
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Custom
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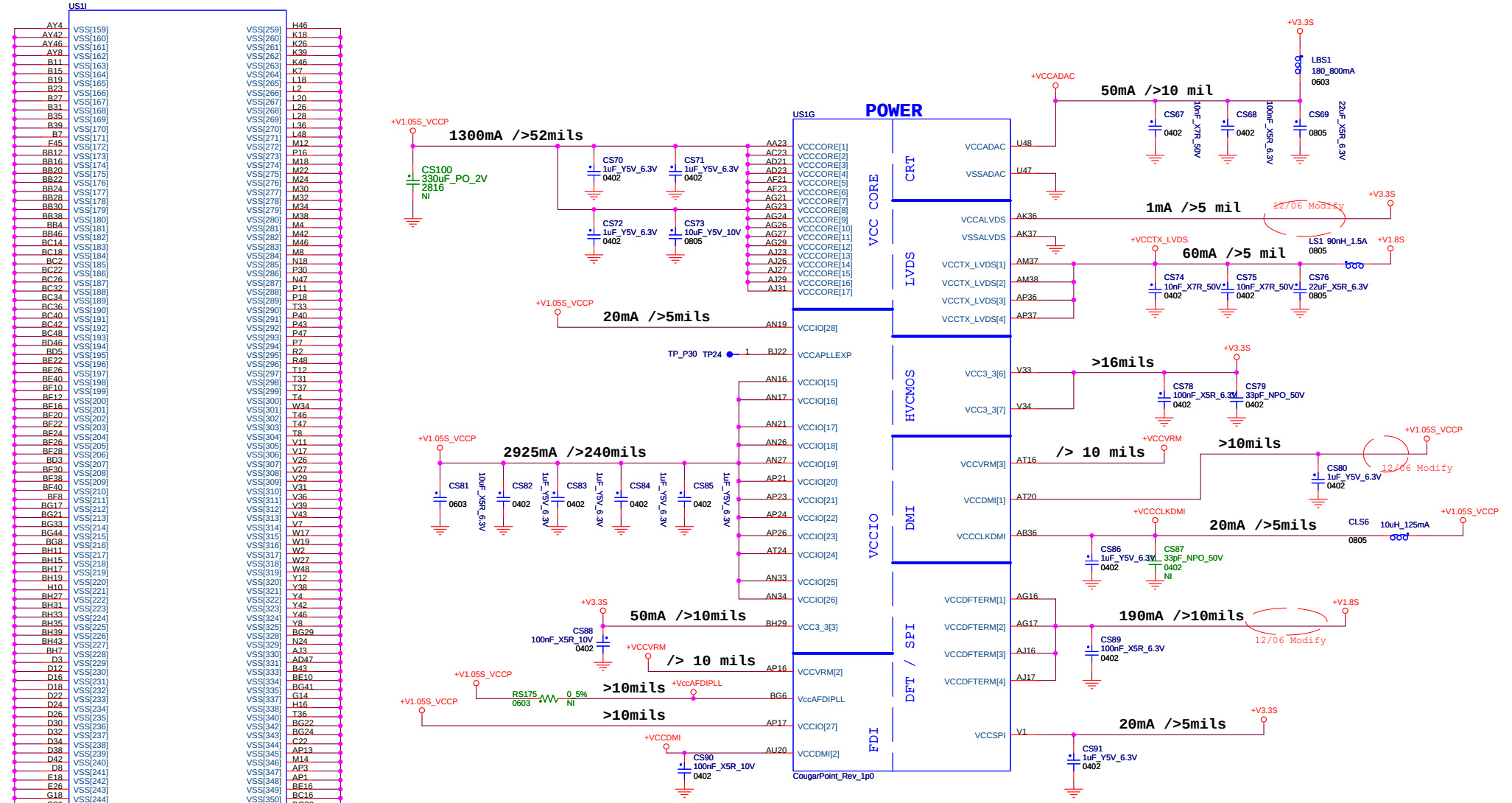
US1I
CougarPoint_Rev_1p0
US1G
POWER
VCC CORE
VCCIO
CRT
LVDS
HVCMOS
DMI
SPI
DFT / FDI
CougarPoint_Rev_1p0
1300mA />52mils
20mA />5mils
2925mA />240mils
50mA />10mils
/> 10 mils
>10mils
>10mils
50mA />10 mil
1mA />5 mil
60mA />5 mil
>16mils
/> 10 mils
>10mils
20mA />5mils
190mA />10mils
20mA />5mils
12/06 Modify
12/06 Modify
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CougarPoint(6 of 6)
Custom
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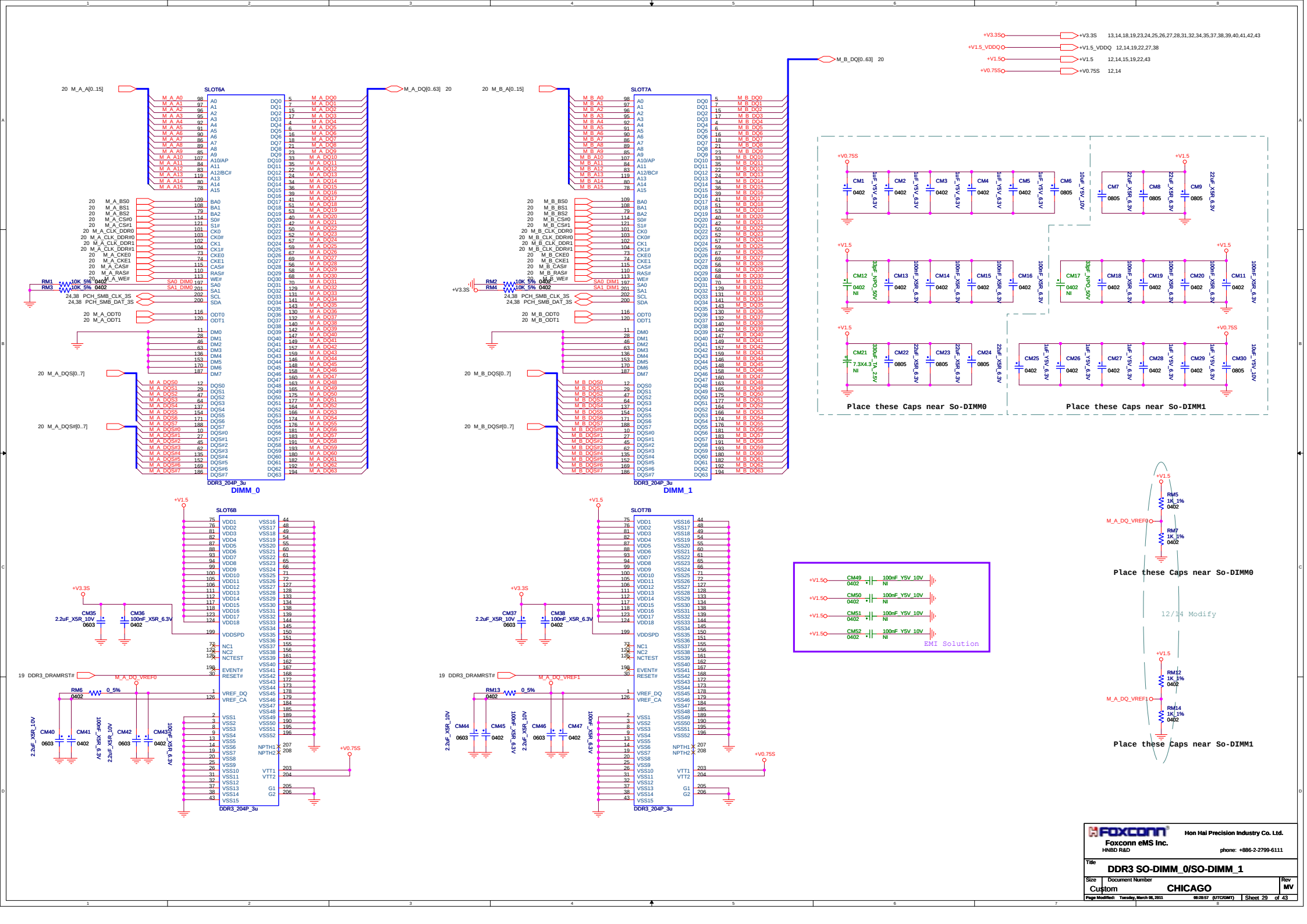

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Title	DDR3 SO-DIMM_0/SO-DIMM_1
Size: Custom	Document Number: CHICAGO
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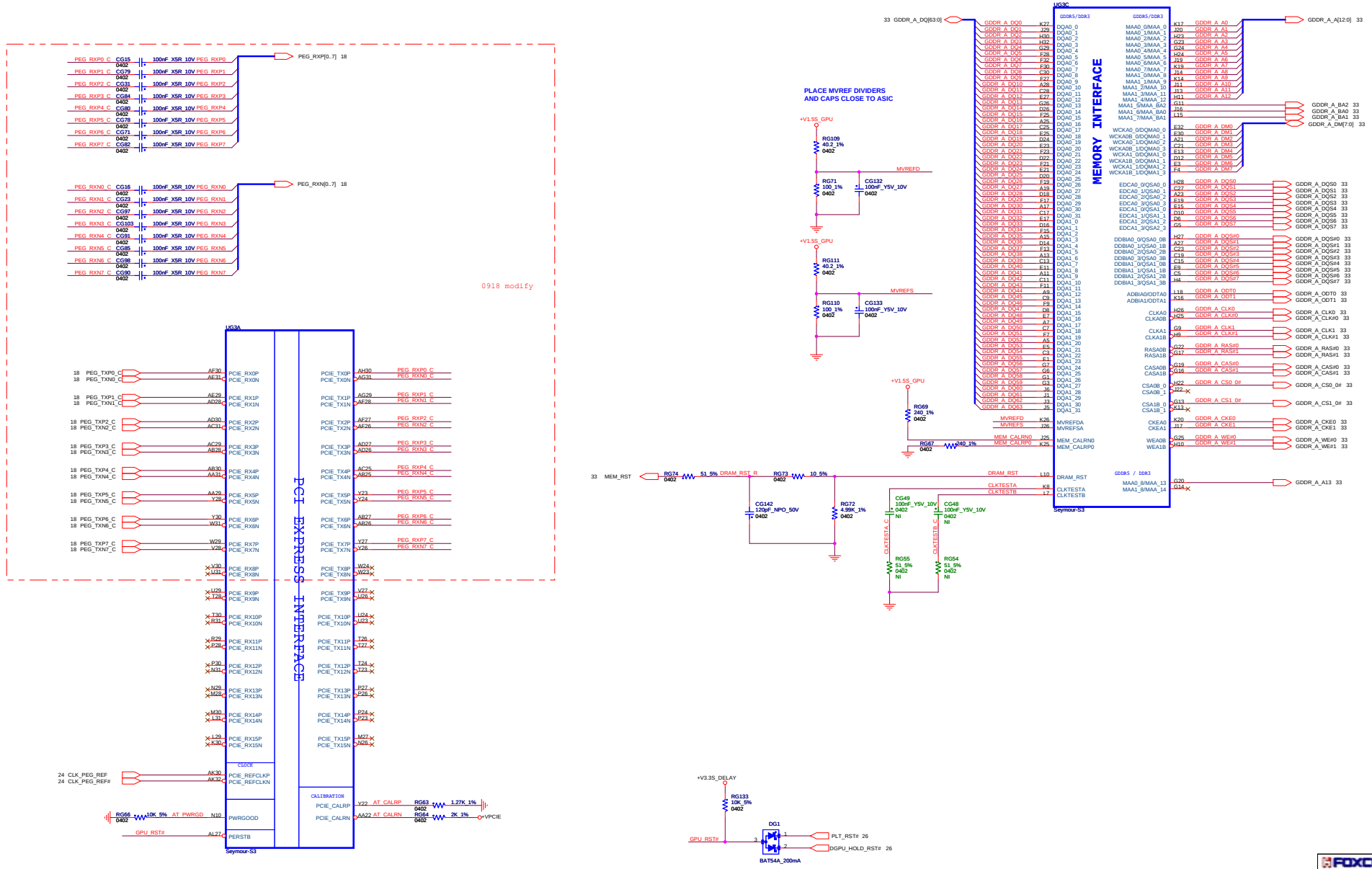

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Title: VGA_S3 (PCI-E) 1/3

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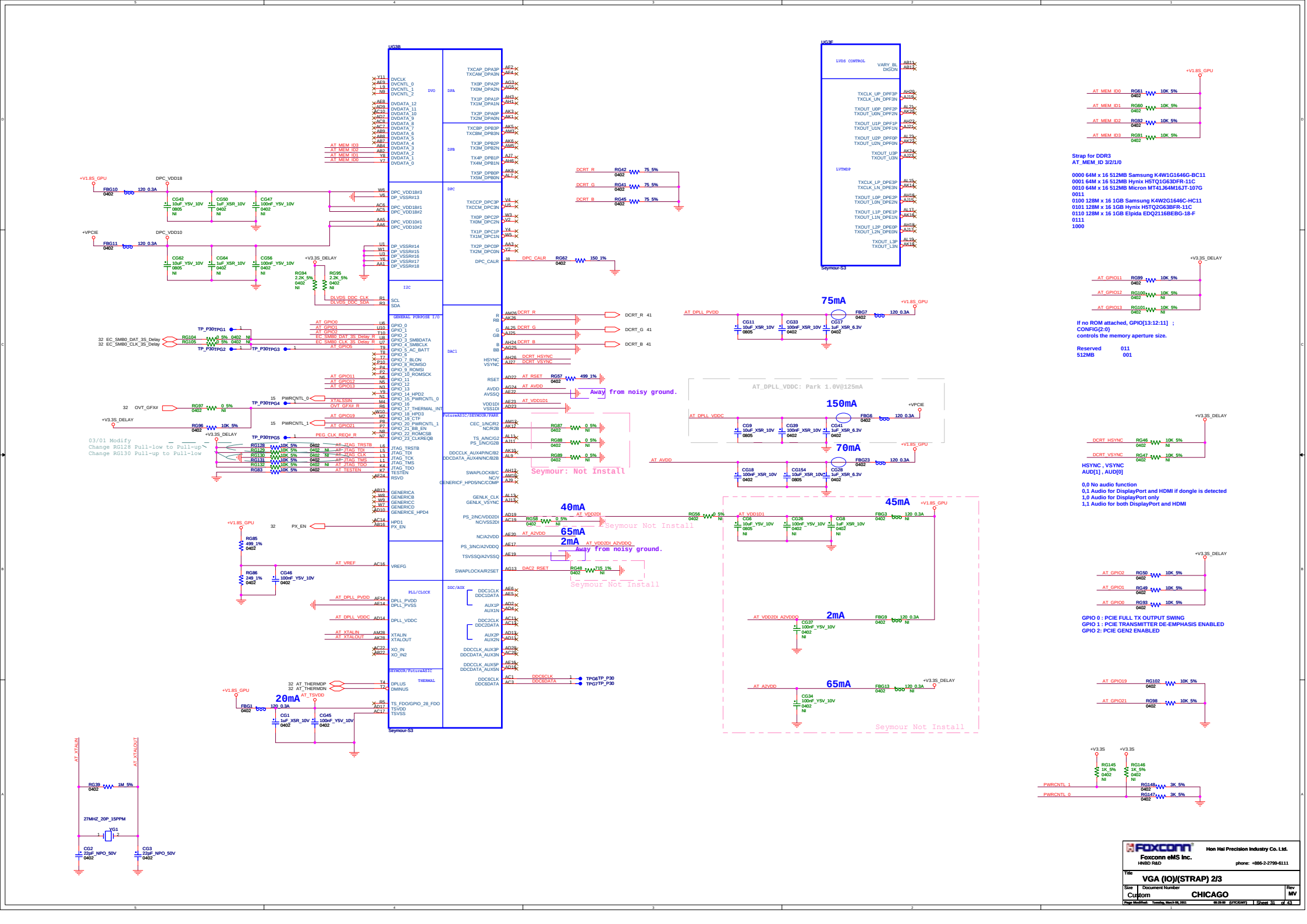
UG3B
Seymour-S3
UG3F
Seymour-S3
Strap for DDR3
AT_MEM_ID 3/2/1/0
0000 64M x 16 512MB Samsung K4W1G1646G-BC11
0001 64M x 16 512MB Hynix H5TQ1G63DFR-11C
0010 64M x 16 512MB Micron MT41J64M16JT-107G
0011
0100 128M x 16 1GB Samsung K4W2G1646C-HC11
0101 128M x 16 1GB Hynix H5TQ2G63BFR-11C
0110 128M x 16 1GB Elpida EDQ2116BEBG-18-F
0111
1000
If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.
Reserved 011
512MB 001
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
03/01 Modify
Change RG128 Pull-low to Pull-up
Change RG130 Pull-up to Pull-low
Away from noisy ground.
Seymour: Not Install
Seymour Not Install
AT_DPLL_VDDC: Park 1.0V@125mA
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
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Title
VGA (IO)/(STRAP) 2/3
Size
Custom
Document Number
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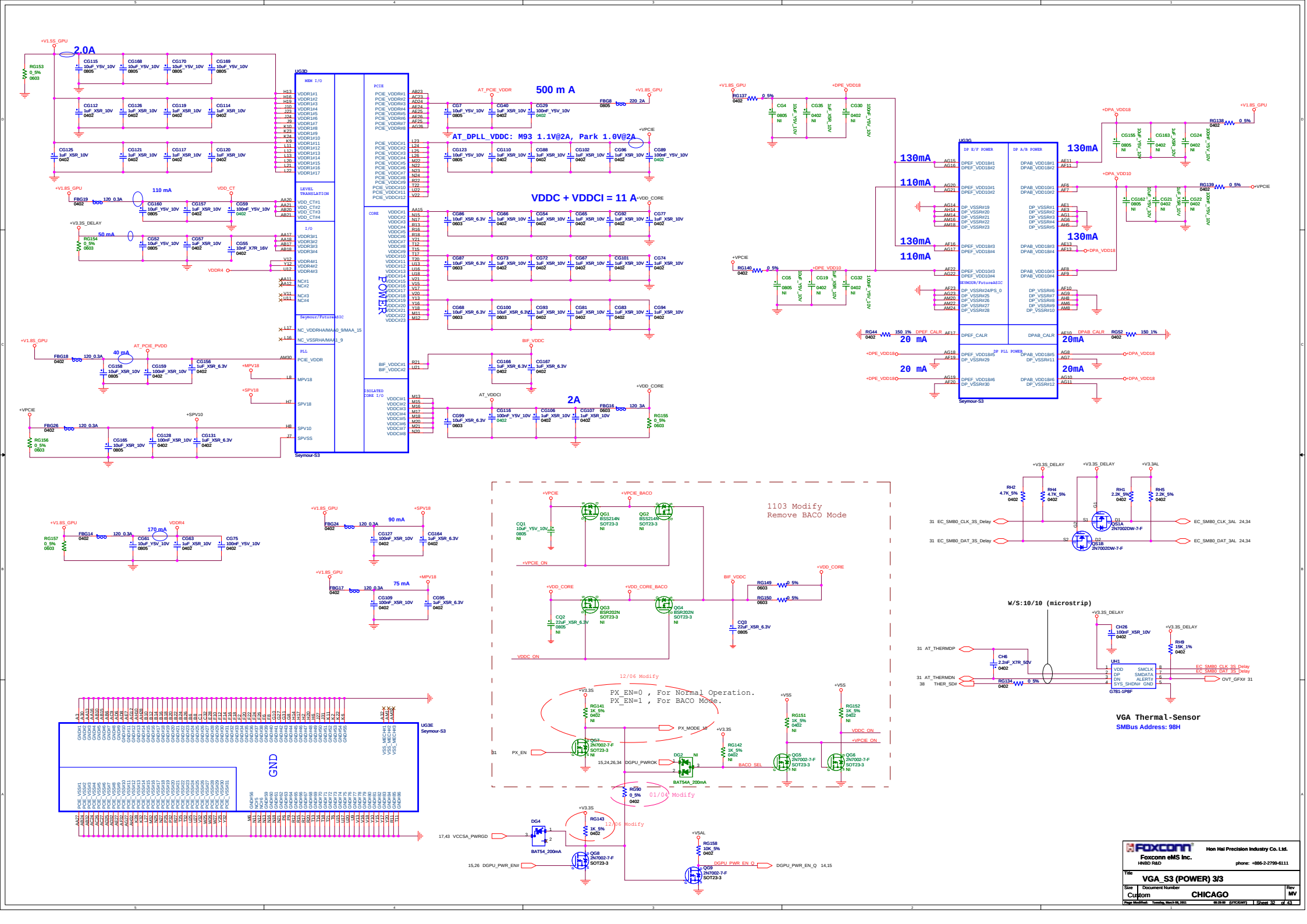
2.0A
500 m A
AT_DPLL_VDDC: M93 1.1V@2A, Park 1.0V@2A
VDDC + VDDCI = 11 A
2A
UG3D
Seymour-S3
UG3E
Seymour-S3
UG3G
Seymour-S3
1103 Modify
Remove BACO Mode
12/06 Modify
01/04 Modify
PX_EN=0 , For Normal Operation.
PX_EN=1 , For BACO Mode.
W/S:10/10 (microstrip)
VGA Thermal-Sensor
SMBus Address: 98H
GND
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VGA_S3 (POWER) 3/3
Custom
CHICAGO
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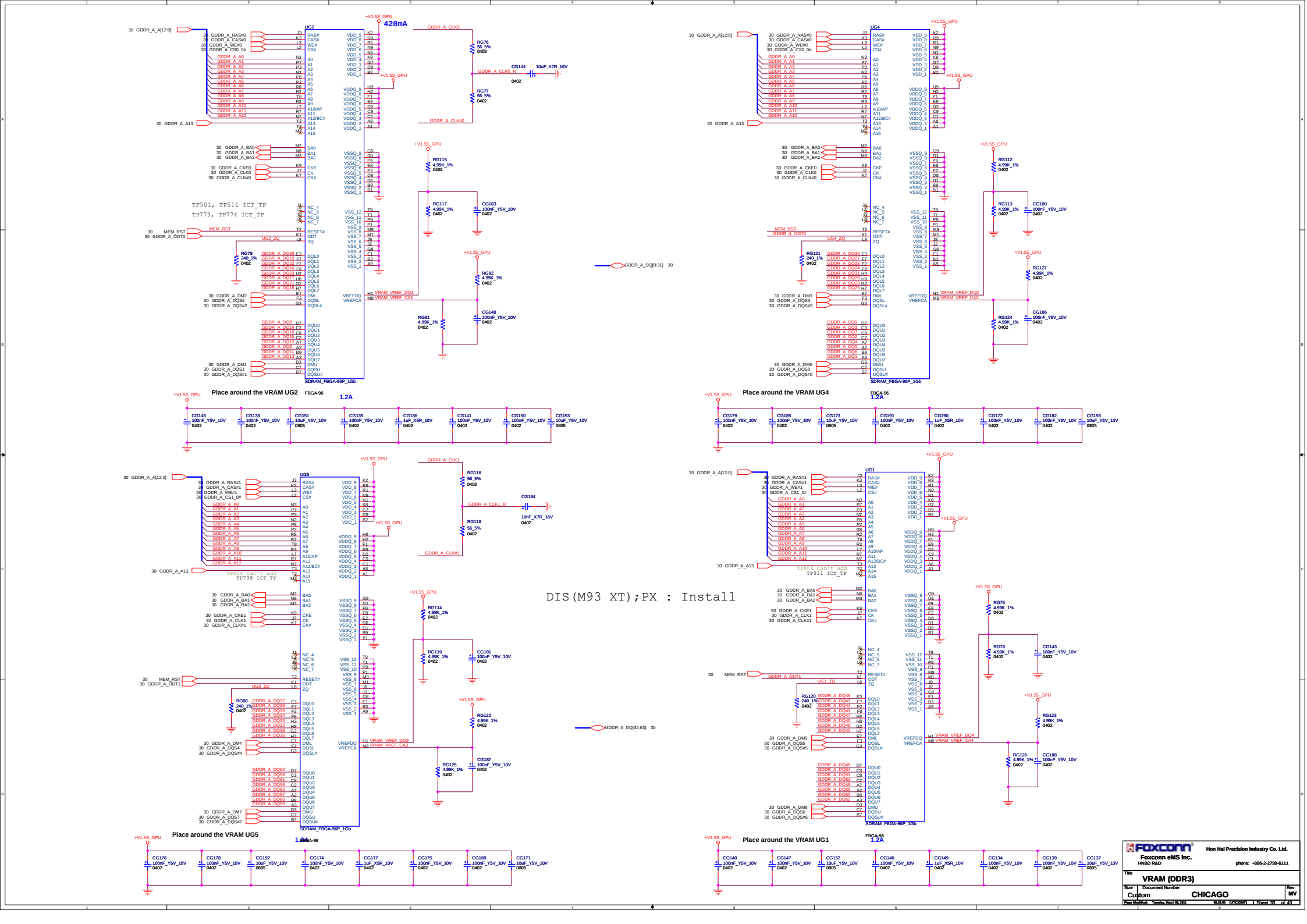
420mA
UG2
TP501, TP511 ICT_TP
TP773, TP774 ICT_TP
Place around the VRAM UG2
FBGA-96
1.2A
SDRAM_FBGA-96P_1Gb
UG4
Place around the VRAM UG4
UG5
TP798 ICT_TP
Place around the VRAM UG5
UG1
TP811 ICT_TP
Place around the VRAM UG1
DIS(M93 XT);PX : Install
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VRAM (DDR3)
Custom
CHICAGO
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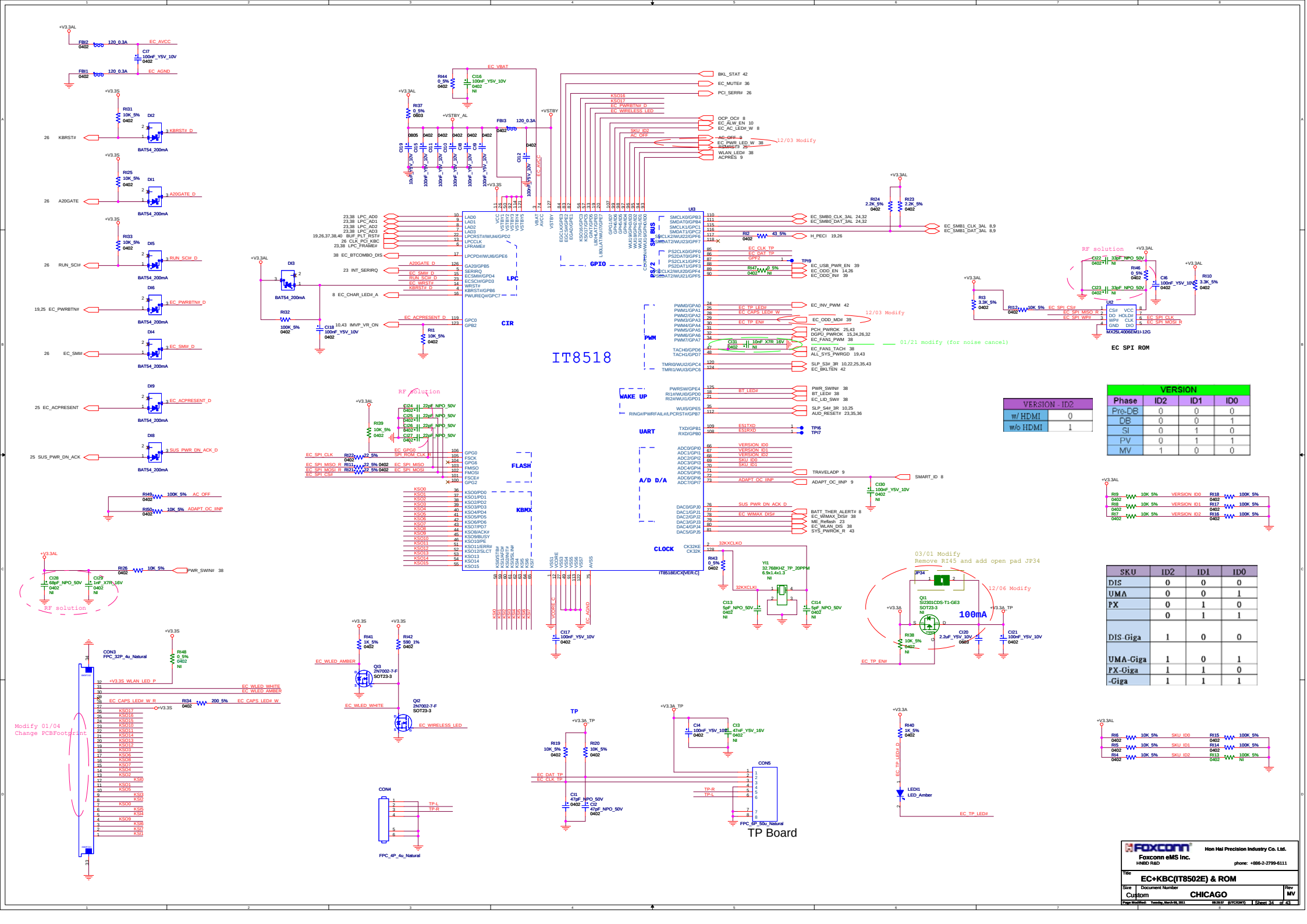
IT8518
IT8518E/CX[VER.C]
LPC
CIR
FLASH
KBMX
GPIO
SMB
PWM
WAKE UP
UART
A/D D/A
CLOCK
RF solution
01/21 modify (for noise cancel)
12/03 Modify
03/01 Modify
Remove RI45 and add open pad JP34
12/06 Modify
100mA
Modify 01/04
Change PCBFootprint
TP Board
EC SPI ROM
VERSION
Phase ID2 ID1 ID0
Pre-DB 0 0 0
DB 0 0 1
SI 0 1 0
PV 0 1 1
MV 1 0 0
VERSION - ID2
w/ HDMI 0
w/o HDMI 1
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
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Title
EC+KBC(IT8502E) & ROM
Size
Custom
Document Number
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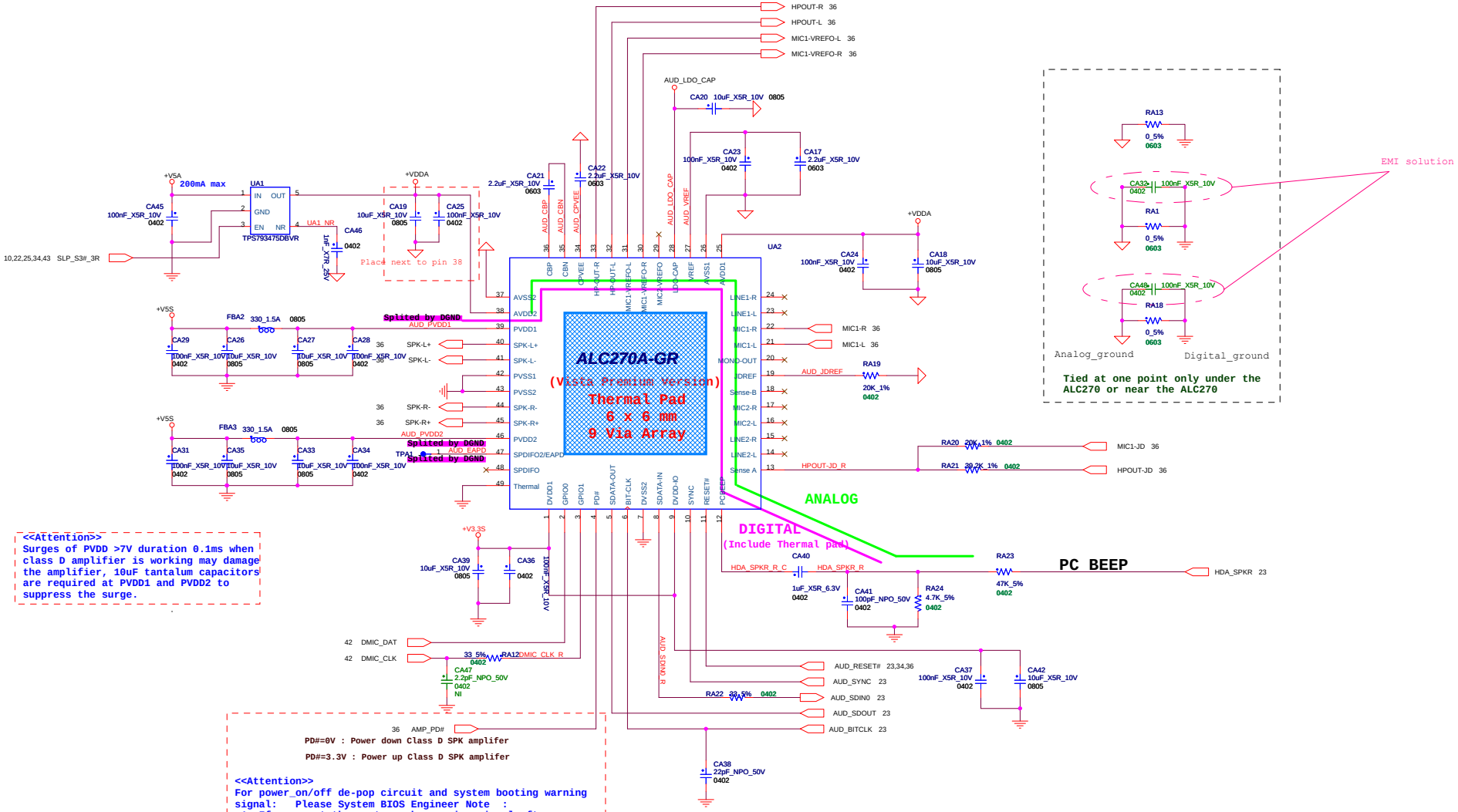

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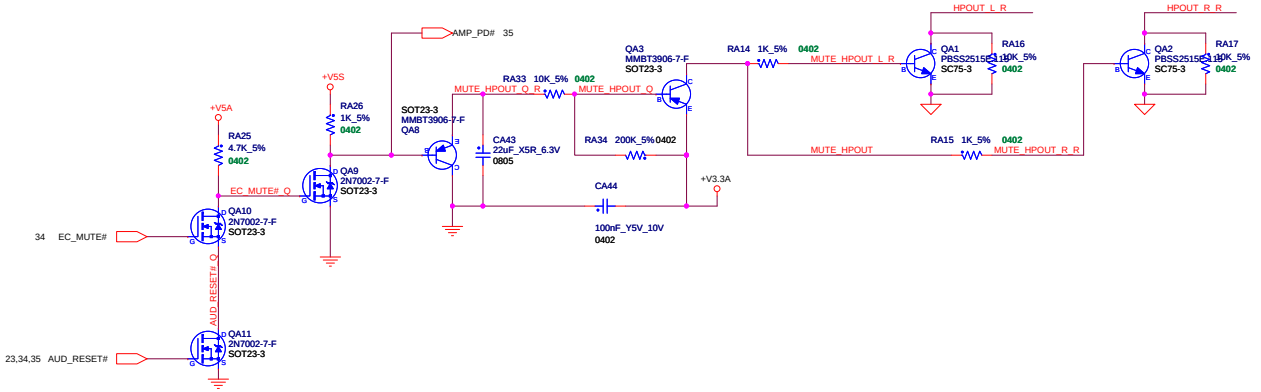
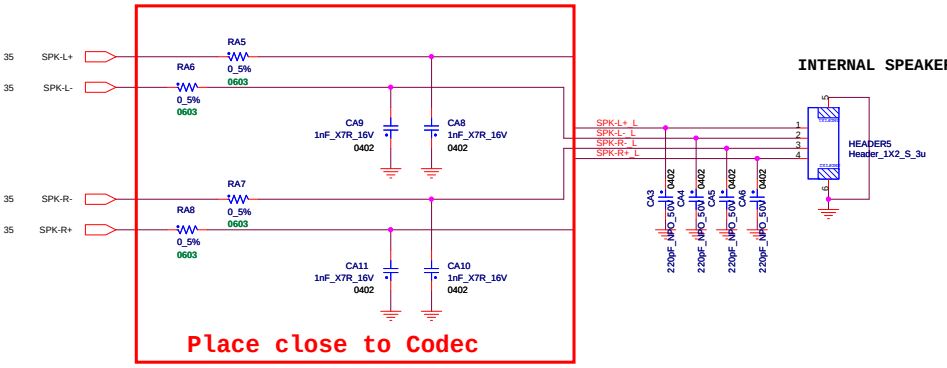
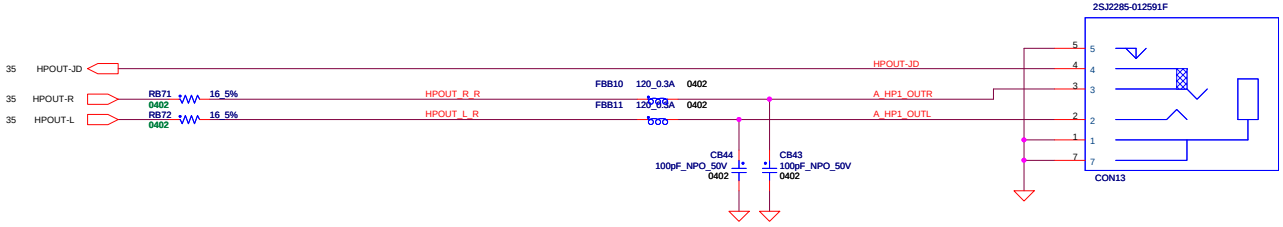
Mute



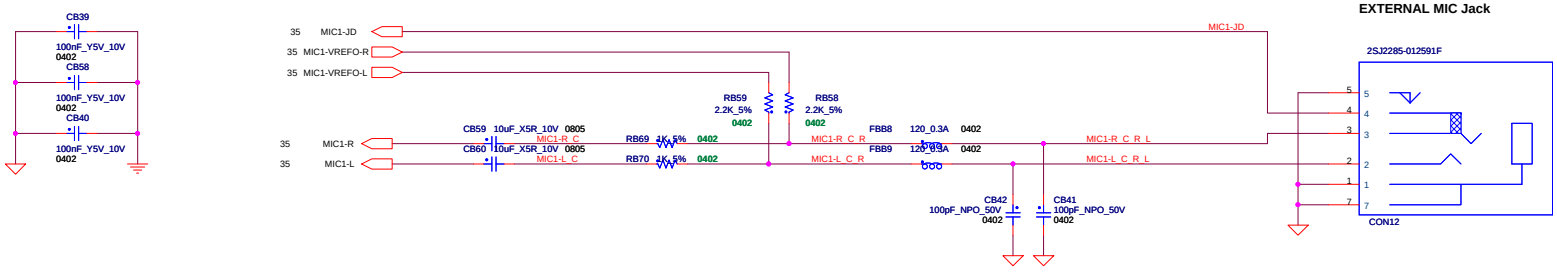
INTERNAL SPEAKER



HEADPHONE Jack



EXTERNAL MIC Jack



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Title: **Audio (JACK+AMP+SPK+Mute)**

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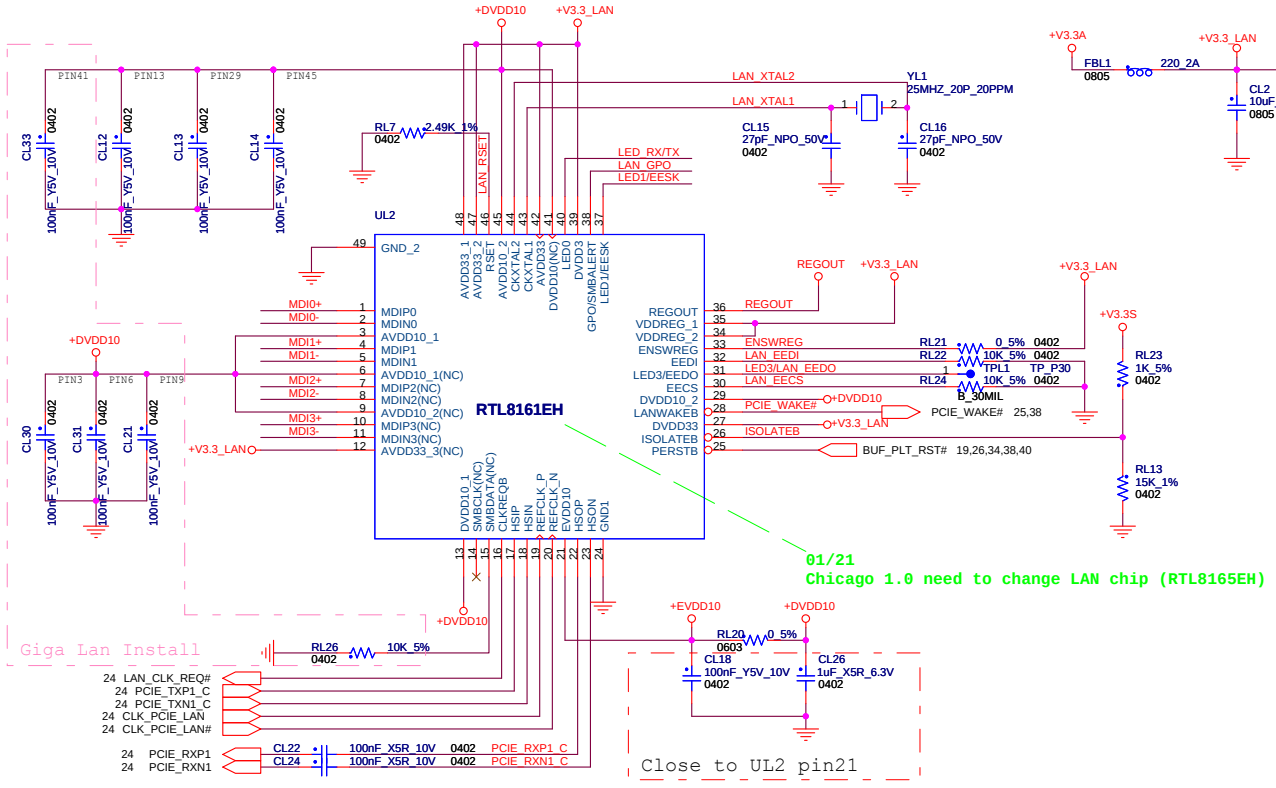
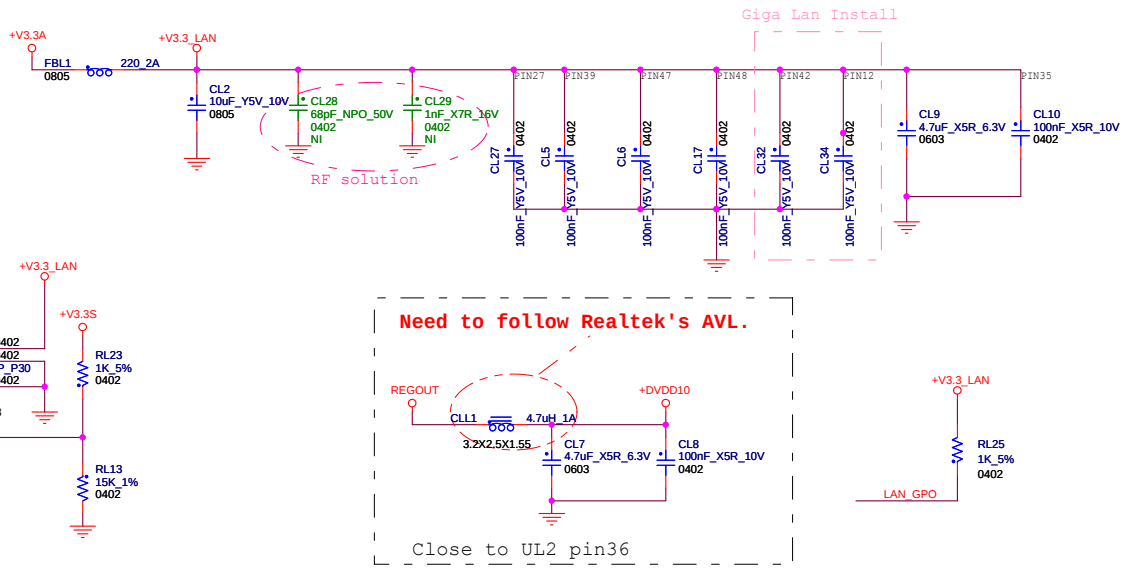
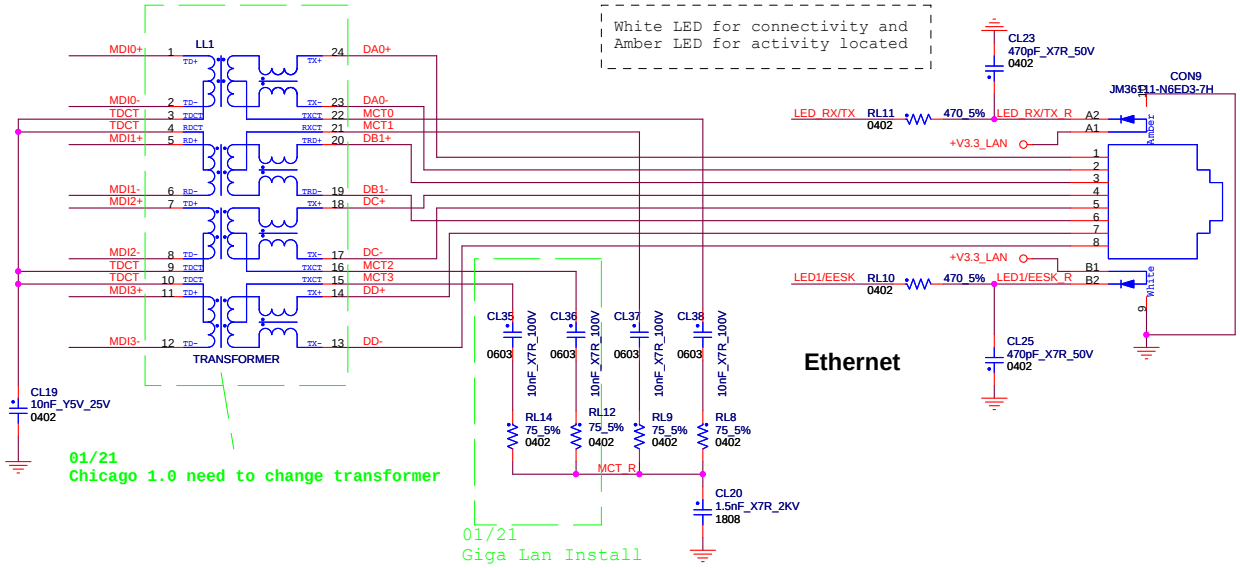


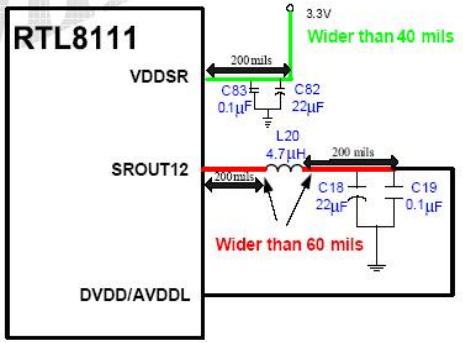




7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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Title	LAN (RTL8165EH)
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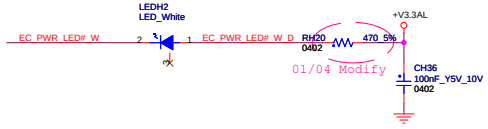
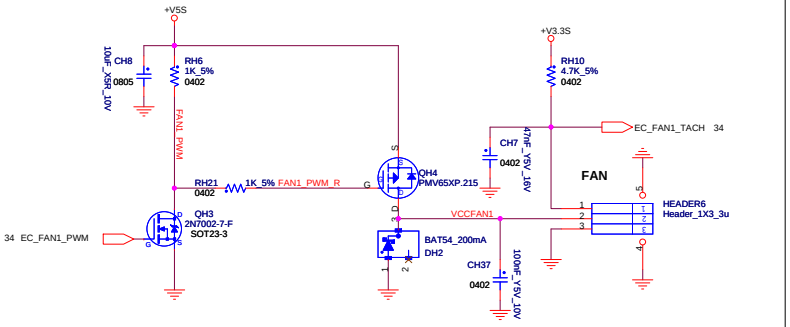
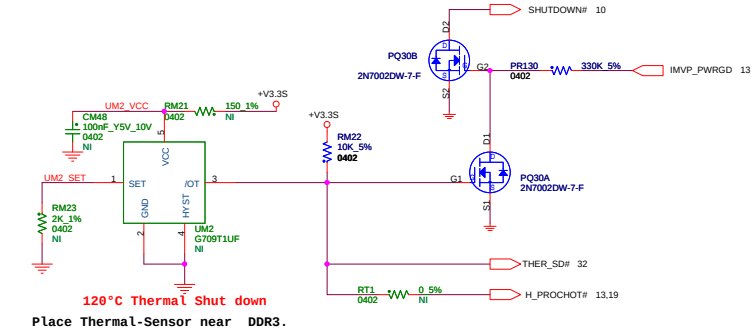
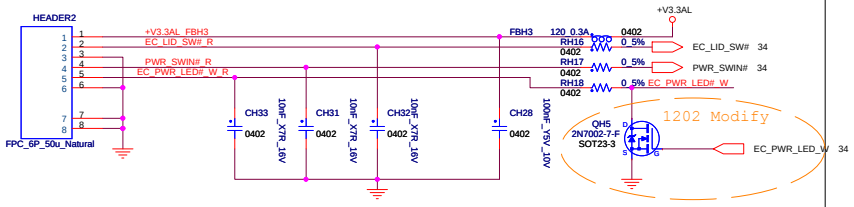
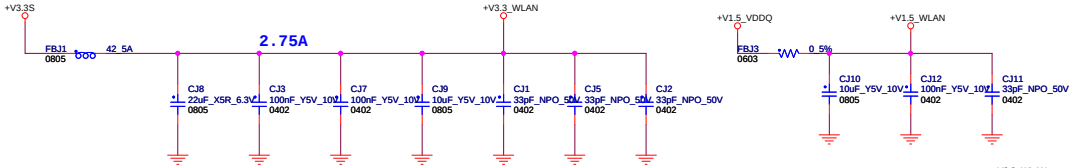


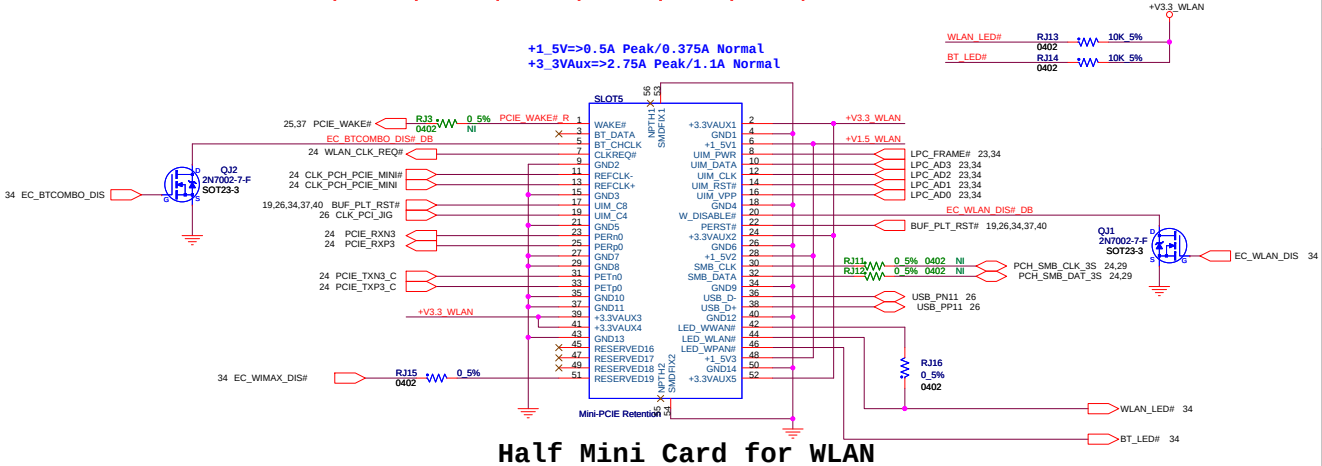




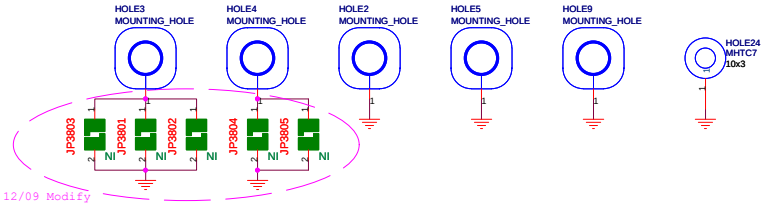
PWR Board CONN.

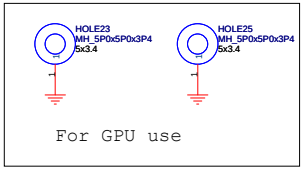


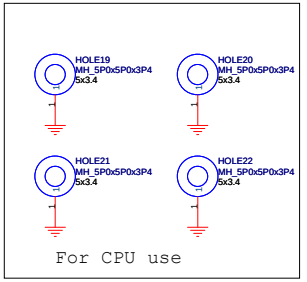




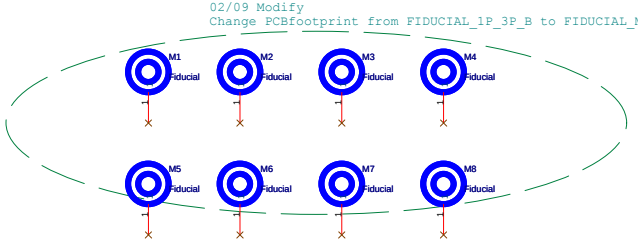
Half Mini Card for WLAN







Mounting HOLE



Fiducial Mark

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Title: Mini PCIe & RJ11 & BT

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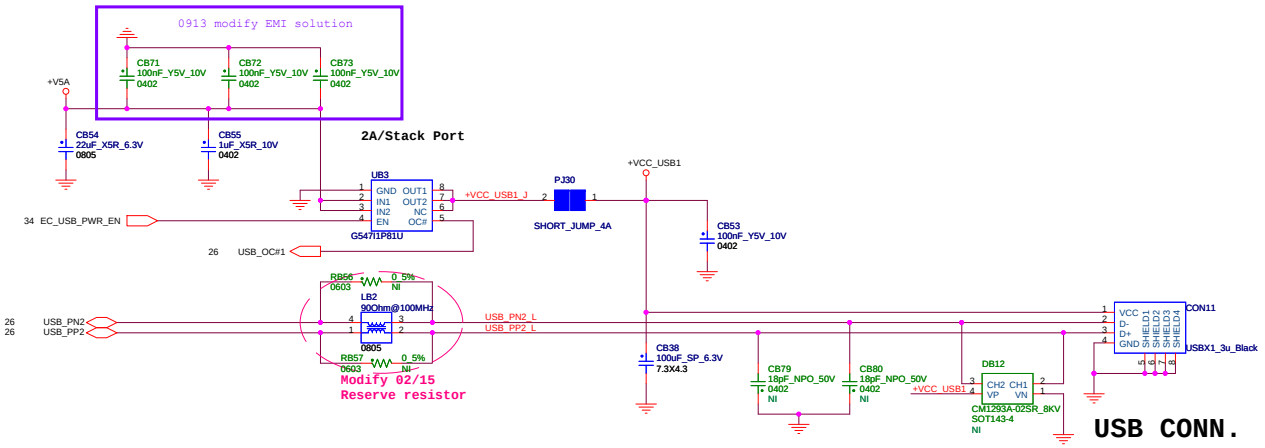
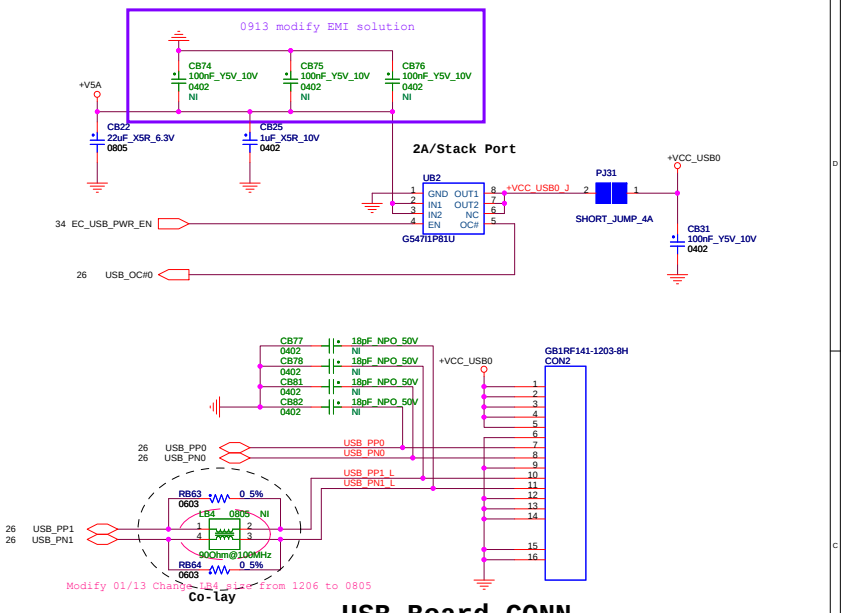
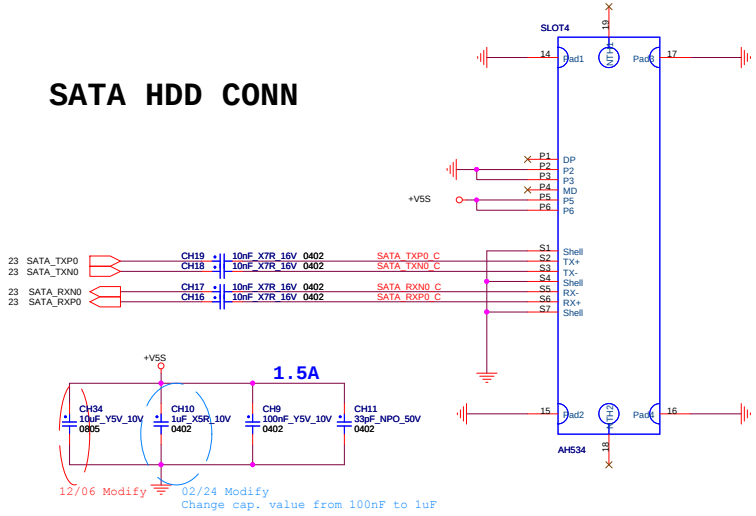


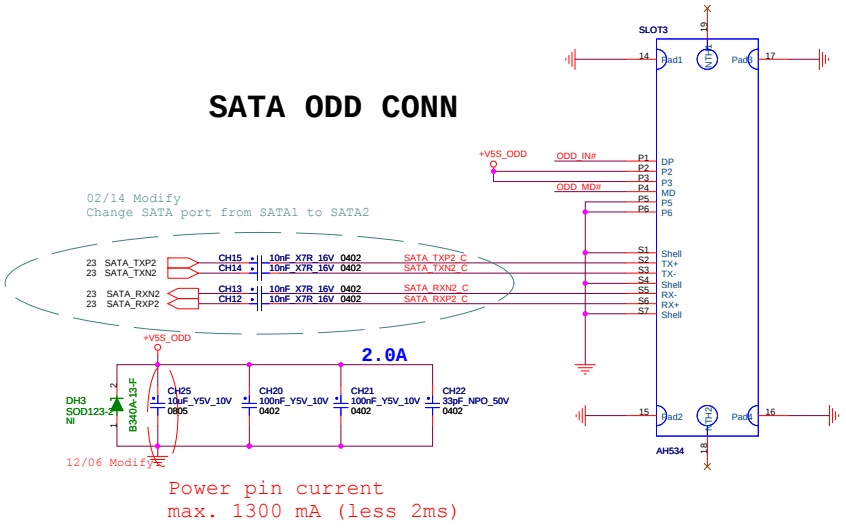


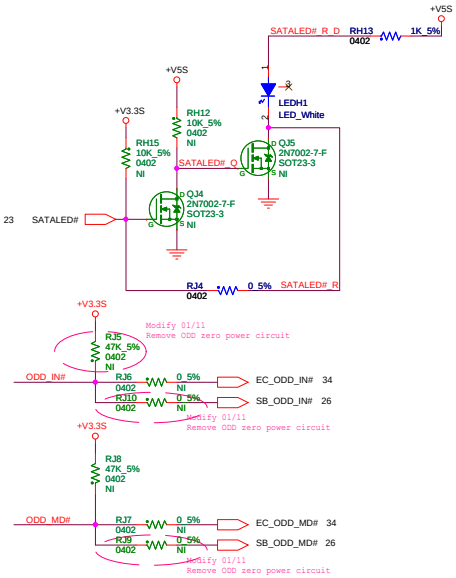
HDD/ODD Status LED

SATA HDD CONN



SATA ODD CONN





FOXCONN
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HNBD R&D
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Title: USBX2/USB DB CONN./SATA CONN.

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Custom	CHICAGO	MV

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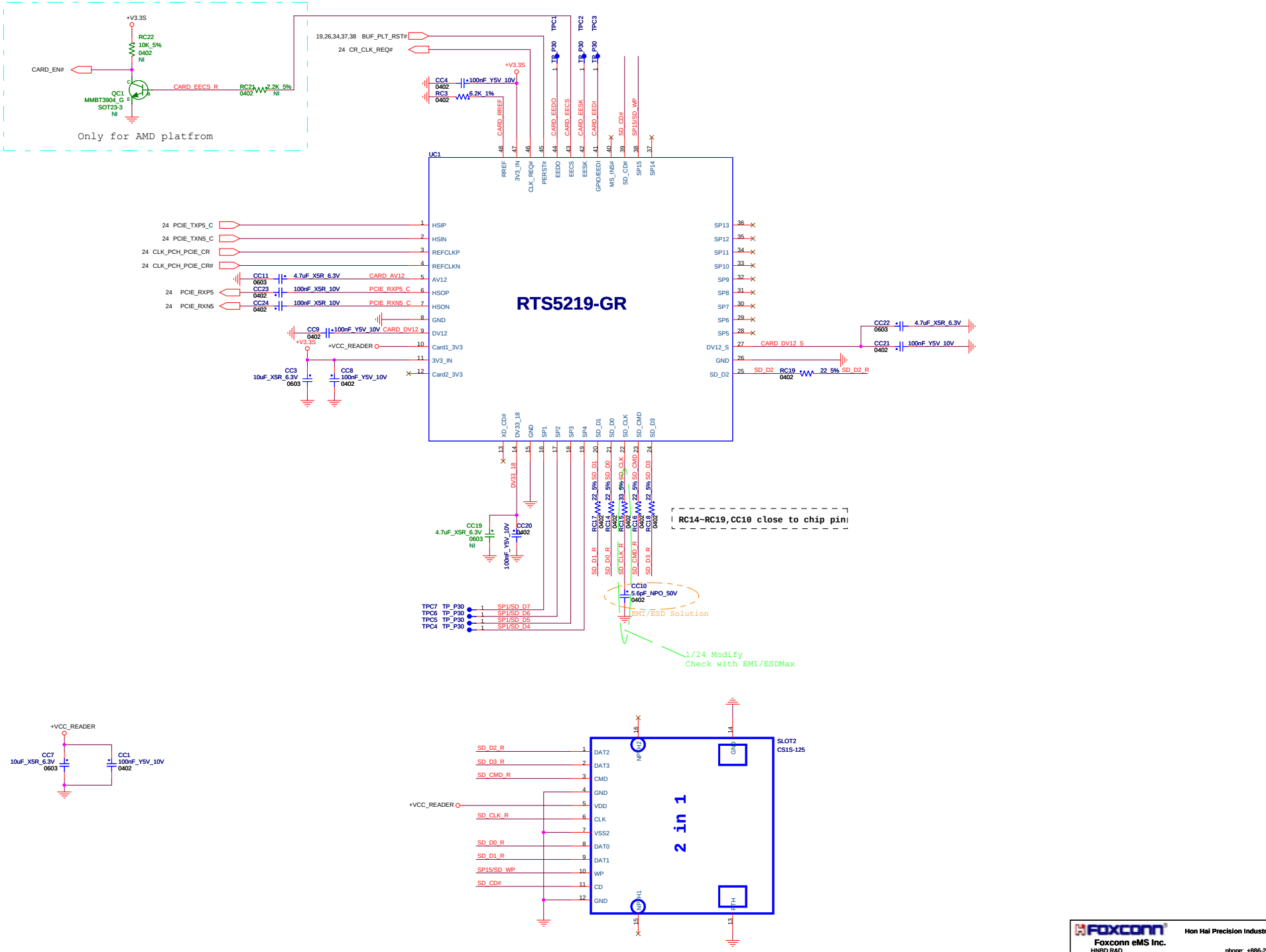

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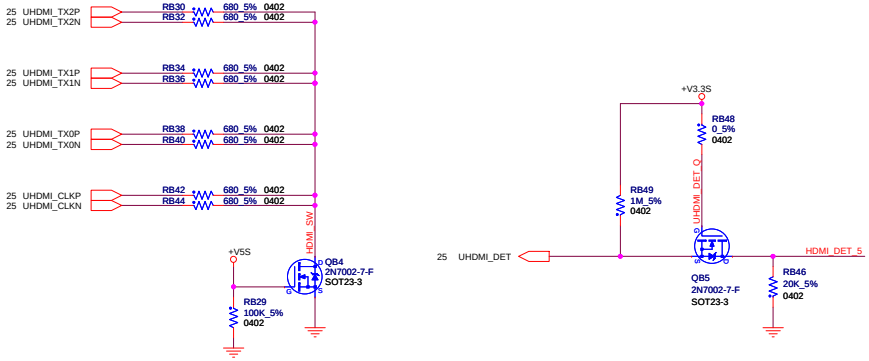

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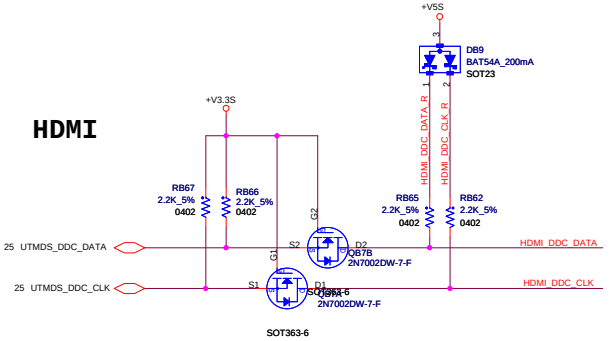

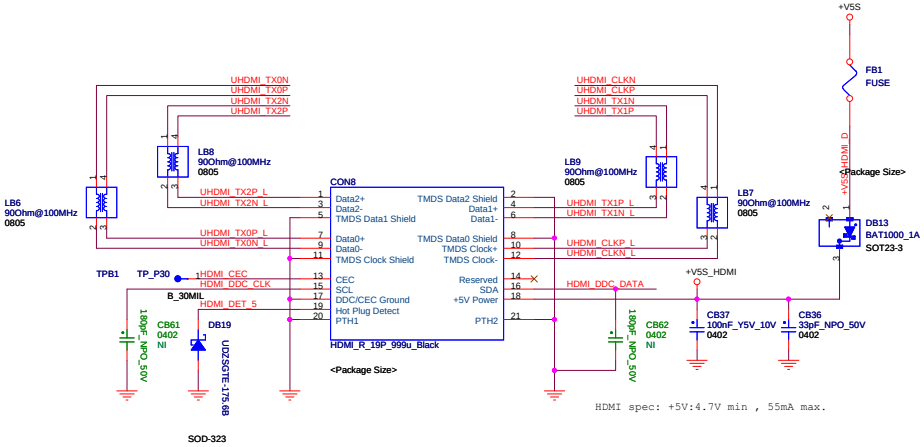

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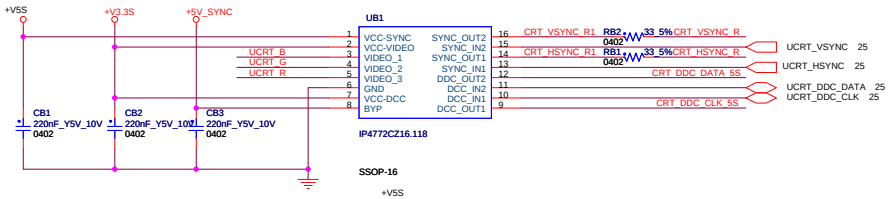

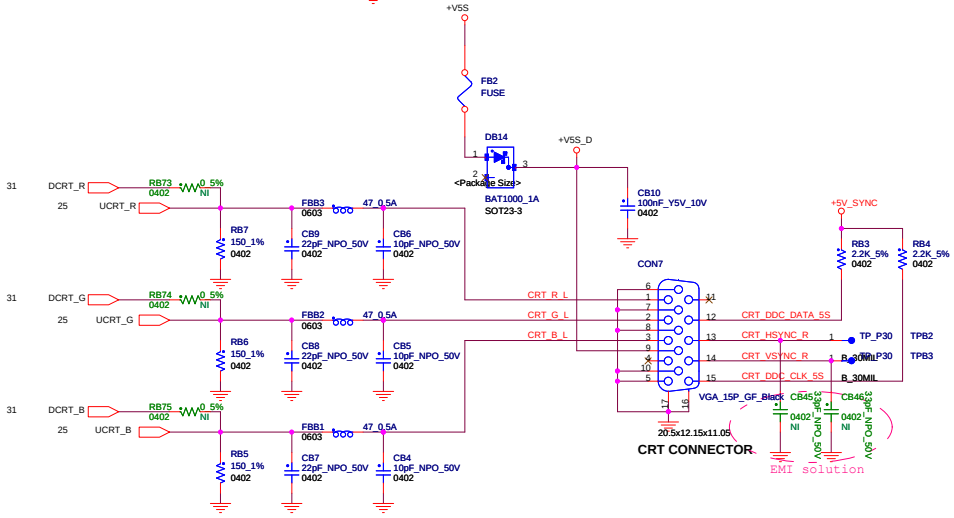

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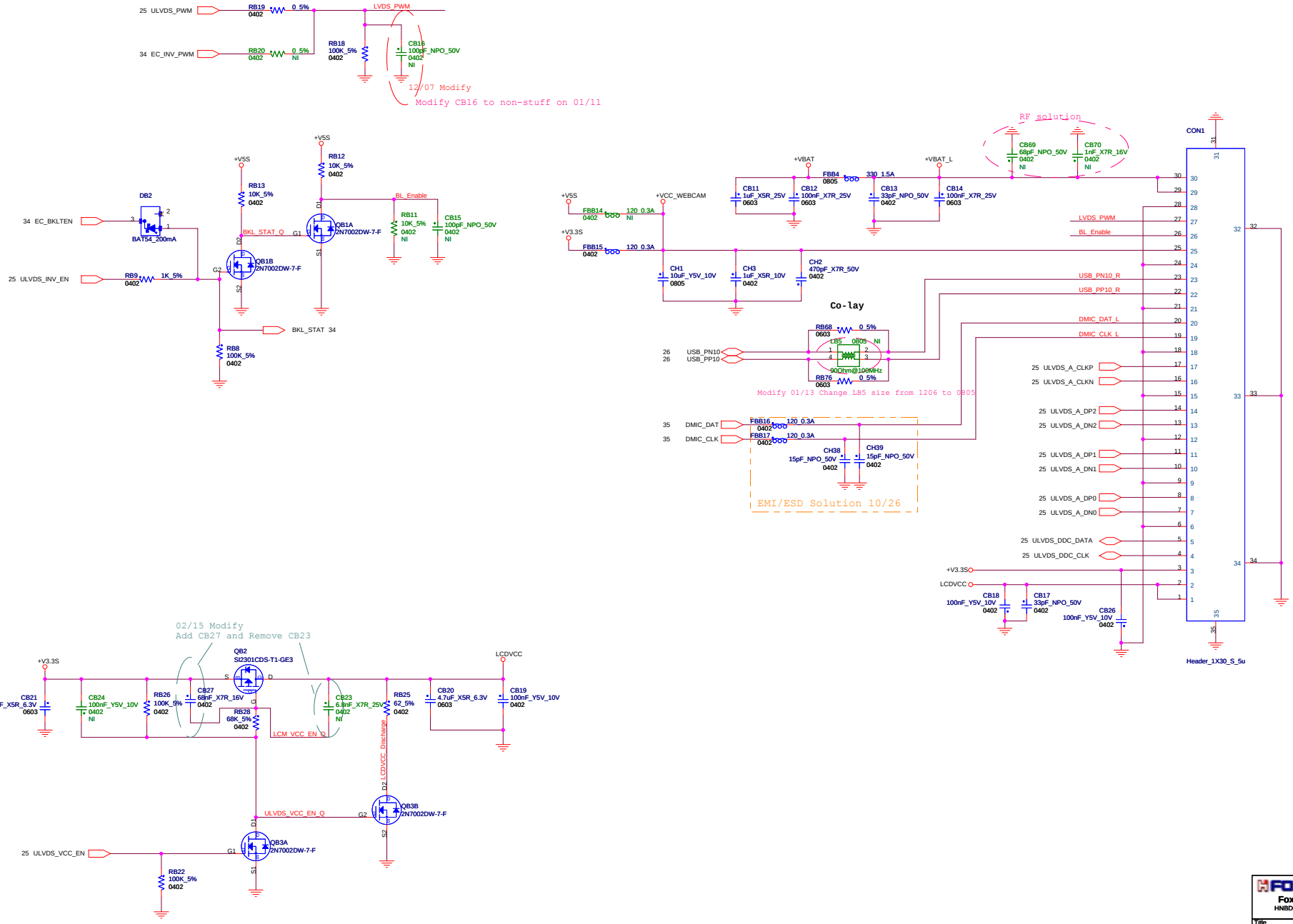

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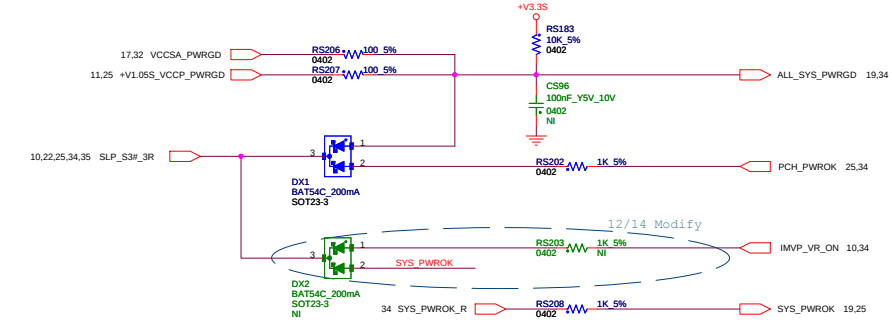

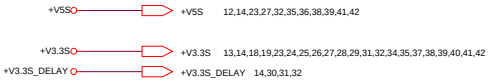

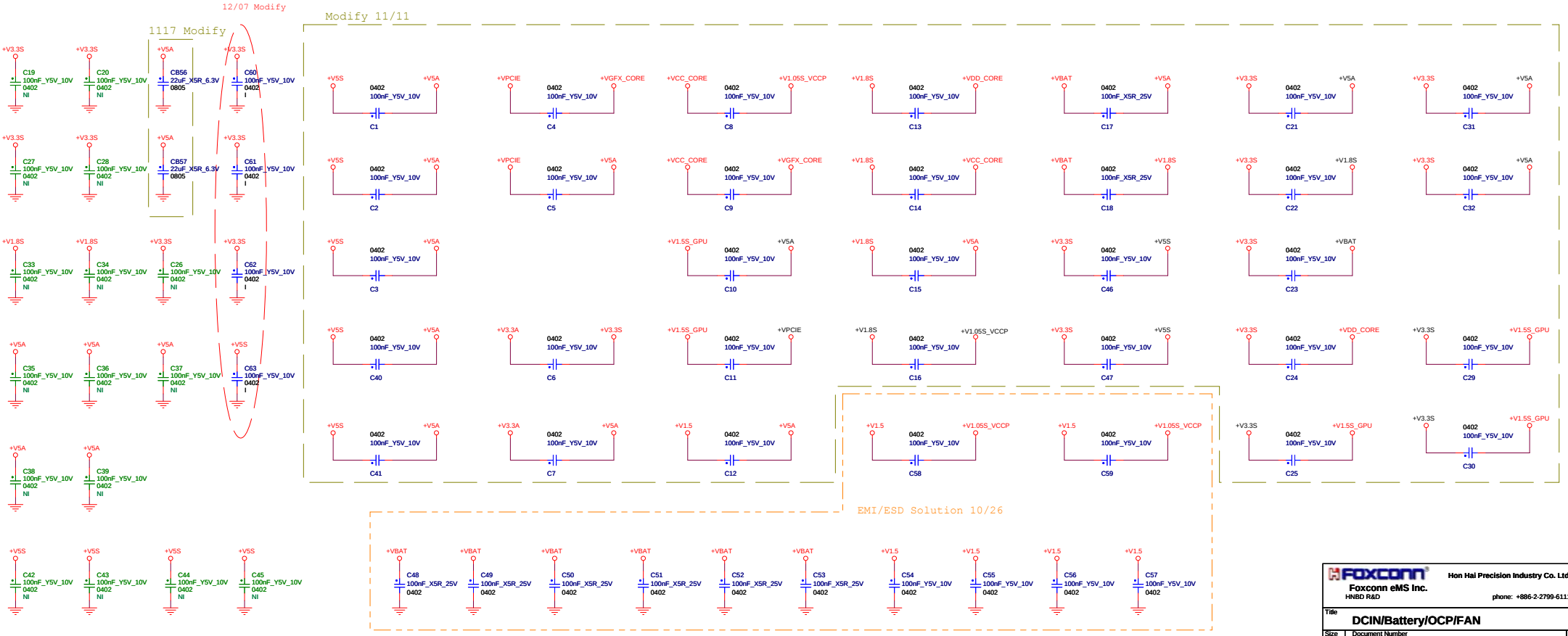

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