

Compal confidential

Schematics Document

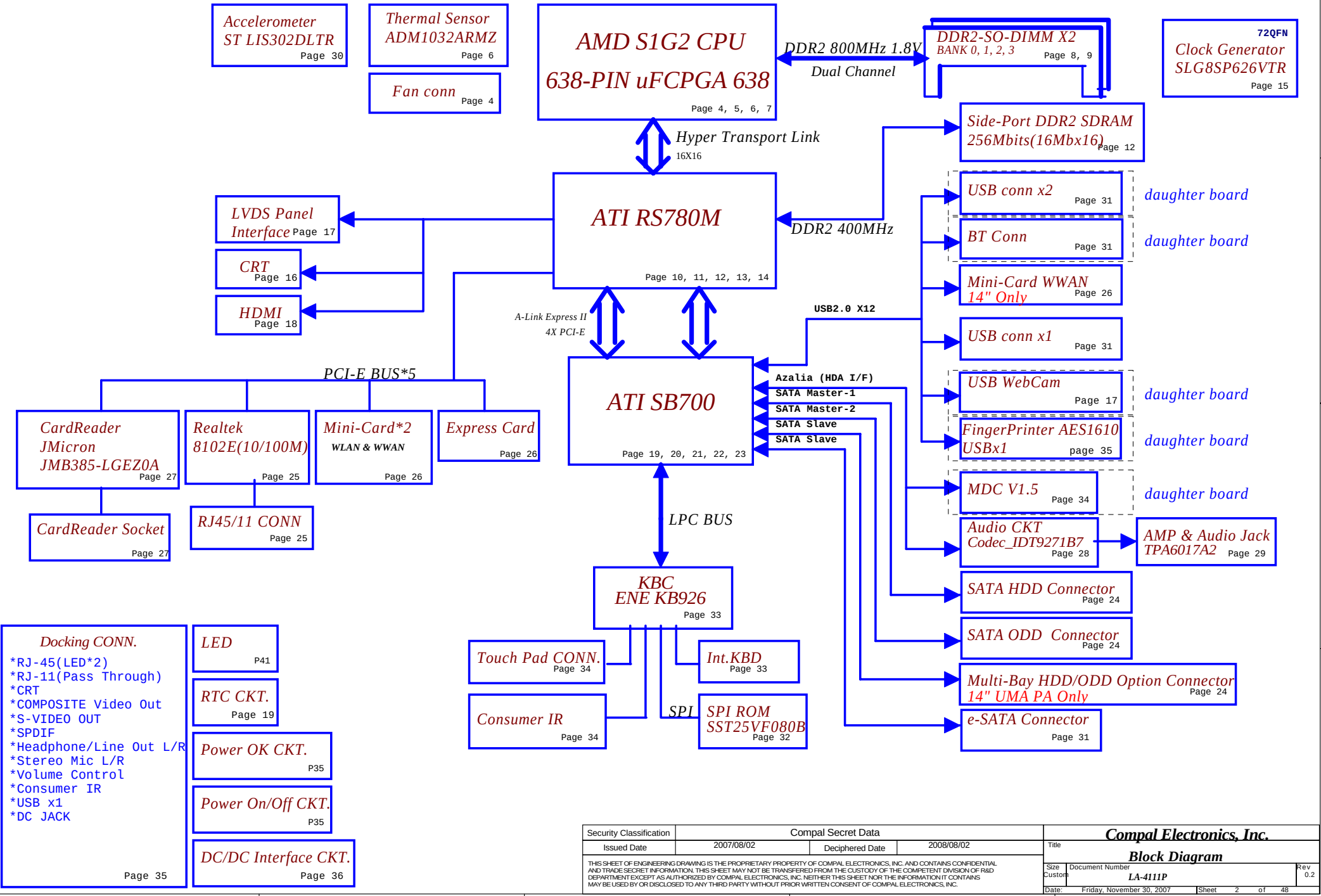
Mobile AMD S1G2 CPU with ATI
RS780M(NB) & SB700(SB) core logic

2007-12-03

REV:0.2

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Cover Sheet	
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Consumer AMD 14" UMA - Ripley (JBL20)



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Voltage Rails

0 MEANS ON X MEANS OFF

power plane				
State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus1 address

EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	CPU	98H	1001 100X b
24C16	A0H	1010 000X b	AD1032-2 CPU	9AH	1001 101X b

Symbol Note :

 : means Digital Ground

 : means Analog Ground

 Layout Notes

Please see VGA@ as no install. No support RX780M.

12/03 update

 : Question Area Mark.(Wait check)

"*" as default BOM setting

PA@ : means install when Ripley PA.

PR@ : means install when Ripley PR.

RM@ : means install when Rachman.

*RP@ : means install when Ripley.

SIDE@ : means install when SidePort support.

*DOCK@ : means install when DOCK support.

*CY@ : means install when Function Board-Cypress.

ENE@ : means install when Function Board-ENE.

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

45@ : Install when 45 level Assy.

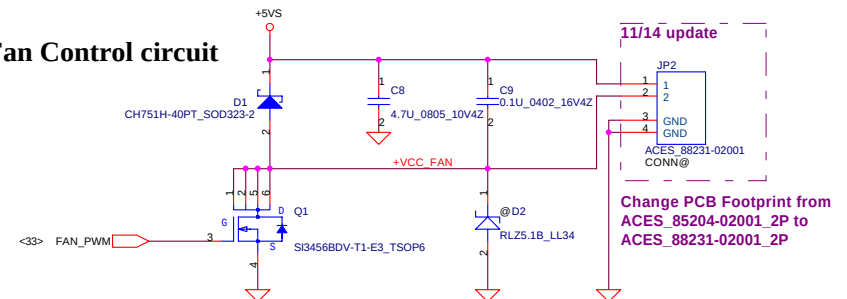
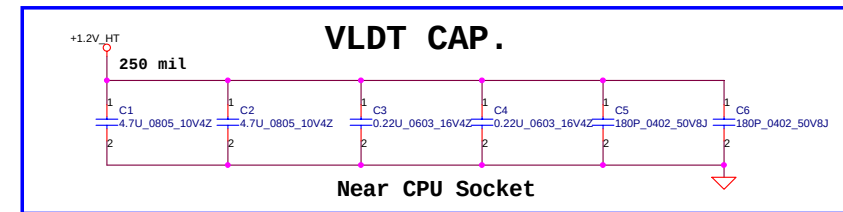
D3E@ : means install when JMircon D3E support

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	X
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	V
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

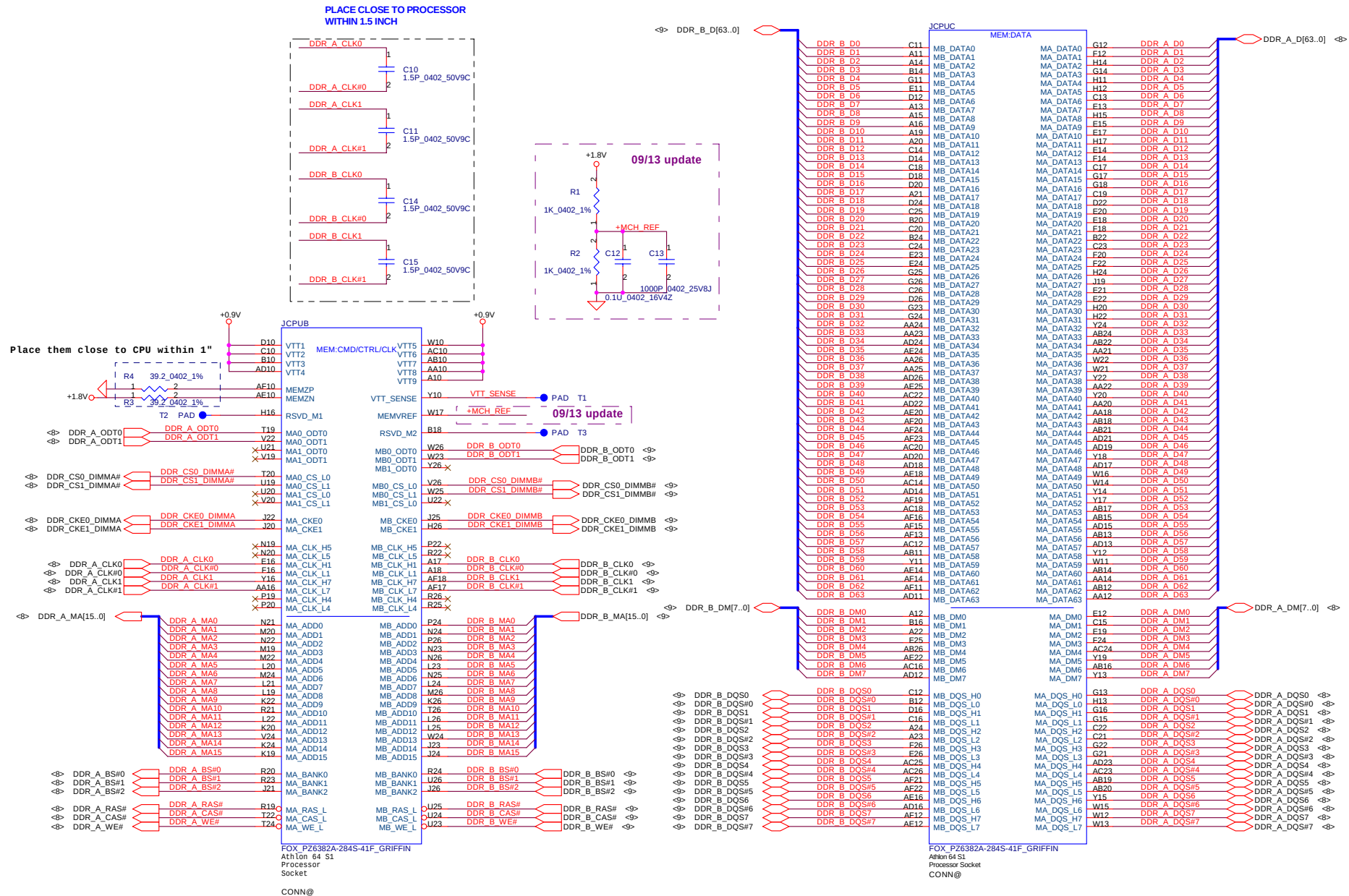
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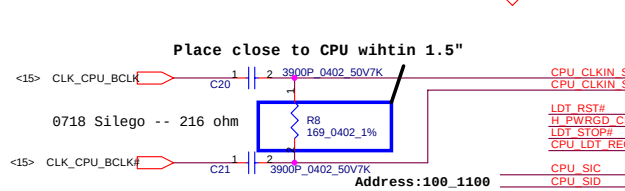
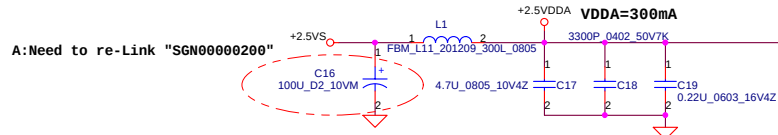


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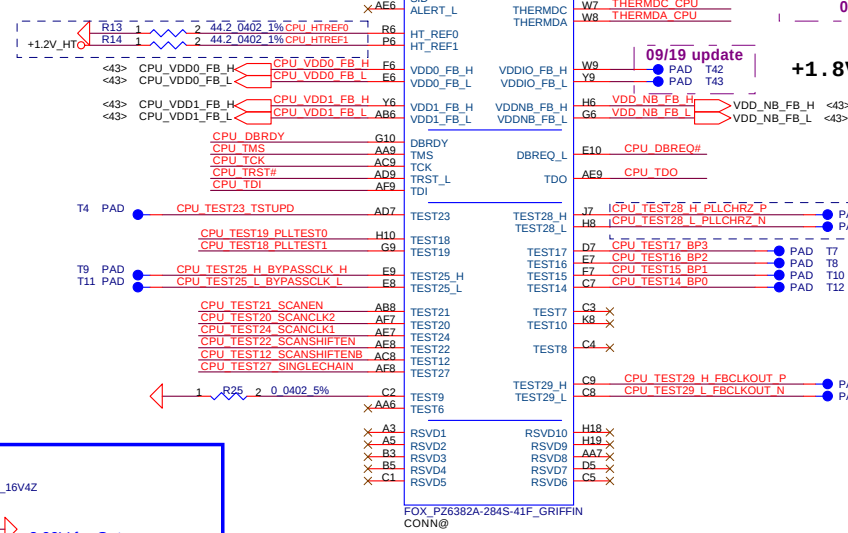
Processor DDR2 Memory Interface



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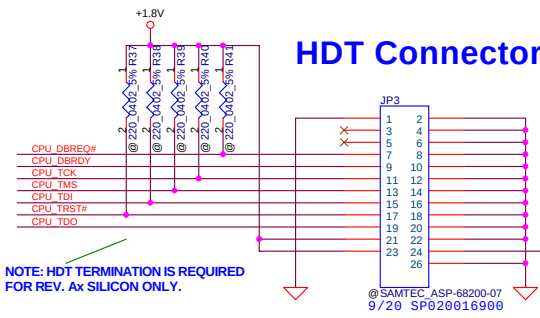
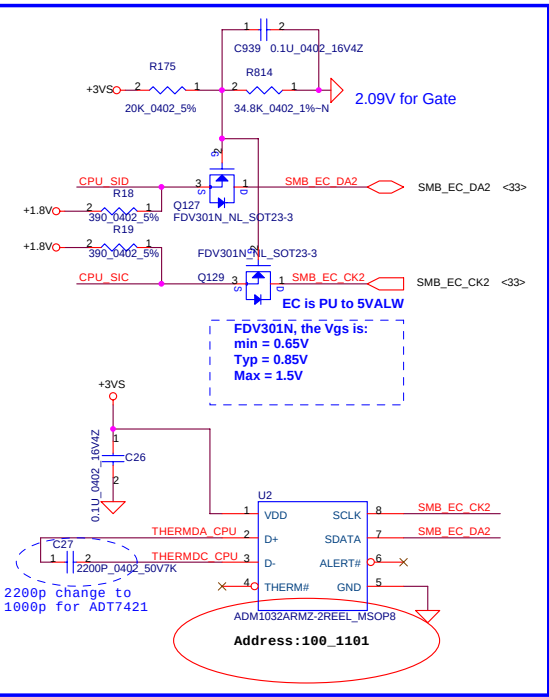
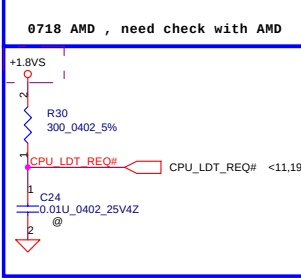
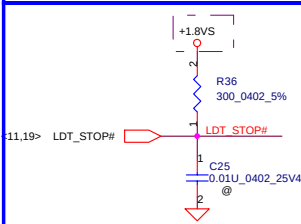
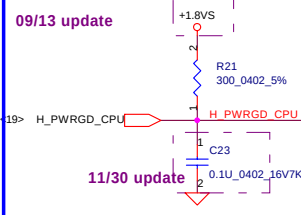
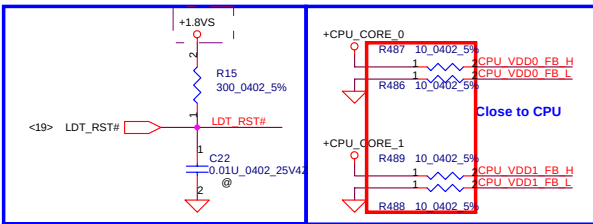


Address:100_1100

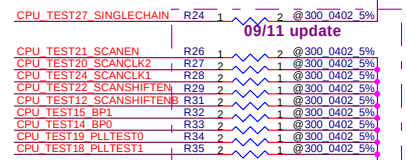


+1.8V sense no support

route as differential as short as possible testpoint under package



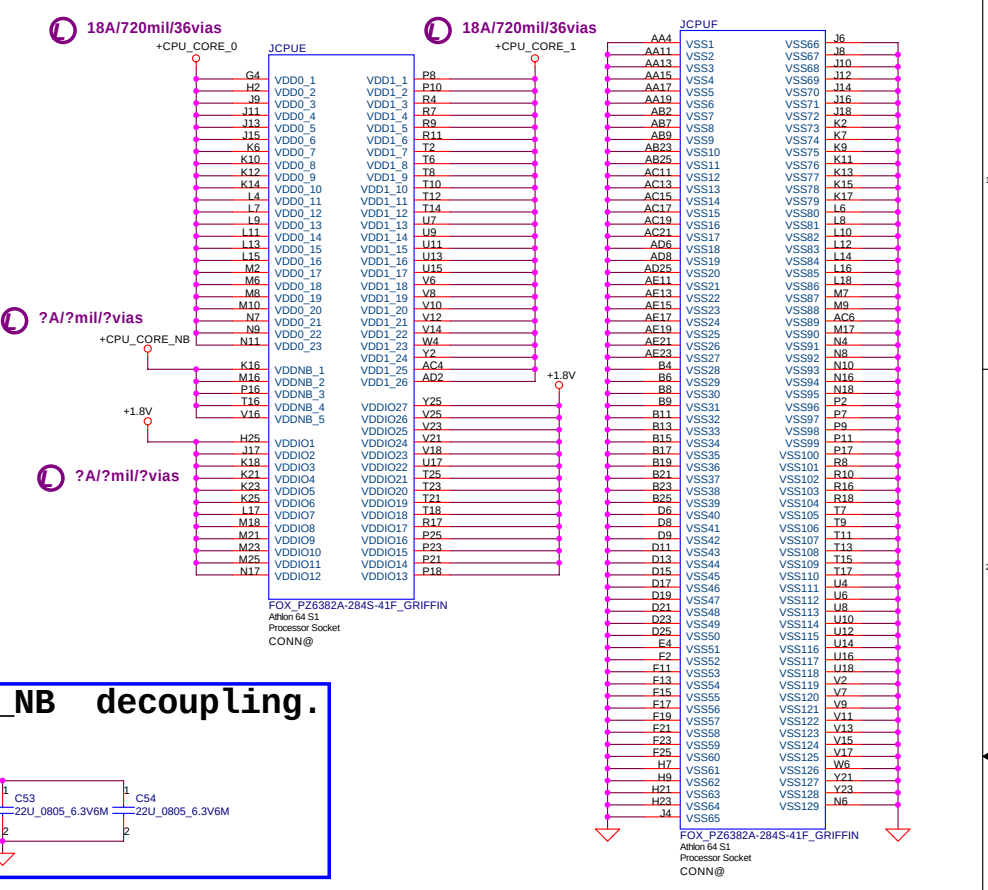
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.



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VDD(+CPU_CORE) decoupling.



Under CPU Socket

Between CPU Socket and DIMM

Between DIMM0 and DIMM1

180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>

A: Add C165 and C176 to follow AMD Layout review recommend for EMI

C: Change to NBO CAP

+CPU_CORE_NB

The diagram shows three capacitors, C52, C53, and C54, connected in a star configuration. Each capacitor is labeled '220V_0805_6.3V6M'. The top terminals of all three capacitors are connected to a common point, which is connected to a red circle labeled '+CPU_CORE_NB'. The bottom terminals of all three capacitors are connected to a common point, which is connected to a red triangle pointing downwards, representing ground.

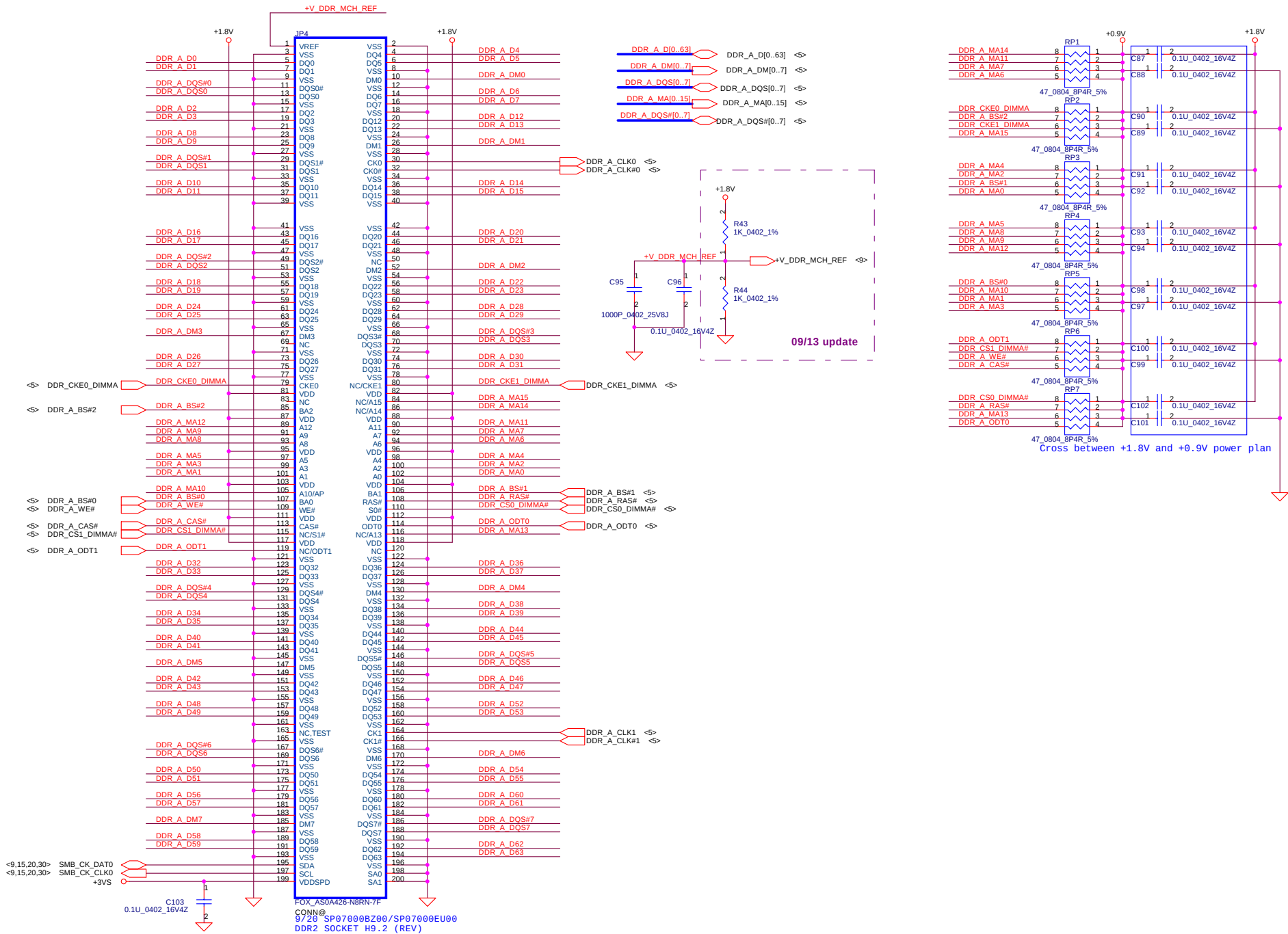
VTT decoupling.

Near Power Supply
 C: Change to NBO CAP
 C59
 220U_Y_4VM

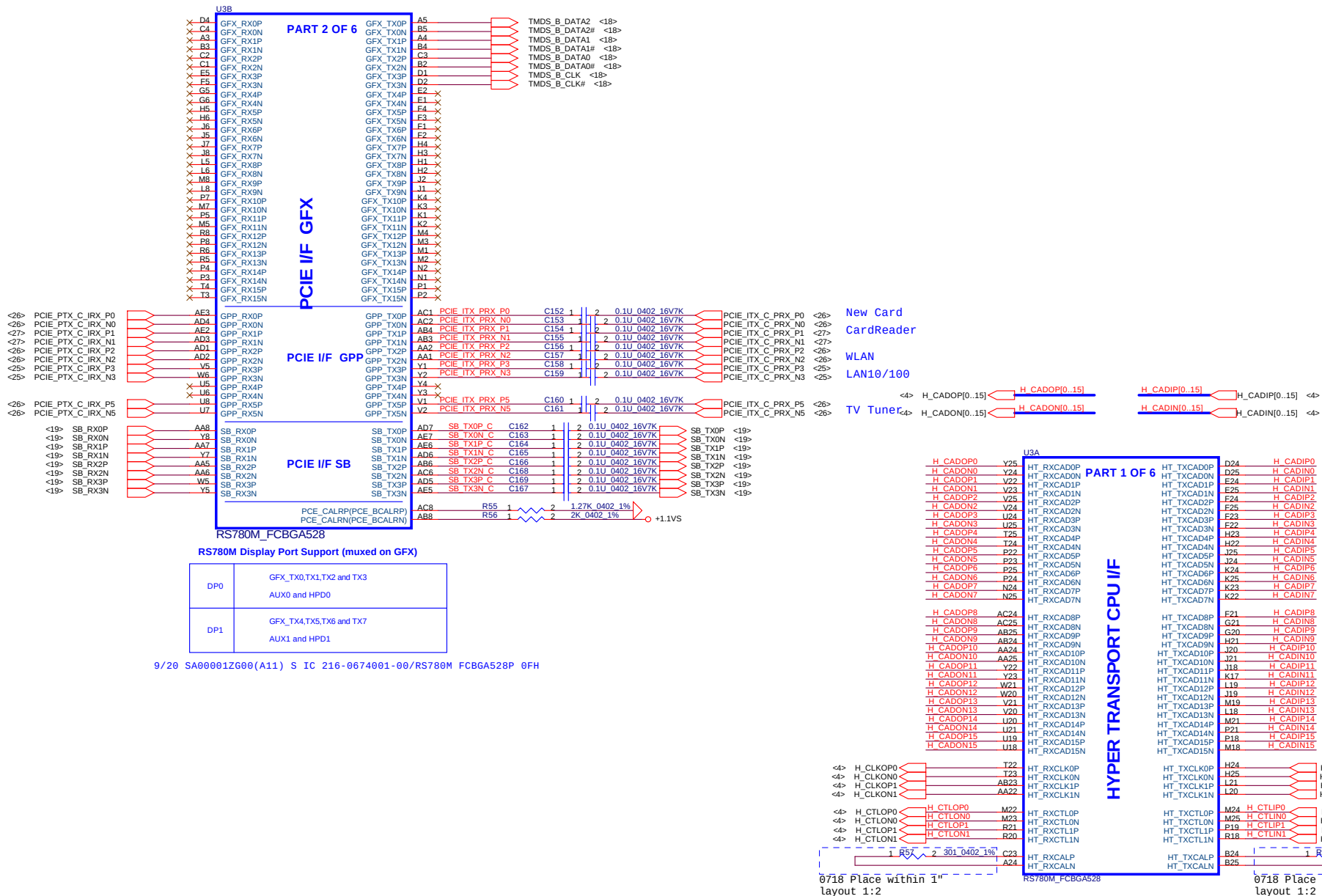
Near CPU Socket Right side.

Near CPU Socket Left side.

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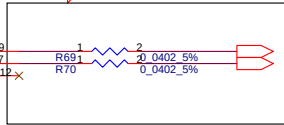


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NEED CHECK R68 & R69 WITH AMD

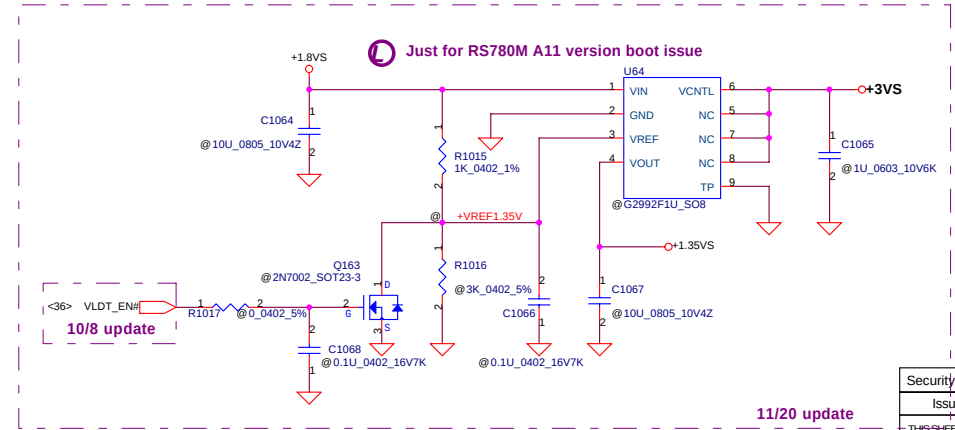
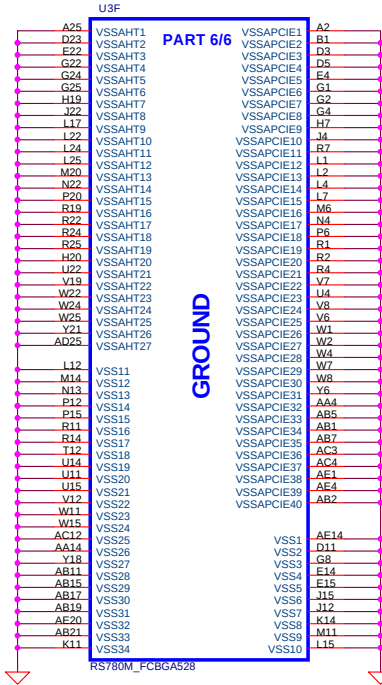
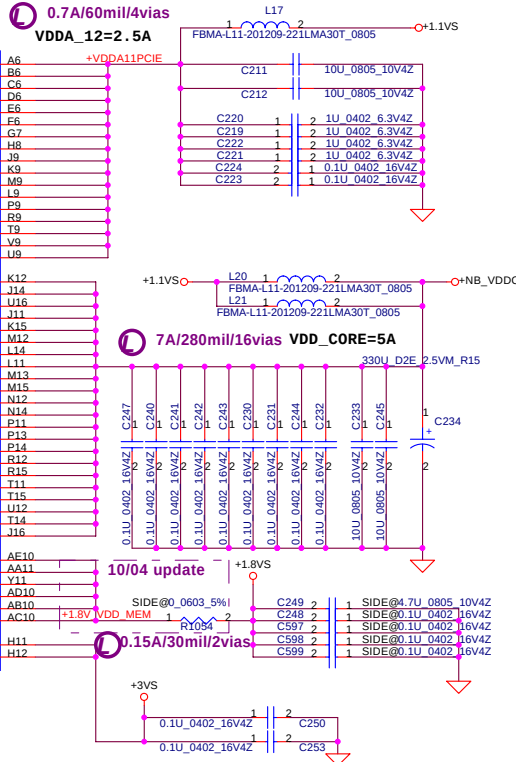
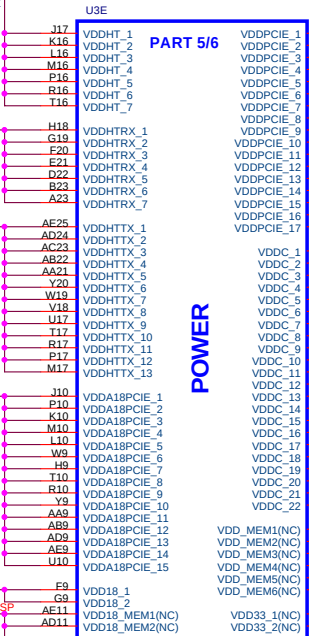
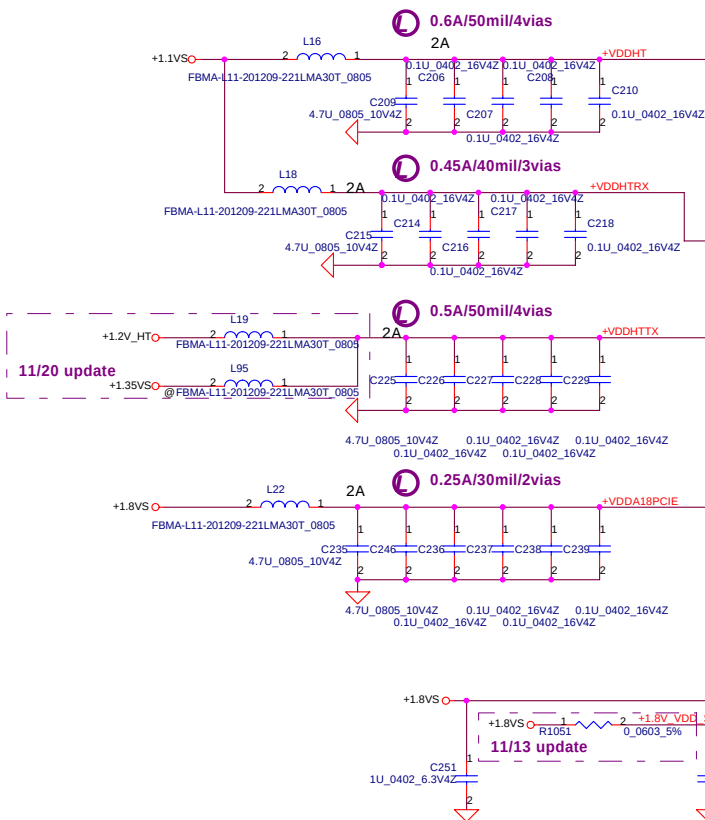
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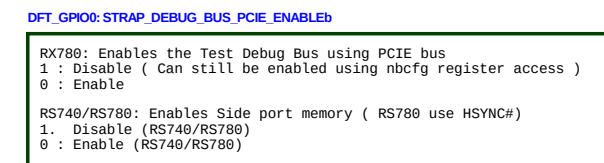
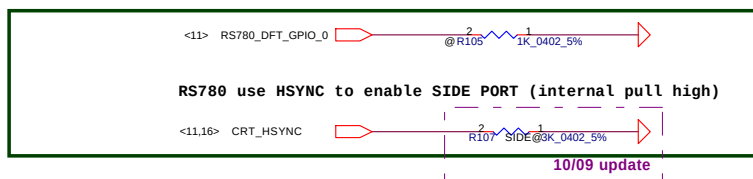
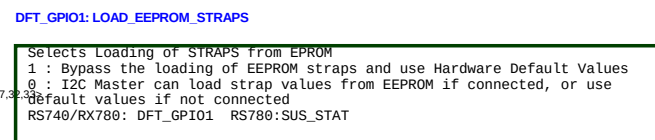
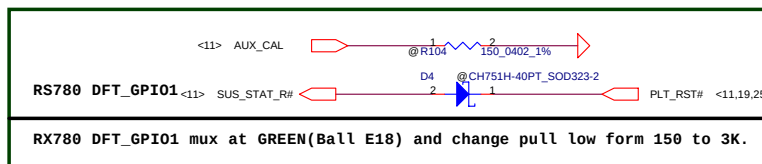
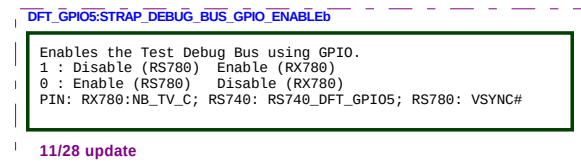
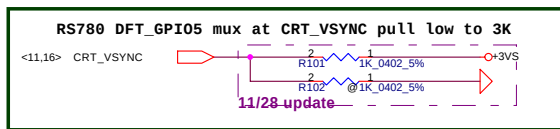
PA_RS780A4
placement close to NB ball

Pin 1: TMSD_HPD(NC) HPD <18>
 Pin 2: SUS_STAT#(Pwm_GPIO5) SUS_STAT_R# <14> **Strap pin**, SUS_STAT# <20>
 Pin 3: THERMALDIODE_P THERMAL DIODE
 Pin 4: THERMALDIODE_N THERMAL DC
 Pin 5: TESTMODE
 Pin 6: D9 1.8K_0402_5%
 Pin 7: D10 1.8K_0402_5%
 Pin 8: PAD T49
 Pin 9: PAD T50 **NB temp to SB**
 Pin 10: D13 1.8K_0402_5%

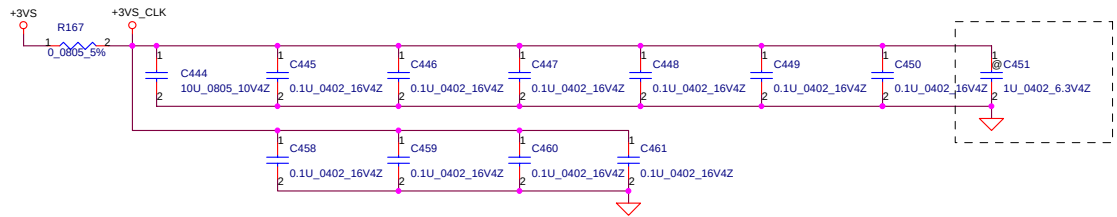
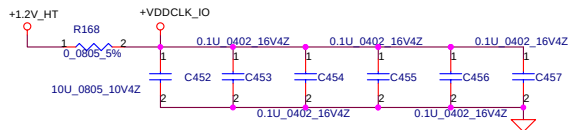
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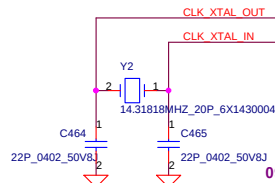
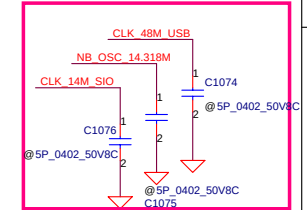
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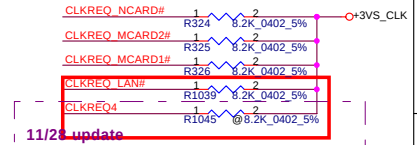
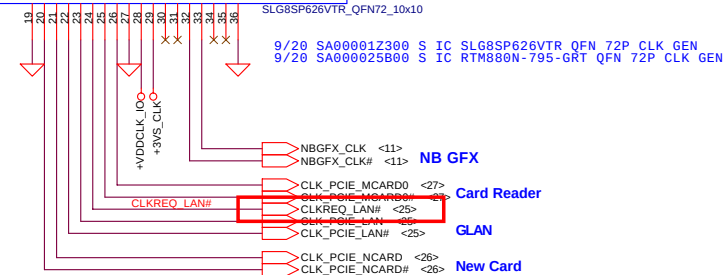
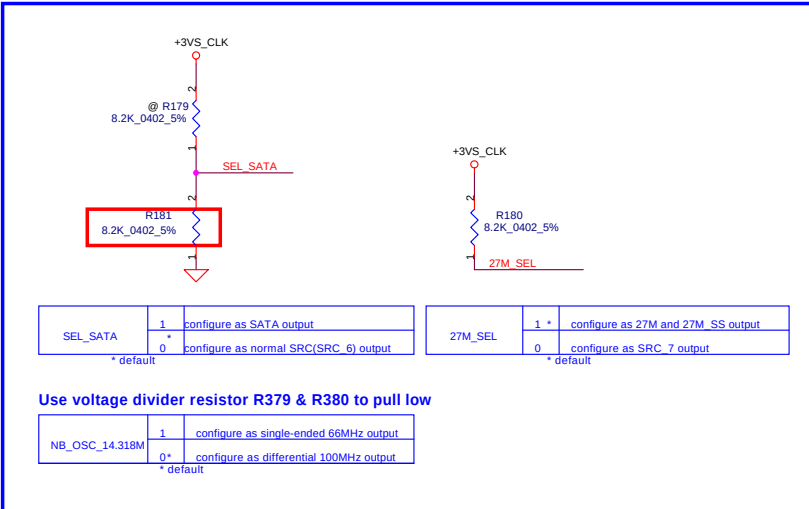
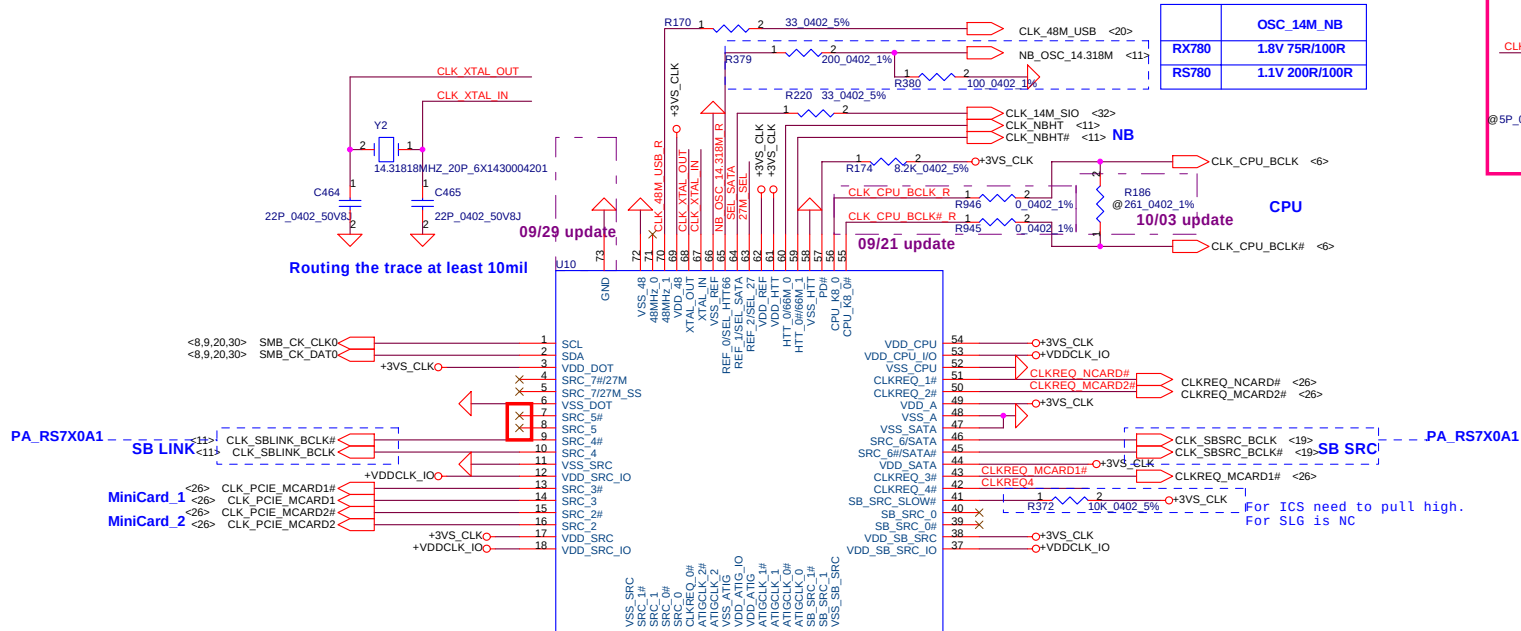
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EMI Caps for single end clock.



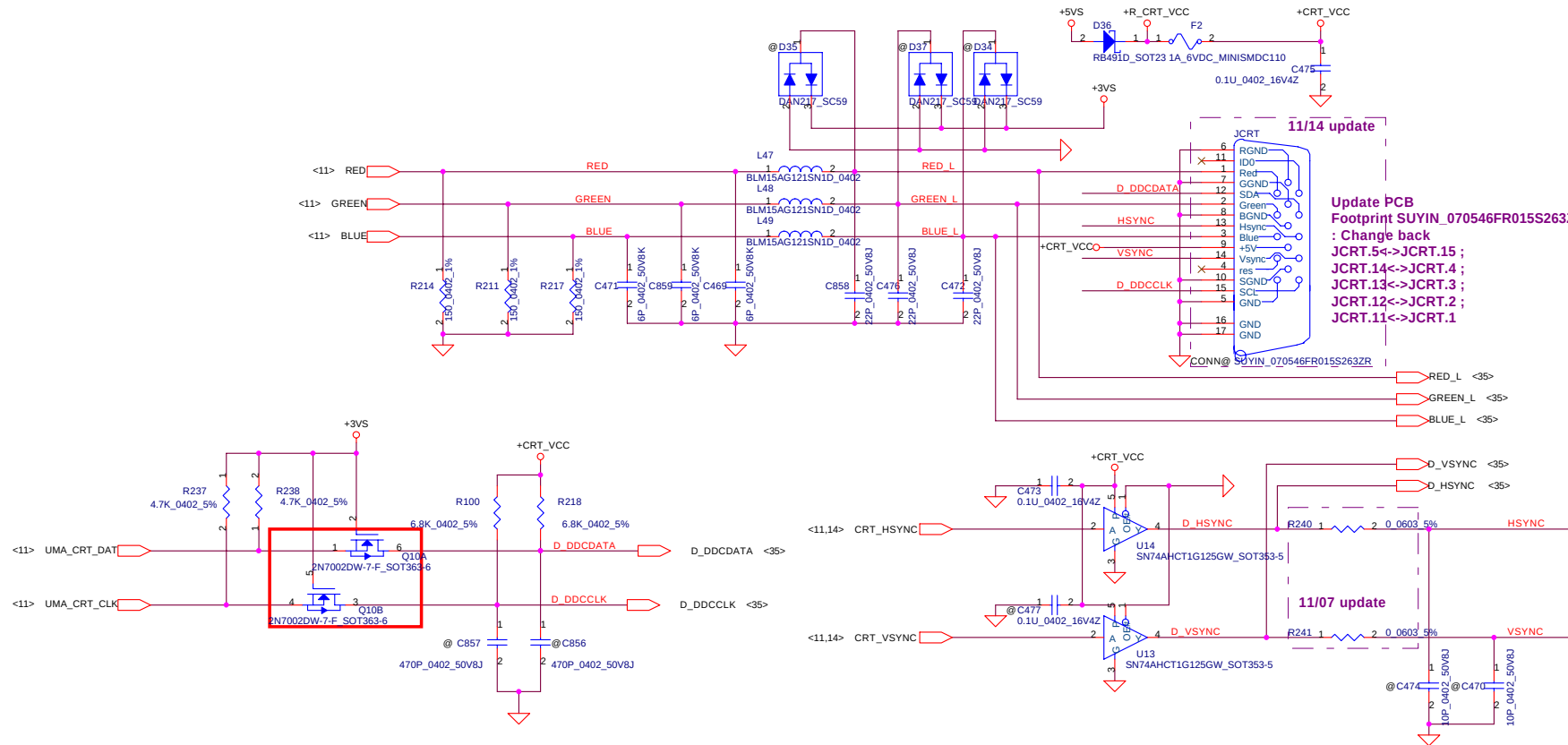
Routing the trace at least 10mil



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFLCKP	100M DIFF	100M DIFF
HT_REFLCKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFLCK	100M DIFF	100M DIFF(IN/OUT)

CRT CONNECTOR



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WebCam+Digital Mic Reserve

Close to JP7

+USB_CAM0

2 @ C1072

10U_0805_10V4Z

1

USB20P5

USB20N5

DMICCLK

DMICDAT

JP7

11/13 update

1 2 3 4 5 6

G1

G2

7 8

ACES_B8231-06001

CONN@

Place R1027-R1030 close to J1VDS

R1027 @0.0402 5%

USB20 P5_1 2 USB20P5

USB20 N5_1 2 USB20N5

R1028 @0.0402 5%

D52

VIN IO1

2 USB20P5

IO2 GND

1

+USB_CAM0

USB20N5

09/26 update

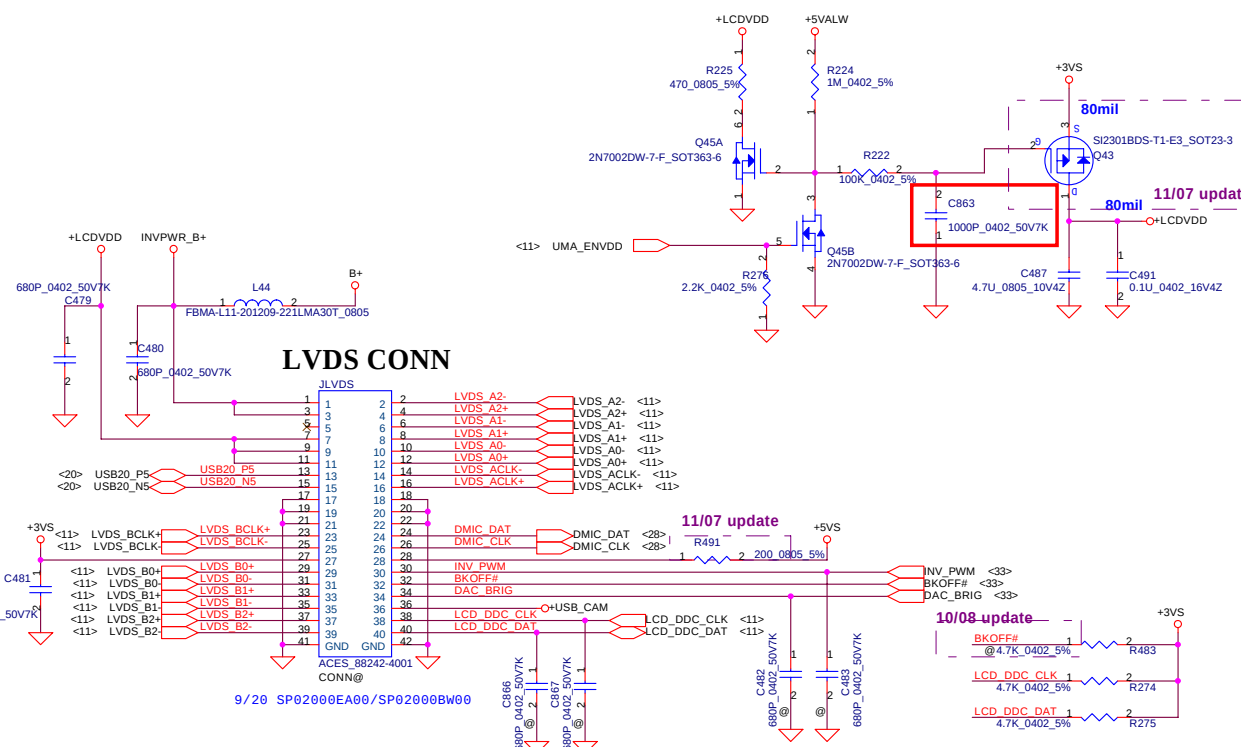
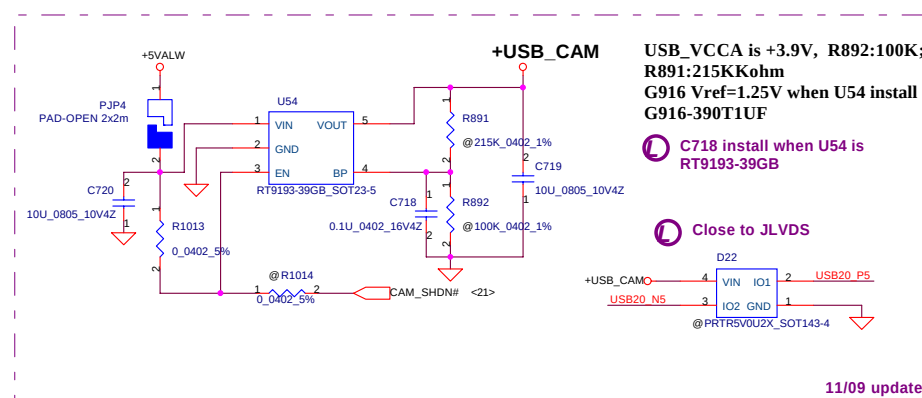
@PRTSR5V0U2X_SOT143-4

R1029 @0.0402 5%

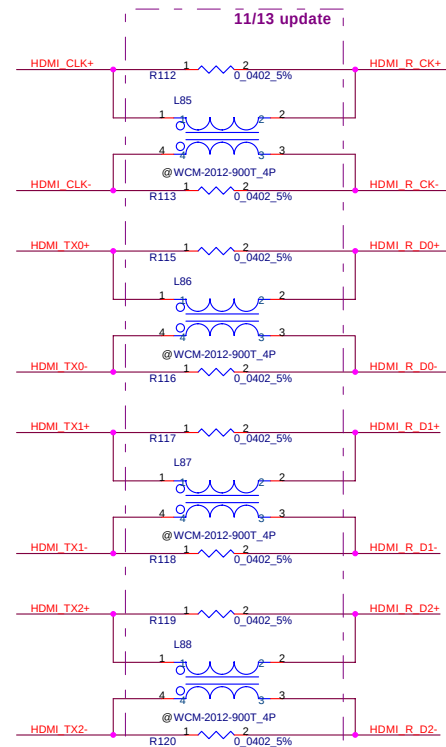
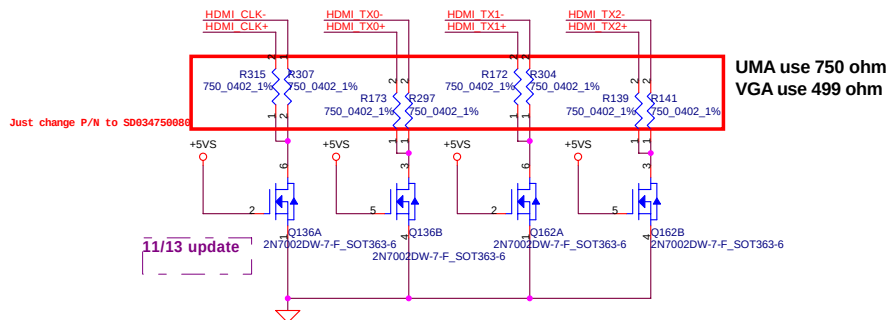
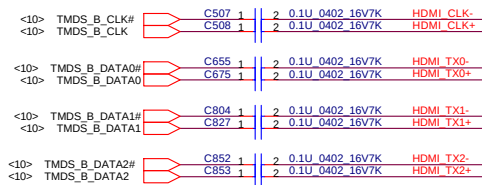
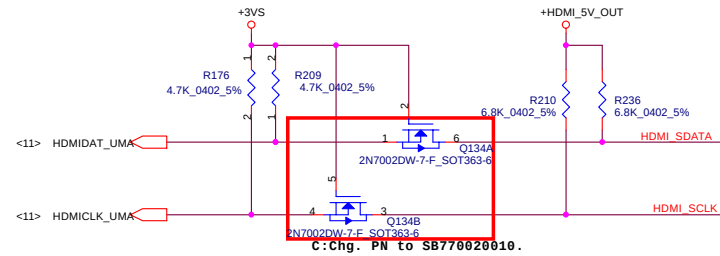
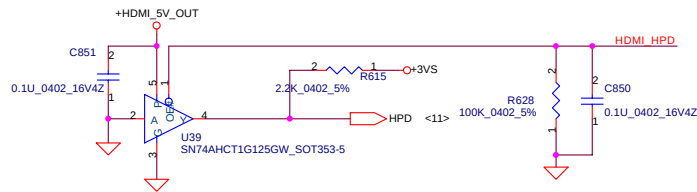
DMIC DAT1 2 DMICDAT

DMIC CLK_1 2 DMICCLK

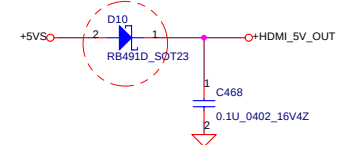
R1030 @0.0402 5%



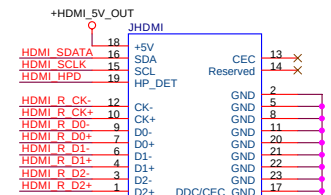
Security Classification		Compal Secret Data		Compal Electronics, Inc. LCD CONN. / WebCam	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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				Custor	0.2
				LA-4111P	
Date:	Friday, November 30, 2007	Sheet	of 48		



MP:Update D10 to meet HDMI.



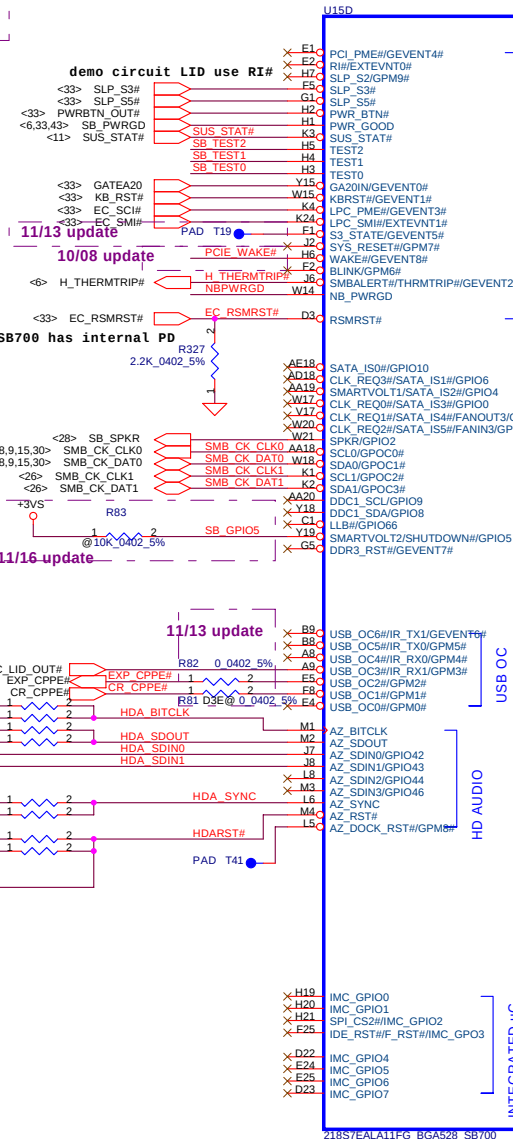
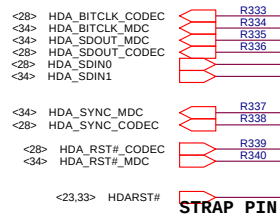
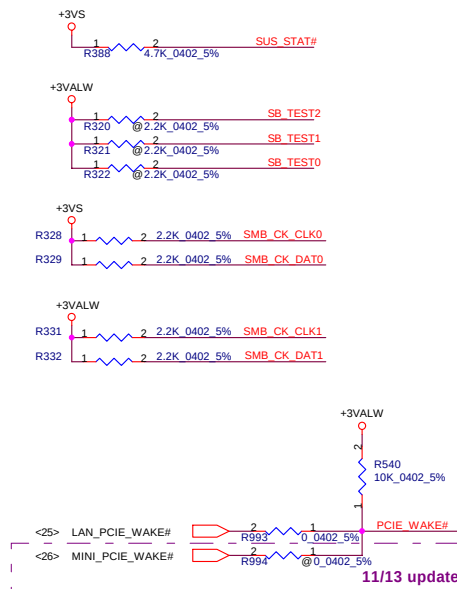
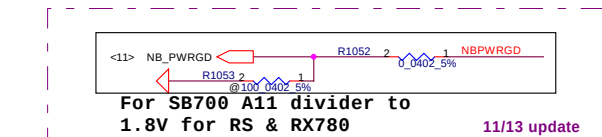
HDMI Connector



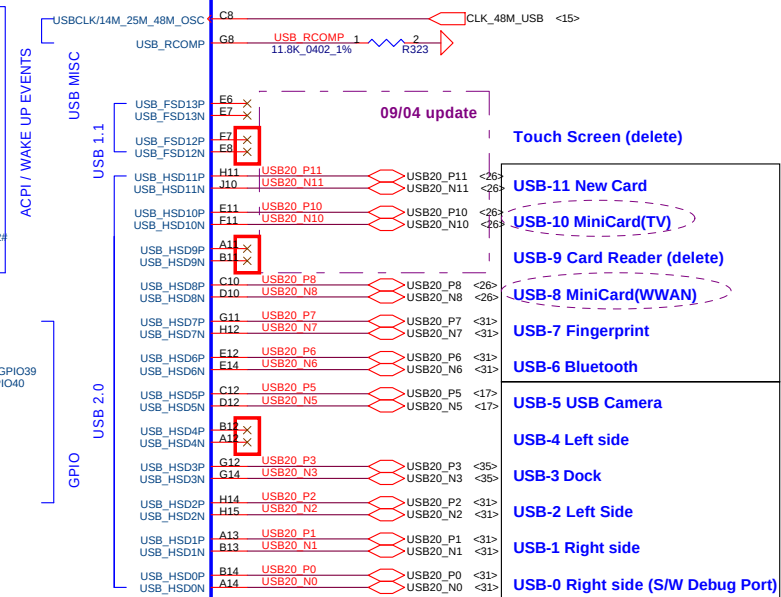
11/14 update

Change PCB Footprint from SW_WCM2012F25_4P to KING_WCM-2012-900T_4P

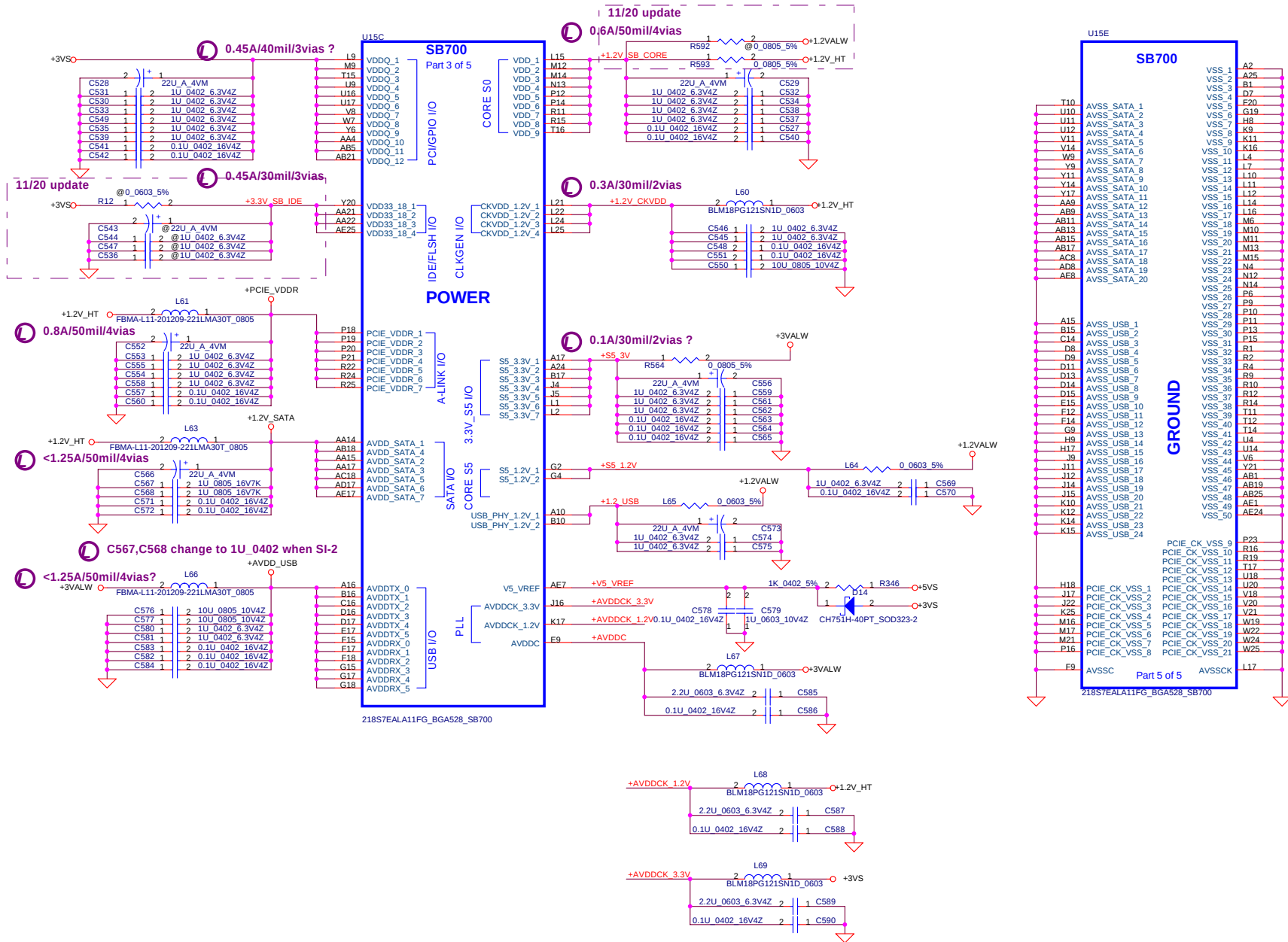
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Issued Date				2007/08/02				Deciphered Date			
2007/08/02				2008/08/02				Friday, November 30, 2007			
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				0.2				Sheet			
				18				of			
				48							



SB700 Part 4 of 5



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Issued Date	2007/08/02	Deciphered Date	2008/08/02	SB700 USB/AC97	
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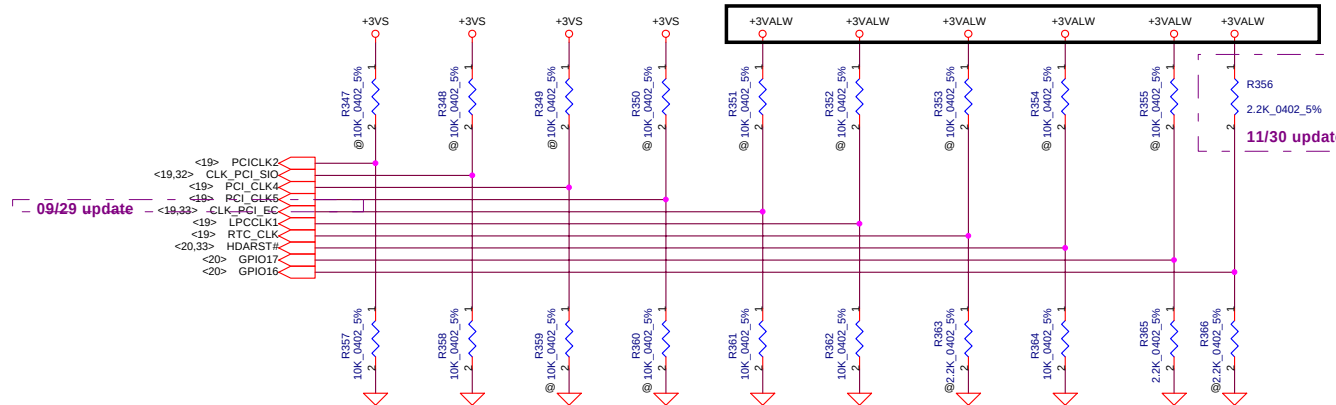


Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	SB700 PWR/GND	
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				Custom	0.2
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

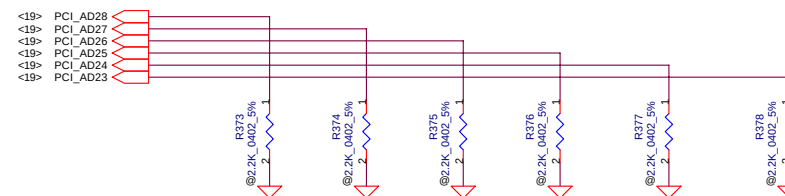
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED		Internal pull up H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



DEBUG STRAPS

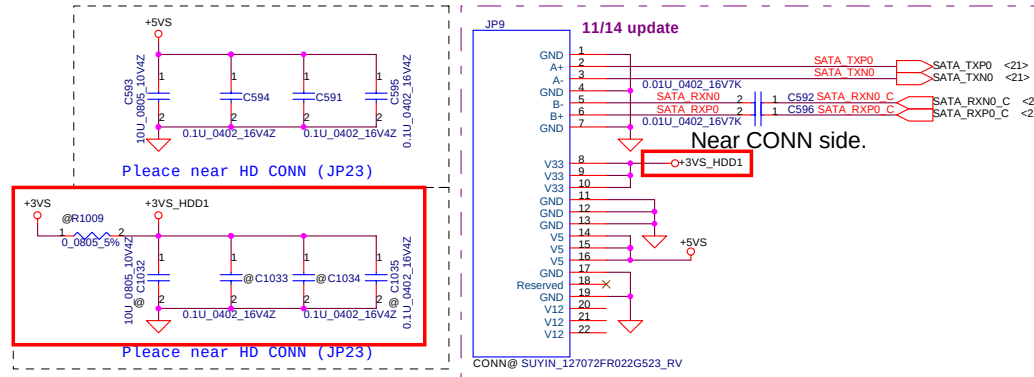
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

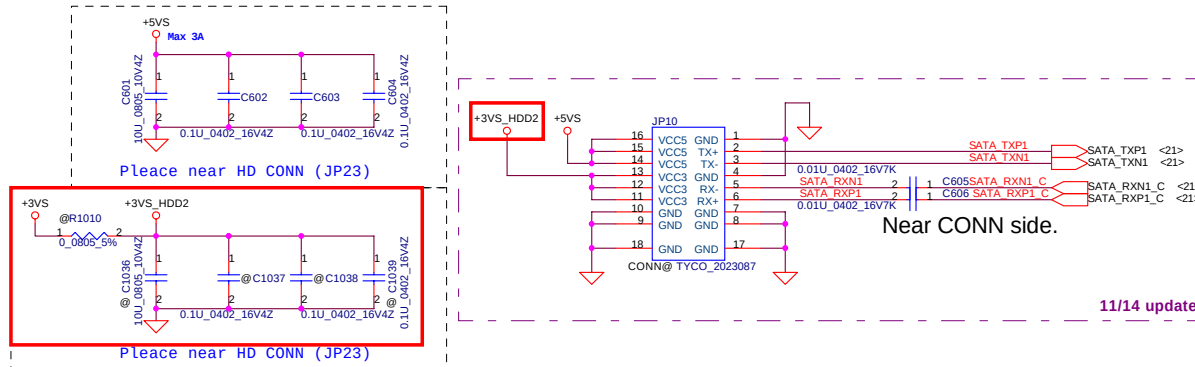


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				SB700 STRAPS		
				Size	Document Number	Rev
Custom	LA-4111P	0.2				
Date:	Friday, November 30, 2007		Sheet	of 48		

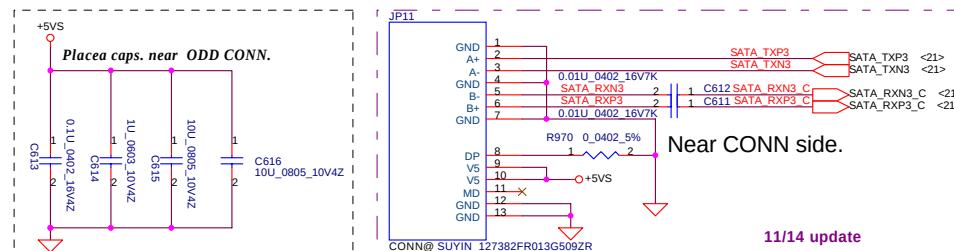
HDD Connector



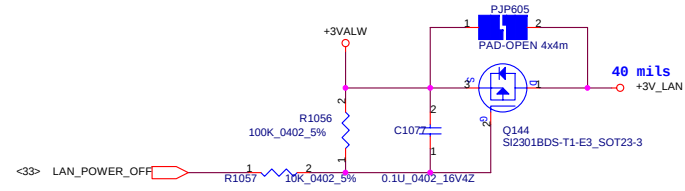
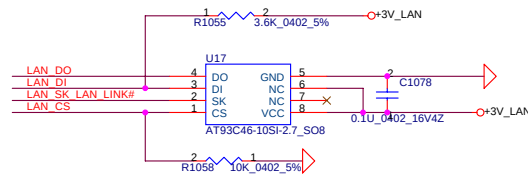
Multi-Bay Connector-option



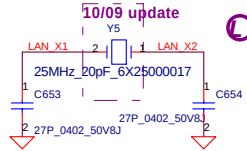
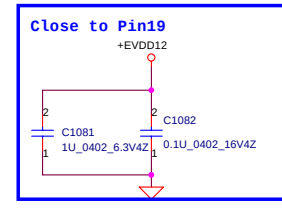
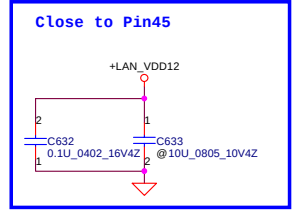
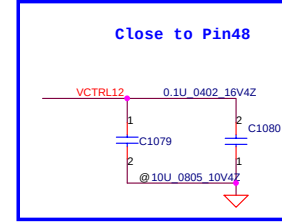
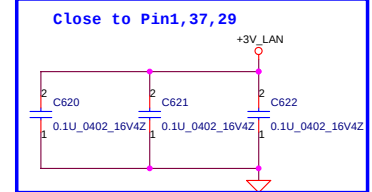
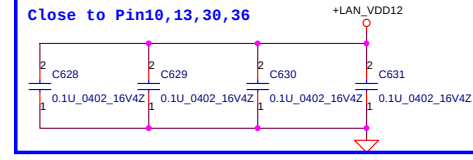
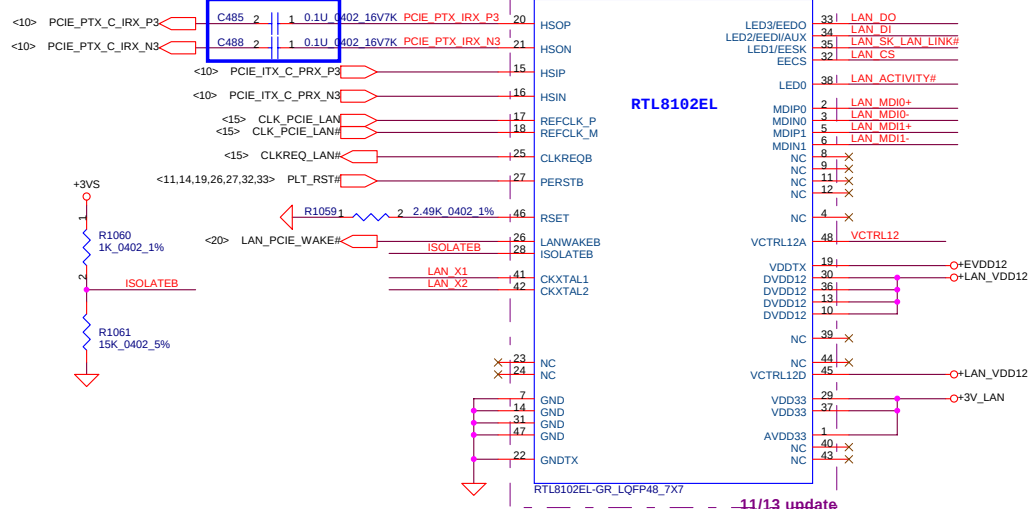
CD-ROM Connector



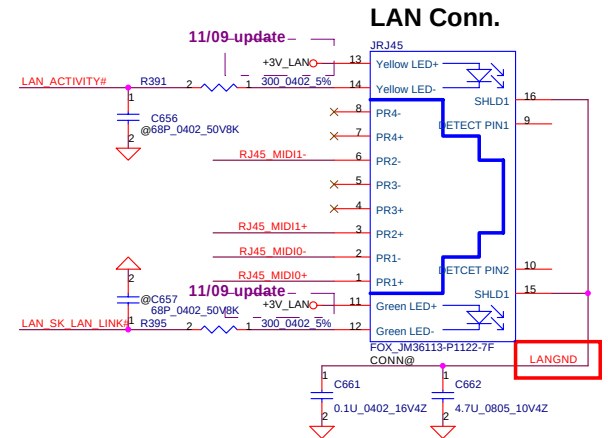
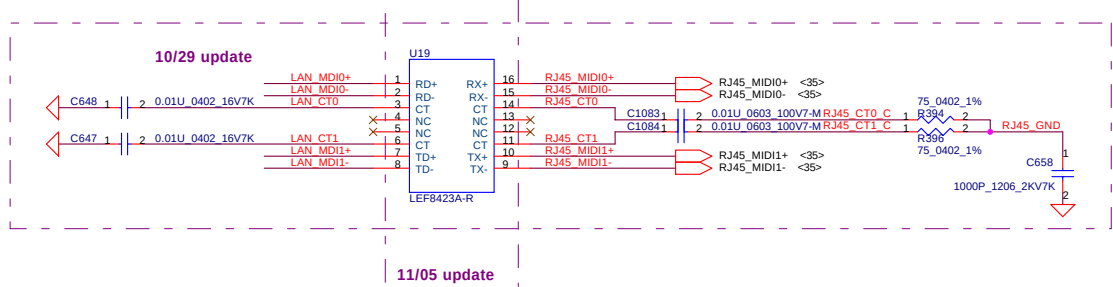
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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Place Close to Chip



Change the PCB Footprint from Y_KDS_1BX25000CK1A_2P to Y_6X25000017_2P

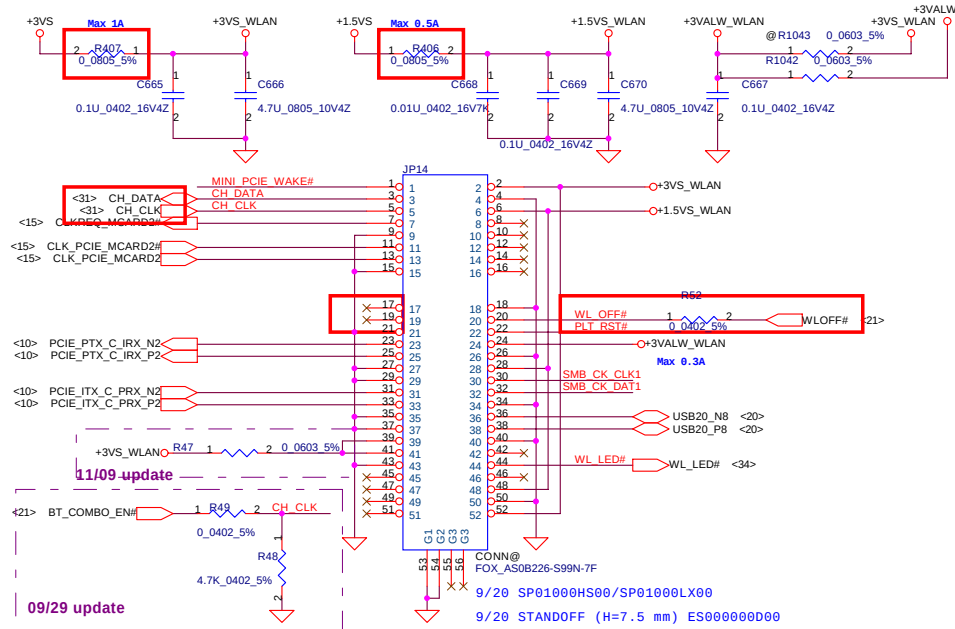


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				Date	Friday, November 30, 2007
				Sheet	of 48

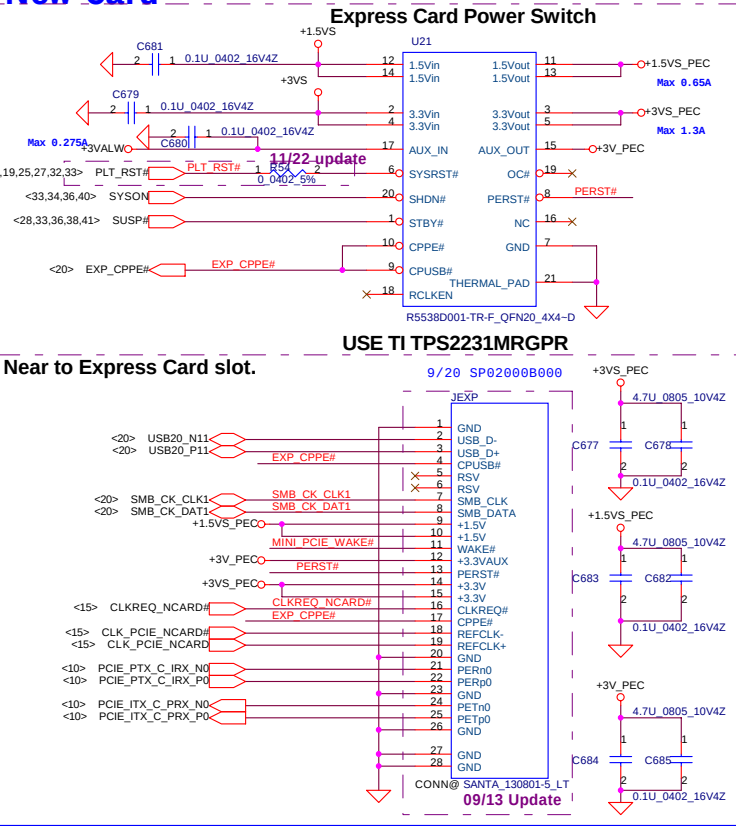
Compal Electronics, Inc.
RTL8111C/8102E 10/100/1000 LAN

9/20 DC234001G00

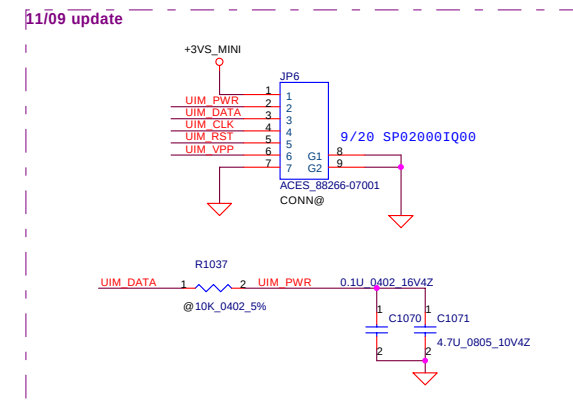
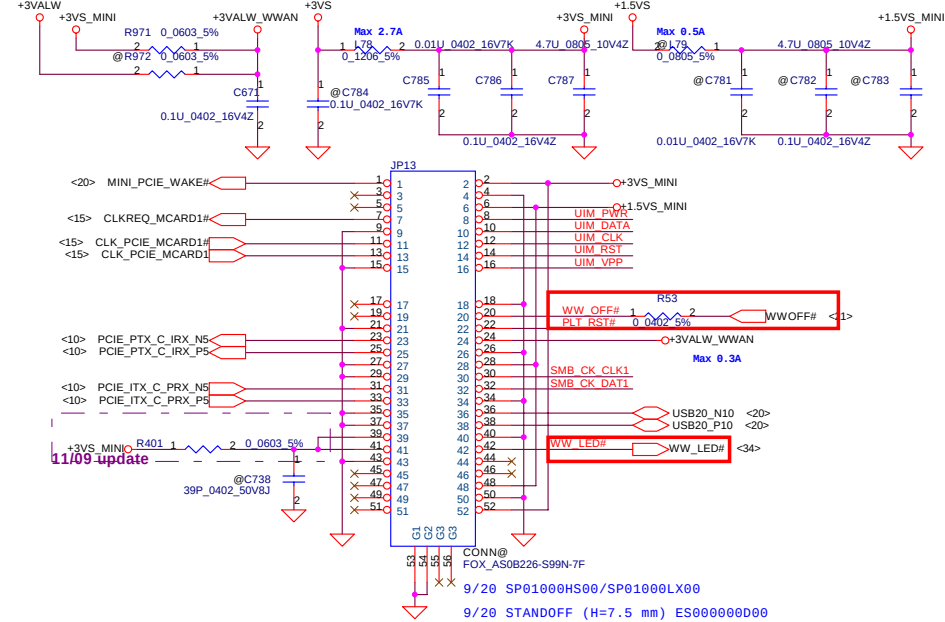
Mini Card Slot 1---WLAN



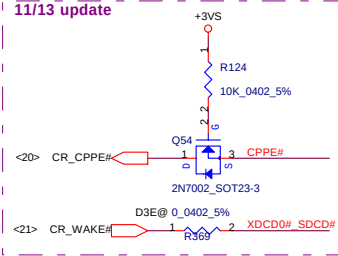
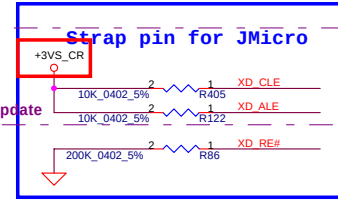
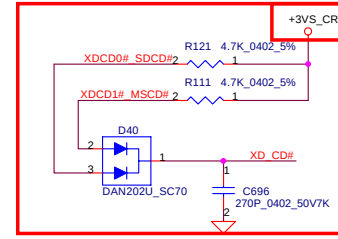
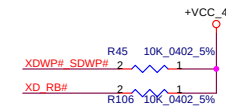
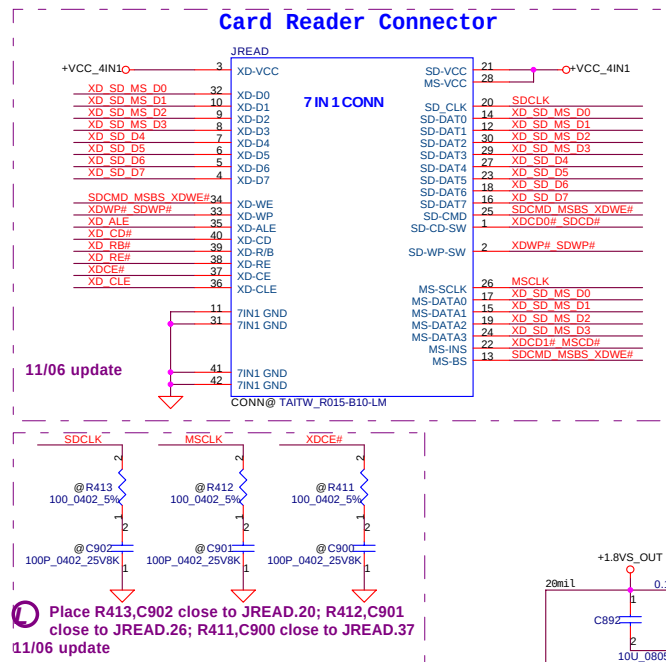
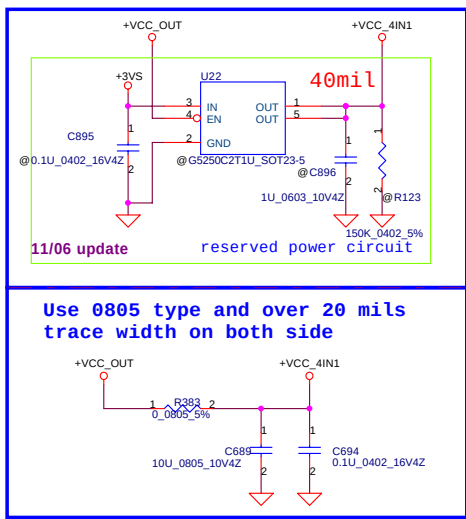
New Card



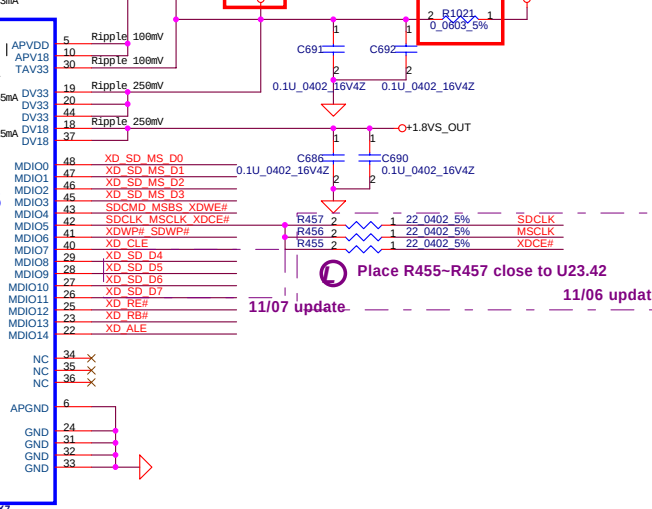
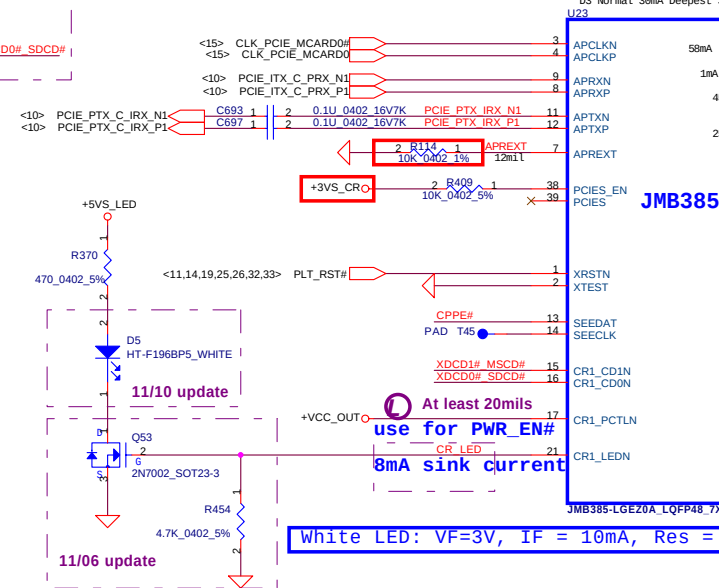
Mini Card Slot 2---TV tuner / WWAN / Robson



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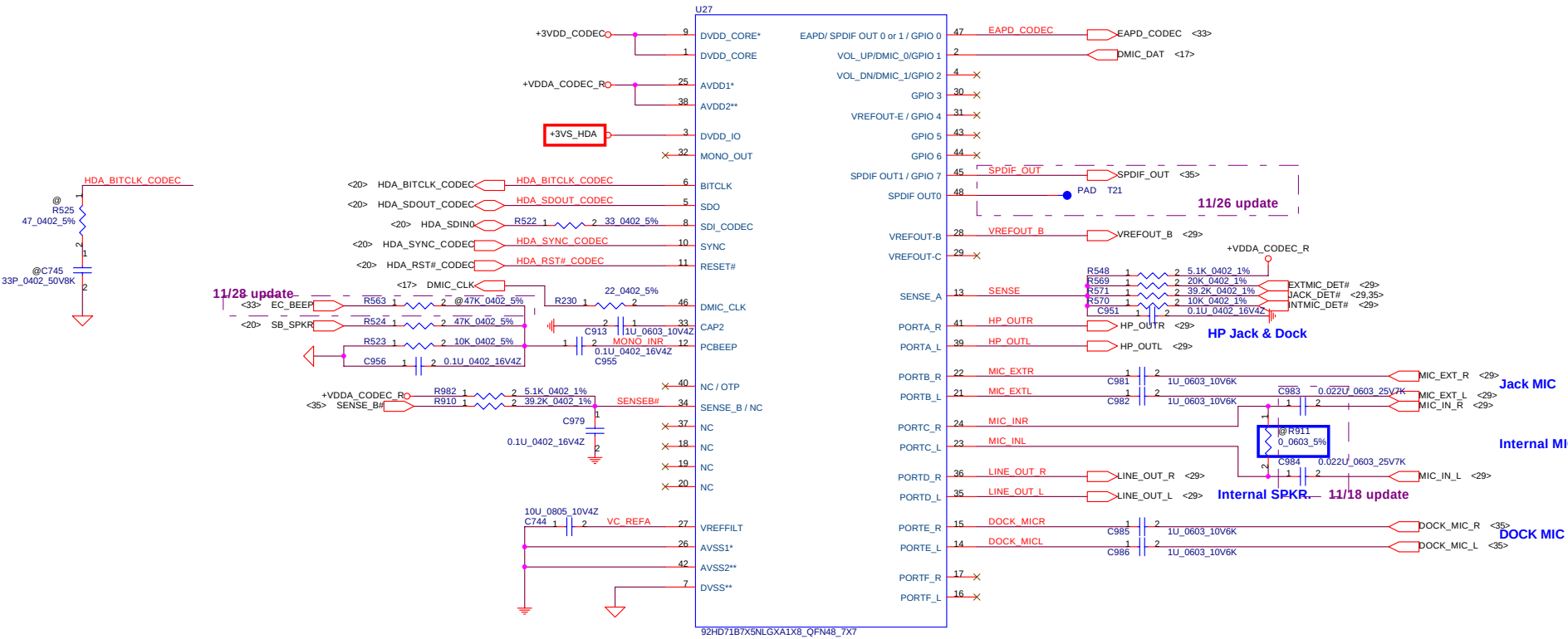
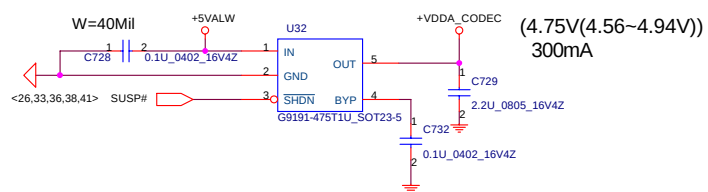
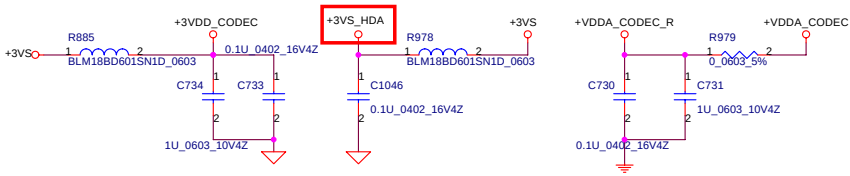
Power Circuit



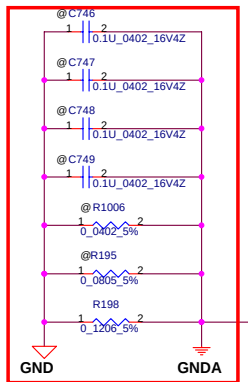
White LED: VF=3V, IF = 10mA, Res = 200 ohm

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				Custom	LA-4111P
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CODEC POWER

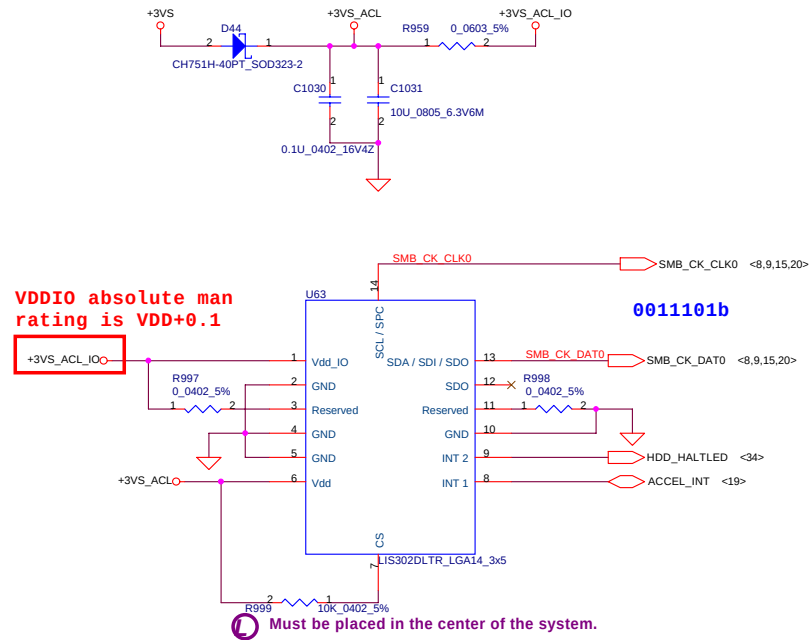


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

ACCELEROMETER



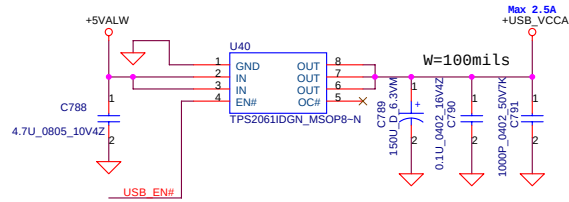
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Accelerometer	
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				Date: Friday, November 30, 2007	Sheet 30 of 48

Compal Electronics, Inc.

Accelerometer

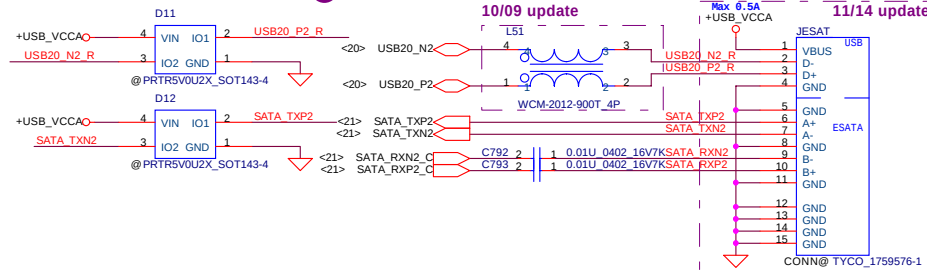
LA-4111P

Left side USB CONNECTOR

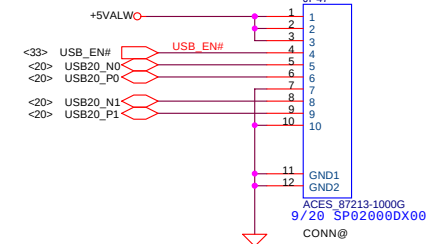


Left side ESATA5/USB2 combination Connector

Change PCB Footprint from SW_WCM2012F2S_4P to KING_WCM-2012-900T_4P

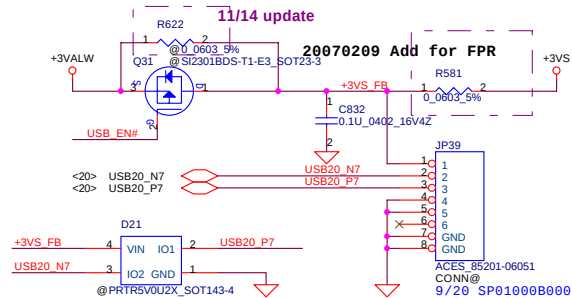


Right side USB 0&1 Board Conn

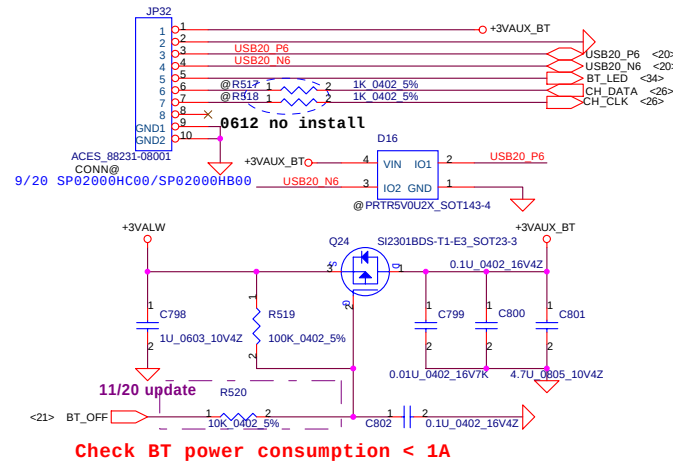


Update Symbol TYCO_1759576-1_11P-T

Finger printer

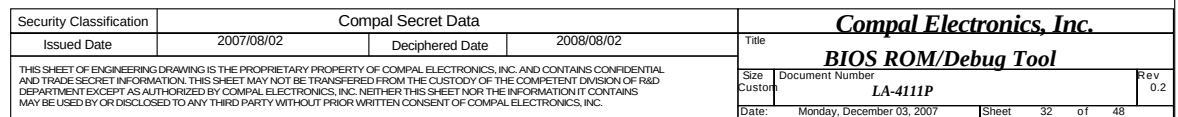
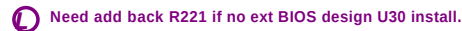


BT Connector

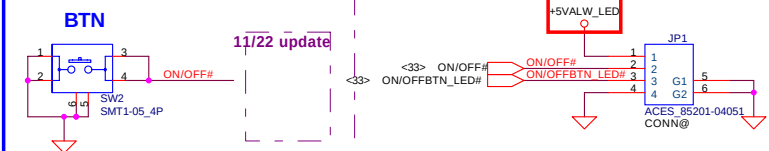


Check BT power consumption < 1A

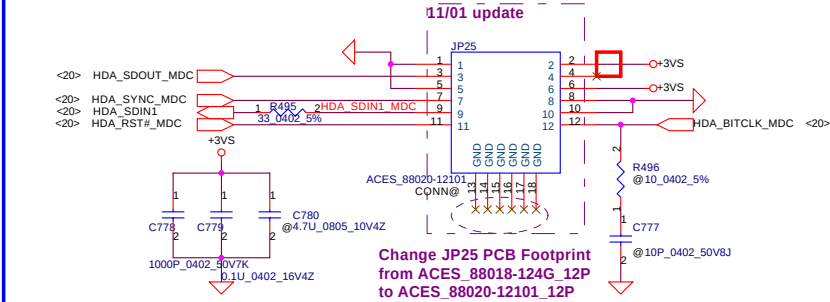
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				Sheet	of 48
				Rev	0.2



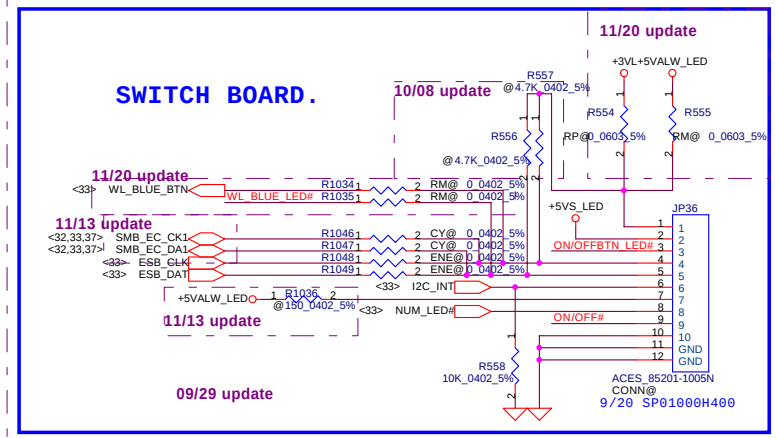
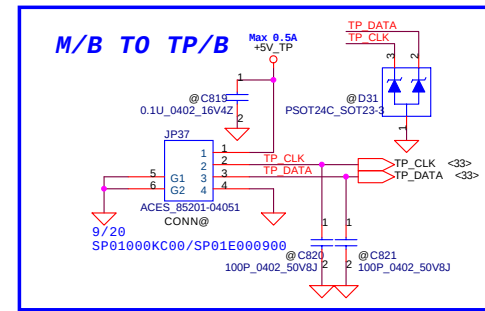
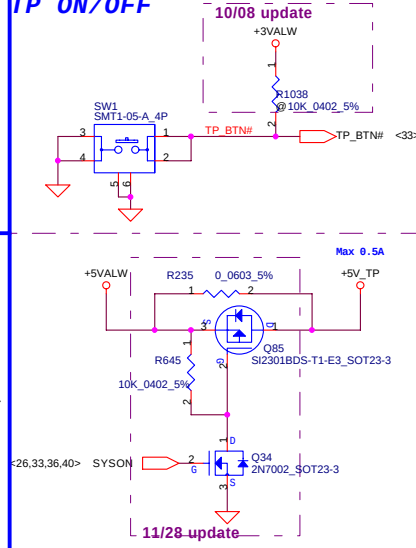
for debug only ON/OFF Button Connector



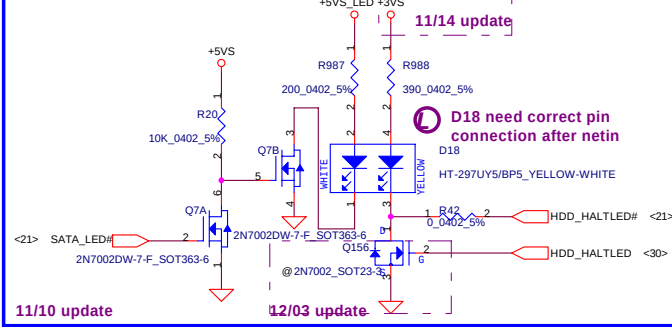
MDC 1.5 Conn.



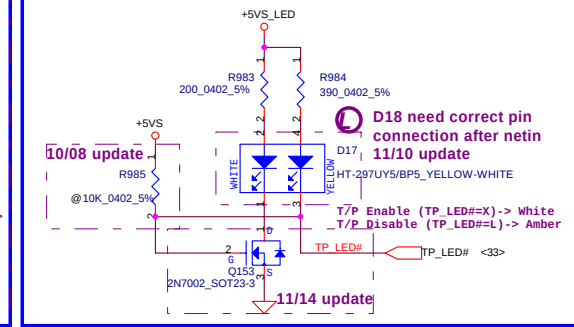
TP ON/OFF



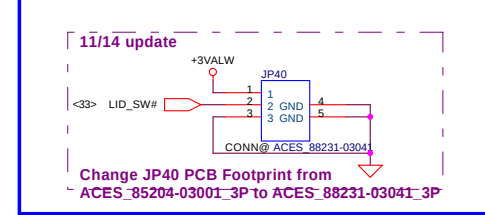
HDD/G-Sensor LED



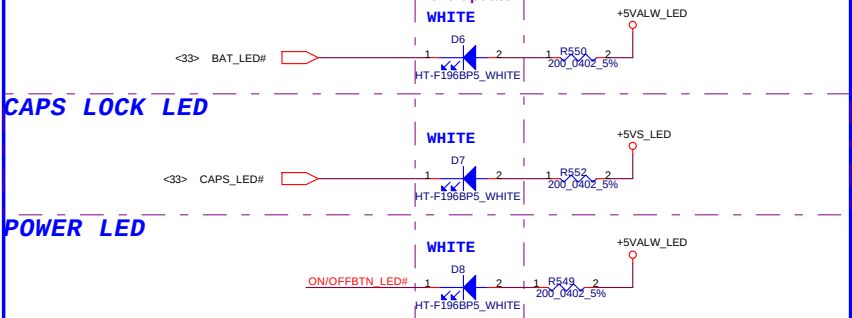
TouchPAD ON/OFF LED



Reed switch BOARD.

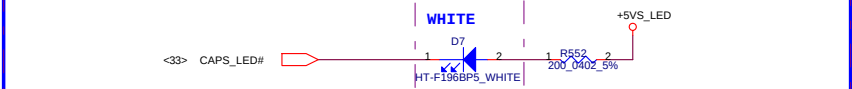


Battery Charge LED

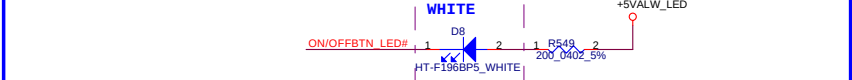


White LED: VF=3V, IF = 10mA, Res = 200 ohm
Amber LED: VF=1.8V, IF = 8mA, Res = 390 ohm

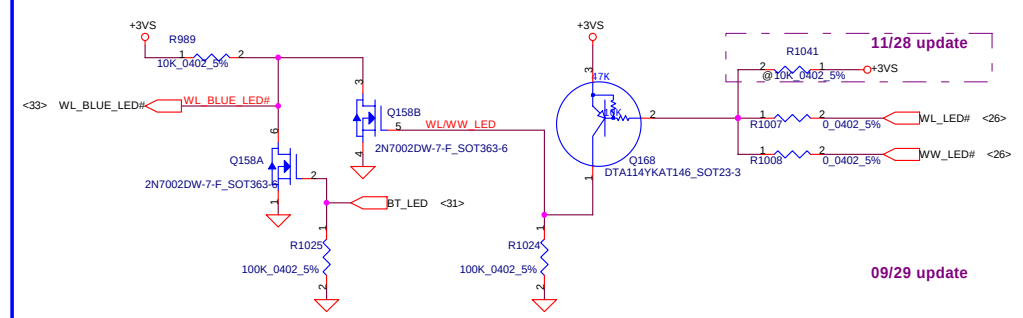
CAPS LOCK LED



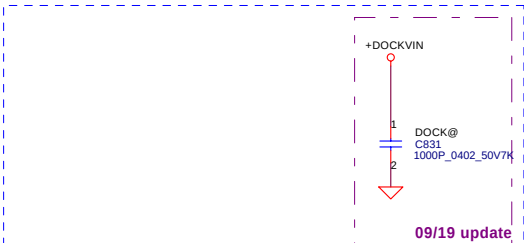
POWER LED



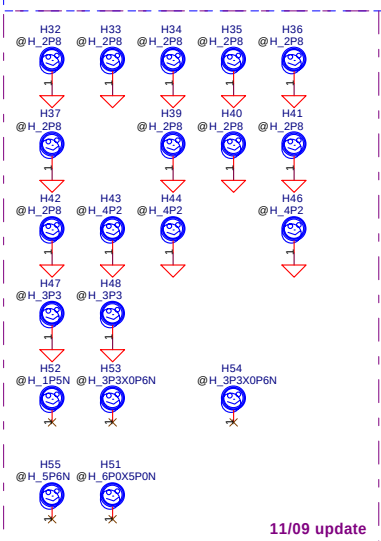
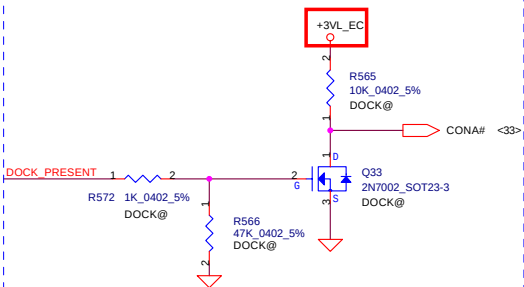
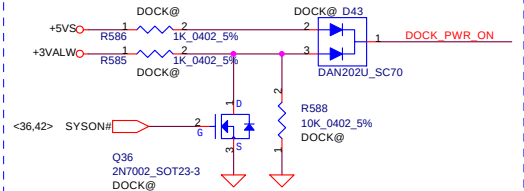
WLAN and BT LED inform pin to KBC



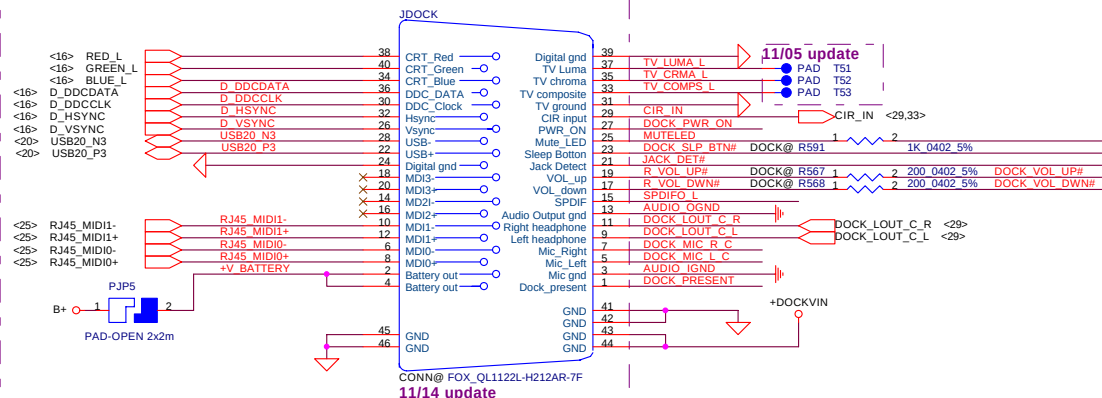
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	TP,MDC,ON/OFF,S/W,LED,Reed	
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				Date: Monday, December 03, 2007	Sheet 34 of 48



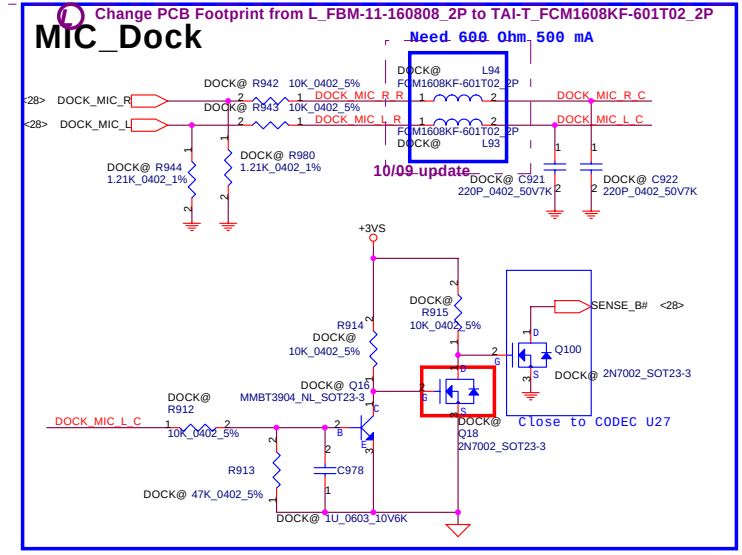
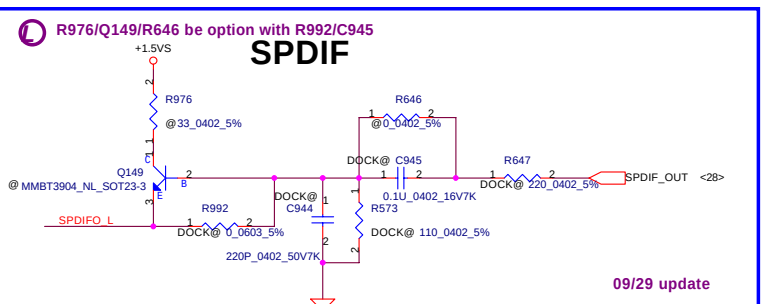
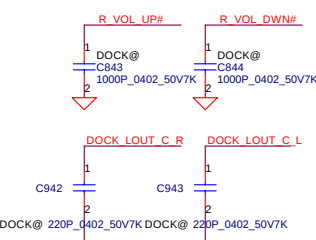
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



Atlas/ Saturn Dock

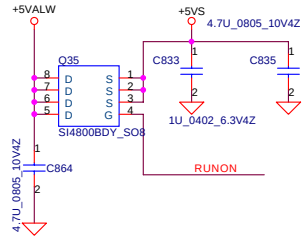


Update symbol finish and swap back
JDOCK Pin38/40, 34/36, 30/32, 26/28,
22/24, 10/12, 6/8 Add pin 45/46 to GND

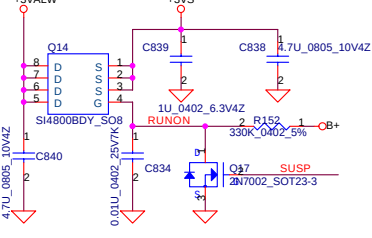


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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Size	Custom	Document Number	LA-4111P	Rev	0.2
Date:	Friday, November 30, 2007	Sheet	of 48	Rev	

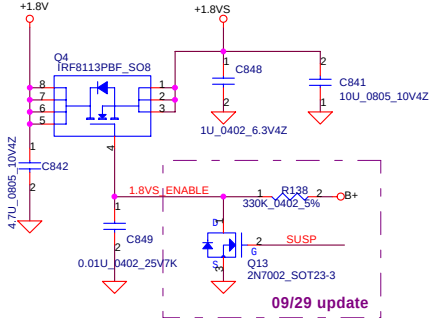
+5VALW TO +5VS



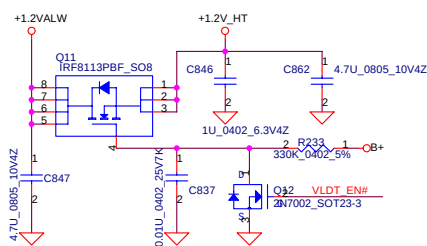
+3VALW TO +3VS



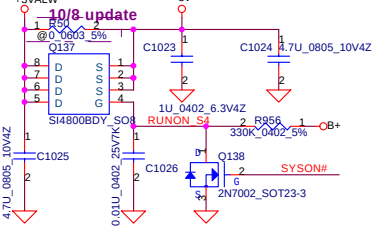
+1.8V TO +1.8VS



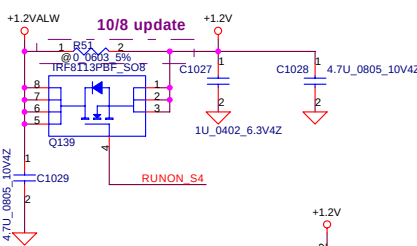
+1.2VALW TO +1.2V_HT



+3VALW TO +3V

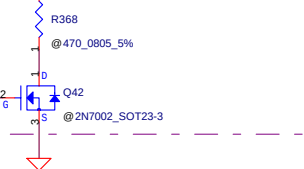


+1.2VALW TO +1.2V



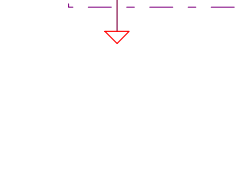
08/23 new add
Reserve until SI-1 stage after SB
USB PHY power saving report

+1.2VALW TO +1.2V

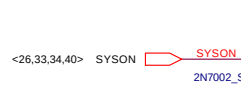


09/29 update (Wait EC Code fix)

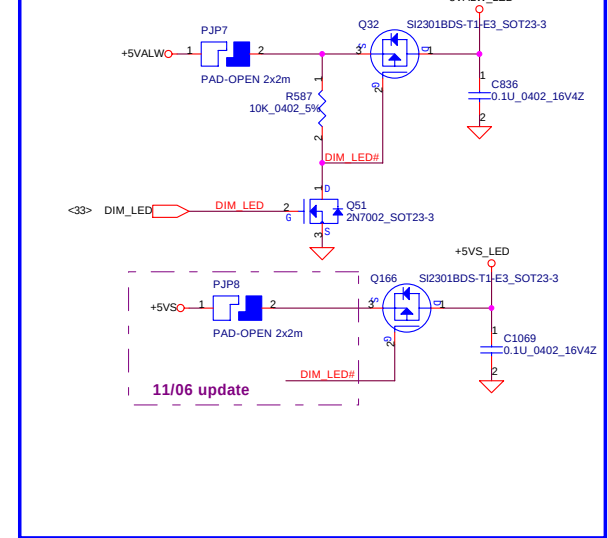
+1.2VALW TO +1.2V



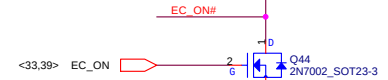
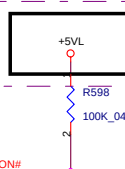
09/13 update



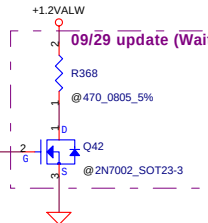
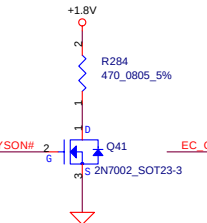
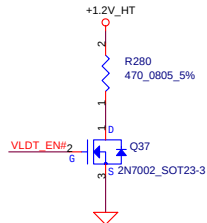
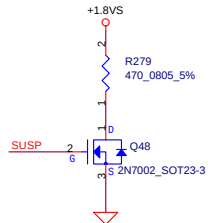
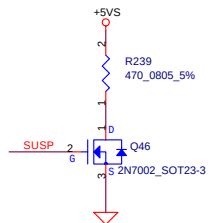
DIM LED



+5VALW_LED TO +5VS_LED



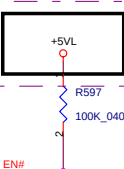
Discharge circuit



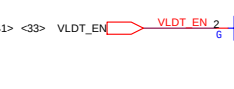
09/13 update (Del +V_DDR_MCH_REFF)

Change to +3VL(same as EC)
to avoid leakage

+5VALW_LED TO +5VS_LED

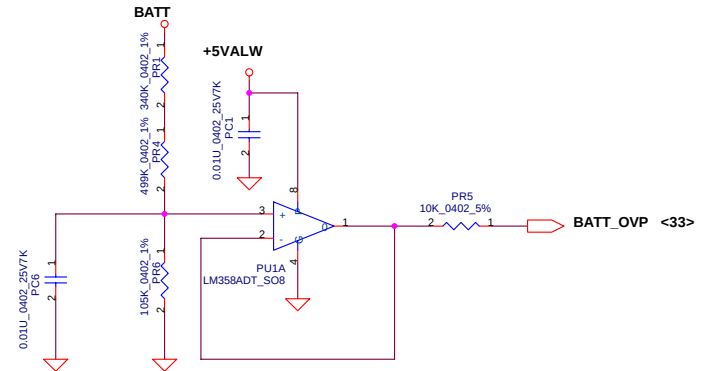
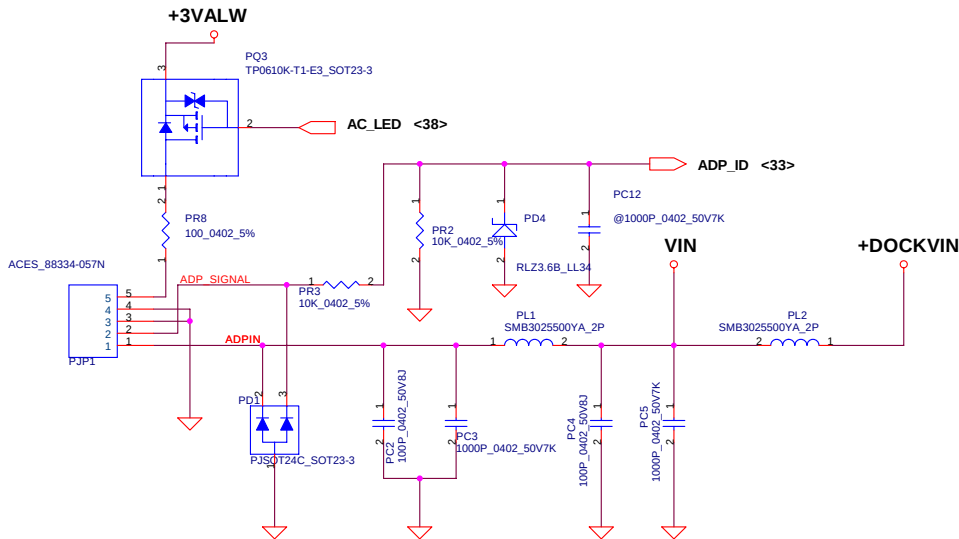


09/13 update

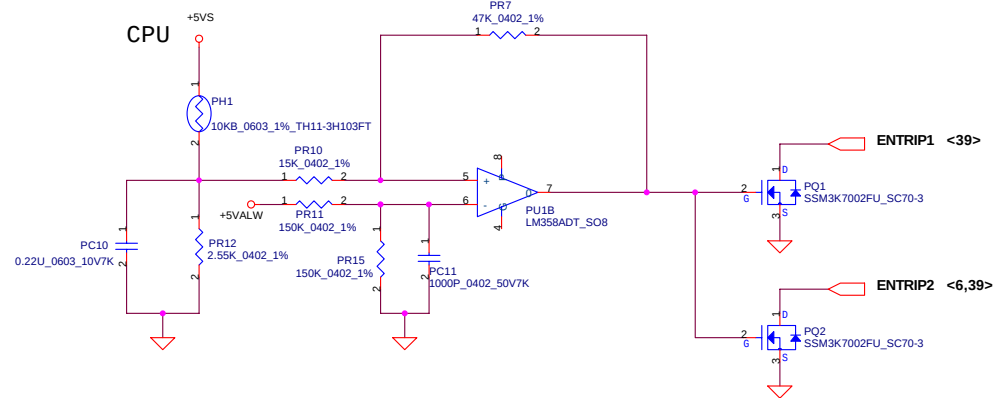
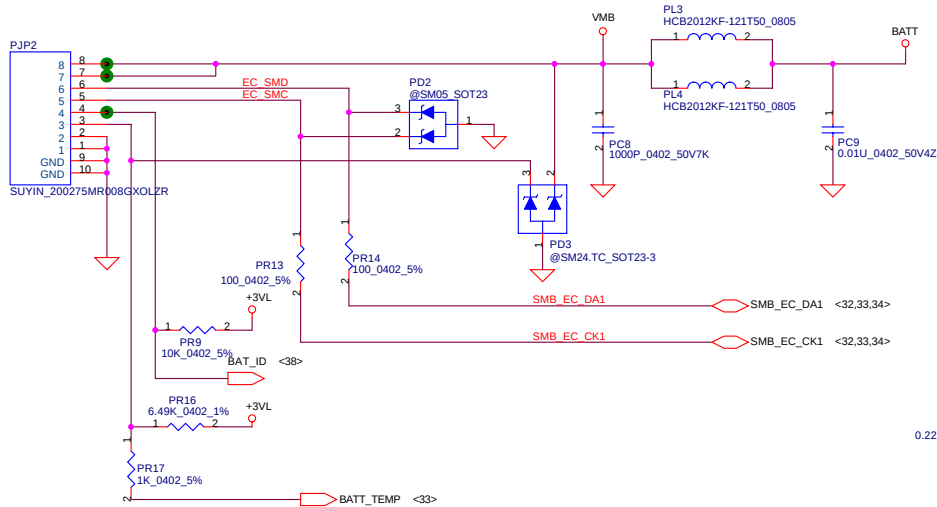


Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				DC/DC Circuits			
2007/08/02				2008/08/02				LA-4111P			
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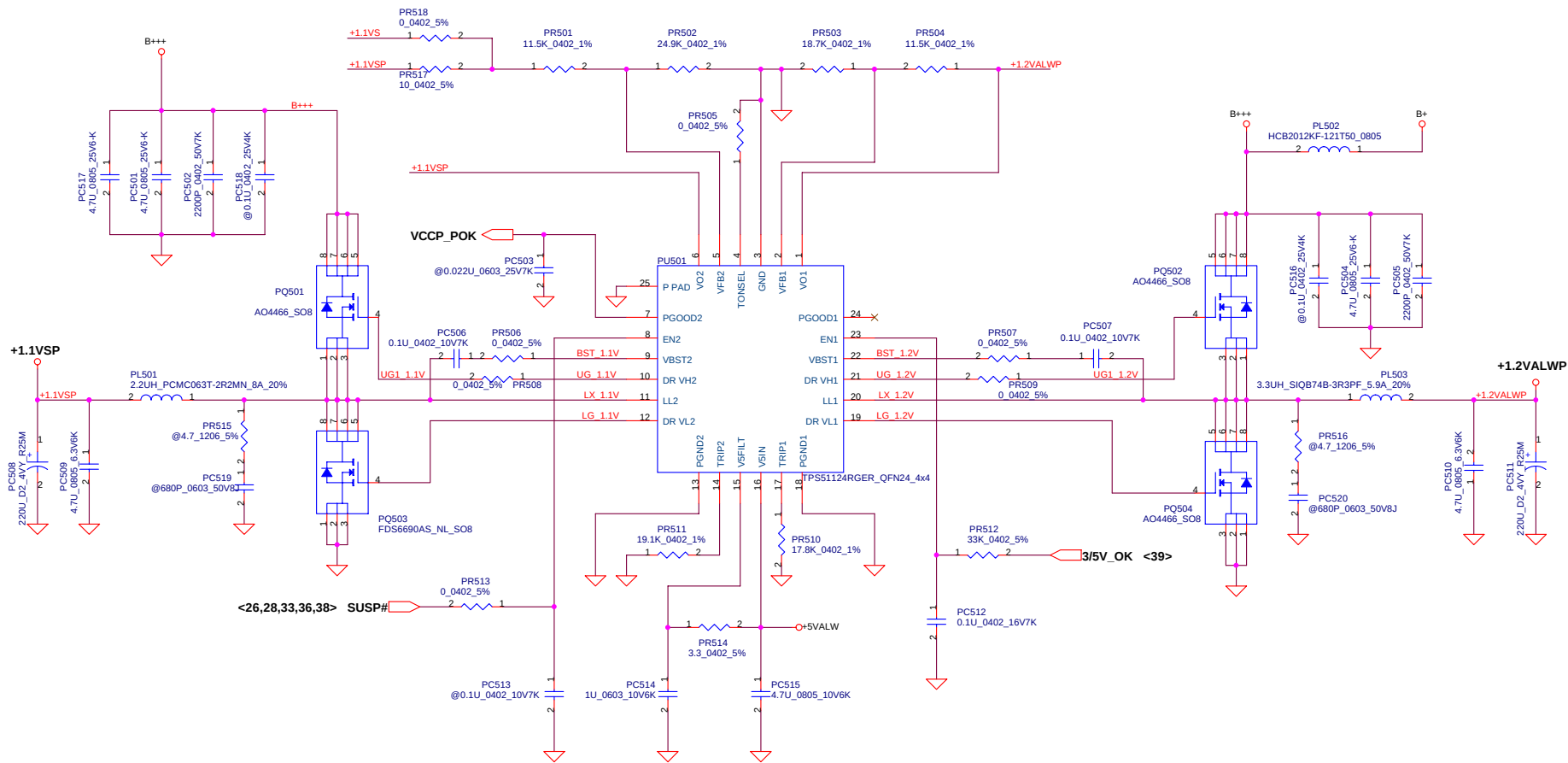
BATT1
45@CR2032 RTC BATTERY



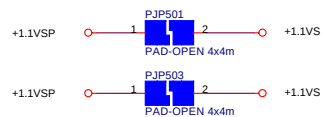
PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



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				Custom	LA-4111P
				Date:	Friday, November 30, 2007
				Sheet	of 48
				Rev	0.1



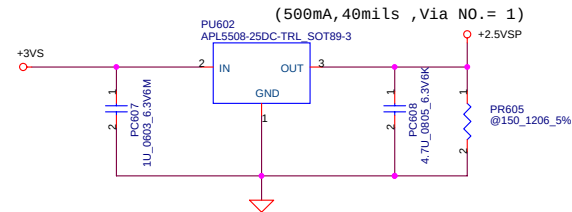
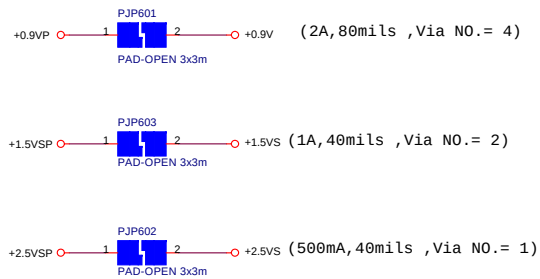
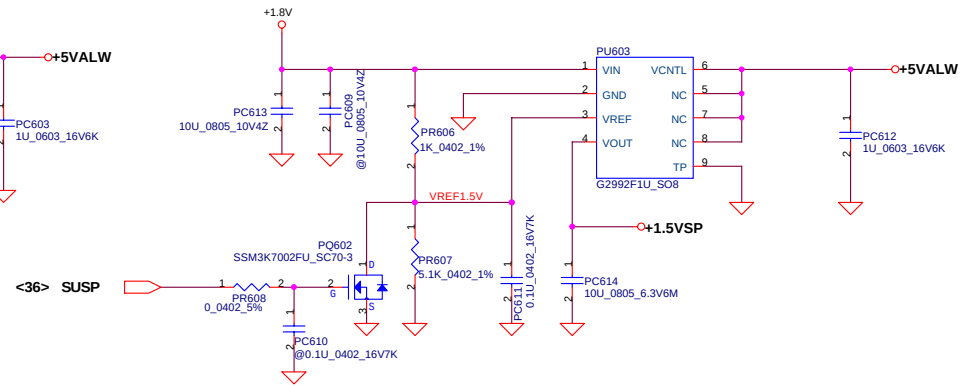
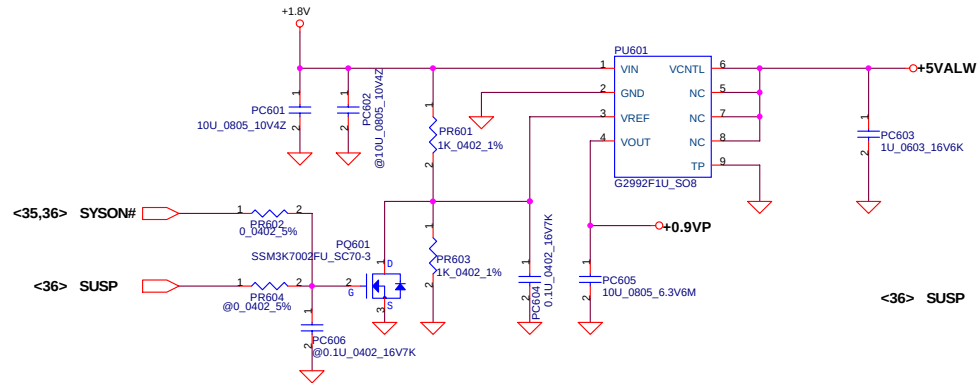
(6A, 240mils, Via N0.=12)



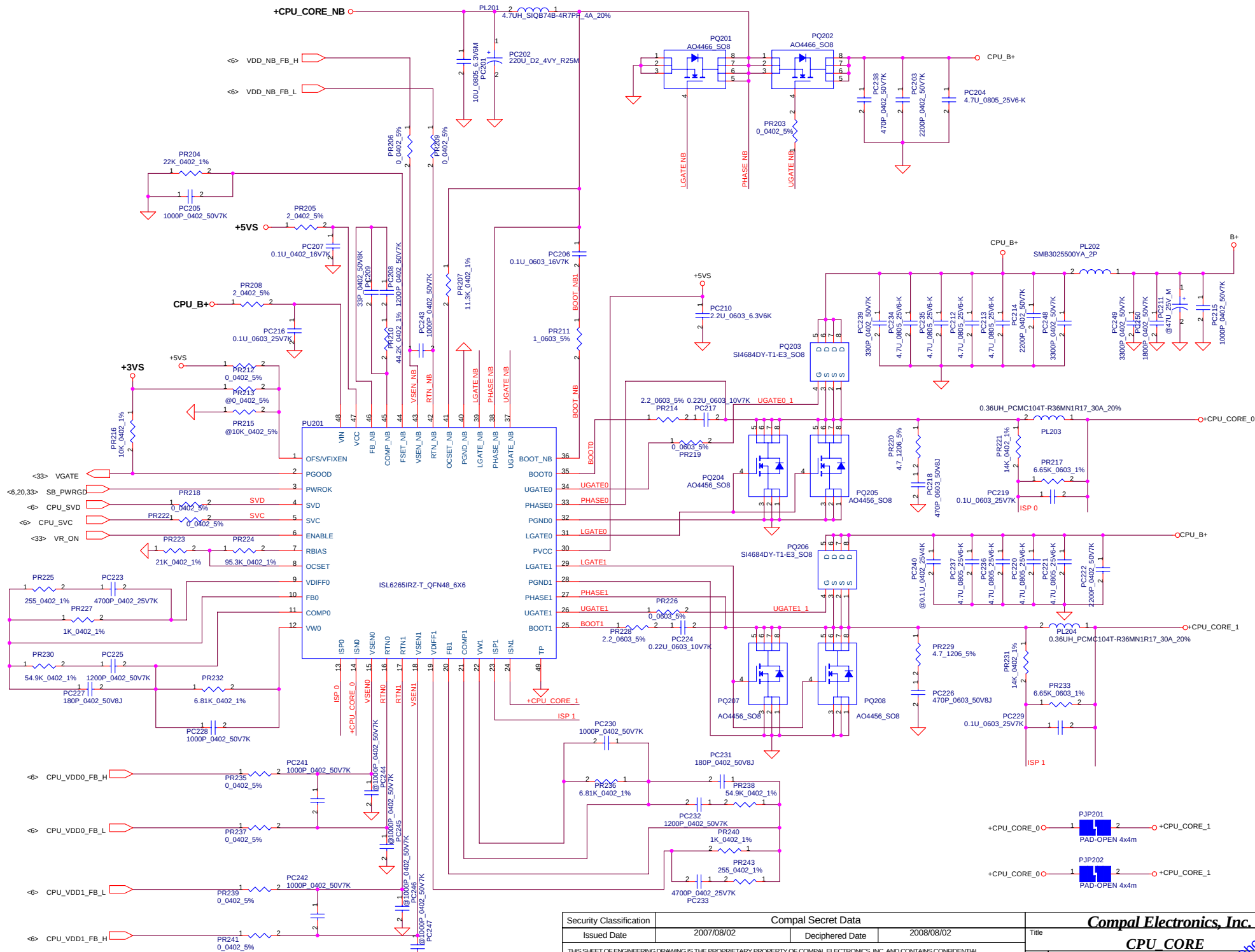
(4A, 160mils, Via N0.=8)



Security Classification	Compal Secret Data			Title		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	1.1VSP/1.2VALWP		
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				Date:	Friday, November 30, 2007	Sheet of 48



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						Size Custom		Document Number		Rev 0.1	
						LA-4111P					
						Date: Friday, November 30, 2007					
						Sheet 42 of 48					



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Issued Date	2007/08/02	Deciphered Date	2008/08/02
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Title			
CPU CORE			
Size	Document Number	Rev	
Custom	LA-4111P	0.1	
Date:	Friday, November 30, 2007	Sheet	of 48

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	9/29	Compal	for Layout	PL3 change the value from SMB3025500YA_2P to HCB2012KF-121T50_0805 and add PL4 the same of the value.	
2	41	1.1VSP/1.2VALWP	9/29	Compal	HW request	PC508 and PC511 change the value from 220U_6.3VM_R15 to 220U_D24VY_R25M	
3	41	1.1VSP/1.2VALWP	9/29	Compal	HW request	Add PJP503	
4	43	CPU_CORE	9/29	Compal	HW request	PC202 change the value from 220U_6.3VM_R15 to 220U_D24VY_R25M	
5	43	CPU_CORE	9/29	Compal	TI FAE suggested that after he review the layout.	Add PC241、PC242、PC243, and the value are 1000P_0402_50V7K. Reserve PC244、PC245、PC246、PC247, and the value are 1000P_0402_50V7K.	
6	43	CPU_CORE	9/29	Compal	TI FAE suggested that after he review the layout.	Add PJP201、PJP202	
7	38	Charger	9/29	Compal	the footprint is wrong	Change the footprint of PR102	
8	37	DC Connector /CPU_OTP	10/08	Compal	for Layout	These two choke are parallel ,it's not series.	
9	38	Charger	10/08	Compal	the footprint is wrong	Change the footprint of PR102	
10	40	1.8VP	10/08	Compal	PWR request	Delete PC410 and PC411	
11	41	1.1VSP/1.2VALWP	10/08	Compal	PWR request	Add PR517、PR518	
12	37	DC Connector /CPU_OTP	11/01	Compal	PWR request	Add PD4、PC12	
13	37	3.3VALWP/5VALWP	11/01	Compal	for Layout	change PQ301, Cencel PQ303	
14	43	CPU_CORE	11/02	Compal	EMI request	Add PC248, PC249, PC250	
15	37	3.3VALWP/5VALWP	11/12	Compal	for Layout	Change PC310, add PC319	

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	LAN	10/29	HW	Change LAN Chip U20 from Marvell 88E8042 to Realtek RTL8102EL	Update the LAN Design page and support circuit	0.2
2	25	LAN	10/29	HPQ	Add POE(Power Over Ethernet) design	Update the LAN Design page and support circuit	0.2
3	16	CRT	10/29	HW	CRT can not display	Change the CRT Conn. signals connection first. Wait correct symbol for fix	0.2
4	29	Audio	10/30	HW	Speaker no sound	Add R973(10K_0402) to +3VALW on HP_DET#	0.2
5	4	FAN	11/01	HW	FAN Conn. not correct part	Change JP2 PCB Footprint from ACES_85204-02001_2P to ACES_88231-02001_2P	0.2
6	29	Speaker	11/01	HW	Speaker Conn. not correct part	Change JP20 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P	0.2
7	34	MDC	11/01	HW	MDC Conn. not correct part	Change JP20 PCB Footprint from ACES_88018-124G_12P to ACES_88020-12101_12P	0.2
8	11,35	TV_OUT	11/05	HW	TV-OUT Function no support	Del R59,R60,R61,R115,R116,R117 and TV-OUT related design.	0.2
9	11,21	NB/SB Thermal	11/05	HW	NB Thermal Function no support (locate too far)	Cancel NB_THERMAL_DA/DC connection between NB and SB,del C500	0.2
10	21,31	SB SATA	11/05	HW	SB SATA Port 5 change to Port 2 for ATI Common Design	Change SB SATA port 5 to port 2	0.2
11	21	SB SATA	11/05	HW	SB SATA_ACT# Pull High become +3VS	Change R343.1 power rail from +5VS to +3VS. Install R343.	0.2
12	21	SB GPIO	11/05	HW	Change SB GPIO refer to JBK00 for common	1. Connect U15.C6 to GND by 0_0402. 2. Change WLOFF# from GPIO50 to GPIO61. 3. Change BT_COMBO_EN# from GPIO51 to GPIO62. 4. Change WWOFF# from GPIO52 to GPIO63.	0.2
13	31	SB SATA	11/05	HW	Vertical L51 1<-->4 , 2<-->3 for layout routing	Vertical L51 1<-->4 , 2<-->3 for layout routing	0.2
14	29	Audio HP OUT	11/05	HW	Add 150UF Caps for each DOCK_LOUT_R/L	Add 150UF Caps for each DOCK_LOUT_R/L	0.2
15	25	LAN Transformor	11/05	HW	Correct U19 LAN Transformor pin definition	Correct U19 LAN Transformor pin definition	0.2
16	21,24	SB SATA	11/06	HW	SB SATA Port 4 change to Port 3 for ATI Open Issue	Change SB SATA port 4 to port 3	0.2
17	36	DIM LED	11/06	HW	Reduce DIM LED unnecessary design	Del R1026 and Q167, add Net "DIM_LED#" for connect. Change location from PJP604 to PJP8.	0.2
18	27	CardReader	11/06	HW	Change CardReader Socket for M/E new part and Chip for JMicron new version	Change JREAD to TAITW_R015-B10-LM. Reserve R413,C902 close to JREAD.20; R412,C901 close to JREAD.26; R411,C900 close to JREAD.37. Change R457 close to U23.42 Add R455,R456 close to U23.42 Del Q169,R1051. Change net CR_LED# become CR_LED connect U23.21 and Q53.2 Add R454 pull down to GND Change R405,R122 from 200K to 10K pull-high Remove C895,U22	0.2

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
19	16	CRT	11/07	HW	Normalize CRT design for common	Change L83,L84 (10_0402) become R241,R240 (0_0603)	0.2
20	17	LCD	11/07	HW	Normalize LCD design for common	Change R491 from 200_0402 to 200_0805	0.2
21	18	LCD	11/07	CIC	CIC feedback RMA concern for common	Change Q43 from AOS3413 to SI2301	0.2
22	33	KBC	11/07	HW	Normalize KB926 Crystal part for common	Change Y7 from 9H03200413 small to 1TJS125DJ4A420P normal.	0.2
23	17	WebCam	11/09	HW	Change U54 WebCam power design and related	Change U54 from G916-390T1UF to RT9193-39GB. Remove R891,R892 if no use G916-390T1UF. Add C718 close to U54.4 for RT9193-39GB. Remove R1027~R1030 for JP7 no install. Change JP7 from 8pin to 6pin	0.2
24	18	HDMI	11/09	HW	Reduce HDMI Design	Remove R490(100K_0402)	0.2
25	19,32	SB-CLK-Debug	11/09	HW	Debug Card no function issue	Del R1031,add R303 close to R301 and U15.P2 Connect for CLK_PCI_SIO2 to JP41.15	0.2
26	25	LAN	11/09	HW	RJ45 LED Power correct back	Change JRJ45.13, JRJ45.11 from +3V_LAN_LED to +3V_LAN	0.2
27	18	HDMI	11/09	HW	Reduce HDMI Design	Remove R490(100K_0402)	0.2
28	6	CPU	11/09	HW	Add H_THERMTRIP# one more way	Add R16 close to Q3.1 for H_THERMTRIP#	0.2
29	33	KBC	11/09	HW	Update KBC Pin Definition for common	Add H_THERMTRIP# to U33.25	0.2
30	35	Holes	11/09	ME	Update for M/E Drawing	Del H49 H50 H38 H45 for M/E drawing change	0.2
31	26	Mini-Card	11/09	HW	Reduce Mini-Card design, change SIM Card design	Replace D17 and D47 become R52 and R53 Del R400 and R46, Change JP6 pin definition for common	0.2
32	33	KBC	11/09	HW	Reserve 0_0603 for KB Back Light	Add R516 (0_0603) between JP48.1/4 and +5VS_LED	0.2
33	27	CardReader	11/10	HW	Correct CardReader LED part	Change D5 from SC500004E00(AQUA_WHITE) to SC500004W00(WHITE)	0.2
34	34	LED Function	11/10	HW	Correct LED function for common	Change LED from D50,D30,D27 SC500004E00 (AQUA_WHITE) to D6,D7,D8 SC500004W00(WHITE) Change LED from D45,D46 SC500004B00 (AQUA_WHITE/AMBER) to D17,D18 SC500005M00 (YELLOW/WHITE); Add Q7,R20 and R42 close to D18	0.2
35	21	SB-GPIO	11/10	HW	Add one more way for GSENSOR LED# inform pin	Add HDD_HALTLED# connect from U15.P8	0.2
36	33	KBC-GPIO	11/11	HW	Add CIR_IN PH to +5VL Add ESB_CLK/DAT PH to +3VL	Add R46 10K_0402 PH to +5VL close to U33 Add R514,R515 10K_0402 PH to +3VL close to U33	0.2
37	6,31	CPU,FPR	11/13	HW	Reduce S3 power consumption	Change R15.2,R21.2,R36.2,R30.2 connection from +1.8V to +1.8VS; Remove R622, install R581	0.2
38	11	NB	11/13	HW	Reduce the level shift design for Chip A12.	Del Q6,R87; Q5,R84 and replace by 0ohm (add R67,R68) connect directly. Install R371 (10K ohm)	0.2
39	17	WebCam	11/13	HW	Update the WebCam+Digital Mic reserver conn.	Change JP7 from SP02000HC00(8pin)-->SP02000IL00(6pin)	0.2
40	6,33	CPU,KBC	11/13	HW	Update THERMTRIP# design to EC	Change R16.2 connection from THERMTRIP# to THERMTRIP#_EC for separate	0.2
41	18	HDMI	11/13	HW	Remove EMI solution become reserve for verify	Add R112,R113,R115~R120 close to each L85~L88 for co-lay	0.2

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	19,32	SB,BIOS	11/13	HW	Reduce SB related design for Chip A12 and others	Del Q155,R986, and add R311 close to U15. Del R1011 become T18, Cancel R1012 and connect to H31 and JP41 directly	0.2
43	21,32	SB,BIOS	11/13	HW	BIOS Debug Tool reserve	Add SB_INT_FLASH_SEL and related (JP12,U30,R228,R226,C489 close to U29)	0.2
44	25	LAN	11/13	HW	Update LAN Chip Symbol link to CIS server	Update LAN Chip U20 Symbol link to CIS server	0.2
45	13	NB	11/13	HW	Add 0ohm_0603 to separate VDD18_MEM	Add R1051(0_0603) between +1.8VS & +1.8V_VDD_SP	0.2
46	18	HDMI	11/13	HW	Reduce HDMI related design for common	Del R490 (100K_0402)	0.2
47	20	SB	11/13	HW	Reduce SB related design for common and A12 chip	Remove R994 (0_0402) Change U15.F1 connection become test point Remove R1053, change R1052 become 0_0402	0.2
48	20,21,27	SB,Cardreader	11/13	HW	Reserve Cardreader D3E function (CR_WAKE# & CR_CPPE#)	Add R81 close to U15;Q54,R124 close to U23 for connect U15.F8 to U23.13 ;Add R369 close to U23 for connect U15.M5 to U23.16	0.2
49	21,33	SB,KBC	11/13	HW	Reduce SB related design for common	Del D51 and R1034, Change the net AC_IN become AC_IN_D	0.2
50	28,33	Codec,KBC	11/13	HPQ	EC_BEEP function for KBC add	Add R563 close to C955; Add R544 close to U33.31	0.2
51	33	KBC	11/13	HW	Reduce S5 Power Consumption	Change R1040.1 connection from +3VL_EC to +3VALW Del R546 PH to +3VL_EC, Del D26 replace by add R547 close to U33 for short	0.2
52	33	KBC	11/13	HW	Reduce KBC Design for common and Ver:C0 Chip Change from SA00001J530 to SA00001J540	Del R537 become Test Point, change R516 become 150_0603 Remove R1044, change R1040 from 10K to 100K Change R528.2 , R529.2 connection from +5VALW to +5VL Install C814 (4.7U_0805)	0.2
53	34	Switch Design	11/13	HW	Update CSD function board design for common	Change JP36.1 connection become +3VL;Change R1046.1 and R1047.1 connection become SMB_EC_CK1/DA1 Change JP36.7 connection from GND to +5VALW_LED by Change Q153 from 2N7002DW to 2N7002	0.2
54	34	LED	11/14	HW	Correct T/P On/Off LED design define Correct G-Sensor LED design define	Change R988.1 connection from +5VS_LED to +3VS	0.2
55	29	Audio-Dock	11/14	HPQ	For GS mark requirement	Add R968,R969 close to C775/C776.	0.2
56	29	Holes	11/14	ME	Update Holes to meet M/E Drawing	Add back H52 become H_1P5N; Del CF4	0.2
57	4,24	Multi-Bay	11/14	ME	Update Symbol to meet M/E Drawing	Update JP2,JP9,JP10,JP11,JP20,JP40,JHDMI,JESAT,JCRT, JDOCK Symbol	0.2
58	33	Holes	11/14	ME	Update Holes to meet M/E Drawing	Add back H52 become H_1P5N; Del CF4	0.2
59	20	SB	11/16	ATI	Reserve to fix the OTS325055 Issue	Reserve R83 PH to +3VS	0.2
60	33	KBC	11/16	EC	Change design for EC team debug	Change JP34.1 from +5VALW to +5VL	0.2
61	35	DOCK	11/16	EMC	Connect DOCK guide pin to GND	Add JDock.45/46 to GND	0.2
62	33	K/B	11/16	HW	Fix KB matrix issue	Del KSI6 and KSO9 out of page net connect	0.2
63	28,29	AUDIO	11/18	HPQ	Make some Audio related design change	Change C983,C984 from 1UF to 0.022UF. Change C1049,C1050,C1040,C1041 from 0.47UF to 0.022UF. Change R1002,R1005 from 20K to 0 ohm. Change C1044 from 10UF to 4.7UF. Remove R1000,R1004; Install R1001,R1003.	0.2
64	29	AUDIO	11/19	HPQ	Make some Audio related design change	Change R968,R969 from 40.2_0402 to 47_0603	0.2

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
65	13	NB	11/20	ATI	Design Change for NB A12 Version chip	Remove U64,C1064,C1065,C1066,C1067,R1015,R1016,Q163,R1017. Install L19, remove L95	0.2
66	22	SB	11/20	ATI	Design Change for SB A12 Version chip	Install R593, remove R592	0.2
67	22	SB	11/20	HW	Reduce SB Power Design-No IDE support	Remove R12,C543,C544,C547,C536	0.2
68	33,34	Function Board	11/20	HW	Reserve for Rachman UMA selective	Reserve R555 for +5VALW_LED, add R554 for +3VL close to JP36.1 Reserve R1034 close to JP36.4,R1035 close JP36.5,Remove R1036 Add R513 PH to +3VS close to U33.19	0.2
69	23	SB	11/20	HW	Make the SB Strap Seeting for common	Install R356 (10K_0402)	0.2
70	31	BlueTooth	11/20	HW	Update BT design for common	Change R520 from 47K_0402 to 10K_0402	0.2
71	34	Power On Switch	11/22	HW	Cancel one reserved power on switch	Del SW3	0.2
72	33	KBC	11/22	HW	Modify SMB_EC_DA1/CK1 PH for common	Change R528,R529 pin 2 connection from +5VL to +3VL	0.2
73	6	CPU	11/22	HW	Link PROCHOT# between CPU and NB	Add R59 close to Q2	0.2
74	19	SB	11/22	HW	Reserve LPCCLK1 for debug card function	Add R308 22_0402 for U15.E22 close to R362.1, remove R301	0.2
75	26	Express Card	11/22	HW	To avoid New Card Switch leakage issue	Add R54(0_0402) close to U21.6	0.2
76	28	Audio Codec	11/22	HW	Reserve SPDIF OUT1 test point for verify	Add T21 close to U27.45	0.2
77	10~13	NB,	11/23	HW	BOM correct for SI-1 SMT build	Update U3(SA00001ZG00-->SA00001ZG20);U10(SA00001Z300-->SA00001Z310);U15(SA00001S510-->SA00001S560)	0.2
78	19	SB	11/23	HW	Change Crystal Res. size for layout space	Change R389 from 0603 to 0402	0.2
79	22	SB	11/26	HW	Reduce SB SATA Power Caps (Confirm with ATI FAE)	Change C567,C568 from 10U_0805 to 1U_0805	0.2
80	28	Codec	11/26	HW	SPDIF0 --> 1 design change to follow Vader	Change U27.48/45 pin connection	0.2
81	34	T/P	11/28	HW	Change T/P Power for reduce S4/S5 power consumption	Remove R235; Add Q85, R645, Q34	0.2
82	14	HDMI	11/28	ATI	Fix HDMI no function issue	Remove R102; Add R101	0.2
83	15	CLK Gen.	11/28	HW	Change design for new version CLK Gen.	Remove R1045	0.2
84	28	Codec	11/28	HW	Change EC_BEEP function become reserve	Remove R563	0.2
85	20,27	SB,CardReader	11/28	HW	Disconnect D3E support for A version to avoid risk	Remove R81,R369	0.2
86	32	BIOS	11/28	HW	Use Ext. BIOS as default	Remove R221	0.2
87	34	LED	11/28	HW	Cancel WLAN/WWAN ext pull high	Remove R1041	0.2
88	19	SB	11/30	HW	Fix PA M/E Interfere issue for SI-1	change Y3 from SJ100001U00 to SJ100006600 with 10PPM	0.2
89	06,19,23	SB	11/30	ATI	ATI recommend for update	Change R312 from 0_0402 to 33_0402; Change R356 from 10K_0402 to 2.2K_0402; Install C23 as 0.1UF_0402	0.2
90	33	KBC	11/30	HW	Change 32.768KHz Main Source Vendor become EPSON	Change Y7 from SJ100001V00 to SJ132P7K220	0.2
91	32	BIOS	12/03	HW	Cancel Ext. BIOS reflash design because of +3VL erroe	Add R221; Remove U30,R226,R228,C489	0.2
92	34	LED	12/03	HW	Cancel G-Sensor INT2 LED function	Remove Q156	0.2