ZY6D SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 璉ゴ
268@ AUDIO 268 璉ゴ
D@ DOCK
D2@ DDR2 璉ゴ
SP@ 疚 (EXT VGA OR DDR2)
ED2@ EXT VGA & DDR2 璉ゴ
CB@ CARDBUS 璉ゴ
NSF@ Non ASF 璉ゴ

I@ INT VGA 璉ゴ
888@ AUDIO 888璉ゴ
D3@ DDR3 璉ゴ
ND@ NON DOCK 璉ゴ
ID2@ INT VGA & DDR2 璉ゴ
ED3@ EXT VGA & DDR3 璉ゴ
ID3@ INT VGA & DDR3 璉ゴ
ASF@ ASF 璉ゴ
NCB@ NON CARDBUS 璉ゴ

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

X'TAL 14.318MHZ
CLOCK GENERATOR
ICS: ICS9LPRS365BGLFT
SELGO: SLG8SP512K05
P2

Penryn 479 uFCPGA P3,P4
CPU Thermal Sensor P3

FSB 667/800/1067 Mhz

DDRII SO-DIMM 0 SO-DIMM 1 P16
Dual Channel DDR2 667/800 MHz

NB Cantiga PM965 P5,P6,P7,P8,P9,P10,P11
CRT Page:19
LVDS Page:19

X4 DMI interface

HDD (SATA)*2 P25
ODD (SATA) P25
SATA0
SATA1
SATA4

SB ICH9M P12,P13,P14,P15
X'TAL 32.768KHZ

PCI-Express
PCIE-4
PCIE-6
WLAN P23
X'TAL 25M

USB 2.0
USB Port x 4 USB0~3 P25
CCD USB7 P19

Azalia
Int MIC P27
Azalia Audio Controller ALC268 & 888 P27
Audio Amplifier P27 & 28

LPC
EC (WPC8769LDG) P32
X'TAL 32.768K
SPI ROM P32
Touch Pad P32
K/B COON. P32

BROADCOM 10/100/1G LAN 5764M P21
SWITCH CIRCUIT Page:22
LAN Page: 33
Transformer P22
RJ45 P22

Connector
Speaker P28
Phone Jack P28
SPDIF P28
Line in P28
MIC Jack P28

Fan Header P31

Quanta Computer Inc.
PROJECT : ZY6D

Size	Document Number	Rev
	Block Diagram	1A
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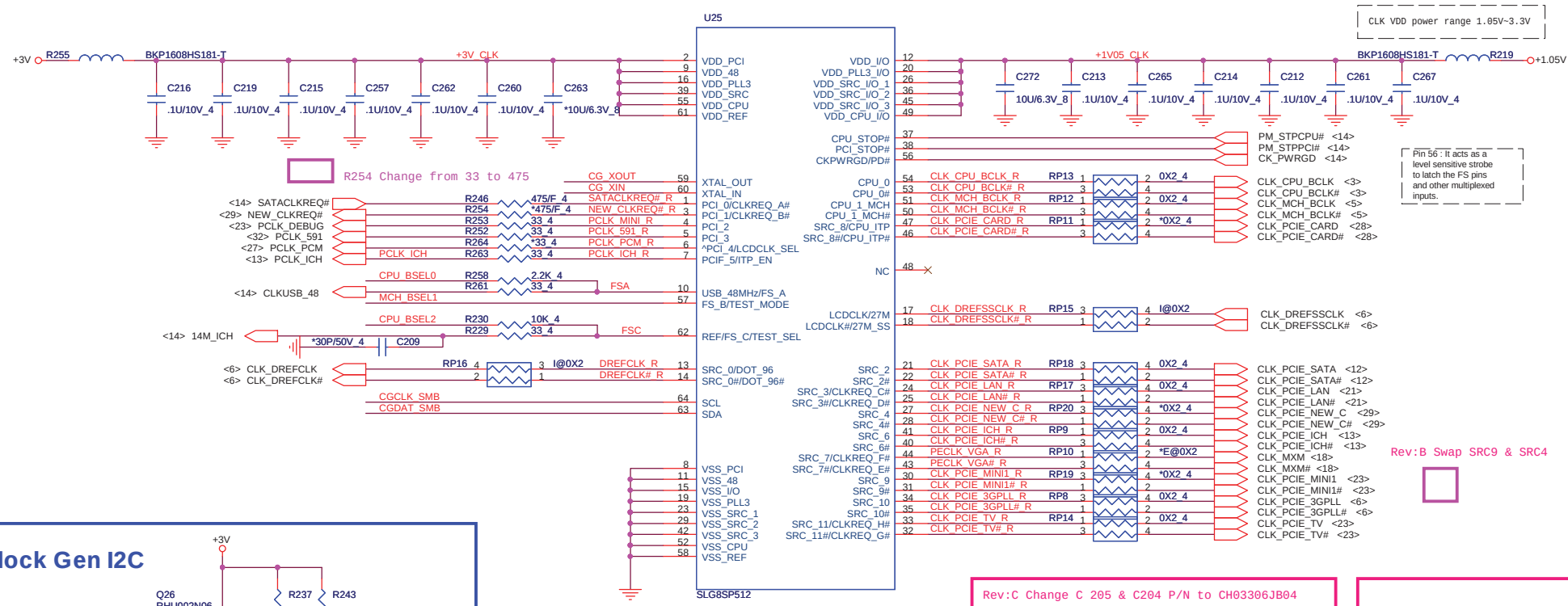
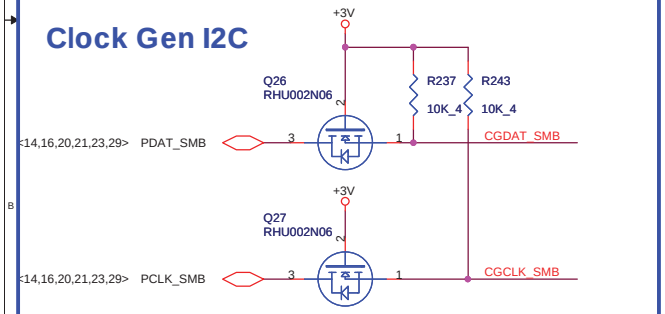
Clock Generator

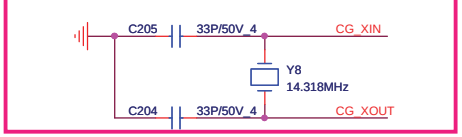


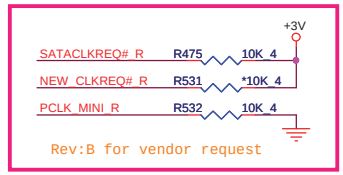
Clock Gen I2C



	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13

Rev:C Change C 205 & C204 P/N to CH03306JB04





CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

<3> CPU_BSEL0 R262 0_4 MCH_BSEL0 <6>

<3> CPU_BSEL1 R226 0_4 MCH_BSEL1 <6>

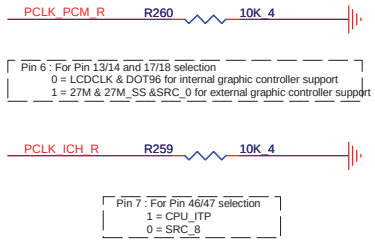
<3> CPU_BSEL2 R231 0_4 MCH_BSEL2 <6>

CRB Rev0.7 : 110(CBA)

BSEL Frequency Select Table

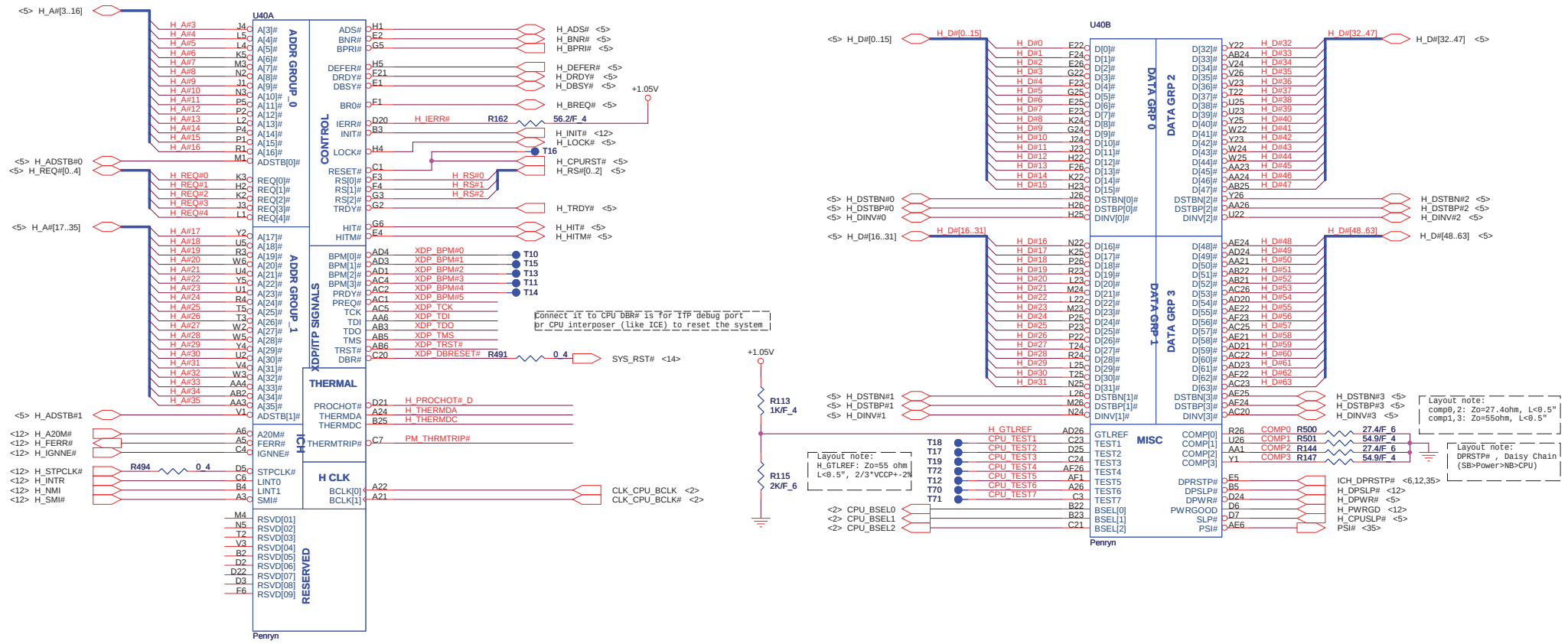
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

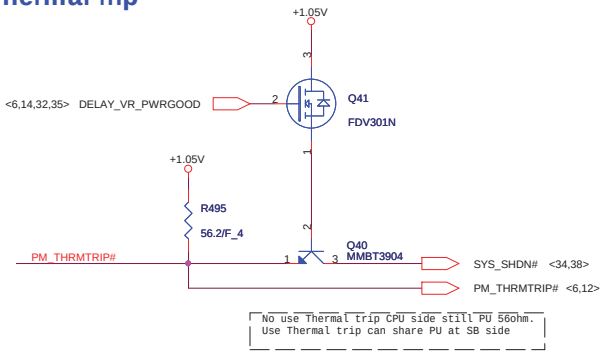


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

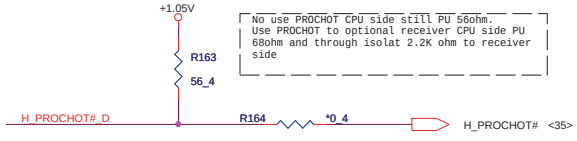
Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
Date: Thursday, August 28, 2008	Sheet 2 of 40	



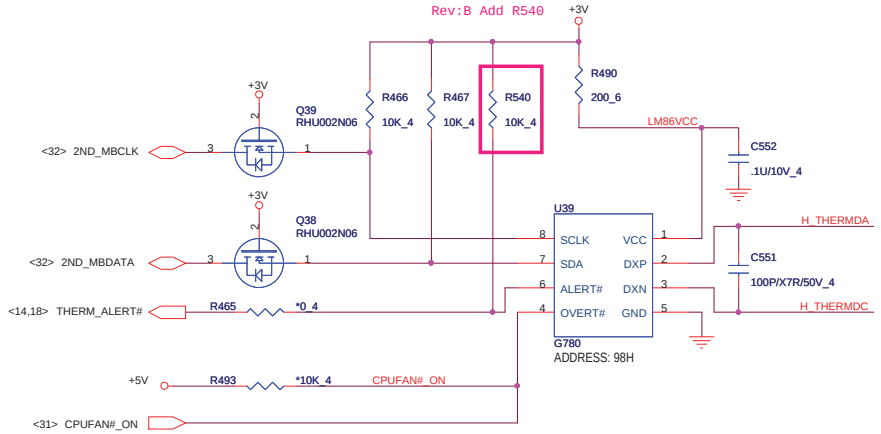
Thermal Trip



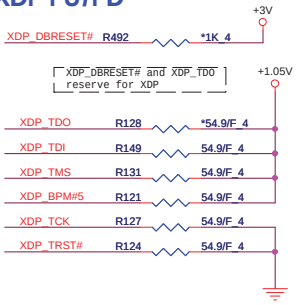
Processor hot



CPU Thermal monitor



XDP PU/PD



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CPU Host Bus	1A
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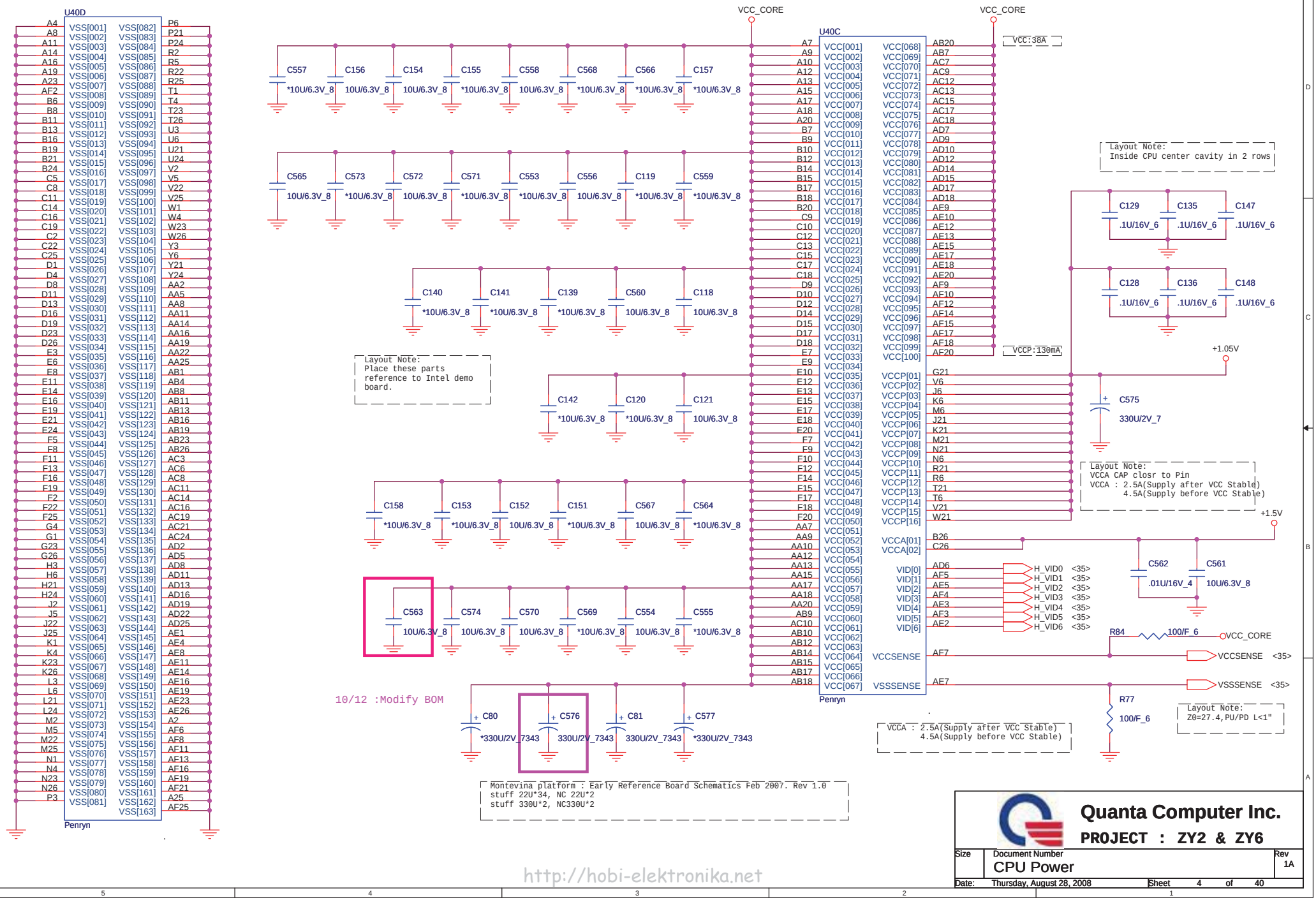
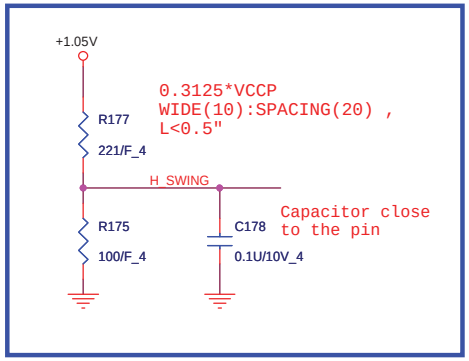
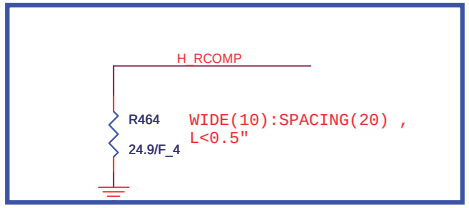
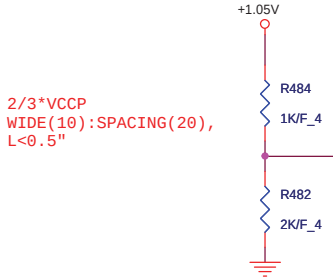
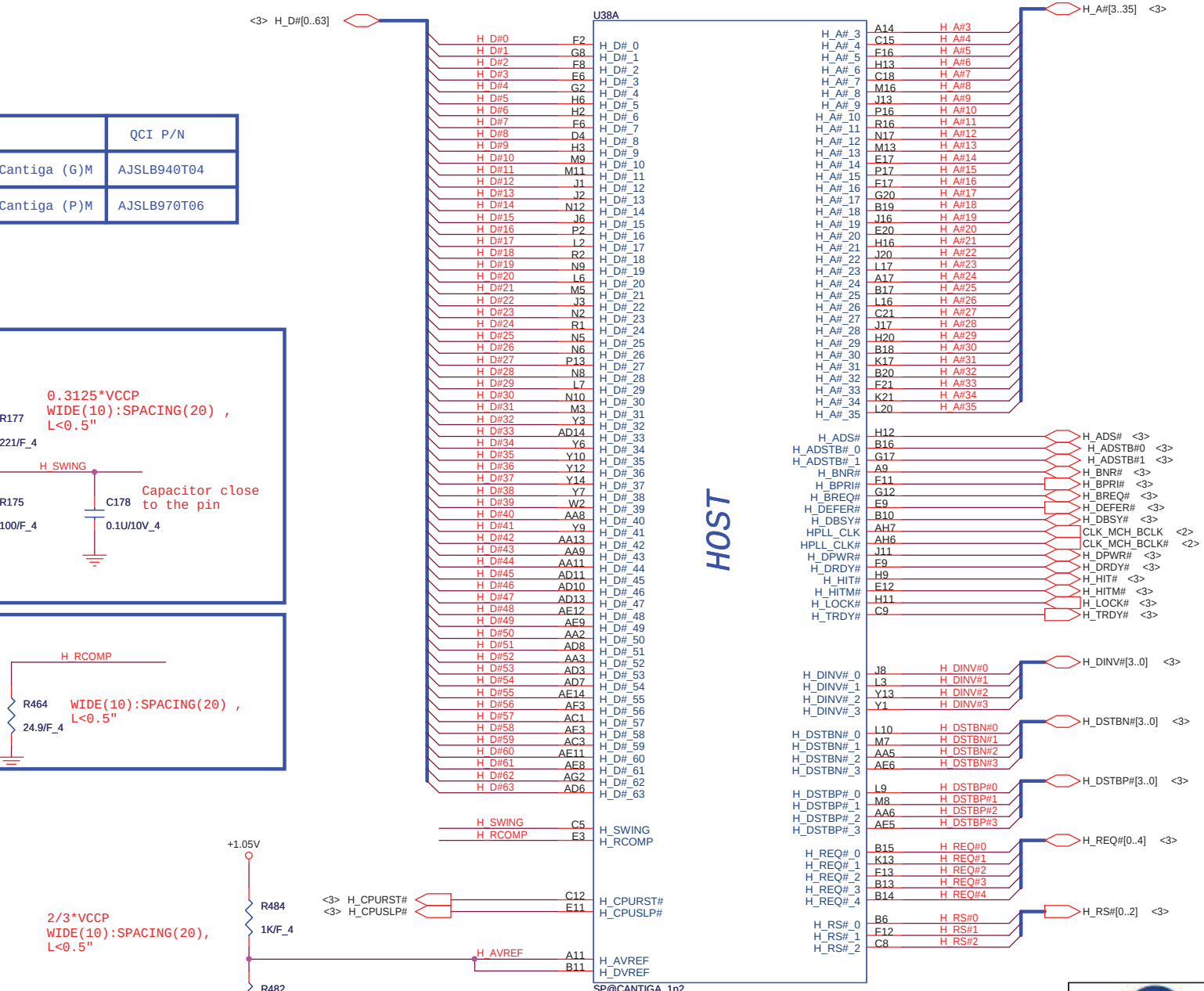


	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06









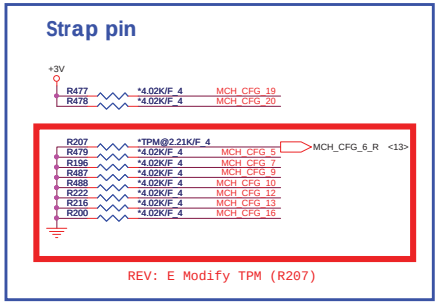
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

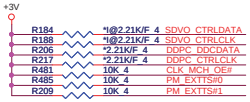
Size	Document Number	Rev
	GMCH HOST	1A
Date: Thursday, August 28, 2008	Sheet 5 of 40	

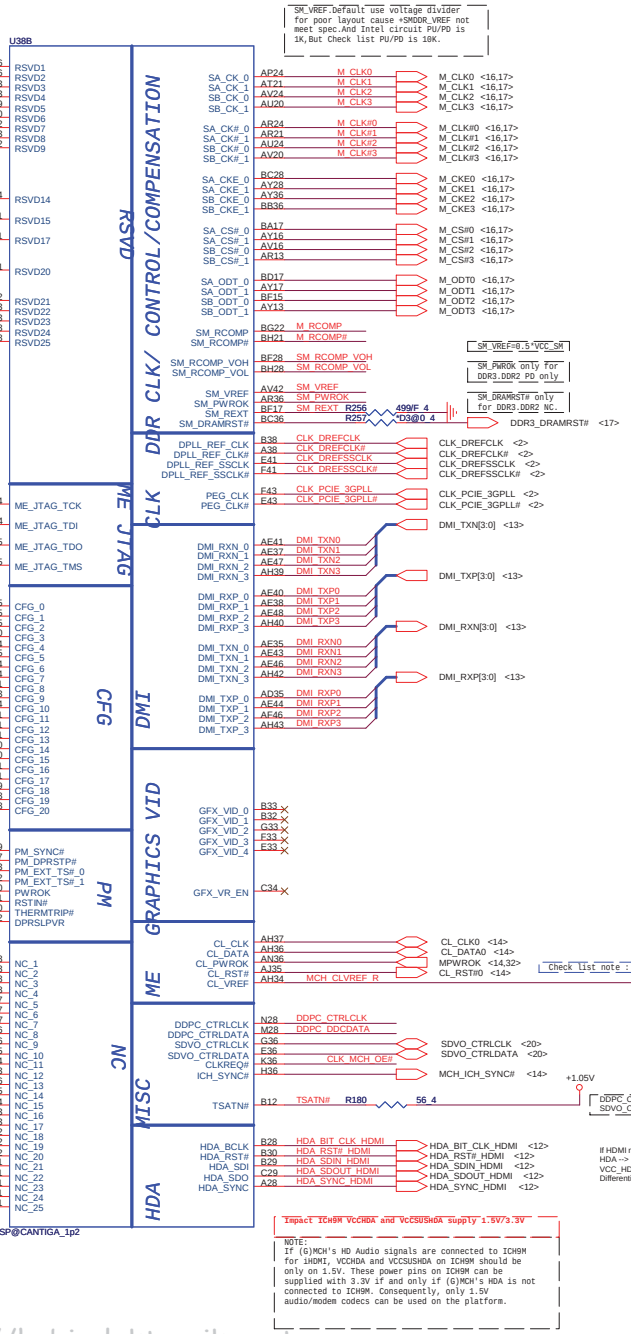
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

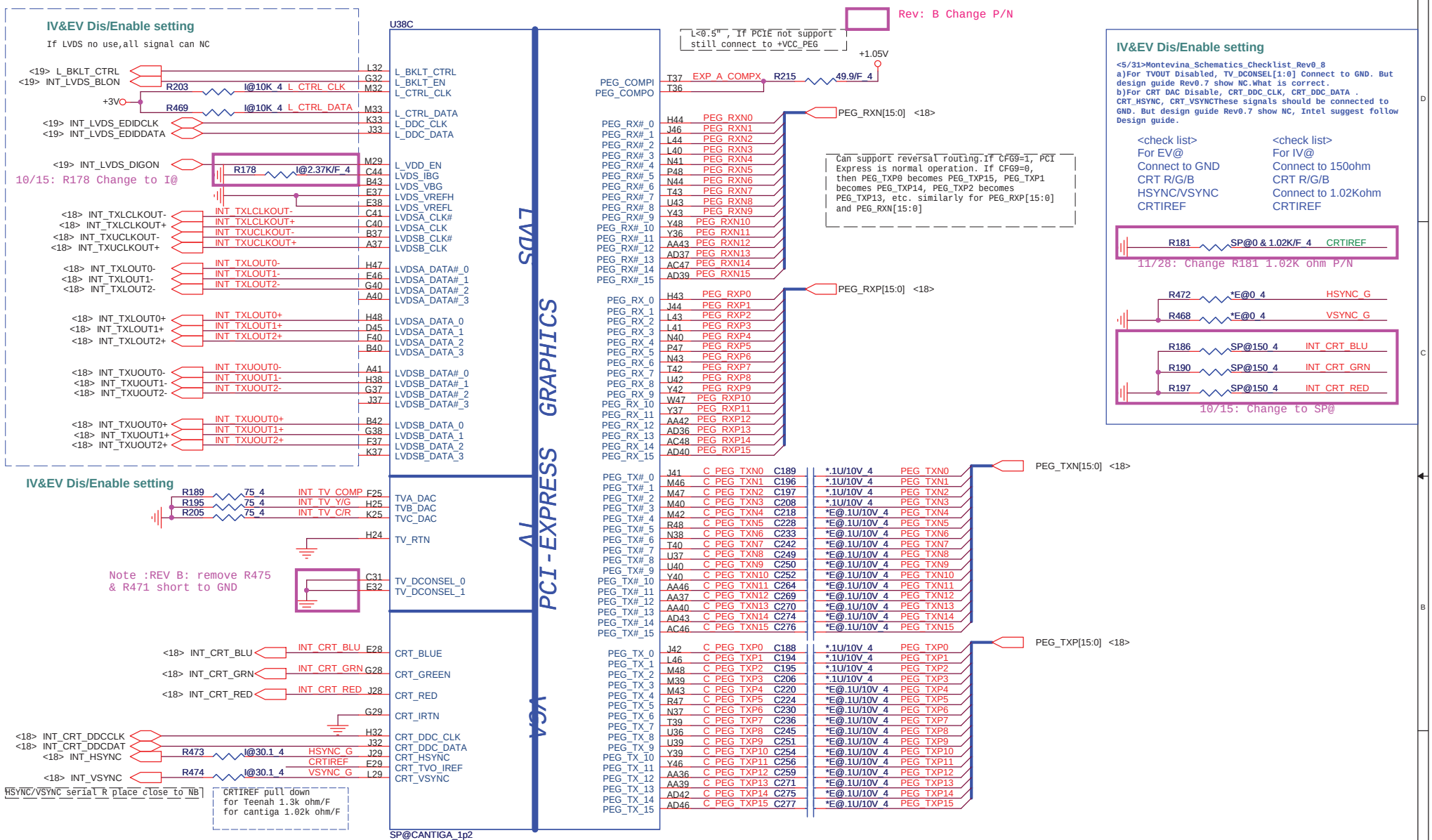
Strap pin

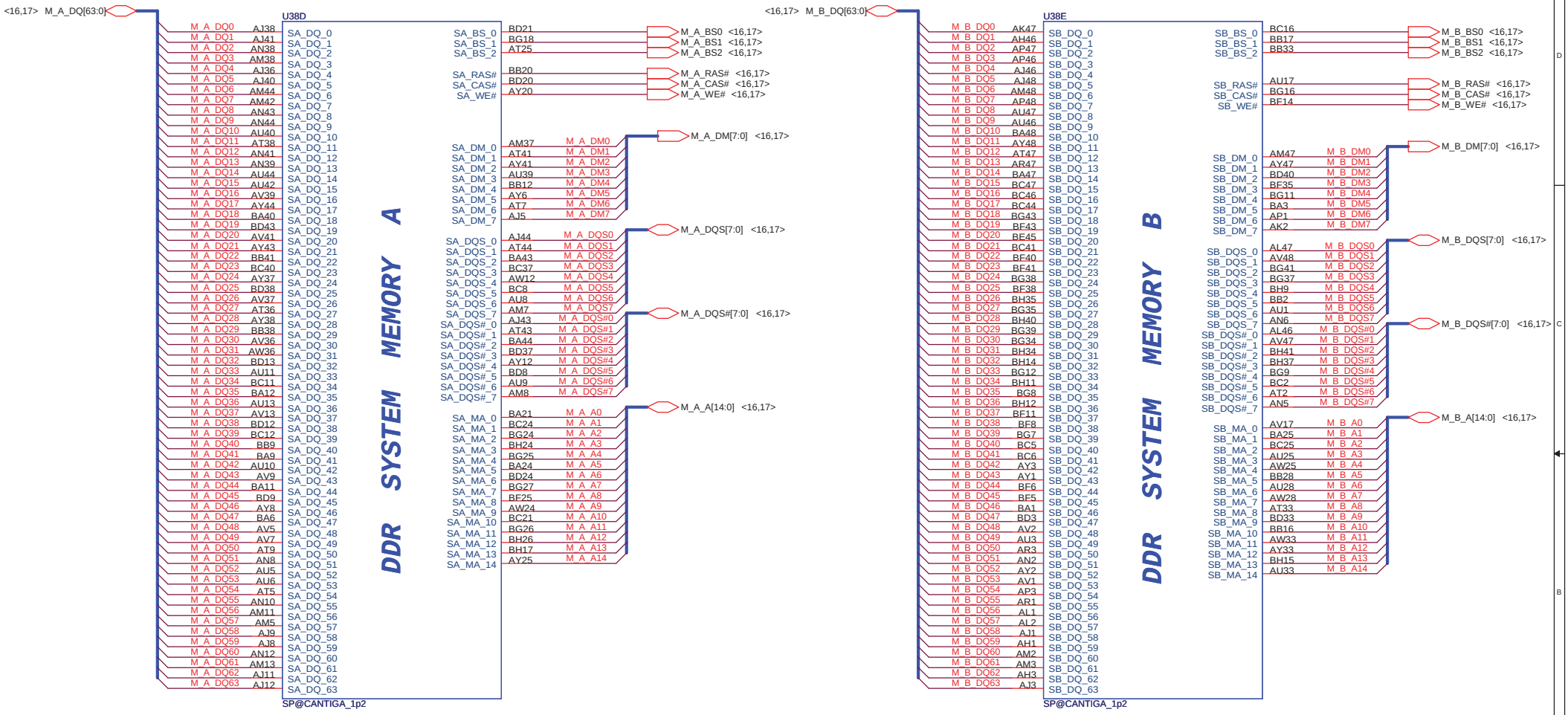






Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: GMCH DMI	Rev: 1A
Date: Thursday, August 28, 2008	Sheet 6 of 40	





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH DDRII	1A
Date: Thursday, August 28, 2008	Sheet 8 of 40	

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL, VCCA_MPLL, VCCA_PEG_PLLVCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND
SP@:INT 1 U
EXT 0 ohm

1.8V
Internal connect to power

U38G
VCC SM POWER
VCC GFX NCTF
VCC GFX
VCC SM LF

U38F
VCC CORE POWER
VCC NCTF

SP@CANTIGA_1p2

+VDR_SUS
+1.05V_AXG
+1.05V
+1.05V_AXG

C519 22U/6V_8
C521 22U/6V_8
C244 0.1U/10V_4
C518 330U/2V_7
Place on the edga

C231 .1U/10V_4
C225 .22U/6V_4
C226 .22U/6V_4
C210 22U/6V_8
C524 330U/2V_7
Place close to the GMCH

R227 I@0_8
R228 I@0_8

C191 I@330U/2.5V_7343
C192 I@330U/2.5V_7343
C200 I@.47U/6V_4
C237 SP@0_6
C217 I@10U/10V_8
C201 I@22U/6V_8
C247 I@.1U/10V_4
C203 I@.1U/10V_4
Place close to the GMCH
Cavity Capacitors

R242 I@10/F_4
R238 I@10/F_4
VCC_AXG_SENSE
VSS_AXG_SENSE

C268 .1U/10V_4
C239 .1U/10V_4
C255 .22U/6V_4
C253 .22U/6V_4
C238 .47U/6V_4
C266 1U/6V_4
C258 1U/6V_4

Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
GMCH VCC,NCTF
Rev 1A
Date: Thursday, August 28, 2008
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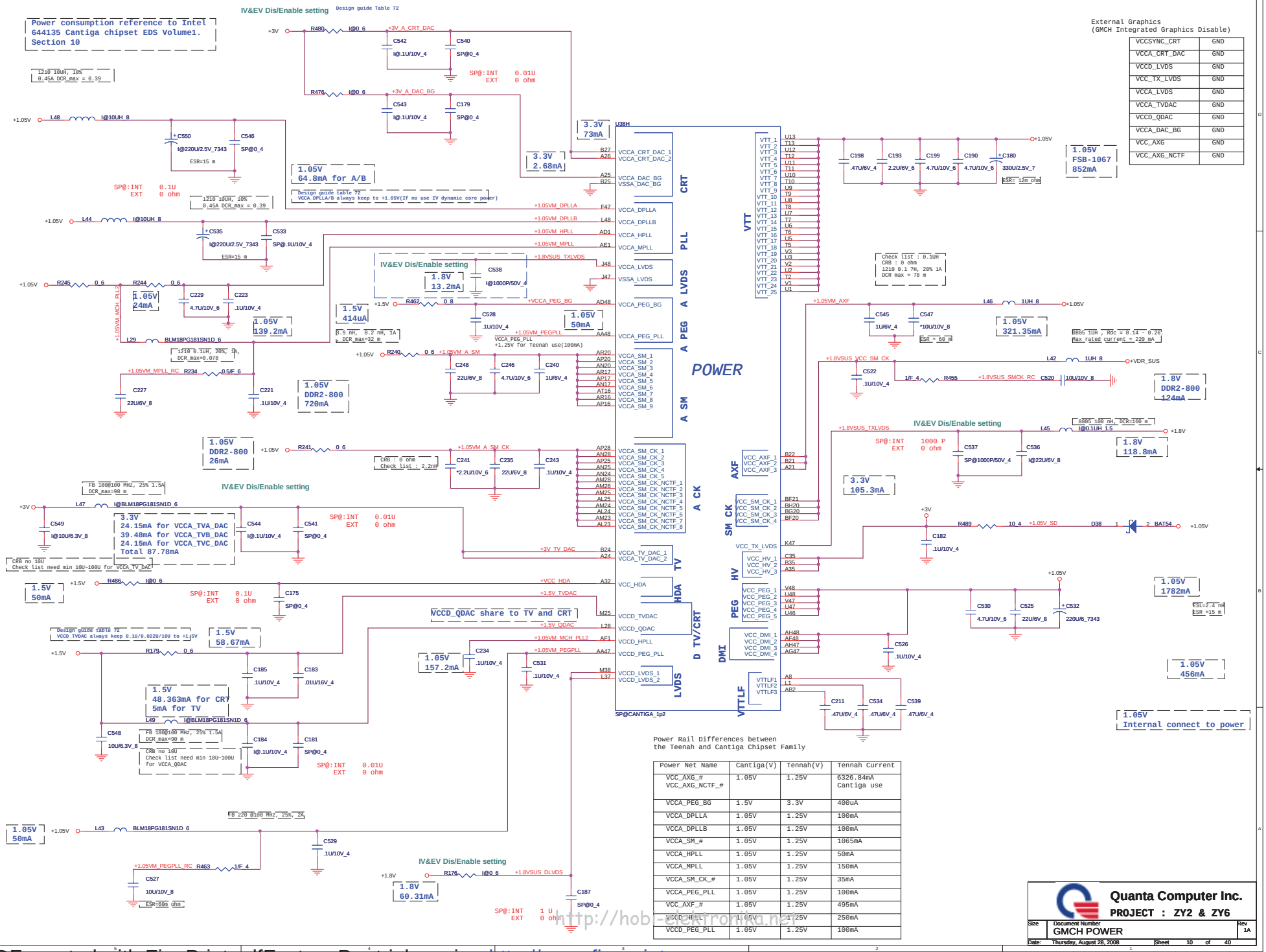

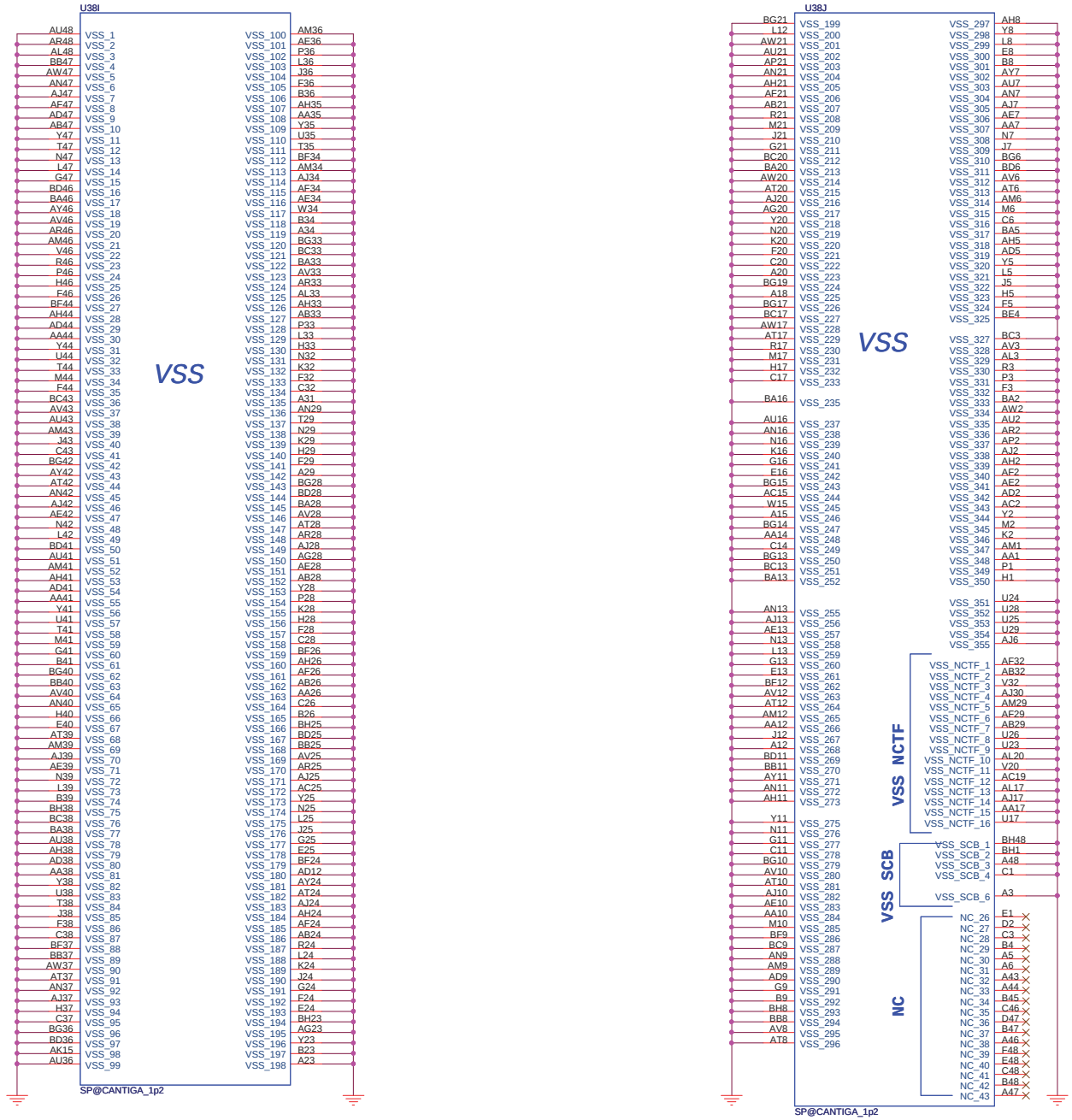

Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VSS	1A
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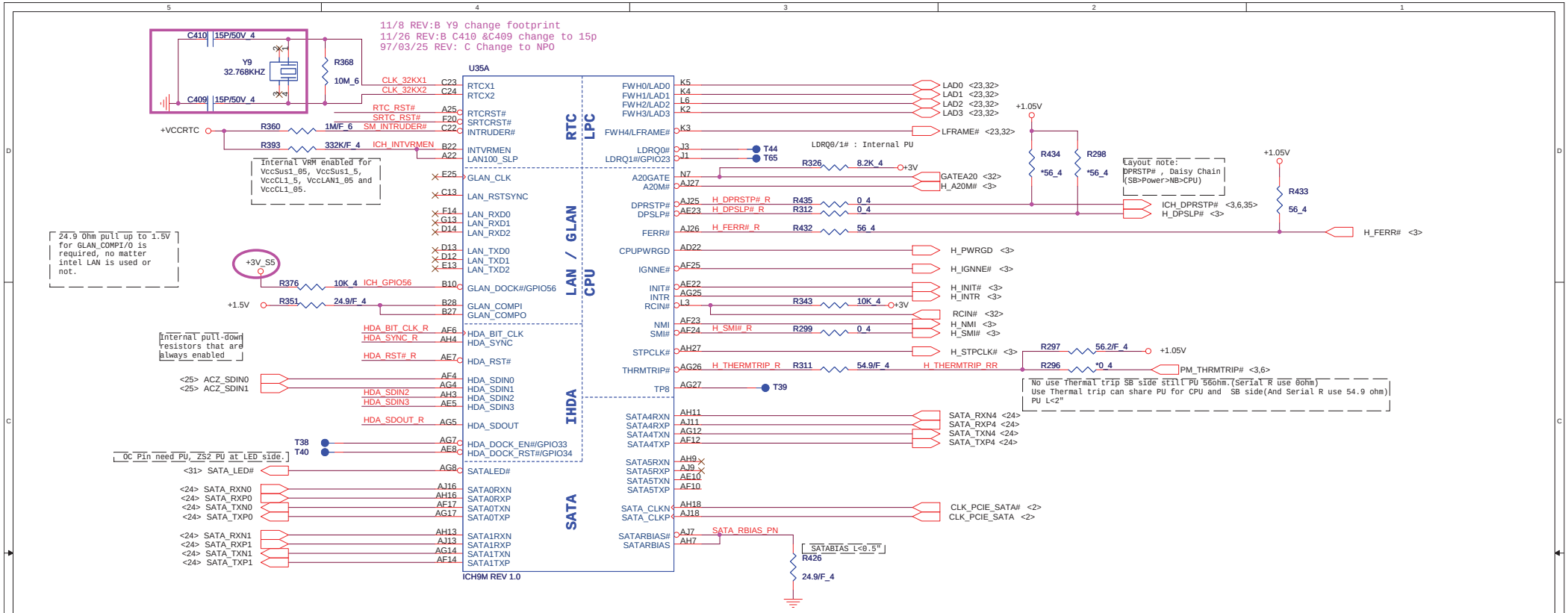
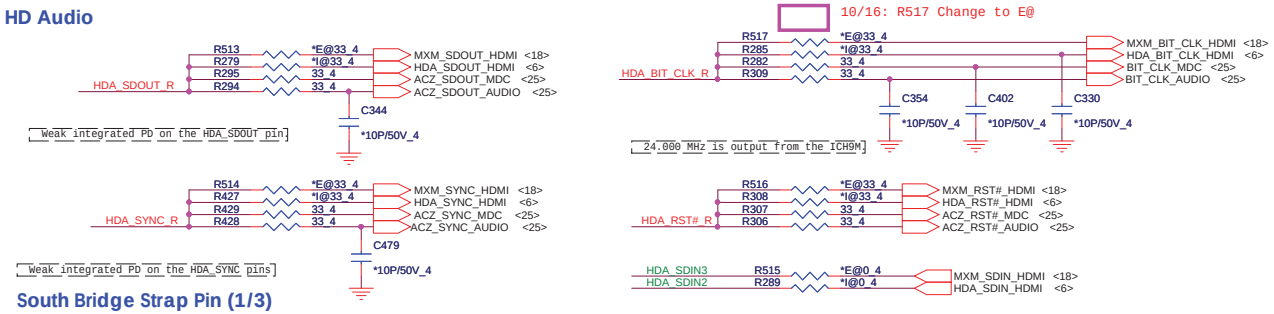


HD Audio

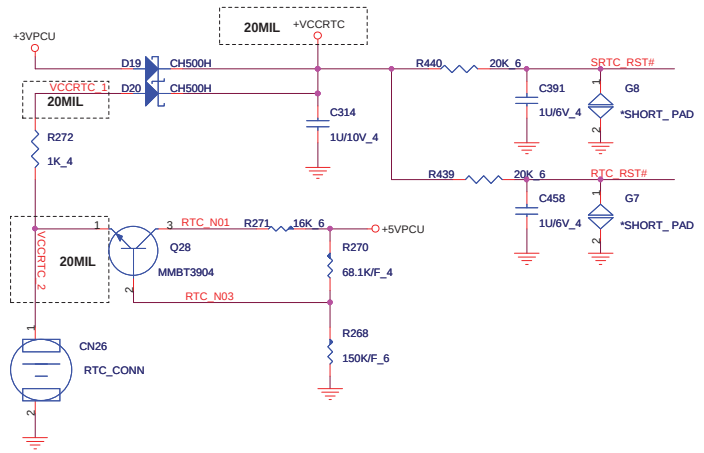


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	<14> ICH_TP3 — ICH_TP3 R406 *1K_4	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUT_R R310 *1K_4 +3V	

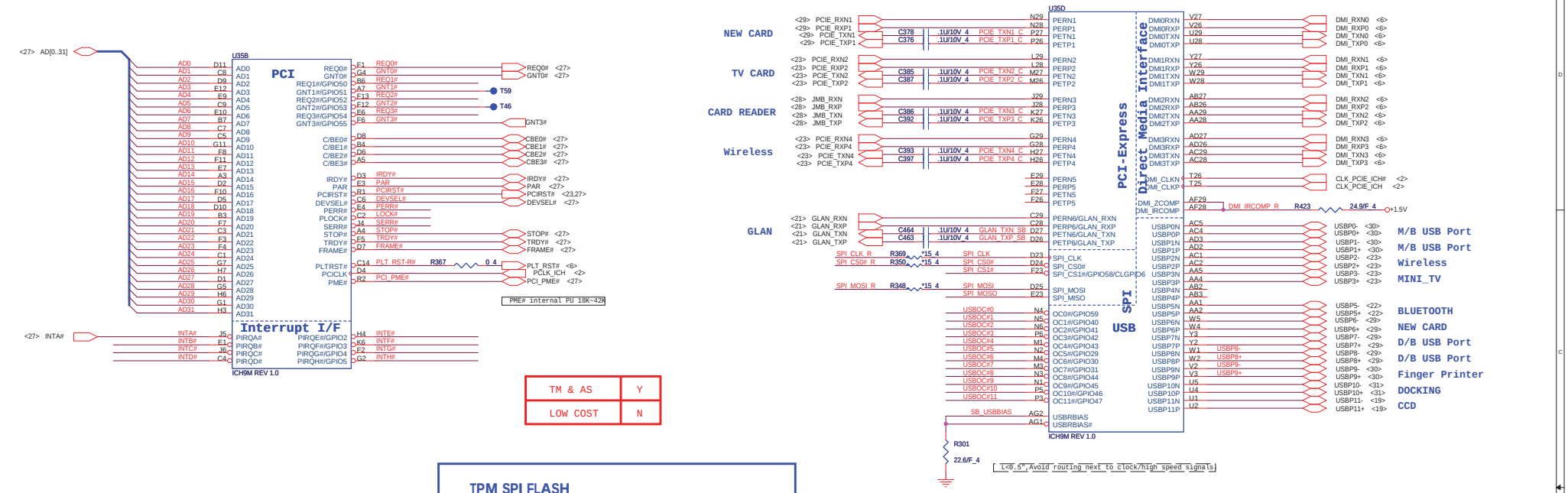
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

RTC

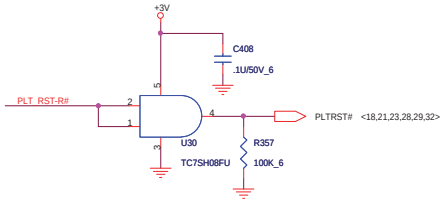


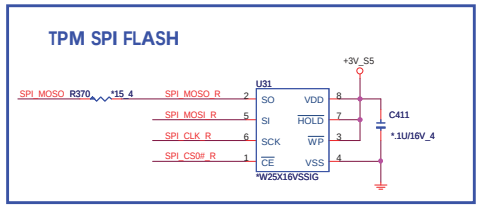
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Thursday, August 28, 2008	Sheet 12 of 40	

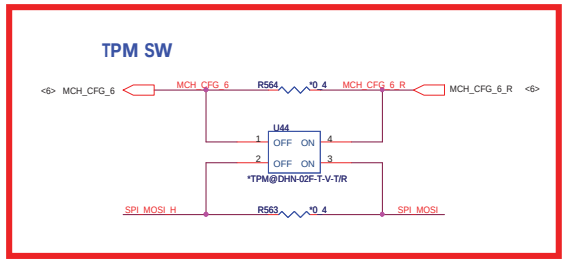


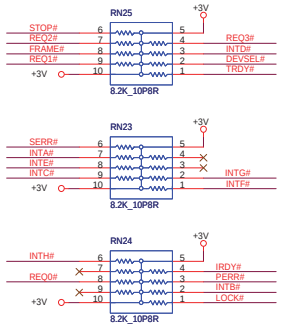
TM & AS	Y
LOW COST	N

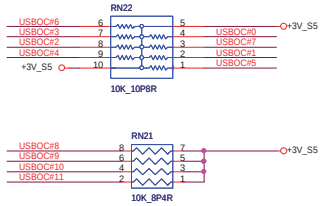




PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T





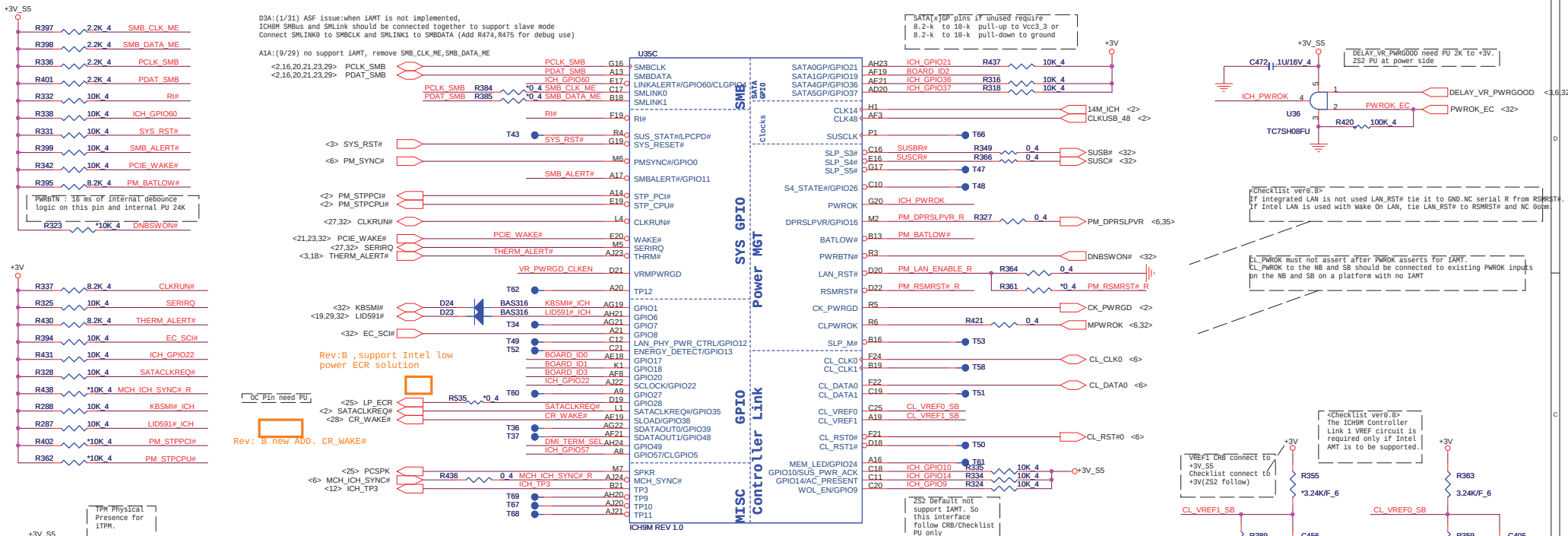


South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R347 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_H R329 *TPM@10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R344 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R340 *1K_4

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A
Date: Thursday, August 28, 2008	Sheet 13 of 40	



South Bridge Strap Pin (3/3)

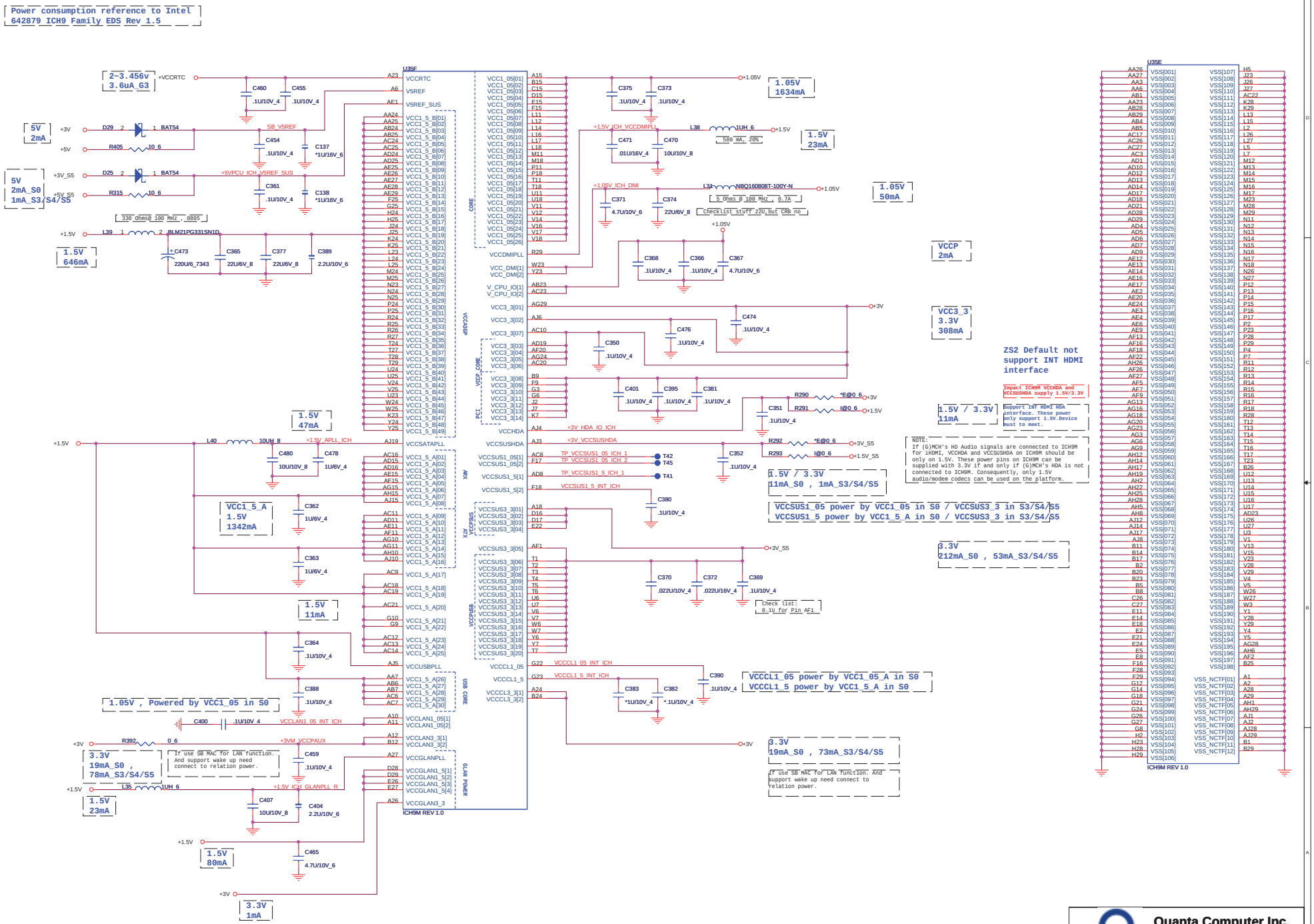
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R346 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R400 *1K_4

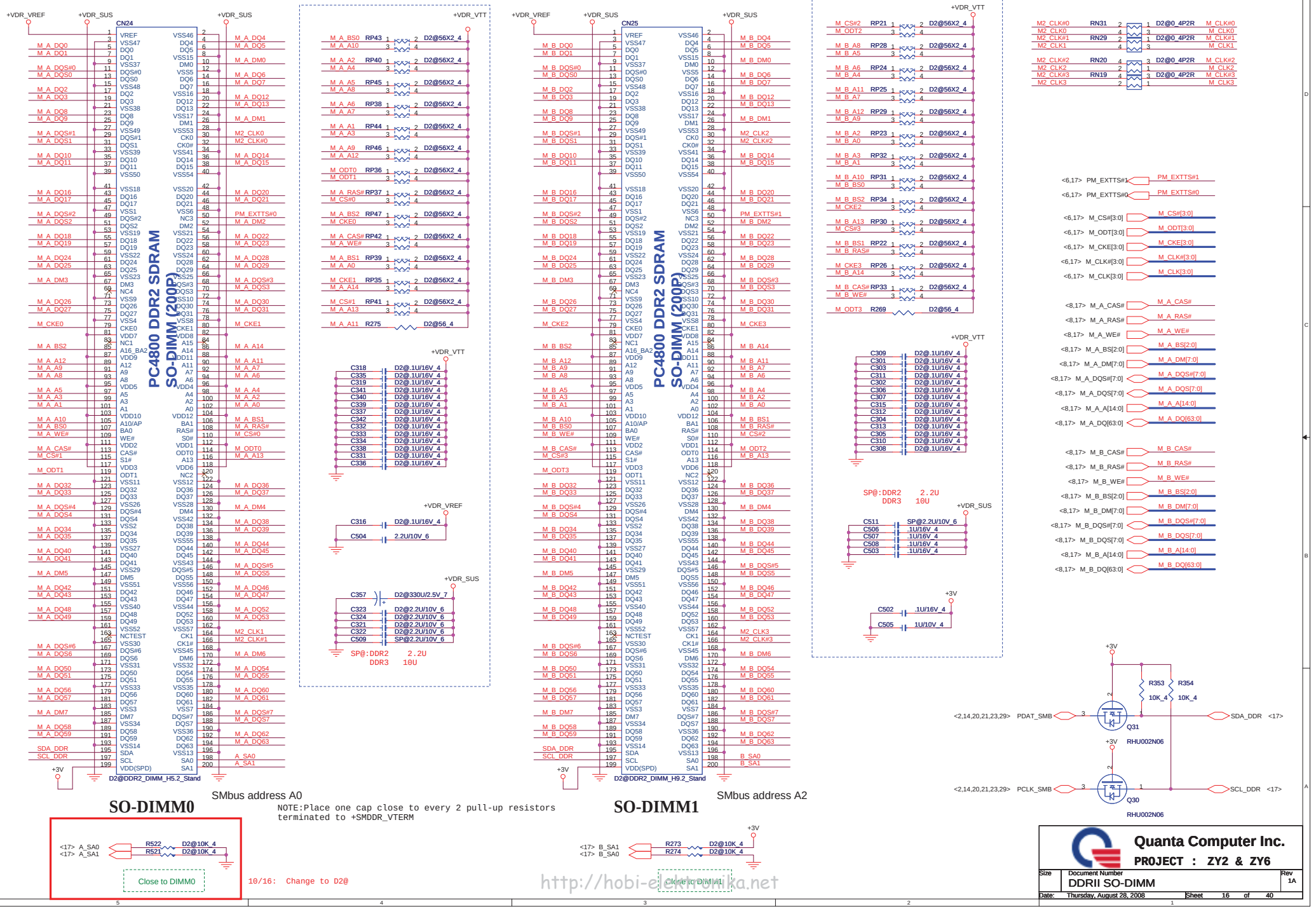
Board ID	ID3	ID2	ID1	ID0
ZY2	0	0	0	0
ZY6	0	0	1	0
ZY2 LOW COST	0	0	0	1
ZY6 LOW COST	0	0	1	1
ZY2 eMachine	0	1	0	0
ZY6 eMachine	0	1	1	0

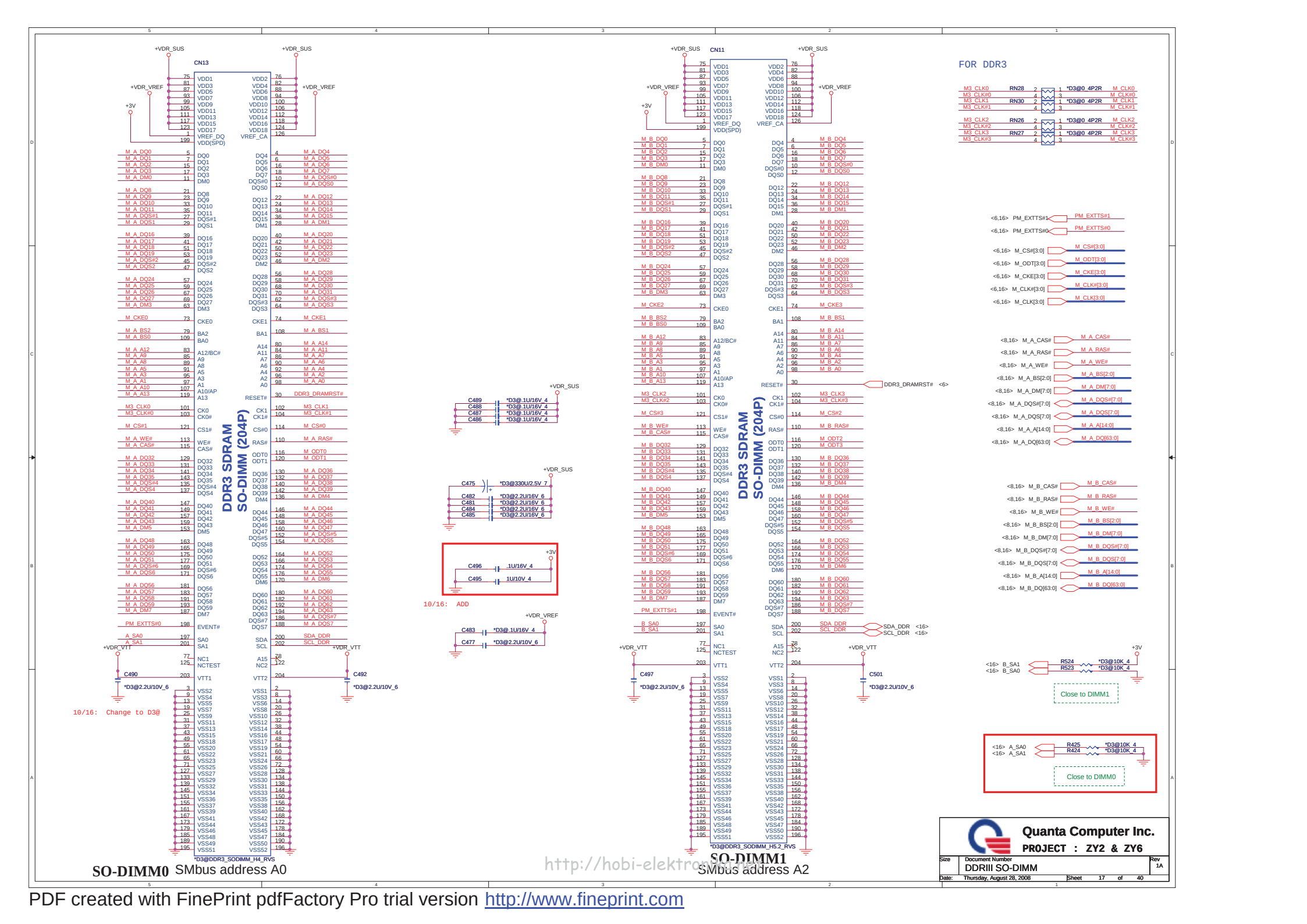
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

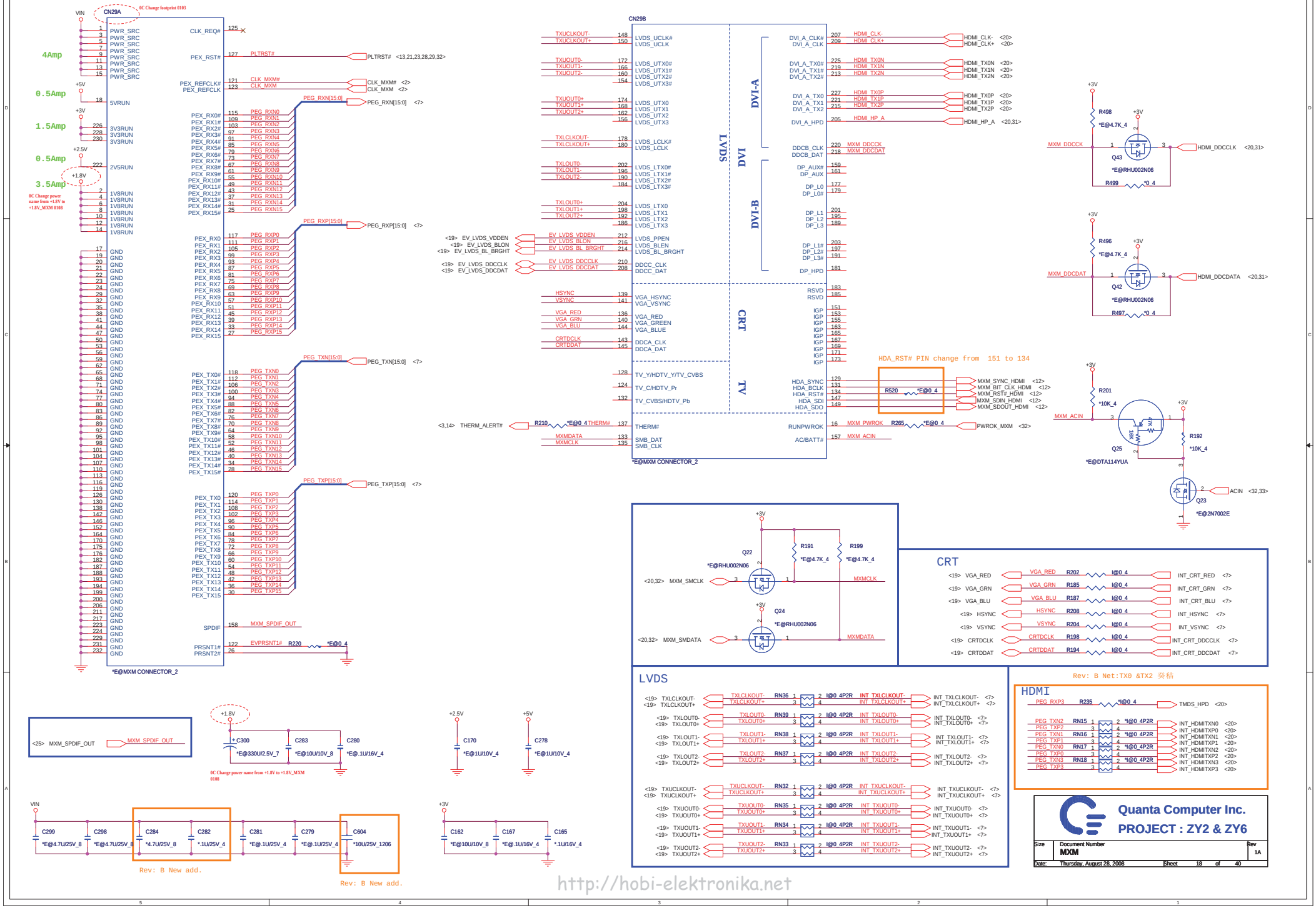
Size	Document Number	Rev
	ICH9M GPIO	1A

Date: Thursday, August 28, 2008 Sheet 14 of 40



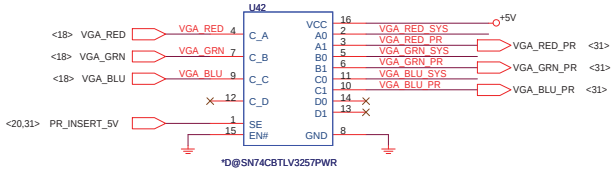


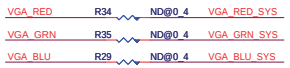




CRT Select

CRT SWITCH

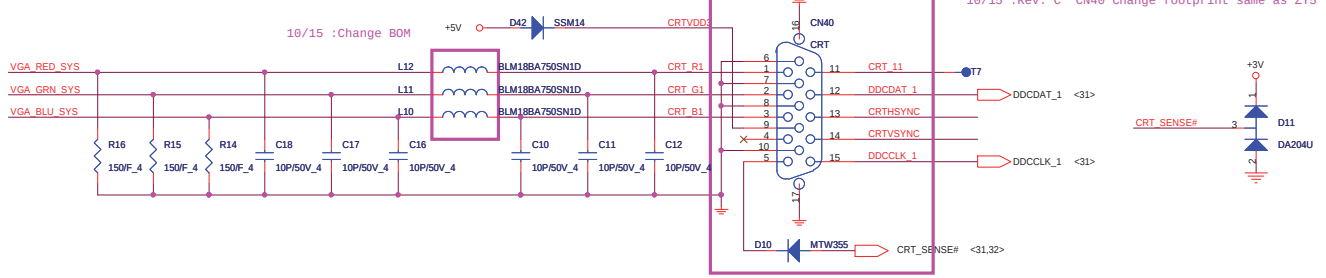


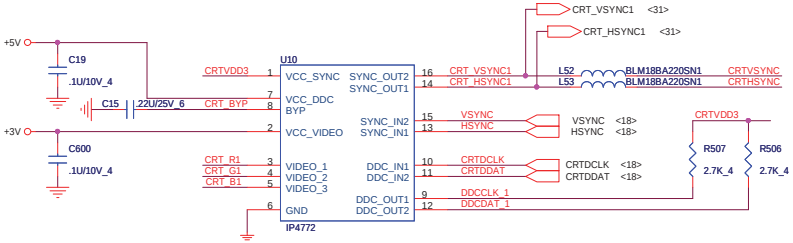


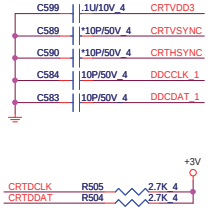
CRT CONNECTOR AND ESD

10/15 :Change BOM

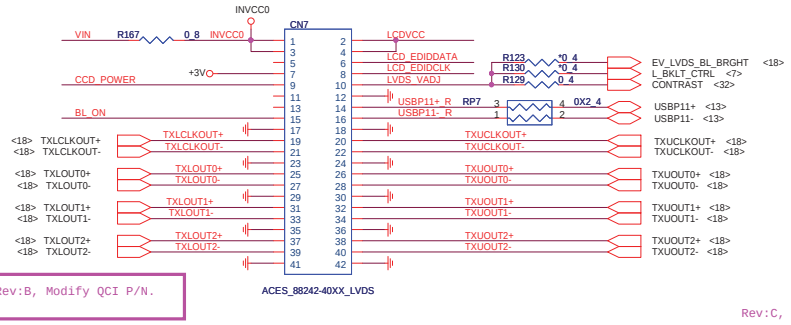
10/15 :Rev: C CN40 Change footprint same as ZY5

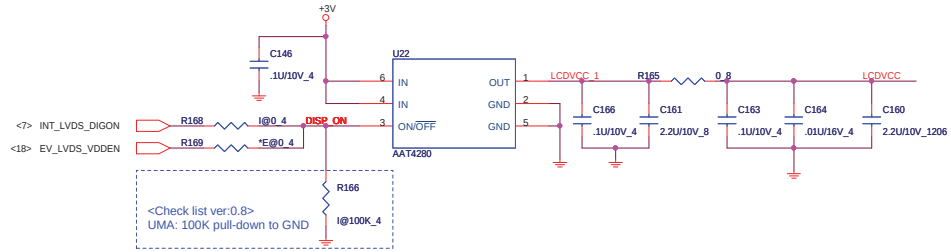


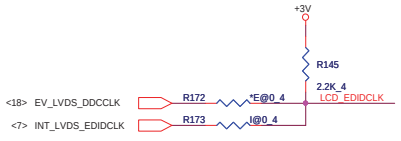




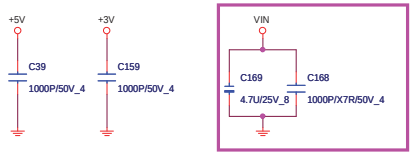
LVDS



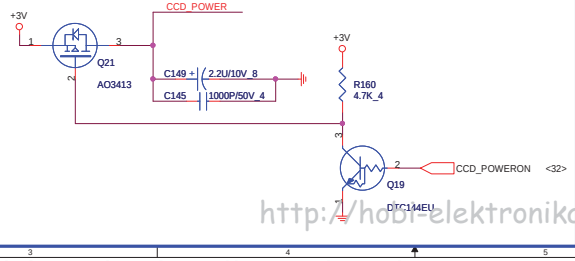




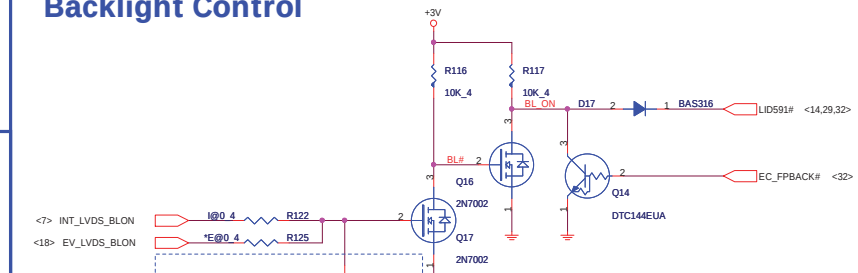
Rev:C, Change to 4.7U 0805



CAMERA MODULE CONNECTOR



Backlight Control



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CRT	1A
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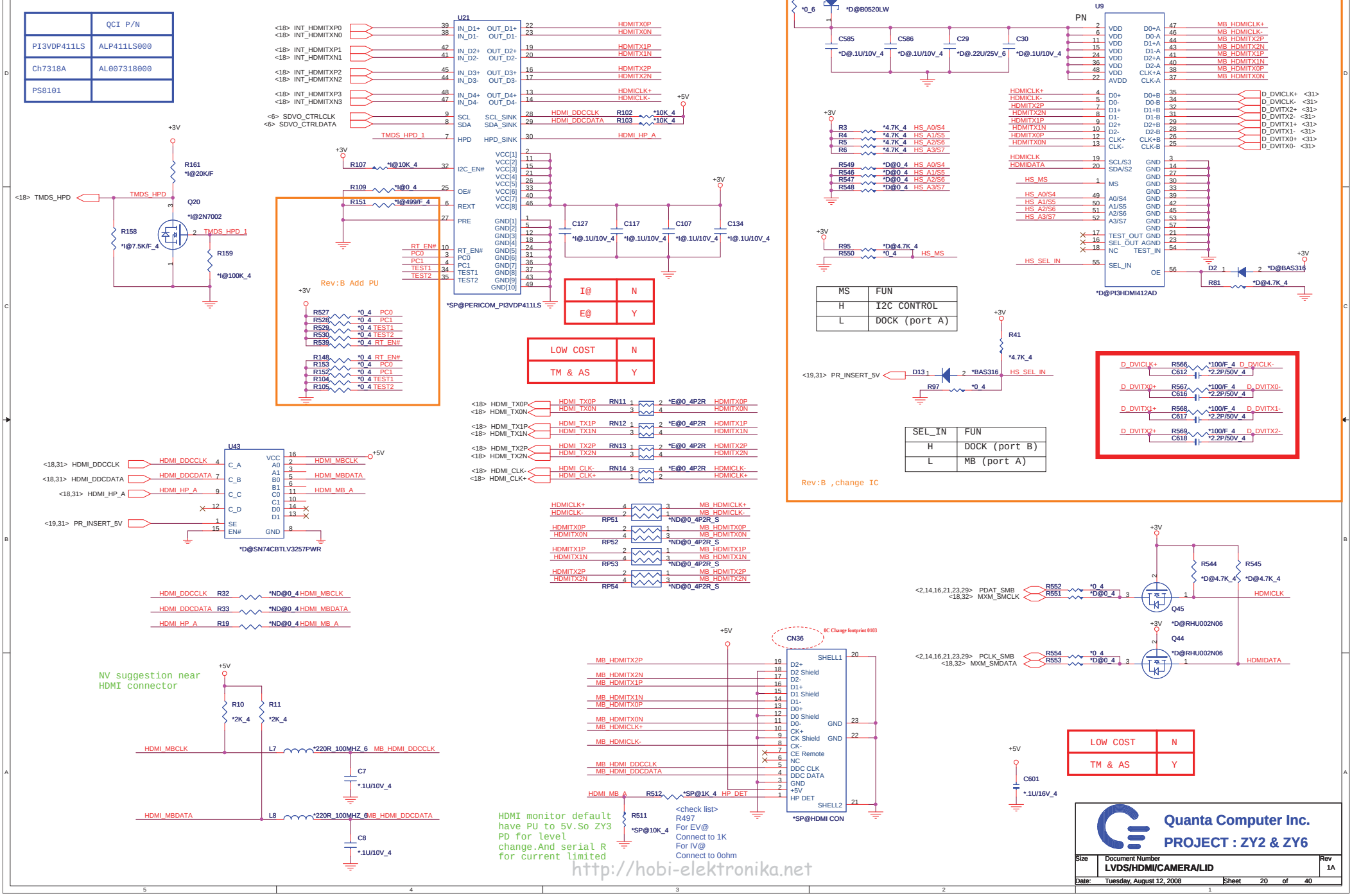
DVI-I CONNECTOR (DVI-D)

	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



I@	N
E@	Y

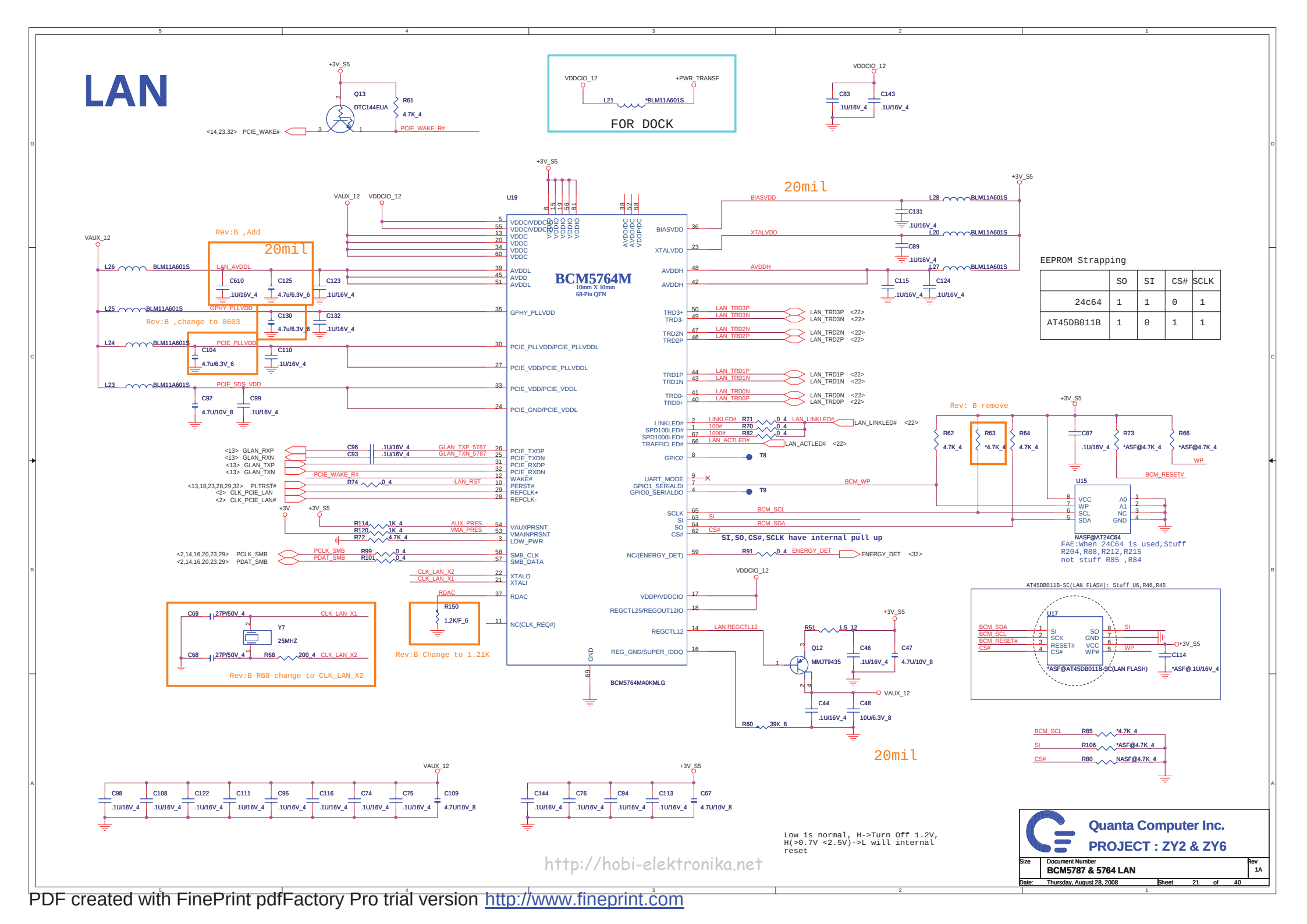
LOW COST	N
TM & AS	Y

MS	FUN
H	I2C CONTROL
L	DOCK (port A)

SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

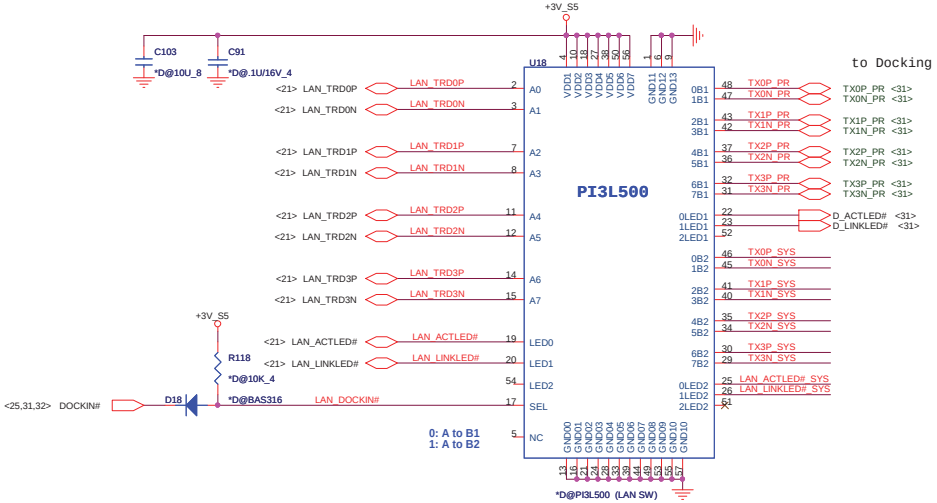
LOW COST	N
TM & AS	Y

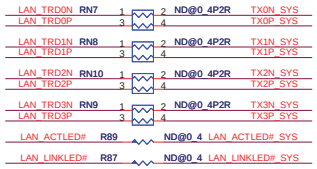
LAN



	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

LAN SWITCH

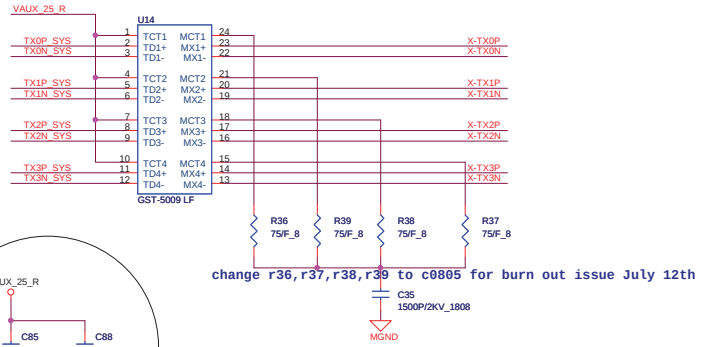


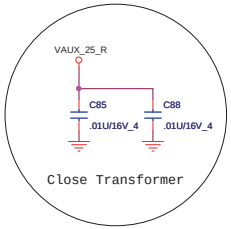


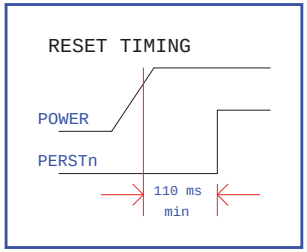
Transfomer

Source 1: DELTA LFE9249 DB0ZR1LAN11

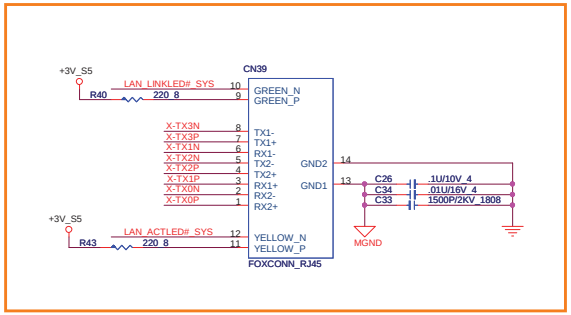
Source 2: Bothand GST5009 DBKN1NLAN03





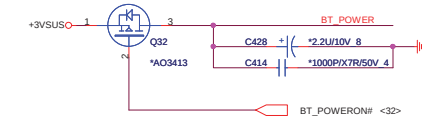


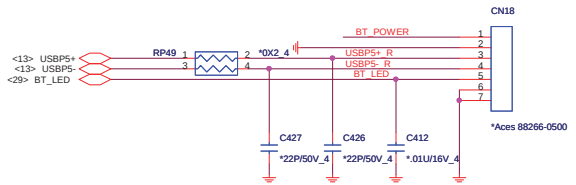
RJ45-11



9/29: change footprint
11/27 :change footprint
11/28 : R43 & R40 Change to 0805
1/31 :Rev: C change PIN define about 9,10,11 & 12

BLUETOOTH MODULE CONNECTOR





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	1A
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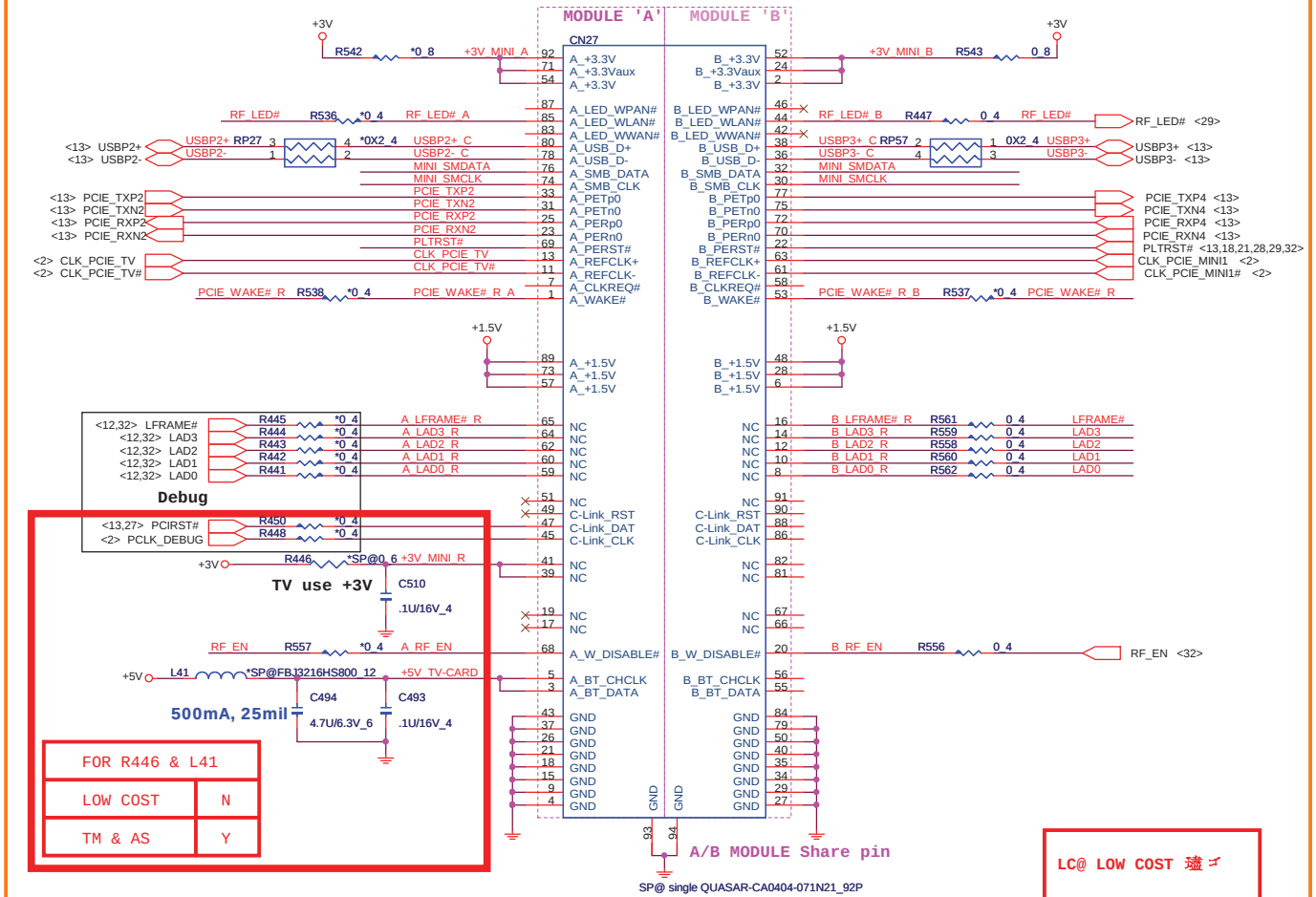
MINI-CARD

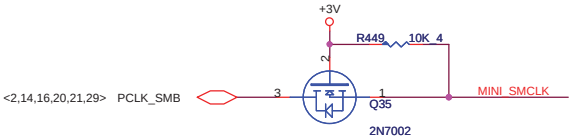
MODULE 'A' TV card

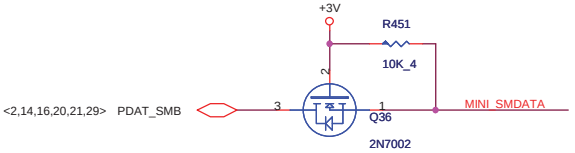
MODULE 'B' Wireless card

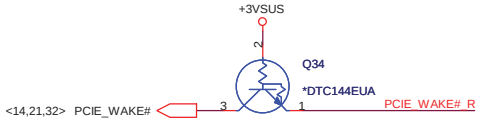
Double Stack MINI CARD

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

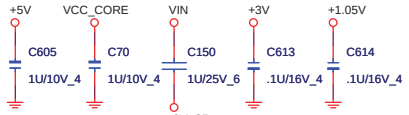


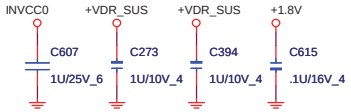




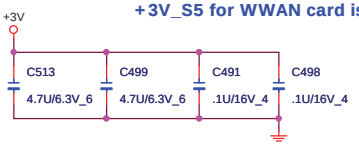


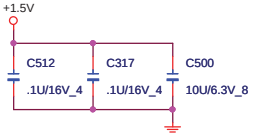
FOR EMI





+3V_S5 for WWAN card is 2.75A





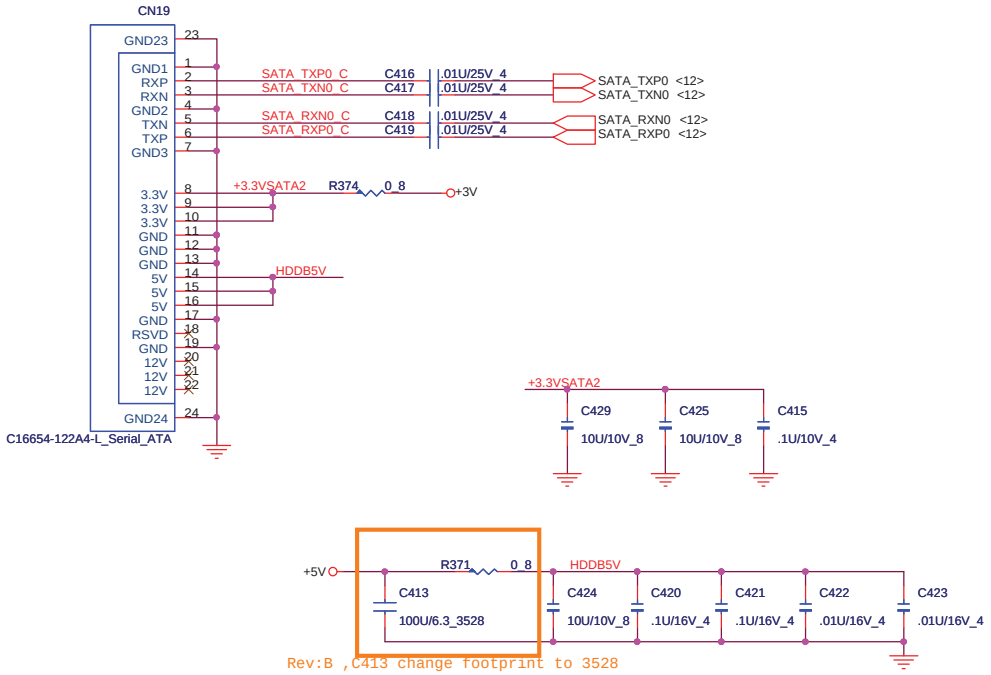
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	MINI PCI-E card/TV/TPM	1A
Date: Tuesday, August 12, 2008	Sheet 23 of 40	

SATA HDD

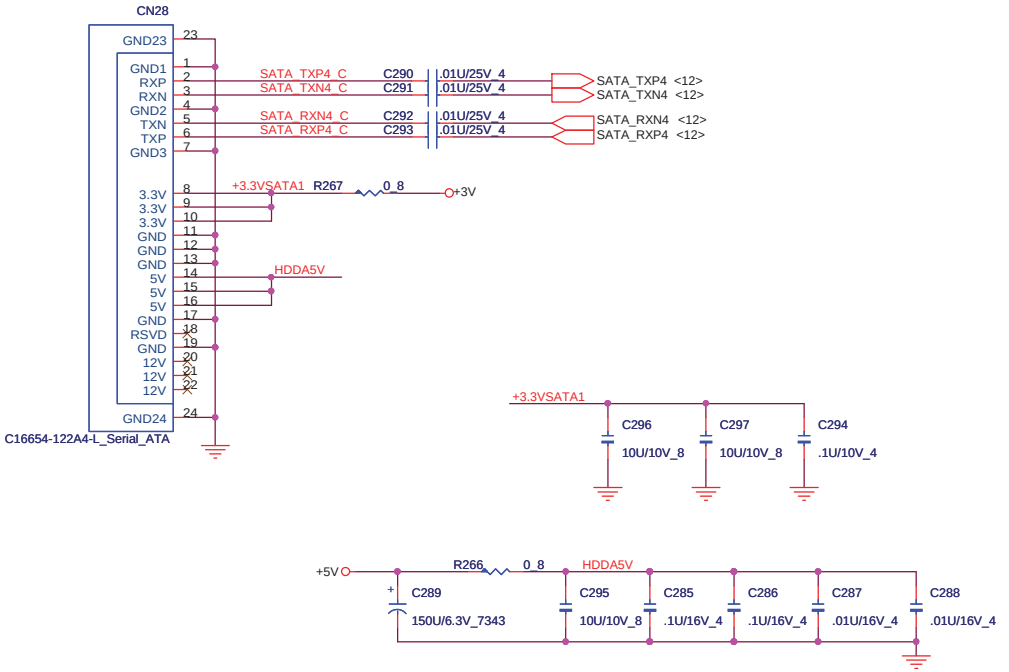
11/8 REV:B Conn. 奔癸秸 CN28 & CN19

Main

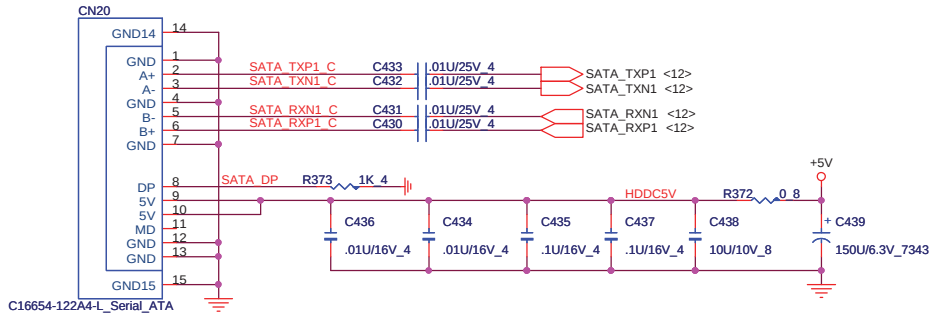


Rev:B ,C413 change footprint to 3528

2ND SATA HDD



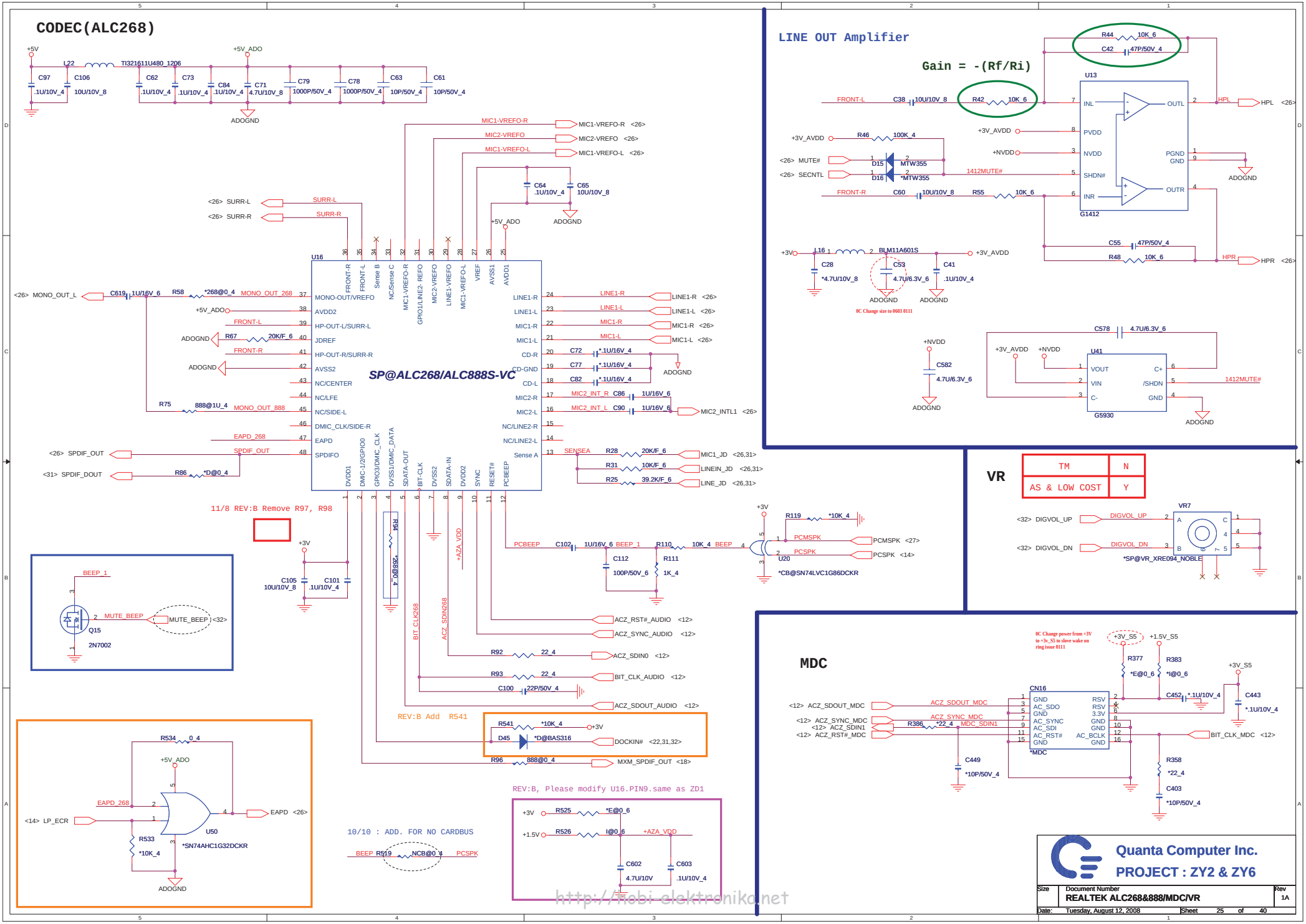
ODD (SATA)



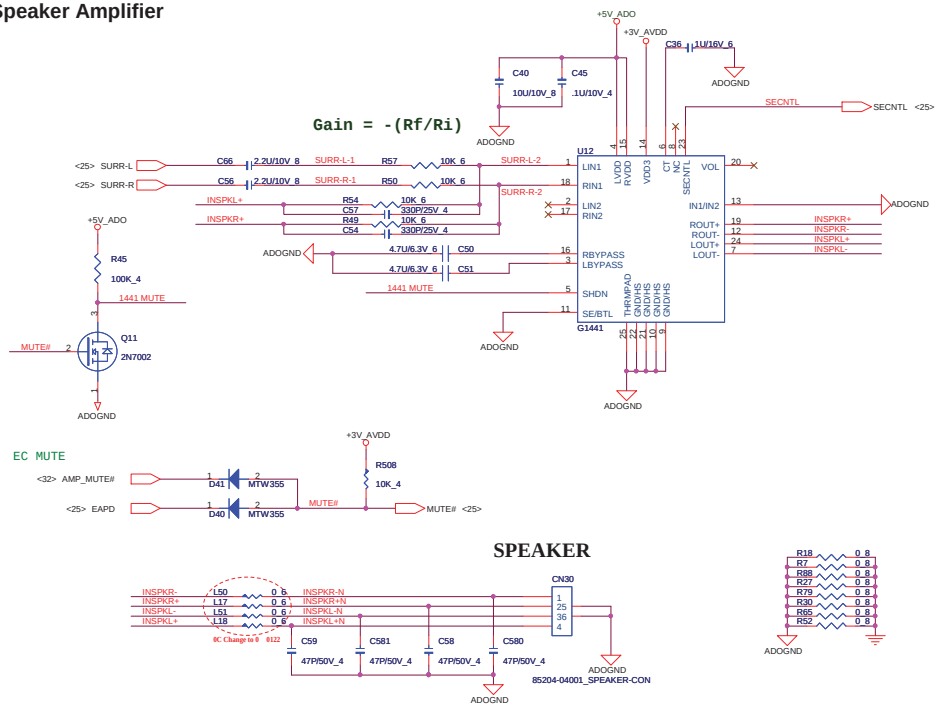
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

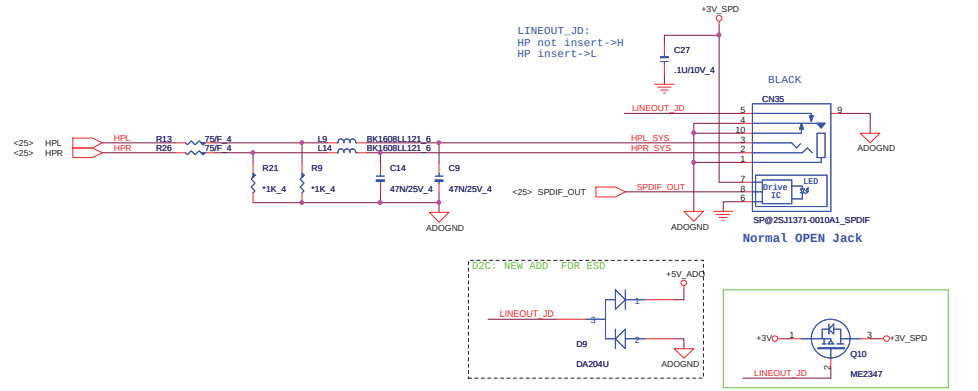
Size	Document Number	Rev
	SATA-HDD & ODD	1A
Date: Wednesday, August 13, 2008	Sheet 24 of 40	

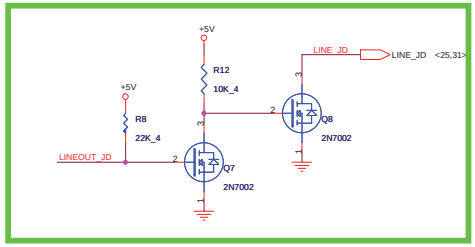


Speaker Amplifier

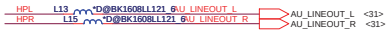


SYSTEM LINE OUT/SPDIF

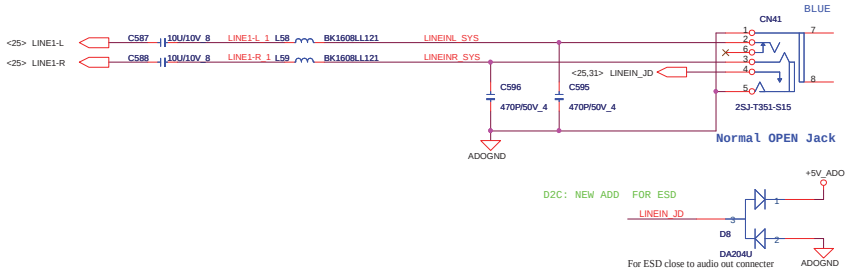


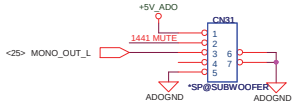


Docking LINE OUT/SPDIF



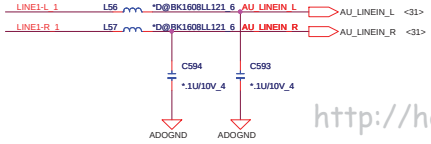
SYSTEM LINE IN/SUBWOOFER



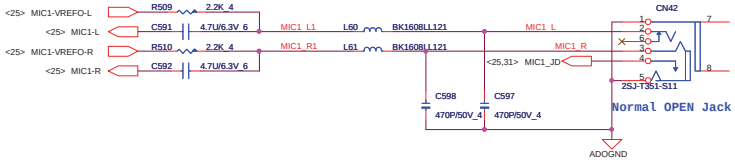


TM & LOW COST	N
AS	Y

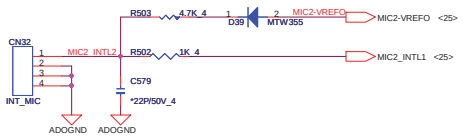
Docking LINE IN



MIC



INT MIC array



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
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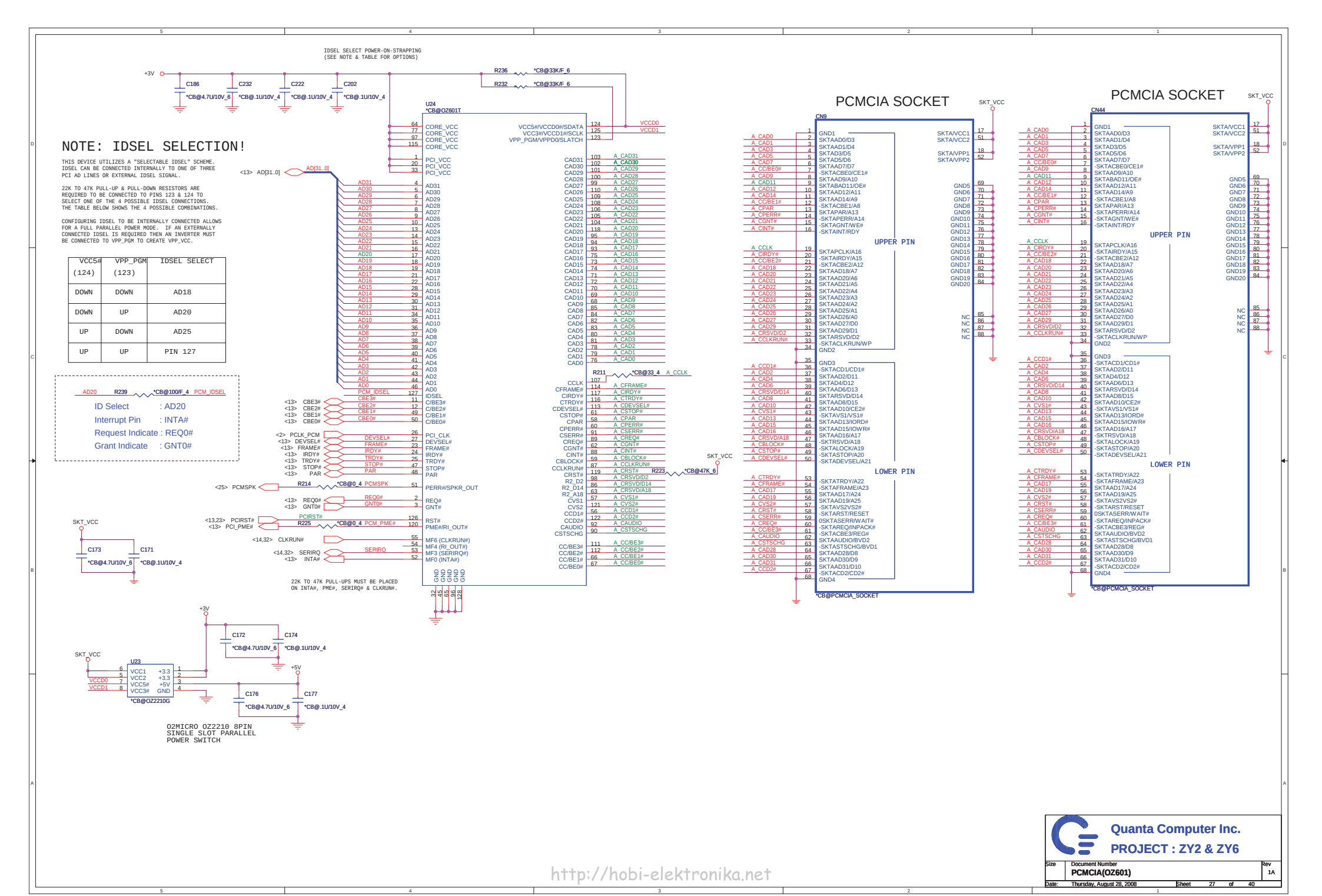
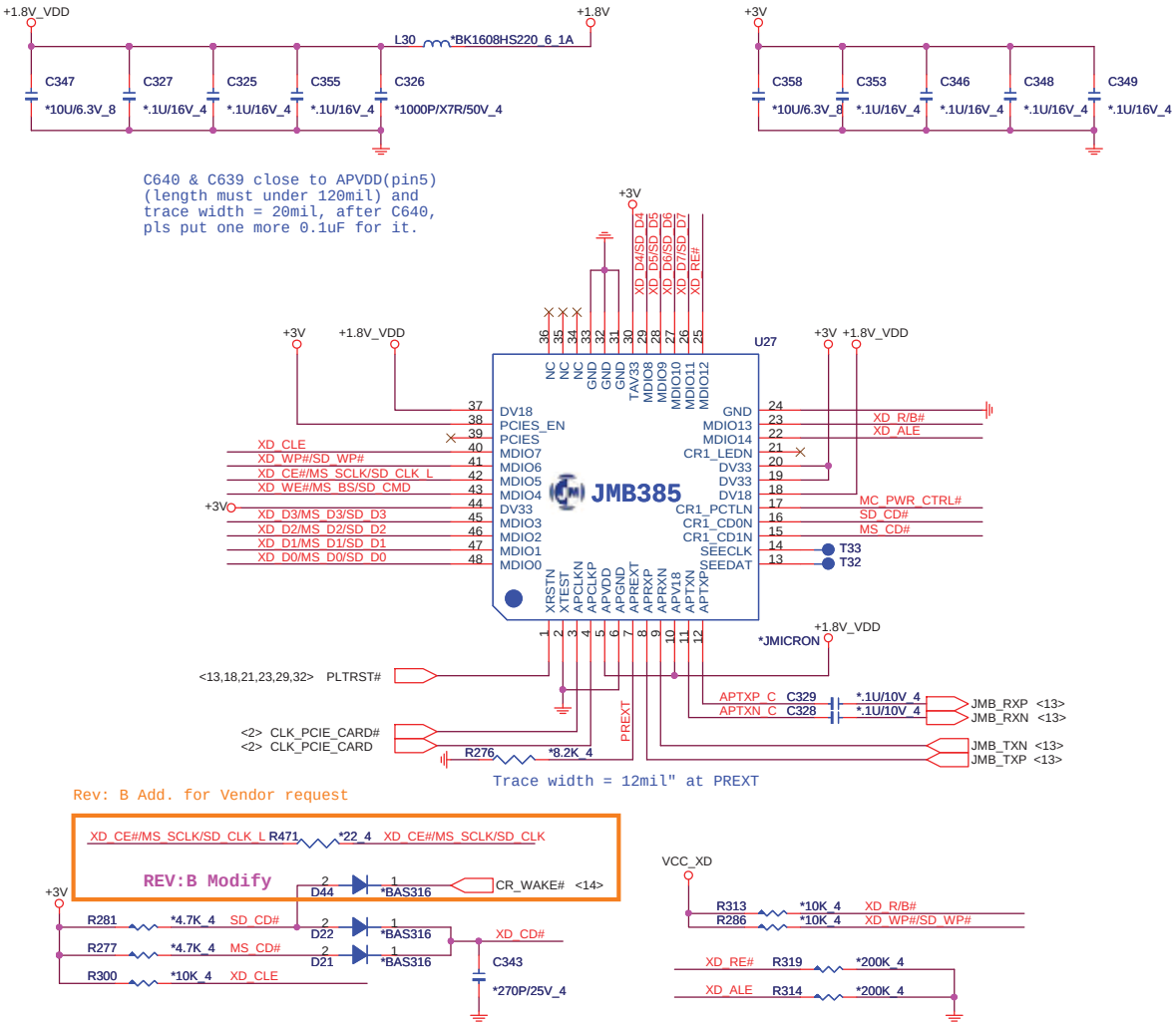
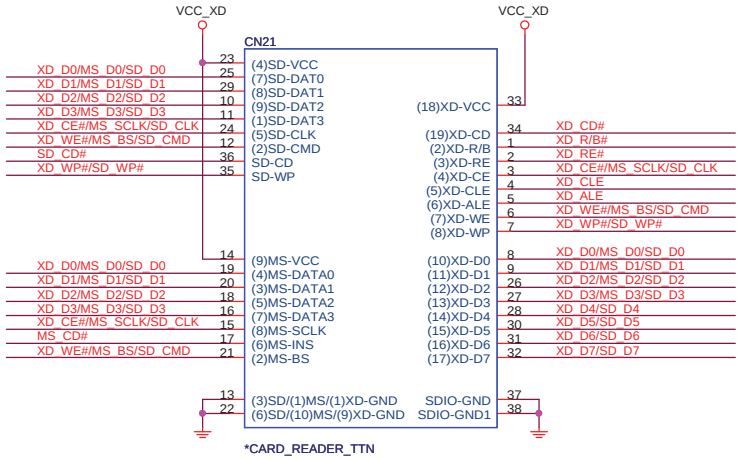
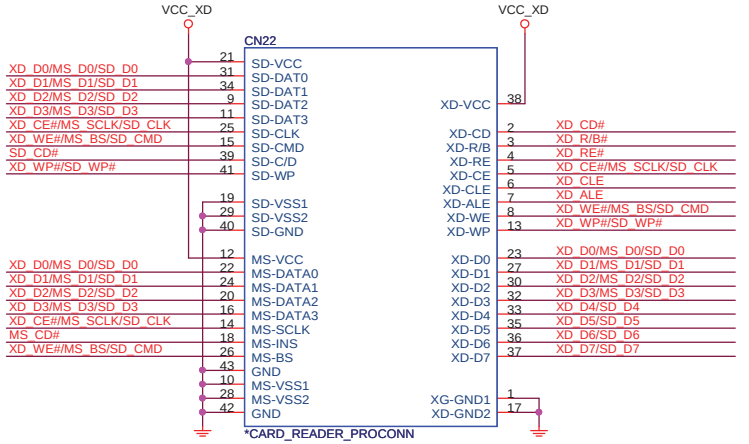


7 IN 1 CARD READER

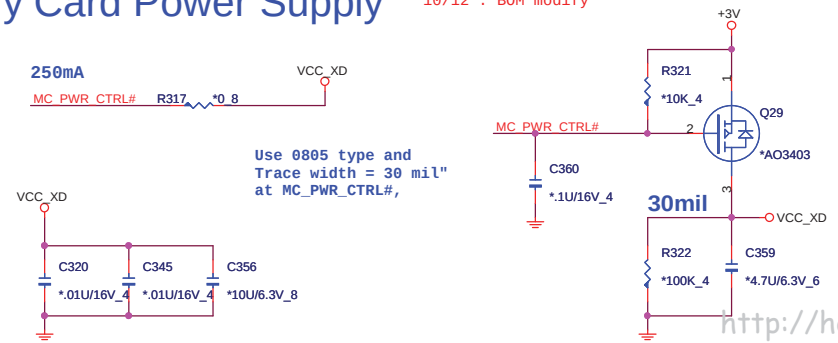






Memory Card Power Supply

10/12 : BOM modify



Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CARD READER JMB385	1A
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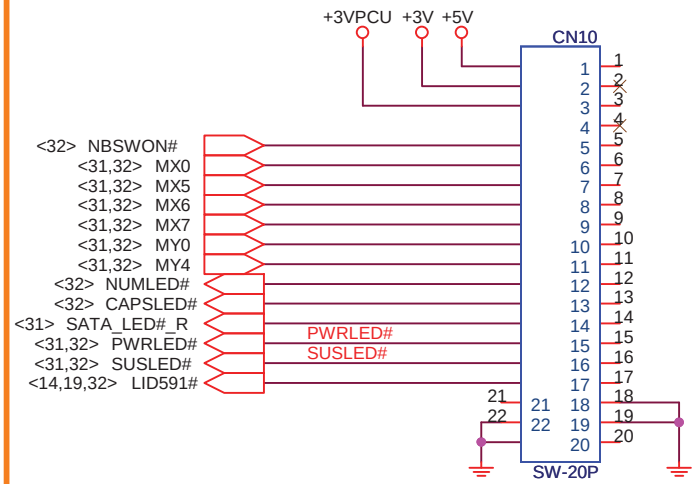
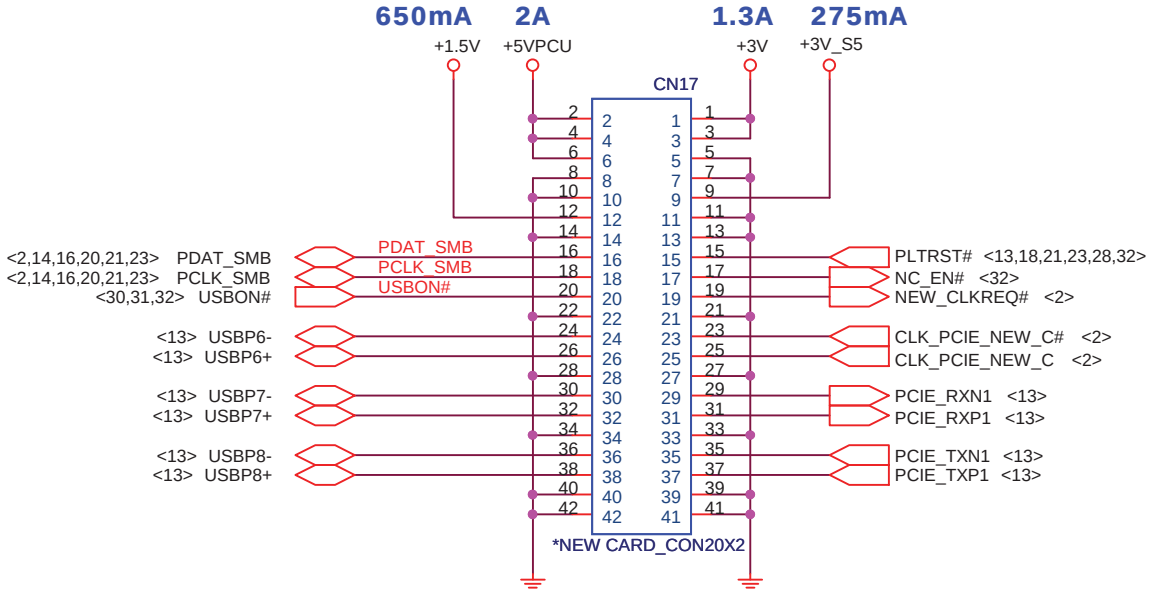
To NEW-CARD & EXT. USB

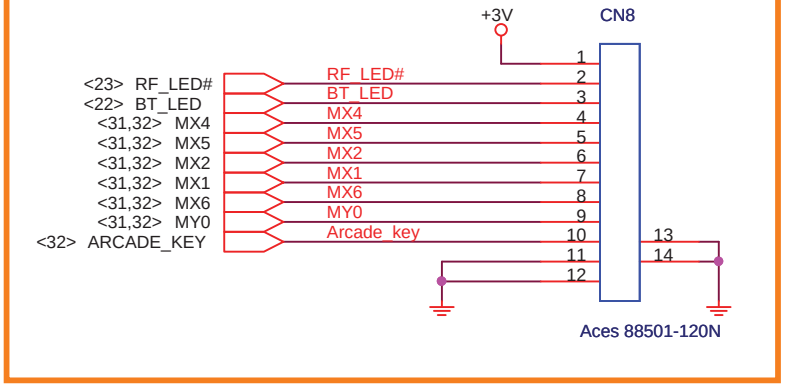
REV:B, CN10 change footprint

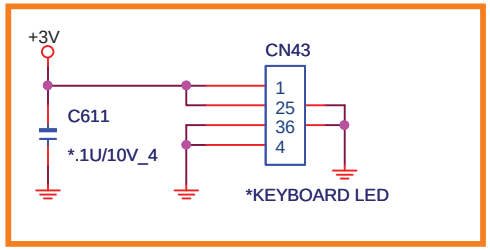


650mA 2A 1.3A 275mA



REV:B, Please change PIN define.same as ZY5
CN8 change footprint





Rev:B Add CN43 For backlight KB

Fnction	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4

Rev:B Change to 蛾 to よPAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395

Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	BTB CONN.	1A
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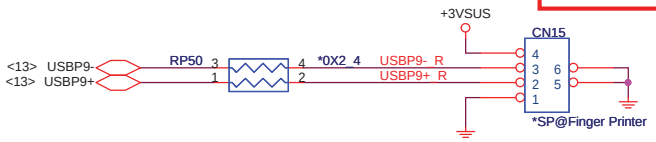
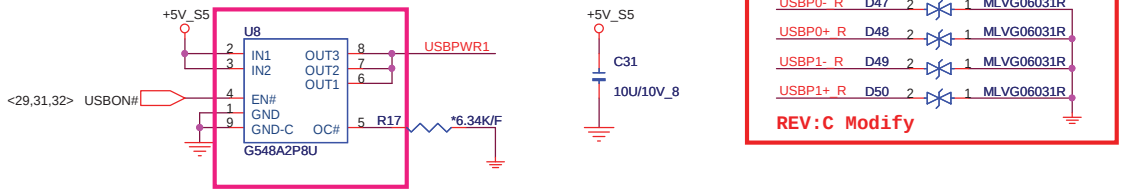
Finger Printer

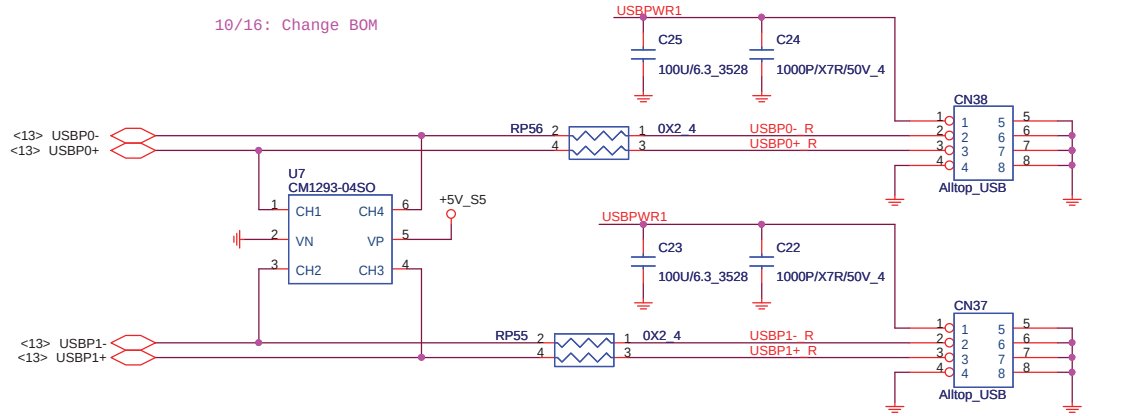
TM & AS	Y
LOW COST	N



USB

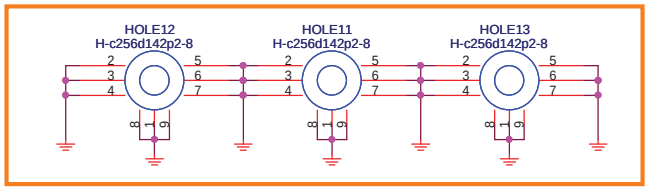


10/16: Change BOM

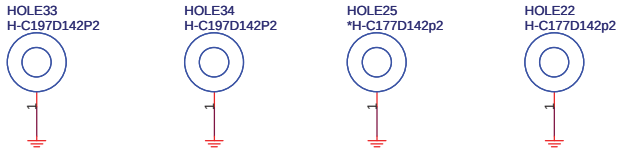


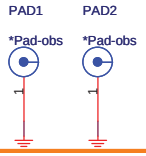
HOLES

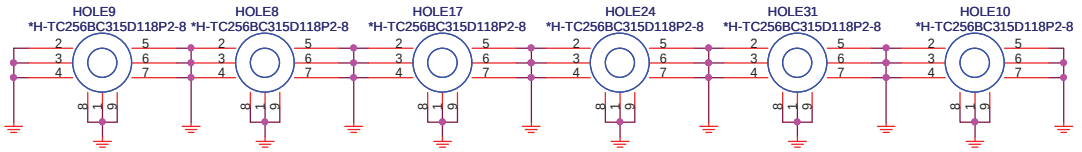
CPU NUT (BOT)



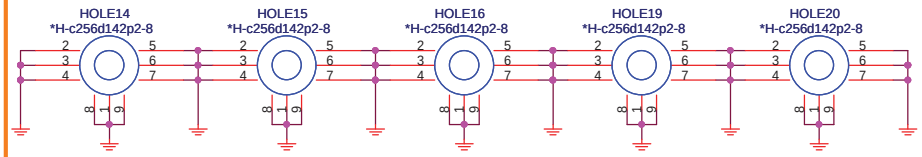
Rev : B Add MINI NUT

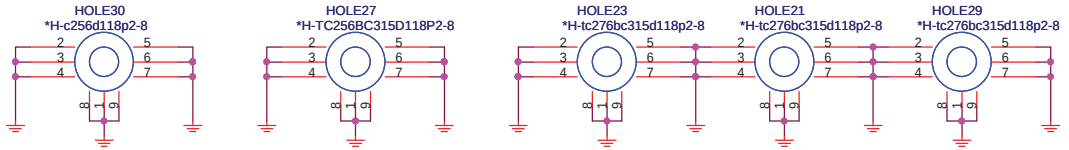




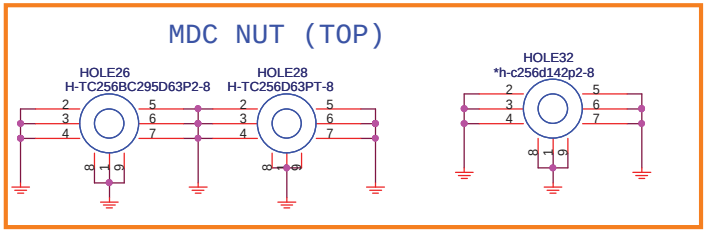


MXM NUT (BOT)

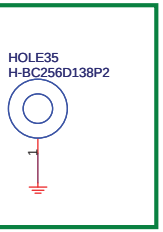




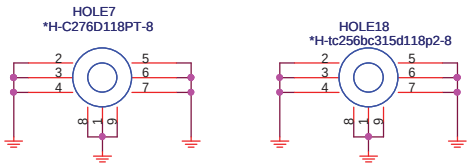
MDC NUT (TOP)



Rev:B New add HOLE32
HOLE26 & 28 Change footprint



HOLE35 瑞穌 BOT



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	USB/FINGER PRINTER	1A
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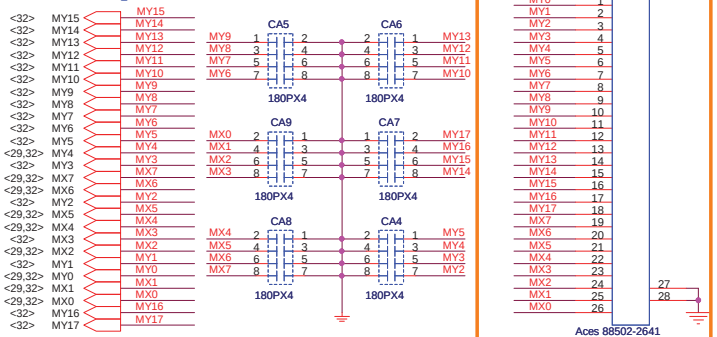
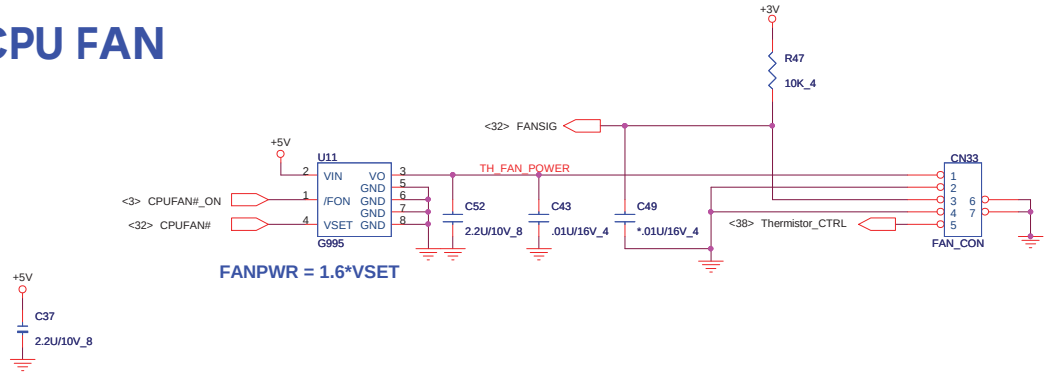
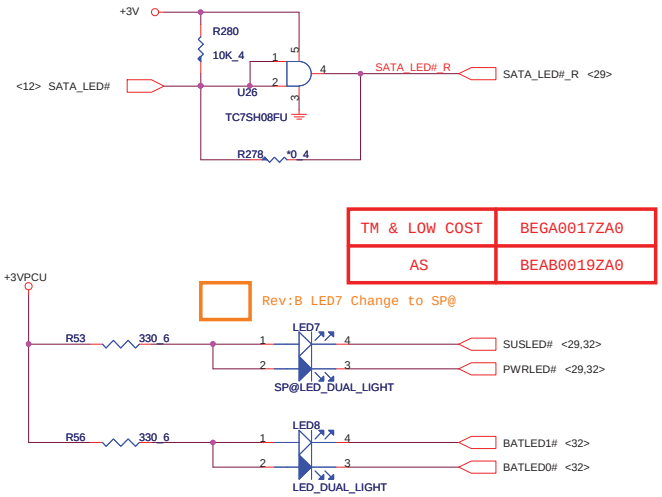
INT K/B



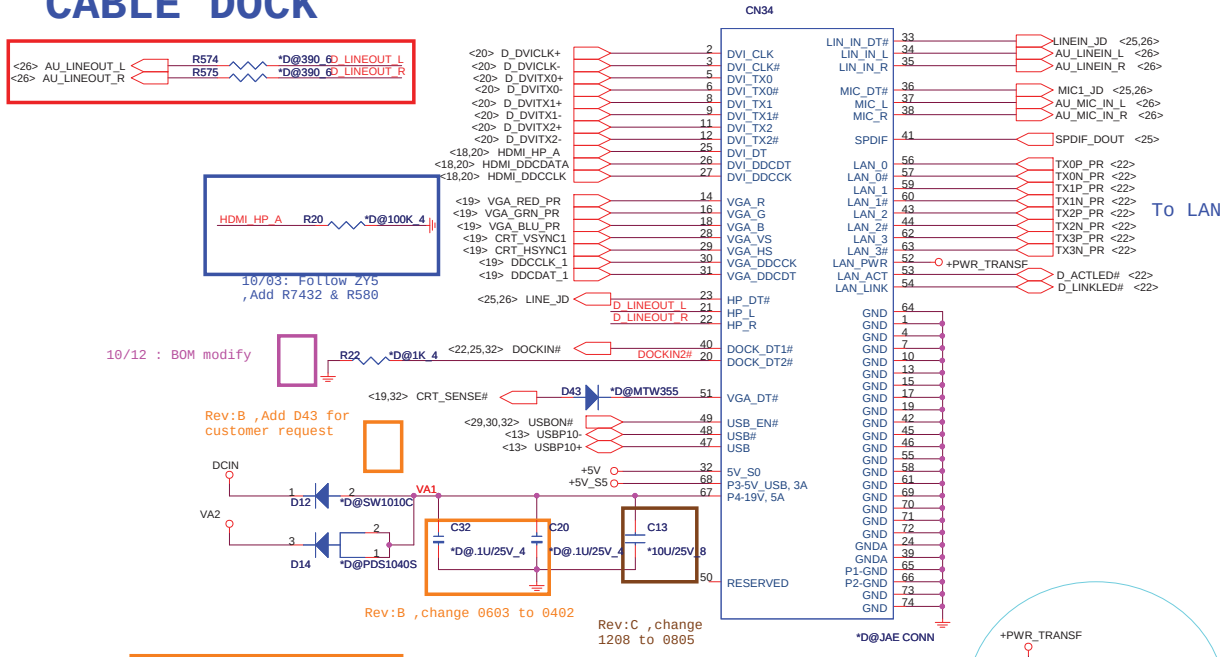
CPU FAN



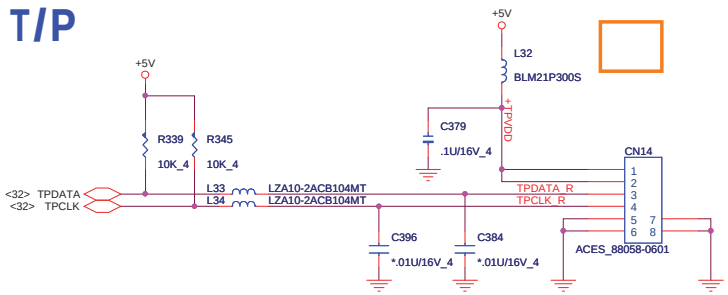
LED

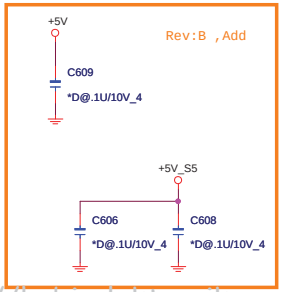


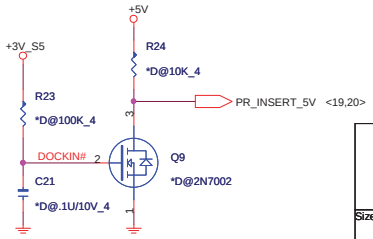
CABLE DOCK



T/P







Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	1A
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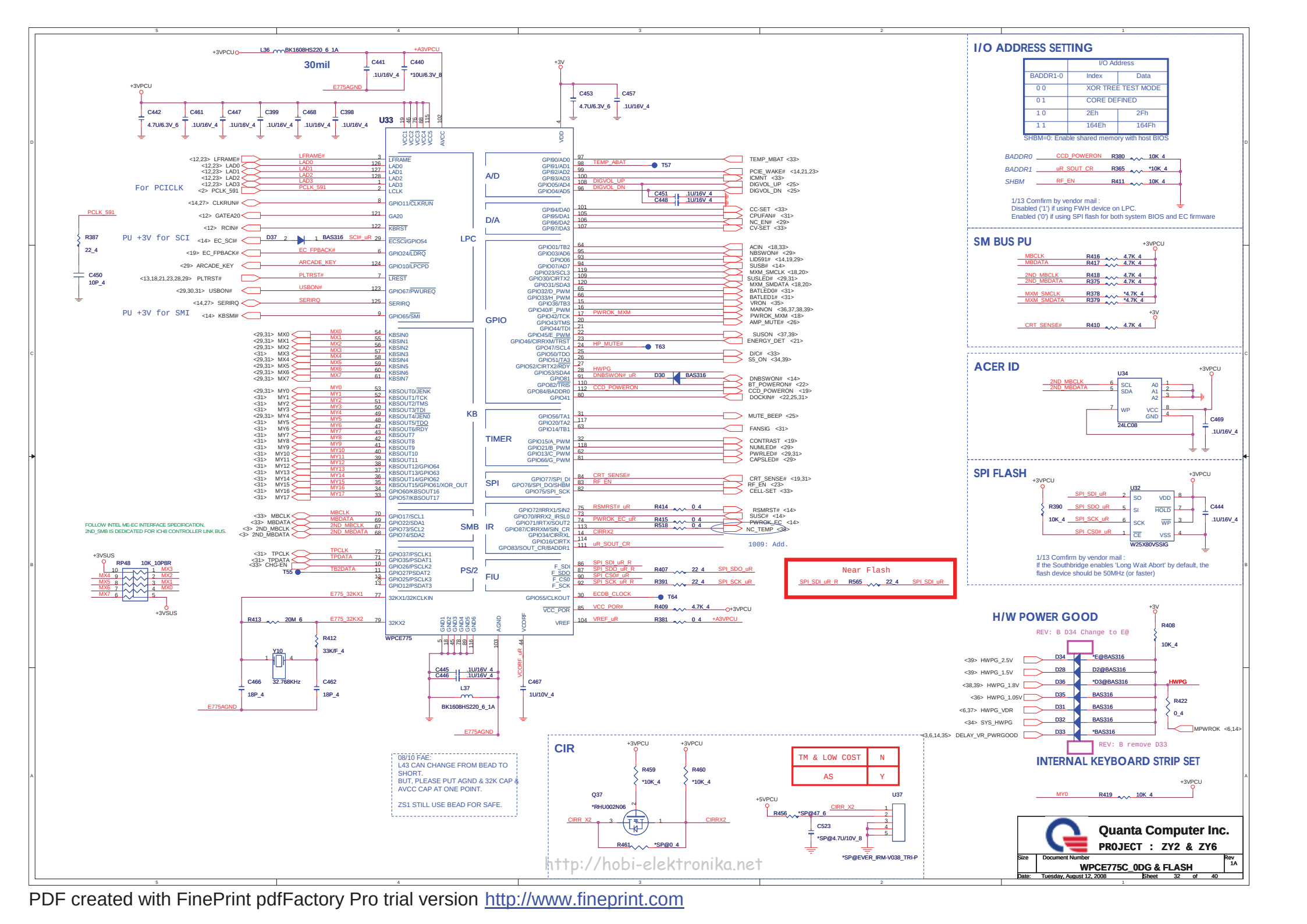

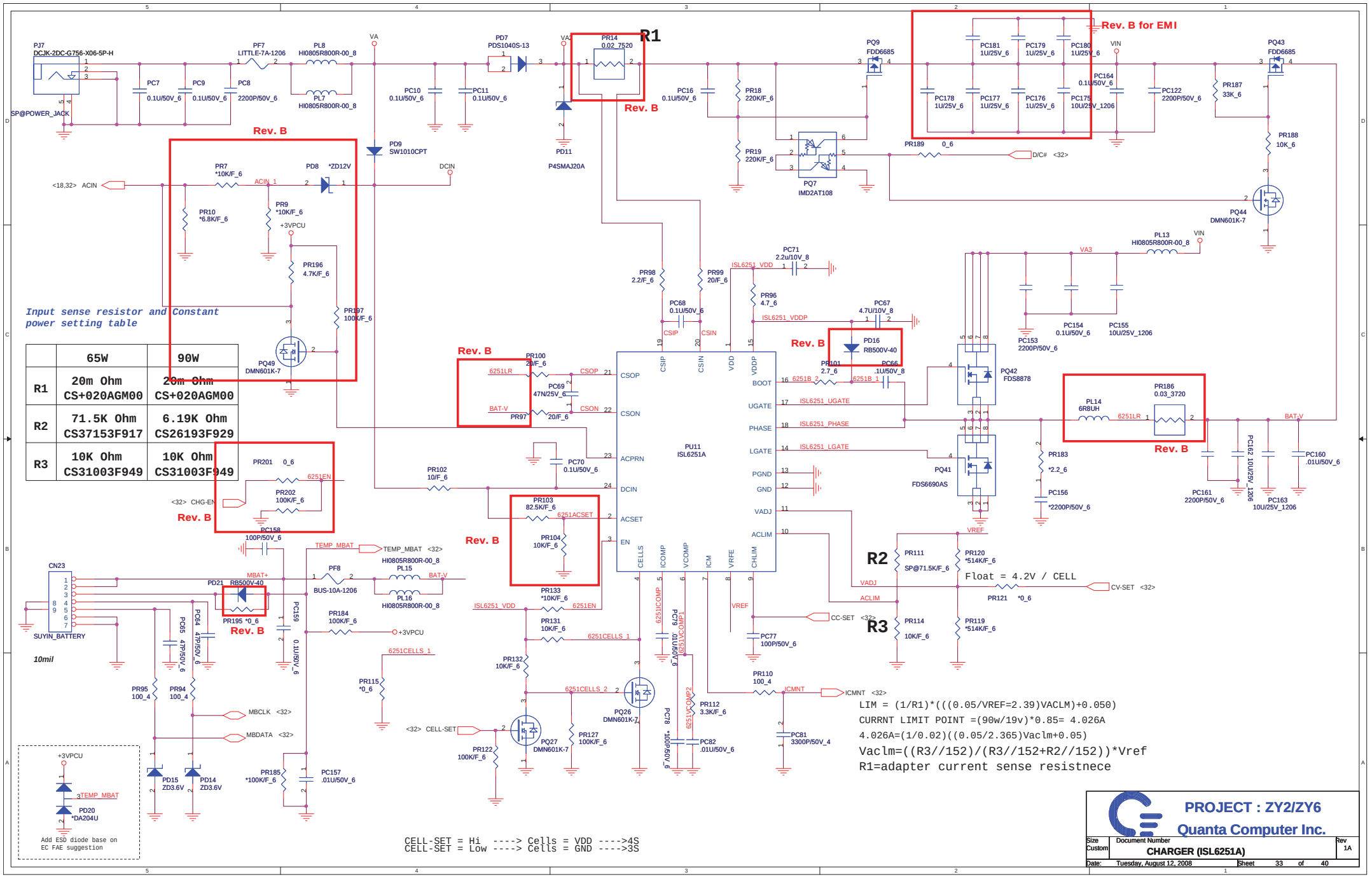

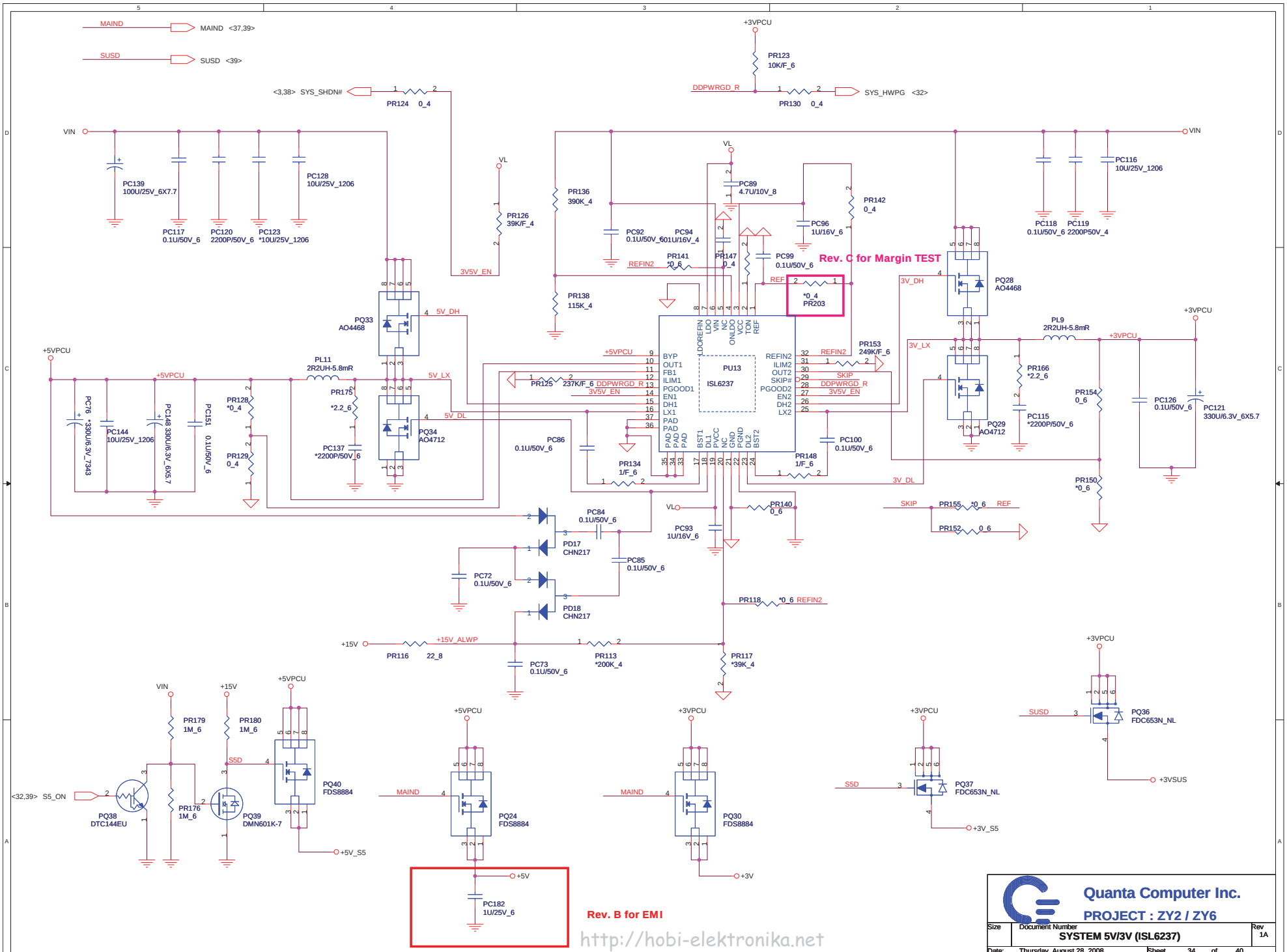

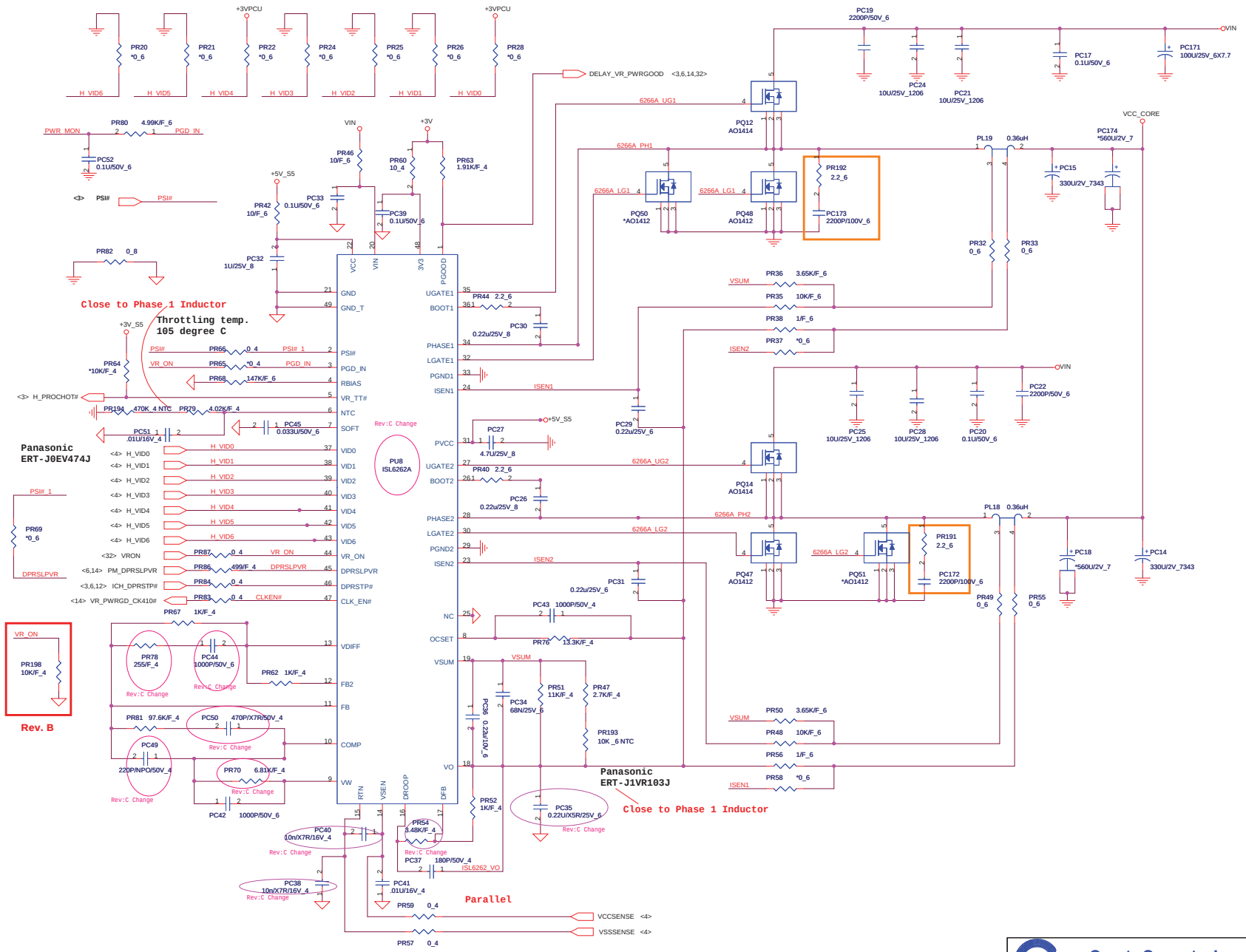

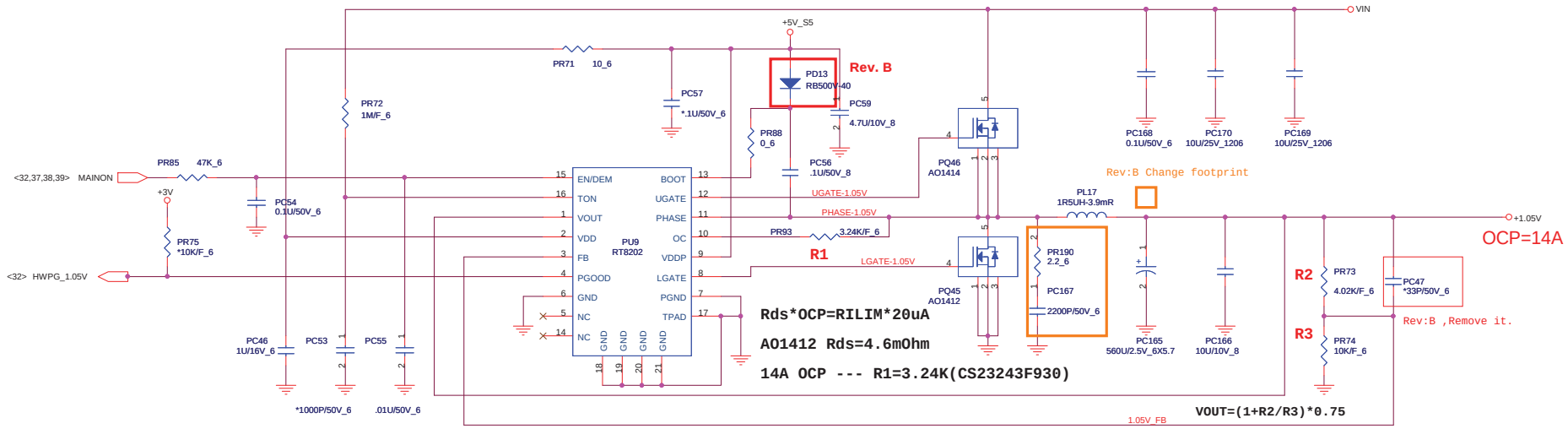

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.

PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A

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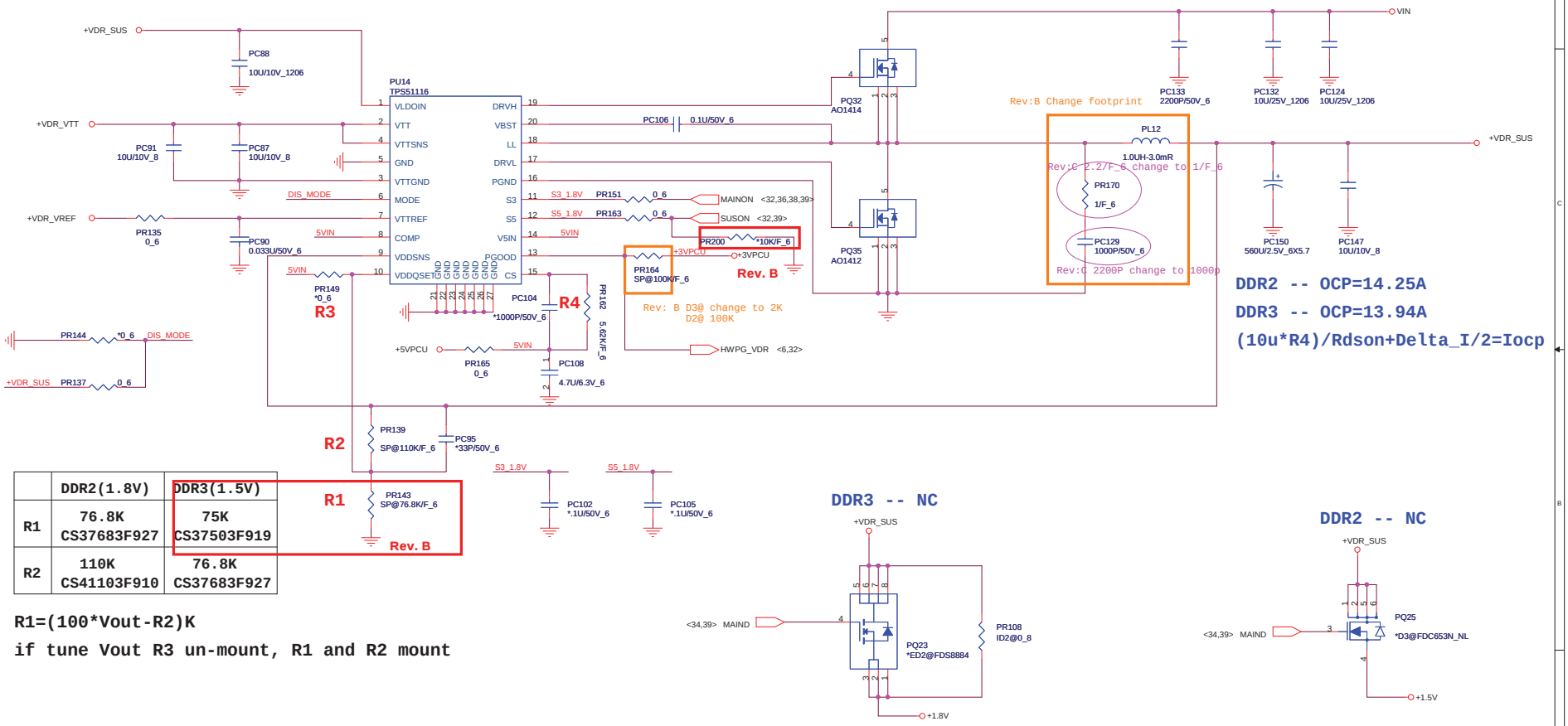

	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

R1=(100*Vout-R2)K

if tune Vout R3 un-mount, R1 and R2 mount

Quanta Computer Inc.		
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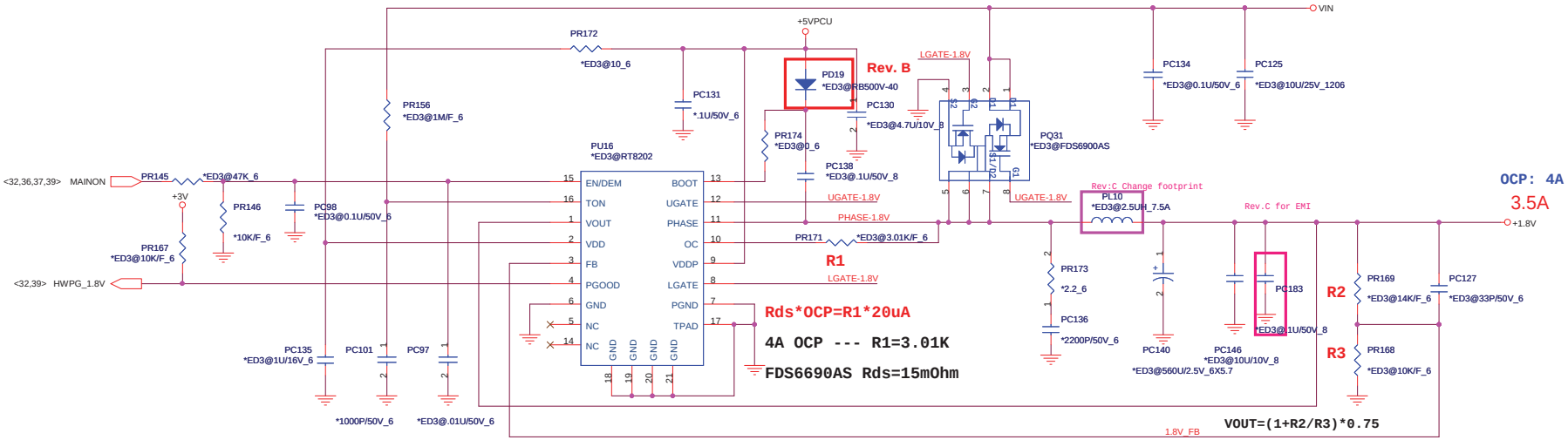
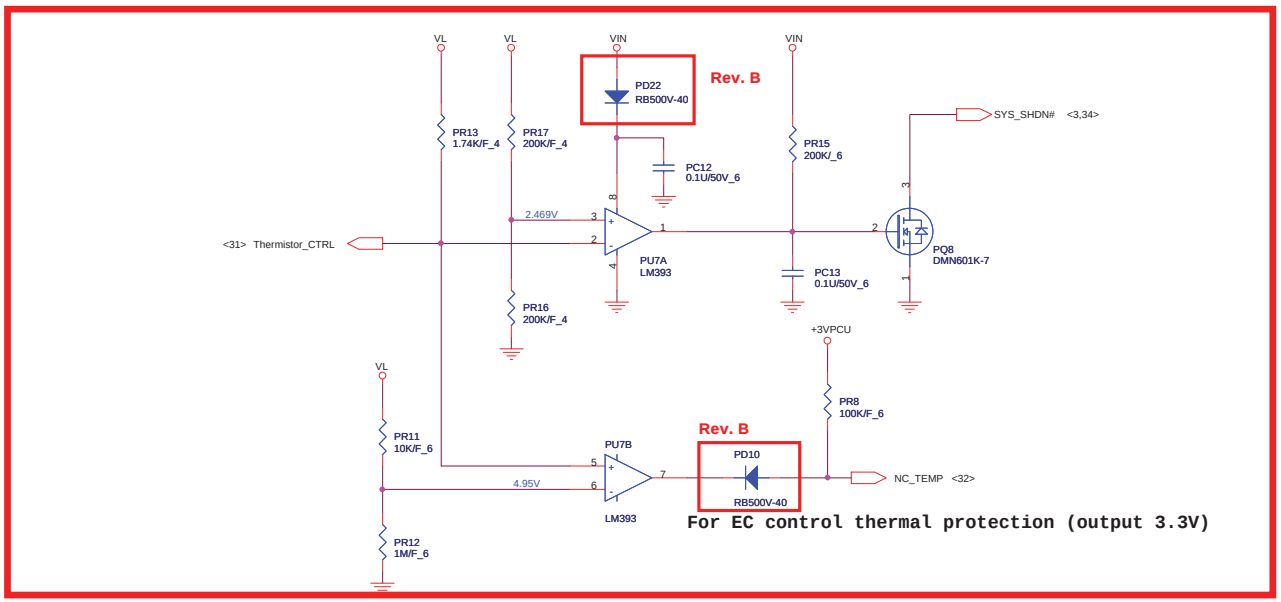


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

thermal protection --0928



Quanta Computer Inc.

PROJECT : ZY2 / ZY6

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	1.8V (RT8202)	1A
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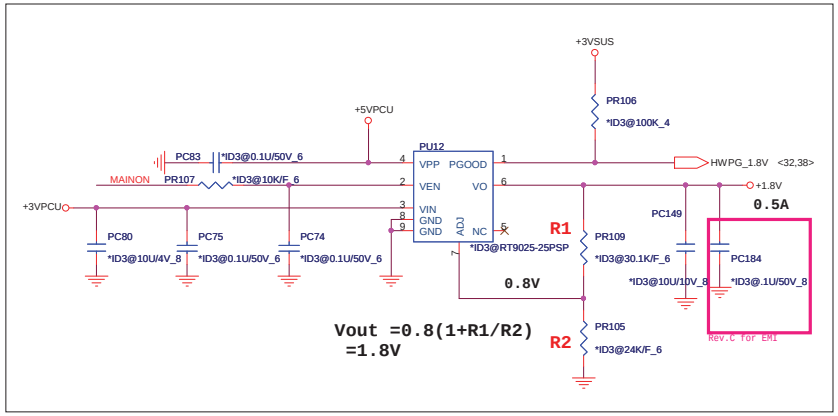
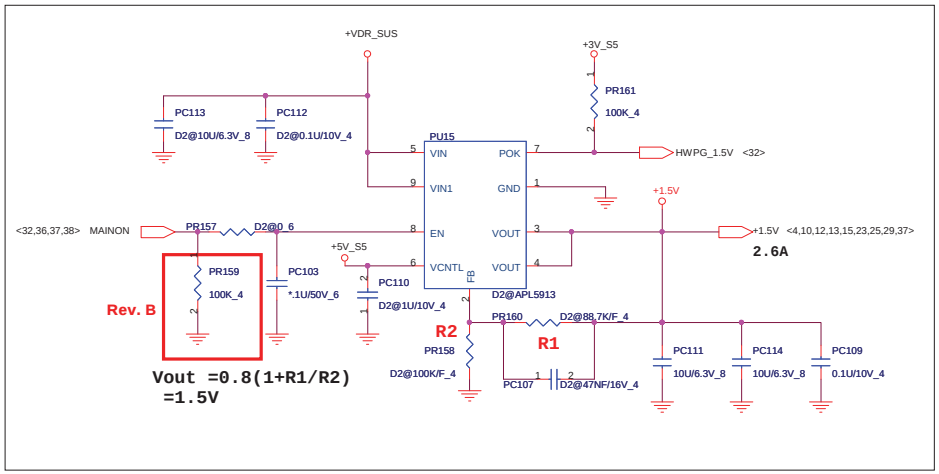
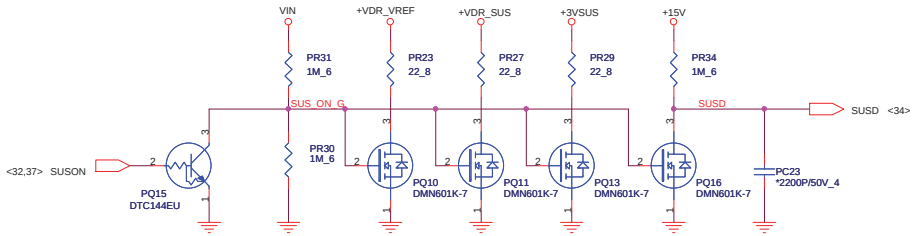
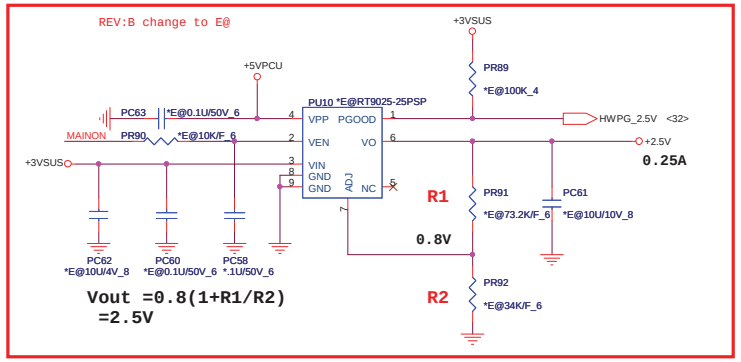
for DDR3 and UMA

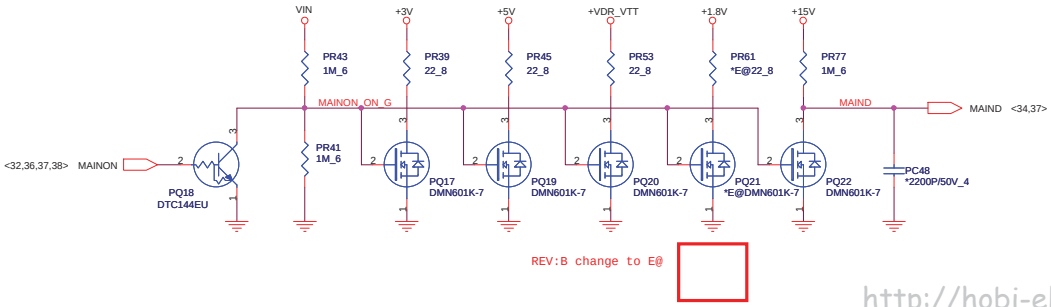


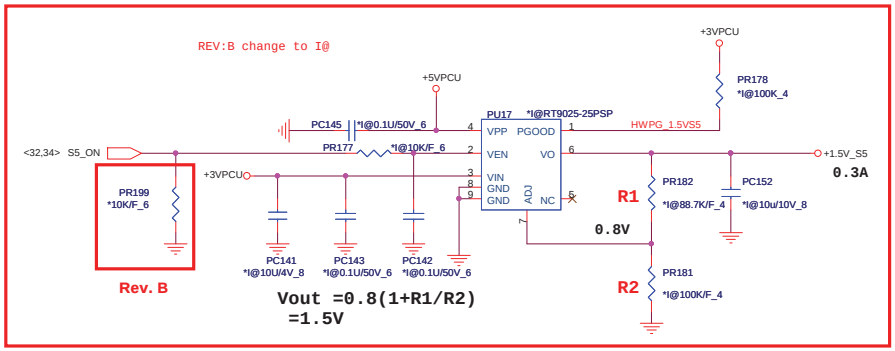
DDR3 -- NC











Quanta Computer Inc.
PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A
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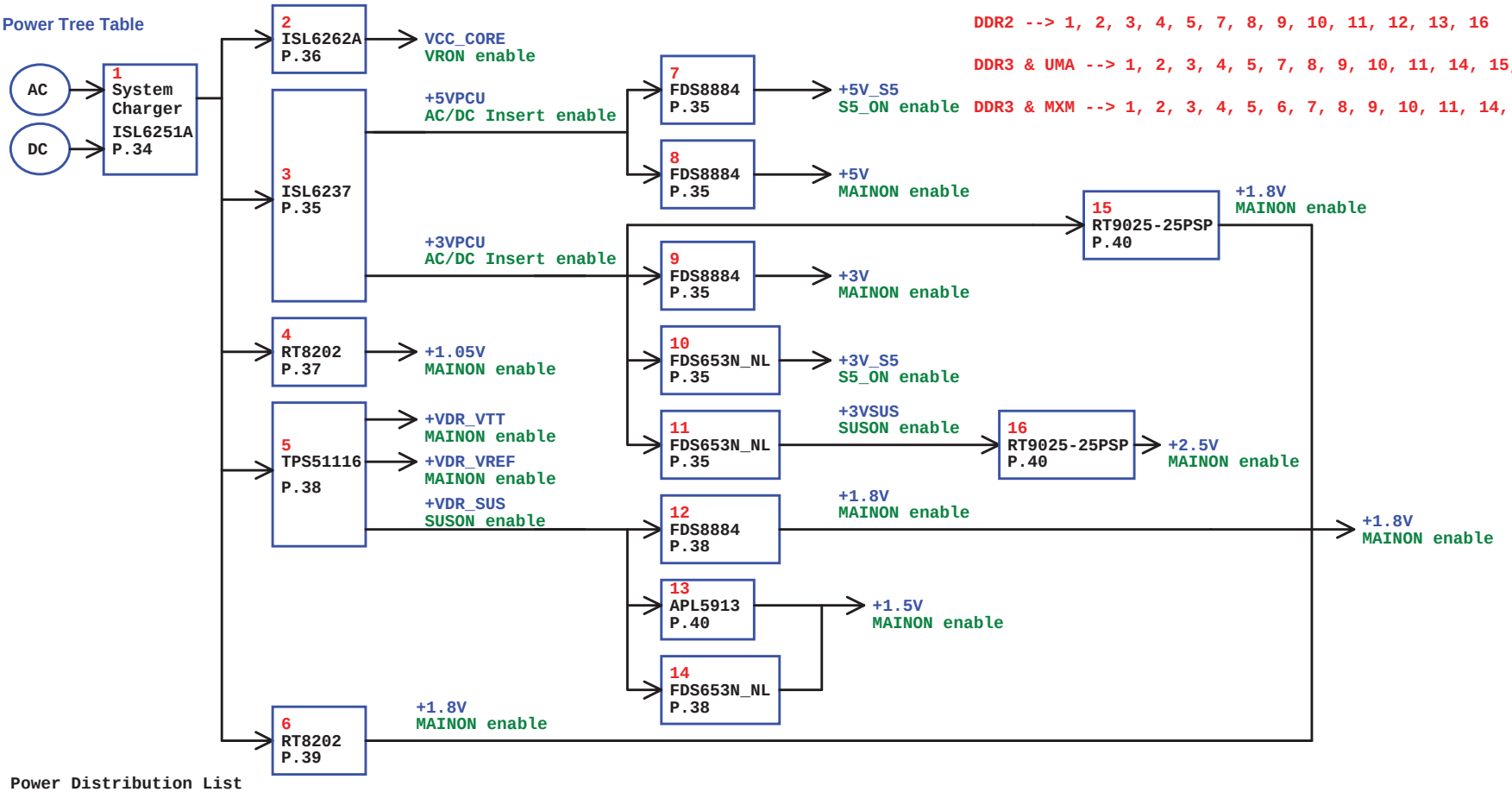
Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Quanta Computer Inc.
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Size | Document Number: Power Tree Table | Rev 1A
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CHANGE LIST

Model	REV	
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : Add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display isuue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 : Change U13 packing from TQFN to TDFN for vendor request
	2B	Page20 : Add R566 ,R567 ,R568 ,R569 ,C612 ,C616 ,C617 ,C618 solve the HDMI EMI issue. Page26 : Change CN41 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Change CN42 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Page30 : Add D47 ,D48, D49 & D50 solve the USB ESD issue. Page31 : Add R574 & R575 (390)solve Docking audio noise issue. Page32 : Add EMI resistor (R565) in SPI flash interface.

MODEL	ZY2 FROM	ZY2 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

PROJECT : ZY2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A

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DOC NO.	PROJECT MODEL :	ZY2	APPROVED BY:		DATE:	2007/ 2/15
	PART NUMBER:		DRAWING BY:		REVISON:	3A