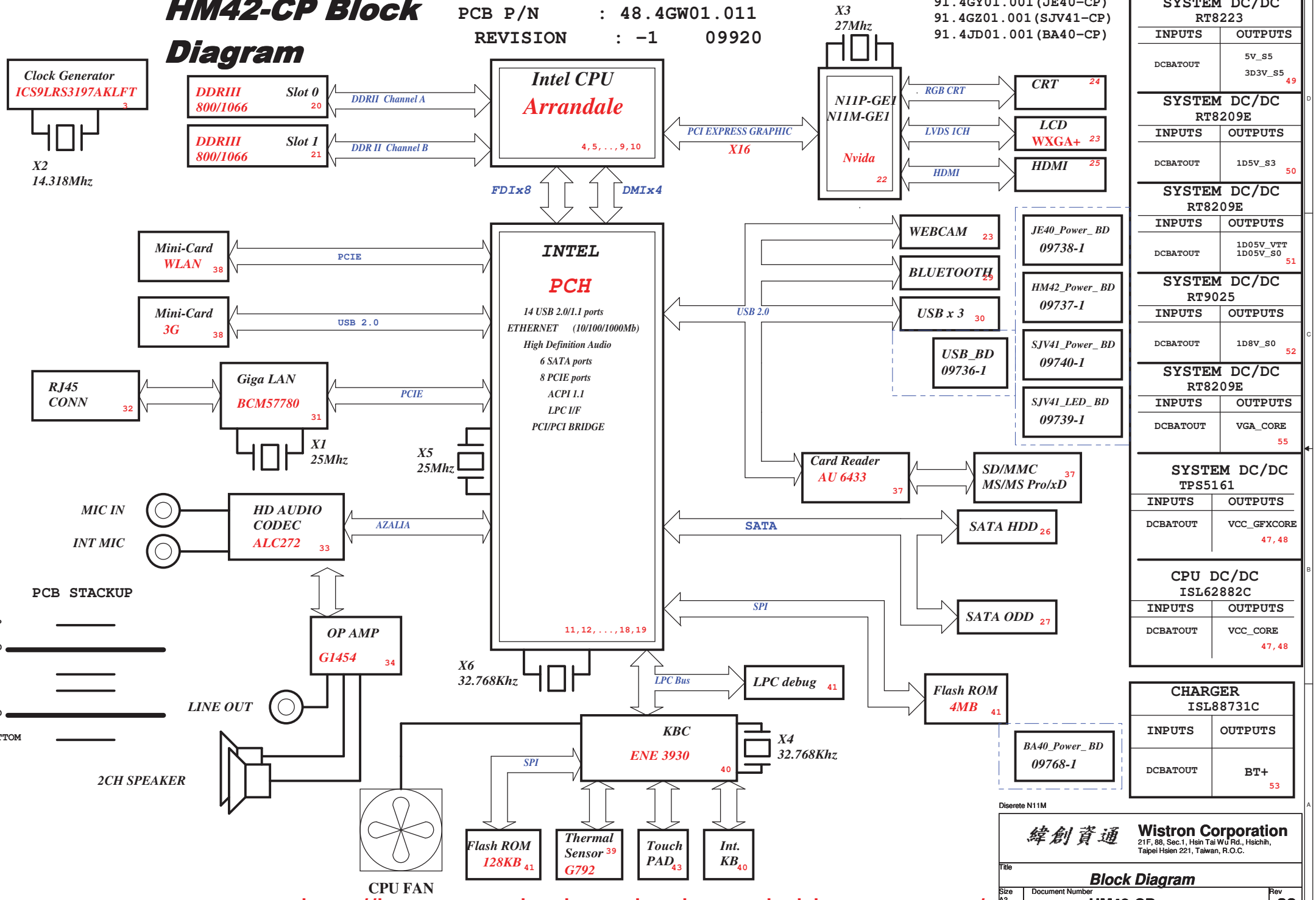
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001(HM42-CP)
91.4GY01.001(JE40-CP)
91.4GZ01.001(SJV41-CP)
91.4JD01.001(BA40-CP)



PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51

SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55

SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47,48

CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

Diserete N11M

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

<Variant Name>

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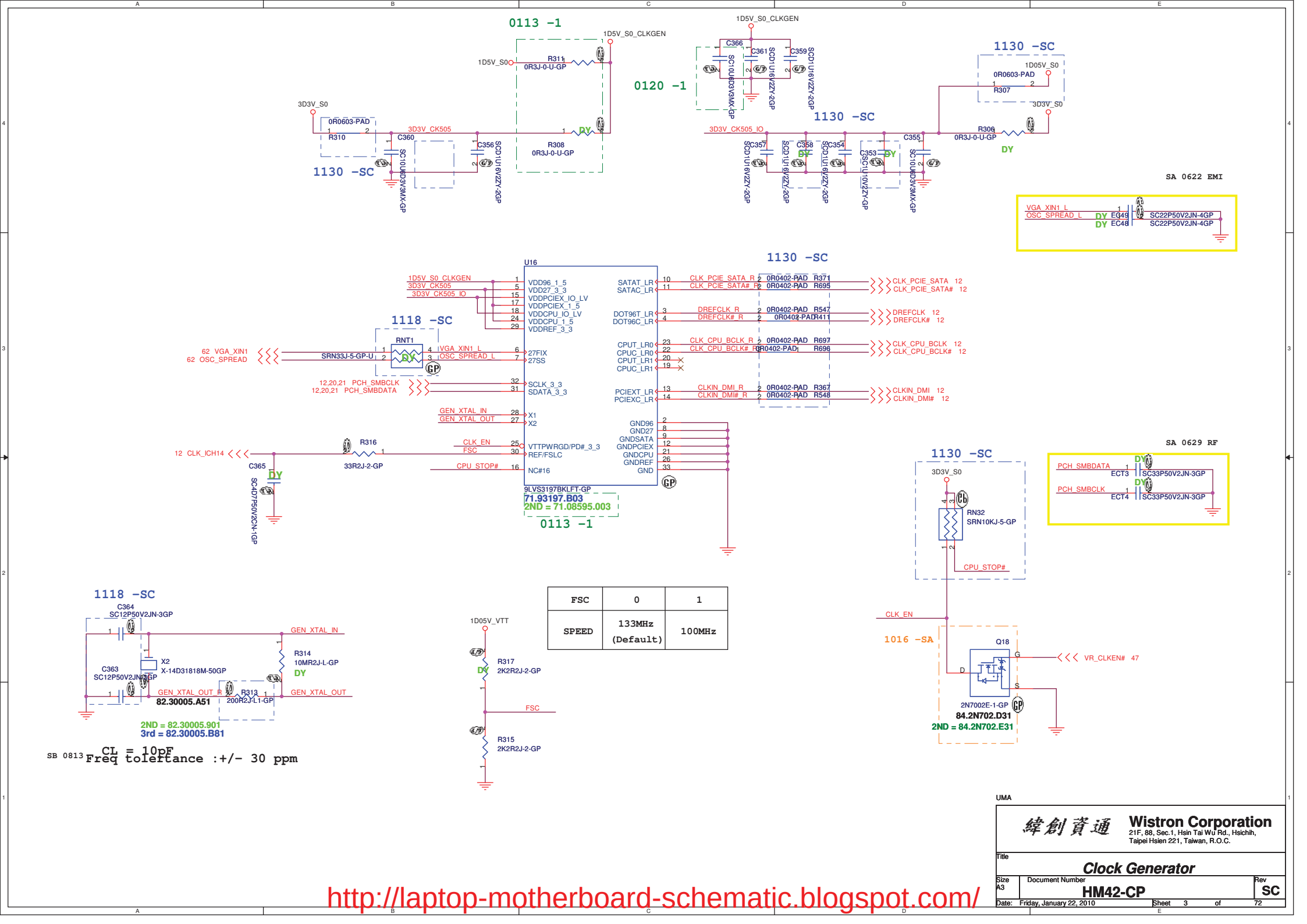

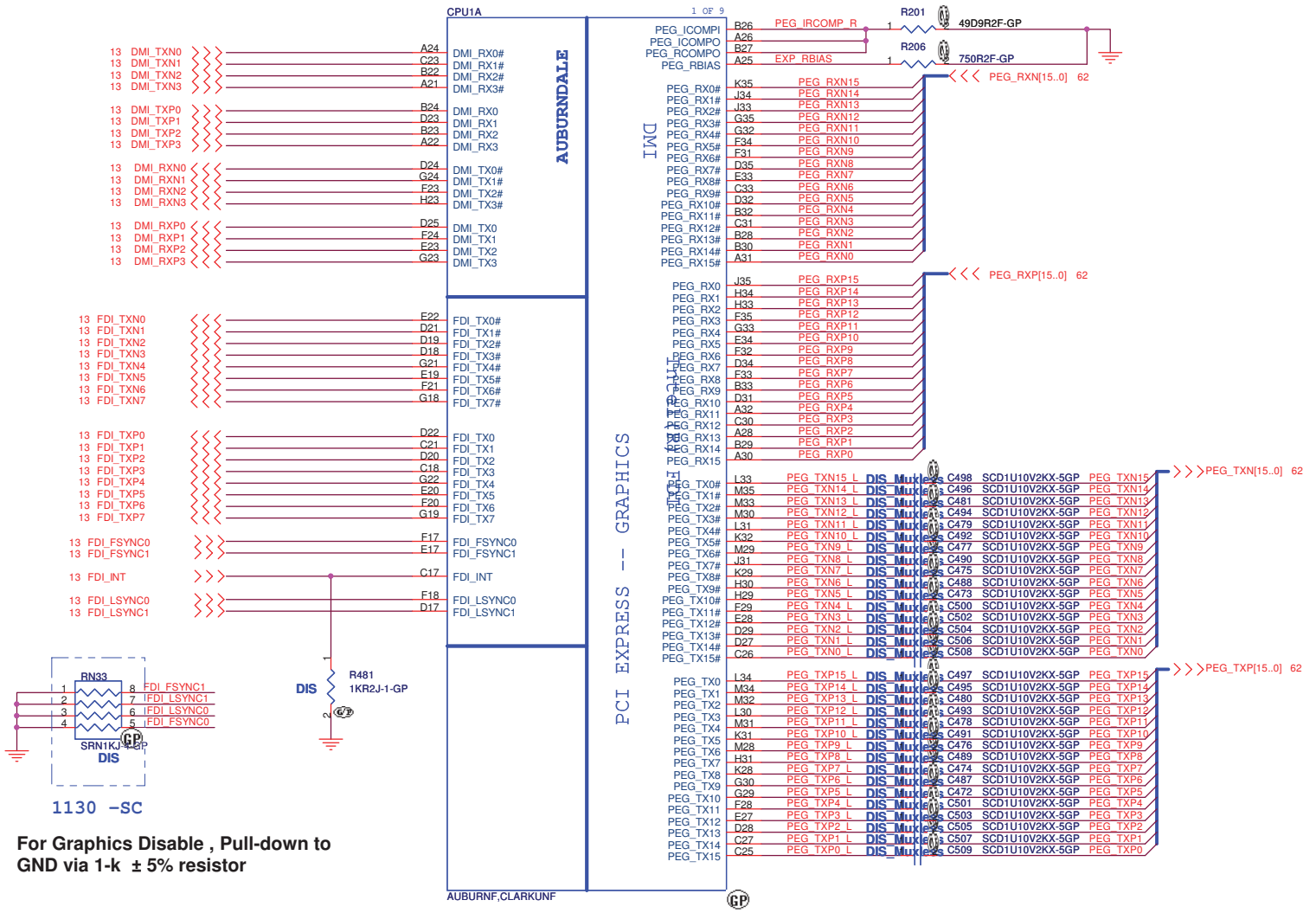

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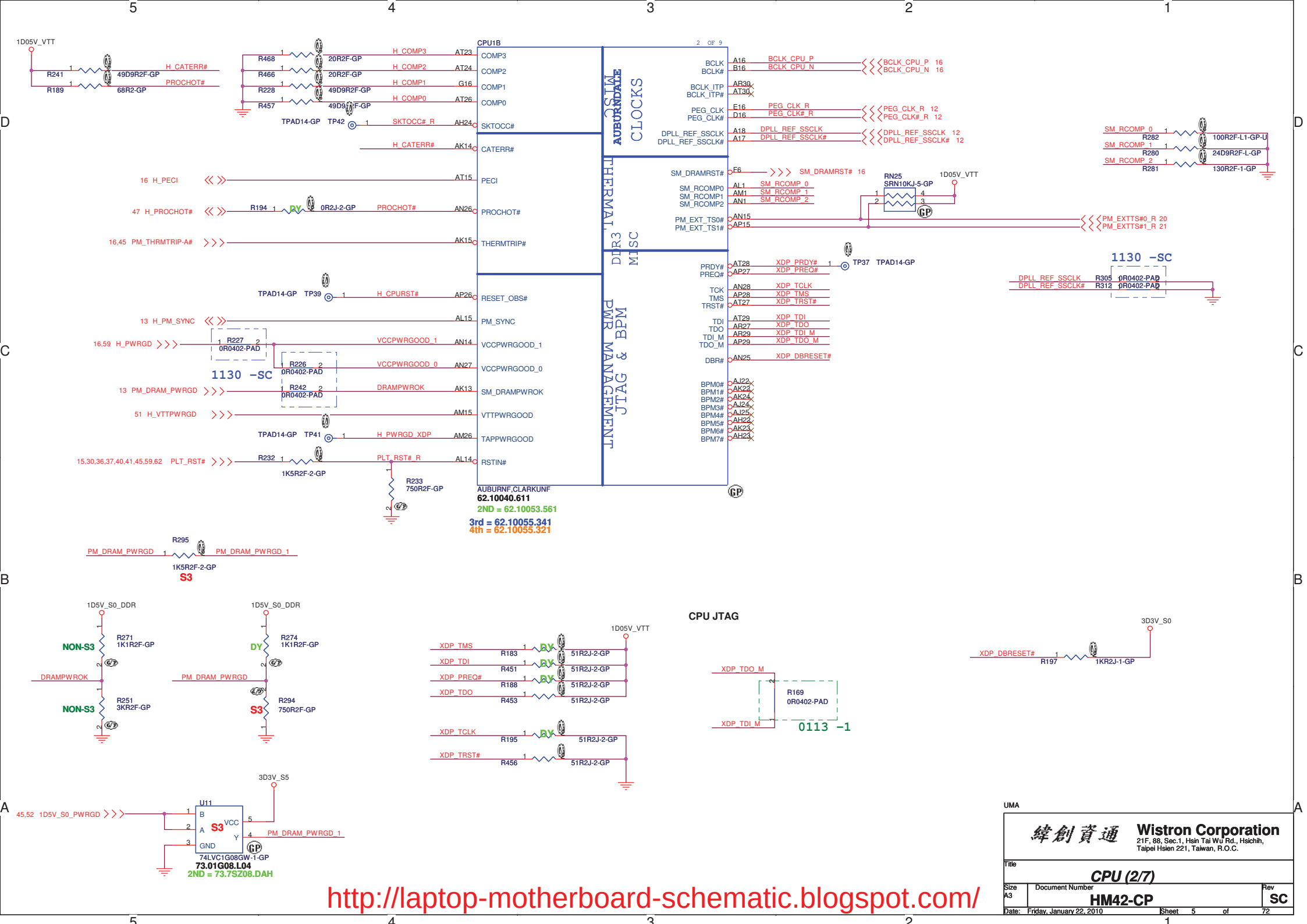
CPU1B
AUBURNDALE
CLOCKS
MISC
THERMAL
DIR3
MISC
JTAG & BPM
PWR MANAGEMENT
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
1130 -SC
CPU JTAG
0113 -1
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
UMA
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CPU (2/7)
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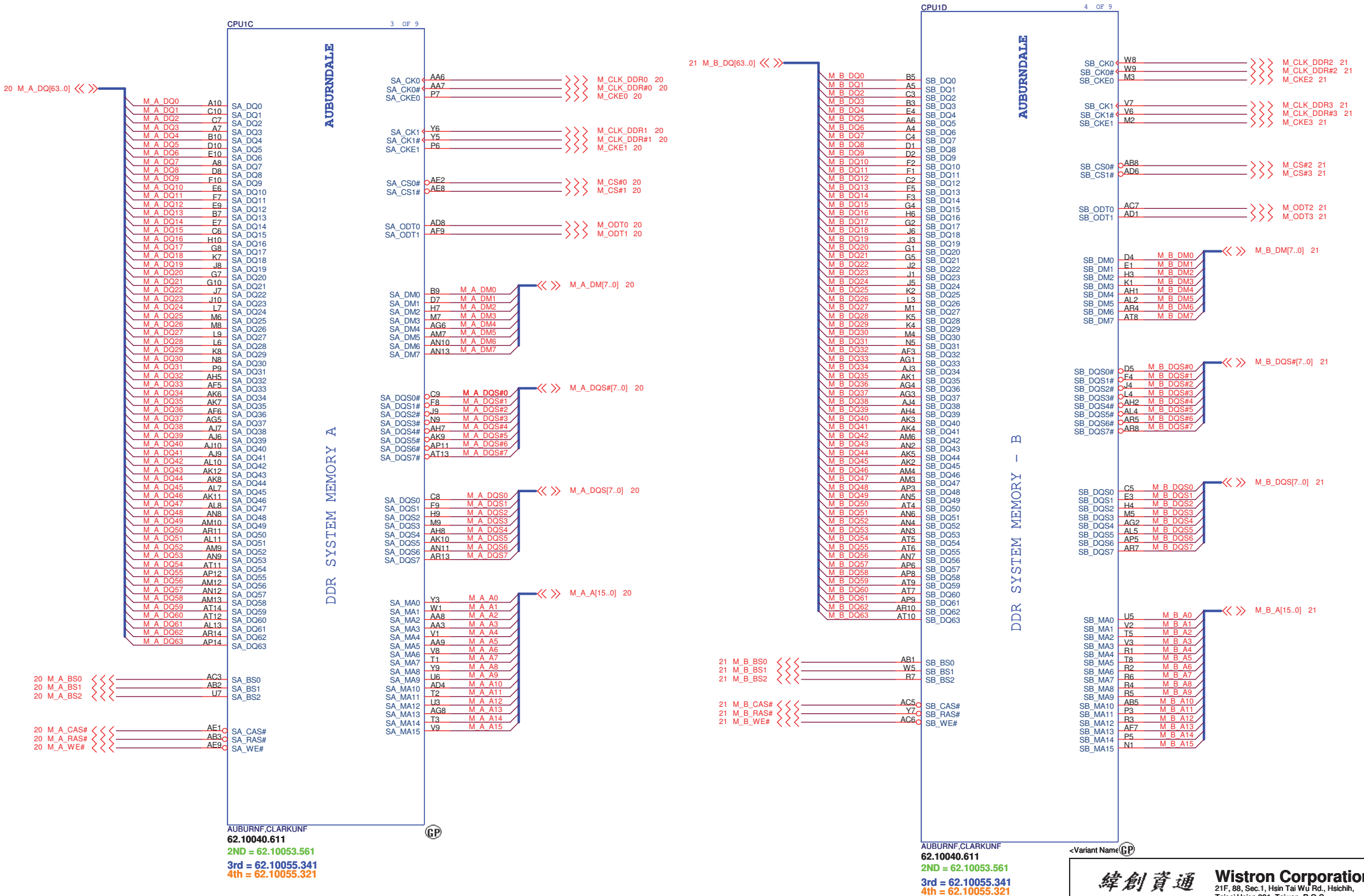

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Title: CPU (3/7)

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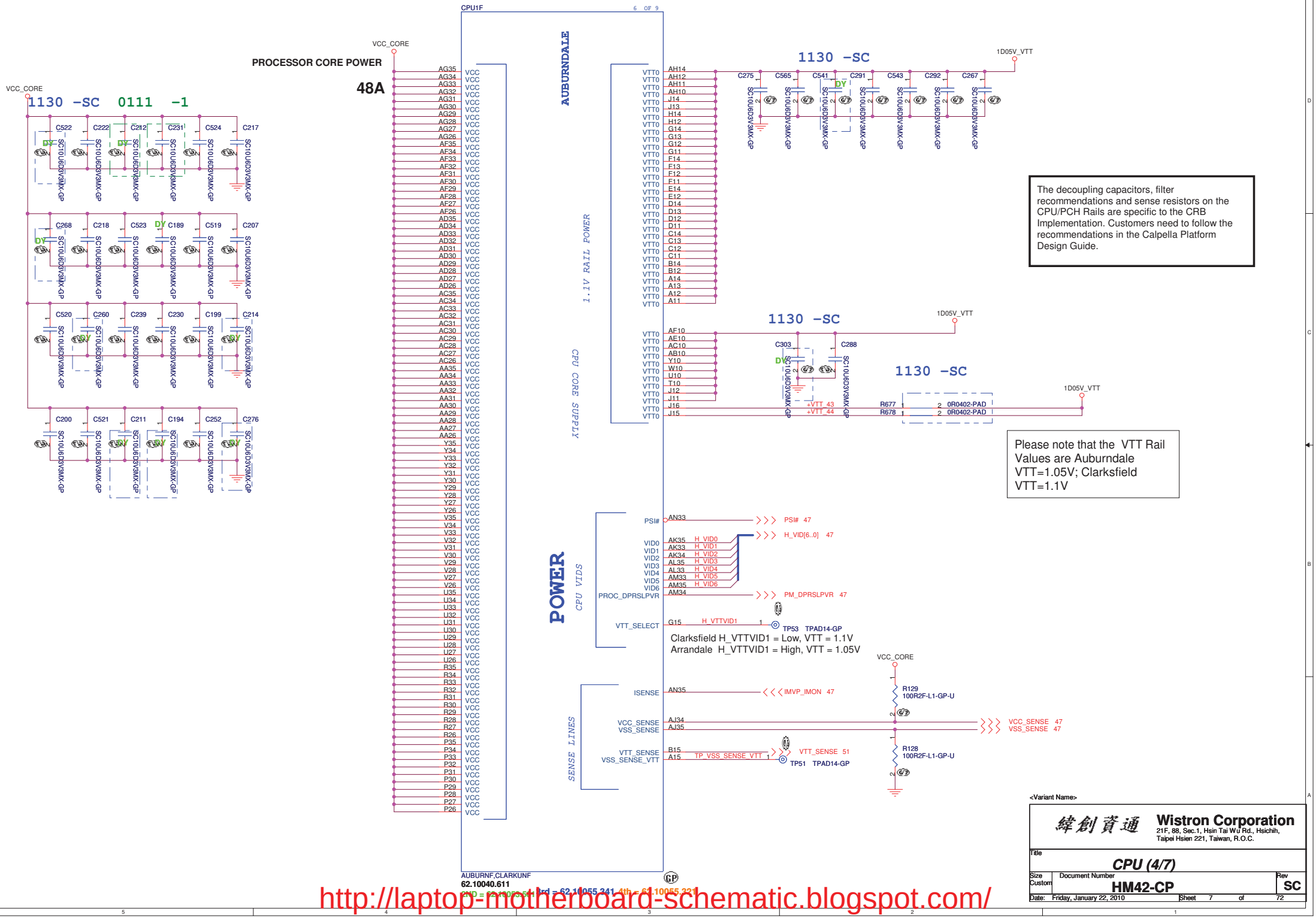

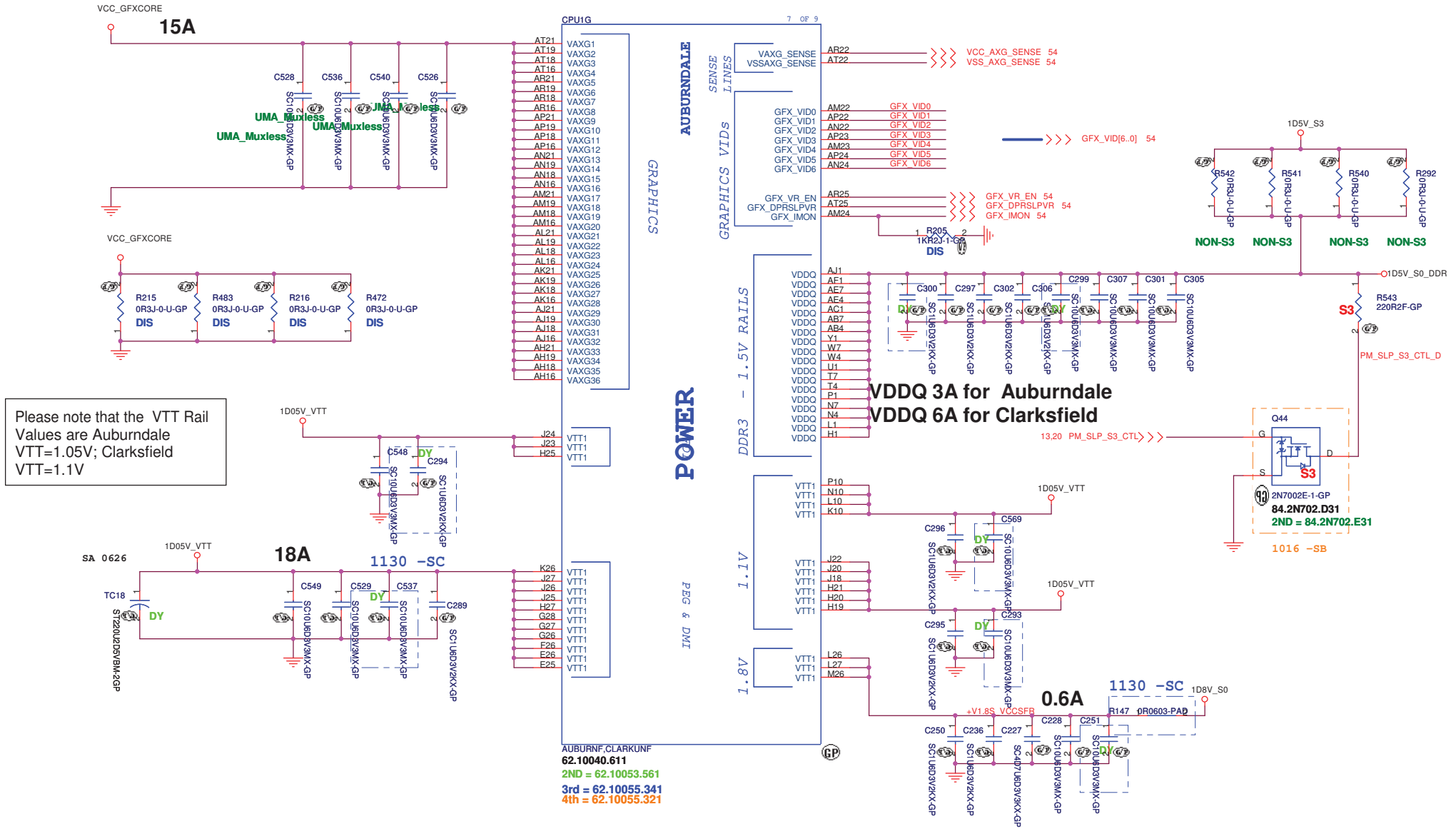

UMA

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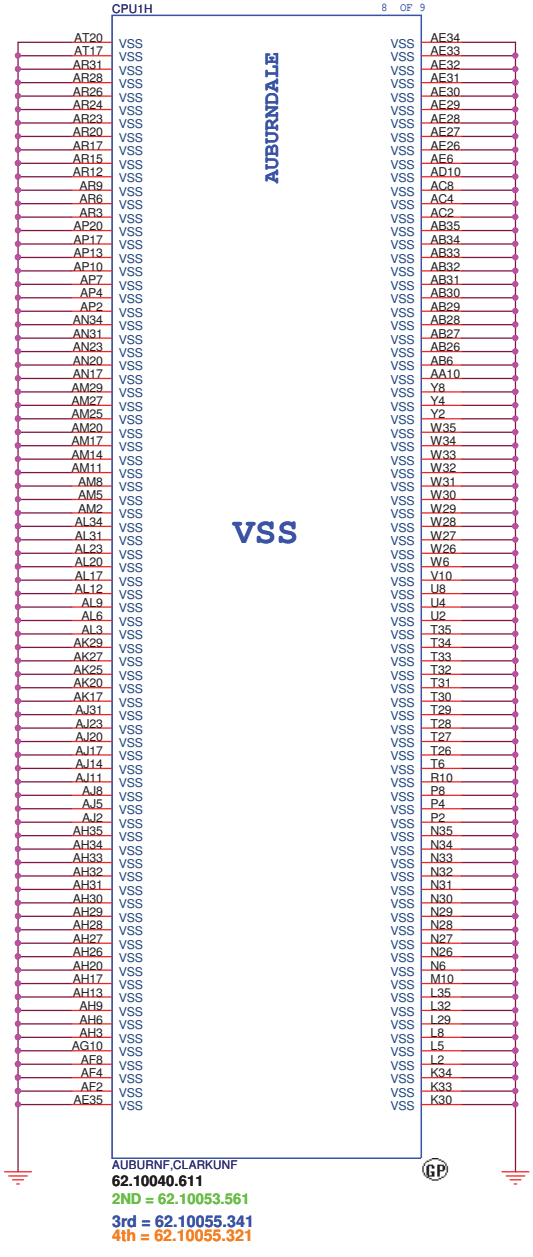

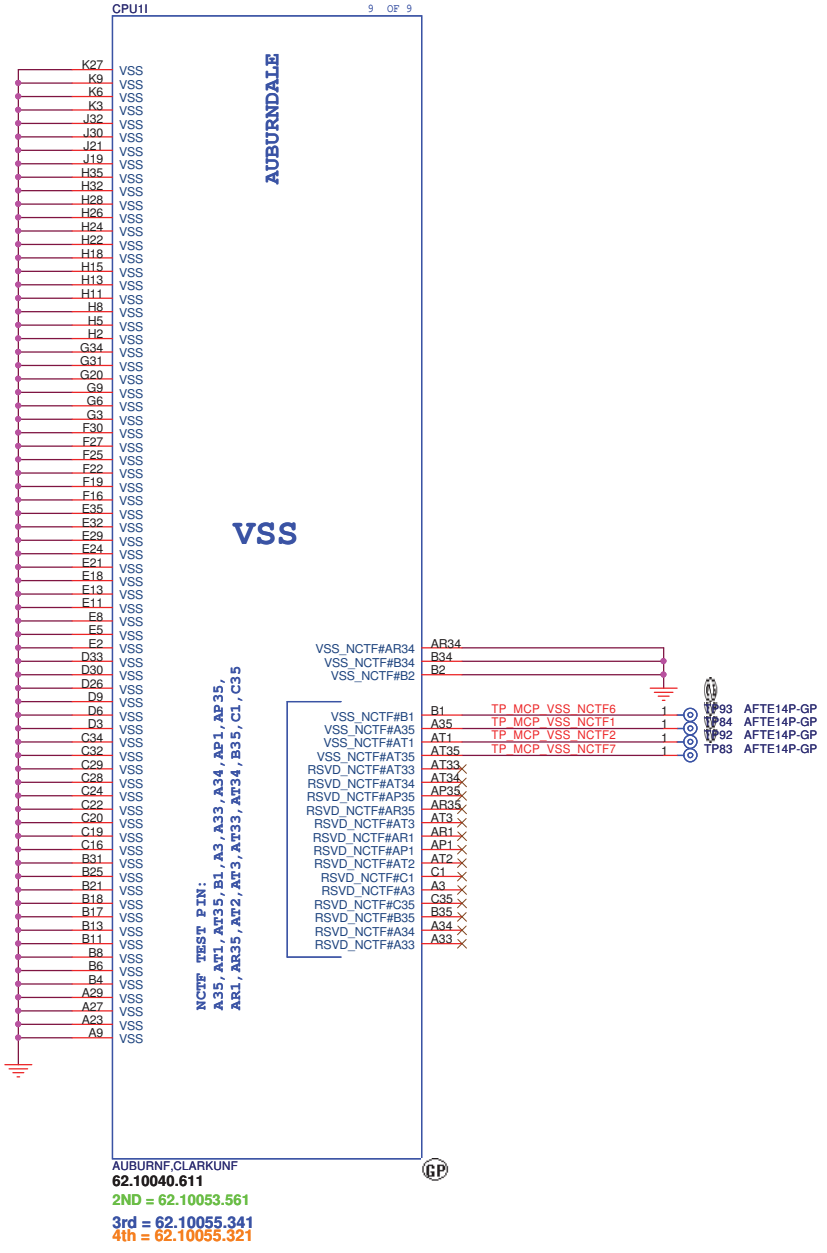

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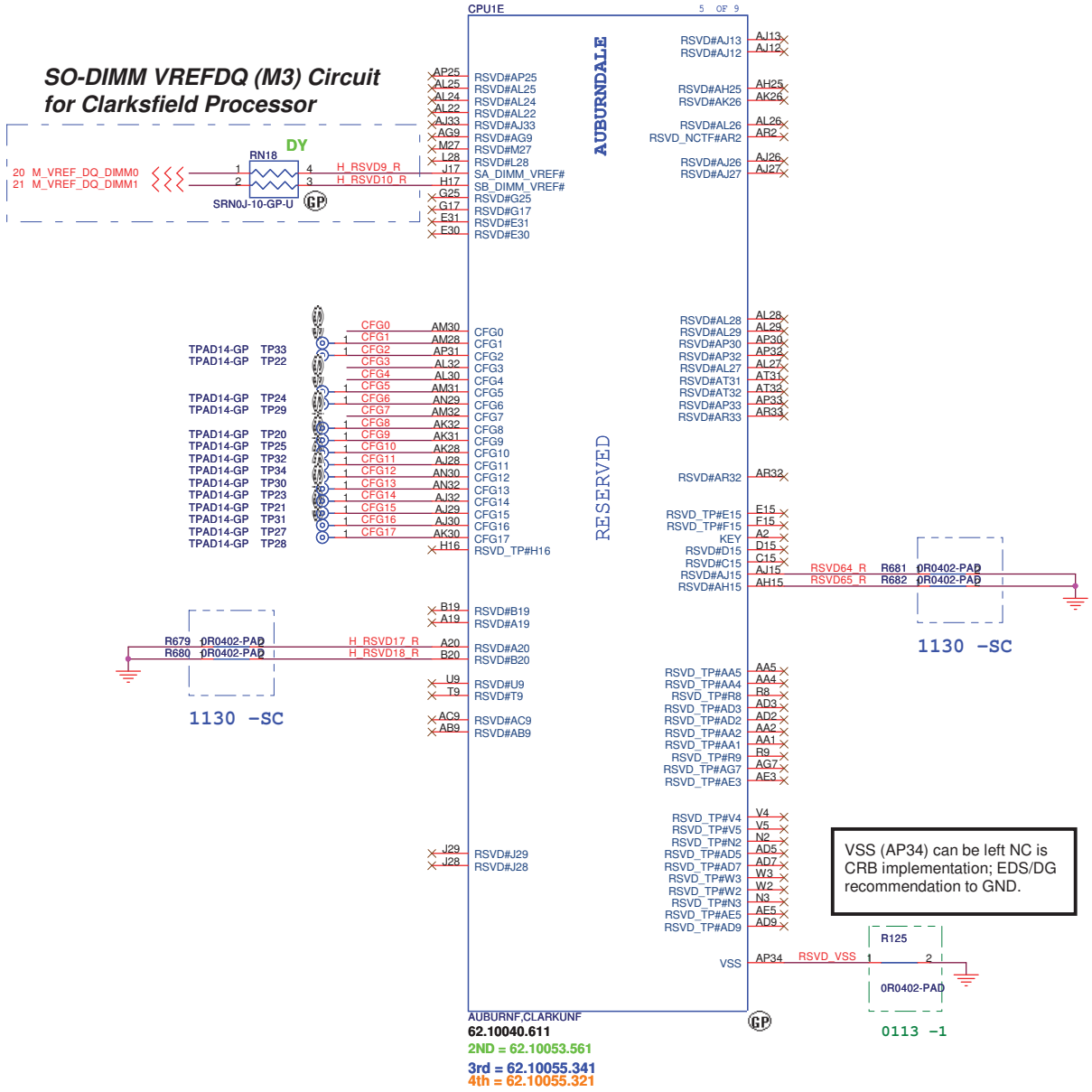

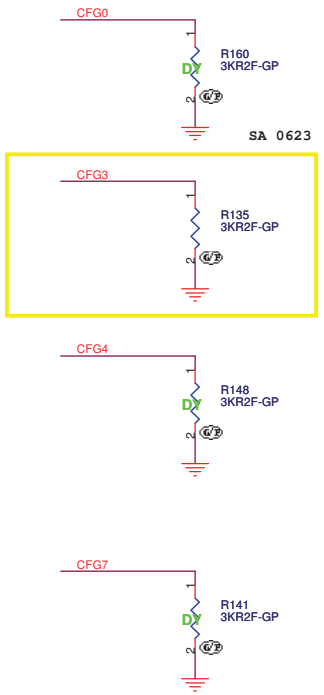

Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Variant Name>

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Title: CPU (7/7)

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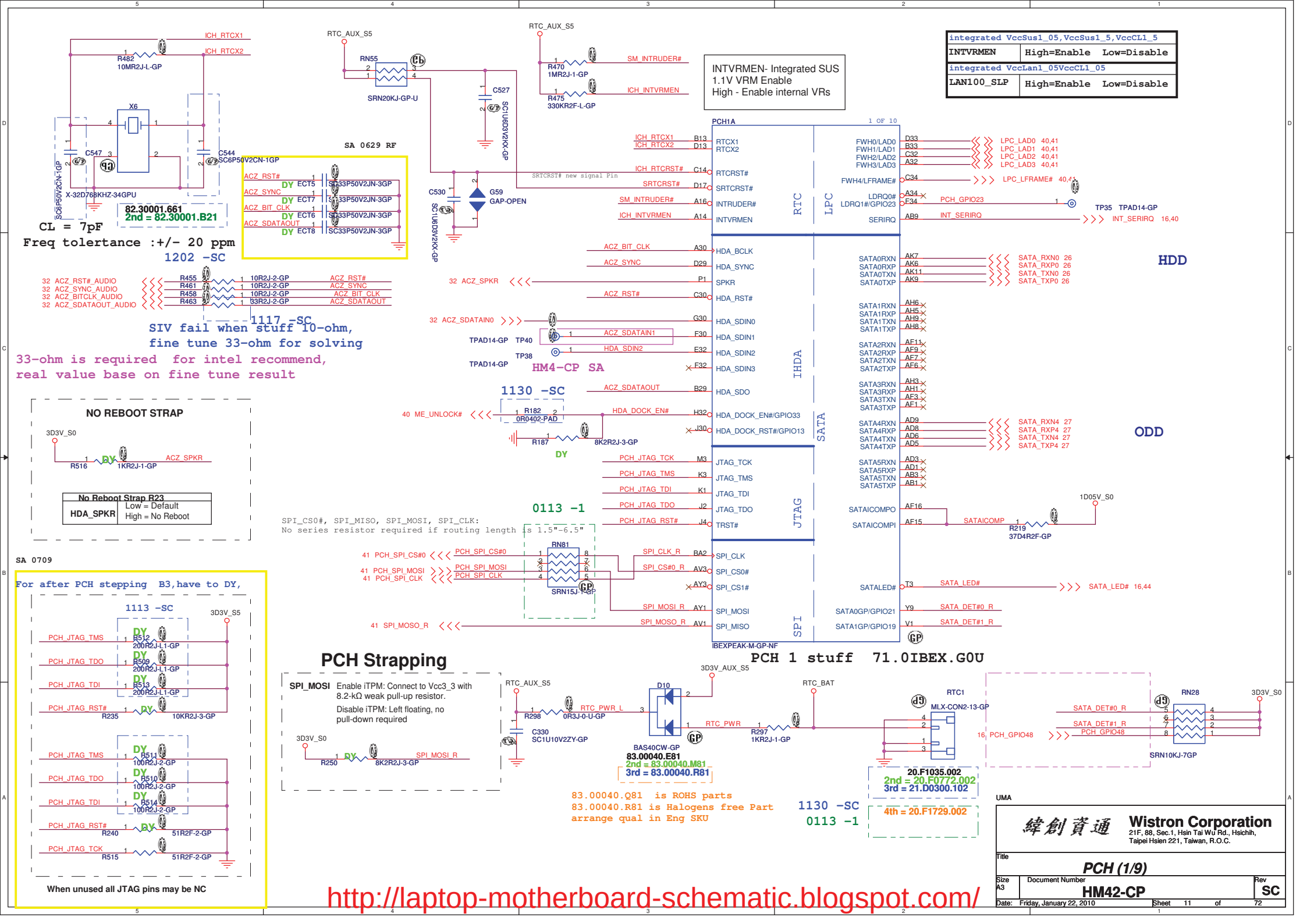
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
ODD
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
CL = 7pF
Freq tolertance :+/- 20 ppm
1202 -SC
SA 0629 RF
SRN20KJ-GP-U
SRTCRST# new signal Pin
GAP-OPEN
SIV fail when stuff 10-ohm,
fine tune 33-ohm for solving
33-ohm is required for intel recommend,
real value base on fine tune result
1117 -SC
HM4-CP SA
1130 -SC
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SA 0709
For after PCH stepping B3,have to DY,
1113 -SC
When unused all JTAG pins may be NC
0113 -1
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
SRN15J-7GP
IBEXPEAK-M-GP-NF
PCH 1 stuff 71.0IBEX.G0U
PCH Strapping
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3rd = 83.00040.R81
83.00040.Q81 is ROHS parts
83.00040.R81 is Halogens free Part
arrange qual in Eng SKU
20.F1035.002
2nd = 20.F0772.002
3rd = 21.D0300.102
4th = 20.F1729.002
SRN10KJ-7GP
UMA
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Title
PCH (1/9)
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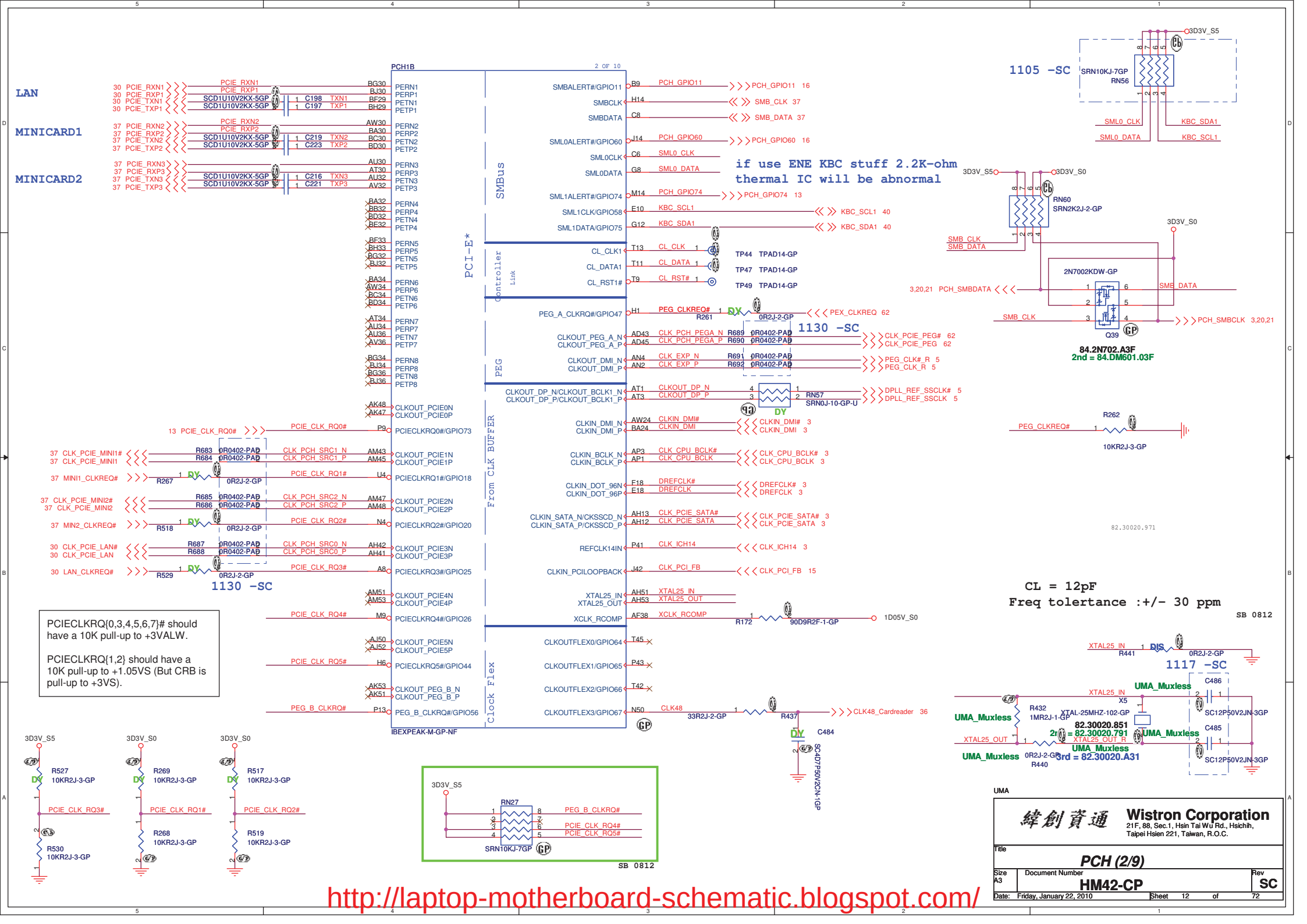
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
PEG
From CLK BUFFER
Clock Flex
Controller Link
IBEXPEAK-M-GP-NF
if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal
1105 -SC
1130 -SC
1130 -SC
1117 -SC
CL = 12pF
Freq tolertance :+/- 30 ppm
SB 0812
SB 0812
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
84.2N702.A3F
2nd = 84.DM601.03F
82.30020.971
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
UMA
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PCH (2/9)
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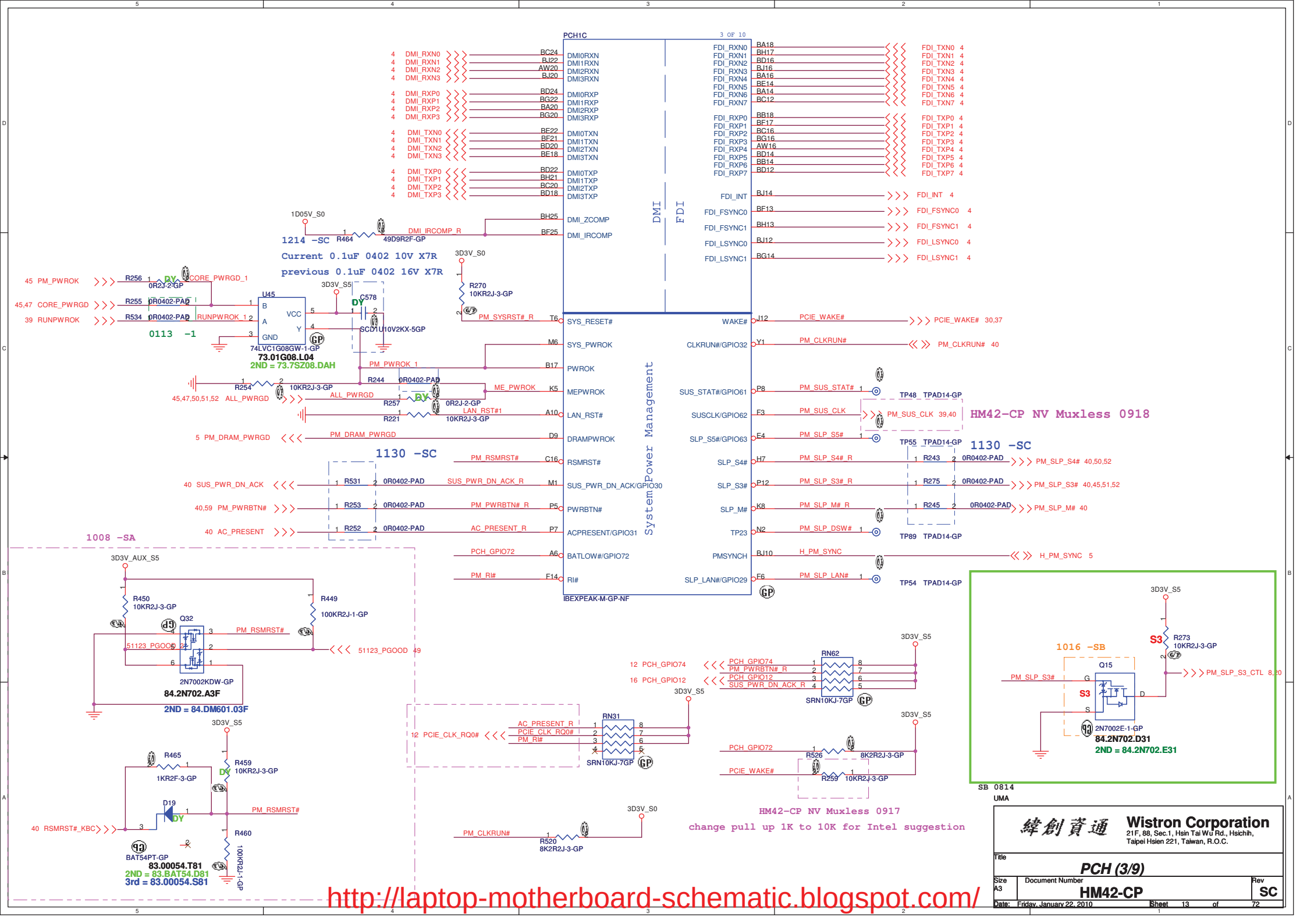
PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
1214 -SC
Current 0.1uF 0402 10V X7R
previous 0.1uF 0402 16V X7R
0113 -1
73.01G08.L04
2ND = 73.7SZ08.DAH
1130 -SC
HM42-CP NV Muxless 0918
1130 -SC
1008 -SA
1016 -SB
84.2N702.A3F
2ND = 84.DM601.03F
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.00054.S81
84.2N702.D31
2ND = 84.2N702.E31
HM42-CP NV Muxless 0917
change pull up 1K to 10K for Intel suggestion
SB 0814
UMA
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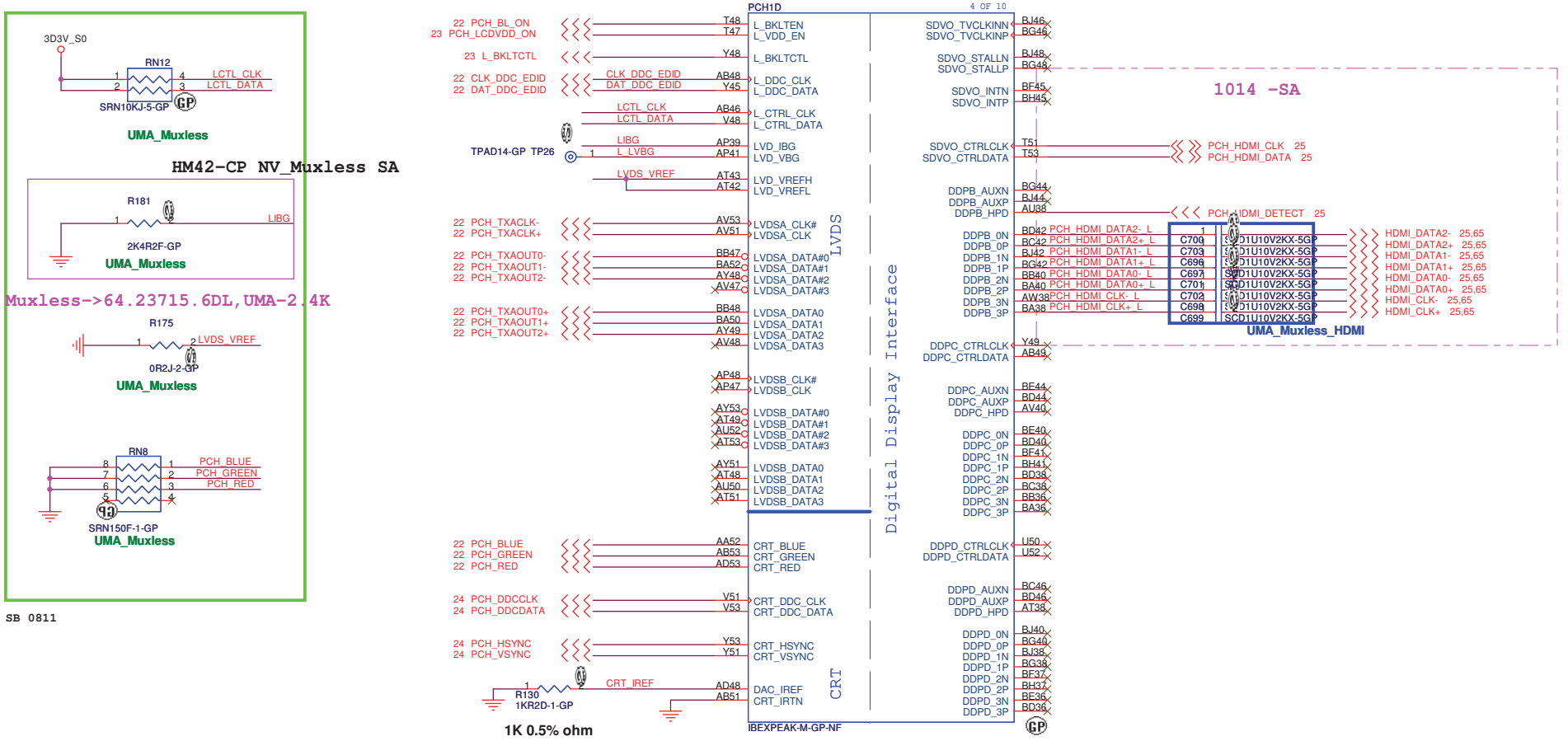

<Core Design>

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Title: PCH (4/9)

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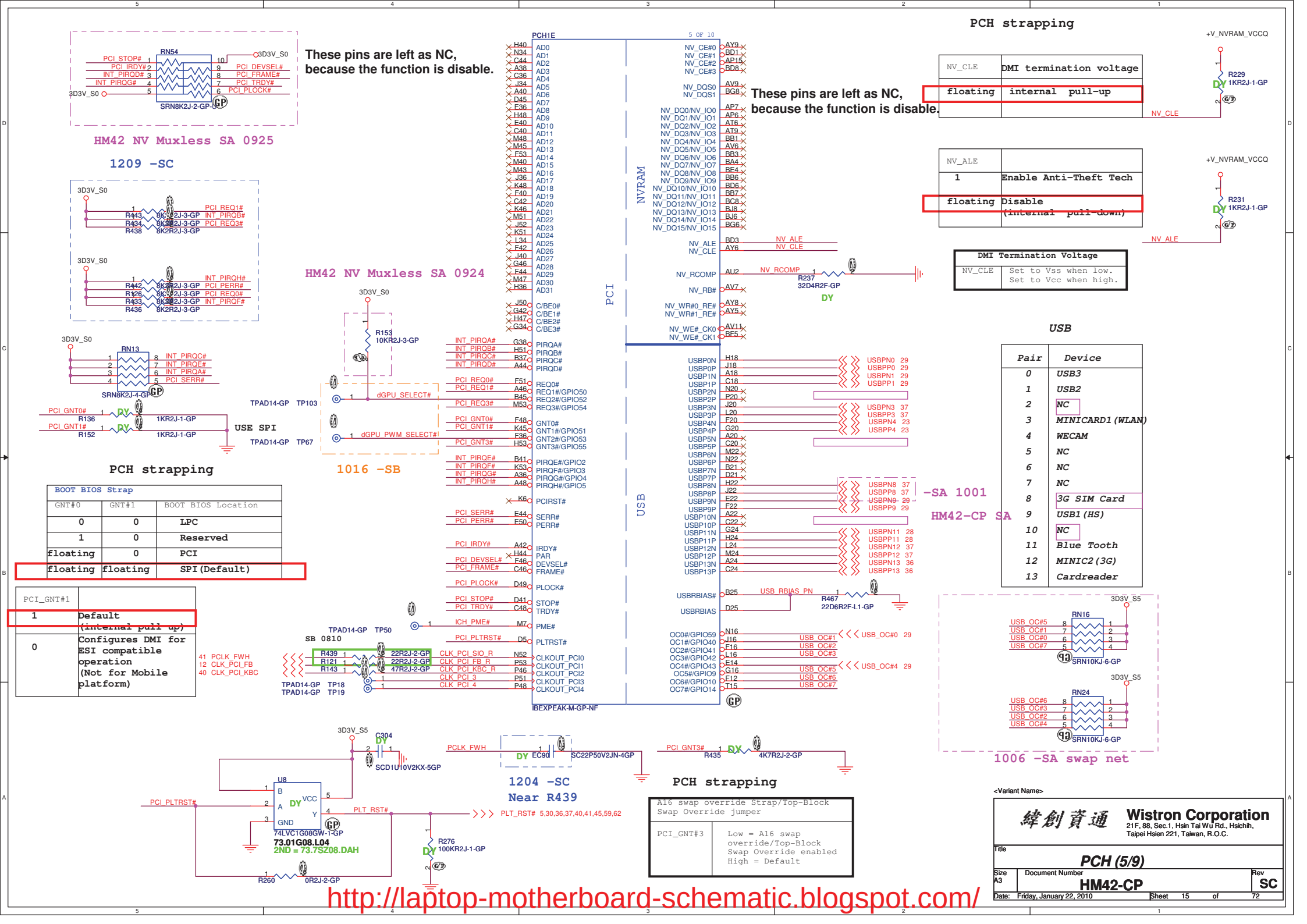
PCH strapping
NV_CLE
DMI termination voltage
floating
internal pull-up
NV_CLE
R229
1KR2J-1-GP
+V_NVRAM_VCCQ
NV_ALE
1
Enable Anti-Theft Tech
floating
Disable
(internal pull-down)
NV_ALE
R231
1KR2J-1-GP
+V_NVRAM_VCCQ
DMI Termination Voltage
NV_CLE
Set to Vss when low.
Set to Vcc when high.
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
PCH1E
5 OF 10
NVRAM
PCI
USB
IBEXPEAK-M-GP-NF
HM42 NV Muxless SA 0925
1209 -SC
HM42 NV Muxless SA 0924
1016 -SB
USE SPI
USB
Pair
Device
0
USB3
1
USB2
2
NC
3
MINICARD1 (WLAN)
4
WECAM
5
NC
6
NC
7
NC
8
3G SIM Card
9
USB1 (HS)
10
NC
11
Blue Tooth
12
MINIC2 (3G)
13
Cardreader
-SA 1001
HM42-CP SA
1006 -SA swap net
PCH strapping
BOOT BIOS Strap
GNT#0
GNT#1
BOOT BIOS Location
0
0
LPC
1
0
Reserved
floating
0
PCI
floating
floating
SPI(Default)
PCI_GNT#1
1
Default
(internal pull up)
0
Configures DMI for ESI compatible operation (Not for Mobile platform)
SB 0810
1204 -SC
Near R439
PCH strapping
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default
73.01G08.L04
2ND = 73.7SZ08.DAH
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

HM42-CP_NV _Muxless SA

PCH1F

6 OF 10

BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

MISC
GPIO
CPU

CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 NC_1 NC_2 NC_3 NC_4 NC_5 INIT3_3V# TP24

VSS_NCTF_8 VSS_NCTF_9 VSS_NCTF_16 VSS_NCTF_17 VSS_NCTF_28
VSS_NCTF#A4 VSS_NCTF#A49 VSS_NCTF#A5 VSS_NCTF#A50 VSS_NCTF#A52 VSS_NCTF#A53 VSS_NCTF#B2 VSS_NCTF#B53 VSS_NCTF#BE1 VSS_NCTF#BE53 VSS_NCTF#BF1 VSS_NCTF#BF53 VSS_NCTF#BH1 VSS_NCTF#BH53 VSS_NCTF#BJ1 VSS_NCTF#BJ2 VSS_NCTF#BJ4 VSS_NCTF#BJ49 VSS_NCTF#BJ5 VSS_NCTF#BJ50 VSS_NCTF#BJ52 VSS_NCTF#BJ53 VSS_NCTF#D1 VSS_NCTF#D53 VSS_NCTF#E1 VSS_NCTF#E53

NCTF
RSVD

NCTF TEST PIN:
A4,A49,A5,A50,A52,A53,B2,B53,BE1,
BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4,
BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

IBEXPEAK-M-GP-NF

PCH_GPIO0 EC_SMI# PX_HDMI# EC_SCI# EC_SWI# PCH_GPIO12 PCH_GPIO15 DGPU_HOLD_RST# DGPU_PWROK PCH_GPIO22 PCH_GPIO24 PCH_GPIO27 PCH_GPIO28 STP_PCI# PCH_GPIO35 DGPU_PWR_EN# dGPU_PRSNT# dGPU_EDID PCH_GPIO39 PCH_GPIO45 RST_GATE PCH_GPIO48 PSW_CLR# PCH_GPIO57

TPAD14-GP TP36 TPAD14-GP TP46 TPAD14-GP TP45 TPAD14-GP TP56 TPAD14-GP TP105

40 EC_SCI# 40 EC_SWI# 13 PCH_GPIO12 62 DGPU_HOLD_RST# 55,61,62 DGPU_PWROK 61 DGPU_PWR_EN# 11 PCH_GPIO48

KA20GATE 40
BCLK_CPU_N_R BCLK_CPU_P_R SRN0J-10-GP-U RN58 BCLK_CPU_N 5 BCLK_CPU_P 5
H_PECI 5
KBRCIN# 40
H_PWRGD 5,59
PCH_THERMTRIP_R R230 54D9R2F-L1-GP PM_THRMTRIP-A# 5,45
R236 56R2J-4-GP 1D05V_VTT
Placed Within 2" from PCH

3D3V_S5 RN30 SRN10KJ-7GP
12 PCH_GPIO11 EC_SWI# 12 PCH_GPIO60 PCH_GPIO28
PCH_GPIO45 R508 8K2R2J-3-GP SB 0819
PCH_GPIO15 R266 1KR2J-1-GP

HM42-CP_NV_Muxless SA
1016 -SB
SB 0814

PSW_CLR# GAP-OPEN G111

SB 0722
AFTE14P-GP TP80 AFTE14P-GP TP88 PCH_TP95 PCH_TP96
AFTE14P-GP TP87 PCH_TP97
AFTE14P-GP TP82 PCH_TP98

3D3V_S0 RN29 SRN10KJ-7GP
11,44 SATA_LED# PCH_GPIO39 11,40 INT_SERIRQ PSW_CLR#

RP1 SRN10KJ-L3-GP
STP_PCI# PCH_GPIO22 PCH_GPIO0 dGPU_EDID EC_SMI# EC_SCI# PX_HDMI#

PCH_GPIO35 R265 10KR2J-3-GP

1D5V_S3 R279 1KR2F-3-GP DDR3_DRAMRST# 20,21
0121 -1 NON-S3 R278 0R2J-2-GP
2ND = 84.2N702.E31
84.2N702.D31
2N7002E-1-GP Q14
3D3V_S5 R272 10KR2F-2-GP RST_GATE
C298 SCD047U25V2KX-GP
SM_DRAMRST# 5 R277 100KR2F-L1-GP
INIT3_3V# TP52 TPAD14-GP

HM42-CP_NV _Muxless SA
3D3V_S0 R263 10KR2J-3-GP DY DGPU_PWR_EN# R264 10KR2J-3-GP
3D3V_S0 R532 10KR2J-3-GP DY DGPU_HOLD_RST# R533 10KR2J-3-GP

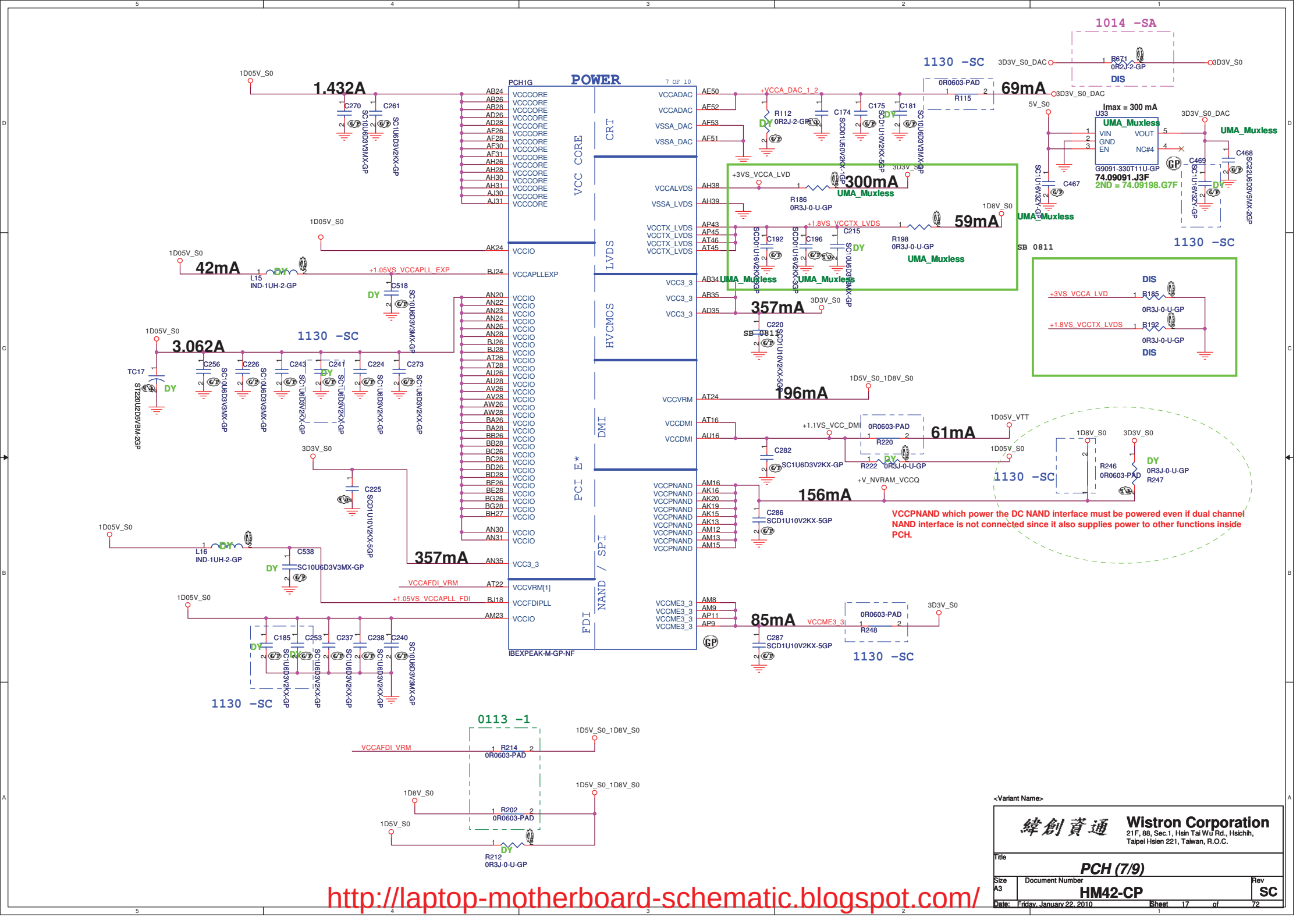
H: No SG function
L: SG Support
3D3V_S0 R224 10KR2J-3-GP DIS_UMA dGPU_PRSNT# R225 10KR2J-3-GP Muxless

SB 0812
3D3V_S5 UMA_Muxless R239 10KR2J-3-GP PCH_GPIO57 R238 10KR2J-3-GP DIS
UMA_DISCRETE#
Optimus: HIGH
UMA: HIGH
DIS ONLY: LOW

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

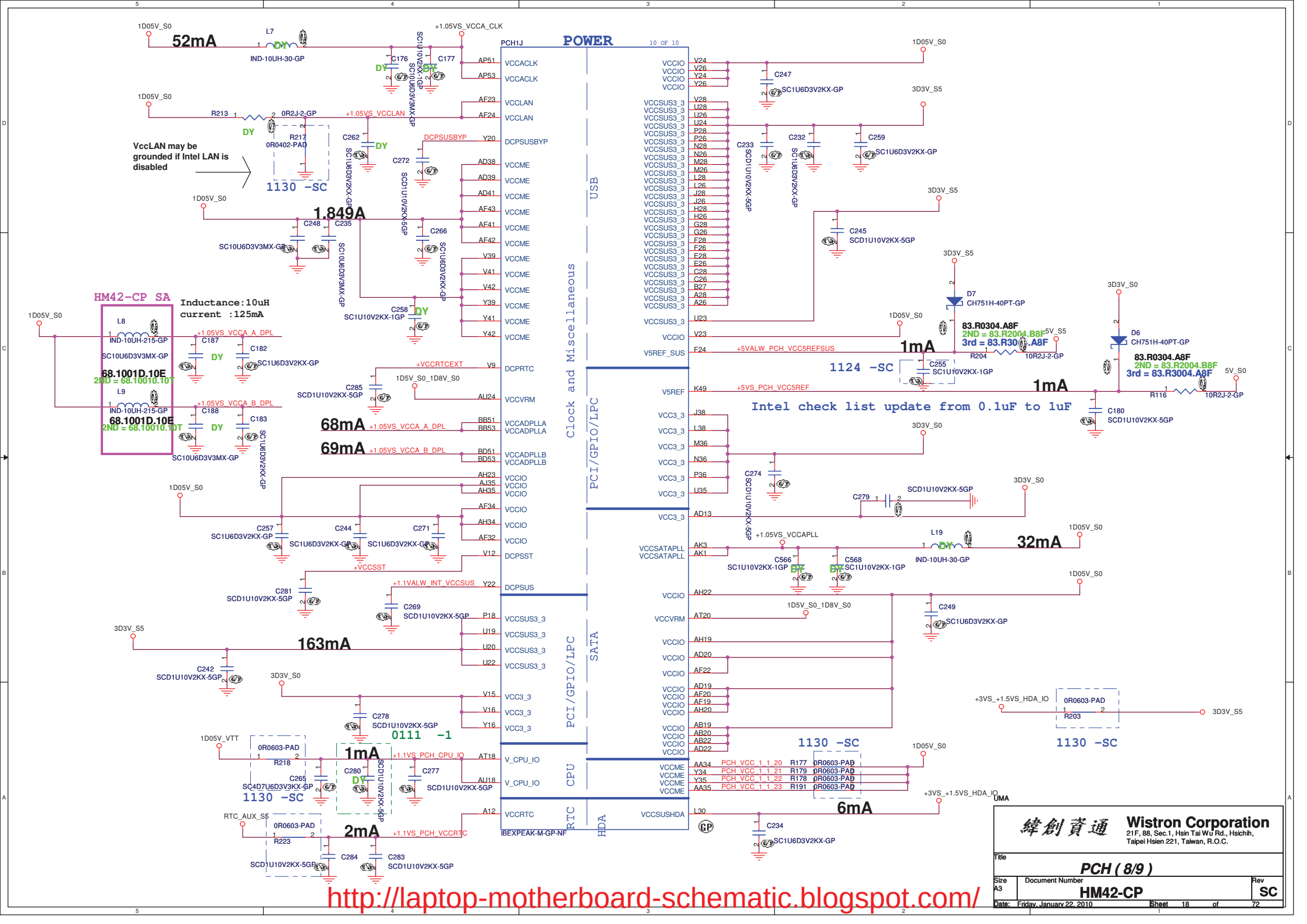
Title: PCH (6/9)
Size: A3 Document Number: HM42-CP Rev: SC
Date: Friday, January 22, 2010 Sheet 16 of 72

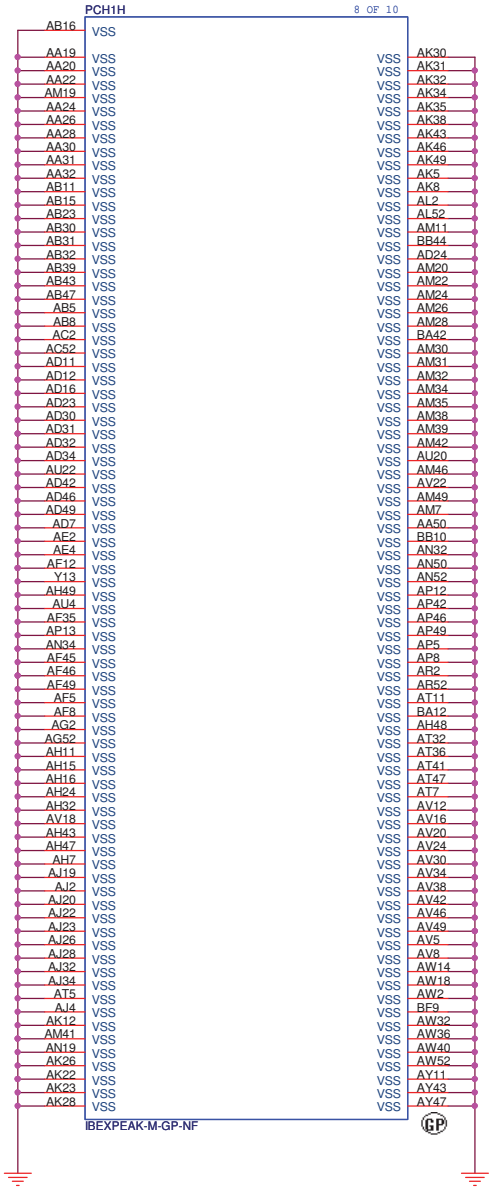


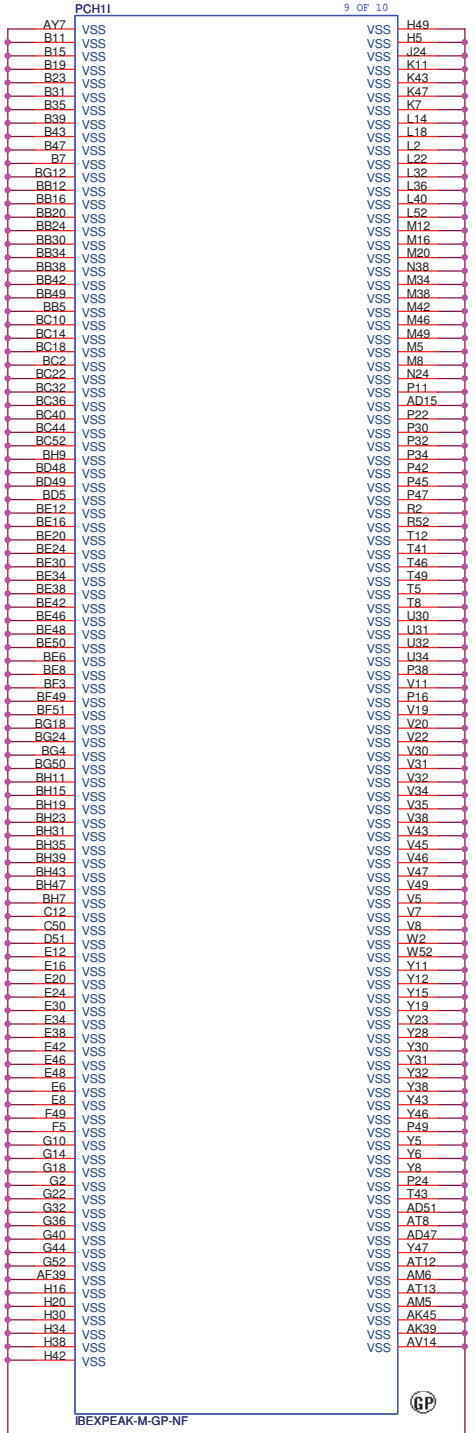
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (7/9)
Size: A3 | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 17 of 72







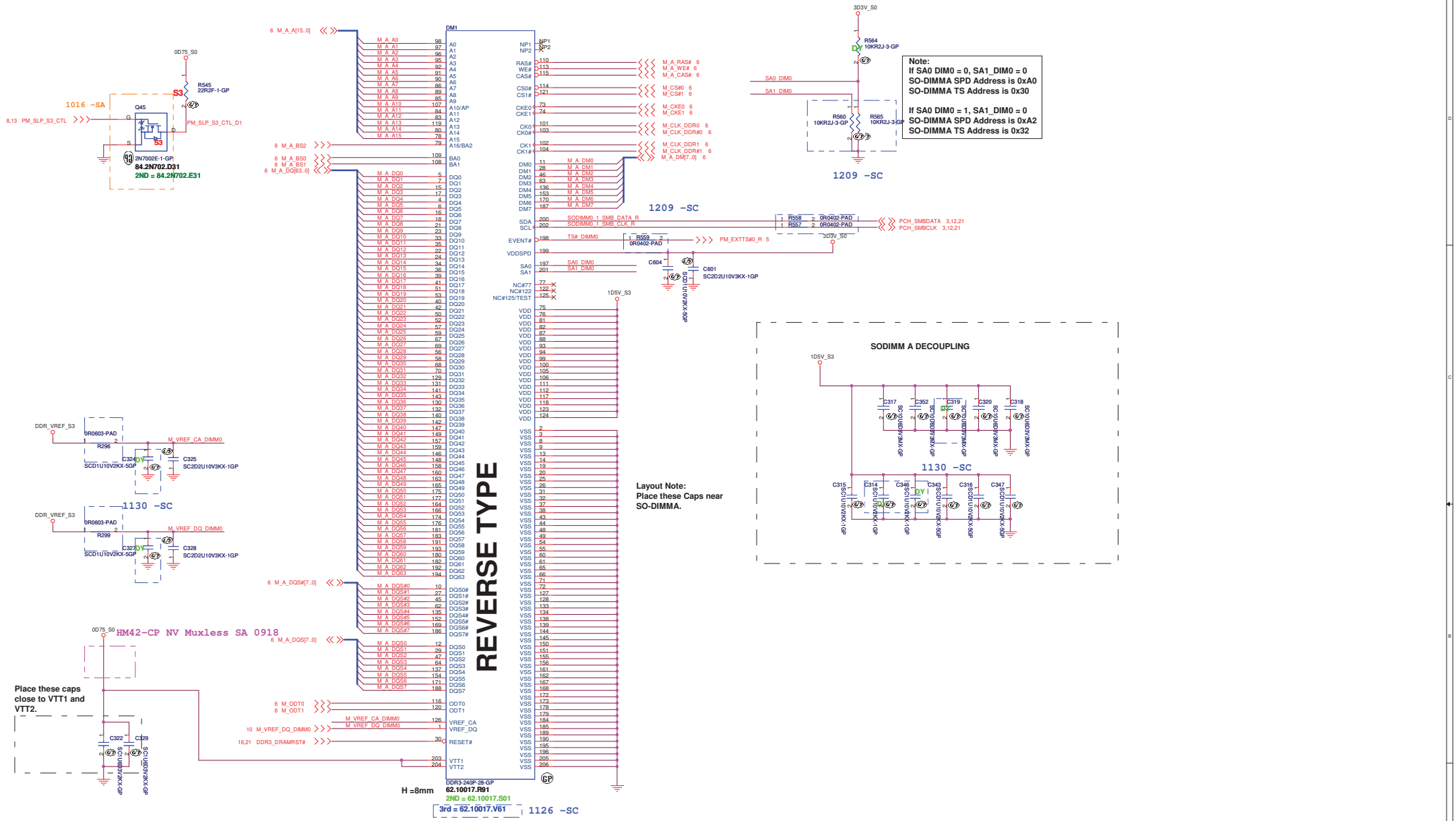
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (9/9)**

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 19 of 72



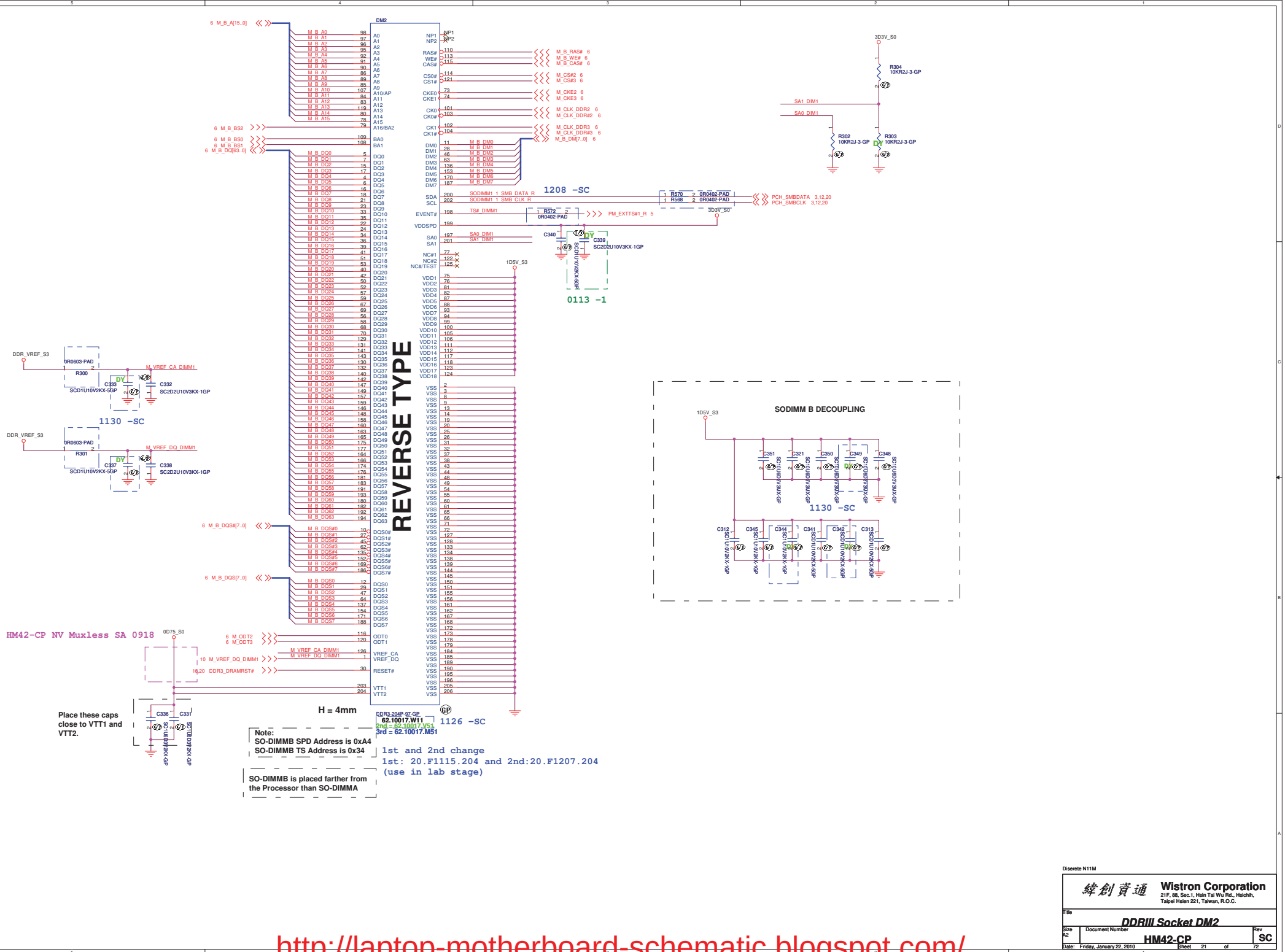
Diserete N11M

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDRIII Socket DM1***

Size	Document Number	Rev
A2	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 20 of 72



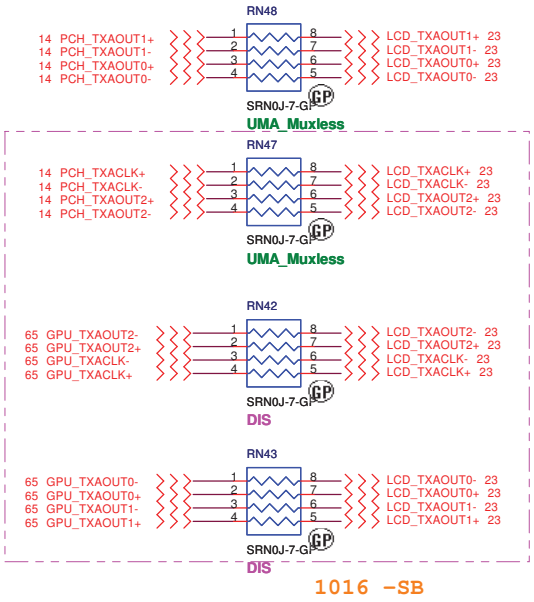
Diserete N11M

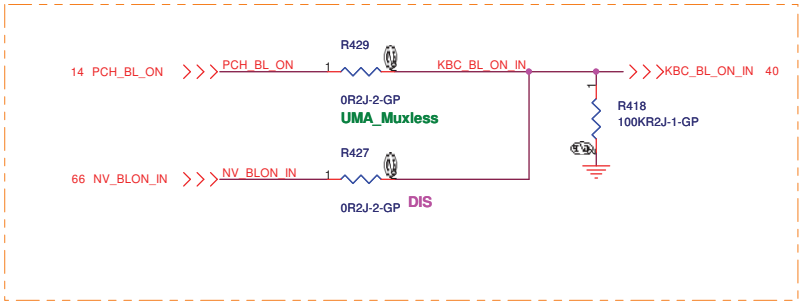
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

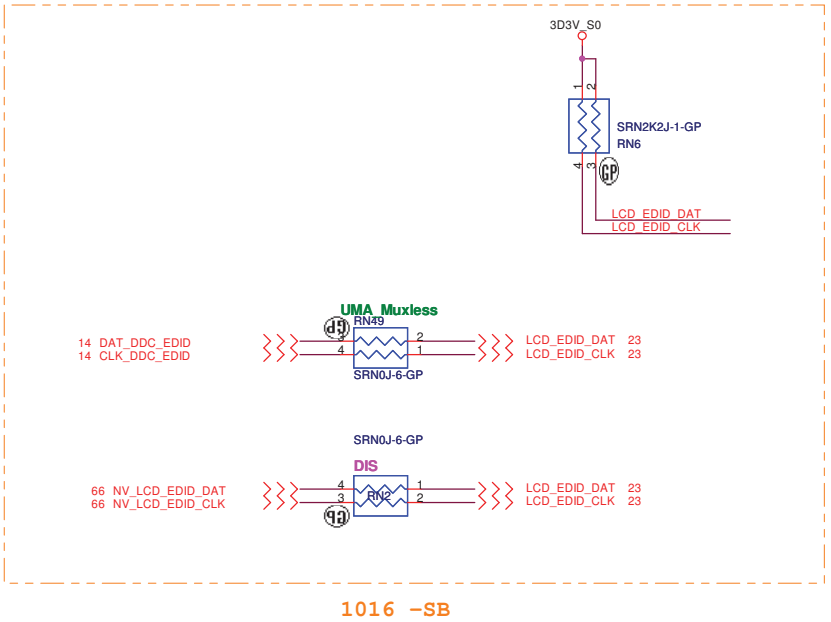
Title: DDRIII Socket DM2

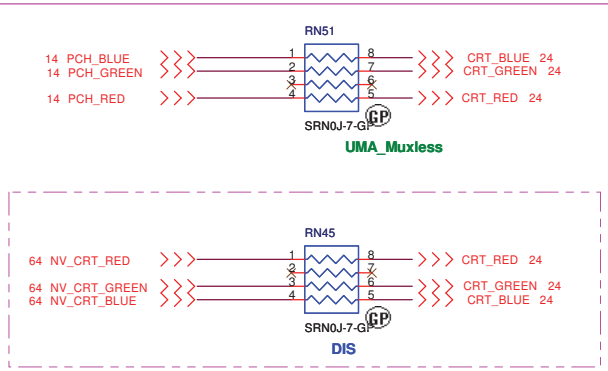
Size: A2 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 21 of 72









UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

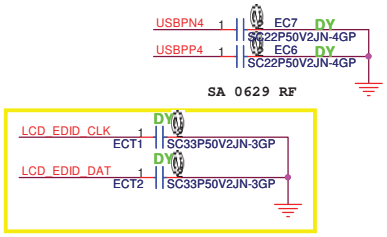
Title: Function

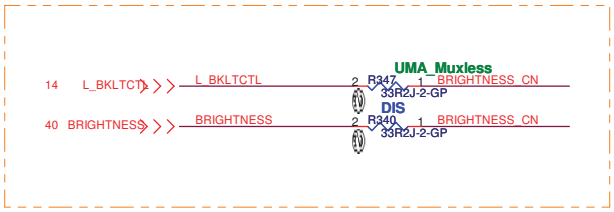
Size	Document Number	Rev
A3	HM42-CP	SC

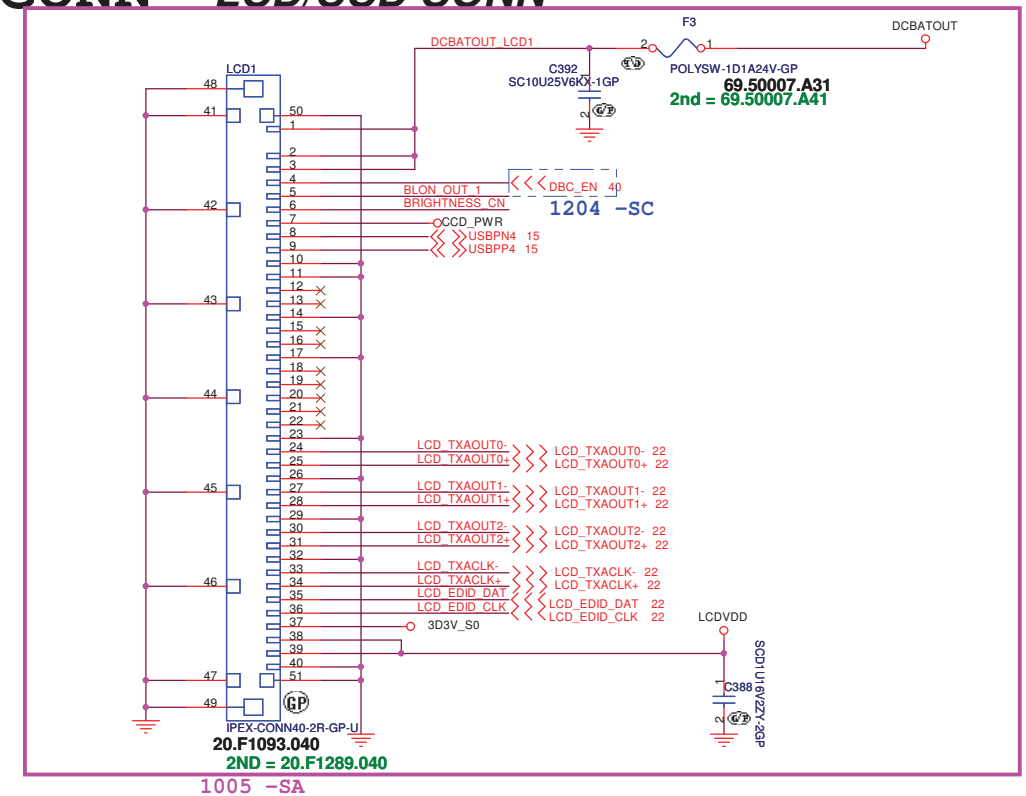
Date: Friday, January 22, 2010 Sheet 22 of 72

LCD/INVERTER/CCD CONN

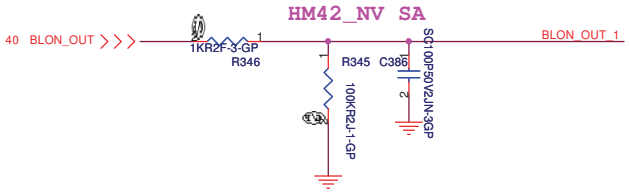
LCD/CCD CONN

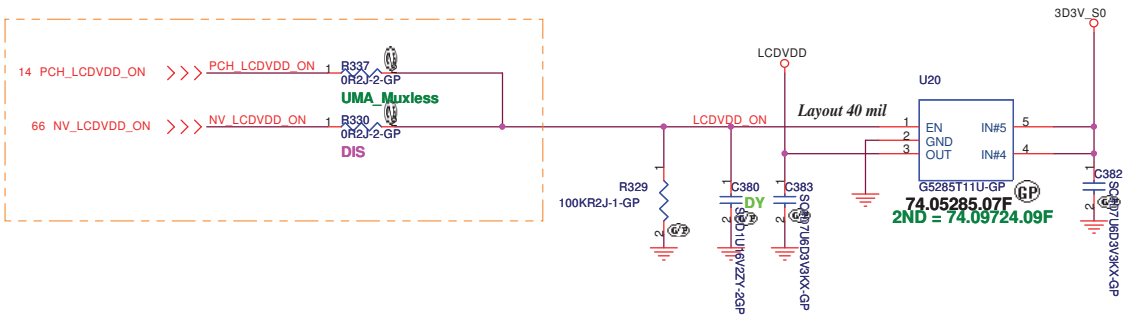




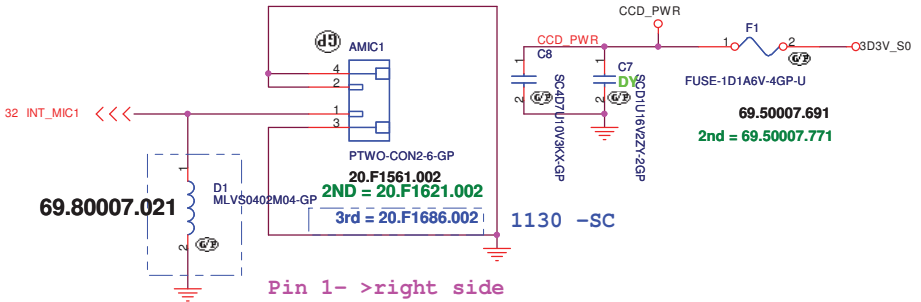


1005 -SA
define same as SJM50-PU,can use SJM50 Cable





Internal Mic

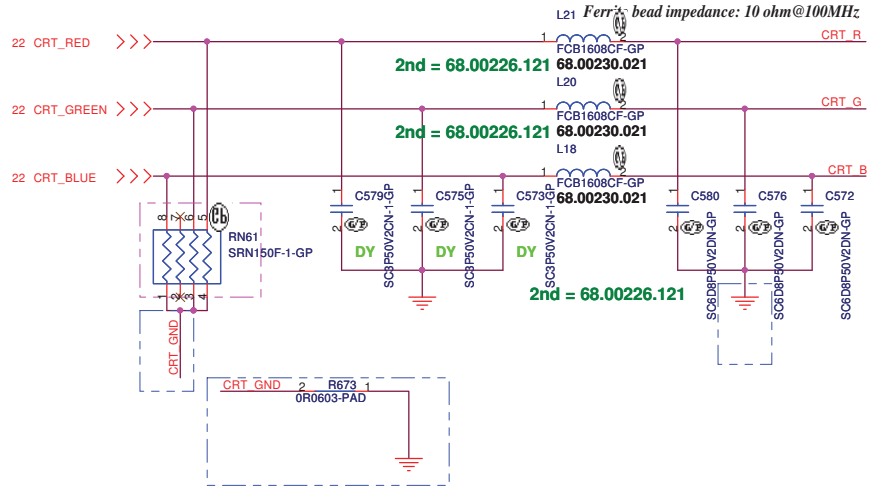


Pin 1- >right side
1209 -SC 20.F1240.002 Pin1->left side
request by EMI Aaron same as JV70-CP

Diserete N11M

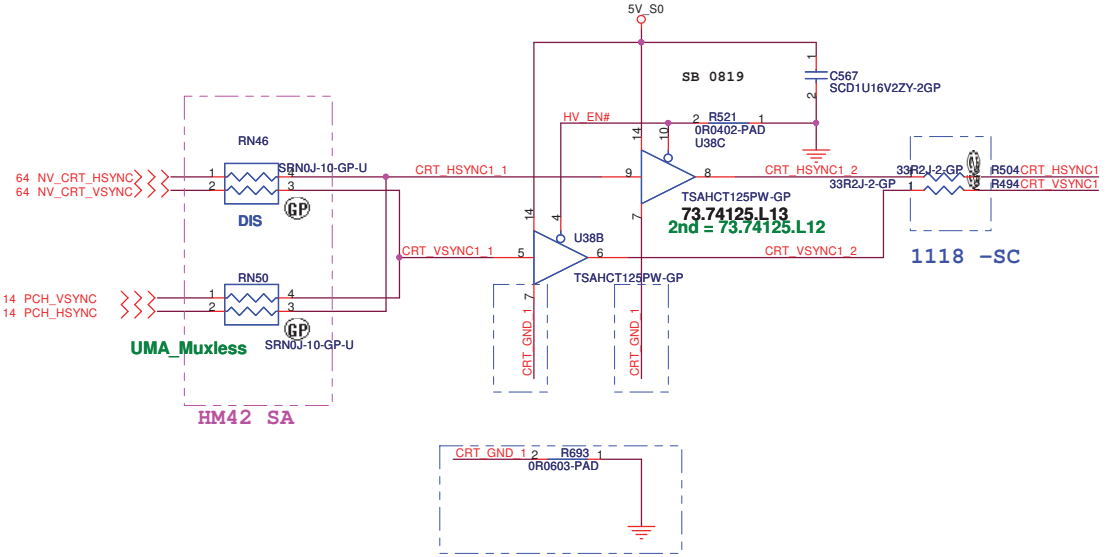
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 23 of 72	

Layout Note:
Place these resistors close to the CRT-out connector

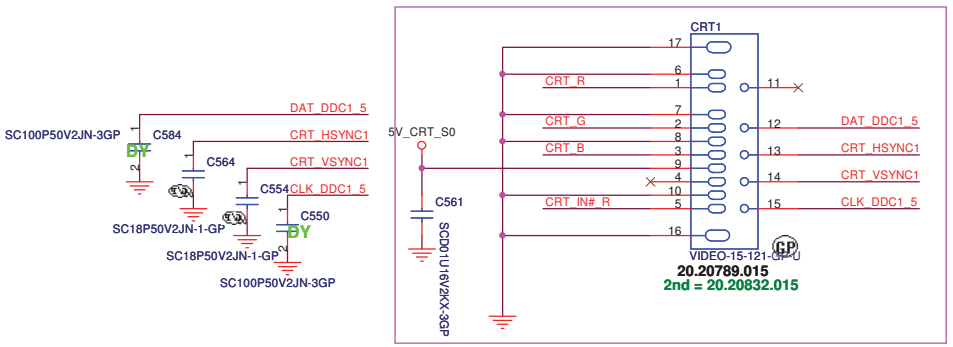


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

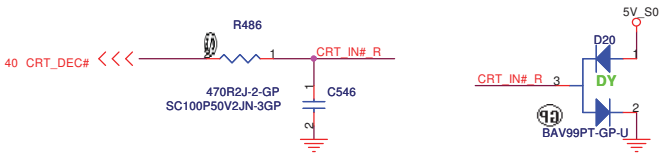
Hsync & Vsync level shift



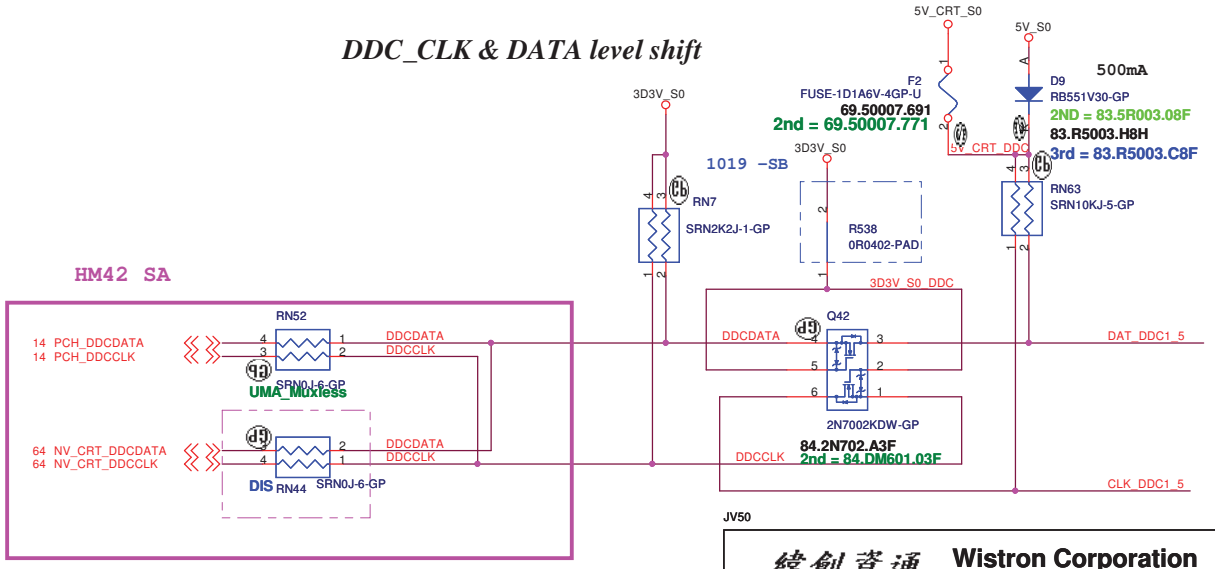
CRT I/F & CONNECTOR



HM42 CP NV Muxless

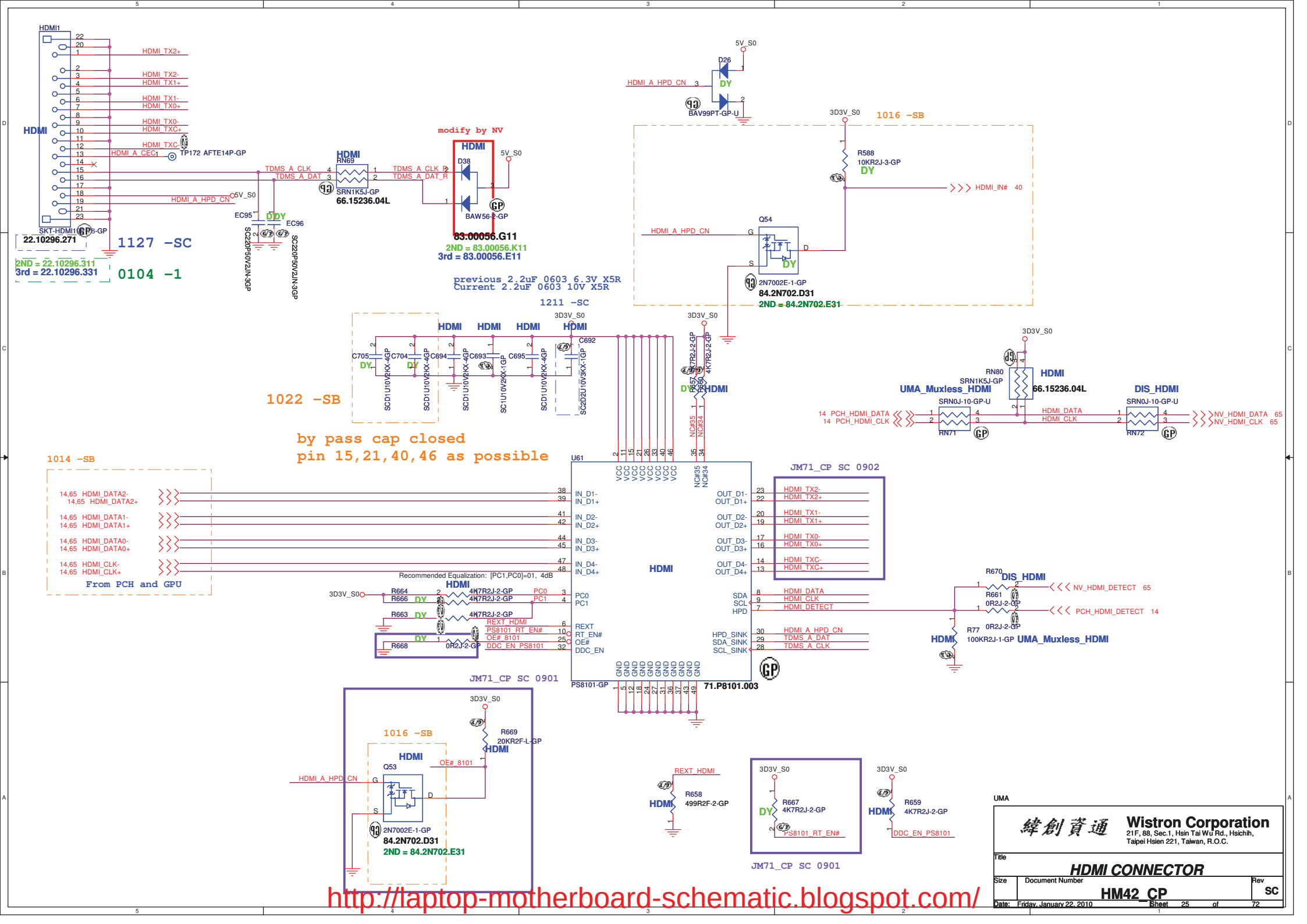


DDC_CLK & DATA level shift



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CRT CONN**		
Size	Document Number: **HM42-CP**	Rev: SC
Date: Friday, January 22, 2010	Sheet 24 of 72	



UMA

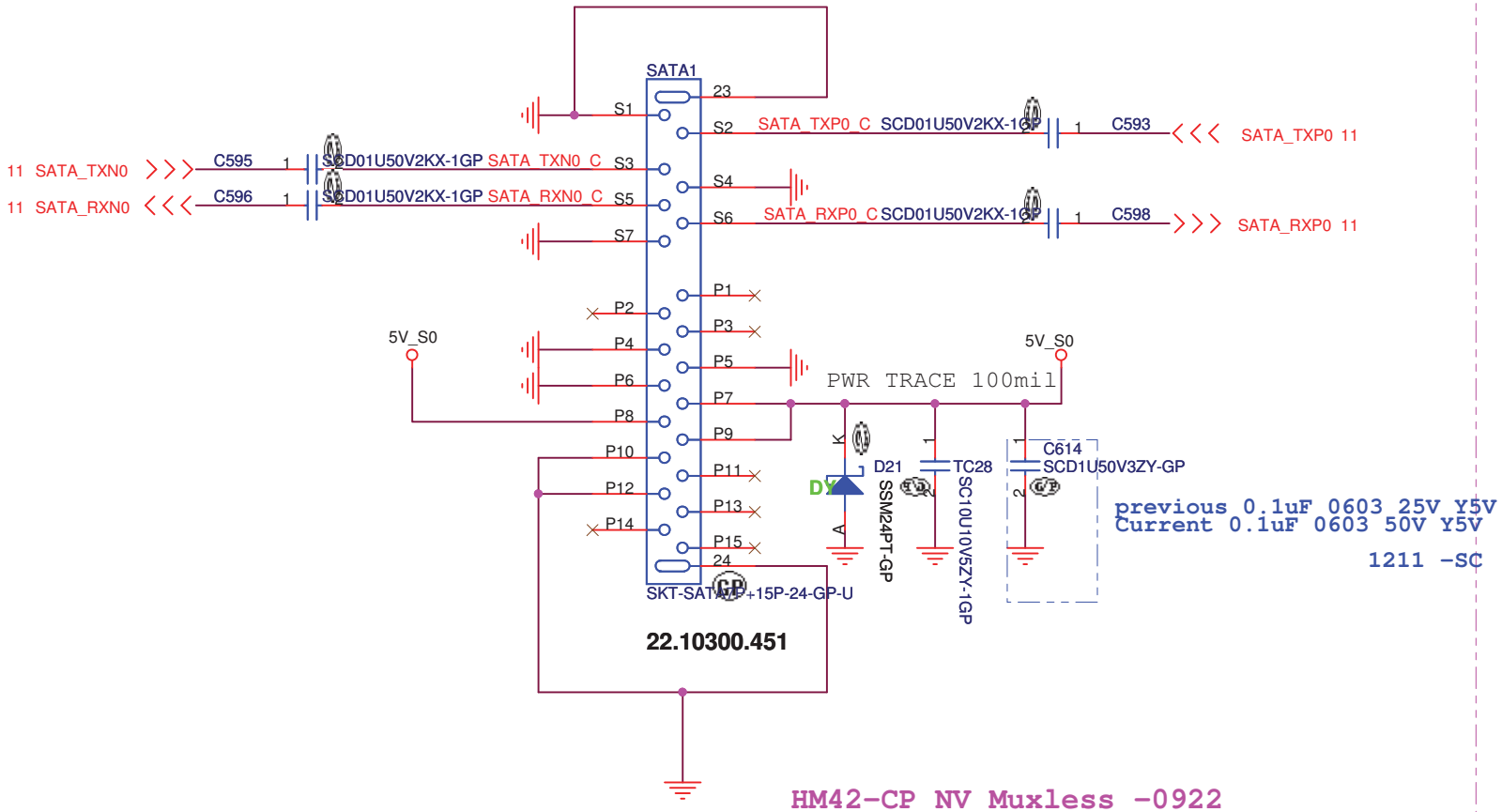
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

Size | Document Number: HM42_CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 25 of 72

SATA Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD CONN		
Size	Document Number: HM42-CP	Rev: SC
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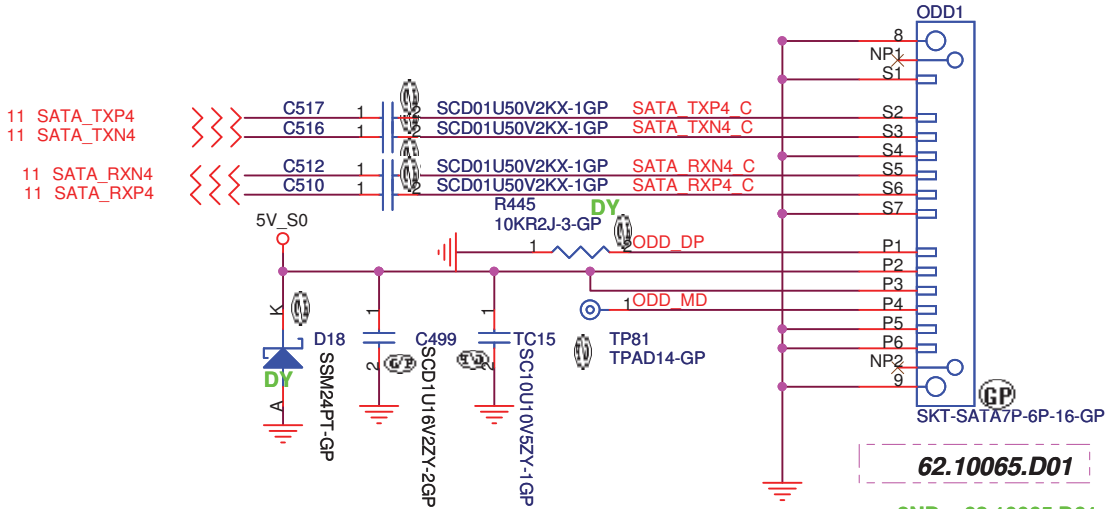
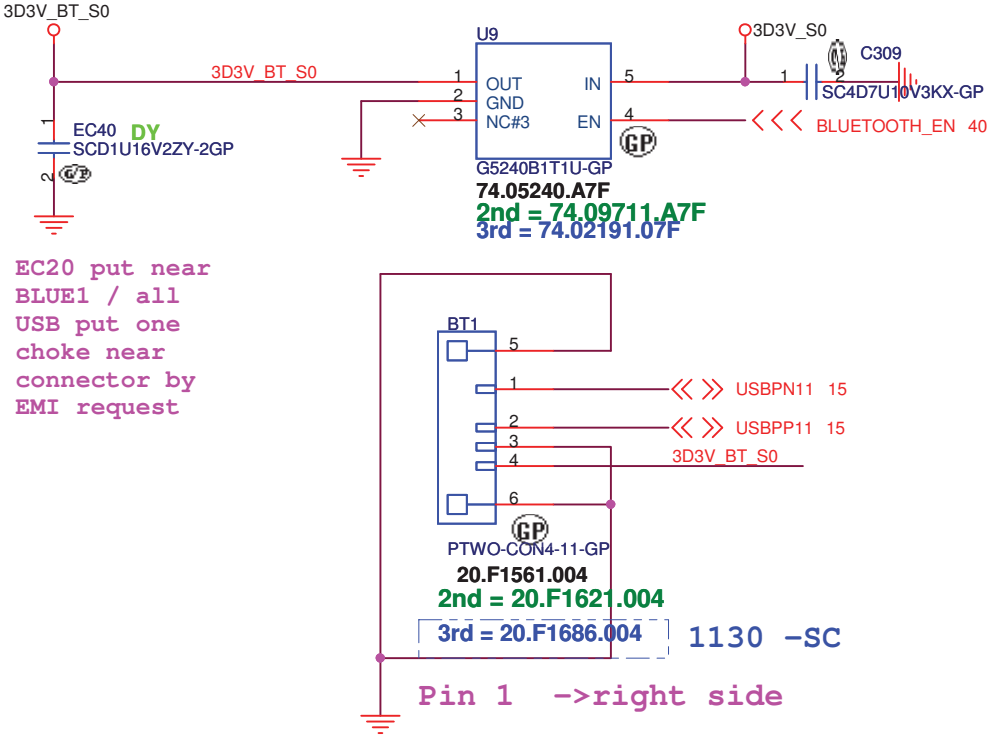
ODD Connector



UMA

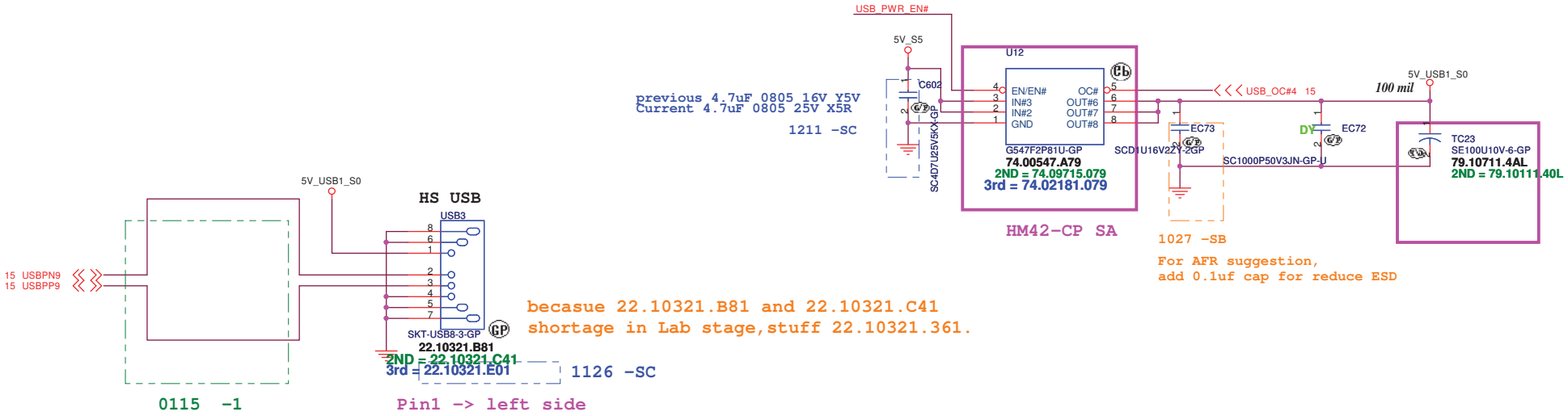
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ODD		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 27 of 72	

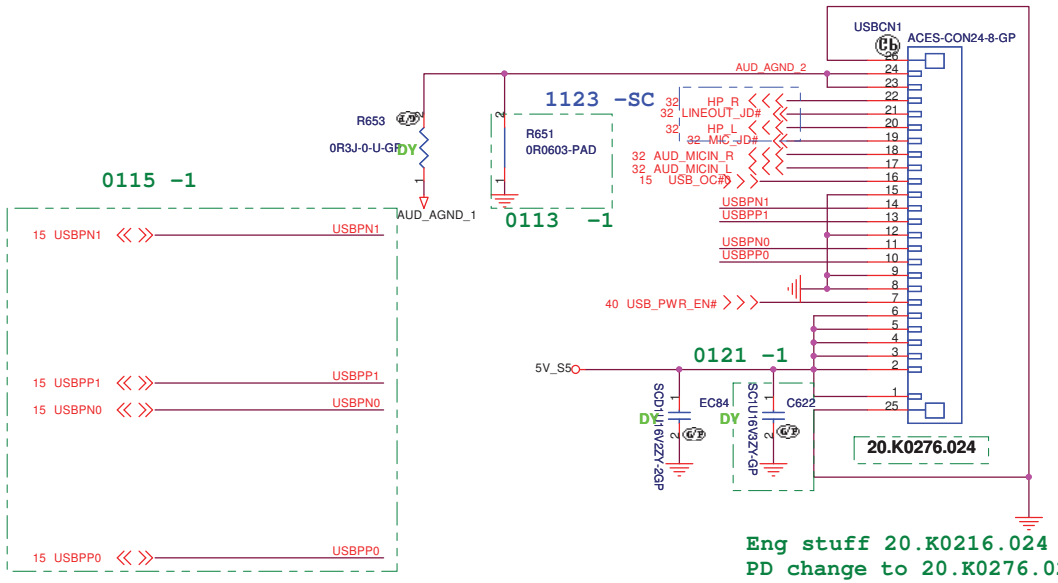
BLUETOOTH MODULE



JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 28 of 72	





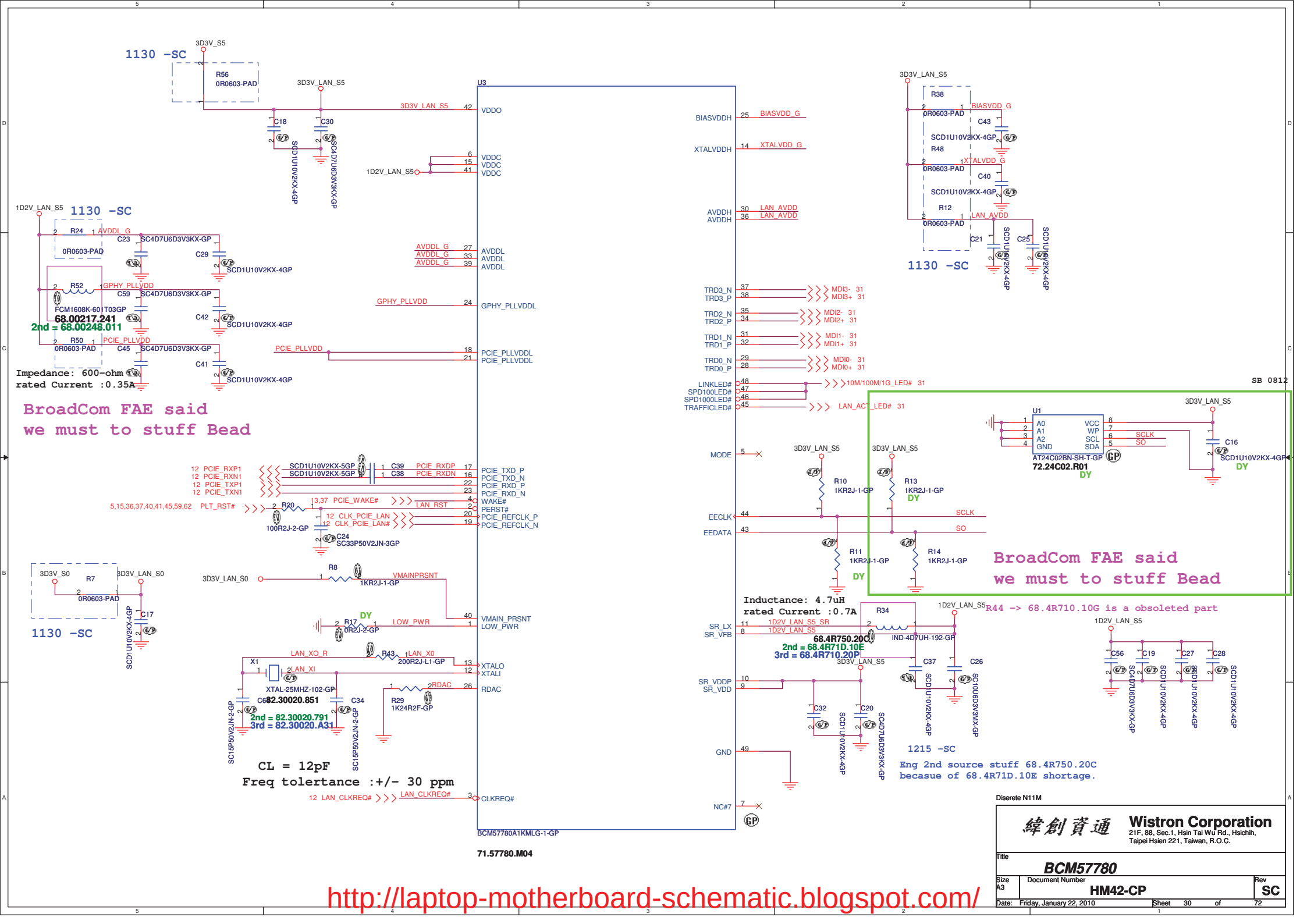
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and Audio CONN

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 29 of 72



Diserete N11M

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***BCM57780***
Size A3	Document Number **HM42-CP** Rev **SC**
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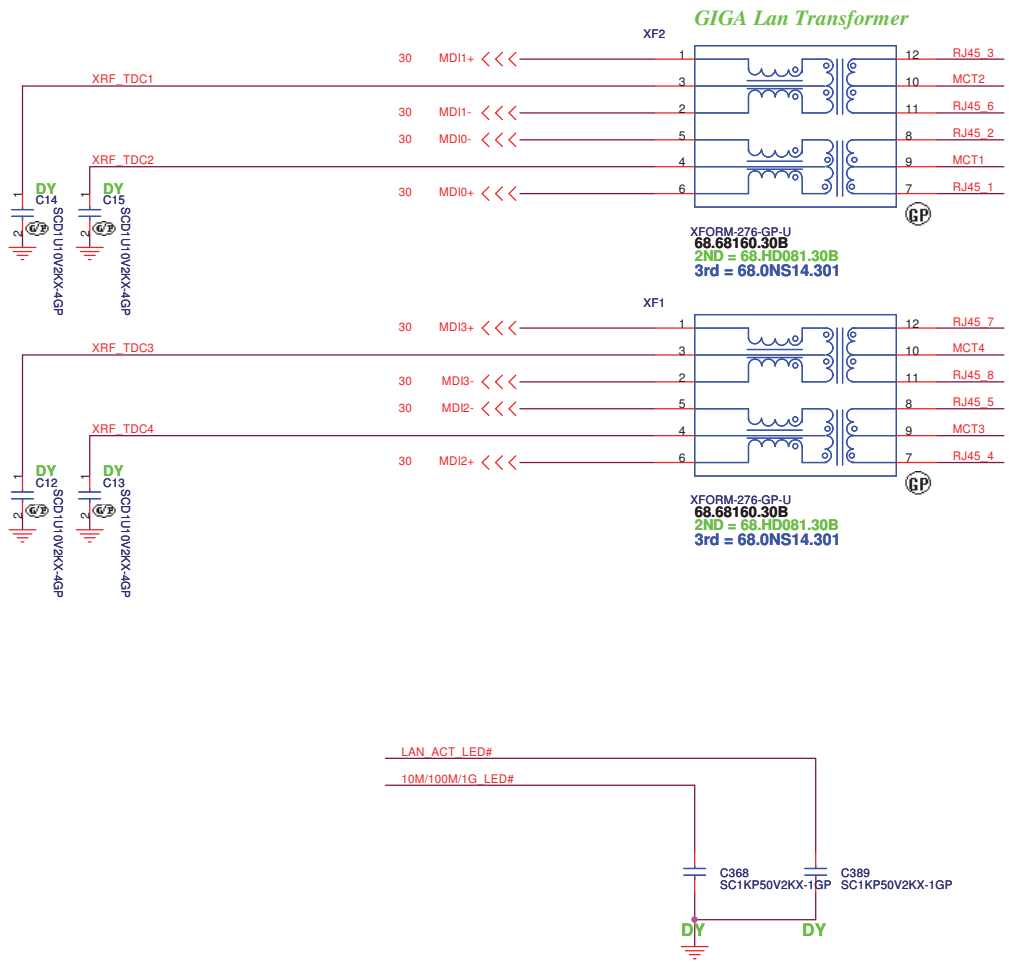
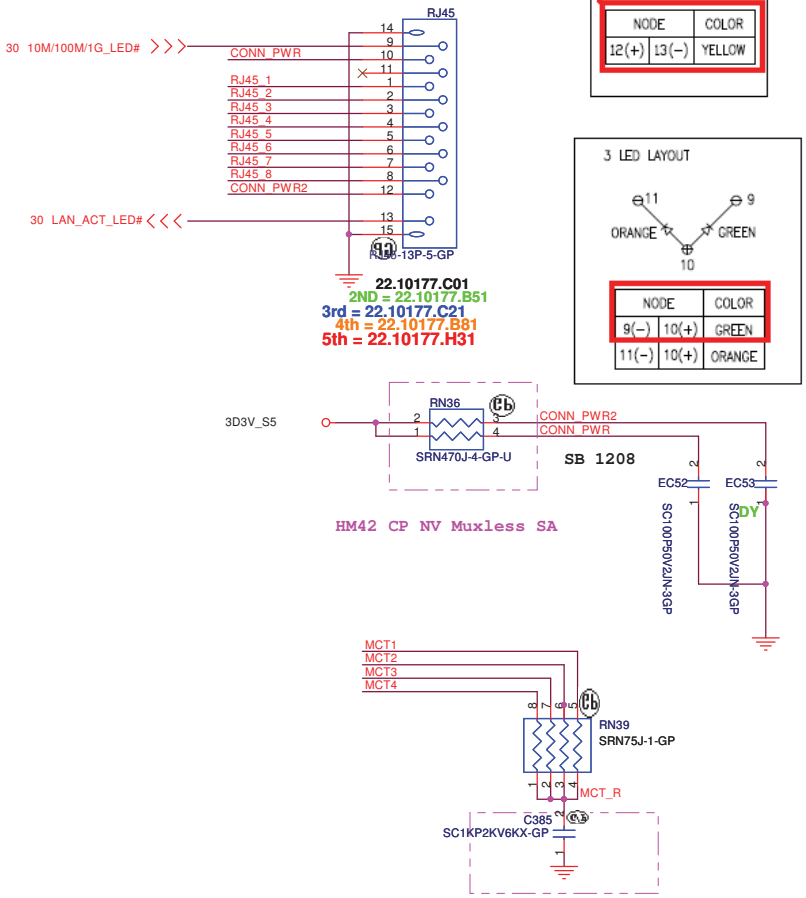
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

GIGA Lan Transformer

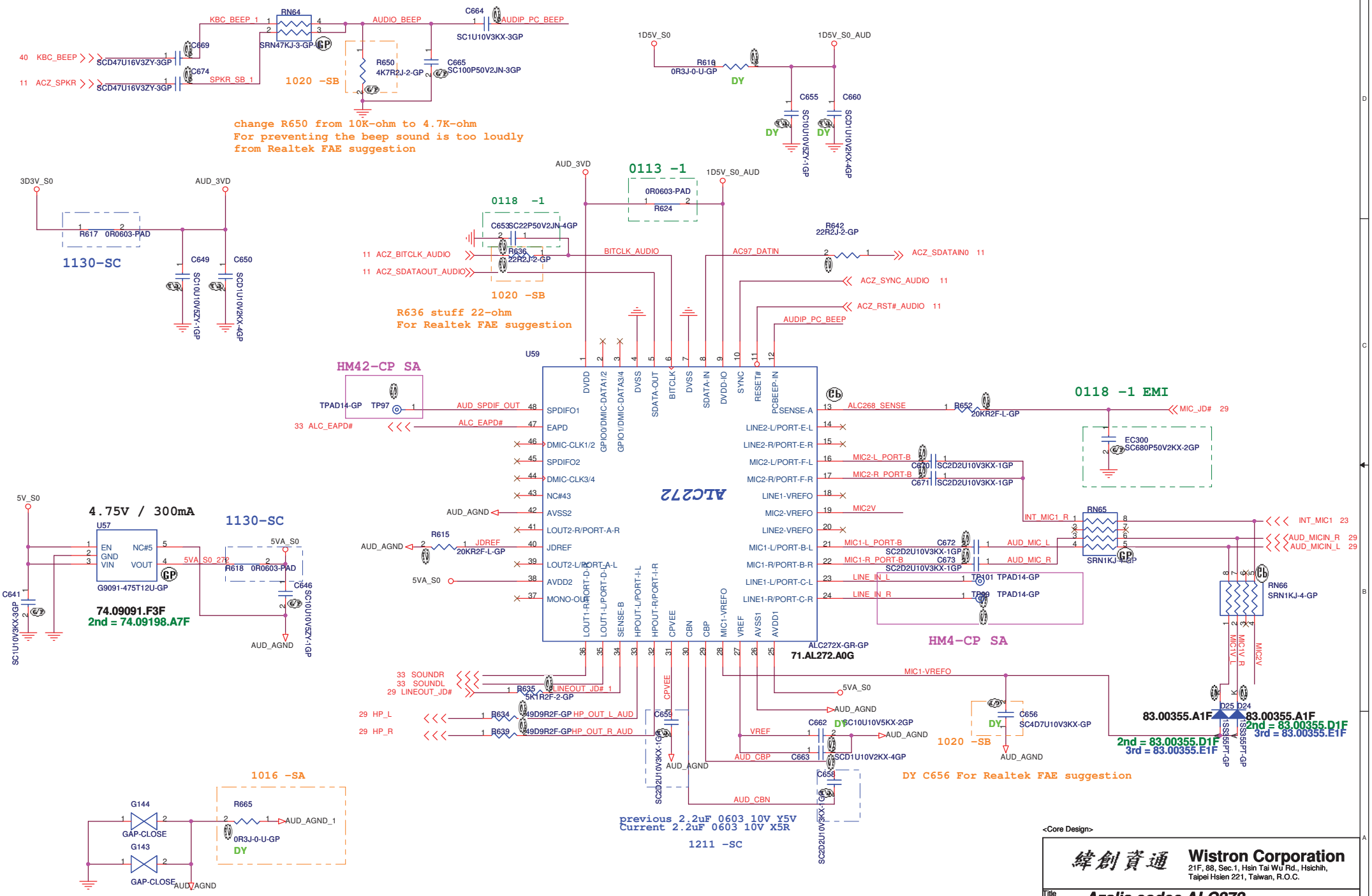




UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN CONN			
Size A3	Document Number HM42-CP		Rev SC
Date: Friday, January 22, 2010	Sheet 31	of	72



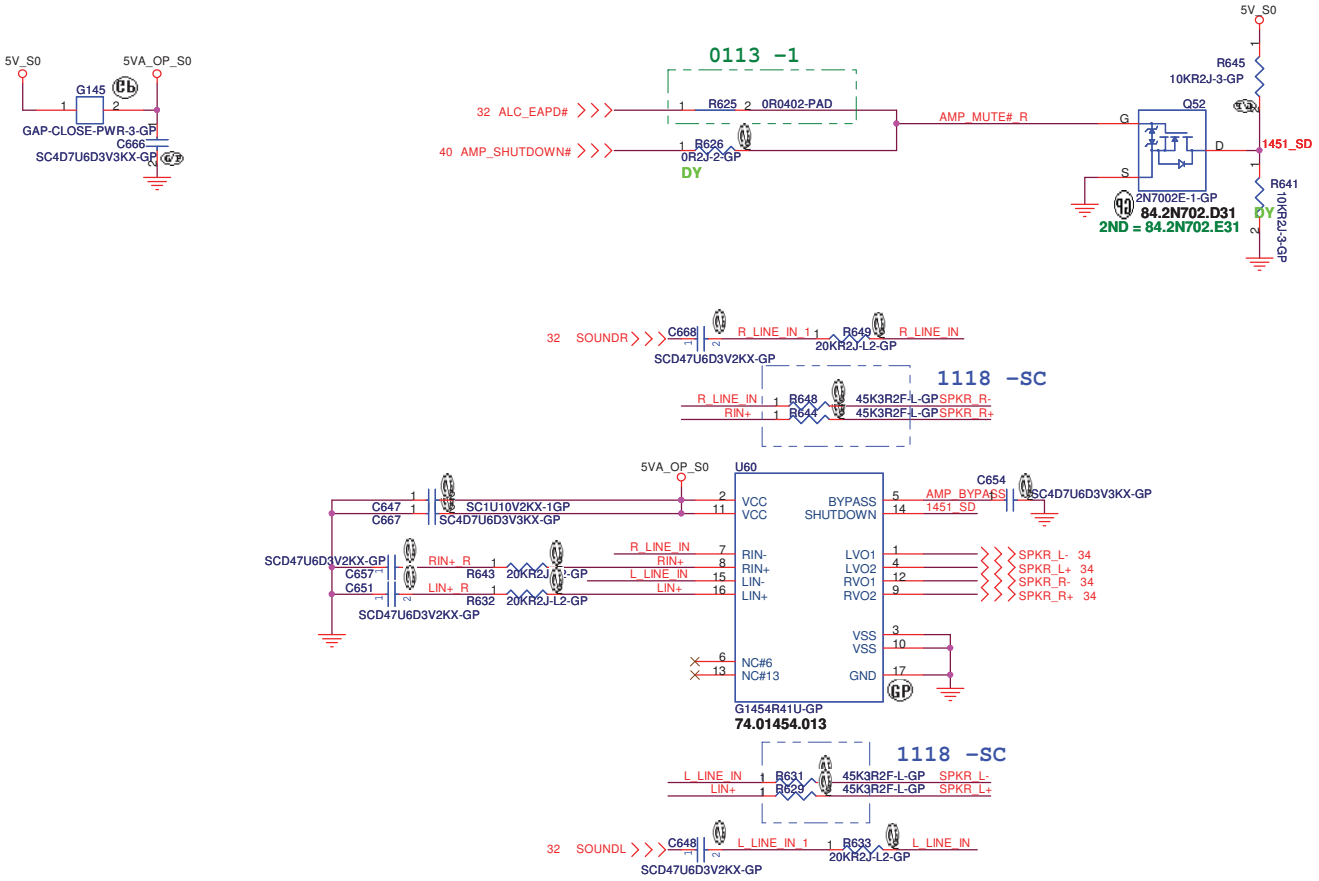
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC272

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 32 of 72




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.446^2/4=1.5W
```

UMA

緯創資通 **Wistron Corporation**
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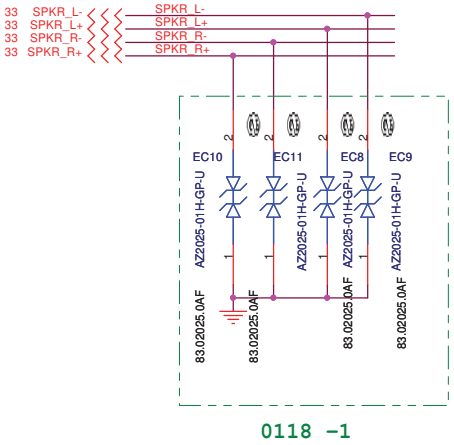
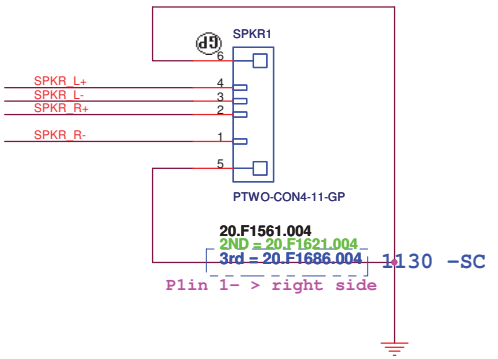
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 33 of 72	

Internal Speaker





Diserete N11M

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

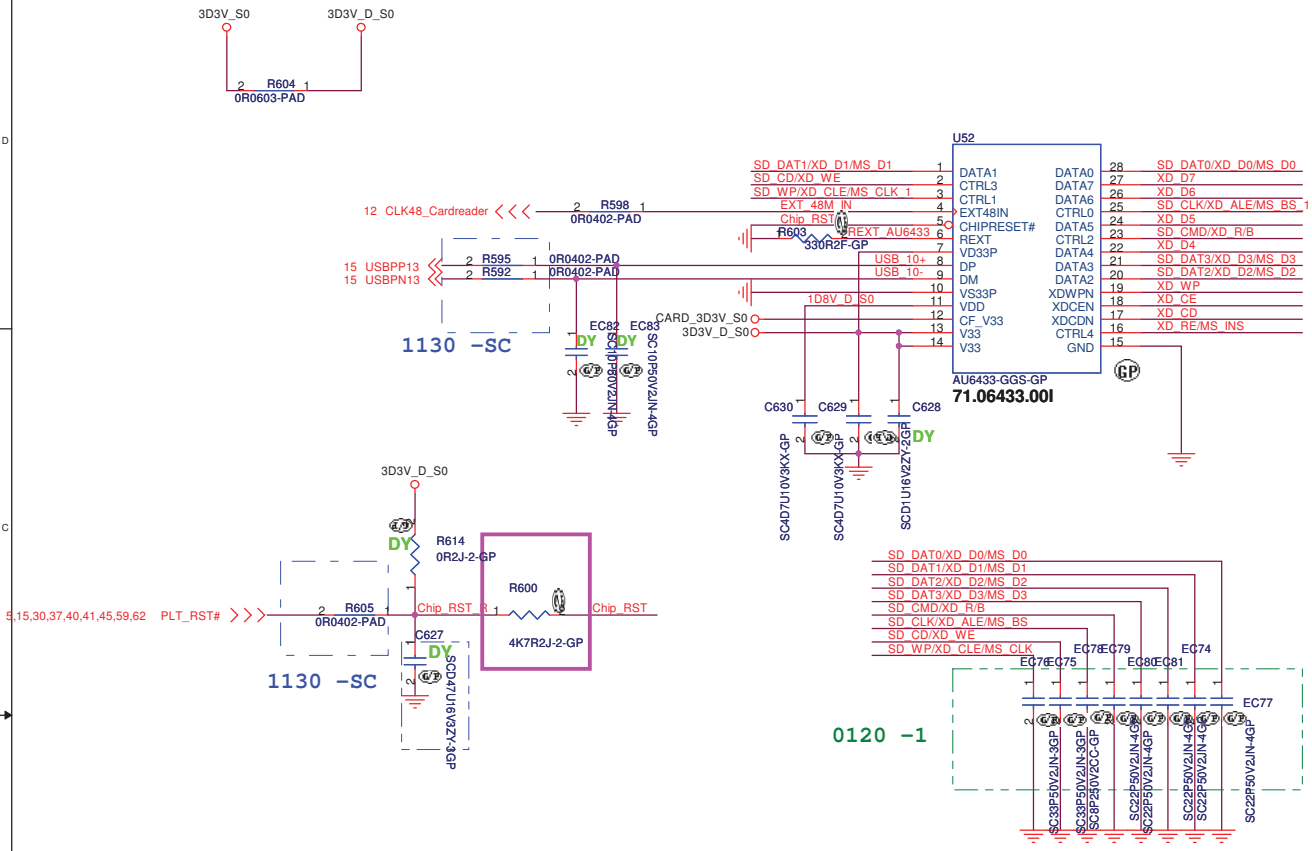
Title	AUDIO SPEARK	
Size	Document Number HM42-CP	Rev SC
Date: Friday, January 22, 2010	Sheet 34 of 72	

JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Resrve_ MDC

Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 35 of	72

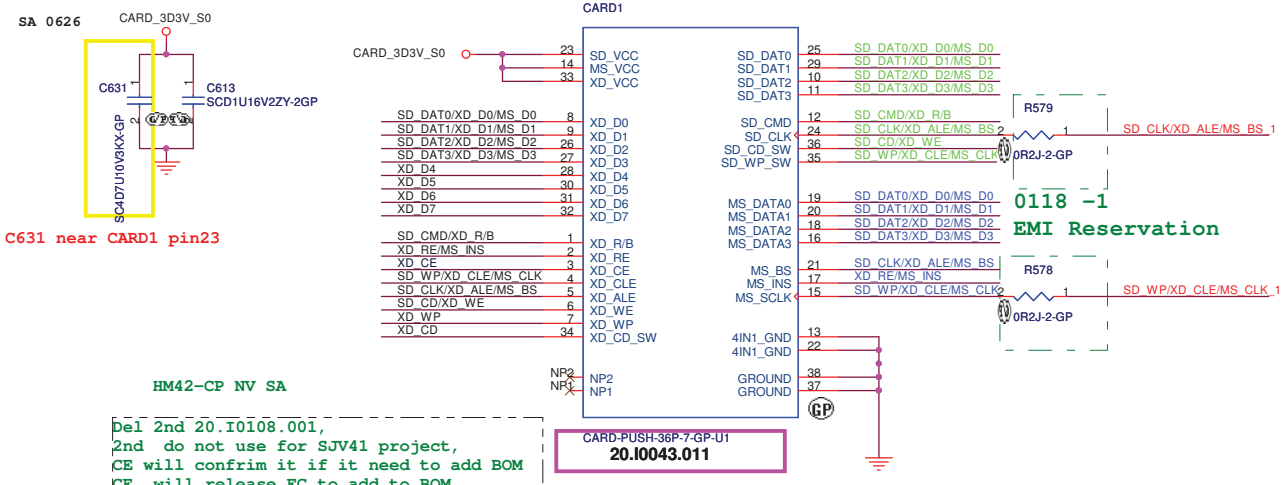


Pin	SD Mode	
	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1 xD-R/B			2P
P2 xD-RE			3P
P3 xD-CE			4P
P4 xD-CLE			5P
P5 xD-ALE			6P
P6 xD-WE			7P
P7 xD-WP			8P
P8 xD-D0			10P
P9 xD-D1			11P
P10 SD-DAT2	9P		
P11 SD-DAT3	1P		
P12 SD-CMD	2P		
P13 4in1-GND	3P/6P	1P/10P	1P/9P
P14 MS-VCC		9P	
P15 MS-SCLK		8P	
P16 MS-DATA3		7P	
P17 MS-INS		6P	
P18 MS-DATA2		5P	
P19 MS-DATA0		4P	

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

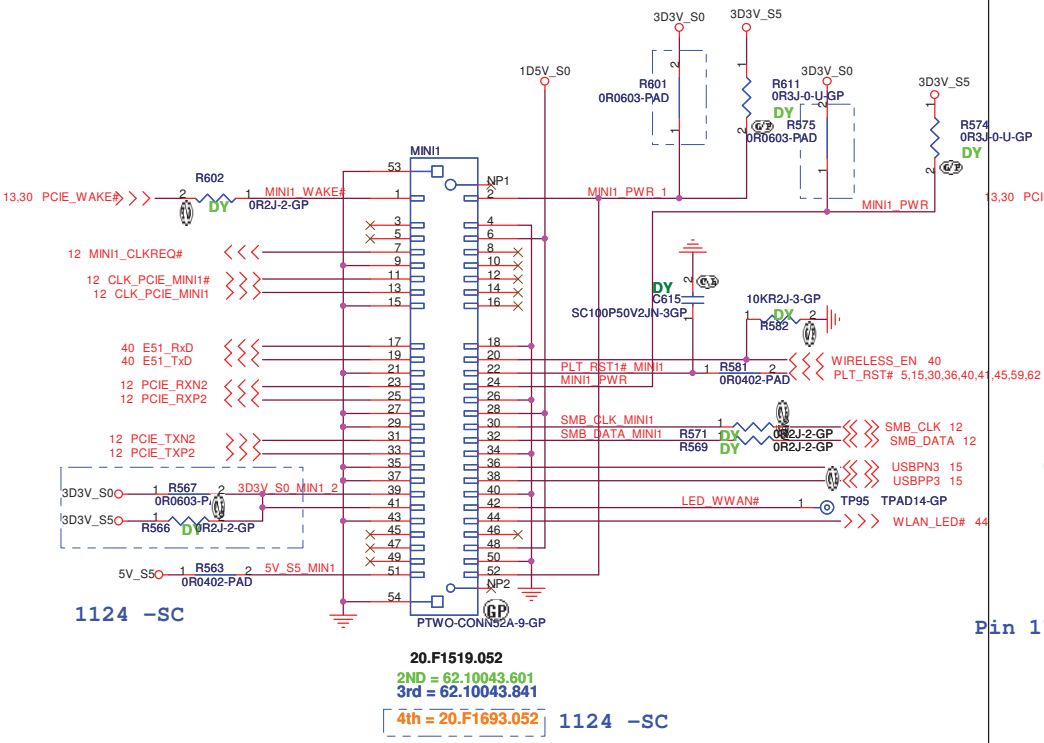
Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2.7V - 3.6V)
10	VSS	Vss

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

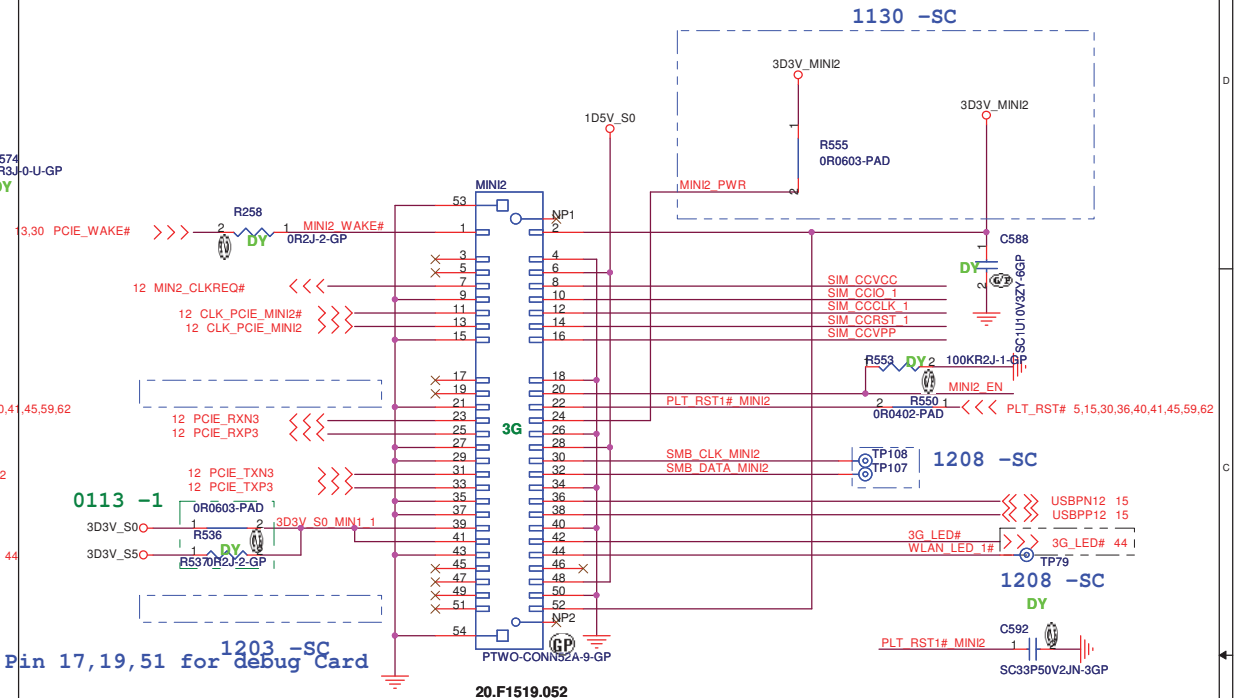
Title: Cardreader
Size: | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 36 of 72

Mini Card Connector(WLAN)
Support debug-card

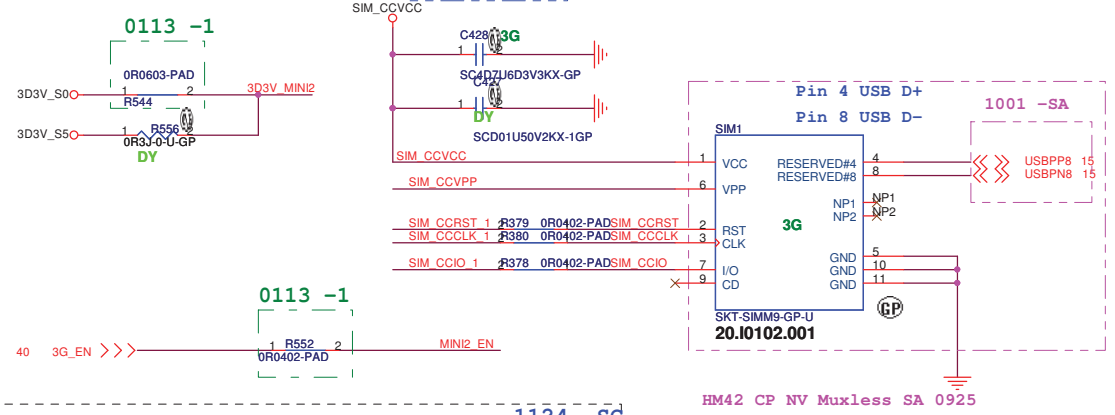


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC

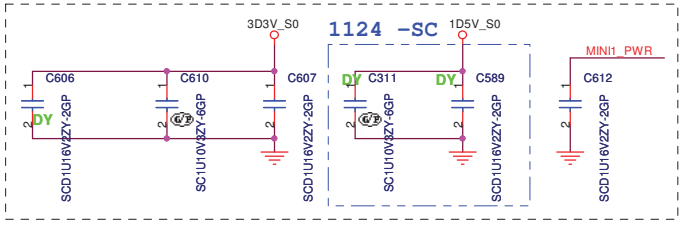
Mini Card Connector(Robson2 and 3G)

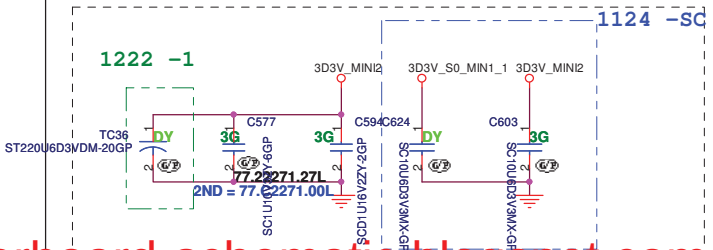


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC



Place near MINI1





Diserete N11M

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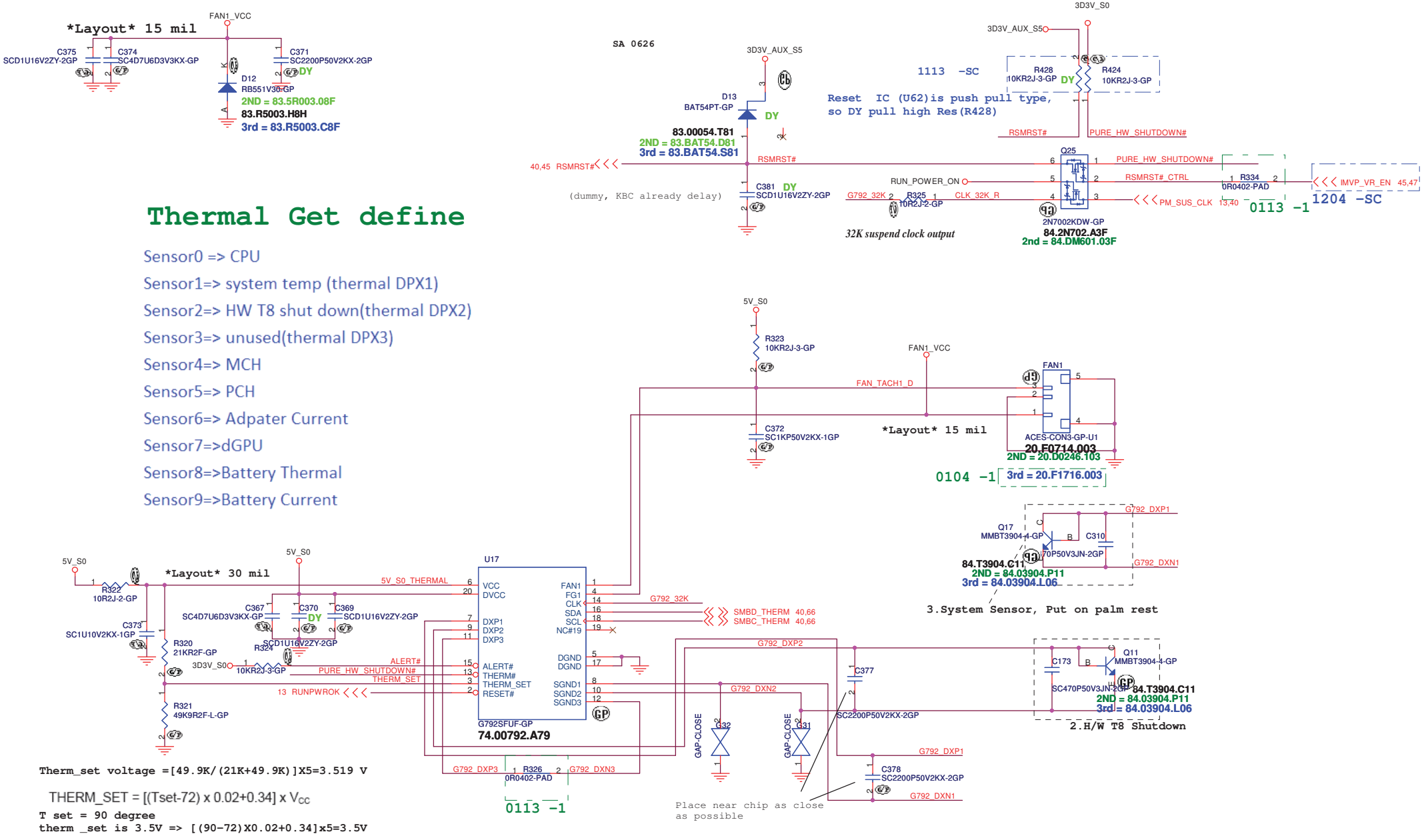
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 37 of 72



UMA

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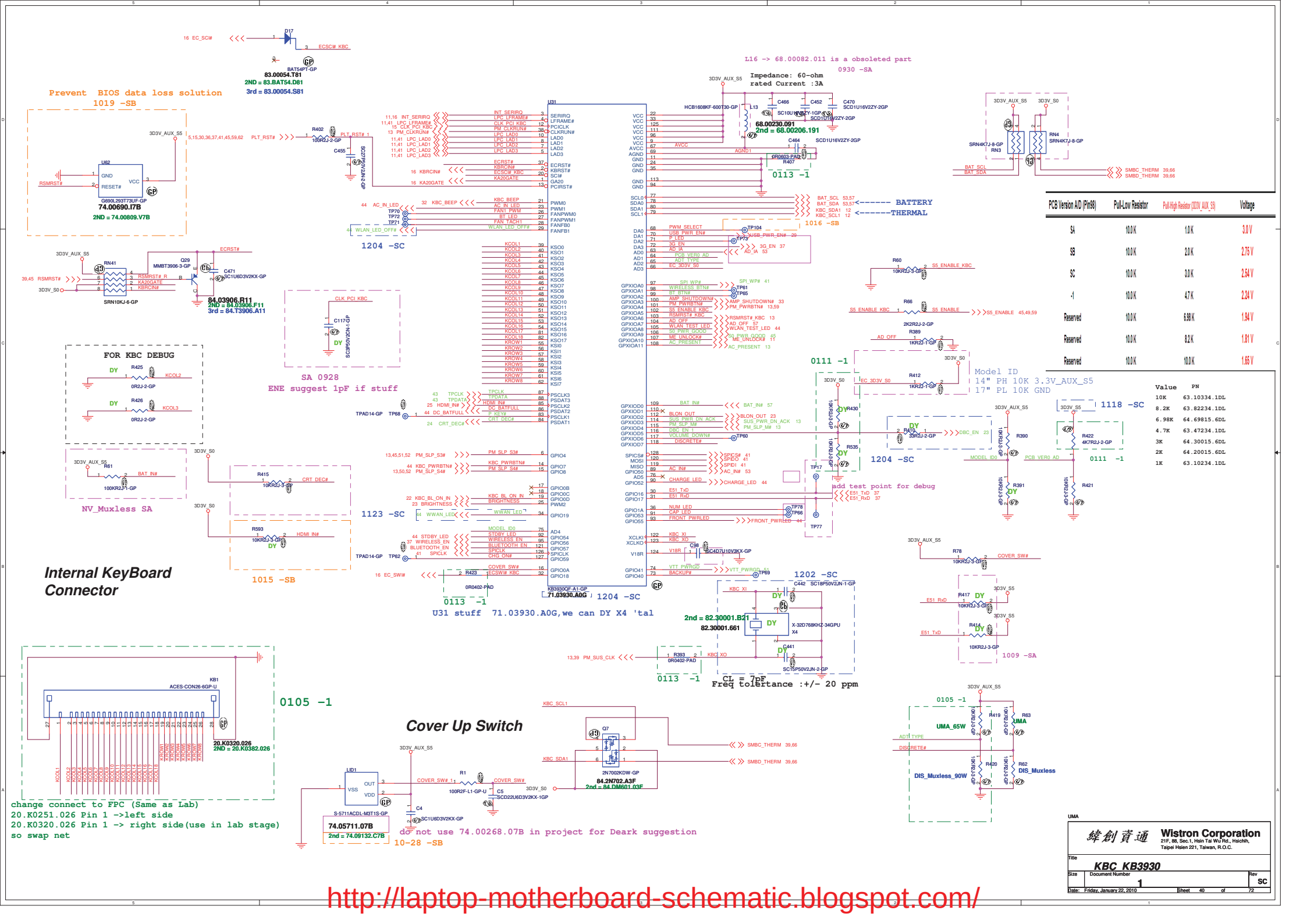
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

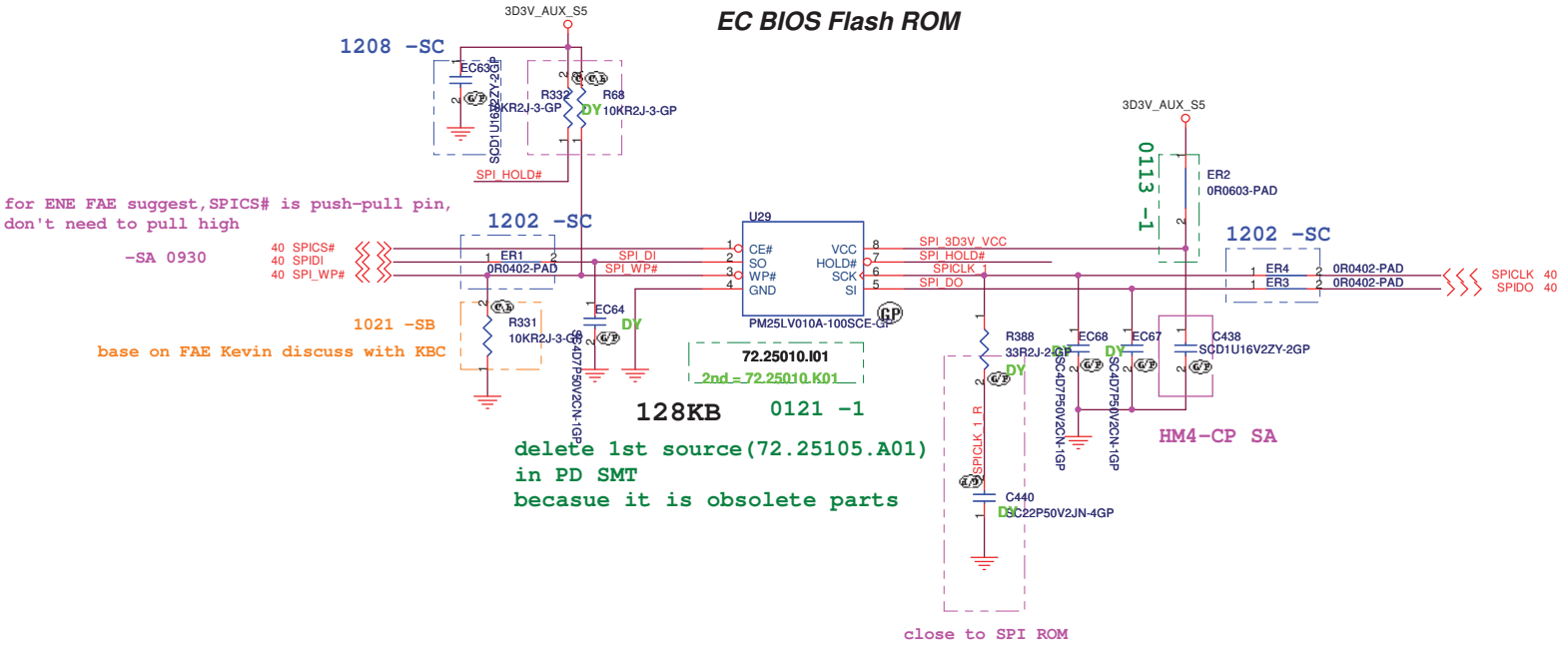
Title: Thermal/Fan Connector

Size | Document Number: HM42-CP | Rev: SC

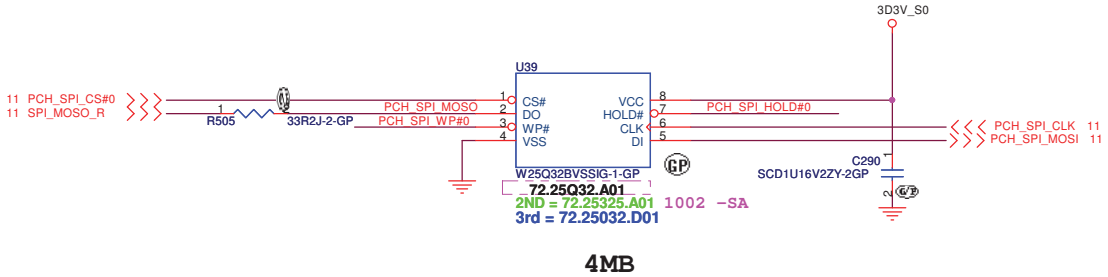
Date: Friday, January 22, 2010 | Sheet 39 of 72

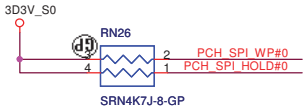


EC BIOS Flash ROM

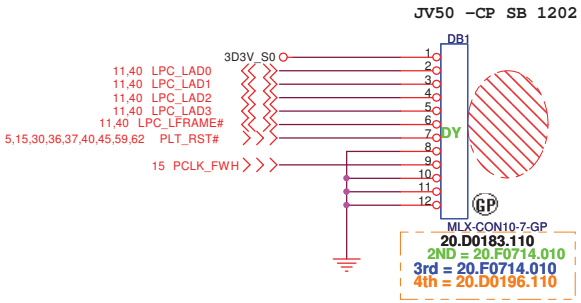


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



Lab only stuff 4th source(20.D0196.110)
Eng and PD DY DB1

Diserete N11M

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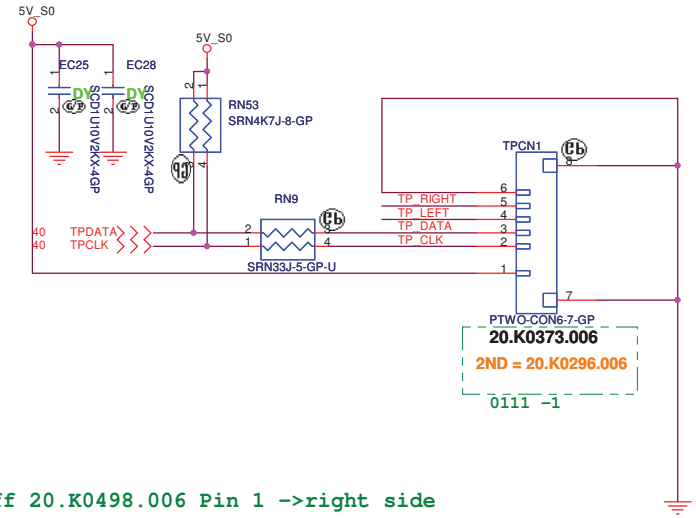
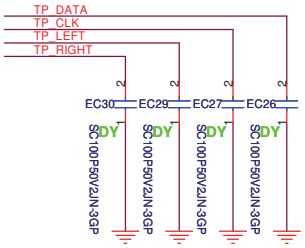
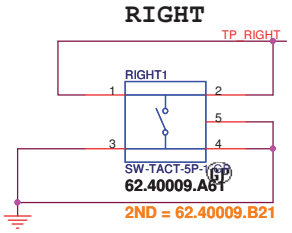
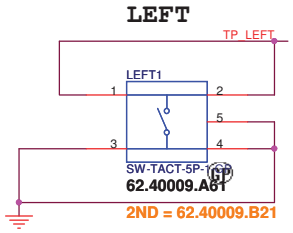
Title		
BIOS		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 41 of 72	





Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



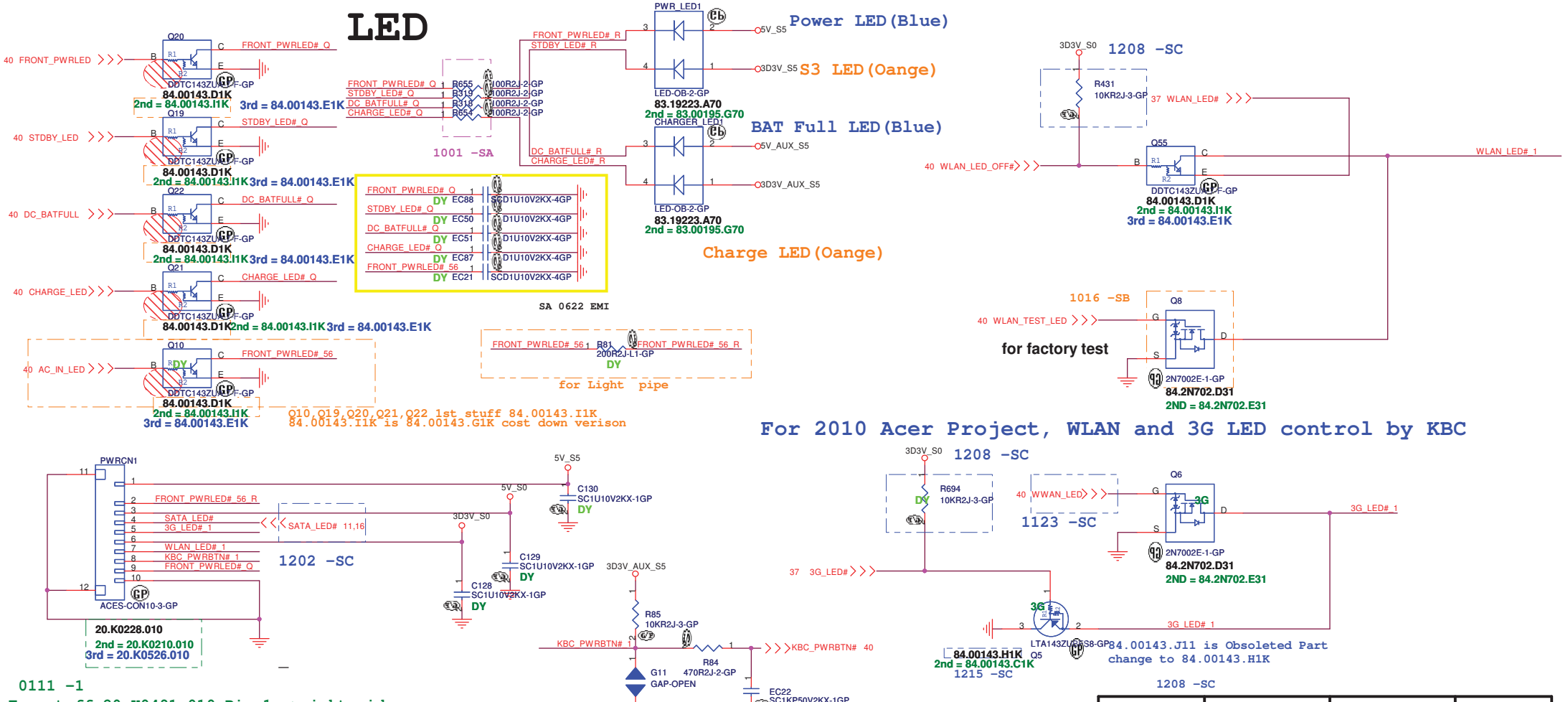


Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD
Size | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 43 of 72

LED



For 2010 Acer Project, WLAN and 3G LED control by KBC

0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

84.00143.H1K ->N11P Samsung/Hynix SKU
84.00143.C1K->N11M Hynix SKU

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

<Core Design>

緯創資通 Wistron Corporation
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Title: LED&POWERBD CONN
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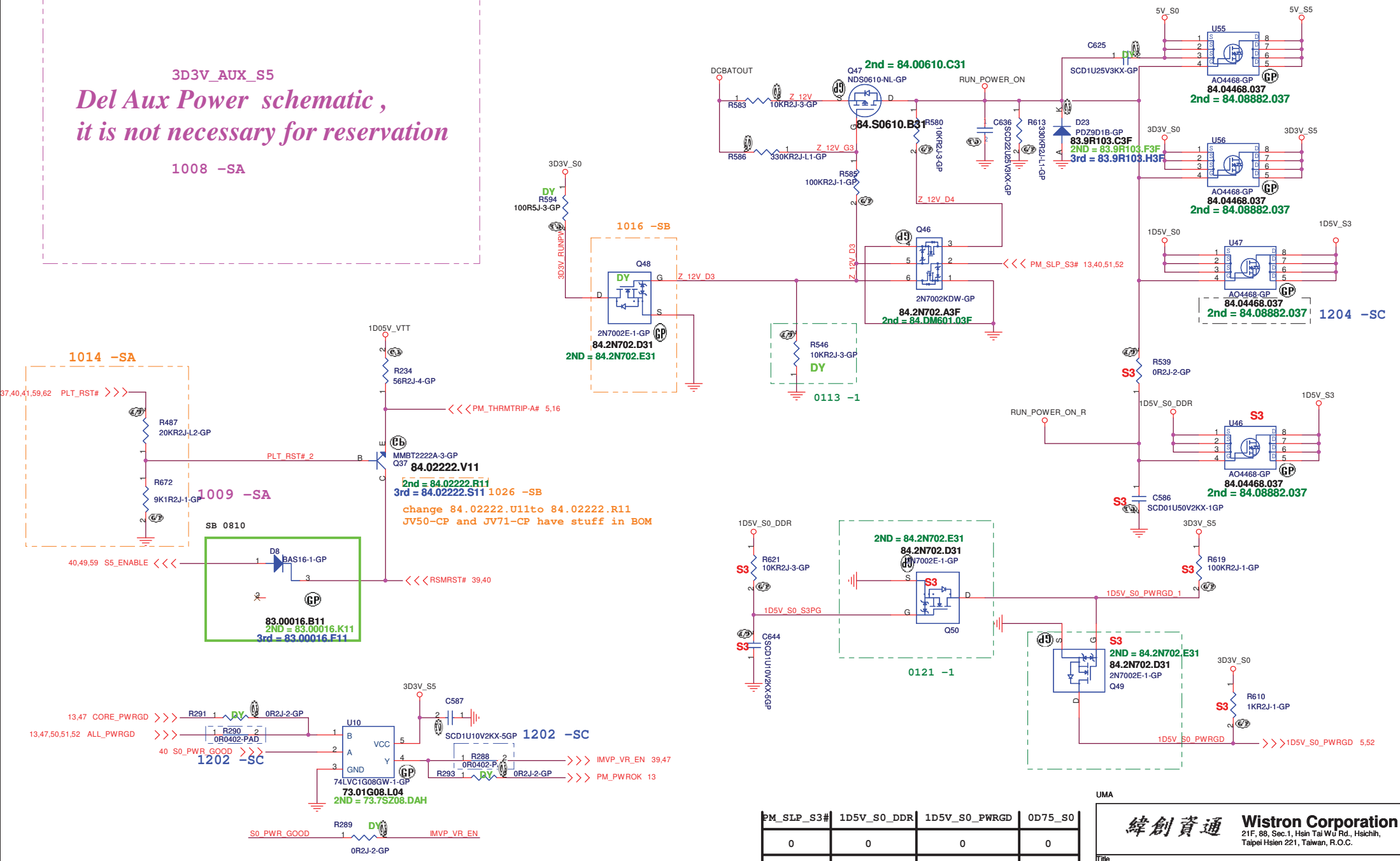
Date: Friday, January 22, 2010 | Sheet 44 of 72

Run Power

3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

Wistron Corporation
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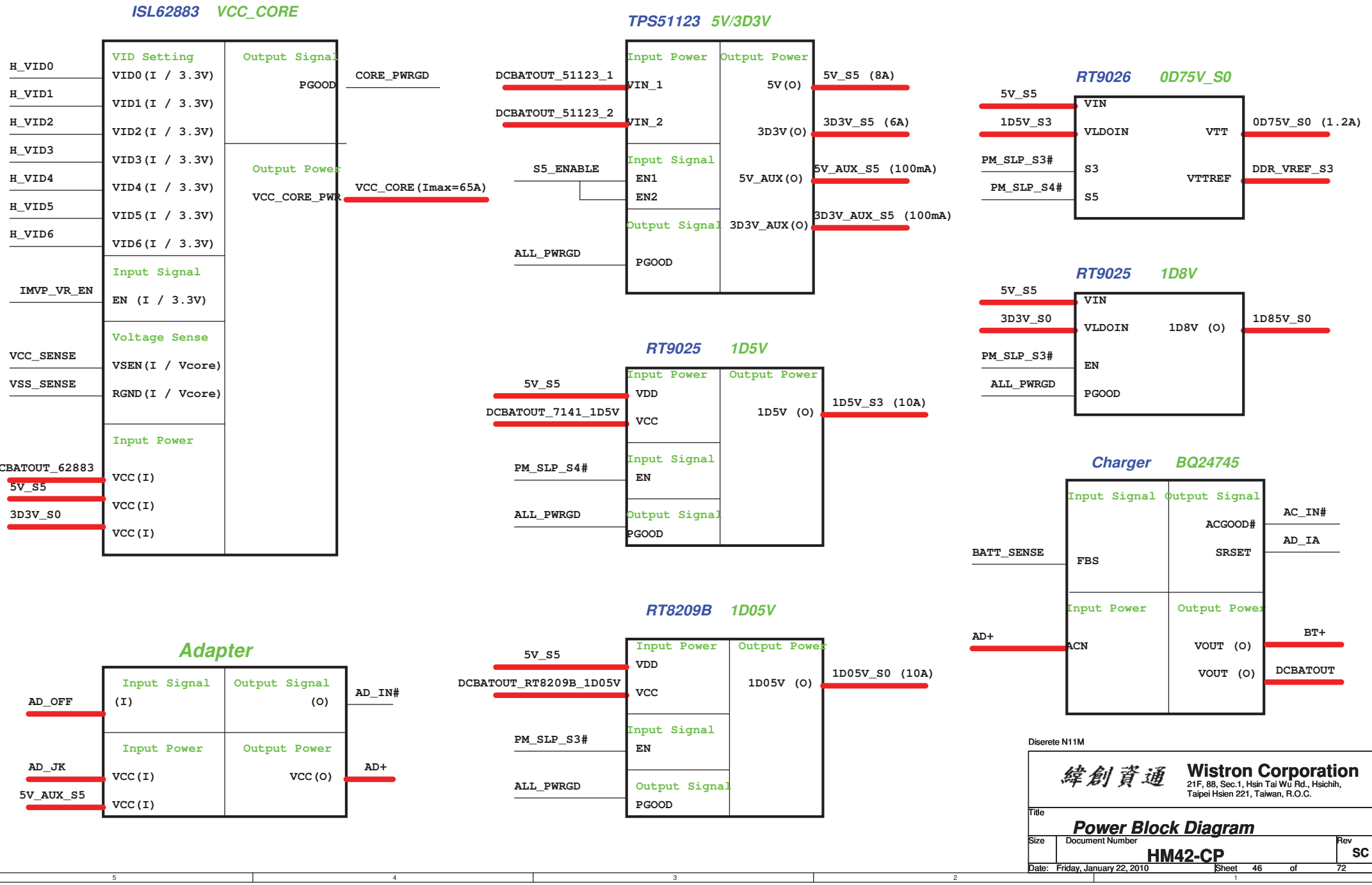
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size: | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 45 of 72



Diserete N11M

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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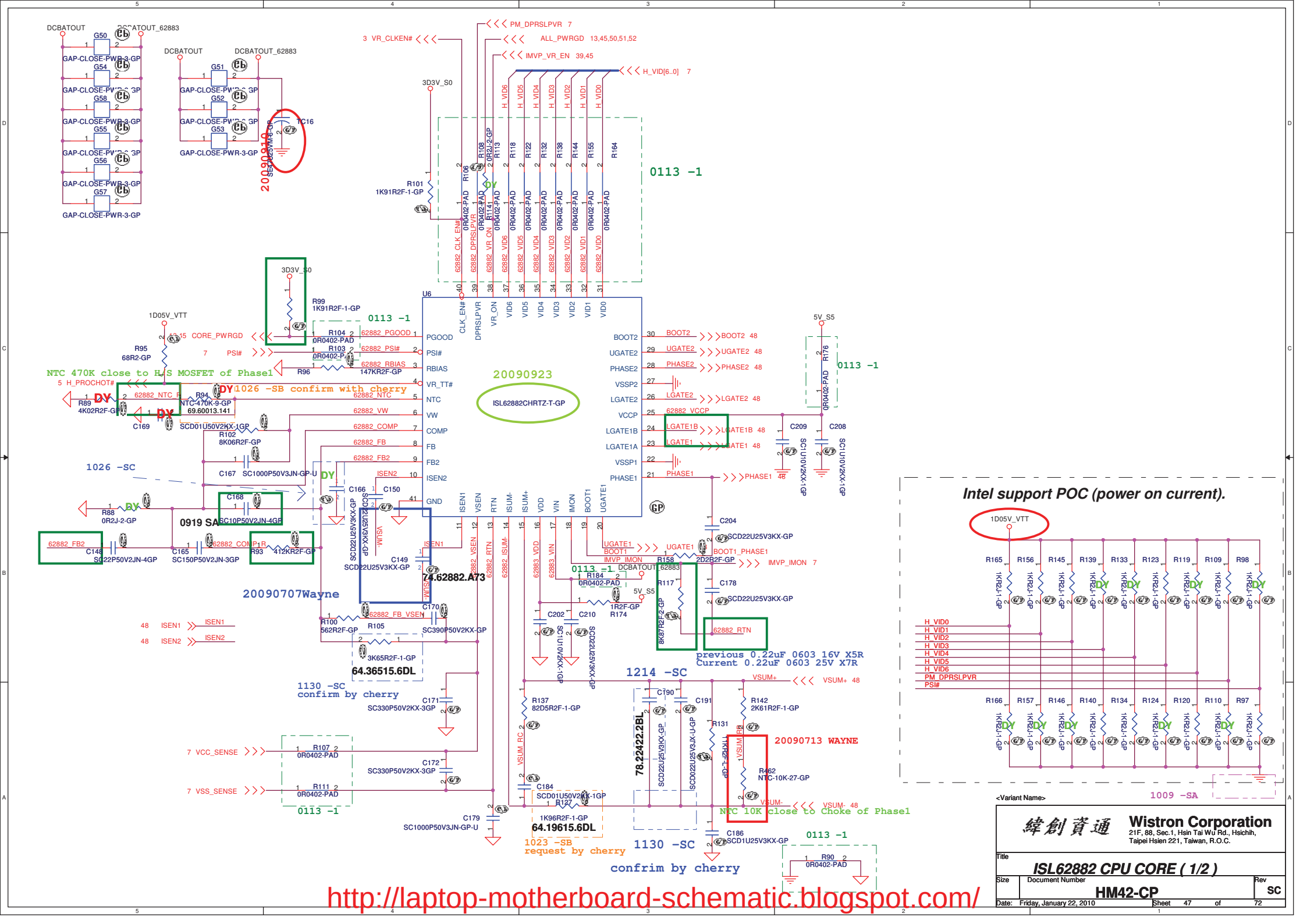
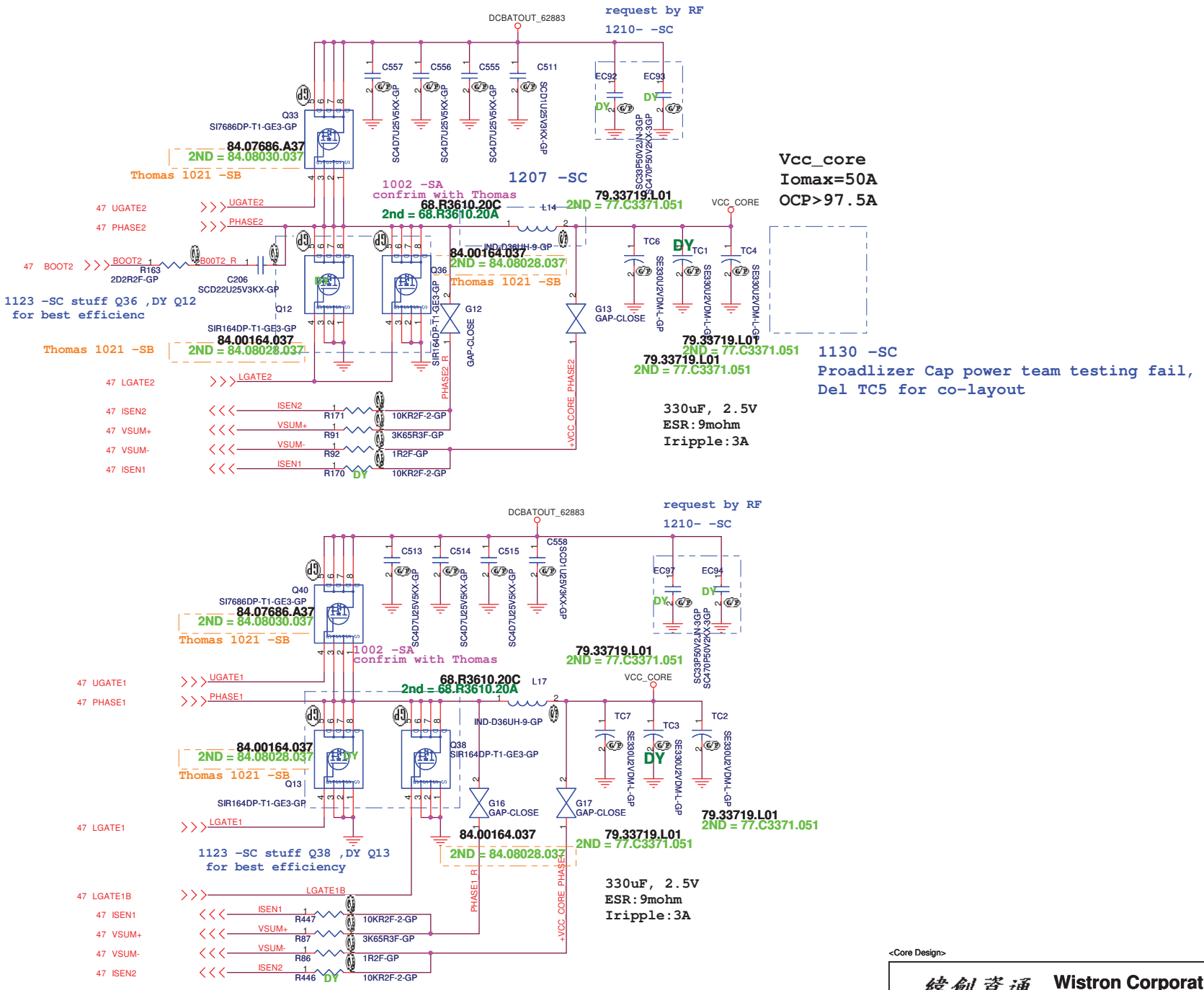
Date: Friday, January 22, 2010 Sheet 46 of 72


DCBATOUT
DCBATOUT_62883
GAP-CLOSE-PWR-3-GP
TC16
20090910
3D3V_S0
PM_DPRSLPVR 7
ALL_PWRGD 13,45,50,51,52
IMVP_VR_EN 39,45
H_VID[6..0] 7
R101 1K91R2F-1-GP
0113 -1
U6
ISL62882CHRTZ-GP
20090923
1D05V_VTT
5V_S5
CORE_PWRGD
PSI#
R95 68R2-GP
R96 147KR2F-GP
R99 1K91R2F-1-GP
NTC 470K close to H_S MOSFET of Phase1
H_PROCHOT#
R89 4K02R2F-GP
R94 NTC-470K-9-GP 69.60013.141
C169 SCD01U50V2KX-1GP
R102 8K06R2F-GP
C167 SC1000P50V3JN-GP-U
1026 -SC
1026 -SB confirm with cherry
R88 0R2J-2-GP
0919 SA
C168 SC10P50V2JN-4GP
C148 SC22P50V2JN-4GP
C165 SC150P50V2JN-3GP
R93 412KR2F-GP
C166 SCD22U25V3KX-GP
C150 SCD22U25V3KX-GP
C149 SCD22U25V3KX-GP
74.62882.A73
20090707Wayne
C170 SC390P50V2KX-GP
R100 562R2F-GP
R105 3K65R2F-1-GP
64.36515.6DL
1130 -SC confirm by cherry
C171 SC330P50V2KX-3GP
C172 SC330P50V2KX-3GP
R107 0R0402-PAD
R111 0R0402-PAD
0113 -1
C179 SC1000P50V3JN-GP-U
R137 82D5R2F-1-GP
C184 SCD01U50V2KX-1GP
R127 1K96R2F-1-GP
64.19615.6DL
1023 -SB request by cherry
C190 SCD22U25V3KX-GP
C191 SCD22U25V3KX-GP
78.22422.2BL
1214 -SC
1130 -SC confrim by cherry
R142 2K61R2F-1-GP
R131 1KR2F-1-GP
R462 NTC-10K-27-GP
20090713 WAYNE
NTC 10K close to Choke of Phase1
C186 SCD1U25V3KX-GP
R90 0R0402-PAD
C202 SCD1U10V2KX-1GP
C210 SCD22U25V3KX-GP
R174 1R2F-GP
R158 2D2R2F-GP
R117 8K87R2F-2-GP
C178 SCD22U25V3KX-GP
C204 SCD22U25V3KX-GP
previous 0.22uF 0603 16V X5R
Current 0.22uF 0603 25V X7R
C209 SC1U10V2KX-1GP
C208 SC1U10V2KX-1GP
R176 0R0402-PAD
Intel support POC (power on current).
R165 R156 R145 R139 R133 R123 R119 R109 R98
R166 R157 R146 R140 R134 R124 R120 R110 R97
1KR2J-1-GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
1009 -SA
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 47 of 72
http://laptop-motherboard-schematic.blogspot.com/



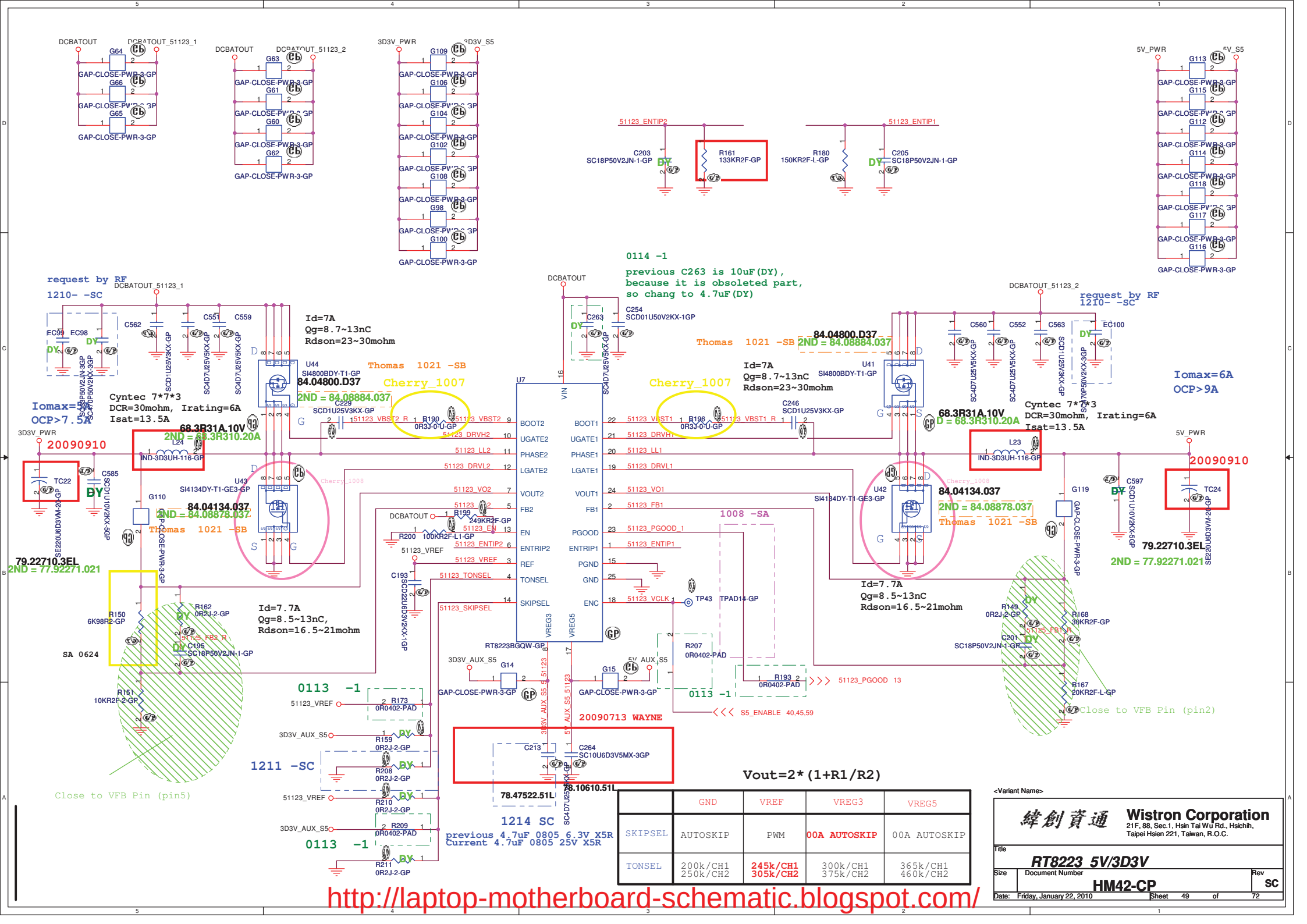
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62882 CPU CORE (1/2)

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 48 of 72



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: RT8223 5V/3D3V
Size: Document Number: HM42-CP Rev: SC
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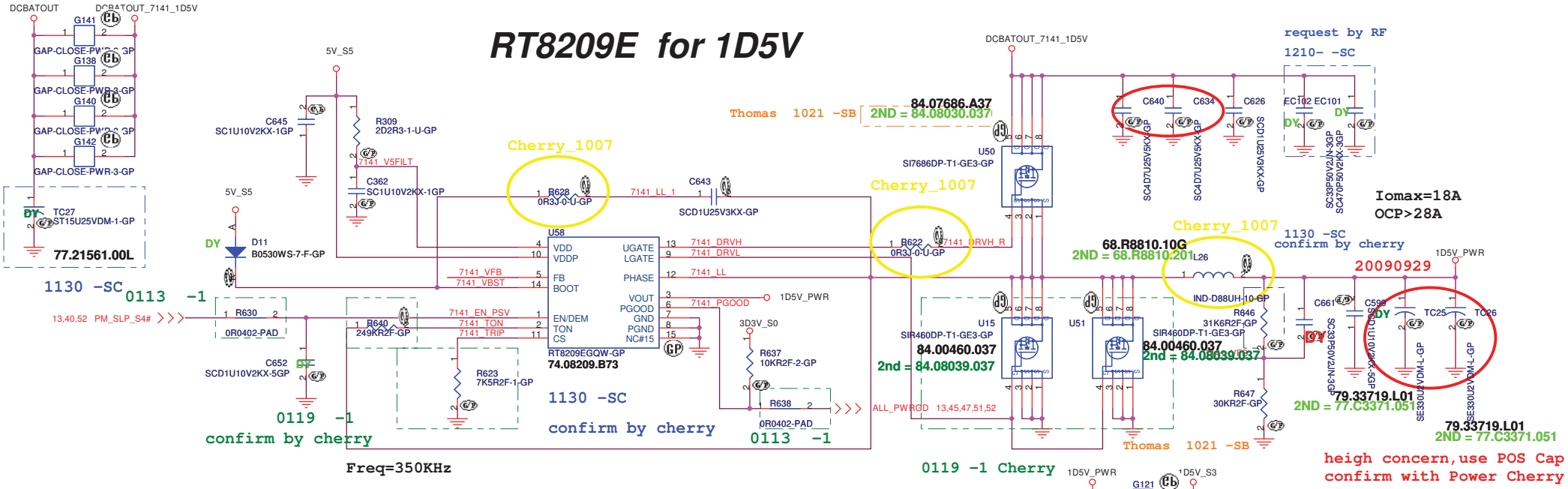
RT8209E for 1D5V



$$V_{CS}\,(mV) = R_{CS}\,(k\Omega) \times 10\,(\mu A)$$

$$I_{LOAD\_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{V_{IN}}$$

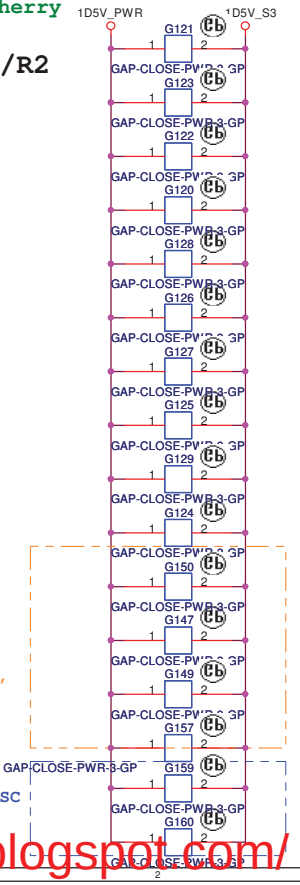
VCS(mV)=9.09KX10uA=90.9mV

I_OCP=[(90.9mV/3.2mohm)+(1/2*350Khz* 0.88uH)*[(19-1.5)*1.5/19]

=28.4 +1.623 *1.38 =30A

Iocp = Io *1.5

Vout=0.75V*(R1+R2)/R2



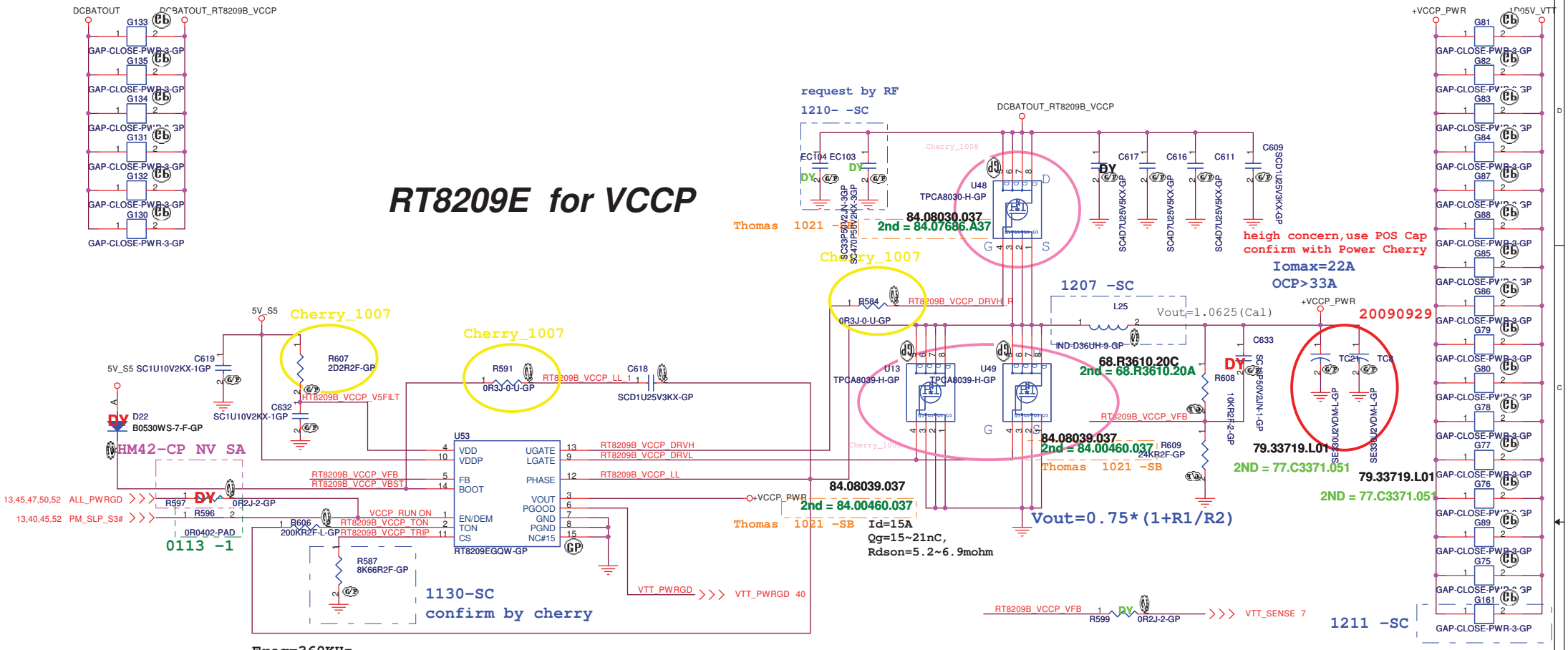
1022 -SB
cherry request 8 pcs Gap,
becasue of space concern,
only add 4pcs Cap.

Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT8209B 1D5V		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 50 of 72	

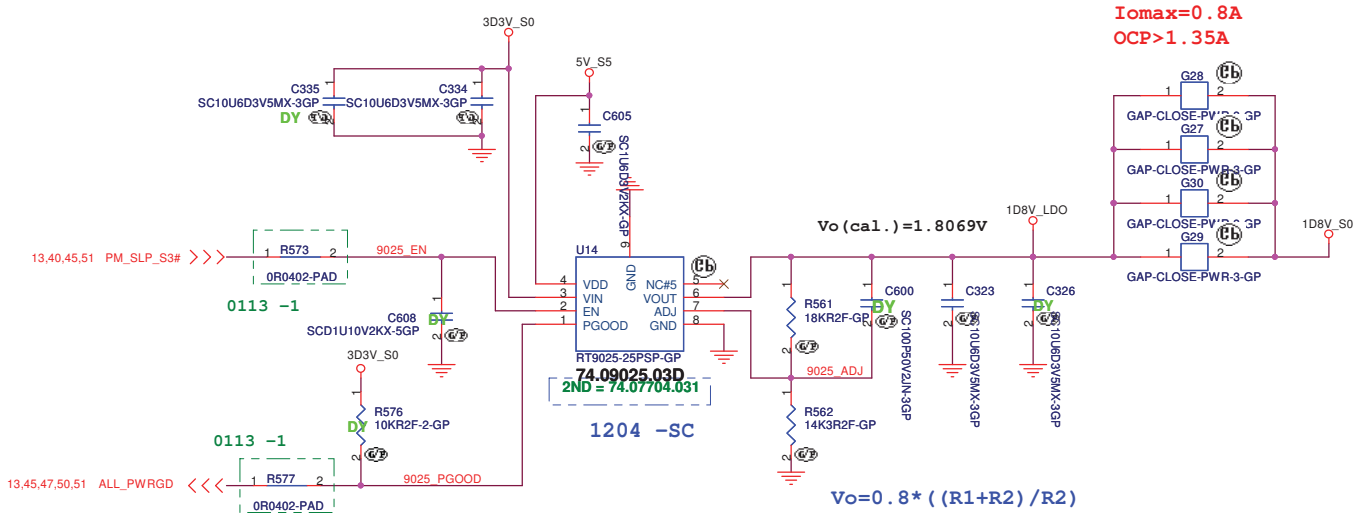
RT8209E for VCCP



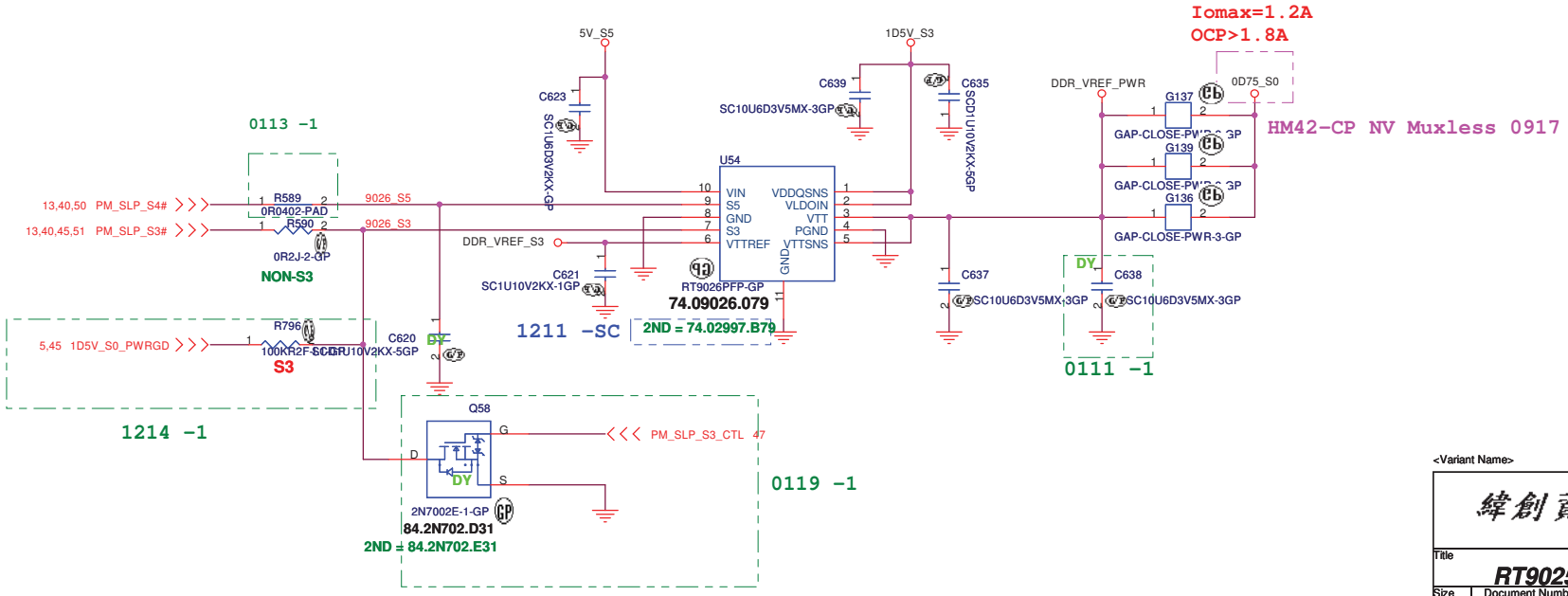
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8209B +VCCP	
Size	Document Number HM42-CP	Rev SC
Date: Friday, January 22, 2010	Sheet 51 of 72	

RT9025 for 1D8V_S0

20090915



RT9026 for 0D75V_S0



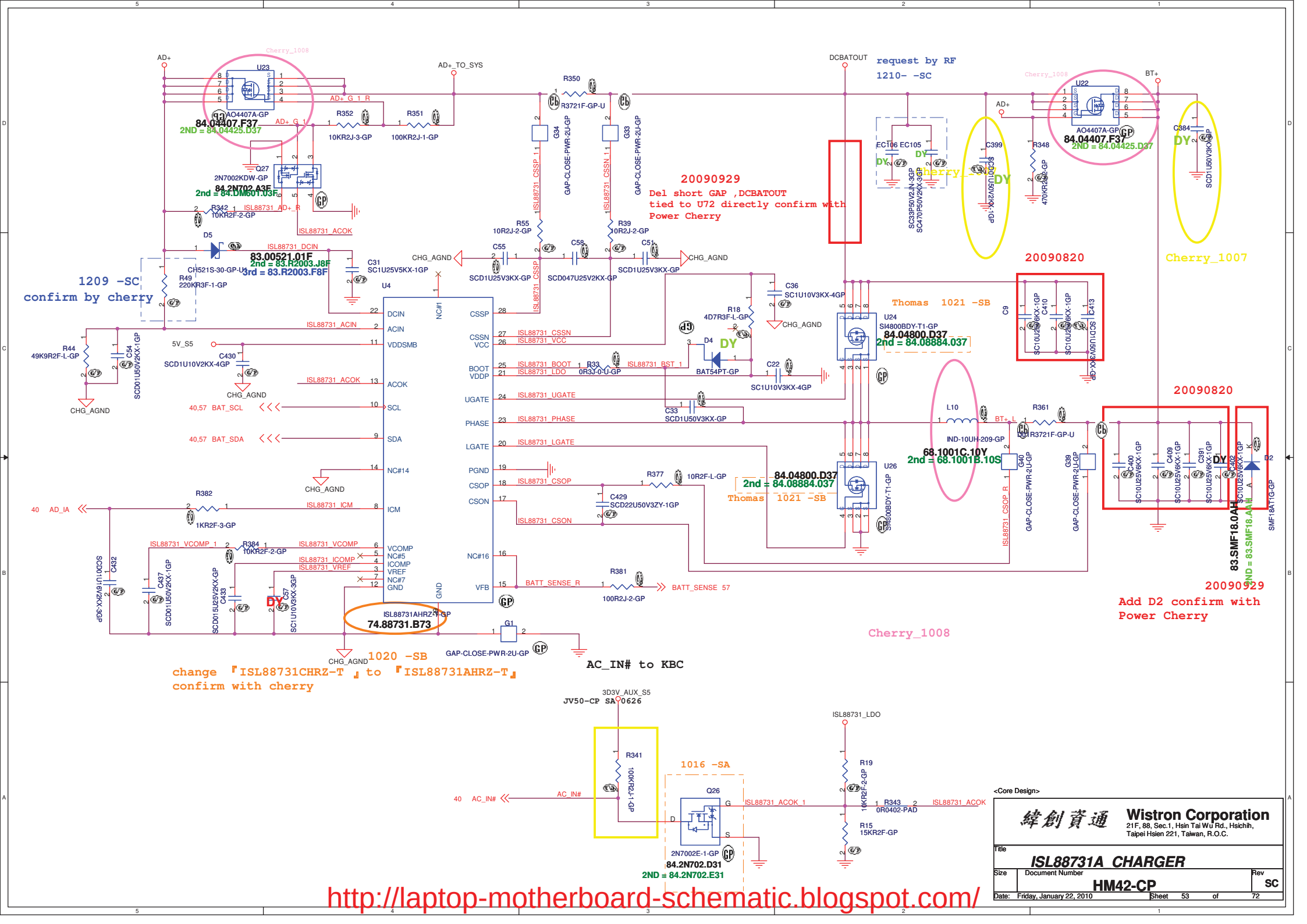
<Variant Name>

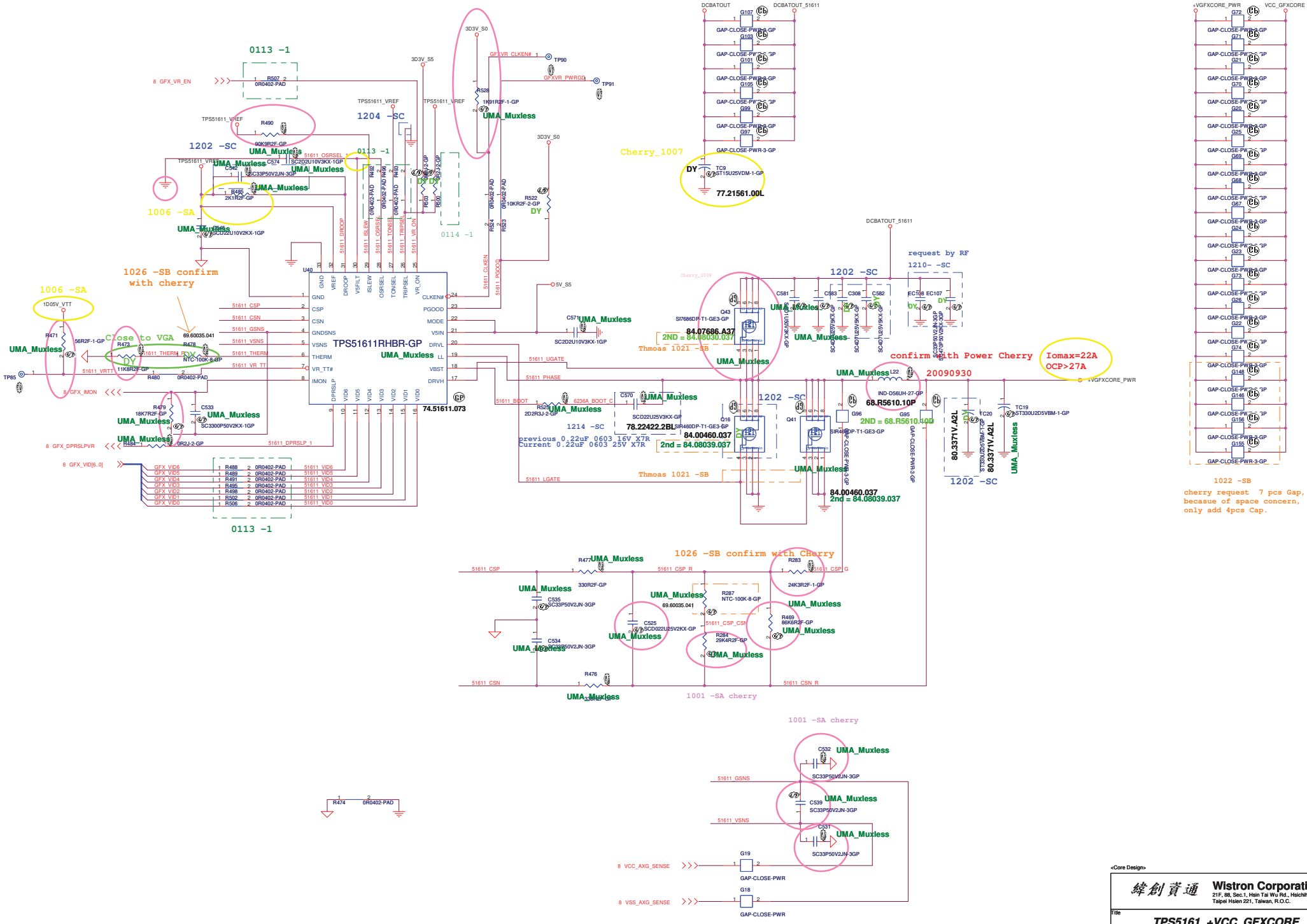
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

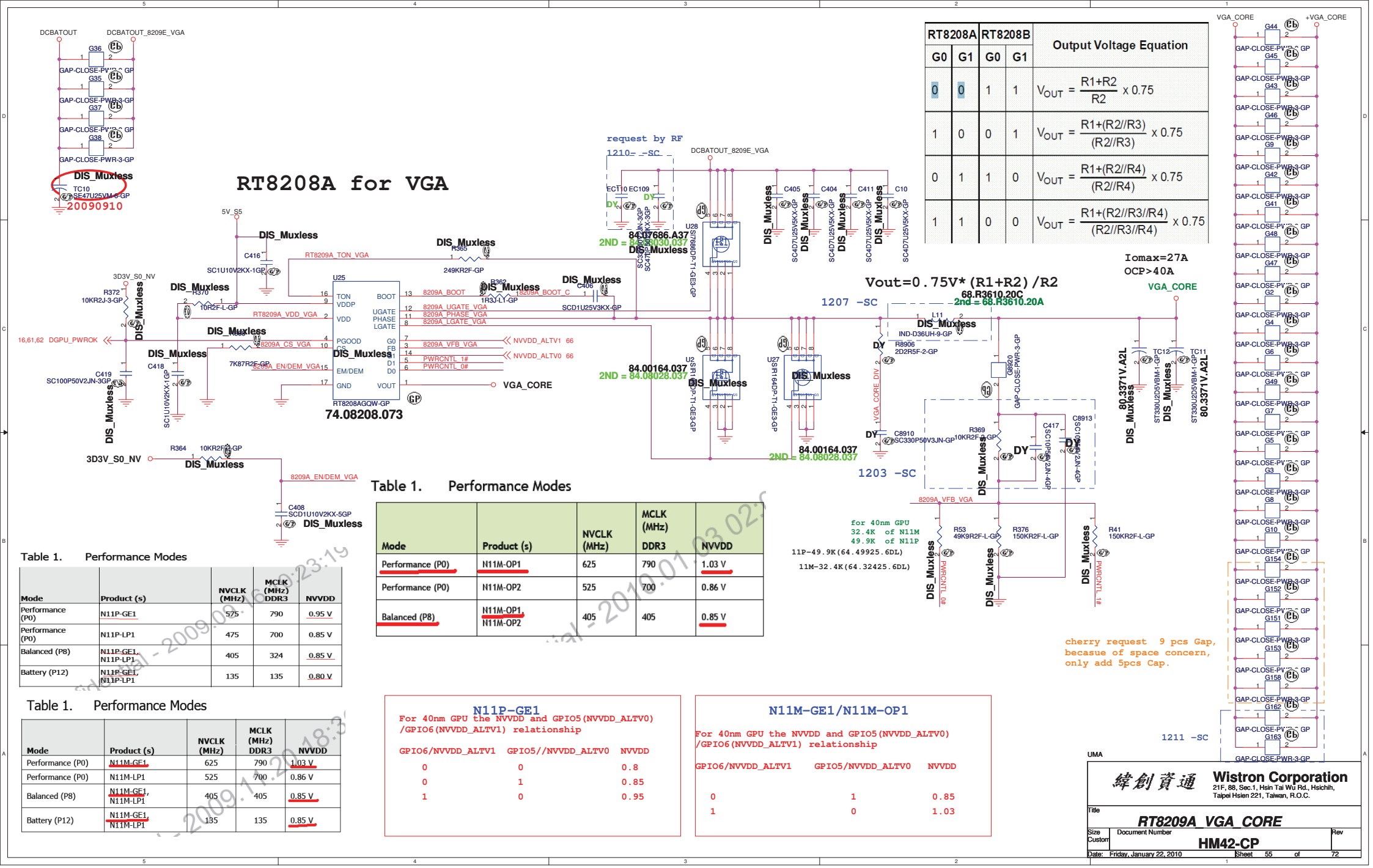
Title: RT9025_1D8V/RT9026_0D75

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 52 of 72







RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

N11P-GE1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5//NVVDD_ALTV0	NVVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5/NVVDD_ALTV0	NVVDD
0	1	0.85
1	0	1.03

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Title: RT8209A_VGA_CORE
Size: Custom | Document Number: HM42-CP | Rev:
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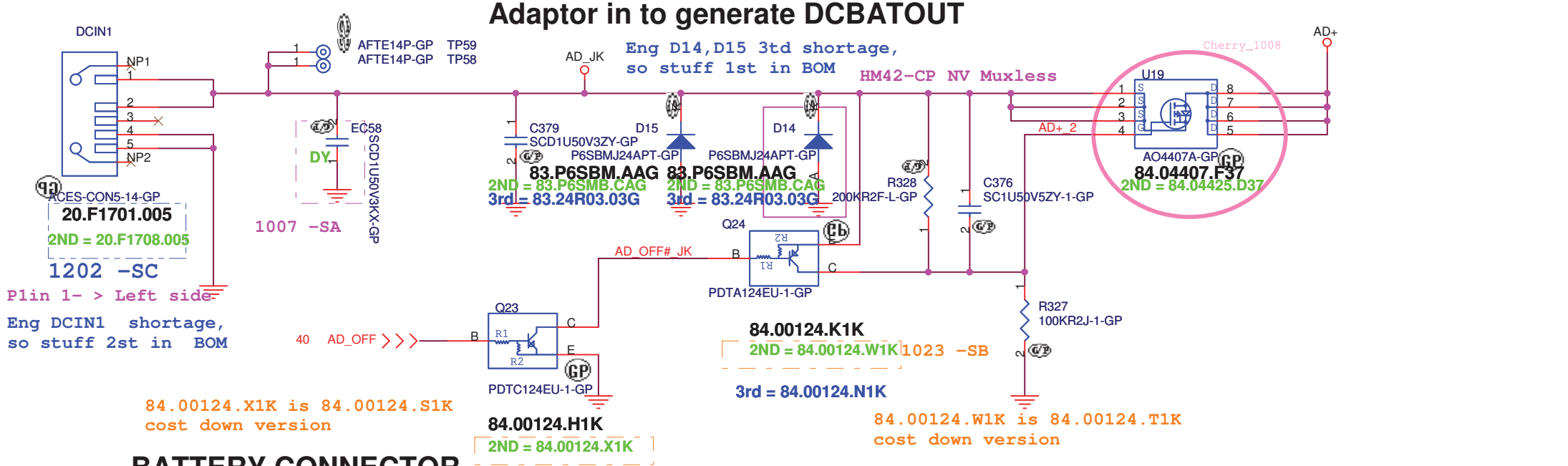
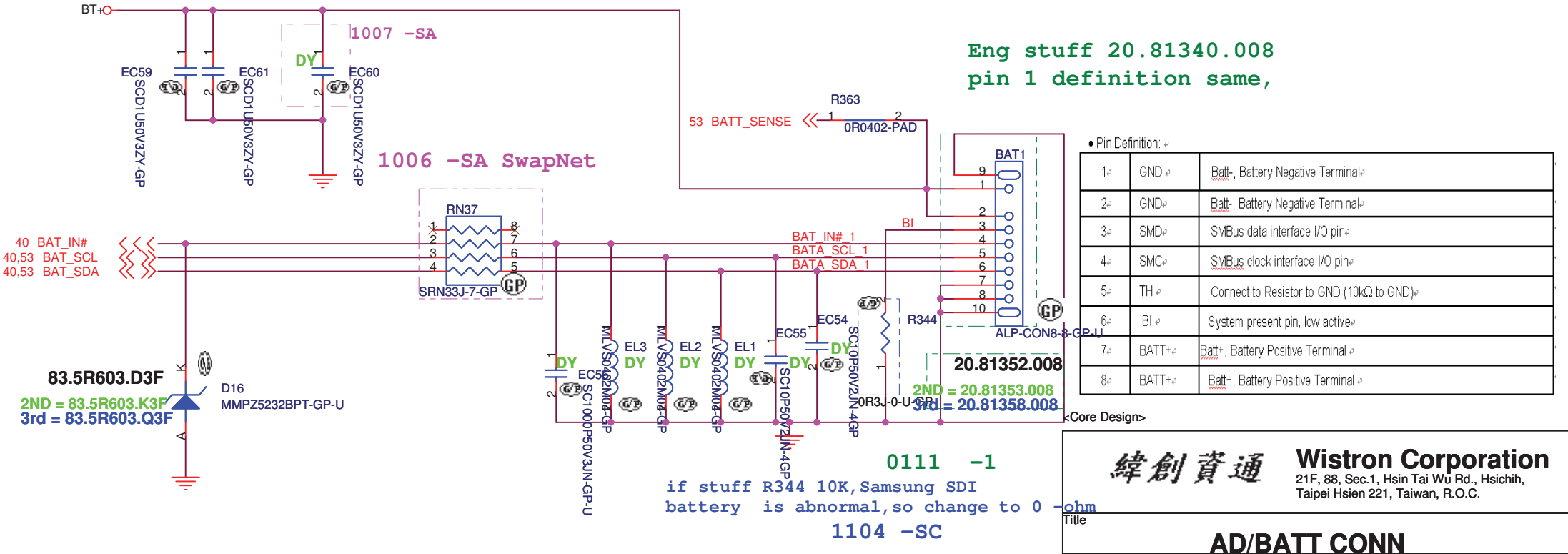
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

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Title: **AD/BATT CONN**

Size	Document Number	Rev
	HM42-CP	SC

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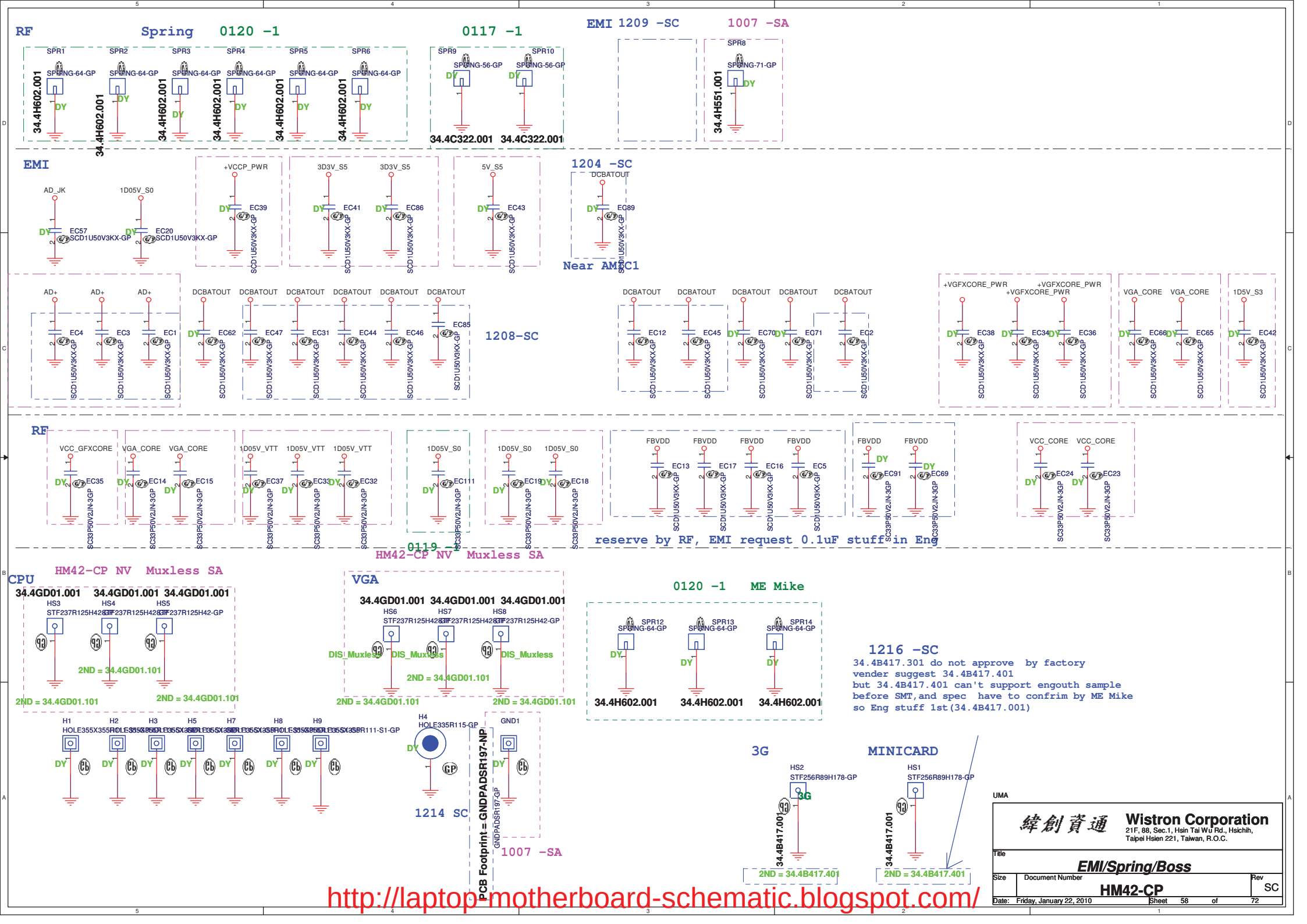
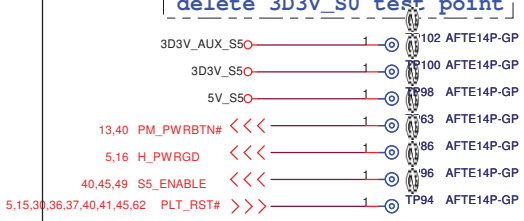


Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Title: AFTE TP

Size | Document Number: HM42-CP | Rev: SC

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+3VS to 1.8V Transfer

I=300mA

U5
VIN 1
GND 2
EN 3
NC#4 4
VOUT 5
G9091-180T11U-GP
74.09091.G3F

DGPU_PWROK_TO1D8V
3D3V_S0_NV
1D8V_S0_NV
DIS_Muxless
C79 SSC1U10V2ZY-GP
C81 SSC1U10V2ZY-GP
DIS_Muxless

C90 SCD1U10V2KX-4GP
DY
1202 -SC
R65 0R0402-PAD
DGPU_PWROK 16,55,62

2nd = 74.07716.07F DIS_Muxless
1030 -SC

+1.5V to FBVDD Transfer

AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

1D5V_S3
DIS_Muxless
U32
C457 SC10U6D3V3MX-GP
DIS_Muxless
CA8039-H-GP
84.08039.037
2nd = 84.00460.037
0118 -1

FBVDD
DIS_Muxless
C463 SCD1U10V2KX-5GP
TC13
77.C1571.09L
2ND = 77.21571.111
1226 -1
TC29 DY
77.C1571.09L
2ND = 77.21571.111
ST150U6D3VBM-1-GP
ST150U6D3VBM-1-GP
1214 -SC

1D05V_S0
1D05V_S0_NV
DIS_Muxless
U30
AO4468-GP
84.04468.037
2nd = 84.08882.037
Lab stuff 84.08882.037

previous 0.1uF 0402 16V X7R
Current 0.1uF 0402 10V X7R

80.15715.12L instead by 77.21571.111
for TM david suggestion

RUN_POWER_ON
84.S0610.B31
2ND = 84.00610.C31
NDS0610-NL-GP
Q28
RUNON_R
DIS_Muxless
R396 330KR2J-L1-GP
DIS_EN_1D5_RUN_R
DIS_Muxless
R67 100KR2J-1-GP
DIS_Muxless
DIS_Muxless
R397 330KR2J-L1-GP

0113 -1
16,55,62 DGPU_PWROK
R70 0R0402-PAD
DGPU_PWROK_R
C100 SCD1U10V2KX-4GP
DY
Q4
DIS_Muxless
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
1016 -SA
DIS_EN_1D5_RUN

Discharge Circuit

FBVDD
R549 470R2J-2-GP
Muxless
DIS_FBVDD_L
Muxless
Q56
DIS_EN_1D5_RUN
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

1D05V_S0_NV
R551 470R2J-2-GP
Muxless
DIS_1D05V_S0_NV_L
Muxless
Q57
DIS_EN_1D5_RUN
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

0113 -1

R58
3D3V_S0
0R5J-5-GP
DIS
3D3V_S0_NV

Q31
AO3413-GP
84.03413.A31
R444 470R2J-2-GP
Muxless
3D3V_S0
R452 100KR2J-1-GP
Muxless
Muxless

VDDR3discharge CKT
DGPU_3D3V_DIS
Q30
Muxless
DGPU_3D3V_EN
1016 -SB
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

3D3V_S0
R454 10KR2J-3-GP
2ND = 84.2N702.E31
Muxless
DGPU_PWR_EN
Q35
Muxless
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

16 DGPU_PWR_EN#
Q34
Muxless
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

UMA

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Title: NV power
Size: A3
Document Number: HM42-CP
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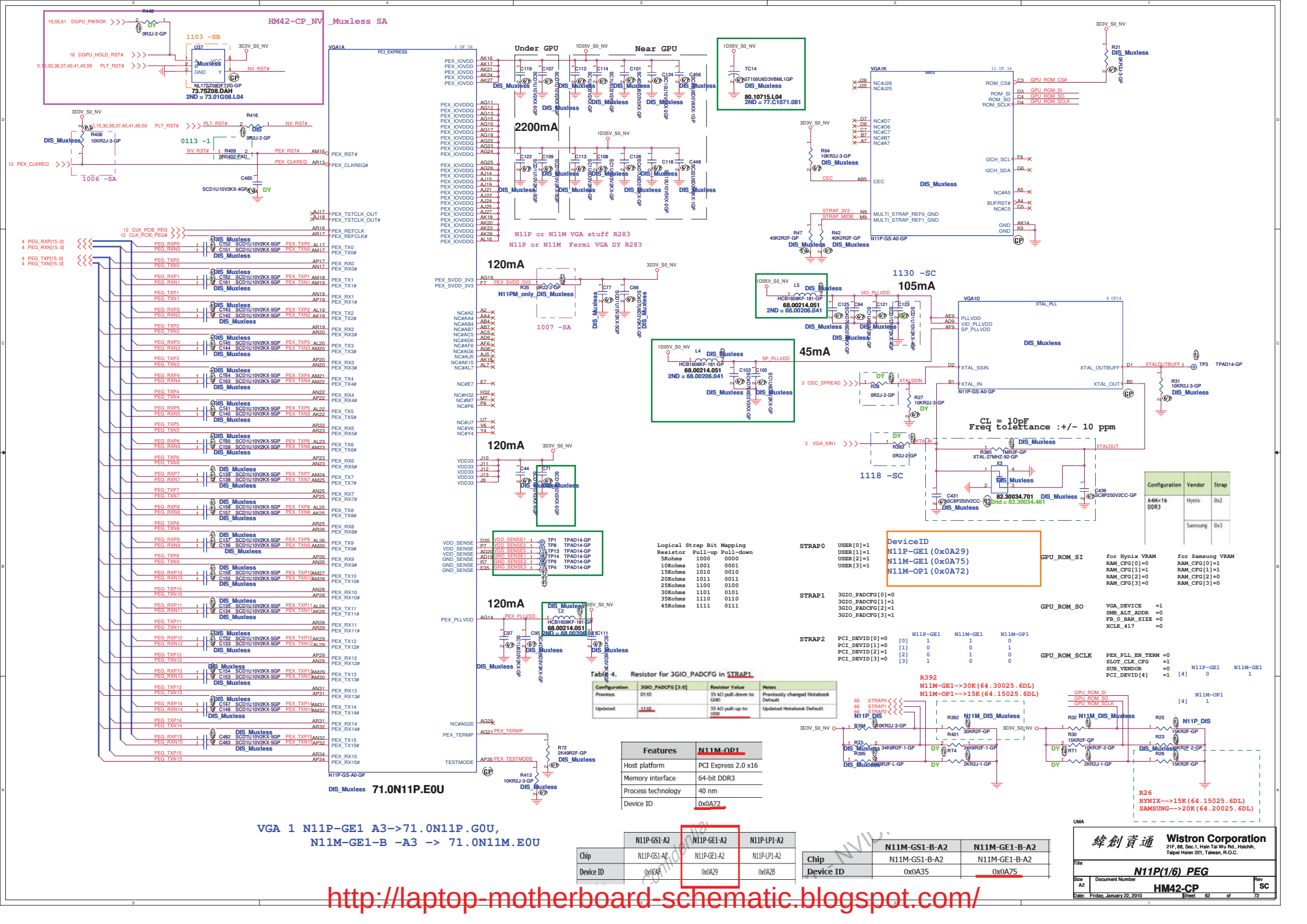


Configuration	Vendor	Strap
64M×16 DDR3	Hynix	0x2
	Samsung	0x3

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

STRAP0 USER[0]=1, USER[1]=1, USER[2]=1, USER[3]=1

STRAP1 3GIO_PADCFG[0]=0, 3GIO_PADCFG[1]=1, 3GIO_PADCFG[2]=1, 3GIO_PADCFG[3]=1

STRAP2

	N11P-GE1	N11M-GE1	N11M-OP1
PCI_DEVID[0]=0	[0] 1	1	0
PCI_DEVID[1]=0	[1] 0	0	1
PCI_DEVID[2]=1	[2] 0	1	0
PCI_DEVID[3]=0	[3] 1	0	0

GPU_ROM_SI: for Hynix VRAM RAM_CFG[0]=0, RAM_CFG[1]=1, RAM_CFG[2]=0, RAM_CFG[3]=0; for Samsung VRAM RAM_CFG[0]=1, RAM_CFG[1]=1, RAM_CFG[2]=0, RAM_CFG[3]=0

GPU_ROM_SO: VGA_DEVICE =1, SMB_ALT_ADDR =0, FB_0_BAR_SIZE =0, XCLK_417 =0

GPU_ROM_SCLK: PEX_PLL_EN_TERM =0, SLOT_CLK_CFG =1, SUB_VENDOR =0, PCI_DEVID[4] =1

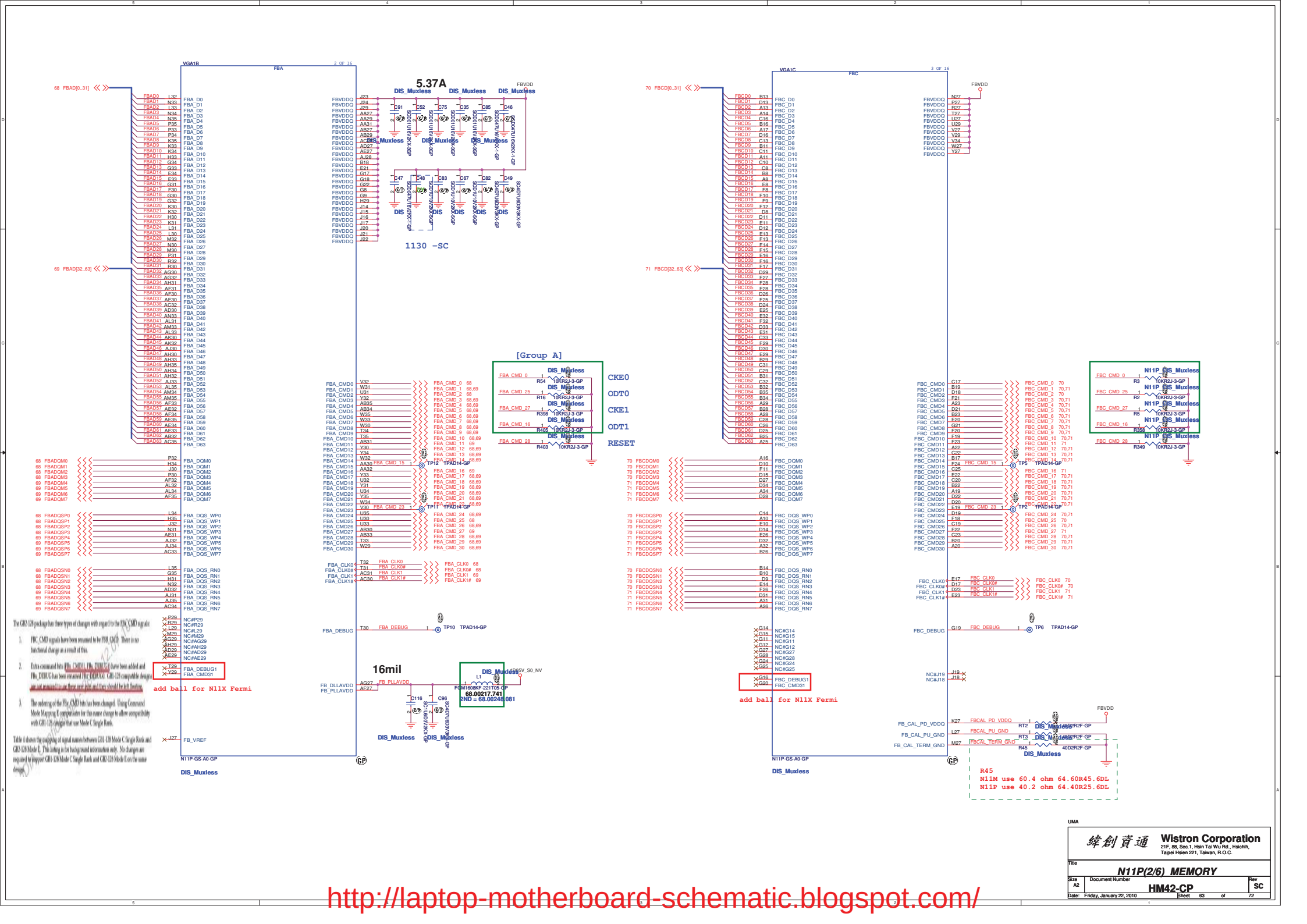
Table 4. Resistor for 3GIO_PADCFG in STRAP1

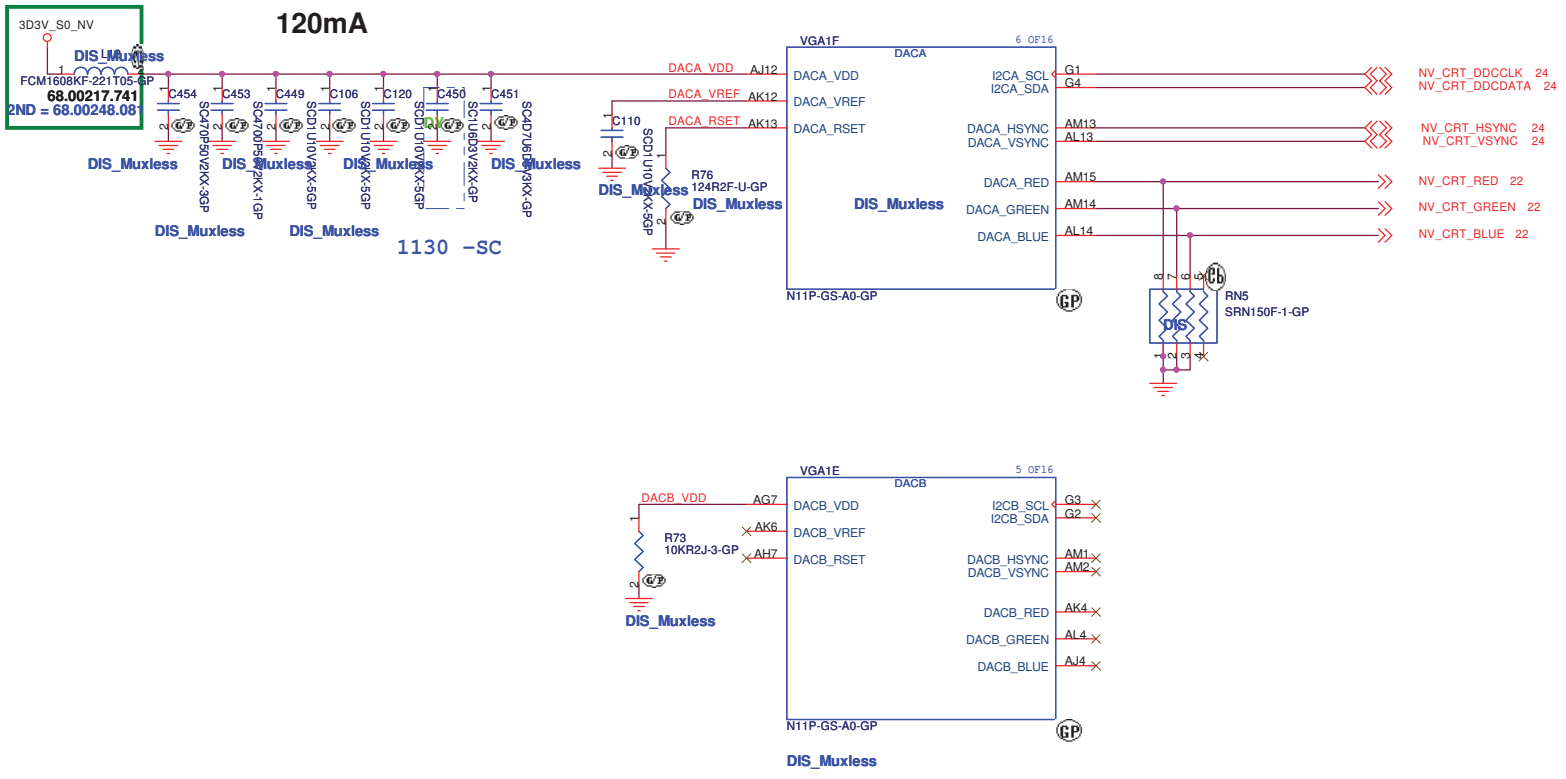
Configuration	3GIO_PADCFG [3:0]	Resistor Value	Notes
Previous	0110	35 kΩ pull-down to GND	Previously changed Notebook Default
Updated	1110	35 kΩ pull-up to VDD	Updated Notebook Default

Features	N11M-OP1
Host platform	PCI Express 2.0 x16
Memory interface	64-bit DDR3
Process technology	40 nm
Device ID	0x0A72

	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0CA0	0x0A29	0x0A2B

	N11M-GS1-B-A2	N11M-GE1-B-A2
Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N11P(3/6)_DAC*		
Size: A3	Document Number: HM42-CP	Rev: SC
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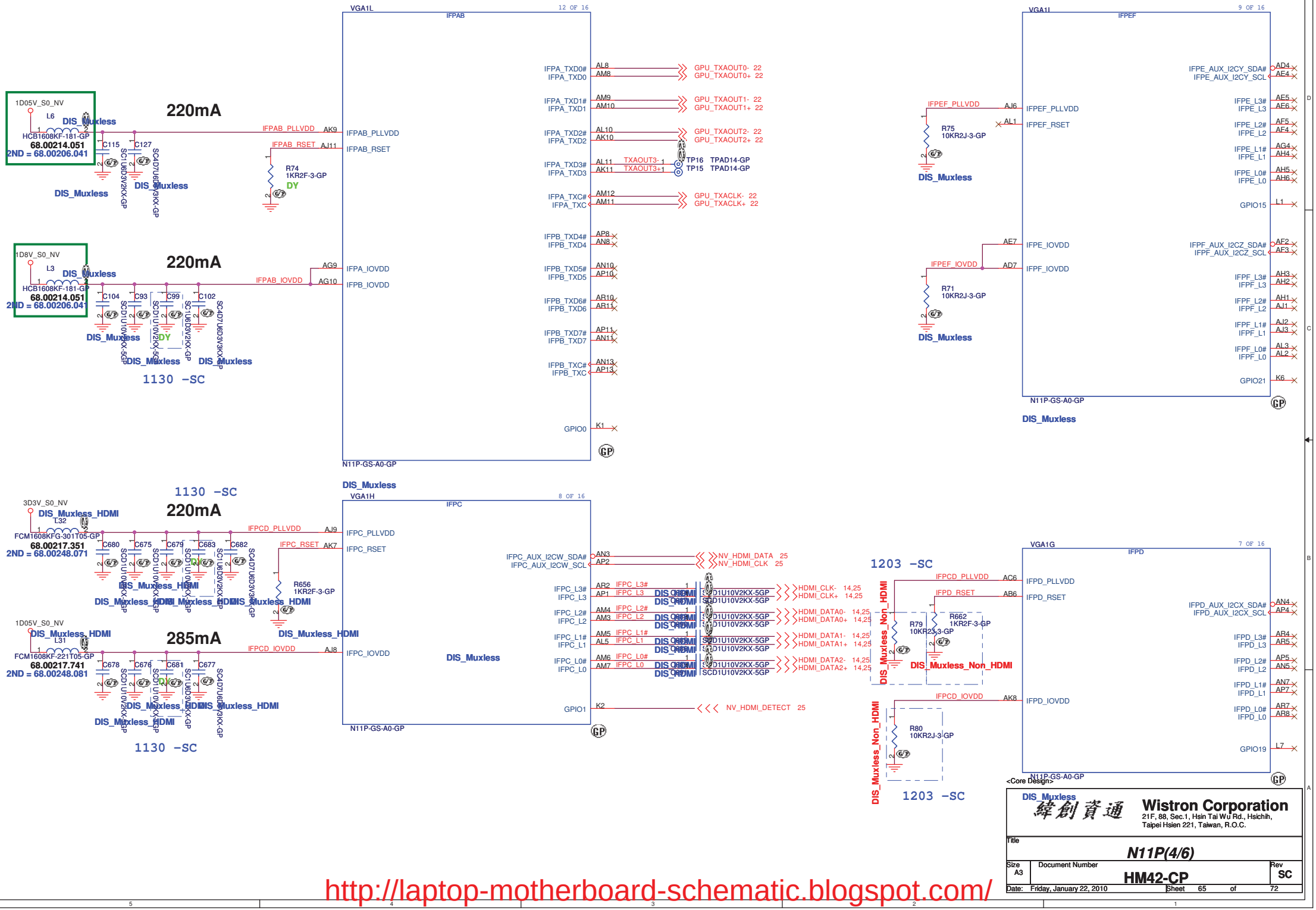

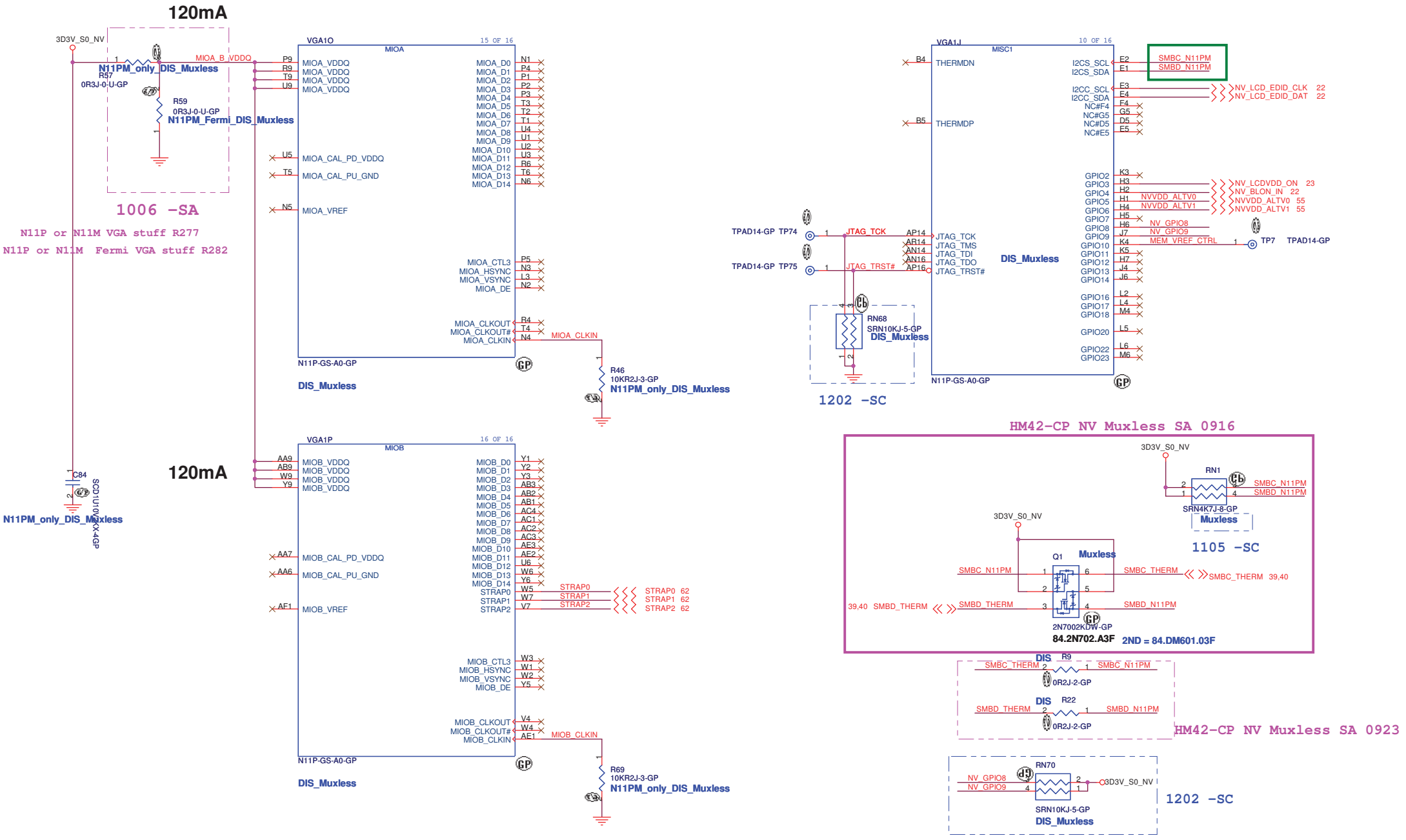

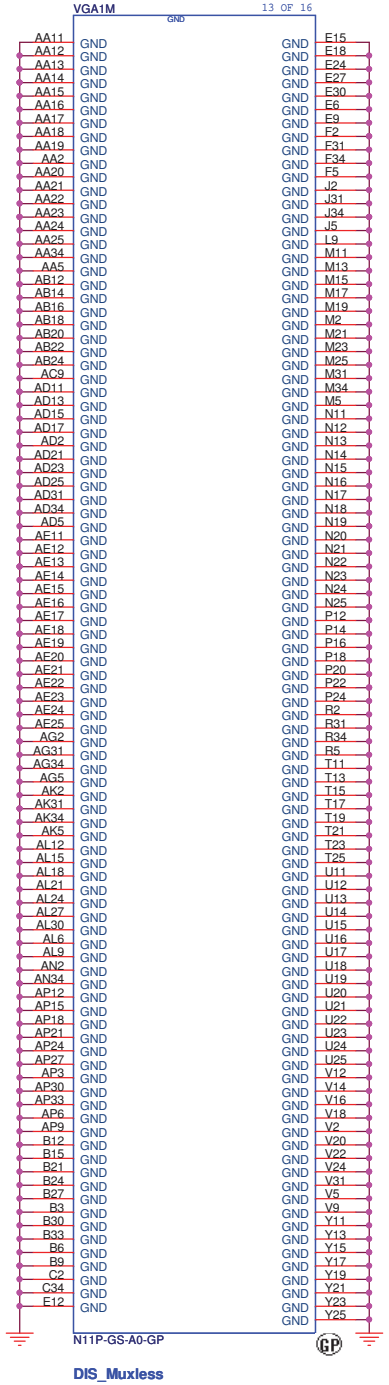

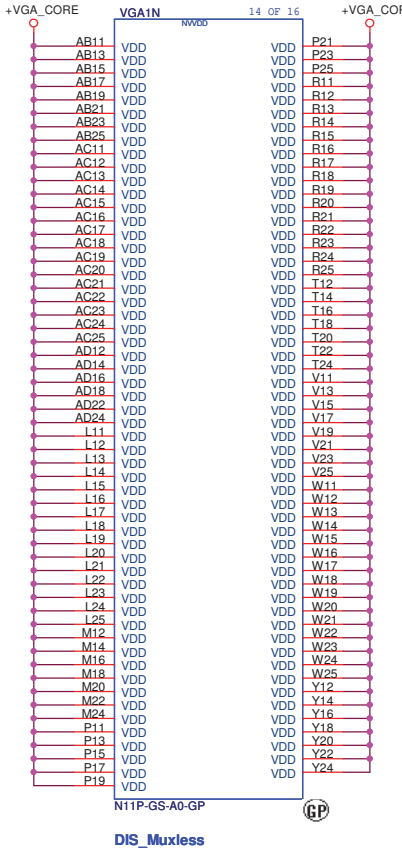

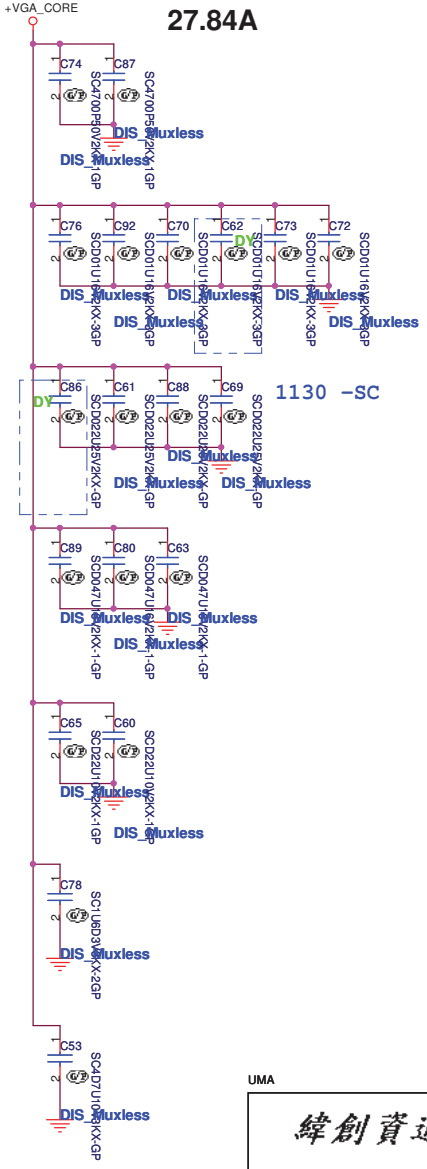

UMA

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Title	***N11P(6/6)_POWER***	
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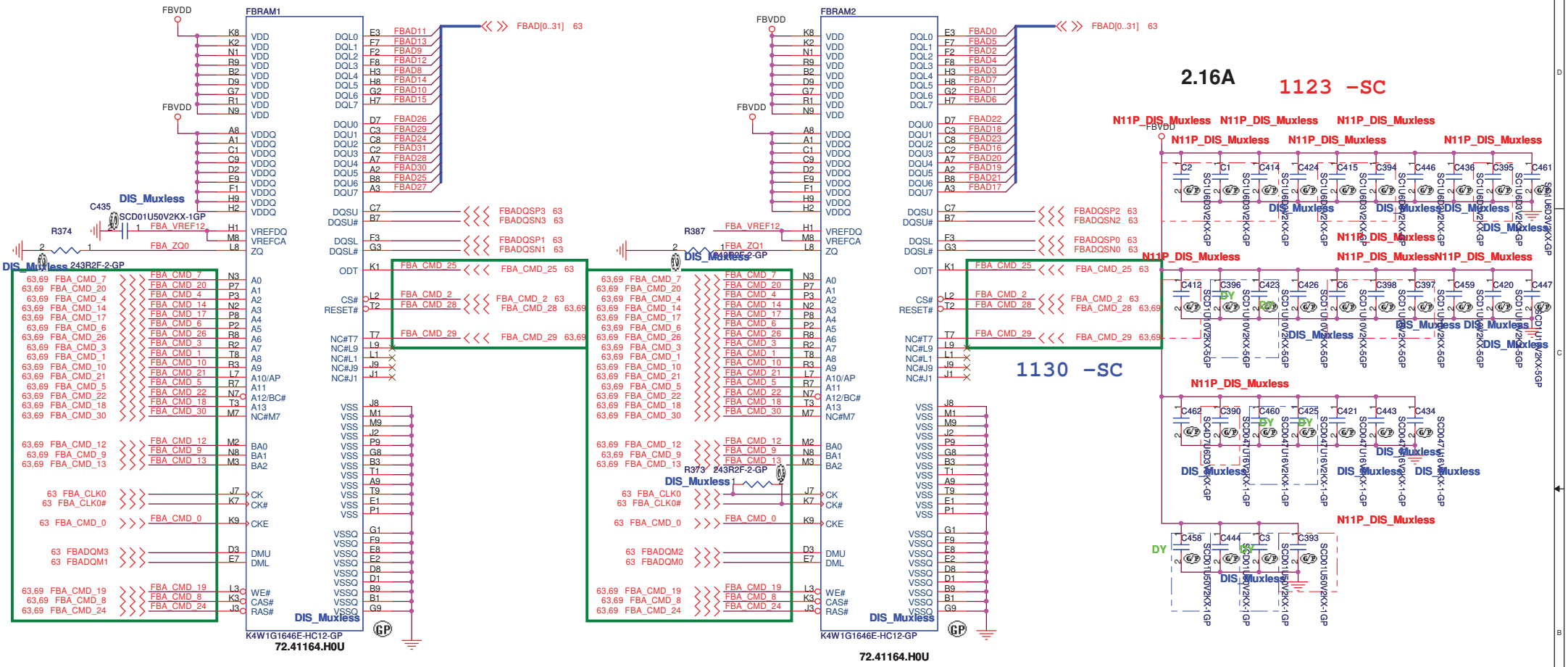
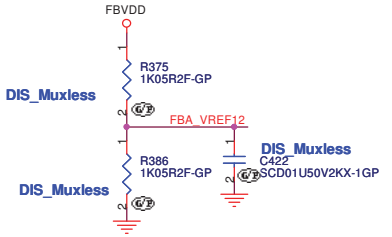
DDR3



SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)



UMA

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Title		
VRAM(1/4)		
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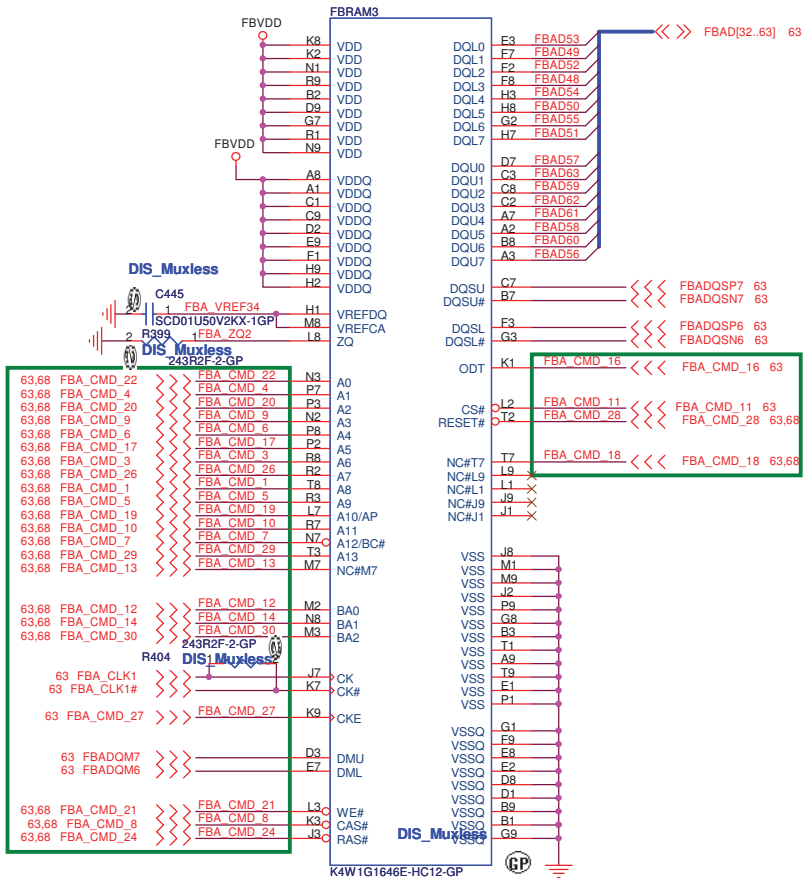
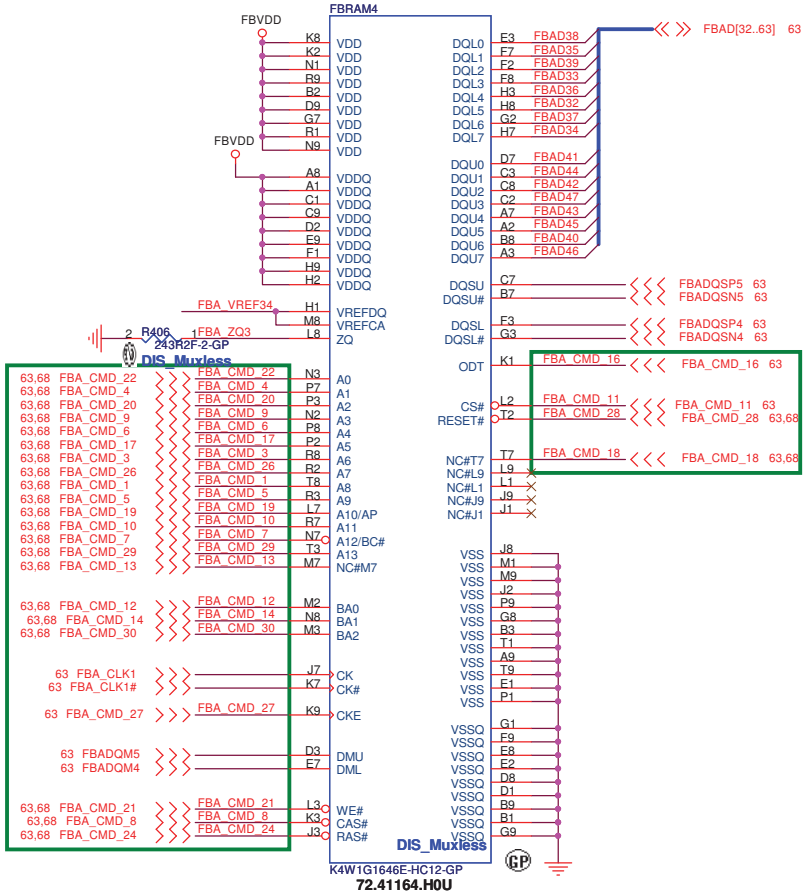
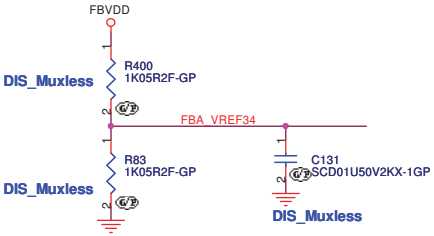
DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

HM42-CP

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Title: ***VRAM(2/4)***		
Size: A3	Document Number: **HM42-CP**	Rev: SC
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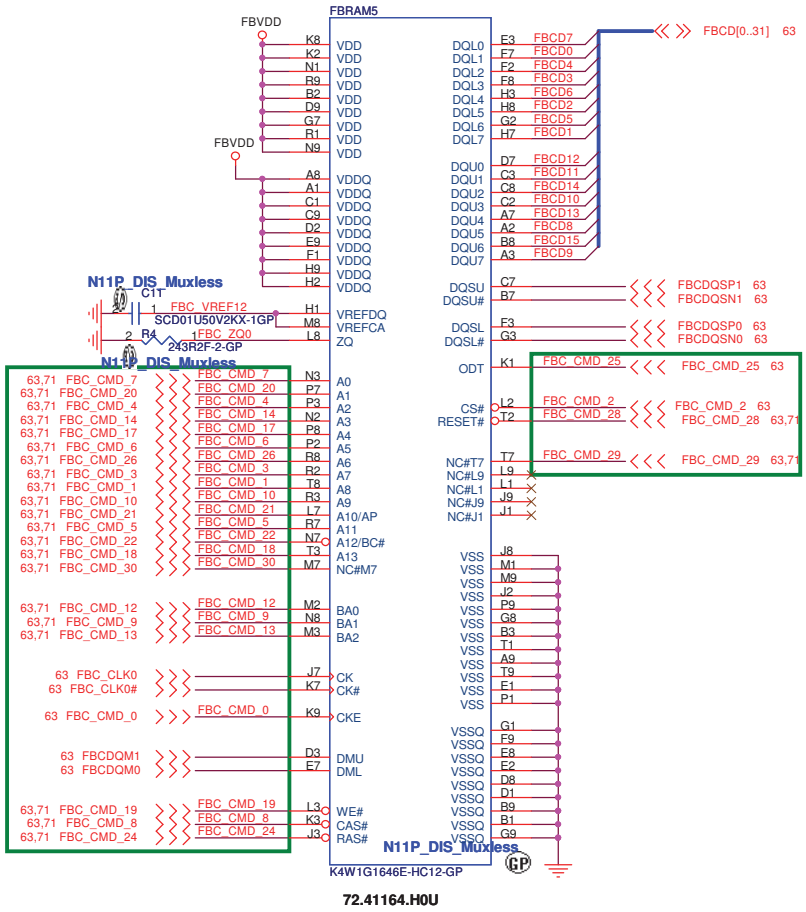
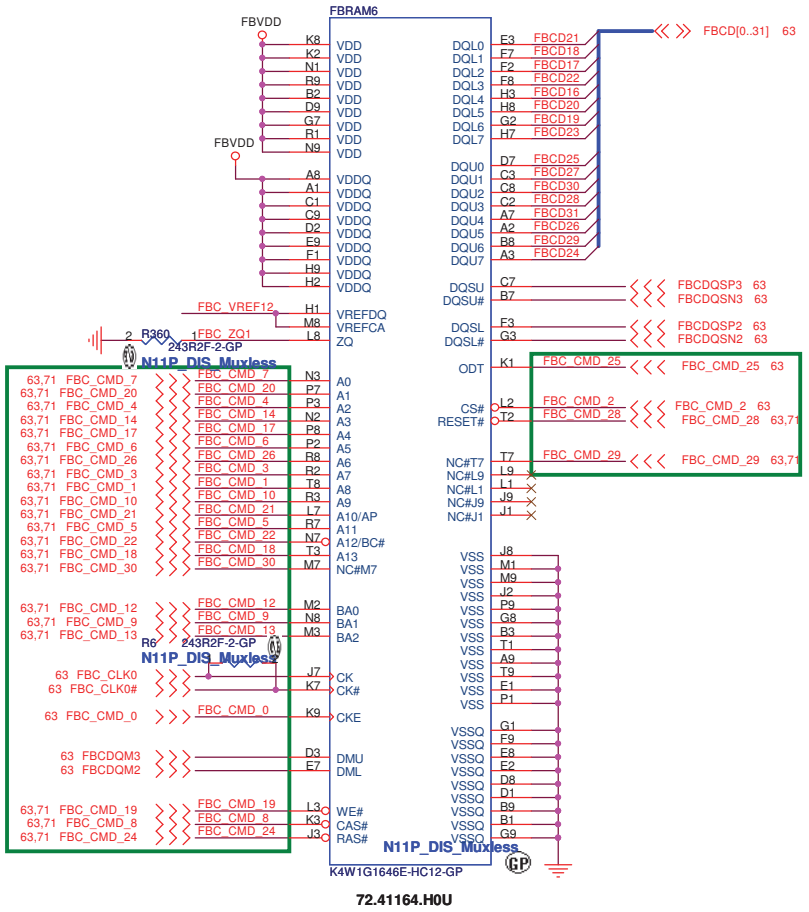
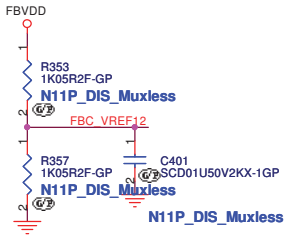
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



HM42-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(3/4)***	
Size A3	Document Number **HM42-CP**	Rev SC
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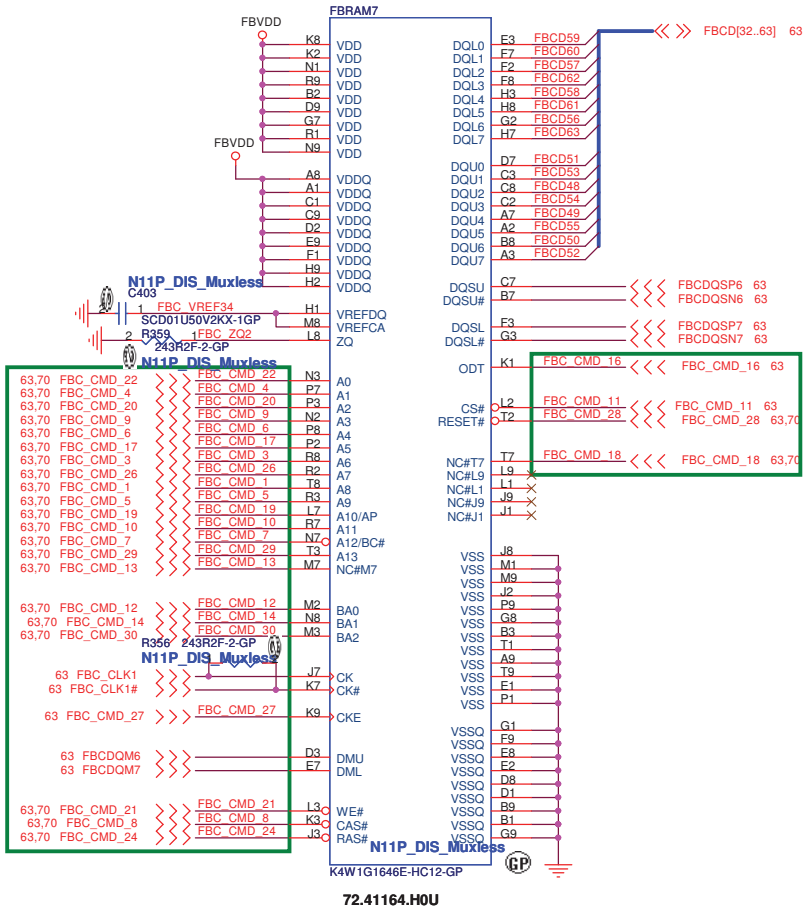
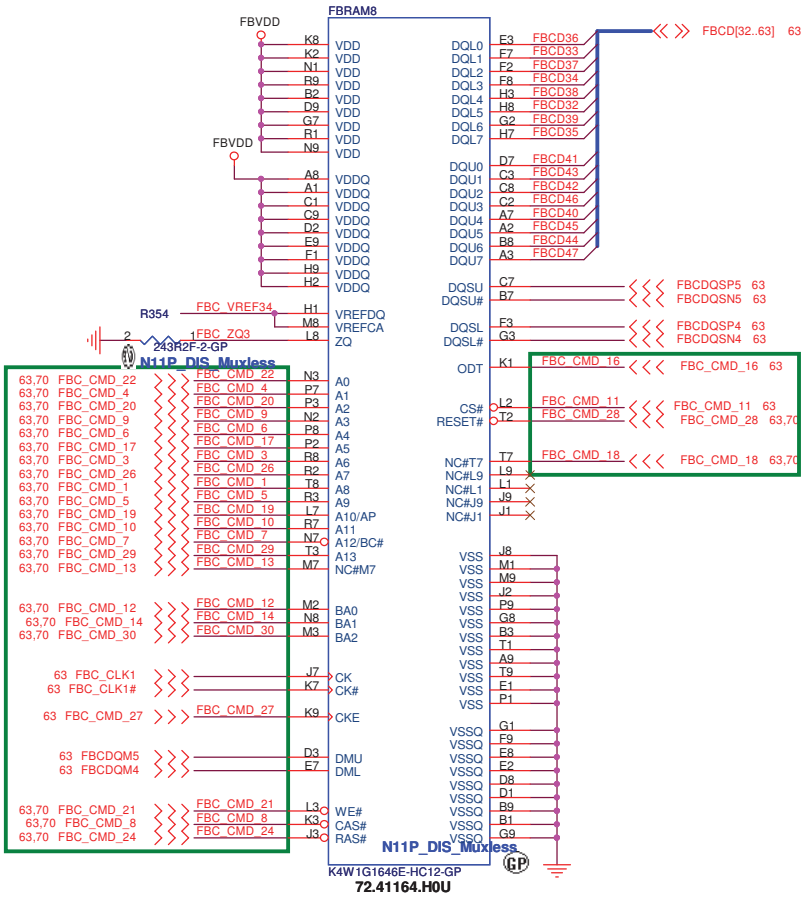
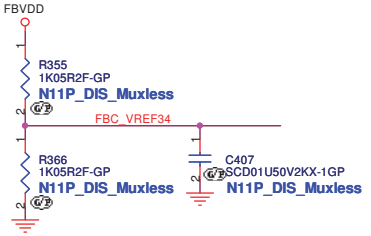
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(4/4)**

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]
PCH1 PN : 71.0IBEX.A0U
[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

[lab -SB]
2nd -> UMA (S01G)
1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)
2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]
2nd -> UMA Non 3G (55.4GY01.S07G)
1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)
1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]
UMA 3G (55.4GY01.M01G)
Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st
Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd
UMA Non 3G (55.4GY01.M04G)
Diserete N11M Hynix_3G(55.4GY01.M05G)
Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st
Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]
qual TPCN1 2nd source(20.K0296.006)
qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd
qual ODD1 3rd source(62.10065.E01)
qual PWRCN1 2nd and 3rd
qual RTC1 4th source
qual BT1 2nd and 3 source
qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

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