ZY5/ZY5D SYSTEM BLOCK DIAGRAM

CPU CORE ISL6265A PAGE 26
NB CORE +1.1V PAGE 27
NB RUN +1.1V PAGE 28
DDR II SMDDR_VTERM 1.8VSUS(TPS51116REGR) PAGE 29
SYSTEM POWER ISL6237 PAGE 25
SYSTEM CHARGER (ISL6251A) PAGE 24
DISCHARGER / +1.1V_S5, +1.2V,+2.5V PAGE 30

INT or EV selector Resistor
DDRII-SODIMM1 PAGE 6
DDRII-SODIMM2 PAGE 6
DDRII 667/800 MHZ
AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 2,3,4,5
CPU THERMAL SENSOR PAGE 4
CPU Fan PAGE 17
HT3 LINK
ZY5D NO USED
MXM Connector PAGE 14
PCI-Express 16X
NORTH BRIDGE & SOUTH BRIDGE
MCP77M
27mm X 27mm, 836pin BGA
PAGE 7,8,9,10,11,12,13
14.318MHz
LPC
PCI-E
X1
Mini PCI-E Card (Wireless LAN) PAGE 16
Mini PCI-E Card (TV TUNER) USB2.0 x1 PAGE 16
Express Card (NEW CARD) USB2.0 Ports x2 PAGE 16
Card reader JMicron JMB385-LGEZ0A PAGE 20
LAN BroadCom PCIE-LAN BCM5787/5764 (10/100/GigaLAN) PAGE 18
RJ45/RJ11 PAGE 15
CABLE DOCK LAN/VGA/DVI/USB/AUDIO PAGE 22
LVDS
CRT
ZY5D NO USED HDMI
LVDS PAGE 15
SN74CBTLV3257PWR Switch PAGE 15
TS3DV520RHUR Switch PAGE 15
CRT
DVI-D
HDMI
CRT PAGE 15
CABLE DOCK PAGE 22
HDMI CONN. PAGE 15
SATA - HDD PAGE 17
SATA0
SATA - HDD PAGE 17
SATA1
ODD(PATA) PAGE 17
SATA2
USB2.0
USB2.0 Ports x2 PAGE 16
Bluetooth x1 PAGE 16
CCD x1 PAGE 15
Fingrprinter x1 PAGE 16
CABLE DOCK USB x1 PAGE 22
PCI
Card Bus PCMCIA O2 Micro OZ601TN PAGE 23
HDA
Azalia AudioController RealTek ALC268/888 PAGE 19
MDC 1.5 PAGE 19
B TEST MODIFY
Audio Amplifier
Int MIC
Speaker
SPIDF/Phone Jack
Line in
MIC Jack
Keyboard PAGE 21
KBC (WPCE775CA0DG) PAGE 21
CIR PAGE 16
Touch Pad PAGE 17
SPI ROM PAGE 21
CABLE DOCK AUDIO PAGE 22

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : GND

Quanta Computer Inc.
PROJECT : ZY5D
Size | Document Number: Block Diagram | Rev 3B
Date: Wednesday, July 30, 2008 | Sheet 1 of 35

7 HT_RXD#[15..0] — HT_RXD#[15..0]
7 HT_RXD[15..0] — HT_RXD[15..0]
7 HT_TXD[15..0] — HT_TXD[15..0]
7 HT_TXD#[15..0] — HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

REV:B Modify

VLDT_RUN

U25A — HT LINK

D1	VLDT_A0	VLDT_B0	AE2
D2	VLDT_A1	VLDT_B1	AE3
D3	VLDT_A2	VLDT_B2	AE4
D4	VLDT_A3	VLDT_B3	AE5

C496 4.7u/6.3V_6

HT_RXD0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_TXD0
HT_RXD#0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_TXD#0
HT_RXD1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_TXD1
HT_RXD#1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_TXD#1
HT_RXD2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_TXD2
HT_RXD#2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_TXD#2
HT_RXD3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_TXD3
HT_RXD#3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_TXD#3
HT_RXD4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_TXD4
HT_RXD#4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_TXD#4
HT_RXD5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_TXD5
HT_RXD#5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_TXD#5
HT_RXD6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_TXD6
HT_RXD#6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_TXD#6
HT_RXD7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_TXD7
HT_RXD#7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_TXD#7
HT_RXD8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_TXD8
HT_RXD#8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_TXD#8
HT_RXD9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_TXD9
HT_RXD#9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_TXD#9
HT_RXD10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_TXD10
HT_RXD#10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_TXD#10
HT_RXD11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_TXD11
HT_RXD#11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_TXD#11
HT_RXD12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_TXD12
HT_RXD#12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_TXD#12
HT_RXD13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_TXD13
HT_RXD#13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_TXD#13
HT_RXD14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_TXD14
HT_RXD#14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_TXD#14
HT_RXD15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_TXD15
HT_RXD#15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_TXD#15

7 HT_CPU_UPCLK0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_DWNCLK0 7
7 HT_CPU_UPCLK#0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_DWNCLK#0 7
7 HT_CPU_UPCLK1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_DWNCLK1 7
7 HT_CPU_UPCLK#1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_DWNCLK#1 7
7 HT_CPU_UPCTL0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_DWNCTL0 7
7 HT_CPU_UPCTL#0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_DWNCTL#0 7
7 HT_CPU_UPCTL1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_DWNCTL1 7
7 HT_CPU_UPCTL#1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_DWNCTL#1 7

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

NO STUB for HT3

R189 *51/F_4 — R187 *51/F_4

VLDT_RUN

HOLE10 *CPU_HOLE — HOLE9 *CPU_HOLE — HOLE19 *CPU_HOLE — HOLE20 *CPU_HOLE

HOLE36 *MINI_HOLE — HOLE37 *MINI_HOLE — HOLE27 *MINI_HOLE — HOLE28 *MINI_HOLE

HOLE8 *MXM_HOLE — HOLE17 *MXM_HOLE — HOLE7 *MXM_HOLE — HOLE16 *MXM_HOLE

HOLE11 *MDC_HOLE — HOLE13 *MDC_HOLE — HOLE6 *MXM1_HOLE — HOLE21 *MXM1_HOLE

PAD2 *EMIPAD — PAD3 *EMIPAD

HOLE3 *H-C295D118P2 — HOLE4 *H-C295D118P2 — HOLE1 *H-C295D118P2 — HOLE23 *H-C295D118P2

HOLE2 *H-C295D118P2 — HOLE5 *H-C295D118P2 — HOLE25 *H-C295D118P2 — HOLE32 *H-C295D118P2

ADOGND

HOLE34 *H-C295D118P2 — HOLE35 *H-C295D118P2 — HOLE33 *H-C295D118P2 — HOLE14 *H-C295D118P2

HOLE38 *FAN_HOLE — HOLE15 *NONP_HOLE1 — HOLE24 *H-C295D118P2

HOLE18 *ODD1_HOLE — HOLE22 *ODD1_HOLE — HOLE26 *HDD1_HOLE — HOLE30 *HDD1_HOLE — HOLE29 *HDD2_HOLE — HOLE31 *HDD2_HOLE

MODIFY 10/17,ALEX

+1.2V — VLDT_RUN

L45 FBJ3216HS800_1206

L48 FBJ3216HS800_1206

Note:on MCP77,(HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

80 ohm(4A)

C528 4.7u/6.3V_6 — C533 4.7u/6.3V_6 — C544 .22u/6.3V_4 — C502 .22u/6.3V_4 — C497 180P_4 — C538 180P_4

LAYOUT: Place bypass cap on topside of board

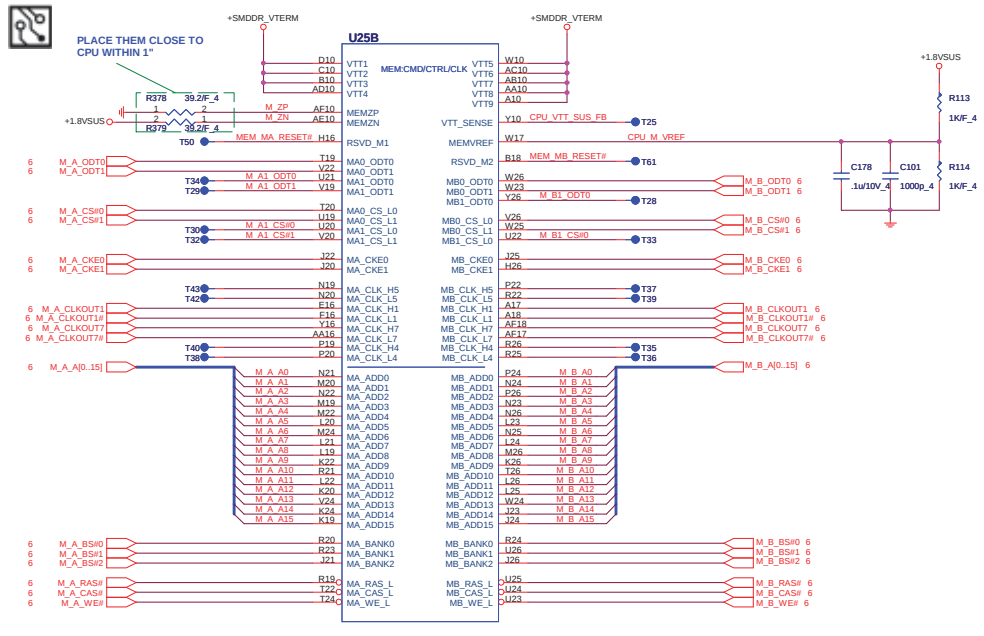
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

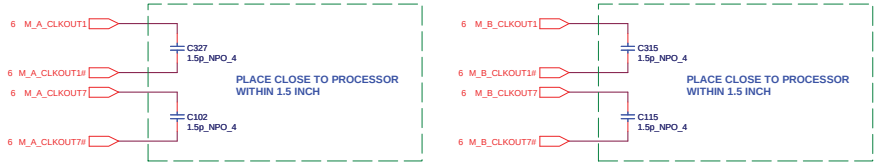
Quanta Computer Inc.
PROJECT : ZY5D

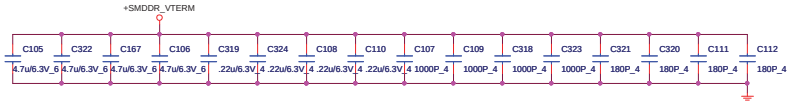
Size	Document Number	Rev
	AMD Griffin HT I/F	3B
Date: Wednesday, May 21, 2008	Sheet 2 of 35	

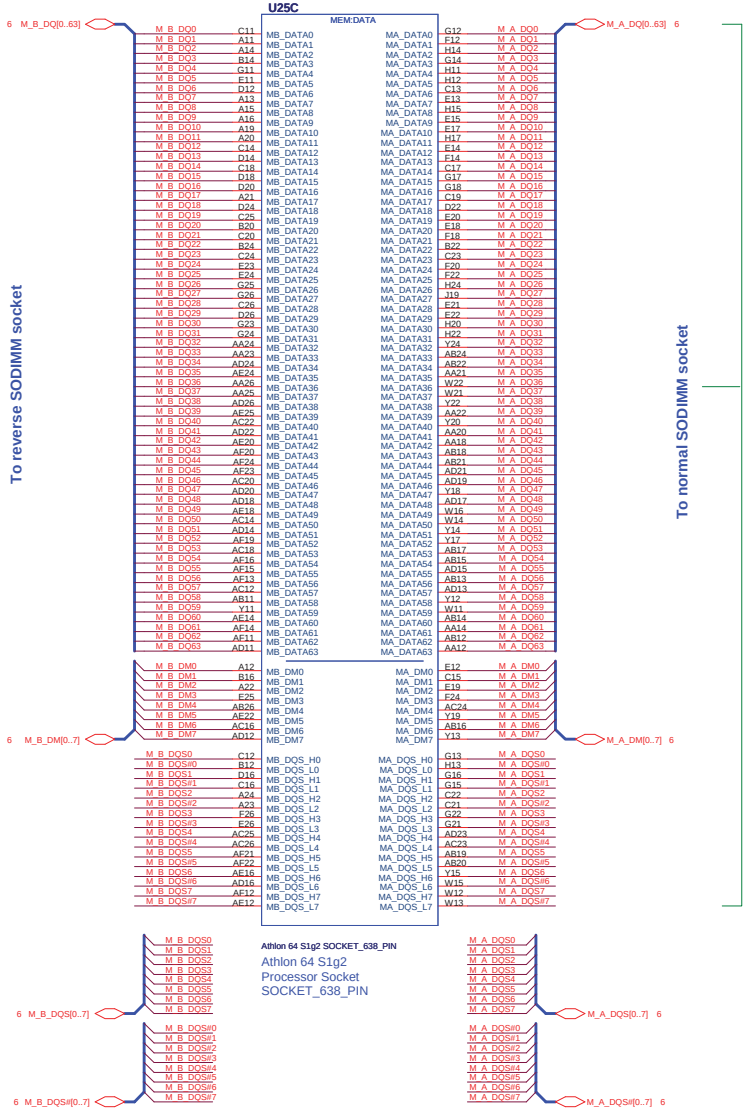
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

Processor DDR2 Memory Interface









Quanta Computer Inc.			
PROJECT : ZY5D			
Size	Document Number		Rev
	AMD Griffin DDRII MEMORY I/F		3B
Date: Wednesday, May 21, 2008	Sheet 3 of 35		

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V — L51 BLM18PG330SN1D_6 — CPU_VDDA_RUN

C595 100u/6.3V_3528 | C588 4.7u/6.3V_6 | C275 .22u/6.3V_4 | C286 3300p/50V_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

+1.8VSUS — R367 390_4 — CPU_SID — CPU_SID 12
R370 390_4 — CPU_SIC — CPU_SIC 12
R388 *390_4
R387 *1K/F_4 — CPU_ALERT

390 Ohm

+1.8VSUS — R100 300_4 — R104 300_4 — Q18 MMBT3904
7 CPU_THERMTRIP# — CPU_THERMTRIP# — R99 0_4 — SYS_SHDN# 25,30

U25D

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

CPU_VDDA_RUN — Keep trace from resisor to CPU within 0.6" — keep trace from caps to CPU within 1.2"

CPU_CLKP — C326 3900P_4 — CPU_CLKIN_SC_P
CPU_CLKN — C325 3900P_4 — CPU_CLKIN_SC_N
R218 169/F_6

place them to CPU within 1.5"

CPU_HT_RESET#
CPU_HT_PWRGD
CPU_HT_LDTSTOP#
CPU_LDT_REQ# CPU

CPU_SIC
CPU_SID
CPU_ALERT

VLDT_RUN — R186 44.2/F_4 — CPU_HTREF0
R182 44.2/F_4 — CPU_HTREF1

CPU_SVC_R
CPU_SVD_R
CPU_THERMTRIP#
CPU_PROCHOT#
CPU_MEMHOT#
CPU_THERMDC
CPU_THERMDA

connect to CPU VDDIO power FB

26 CPU_VDD0_FB_H — CPU_VDDIO_FB_H 29
26 CPU_VDD0_FB_L — CPU_VDDIO_FB_L 29

connect to CPU CORE power FB

26 CPU_VDD1_FB_H — VDD_NB_FB_H 26
26 CPU_VDD1_FB_L — VDD_NB_FB_L 26

connect to CPU VDDNB power FB

CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_DBREQ#
CPU_TDO

route as differential as short as possible testpoint under package

CPU_TEST23_TSTUPD
CPU_TEST18_PLLTEST1
CPU_TEST19_PLLTEST0
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST21_SCANEN
CPU_TEST20_SCANCLK2
CPU_TEST24_SCANCLK1
CPU_TEST22_SCANSHIFTEN
CPU_TEST12_SCANSHIFTENB
CPU_TEST27_SINGLECHAIN
R215 0_4 CPU_TEST9_ANALOGIN — CPU_TEST6_DIECRACKMON
CPU_TEST7_ANALOG_T
CPU_TEST10_ANALOGOUT
CPU_TEST8_DIG_T
CPU_TEST29_H_FBCLKOUT_P
CPU_TEST29_L_FBCLKOUT_N

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10

REV:E Modify by AMD

+1.8VSUS — R206 300_4 — R469 300_4

+1.8VSUS — R456 300_4 — 7 HTCPU_PWRGD — R455 0_4 — CPU_HT_PWRGD
C650 .1u/10V_4

REV:B Modify

+1.8VSUS — R465 300_4 — 7 HTCPU_STOP# — R464 0_4 — CPU_HT_LDTSTOP#

+1.8VSUS — R457 300_4 — 7 HTCPU_RST# — R458 0_4 — CPU_HT_RESET#

+1.8VSUS — R466 300_4 — Add pull up
CPU_LDT_REQ# CPU — R467 0_4 — HTCPU_REQ# — HTCPU_REQ# 7

+1.8VSUS — R97 300_4 — R98 330_4 — Q16 MMBT3904
CPU_PROCHOT# — EC_PROCHOT# 21
R96 *0_4 — MCP77_PROCHOT# 7

CHECK MCP thermal

+1.8VSUS — R168 *300_4 — R112 *330_4 — Q17 *MMBT3904
CPU_MEMHOT# — CPUMEMHOT# 21

connect to CPU CORE power controlier

VID Override Circuit

+1.8VSUS — R454 1K_4 — R453 1K_4
CPU_SVC_R — R452 0_4 — Serial VID Clock — SVC 26
CPU_SVD_R — R451 0_4 — Serial VID Data — SVD 26
HTCPU_PWRGD — R459 0_4 — PGD_IN 26
R462 *220_4 — R461 *220_4

VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

+1.8VSUS — CPU_TEST27_SINGLECHAIN — R382 *300_4

CPU_TEST18_PLLTEST1 R204 *300_4
CPU_TEST19_PLLTEST0 R203 *300_4
CPU_TEST15_BP1 R470 *300_4
CPU_TEST14_BP0 R471 *300_4

CPU_TEST23_TSTUPD R555 300_4
CPU_TEST21_SCANEN R396 300_4
CPU_TEST20_SCANCLK2 R385 300_4
CPU_TEST24_SCANCLK1 R386 300_4
CPU_TEST22_SCANSHIFTEN R384 *300_4
CPU_TEST12_SCANSHIFTENB R391 *300_4

Rev:E Add R555 by AMD Design guide 41650 V1_03 on 5/8.

Need Check with nVidia

HDT CONNECTOR

+1.8VSUS — R388 *220_4 — R380 *220_4 — R477 *220_4 — R383 *220_4 — R478 300_4

CPU_DBREQ# T92
CPU_DBRDY T55
CPU_TCK T81
CPU_TMS T31
CPU_TDI T75
CPU_TRST# T79
CPU_TDO T4

HDTGND — CN21 *ASP-68200-07-25P-LDV

GND1 GND2 RSVD1 GND4 RSVD0 GND6 DBREQ_L GND8 DBRDY GND10 TCK GND12 TMS GND14 TDI GND16 TRST_L GND18 TDO GND20 VCC_PROC_IO_21 GND22 VCC_PROC_IO_23 RESET_L GND26 KEY

H_HTCPU_RST#

+1.8VSUS — R475 *10K_4 — R473 *1K/F_4 — H_HTCPU_RST#
CPU_HT_RESET# — Q45 *MMBT3904

CPU H/W MONITOR

2/20/08' Reserve 0 ohm for CPU thermal issue on C-test

+3V — R151 47/F_6 3V_THM — 15 MIL
R515 *0_4 — C120 .1u/10V_4
CPU_THERMDC — C117 2200P_4 — CPU_THERMDA
10 mil trace / 10 mil space

Address 98H

U7 G786: VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND

KBSMDAT
KBSMCLK

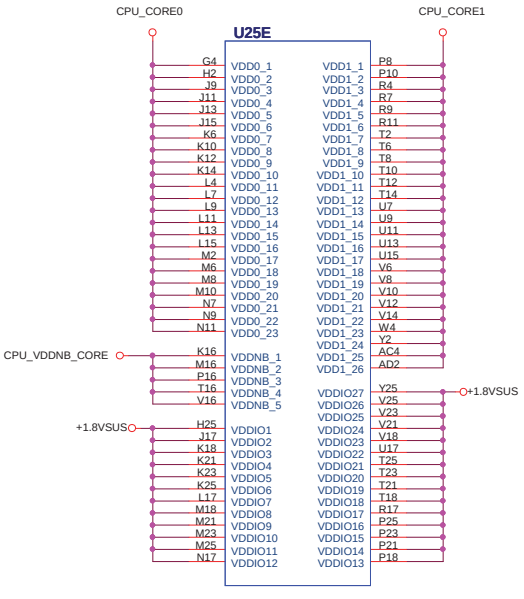
R136 10K_4 — Q33 2N7002E — To SB GPIO — THERM_ALERT# 12

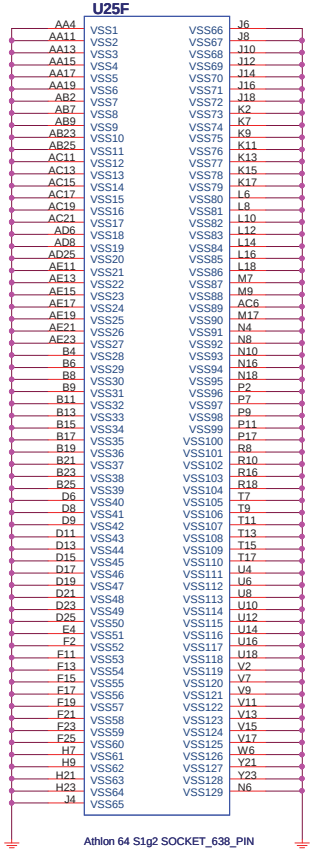
R140 4.7K_4 — Q37 2N7002E — 2ND_MBDATA 21
R143 4.7K_4 — Q36 2N7002E — 2ND_MBCLK 21

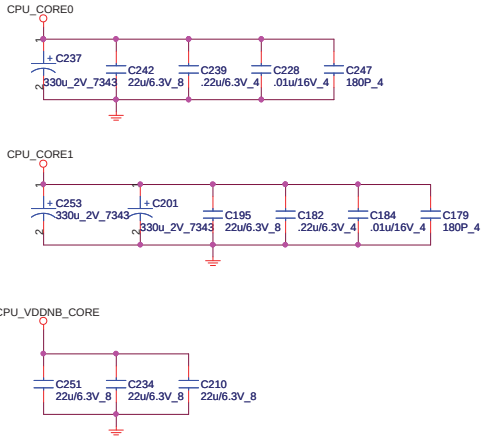
R128 10K_4 — To FAN — CPUFAN#_ON 17

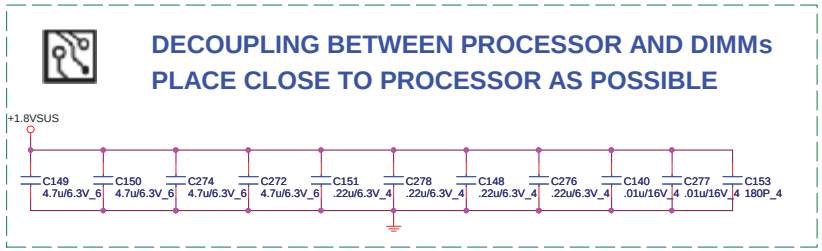
Quanta Computer Inc.
PROJECT : ZY5D
Size | Document Number: AMD Griffin CTRL & DEBUG | Rev 3B
Date: Wednesday, May 21, 2008 | Sheet 4 of 35

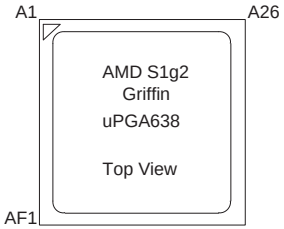
PROCESSOR POWER AND GROUND



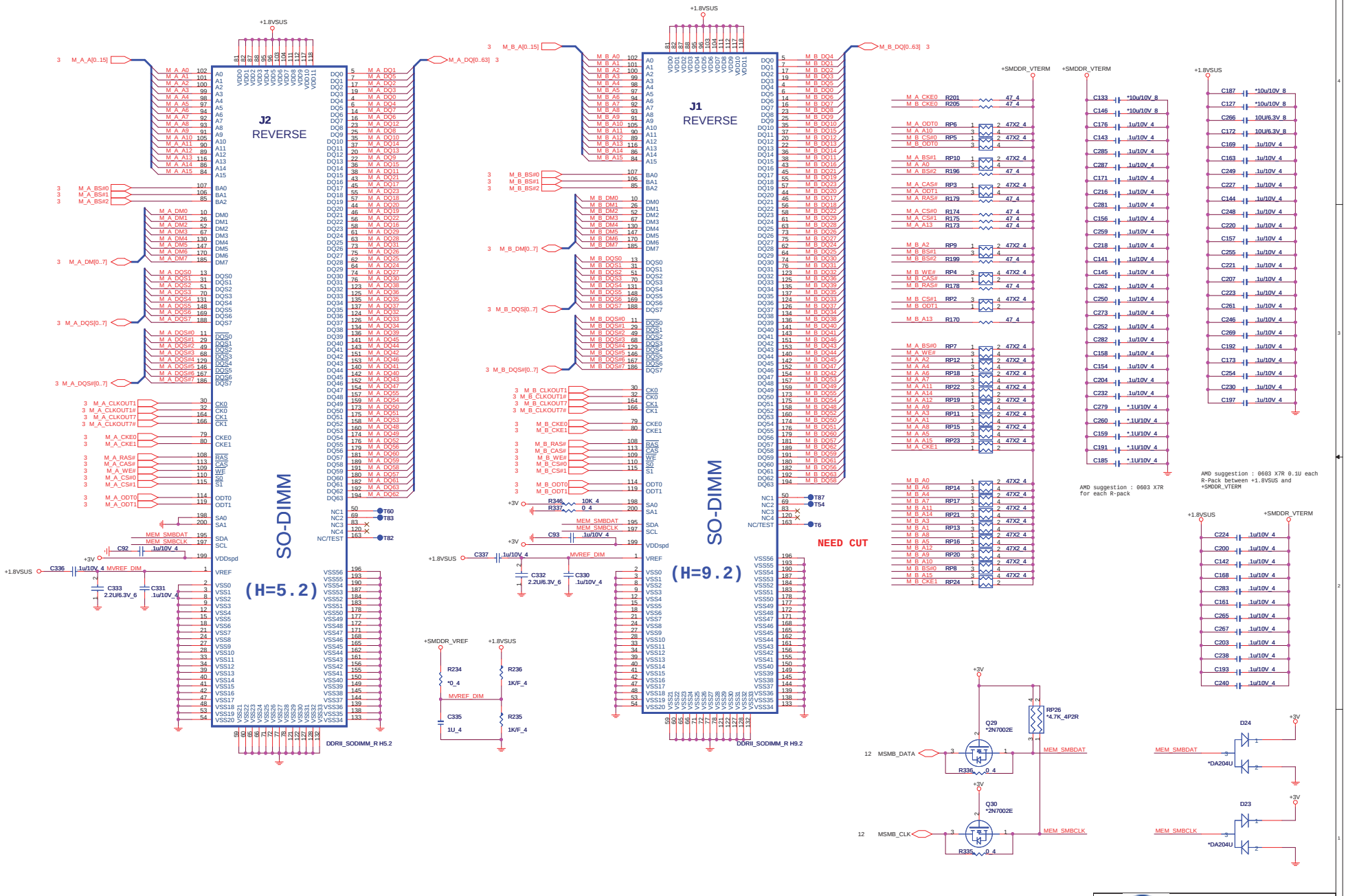


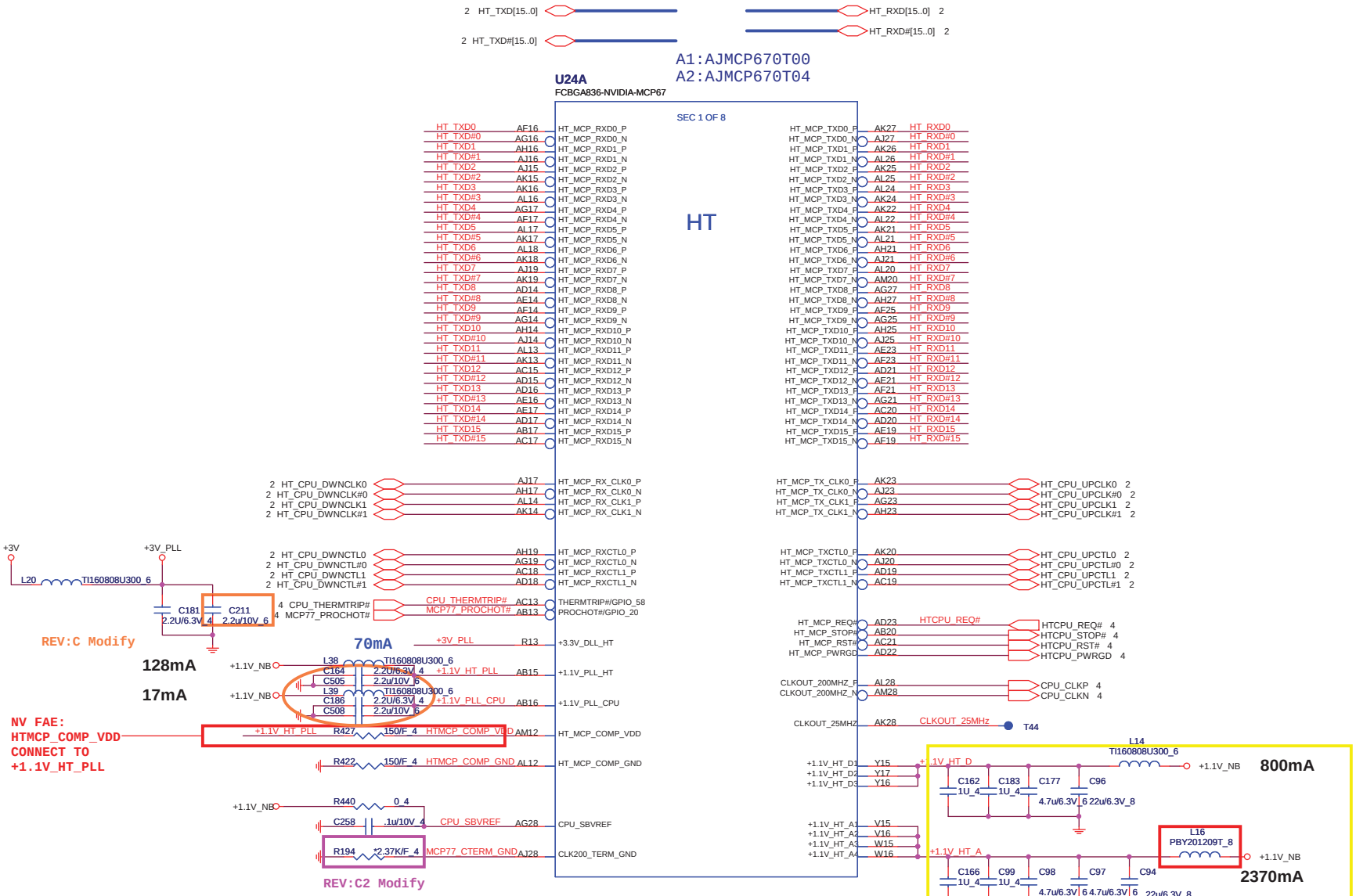


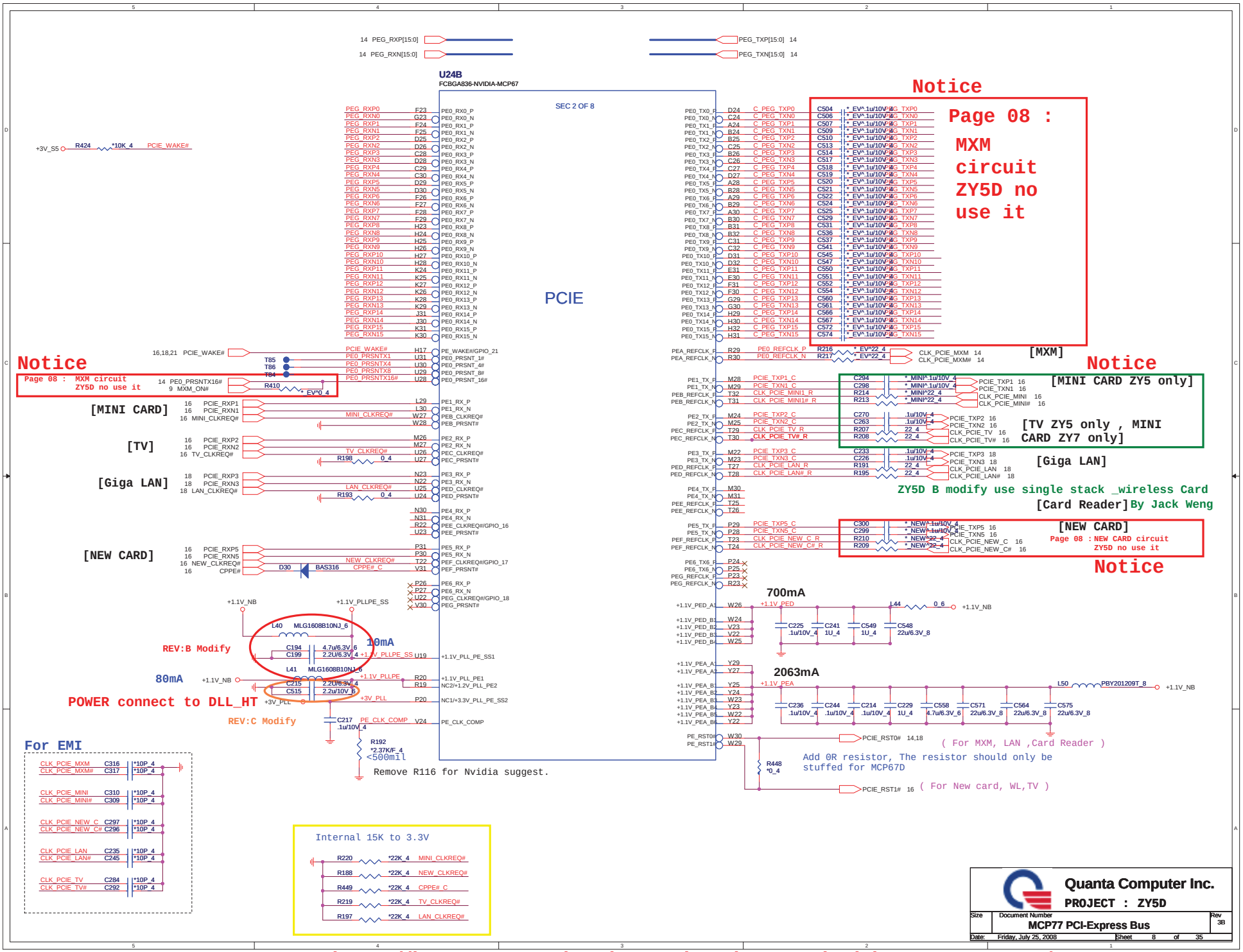


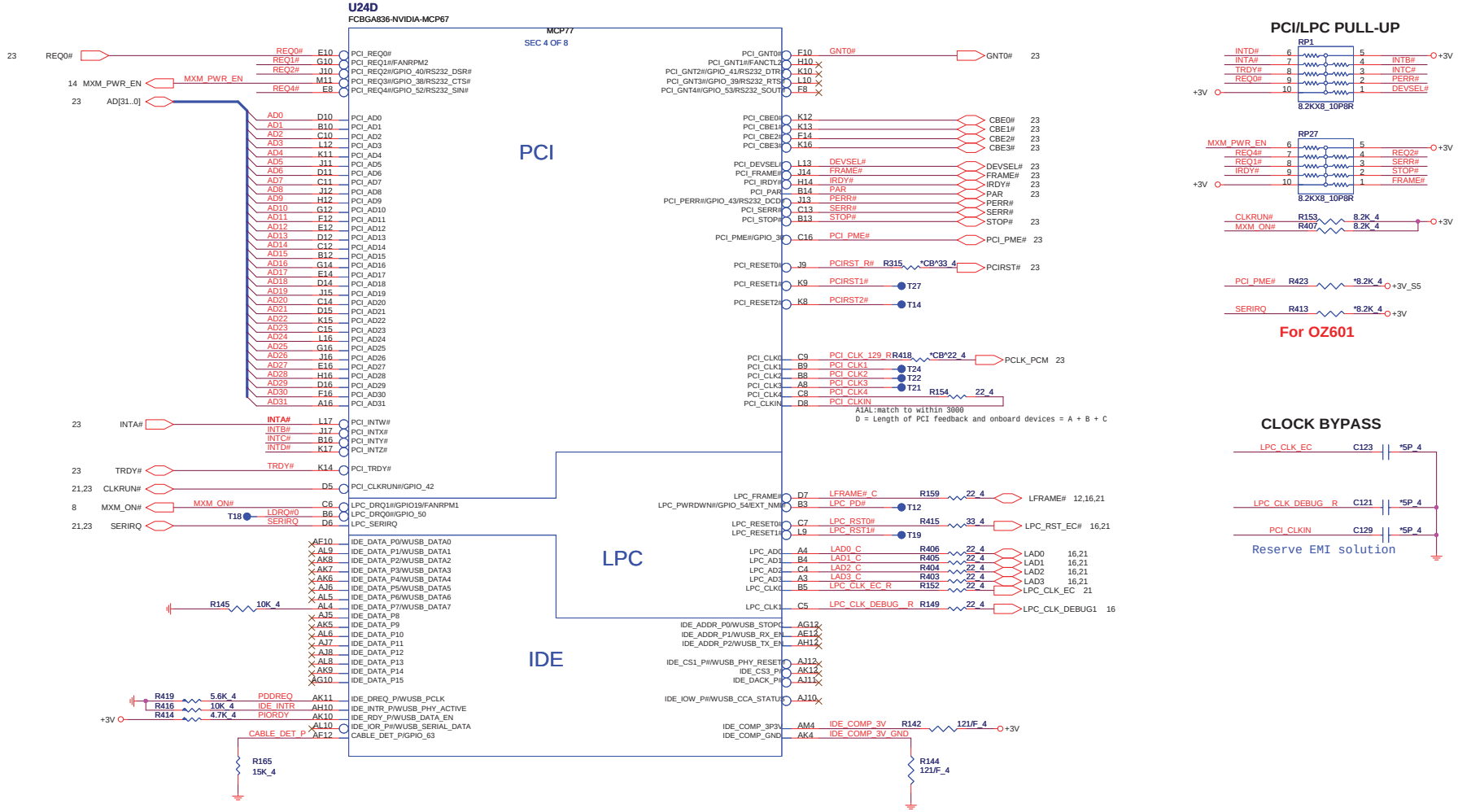


Quanta Computer Inc.		
PROJECT : ZY5D		
Size	Document Number: AMD Griffin PWR & GND	Rev: 3B
Date: Wednesday, May 21, 2008	Sheet 5 of 35	

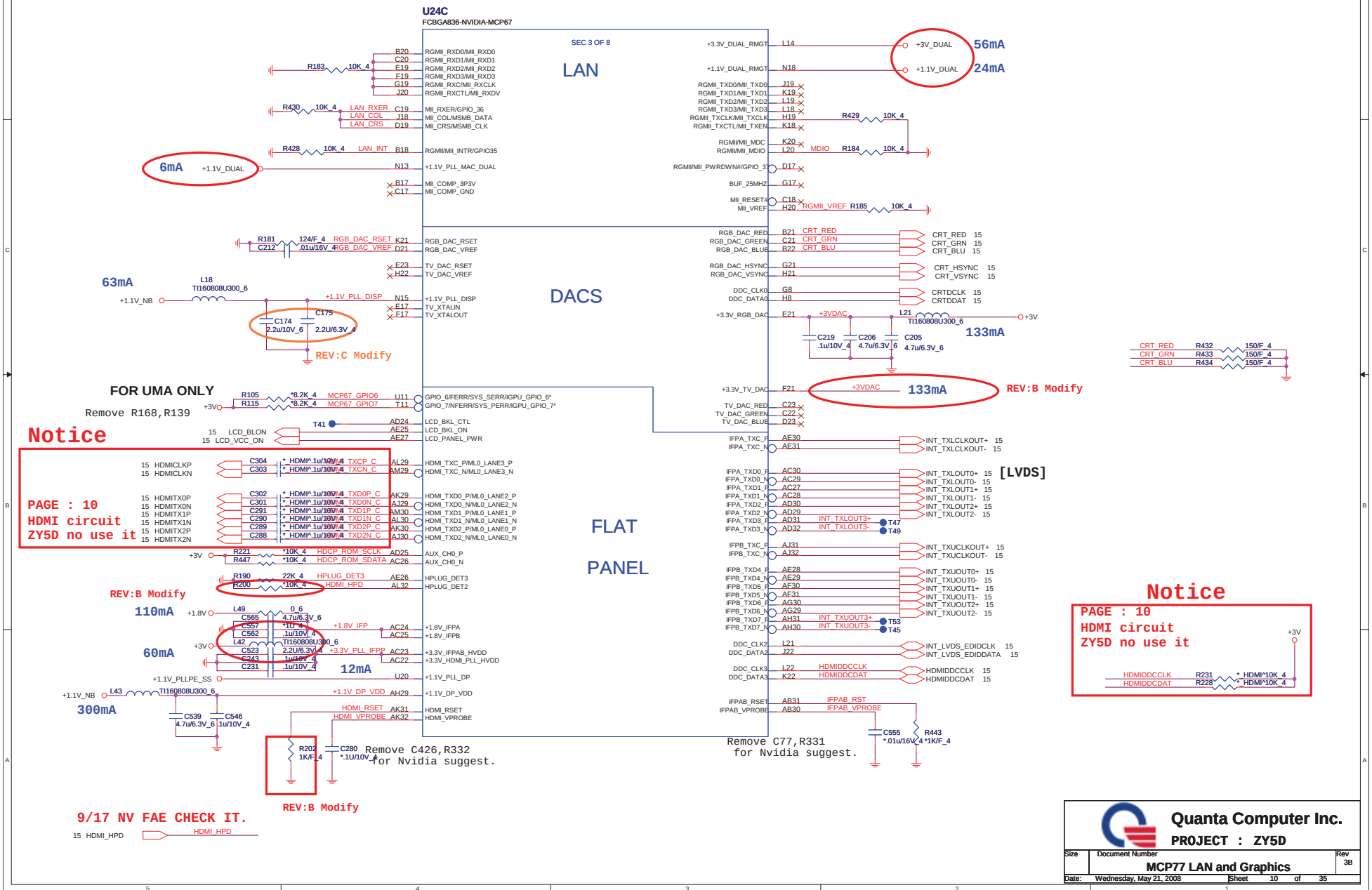


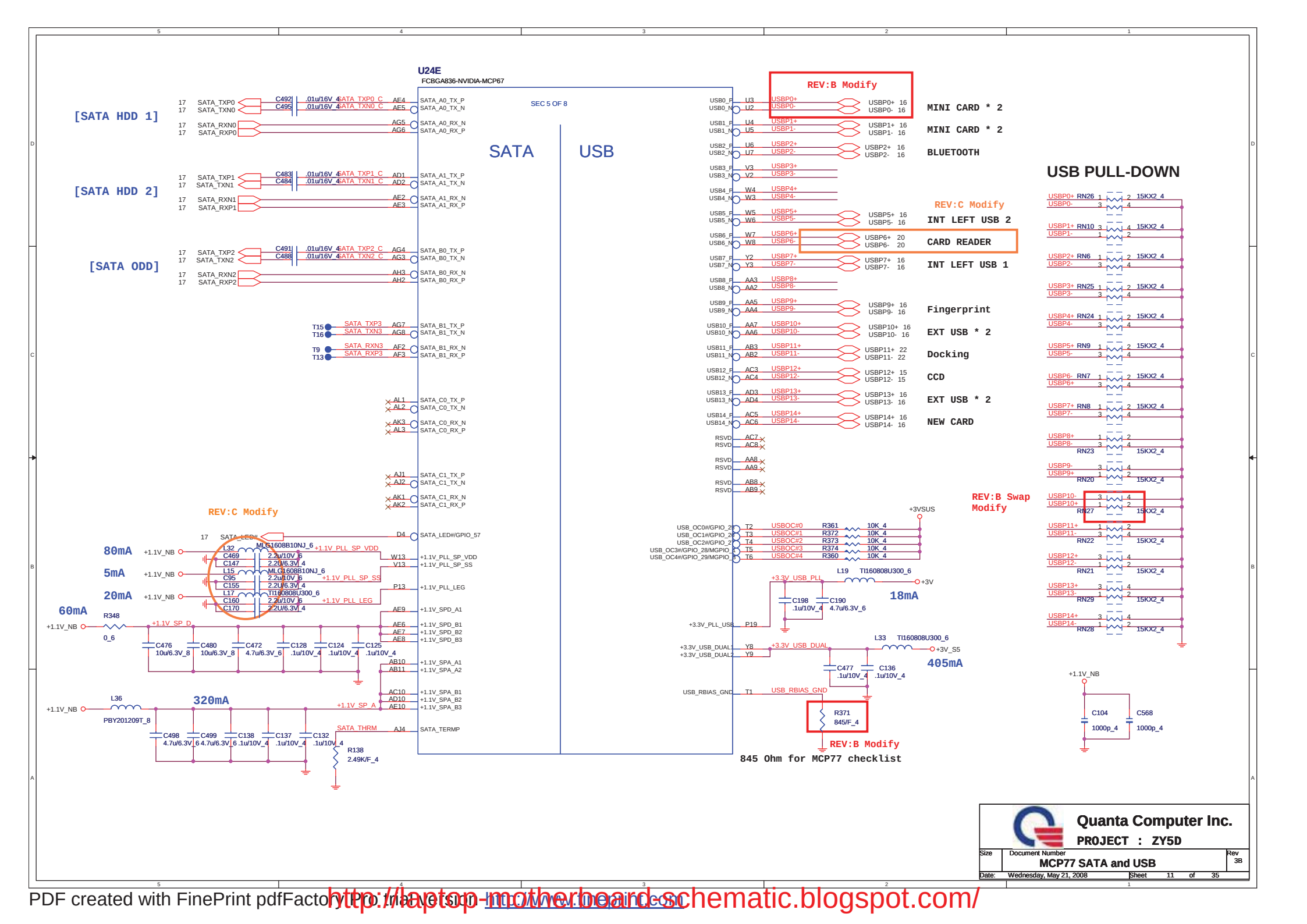


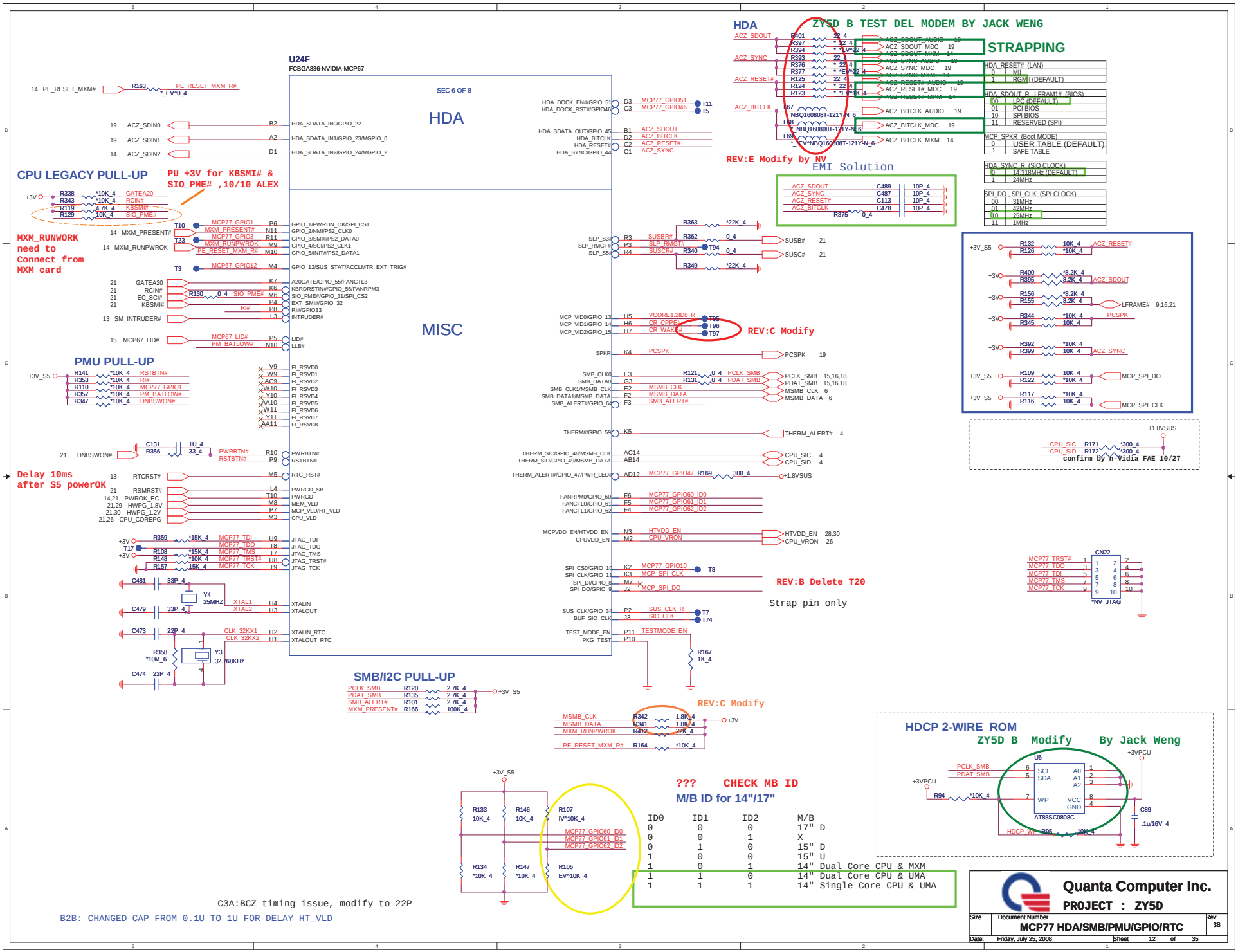




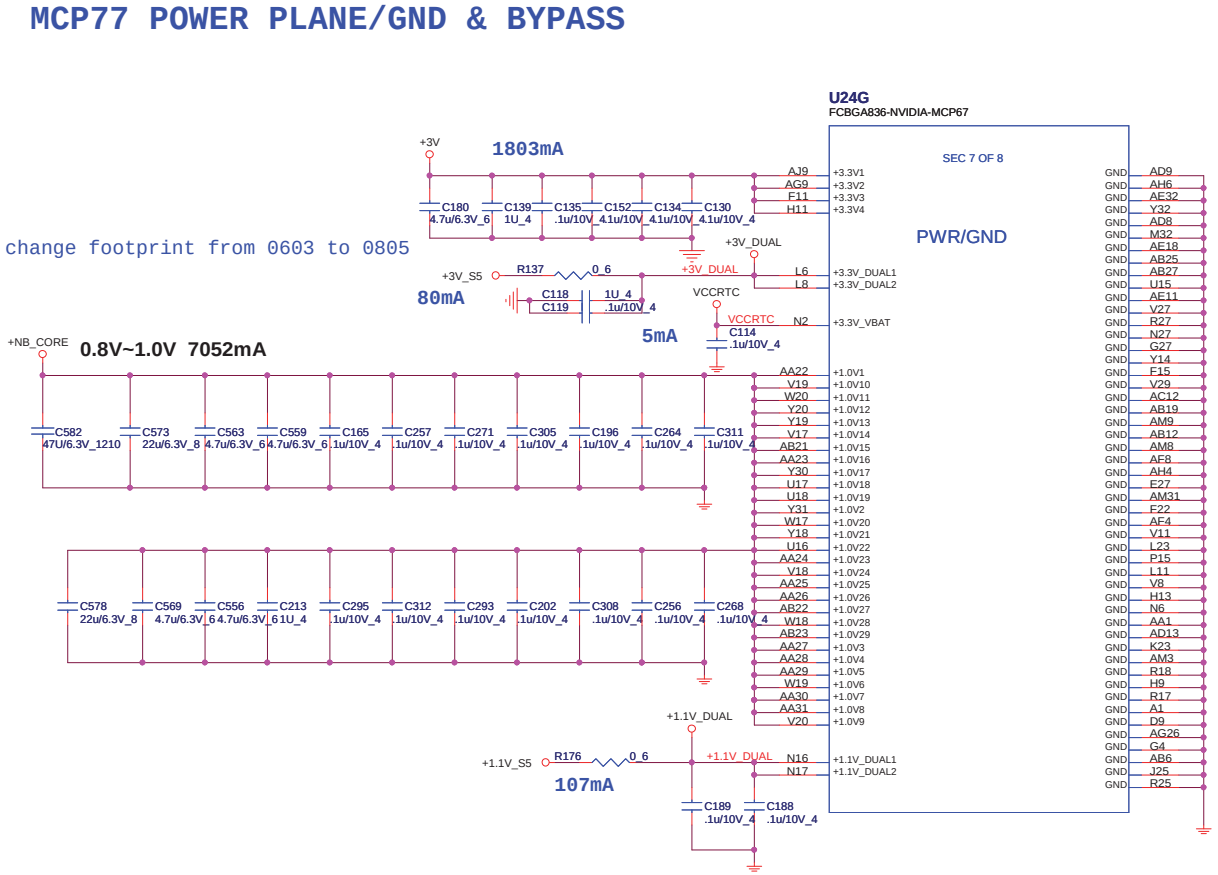
Quanta Computer Inc.			
PROJECT : ZY5D			
Size	Document Number		Rev
	MCP77 PCI/LPC/IDE		3B
Date: Wednesday, May 21, 2008	Sheet 9 of 35		

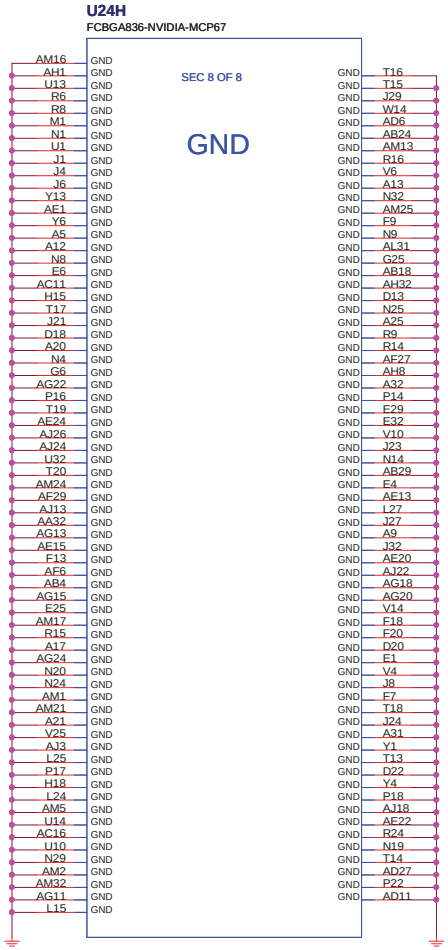


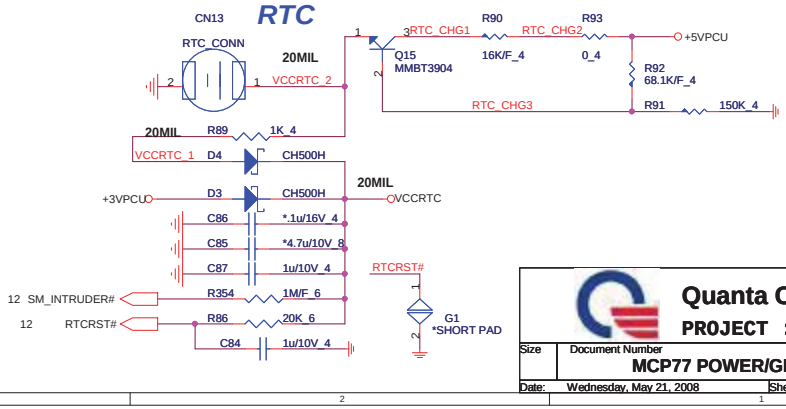




MCP77 POWER PLANE/GND & BYPASS



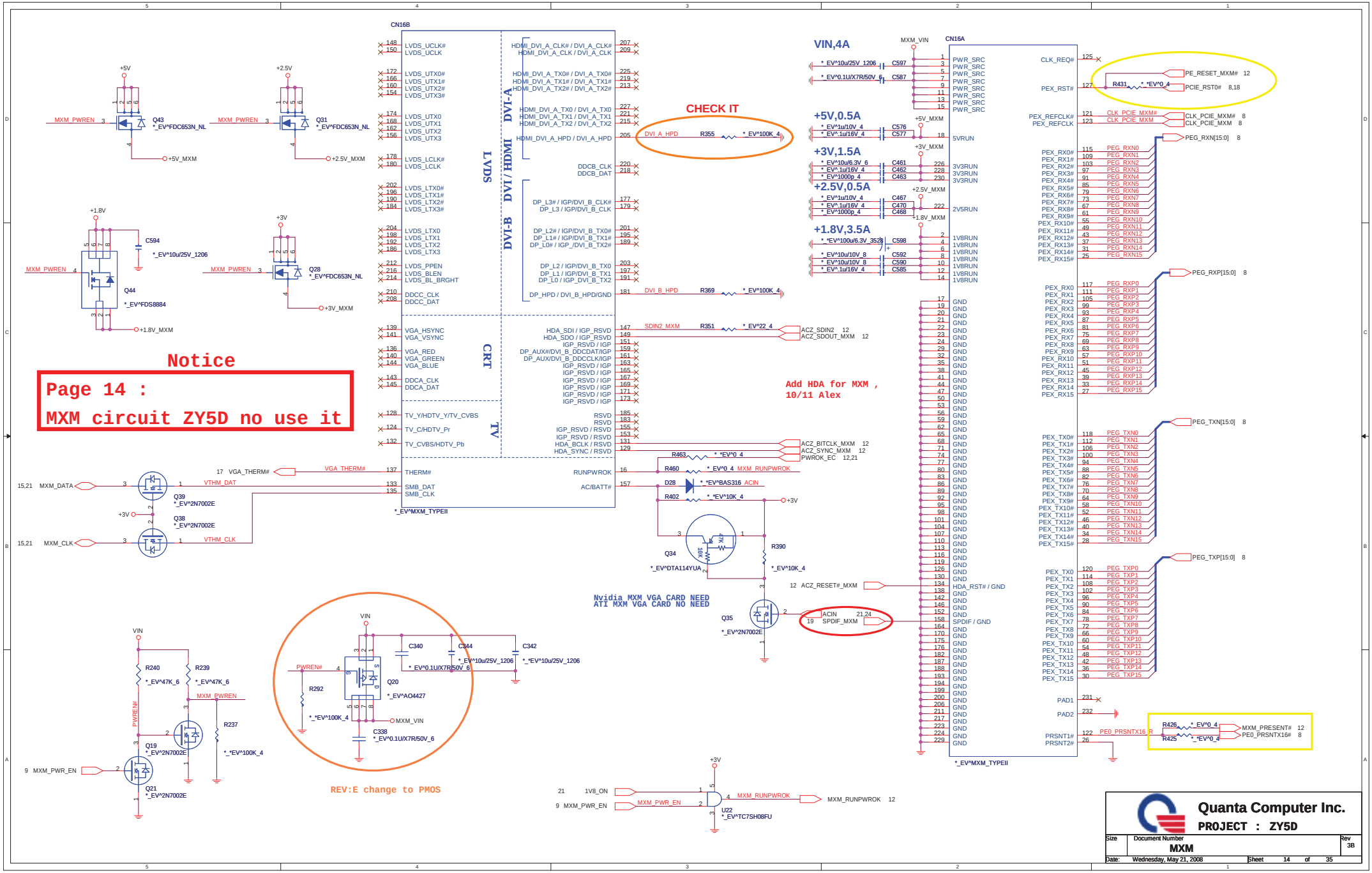




Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 POWER/GND	3B

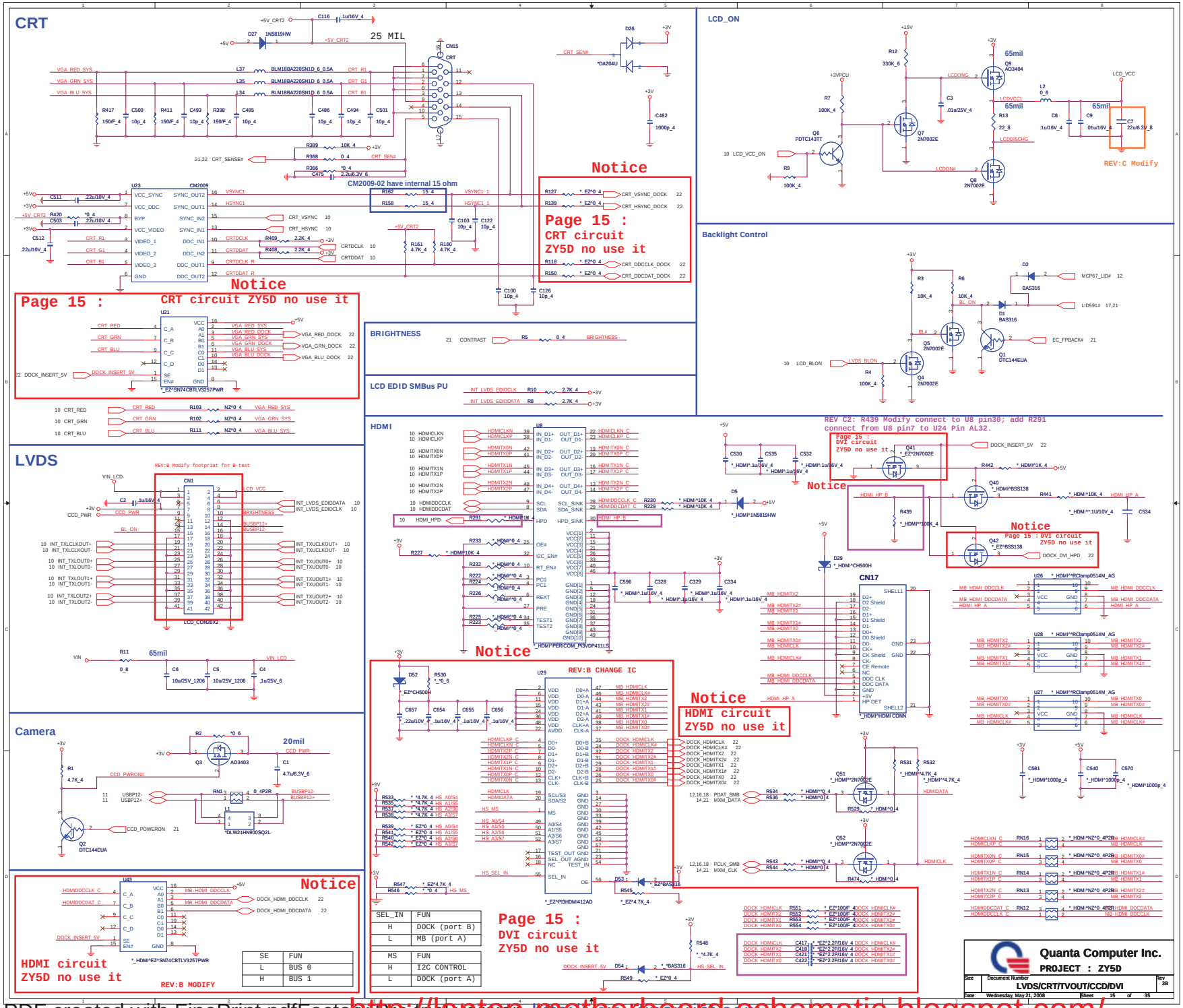
Date: Wednesday, May 21, 2008 Sheet 13 of 35

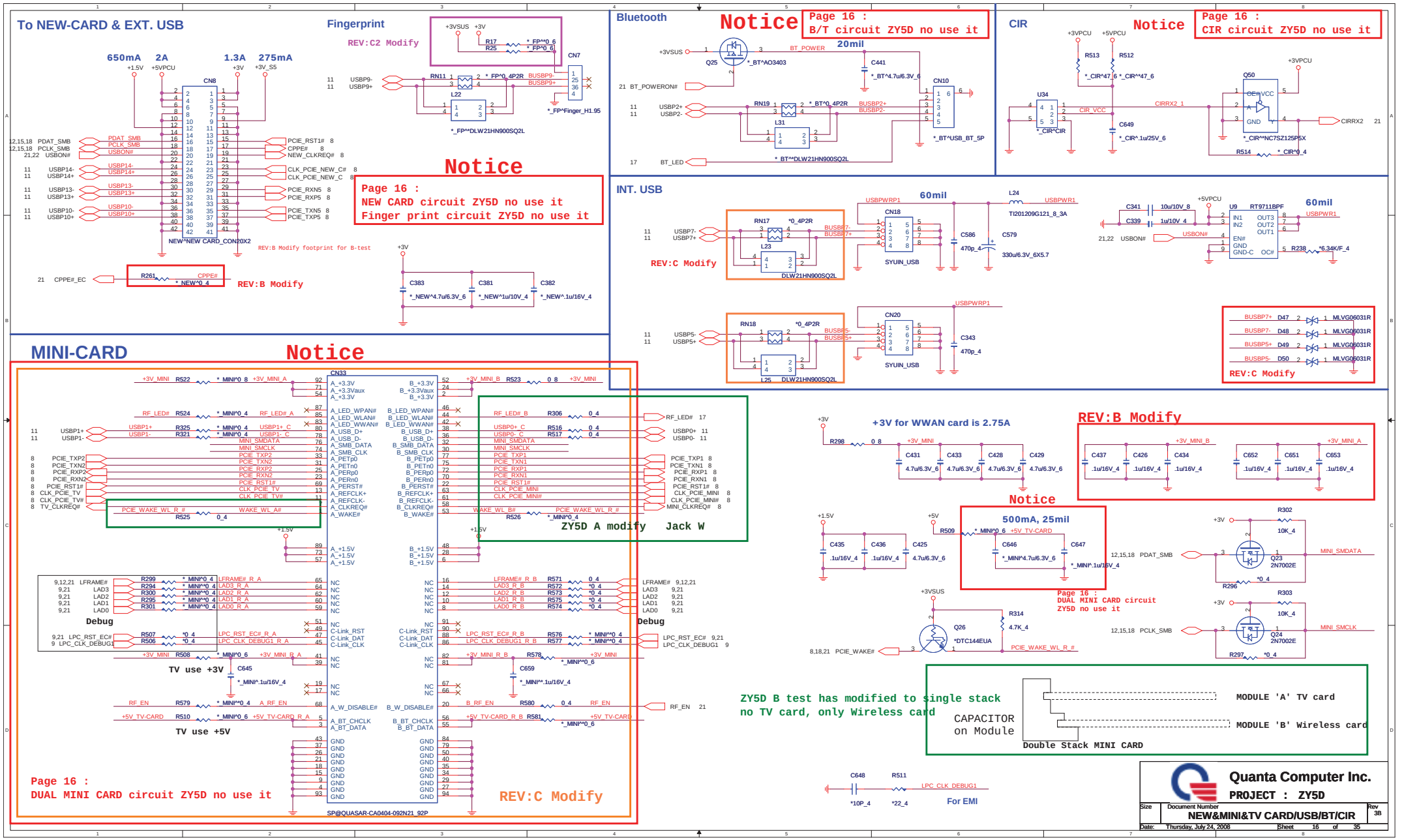


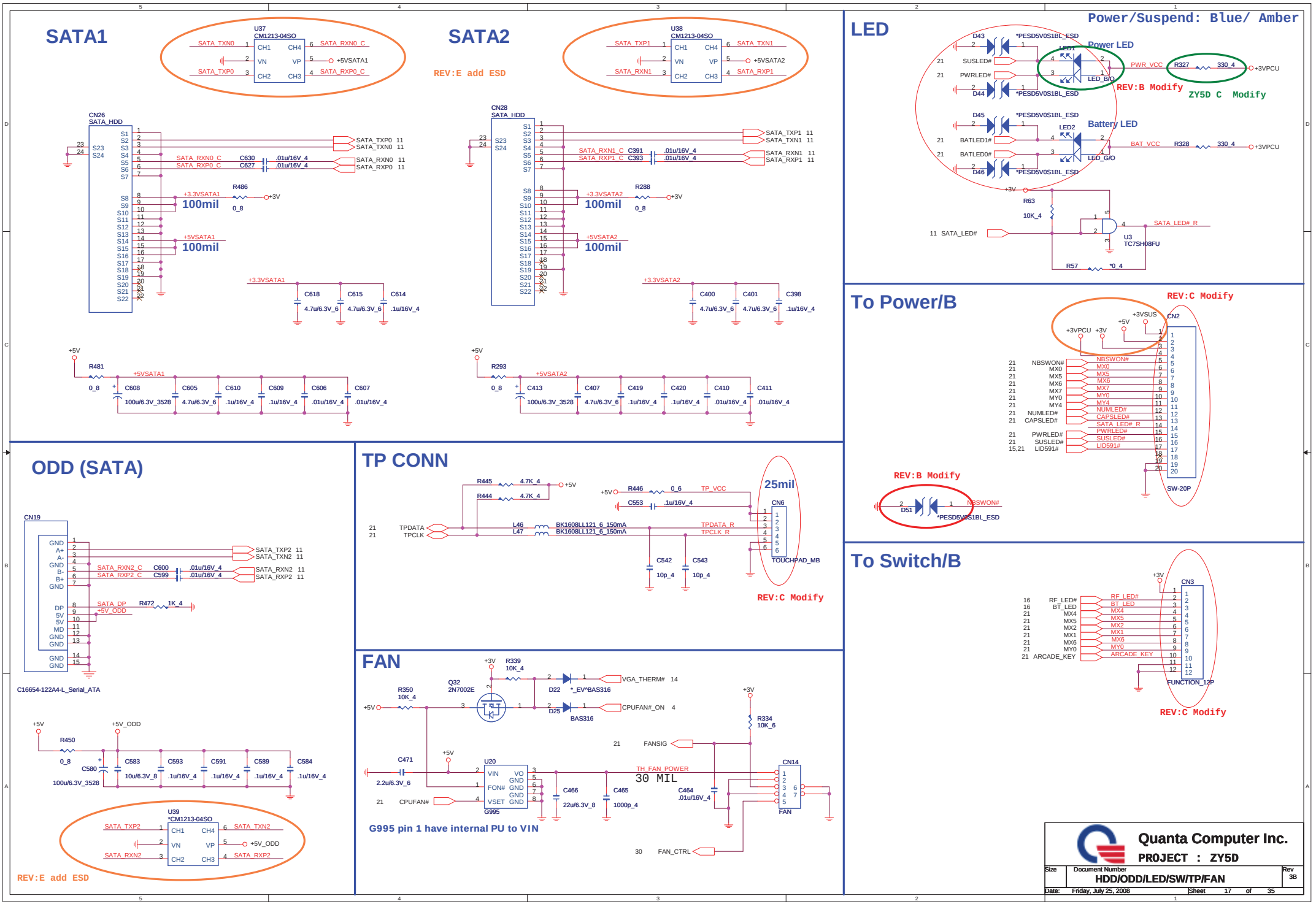
Notice

Page 14 :

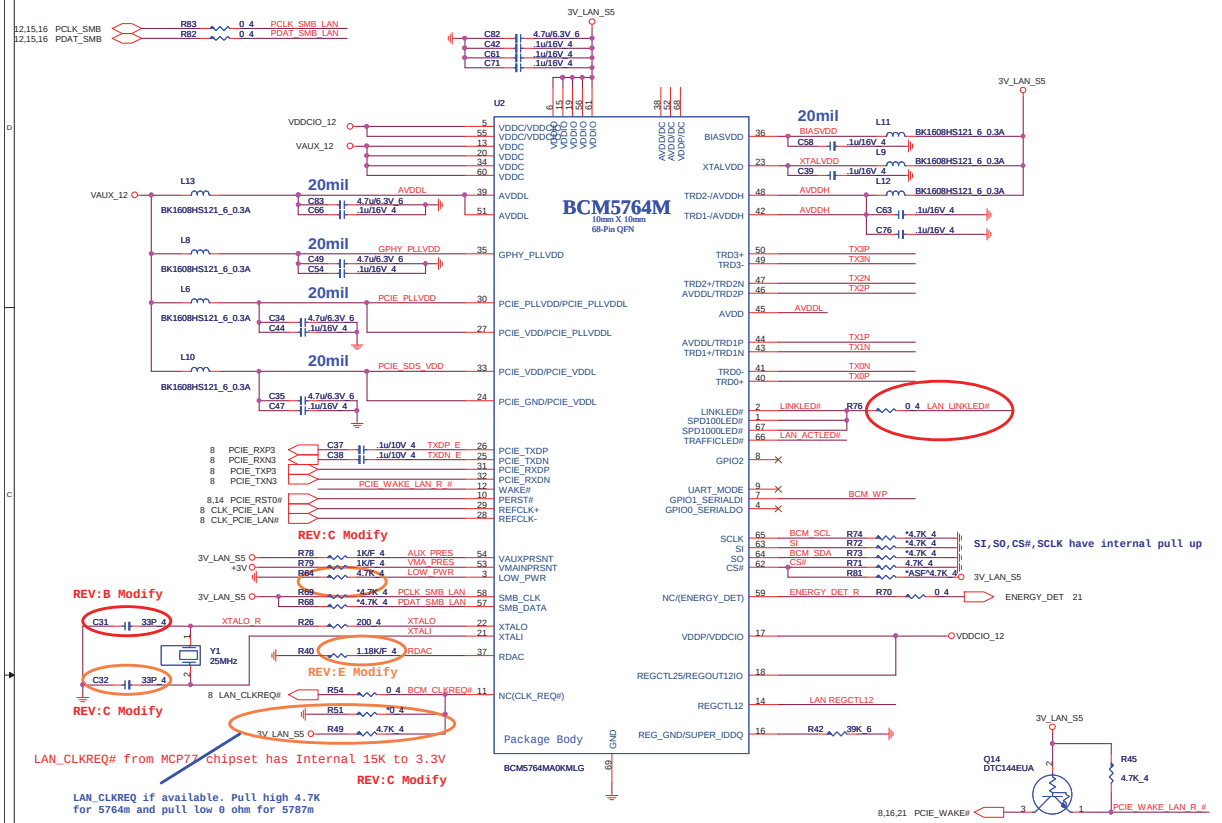
MXM circuit ZY5D no use it



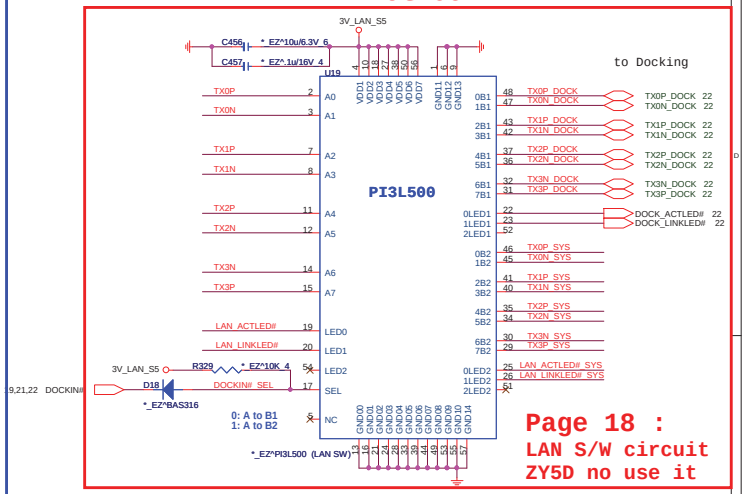




Giga LAN BCM5787M/5764M



LAN SWITCH

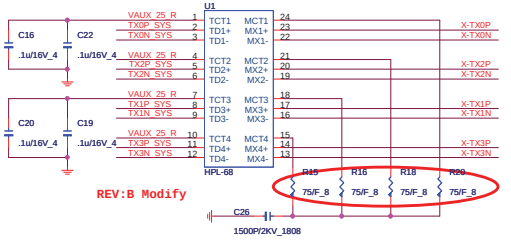


Notice

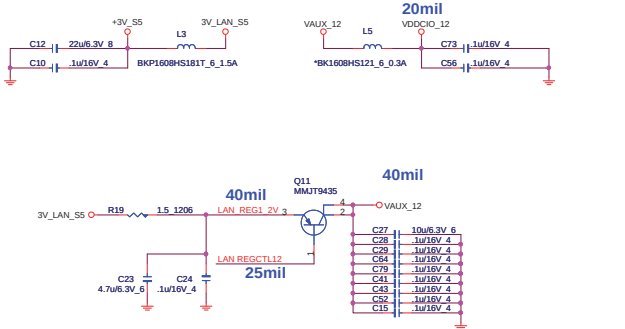
Page 18 :
LAN S/W circuit
ZY5D no use it

Transfomer

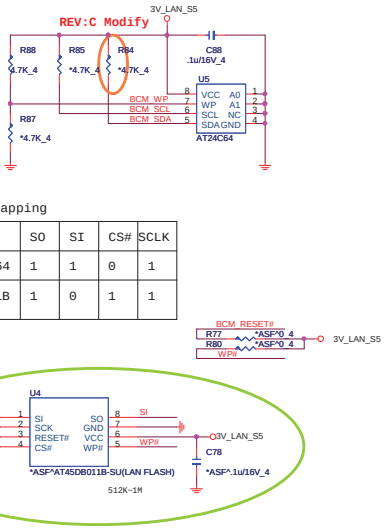
Source 1:	DELTA	LFE9249	DB0ZR1LAN11
Source 2:	Bothand	GST5009	DBKN1NLAN03



LAN POWER



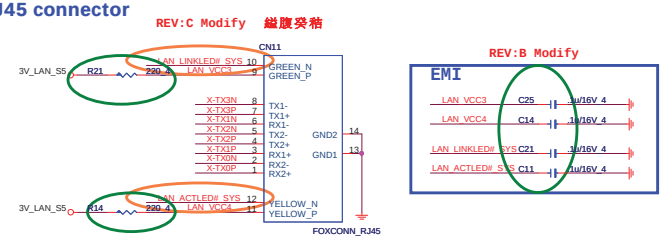
EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

RJ45 connector

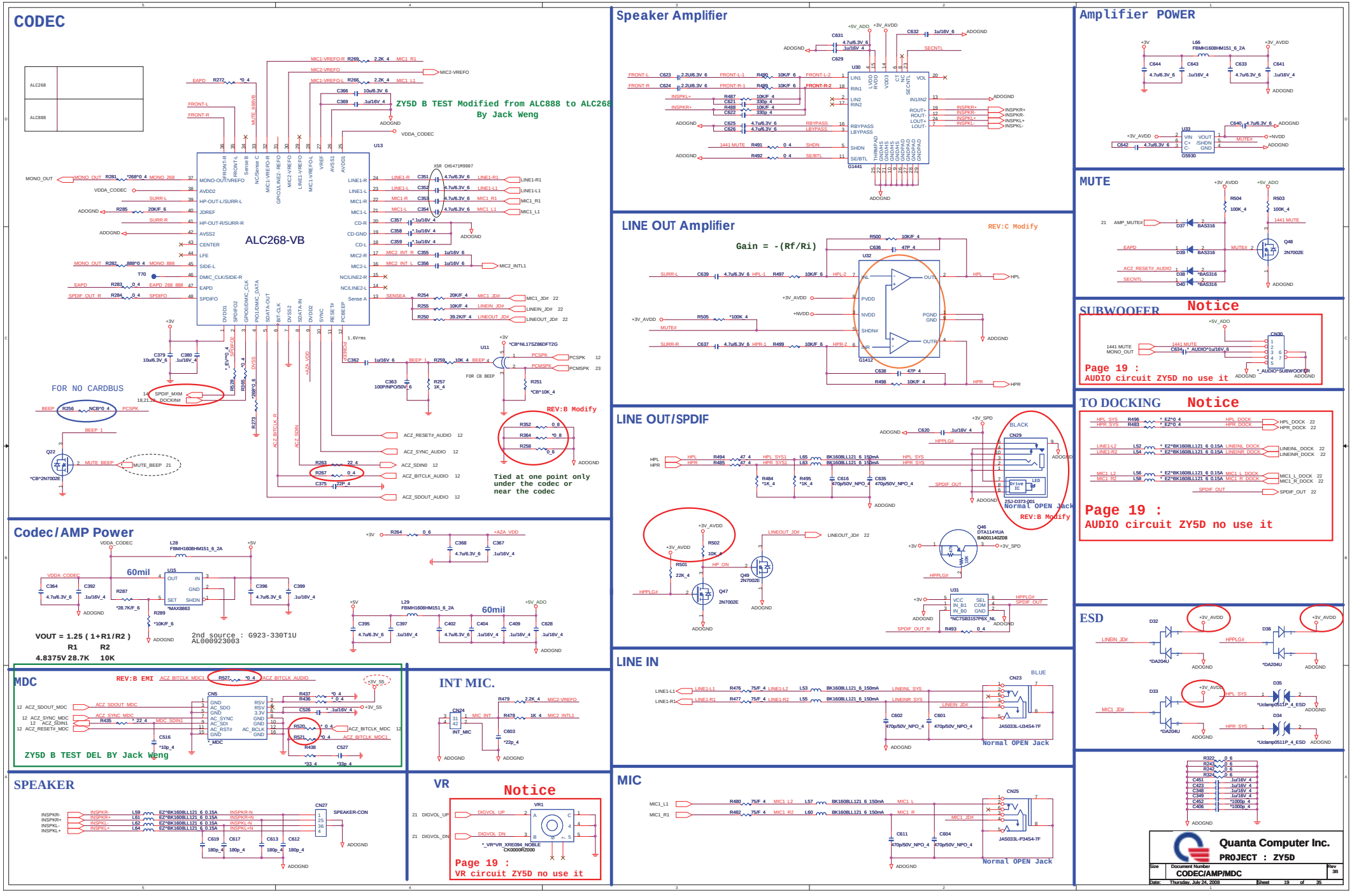


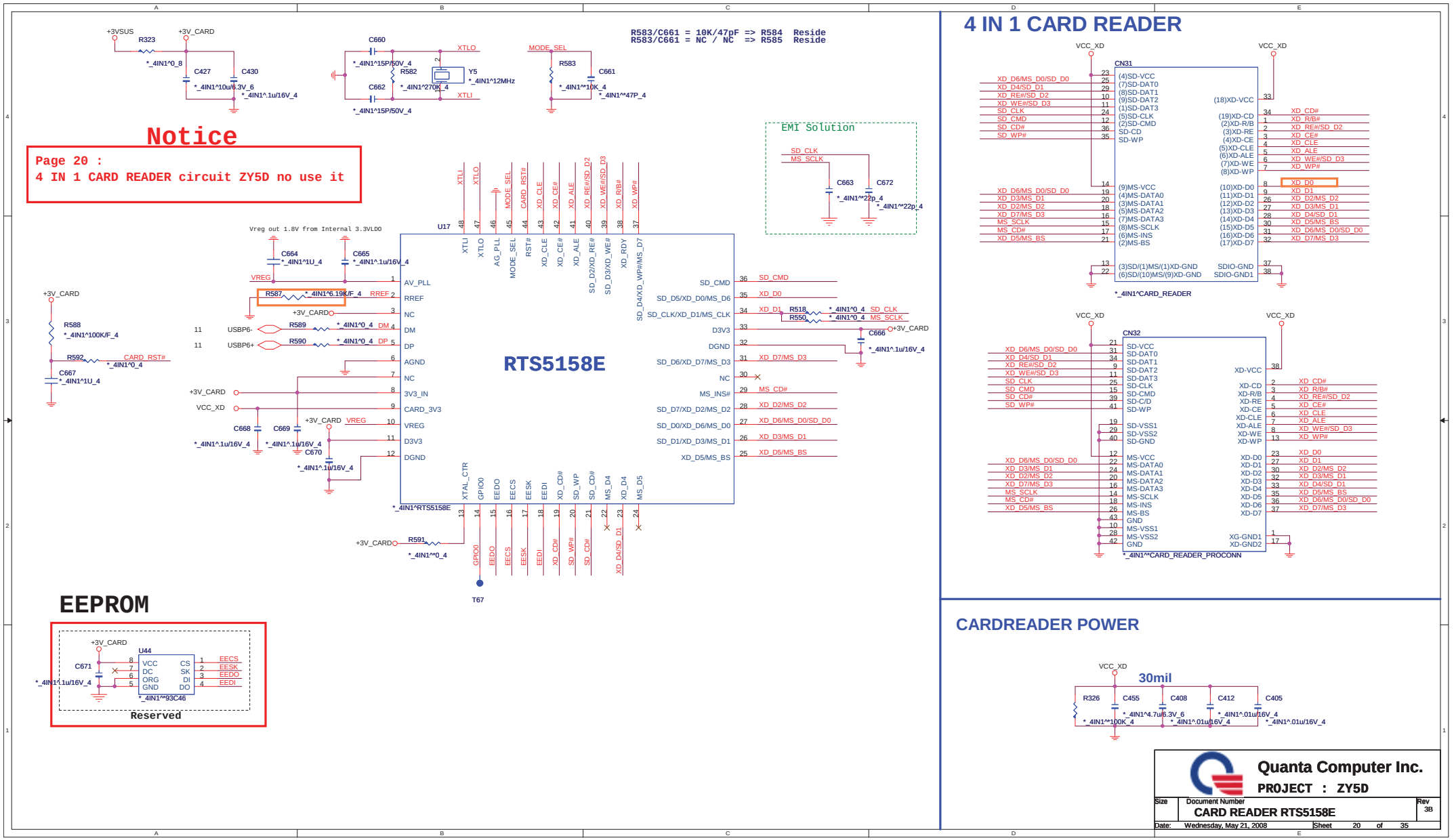
ZY5D C TEST Modified footprint from 0402 to 0805
to solve Lan burnt issue on Acer project
By Jack Weng

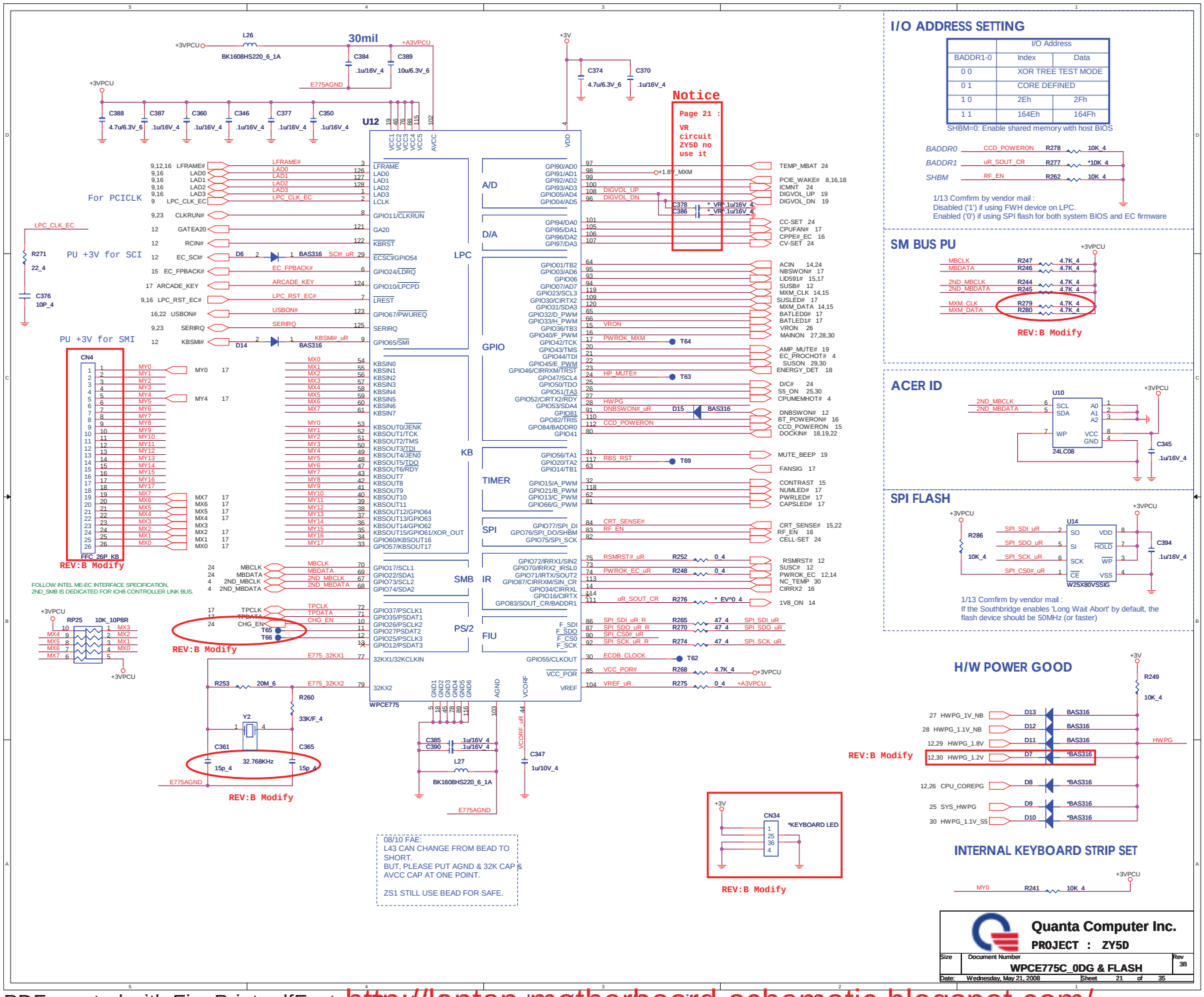
Quanta Computer Inc.
PROJECT : ZY5D

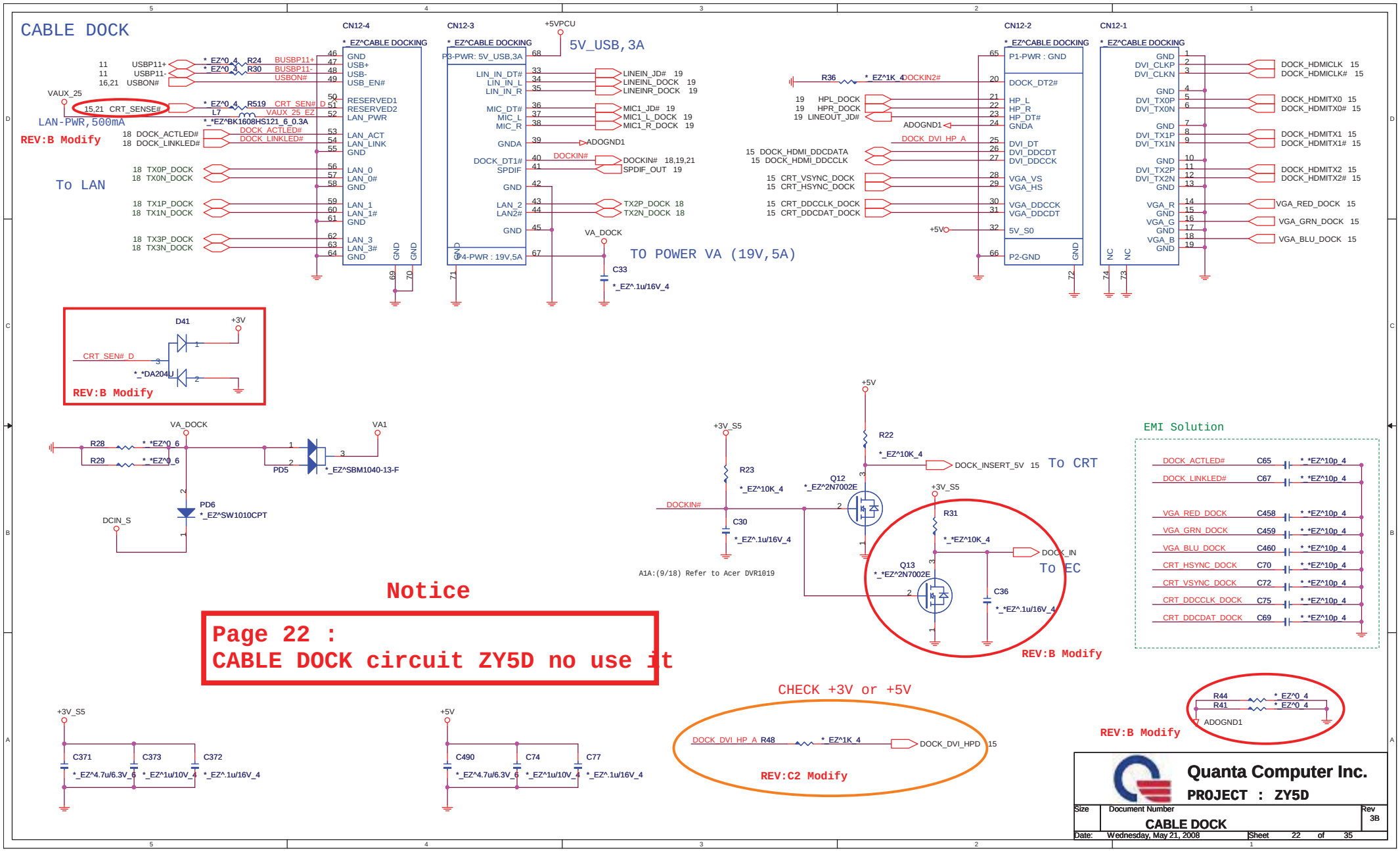
Size	Document Number	Rev
	GigaLAN BCM5787M/5764M & RJ45	3B

Date: Thursday, July 24, 2008 Sheet 18 of 35









NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R309 *CB^100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

For EMI

PCLK_PCM — R290 *CB^22_4 — C414 *CB^22p_4

IDSEL SELECT POWER-ON-STRAPPING (SEE NOTE & TABLE FOR OPTIONS)

+3V — C415 *CB^4.7u/6.3V_6, C416 *CB^.1u/16V_4, C403 *CB^.1u/16V_4, C439 *CB^.1u/16V_4

R313 *CB^33K/F_6 — VPPD0
R312 *CB^33K/F_6 — VCCD1

U16 *CB^OZ601T

64	CORE_VCC	VCC5#/VCCD0#/SDATA	124
77	CORE_VCC	VCC3#/VCCD1#/SCLK	125
97	CORE_VCC	VPP_PGM/VPPD0/SLATCH	123
115	CORE_VCC		
1	PCI_VCC		
20	PCI_VCC		
33	PCI_VCC		

9 AD[31..0]

AD31	4	AD31	CAD31 103 A_CAD31
AD30	5	AD30	CAD30 102 A_CAD30
AD29	6	AD29	CAD29 101 A_CAD29
AD28	7	AD28	CAD28 100 A_CAD28
AD27	8	AD27	CAD27 99 A_CAD27
AD26	9	AD26	CAD26 110 A_CAD26
AD25	10	AD25	CAD25 109 A_CAD25
AD24	13	AD24	CAD24 108 A_CAD24
AD23	14	AD23	CAD23 106 A_CAD23
AD22	15	AD22	CAD22 105 A_CAD22
AD21	16	AD21	CAD21 104 A_CAD21
AD20	17	AD20	CAD20 118 A_CAD20
AD19	18	AD19	CAD19 95 A_CAD19
AD18	19	AD18	CAD18 94 A_CAD18
AD17	21	AD17	CAD17 93 A_CAD17
AD16	22	AD16	CAD16 75 A_CAD16
AD15	28	AD15	CAD15 73 A_CAD15
AD14	29	AD14	CAD14 74 A_CAD14
AD13	30	AD13	CAD13 71 A_CAD13
AD12	31	AD12	CAD12 72 A_CAD12
AD11	34	AD11	CAD11 70 A_CAD11
AD10	35	AD10	CAD10 69 A_CAD10
AD9	36	AD9	CAD9 68 A_CAD9
AD8	37	AD8	CAD8 85 A_CAD8
AD7	38	AD7	CAD7 84 A_CAD7
AD6	39	AD6	CAD6 82 A_CAD6
AD5	40	AD5	CAD5 83 A_CAD5
AD4	41	AD4	CAD4 80 A_CAD4
AD3	42	AD3	CAD3 81 A_CAD3
AD2	43	AD2	CAD2 78 A_CAD2
AD1	44	AD1	CAD1 79 A_CAD1
AD0	46	AD0	CAD0 76 A_CAD0
PCM_IDSEL	127	IDSEL	

9 CBE3#	CBE3# 11	C/BE3#	CCLK 107 R_A_CCLK
9 CBE2#	CBE2# 12	C/BE2#	CFRAME# 114 A_CFRAME#
9 CBE1#	CBE1# 49	C/BE1#	CIRDY# 117 A_CIRDY#
9 CBE0#	CBE0# 50	C/BE0#	CTRDY# 116 A_CTRDY#
			CDEVSEL# 113 A_CDEVSEL#
9 PCLK_PCM	26	PCI_CLK	CSTOP# 61 A_CSTOP#
9 DEVSEL#	DEVSEL# 27	DEVSEL#	CPAR 58 A_CPAR
9 FRAME#	FRAME# 23	FRAME#	CPERR# 60 A_CPERR#
9 IRDY#	IRDY# 24	IRDY#	CSERR# 91 A_CSERR#
9 TRDY#	TRDY# 25	TRDY#	CREQ# 89 A_CREQ#
9 STOP#	STOP# 47	STOP#	CGNT# 62 A_CGNT#
9 PAR	PAR 48	PAR	CINT# 88 A_CINT#
			CBLOCK# 59 A_CBLOCK#
		PERR#/SPKR_OUT	CCLKRUN# 87 A_CCLKRUN#
19 PCMSPK	PCMSPK 51		CRST# 119 A_CRST# R311 *CB^47K SKT_VCC
9 REQ0#	REQ0# 2	REQ#	R2_D2 98 A_CRSVD/D2
9 GNT0#	GNT0# 3	GNT#	R2_D14 86 A_CRSVD/D14
			R2_A18 63 A_CRSVD/A18
9 PCIRST#	R308 *CB^0_4 PCIRST#_R 126	RST#	CVS1 57 A_CVS1#
9 PCI_PME#	R310 *CB^0_4 PCM_PME# 120	PME#/RI_OUT#	CVS2 121 A_CVS2#
			CCD1# 56 A_CCD1#
9,21 CLKRUN#	55	MF6 (CLKRUN#)	CCD2# 122 A_CCD2#
		MF4 (RI_OUT#)	CAUDIO 92 A_CAUDIO
9,21 SERIRQ	SERIRQ 53	MF3 (SERIRQ#)	CSTSCHG 90 A_CSTSCHG
9 INTA#	52	MF0 (INTA#)	
			CC/BE3# 111 A_CC/BE3#
			CC/BE2# 112 A_CC/BE2#
			CC/BE1# 66 A_CC/BE1#
			CC/BE0# 67 A_CC/BE0#

GND GND GND GND GND — 32 45 65 96 128

R_A_CCLK R307 *CB^33_4 A_CCLK

PCMCIA SOCKET

CN9 — Check it

A_CAD0	2	GND1	SKTA/VCC1 17 SKT_VCC
A_CAD1	3	SKTAAD0/D3	SKTA/VCC2 51
A_CAD3	4	SKTAAD1/D4	
A_CAD5	5	SKTAD3/D5	SKTA/VPP1 18
A_CAD7	6	SKTAD5/D6	SKTA/VPP2 52
A_CC/BE0#	7	SKTAAD7/D7	
A_CAD9	8	-SKTACBE0/CE1#	
A_CAD11	9	SKTAAD9/A10	GND5 69
A_CAD12	10	SKTABAD11/OE#	GND6 70
A_CAD14	11	SKTAAD12/A11	GND7 71
A_CC/BE1#	12	SKTAAD14/A9	GND8 72
A_CPAR	13	-SKTACBE1/A8	GND9 73
A_CPERR#	14	SKTAPAR/A13	GND10 74
A_CGNT#	15	-SKTAPERR/A14	GND11 75
A_CINT#	16	-SKTAGNT/WE#	GND12 76
		-SKTAINT/RDY	GND13 77
		UPPER PIN	GND14 78
A_CCLK	19	SKTAPCLK/A16	GND15 79
A_CIRDY#	20	-SKTAIRDY/A15	GND16 80
A_CC/BE2#	21	-SKTACBE2/A12	GND17 81
A_CAD18	22	SKTAAD18/A7	GND18 82
A_CAD20	23	SKTAAD20/A6	GND19 83
A_CAD21	24	SKTAAD21/A5	GND20 84
A_CAD22	25	SKTAAD22/A4	
A_CAD23	26	SKTAAD23/A3	
A_CAD24	27	SKTAAD24/A2	
A_CAD25	28	SKTAAD25/A1	NC 85
A_CAD26	29	SKTAAD26/A0	NC 86
A_CAD27	30	SKTAAD27/D0	NC 87
A_CAD29	31	SKTAAD29/D1	NC 88
A_CRSVD/D2	32	SKTARSVD/D2	
A_CCLKRUN#	33	-SKTACLKRUN/WP	
	34	GND2	
	35	GND3	
A_CCD1#	36	-SKTACD1/CD1#	
A_CAD2	37	SKTAAD2/D11	
A_CAD4	38	SKTAD4/D12	
A_CAD6	39	SKTAAD6/D13	
A_CRSVD/D14	40	SKTARSVD/D14	
A_CAD8	41	SKTAAD8/D15	
A_CAD10	42	SKTAD10/CE2#	
A_CVS1#	43	-SKTAVS1/VS1#	
A_CAD13	44	SKTAAD13/IORD#	
A_CAD15	45	SKTAAD15/IOWR#	
A_CAD16	46	SKTAAD16/A17	
A_CRSVD/A18	47	-SKTRSVD/A18	
A_CBLOCK#	48	-SKTALOCK/A19	
A_CSTOP#	49	-SKTASTOP/A20	
A_CDEVSEL#	50	-SKTADEVSEL/A21	
		LOWER PIN	
A_CTRDY#	53	-SKTATRDY/A22	
A_CFRAME#	54	-SKTAFRAME/A23	
A_CAD17	55	SKTAAD17/A24	
A_CAD19	56	SKTAAD19/A25	
A_CVS2#	57	-SKTAVS2VS2#	
A_CRST#	58	-SKTARST/RESET	
A_CSERR#	59	0SKTASERR/WAIT#	
A_CREQ#	60	-SKTAREQ/INPACK#	
A_CC/BE3#	61	-SKTACBE3/REG#	
A_CAUDIO	62	SKTAAUDIO/BVD2	
A_CSTSCHG	63	-SKTASTSCHG/BVD1	
A_CAD28	64	SKTAAD28/D8	
A_CAD30	65	SKTAAD30/D9	
A_CAD31	66	SKTAAD31/D10	
A_CCD2#	67	-SKTACD2/CD2#	
	68	GND4	

*CB^PCMCIA_SOCKET

Footprint

SKT_VCC — +3V — +5V

C443 C449 *CB^4.7u/6.3V_6 *CB^.1u/16V_4
C453 C450 *CB^4.7u/6.3V_6 *CB^.1u/16V_4
C442 C444 *CB^4.7u/6.3V_6 *CB^.1u/16V_4

U18 *CB^OZ2210G

6	VCC1	+3.3	1
5	VCC2	+3.3	2
7	VCC5#	+5V	3
8	VCC3#	GND	4

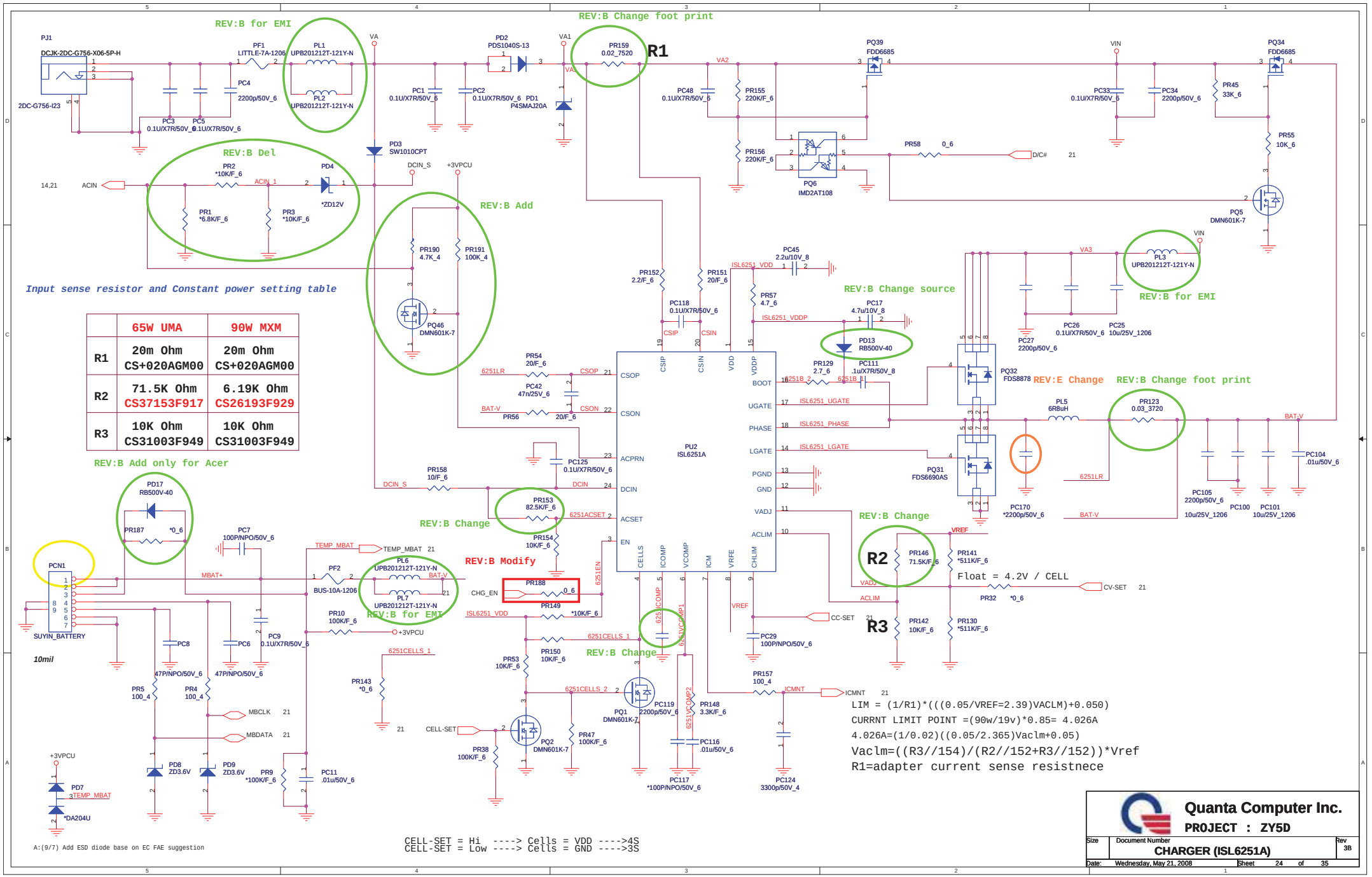
VCCD0 VCCD1

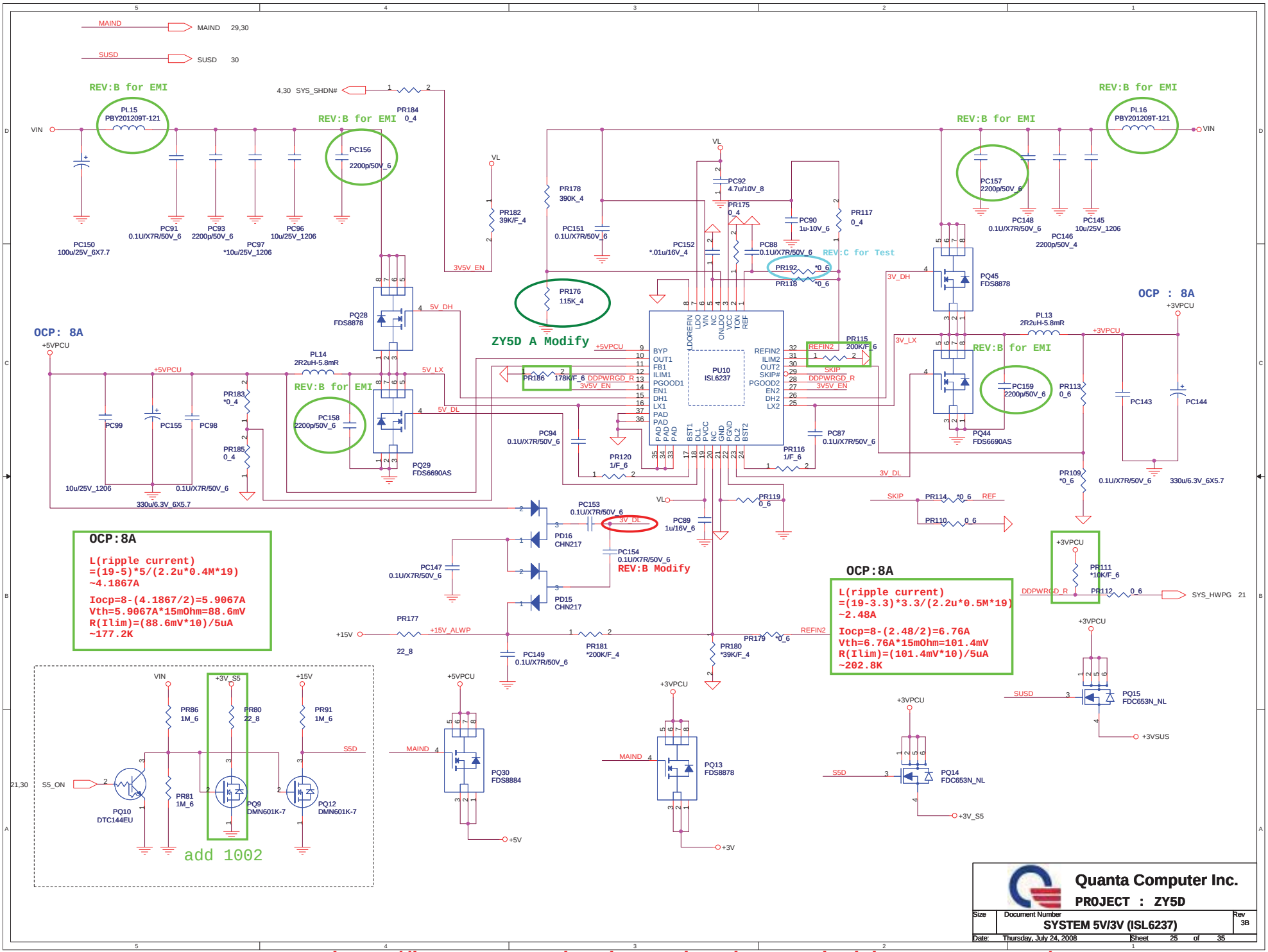
Check Footprint & P/N

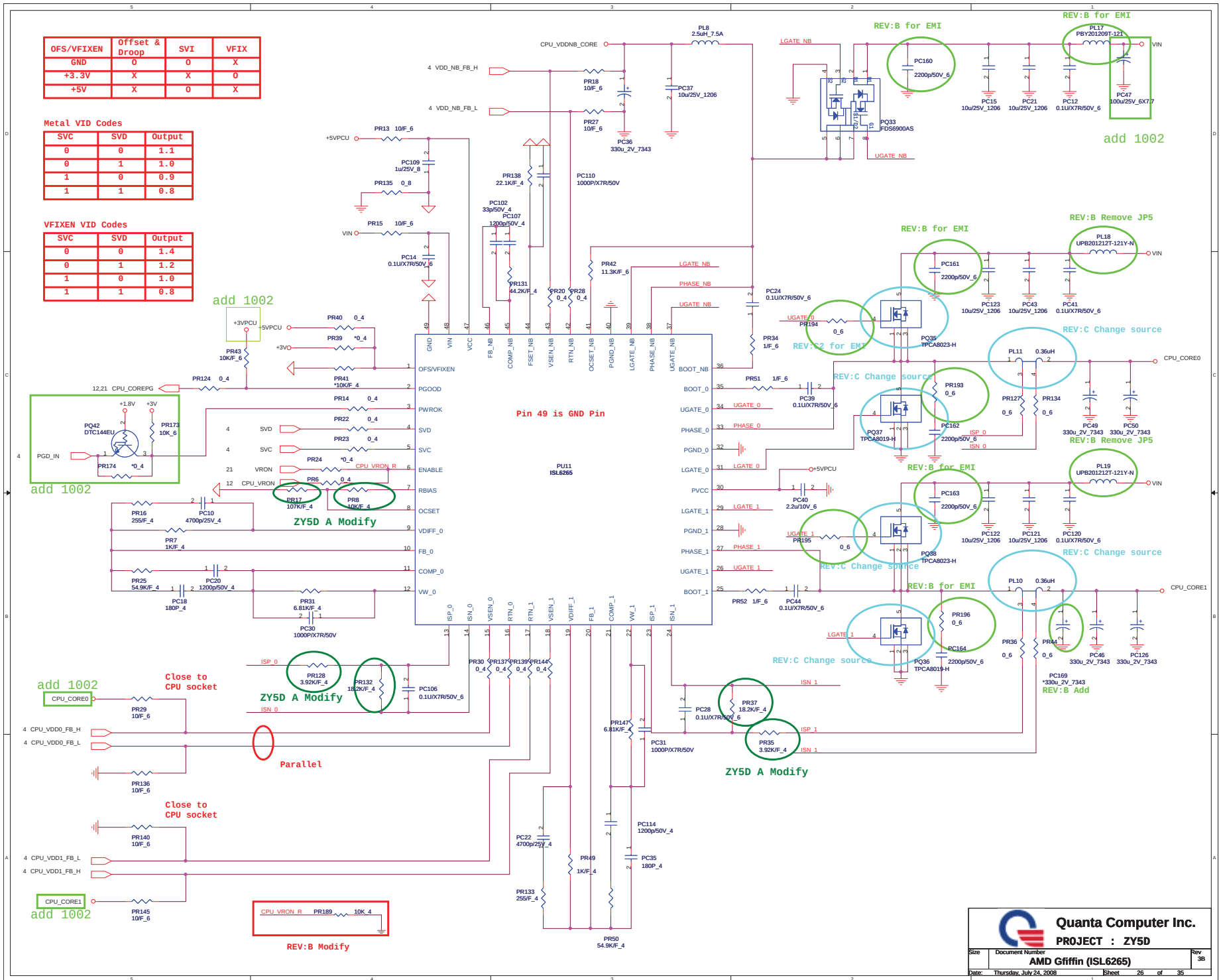
22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

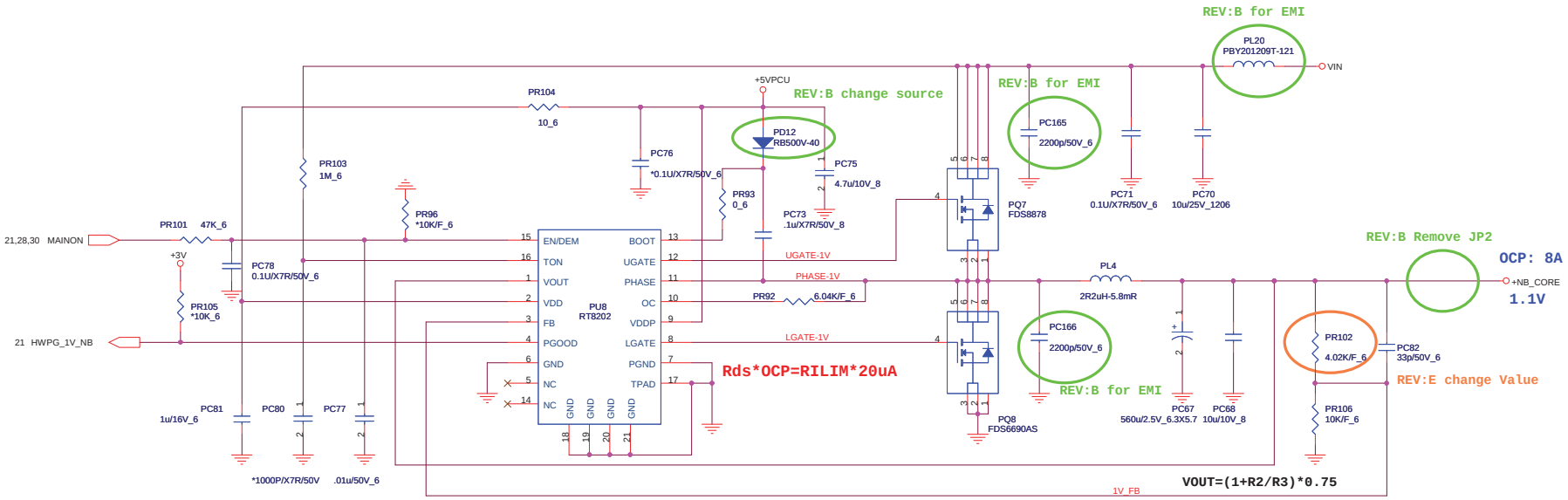
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	PCMCIA(OZ601)	3B
Date: Wednesday, May 21, 2008	Sheet 23 of 35	







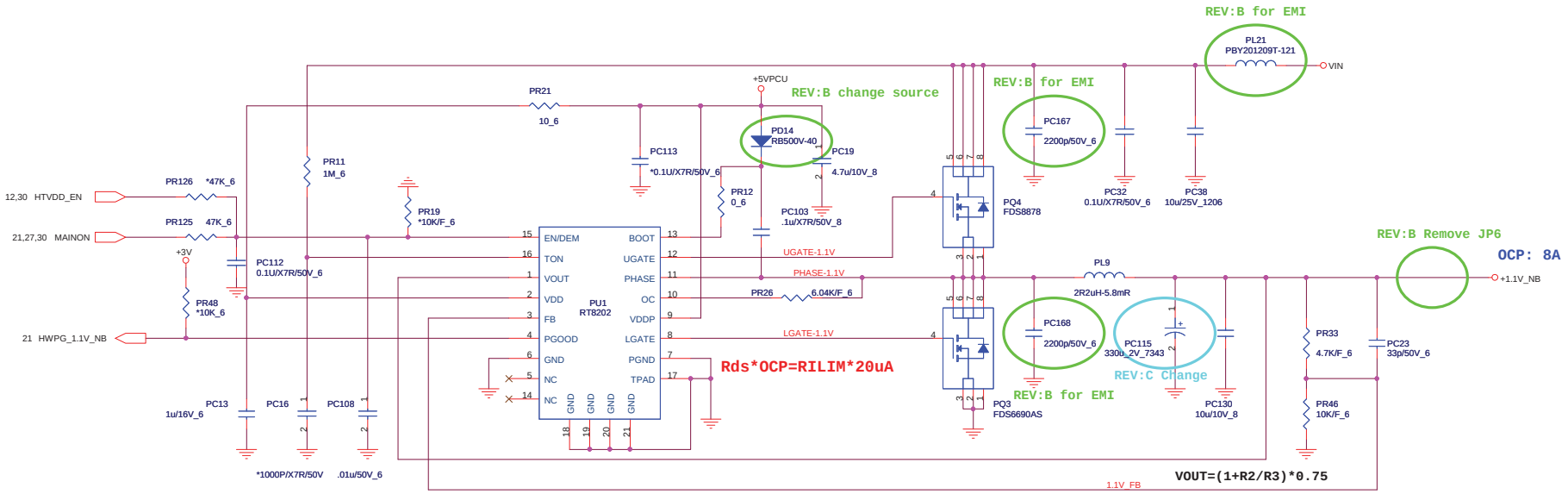


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm

Quanta Computer Inc.		
PROJECT : ZY5D		
Size	Document Number: NB_CORE(RT8202)	Rev: 3B
Date: Wednesday, May 21, 2008	Sheet 27 of 35	

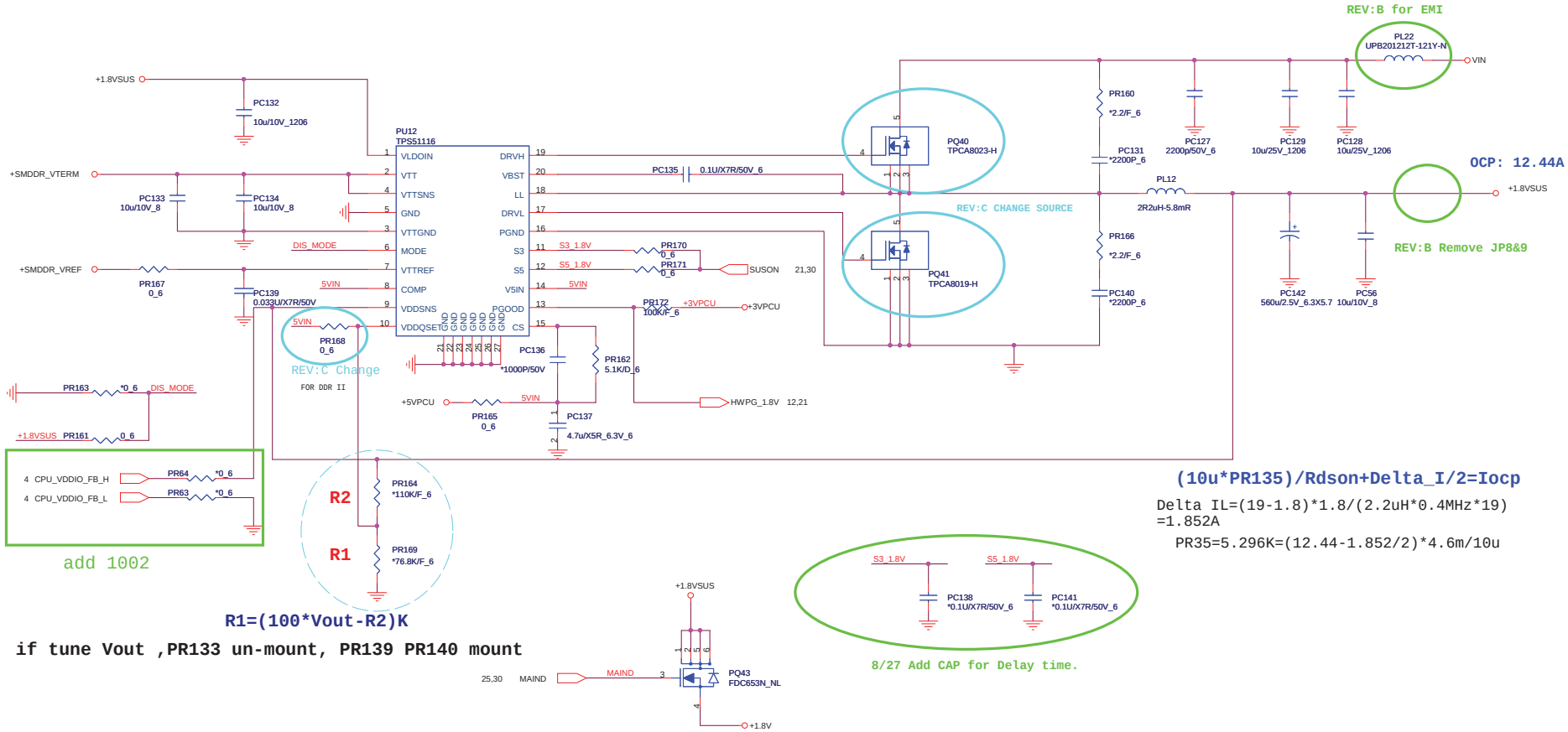


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

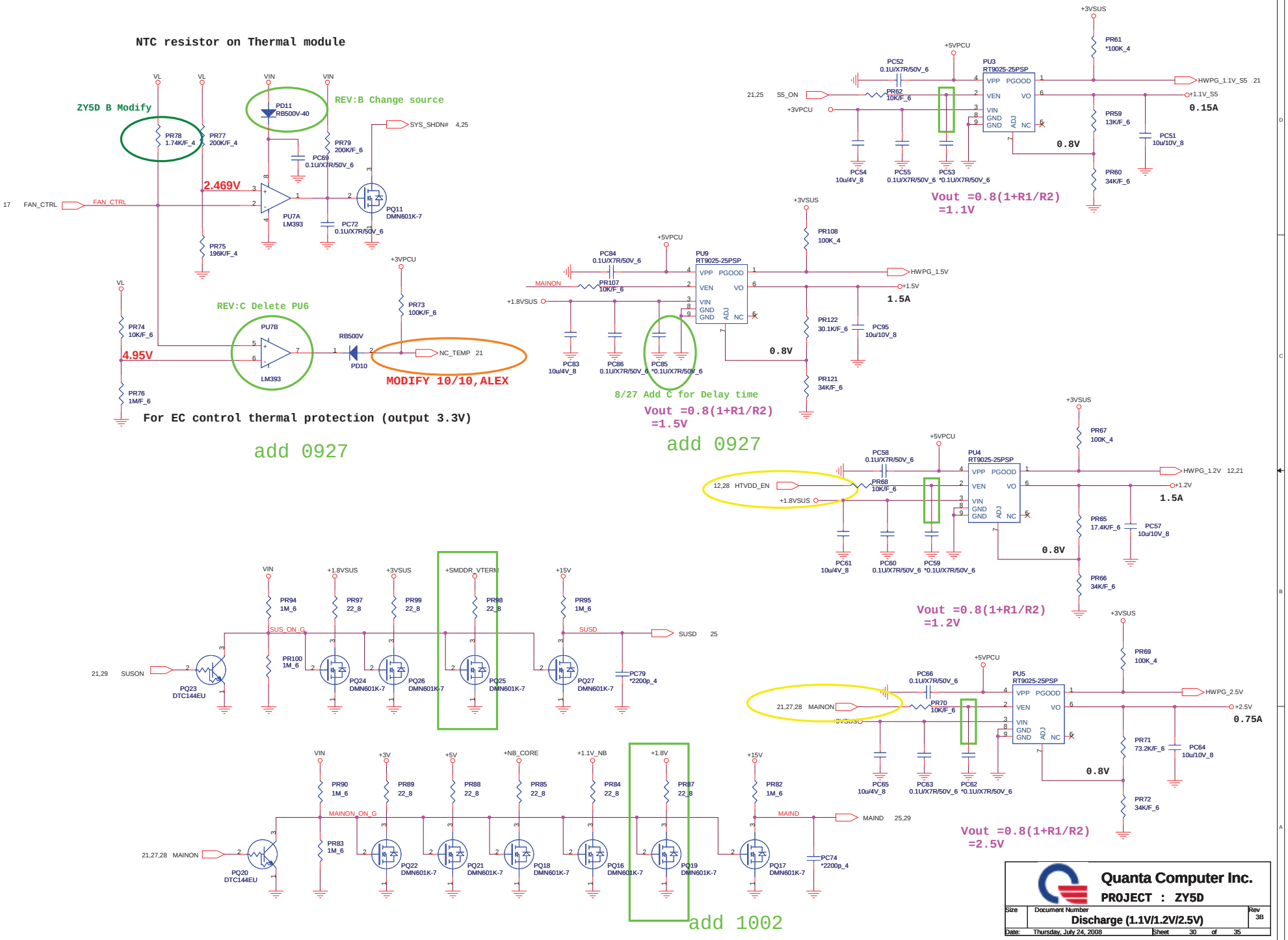
8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm

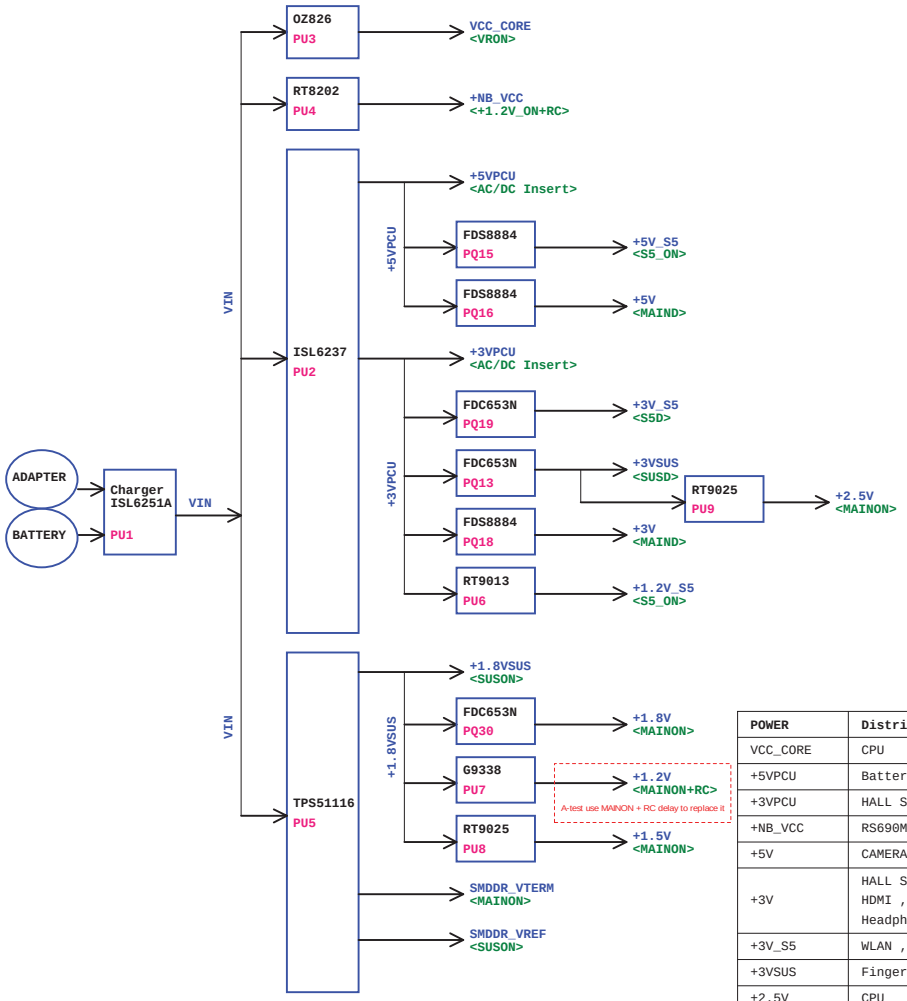
Quanta Computer Inc.		
PROJECT : ZY5D		
Size	Document Number: NB_VCC (RT8202)	Rev: 3B
Date: Wednesday, May 21, 2008	Sheet 28 of 35	



Quanta Computer Inc.
PROJECT : ZY5D

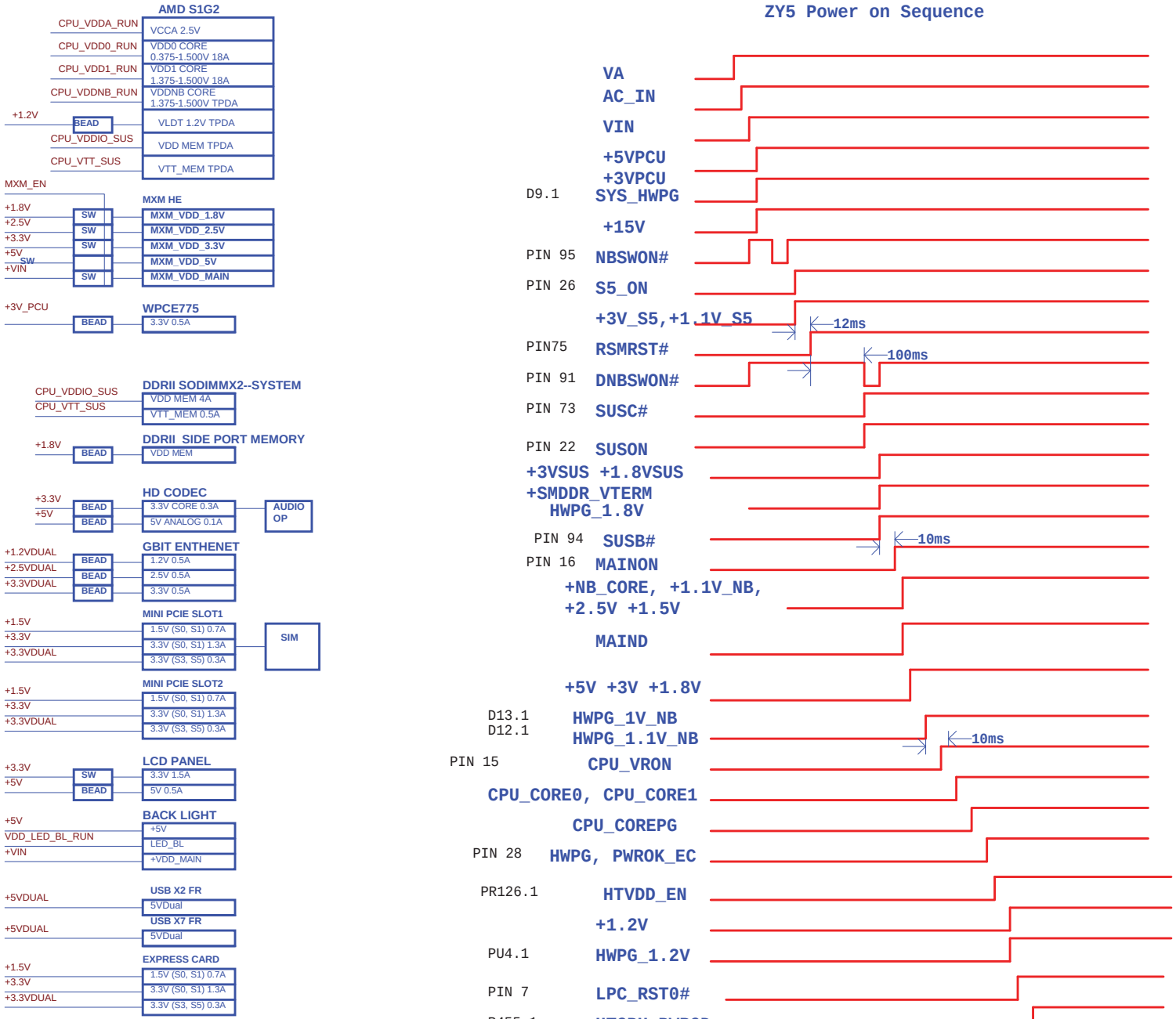
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	3B
Date: Wednesday, May 21, 2008	Sheet 29 of 35	





POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

Quanta Computer Inc.
PROJECT : ZY5D
Power Tree



Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
POWER SEQUENCE CHART
Rev 3B
Date: Wednesday, May 21, 2008
Sheet 32 of 35