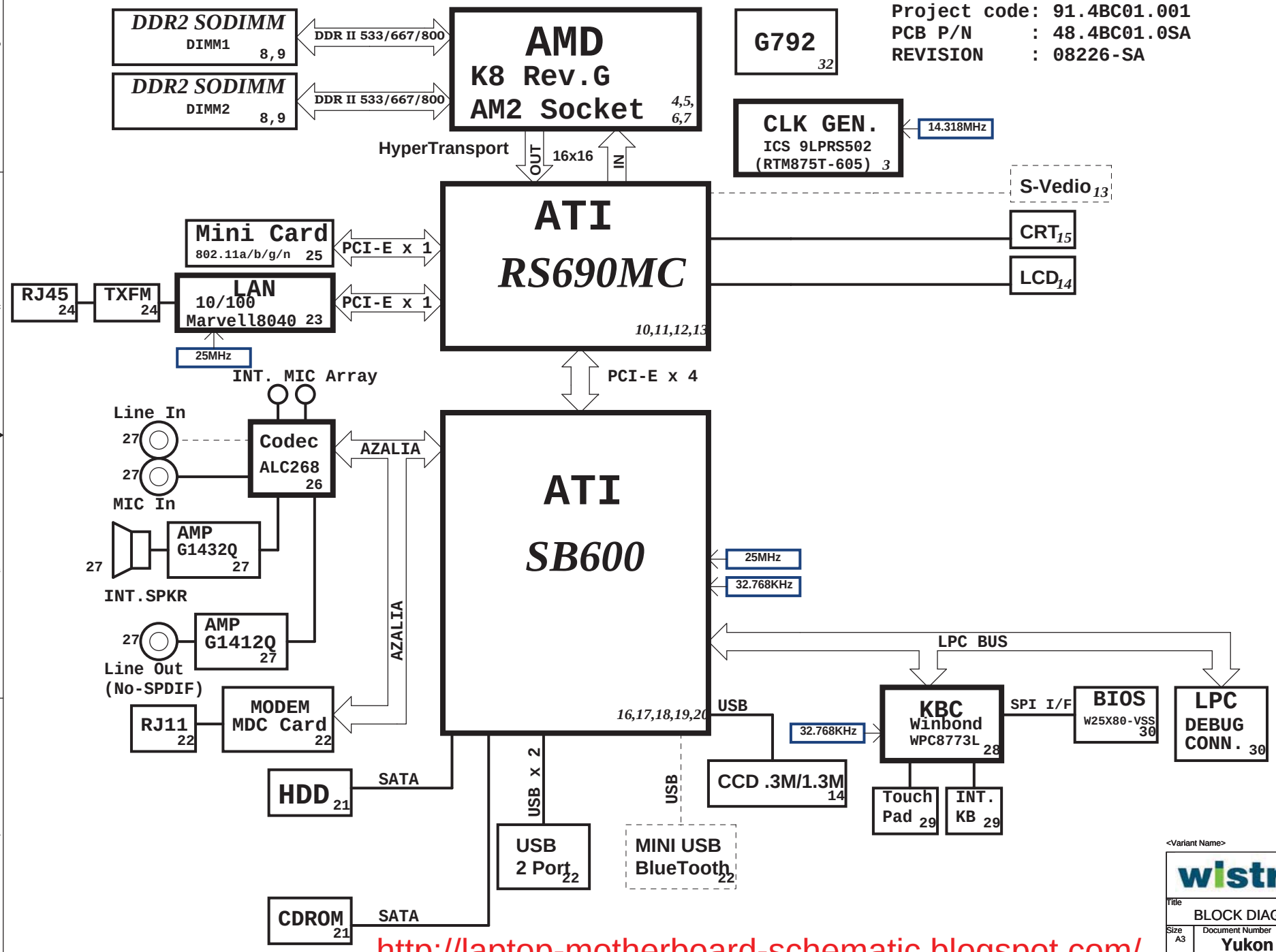
Yukon Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 1 of 43

<Core Design>

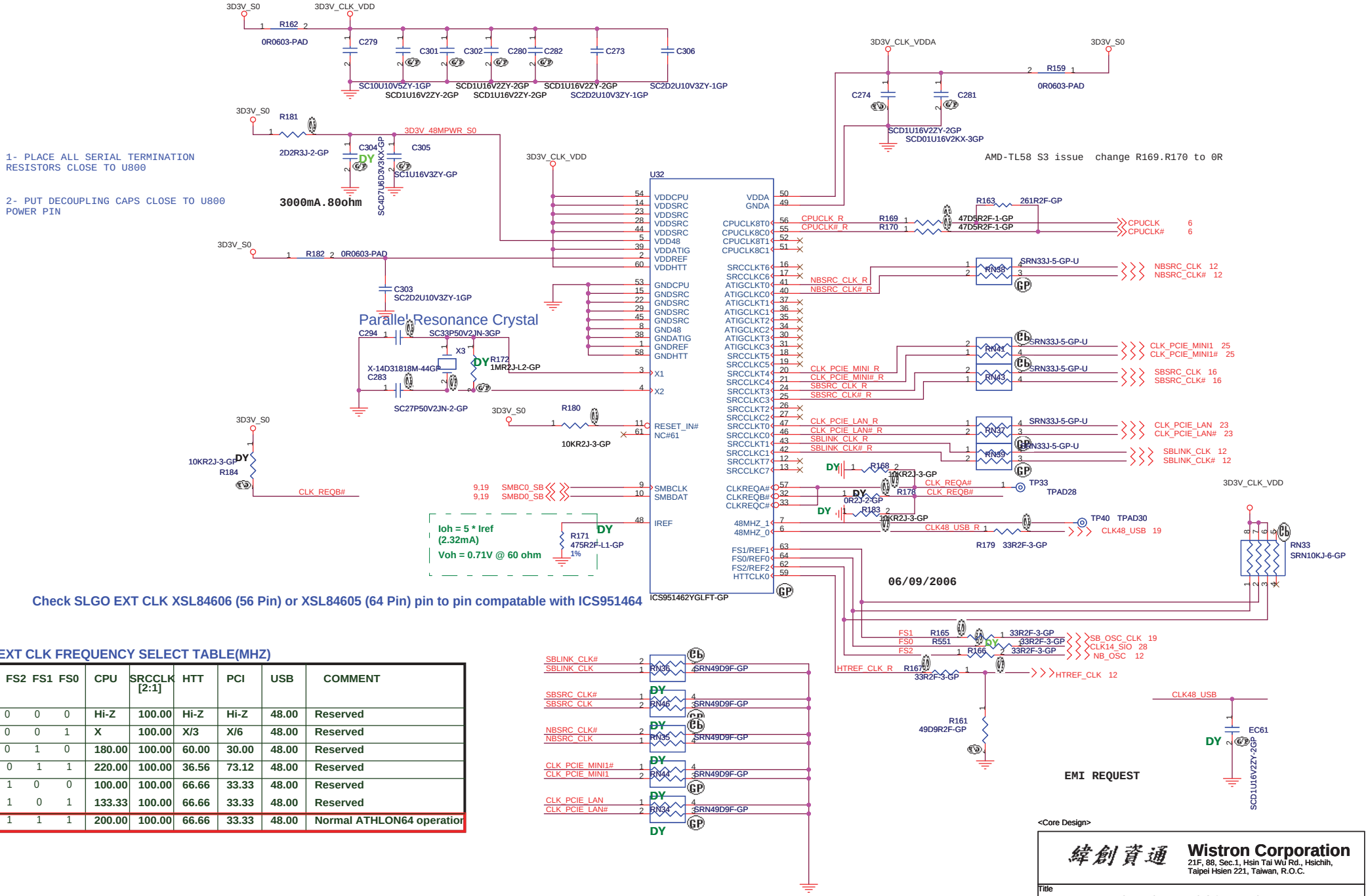
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHANGE HISTORY**

Size	Document Number	Rev
A3	Yukon	SA

Date: Thursday, July 03, 2008 Sheet 2 of 43



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

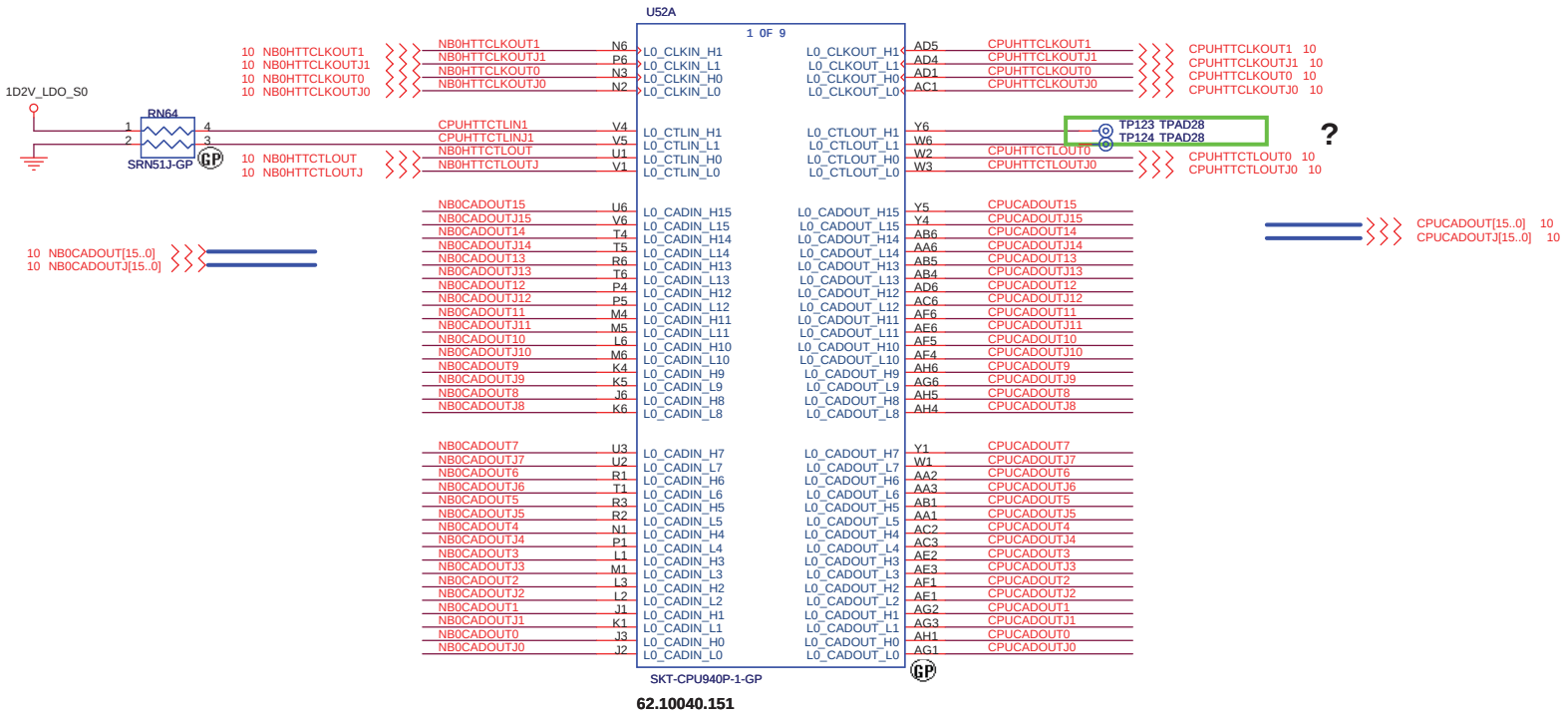
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

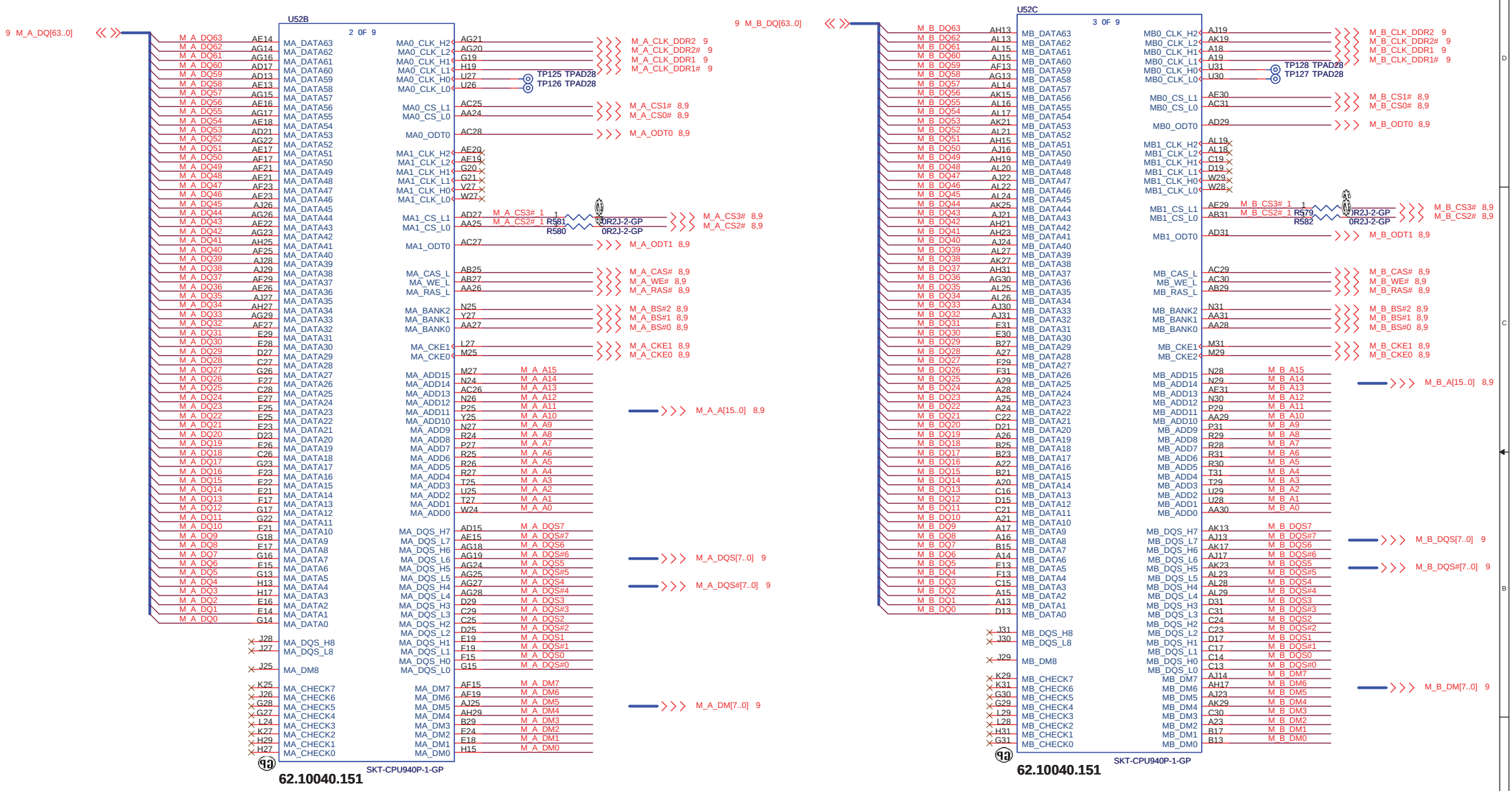
Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 3 of 43



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU(1/4)_HyperTransport I/F*		
Size: A3	Document Number: Yukon	Rev: SA
Date: Thursday, July 03, 2008	Sheet 4 of 43	



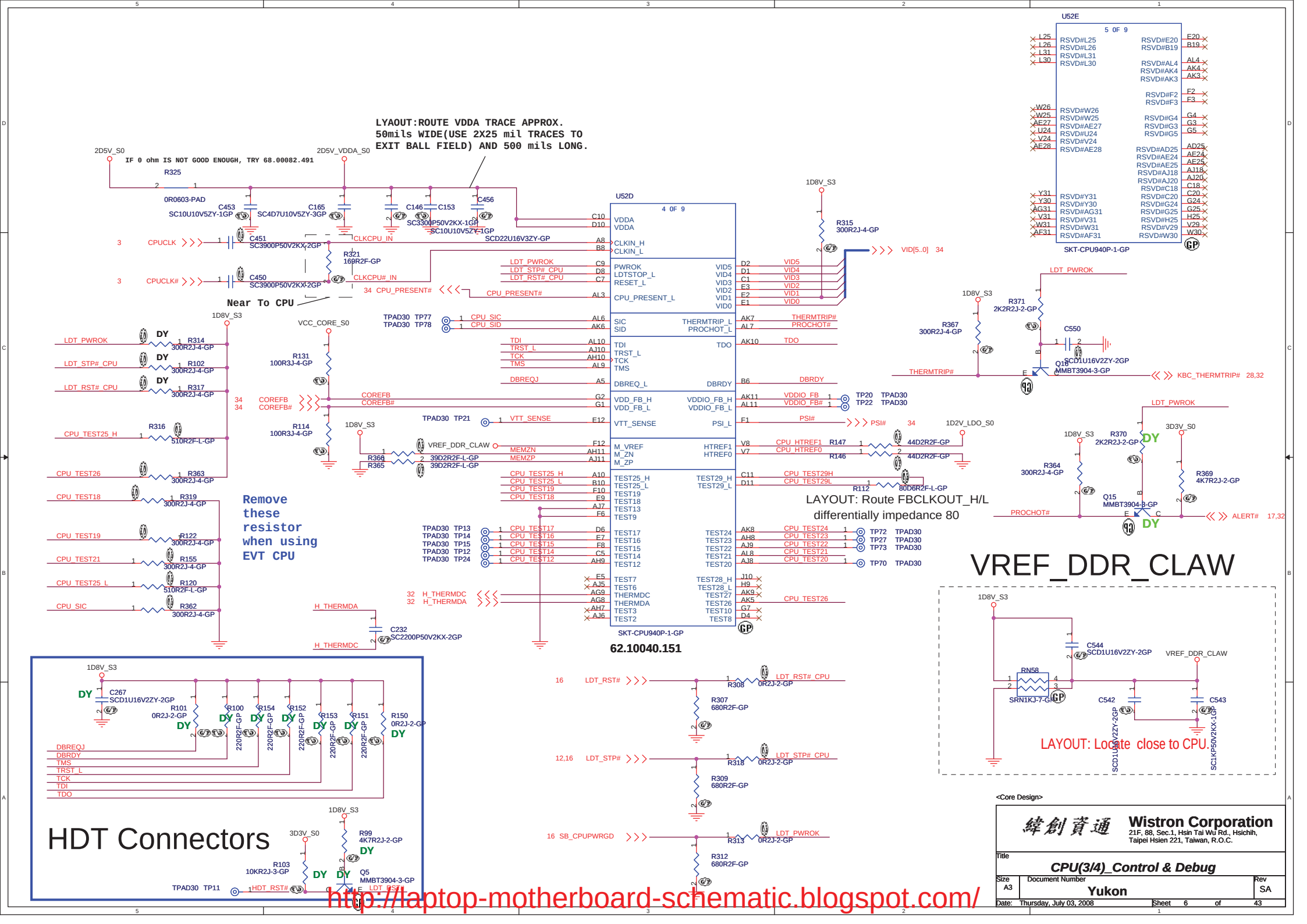
<Core Design>

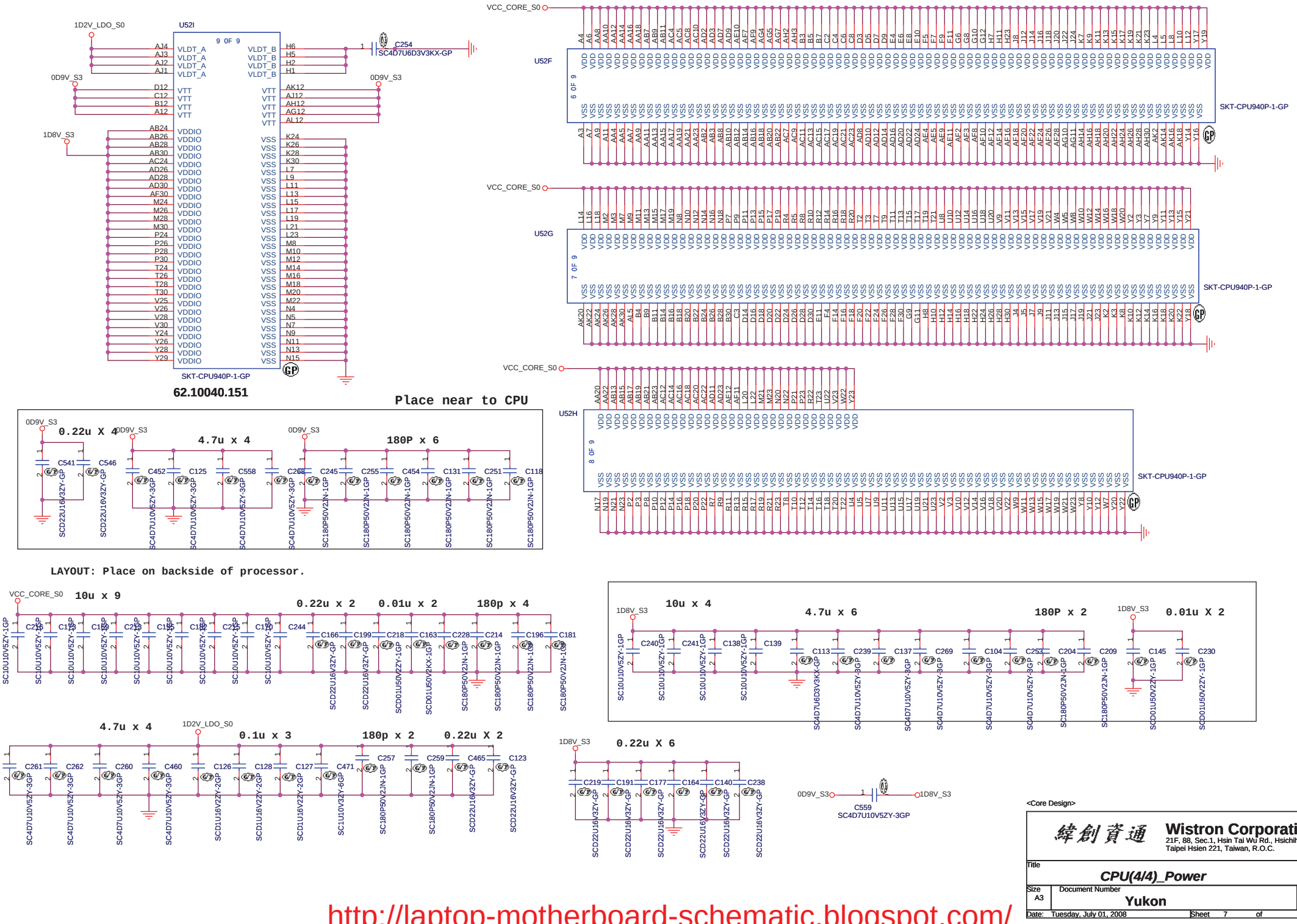
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 5 of 43


LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
Near To CPU
Remove these resistor when using EVT CPU
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80
62.10040.151
VREF_DDR_CLAW
LAYOUT: Locate close to CPU
HDT Connectors
http://laptop-motherboard-schematic.blogspot.com/
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU(3/4)_Control & Debug
Yukon
Thursday, July 03, 2008



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

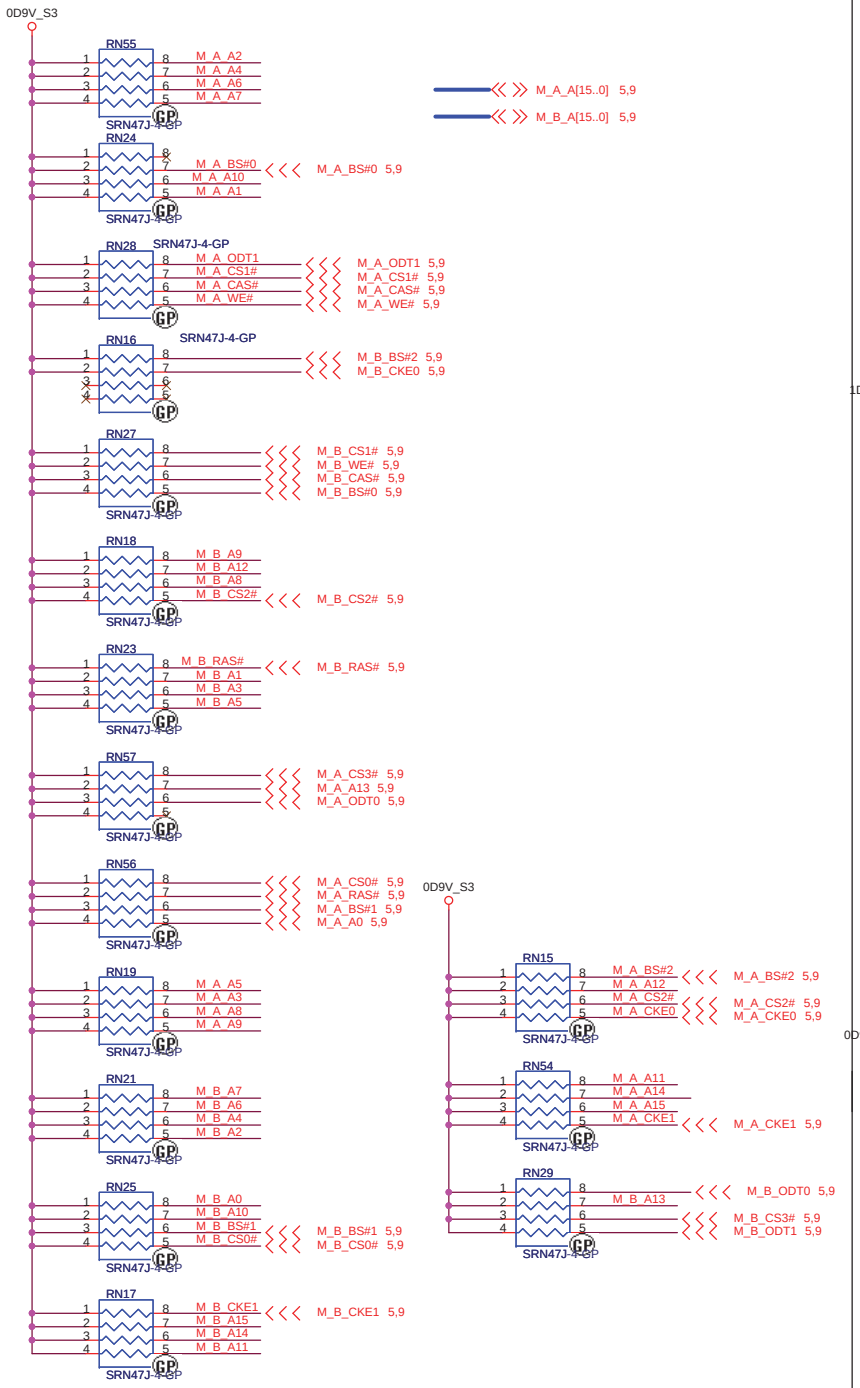
Title: CPU(4/4)_Power

Size: A3 | Document Number: Yukon | Rev: SA

Date: Tuesday, July 01, 2008 | Sheet 7 of 43

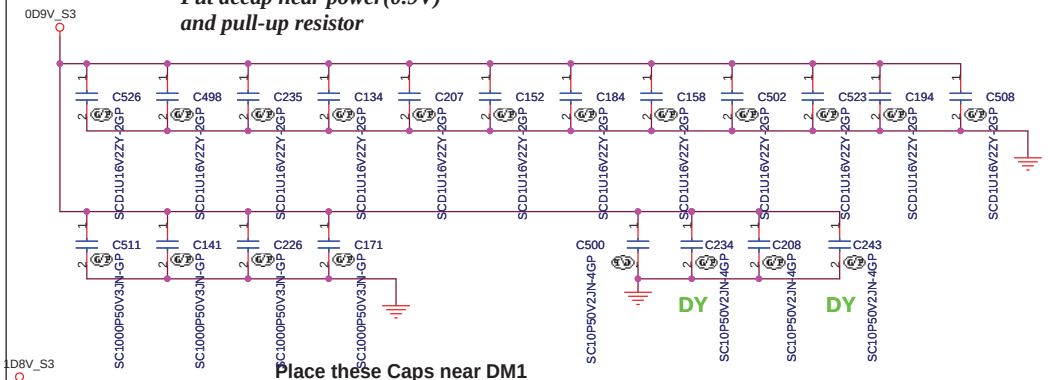
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

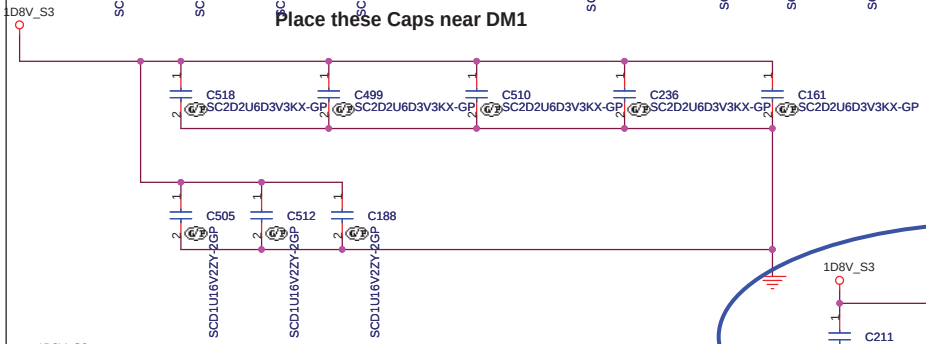


Decoupling Capacitor

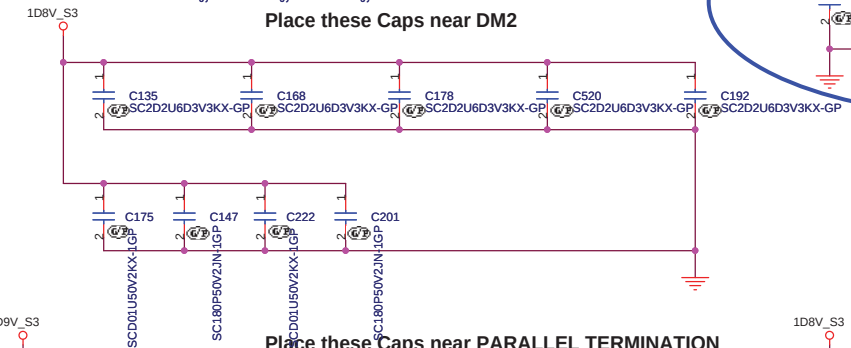
Put decap near power(0.9V) and pull-up resistor

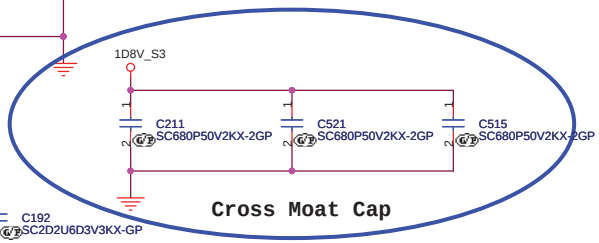


Place these Caps near DM1

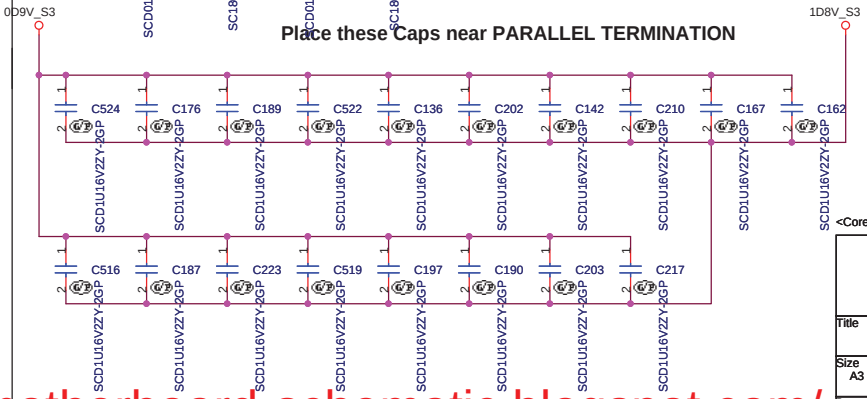


Place these Caps near DM2





Place these Caps near PARALLEL TERMINATION



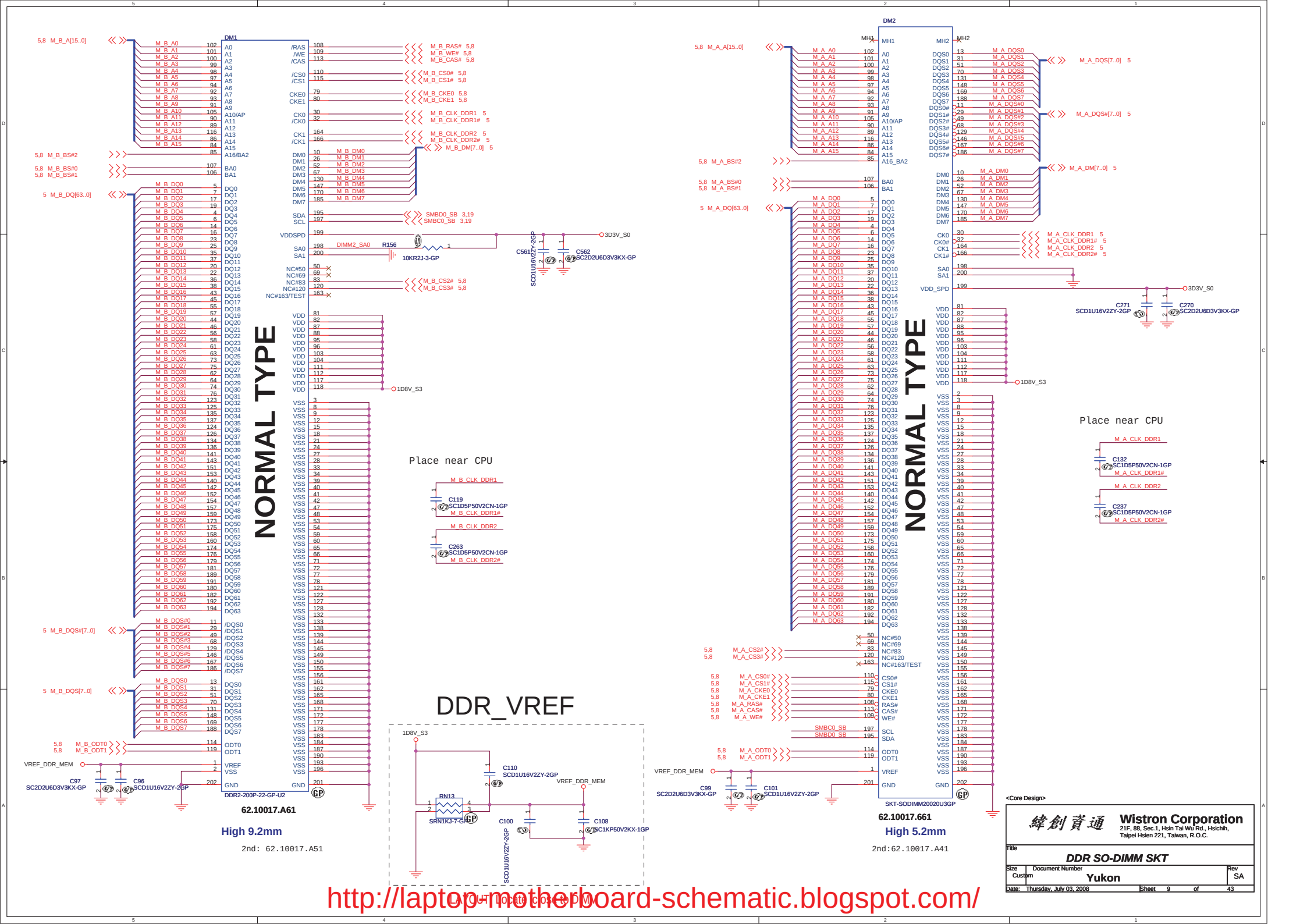
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DAMPING & TERMINATION

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 8 of 43


DM1
NORMAL TYPE
DDR2-200P-22-GP-U2
62.10017.A61
High 9.2mm
2nd: 62.10017.A51
Place near CPU
DDR_VREF
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
2nd:62.10017.A41
Place near CPU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR SO-DIMM SKT
Yukon
Thursday, July 03, 2008
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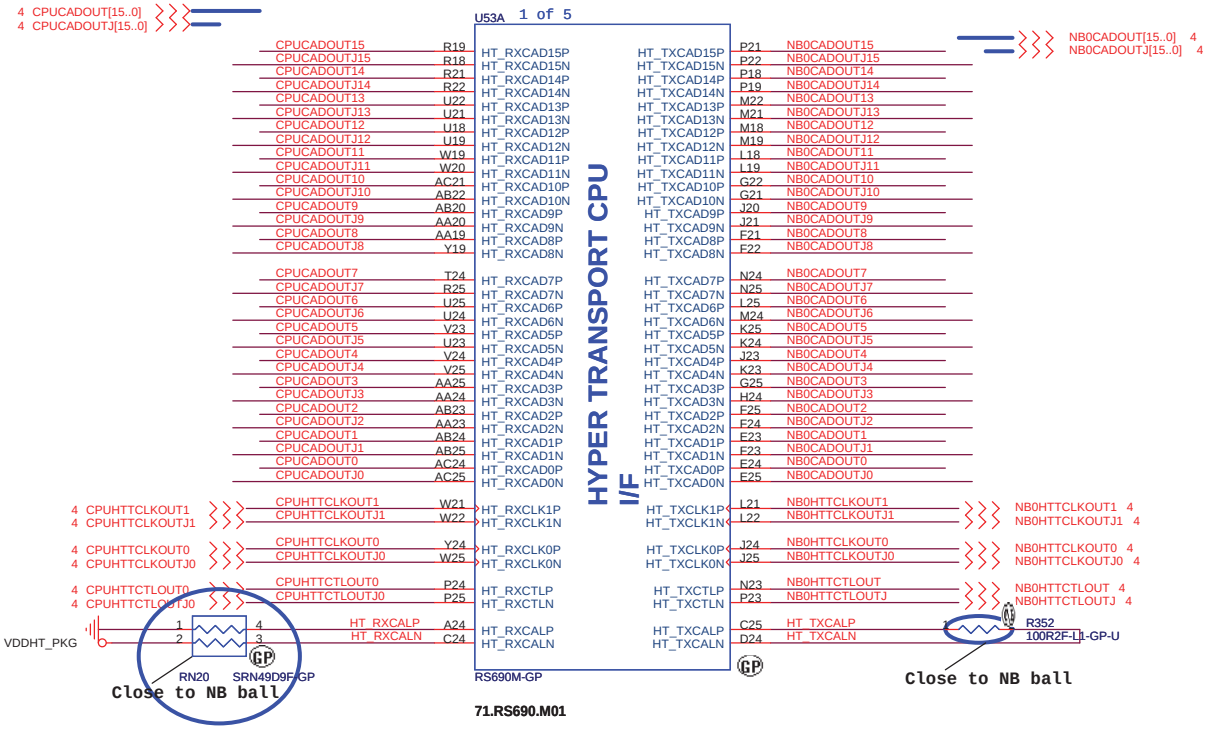
CLAW HAMMER TO NB

NB TO CLAW HAMMER



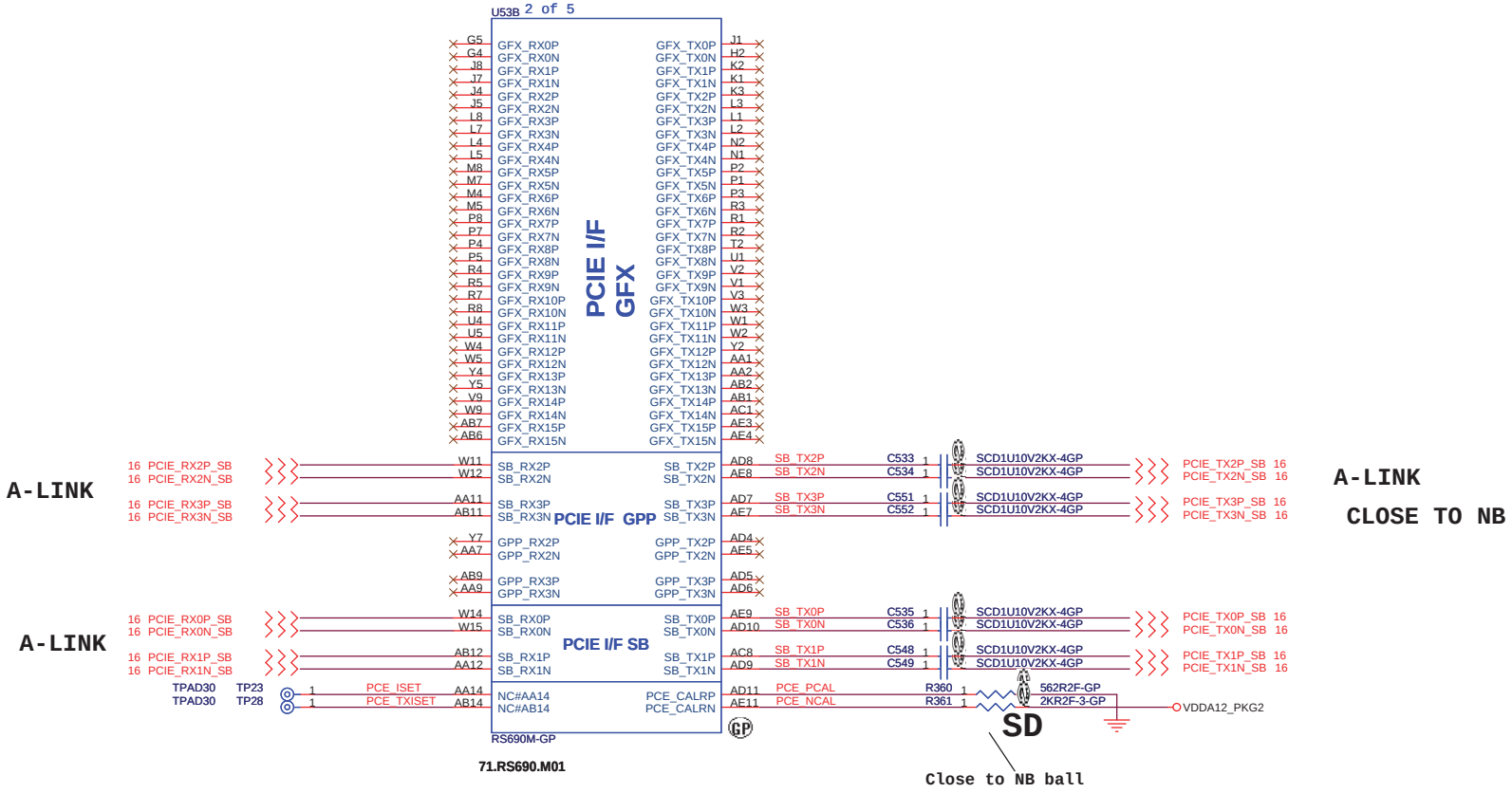
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 10 of 43



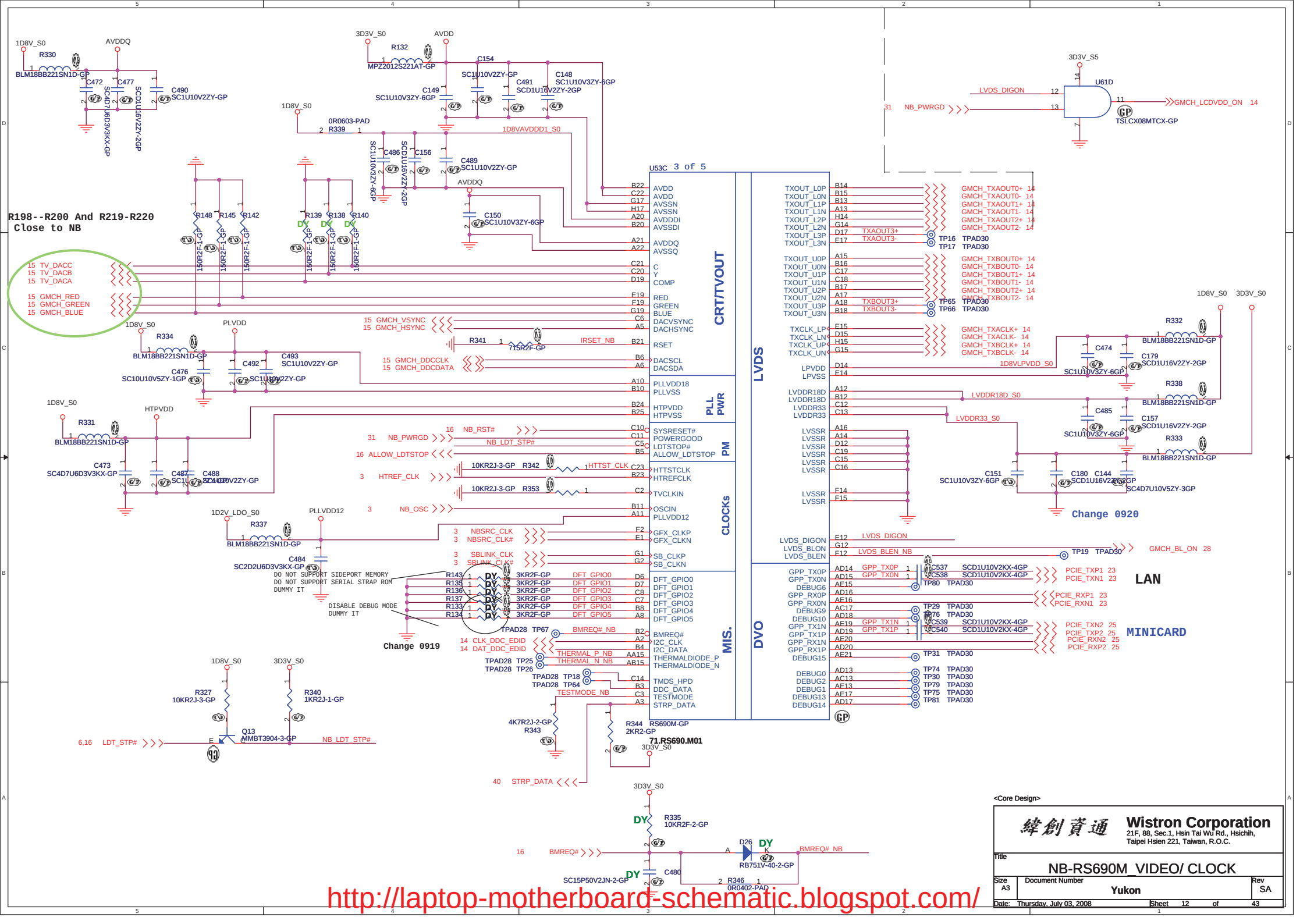
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 11 of 43



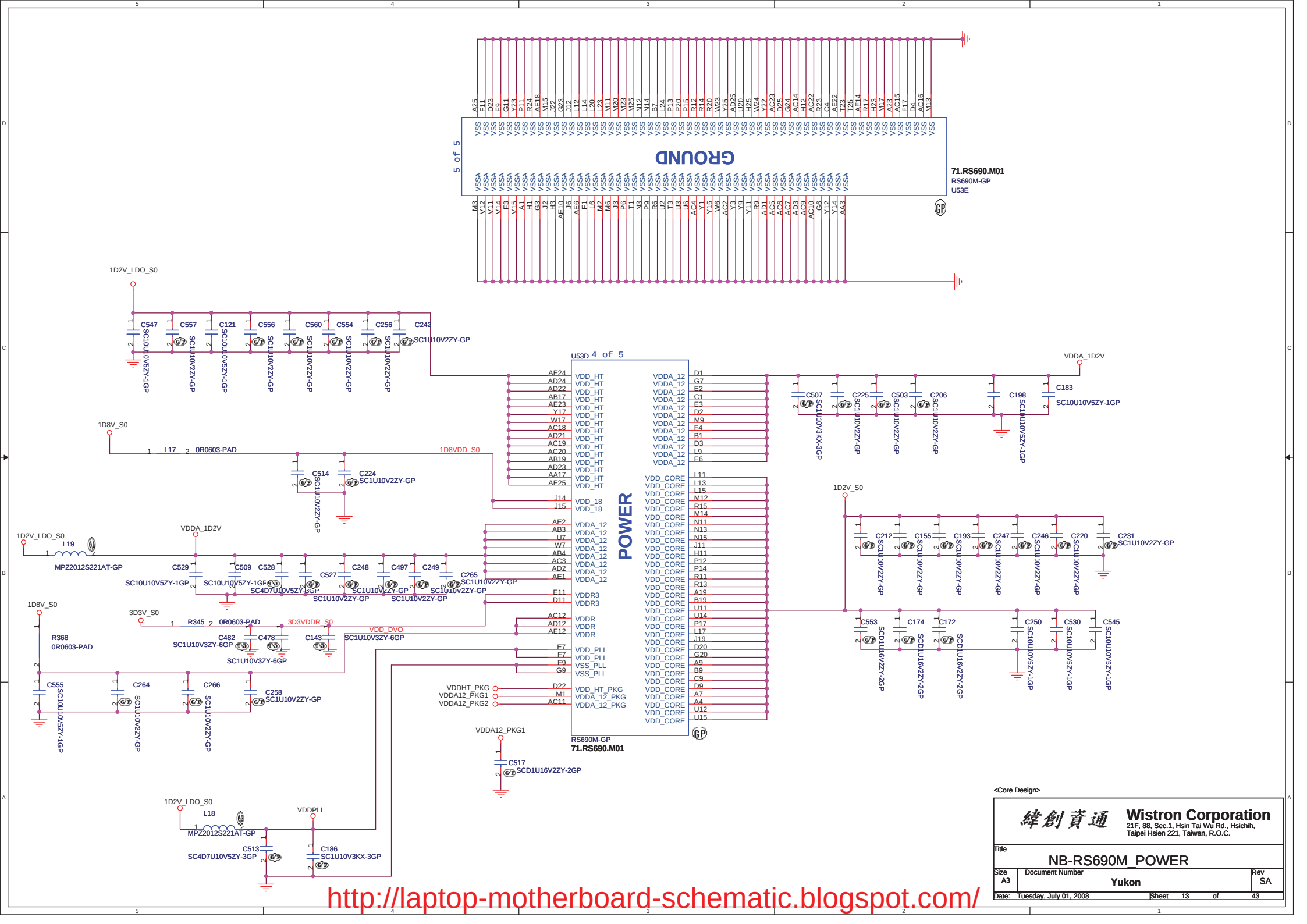
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_VIDEO/ CLOCK

Size	Document Number	Rev
A3	Yukon	SA

Date: Thursday, July 03, 2008 Sheet 12 of 43



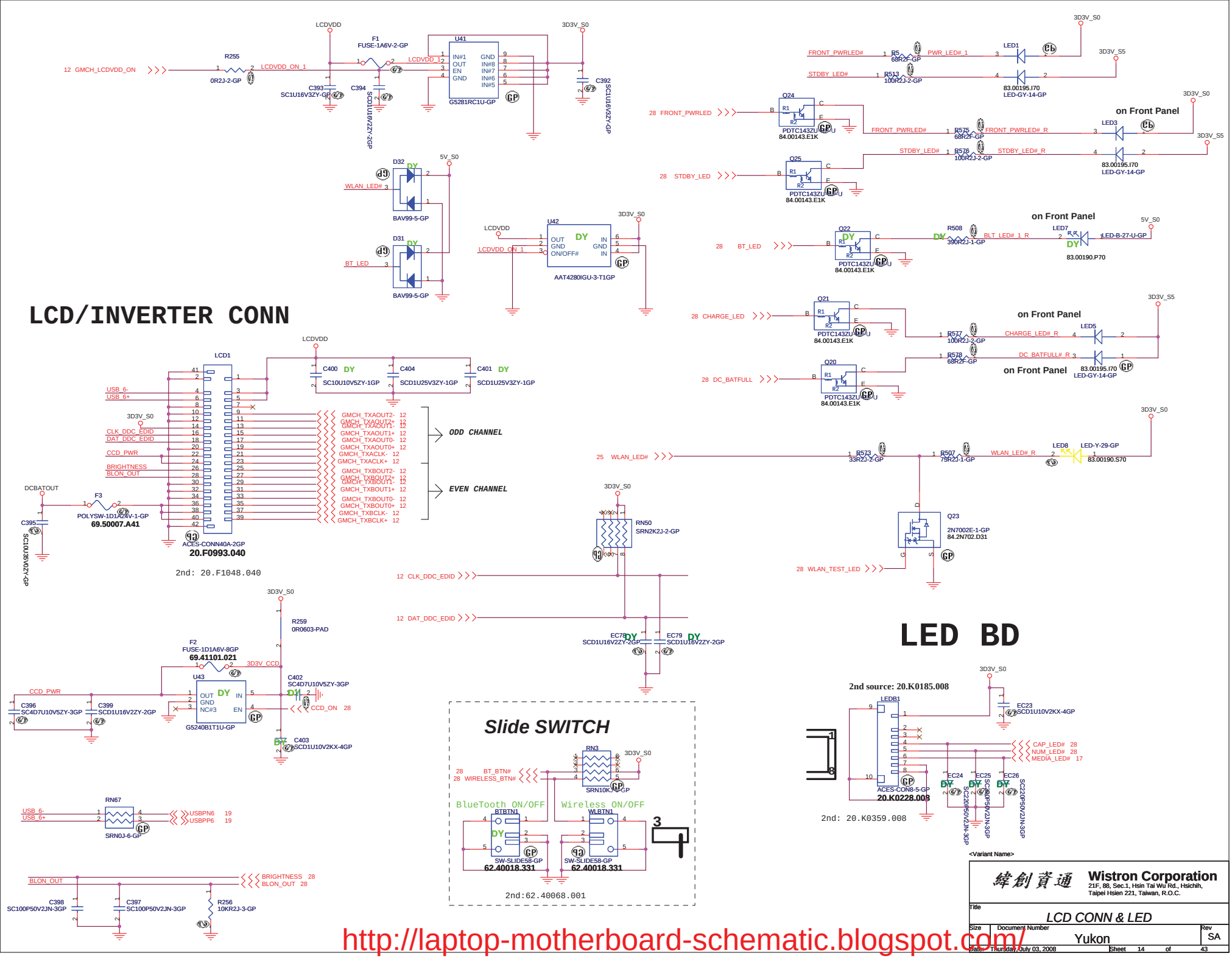
<Core Design>

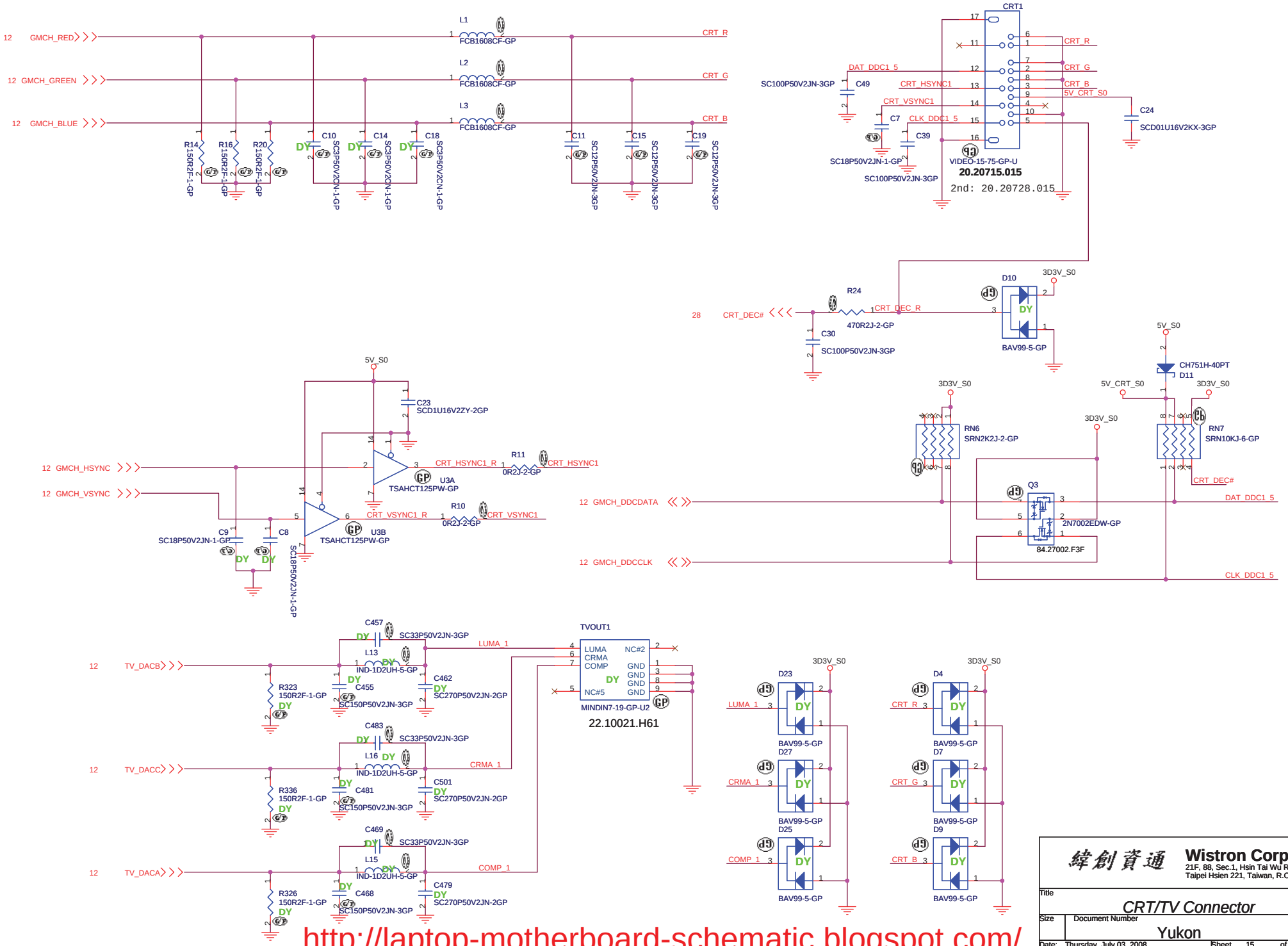
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_POWER

Size: A3 | Document Number: Yukon | Rev: SA

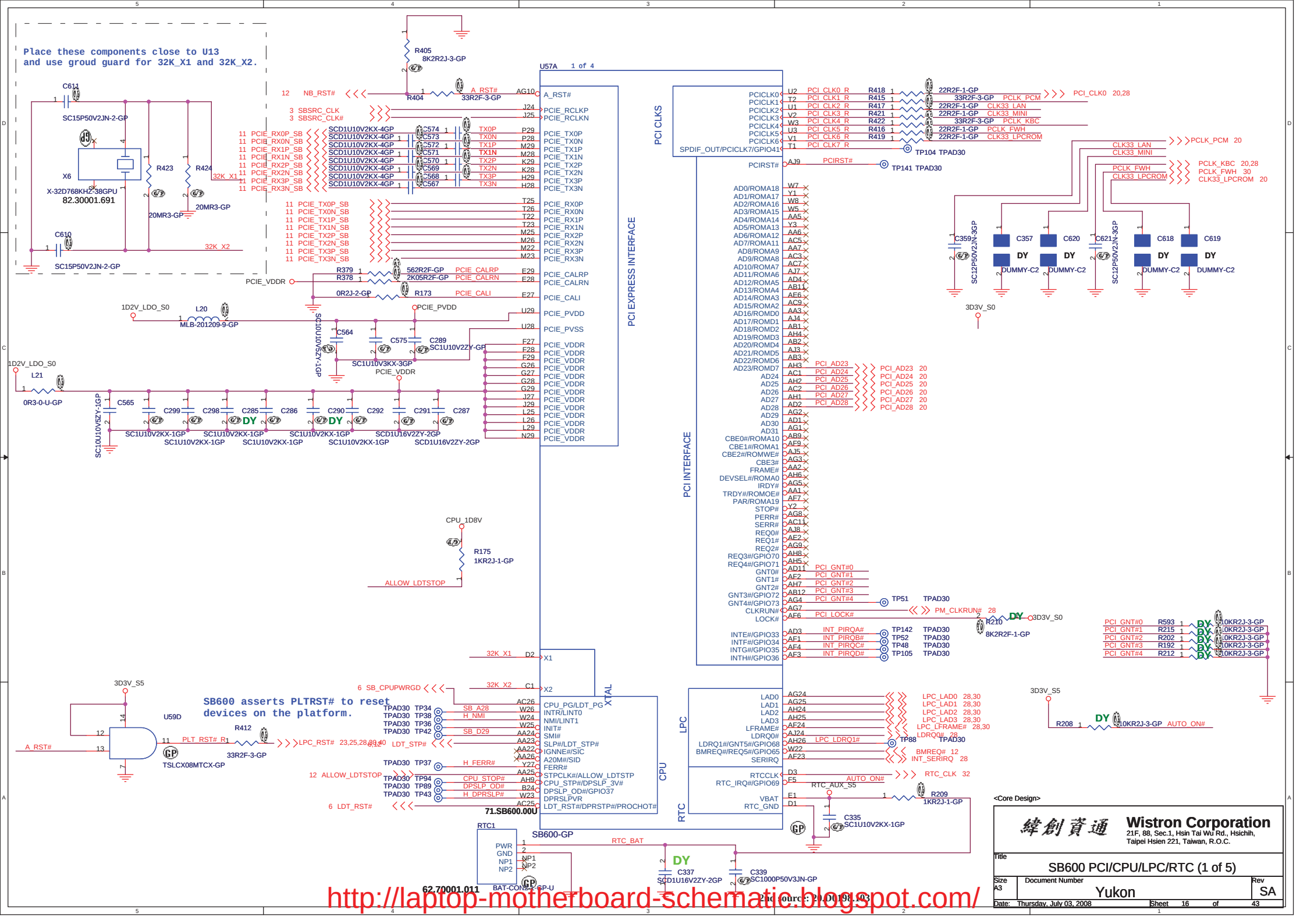
Date: Tuesday, July 01, 2008 | Sheet 13 of 43



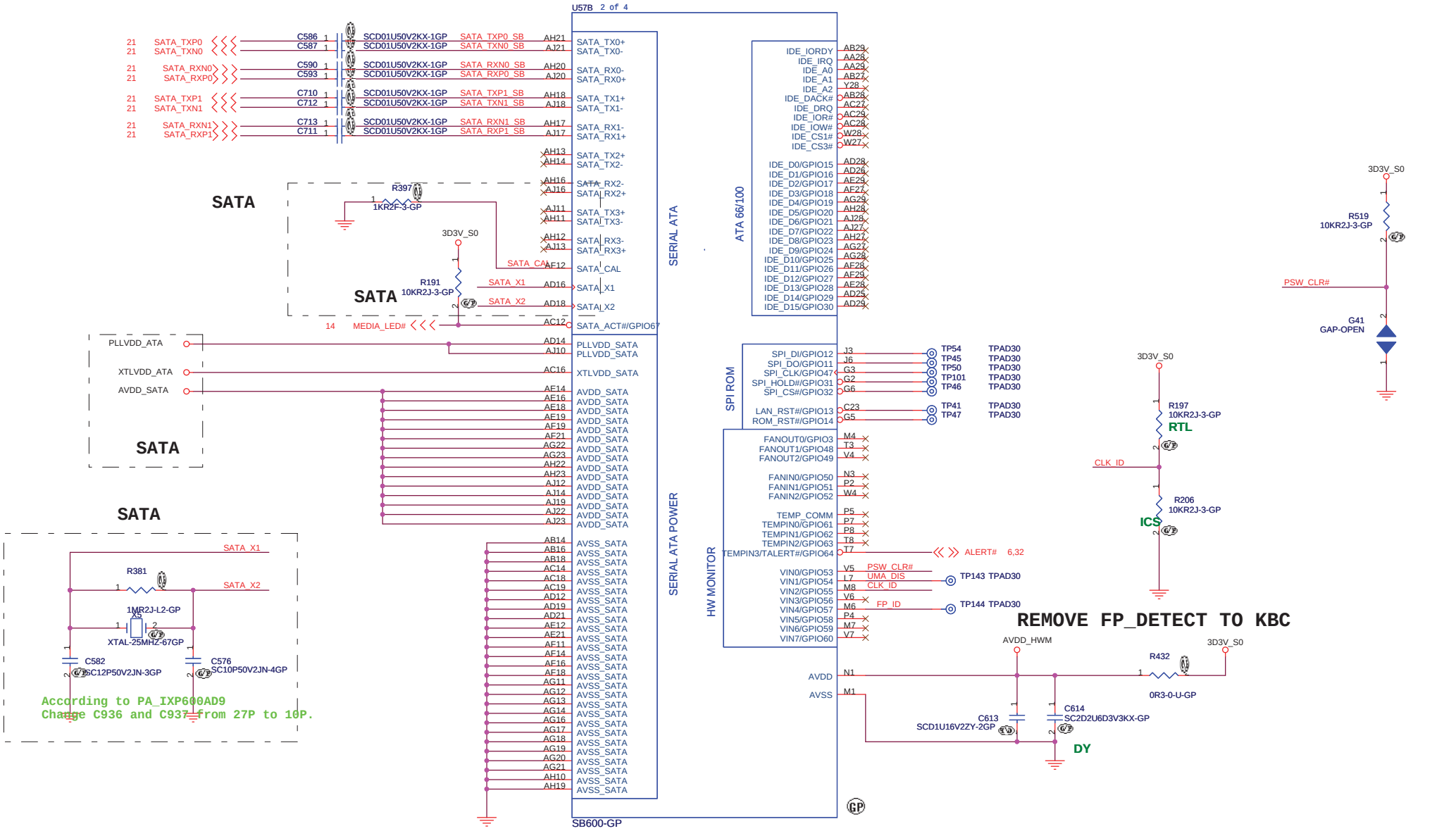


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: Document Number: Yukon
Rev: SA
Date: Thursday, July 03, 2008
Sheet 15 of 43


Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.
SB600 asserts PLTRST# to reset
devices on the platform.
U57A 1 of 4
SB600-GP
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
LPC
CPU
RTC
XTAL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 PCI/CPU/LPC/RTC (1 of 5)
Yukon
Size A3
Rev SA
Date: Thursday, July 03, 2008
Sheet 16 of 43
71.SB600.00U
62.70001.011
2nd source: 20.00198.143
http://laptop-motherboard-schematic.blogspot.com/

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460



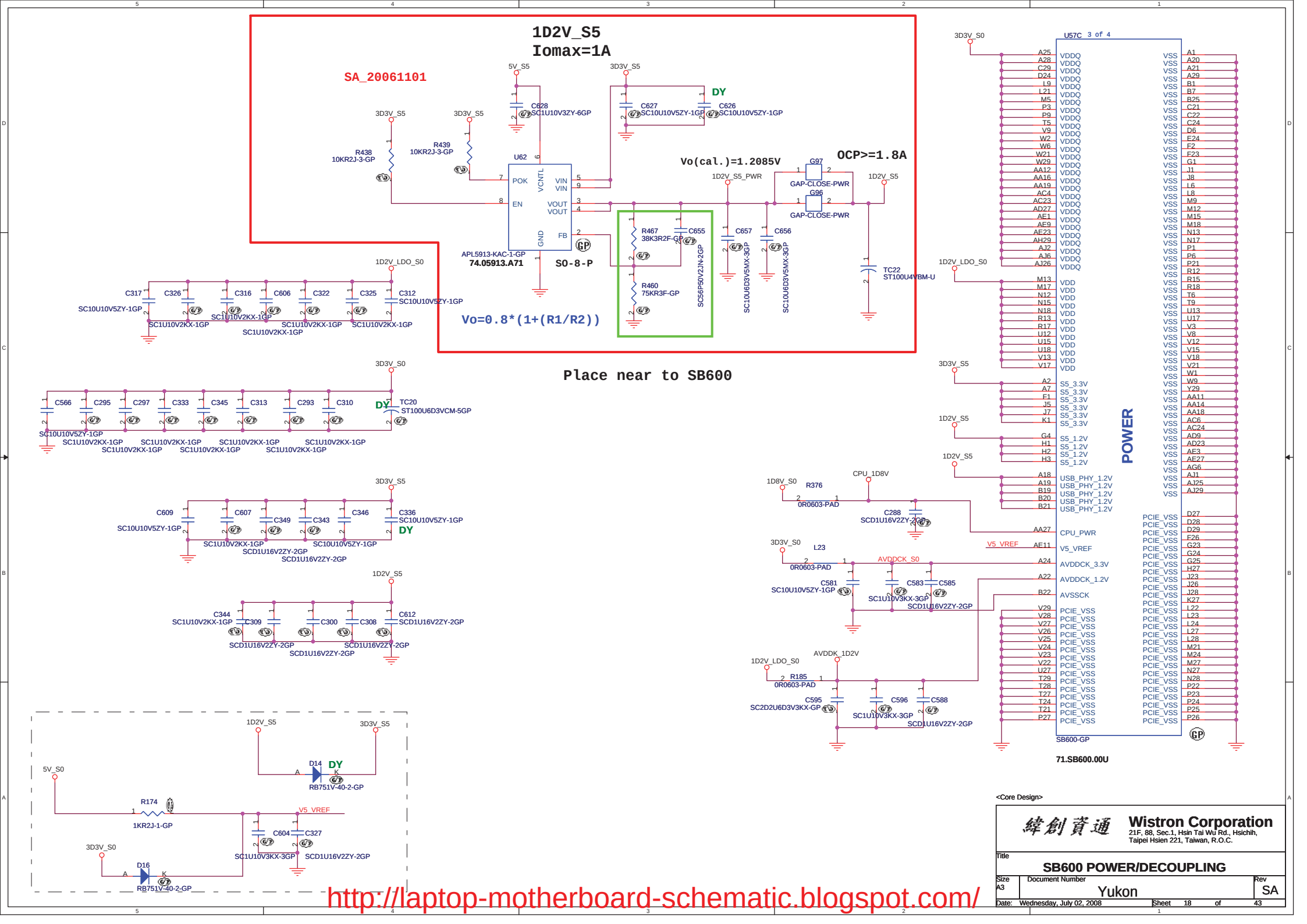
<Core Design>

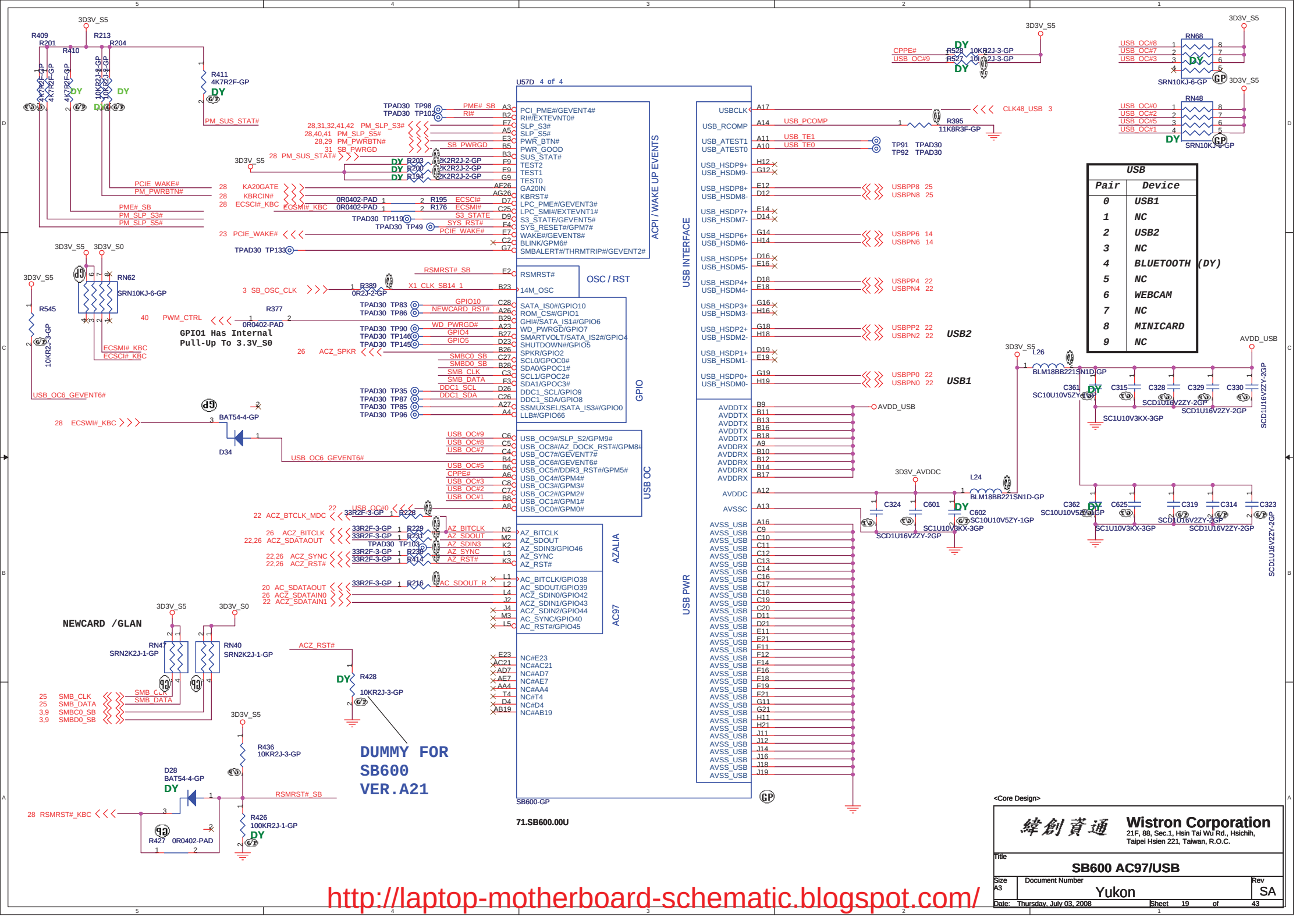
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

Size	Document Number	Rev
A3	Yukon	SA

Date: Thursday, July 03, 2008 Sheet 17 of 43


1D2V_S5
Iomax=1A
SA_20061101
Vo(cal.)=1.2085V
OCP>=1.8A
Vo=0.8*(1+(R1/R2))
Place near to SB600
APL5913-KAC-1-GP
74.05913.A71
SO-8-P
U62
U57C 3 of 4
POWER
SB600-GP
71.SB600.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 POWER/DECOUPLING
Yukon
Wednesday, July 02, 2008
http://laptop-motherboard-schematic.blogspot.com/


USB
Pair Device
0 USB1
1 NC
2 USB2
3 NC
4 BLUETOOTH (DY)
5 NC
6 WEBCAM
7 NC
8 MINICARD
9 NC
USB2
USB1
GPIO1 Has Internal
Pull-Up To 3.3V_S0
NEWCARD /GLAN
DUMMY FOR
SB600
VER.A21
SB600-GP
71.SB600.00U
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 AC97/USB
Yukon
Thursday, July 03, 2008
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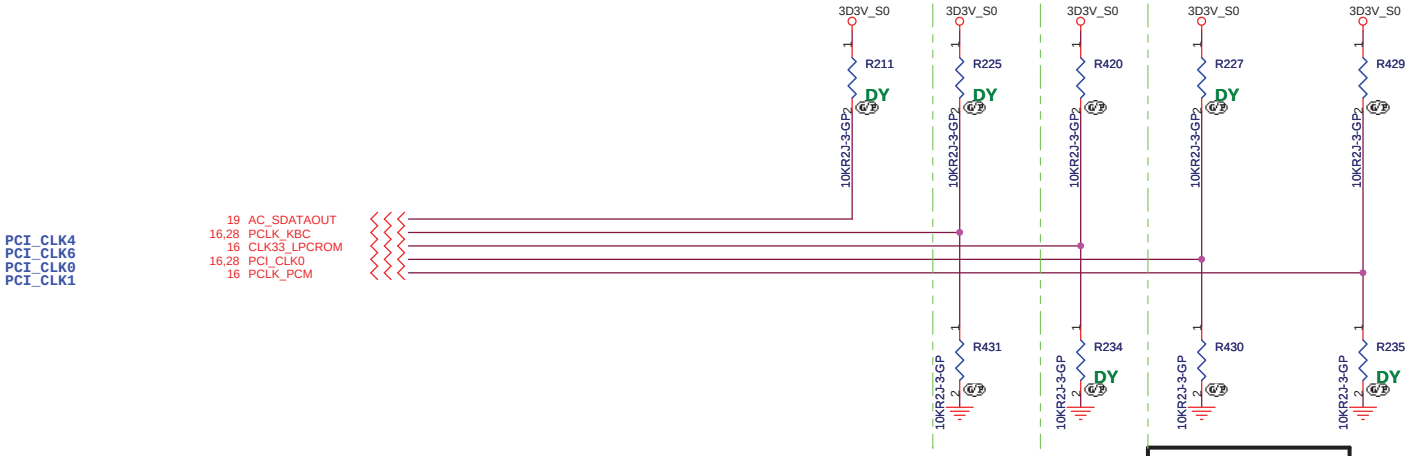
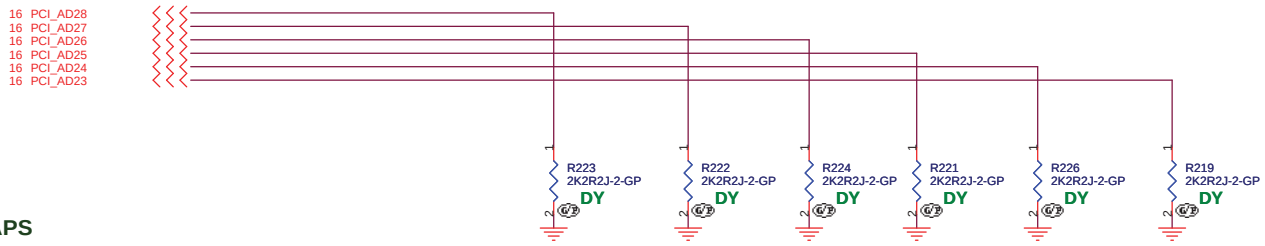
http://laptop-motherboard-schematic.blogspot.com/



REQUIRED SYSTEM STRAPS

				SB600	
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

Size: A3 | Document Number: Yukon | Rev: SA

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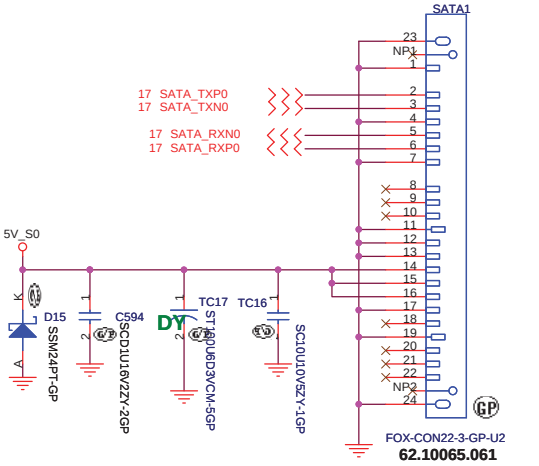
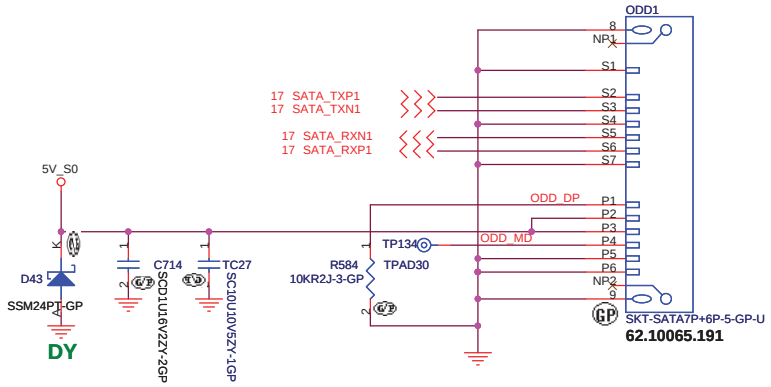
SATA HD Connector



2nd: 62.10065.091

SATA ODD Connector



bom1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD and CDROM

Size	Document Number	Rev
	Yukon	SA

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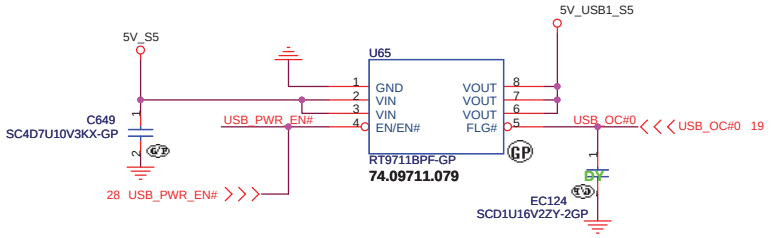
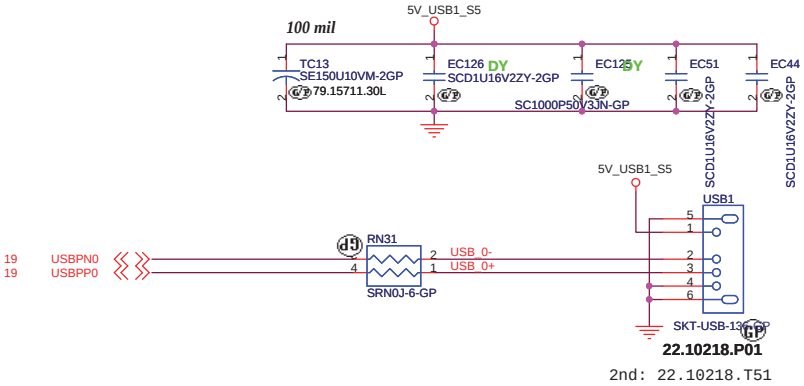
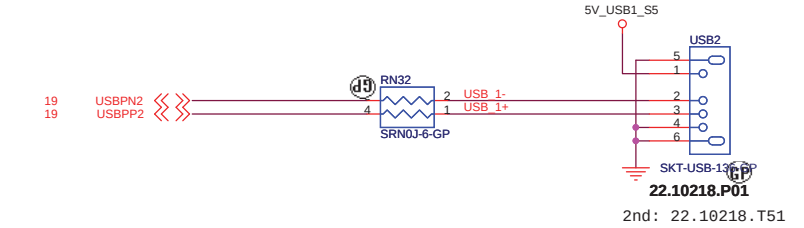
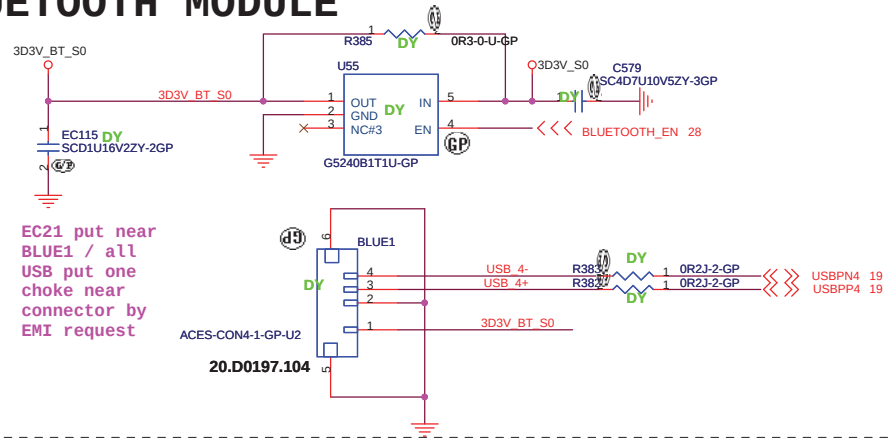


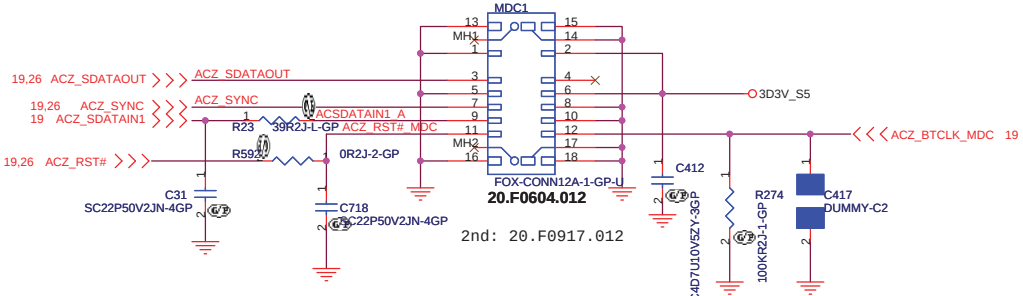


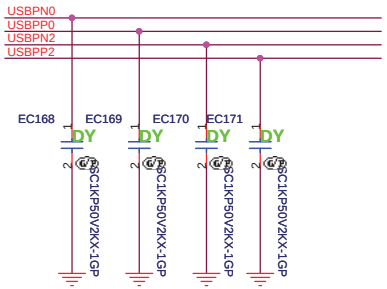


BLUETOOTH MODULE



MDC 1.5 CONN





bom1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size	Document Number	Rev
	Yukon	SA

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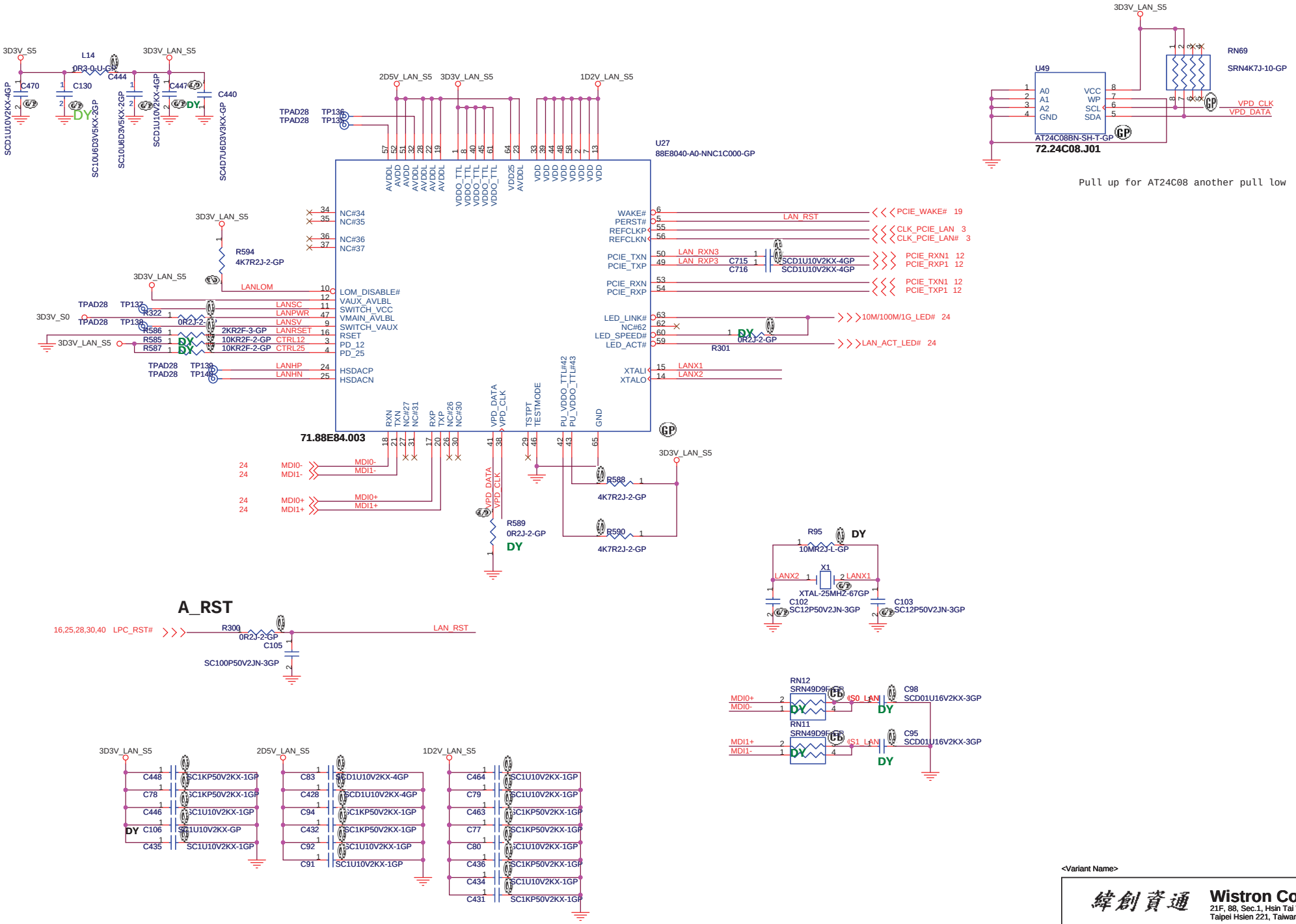
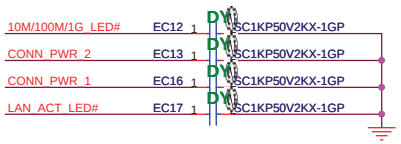
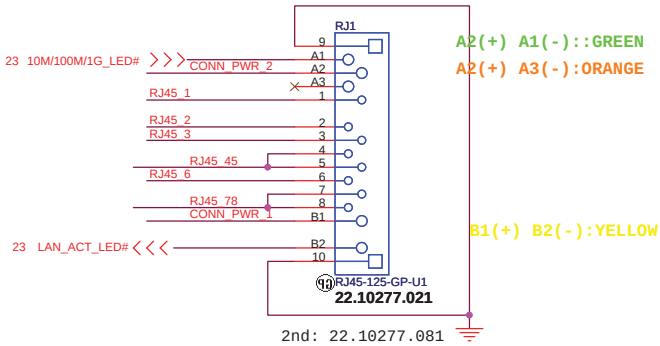
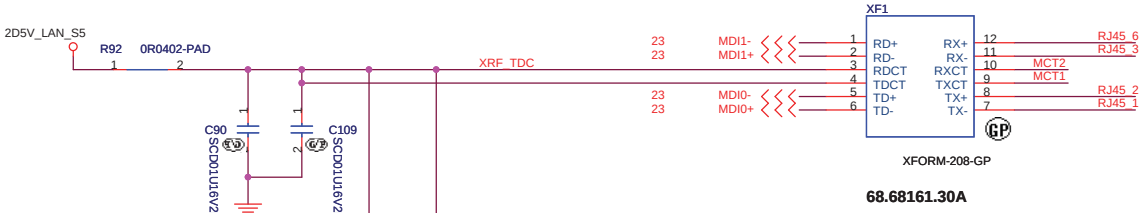


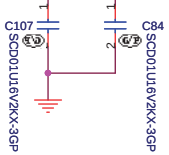
LAN Connector





10/100 Lan Transformer

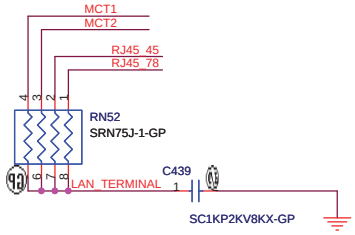


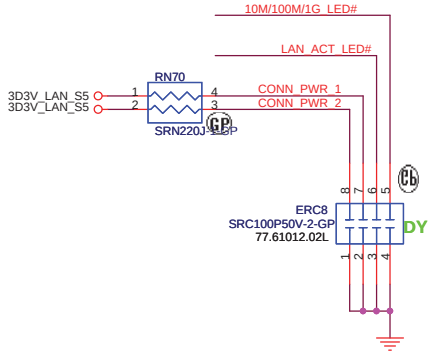


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers





10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

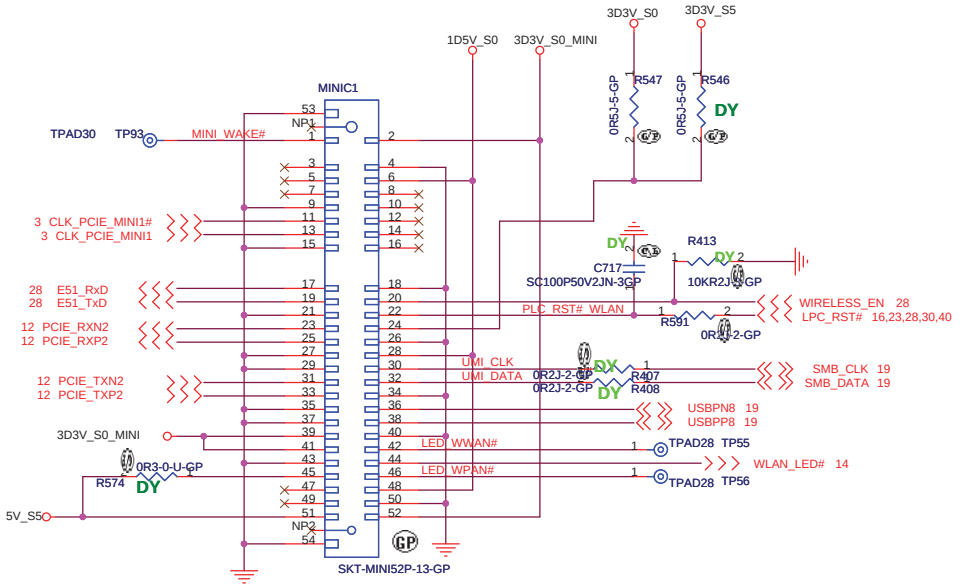
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: Yukon | Rev: SA
Date: Thursday, July 03, 2008 | Sheet 24 of 43

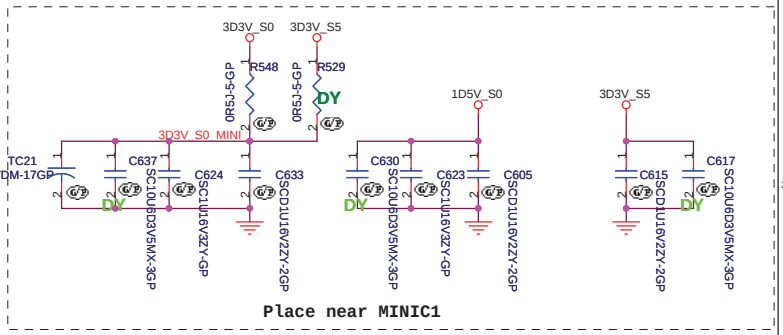
Mini Card Connector

NEWCARD Connector



62.10043.461

2nd:20.F1049.052



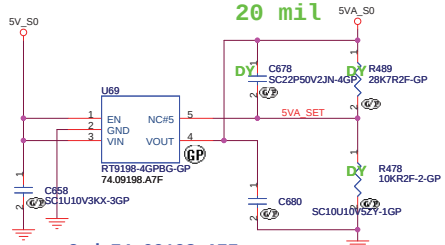
Place near MINIC1

bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size	Document Number **Yukon**	Rev SA
Date: Thursday, July 03, 2008	Sheet 25 of 43	

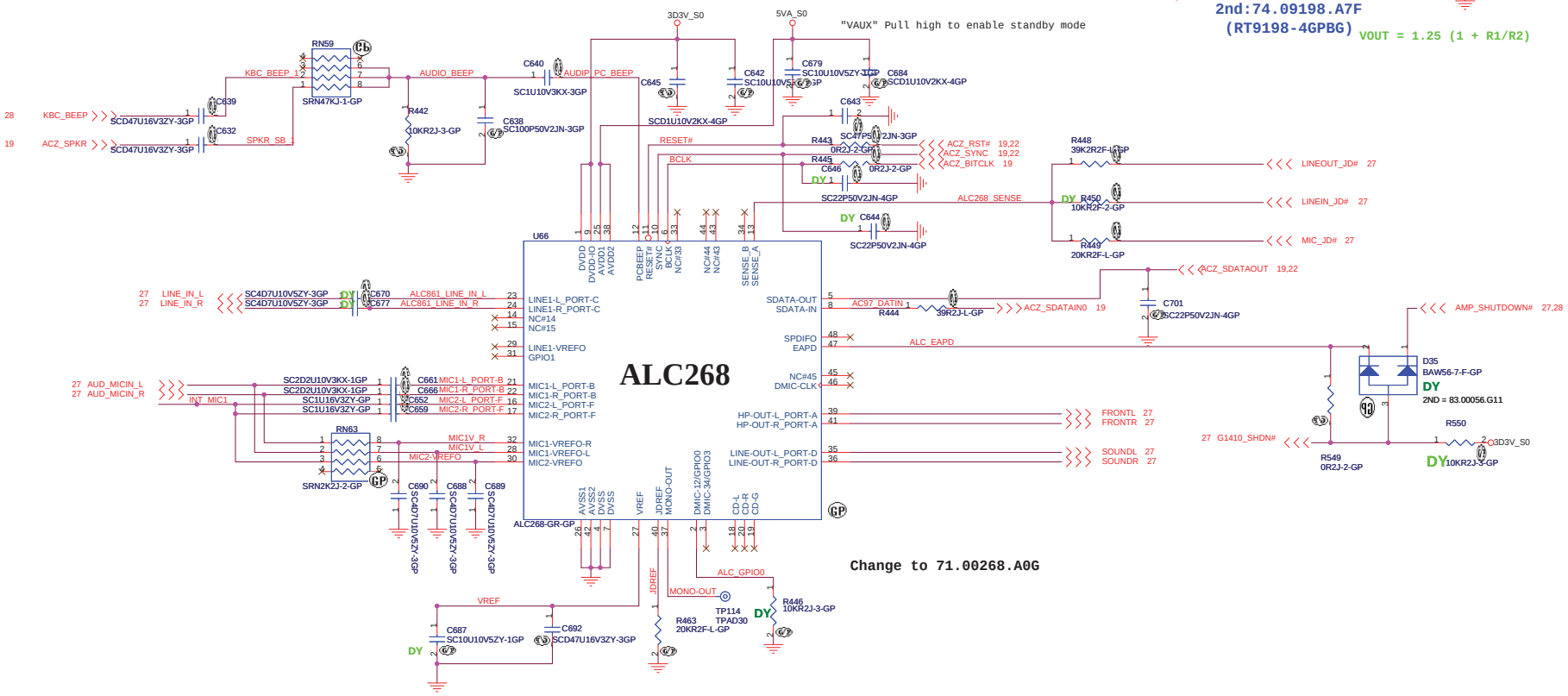
POWER GENERATE

Layout
20 mil



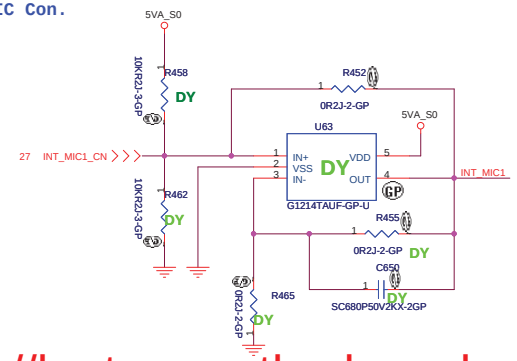
2nd:74.09198.A7F
(RT9198-4GPBG)

VOUT = 1.25 (1 + R1/R2)



Change to 71.00268.A0G

Near INTMIC Con.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

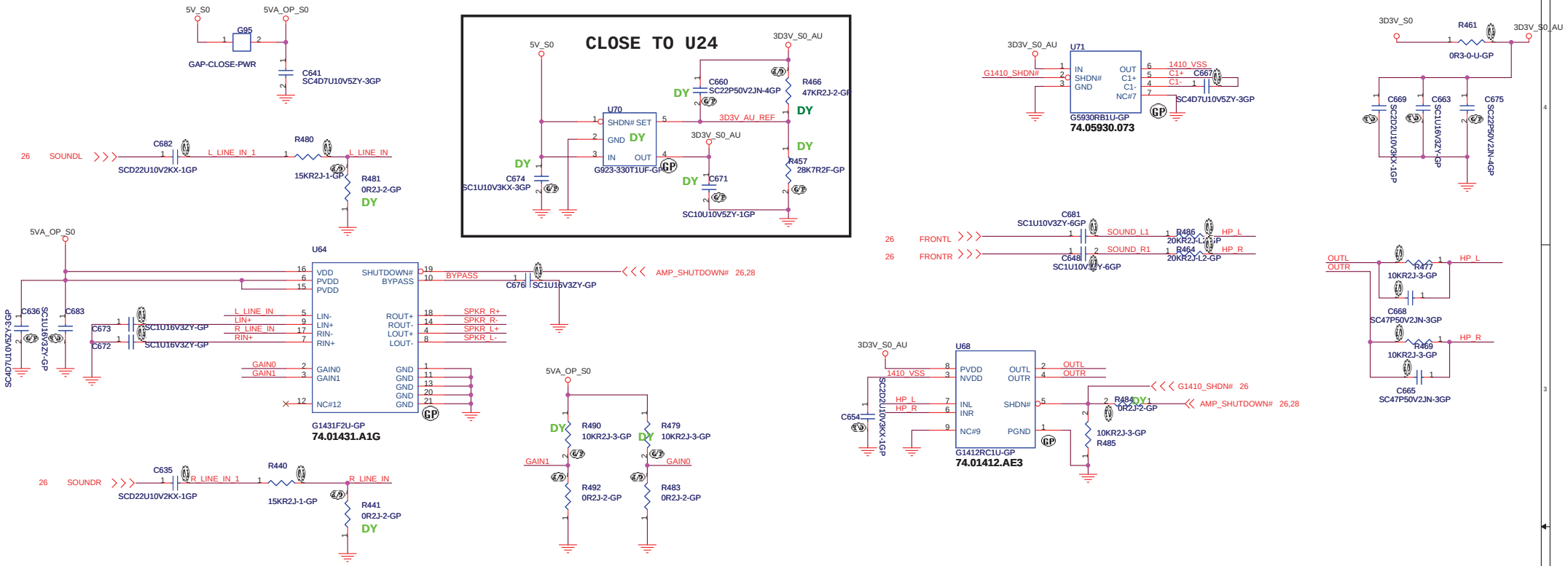
Title: AZALIA CODEC - ALC268

Size | Document Number: Yukon | Rev: SA

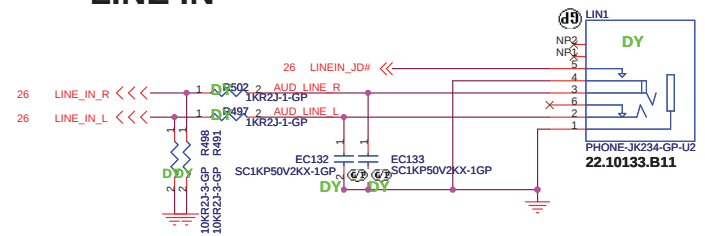
Date: Thursday, July 03, 2008 | Sheet 26 of 43

AUDIO OP AMPLIFIER

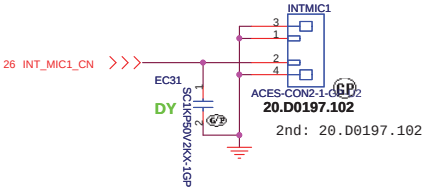
KBC_MUTE_GPIO8



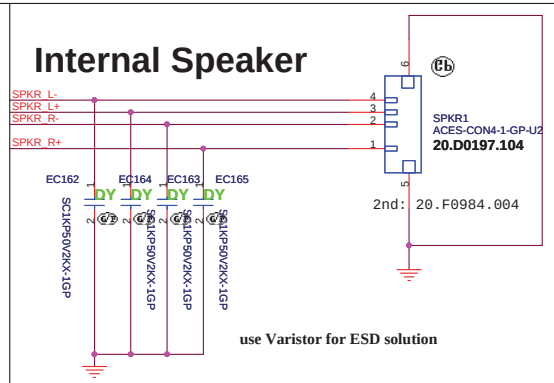
LINE IN



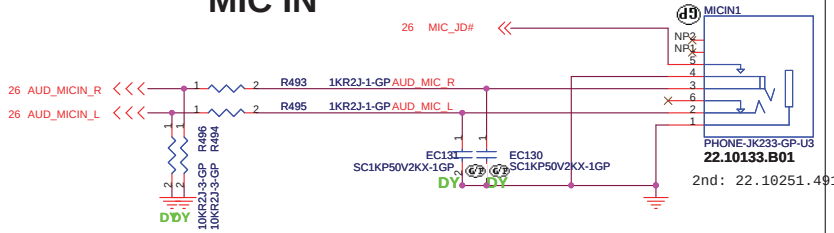
Internal Microphone



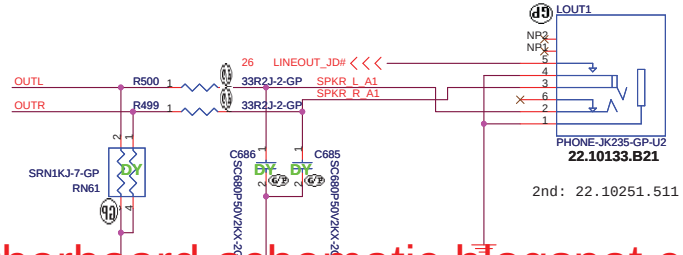
Internal Speaker



MIC IN



LINE OUT



<Variant Name>

緯創資通 **Wistron Corporation**
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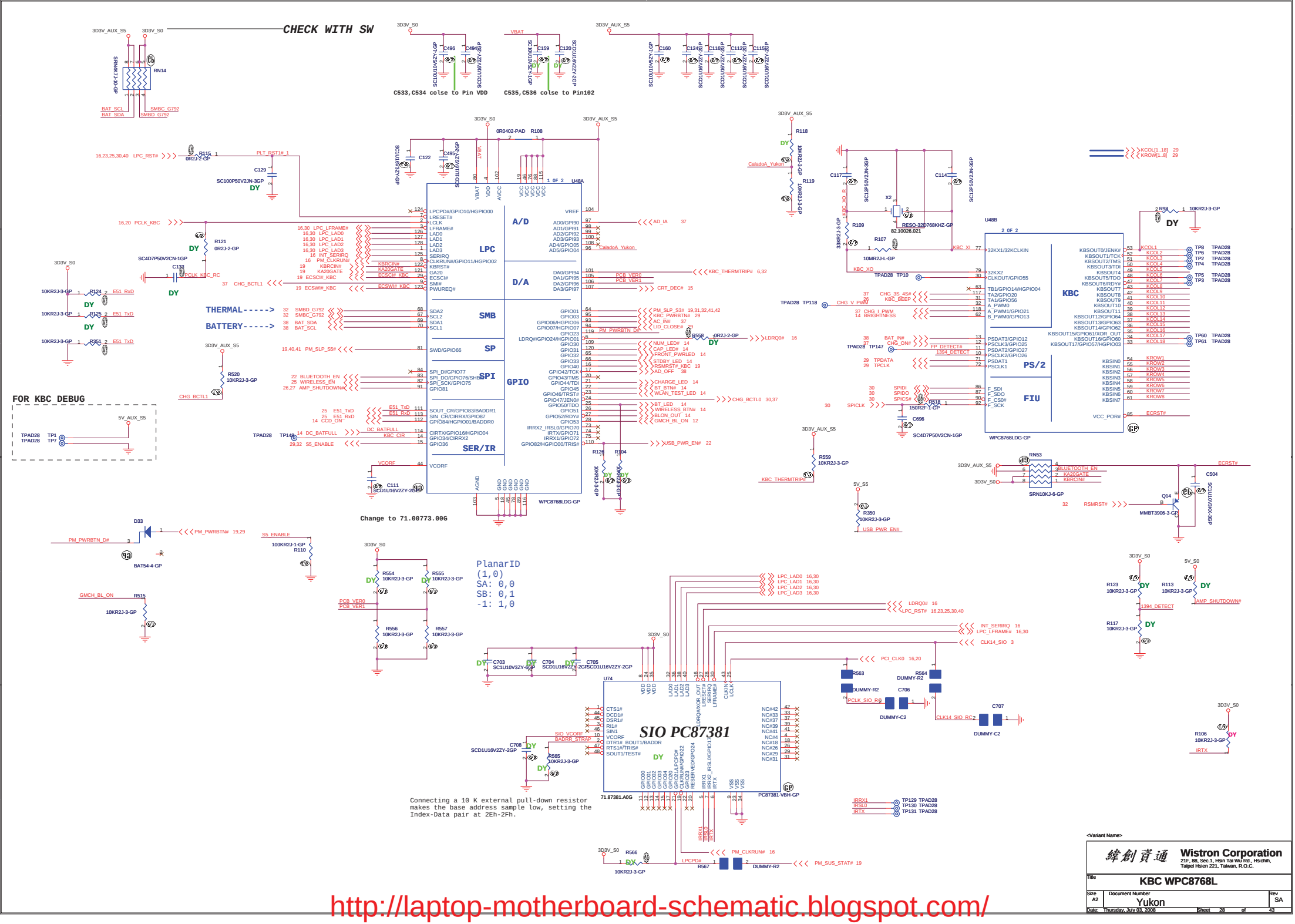
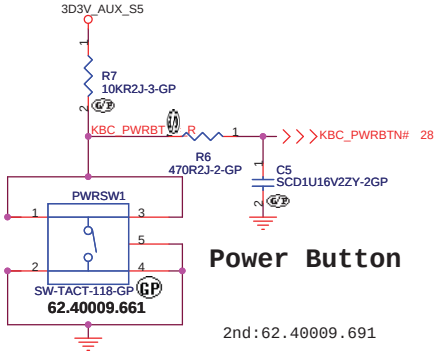
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP AND JACK*

Size	Document Number	Rev
	Yukon	SA

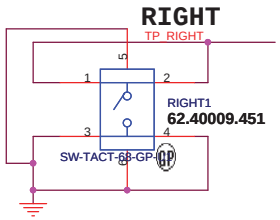
Date: Thursday, July 03, 2008 Sheet 27 of 43

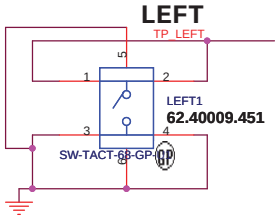

CHECK WITH SW
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
Change to 71.00773.00G
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
SIO PC87381
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
THERMAL-----> 32 SMBD_G792 32 SMBC_G792
BATTERY-----> 38 BAT_SDA 38 BAT_SCL
FOR KBC DEBUG
KBC
PS/2
FIU
WPC8768LDG-GP
PC87381-VBH-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Yukon
Thursday, July 03, 2008
http://laptop-motherboard-schematic.blogspot.com/



Power Button

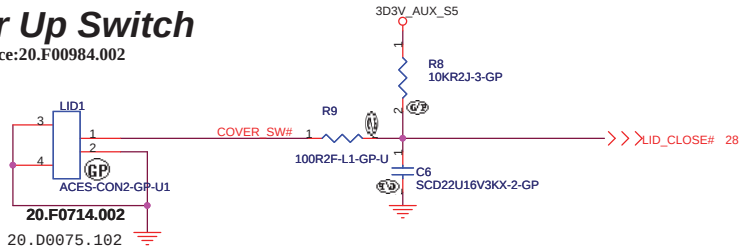
2nd:62.40009.691





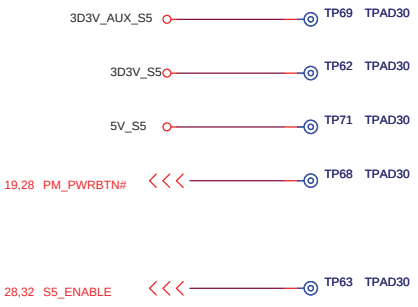
Cover Up Switch

2nd source:20.F00984.002

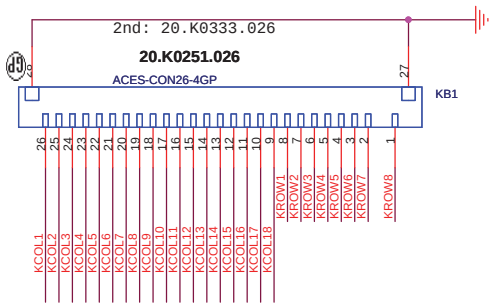


2nd: 20.D0075.102

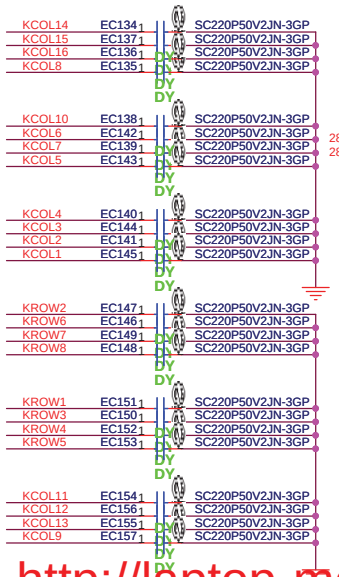
Check test point

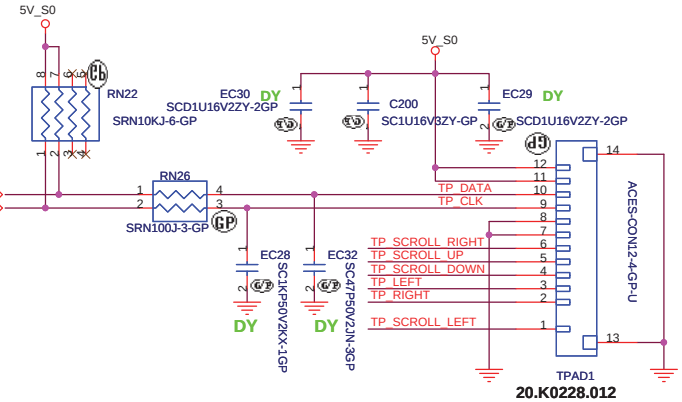


Test Point放在Dimm Door打開可量測處

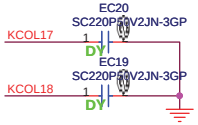


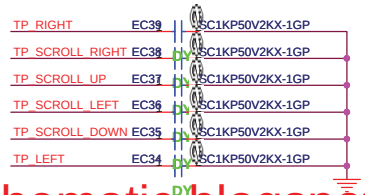
EMI Bypass cap.





2nd: 20.K0359.012





KROW[1..8] 28

KCOL[1..18] 28

Internal KeyBoard CONN

1 25

CHECK KB SPEC. AND PIN DEFINE

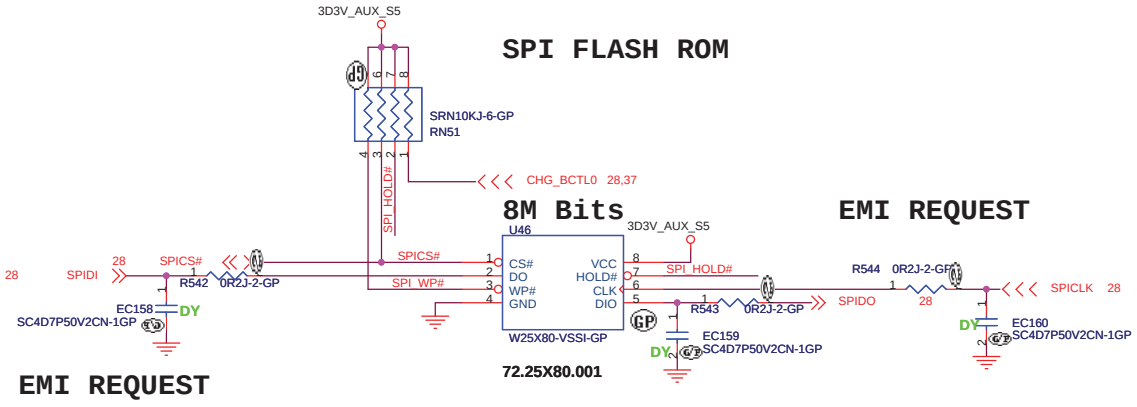
bom1

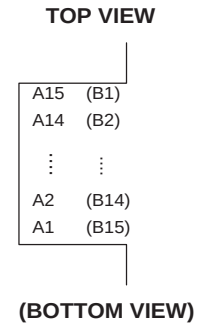
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

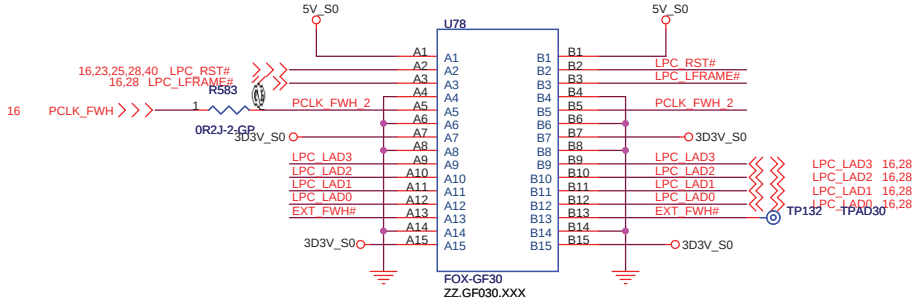
Title: BUTTONs / KB / TOUCHPAD

Size | Document Number: Yukon | Rev: SA

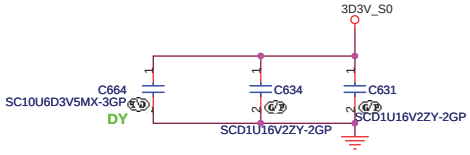
Date: Thursday, July 03, 2008 | Sheet 29 of 43







Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

Size	Document Number	Rev
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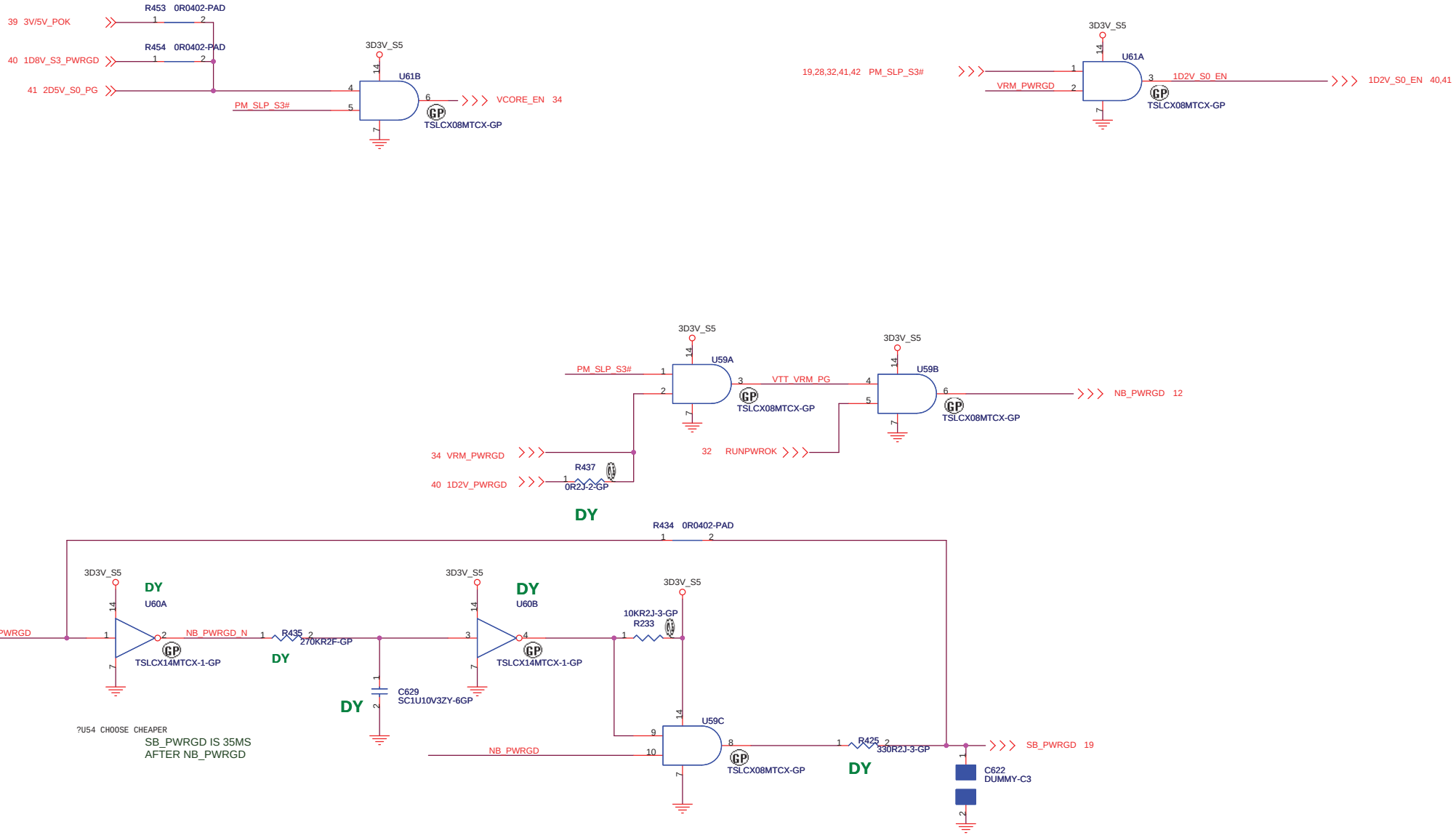


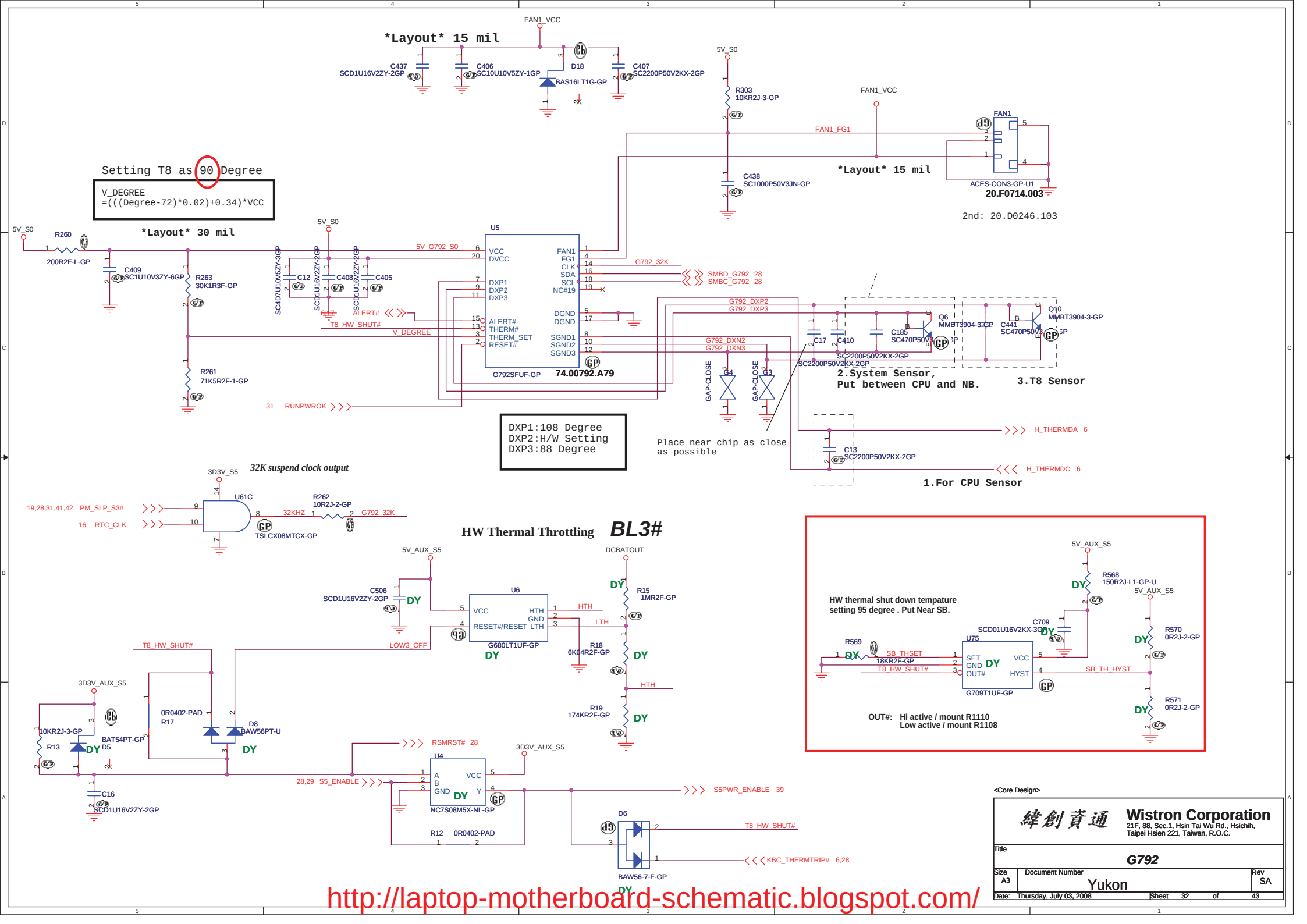
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size: A3 | Document Number: Yukon | Rev: SA

Date: Thursday, July 03, 2008 | Sheet 31 of 43



CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 — INPUT — OUT — 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 — INPUT — OUT — 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal (I)
Input Power VCC(I) VCC(I)

Output Signal (O)
Output Power VCC(O)

AD_IN
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

Output Power
VCC (O)
VCC (O)

Input Power
DCIN (I)

AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)
VCC(O)

DCBATOUT
5V_S5

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal SS_STBY1(I / 5V) FOR 1.2V
Input Power VCC VIN

Output Power
1D2V_PWR

1D2V (6.5A)
AD+

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal SS_STBY1(I / 5V) FOR 1.2V
Input Power VCC VIN

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

<Core Design>

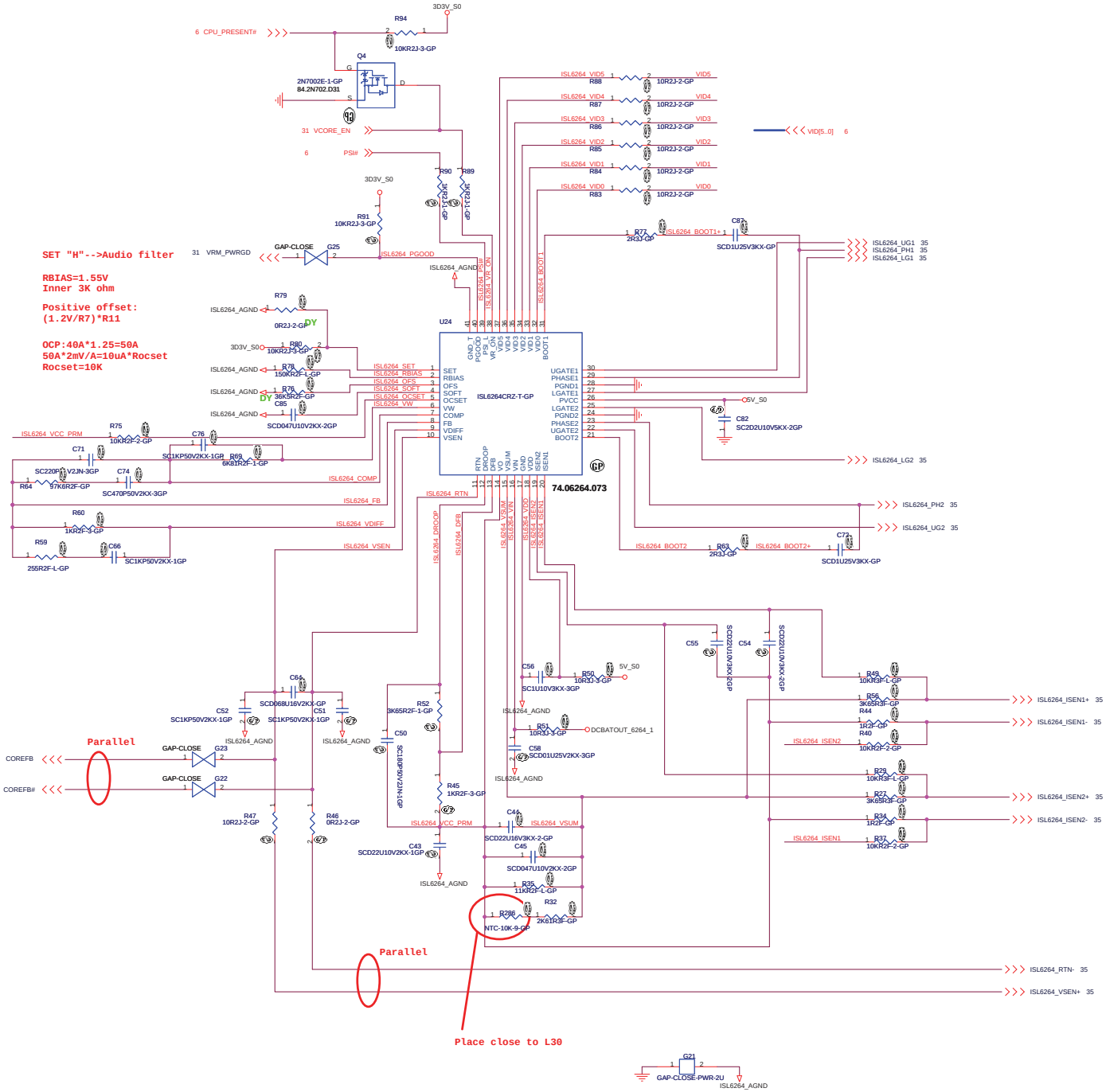
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram
Size: A3 | Document Number: Yukon | Rev: SA
Date: Tuesday, July 01, 2008 | Sheet 33 of 43

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1
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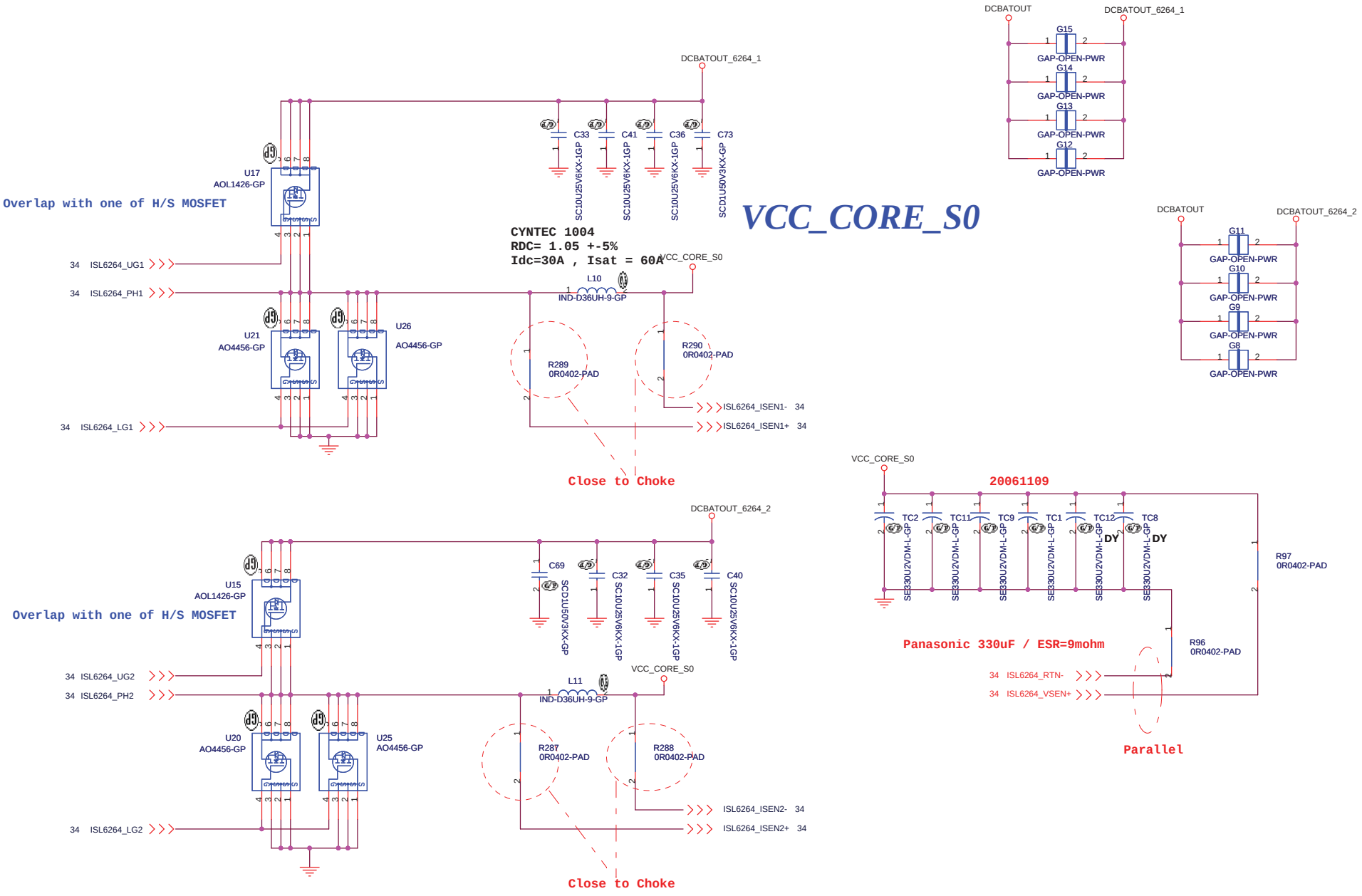

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Title: CPU Vcore Power_2

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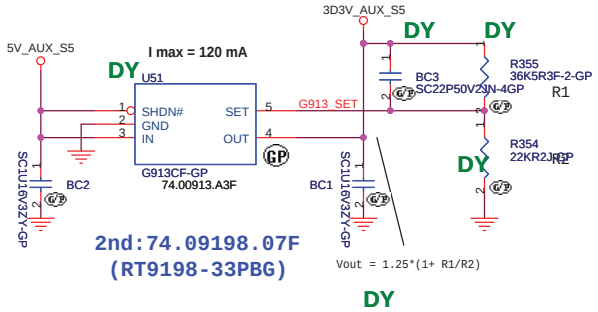
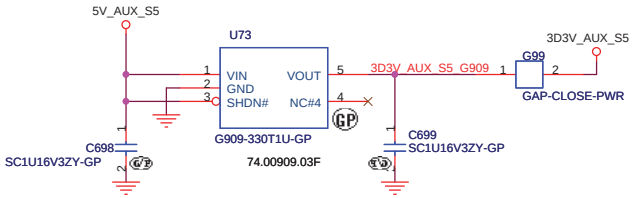
Aux Power

3D3V_AUX_S5

SB



Aux Power 3D3V_AUX_S5



<Core Design>

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Title: 3D3V_AUX		
Size: A3	Document Number: Yukon	Rev: SA
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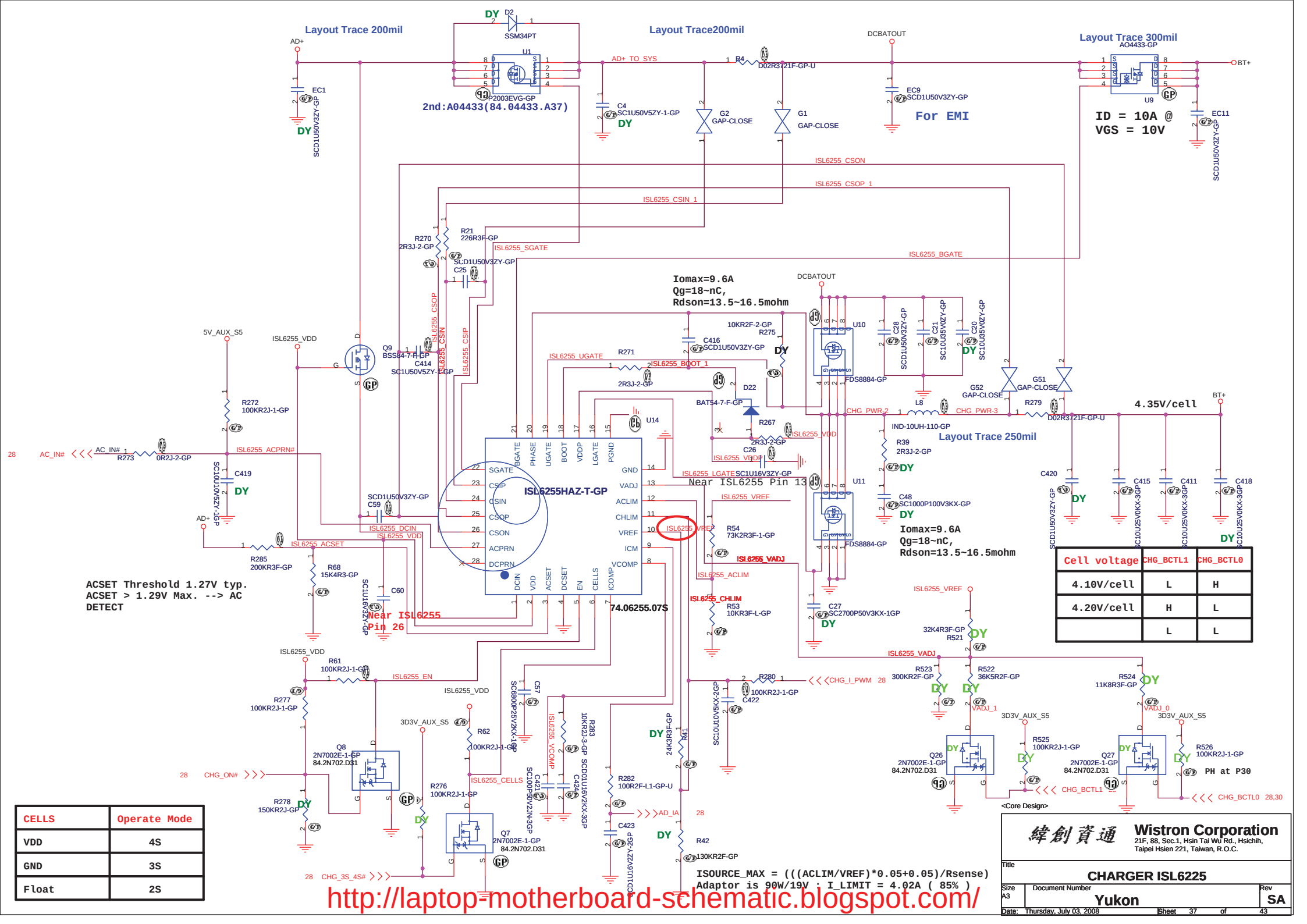
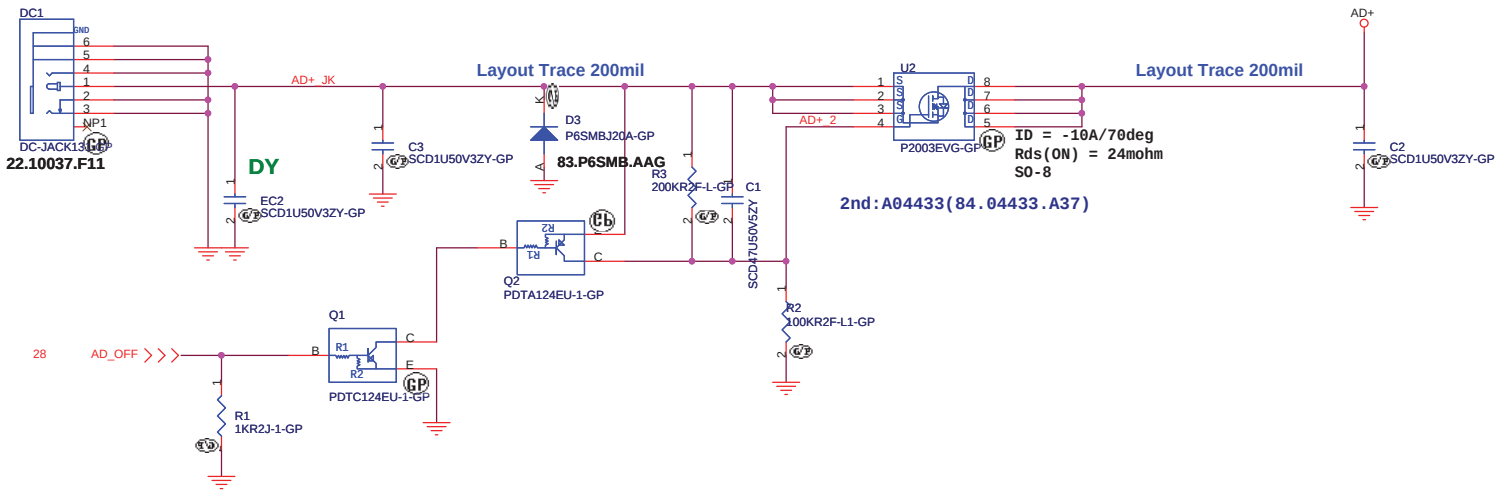


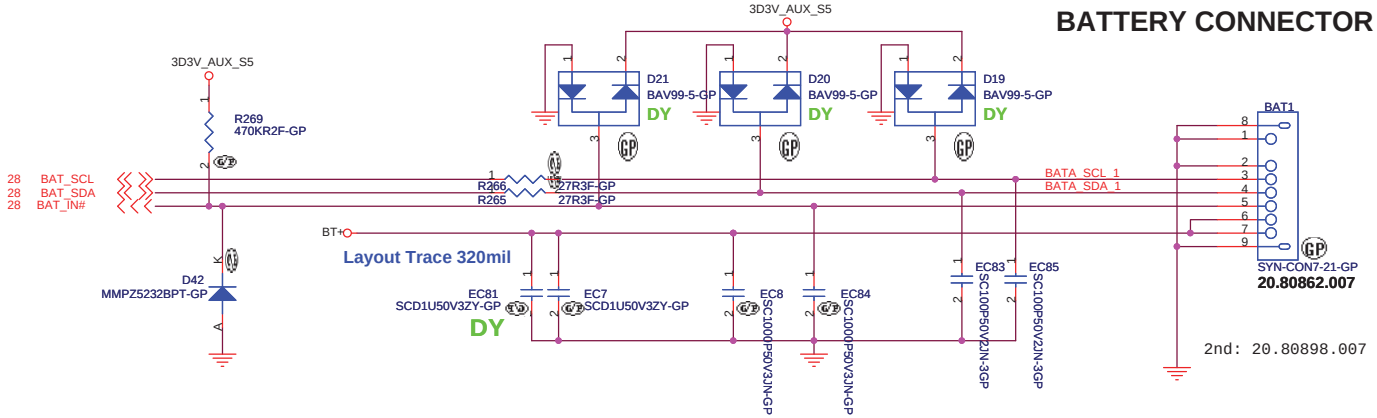
Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

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Title	AD/BATT CONN	
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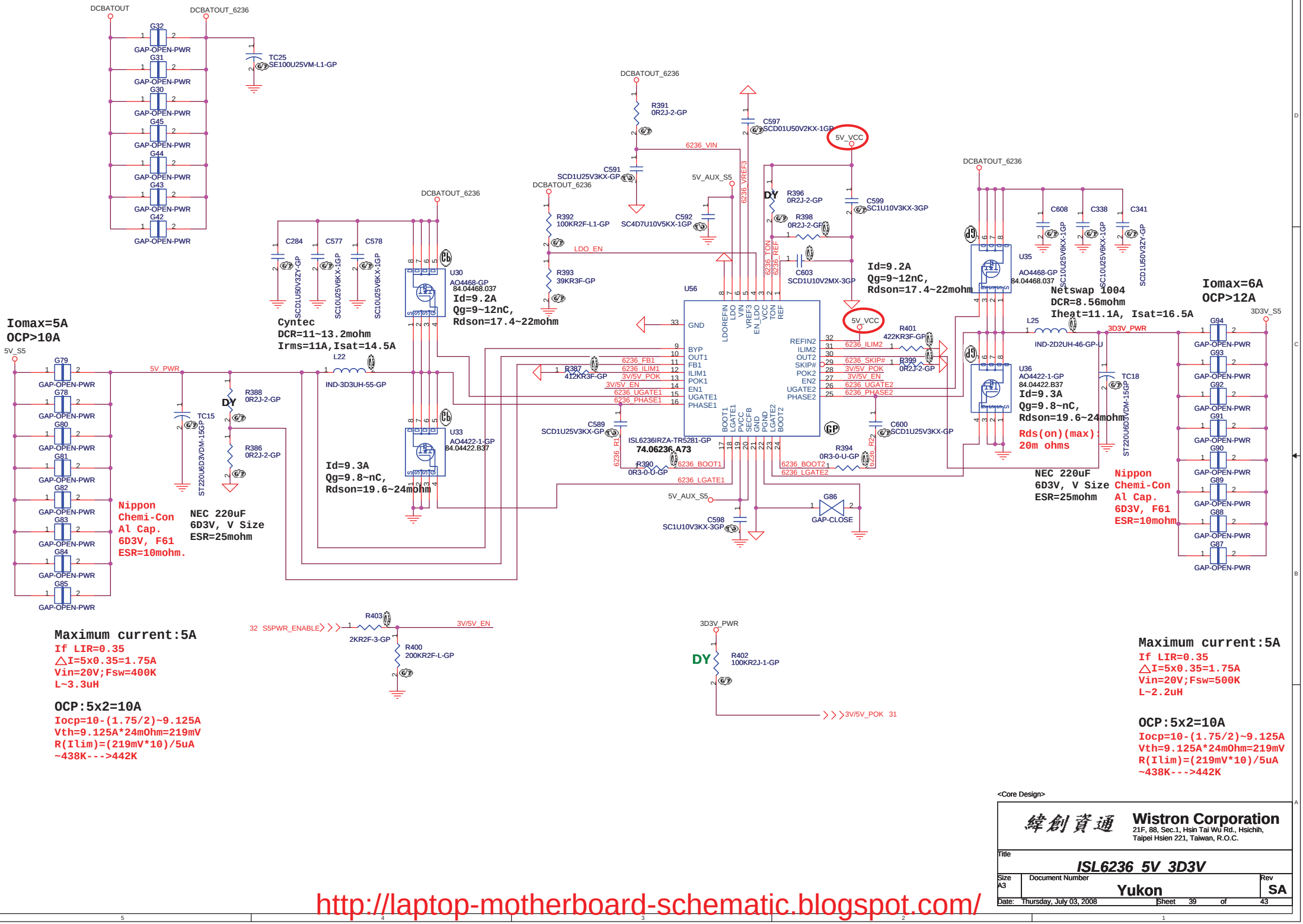
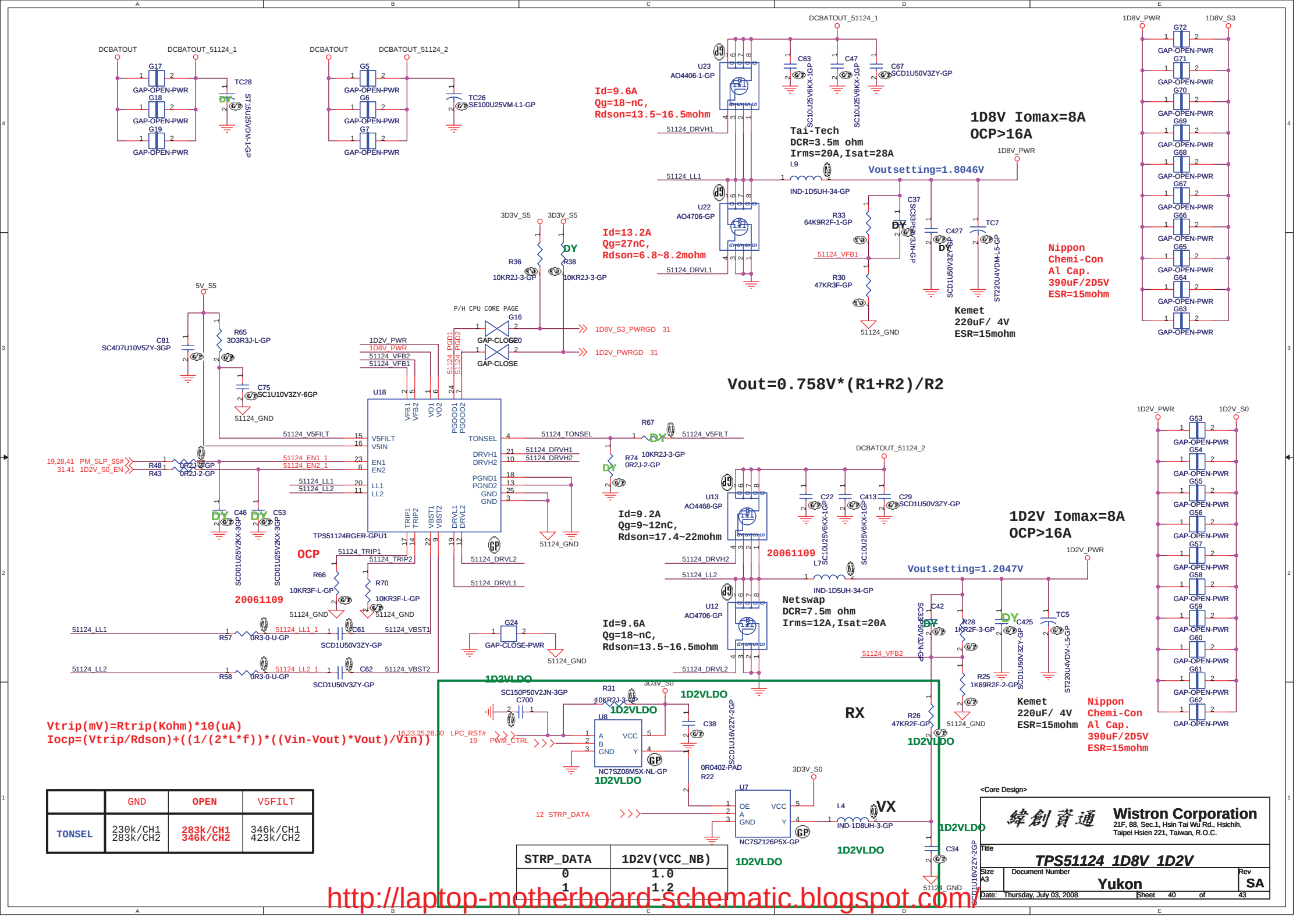
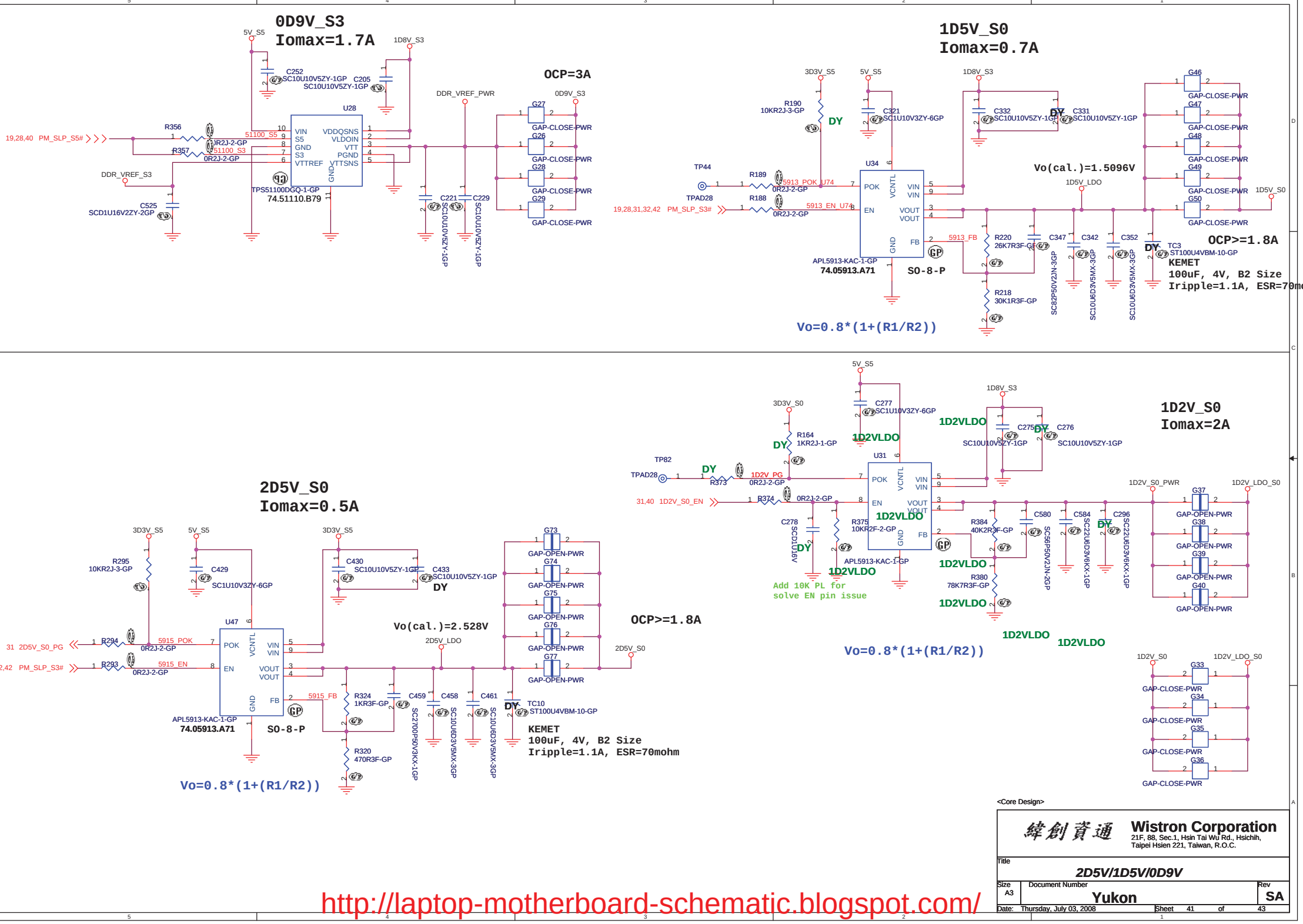
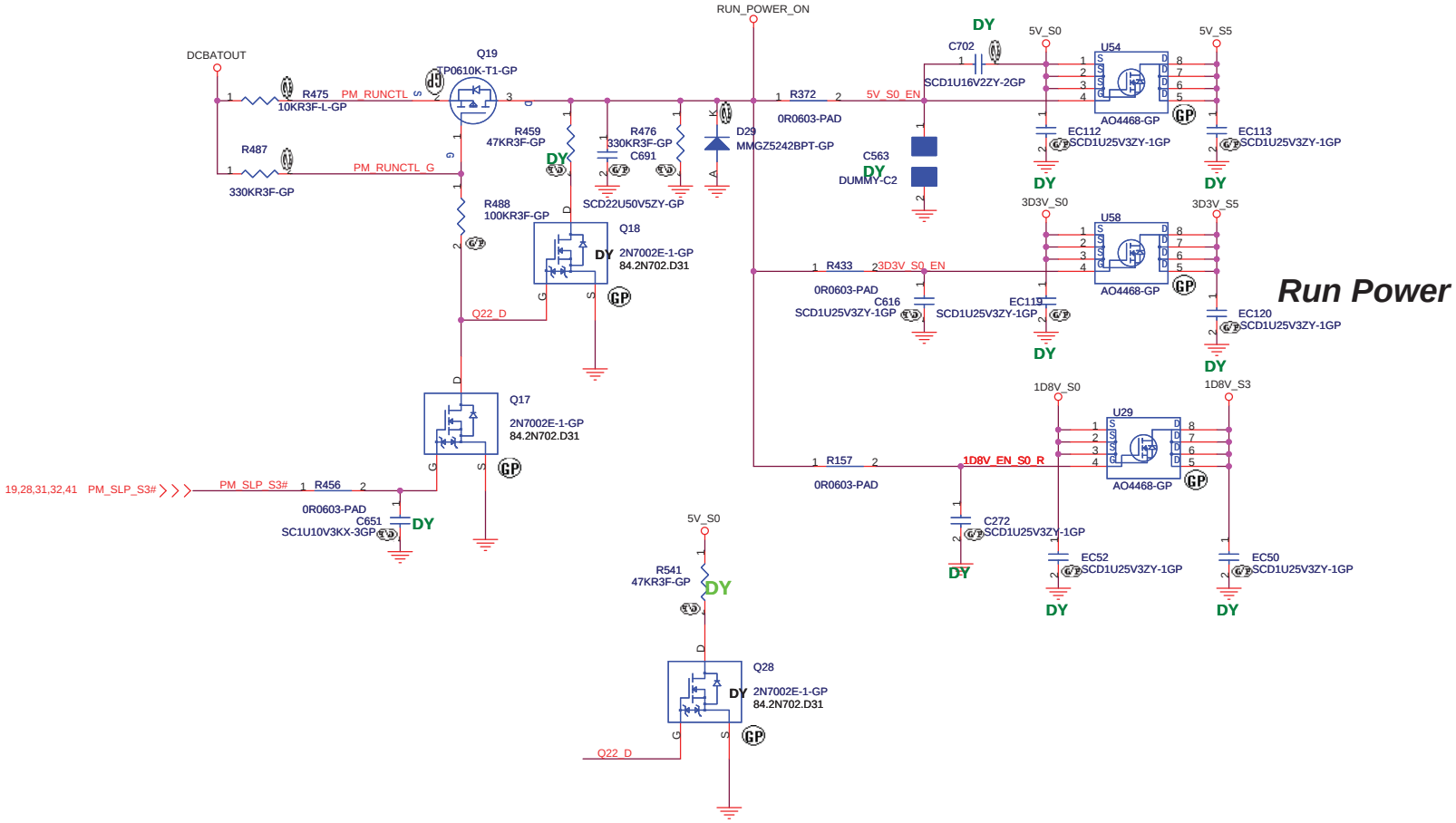




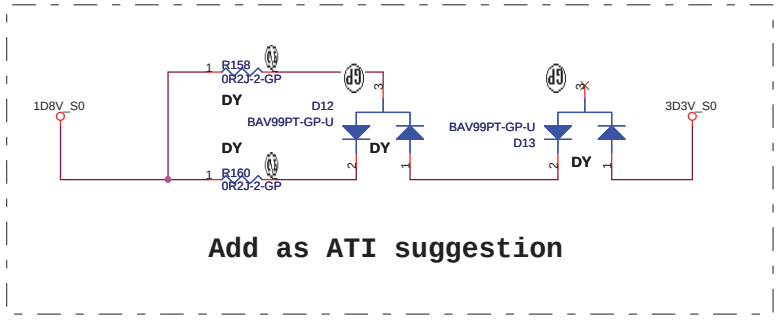
	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2





Run Power



Power On Logic

<Core Design>

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Title	***RUB POWER***
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SA

5V_S0
U3C
TSAHCT125PW-GP

DUMMY in SA

3D3V_S5
U60C
U60D
U60E
U60F
TSLCX14MTCX-1-GP
DY
34.42Y01.001
34.42Y01.001
34.4G502.001

CPU
Near H8
K1 DY
K2 DY
SPRING-5-GP
34.41Y01.001
34.41Y01.001
34.42Y01.001
34.42Y01.001

CPU
PCMCIA
Near H8
Near H15
Near CCD
K4 DY
K5 DY
K10 DY
K6 DY
K9 DY
K8 DY
K7
K3 DY
SPRING-23-GP
SPRING-7
34.39S07.001
34.49U26.001

K11
K12
SPRING-23-GP
34.39S07.001
34.39S07.001

H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H10 HOLE
H11 HOLE
H12 HOLE
GP8 GNDPAD
GP7 GNDPAD
GP5 GNDPAD
GP1 GNDPAD
GP2 GNDPAD
GP3 GNDPAD
GP4 GNDPAD
GP6 GNDPAD
GP10 GNDPAD

H13 HOLE
H14 HOLE
H15 HOLE
BOT(MDC)
34.42Y01.011

H16 HOLE
H18 HOLE
H17 HOLE
H19 HOLE
H20 HOLE
BOT(CPU)
H20 34.42Y01.011

H23 HOLE
H24 HOLE
BOT(MINI CARD)
34.4G502.001

34.49U26.001
K13 SPRING-7
K16 SPRING-7
K17 SPRING-7
K18 SPRING-7
K19 SPRING-7
K20 SPRING-7
K21 SPRING-7
K22 SPRING-7

34.39S07.001
K26 SPRING-23-GP
K27 SPRING-23-GP
K28 SPRING-23-GP

DCBATOUT
EC3 EC4 EC82 EC88 EC92 EC21 EC99 EC101 EC108 EC86 EC10 EC5 EC80
SCD1U25V2ZY-1GP

VCC_CORE_S0
EC94 EC15 EC97 EC47 EC104
SCD1U16V2ZY-6P

1D8V_S0
EC111 EC98 EC46 EC53 EC54 EC55
SCD1U16V2ZY-6P

3D3V_S0
EC87 EC91 EC90 EC100 EC76 EC6 EC121 EC59 EC71 EC57 EC68 EC109
DY
SCD1U16V2ZY-6P

1D8V_S3
EC93 EC18 EC66 EC49 EC48 EC22
DY
SCD1U16V2ZY-6P

5V_USB1_S5
EC102 EC56 EC106 EC74 EC123 EC69 EC75
DY
SCD1U16V2ZY-6P

3D3V_AUX_S5
EC161
SCD1U16V2ZY-6P

5V_S0
EC14 EC27 EC103 EC110 EC122 EC70 EC67
DY
SCD1U16V2ZY-6P

1D2V_S0
EC89 EC116 EC95 EC96 EC105 EC107 EC58
DY
SCD1U16V2ZY-6P

<Core Design>

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Size: Document Number: Yukon
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