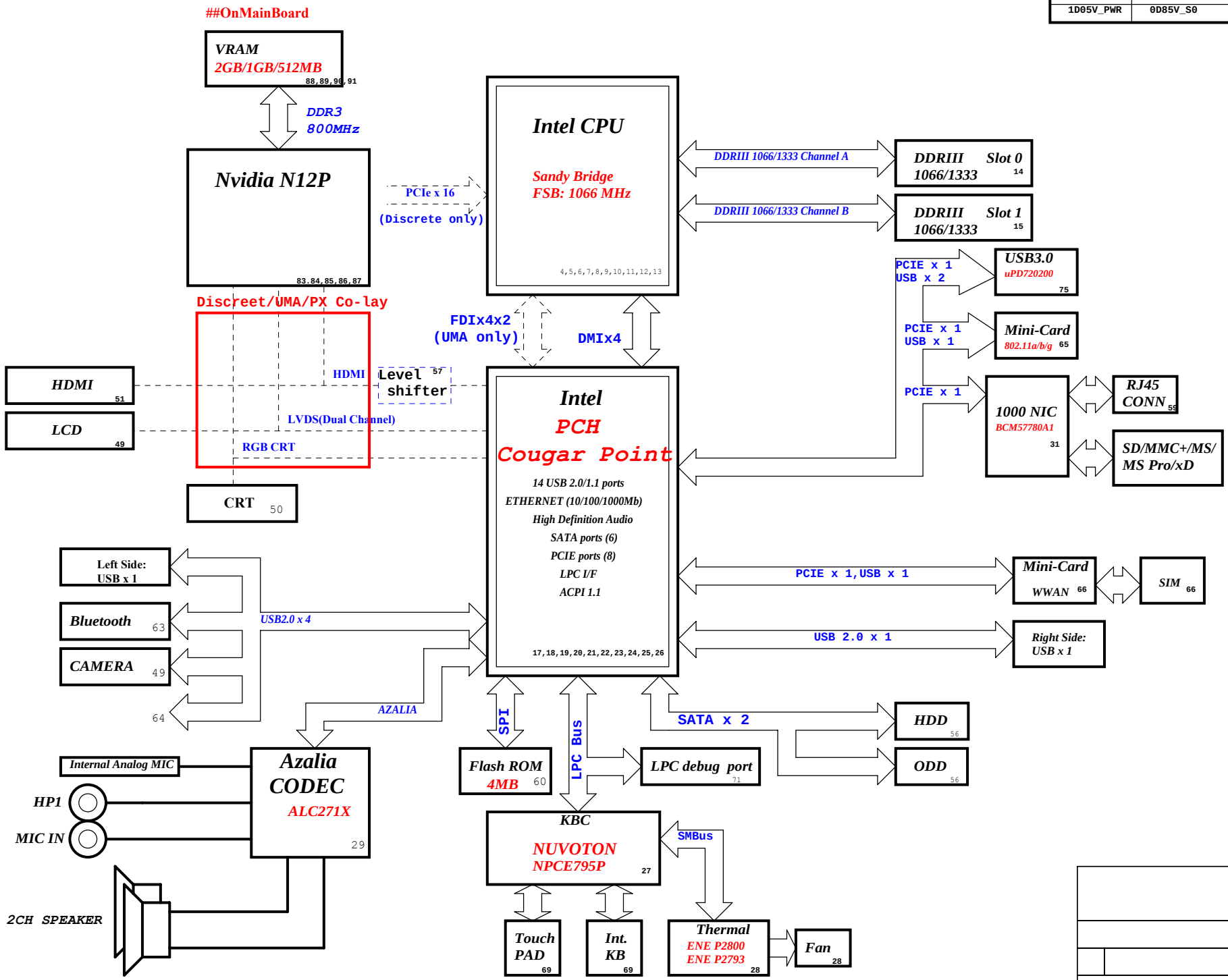


SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

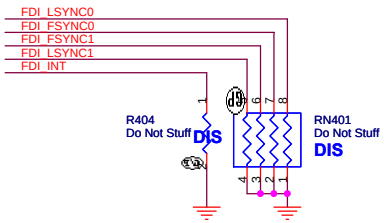
NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

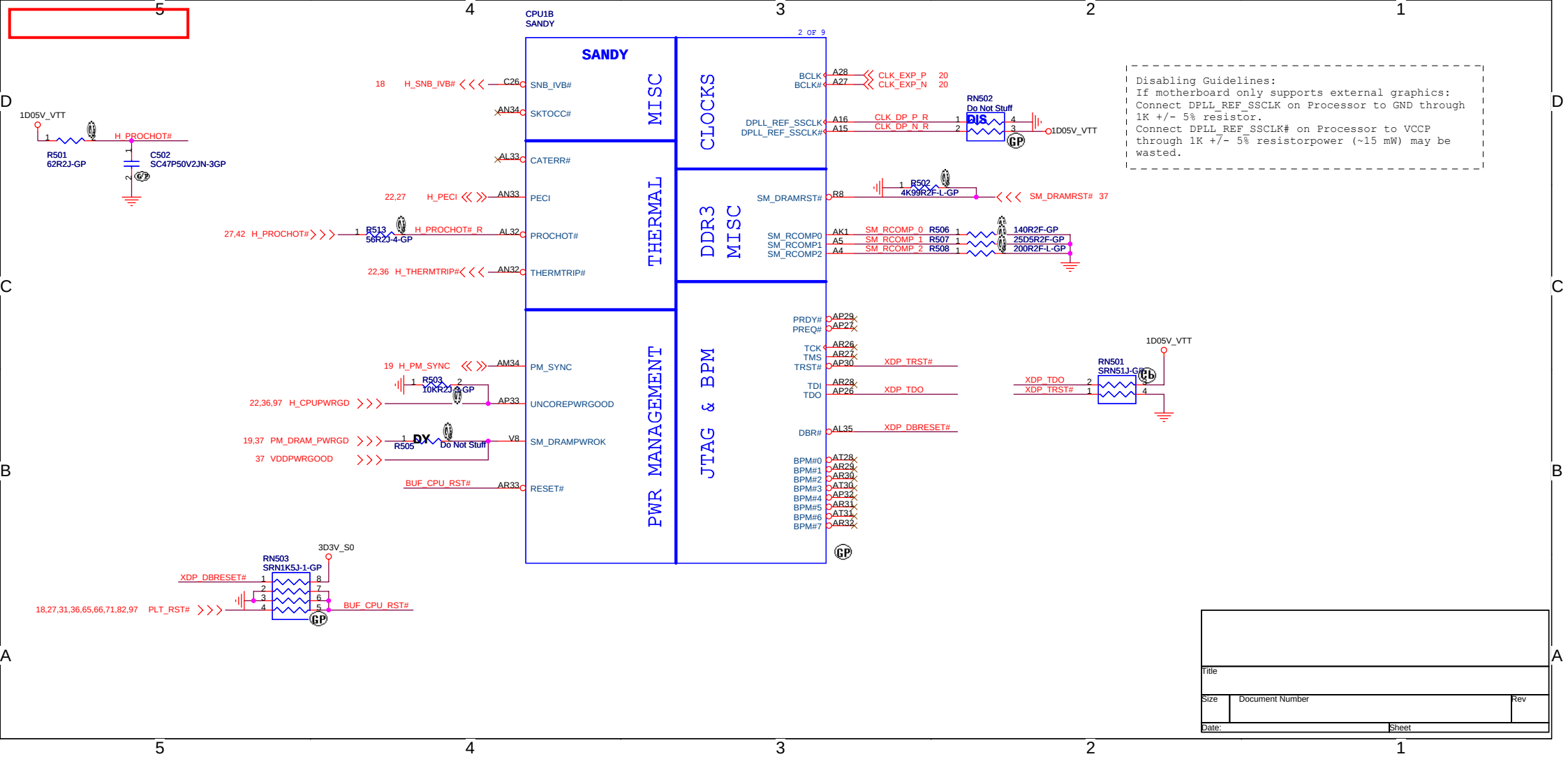
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.




CPU1B
SANDY
2 OF 9
SANDY
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
1D05V_VTT
H_PROCHOT#
R501
62R2J-GP
C502
SC47P50V2JN-3GP
H_SNB_IVB#
H_PECI
H_PROCHOT# R
R513
56R2J-4-GP
H_THERMTRIP#
H_PM_SYNC
R503
10KR2J-3-GP
H_CPUPWRGD
PM_DRAM_PWRGD
R505
Do Not Stuff
VDDPWRGOOD
BUF_CPU_RST#
CLK_EXP_P
CLK_EXP_N
CLK_DP_P_R
CLK_DP_N_R
RN502
Do Not Stuff
R502
4K99R2F-L-GP
SM_DRAMRST#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
R506
R507
R508
140R2F-GP
25D5R2F-GP
200R2F-L-GP
XDP_TRST#
XDP_TDO
XDP_DBRESET#
RN501
SRN51J-GP
RN503
SRN1K5J-1-GP
3D3V_S0
PLT_RST#
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.
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Date:
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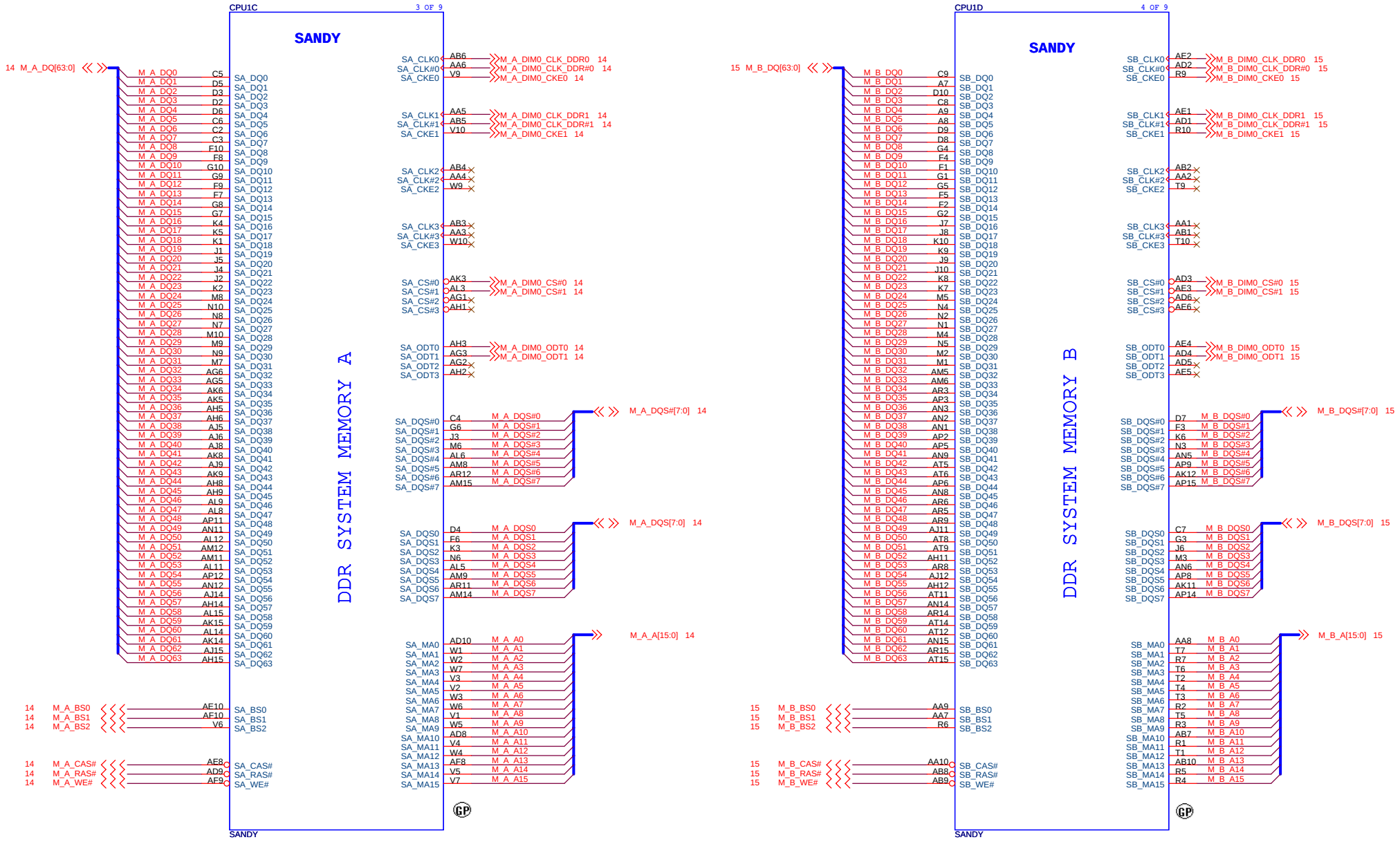

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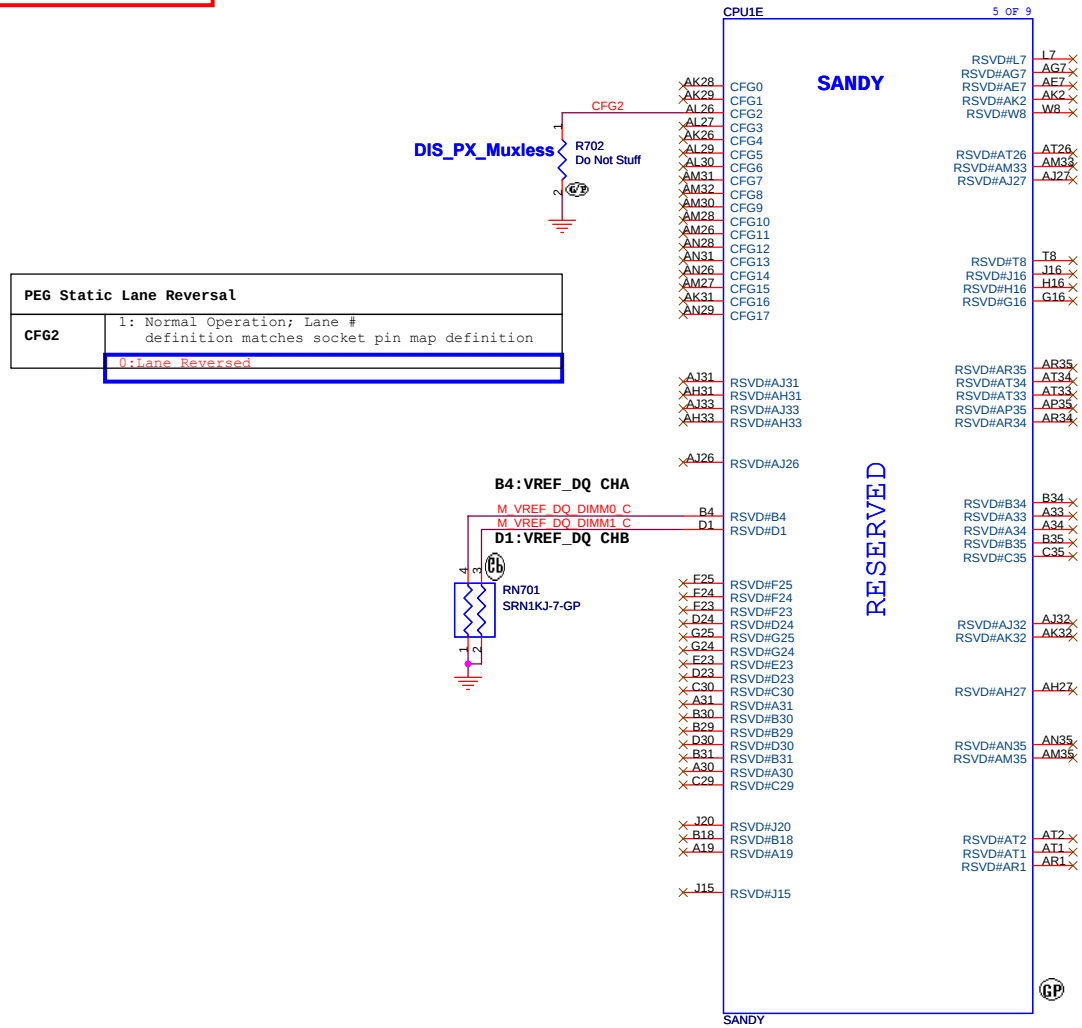

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POWER

PROCESSOR CORE POWER

53A

CPU1F

SANDY

6 OF 9

VCC_CORE

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

1D05V_VTT

VIDALERT#
VIDSCLK
VIDSOUT

H_CPU_SVIDALRT#
H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42

R803 43R2J-GP

VR_SVID_ALERT# 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

VCC_SENSE
VSS_SENSE

VCCSENSE 42
VSSSENSE 42

VCCIO_SENSE
VSSIO_SENSE

VCCIO_SENSE 45
VSSIO_SENSE 45

Title		
Size	Document Number	Rev
Date:	Sheet	

POWER

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff DY UMA_PX_Muxless
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 Do Not Stuff DY UMA_PX_Muxless
C907 Do Not Stuff DY UMA_PX_Muxless
C908 SC10U6D3V5KX-1GP
C918 Do Not Stuff DY UMA_PX_Muxless
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP

CPU1G — SANDY — 7 OF 9

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

GRAPHICS

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff DY
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 Do Not Stuff DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

C916 Do Not Stuff DY
C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 10R2J-2-GP
R902 need be close to pin H23.

MISC

VCCSA_SENSE H23 — VCCUSA_SENSE — TP901 Do Not Stuff

FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6 A6 A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

SANDY

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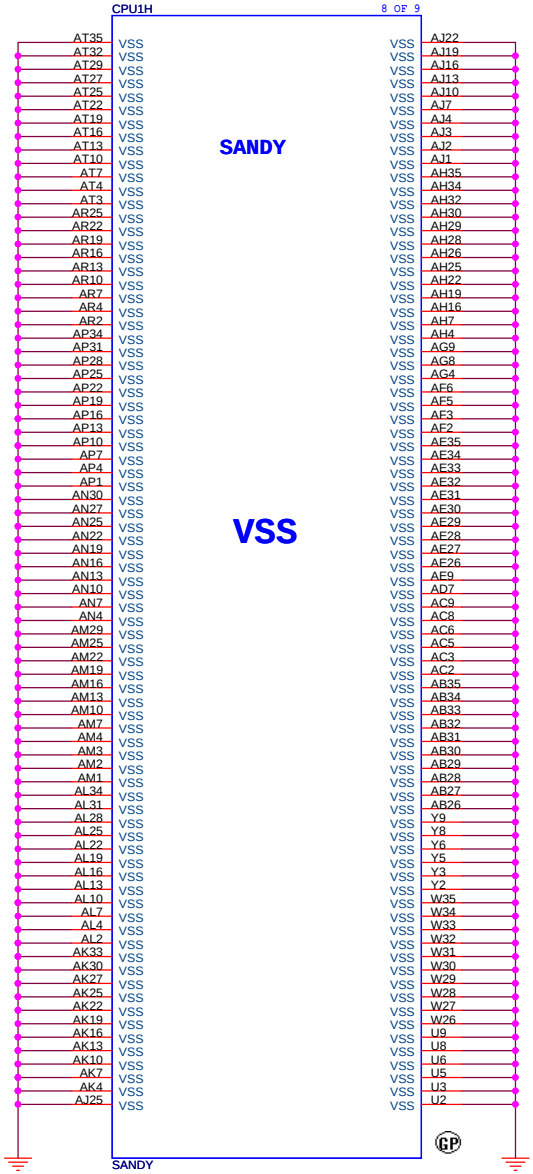
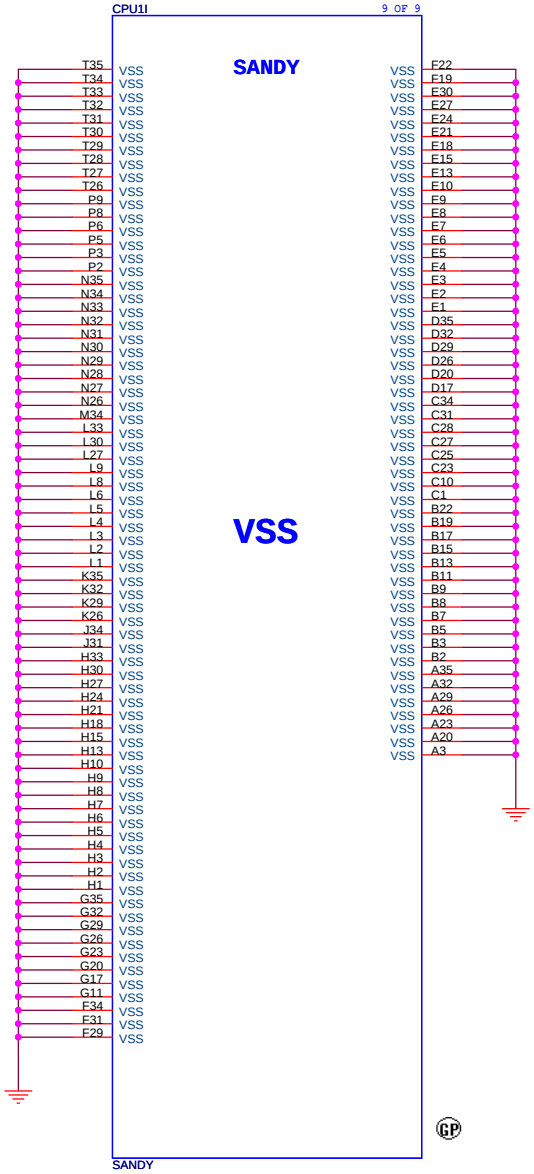
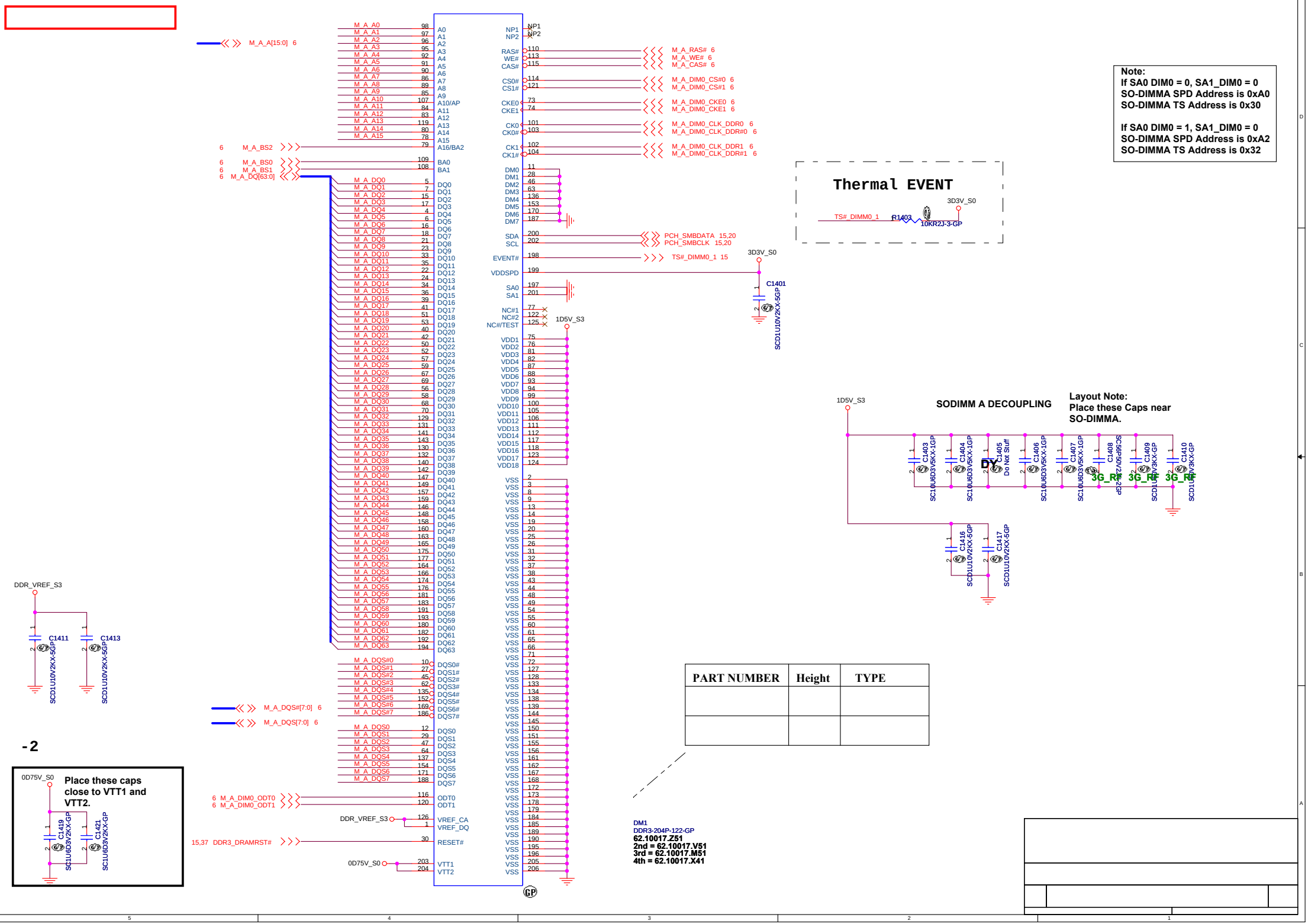
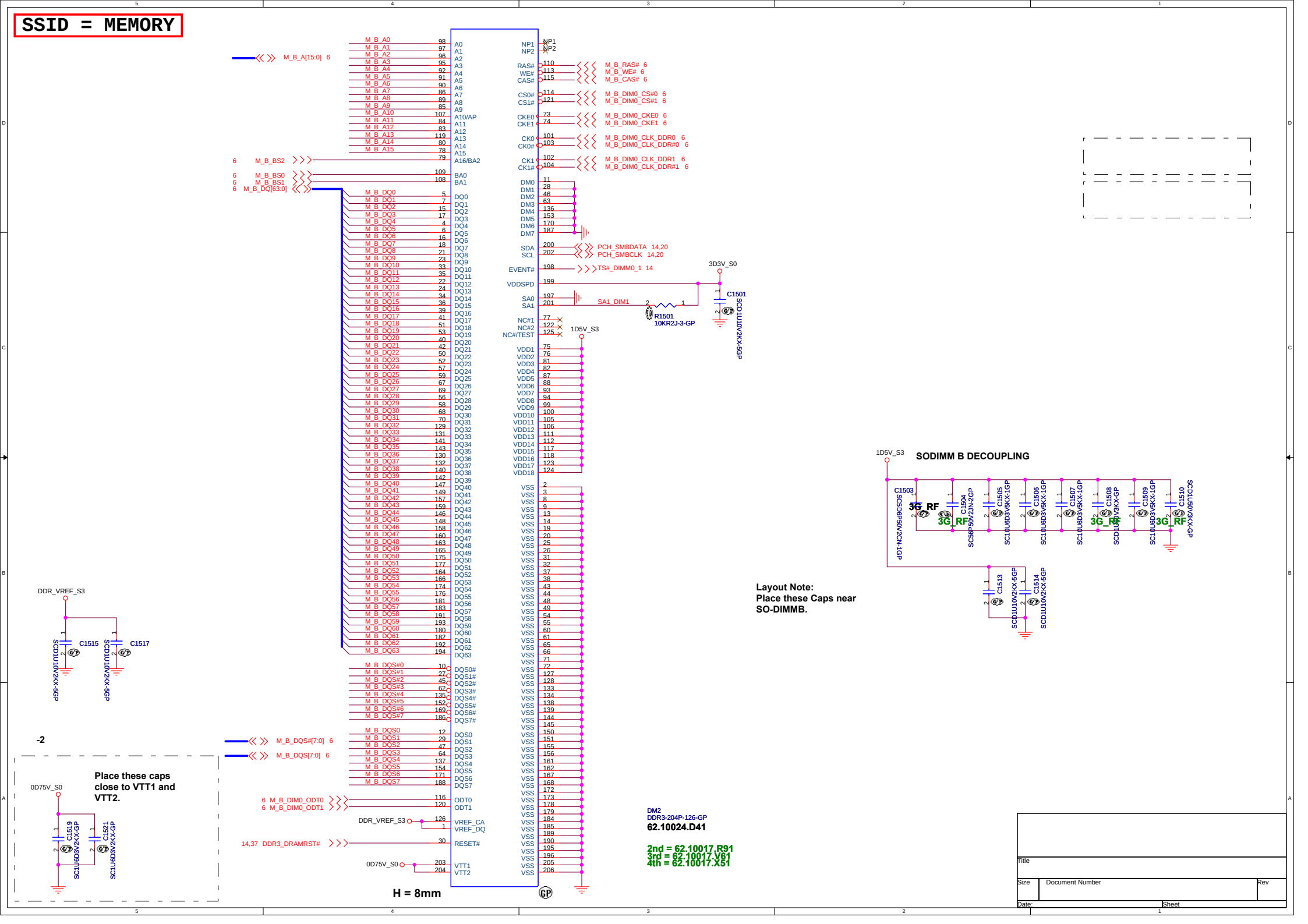

CPU1H
8 OF 9
SANDY
VSS
SANDY
AT35 AT32 AT29 AT27 AT25 AT22 AT19 AT16 AT13 AT10 AT7 AT4 AT3
AR25 AR22 AR19 AR16 AR13 AR10 AR7 AR4 AR2
AP34 AP31 AP28 AP25 AP22 AP19 AP16 AP13 AP10 AP7 AP4 AP1
AN30 AN27 AN25 AN22 AN19 AN16 AN13 AN10 AN7 AN4
AM29 AM25 AM22 AM19 AM16 AM13 AM10 AM7 AM4 AM3 AM2 AM1
AL34 AL31 AL28 AL25 AL22 AL19 AL16 AL13 AL10 AL7 AL4 AL2
AK33 AK30 AK27 AK25 AK22 AK19 AK16 AK13 AK10 AK7 AK4 AJ25
AJ22 AJ19 AJ16 AJ13 AJ10 AJ7 AJ4 AJ3 AJ2 AJ1
AH35 AH34 AH32 AH30 AH29 AH28 AH26 AH25 AH22 AH19 AH16 AH7 AH4
AG9 AG8 AG4
AF6 AF5 AF3 AF2
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AE9
AD7
AC9 AC8 AC6 AC5 AC3 AC2
AB35 AB34 AB33 AB32 AB31 AB30 AB29 AB28 AB27 AB26
Y9 Y8 Y6 Y5 Y3 Y2
W35 W34 W33 W32 W31 W30 W29 W28 W27 W26
U9 U8 U6 U5 U3 U2
GP
SANDY


CPU1I
9 OF 9
SANDY
VSS
SANDY
T35 T34 T33 T32 T31 T30 T29 T28 T27 T26
P9 P8 P6 P5 P3 P2
N35 N34 N33 N32 N31 N30 N29 N28 N27 N26
M34
L33 L30 L27 L9 L8 L6 L5 L4 L3 L2 L1
K35 K32 K29 K26
J34 J31
H33 H30 H27 H24 H21 H18 H15 H13 H10 H9 H8 H7 H6 H5 H4 H3 H2 H1
G35 G32 G29 G26 G23 G20 G17 G11
F34 F31 F29
F22 F19 E30 E27 E24 E21 E18 E15 E13 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1
D35 D32 D29 D26 D20 D17
C34 C31 C28 C27 C25 C23 C10 C1
B22 B19 B17 B15 B13 B11 B9 B8 B7 B5 B3 B2
A35 A32 A29 A26 A23 A20 A3
GP
SANDY


M_A_A[15:0] 6
M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6
M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6
M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6
DDR_VREF_S3
15,37 DDR3_DRAMRST#
0D75V_S0
M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6
PCH_SMBDATA 15,20
PCH_SMBCLK 15,20
TS#_DIMM0_1 15
3D3V_S0
1D5V_S3
C1401
SCD1U10V2KX-5GP
Thermal EVENT
TS#_DIMM0_1
R1403
10KR2J-3-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
C1403
C1404
C1405
Do Not Stuff
C1406
C1407
C1408
C1409
C1410
C1416
C1417
SC10U6D3V5KX-1GP
SCD1U10V3KX-GP
SCD1U10V2KX-5GP
DY
3G_RF
DDR_VREF_S3
C1411
C1413
-2
0D75V_S0
Place these caps
close to VTT1 and
VTT2.
C1419
C1421
SC1U6D3V2KX-GP
DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41
PART NUMBER
Height
TYPE

SSID = MEMORY



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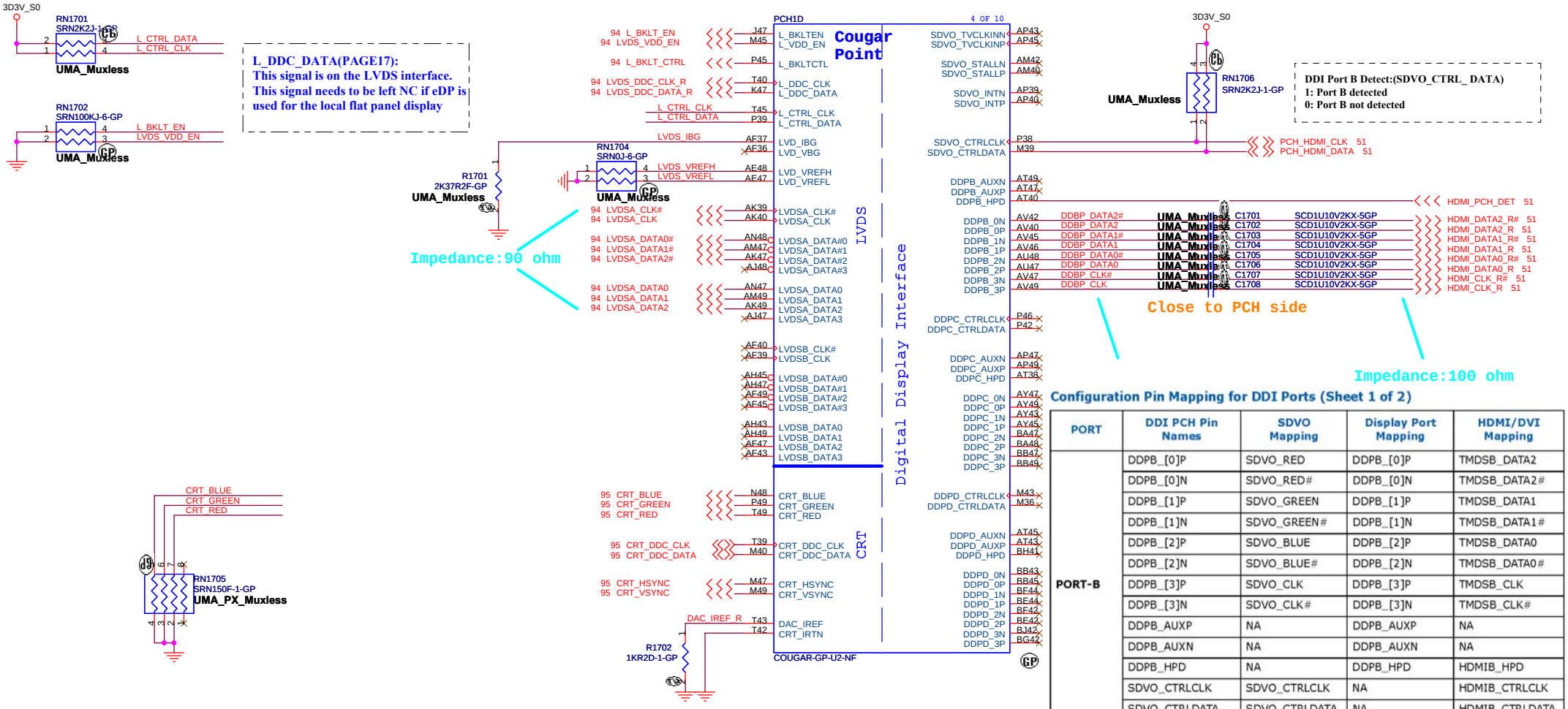
Date:	Sheet

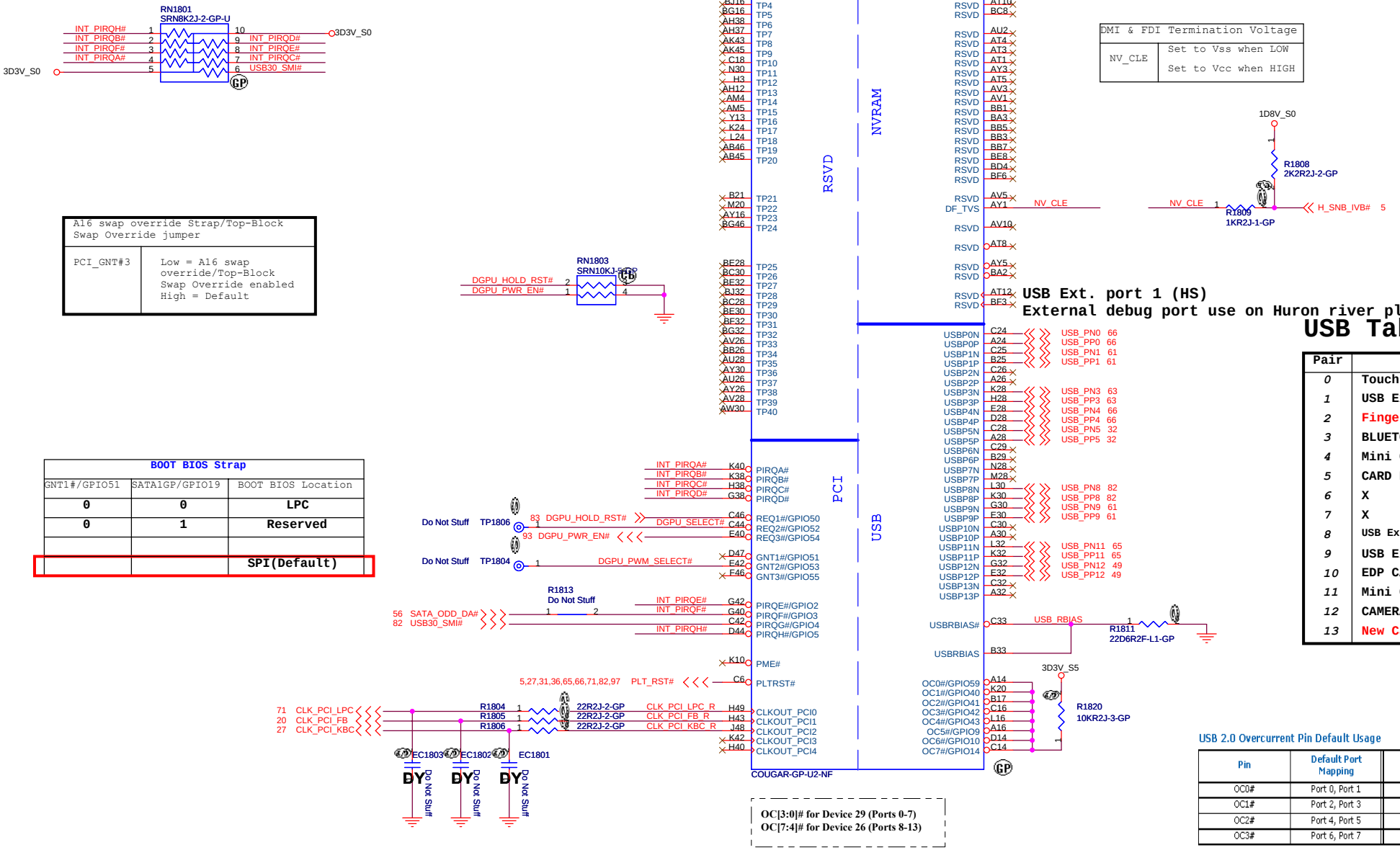


Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Title		
Size	Document Number	Rev
Date:	Sheet	

SSID = PCH



USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

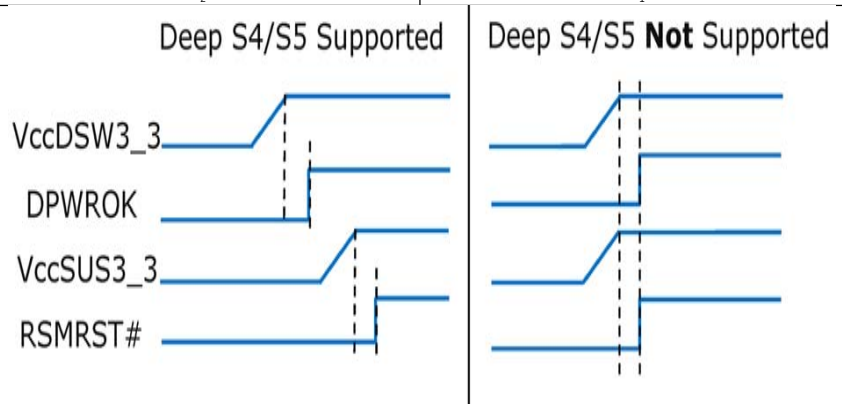
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Title

Size | Document Number | Rev

Date: | Sheet

SSID = PCH



PCH1C — Cougar Point — 3 OF 10 — System Power Management

DMI: DMI0RXN/DMI1RXN/DMI2RXN/DMI3RXN, DMI0RXP/DMI1RXP/DMI2RXP/DMI3RXP, DMI0TXN/DMI1TXN/DMI2TXN/DMI3TXN, DMI0TXP/DMI1TXP/DMI2TXP/DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

DMI_ZCOMP — R1901 49D9R2F-GP — DMI_COMP_R

DMI_IRCOMP

DMI2RBIAS — R1902 750R2F-GP — RBIAS_CPY

1D05V_VTT

R1926 Do Not Stuff (DY) — SYS_PWROK

R1904 100KR2J-1-GP — PWROK

0628 Modify:
Change R1904 to 100K 0402 from 10K and default stuff.

SUSACK# — SUS_PWR_ACK

SYS_RESET# — R1905 10KR2J-3-GP — 3D3V_S0

SYS_PWROK — 36 SYS_PWROK

PWROK — R1924 Do Not Stuff — 27,42 S0_PWR_GOOD

APWROK

DRAMPWROK — 5,37 PM_DRAM_PWRGD

RSMRST# — PM_RSMRST#

SUSWARN#/SUSPWRDNACK/GPIO30 — 27 SUS_PWR_ACK

PWRBTN# — 27,97 PM_PWRBTN#

ACPRESENT/GPIO31 — 27 AC_PRESENT

BATLOW#/GPIO72 — BATLOW#

RI# — PM_RI#

DSWVRMEN — A18 DSWODVREN

DPWROK — F22 PCH_DPWROK — R1910 Do Not Stuff (DY) — R1911 Do Not Stuff — PM_RSMRST# — RTC_AUX_S5

WAKE# — B9 PCIE_WAKE# 31,65,66,82

CLKRUN#/GPIO32 — N3 PM_CLKRUN# 27

SUS_STAT#/GPIO61 — G8

SUSCLK/GPIO62 — N14 PCH_SUSCLK_KBC 27

SLP_S5#/GPIO63 — D10

SLP_S4# — H4 PM_SLP_S4# 27,46

SLP_S3# — F4 PM_SLP_S3# 27,36,37,47,92

SLP_A# — G10

SLP_SUS# — G16

PMSYNCH — AP14 H_PM_SYNC 5

SLP_LAN#/GPIO29 — K14

COUGAR-GP-U2-NF

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 (DY) Do Not Stuff

PM_CLKRUN# — R1919 8K2R2J-3-GP — 3D3V_S0

3D3V_S5 — RN1901 SRN10KJ-6-GP — BATLOW# / PM_RI# / AC_PRESENT / SUS_PWR_ACK

R1921 10KR2J-3-GP — PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP — PM_RSMRST#

3D3V_AUX_S5 — R1909 100KR2J-1-GP — R1916 10KR2J-3-GP — 3V_5V_POK_#

Q1901 2N7002KDW-GP — PM_RSMRST# — R1912 1KR2J-1-GP — RSMRST#_KBC 27 — 3V_5V_POK 41

84.2N702.A3F
2nd = 84.DM601.03F

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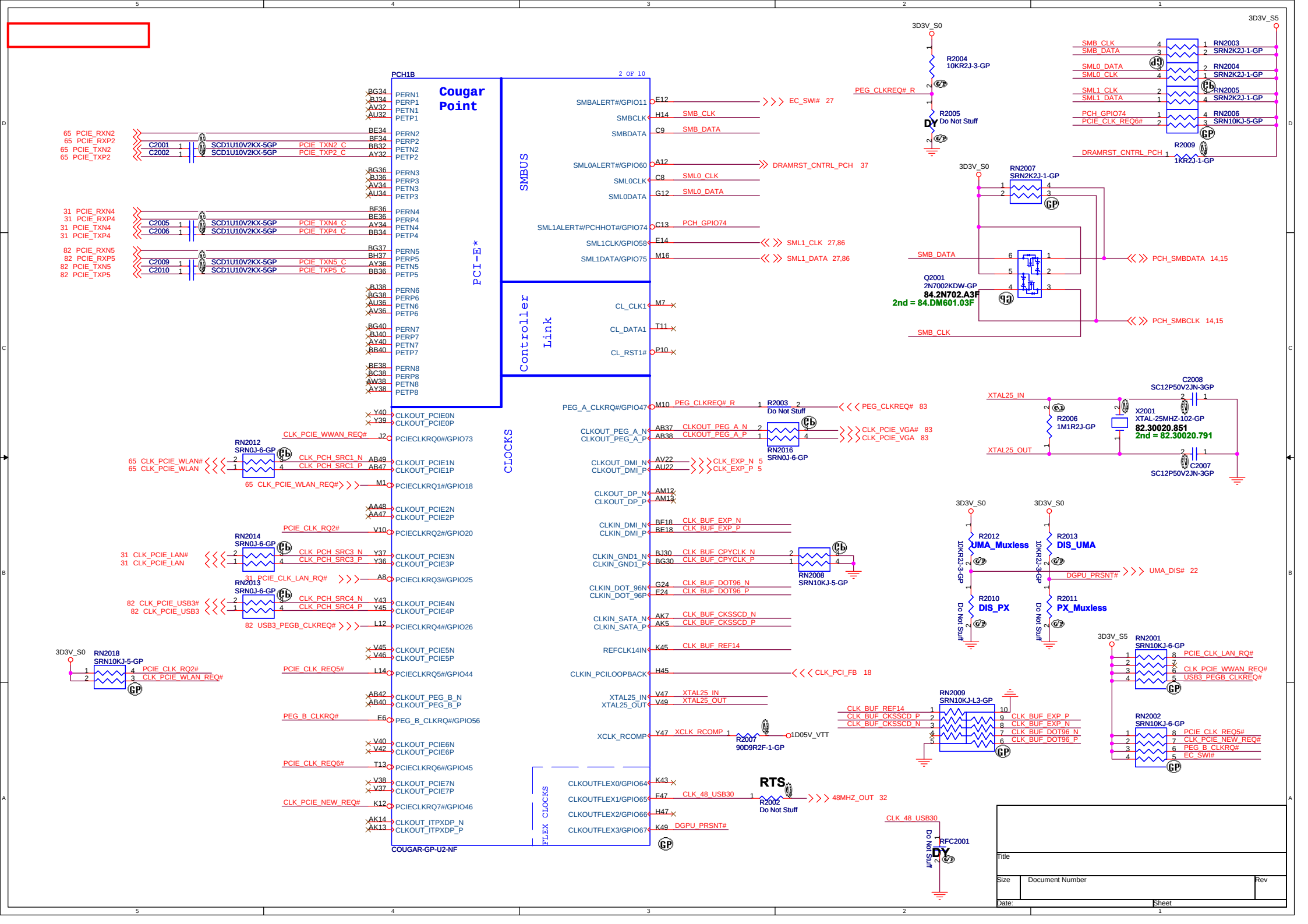
PCH1B
Cougar Point
2 OF 10
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR-GP-U2-NF
3D3V_S0
3D3V_S5
R2004 10KR2J-3-GP
R2005 Do Not Stuff
R2009 1KR2J-1-GP
RN2003 SRN2K2J-1-GP
RN2004 SRN2K2J-1-GP
RN2005 SRN2K2J-1-GP
RN2006 SRN10KJ-5-GP
RN2007 SRN2K2J-1-GP
Q2001 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
SMB_CLK
SMB_DATA
SML0_CLK
SML0_DATA
SML1_CLK
SML1_DATA
PCH_GPIO74
PCIE_CLK_REQ6#
DRAMRST_CNTRL_PCH
PCH_SMBDATA 14,15
PCH_SMBCLK 14,15
PEG_CLKREQ# R
EC_SWI# 27
DRAMRST_CNTRL_PCH 37
SML1_CLK 27,86
SML1_DATA 27,86
C2001 SCD1U10V2KX-5GP
C2002 SCD1U10V2KX-5GP
C2005 SCD1U10V2KX-5GP
C2006 SCD1U10V2KX-5GP
C2009 SCD1U10V2KX-5GP
C2010 SCD1U10V2KX-5GP
RN2012 SRN0J-6-GP
RN2014 SRN0J-6-GP
RN2013 SRN0J-6-GP
RN2018 SRN10KJ-5-GP
RN2016 SRN0J-6-GP
RN2008 SRN10KJ-5-GP
R2003 Do Not Stuff
X2001 XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
R2006 1M1R2J-GP
C2007 SC12P50V2JN-3GP
C2008 SC12P50V2JN-3GP
R2012 UMA_Muxless
R2013 DIS_UMA
R2010 DIS_PX
R2011 PX_Muxless
RN2001 SRN10KJ-6-GP
RN2002 SRN10KJ-6-GP
RN2009 SRN10KJ-L3-GP
R2007 90D9R2F-1-GP
R2002 Do Not Stuff
RFC2001
RTS
Title
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Document Number
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Date:
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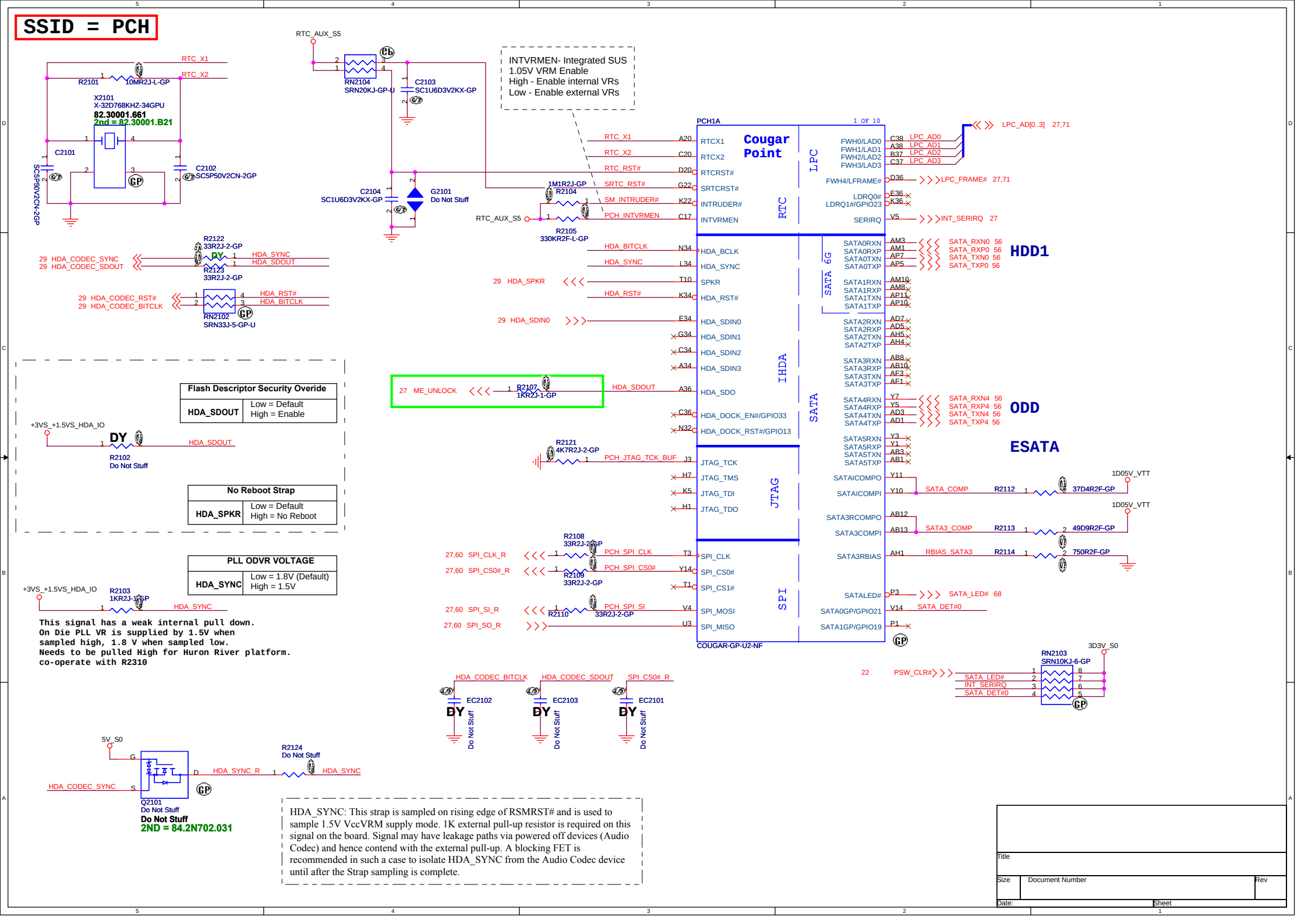
RTC_X1
RTC_X2
R2101
10MR2J-L-GP
X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101
SC5P50V2CN-2GP
C2102
SC5P50V2CN-2GP
RTC_AUX_S5
RN2104
SRN20KJ-GP-U
C2103
SC1U6D3V2KX-GP
C2104
SC1U6D3V2KX-GP
G2101
Do Not Stuff
INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs
PCH1A
1 OF 10
Cougar Point
RTC
LPC
SATA
IHDA
JTAG
SPI
COUGAR-GP-U2-NF
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
HDD1
ODD
ESATA
SATA_COMP
SATA3_COMP
RBIAS_SATA3
SATA_LED#
SATA_DET#0
R2122
33R2J-2-GP
R2123
33R2J-2-GP
RN2102
SRN33J-5-GP-U
R2104
1M1R2J-GP
R2105
330KR2F-L-GP
R2107
1KR2J-1-GP
R2121
4K7R2J-2-GP
R2108
33R2J-2-GP
R2109
33R2J-2-GP
R2110
33R2J-2-GP
R2112
37D4R2F-GP
R2113
49D9R2F-GP
R2114
750R2F-GP
RN2103
SRN10KJ-6-GP
R2102
Do Not Stuff
R2103
1KR2J-1-GP
R2124
Do Not Stuff
Q2101
Do Not Stuff
EC2102
EC2103
EC2101
Flash Descriptor Security Overide
HDA_SDOUT
Low = Default
High = Enable
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V (Default)
High = 1.5V
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310
Do Not Stuff
2ND = 84.2N702.031
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.
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Document Number
Rev
Date:
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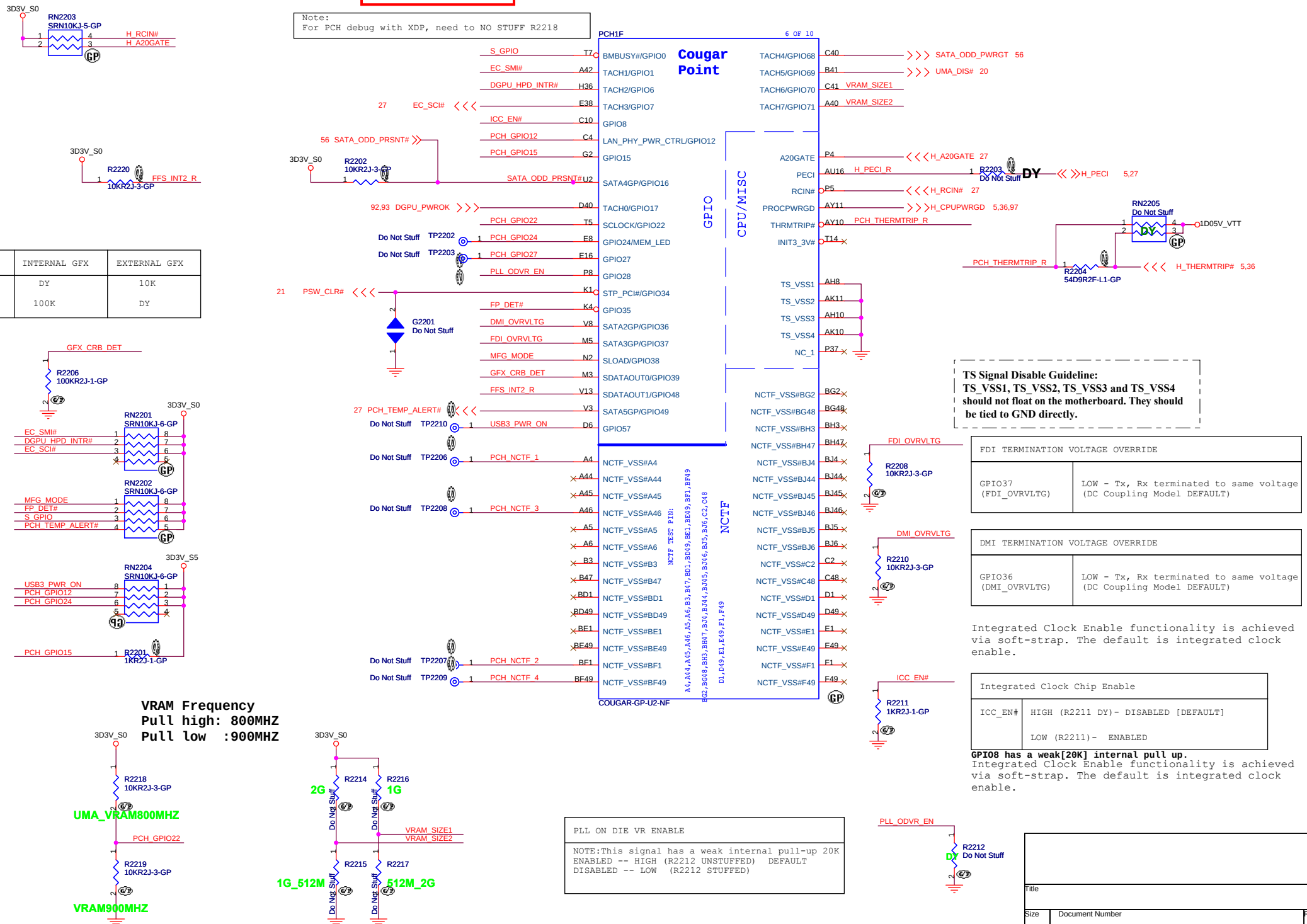

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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SSID = PCH

POWER

PCH1G — Cougar Point — 7 OF 10 — COUGAR-GP-U2-NF

VCC CORE

1D05V_VTT — 1.3A — (1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP; C2302 SC1U6D3V2KX-GP; C2303 SC1U6D3V2KX-GP; C2304 SC1U6D3V2KX-GP

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 — VCCCORE

CRT

VCCADAC — U48 — +VCCA_DAC_1_2

(0.1uF/0.01uF x1) (10uF x1_0603)

C2313 SCD01U10V2KX-3GP; C2314 SCD01U10V2KX-5GP; C2315 Do Not Stuff

R2301 Do Not Stuff — 3D3V_S0

R2315 Do Not Stuff — 3D3V_DAC_S0

VSSADAC — U47

UMA_PX_Muxless UMA_PX_Muxless

LVDS

VCCALVDS — AK36 — +3VS_VCCA_LVDS

VSSALVDS — AK37

C2316 SCD01U10V2KX-3GP; C2317 SCD01U10V2KX-3GP; C2318 Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

R2303 Do Not Stuff

0.001A

R2304 0R3J-0-U-GP — 3D3V_S0

UMA_PX_Muxless

VCCTX_LVDS — AM37 AM38 AP36 AP37

0.06A

+1.8VS_VCCTX_LVDS

R2309 Do Not Stuff

R2305 0R5J-5-GP — 1D8V_S0

UMA_PX_Muxless

(0.01uF x2) (22uF x1)

HVCMOS

1D05V_VTT — AN19 — VCCIO

BJ22 — VCCAPLLEXP

1D05V_VTT — 2.925A(Total current of VCCIO) — (1uF x4)

C2306 Do Not Stuff; C2307 SC1U6D3V2KX-GP; C2308 SC1U6D3V2KX-GP; C2309 SC1U6D3V2KX-GP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 — VCCIO

VCC3_3 — V33 V34 — 3D3V_S0

C2319 SCD1U10V2KX-5GP

DMI

VCCVRM — AT16 — VCCVRM_S0

VCCDMI — AT20 — 1D05V_VTT — (1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI — AB36

0.02A

+1.05VS_VCC_DMI_CCI

L2303 IND-10UH-218-GP — 1D05V_VTT

68.10050.10Y

2nd = 68.10090.10B

(1uFx1) (10uFx1)

C2321 SC1U6D3V2KX-GP; C2325 Do Not Stuff

NAND / SPI

VccDFTERM — AG16 AG17 AJ16 AJ17

1D8V_S0 — 0.19A

C2326 SCD1U10V2KX-5GP; C2322 SCD1U10V2KX-5GP

VCCSPI — V1

0.02A — 3D3V_S5 — (1uFx1)

C2323 SC1U6D3V2KX-GP

FDI

0.266A (Totally VCC3_3 current) — 3D3V_S0 — (0.1uF x1)

BH29 — VCC3_3

C2310 SCD1U10V2KX-5GP

0.159A(Totally current of VCCVRM)

VCCVRM_S0 — AP16 — VCCVRM

BG6 — VCCAFDIPLL

1D05V_VTT — AP17 — VCCIO

1D05V_VTT — AU20 — VCCDMI

0.042A (Totally current of VCCDMI)

U2301 — 5V_S0 → 3D3V_DAC_S0

U2301 G9091-330T11U-GP

74.09091.J3F

2nd = 74.09198.G7F

VIN GND EN — VOUT NC#4

C2311 SC1U6D3V2KX-1GP; C2312 SC1U6D3V2KX-GP; C2327 SC1U6D3V3MX-GP

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

U2302 — 3D3V_S0 / 1D5V_S0 → VCCVRM_S0

U2302 G913CF-GP

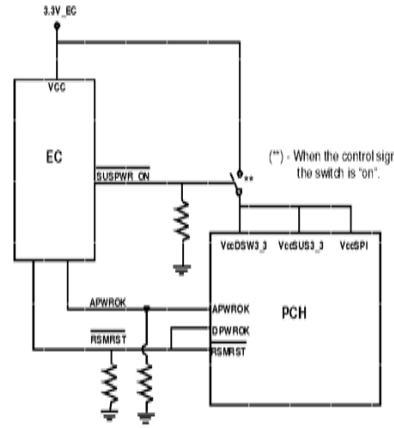
74.00913.A3F

SHDN# GND IN — SET OUT

C2328 SC1U10V3KX-3GP; C2329 SC4D7U6D3V3KX-GP; C2330 SC22P50V2JN-4GP; C2331 SCD1U10V2KX-5GP; R2316 2K8R2F-GP; R2317 10KR2J-3-GP

DY

Refer to NPCE795 shared SPI flash architecture



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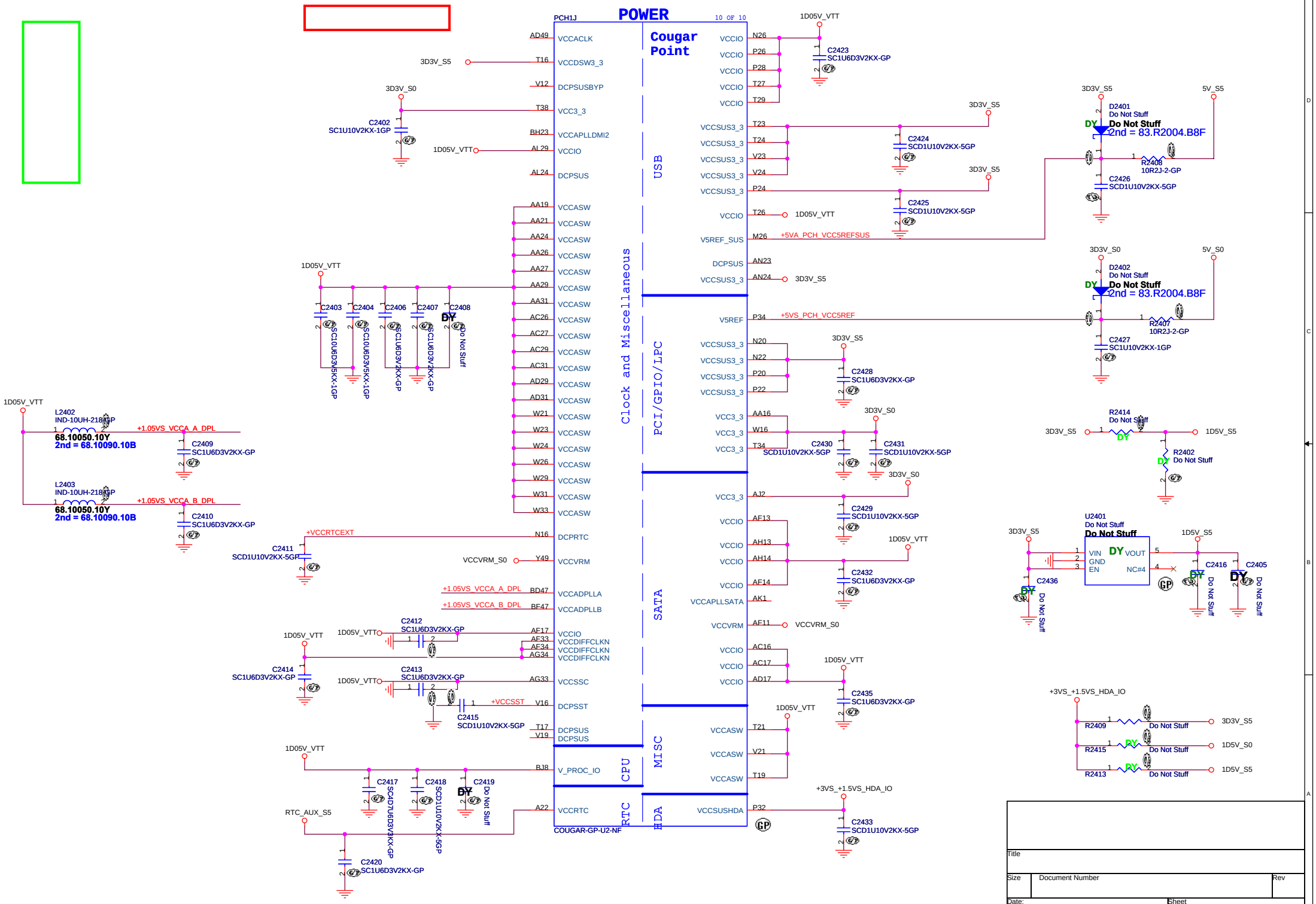
POWER
PCH1J
10 OF 10
Cougar Point
COUGAR-GP-U2-NF
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3
VCCAPLLDMI2
VCCIO
DCPSUS
VCCASW
V5REF_SUS
V5REF
VCCSUS3_3
VCC3_3
VCCADPLLA
VCCADPLLB
VCCVRM
VCCSSC
DCPSST
V_PROC_IO
DCPRTC
VCCAPLLSATA
VCCSUSHDA
1D05V_VTT
3D3V_S5
3D3V_S0
5V_S5
5V_S0
+5VA_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
VCCVRM_S0
RTC_AUX_S5
+3VS_+1.5VS_HDA_IO
L2402
IND-10UH-218MP
68.10050.10Y
2nd = 68.10090.10B
L2403
IND-10UH-218MP
68.10050.10Y
2nd = 68.10090.10B
D2401
D2402
Do Not Stuff
2nd = 83.R2004.B8F
U2401
Do Not Stuff
VIN
GND
EN
VOUT
NC#4
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Document Number
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Date:
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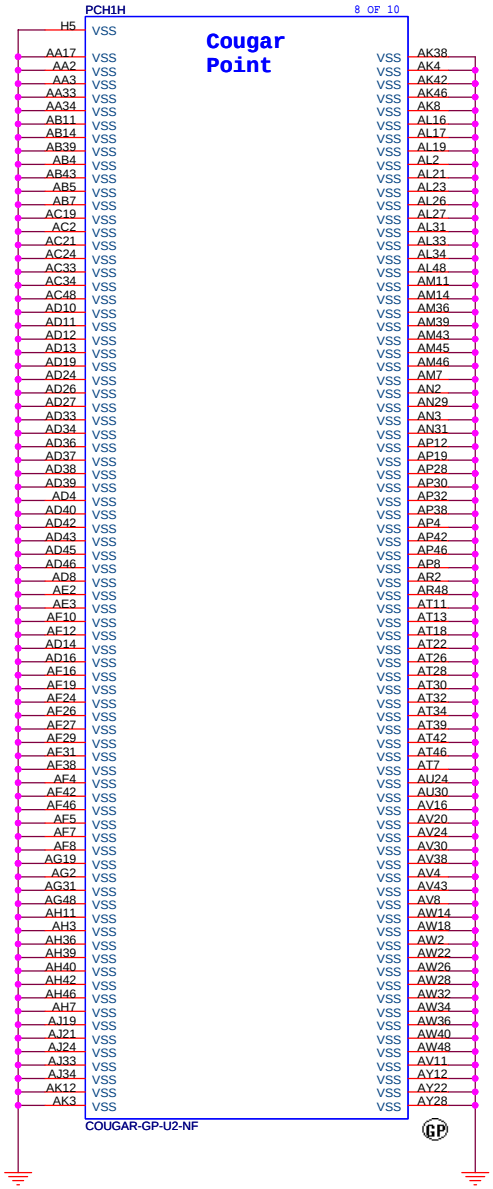

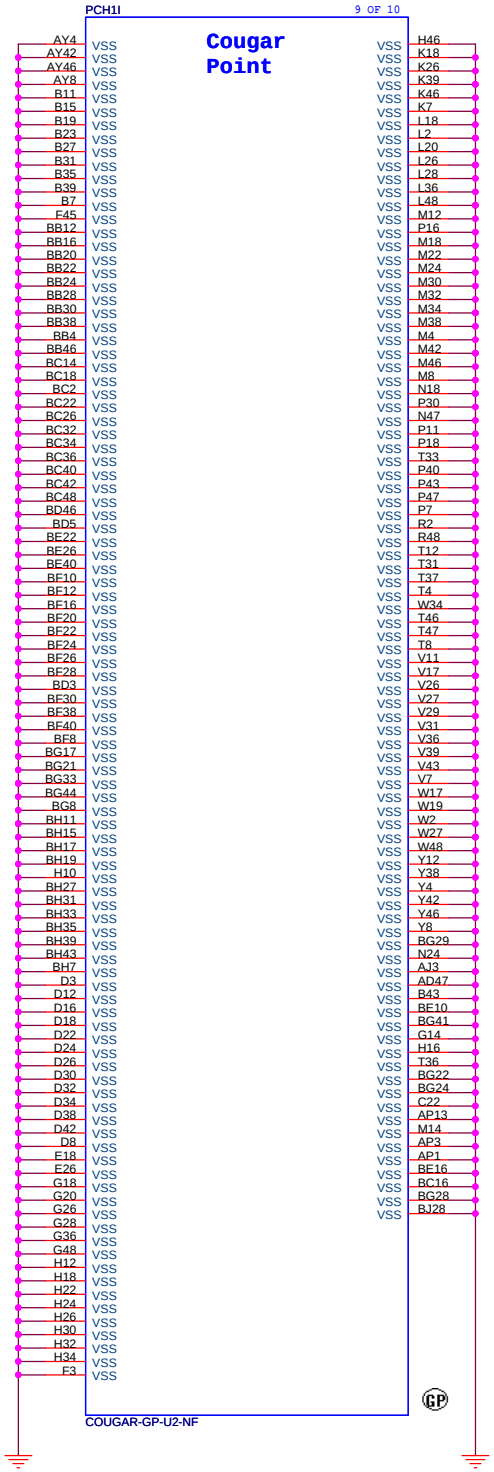

Title		
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Date:	Sheet	

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K		3.0V
SB			2.75V
		47.0K	
		64.9K	
Reserved		76.8	
Reserved			1.65V

PSL SOLUTION
(Power Switch Control Logic)

EC_ENABLE → R2767 Do Not Stuff DY → KBC_ON#_R → RN2706 Do Not Stuff 4-3 1-2 PSL → KBC_ON#_GATE → Q2703 Do Not Stuff 2-3 1-4 PSL → C2713 Do Not Stuff PSL

Q2705 Do Not Stuff 2-3 1-4 PSL

Do Not Stuff
2ND = 84.2N702.031

Do Not Stuff
2ND = 84.03413.A31

R2772 Do Not Stuff

EC_GPIO47 High Active

PROCHOT_EC → R2732 100KR2F-L1-GP → Q2702 2N7002K-2-GP 2-3 1-4 → H_PROCHOT#_EC → R2733 Do Not Stuff → H_PROCHOT# 5,42

Do Not Stuff
84.2N702.J31
2ND = 84.2N702.031

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K		0.55V
120W	33.0K		0.82V
	47.0K		1.06V
	64.9K	100.0K	

ADT_TYPE → R2708 65W 100KR2F-3-GP 2-3 1-4 → R2710 UMA
DISCRETE# → R2709 90W 100KR2F-3-GP 2-3 1-4 → R2739 Do Not Stuff → DIS_PX_Muxless

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

0604 Modify:
Add Pull down 100k ohm at F_SDI for Power consumption concern.

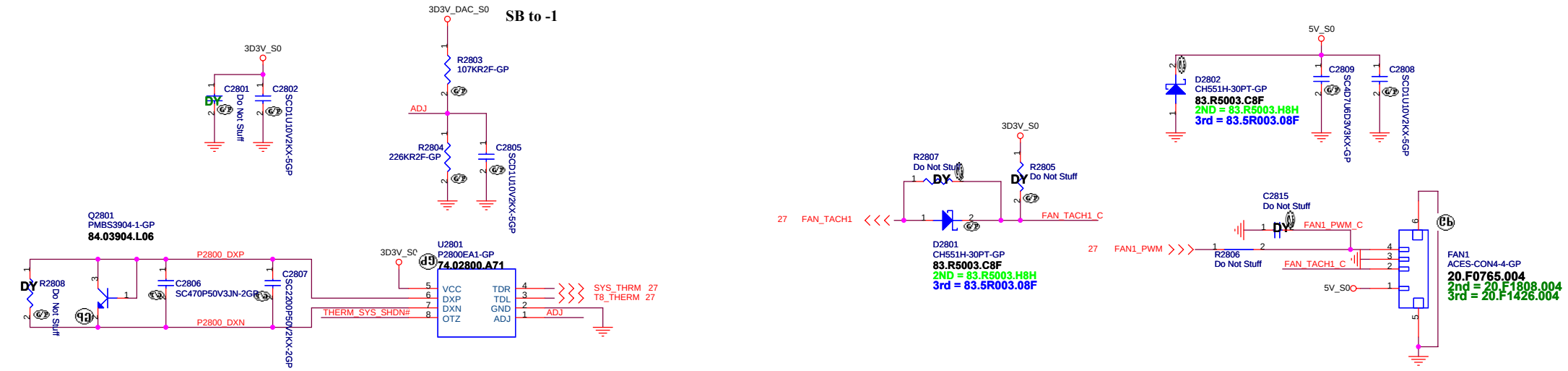
U2701A NPCE795PA0DX-GP-U

U2701B NPCE795PA0DX-GP-U

U2702 Do Not Stuff

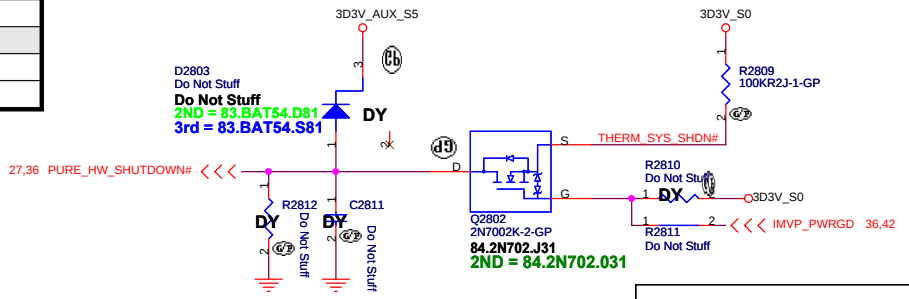
Q2701 MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11

D2701 Do Not Stuff
Do Not Stuff
2nd = 83.BAT54.N81
3nd = 83.00054.T81



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

R_{ADJ1} (KΩ)	R_{ADJ2} (KΩ)	V_{ADJ} (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



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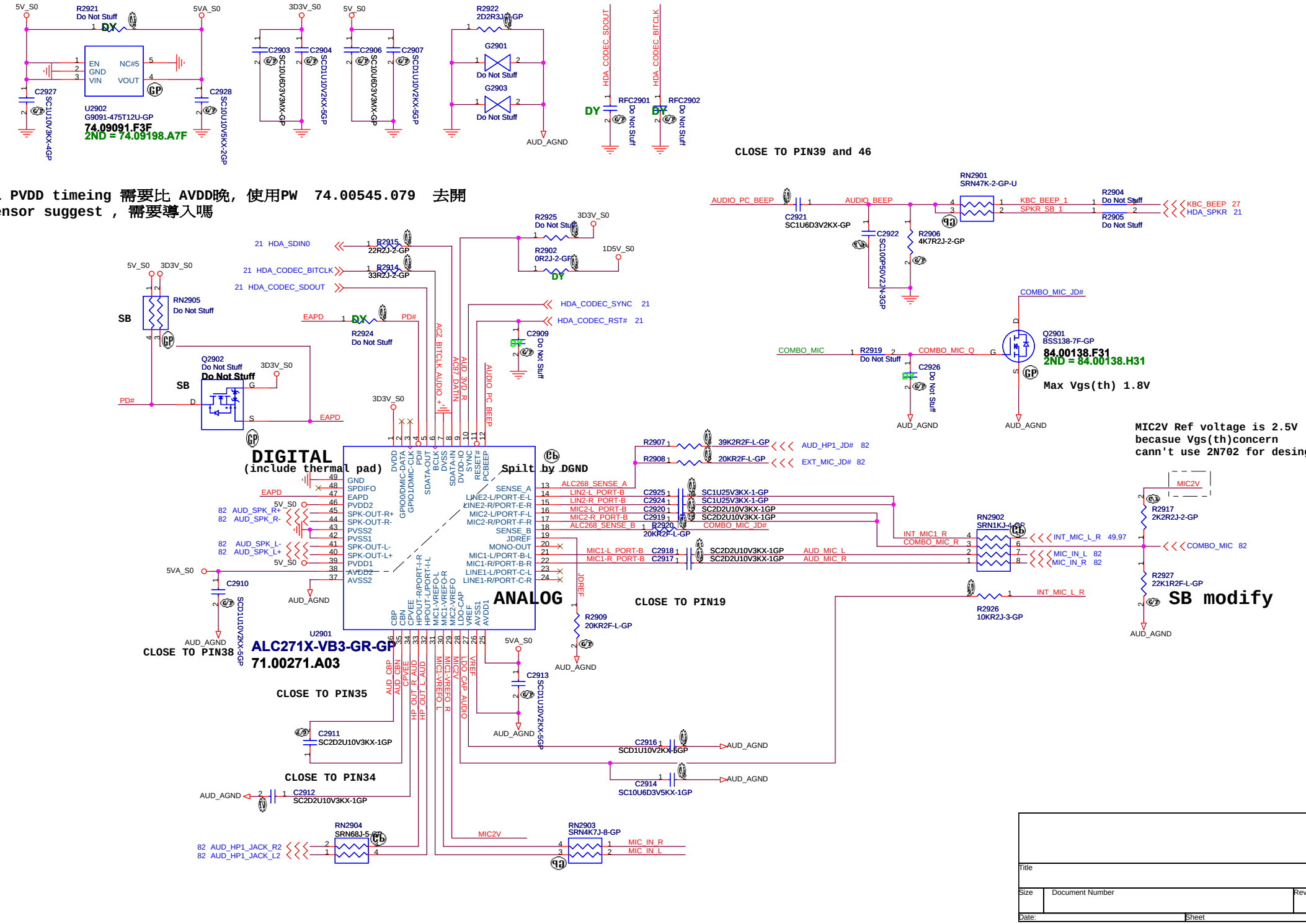
Size | Document Number | Rev

Date: | Sheet


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN39 and 46
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
SB modify
Max Vgs(th) 1.8V
84.00138.F31
2ND = 84.00138.H31
74.09091.F3F
2ND = 74.09198.A7F
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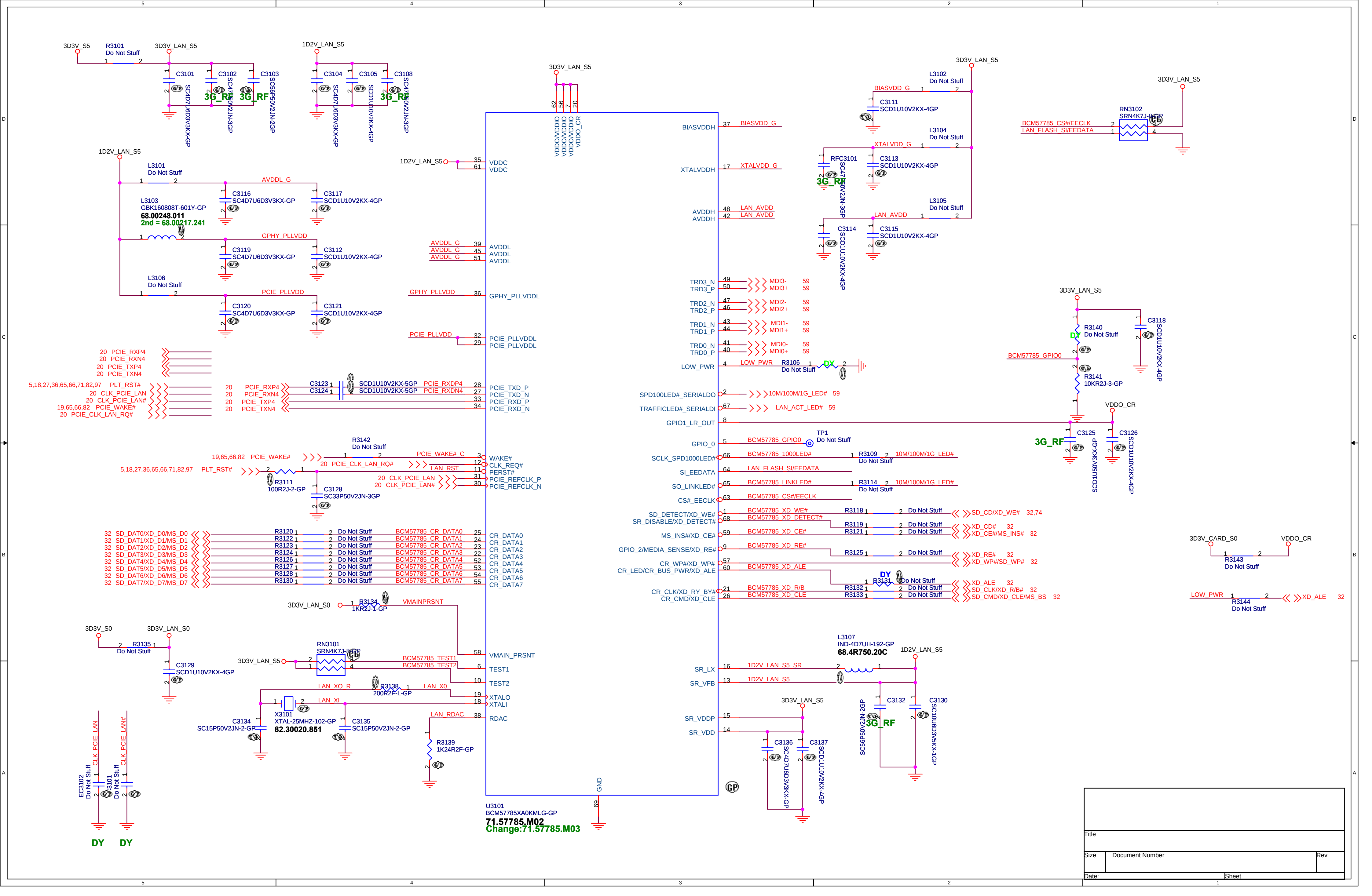

3D3V_S5
R3101
Do Not Stuff
3D3V_LAN_S5
C3101
C3102
C3103
SC4D7U6D3V3KX-GP
SC47P50V2JN-3GP
SC56P50V2JN-2GP
3G_RF
1D2V_LAN_S5
C3104
C3105
C3108
SCD1U10V2KX-4GP
L3101
Do Not Stuff
AVDDL_G
C3116
C3117
L3103
GBK160808T-601Y-GP
68.00248.011
2nd = 68.00217.241
GPHY_PLLVDD
C3119
C3112
L3106
PCIE_PLLVDD
C3120
C3121
20 PCIE_RXP4
20 PCIE_RXN4
20 PCIE_TXP4
20 PCIE_TXN4
5,18,27,36,65,66,71,82,97 PLT_RST#
20 CLK_PCIE_LAN
20 CLK_PCIE_LAN#
19,65,66,82 PCIE_WAKE#
20 PCIE_CLK_LAN_RQ#
C3123
C3124
SCD1U10V2KX-5GP
PCIE_RXDP4
PCIE_RXDN4
R3142
Do Not Stuff
PCIE_WAKE#_C
LAN_RST
R3111
100R2J-2-GP
C3128
SC33P50V2JN-3GP
32 SD_DAT0/XD_D0/MS_D0
32 SD_DAT1/XD_D1/MS_D1
32 SD_DAT2/XD_D2/MS_D2
32 SD_DAT3/XD_D3/MS_D3
32 SD_DAT4/XD_D4/MS_D4
32 SD_DAT5/XD_D5/MS_D5
32 SD_DAT6/XD_D6/MS_D6
32 SD_DAT7/XD_D7/MS_D7
R3120 R3122 R3123 R3124 R3126 R3127 R3128 R3130
BCM57785_CR_DATA0 … BCM57785_CR_DATA7
3D3V_LAN_S0
R3134
1KR2J-1-GP
VMAINPRSNT
3D3V_S0
R3135
C3129
RN3101
SRN4K7J-8-GP
BCM57785_TEST1
BCM57785_TEST2
LAN_XO_R
R3138
200R2F-L-GP
LAN_X0
LAN_XI
X3101
XTAL-25MHZ-102-GP
82.30020.851
C3134
SC15P50V2JN-2-GP
C3135
SC15P50V2JN-2-GP
LAN_RDAC
R3139
1K24R2F-GP
EC3102
EC3101
Do Not Stuff
CLK_PCIE_LAN
CLK_PCIE_LAN#
DY
VDDO/VDDIO
VDDO_CR
VDDC
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
CLK_REQ#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
CR_DATA0 … CR_DATA7
VMAIN_PRSNT
TEST1
TEST2
XTALO
XTALI
RDAC
GND
U3101
BCM57785XA0KMLG-GP
71.57785.M02
Change:71.57785.M03
BIASVDDH
XTALVDDH
AVDDH
TRD3_N TRD3_P TRD2_N TRD2_P TRD1_N TRD1_P TRD0_N TRD0_P
MDI3- MDI3+ MDI2- MDI2+ MDI1- MDI1+ MDI0- MDI0+ 59
LOW_PWR
R3106
SPD100LED#_SERIALDO
TRAFFICLED#_SERIALDI
10M/100M/1G_LED# 59
LAN_ACT_LED# 59
GPIO1_LR_OUT
GPIO_0
TP1
BCM57785_GPIO0
SCLK_SPD1000LED#
BCM57785_1000LED#
R3109
SI_EEDATA
LAN_FLASH_SI/EEDATA
SO_LINKLED#
BCM57785_LINKLED#
R3114
CS#_EECLK
BCM57785_CS#/EECLK
SD_DETECT/XD_WE#
SR_DISABLE/XD_DETECT#
MS_INS#/XD_CE#
GPIO_2/MEDIA_SENSE/XD_RE#
CR_WP#/XD_WP#
CR_LED/CR_BUS_PWR/XD_ALE
CR_CLK/XD_RY_BY#
CR_CMD/XD_CLE
BCM57785_XD_WE#
BCM57785_XD_DETECT#
BCM57785_XD_CE#
BCM57785_XD_RE#
BCM57785_XD_ALE
BCM57785_XD_R/B
BCM57785_XD_CLE
R3118 R3119 R3121 R3125 R3131 R3132 R3133
SD_CD/XD_WE# 32,74
XD_CD# 32
XD_CE#/MS_INS# 32
XD_RE# 32
XD_WP#/SD_WP# 32
XD_ALE 32
SD_CLK/XD_R/B# 32
SD_CMD/XD_CLE/MS_BS 32
SR_LX
SR_VFB
SR_VDDP
SR_VDD
1D2V_LAN_S5_SR
L3107
IND-4D7UH-192-GP
68.4R750.20C
C3132
C3130
SC10U6D3V5KX-1GP
C3136
C3137
L3102
BIASVDD_G
C3111
L3104
XTALVDD_G
RFC3101
C3113
L3105
LAN_AVDD
C3114
C3115
RN3102
SRN4K7J-8-GP
3D3V_LAN_S5
R3140
R3141
10KR2J-3-GP
C3118
BCM57785_GPIO0
VDDO_CR
C3125
C3126
SCD1U50V3KX-GP
3D3V_CARD_S0
R3143
R3144
XD_ALE 32
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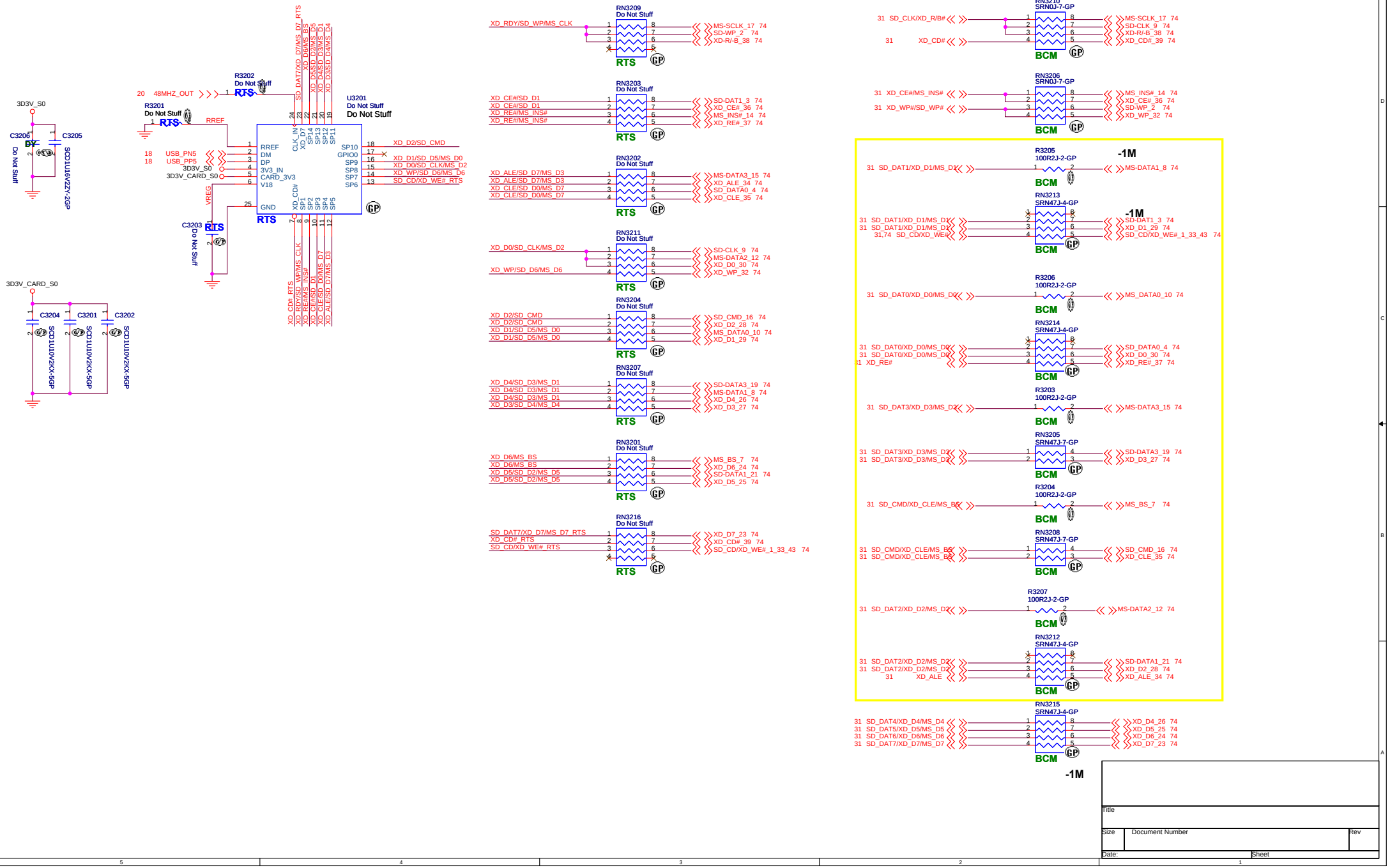
3D3V_S0
C3206
DY
C3205
SCD1U16V2ZY-2GP
Do Not Stuff
3D3V_CARD_S0
C3204
C3201
C3202
SCD1U10V2KX-5GP
R3202
Do Not Stuff
R3201
Do Not Stuff
RTS
20 48MHZ_OUT
RREF
VREG
C3203
Do Not Stuff
U3201
Do Not Stuff
Do Not Stuff
RREF
DM
DP
3V3_IN
CARD_3V3
V18
GND
CLK_IN
XD_CD#
SP0
SP1
SP2
SP3
SP4
SP5
SP6
SP7
SP8
SP9
SP10
SP11
SP12
SP13
SP14
GPIO0
18 USB_PN5
18 USB_PP5
3D3V_S0
3D3V_CARD_S0
XD_D2/SD_CMD
XD_D1/SD_D5/MS_D0
XD_D0/SD_CLK/MS_D2
XD_WP/SD_D6/MS_D6
SD_CD/XD_WE#_RTS
SD_DAT7/XD_D7/MS_D7_RTS
XD_D6/MS_BS
XD_D5/SD_D2/MS_D5
XD_D4/SD_D3/MS_D1
XD_D3/SD_D4/MS_D4
XD_CD#_RTS
XD_RDY/SD_WP/MS_CLK
XD_RE#/MS_INS#
XD_CE#/SD_D1/MS_D7
XD_CLE/SD_D0/MS_D3
XD_ALE/SD_D7/MS_D3
RN3209
Do Not Stuff
XD_RDY/SD_WP/MS_CLK
MS-SCLK_17 74
SD-WP_2 74
XD-R/-B_38 74
RN3203
Do Not Stuff
XD_CE#/SD_D1
XD_CE#/SD_D1
XD_RE#/MS_INS#
XD_RE#/MS_INS#
SD-DAT1_3 74
XD_CE#_36 74
MS_INS#_14 74
XD_RE#_37 74
RN3202
Do Not Stuff
XD_ALE/SD_D7/MS_D3
XD_ALE/SD_D7/MS_D3
XD_CLE/SD_D0/MS_D7
XD_CLE/SD_D0/MS_D7
MS-DATA3_15 74
XD_ALE_34 74
SD_DATA0_4 74
XD_CLE_35 74
RN3211
Do Not Stuff
XD_D0/SD_CLK/MS_D2
XD_WP/SD_D6/MS_D6
SD-CLK_9 74
MS-DATA2_12 74
XD_D0_30 74
XD_WP_32 74
RN3204
Do Not Stuff
XD_D2/SD_CMD
XD_D2/SD_CMD
XD_D1/SD_D5/MS_D0
XD_D1/SD_D5/MS_D0
SD_CMD_16 74
XD_D2_28 74
MS_DATA0_10 74
XD_D1_29 74
RN3207
Do Not Stuff
XD_D4/SD_D3/MS_D1
XD_D4/SD_D3/MS_D1
XD_D4/SD_D3/MS_D1
XD_D3/SD_D4/MS_D4
SD-DATA3_19 74
MS-DATA1_8 74
XD_D4_26 74
XD_D3_27 74
RN3201
Do Not Stuff
XD_D6/MS_BS
XD_D6/MS_BS
XD_D5/SD_D2/MS_D5
XD_D5/SD_D2/MS_D5
MS_BS_7 74
XD_D6_24 74
SD-DATA1_21 74
XD_D5_25 74
RN3216
Do Not Stuff
SD_DAT7/XD_D7/MS_D7_RTS
XD_CD#_RTS
SD_CD/XD_WE#_RTS
XD_D7_23 74
XD_CD#_39 74
SD_CD/XD_WE#_1_33_43 74
RTS
GP
RN3210
SRN0J-7-GP
31 SD_CLK/XD_R/B#
31 XD_CD#
MS-SCLK_17 74
SD-CLK_9 74
XD-R/-B_38 74
XD_CD#_39 74
BCM
RN3206
SRN0J-7-GP
31 XD_CE#/MS_INS#
31 XD_WP#/SD_WP#
MS_INS#_14 74
XD_CE#_36 74
SD-WP_2 74
XD_WP_32 74
-1M
R3205
100R2J-2-GP
31 SD_DAT1/XD_D1/MS_D1
MS-DATA1_8 74
RN3213
SRN47J-4-GP
31 SD_DAT1/XD_D1/MS_D1
31 SD_DAT1/XD_D1/MS_D1
31,74 SD_CD/XD_WE#
SD-DAT1_3 74
XD_D1_29 74
SD_CD/XD_WE#_1_33_43 74
R3206
100R2J-2-GP
31 SD_DAT0/XD_D0/MS_D0
MS_DATA0_10 74
RN3214
SRN47J-4-GP
31 SD_DAT0/XD_D0/MS_D0
31 SD_DAT0/XD_D0/MS_D0
31 XD_RE#
SD_DATA0_4 74
XD_D0_30 74
XD_RE#_37 74
R3203
100R2J-2-GP
31 SD_DAT3/XD_D3/MS_D3
MS-DATA3_15 74
RN3205
SRN47J-7-GP
31 SD_DAT3/XD_D3/MS_D3
31 SD_DAT3/XD_D3/MS_D3
SD-DATA3_19 74
XD_D3_27 74
R3204
100R2J-2-GP
31 SD_CMD/XD_CLE/MS_B
MS_BS_7 74
RN3208
SRN47J-7-GP
31 SD_CMD/XD_CLE/MS_B
31 SD_CMD/XD_CLE/MS_B
SD_CMD_16 74
XD_CLE_35 74
R3207
100R2J-2-GP
31 SD_DAT2/XD_D2/MS_D2
MS-DATA2_12 74
RN3212
SRN47J-4-GP
31 SD_DAT2/XD_D2/MS_D2
31 SD_DAT2/XD_D2/MS_D2
31 XD_ALE
SD-DATA1_21 74
XD_D2_28 74
XD_ALE_34 74
RN3215
SRN47J-4-GP
31 SD_DAT4/XD_D4/MS_D4
31 SD_DAT5/XD_D5/MS_D5
31 SD_DAT6/XD_D6/MS_D6
31 SD_DAT7/XD_D7/MS_D7
XD_D4_26 74
XD_D5_25 74
XD_D6_24 74
XD_D7_23 74
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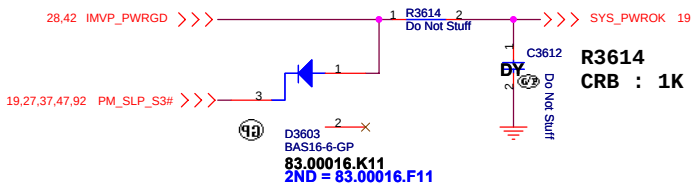
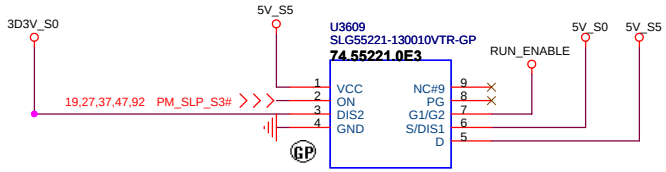
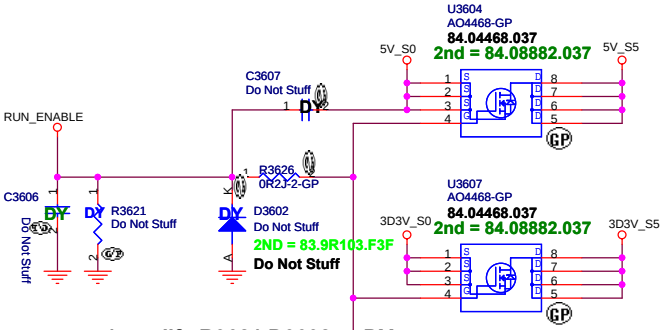
Power Sequence



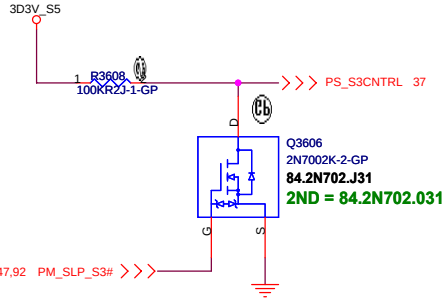
R3614
CRB : 1K

ANNIE Run Power



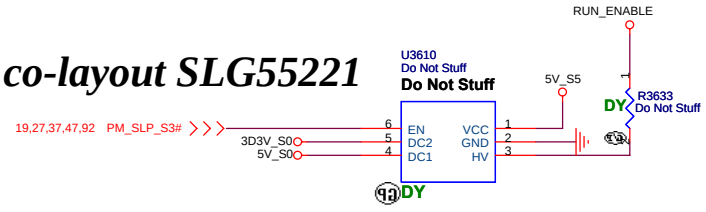


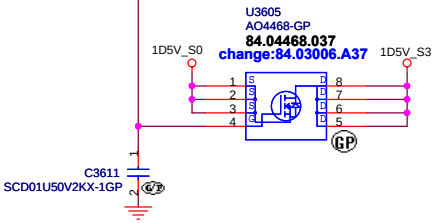
-1 modify R3621,D3602 to DY



SB modify part number

-1 co-layout SLG55221

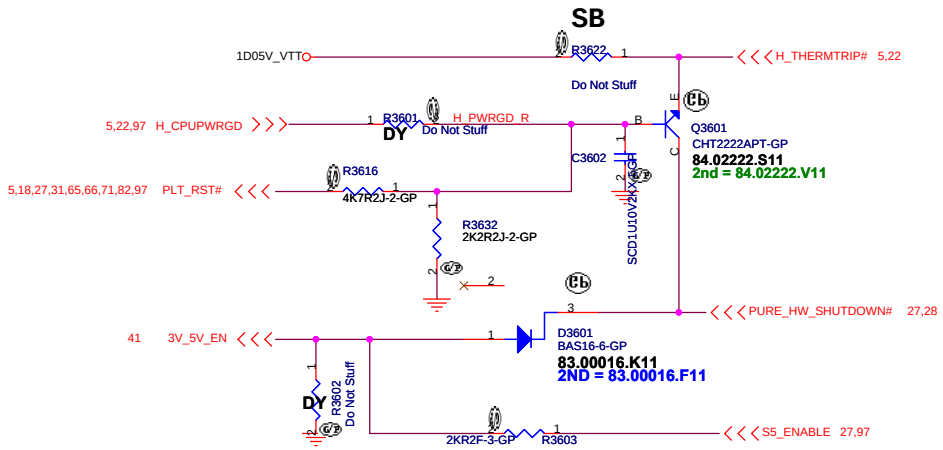




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



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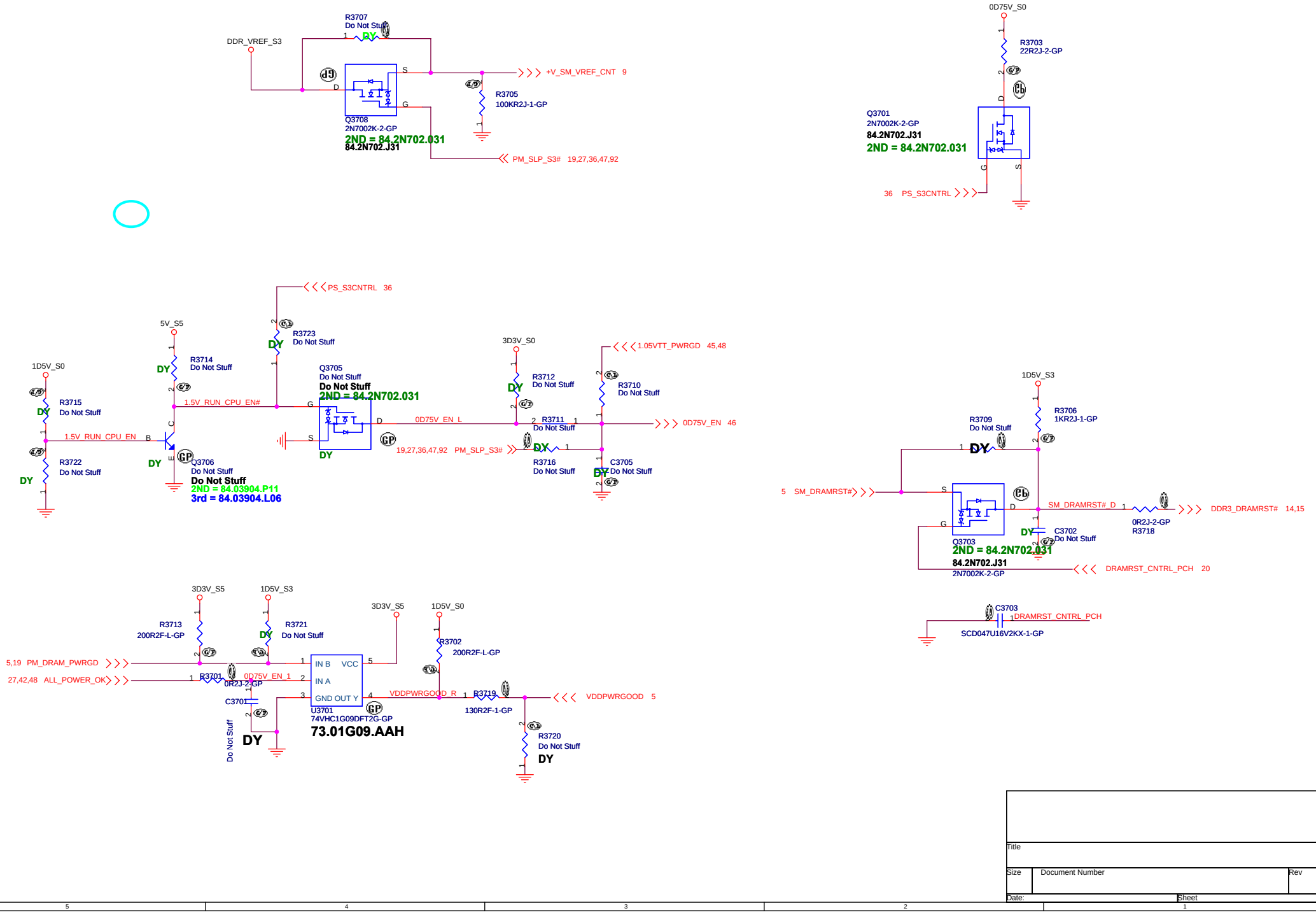

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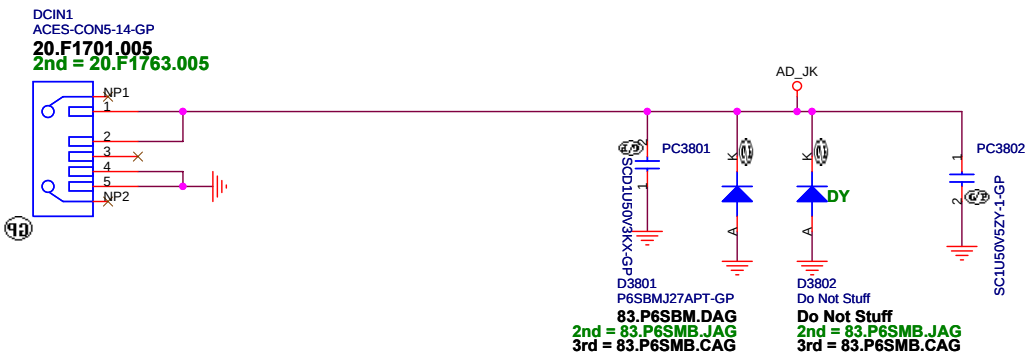

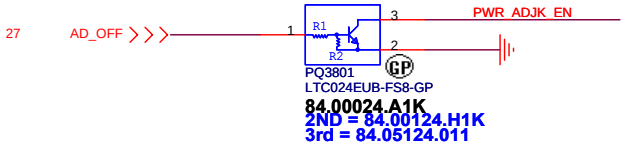

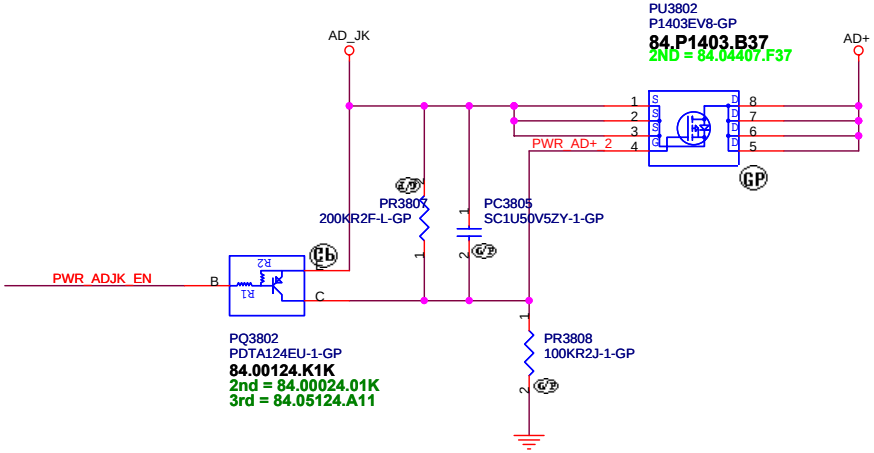

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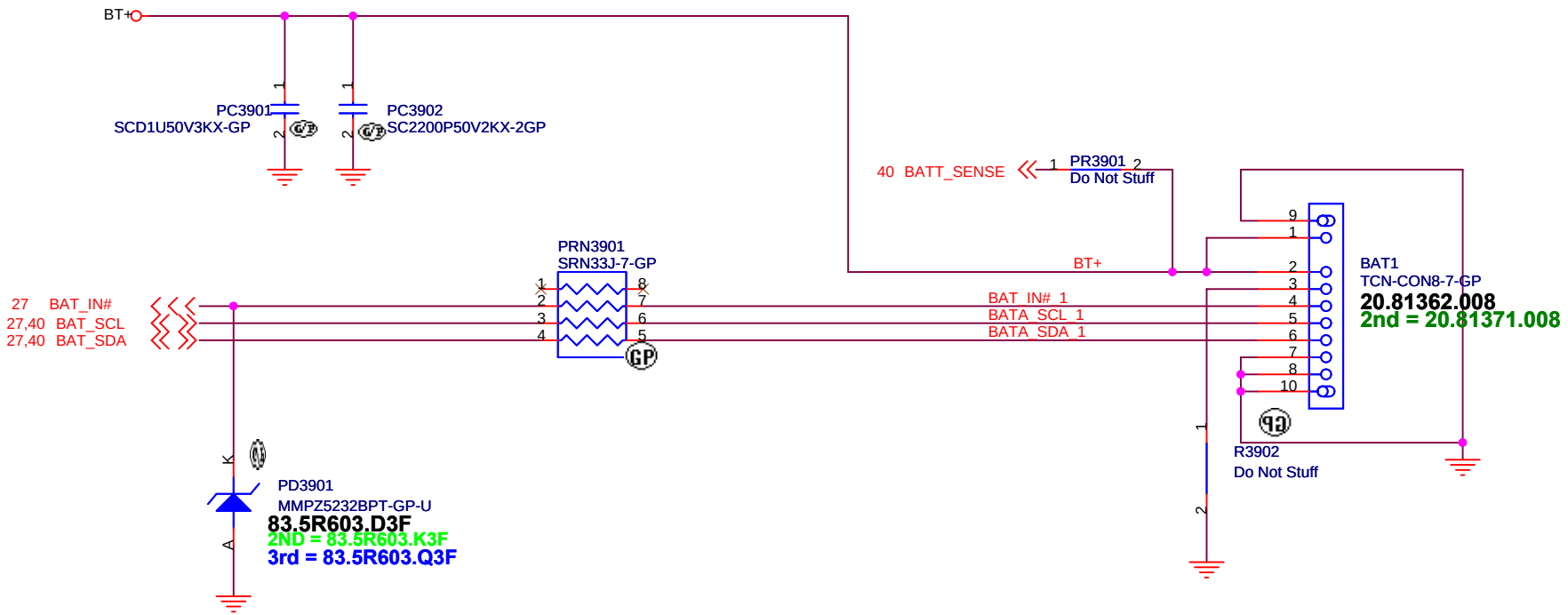

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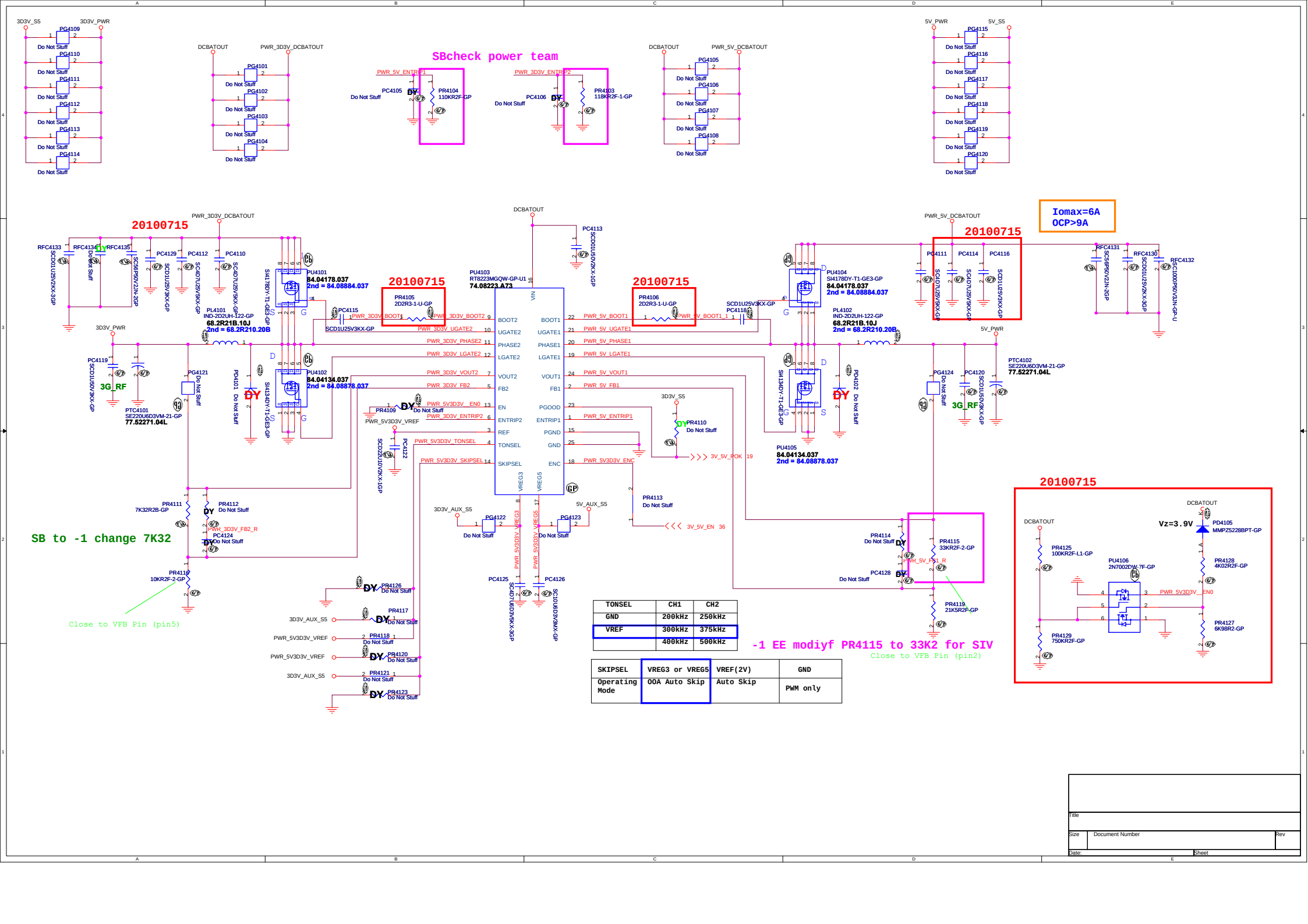
AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

20100706 Wayne

20101018

-1M

-1M



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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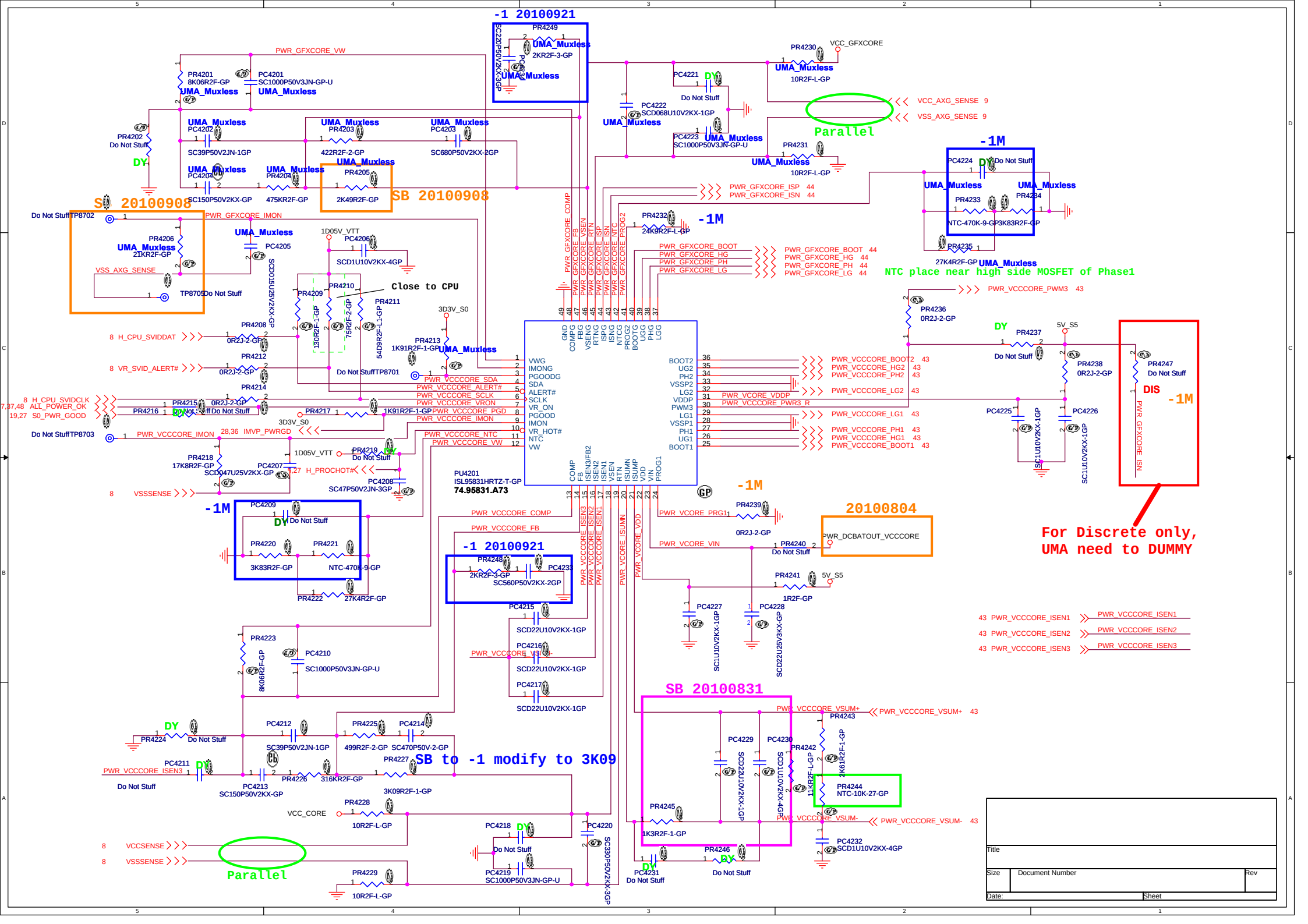
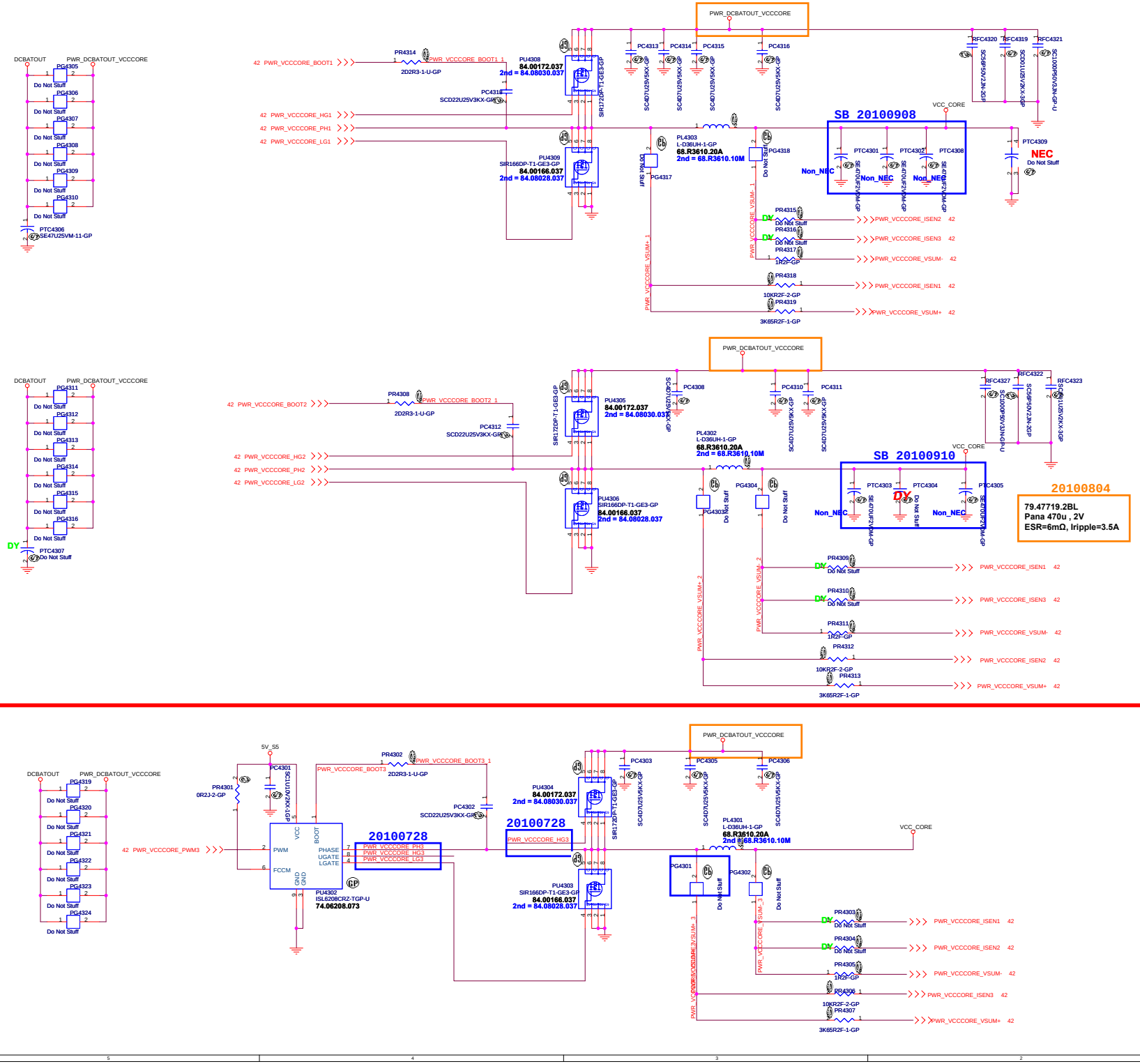

-1 20100921
SB 20100908
-1M
Parallel
NTC place near high side MOSFET of Phase1
Close to CPU
20100804
For Discrete only,
UMA need to DUMMY
SB 20100831
SB to -1 modify to 3K09
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
PWR_GFXCORE_VW
VCC_GFXCORE
VCC_AXG_SENSE 9
VSS_AXG_SENSE 9
PWR_GFXCORE_IMON
PWR_GFXCORE_ISP 44
PWR_GFXCORE_ISN 44
PWR_GFXCORE_BOOT 44
PWR_GFXCORE_HG 44
PWR_GFXCORE_PH 44
PWR_GFXCORE_LG 44
PWR_VCCCORE_PWM3 43
PWR_VCCCORE_BOOT2 43
PWR_VCCCORE_HG2 43
PWR_VCCCORE_PH2 43
PWR_VCCCORE_LG2 43
PWR_VCCCORE_LG1 43
PWR_VCCCORE_PH1 43
PWR_VCCCORE_HG1 43
PWR_VCCCORE_BOOT1 43
PWR_VCCCORE_VSUM+ 43
PWR_VCCCORE_VSUM- 43
PWR_VCCCORE_ISEN1 43
PWR_VCCCORE_ISEN2 43
PWR_VCCCORE_ISEN3 43
PWR_DCBATOUT_VCCCORE
VCC_CORE
VCCSENSE 8
VSSSENSE 8
H_CPU_SVIDDAT 8
VR_SVID_ALERT# 8
H_CPU_SVIDCLK 8
ALL_POWER_OK 7,37,48
S0_PWR_GOOD 19,27
IMVP_PWRGD 28,36
H_PROCHOT# 9,27
Do Not Stuff
DY
UMA_Muxless


PWR_DCBATOUT_VCCCORE
DCBATOUT
PG4305
PG4306
PG4307
PG4308
PG4309
PG4310
Do Not Stuff
PTC4306
SE47U25VM-11-GP
PR4314
2D2R3-1-U-GP
PU4308
84.00172.037
2nd = 84.08030.037
SIR172DP-T1-GE3-GP
PC4318
SCD22U25V3KX-GP
PC4313
PC4314
PC4315
PC4316
SC4D7U25V5KX-GP
RFC4320
RFC4319
RFC4321
SC5R6P50V2JN-GP
SCD01U25V3KX-3GP
SC010P50V3JN-GP-U
VCC_CORE
SB 20100908
PTC4301
PTC4302
PTC4308
SE220U2VAM-GP
Non_NEC
PTC4309
NEC
PL4303
L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.10M
PG4317
PG4318
PR4315
PR4316
PR4317
1K2F-GP
PR4318
10KR2F-2-GP
PR4319
3K65R2F-1-GP
PWR_VCCCORE_VSUM- 1
PWR_VCCCORE_VSUM+ 1
PWR_VCCCORE_ISEN2 42
PWR_VCCCORE_ISEN3 42
PWR_VCCCORE_VSUM- 42
PWR_VCCCORE_ISEN1 42
PWR_VCCCORE_VSUM+ 42
42 PWR_VCCCORE_BOOT1
42 PWR_VCCCORE_HG1
42 PWR_VCCCORE_PH1
42 PWR_VCCCORE_LG1
PWR_VCCCORE_BOOT1_1
PU4309
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
DY
Do Not Stuff
PWR_DCBATOUT_VCCCORE
DCBATOUT
PG4311
PG4312
PG4313
PG4314
PG4315
PG4316
PTC4307
PR4308
2D2R3-1-U-GP
PU4305
84.00172.037
2nd = 84.08030.037
PC4312
SCD22U25V3KX-GP
PC4308
PC4310
PC4311
RFC4322
RFC4327
RFC4323
SC5R6P50V2JN-3SP
SCD01U25V2KX-3GP
SC010P50V3JN-GP-U
PL4302
L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.10M
PG4303
PG4304
VCC_CORE
SB 20100910
PTC4303
PTC4304
PTC4305
SE470U2FVAM-GP
Non_NEC
20100804
79.47719.2BL
Pana 470u , 2V
ESR=6mΩ, Iripple=3.5A
PR4309
PR4310
PR4311
1K2F-GP
PR4312
10KR2F-2-GP
PR4313
3K65R2F-1-GP
PWR_VCCCORE_VSUM- 2
PWR_VCCCORE_VSUM+ 2
PWR_VCCCORE_ISEN1 42
PWR_VCCCORE_ISEN3 42
PWR_VCCCORE_VSUM- 42
PWR_VCCCORE_ISEN2 42
PWR_VCCCORE_VSUM+ 42
42 PWR_VCCCORE_BOOT2
42 PWR_VCCCORE_HG2
42 PWR_VCCCORE_PH2
42 PWR_VCCCORE_LG2
PWR_VCCCORE_BOOT2_1
PU4306
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
DY
Do Not Stuff
PWR_DCBATOUT_VCCCORE
DCBATOUT
PG4319
PG4320
PG4321
PG4322
PG4323
PG4324
Do Not Stuff
5V_S5
PC4301
PR4301
0R2J-2-GP
PR4302
2D2R3-1-U-GP
PWR_VCCCORE_BOOT3_1
PC4302
SCD22U25V3KX-GP
PU4302
ISL6208CRZ-TGP-U
74.06208.073
PWM
FCCM
PHASE
UGATE
LGATE
VCC
BOOT
GND
20100728
PWR_VCCCORE_PH3
PWR_VCCCORE_HG3
PWR_VCCCORE_LG3
42 PWR_VCCCORE_PWM3
PU4304
84.00172.037
2nd = 84.08030.037
PC4303
PC4305
PC4306
SC4D7U25V5KX-GP
PU4303
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
PL4301
L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.10M
PG4301
PG4302
VCC_CORE
PR4303
PR4304
PR4305
1K2F-GP
PR4306
10KR2F-2-GP
PR4307
3K65R2F-1-GP
PWR_VCCCORE_VSUM- 3
PWR_VCCCORE_VSUM+ 3
PWR_VCCCORE_ISEN1 42
PWR_VCCCORE_ISEN2 42
PWR_VCCCORE_VSUM- 42
PWR_VCCCORE_ISEN3 42
PWR_VCCCORE_VSUM+ 42
Title
Size
Document Number
Rev
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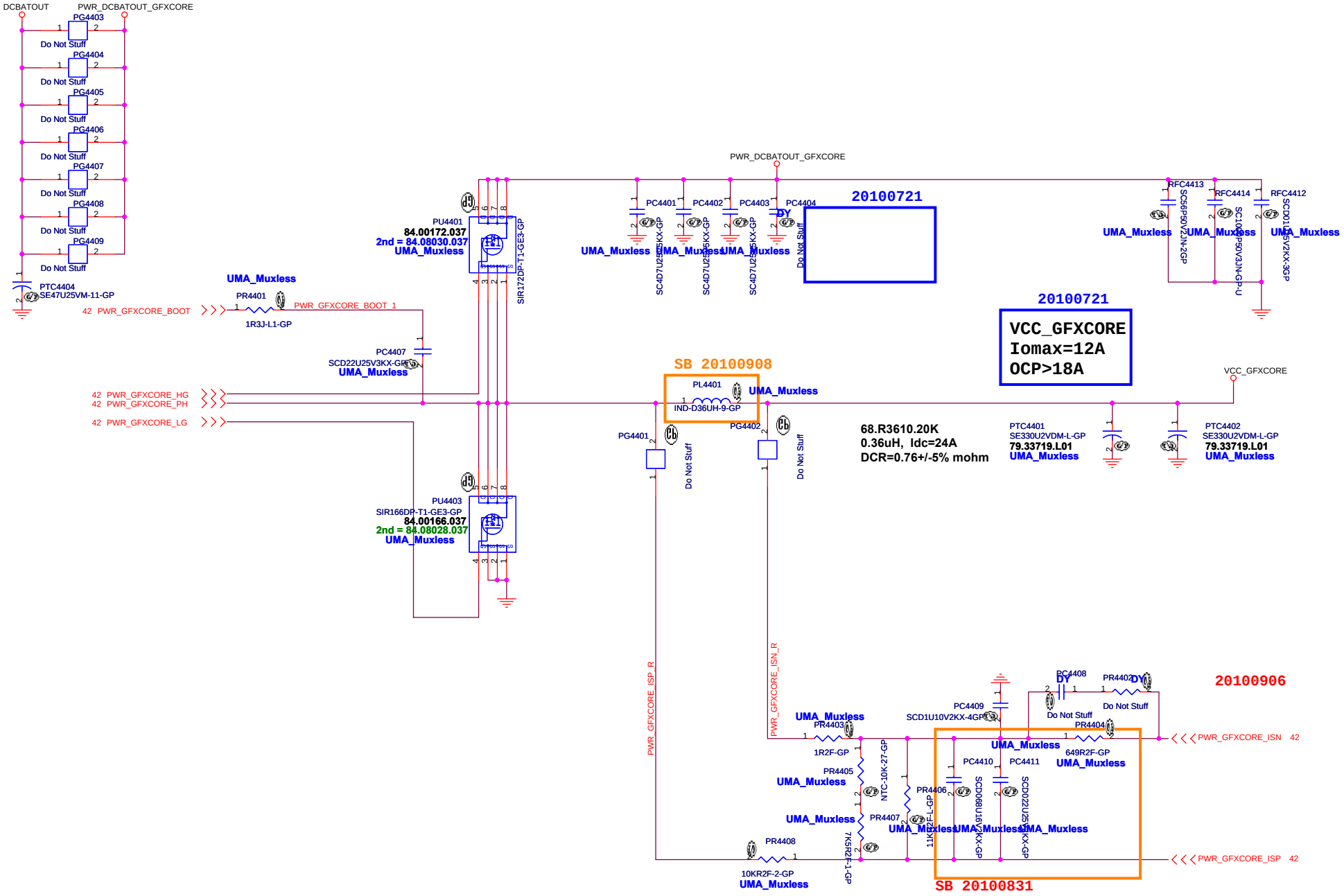

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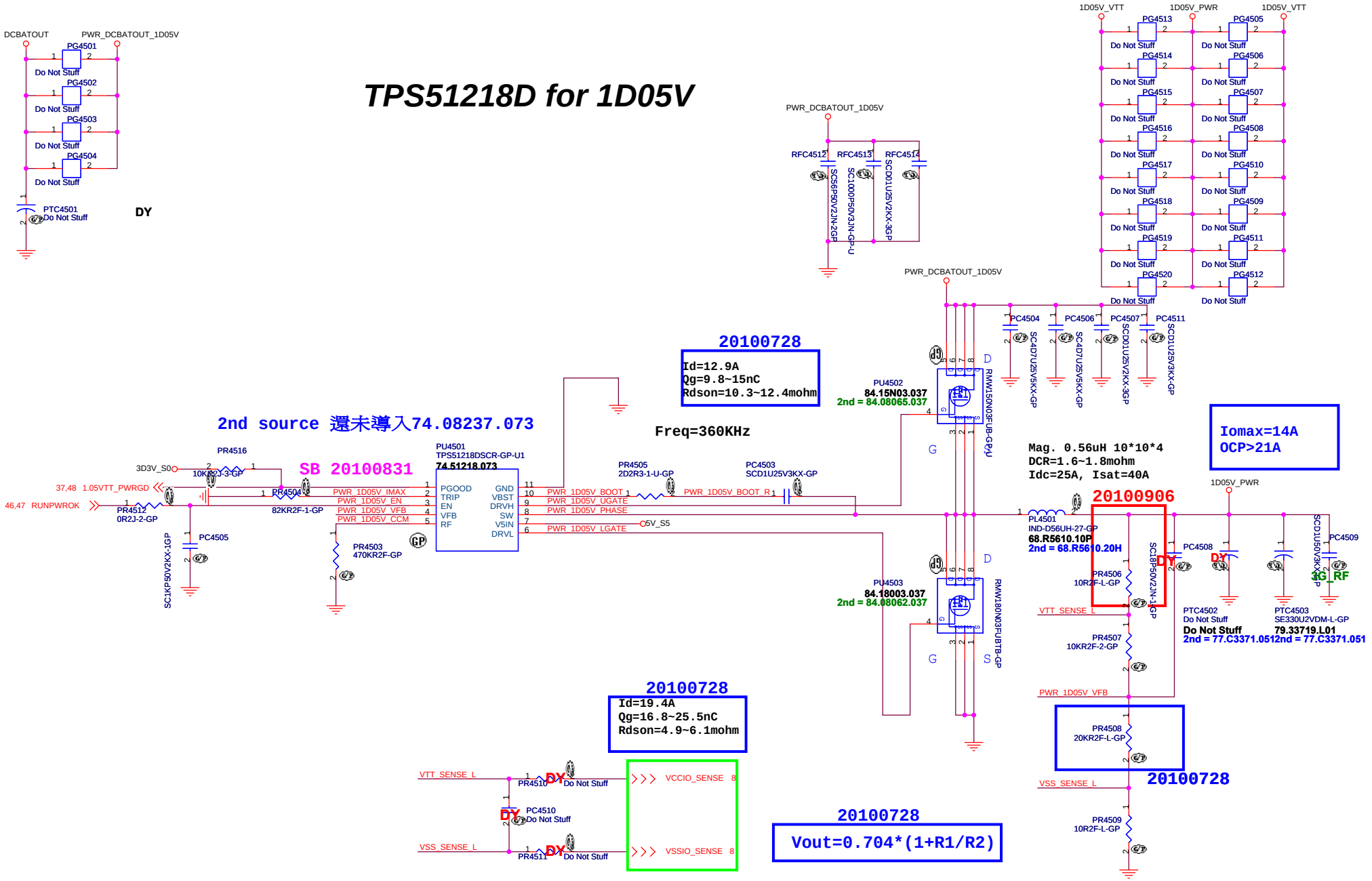
TPS51218D for 1D05V



Title			
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Date:		Sheet	

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V

20100805

20100831 SB

20100728

Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

20100906

20100728

20100728

DCBATOUT
PWR_DCBATOUT_1D5V
PG4601
PG4602
PG4603
PG4604
Do Not Stuff
PTC4601
DY

19,27 PM_SLP_S4#
PR4612
PWR_1D5V_EN
PC4612
DY

3D3V_S5
PR4602
10KR2F-2-GP
Close to pin23

45,47 RUNPWROK
PWR_DCBATOUT_1D5V
PR4610
620KR2F-GP
PWR_1D5V_TON
PWR_1D5V_EN
PWR_0D75V_EN
PWR_1D5V_VTTIN
1D5V_S3
PG4605
PG4606
PC4603
SC10U6D3V5MX-3GP
PG4607
DDR_VREF_PWR
Close to pin23

PWR_1D5V_VCC5
PR4604
5D1R2F-GP
5V_S5
PC4606
SC1U10V2KX-1GP
PC4602
SC1K50V2KX-1GP
PR4603
12K4R2F-GP
PWR_1D5V_VDDP
PR4605
C694
SC1U10V2KX-1GP
PWR_1D5V_CS

CS
VDD
VDDP
PGOOD
TON
S5
S3
VLDOIN
NC#7
VTTGND
MODE
VTT
VTTSNS
GND
BOOT
UGATE
PHASE
LGATE
PGND
NC#17
VDDQ
FB
DEM
VTTREF

PWR_1D5V_BOOT
PWR_1D5V_UGATE
PWR_1D5V_PHASE
PWR_1D5V_LGATE
PWR_1D5V_VDDQ
PWR_1D5V_FB
5V_S5

PR4606
2D2R3-1-U-GP
PWR_1D5V_PHASE_L
PC4609
SCD1U25V3KX-GP

PU4601
RT8207LGQW-GP-U1
74.08207.B73

-1 PR4608 需要將來都改32K4F,將

R1
PR4608
33KR2F-GP
DY
PC4610
Do Not Stuff

R2
PR4609
30KR2F-GP

PR4607
Do Not Stuff
DDR_VREF_S3
PWR_1D5V_VTTREF
PC4608
SCD033U16V2KX-GP

Close to output cap pin1, not inside of the output cap
2nd source 還未導入74.51116.073
Close to PIN9

+0.75VS
Iomax: 1.2A

37 0D75V_EN
PR4615
PWR_0D75V_EN

0D75V_S0
PG4608
PG4609
DDR_VREF_PWR
PC4604
PC4605
SC10U6D3V5MX-3GP
DY

PWR_DCBATOUT_1D5V
RFC4617
RFC4618
RFC4616
SC1U25V2KX-3GP
SC1000P50V3JN-GP-U
SC5P50V2JN-2GP

PU4602
84.15N03.037
2nd = 84.08065.037
RMW150N03FUB-GP-U1

PU4603
84.18003.037
2nd = 84.18002.037
RMW180N03FUBTB-GP

PC4611
PC4614
PC4616
PC4617
PC4615
SC4D7U25V5KX-GP
SCD1U25V3KX-GP

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A
Iomax=12A
OCP>20A

1D5V_S3
PL4601
IND-1UH-93-GP
68.1R01B.10J
2nd = 68.1R01C.10Q
PC4613
DY
PTC4602
SE390U2D5VM-7GP
79.3971V.30L
2nd = 79.3971V.6AL
Matsuki cap 390uF
2.5V, ESR=10mohm

Vout=0.75*(1+R1/R2)

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

Title		
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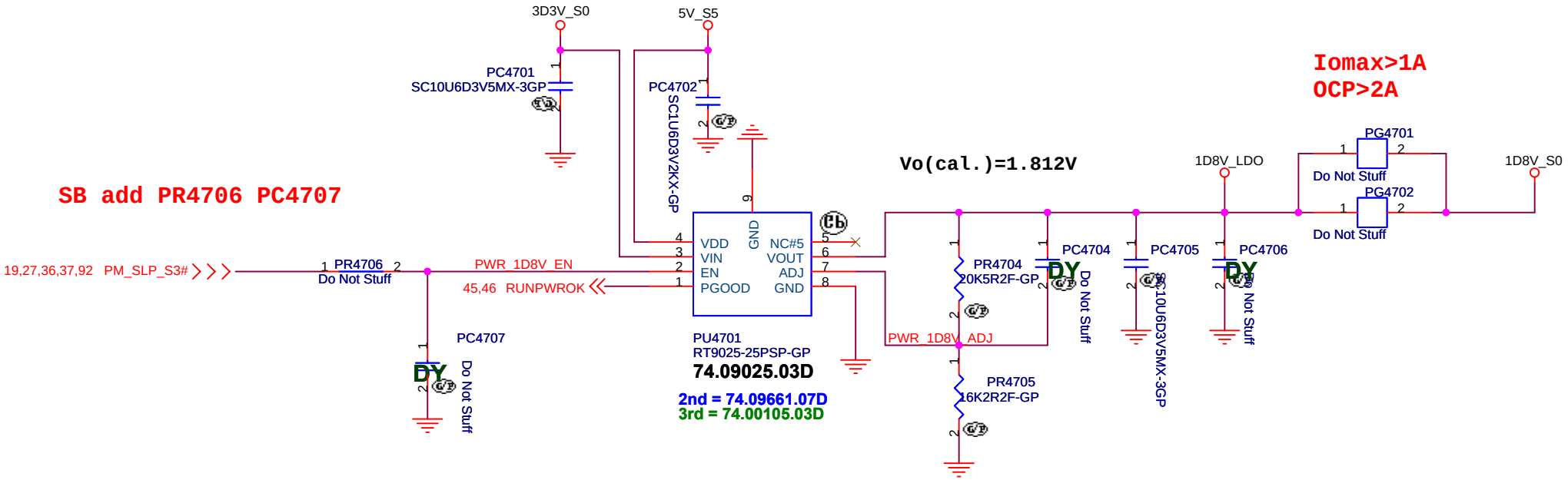
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



Title		
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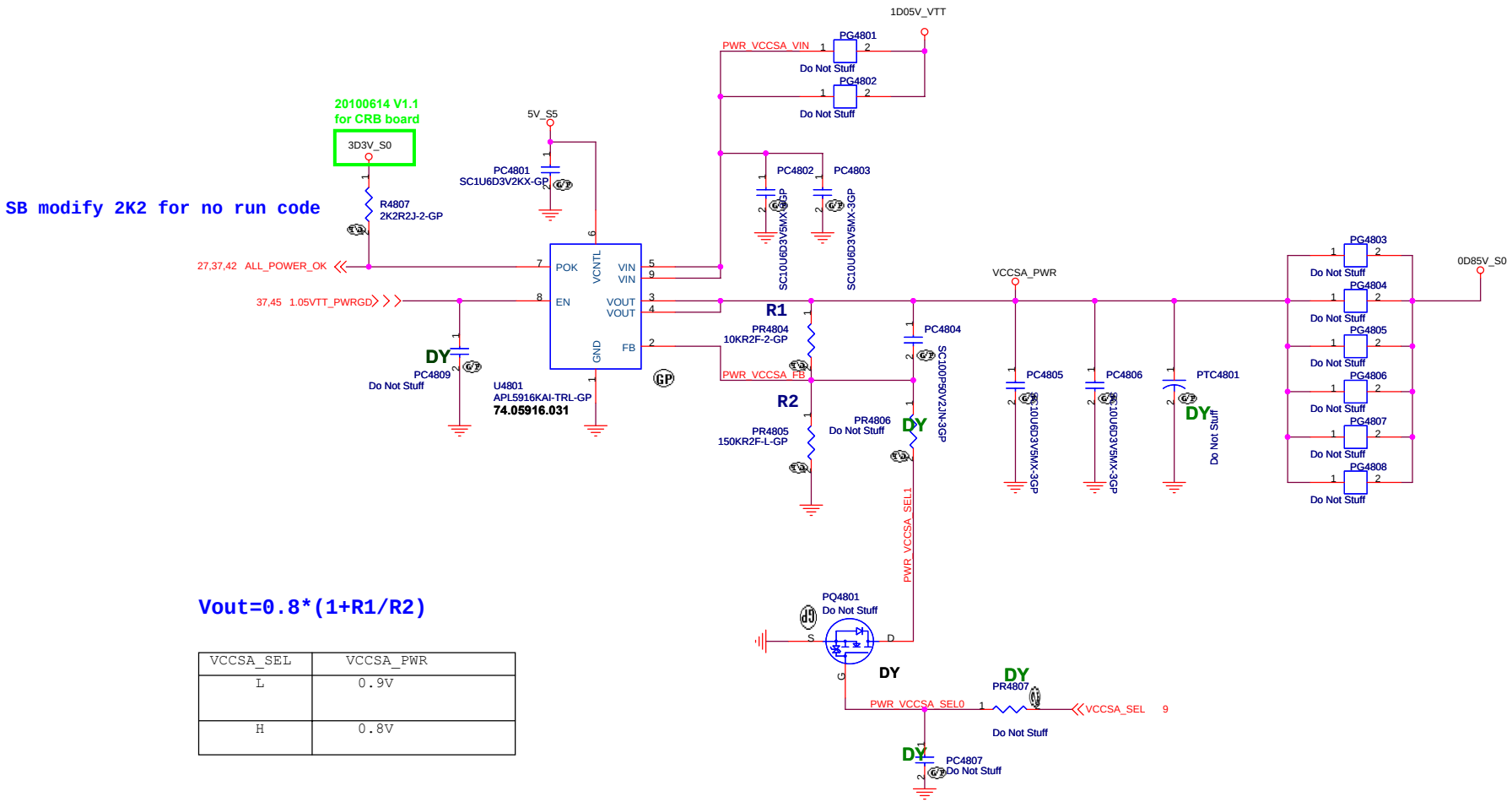
APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

Title		
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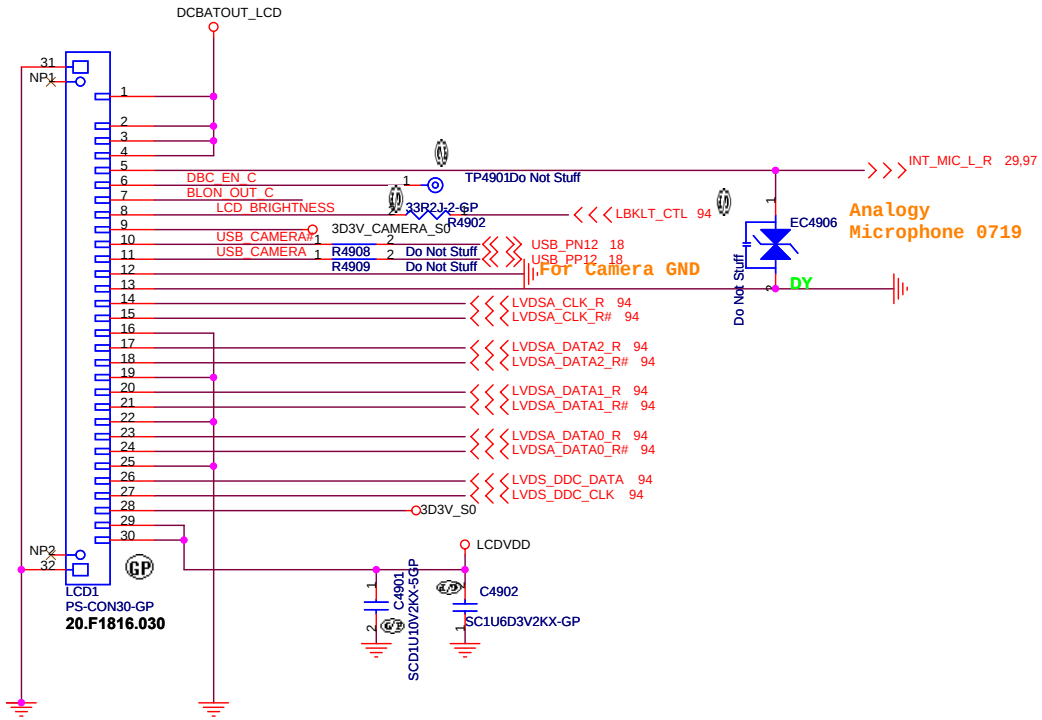
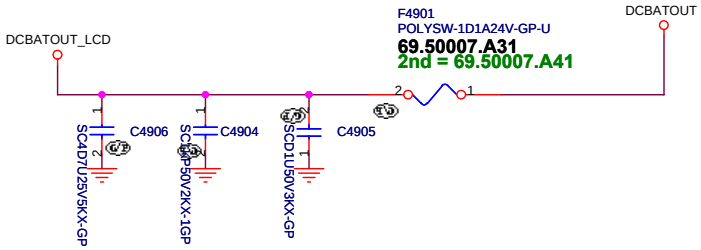
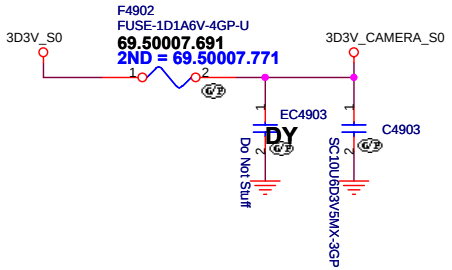
LVDS CONNECTOR



INVERTER POWER

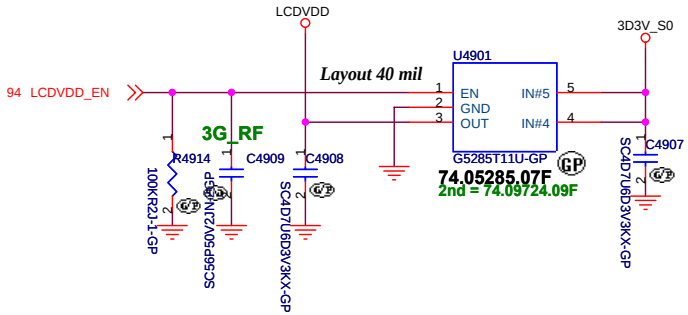


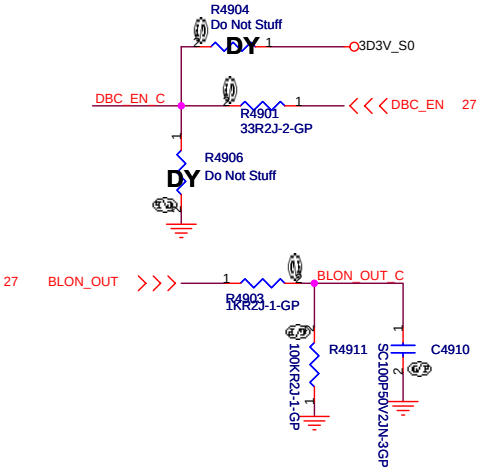
Camera Power



SSID = VIDEO

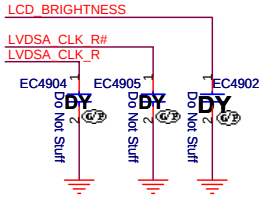
LCD POWER for ANNIE





For EMI request

Close to LVDS connector



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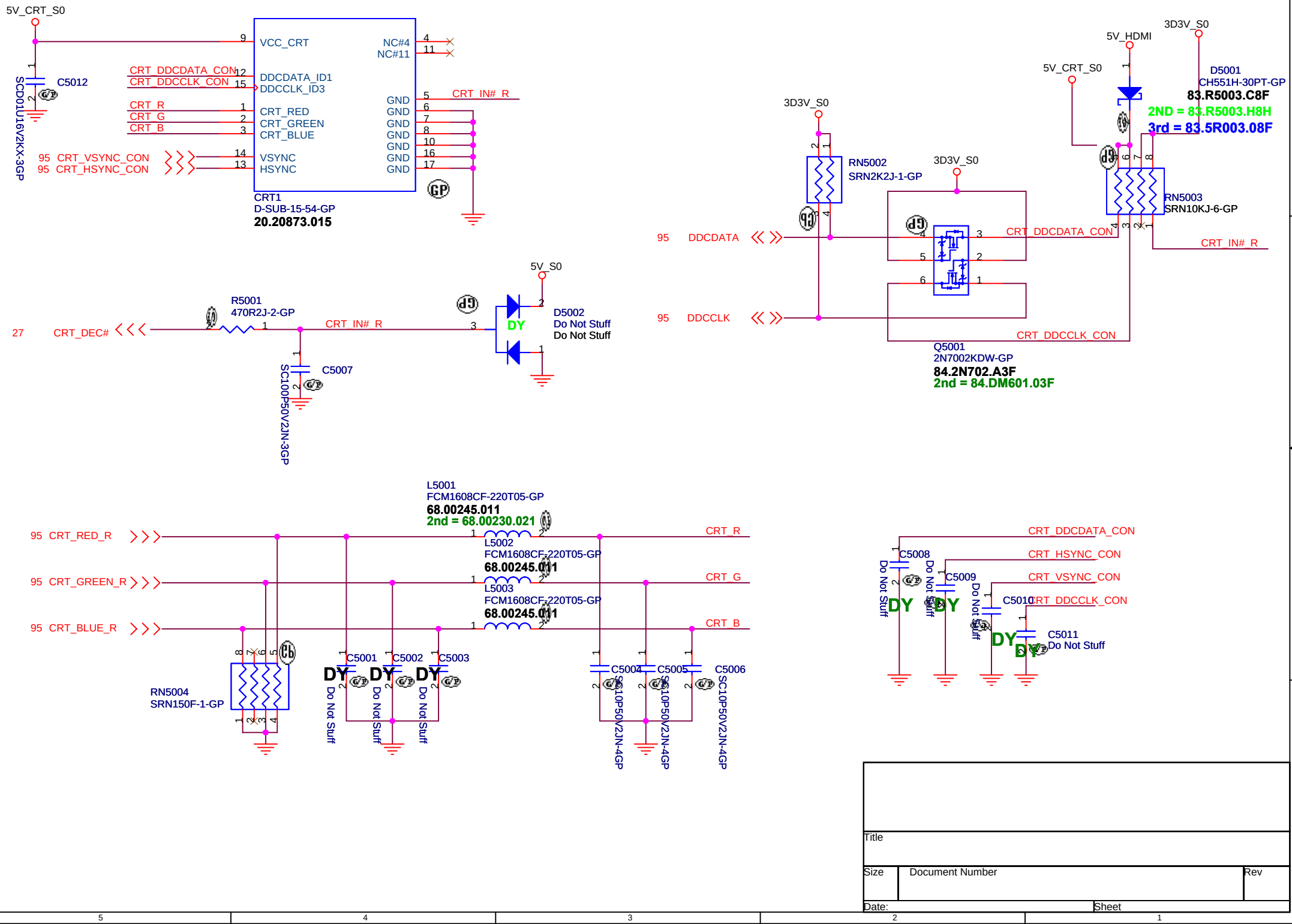
5V_CRT_S0
C5012
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
95 CRT_VSYNC_CON
95 CRT_HSYNC_CON
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
CRT_IN#_R
CRT1
D-SUB-15-54-GP
20.20873.015
3D3V_S0
5V_HDMI
5V_CRT_S0
D5001
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-6-GP
95 DDCDATA
95 DDCCLK
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_IN#_R
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
5V_S0
R5001
470R2J-2-GP
27 CRT_DEC#
CRT_IN#_R
D5002
Do Not Stuff
Do Not Stuff
C5007
SC100P50V2JN-3GP
L5001
FCM1608CF-220T05-GP
68.00245.011
2nd = 68.00230.021
L5002
FCM1608CF-220T05-GP
68.00245.011
L5003
FCM1608CF-220T05-GP
68.00245.011
95 CRT_RED_R
95 CRT_GREEN_R
95 CRT_BLUE_R
CRT_R
CRT_G
CRT_B
RN5004
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
DY
Do Not Stuff
SC10P50V2JN-4GP
C5008
C5009
C5010
C5011
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
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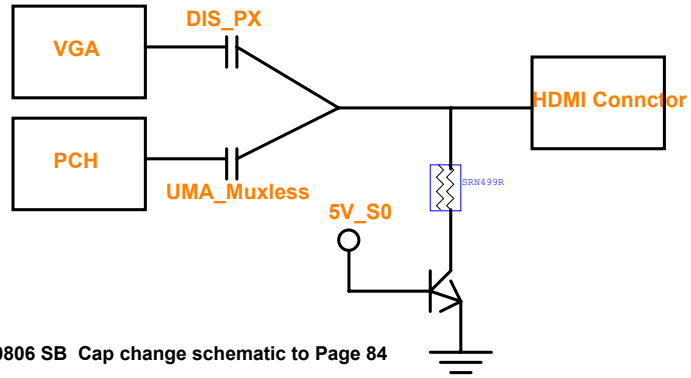
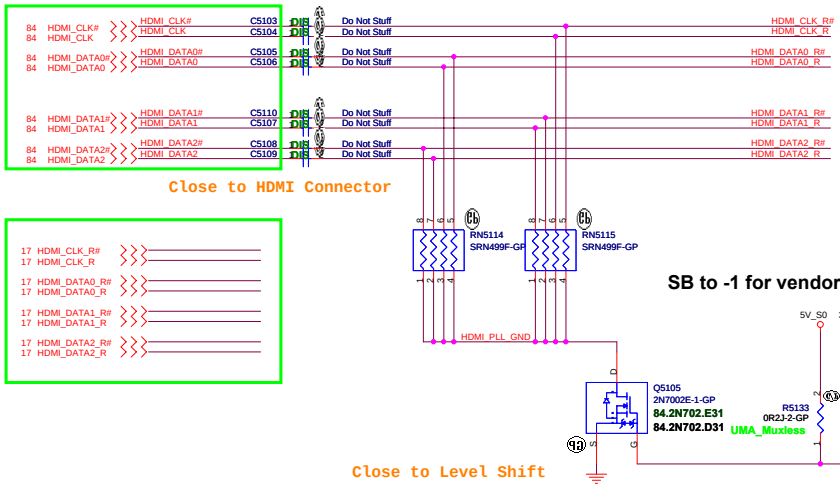
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

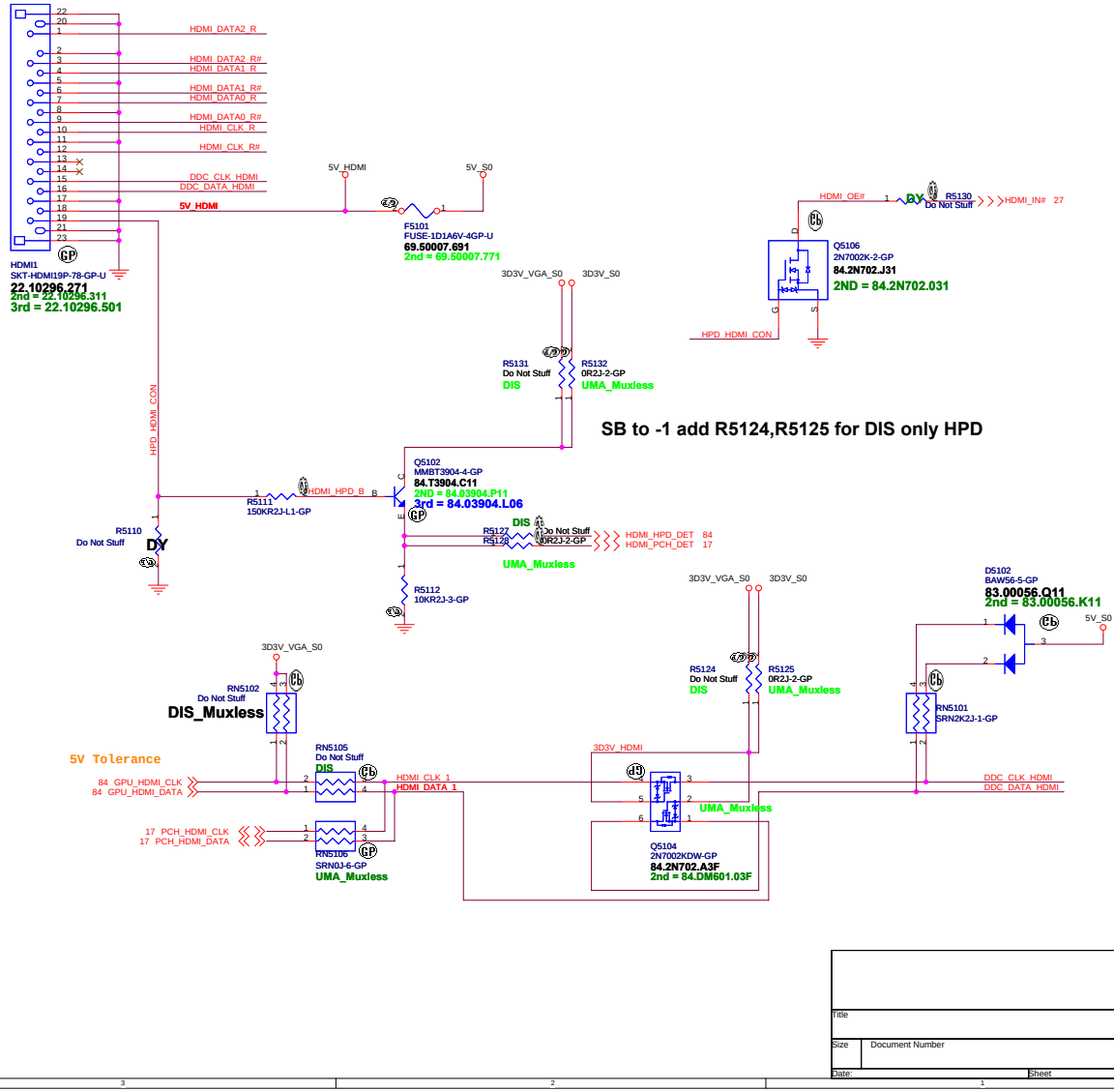
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



HDMI CONN



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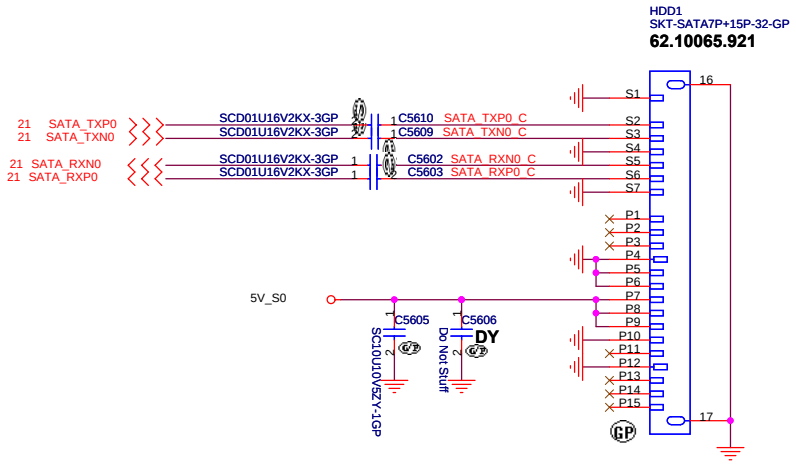
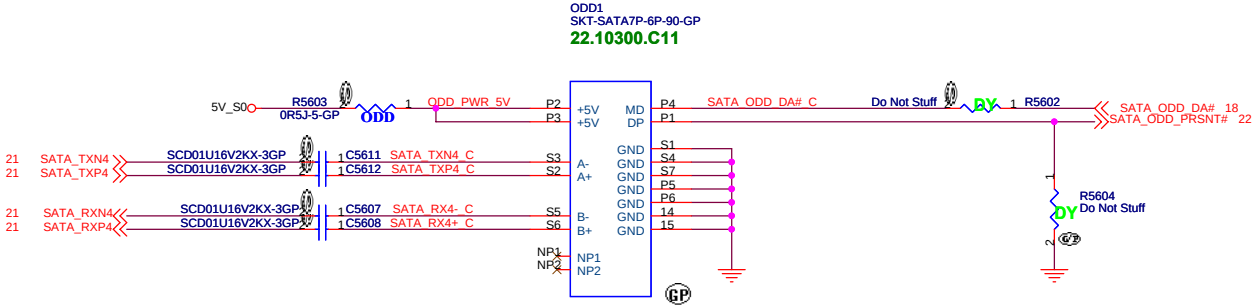
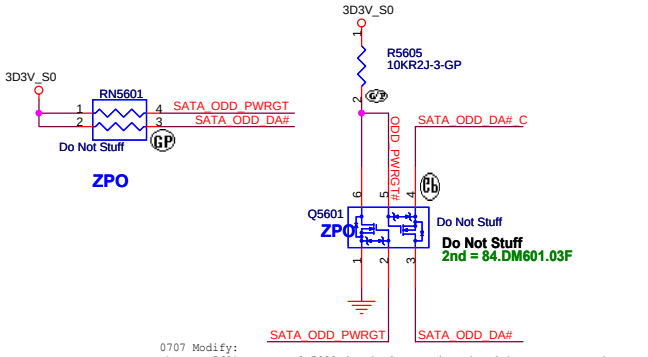
Date:		Sheet



ODD Connector



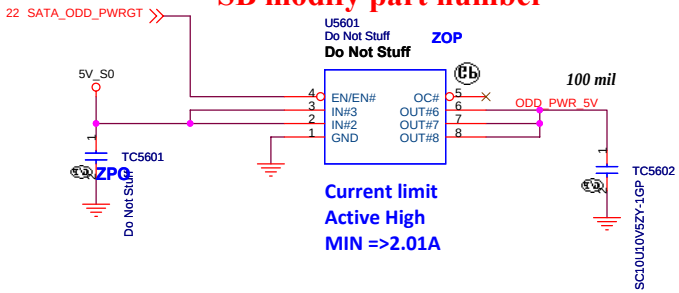


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



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GIGA Lan Transformer

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

SB modiyf Pin9 Pin10 SWAP

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

RN5901
SRN470J-4-GP-U

EC5901 EC5902
Do Not Stuff
DY DY

SB modify For EMI

U5901 U5902 U5903 U5904
TVLST2304AD0-GP
SURGE

GDT1 GDT2 GDT3 GDT4
B88069X9231T203-GP
SURGE

R5903J R5901J R5902J R5904
75R3J-L-GP

C5905
SC1KP2KV6KX-GP

C5907 C5906
DY DY
Do Not Stuff

EC5910 EC5909 EC5903 EC5904 EC5905 EC5906 EC5908 EC5907
SCD28P50V2CN-GP

C5916 C5917 C5918 C5919
DY Do Not Stuff

Title			
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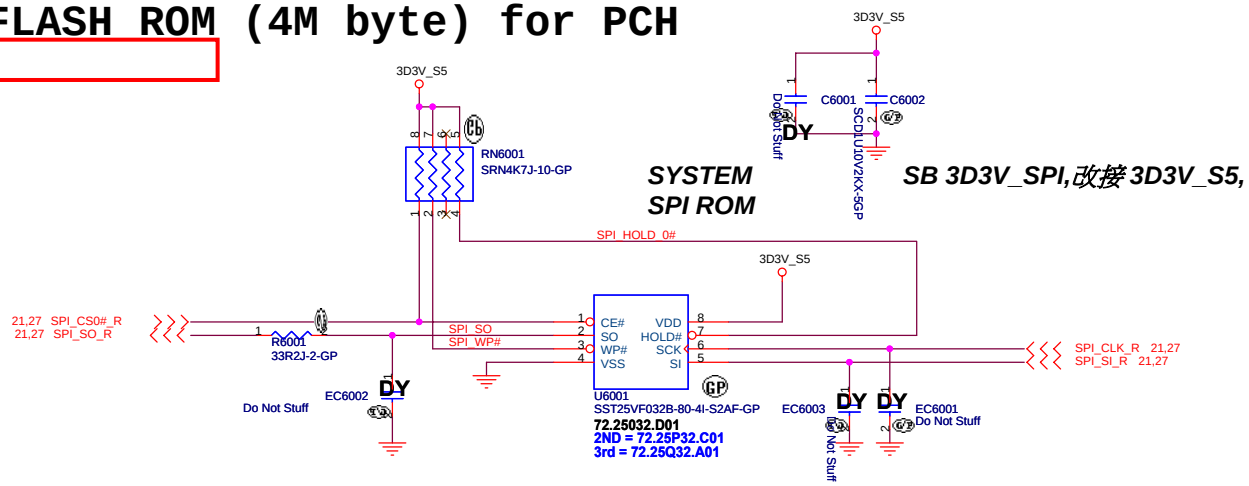
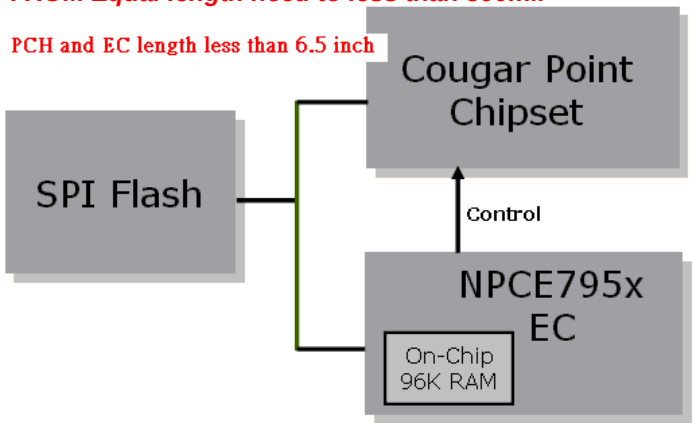
SPI FLASH ROM (4M byte) for PCH

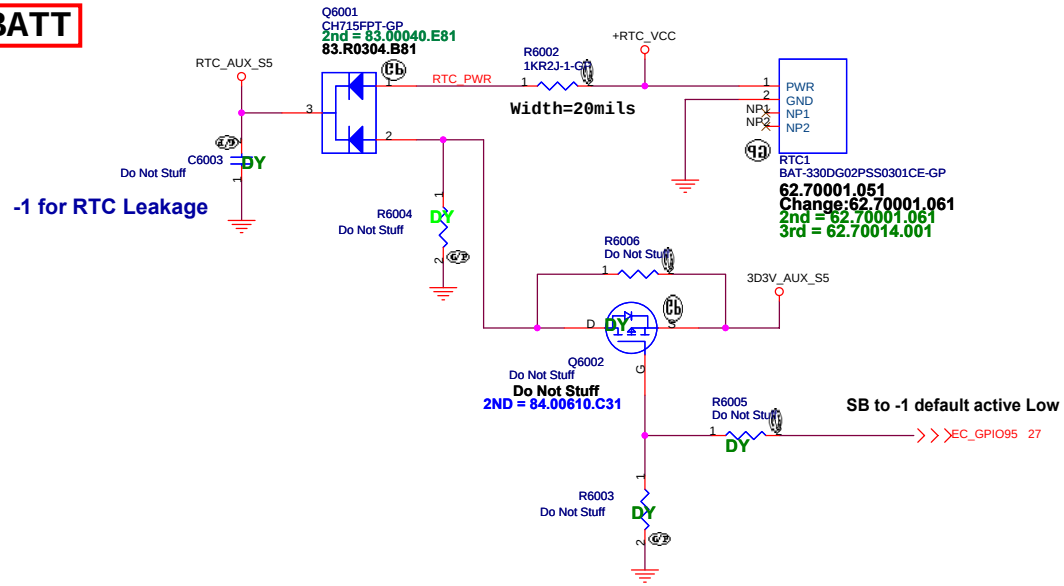


SPI ROM Equal length need to less than 500mil

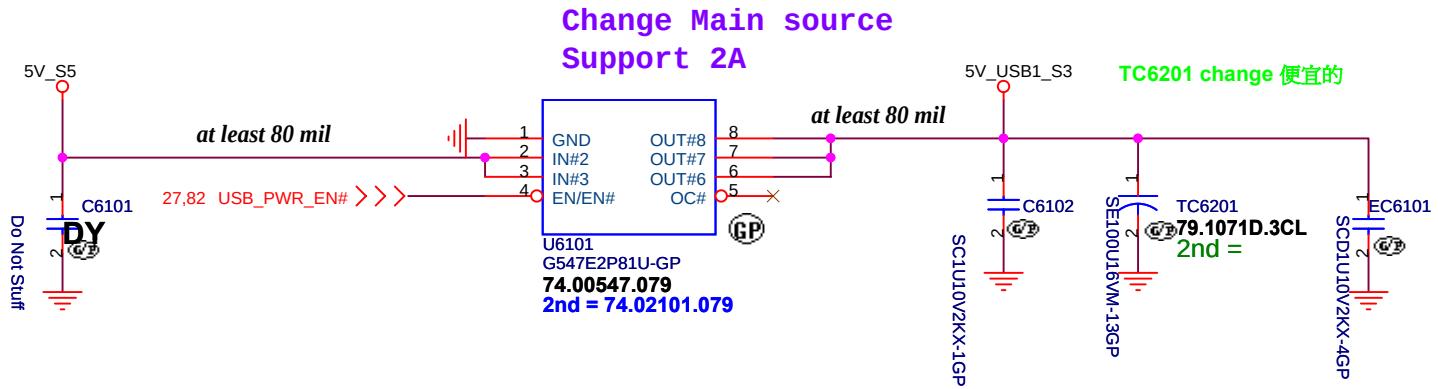
PCH and EC length less than 6.5 inch

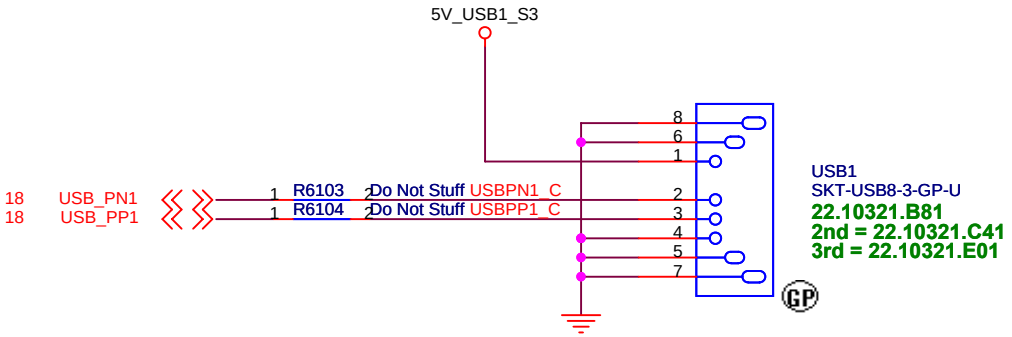


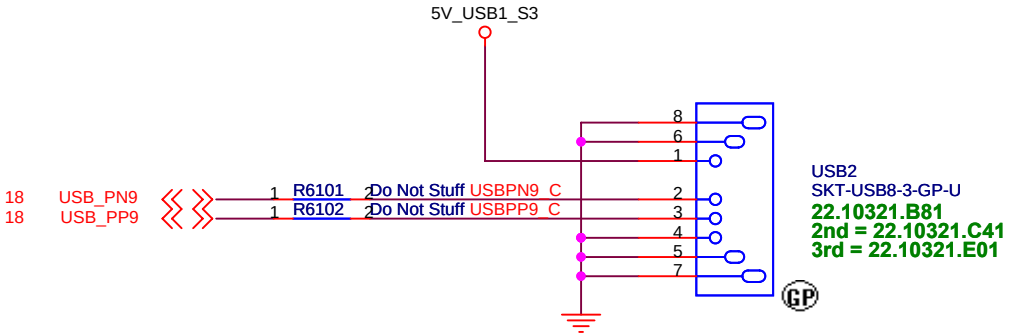
SSID = RBATT



Title		
Size	Document Number	Rev
Date:	Sheet	







Title		
Size	Document Number	Rev
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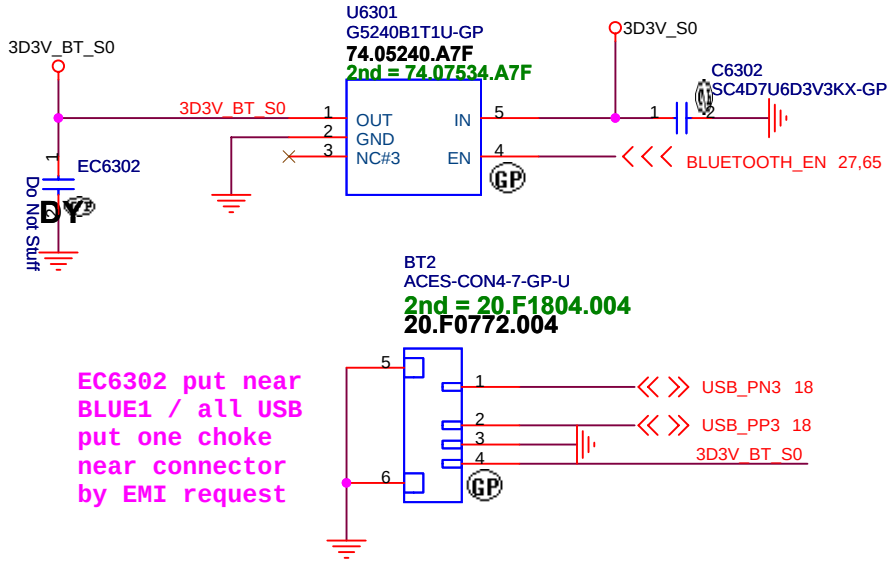
Bluetooth Module conn.

ANNIE Bluetooth Module



Title		
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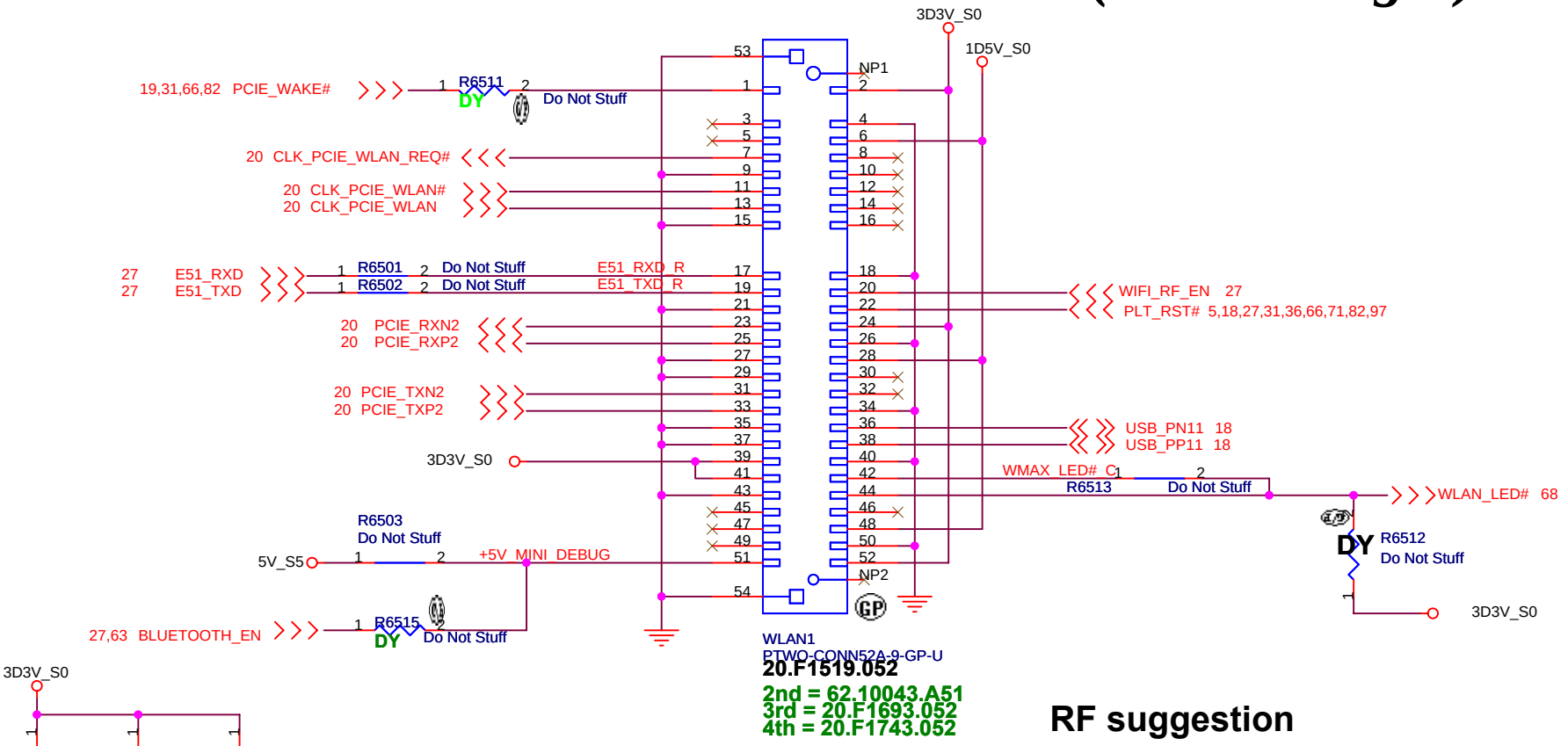
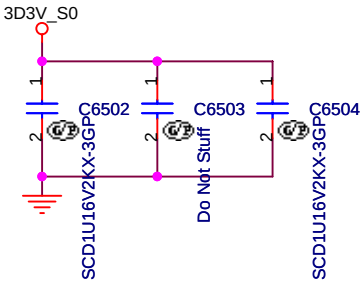
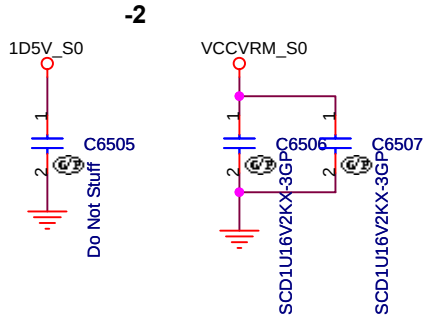
Date:	Sheet	

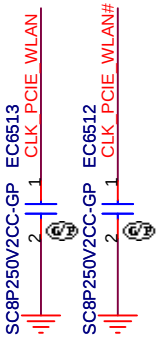
Mini Card Connector(802.11a/b/g/n)



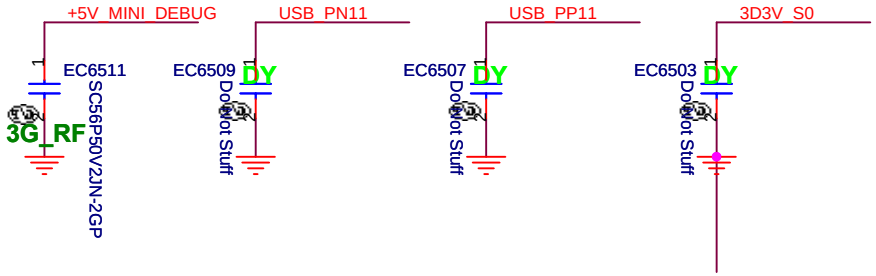


SB modify for SIV





RF suggestion



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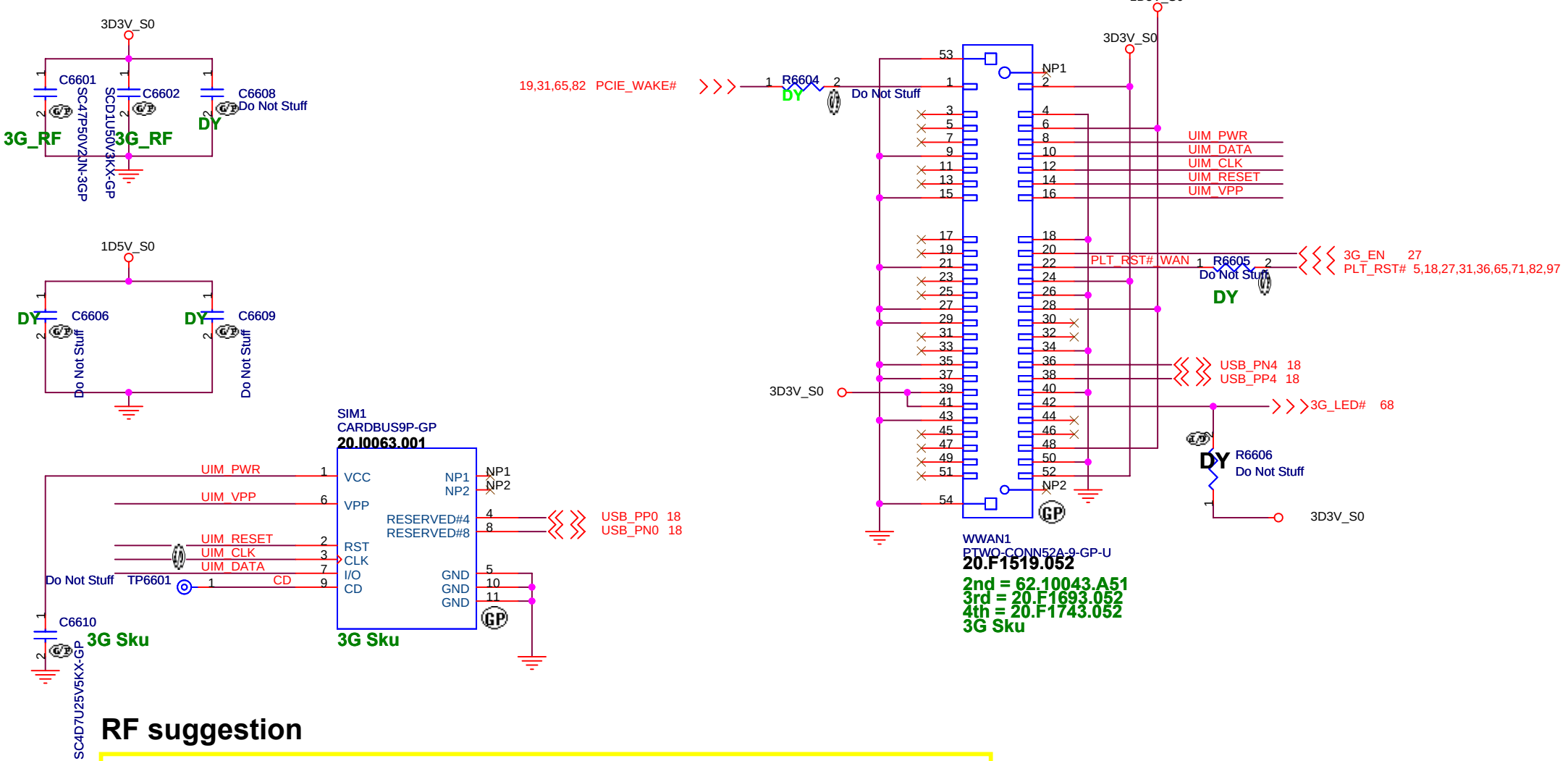
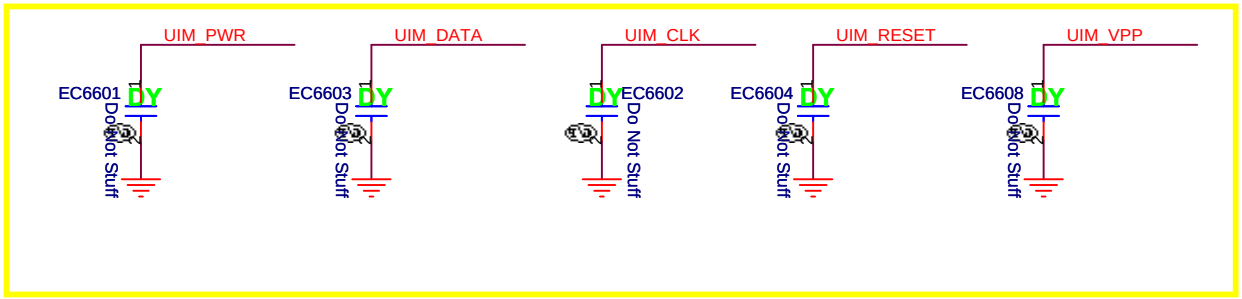
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



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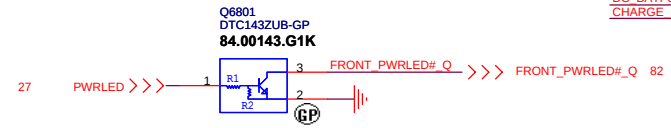
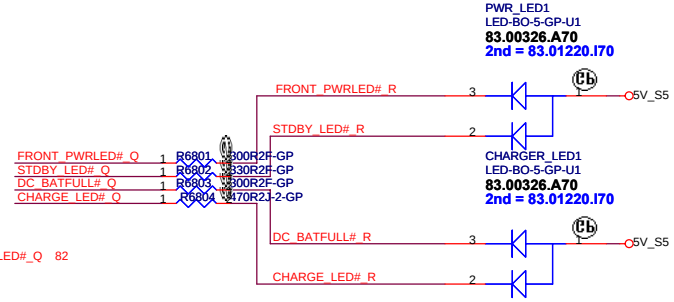
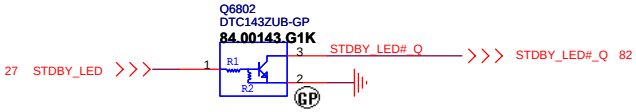
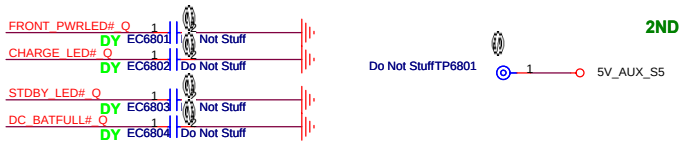
Power button LED



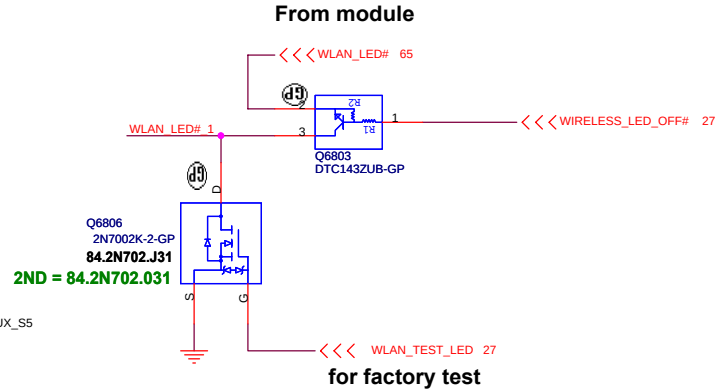


Power STDBY_LED

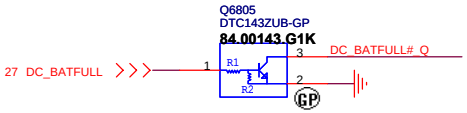




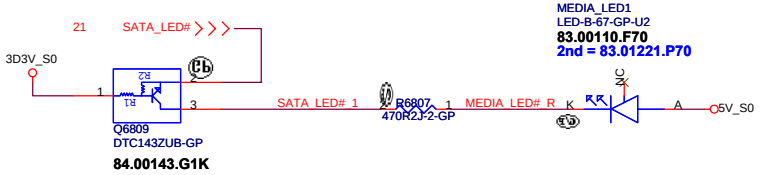
WLAN_LED



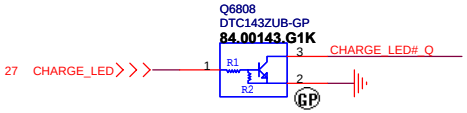
Battery LED2(DC_BATFULL)

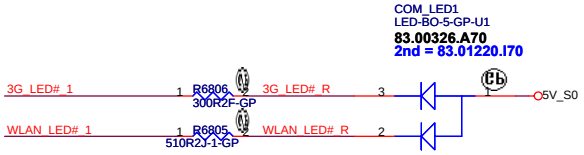


SATA HDD LED

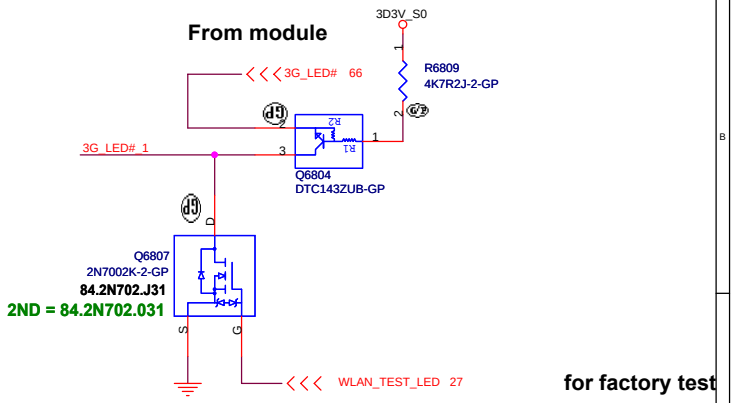


Battery LED1(CHARGE)





3G LED



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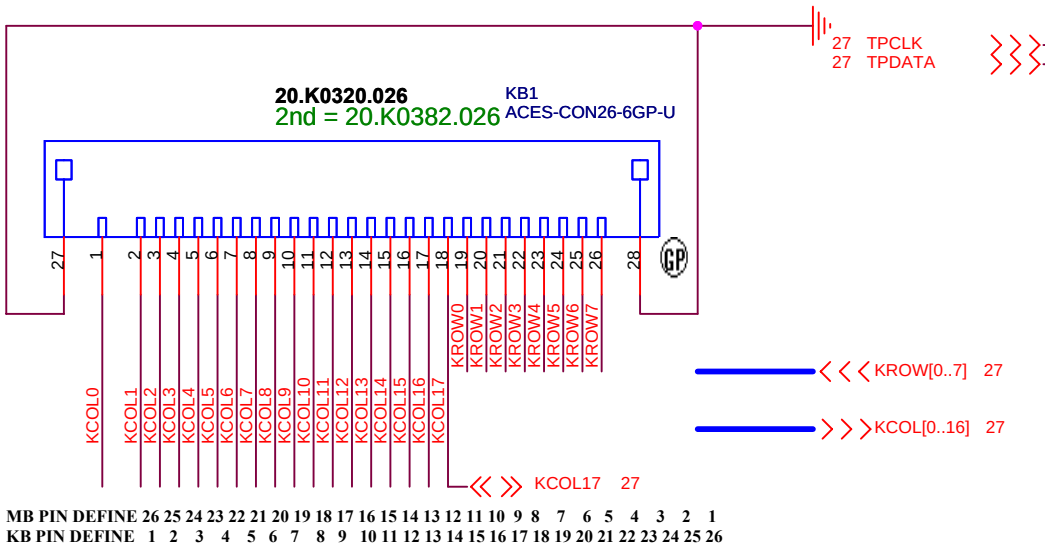
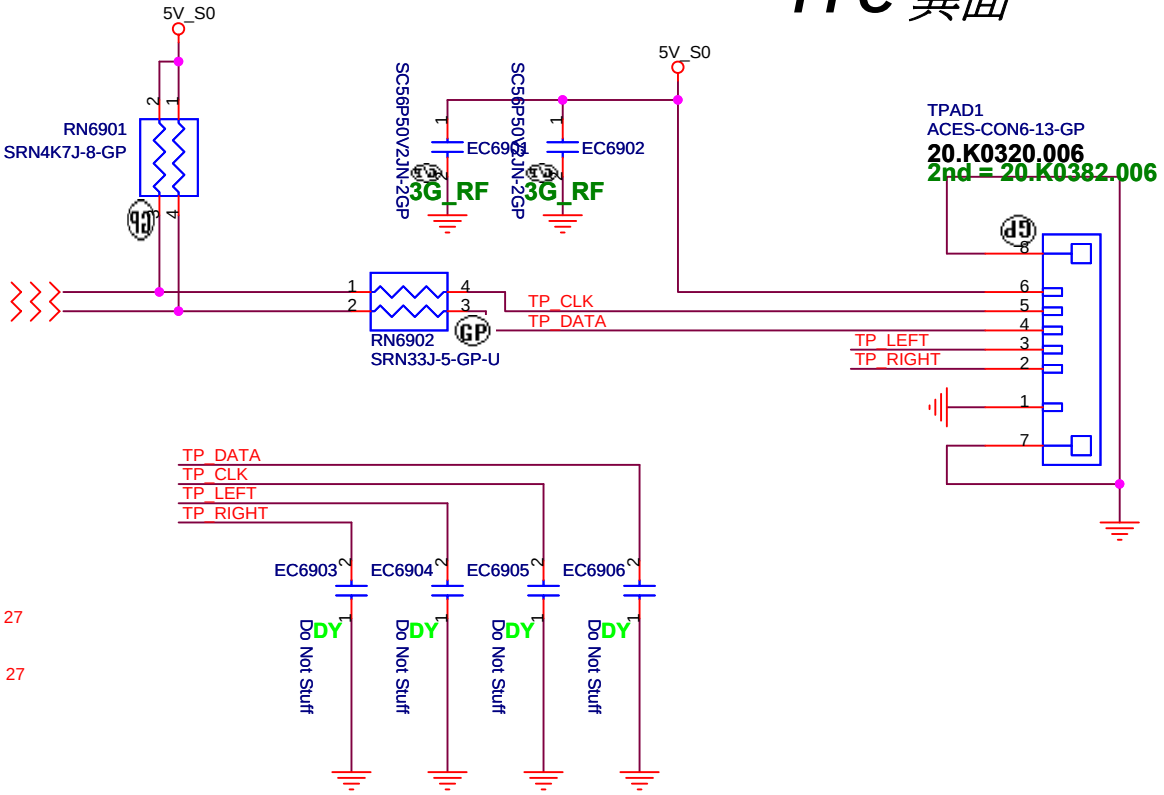
TOUCH PAD

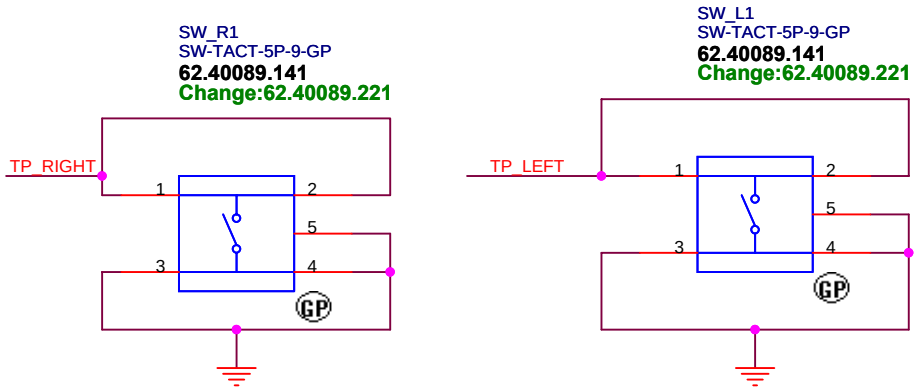
FFC 異面

Internal KeyBoard Connector





26 K/B 1 **SB to -1 modify Part number**



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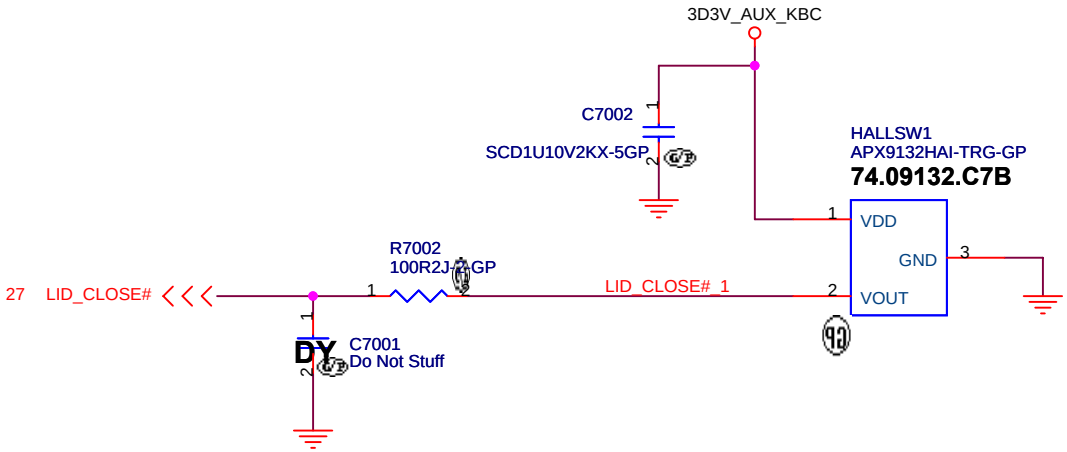

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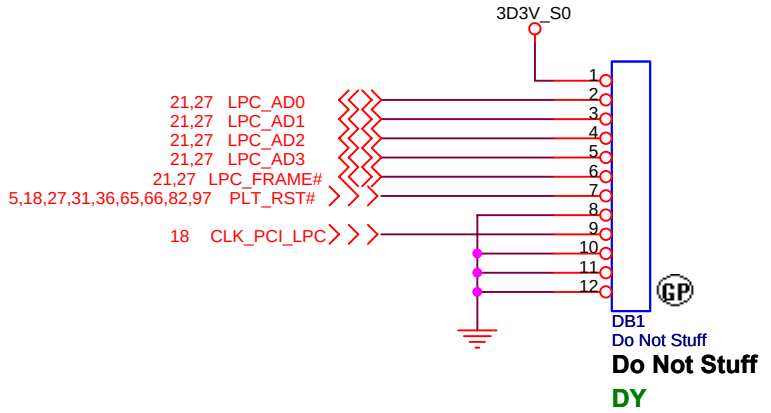
Date:	Sheet	



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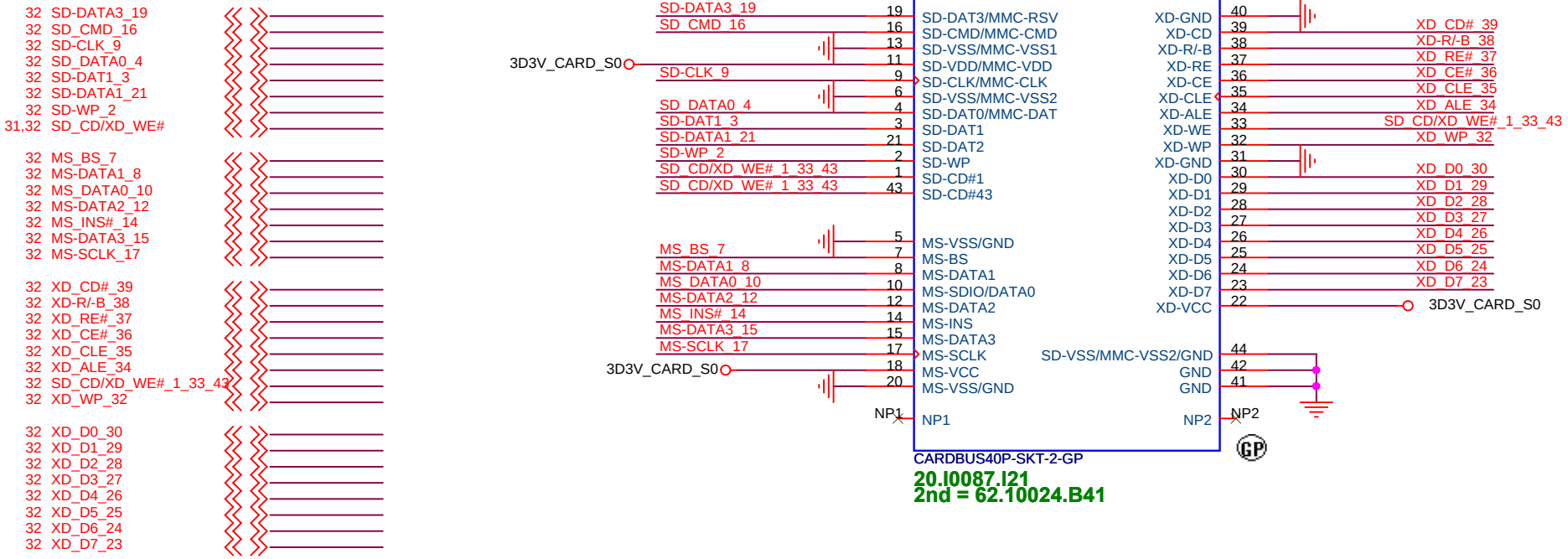
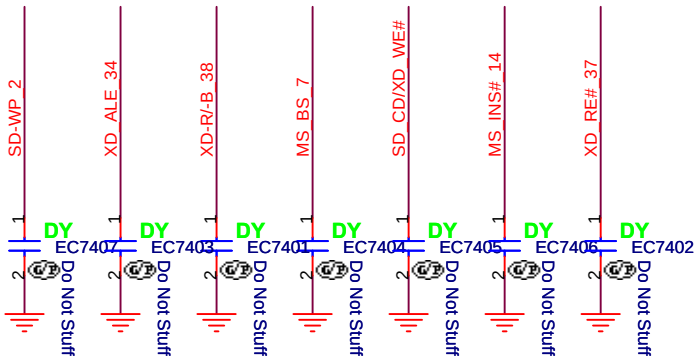
Size	Document Number	Rev
Date:		Sheet

SD/XD/MS Card Reader





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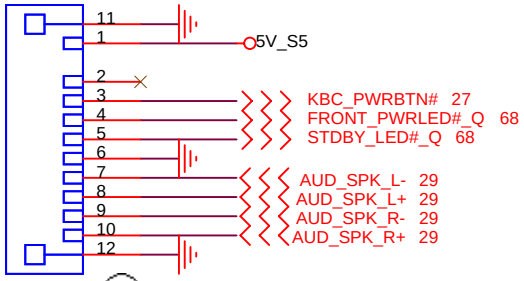
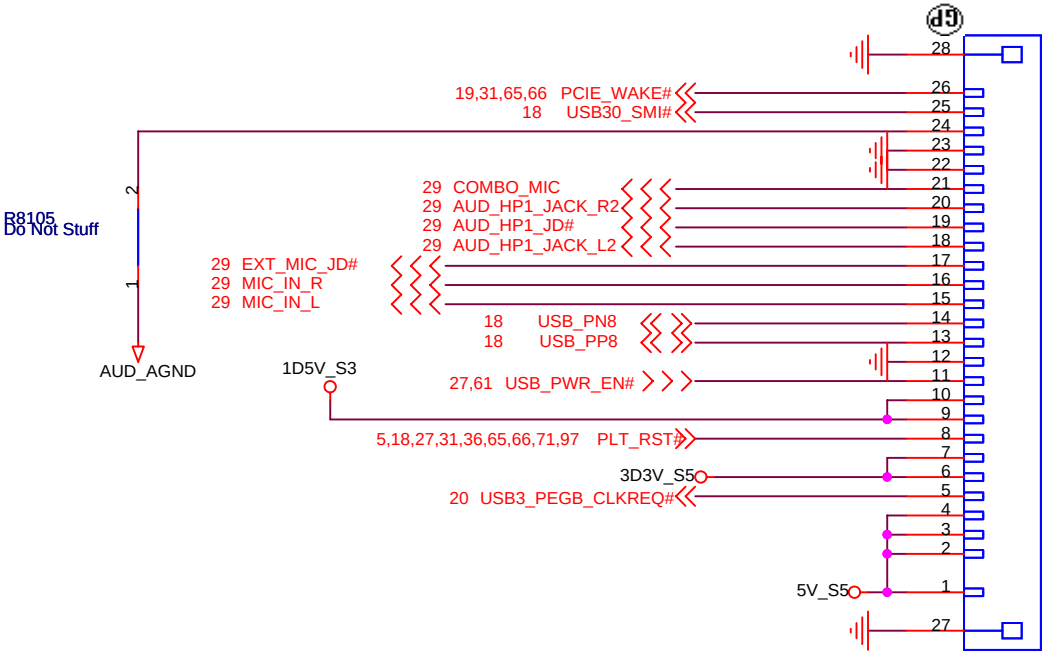
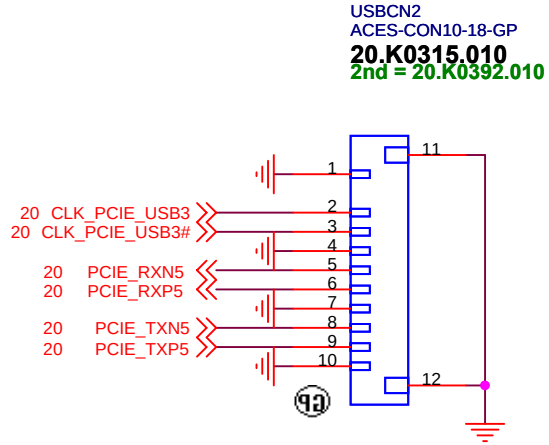
Size	Document Number	Rev
Date:		Sheet



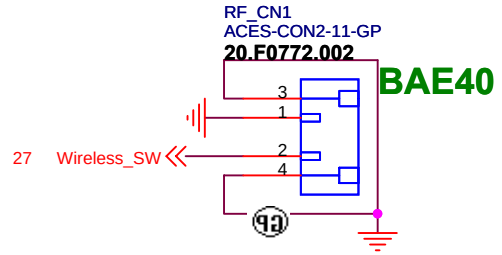
PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026



USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40

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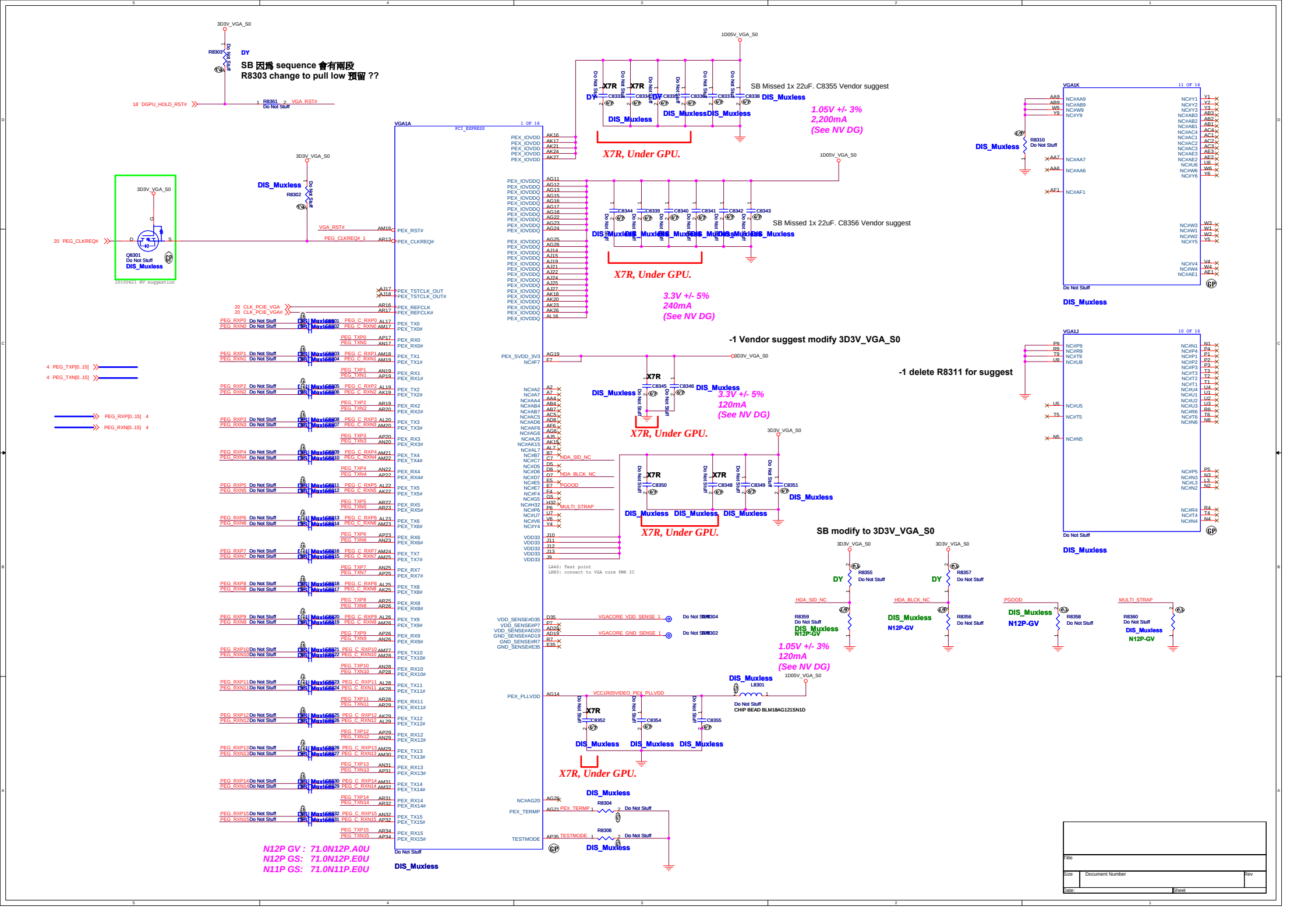
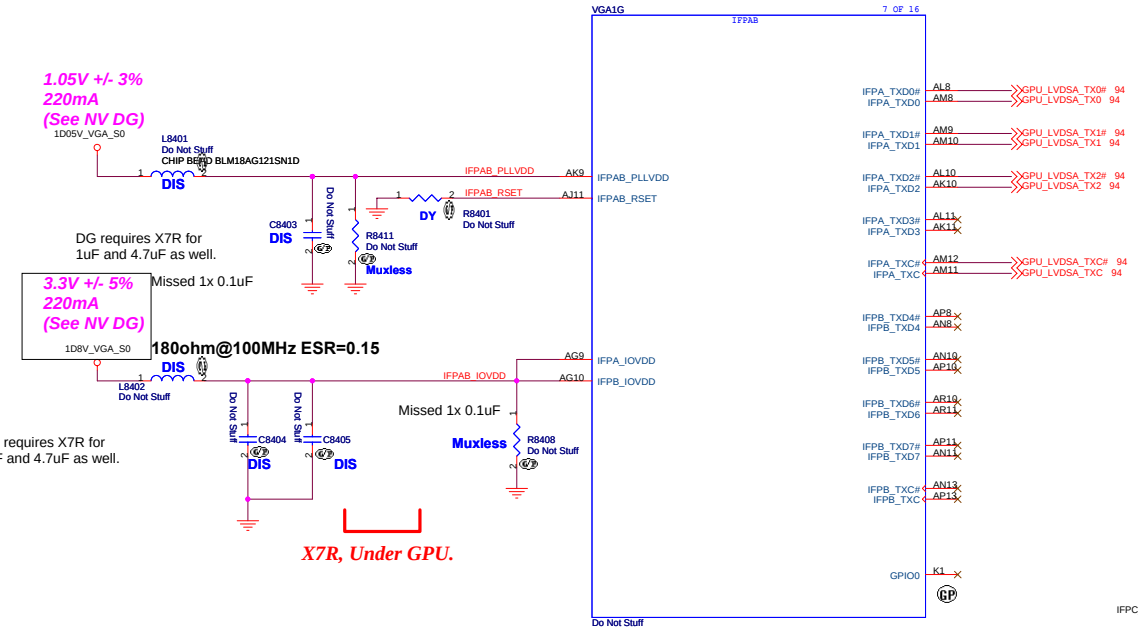
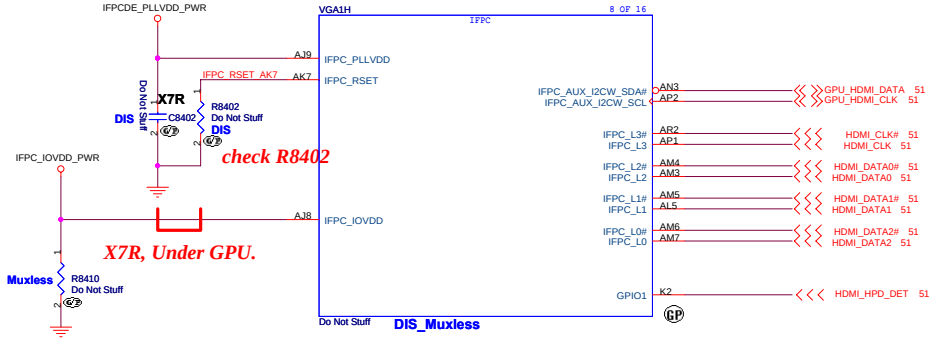
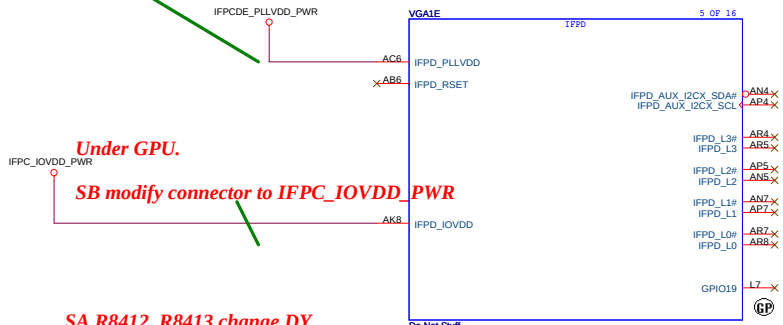

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U

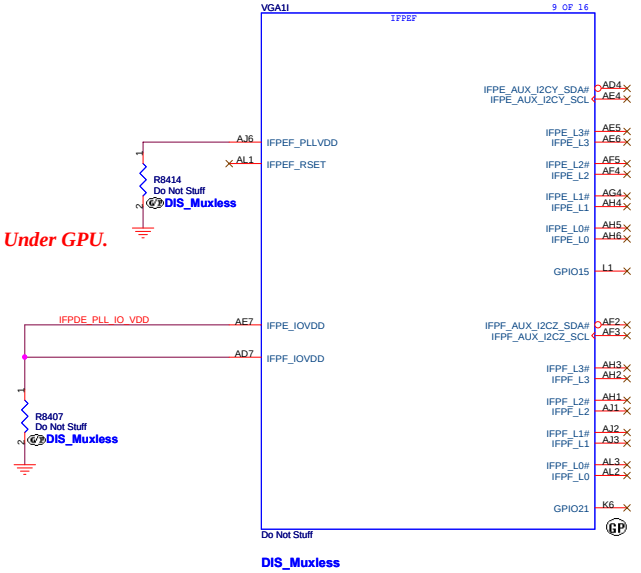
LVDS Interface





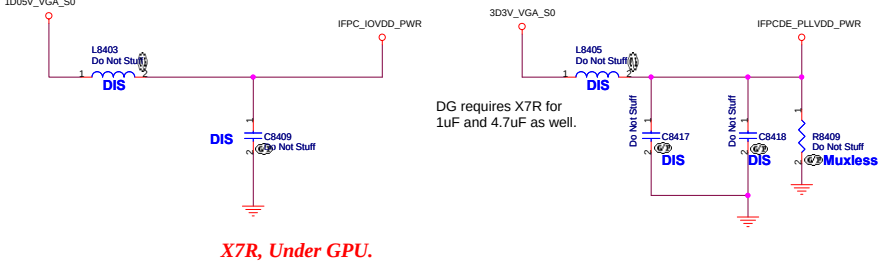
SB modify connector to IFPCDE_PLLVDD_PWR





SA R8412, R8413 change DY
SB R8412, R8413 change delete

HDMI Interface



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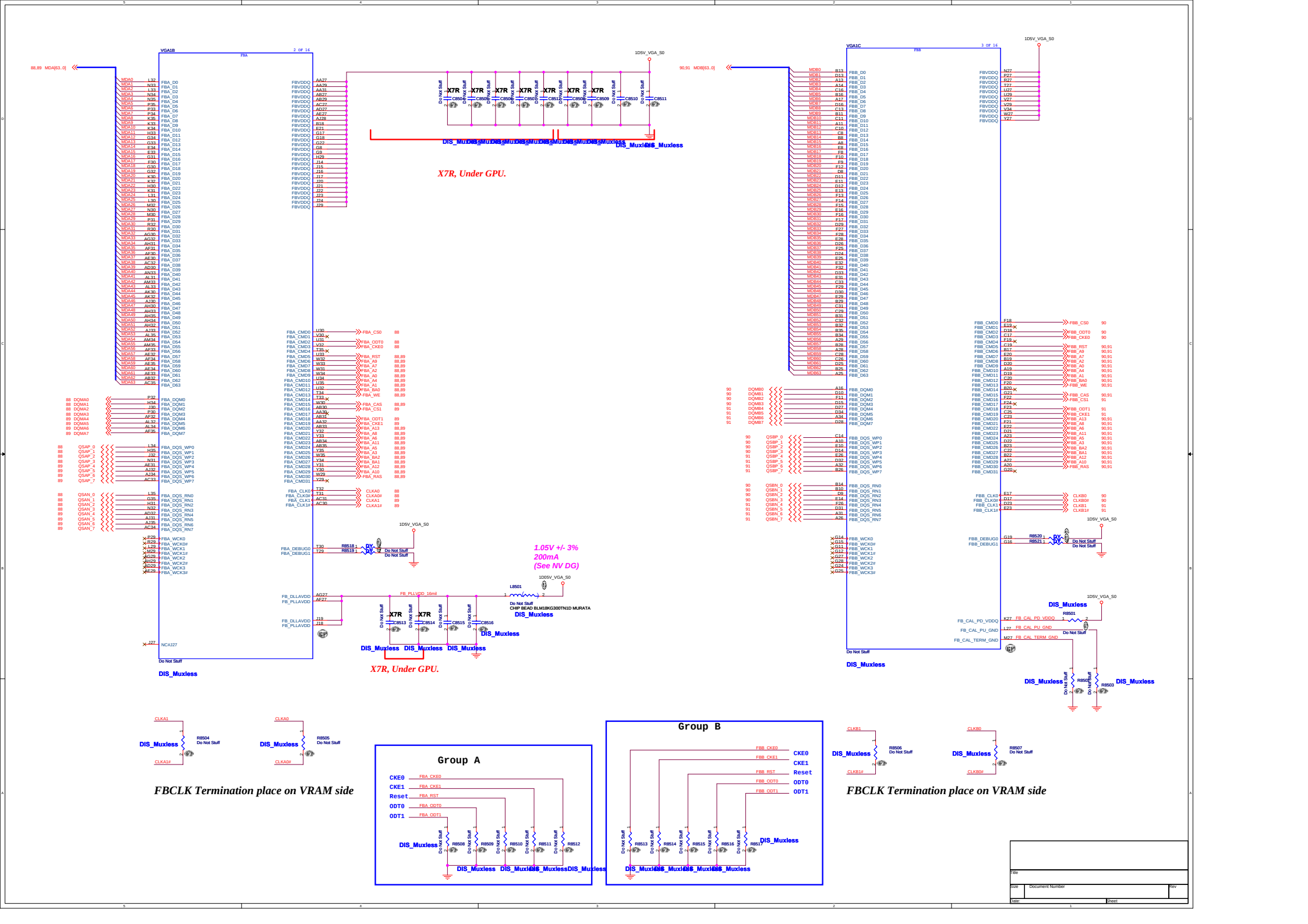

VGA1B
FBA
2 OF 16
VGA1C
FBB
3 OF 16
1D5V_VGA_S0
X7R, Under GPU.
1.05V +/- 3%
200mA
(See NV DG)
DIS_Muxless
Do Not Stuff
Group A
Group B
CKE0
CKE1
Reset
ODT0
ODT1
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side

3.3V +/- 5%
120mA
(See NV DG)

X7R, Under GPU.

Missed 3x 0.1uF

delete 10K DY to GND

SB DIS_Muxless 都要上件或DY??

SB HOSONIC modify to 12P, R8607 modify to 390R

VGA Thermal sensor P2800

Modify SMBUS

SB 修改上件,才能跑全速

Pull high 在Page 94

预留0.9V

SB R8619 15" DY

SJM50-CP SUPPORT							
P-STATE	NVVDD_ALT_V1	NVVDD_ALT_V0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N12P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V

NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

```
for 1Gbit      for 2Gbit      for 1Gbit      for 2Gbit
Hynix VRAM     Hynix VRAM     Samsung VRAM   Samsung VRAM
RAM_CFG[0]=0   RAM_CFG[0]=0   RAM_CFG[0]=1   RAM_CFG[0]=1
RAM_CFG[1]=1   RAM_CFG[1]=1   RAM_CFG[1]=1   RAM_CFG[1]=1
RAM_CFG[2]=0   RAM_CFG[2]=1   RAM_CFG[2]=0   RAM_CFG[2]=1
RAM_CFG[3]=0   RAM_CFG[3]=0   RAM_CFG[3]=0   RAM_CFG[3]=0
```

GPU_ROM_SO

```
VGA_DEVICE   =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417     =0 (High bit)
```

GPU_ROM_SCLK

```
PEX_PLL_EN_TERM =0
SLOT_CLK_CFG    =1
SUB_VENDOR      =0
PCI_DEVID[4]    =1
```

N11P Fermi QS 1

```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
5Kohms    1000    0000
10Kohms   1001    0001
15Kohms   1010    0010
20Kohms   1011    0011
25Kohms   1100    0100
30Kohms   1101    0101
35Kohms   1110    0110
45Kohms   1111    0111
```

Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

SB change 3D3V_VGA_S0, R8638 change DY

TABLE NVIDIA

-1 modify N12P GV setting

71.0N12P.E0U → 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

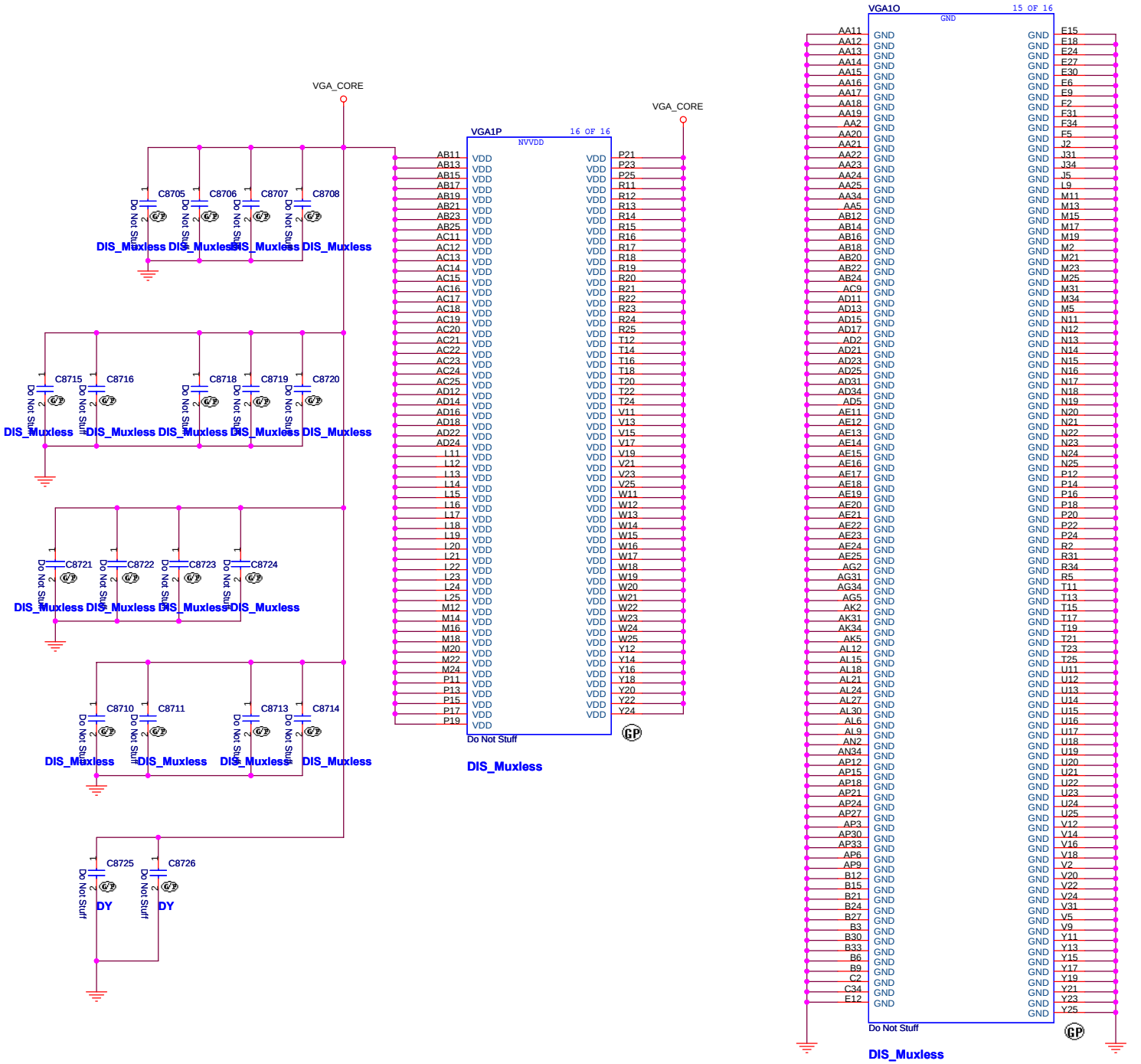
STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

USE 1111 (45K)

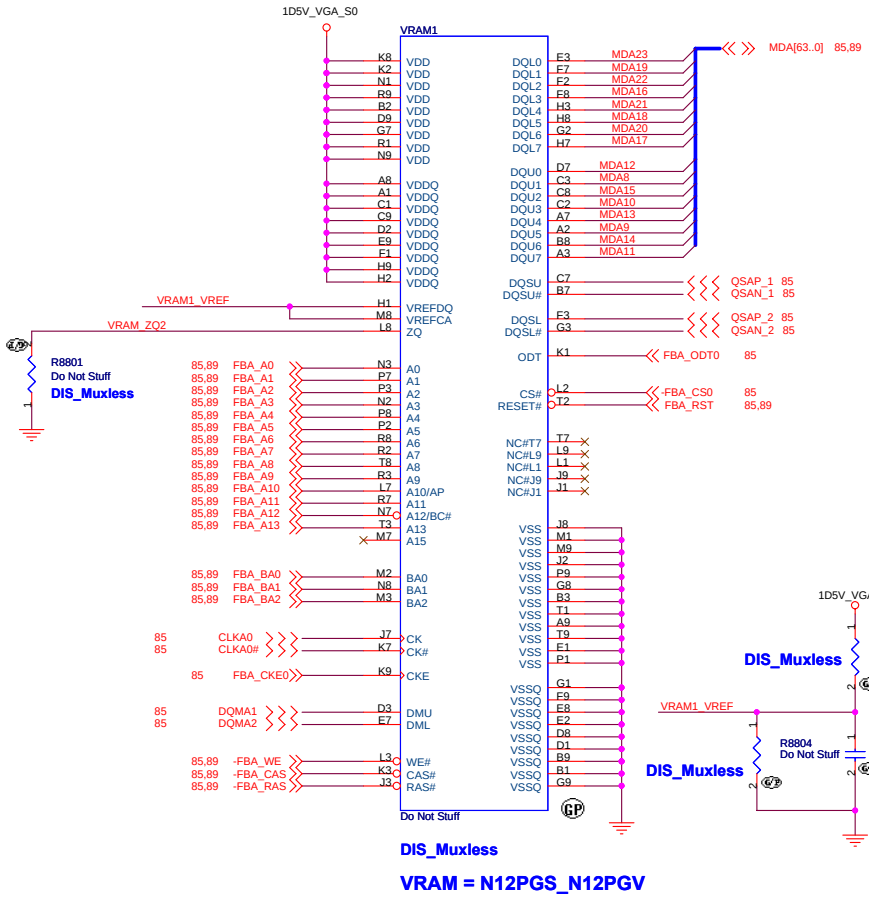
STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — USE 0110 (35K)

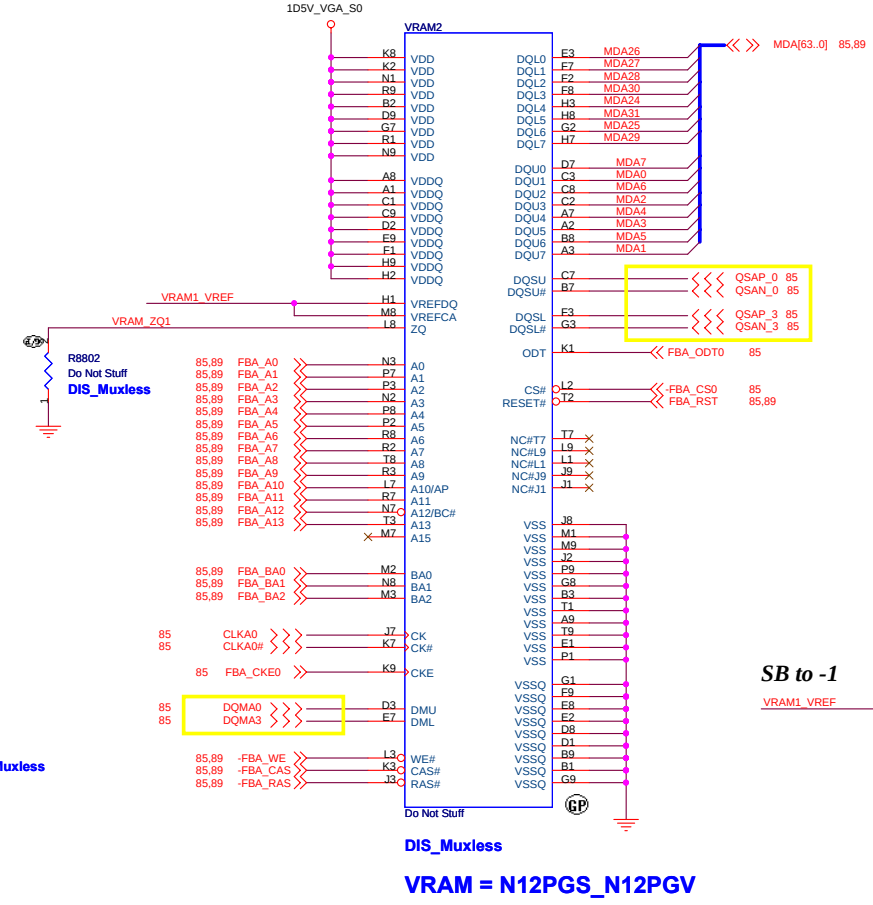
STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

N12PGS_N12PGV:64.49915.6DL

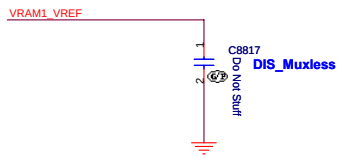


Title		
Size	Document Number	Rev
Date:	Sheet	

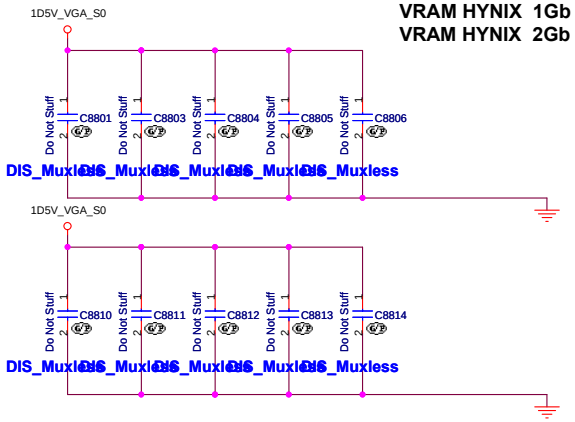


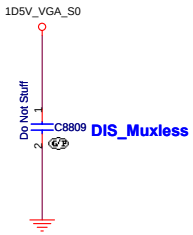


SB to -1



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





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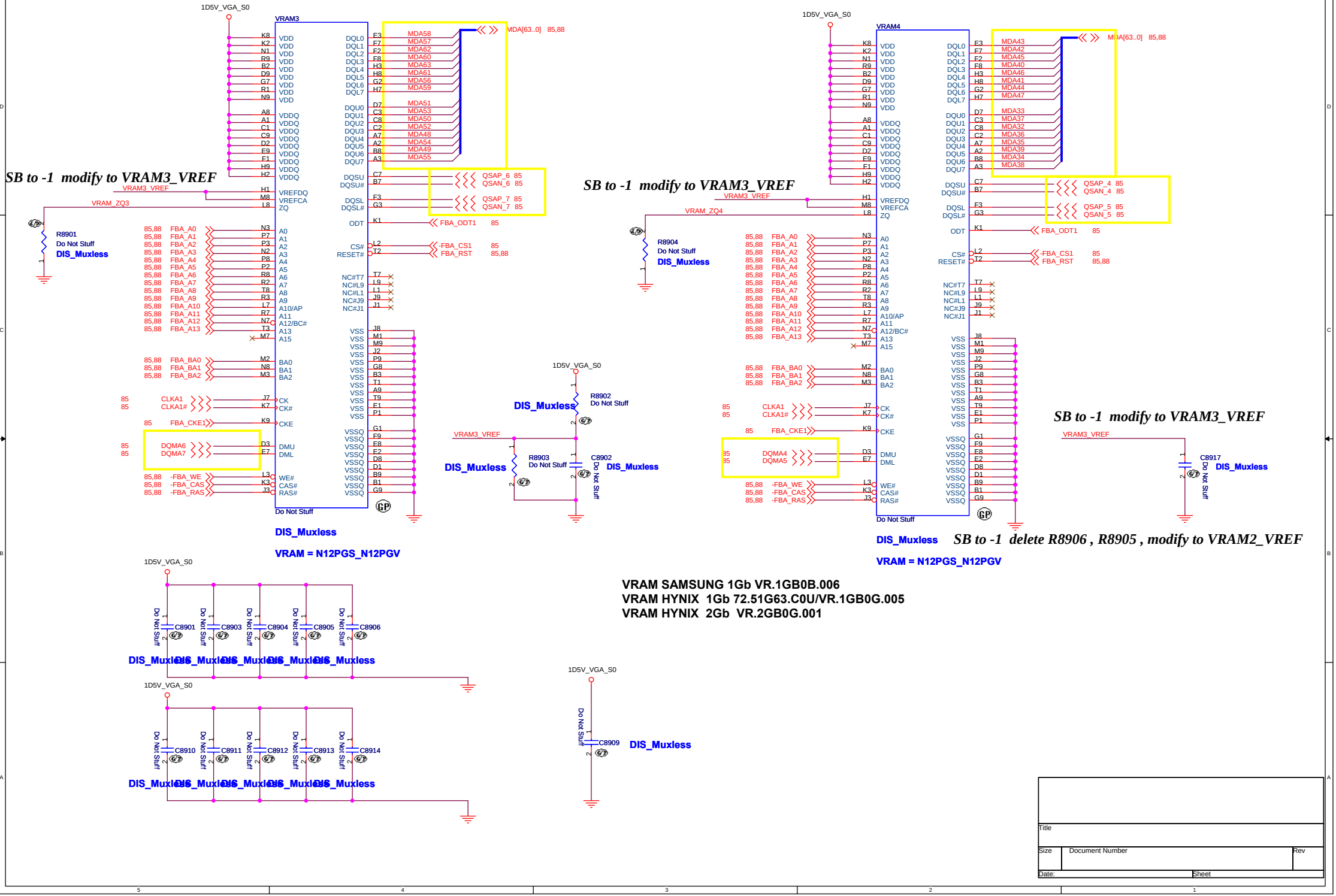
Date:		Sheet


1D5V_VGA_S0
VRAM3
VRAM4
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 delete R8906 , R8905 , modify to VRAM2_VREF
R8901
R8904
R8902
R8903
C8902
C8917
Do Not Stuff
DIS_Muxless
VRAM = N12PGS_N12PGV
VRAM = N12PGS_N12PGV
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
C8901
C8903
C8904
C8905
C8906
C8910
C8911
C8912
C8913
C8914
C8909
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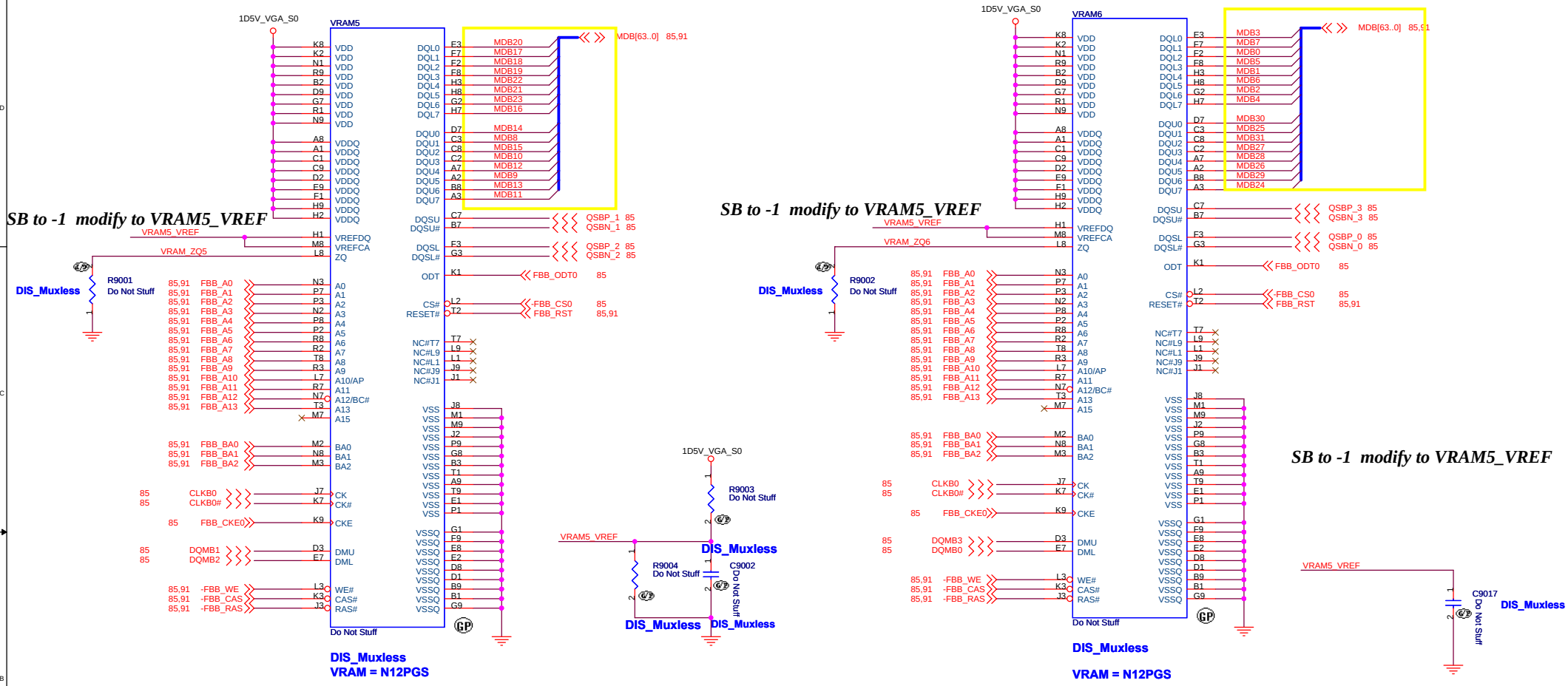
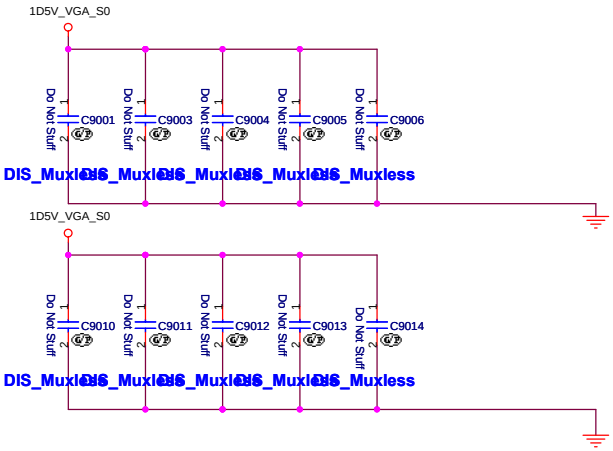
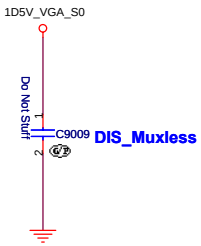


VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





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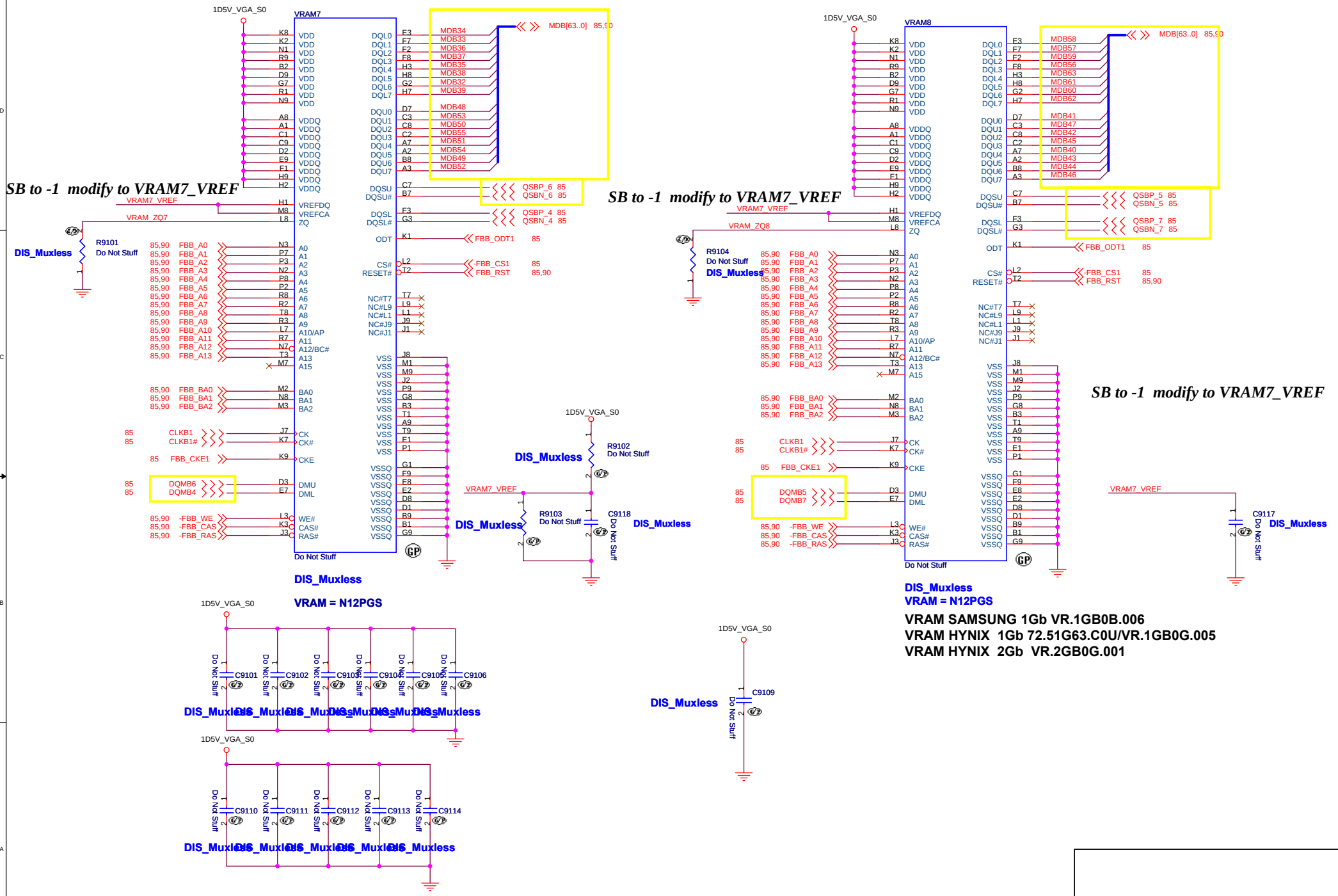
SB to -1 modify to VRAM7_VREF
VRAM7
1D5V_VGA_S0
VRAM7_VREF
VRAM_ZQ7
R9101
Do Not Stuff
DIS_Muxless
MDB[63..0]
QSBP_6
QSBN_6
QSBP_4
QSBN_4
FBB_ODT1
FBB_CS1
FBB_RST
FBB_A0
FBB_A1
FBB_A2
FBB_A3
FBB_A4
FBB_A5
FBB_A6
FBB_A7
FBB_A8
FBB_A9
FBB_A10
FBB_A11
FBB_A12
FBB_A13
FBB_BA0
FBB_BA1
FBB_BA2
CLKB1
CLKB1#
FBB_CKE1
DQMB6
DQMB4
-FBB_WE
-FBB_CAS
-FBB_RAS
R9102
R9103
C9118
VRAM = N12PGS
C9101
C9102
C9103
C9104
C9105
C9106
C9110
C9111
C9112
C9113
C9114
SB to -1 modify to VRAM7_VREF
VRAM8
VRAM_ZQ8
R9104
QSBP_5
QSBN_5
QSBP_7
QSBN_7
DQMB5
DQMB7
C9117
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
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20100715

SSID = PWR.Plane.Regulator_GFX

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Vout=0.75V*(R1+R2)/R2

SB to -1 modify PR9213 VGA_Core to 1.05V

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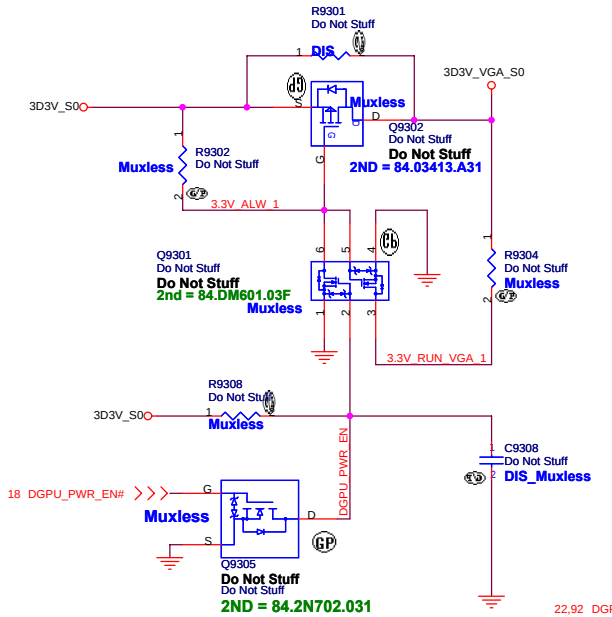
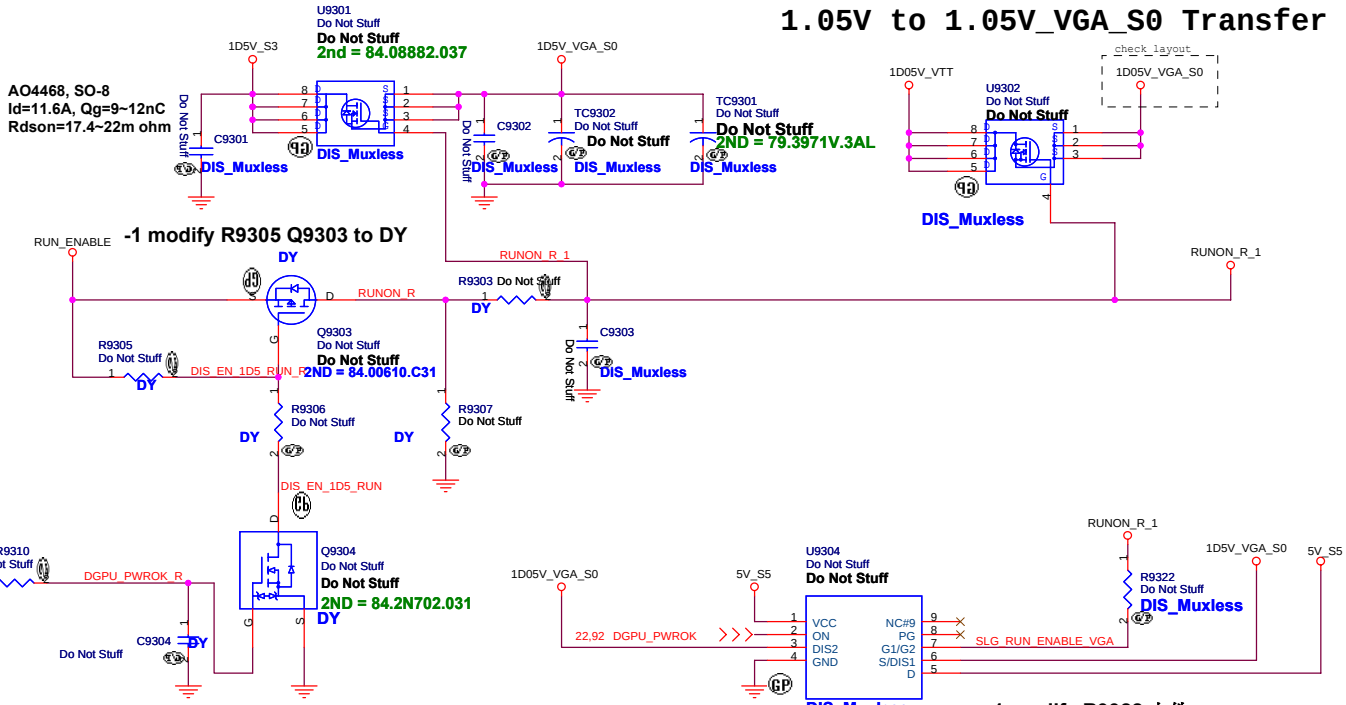
+3VS to 3.3V_DELAY Transfer



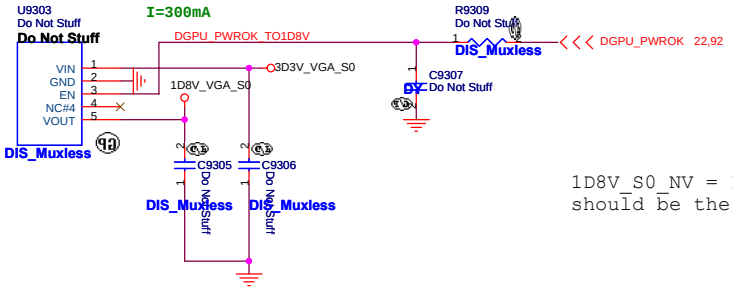
1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

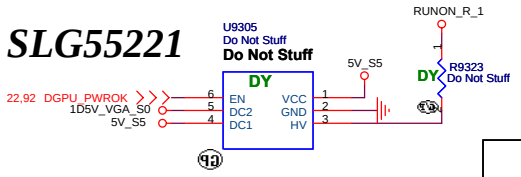


+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



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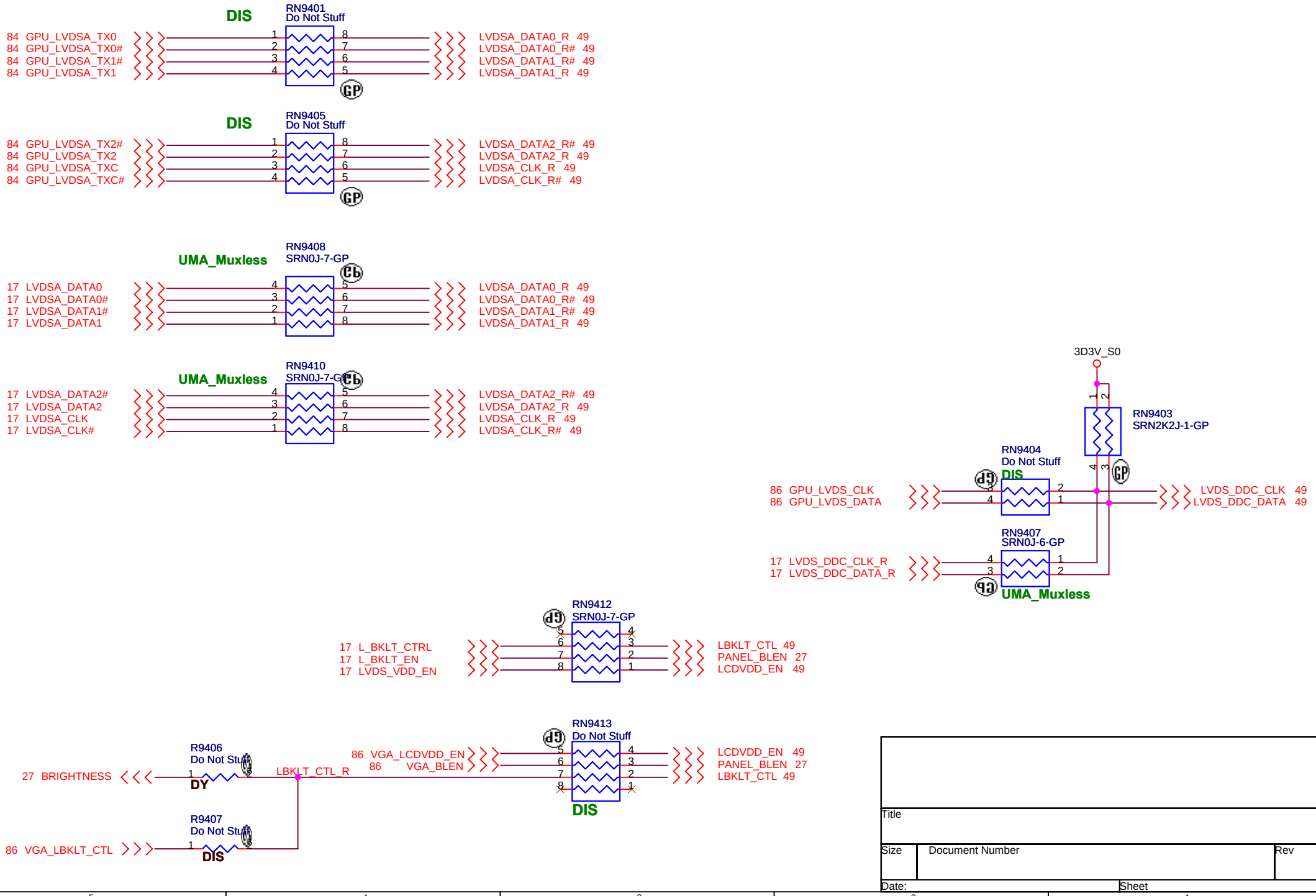
DIS
RN9401
Do Not Stuff
84 GPU_LVDSA_TX0
84 GPU_LVDSA_TX0#
84 GPU_LVDSA_TX1#
84 GPU_LVDSA_TX1
LVDSA_DATA0_R 49
LVDSA_DATA0_R# 49
LVDSA_DATA1_R# 49
LVDSA_DATA1_R 49
DIS
RN9405
Do Not Stuff
84 GPU_LVDSA_TX2#
84 GPU_LVDSA_TX2
84 GPU_LVDSA_TXC
84 GPU_LVDSA_TXC#
LVDSA_DATA2_R# 49
LVDSA_DATA2_R 49
LVDSA_CLK_R 49
LVDSA_CLK_R# 49
UMA_Muxless
RN9408
SRN0J-7-GP
17 LVDSA_DATA0
17 LVDSA_DATA0#
17 LVDSA_DATA1#
17 LVDSA_DATA1
LVDSA_DATA0_R 49
LVDSA_DATA0_R# 49
LVDSA_DATA1_R# 49
LVDSA_DATA1_R 49
UMA_Muxless
RN9410
SRN0J-7-GP
17 LVDSA_DATA2#
17 LVDSA_DATA2
17 LVDSA_CLK
17 LVDSA_CLK#
LVDSA_DATA2_R# 49
LVDSA_DATA2_R 49
LVDSA_CLK_R 49
LVDSA_CLK_R# 49
3D3V_S0
RN9403
SRN2K2J-1-GP
RN9404
Do Not Stuff
DIS
86 GPU_LVDS_CLK
86 GPU_LVDS_DATA
LVDS_DDC_CLK 49
LVDS_DDC_DATA 49
RN9407
SRN0J-6-GP
17 LVDS_DDC_CLK_R
17 LVDS_DDC_DATA_R
UMA_Muxless
RN9412
SRN0J-7-GP
17 L_BKLT_CTRL
17 L_BKLT_EN
17 LVDS_VDD_EN
LBKLT_CTL 49
PANEL_BLEN 27
LCDVDD_EN 49
RN9413
Do Not Stuff
86 VGA_LCDVDD_EN
86 VGA_BLEN
LCDVDD_EN 49
PANEL_BLEN 27
LBKLT_CTL 49
DIS
R9406
Do Not Stuff
27 BRIGHTNESS
LBKLT_CTL_R
DY
R9407
Do Not Stuff
86 VGA_LBKLT_CTL
DIS
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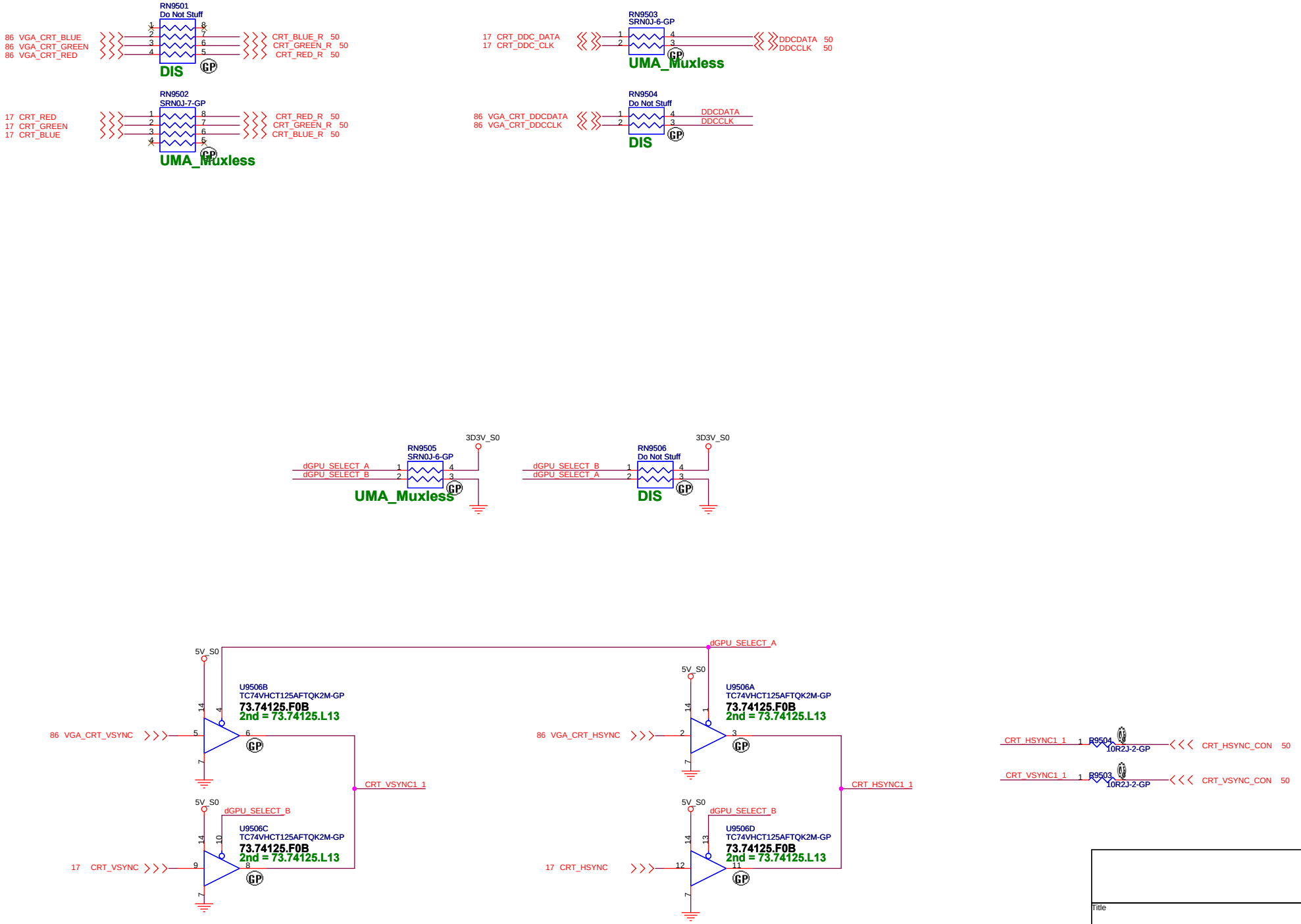
RN9501
Do Not Stuff
86 VGA_CRT_BLUE
86 VGA_CRT_GREEN
86 VGA_CRT_RED
CRT_BLUE_R 50
CRT_GREEN_R 50
CRT_RED_R 50
DIS
RN9503
SRN0J-6-GP
17 CRT_DDC_DATA
17 CRT_DDC_CLK
DDCDATA 50
DDCCLK 50
UMA_Muxless
RN9502
SRN0J-7-GP
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
CRT_RED_R 50
CRT_GREEN_R 50
CRT_BLUE_R 50
UMA_Muxless
RN9504
Do Not Stuff
86 VGA_CRT_DDCDATA
86 VGA_CRT_DDCCLK
DDCDATA
DDCCLK
DIS
3D3V_S0
RN9505
SRN0J-6-GP
dGPU_SELECT_A
dGPU_SELECT_B
UMA_Muxless
3D3V_S0
RN9506
Do Not Stuff
dGPU_SELECT_B
dGPU_SELECT_A
DIS
5V_S0
U9506B
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
86 VGA_CRT_VSYNC
CRT_VSYNC1_1
5V_S0
dGPU_SELECT_B
U9506C
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
17 CRT_VSYNC
dGPU_SELECT_A
5V_S0
U9506A
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
86 VGA_CRT_HSYNC
CRT_HSYNC1_1
5V_S0
dGPU_SELECT_B
U9506D
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
17 CRT_HSYNC
CRT_HSYNC1_1 1
R9504
10R2J-2-GP
CRT_HSYNC_CON 50
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R9503
10R2J-2-GP
CRT_VSYNC_CON 50
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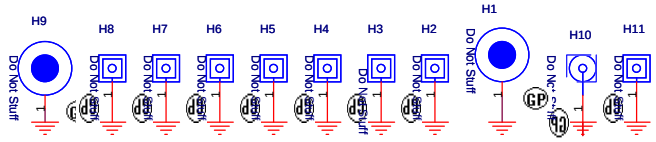
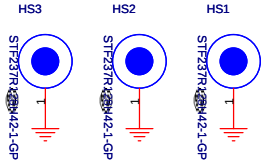
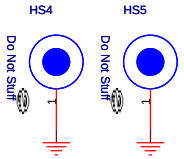


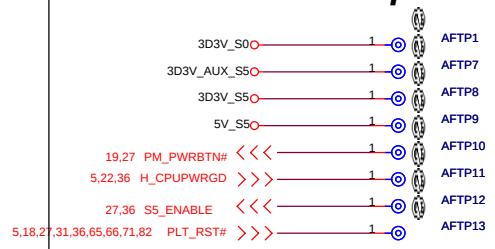
CPU



VGA



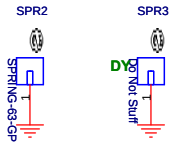
Check test point



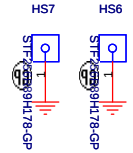
Test Point放在Dimm Door打開可量測處

SB to -1 BOM add SPR2

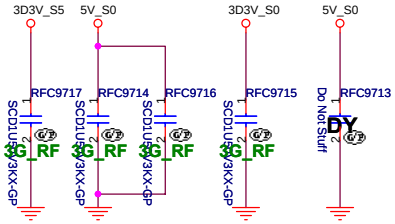
-2 delete SPR5

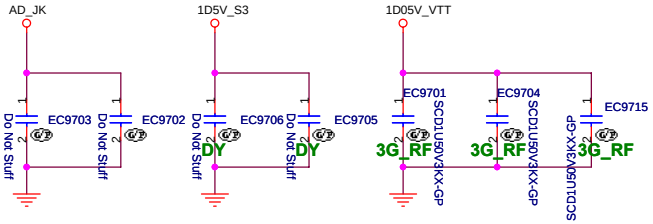


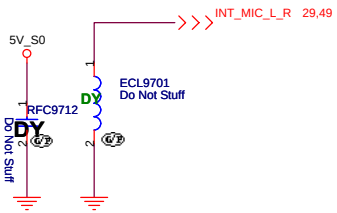
Change:34.40V16.001

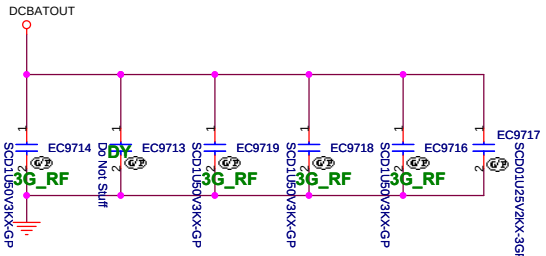


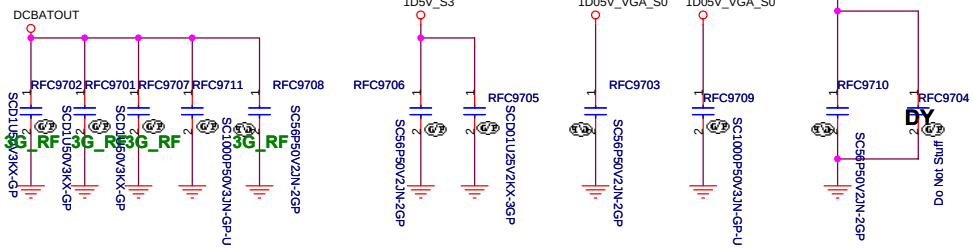
3G Sku

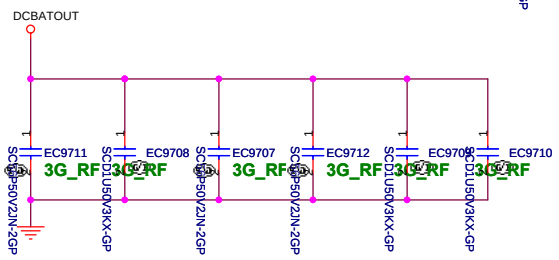












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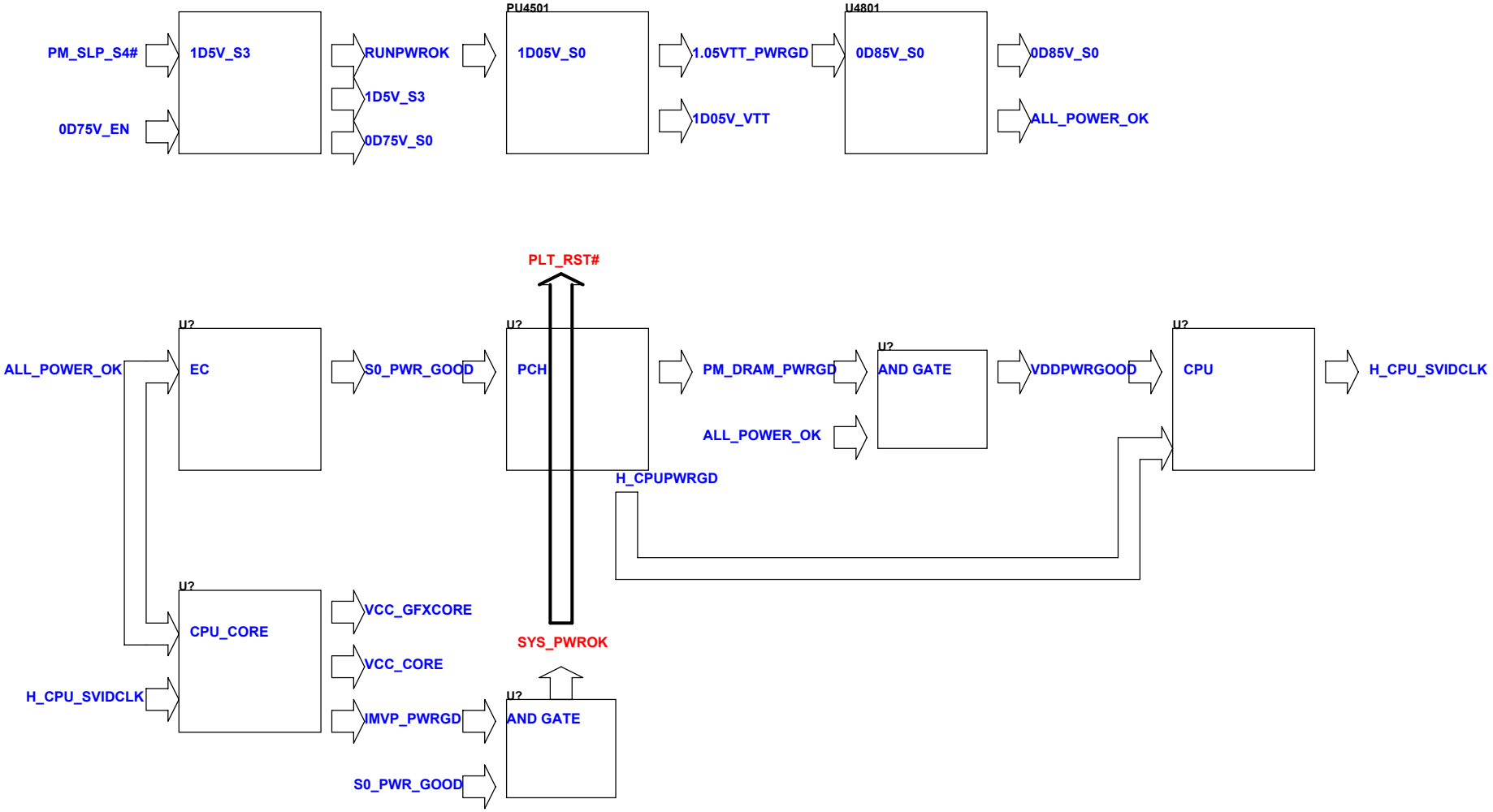

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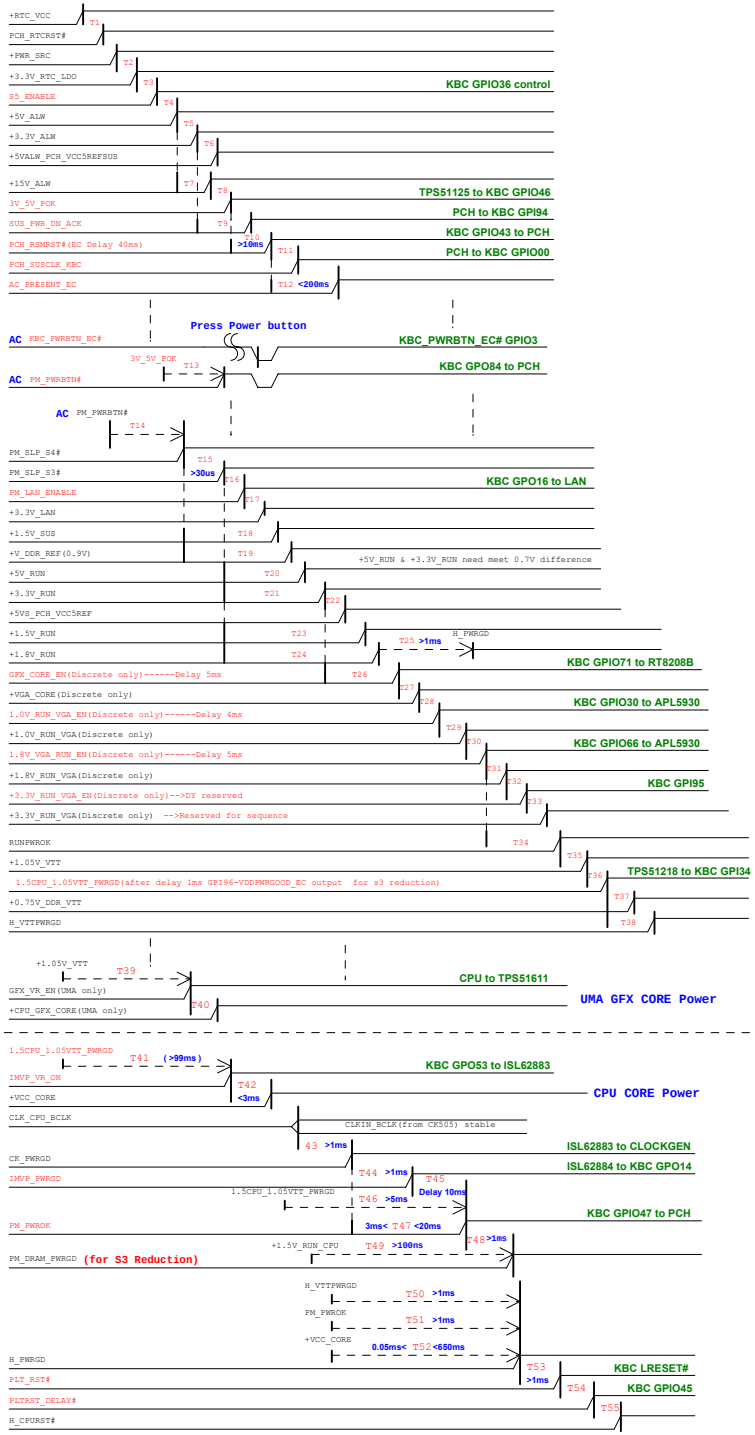
Intel-Power Up Sequence

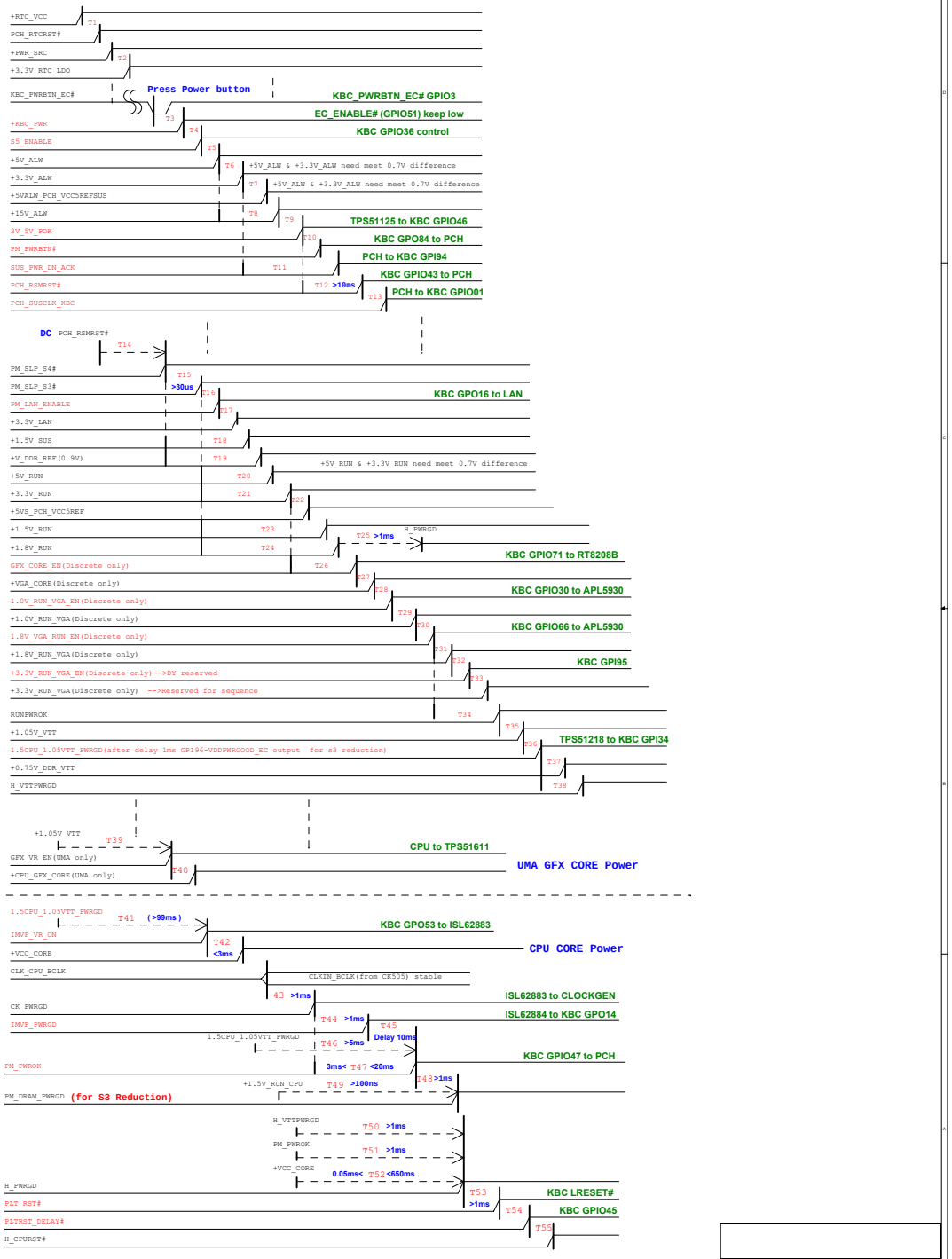
(AC mode)

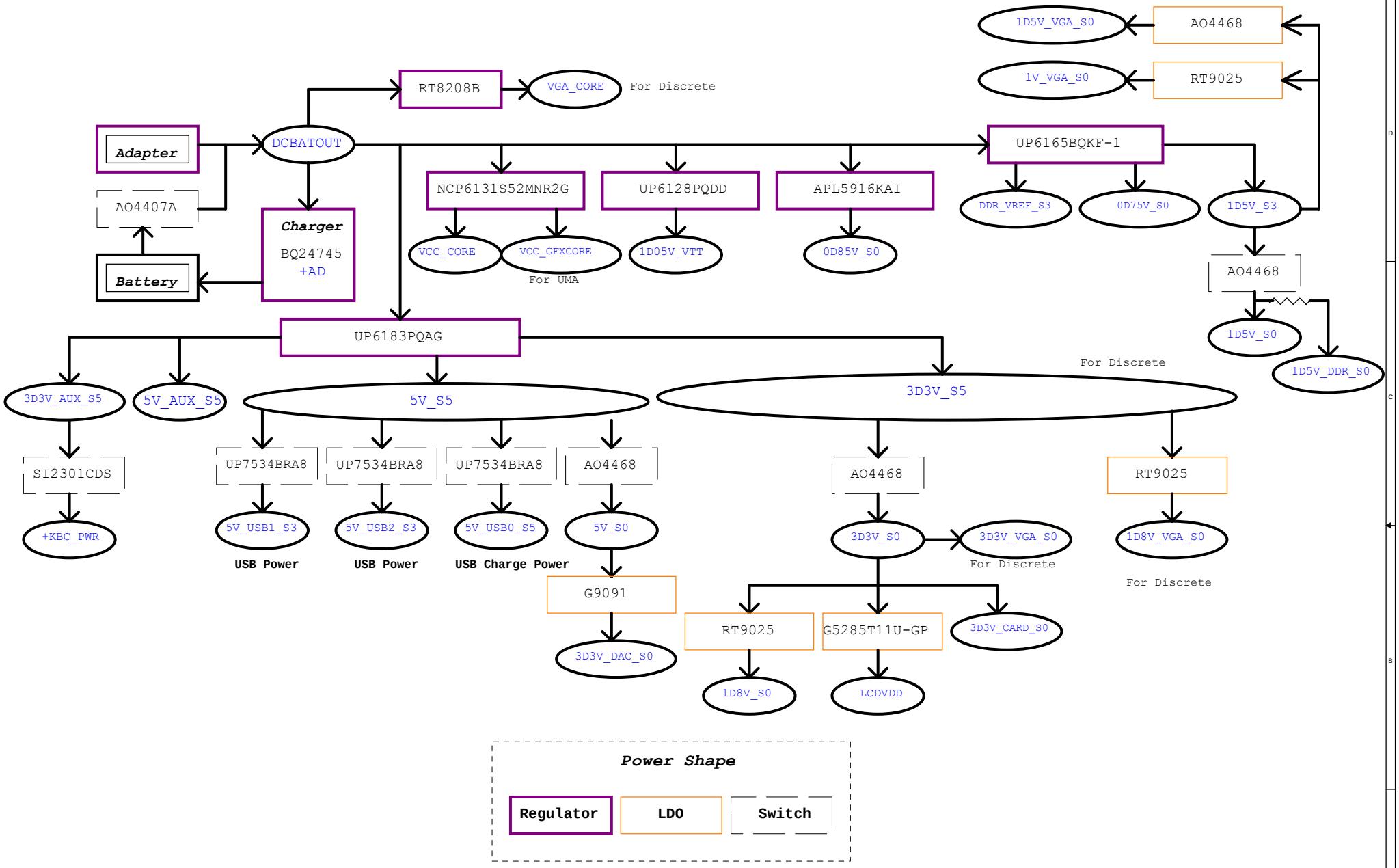
red word: KBC GPIO



(DC mode)

red word: KBC GPIO





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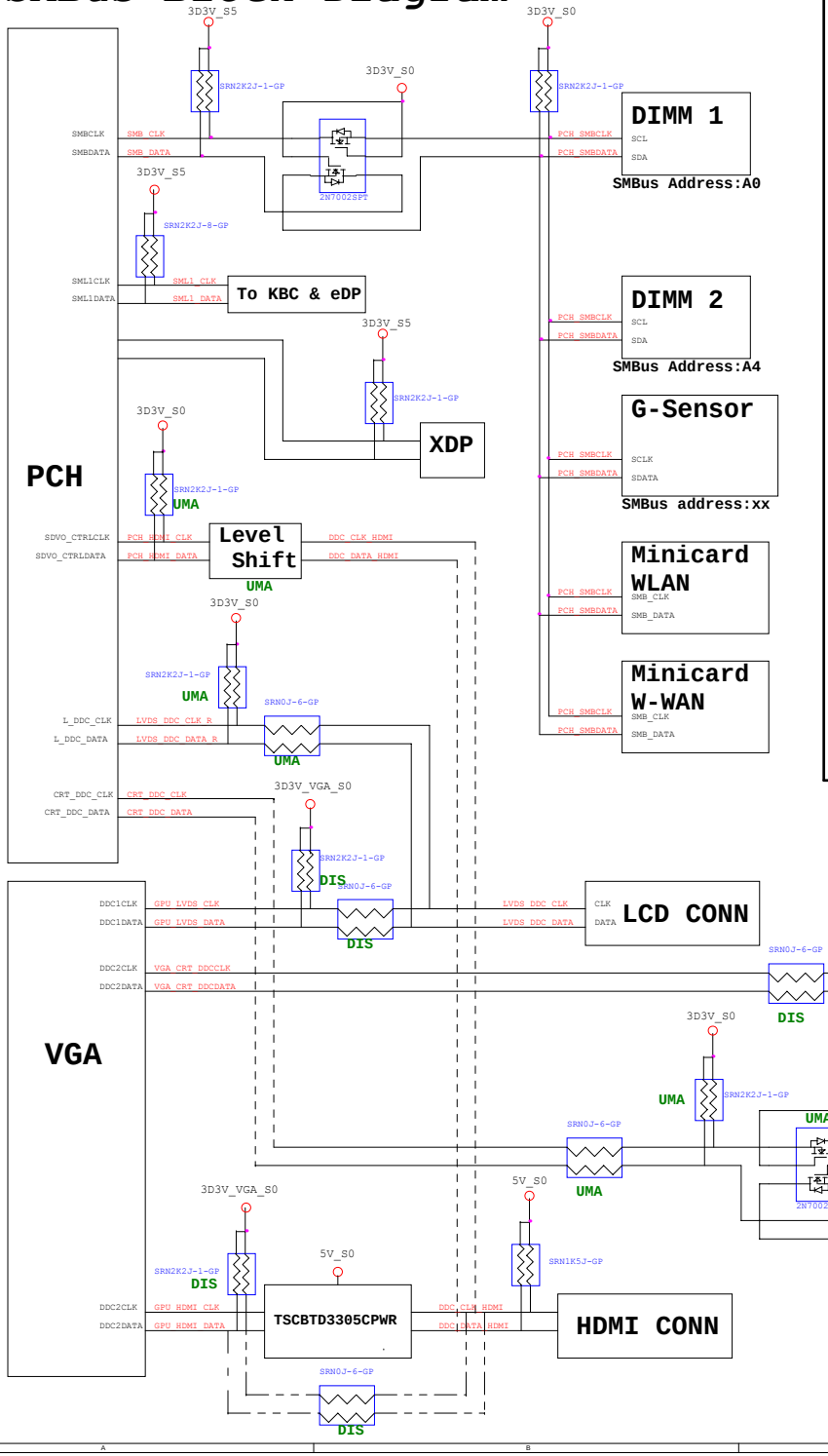
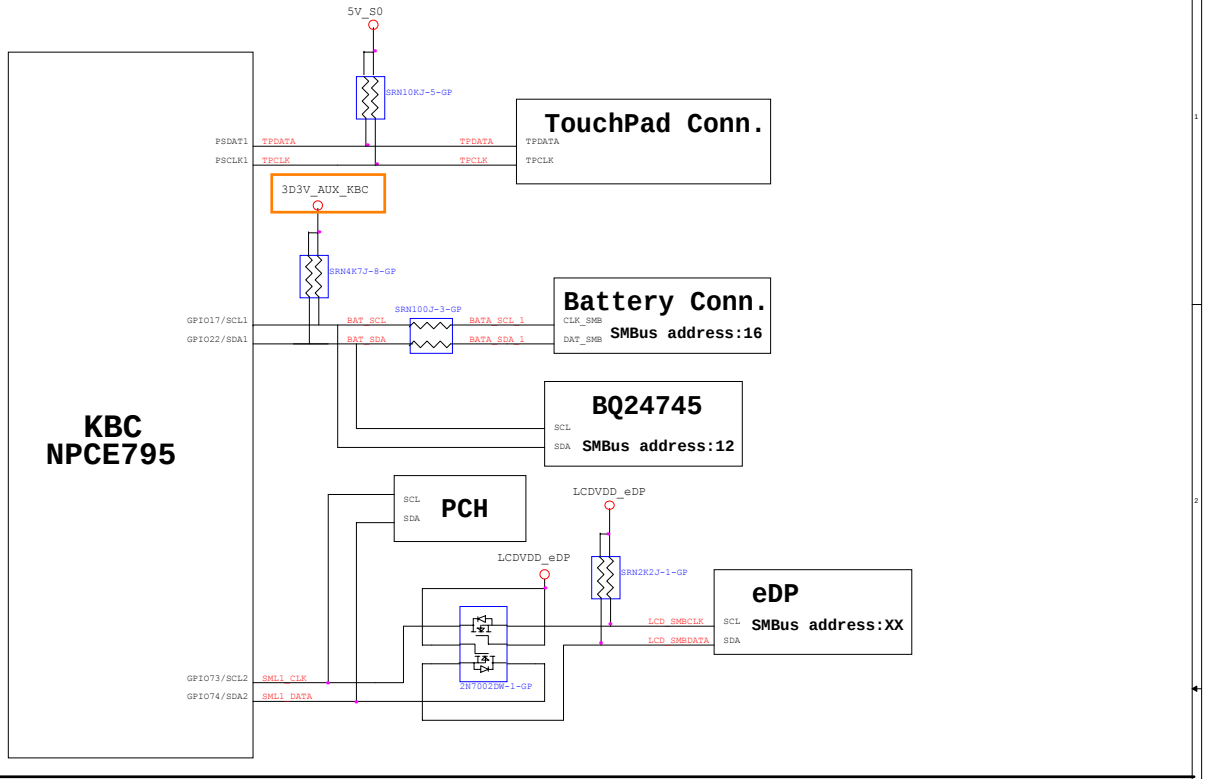
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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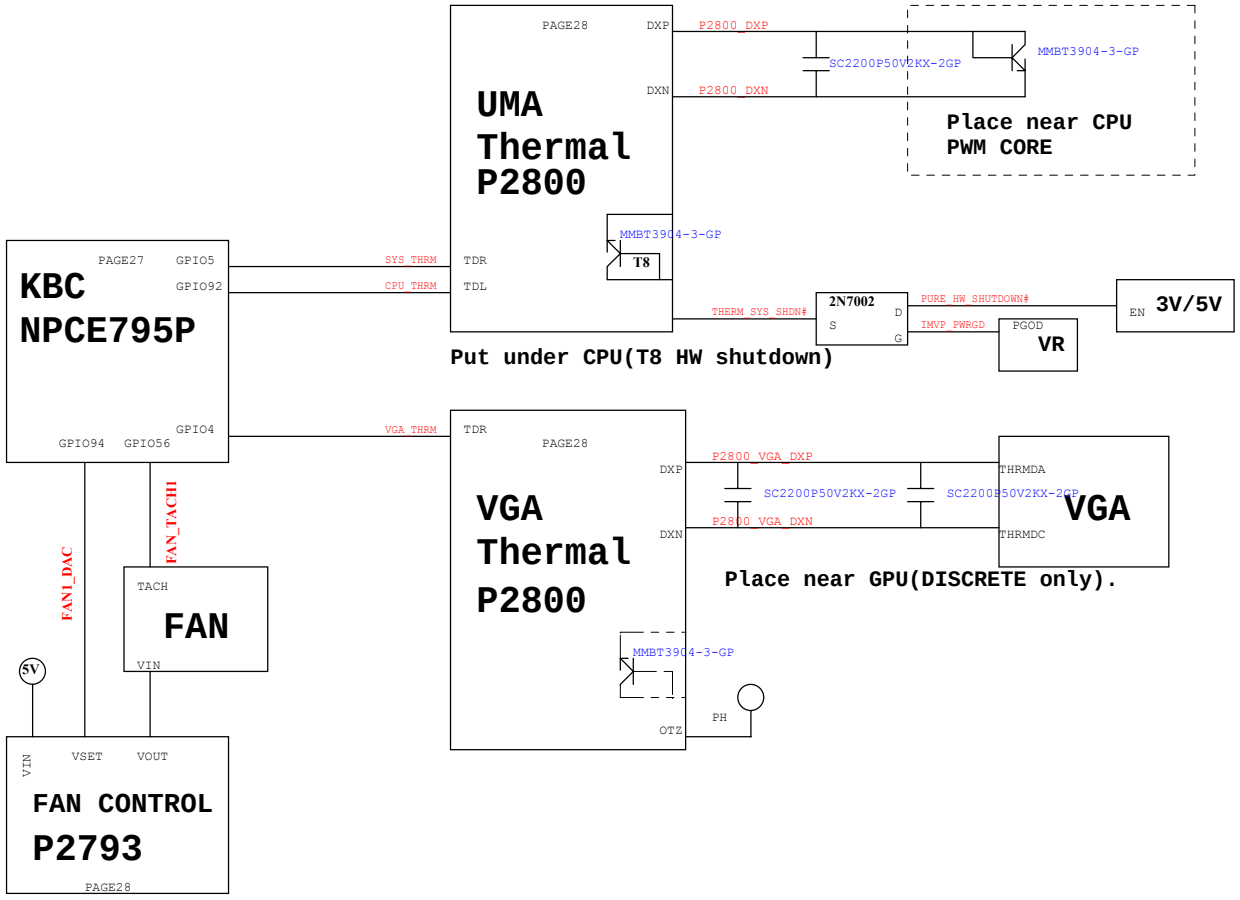
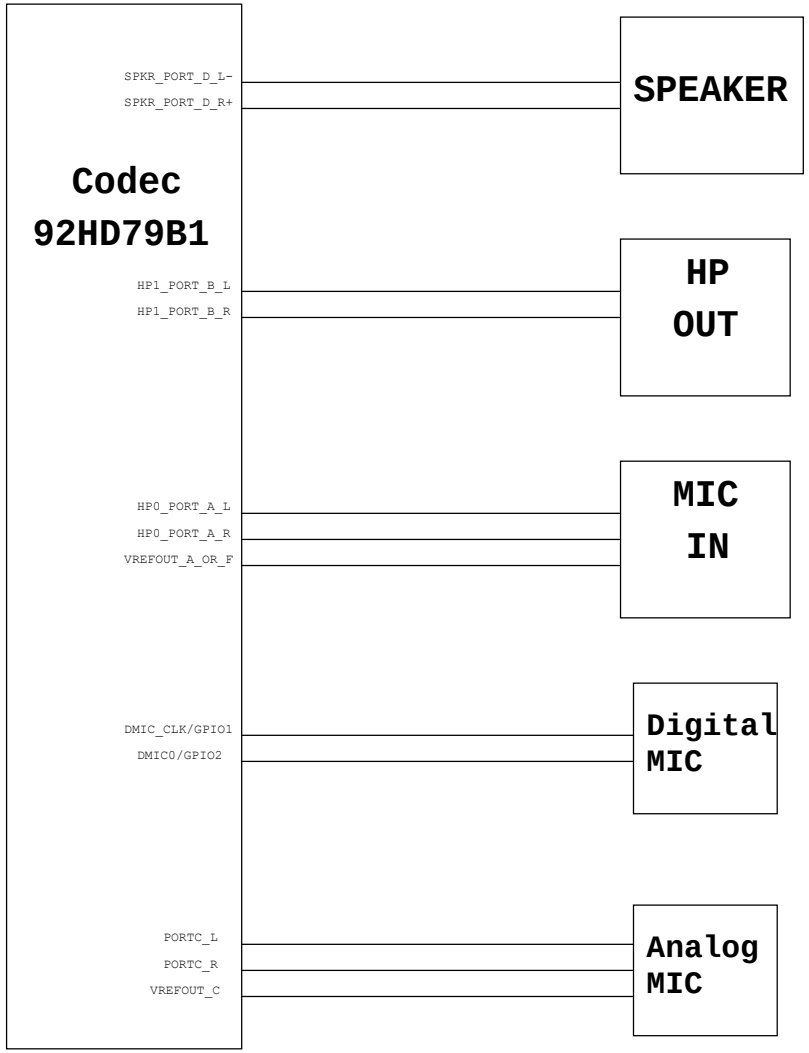
Thermal Block Diagram



Audio Block Diagram



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