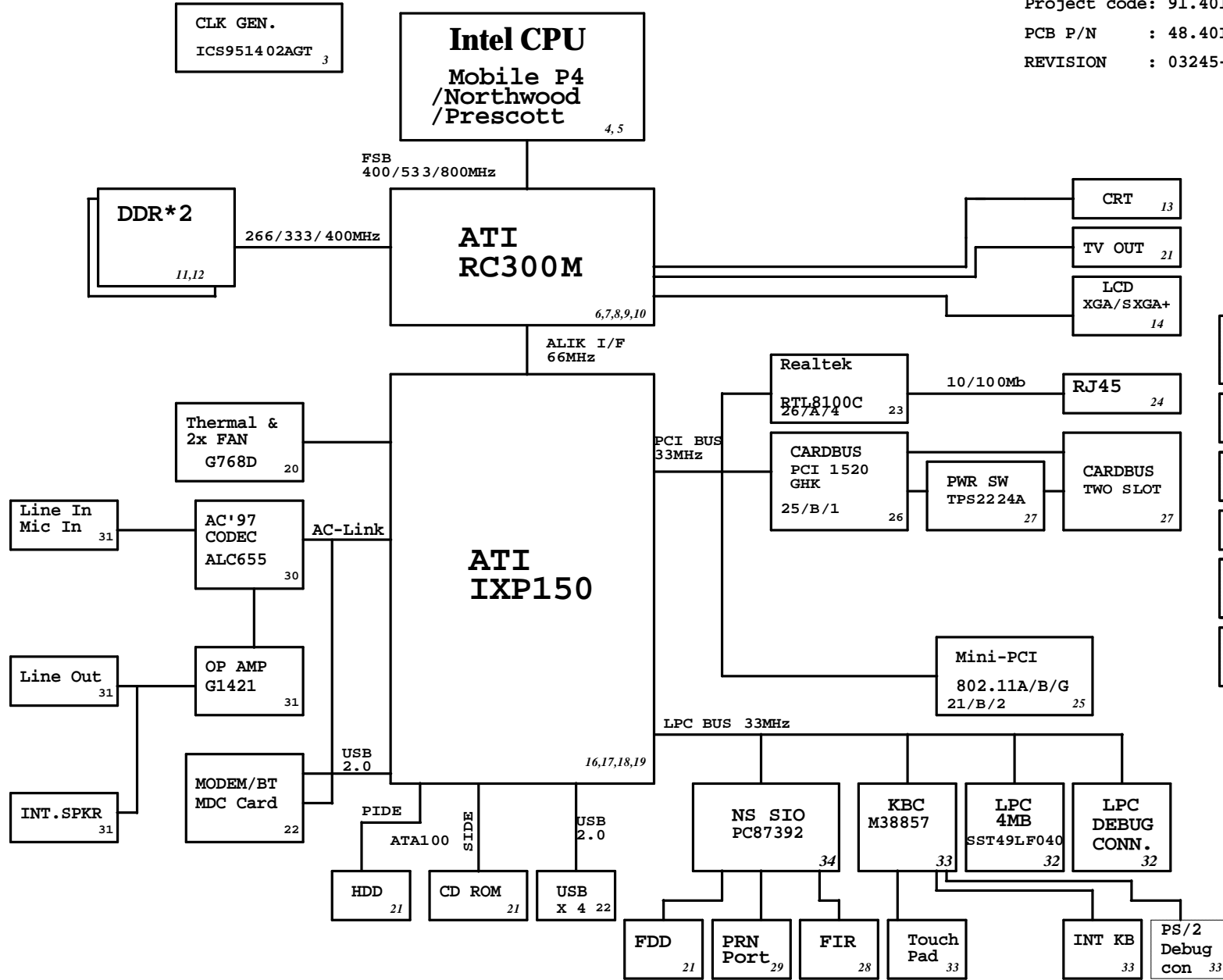


YUHINA2&3 Block Diagram

Project code: 91.40I01.001
 PCB P/N : 48.40I01.0SB
 REVISION : 03245-2



SYSTEM DC/DC TPS51020DBT 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 5V_S3 5V_S0 3D3V_S5 3D3V_S3 3D3V_S0
SYSTEM DC/DC TPS5110 37	
INPUTS	OUTPUTS
DCBATOUT	2D5V_S5 1D5V_S0
APL5331 36	
2D5V_S3	1D25V_S0

CPU DC/DC MAX1546AETL 39,40 CM2843ACIM25 39	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 1.3V 44A +VID 1.2V 0.3A

MAXIM CHARGER MAX1909 41	
INPUTS	OUTPUTS
DCBATOUT	BT+ 1.8V 4.0A UP+5V 5V 10.0mA

PCB LAYER	
L1:	Signal 1
L2:	VCC/GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	Signal 4



- Micro-P ATTINY12L-4SI 42
- BAT CONN 43
- AD CONN 43
- INVERTER 14
- Power Button 35
- EMI 45



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 Taipei Hsien 221, Taiwan, R.O.C.




Title: **BLOCK DIAGRAM**


Size	Document Number	Rev
Custor	YUHINA2&3	-2



Date: Tuesday, March 23, 2004 Sheet 1 of 46




1D2V_VID  1D2V_VID 4,5,39
 1D5V_S0  1D5V_S0 6,9,15,36,45




 2D5V_S0  2D5V_S0 7,15,18,44,45
 2D5V_S3  2D5V_S3 8,9,11,12,18,36,37,44,45



 3D3V_S0  3D3V_S0 3,4,6,7,9,11,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,30,32,33,34,35,39,44,45,46
 3D3V_S3  3D3V_S3 8,14,16,17,18,19,30,33,44,45
 3D3V_S5  3D3V_S5 4,8,17,18,19,22,30,35,36,38,44,45


 3D3V_LAN_S5  3D3V_LAN_S5 22,23,24,44




 5V_USB1_S0  5V_USB1_S0 22
 5V_USB3_S0  5V_USB3_S0 22

 5V_CRT_S0  5V_CRT_S0 13
 5VA_AUD_S0  5VA_AUD_S0 30,31,46
 5V_S0  5V_S0 6,9,13,14,15,18,20,21,22,25,27,29,30,31,32,33,34,36,39,40,42,44,45

 5V_S5  5V_S5 15,37,38,42,44
 +5V_UP_S5  +5V_UP_S5 14,42,45
 5V_AUX_S5  5V_AUX_S5 16,20,35,38,39,41,42,43,45,46

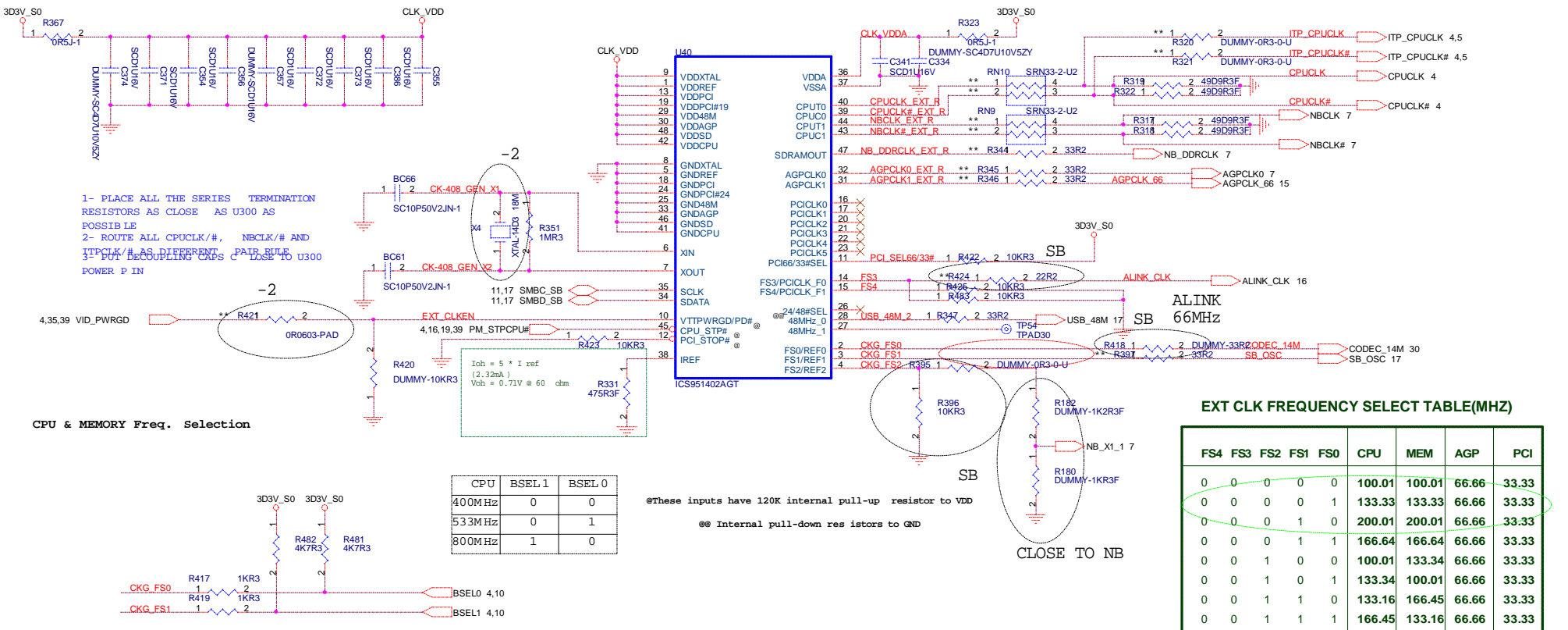
 LCDVDD  LCDVDD 14
 AD+  AD+ 41,43,45

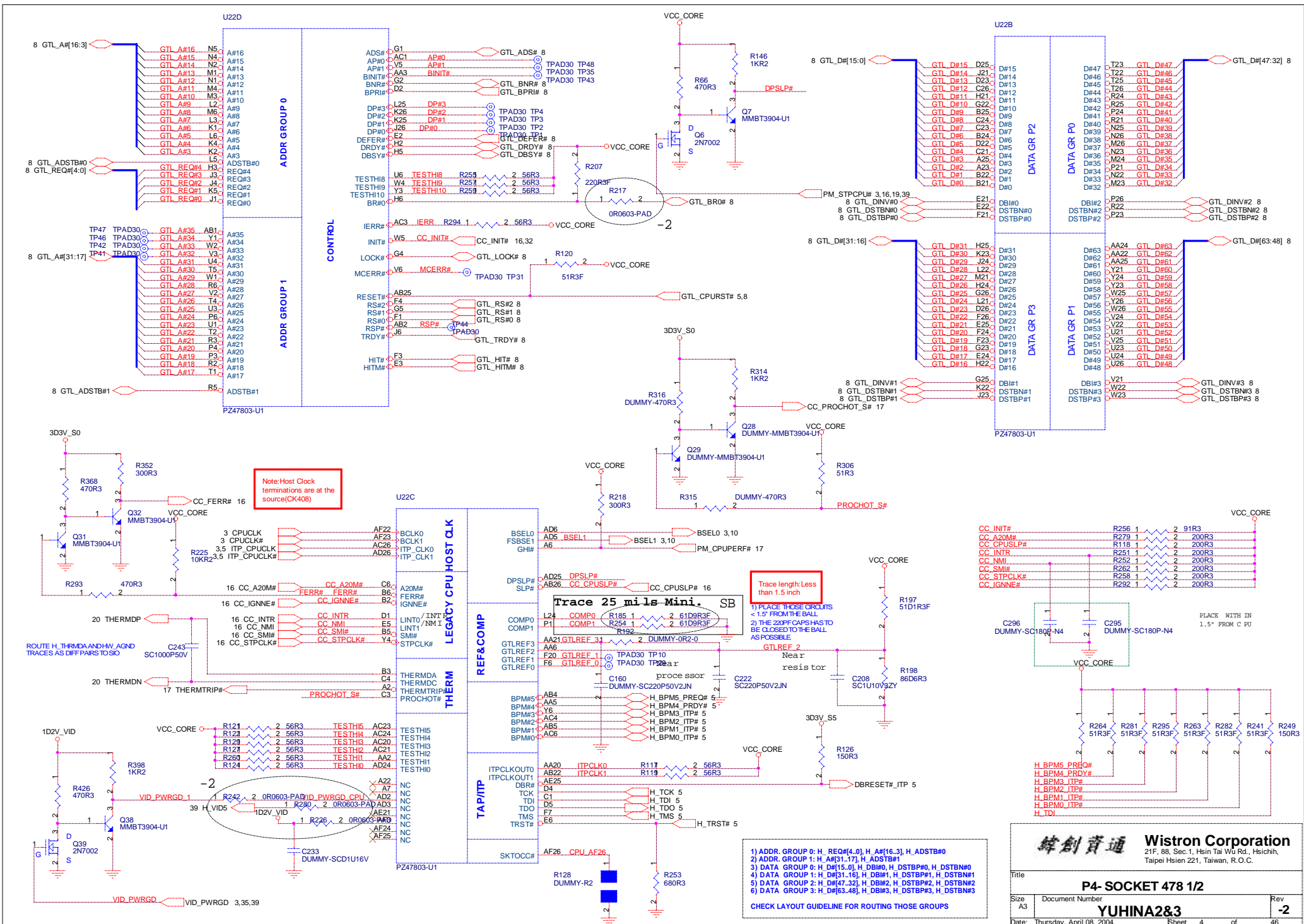
 DCBATOUT  DCBATOUT 14,15,18,20,35,37,38,40,41,42,44,45,46

 VCC_FAN  VCC_FAN 20
 A_SKT_VCC_S0  A_SKT_VCC_S0 26,27
 A_SKT_VPP_S0  A_SKT_VPP_S0 27

PCI DEVICE RESOURCE ASSIGNMENT

	BUS	DEVICE	IDSEL	PCI_REQ#	PCI_GNT#	INT_IRQ#
LAN	1	5	PCI_AD26	REQ#4	GNT#4	IRQD#
CardBus	1	9	PCI_AD20	REQ#1	GNT#1	IRQB# / IRQA#
MiniPCI	1	6	PCI_AD21	REQ#2	GNT#2	IRQE#





Note: Host Clock terminations are at the source (CK408)

Trace length: Less than 1.5 inch

- 1) ADDR. GROUP 0: H. REQ#(4..0), H. A#(16..3), H. ADSTB#0
 - 2) ADDR. GROUP 1: H. A#(31..17), H. ADSTB#1
 - 3) DATA GROUP 0: H. D#(15..0), H. DB#0, H. DSTB#0, H. DSTBN#0
 - 4) DATA GROUP 1: H. D#(63..48), H. DB#1, H. DSTB#1, H. DSTBN#1
 - 5) DATA GROUP 2: H. D#(47..32), H. DB#2, H. DSTB#2, H. DSTBN#2
 - 6) DATA GROUP 3: H. D#(63..48), H. DB#3, H. DSTB#3, H. DSTBN#3
- CHECK LAYOUT GUIDELINE FOR ROUTING THOSE GROUPS

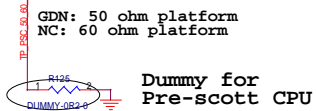
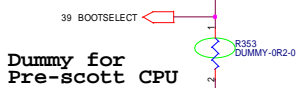
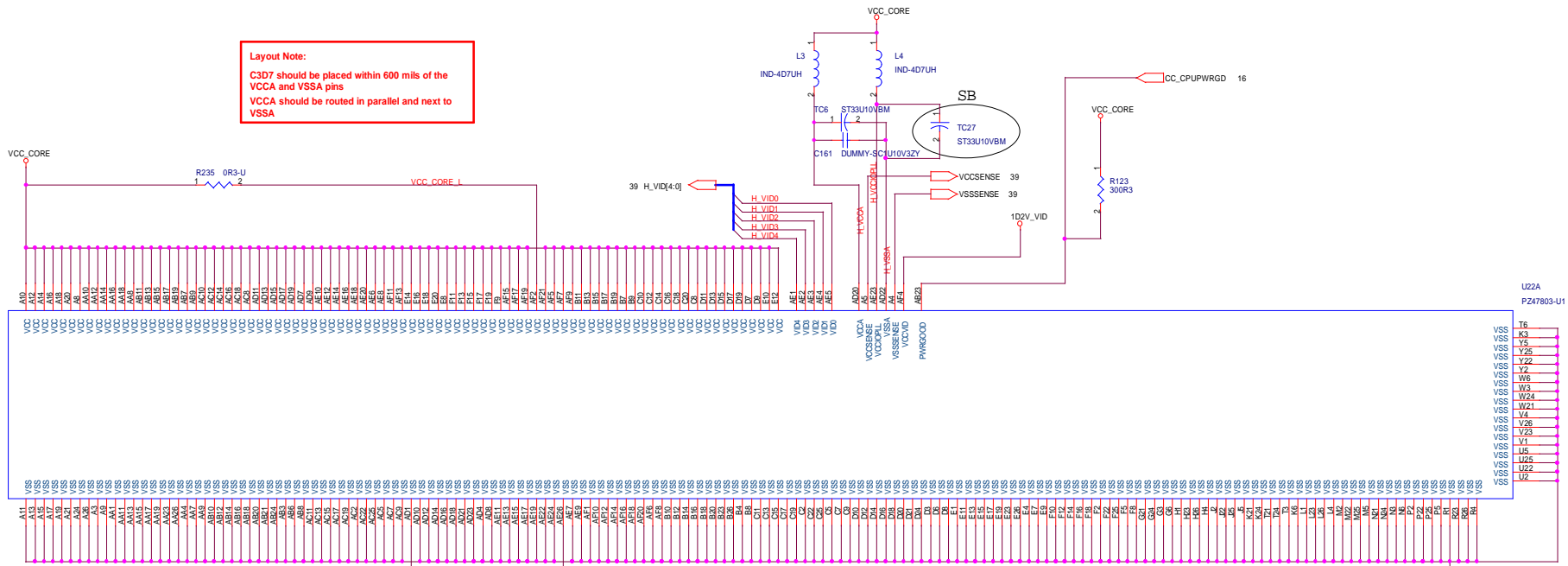
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **P4-SOCKET 478 1/2**

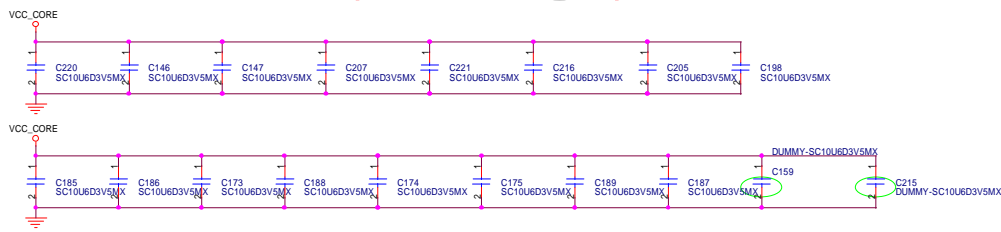
Size: A3 Document Number: **YUHINA2&3** Rev: **-2**

Date: Thursday, April 08, 2004 Sheet 4 of 46

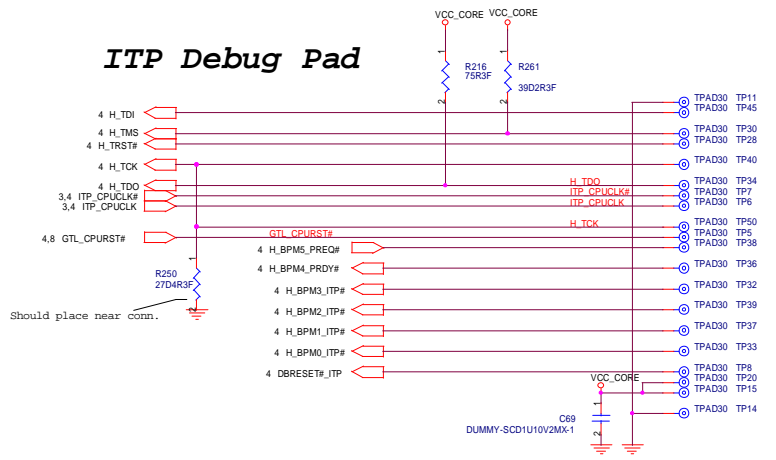
Layout Note:
 C3D7 should be placed within 600 mils of the VCCA and VSSA pins
 VCCA should be routed in parallel and next to VSSA



**10U/X5R 1206 DECOUPLING CAPS
 8X IN SOCKET CAVITY
 10X IN CRB**

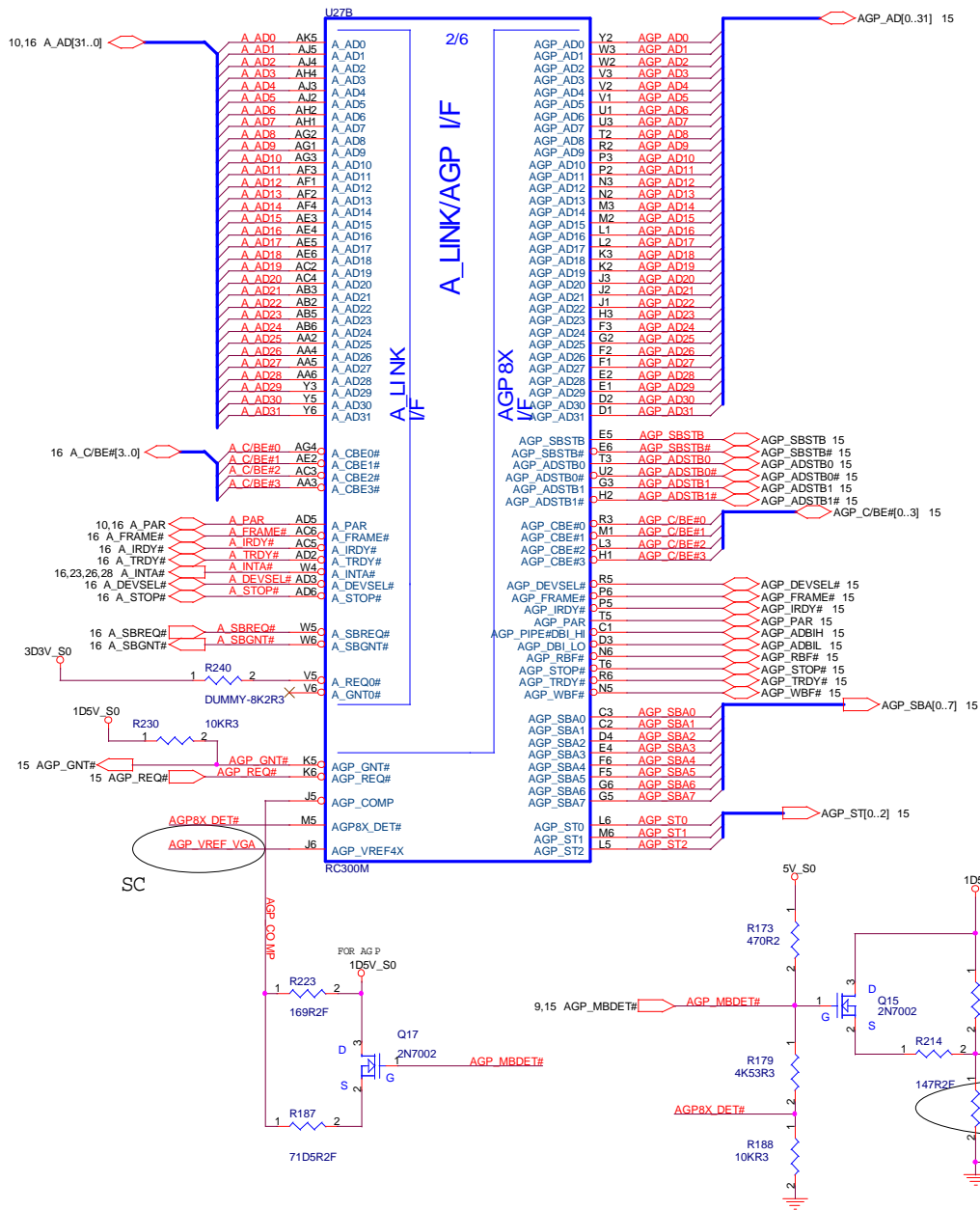


ITP Debug Pad



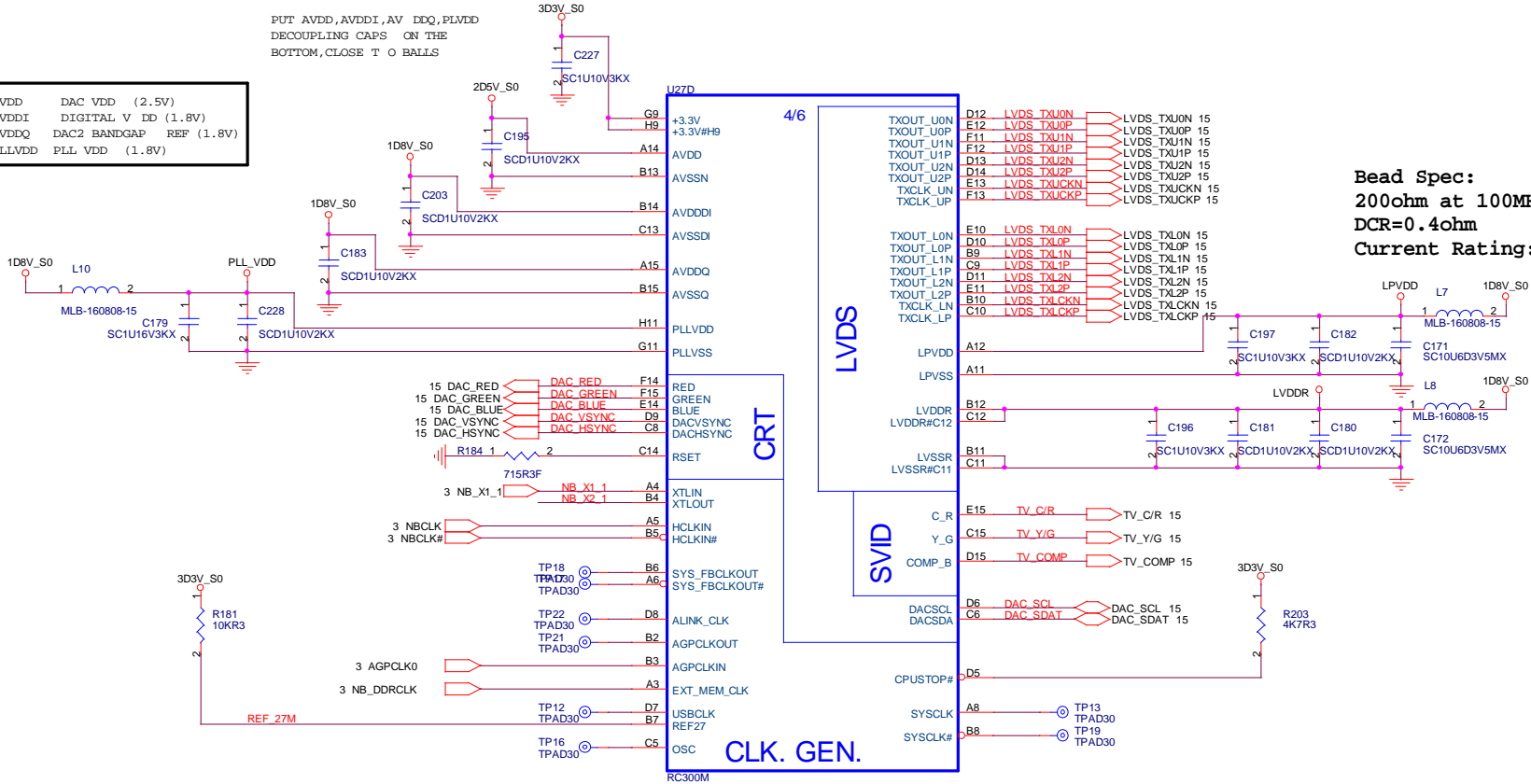
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			P4- SOCKET 478 2/2
Size	Document Number	Rev	
Custom	YUHINA2&3	-2	
Date:	Thursday, April 08, 2004	Sheet	5 of 46

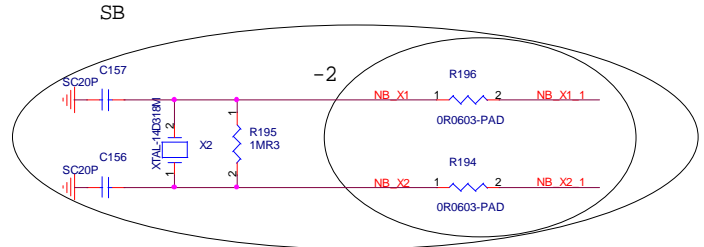


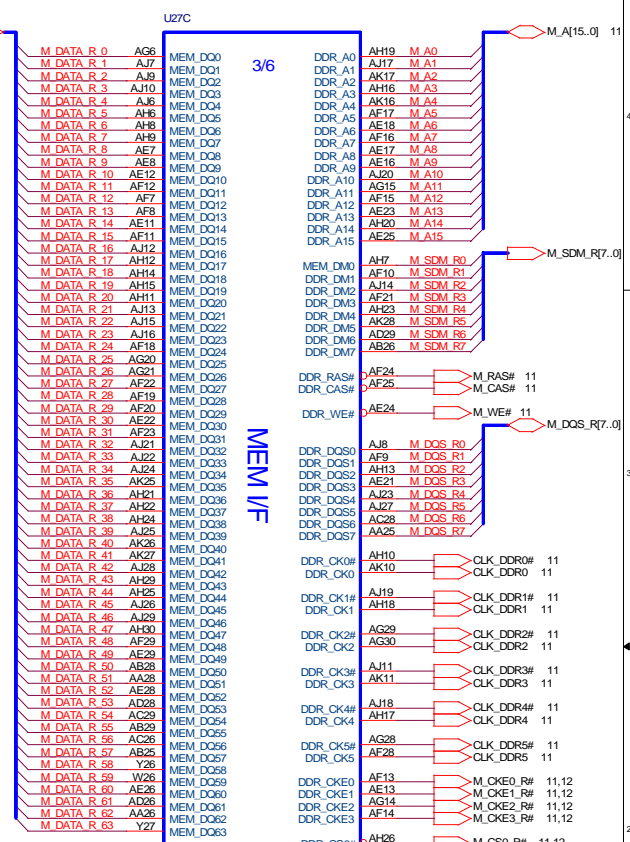
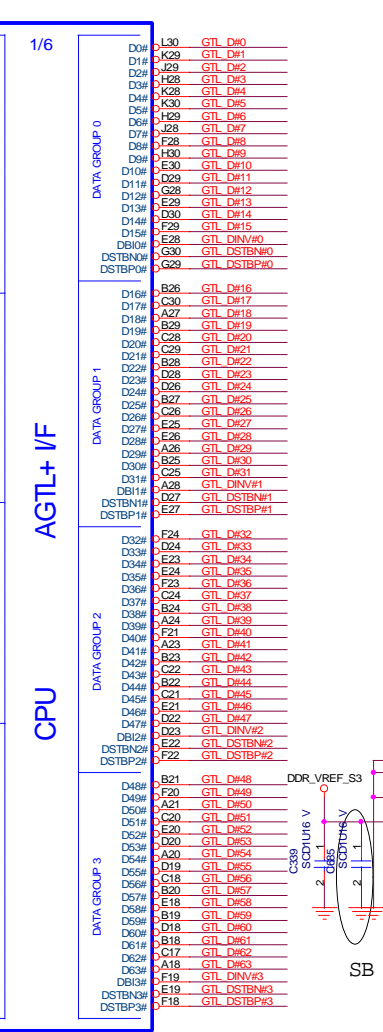
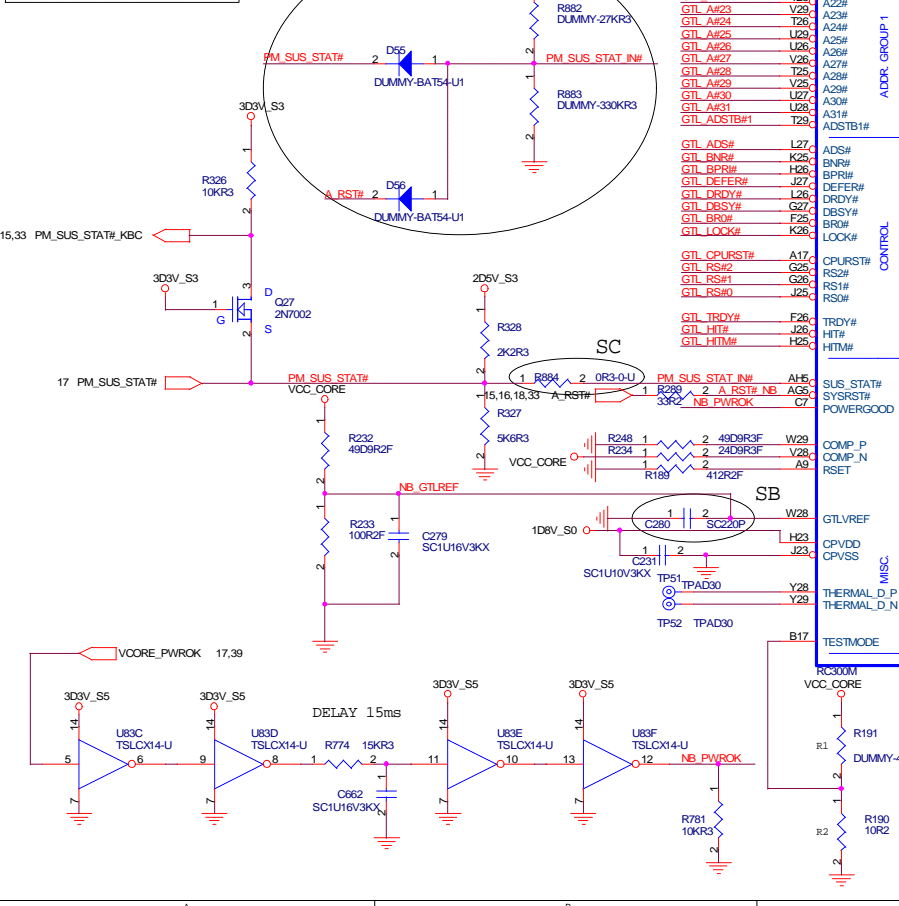
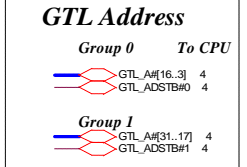
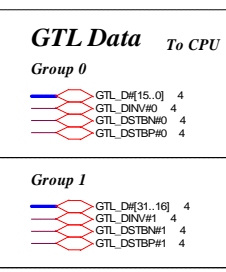
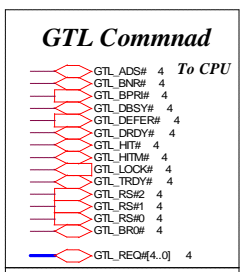
AVDD DAC VDD (2.5V)
 AVDDI DIGITAL V DD (1.8V)
 AVDDQ DAC2 BANDGAP REF (1.8V)
 PLLVDD PLL VDD (1.8V)

PUT AVDD,AVDDI,AV DDQ,PLVDD
 DECOUPLING CAPS ON THE
 BOTTOM,CLOSE T O BALLS



Bead Spec:
200ohm at 100MHZ
DCR=0.4ohm
Current Rating: 200mA





RESISTOR	RC300M MODE
R1	TEST MODE
R2	NORMAL MODE

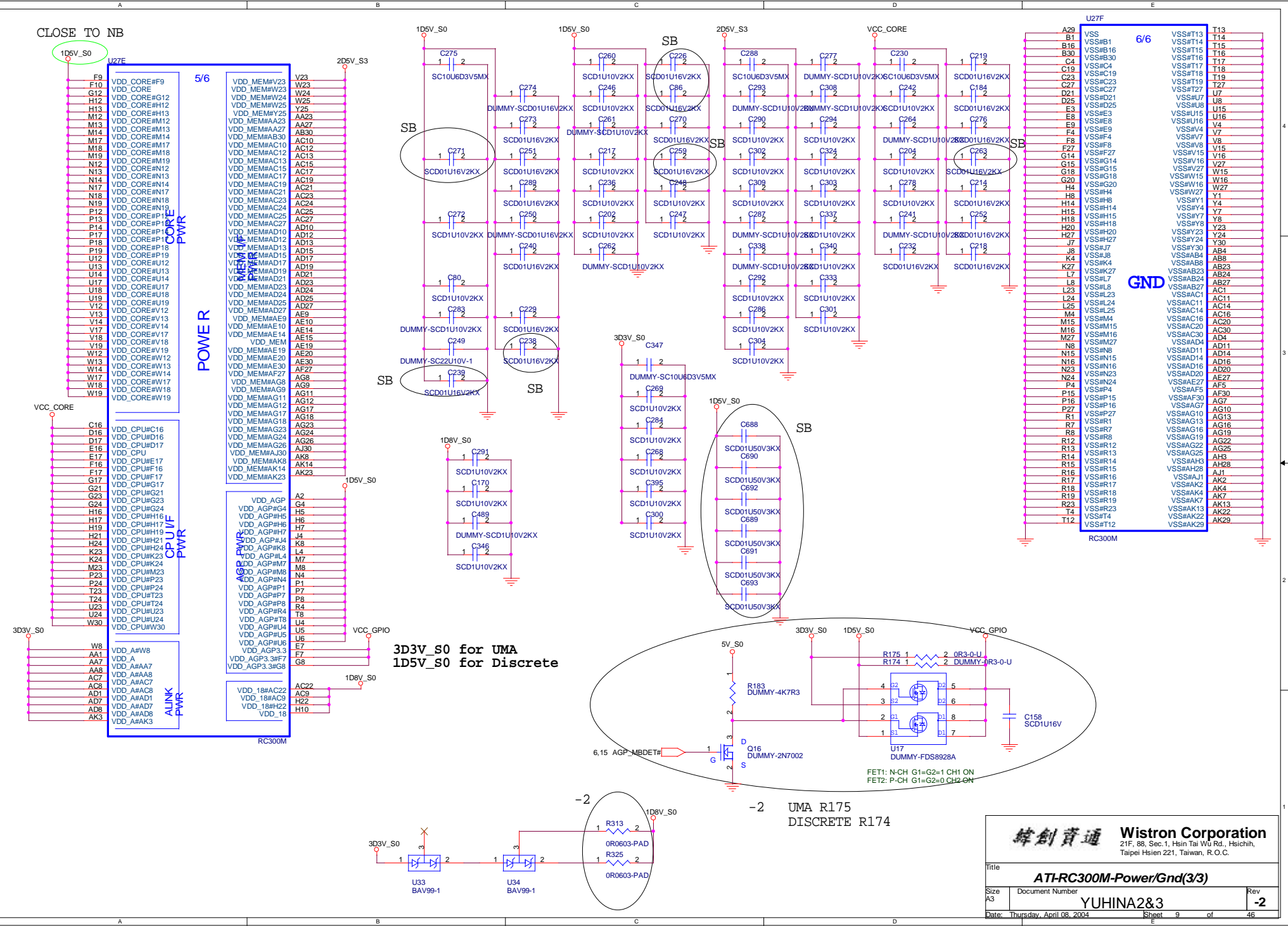
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ATI RC300M (2/3)

Size: Custom | Document Number: YUHINA283 | Rev: -2

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CLOSE TO NB



3D3V_S0 for UMA
1D5V_S0 for Discrete

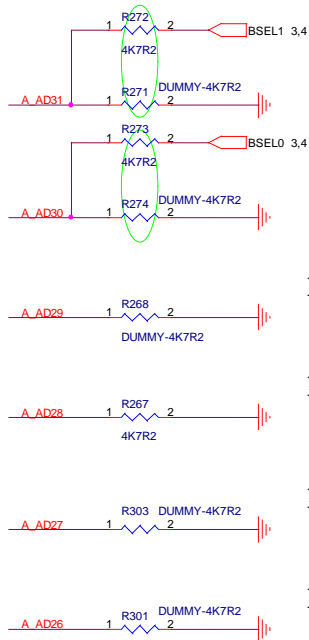
UMA R175
DISCRETE R174

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Title: **ATI-RC300M-Power/Gnd(3/3)**

Size A3 Document Number **YUHINA2&3** Rev **-2**

Date: Thursday, April 08, 2004 Sheet 9 of 46



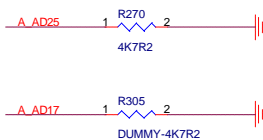
A_AD[31..30] : FSB CLK SPEED
 Default : 00
 00: 100MHZ
 01: 133MHZ
 10: 200MHZ
 11: 166MHZ

A_AD29 : STRAP CONFIGURATION
 Default : 1
 0: REDUCED SET
 1: FULL SET

A_AD28 : SPREAD SPECTRUM ENABLE
 Default : 0
 0: DISABLE SS
 1: ENABLE SS

A_AD27 : FrcShortTReset#
 Default : 1
 0: TESTE MODE
 1: NORMAL MODE

A_AD26 : ENABLE IOQ
 Default : 1
 0: IOQ=1
 1: IOQ=12



A_AD25,A_AD17 : CPU VOLTAGE[1..0]
 Default : 01
 00: 1.05V (MOBILE CPU)
 01: 1.35V (MOBILE CPU)
 10: 1.45V (DESKTOP CPU)
 11: 1.75V (DESKTOP CPU)



A_AD24 : MOBILE CPU SELECT
 Default : 1
 0: BANIAS CPU
 1: NOT BANIAS CPU



A_AD23 : CLOCK BYPASS DISABLE
 Default : 1
 0: TEST MODE
 1: NORMAL OPERATION



A_AD22 : OSC PAD OUTPUT PCICLK
 Default : 1
 0: OSC PIN DRIVES PCICLK
 1: OSC PIN DRIVES OSC CLK



A_AD21 : AUTO_CAL ENABLE
 Default : 1
 0: DISABLE AUTO_CAL
 1: ENABLE AUTO_CAL

RC300M STRAPPING



A_AD20 : INTERNAL CLK GEN ENABLE
 Default : 1
 0: EXTERNAL CLOCK GENERATOR
 1: INTERNAL CLOCK GENERATOR



A_AD19 : MEMORY IO VOLTAGE SELECTION
 Default : 1
 0: 1.8V
 1: 2.5V



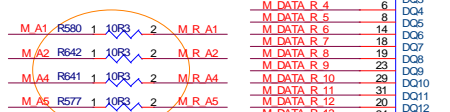
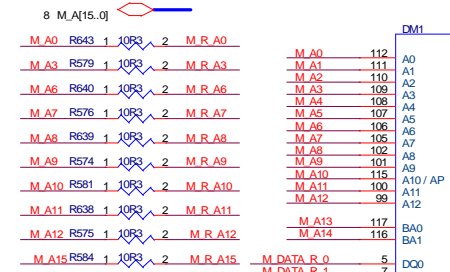
A_AD18 : ENABLE PHASE CALIBRATION
 Default : 0
 0: DISABLE
 1: ENABLE



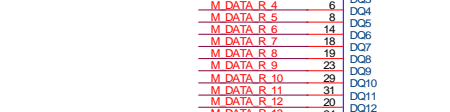
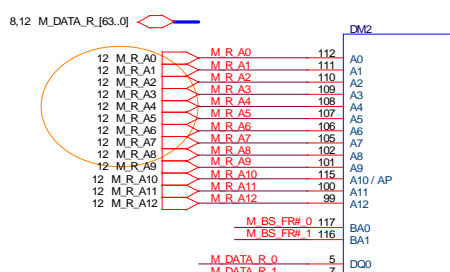
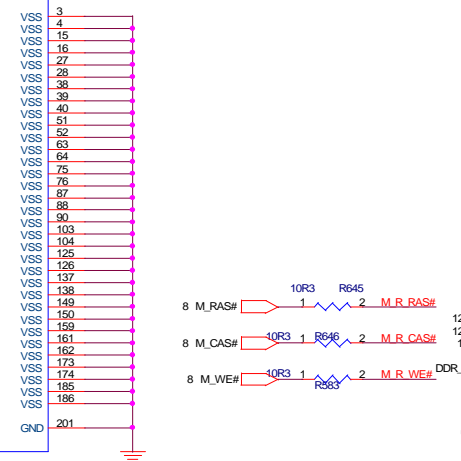
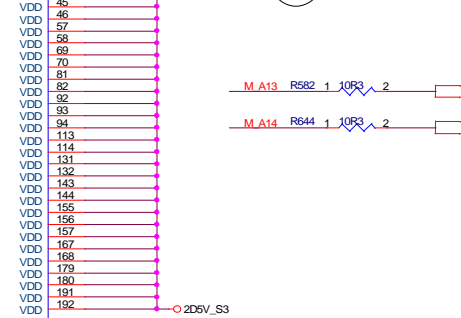
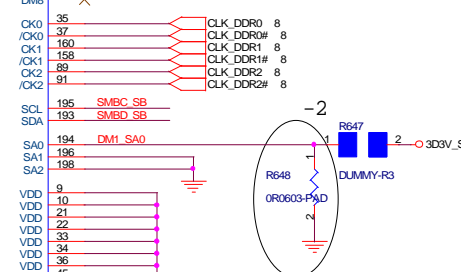
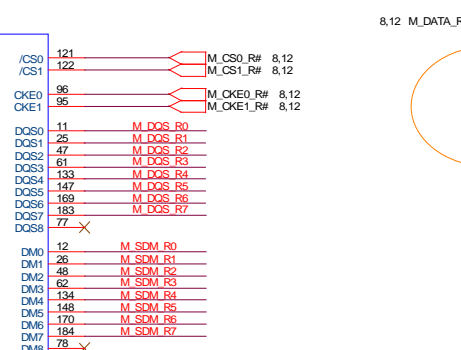
PAR : EXTENDED DEBUG MODE
 Default : 1
 0: DEBUG MODE
 1: NORMAL OPERATION

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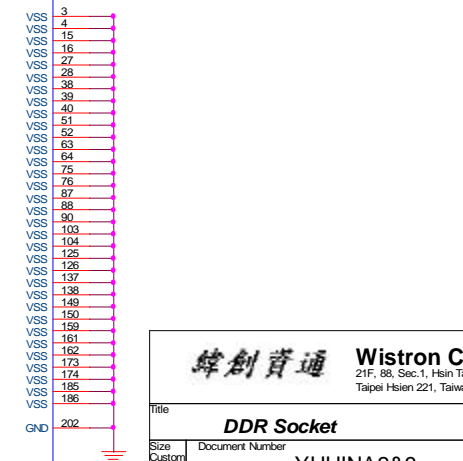
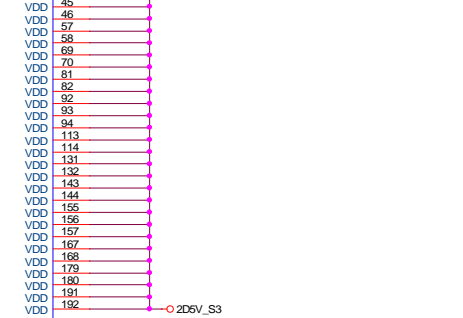
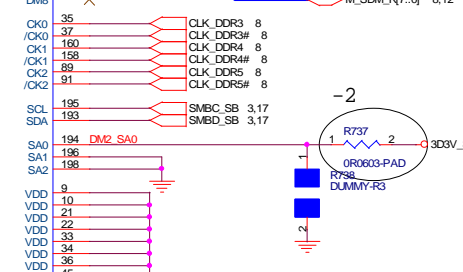
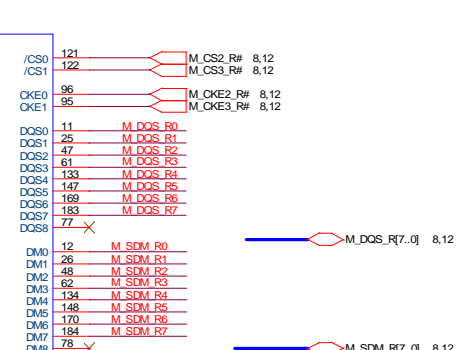
Title		NB STRAPPING	
Size	Document Number	Rev	
A3	YUHINA2&3	-2	
Date: Thursday, April 08, 2004	Sheet 10	of	46



REVERSE TYPE



NORMAL TYPE

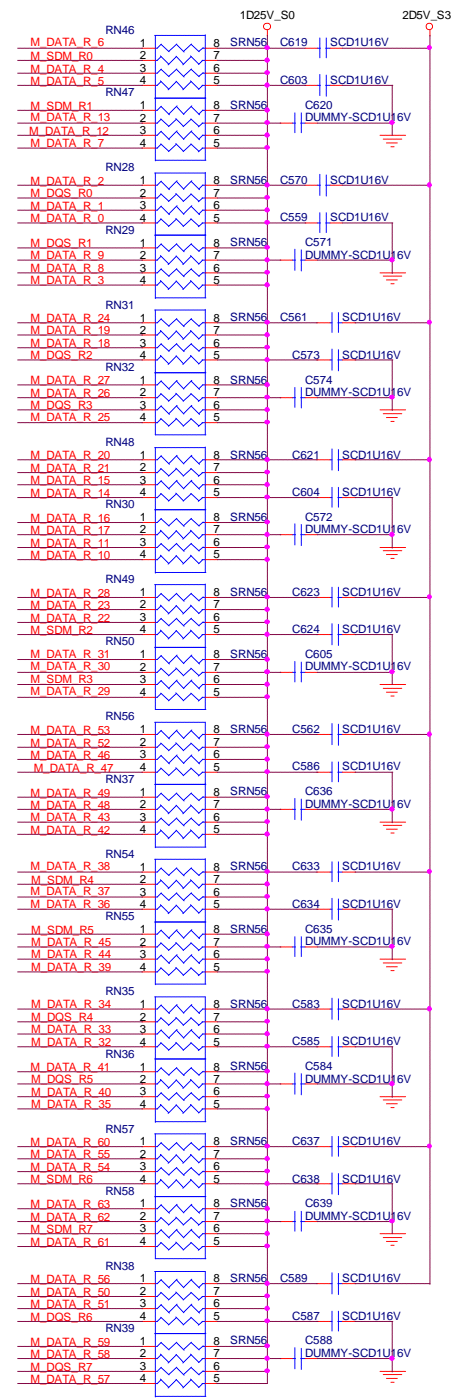
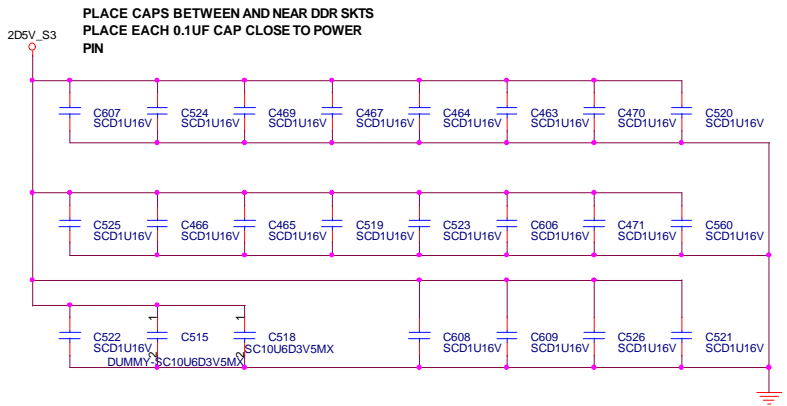


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Taipai Hsien 221, Taiwan, R.O.C.

Title: **DDR Socket**

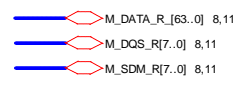
Size: Custom Document Number: **YUHINA2&3** Rev: **-2**

Date: Thursday, April 08, 2004 Sheet 11 of 46

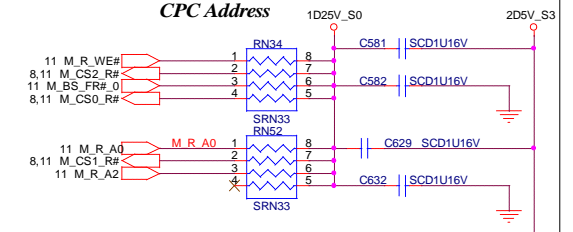


PARALLEL TERMINATION

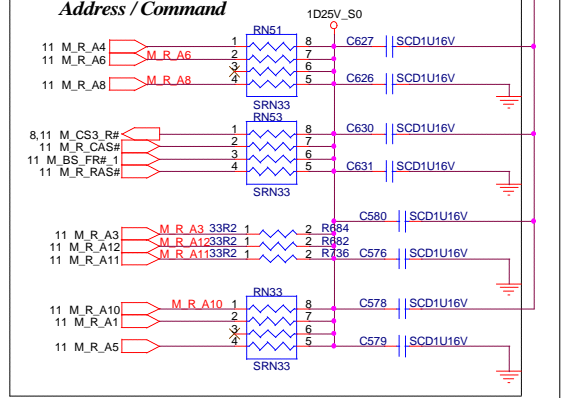
PULL HIGH STUBS < 0.8", PLACE Rps CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



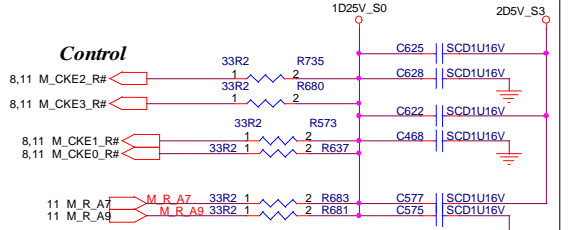
CPC Address



Address / Command



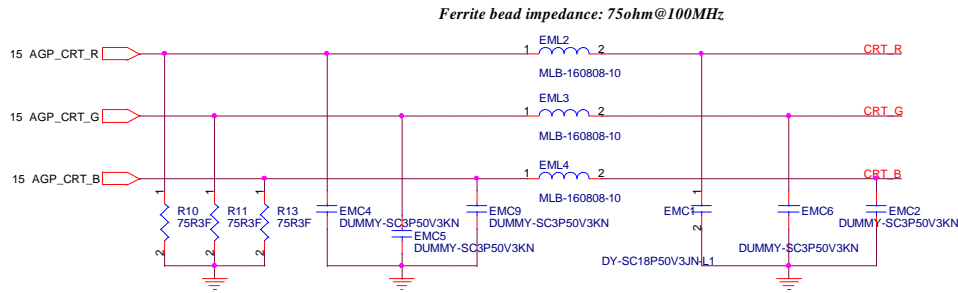
Control



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Title		
DDR Serial/Terminator Resistor		
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Date: Thursday, April 08, 2004	Sheet 12 of 46	

CRT I/F & CONNECTOR

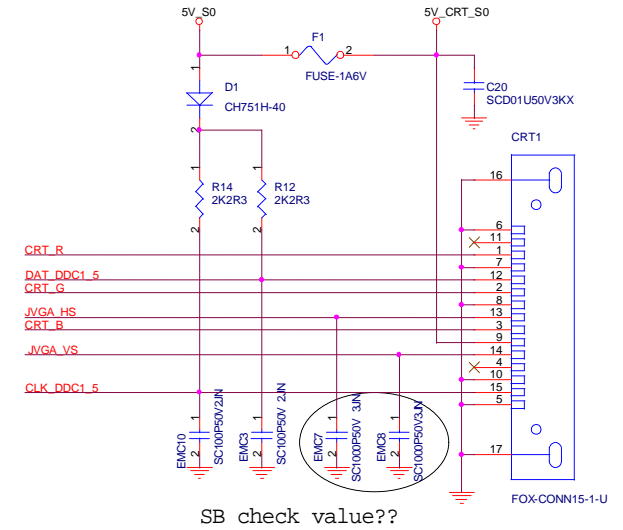


Layout Note:

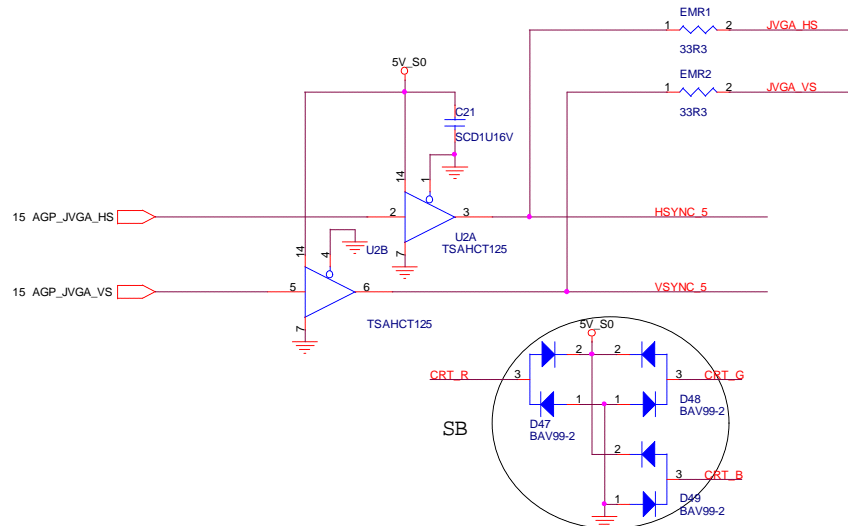
- * Must be a ground return path between this ground and the ground on the VGA connector.
- * 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

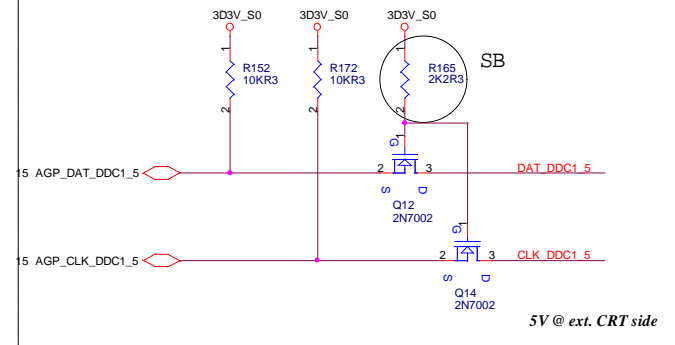
RDDP 1.0



Hsync & Vsync level shift



DDC_CLK & DATA level shift

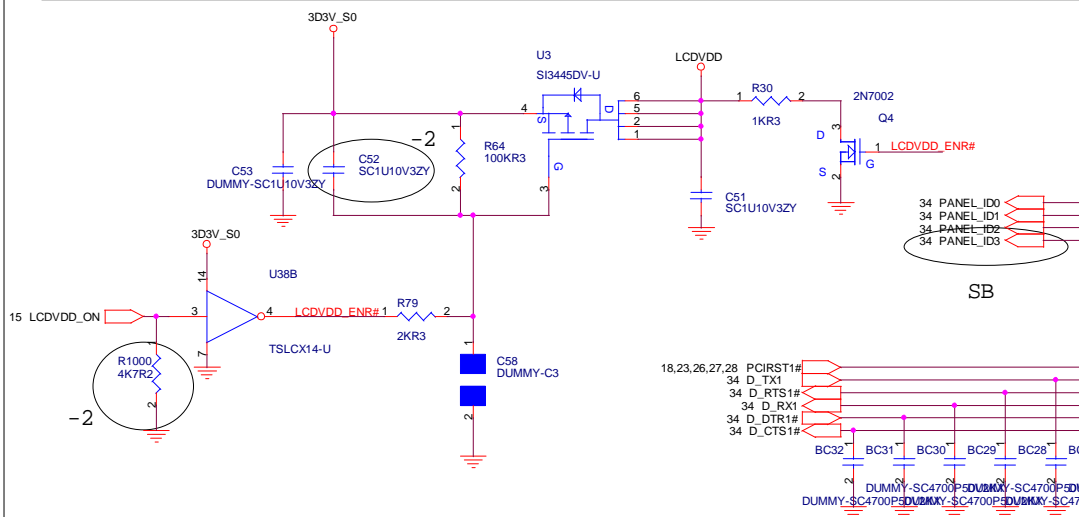
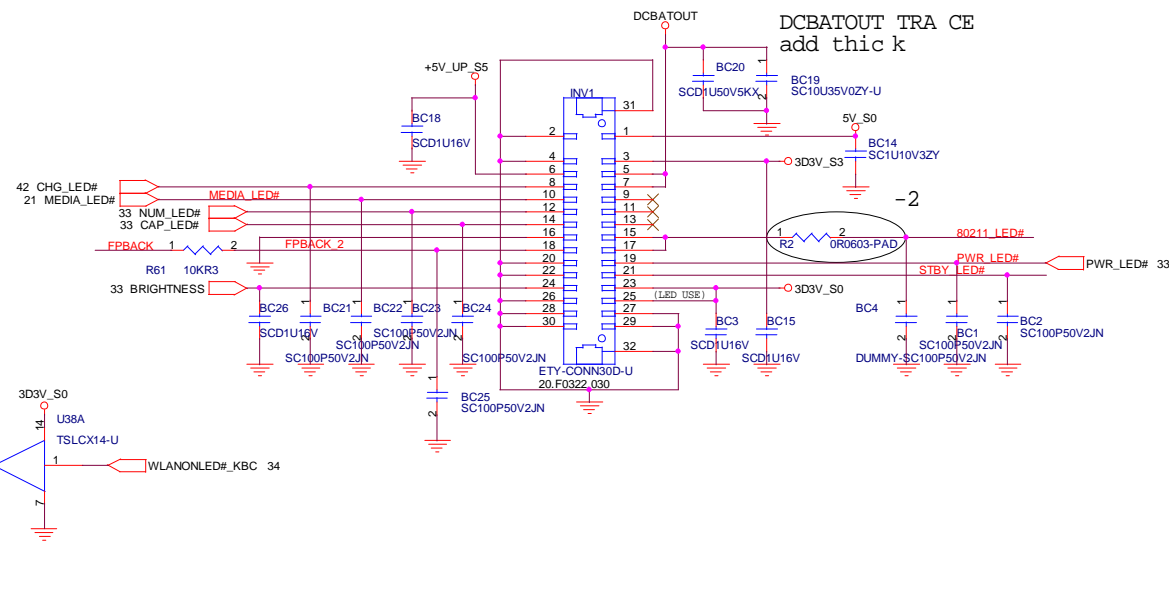
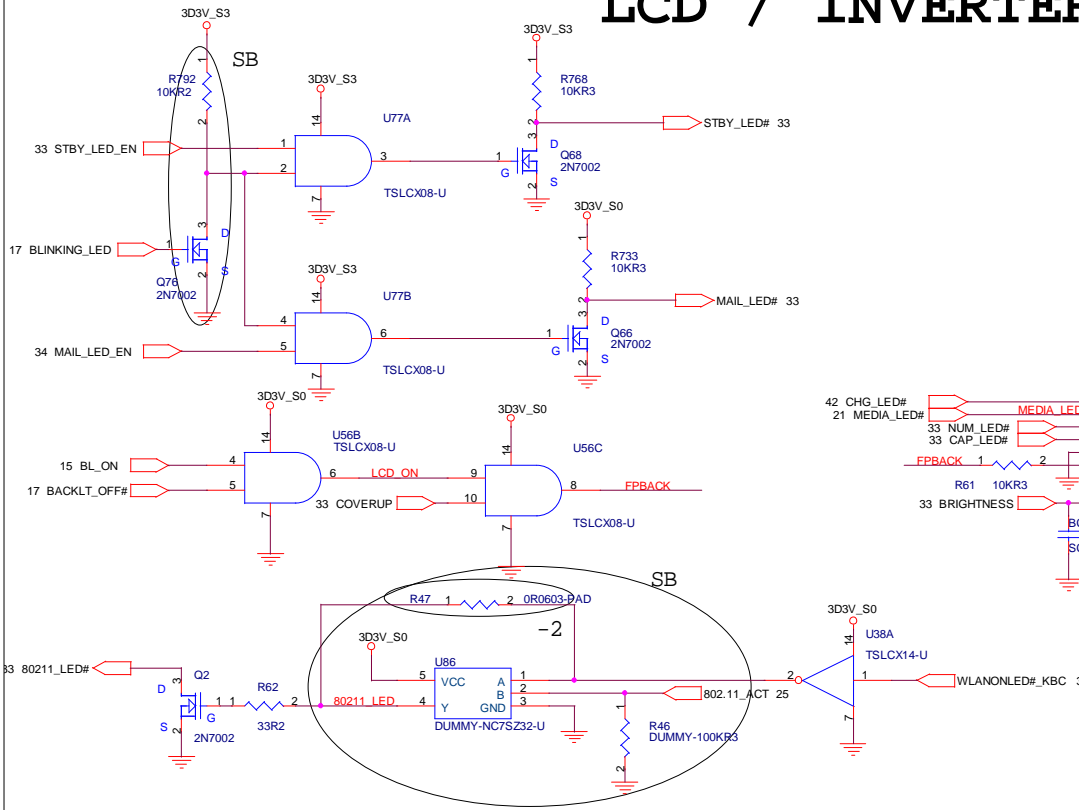


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Title CRT Connector		
Size A3	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 08, 2004 Sheet 13 of 46		

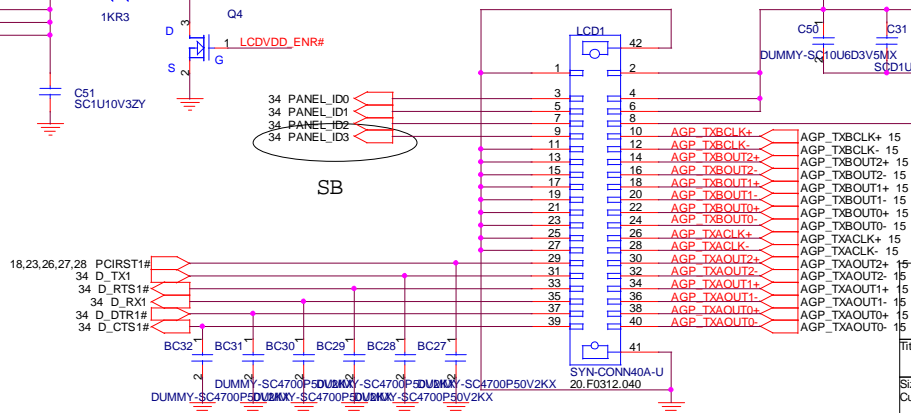
LCD / INVERTER INTERFACE

TOP VIEW
INV CONN
1 2 39



LCD CONN

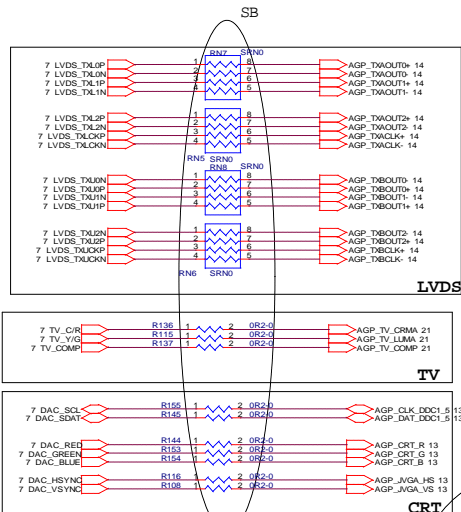
TOP VIEW
LCD CONN
1 2 39



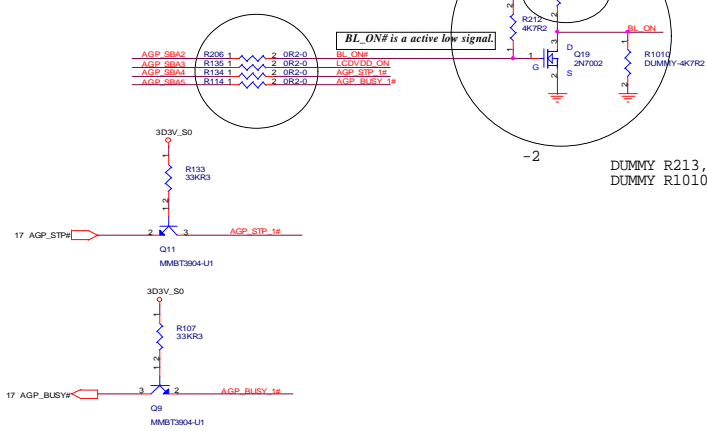
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Title LCD/Inverter Connector		
Size Custom	Document Number YUHINA2&3	Rev -2
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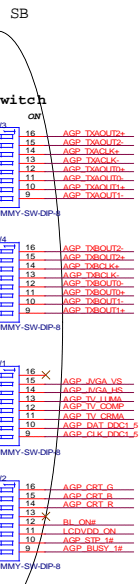
Select Int./Ext. VGA



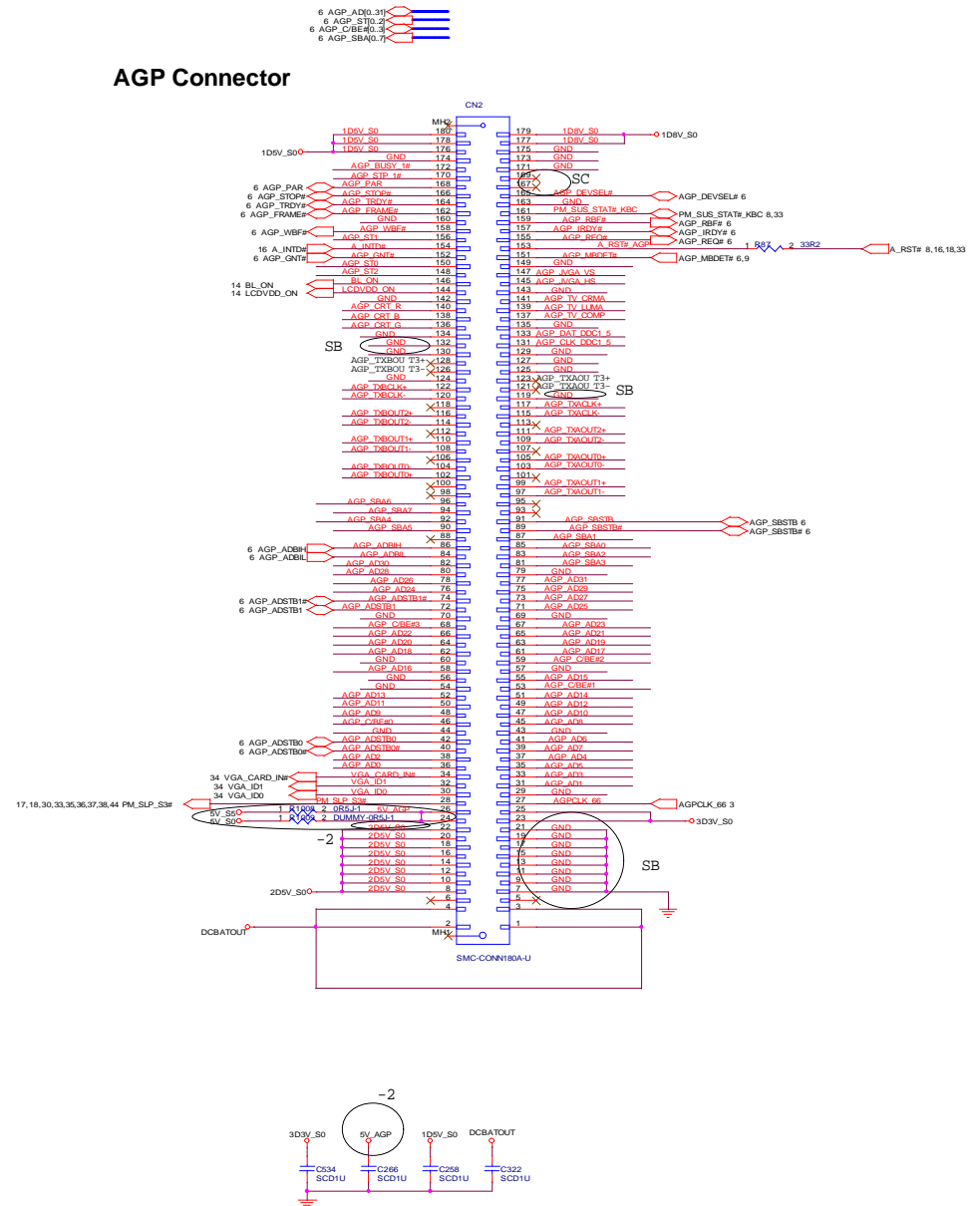
(Close to the AGP connector)

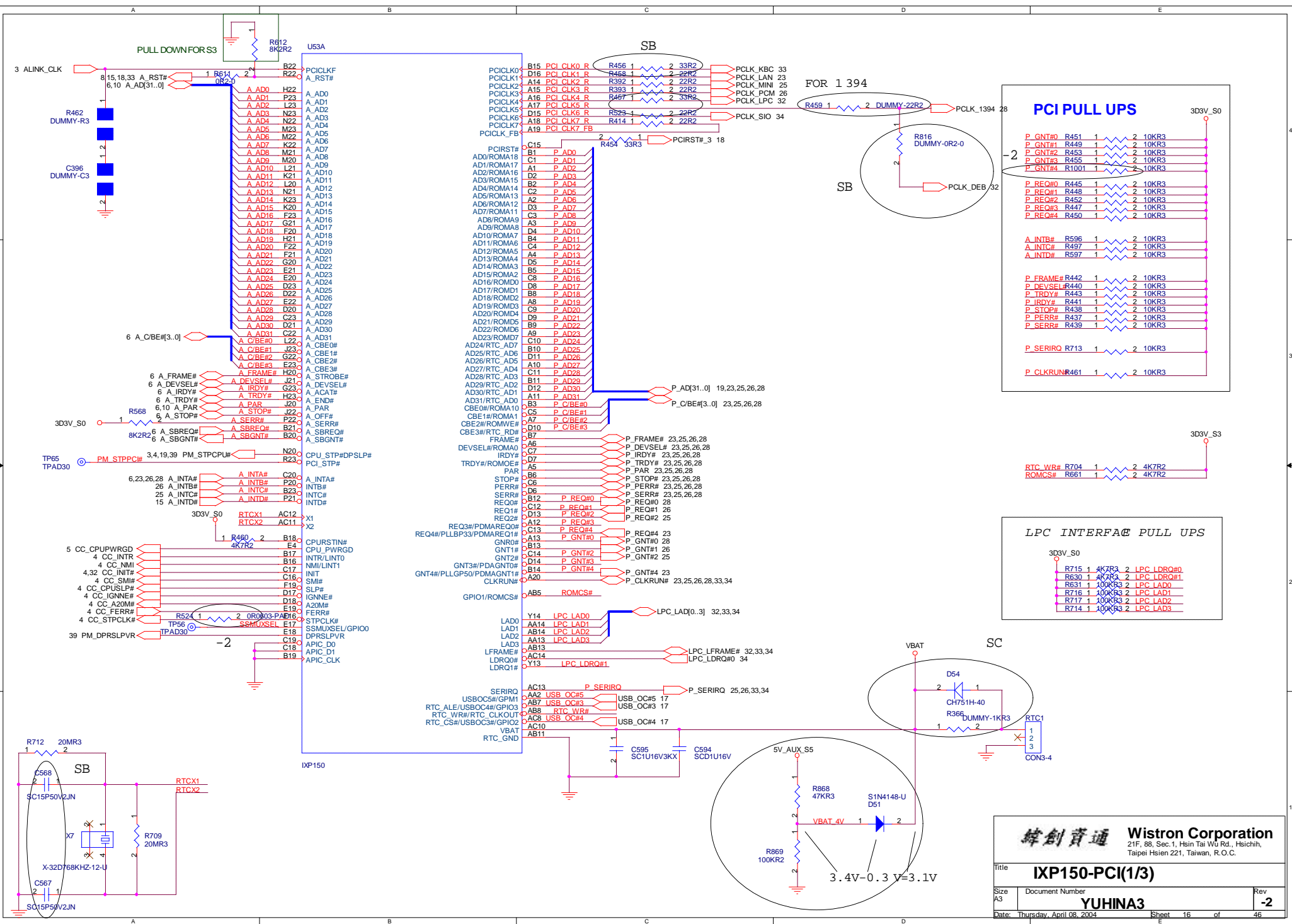


DUMMY R213,R212 for discrete
DUMMY R1010 for UMA

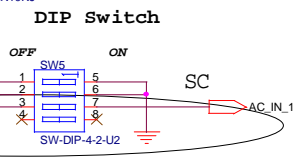
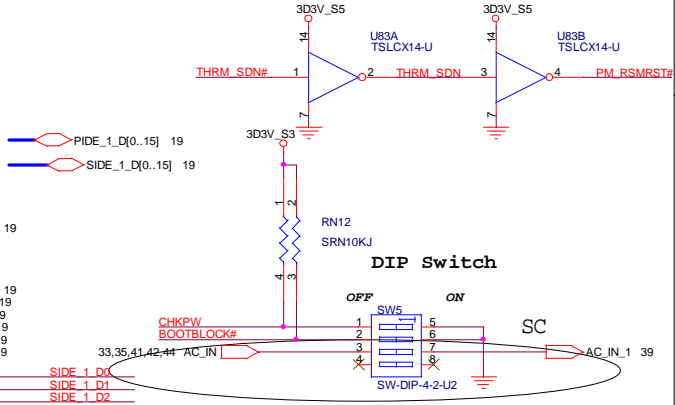
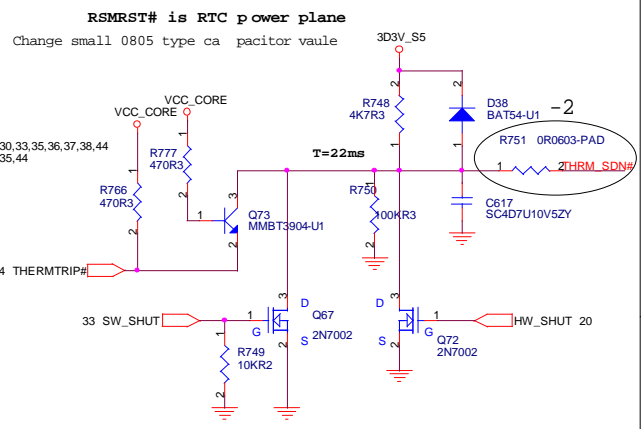
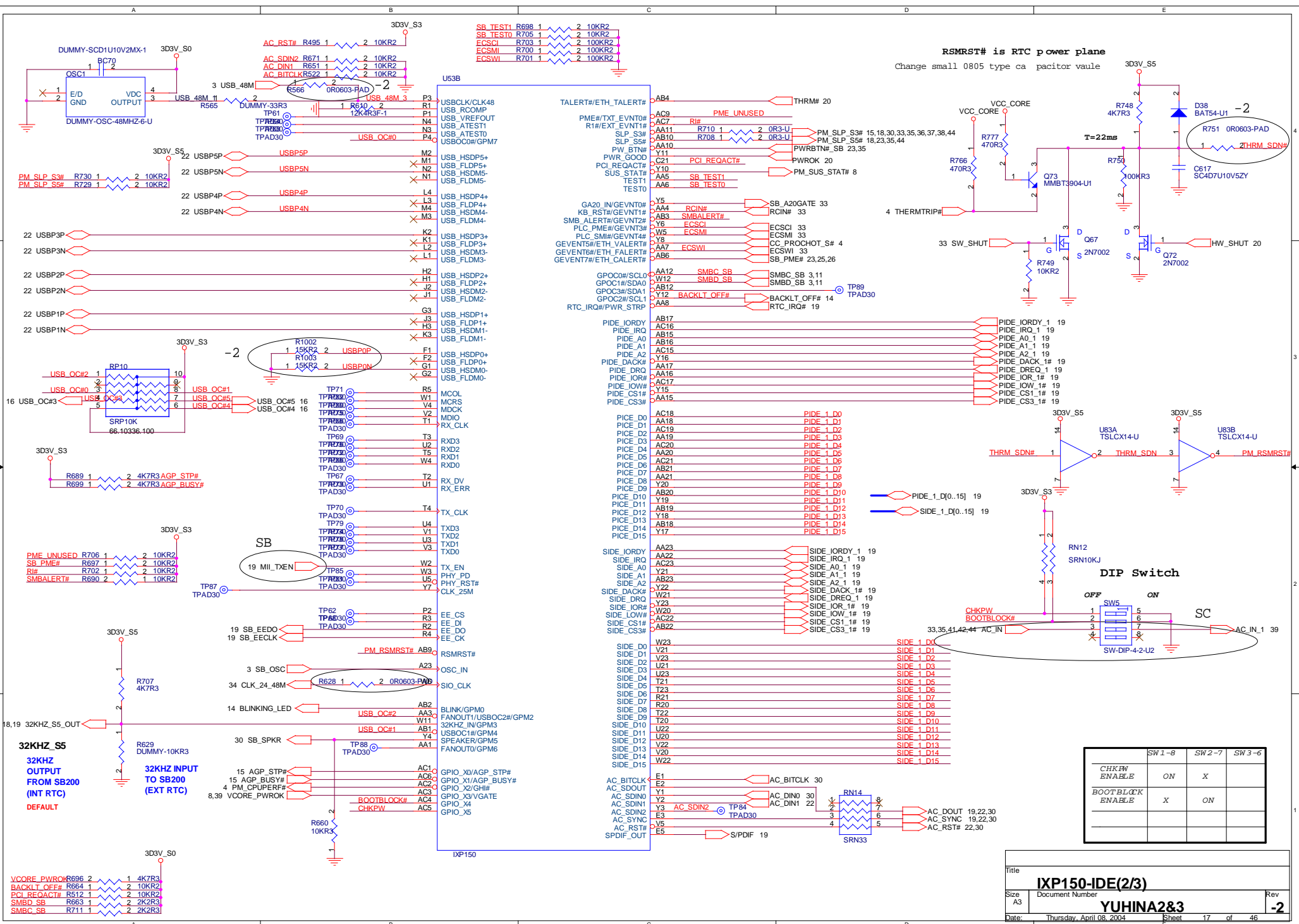


AGP Connector

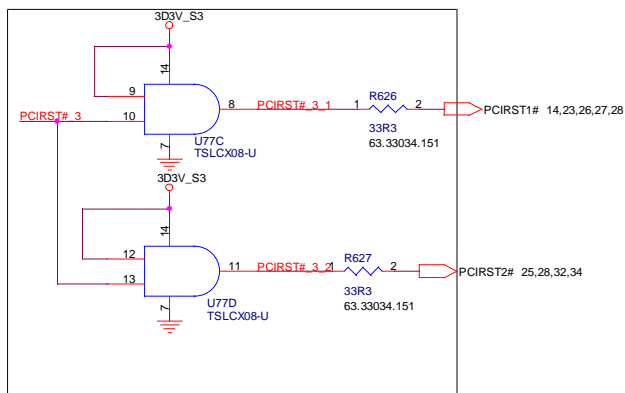
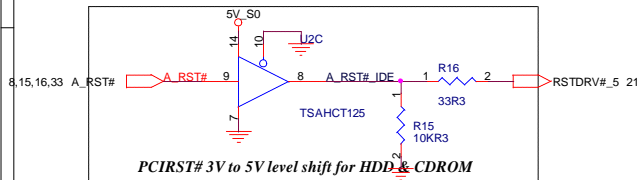
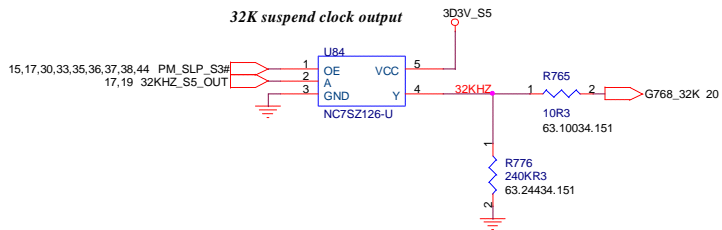




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 Taipei Hsien 221, Taiwan, R.O.C.

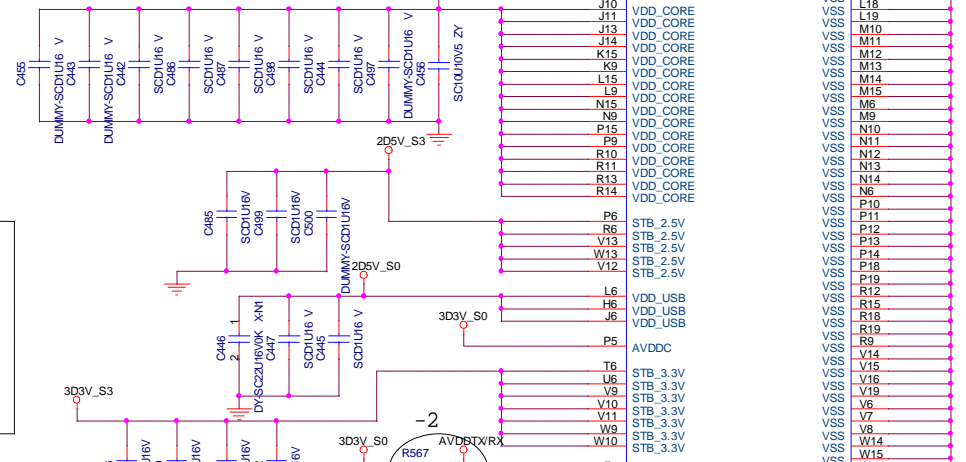
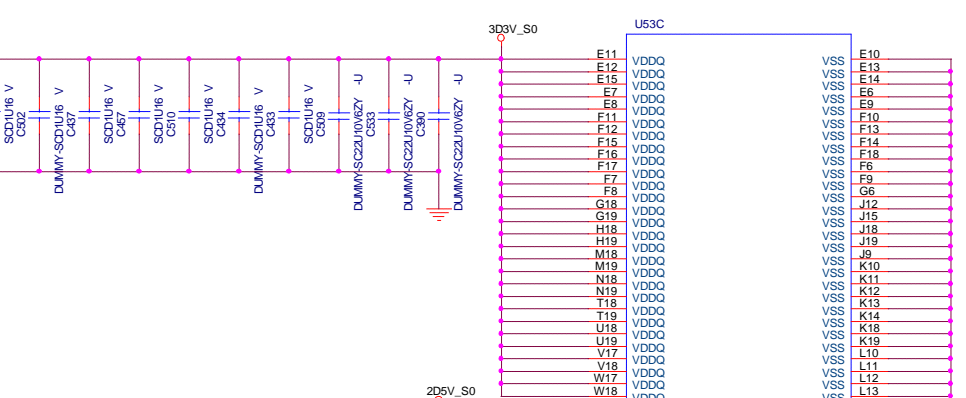
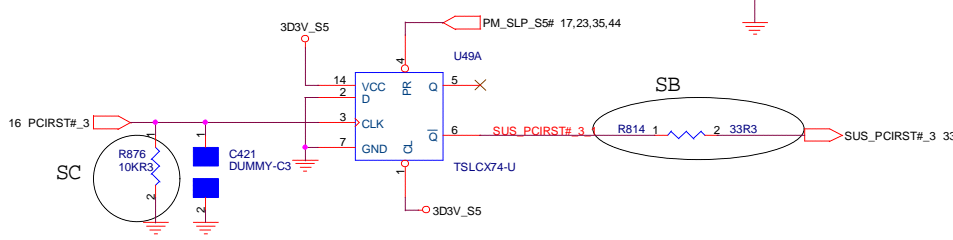
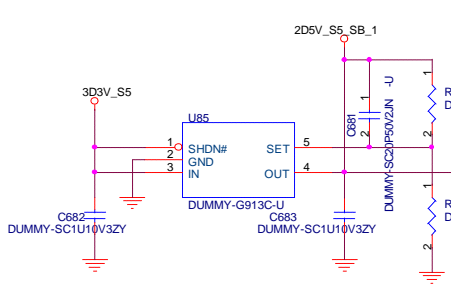


	SW 1-6	SW 2-7	SW 3-6
CHKPW ENABLE	ON	X	
BOOTBLK ENABLE	X	ON	



Power Consumption

- 3D3V_S5: 340uA
- 2D5V_S5: 6D8mA
- 3D3V_S3: 156mA
- 2D5V_S3: 48mA
- 3D3V_S0: 40mA
- 2D5_S0: 302mA
- 5V_S0: 70uA
- VCC_CORE_S0: 100mA

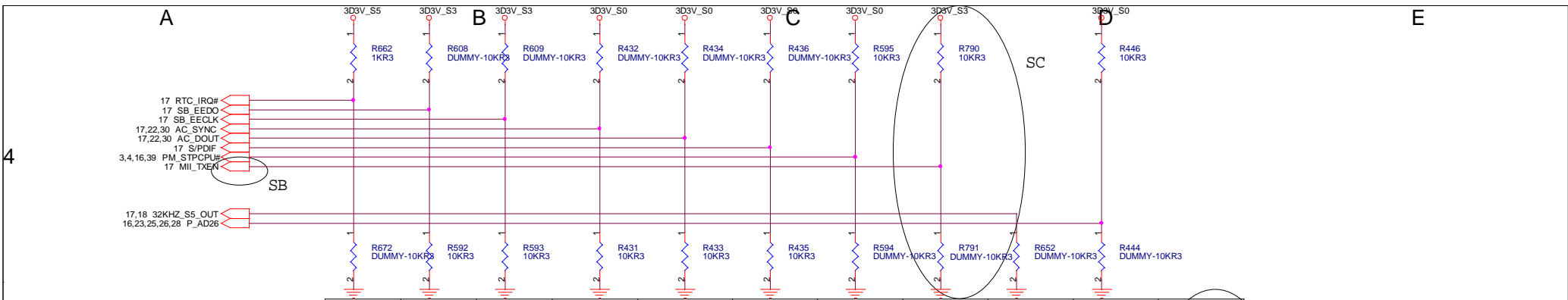


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Title: **IXP150(3/3)**

Size: Custom Document Number: **YUHINA2&3** Rev: **-2**

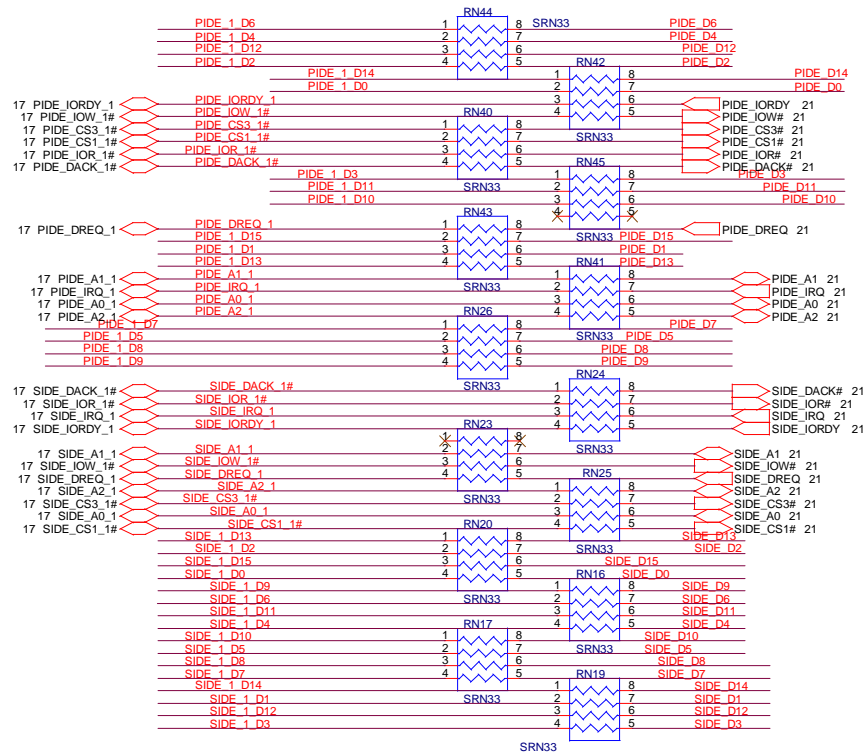
Date: Thursday, April 08, 2004 Sheet 18 of 46

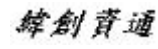


REQUIRED SYSTEM STRAPS

OVERLAP COMMON PADS
FOR DUAL-OP
RESISTORS

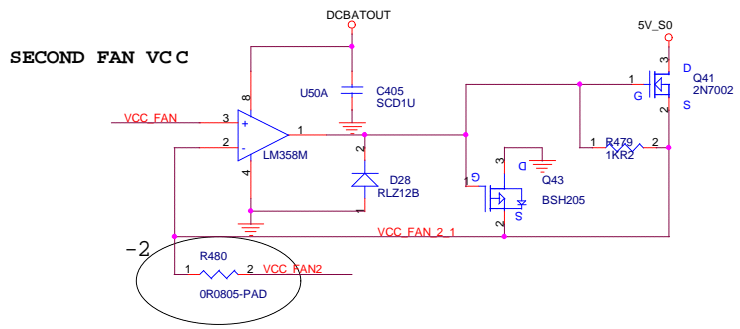
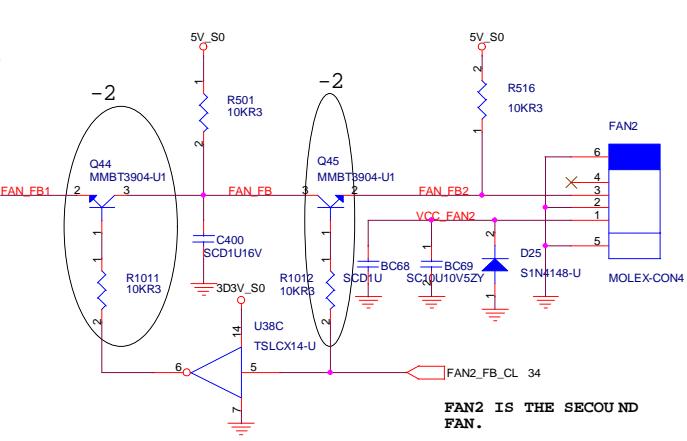
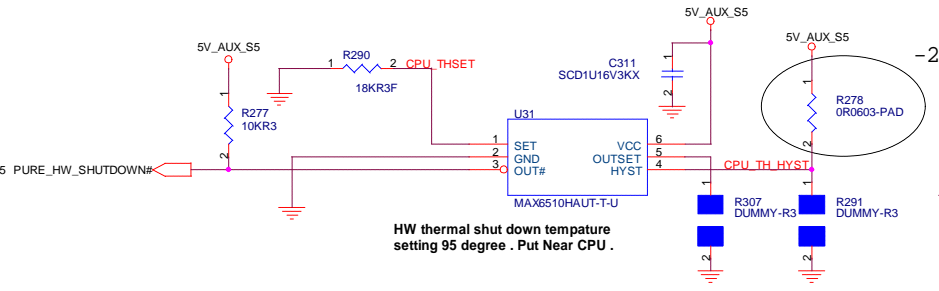
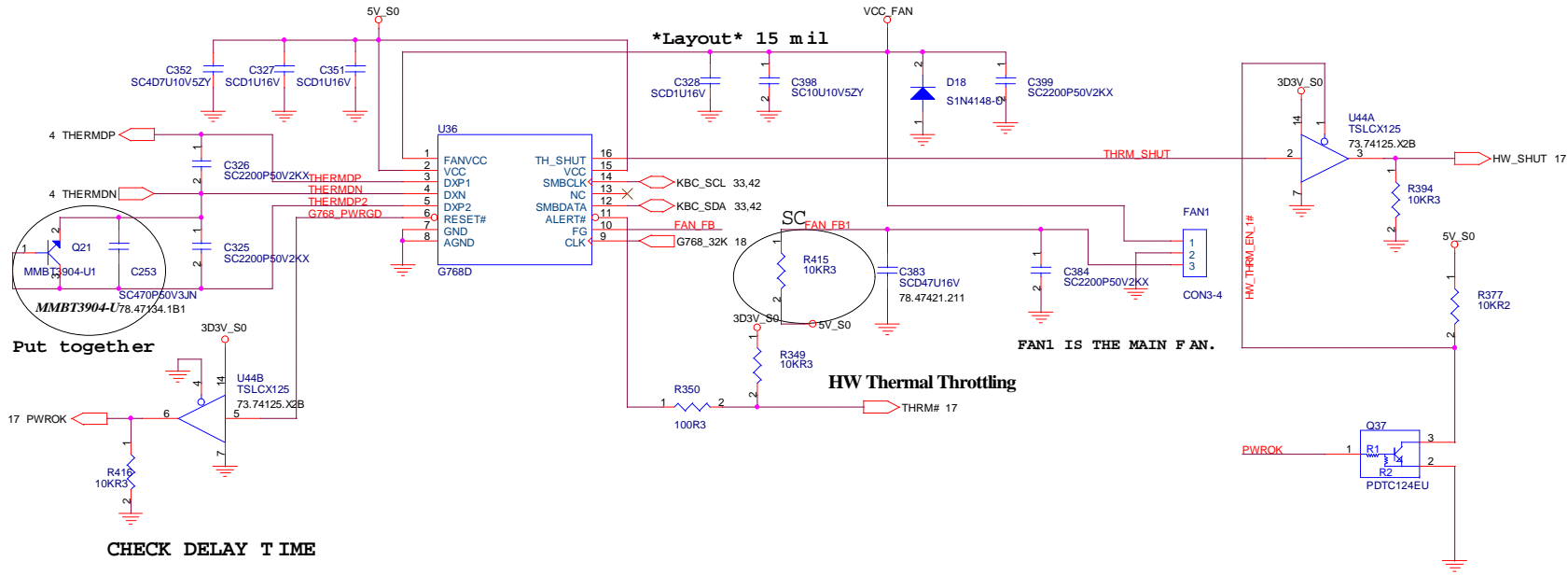
	ACPWRON	EEDO	EECK	AC_SYNC	AC_SDOOUT	SPDIF_OUT	CPU_STP#	32KHZ_S5	PCI_AD26	TX_EN
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	ROM ON PCI BUS DEFAULT	INIT ACTIVE HIGH(AMD) DEFAULT	33MHz NB BUS DEFAULT	SIO 24MHz DEFAULT	ENABLE SPEED STEP DEFAULT	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT	BIOS use LPC cycle DEFAULT	DISABLE CPU FREQ SETTING DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP	32KHZ INPUT TO SB200 (EXT RTC)	BIOS uSE FW Cycle	ENABLE CPU FREQSETTING




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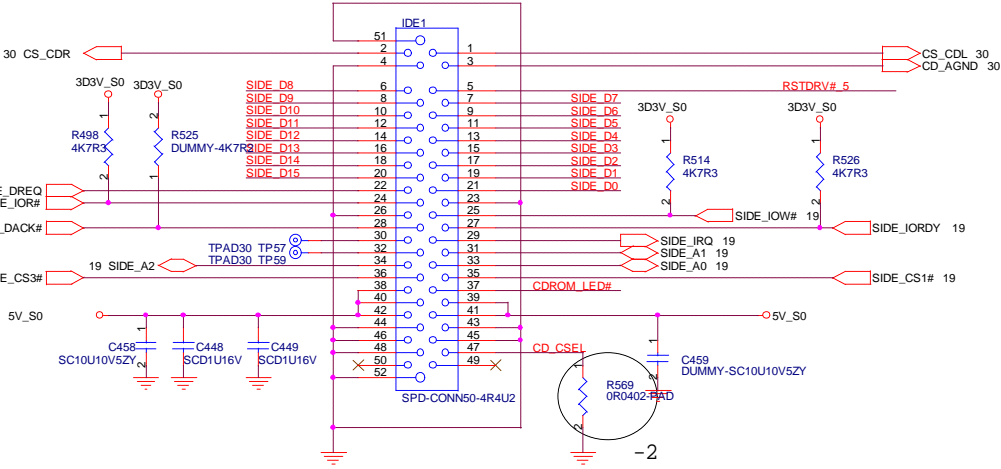
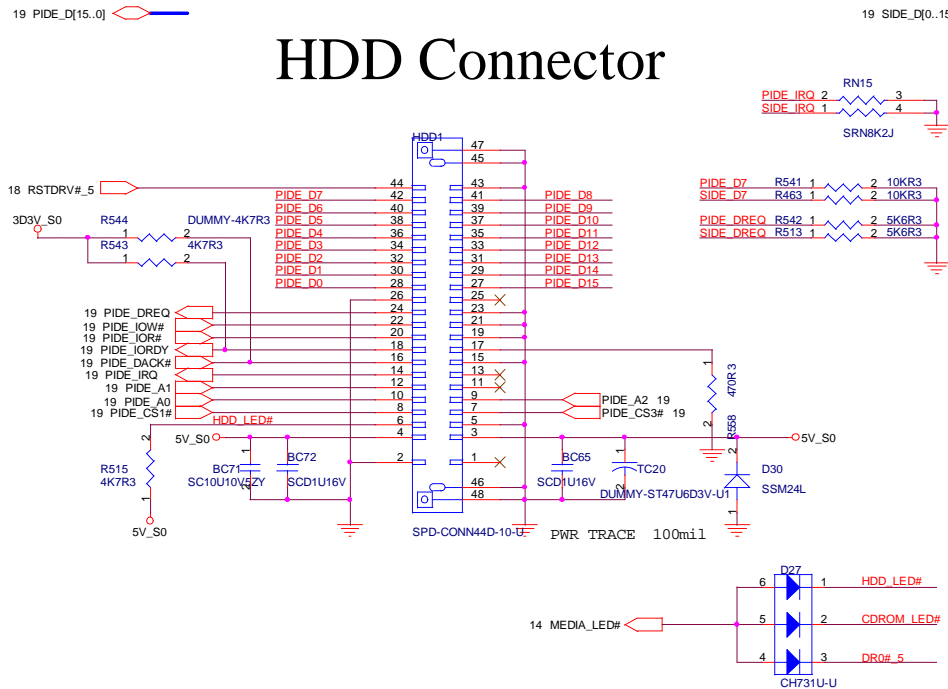
Title		SB STRAPPING	
Size	A3	Document Number	YUHINA2&3
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G768D thermal sensor & Fan controller



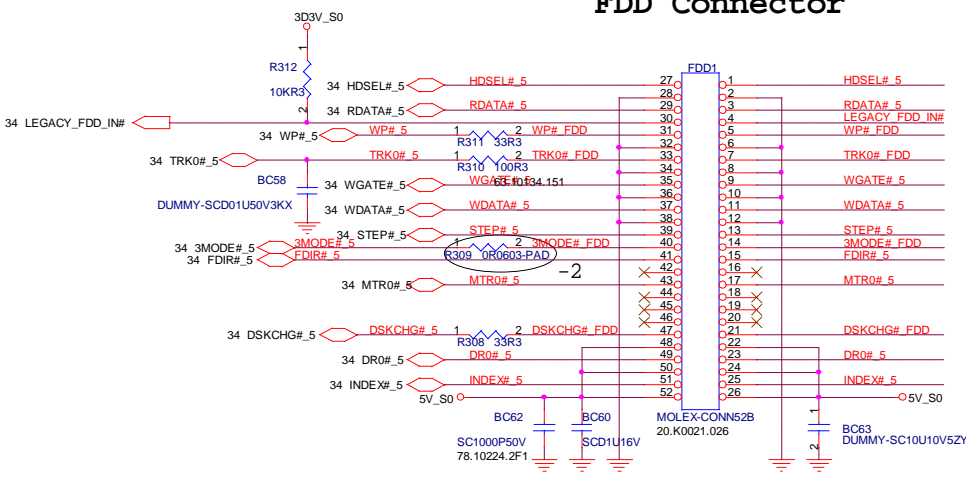
CD-ROM CONN

HDD Connector

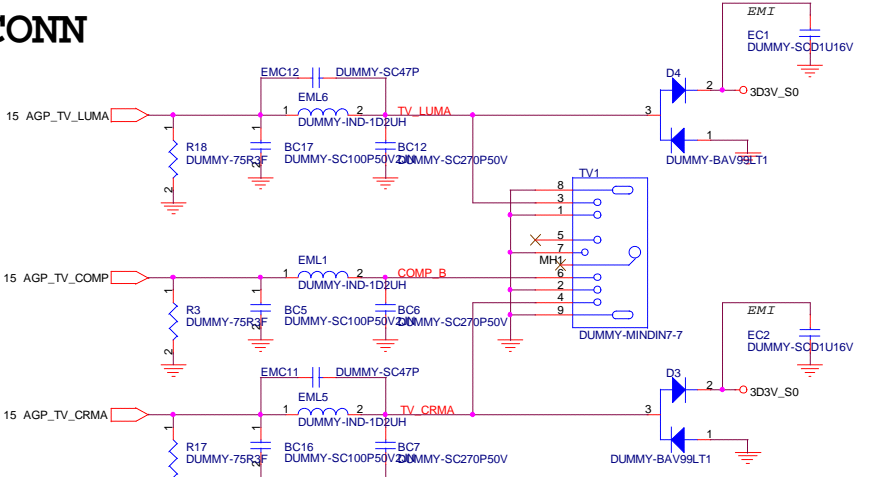


CHECK PIDE/SIDE DIAG# PIN

FDD Connector



TV CONN



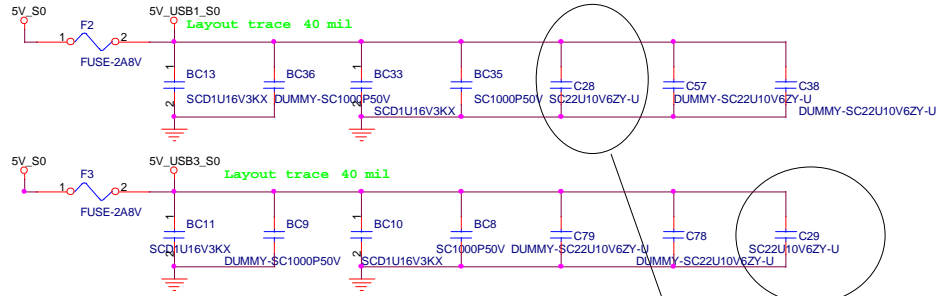
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD and CDROM and FDD CONN/TV CONN**

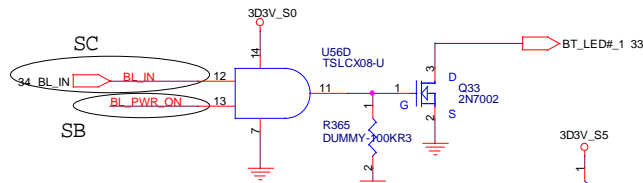
Size A3 Document Number **YUHINA2&3** Rev **-2**

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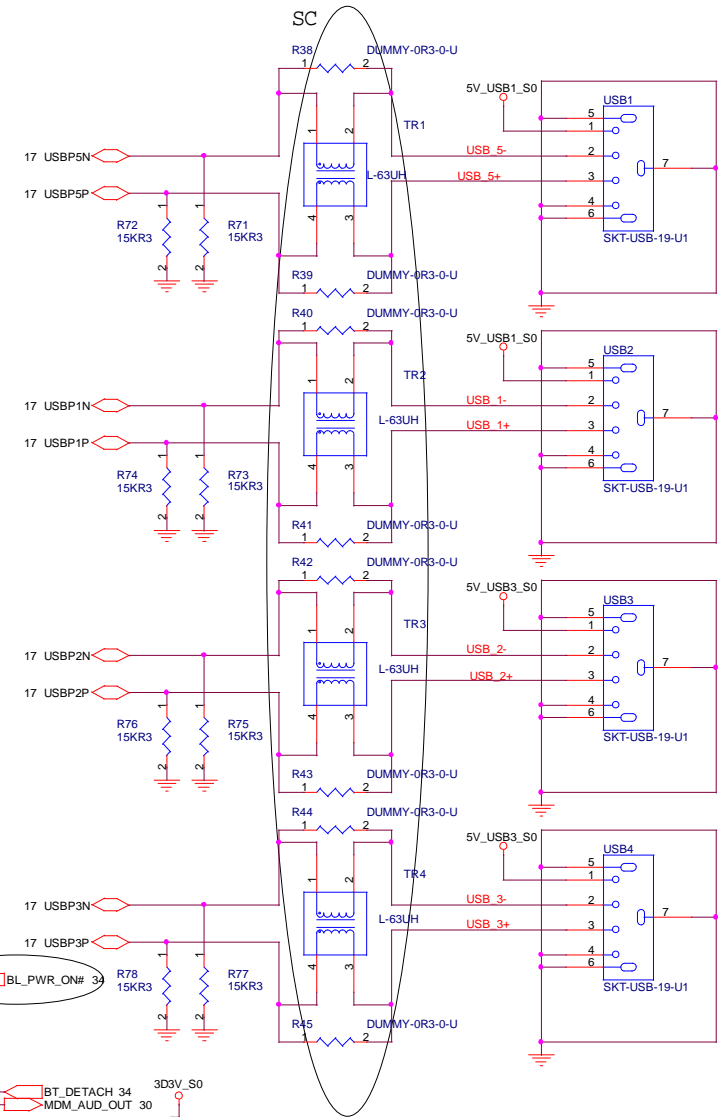
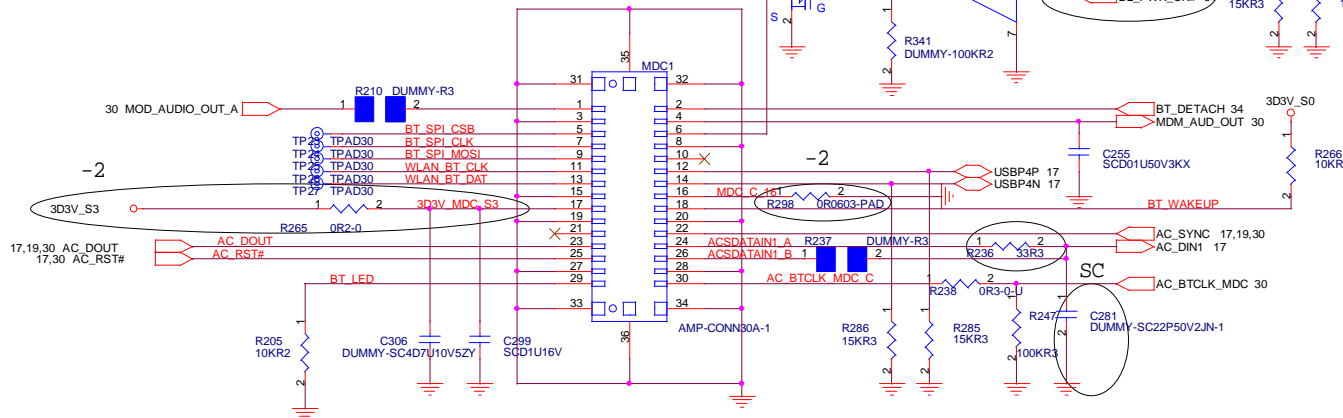
USB PORT



-2

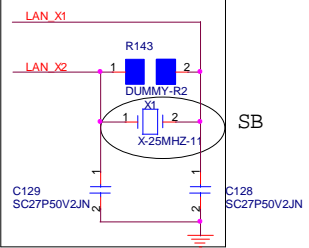


MDC/BT

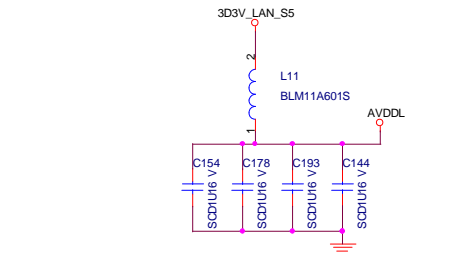
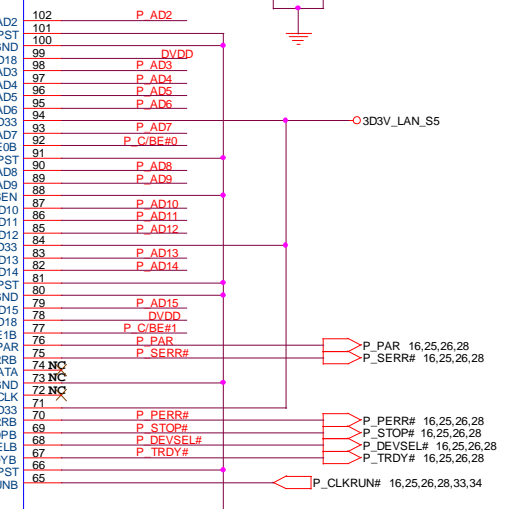
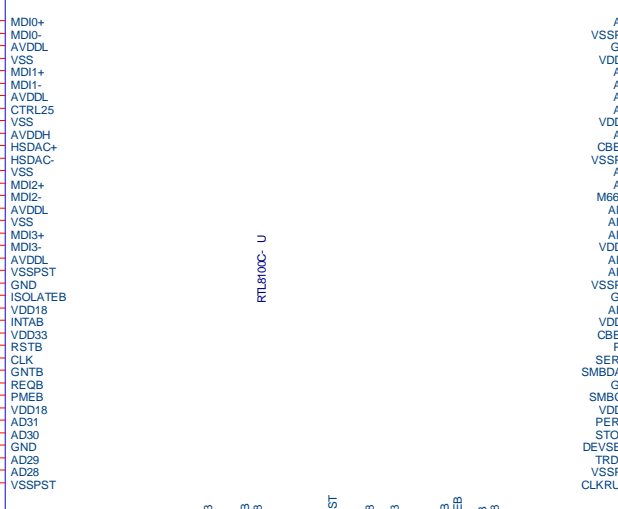
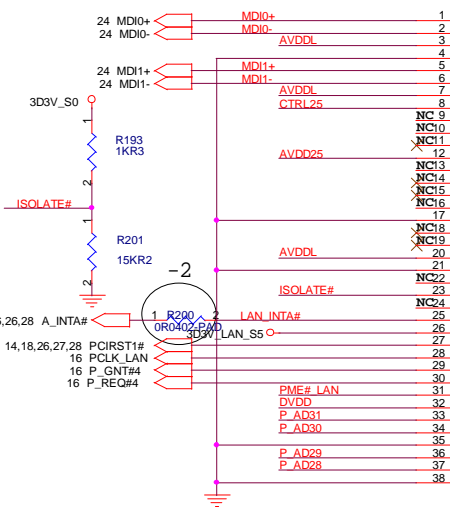
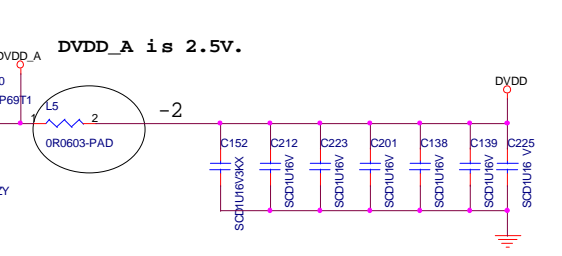
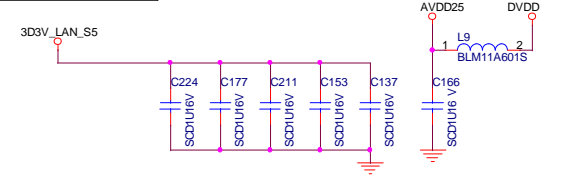
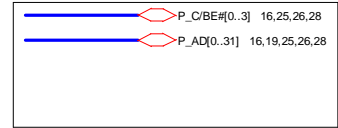
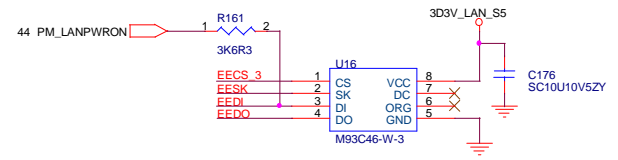


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Title			
USB and MDC/BT IF and LAN			
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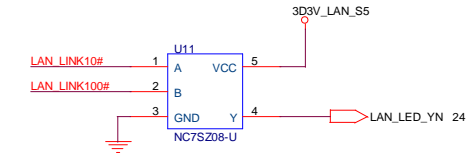
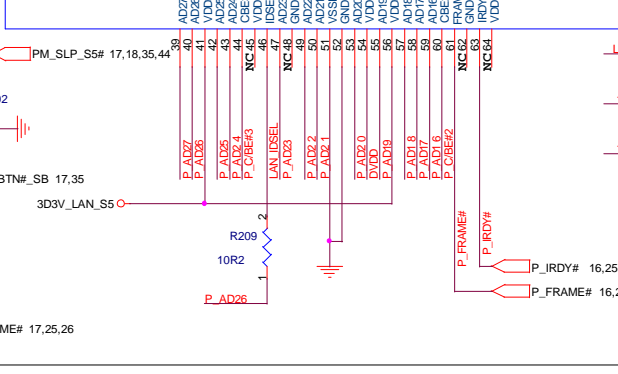
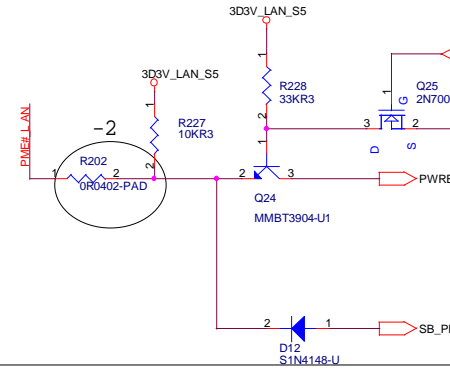
Close to RTL8100C
Pin121, Pin122



SB



At RTL8100C (10/100) application, AVDDL is 3.3V.



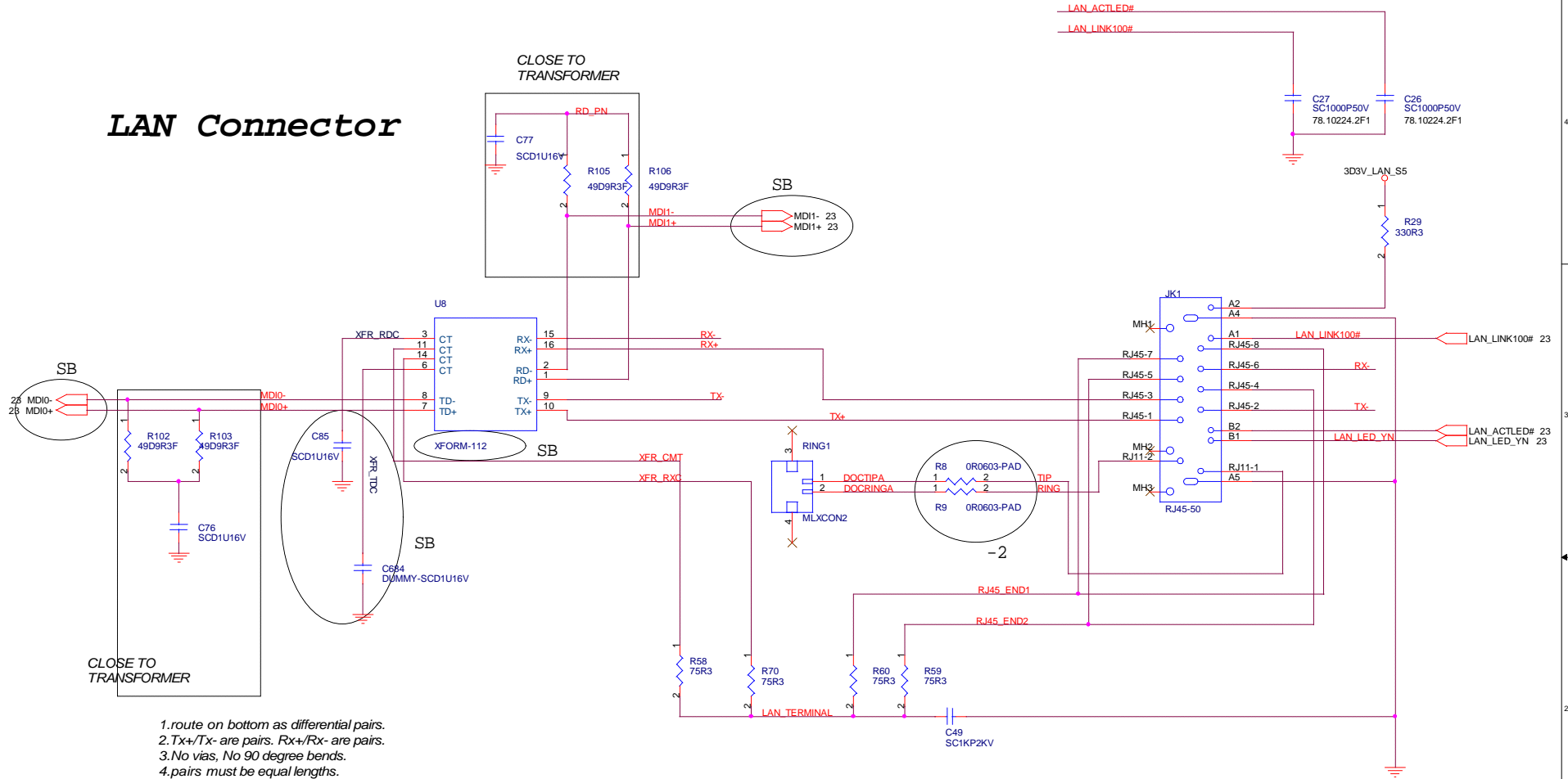
緯創資通 Wistron Corporation
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Title: **LAN RTL8100C**

Size A3 Document Number: **YUHINA2&3** Rev: **-2**

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LAN Connector

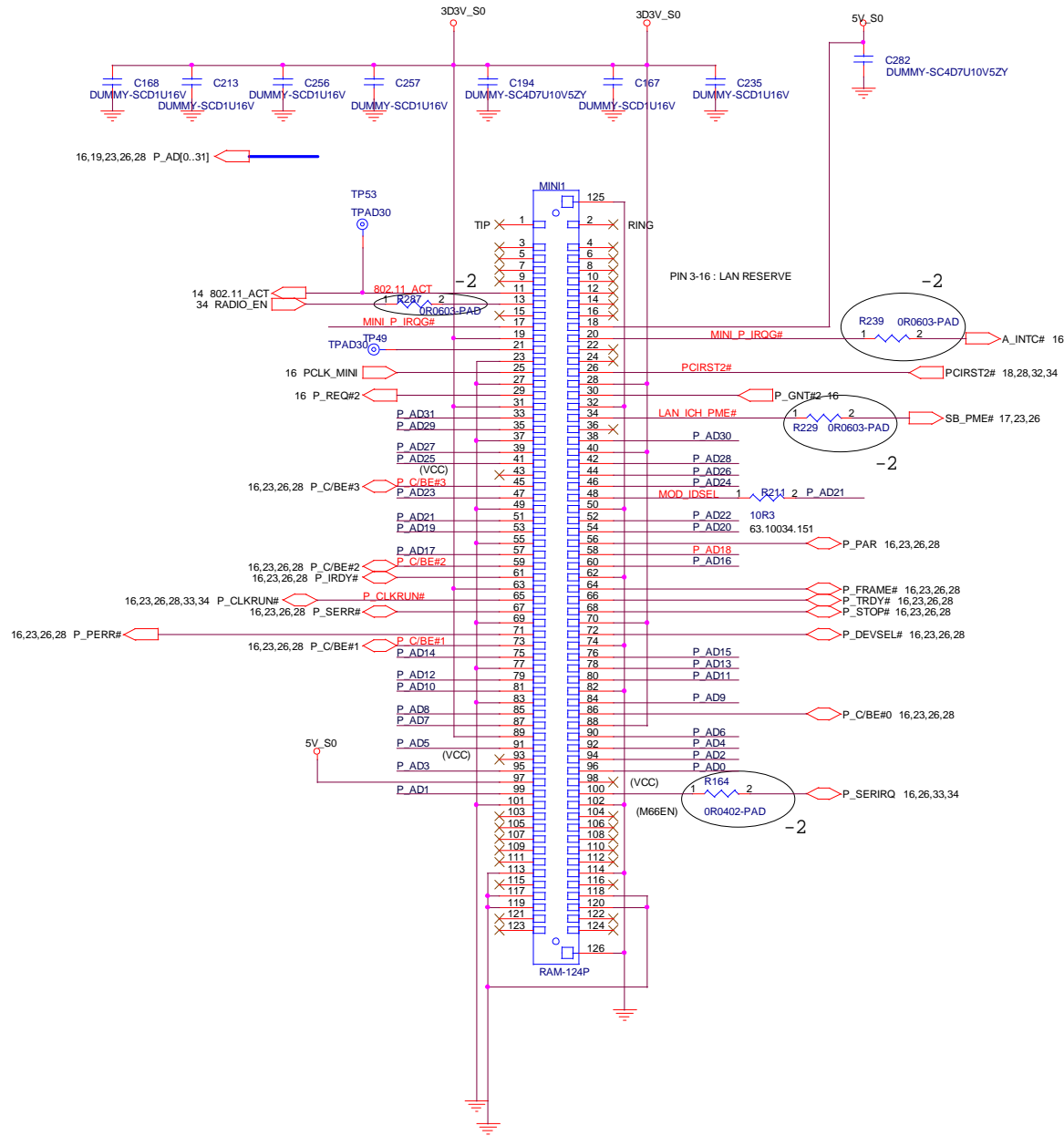


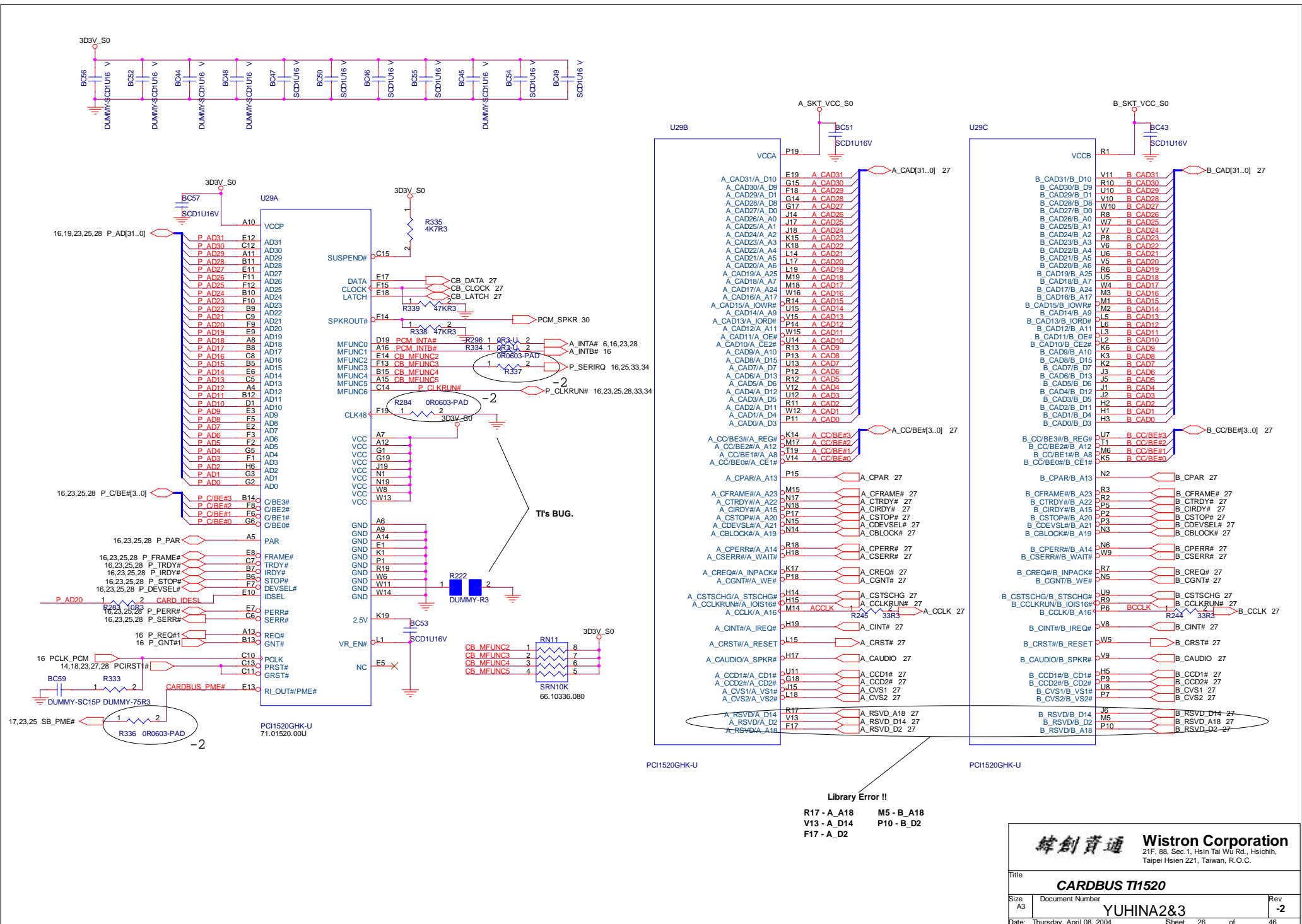
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

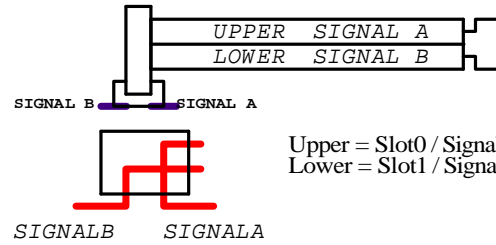
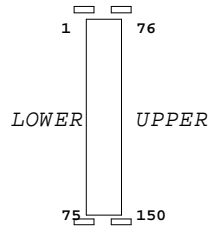
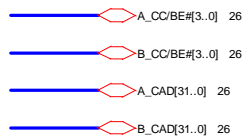
DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

Green LED---Speed100:ON/Speed10:OFF
Yellow LED---Link:ON ,TX/RX:Flash

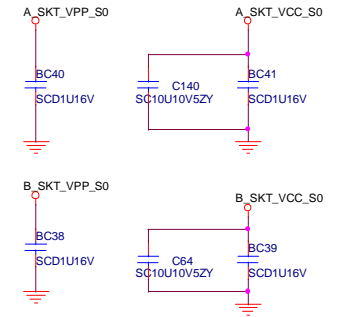
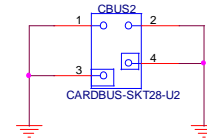
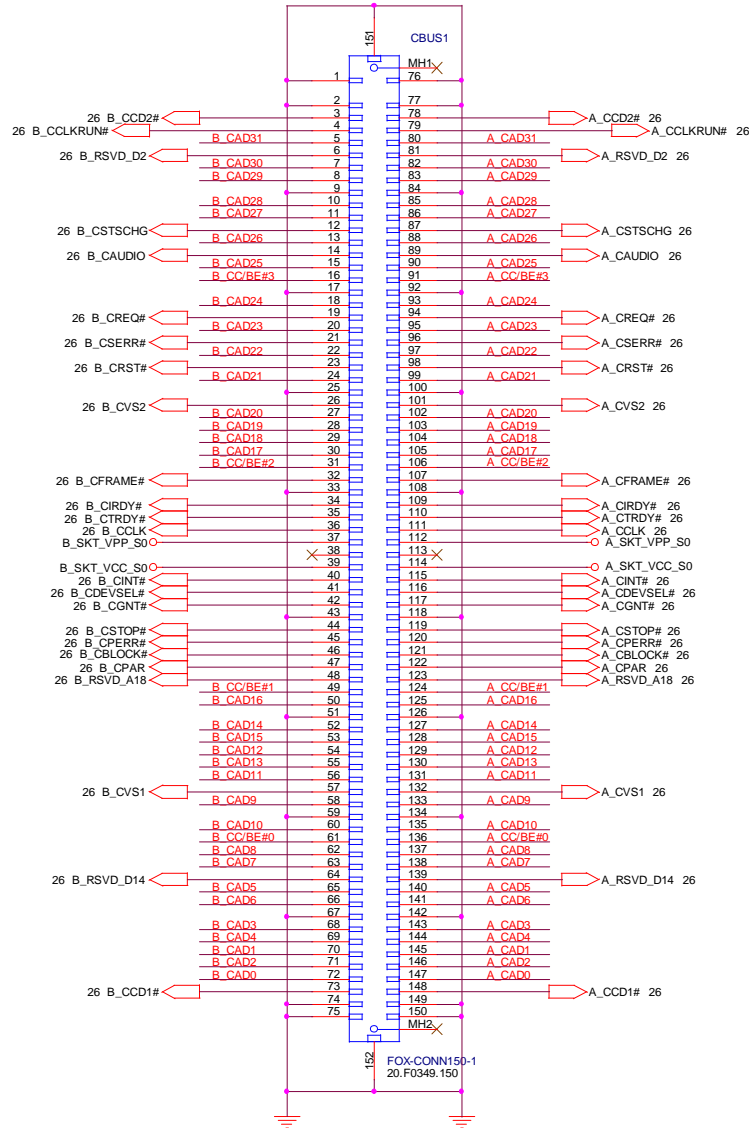
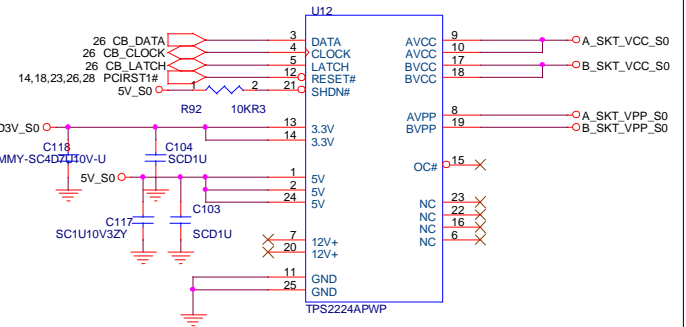
Mini PCI



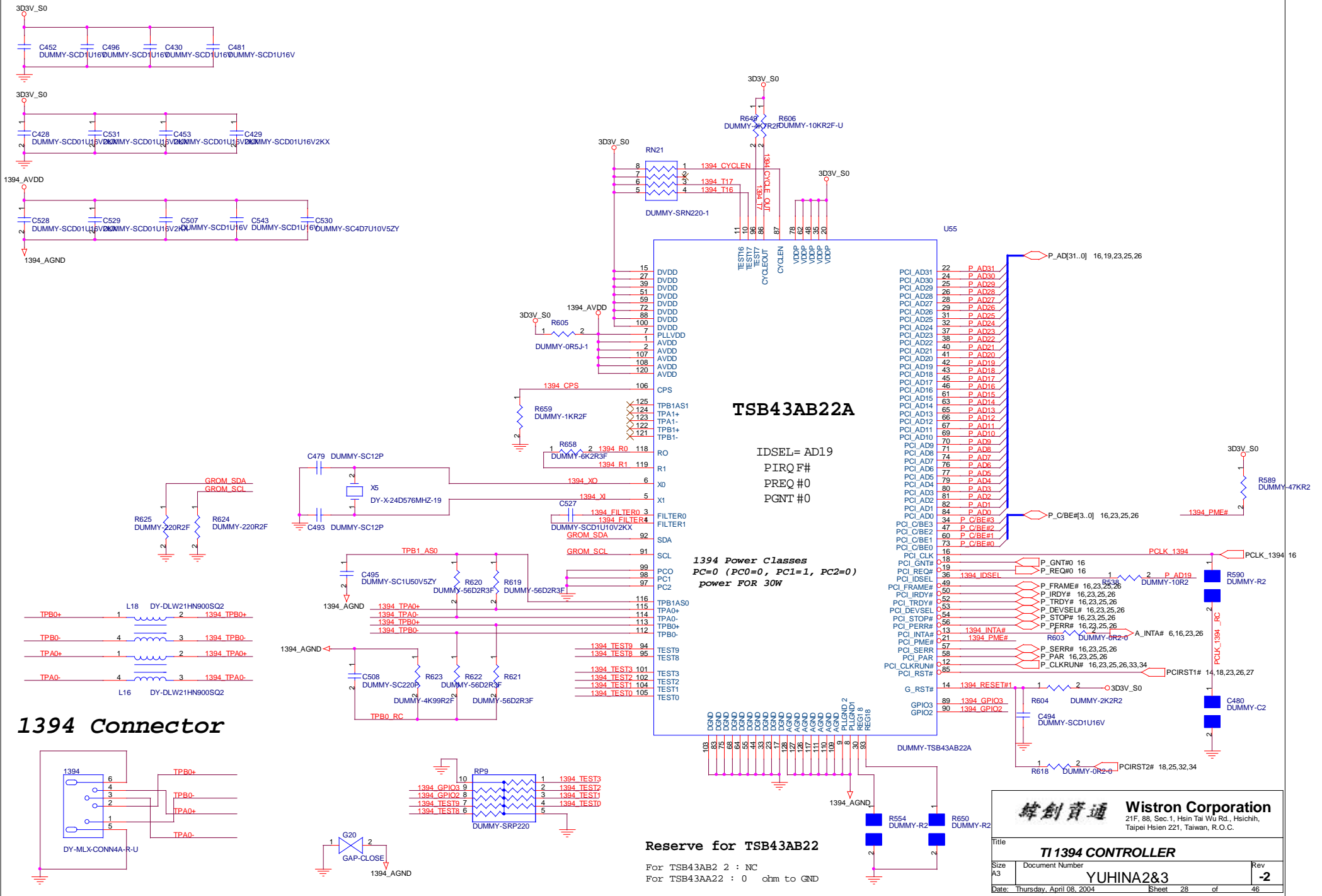




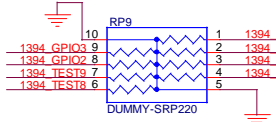
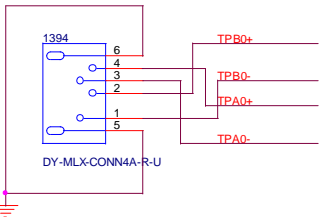
Upper = Slot0 / Signal A = Conn B
 Lower = Slot1 / Signal B = Conn A



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Title		
CARBUS CONN / PWR SW		
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1394 Connector



TSB43AB22A

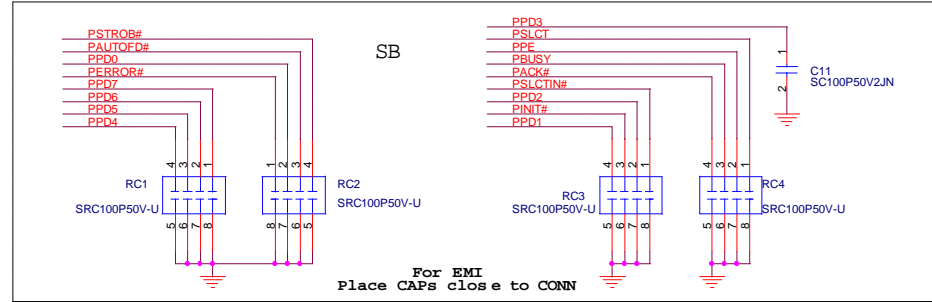
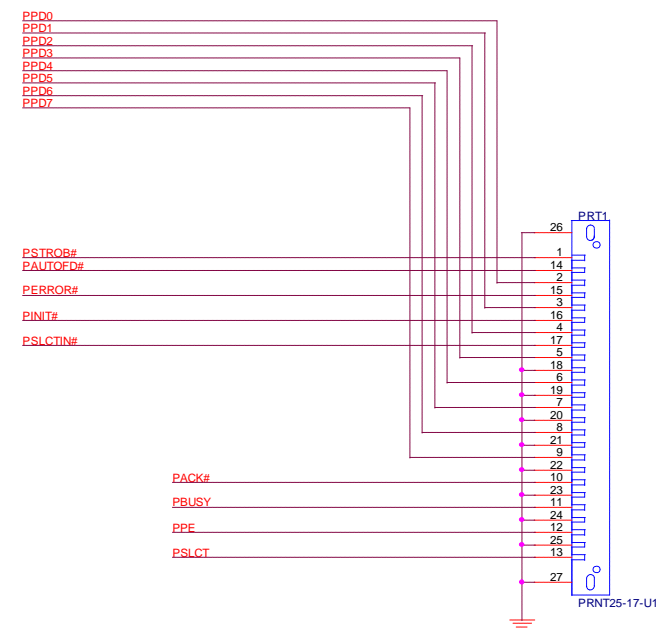
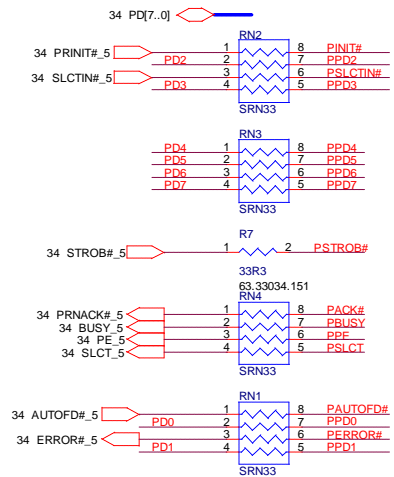
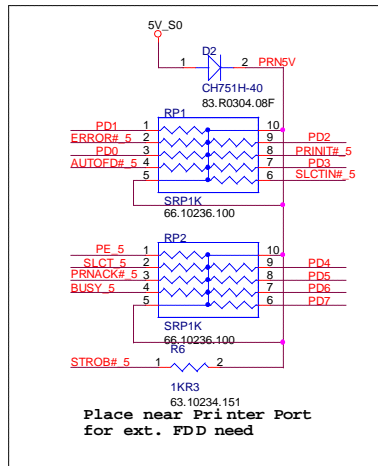
IDSEL= AD19
 PIRQ#0
 PREQ#0
 PGNT#0

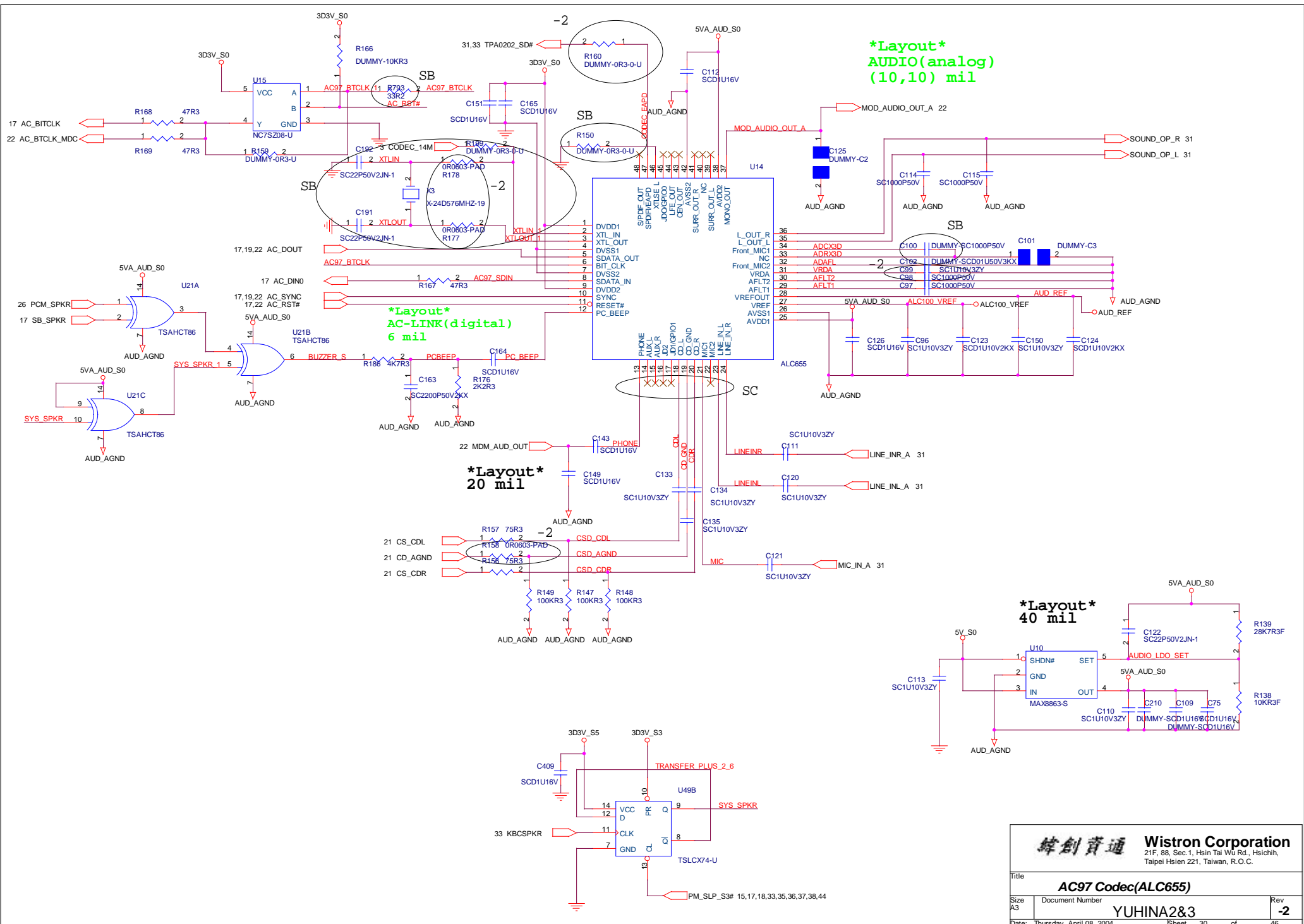
1394 Power Classes
 PC=0 (PC0=0, PC1=1, PC2=0)
 power FOR 30W

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Title TI 1394 CONTROLLER			
Size A3	Document Number YUHINA2&3	Rev -2	
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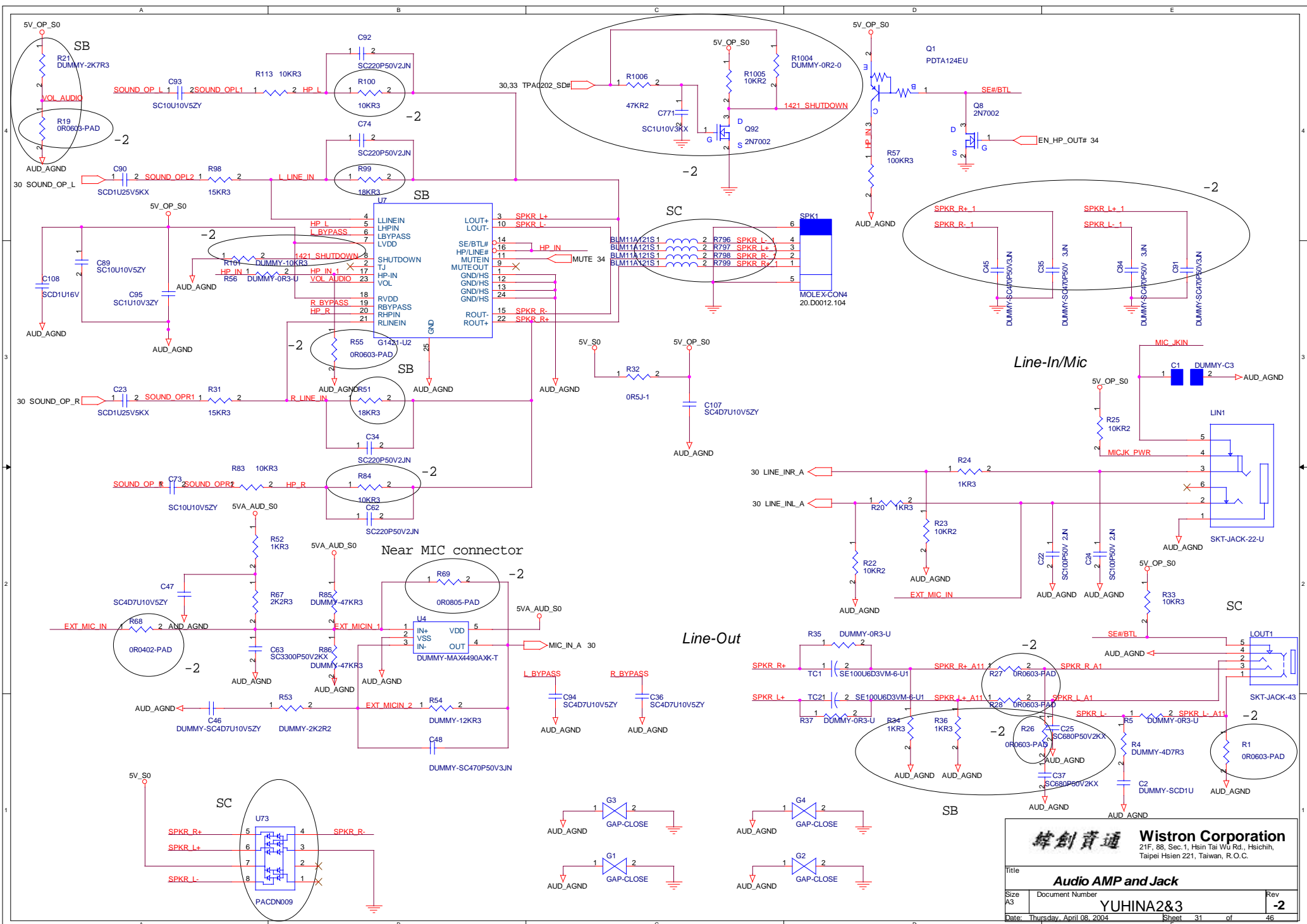
Reserve for TSB43AB22
 For TSB43AB2 2 : NC
 For TSB43AA22 : 0 ohm to GND

PRINTER PORT



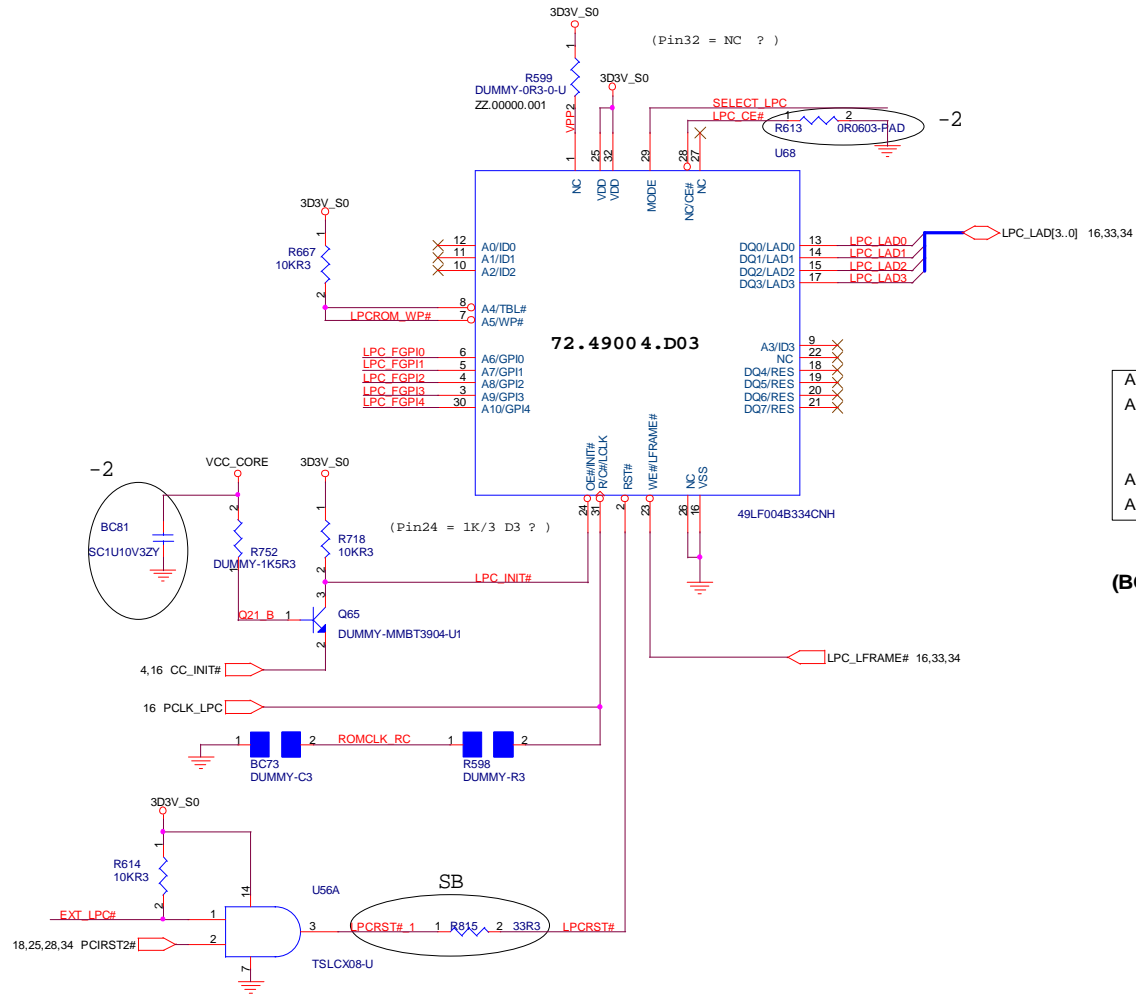
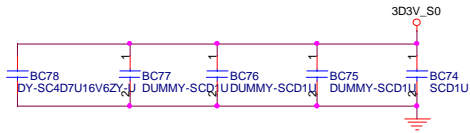
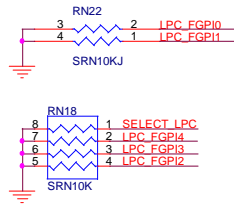


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Title			
AC97 Codec(ALC655)			
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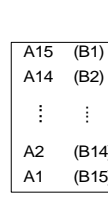


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Title Audio AMP and Jack		
Size A3	Document Number YUHINA2&3	Rev -2
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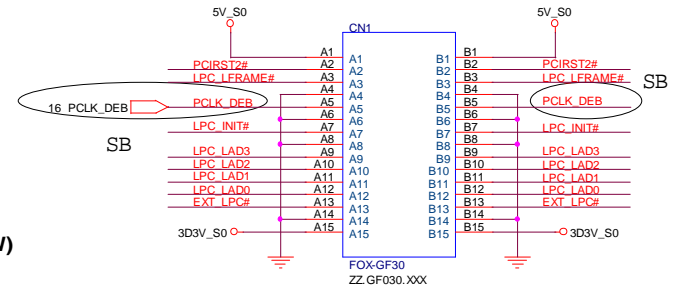


TOP VIEW



(BOTTOM VIEW)

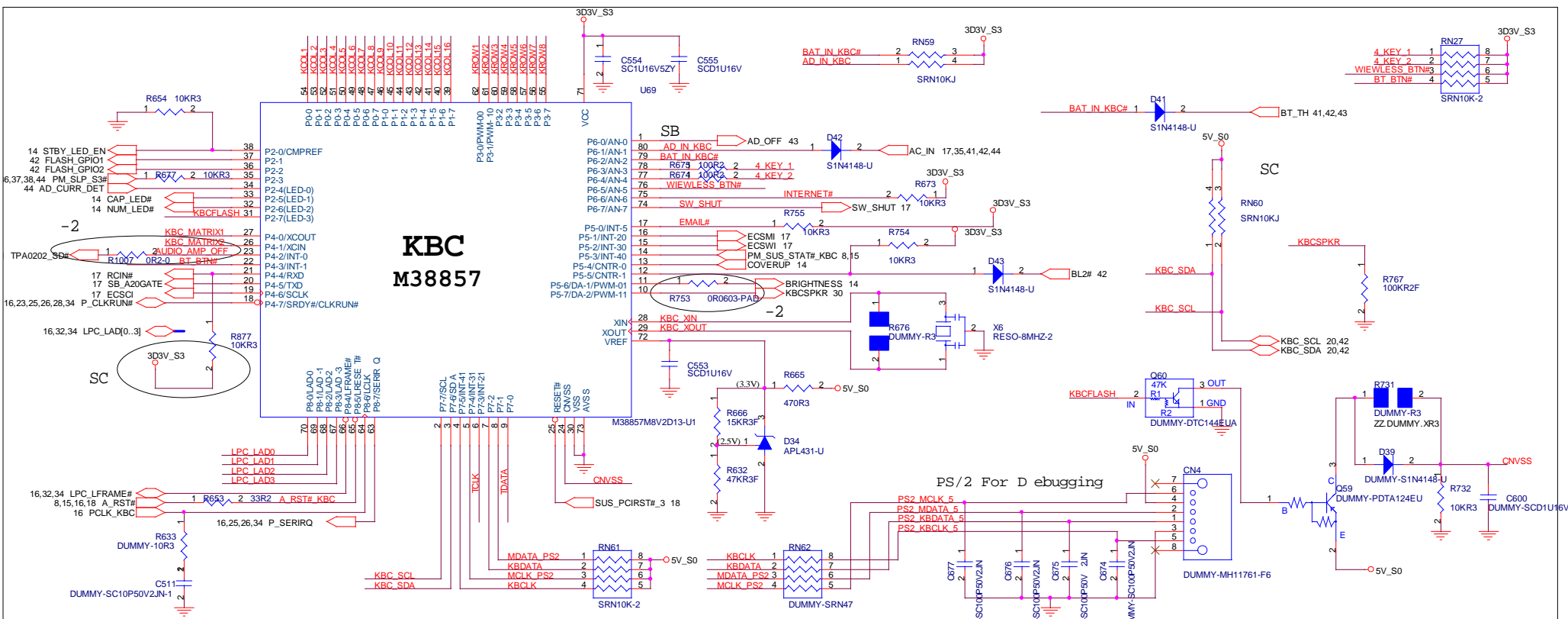
GOLDEN FINGER FOR DEBUG BOARD



PLCC 32pin ST: 72.50040.003
 PLCC 32pin SST: 72.49004.B03

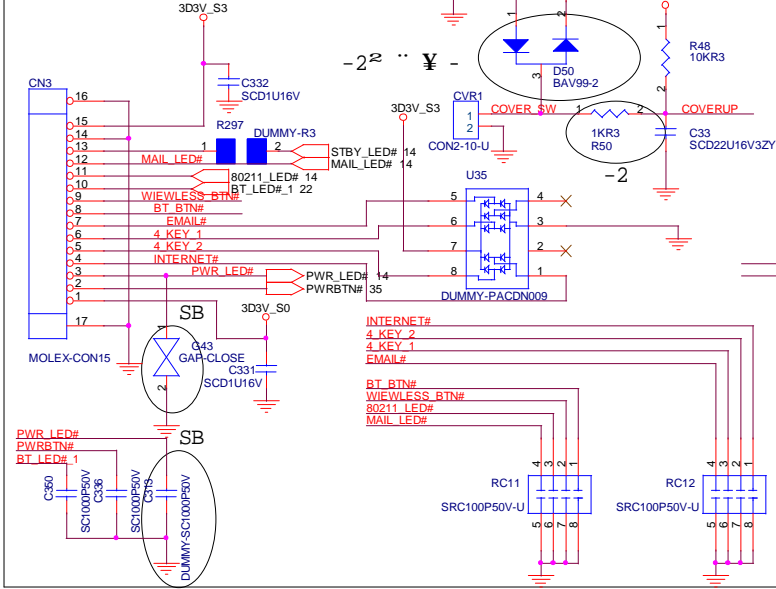
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title LPC and Debug		
Size A3	Document Number YUHINA2&3	Rev -2
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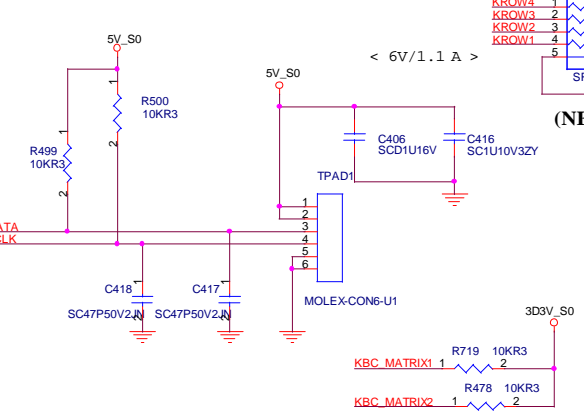


KBC M38857

Launch Board Connector



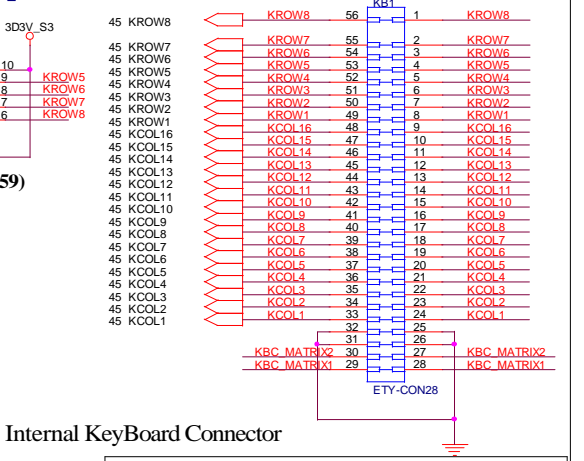
TouchPad Connector



Keyboard matrix

	US	Europe	Jap	Others
MATRIX1	HIGH	LOW	HIGH	LOW
MATRIX2	HIGH	HIGH	LOW	LOW

Internal Keyboard Connector

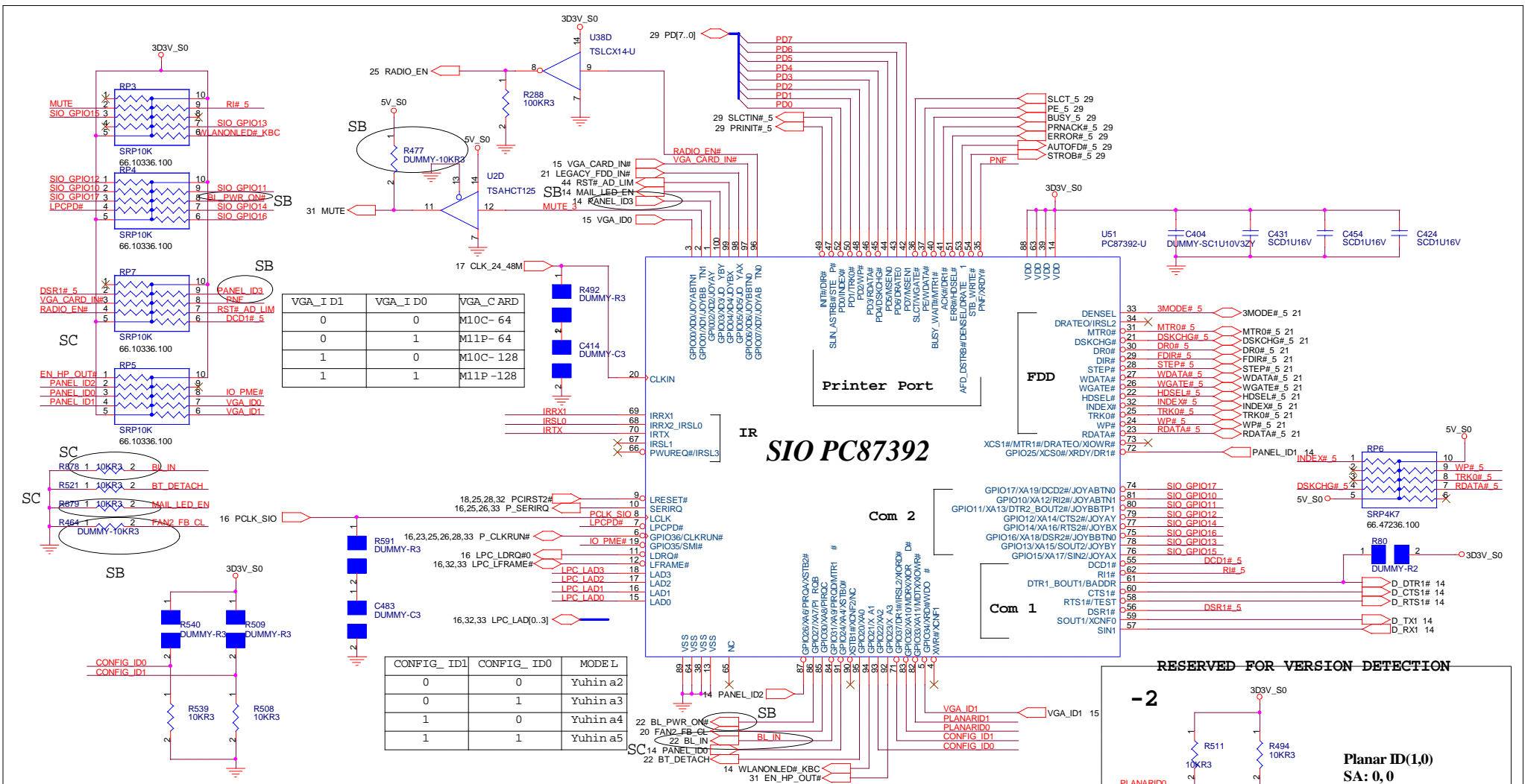


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Title: **KBC(38857)**

Size: A3 Document Number: **YUHINA2&3** Rev: **-2**

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VGA_I D1	VGA_I D0	VGA_C ARD
0	0	M10C-64
0	1	M11P-64
1	0	M10C-128
1	1	M11P-128

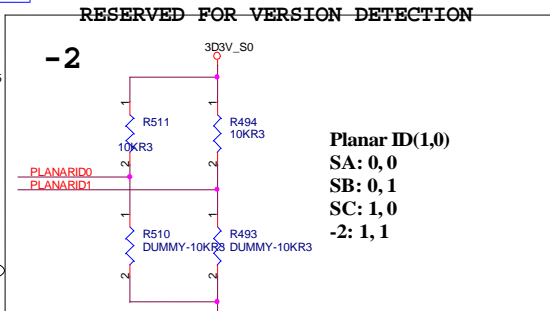
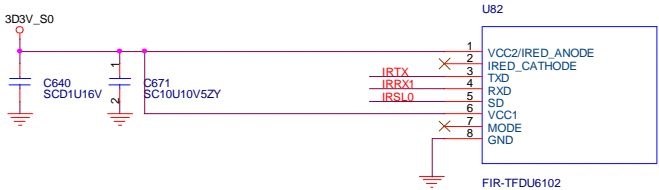
CONFIG_ID1	CONFIG_ID0	MODE L
0	0	Yuhin a2
0	1	Yuhin a3
1	0	Yuhin a4
1	1	Yuhin a5

PANEL ID D EFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDO RS
0	0	0	0	15" SX GA+
0	0	0	1	Hydis (14") SPWG
0	0	1	0	15" WI DE
0	0	1	1	Hitachi (15")
0	1	0	1	AU (15 ")
0	1	1	0	CMO(15 ")
0	1	1	1	CMO(14 ")
0	1	0	1	AU (14 ")
0	1	1	0	AU (14 ")**
0	1	1	1	No Panel

Note : AU (≠ 1),CMO(⊕ -),** : With Digitizer

Infineon FIR Module

Layout Guide:
(1) FIR_5V : 30 mils

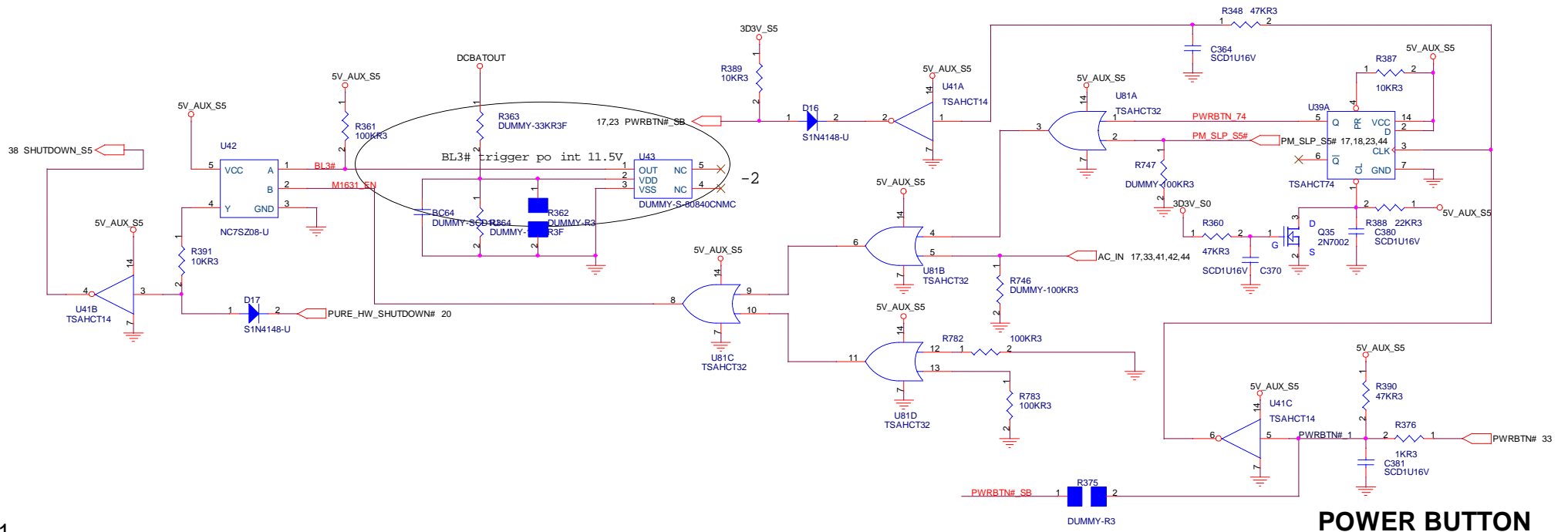


緯創資通 Wistron Corporation
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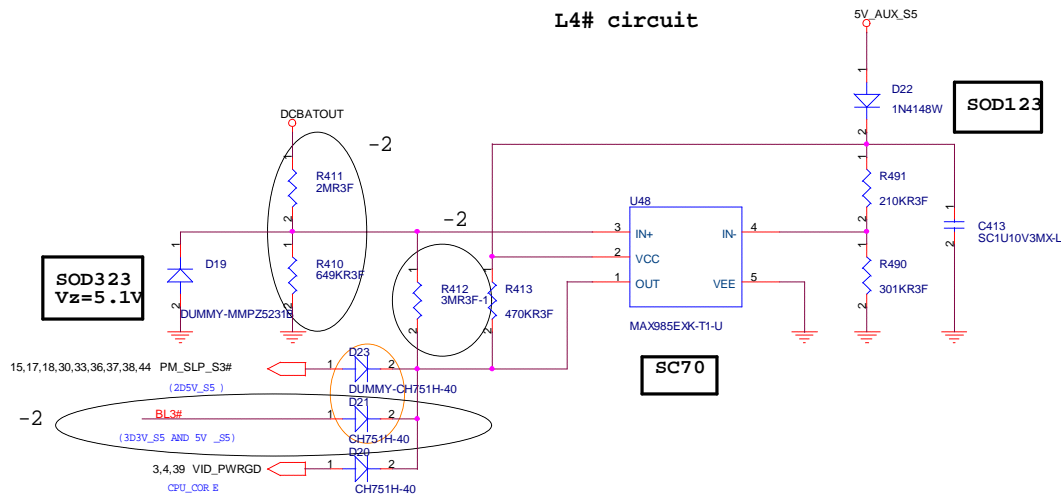
Title: **SIO(87392)**

Size: A3 Document Number: **YUHINA2&3** Rev: **-2**

Date: Thursday, April 08, 2004 Sheet: 34 of 46



L4# circuit



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Title POWER ON CIRCUIT		
Size A3	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 06, 2004	Sheet 35	of 46

A

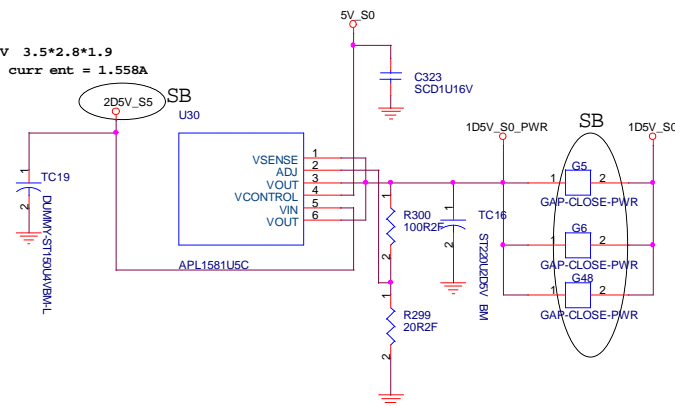
B

C

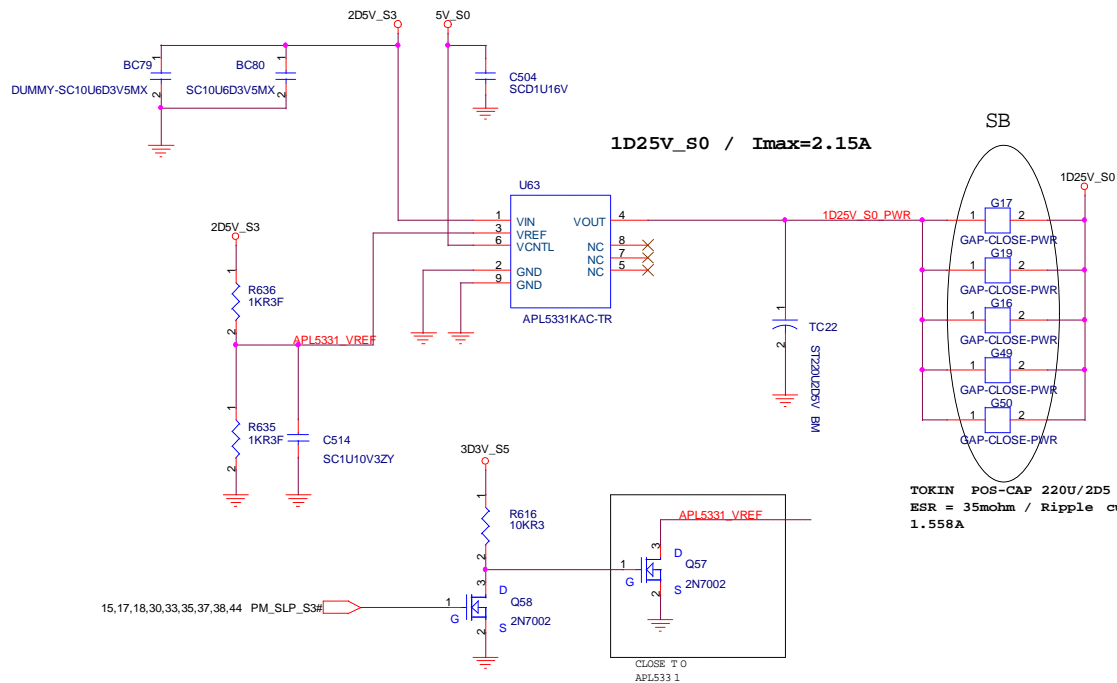
D

E

TOKIN POS-CAP 150U/4V 3.5*2.8*1.9
ESR = 35mohm / Ripple current = 1.558A



TOKIN POS-CAP 220U/2D5 3.5*2.8*1.9
ESR = 35mohm / Ripple current = 1.558A



TOKIN POS-CAP 220U/2D5 3.5*2.8*1.9
ESR = 35mohm / Ripple current = 1.558A

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
1D25V_S0_APL5331 / 1D5V_S0_APL1581/L4

Size A3 Document Number YUHINA2&3 Rev -2

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A

B

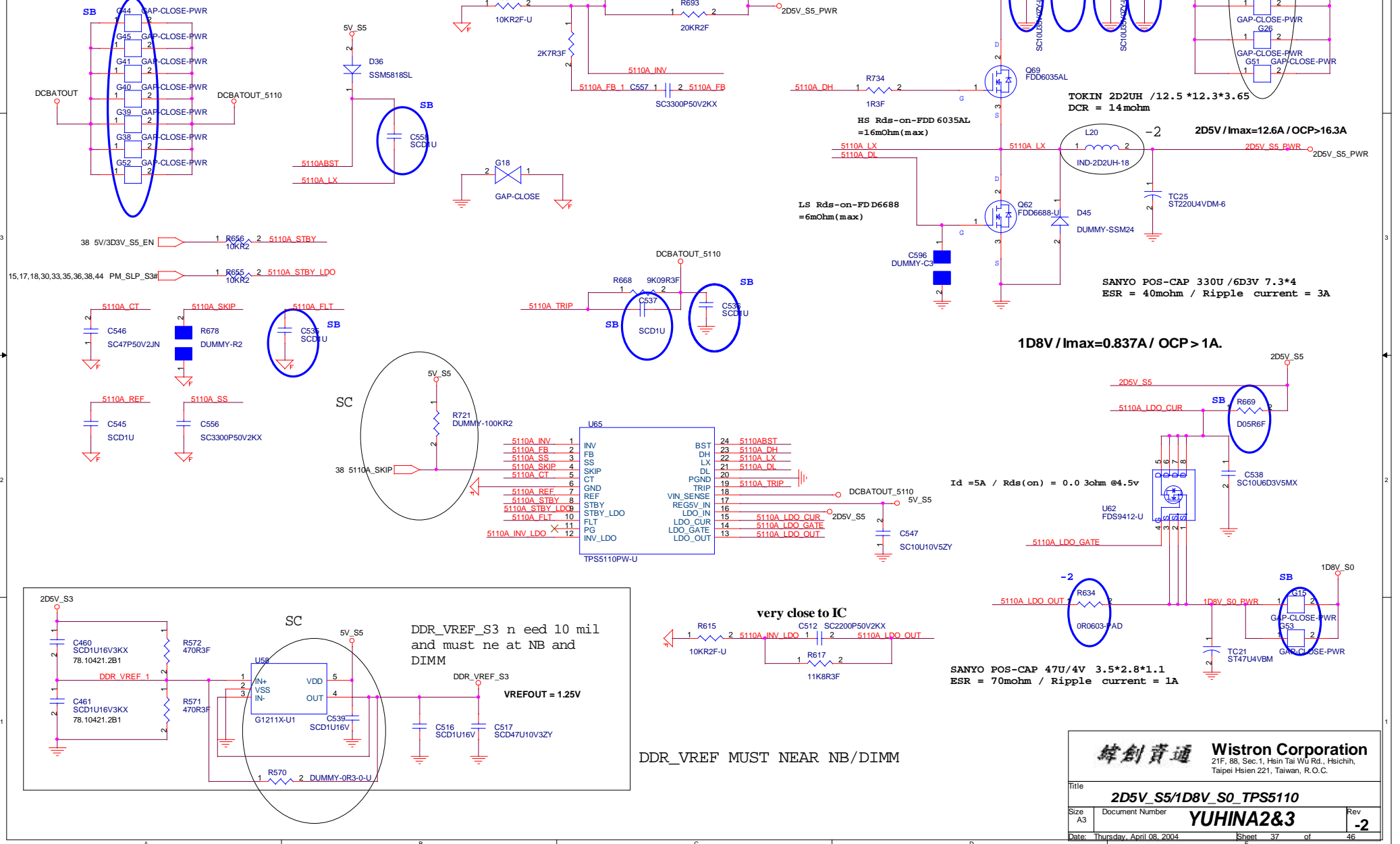
C

D

E

TI TPS5110 for 2.5V and 1.8V

CT = 47pF/300KHz
2D5V_S5: 1.2.6Amax , OCP > 16.3A
1D8V_S0: 0.837Amax , OCP > 1A

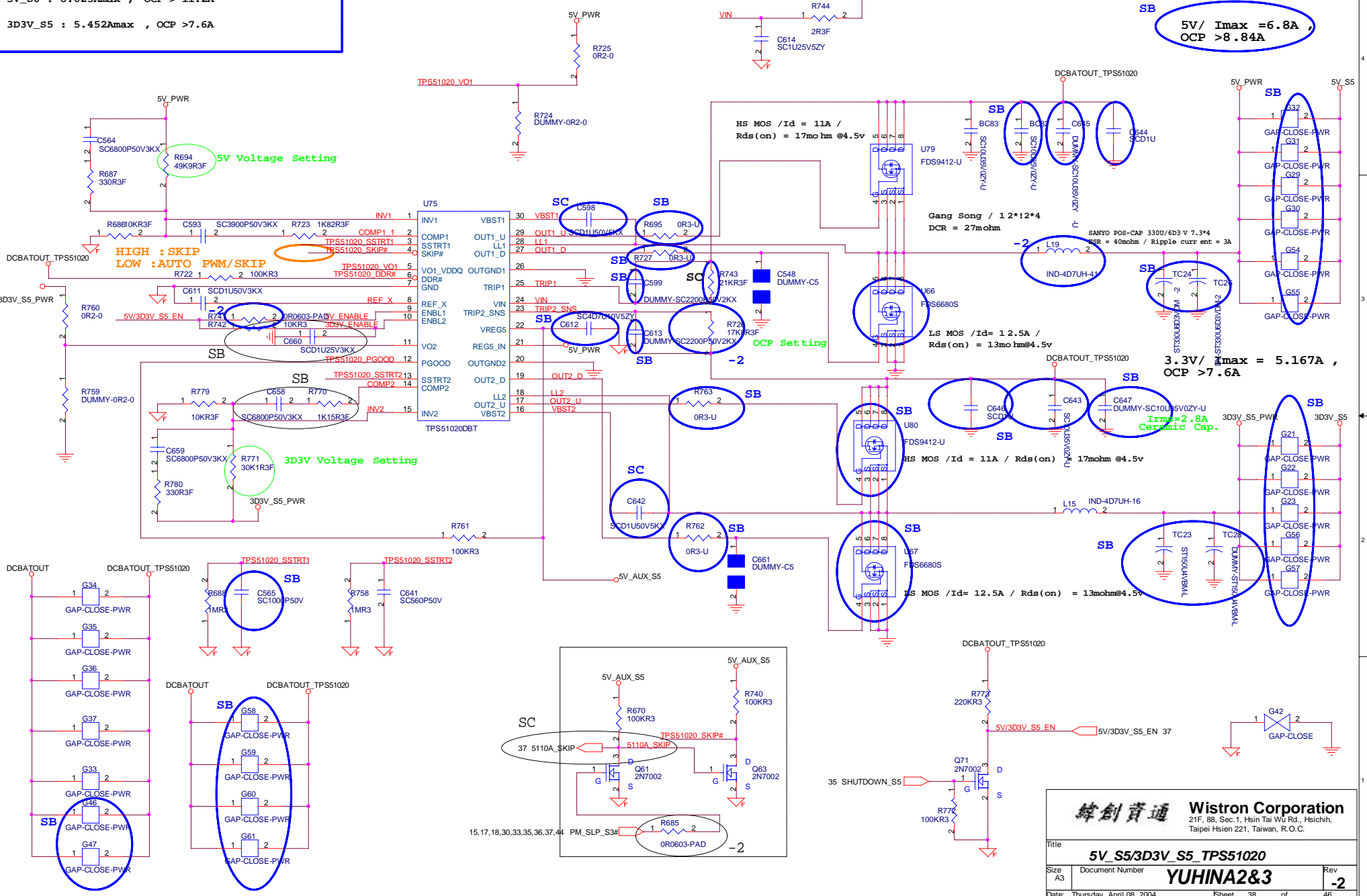


緯創資通 Wistron Corporation
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Title 2D5V_S5/1D8V_S0_TPS5110		
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TI TPS51020 for 5V and 3D3V

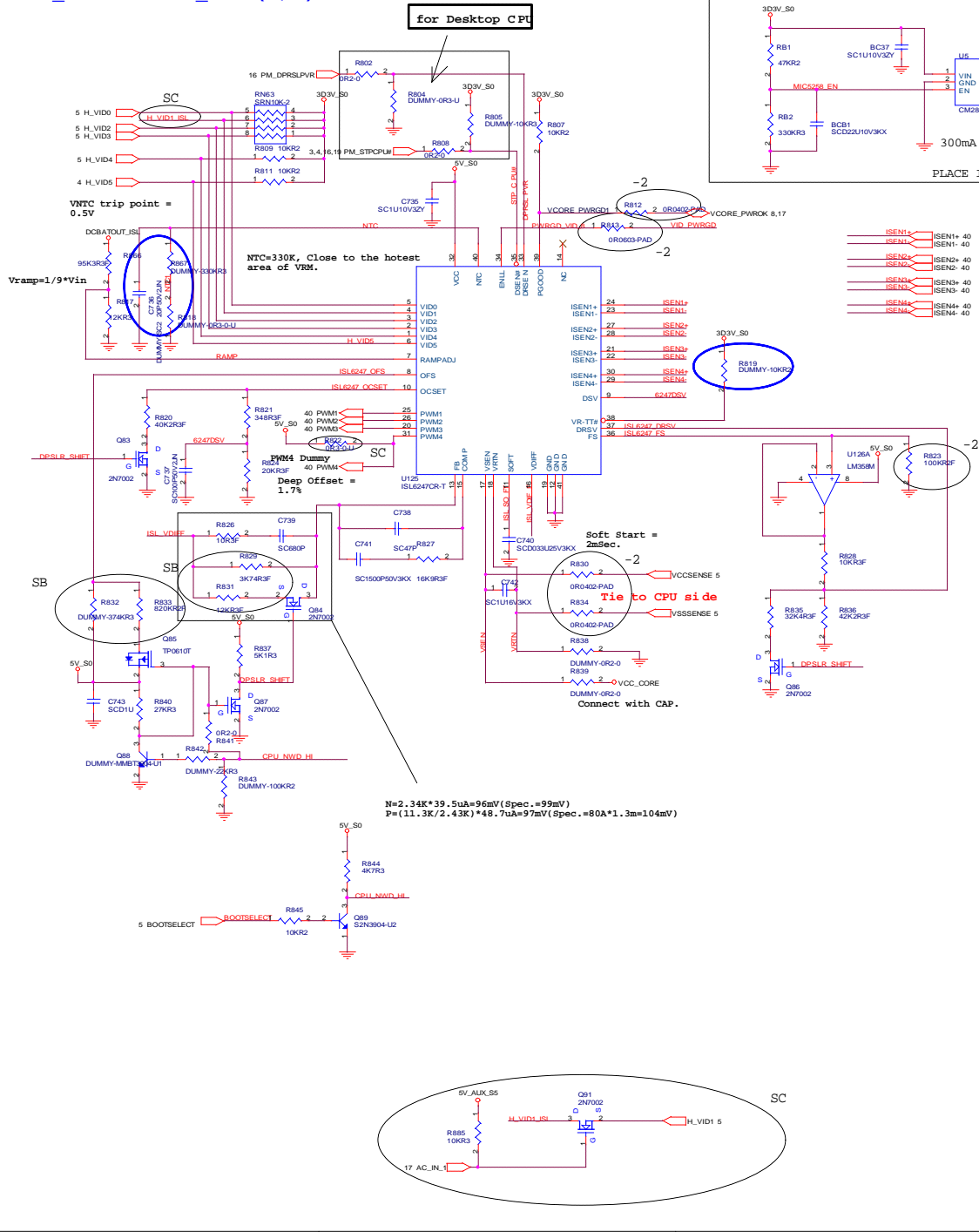
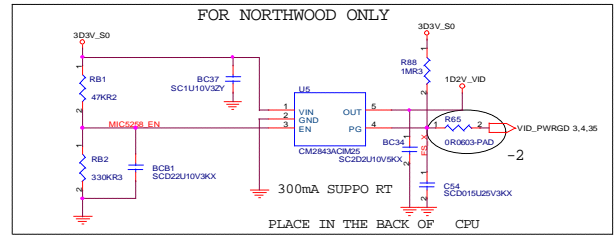
$SSTRT2 \ \& \ SSTRT1 = 1M \ \Omega / 270KHz$
 $5V_S0 : 8.625A_{max} , OCP > 11.2A$
 $3D3V_S5 : 5.452A_{max} , OCP > 7.6A$



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Title		
5V_S5/3D3V_S5_TPS51020		
Size	Document Number	Rev
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CPU_Vcore IMVP5_FMB1(1/2)



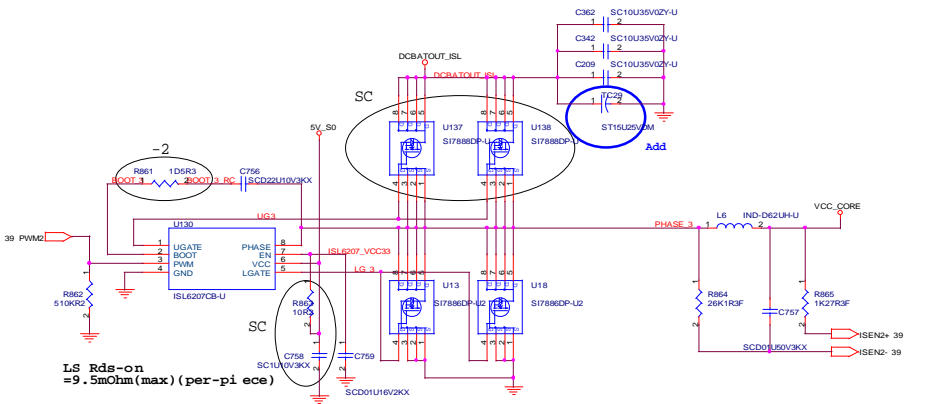
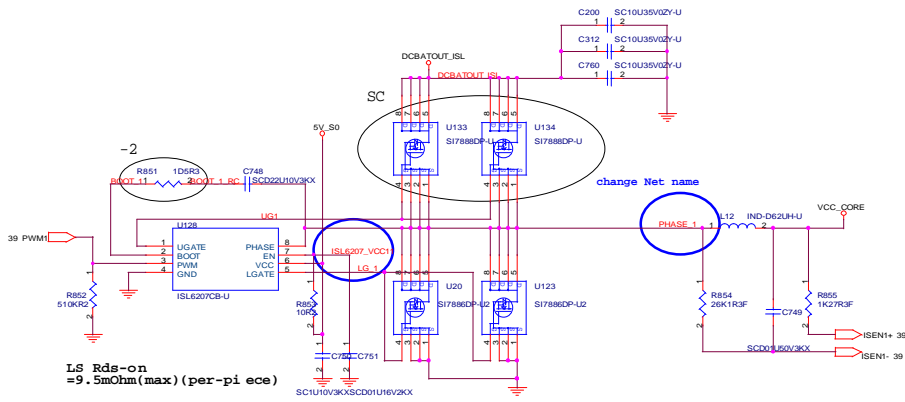
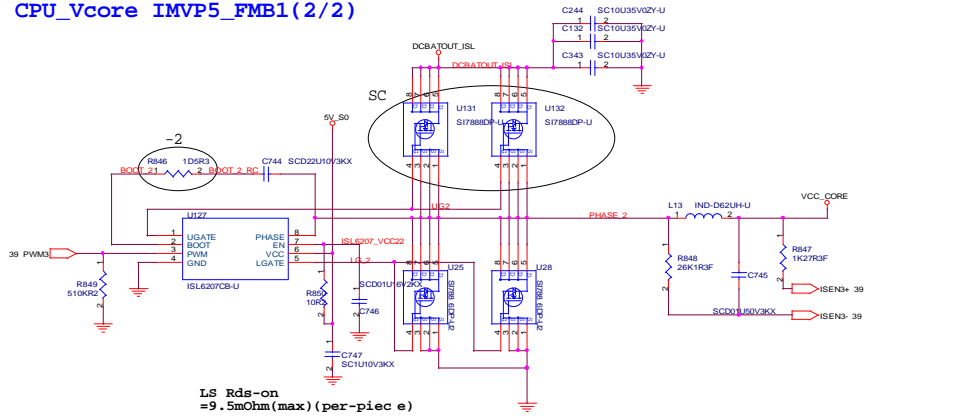
Voltage Identification Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
X	1	1	1	1	1	OFF
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	1	1	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750

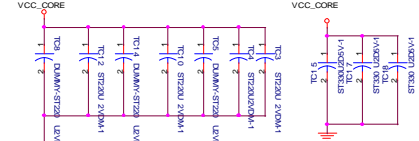
Voltage Identification Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	1	1	1	1.4875
0	1	1	1	1	0	1.5000
0	1	1	1	1	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	1	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	1	1.5875
0	1	0	1	0	1	1.6000

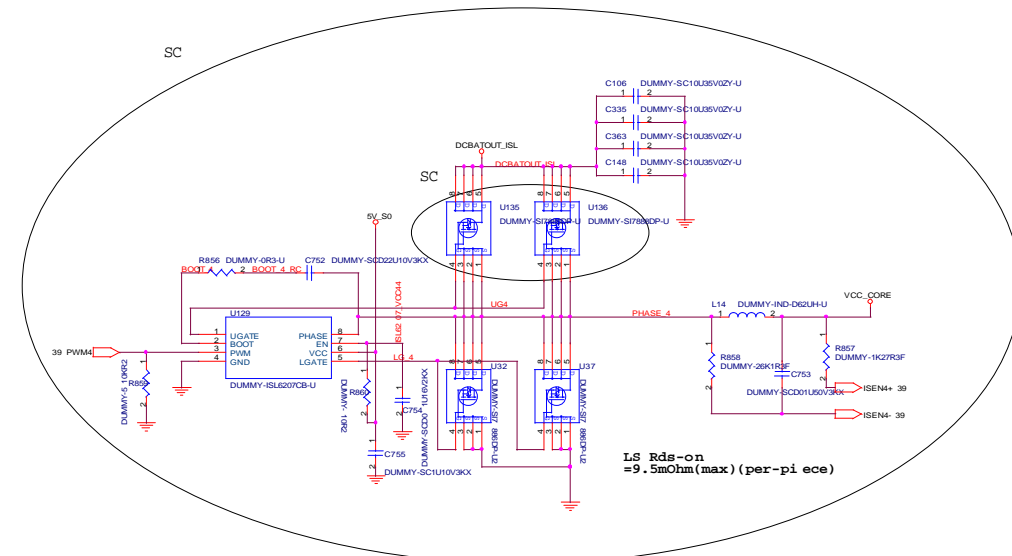
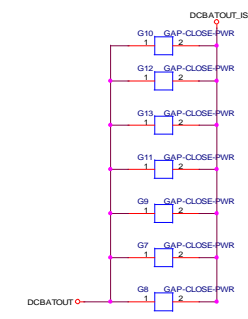
CPU_Vcore IMVP5_FMB1(2/2)

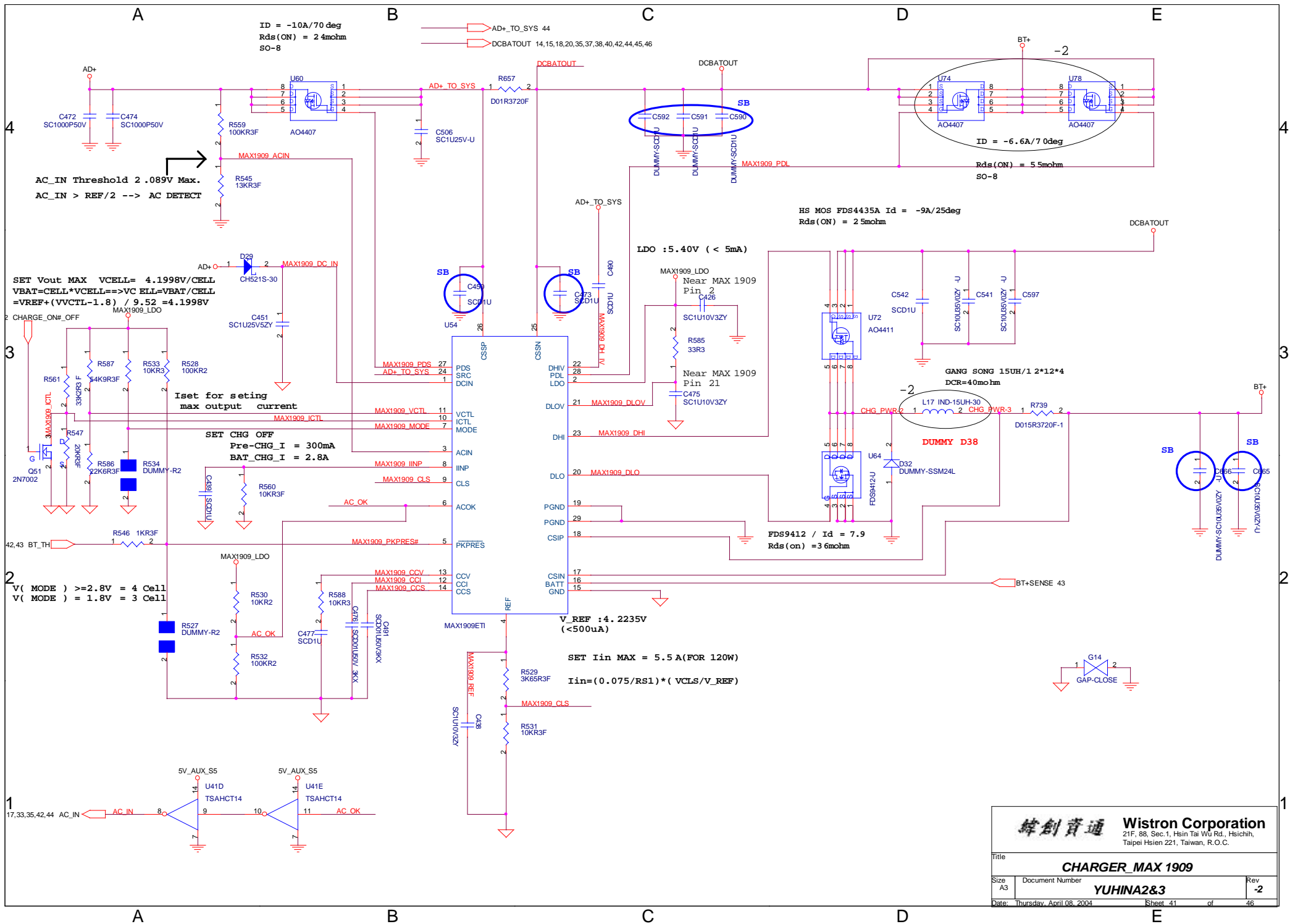


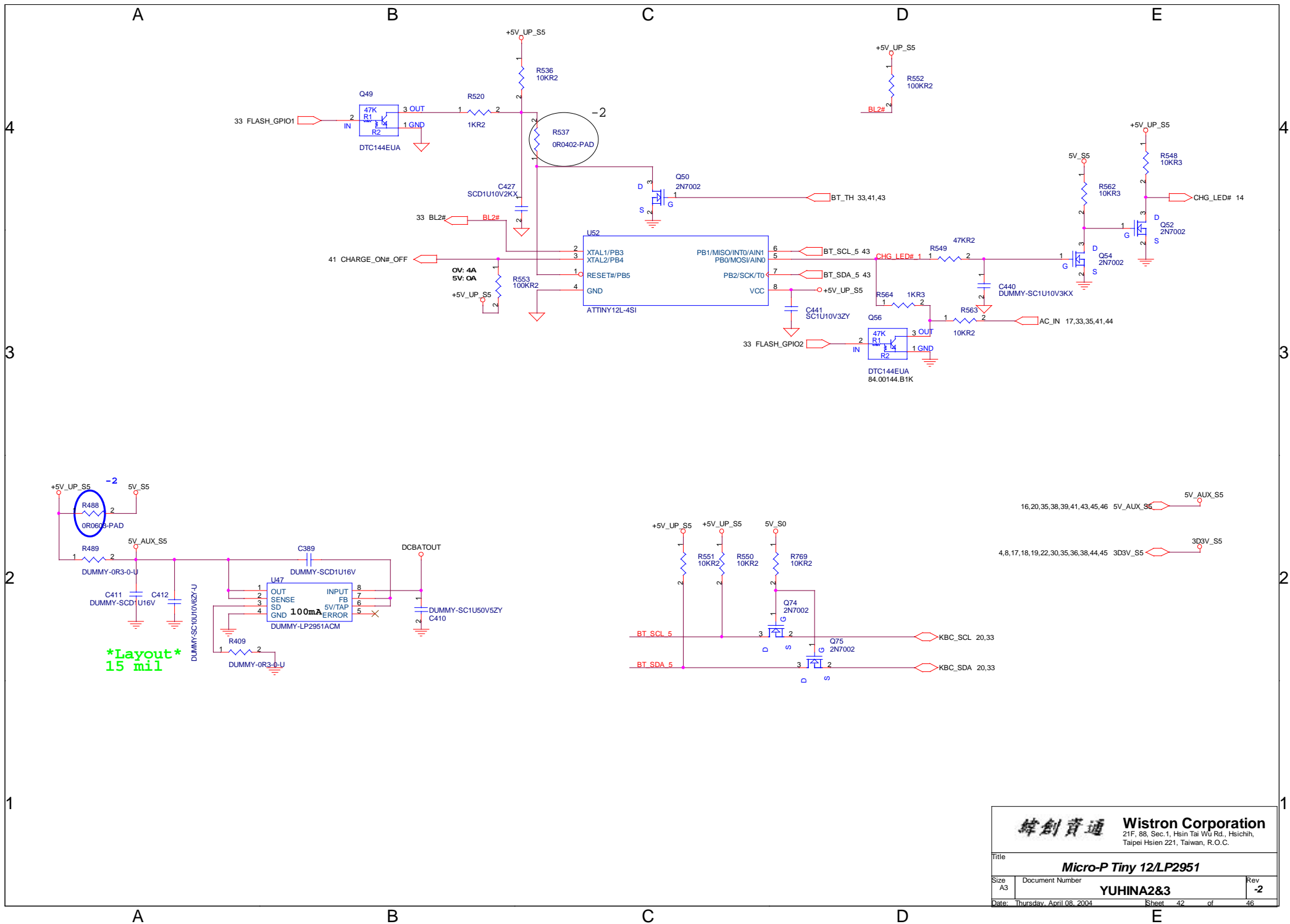
PLACE IN THE BACK OF CPU, ESR < (TED)mohm,



PANASONIC/ 330U2V 7.3*4.3*1.9
ESR=9mohm / ripple current
=3A



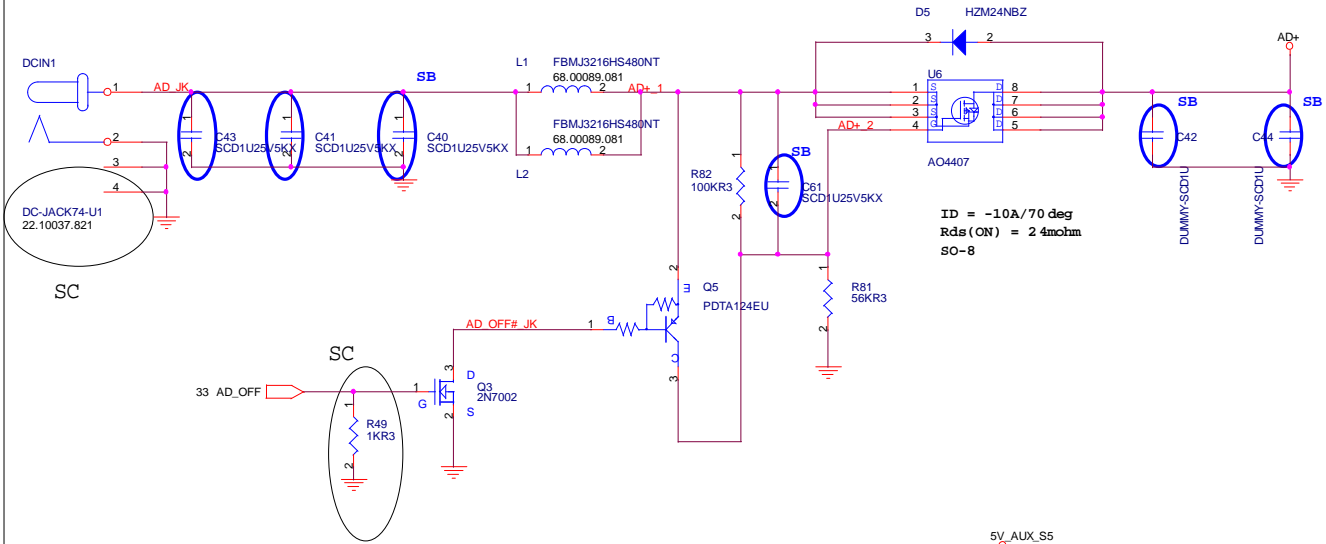




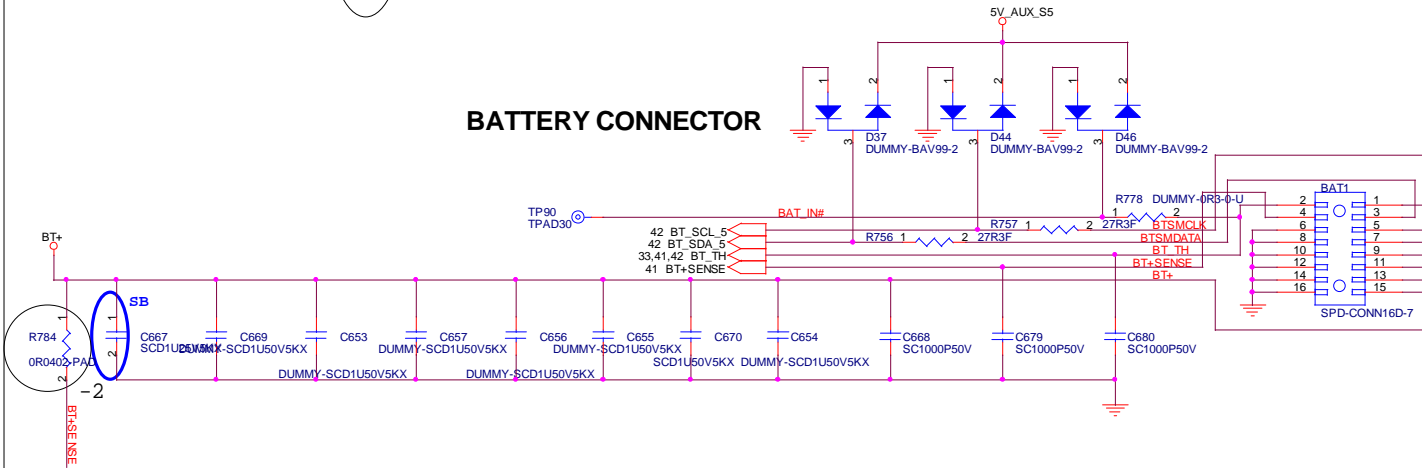
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Title		
Micro-P Tiny 12/LP2951		
Size	Document Number	Rev
A3	YUHINA2&3	-2
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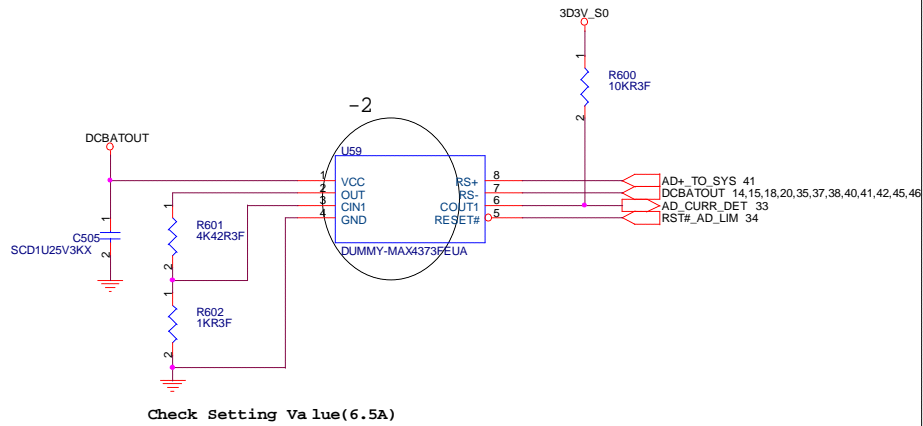
Adaptor in to generate DCBATOUT



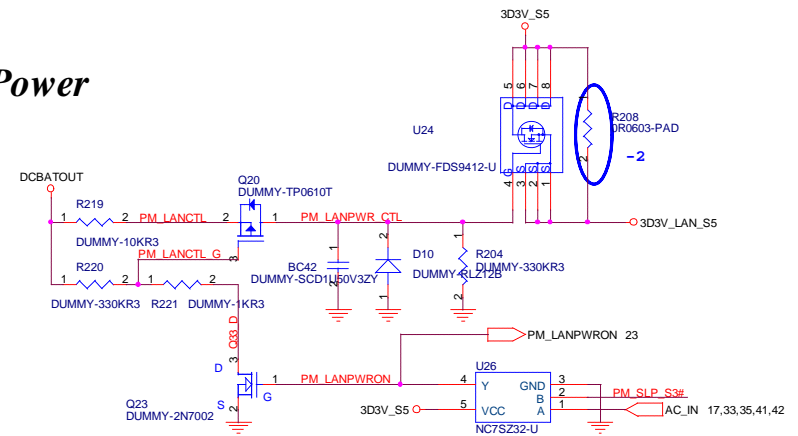
BATTERY CONNECTOR



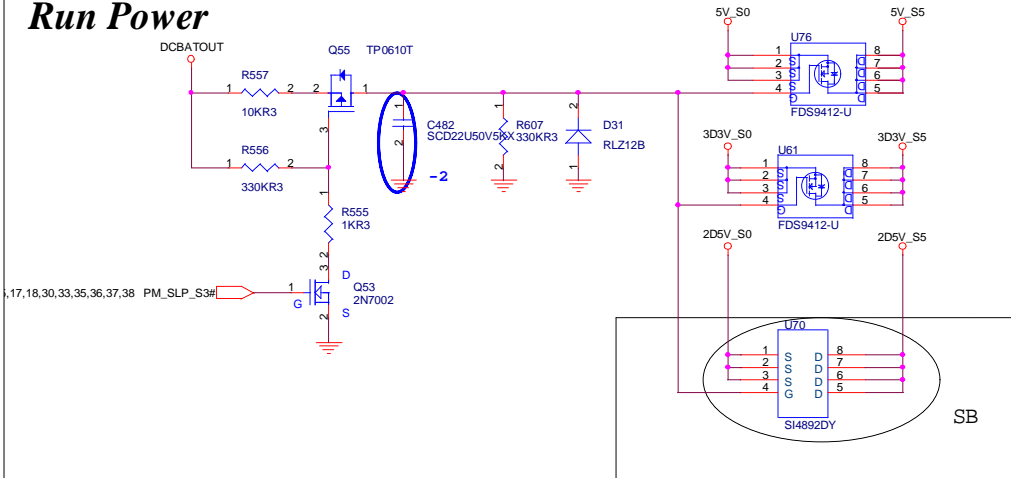
緯創資通		Wistron Corporation	
21F, 98, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 98, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AD/BATT CONN			
Size A3	Document Number YUHINA2&3	Rev -2	
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LAN Power

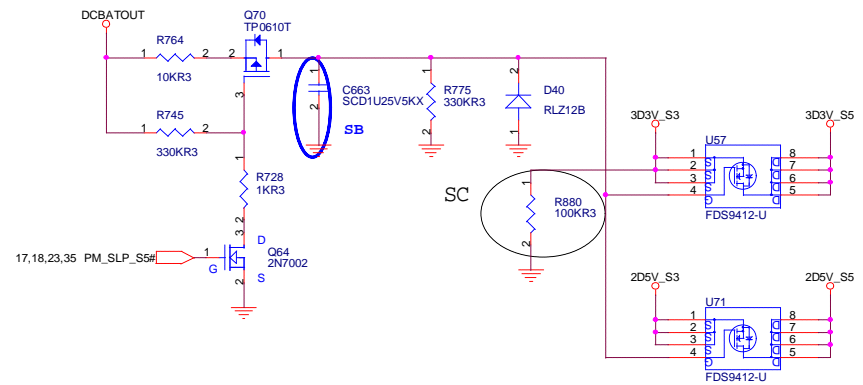


Run Power



Suspend Power

Support standby wakeup LAN only

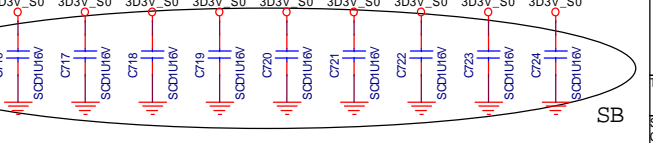
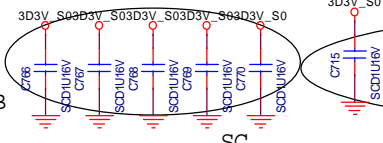
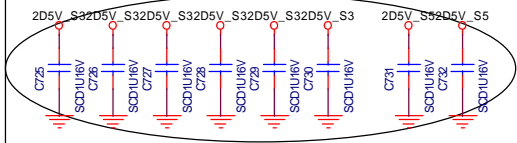
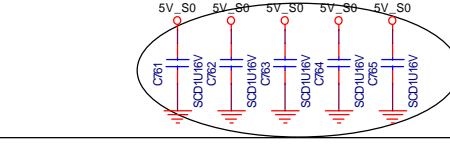
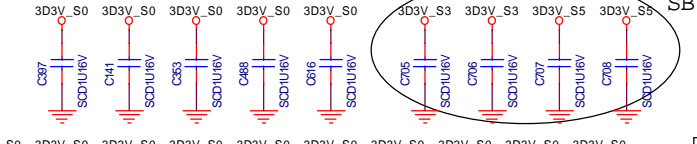
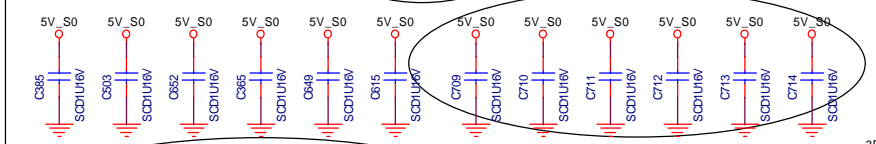
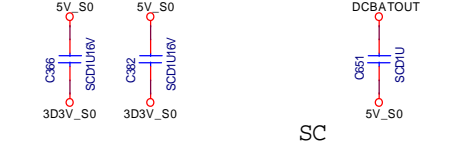
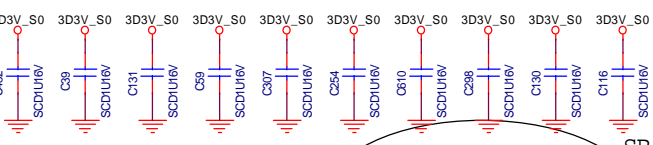
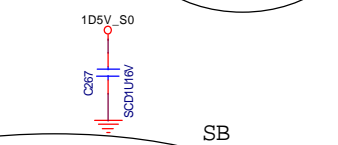
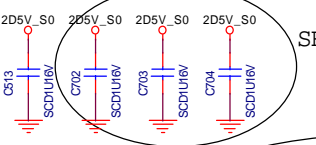
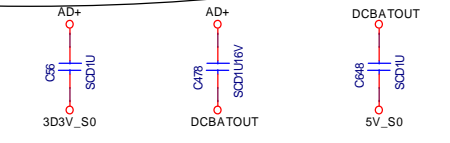
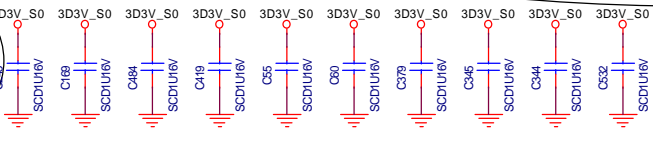
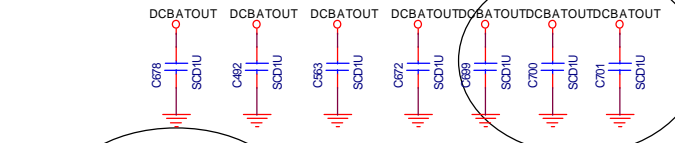
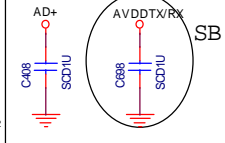
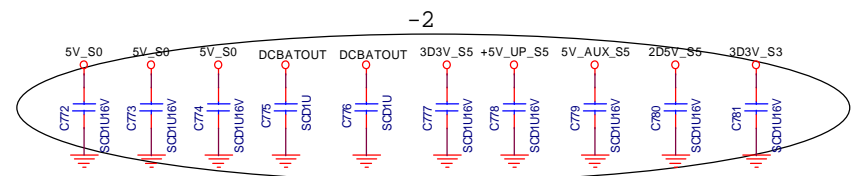
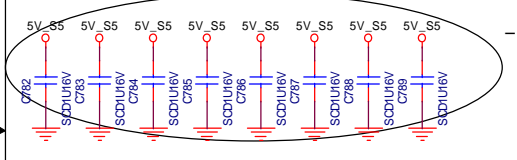
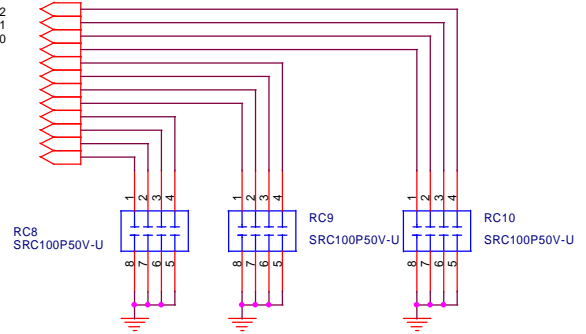
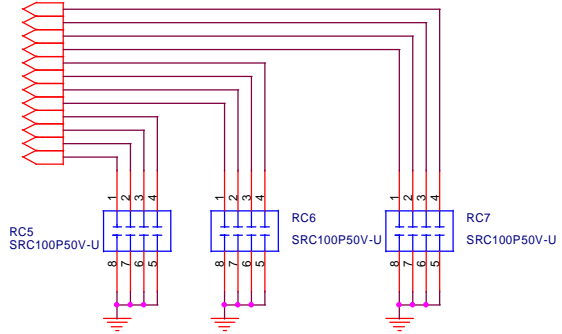


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Title		
PWRPLANE&RESETLOGIC		
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- 33 KROW8
- 33 KROW7
- 33 KROW6
- 33 KROW5
- 33 KROW4
- 33 KROW3
- 33 KROW2
- 33 KROW1
- 33 KCOL15
- 33 KCOL14
- 33 KCOL13

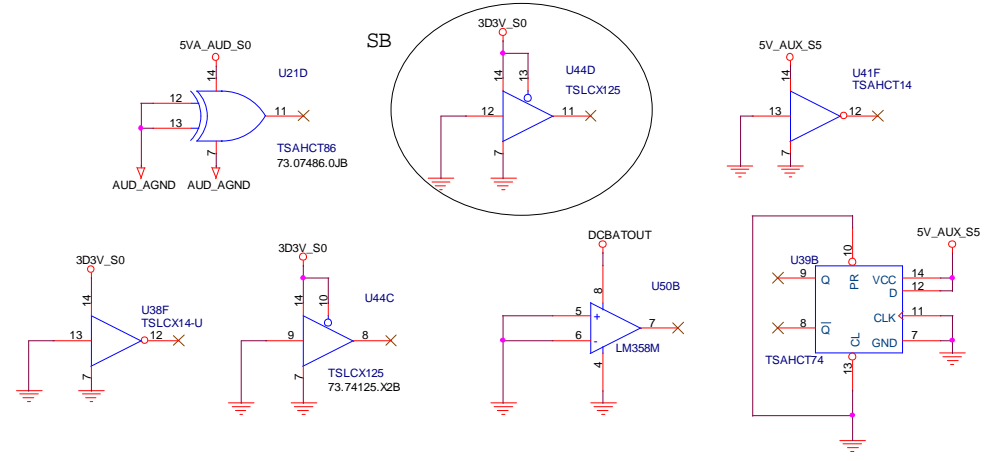
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- 33 KCOL1



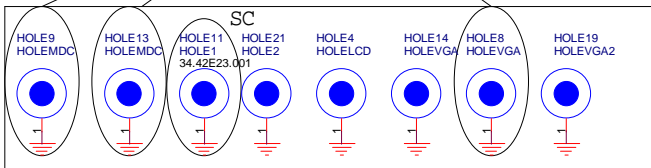
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Taipei Hsien 221, Taiwan, R. O. C.

Title		Rev	
EMI			
Size Custom	Document Number	YUHINA2&3	
Date: Thursday, April 08, 2004	Sheet 45	of 46	

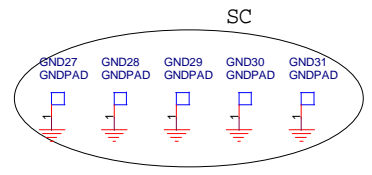
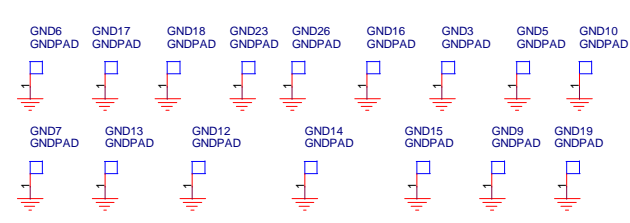
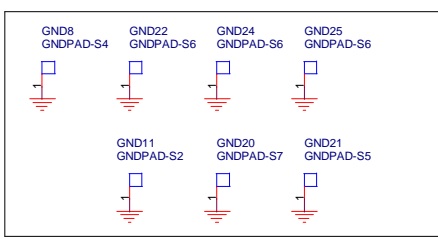
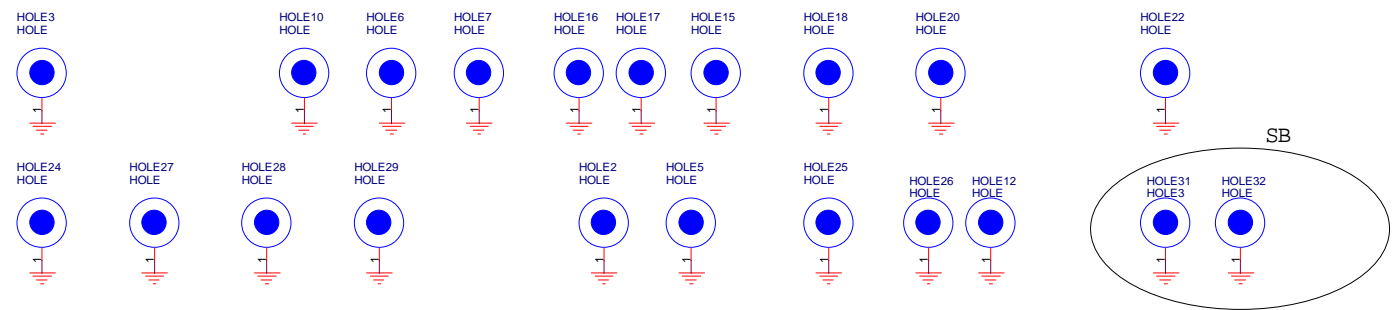
NO USE LOGIC



SB α | - » α ∩



SPARE GATES



<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title MISC</p>	
<p>Size A3</p>	<p>Document Number YUHINA2&3</p>
<p>Date: Thursday, April 08, 2004</p>	<p>Sheet 46 of 46</p>
<p>Rev -2</p>	