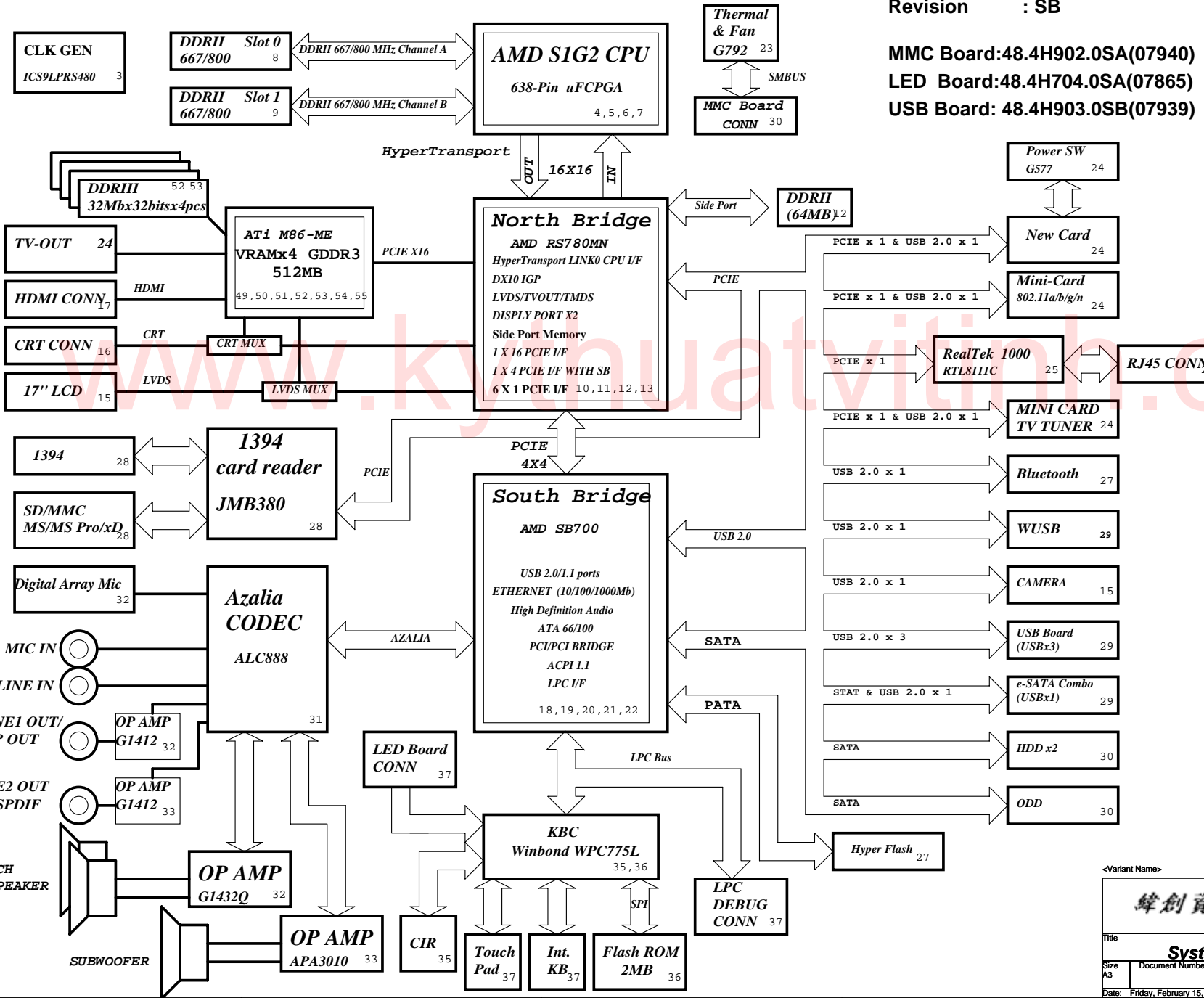


X17 Block Diagram

Project code : 91.4H901.001
 PCB Number : 07256
 Revision : SB



CPU V_CORE	
ISL6265 40, 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

MMC Board: 48.4H902.0SA(07940)
 LED Board: 48.4H704.0SA(07865)
 USB Board: 48.4H903.0SB(07939)

SYSTEM DC/DC	
TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC	
TPS51125 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC	
LDO 45	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC	
LDO 45	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC	
TPS51125 42	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Variant Name>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **System Block Diagram**

Size A3	Document Number X17	Rev SA
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Date: Friday, February 15, 2008 Sheet 1 of 56

		USB PORT#	DESTINATION
SB700	2.0	0	Combo (ESATA/USB)
		1	USB1
		2	USB2
		3	CAMERA
		4	Bluetooth
		5	NEW CARD
		6	USB3
		7	WLAN
		8	TV TUNER
		9	WUSB
	10	NC	
	11	NC	
	1.1	12	NC
	13	NC	

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER & 1394
Lane 4	TV tuner
Lane 5	NC

SB700 Functional Strap Definitions

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M
 Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			(DO NOT INSTALL)	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7XM and M86M ONLY) Note:1	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82M ONLY) Note:2	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYN	VGA ENABLED	0	0
BIF_HDMI_EN	HSYN	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE, MAKE AND SIZE INFO	X X X X	X X X X

Release BOM need modify

Page	Location	Schematic	BOM	2nd Source
P3	U41 (CLK GEN)	71.09480.003	71.09480.003	71.08628.003
P10	U65 (RS780MN)	71.RS780.M02	71.RS780.M07	
P18	U74 (SB700)	71.SB700.M02	71.SB700.M06	
P41	U57, U11, U52, U51, (CPU power) U56, U53	ZZ.COMBO.001	84.04634.037	
P46	U62 (GPU power)	ZZ.COMBO.001	84.07686.037	
P12	U17 (Side Port)	72.18512.M0U		72.18512.M0U (Qimonda) 72.55162.00U (HYNIX) 72.45116.A0U (Samsung)
P53 P54	U68~U71 (Vram)	72.18321.00U (Qimonda 700M)		72.18321.A0U (Qimonda 900M) 72.18321.00U (Qimonda 700M) 72.41032.B0U (Samsung)

Main source 3rd source

ATI RESERVED CONFIGURATION STRAPS								
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET								
VHAD0	VIP0	VIP2	VIP4	VIP6	VIP7	GPIO2	GPIO3	H2SYN
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET								
GPIO_28_TDO	GENERICC	GPIO21_BB_EN						

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED
 NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED
 IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

<Variant Name>

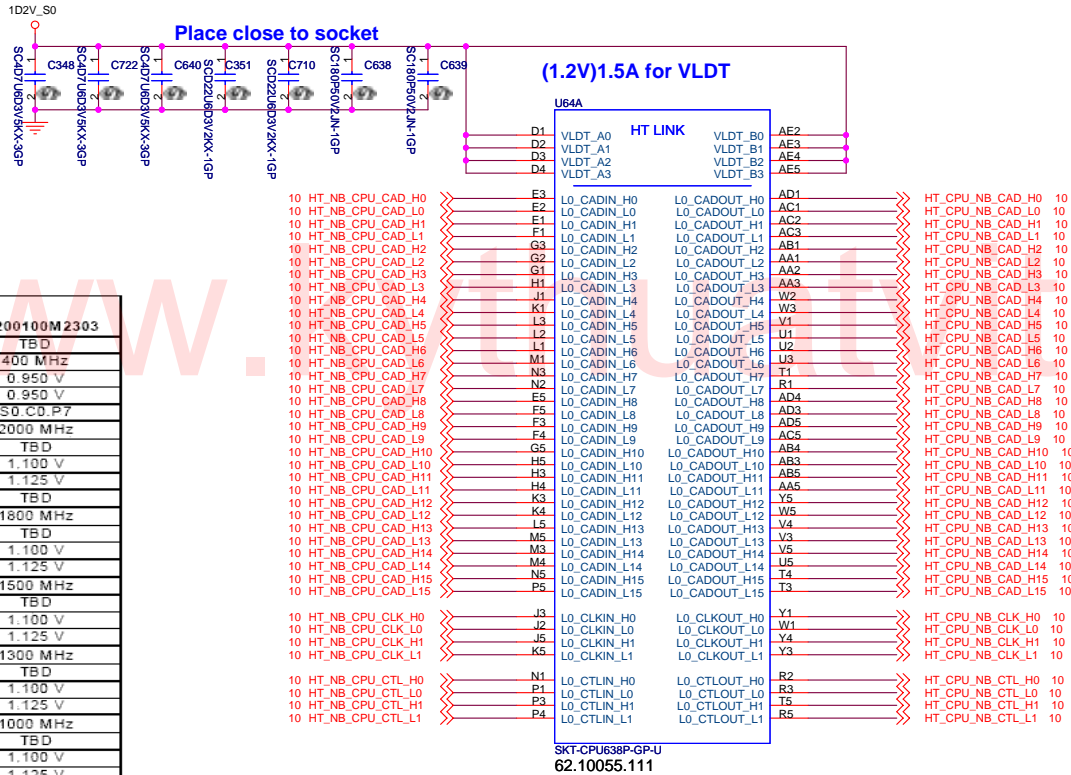
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Table of Content**

Size: A3 Document Number: **X17** Rev: **SA**

Date: Friday, February 15, 2008 Sheet 2 of 56

SSID = CPU



State	Specification	Notes	2M200100M2303
S0.CO.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
S0.CO.P0	Startup F-state		S0.CO.P7
	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.CO.P1	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
	CPU COF	1	1800 MHz
	TDP	3	TBD
S0.CO.P2	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
	TDP	3	TBD
S0.CO.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.CO.P4	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
S0.CO.P5	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
S0.CO.P6	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	500 MHz
	TDP	3	TBD
S0.CO.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD

- 10 HT_NB_CPU_CAD_H0
- 10 HT_NB_CPU_CAD_L0
- 10 HT_NB_CPU_CAD_H1
- 10 HT_NB_CPU_CAD_L1
- 10 HT_NB_CPU_CAD_H2
- 10 HT_NB_CPU_CAD_L2
- 10 HT_NB_CPU_CAD_H3
- 10 HT_NB_CPU_CAD_L3
- 10 HT_NB_CPU_CAD_H4
- 10 HT_NB_CPU_CAD_L4
- 10 HT_NB_CPU_CAD_H5
- 10 HT_NB_CPU_CAD_L5
- 10 HT_NB_CPU_CAD_H6
- 10 HT_NB_CPU_CAD_L6
- 10 HT_NB_CPU_CAD_H7
- 10 HT_NB_CPU_CAD_L7
- 10 HT_NB_CPU_CAD_H8
- 10 HT_NB_CPU_CAD_L8
- 10 HT_NB_CPU_CAD_H9
- 10 HT_NB_CPU_CAD_L9
- 10 HT_NB_CPU_CAD_H10
- 10 HT_NB_CPU_CAD_L10
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- 10 HT_NB_CPU_CAD_H14
- 10 HT_NB_CPU_CAD_L14
- 10 HT_NB_CPU_CAD_H15
- 10 HT_NB_CPU_CAD_L15
- 10 HT_NB_CPU_CLK_H0
- 10 HT_NB_CPU_CLK_L0
- 10 HT_NB_CPU_CLK_H1
- 10 HT_NB_CPU_CLK_L1
- 10 HT_NB_CPU_CTL_H0
- 10 HT_NB_CPU_CTL_L0
- 10 HT_NB_CPU_CTL_H1
- 10 HT_NB_CPU_CTL_L1

SKT-CPU638P-GP-U
62.10055.111

<Variant Name>

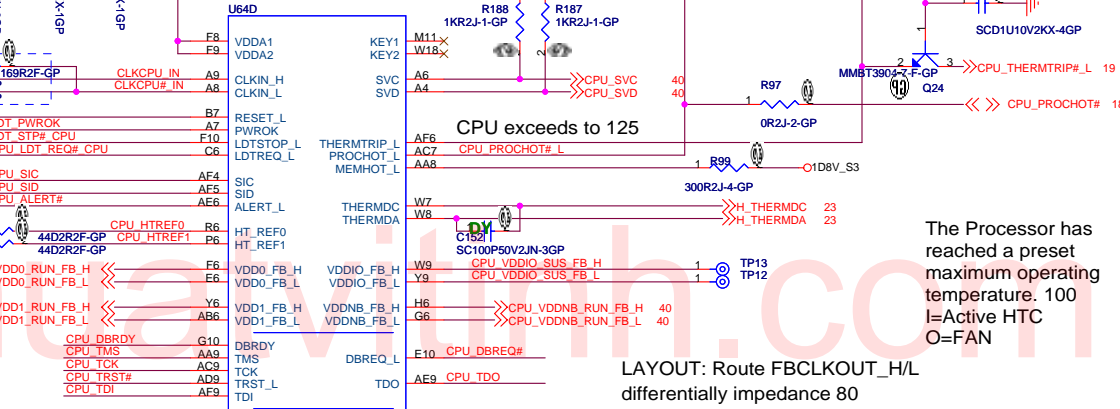
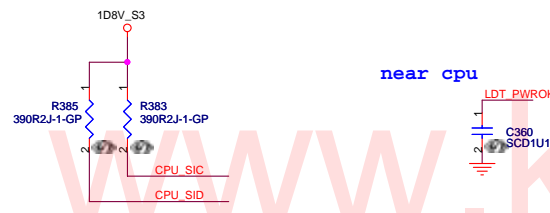
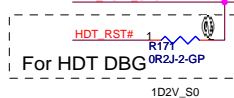
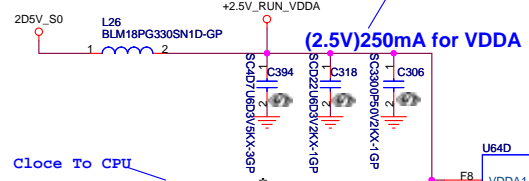
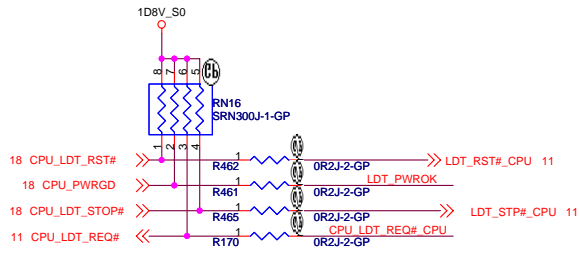
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Title
CPU HT LINK I/F (1/4)

Size A3 Document Number **X17** Rev **SA**

Date: Friday, February 15, 2008 Sheet 4 of 56

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

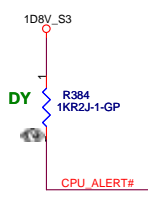


CPU exceeds to 125

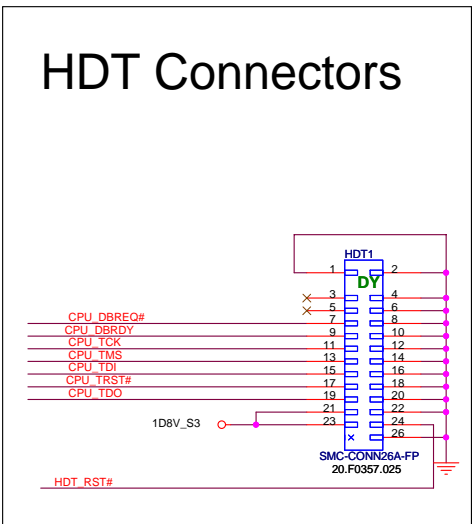
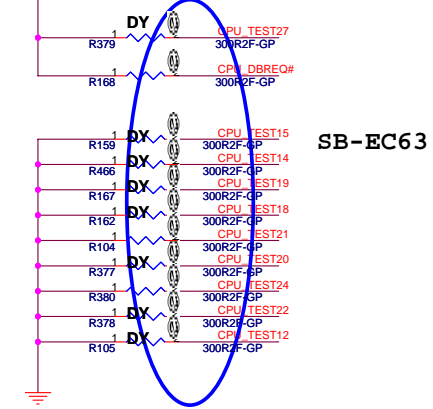
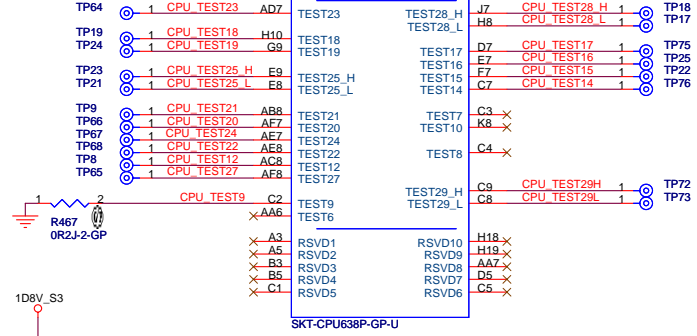
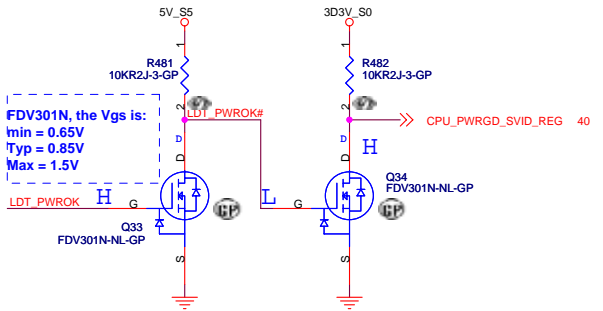
The Processor has reached a preset maximum operating temperature. 100
I=Active HTC
O=Fan

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Sideband temperature



CPU temperature sensor driver INT event to EC



<Variant Name>

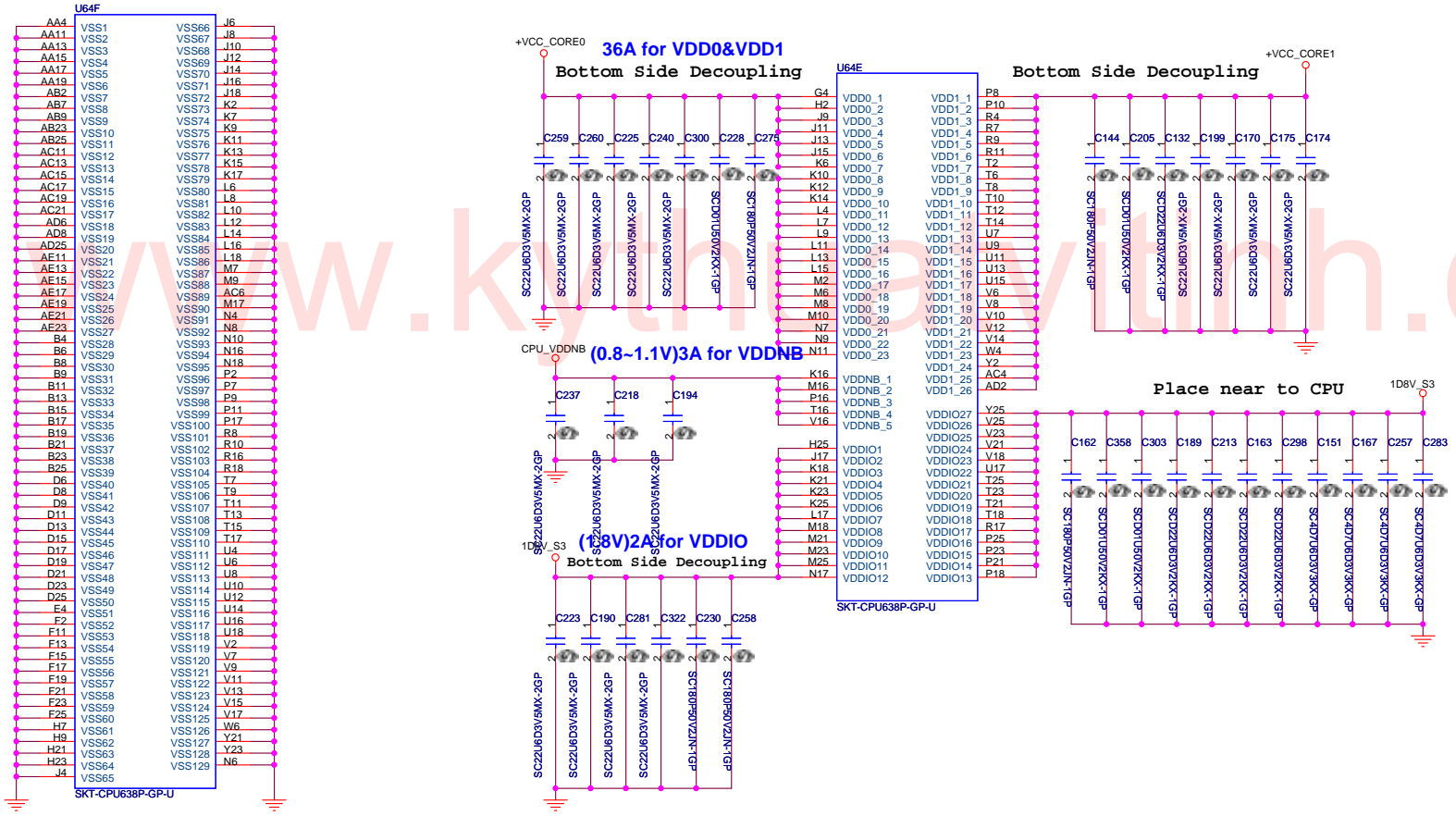
緯創資通 Wistron Corporation
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Title
CPU Control&Debug (3/4)

Size A3 Document Number X17 Rev SA

Date: Friday, February 15, 2008 Sheet 6 of 56

SSID = CPU



<Variant Name>

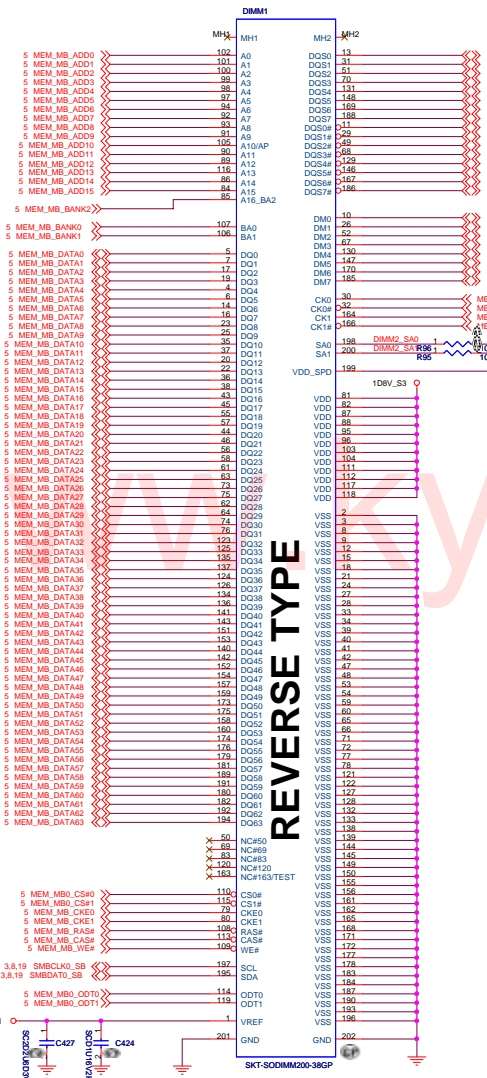
緯創資通 Wistron Corporation
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Title

CPU Power (4/4)

Size A3	Document Number	Rev SA
	X17	

Date: Friday, February 15, 2008 Sheet 7 of 56



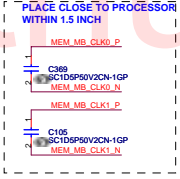
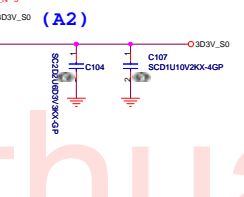
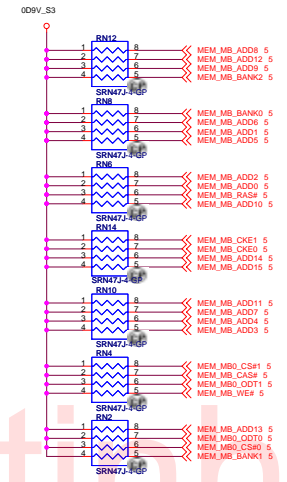
62.10017.E31
HI 5.2mm

Place C2.2uF and 0.1uF < 500mils from DDR connector!

PARALLEL TERMINATION

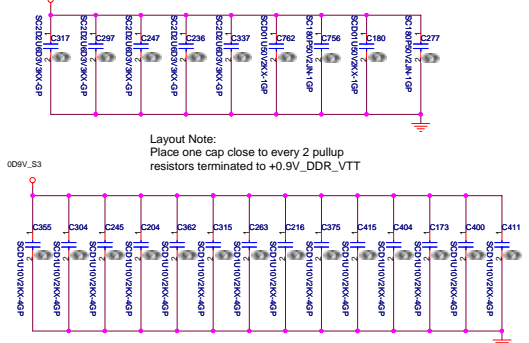
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR address and Control Signals.



Decoupling Capacitor

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

SSID = N.B

SB-EC-81

STRAP_DEBUG_BUS_GPIO_ENABLE

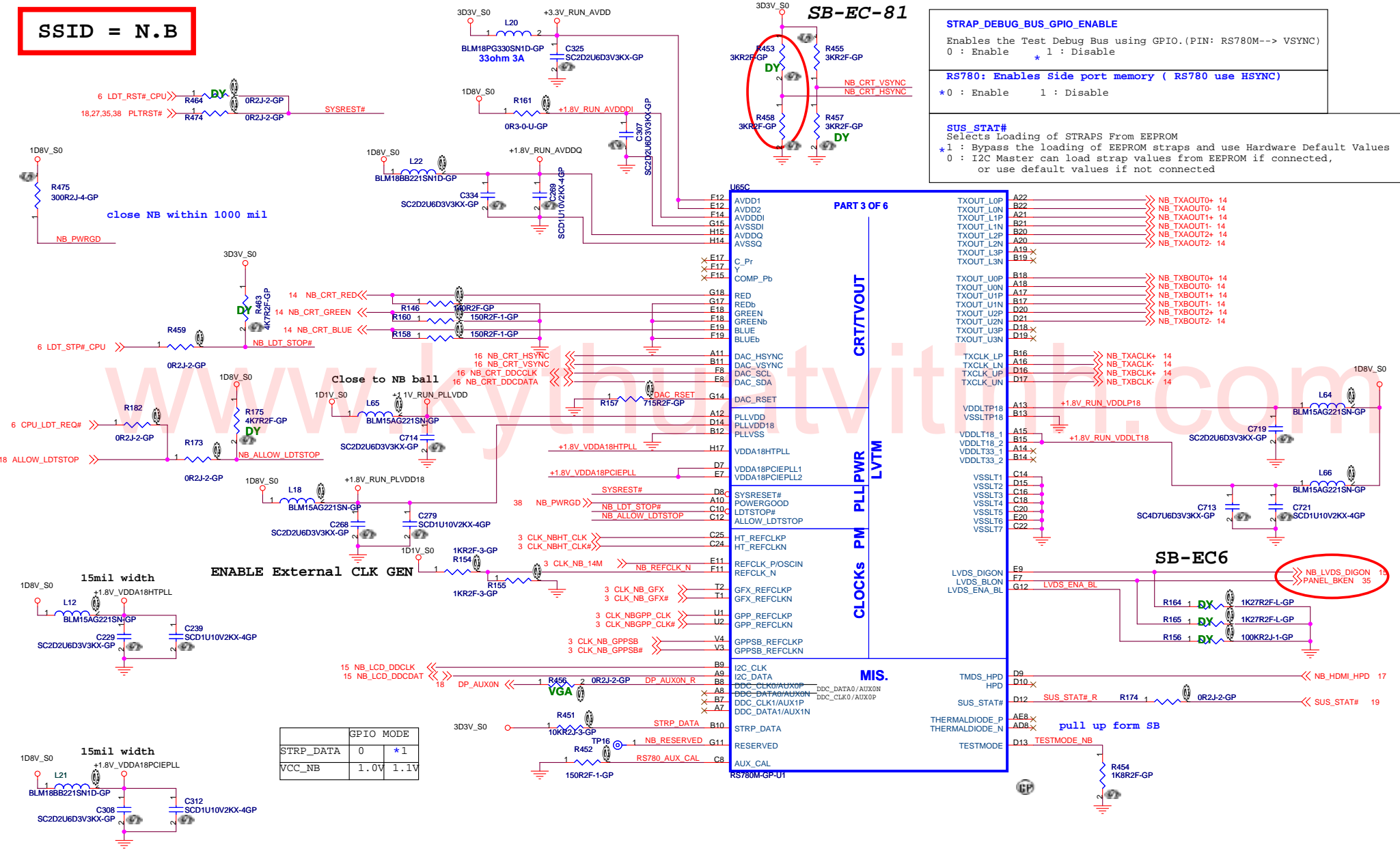
Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC)
 0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

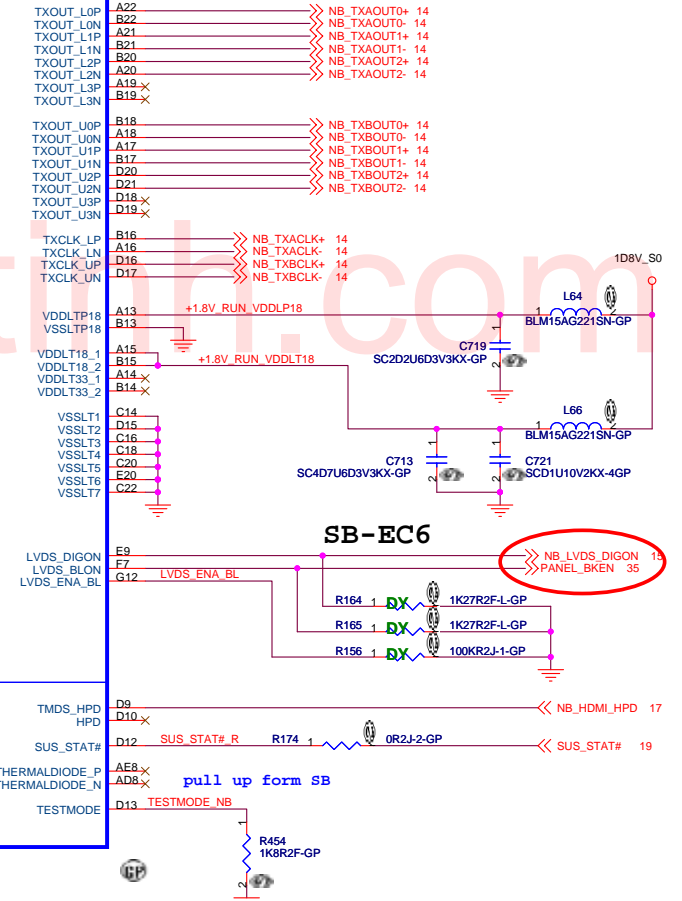
* 0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
 * 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected,
 or use default values if not connected



STRP_DATA	GPIO MODE	
STRP_DATA	0	* 1
VCC_NB	1.0V	1.1V



<Variant Name>

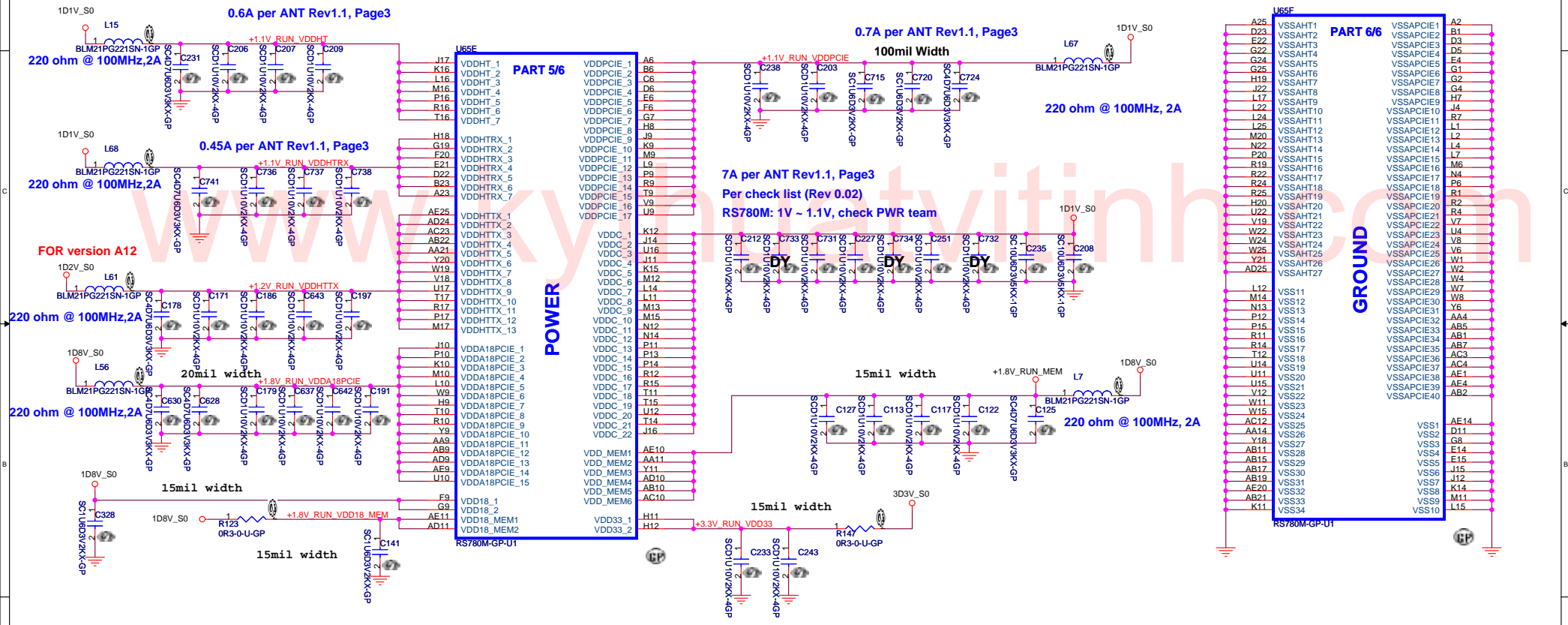
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS780M LVDS&CRT (2/4)**

Size: A3 Document Number: **X17** Rev: SA

Date: Tuesday, February 19, 2008 Sheet 11 of 56

SSID = N.B

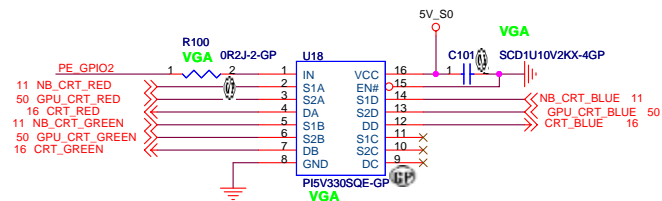
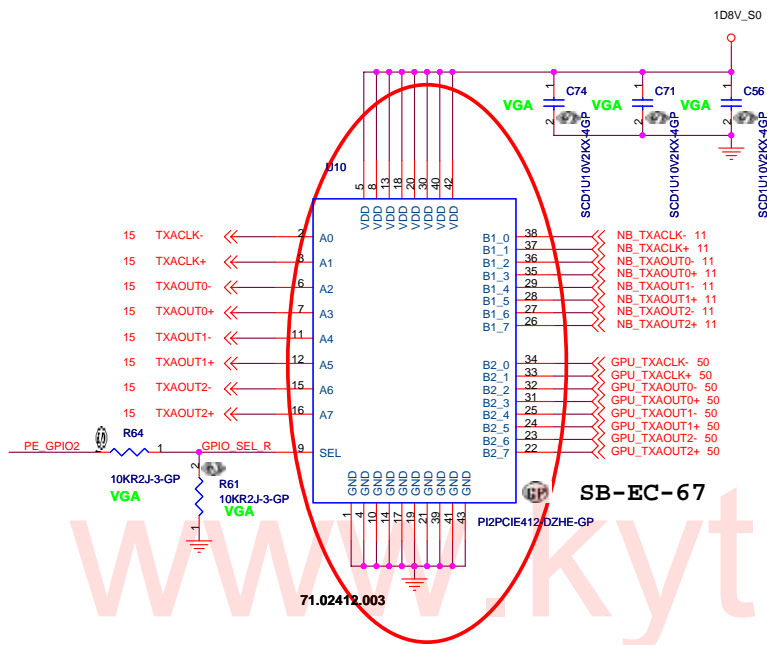


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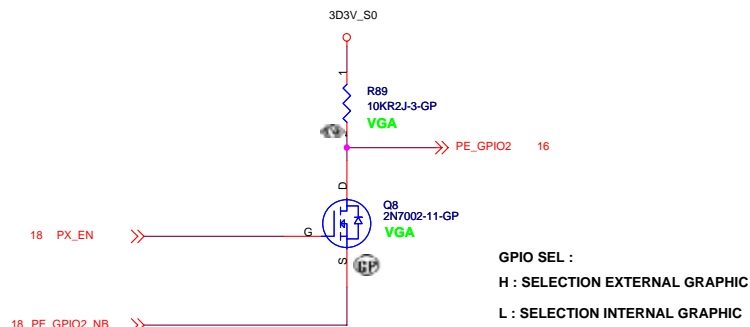
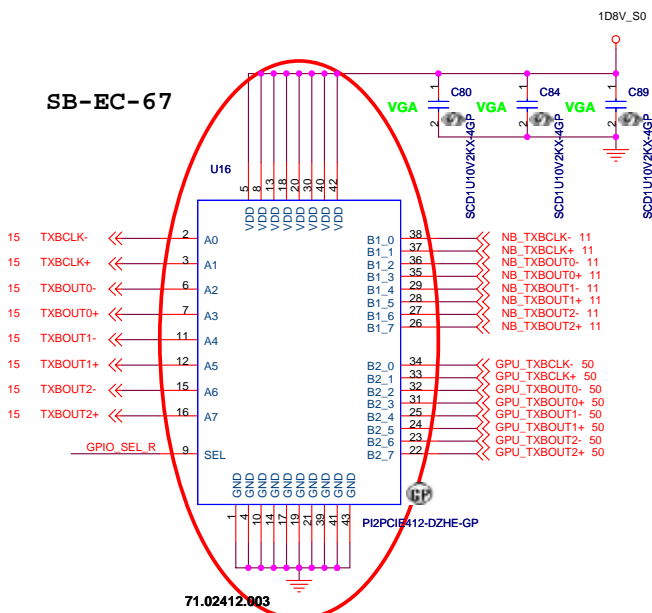
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS780M PWR&GD (4/4)**

Size: A3	Document Number: X17	Rev: SA
Date: Friday, February 15, 2008	Sheet: 13	of: 56



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<Variant Name>

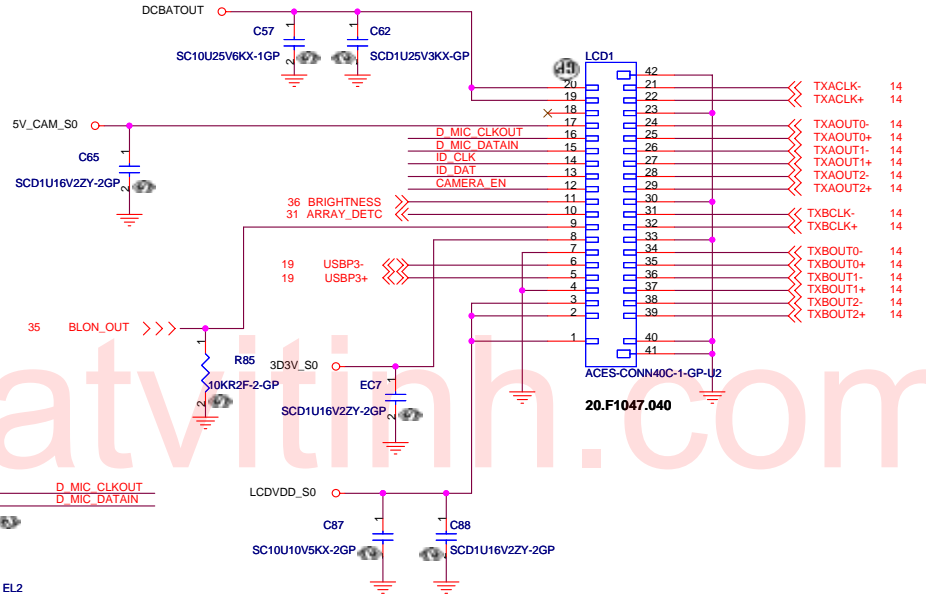
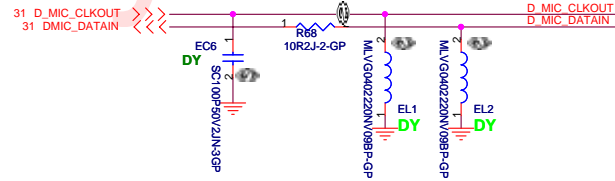
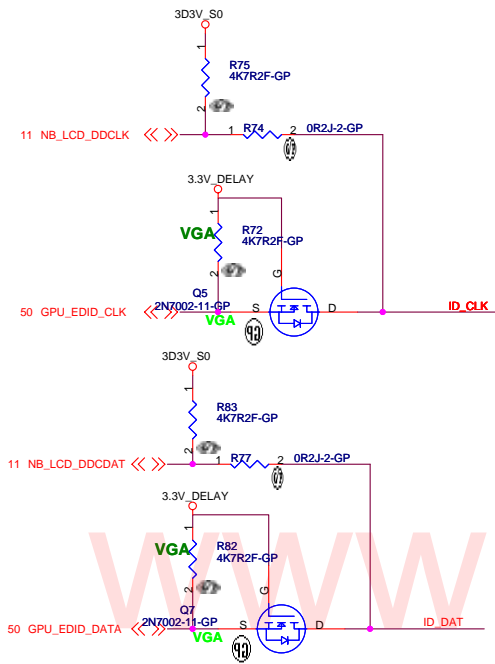
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT / LVDS MUX

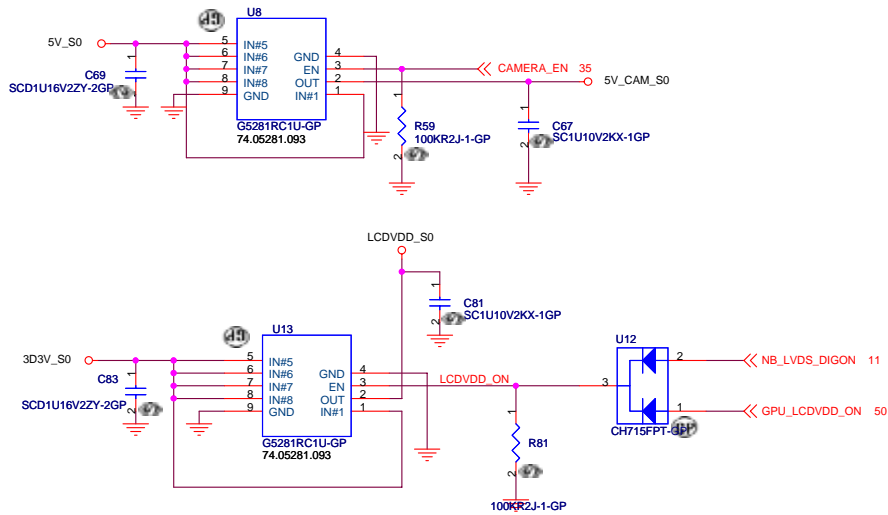
Size A3 Document Number X17 Rev SA

Date: Tuesday, February 19, 2008 Sheet 14 of 56

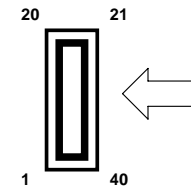
LCD CONNECTOR



CAMERA POWER



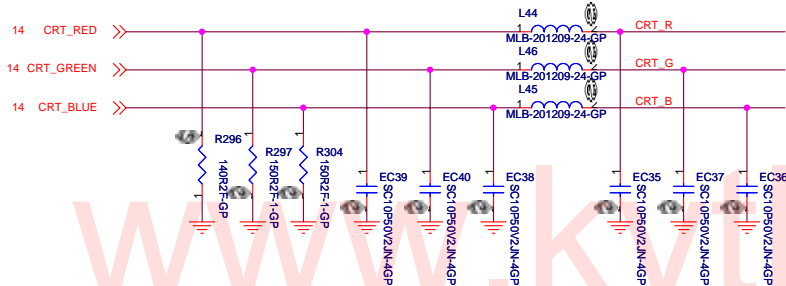
TOP VIEW



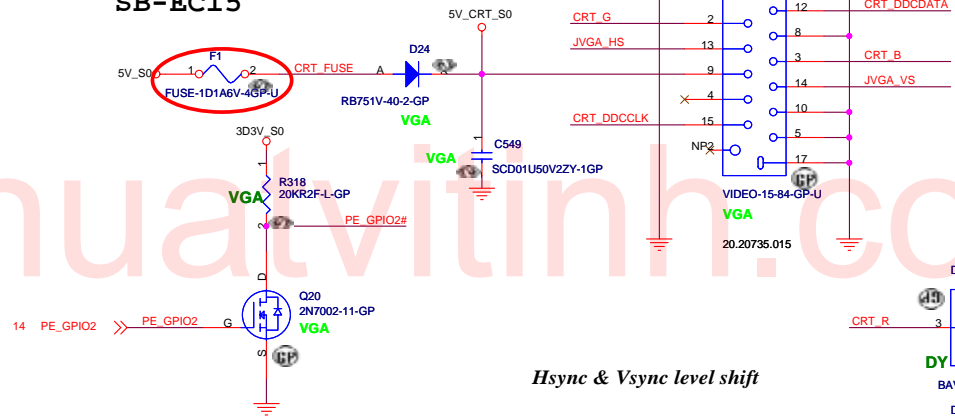
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Title LCD CONN/CAMERA		
Size A3	Document Number X17	Rev SA
Date: Tuesday, February 19, 2008	Sheet 15 of 56	

CRT I/F & CONNECTOR

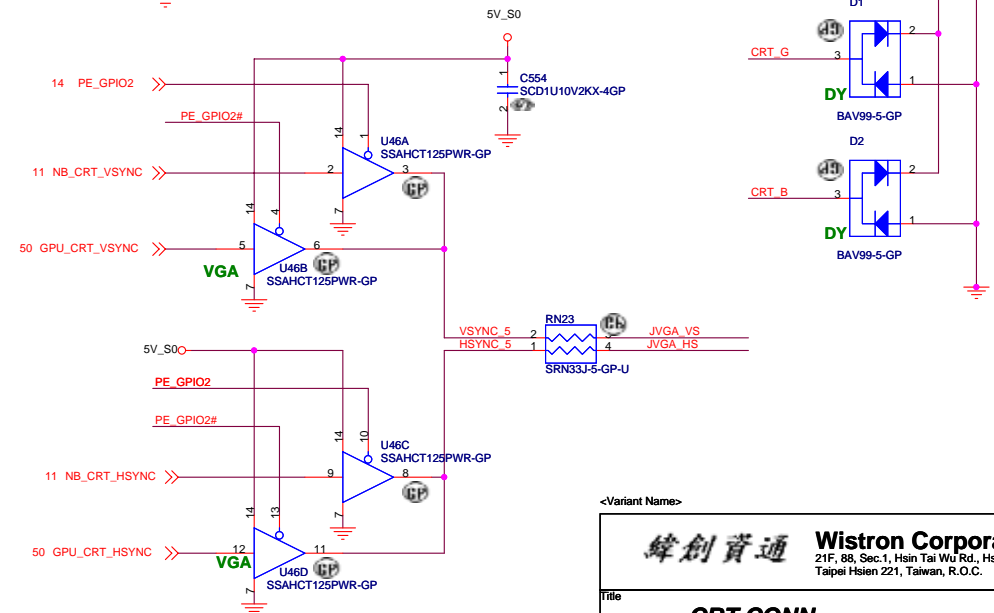
Layout Note:
Place these resistors close to the CRT-out connector



SB-EC15



Hsync & Vsync level shift



<Variant Name>

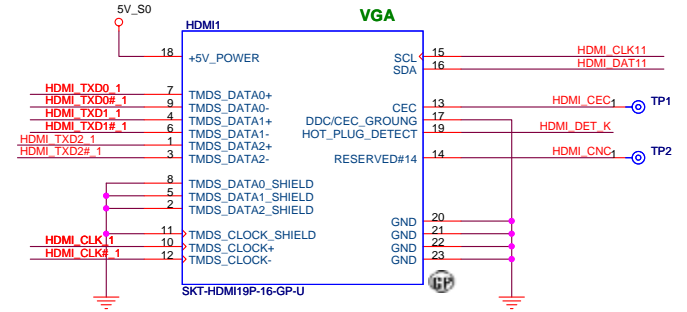
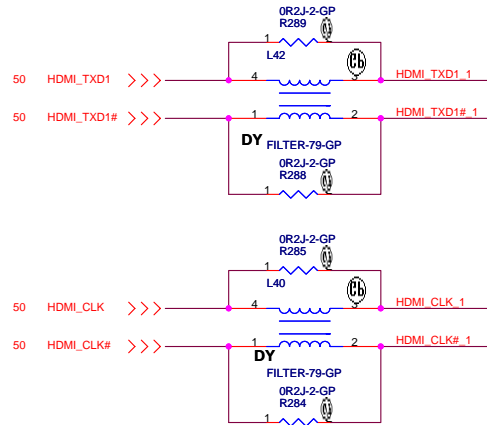
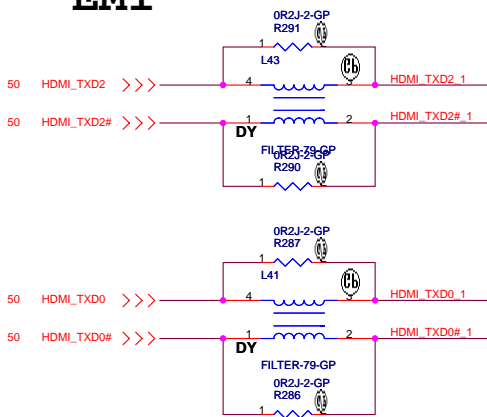
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT CONN

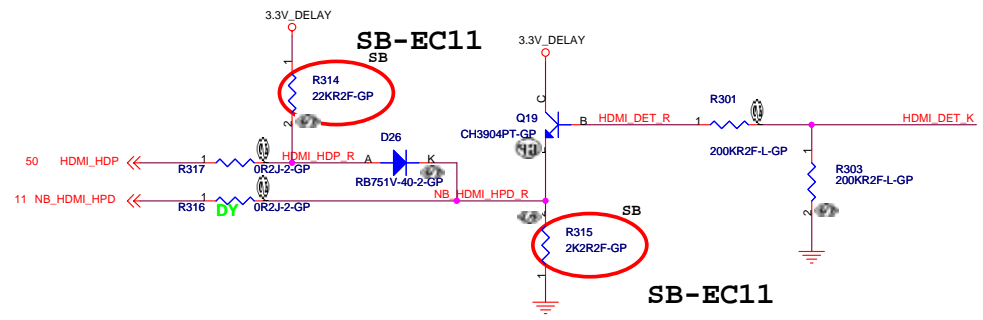
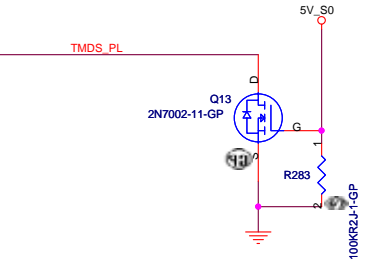
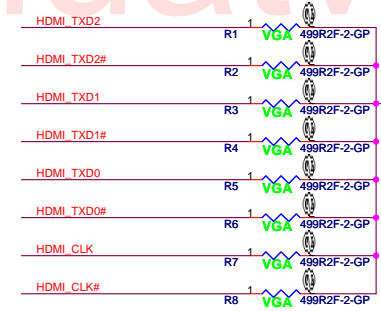
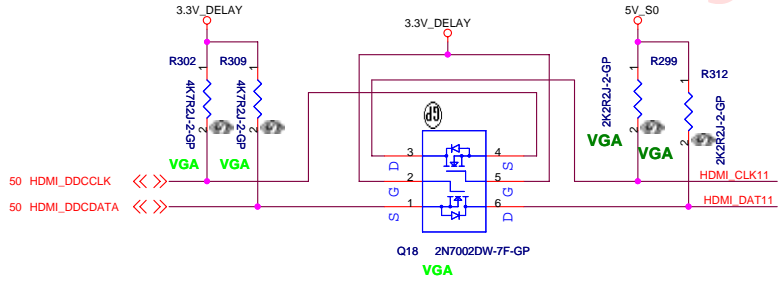
Size A3 Document Number **X17** Rev **SA**

Date: Tuesday, February 19, 2008 Sheet 16 of 56

EMI



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<Variant Name>

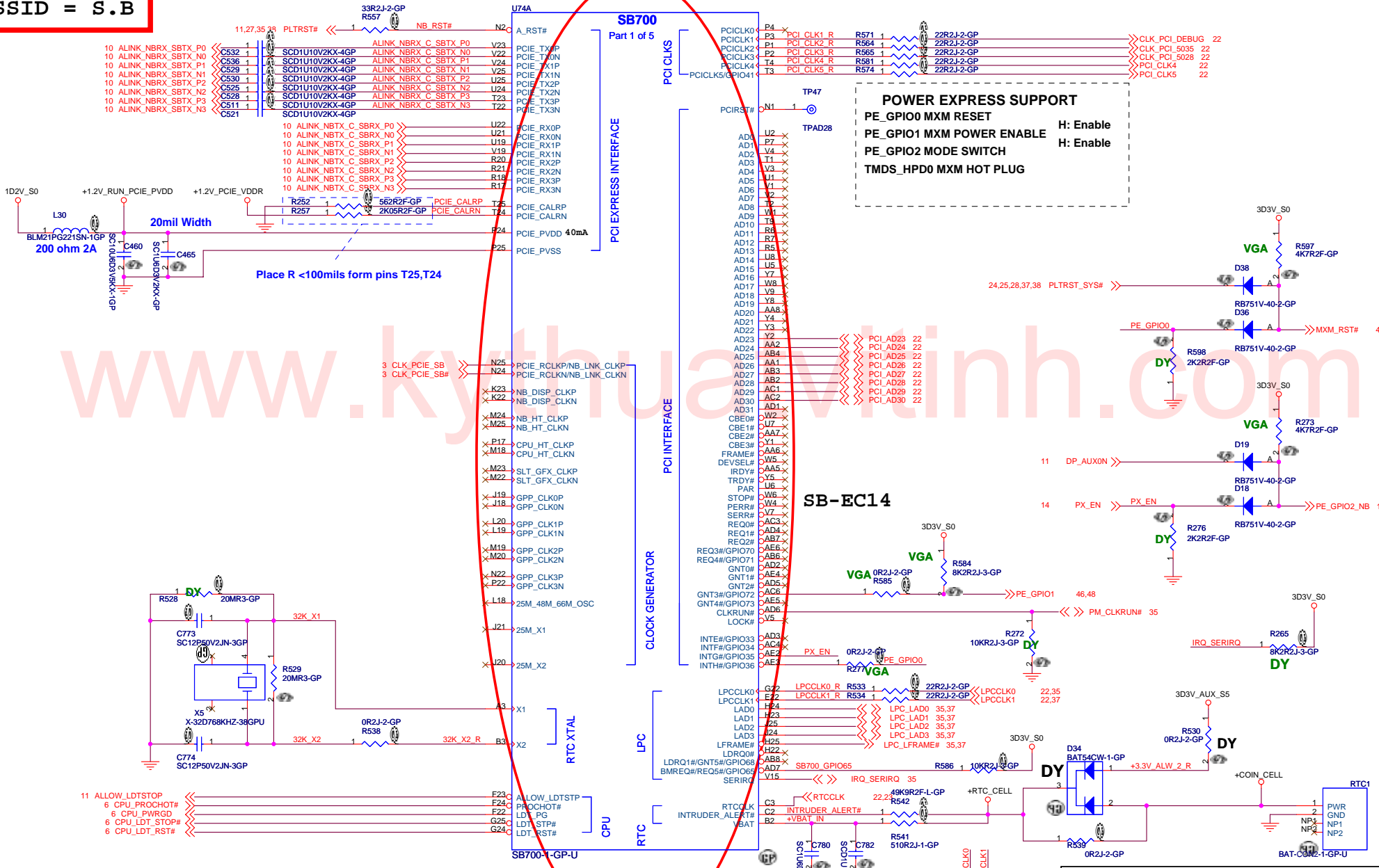
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DVI & HDMI CONN**

Size: A3 Document Number: **X17** Rev: **SA**

Date: Friday, February 15, 2008 Sheet 17 of 56

SSID = S.B

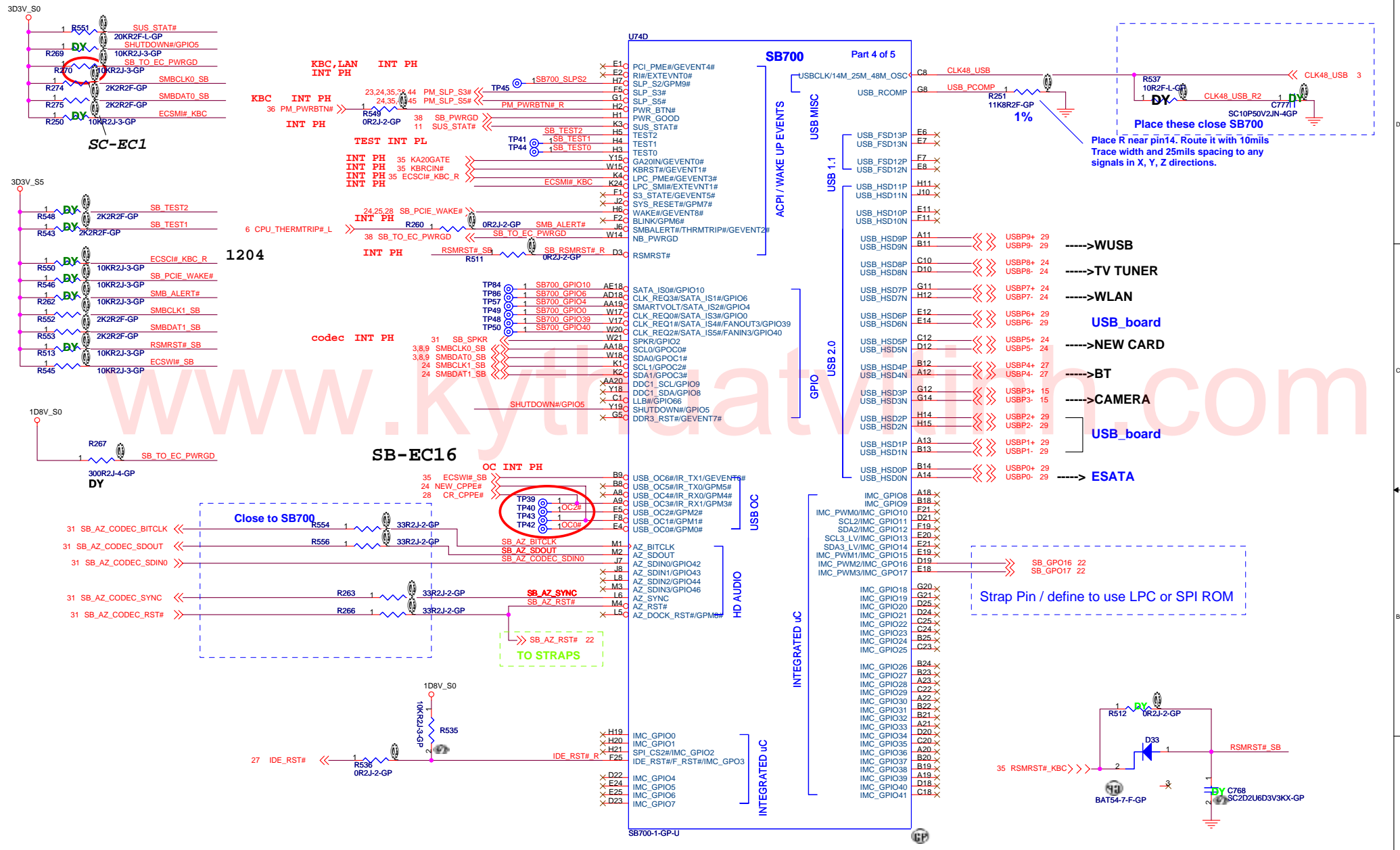


Symbol use (71.SB700.002)
 BOM use AMD SB700 (71.SB700.006)

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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ATI-SB700 PCIE&PCI (1/5)

File	Document Number			Rev
Size	X17			SA
Date:	Friday, February 15, 2008	Sheet	18	of 56

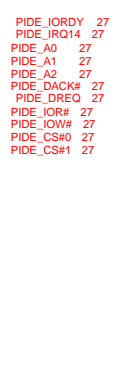
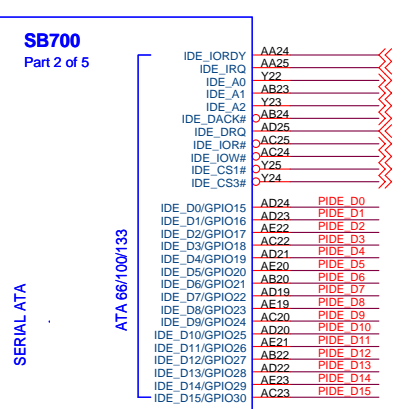
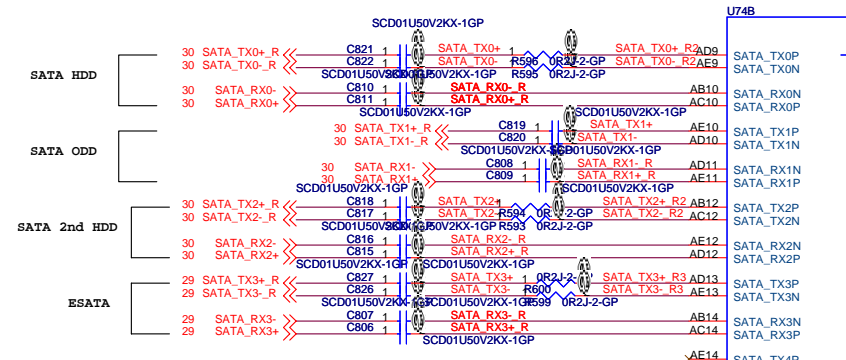


緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

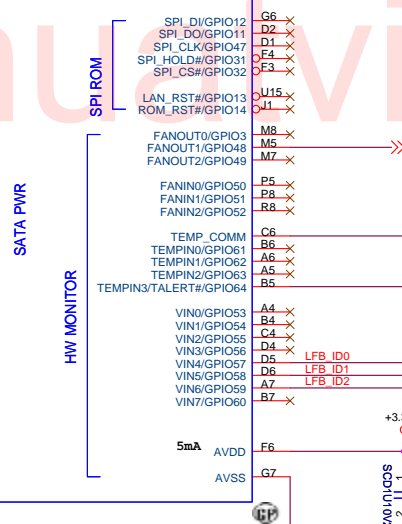
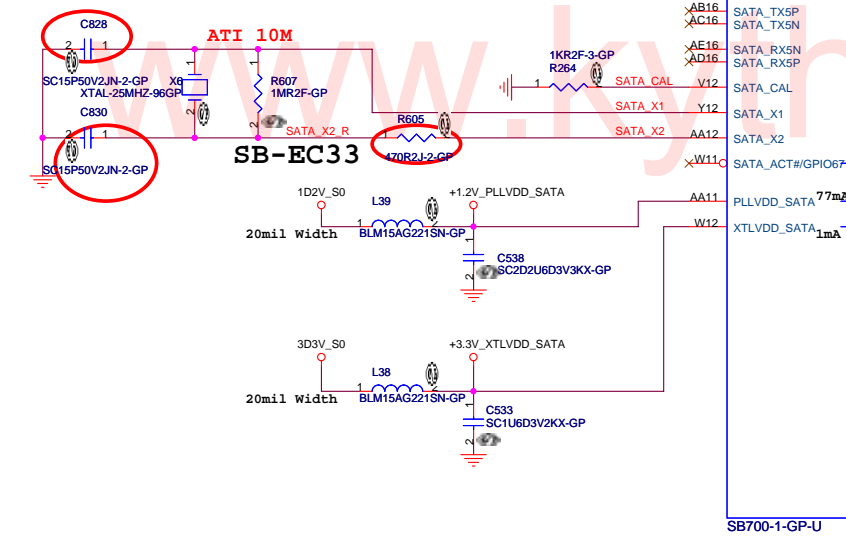
Title: **ATI-SB700 USB&GPIO (2/5)**

Size A3 Document Number **X17** Rev **SA**

Date: Tuesday, February 19, 2008 Sheet 19 of 56



SB-EC33

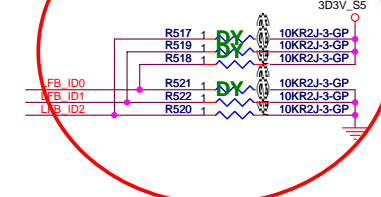


Local Frame Buffer Strapping List
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0
*Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

SB-EC64

LFB_ID0 to LFB_ID2 got internal PU to S5.



<Variant Name>

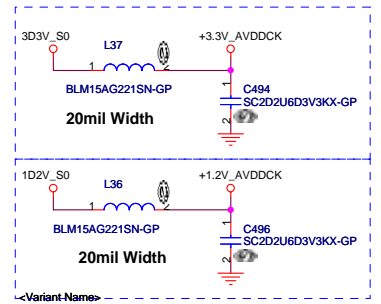
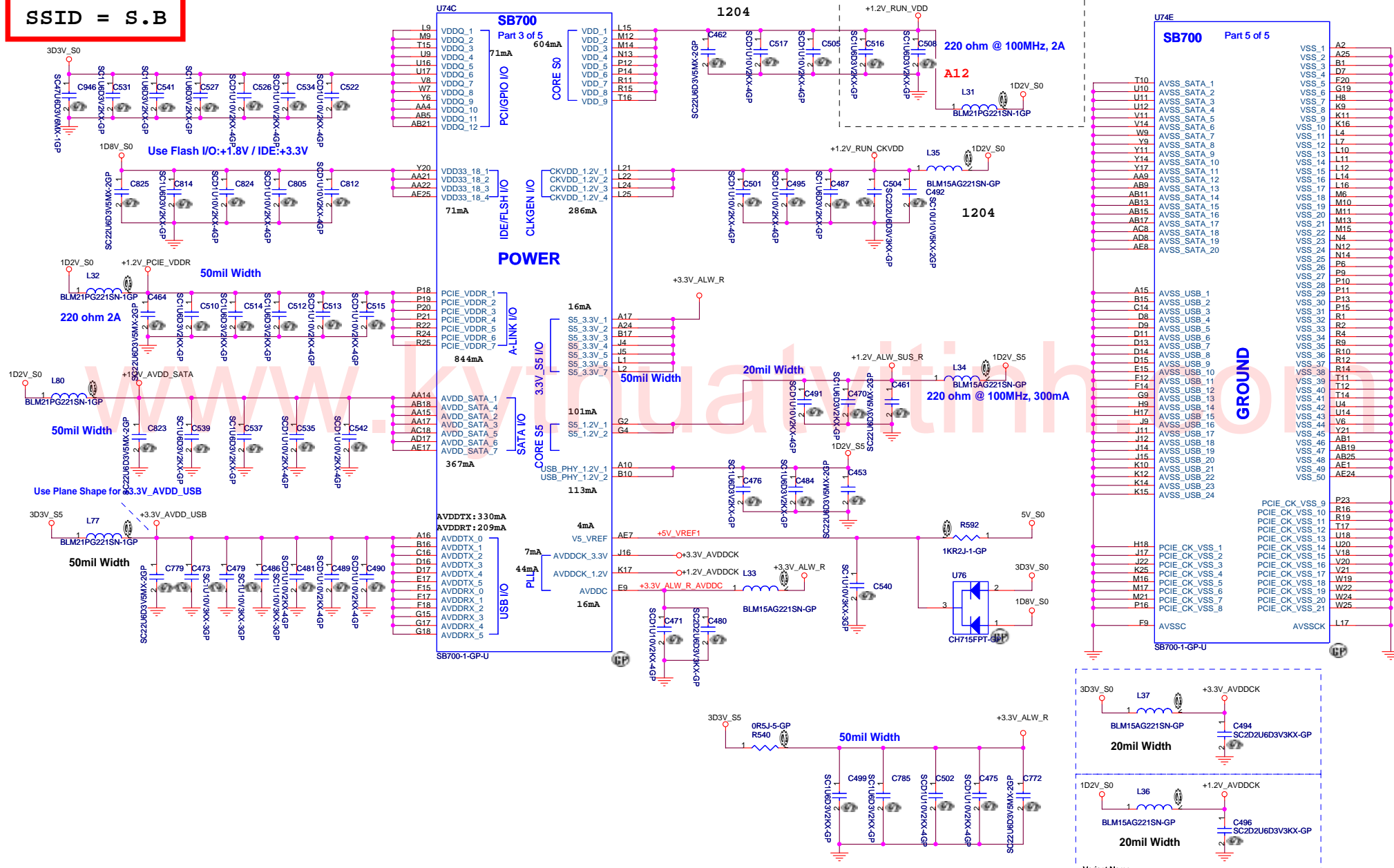
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title
ATI-SB700 SATA-IDE (3/5)

Size A3 Document Number **X17** Rev **SA**

Date: Tuesday, February 19, 2008 Sheet 20 of 56

SSID = S.B



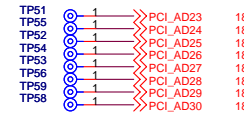
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB700 POWER&GND (4/5)**

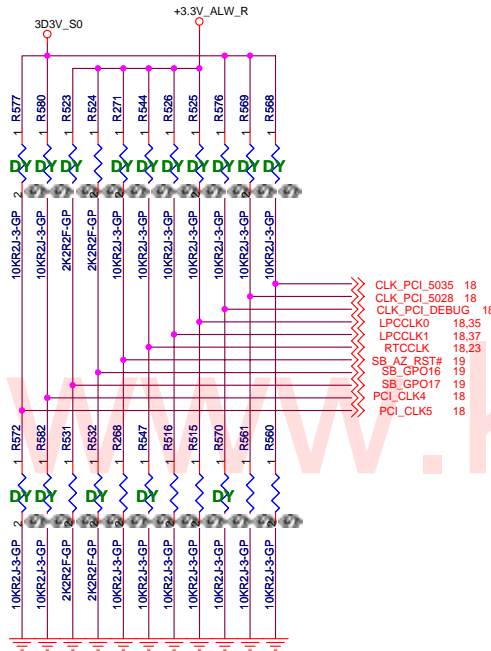
Size A3	Document Number	X17	Rev	SA
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SSID = S.B

DEBUG STRAPS



REQUIRED STRAPS



CLK_PCI_5035 18
 CLK_PCI_5028 18
 CLK_PCI_DEBUG 18
 LPCCLK0 18,35
 LPCCLK1 18,37
 RTCCCLK 18,23
 SB_AZ_RST# 19
 SB_GPO16 19
 SB_GPO17 19
 PCI_CLK4 18
 PCI_CLK5 18

REQUIRED SYSTEM STRAPS

	CLK_PCI_5035	CLK_PCI_5028	CLK_PCI_DEBUG	LPCCLK0	LPCCLK1	RTCCCLK	AZ_RST#	SB_GPO17, SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM
	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

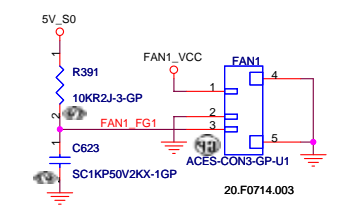
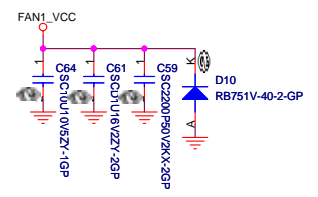
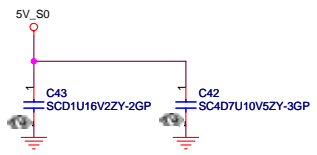
<Variant Name>

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Title
ATI-SB700 STRAPPING (5/5)

Size A3 Document Number **X17** Rev SA

Date: Tuesday, February 19, 2008 Sheet 22 of 56

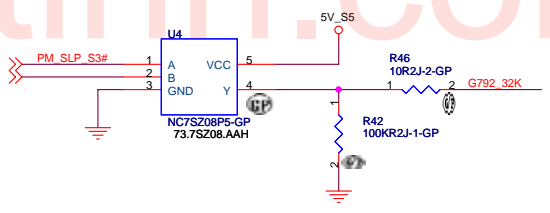
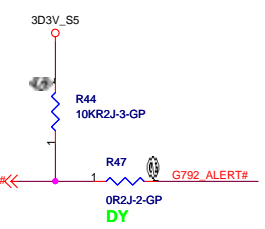
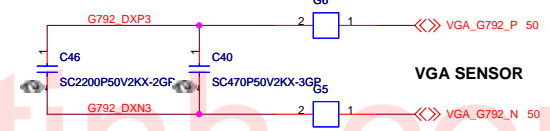
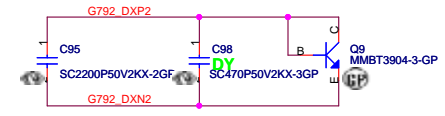
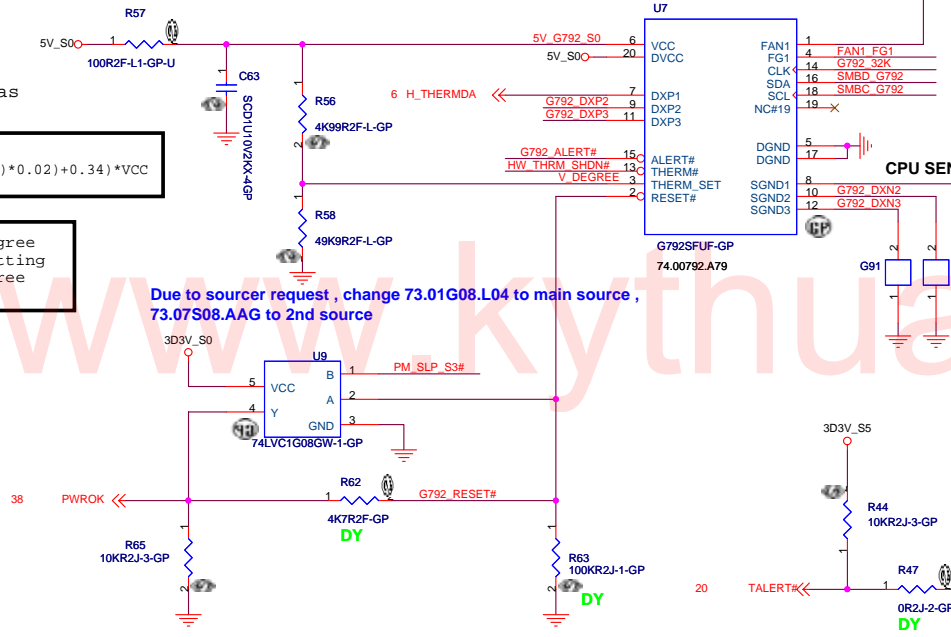


Setting T8 as 100 Degree

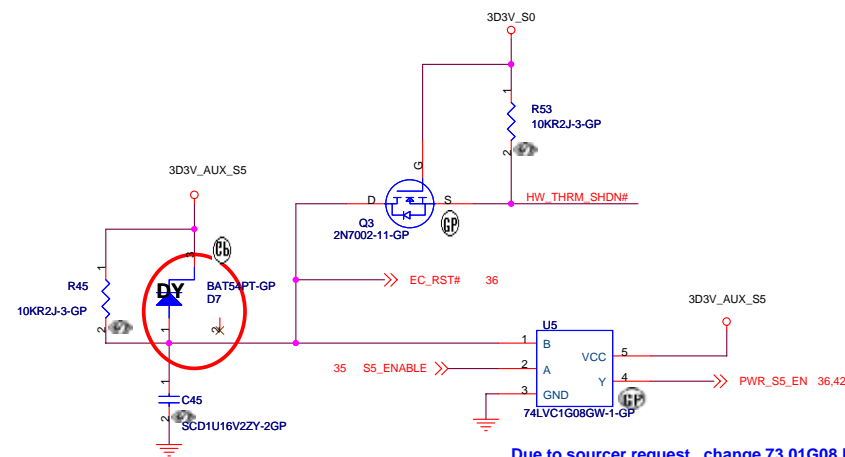
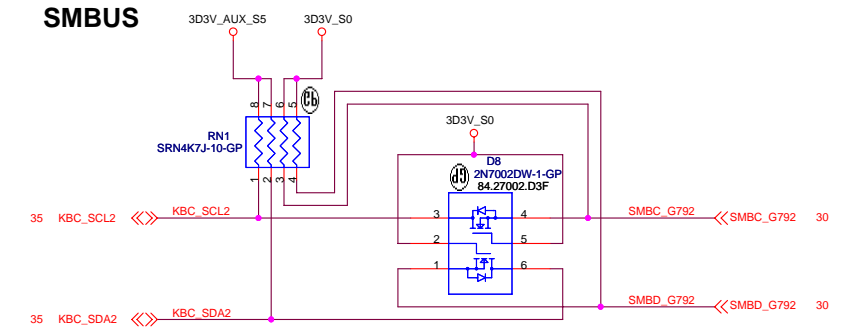
$$V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Due to sourcer request , change 73.01G08.L04 to main source , 73.07S08.AAG to 2nd source



SMBUS



Due to sourcer request , change 73.01G08.L04 to main source , 73.07S08.AAG to 2nd source

<Variant Name>

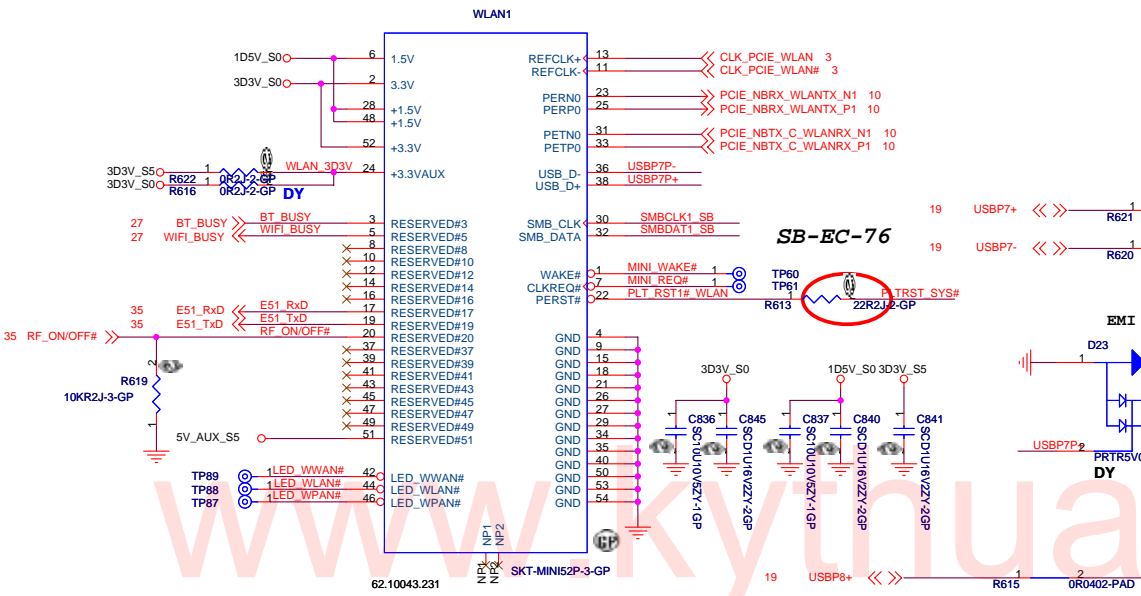
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL G792**

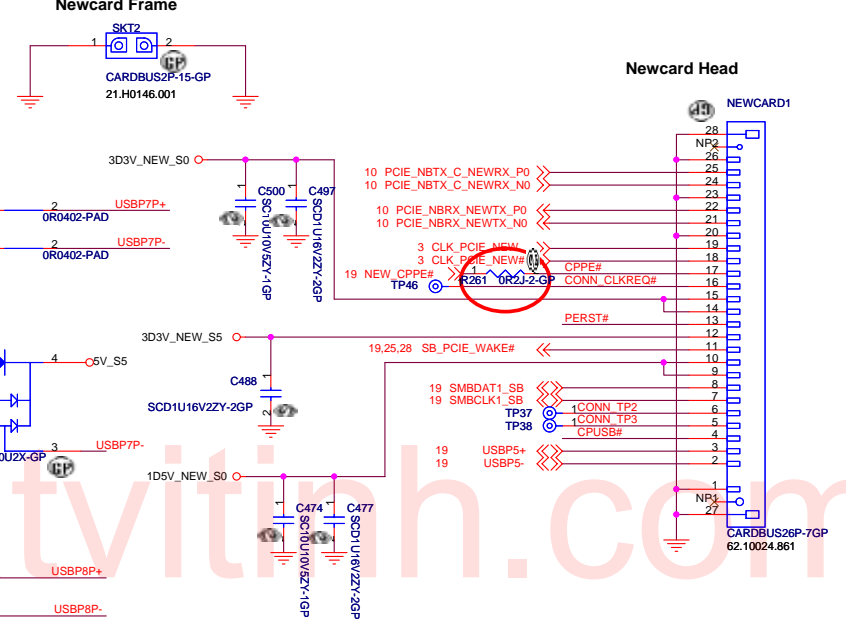
Size A3	Document Number	Rev SA
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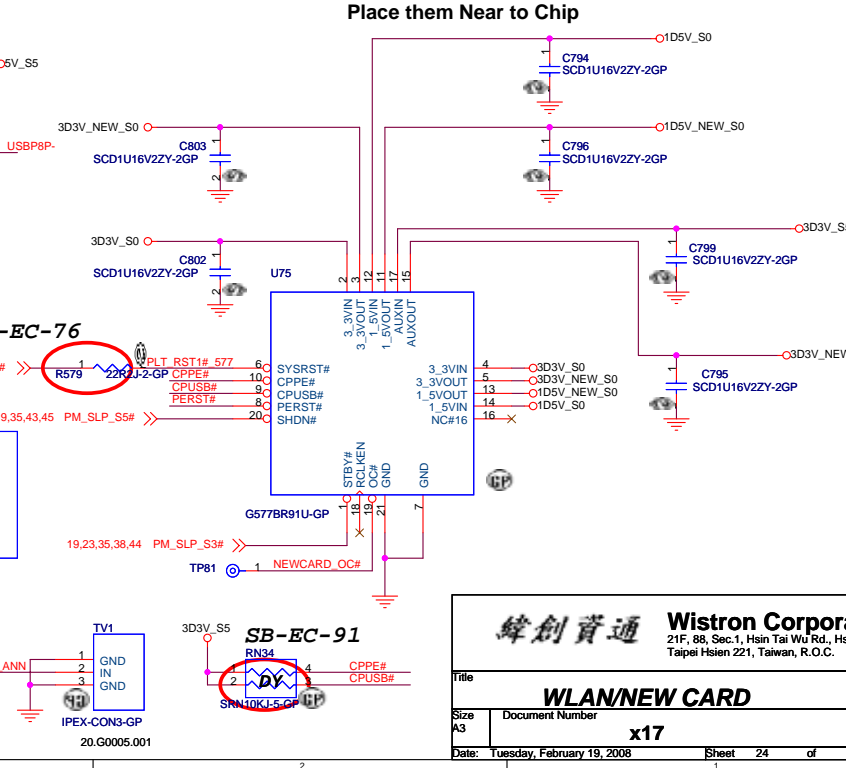
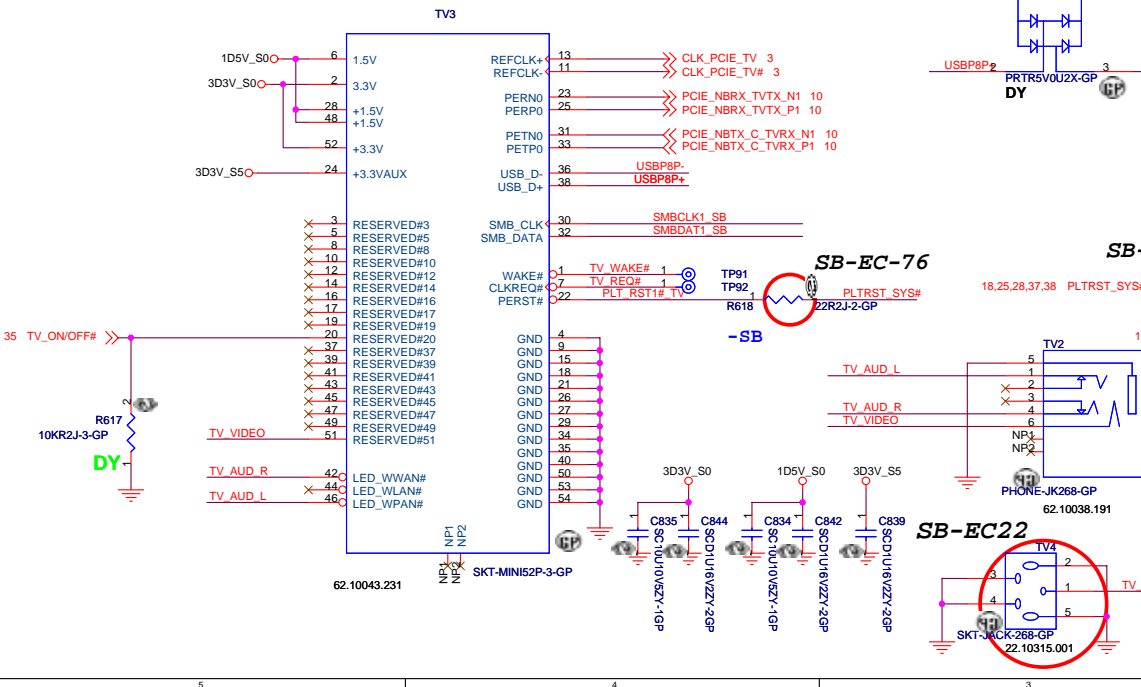
WLAN Connector



NEWCARD Connector



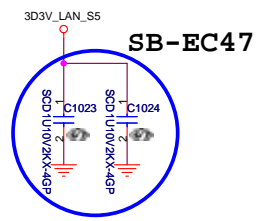
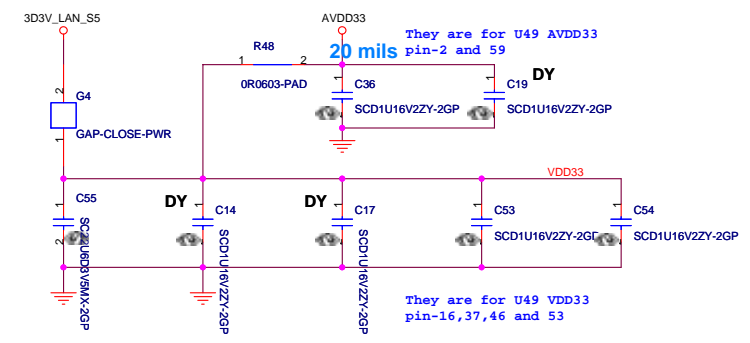
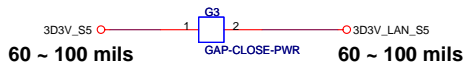
TV TUNER Connector



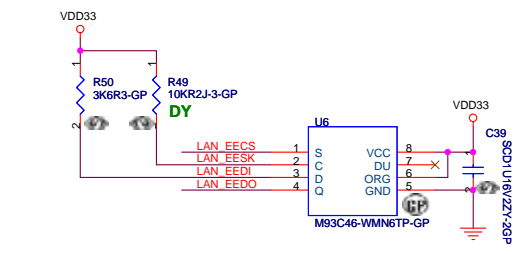
緯創資通 Wistron Corporation
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WLAN/NEW CARD

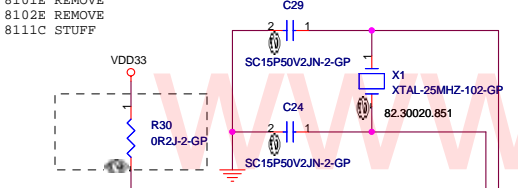
File	Document Number	Rev
Size	x17	SA
Date: Tuesday, February 19, 2008	Sheet 24	of 56



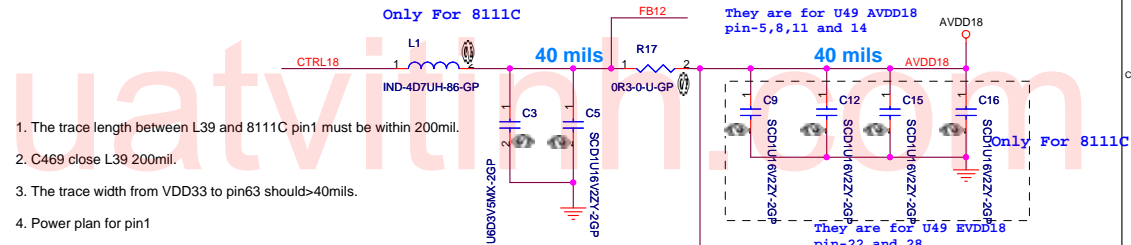
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)



8101E REMOVE
8102E REMOVE
8111C STUFF



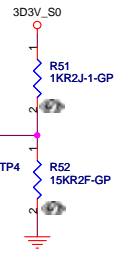
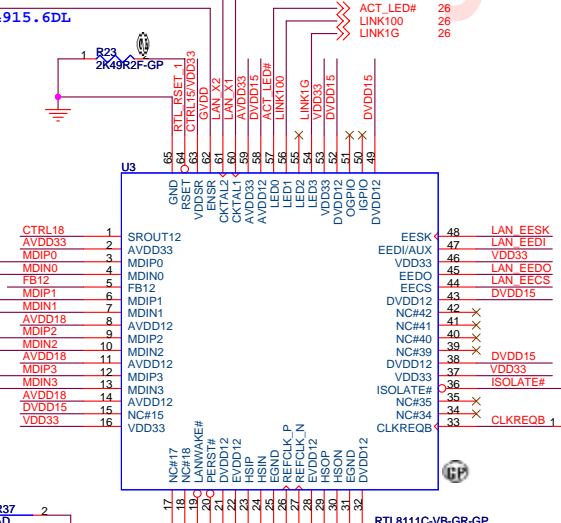
8111C/8102E 2.49K 64.24915.6DL
8101E 2K 64.20015.6DL



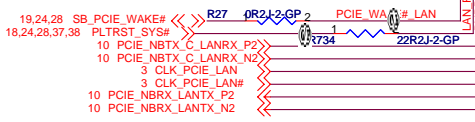
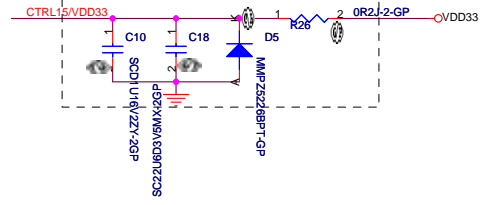
1. The trace length between L39 and 8111C pin1 must be within 200mil.
2. C469 close L39 200mil.
3. The trace width from VDD33 to pin63 should >40mils.
4. Power plan for pin1

Power plan for pin1

26	MDIP0	CTRL18	1
26	MDIP0	AVDD33	2
26	MDIN0	MDIP0	3
26	MDIP1	MDIN0	4
26	MDIN1	MDIP1	5
26	MDIN1	MDIN1	6
26	MDIP2	AVDD18	7
26	MDIN2	MDIP2	8
26	MDIN2	MDIN2	9
26	MDIP3	AVDD18	10
26	MDIN3	MDIP3	11
26	MDIN3	MDIN3	12
26	MDIP3	AVDD18	13
26	MDIN3	MDIP3	14
26	MDIN3	MDIN3	15
26	MDIN3	VDD33	16



1. Pin1 should be near inductor (4.7u H,L39) then 22u F(C469) then 0.1u F(C470).
2. Pin 63 should be near 0.1u F(C493) then 22u F(C494).
3. C471,C472,C473, and C474 as close as possible to RTL8111C



19,24,28 SB_PCIE_WAKE#
18,24,28,37,38 PLTRST_SYSP
10 PCIE_NBTX_C_LANRX_P2
10 PCIE_NBTX_C_LANRX_N2
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
10 PCIE_NBRX_LANTX_P2
10 PCIE_NBRX_LANTX_N2

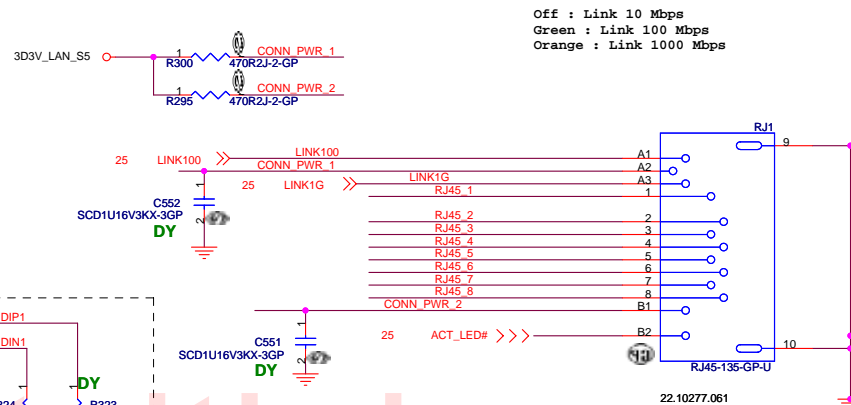
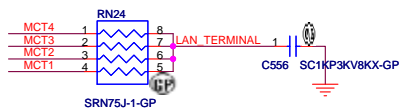
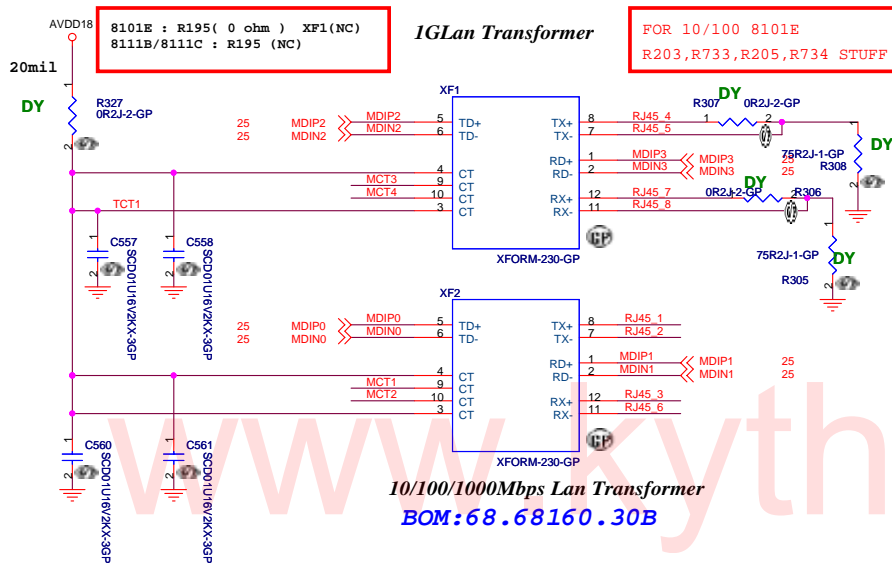
<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

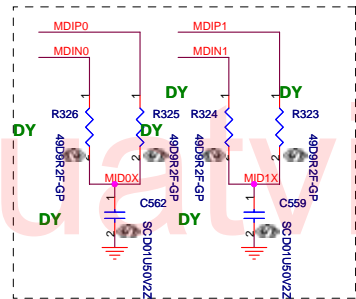
Title: **LAN 8111C/8101E**

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Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps



Green : Link up
Blinking : TX/RX activity

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

<Variant Name>

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Title

LAN Connector

Size

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Rev

SA

Date: Monday, February 18, 2008

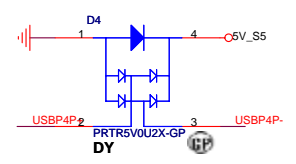
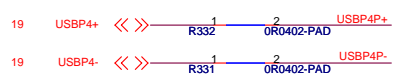
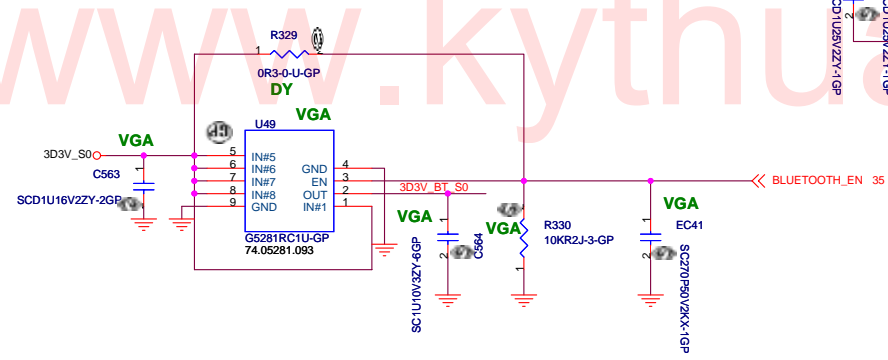
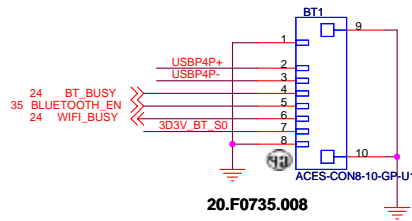
Sheet 26

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56

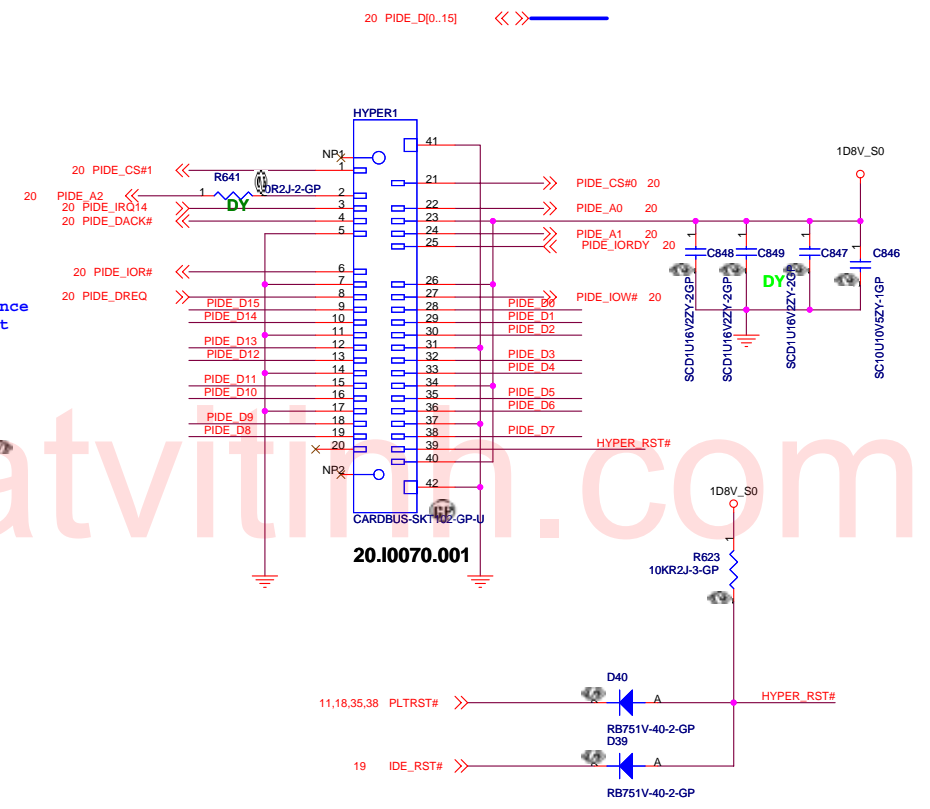
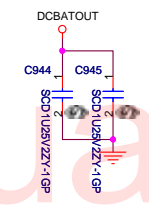
HYPER FLASH

Bluetooth



EMI

For HF reference
different moat



<Variant Name>

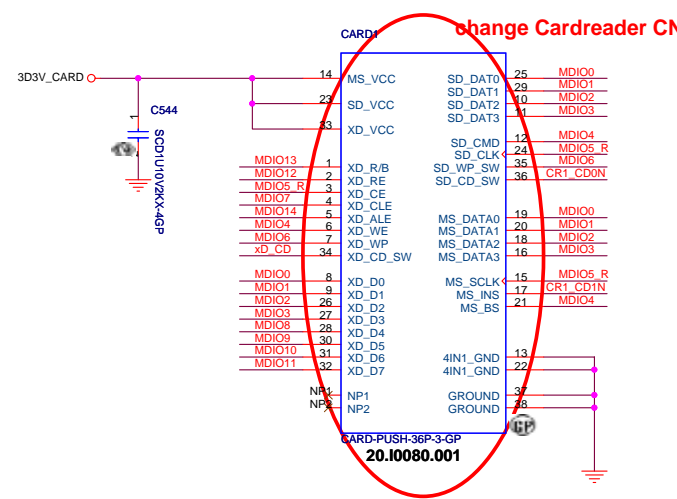
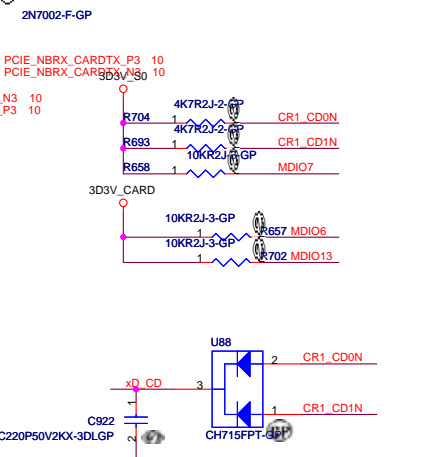
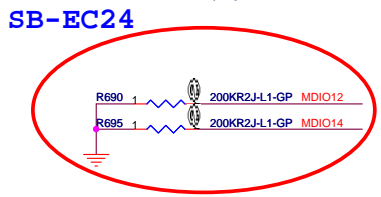
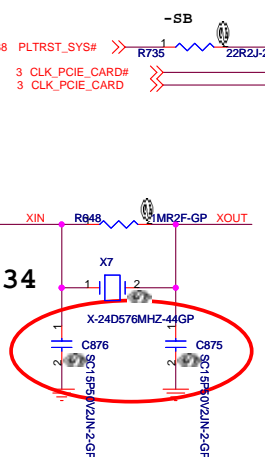
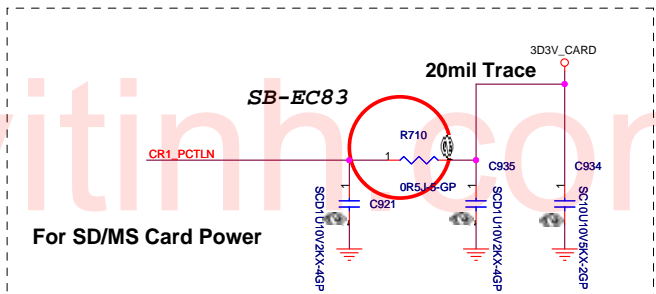
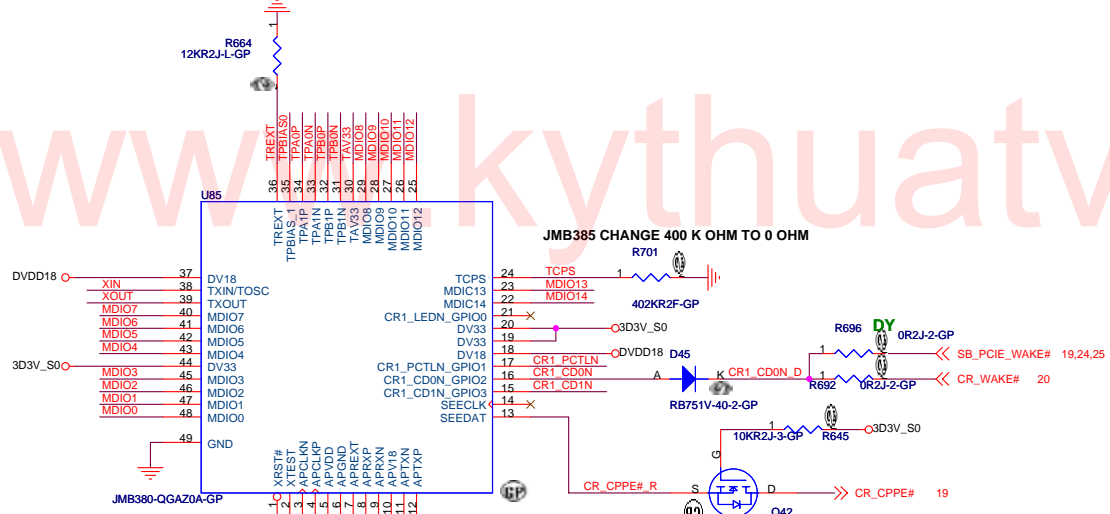
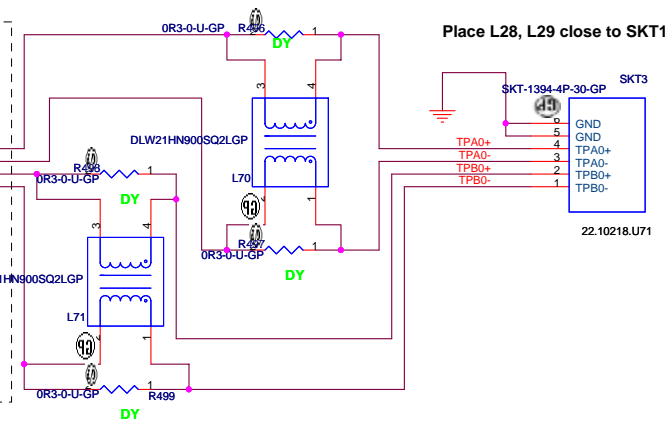
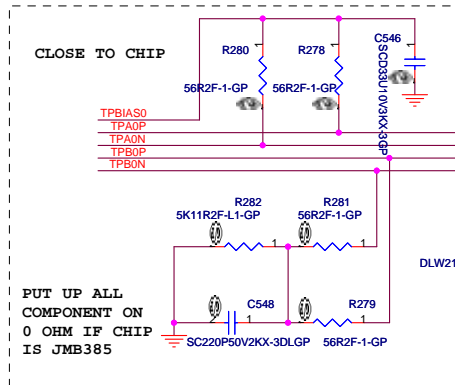
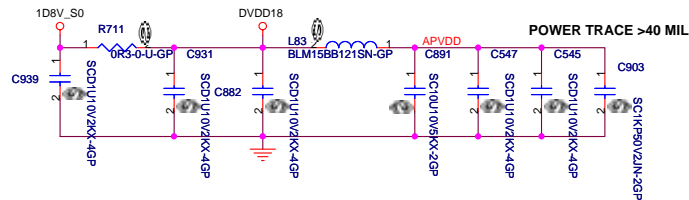
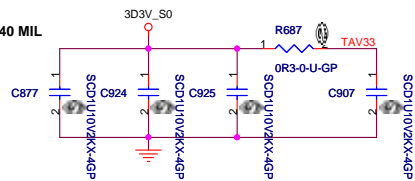
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Title
HYPER FLASH/BT

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POWER TRACE >40 MIL



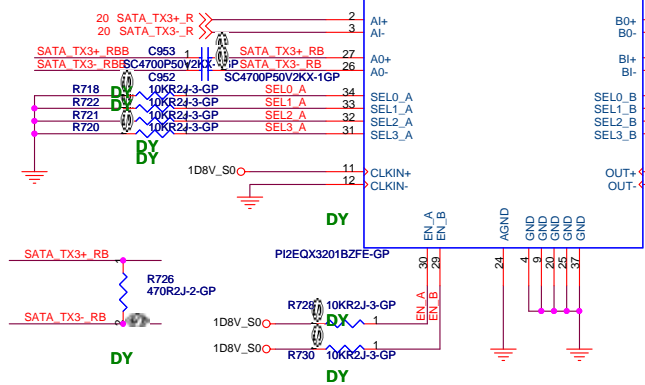
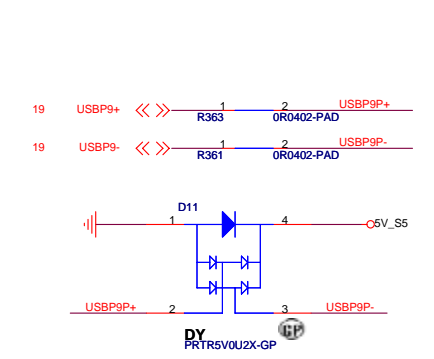
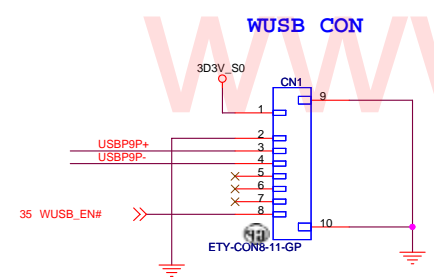
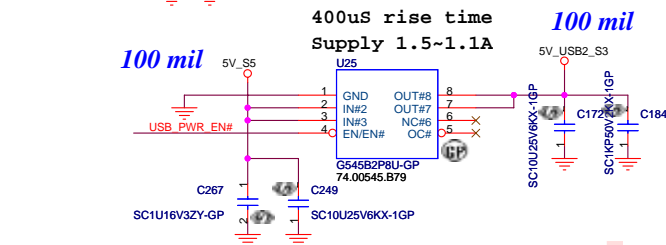
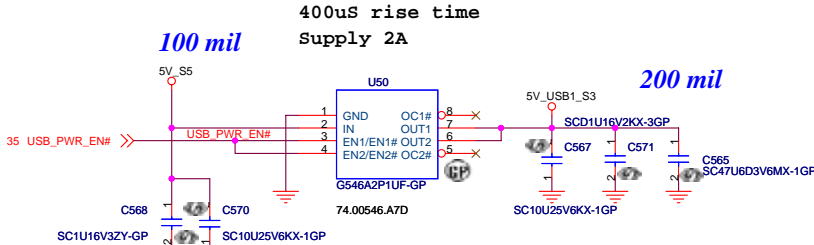
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

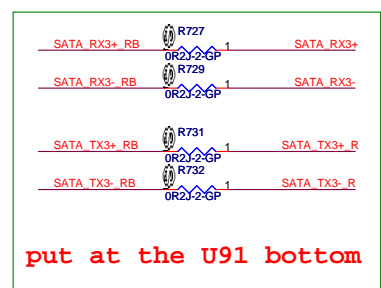
Title: **1394/CARD READER**

Size: A3 Document Number: **X17** Rev: SA

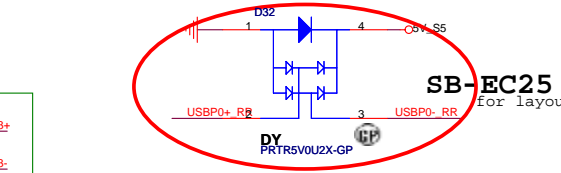
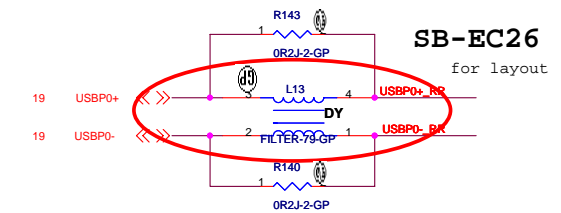
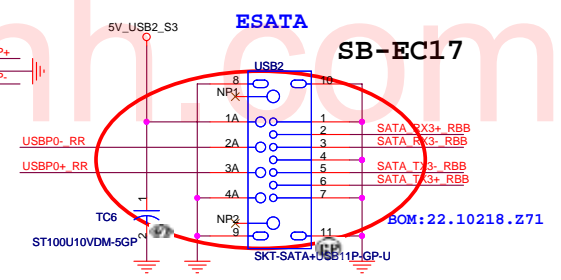
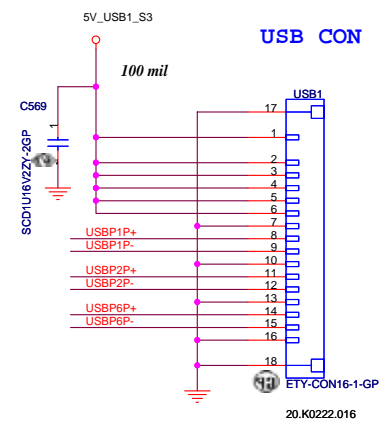
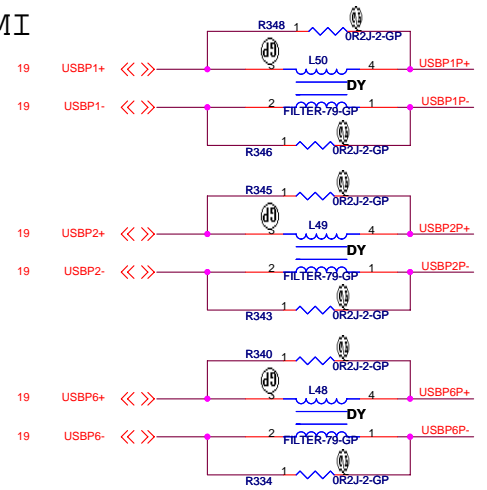
Date: Friday, February 15, 2008 Sheet 28 of 56



put close to connector



EMI



<Variant Name>

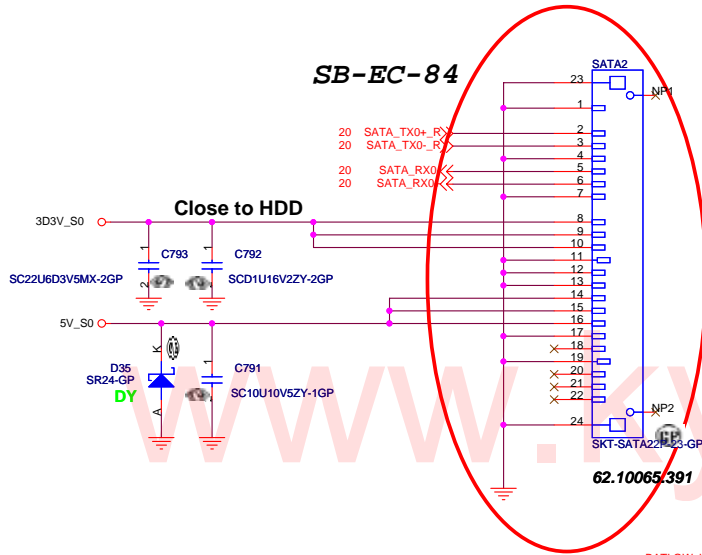
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/ESATA CONN**

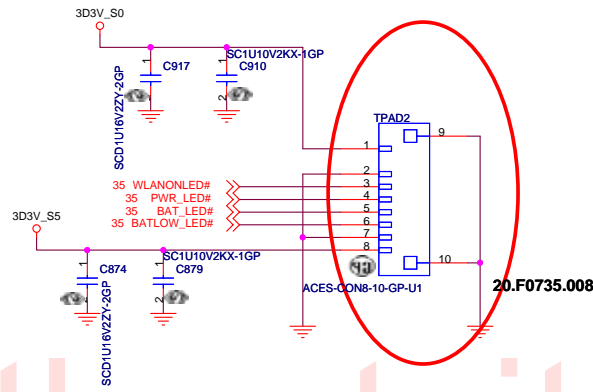
Size A3 Document Number: **X17** Rev: **SA**

Date: Friday, February 15, 2008 Sheet 29 of 56

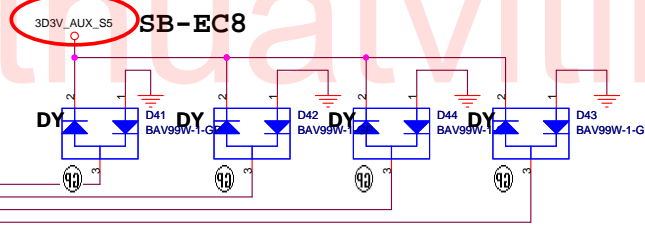
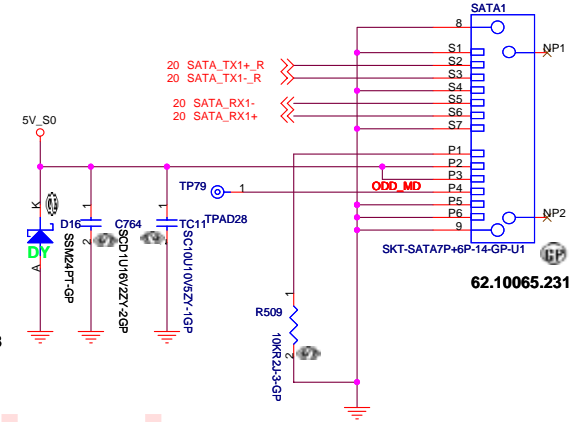
SATA HDD Connector



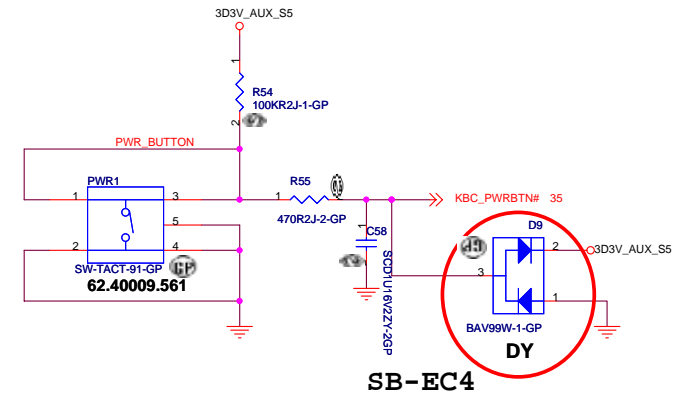
LED BD CONN



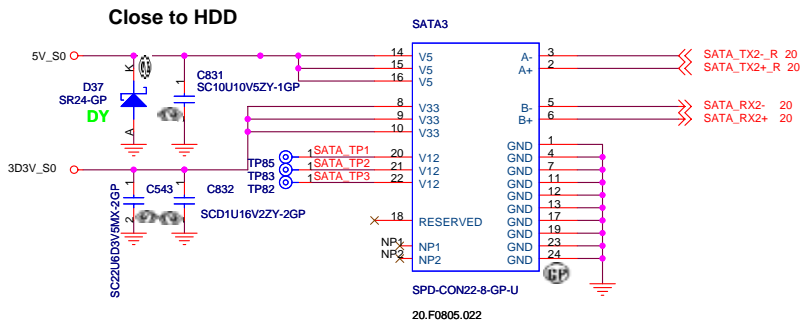
SATA ODD Connector



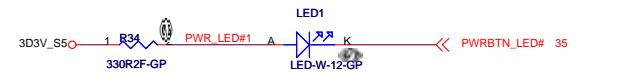
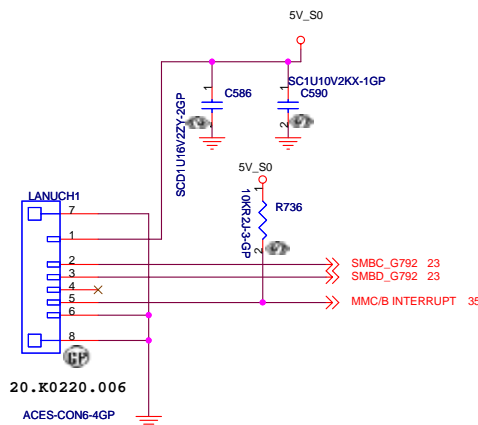
POWER BUTTON



SATA HDD2 Connector



MMC BD CONN

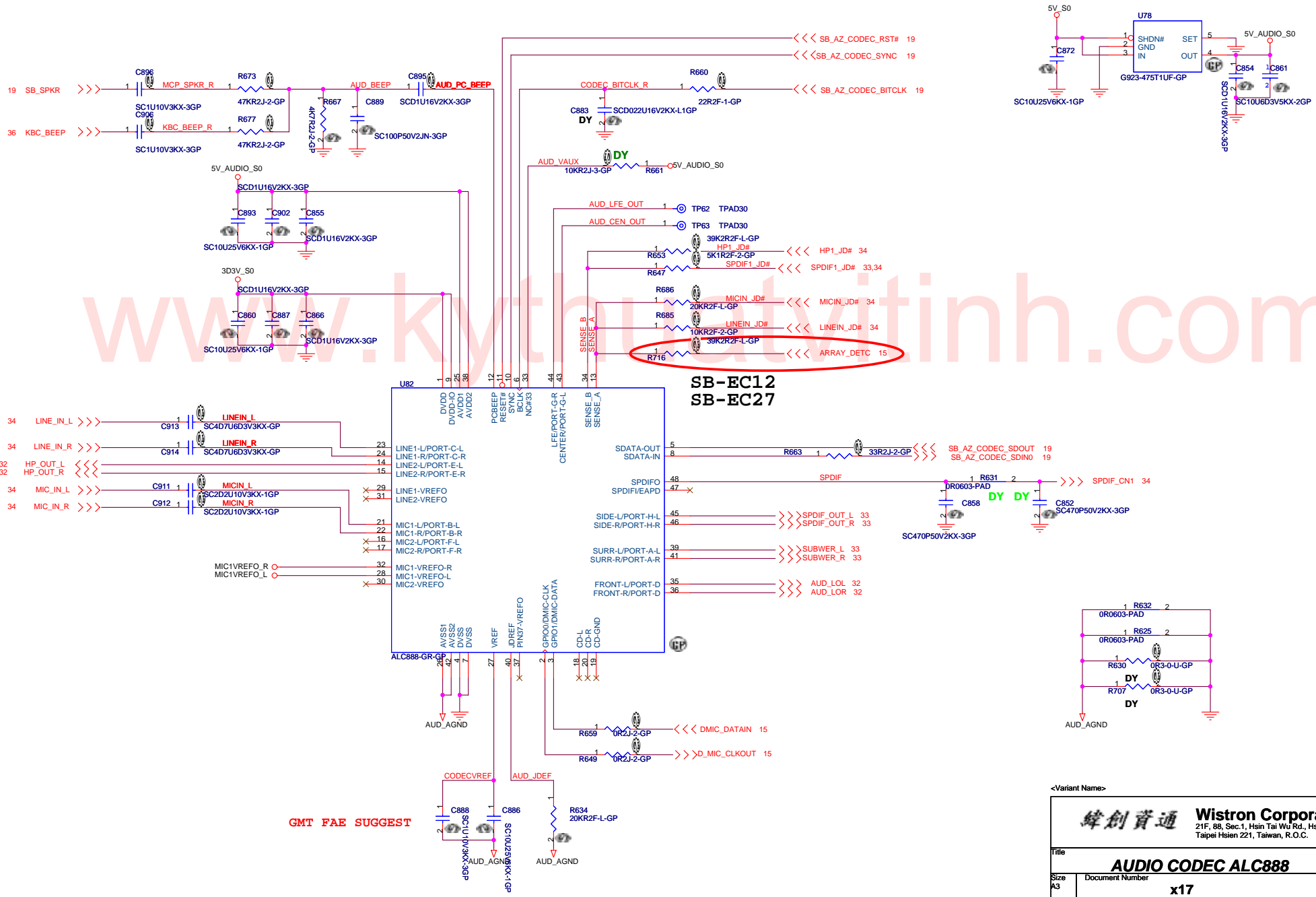


Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **HDD/CDROM/LED/LAUNCH**

Size: A3 Document Number: **X17** Rev: **SA**

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GMT FAE SUGGEST

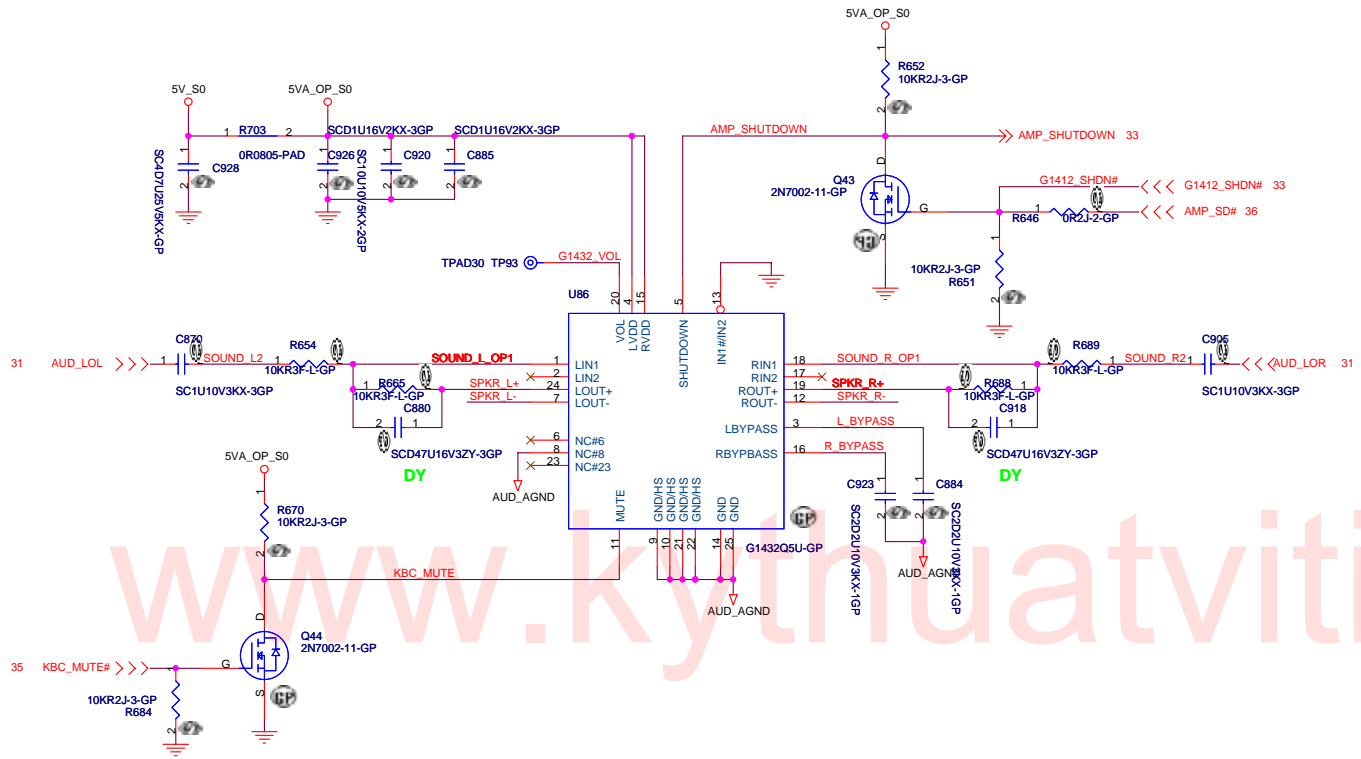
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC ALC888**

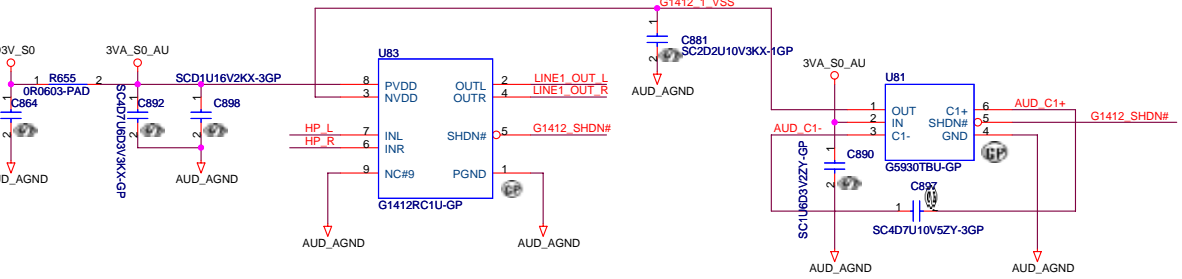
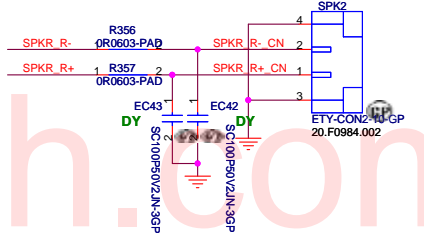
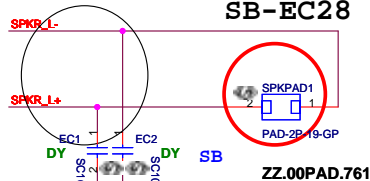
Size A3	Document Number	x17	Rev SA
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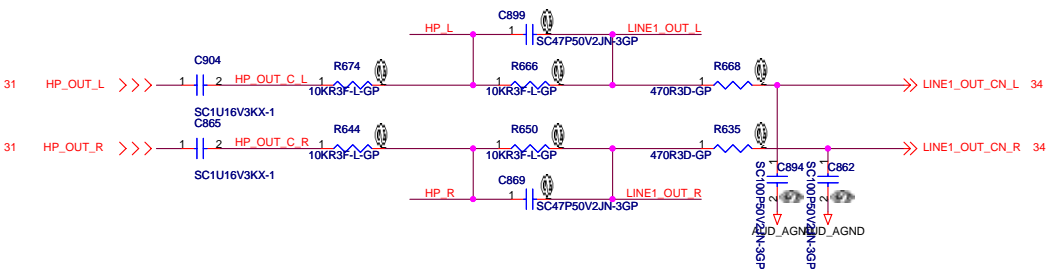


Internal Speaker

SB-EC74



LINE Out



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

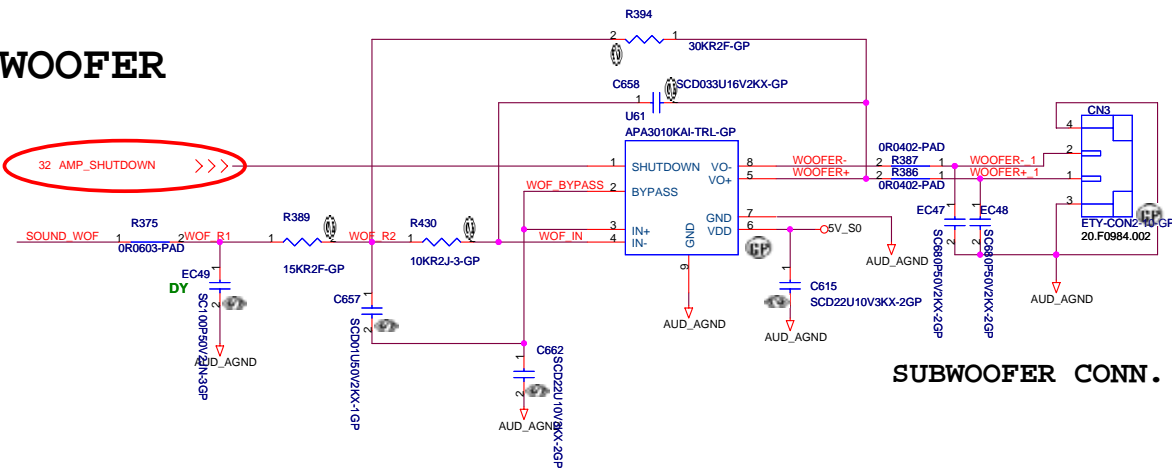
Title: **AUDIO AMP/Speaker**

Size: A3	Document Number: X17	Rev: SA
Date: Tuesday, February 19, 2008	Sheet: 32	of: 56

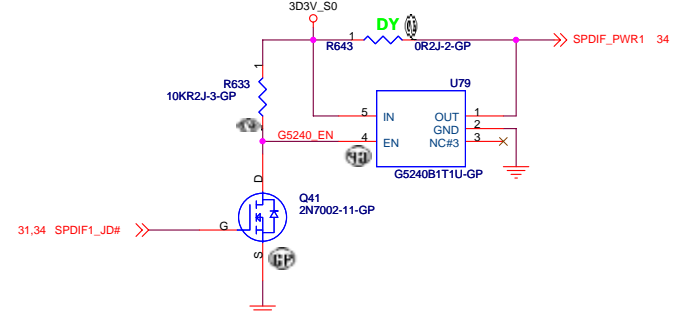
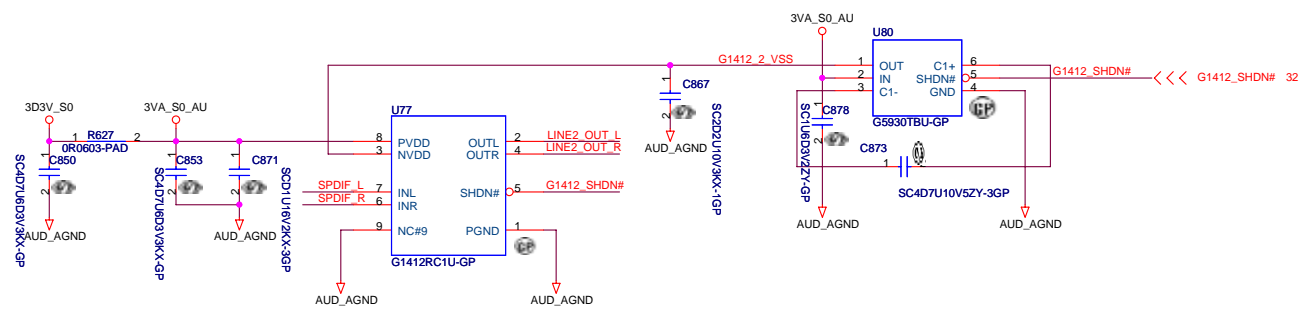
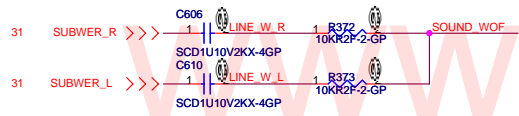
SUBWOOFER

SB-EC10

32 AMP_SHUTDOWN >>>



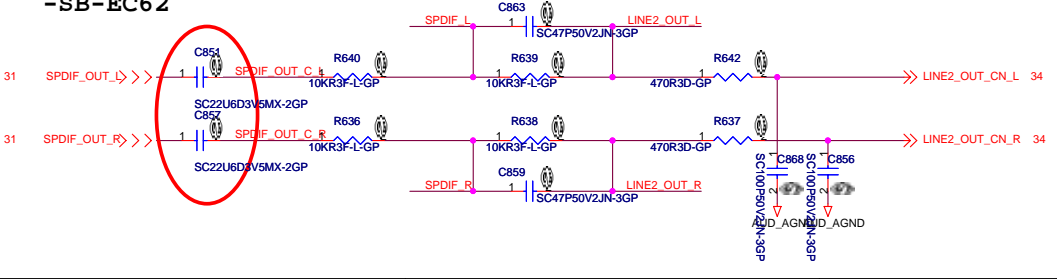
SUBWOOFER CONN.

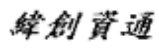


LINE2 Out

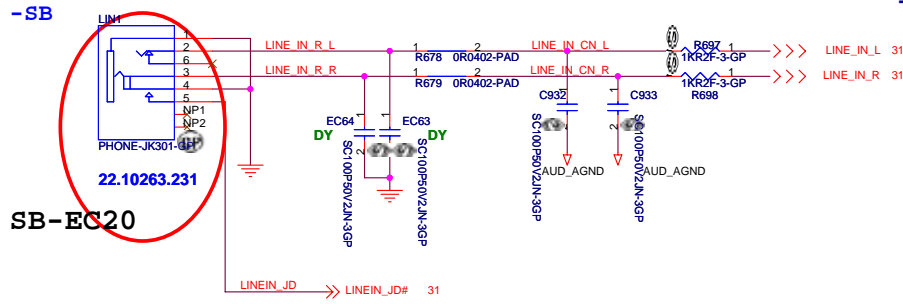
-SB-EC62

32 AMP_SHUTDOWN >>>

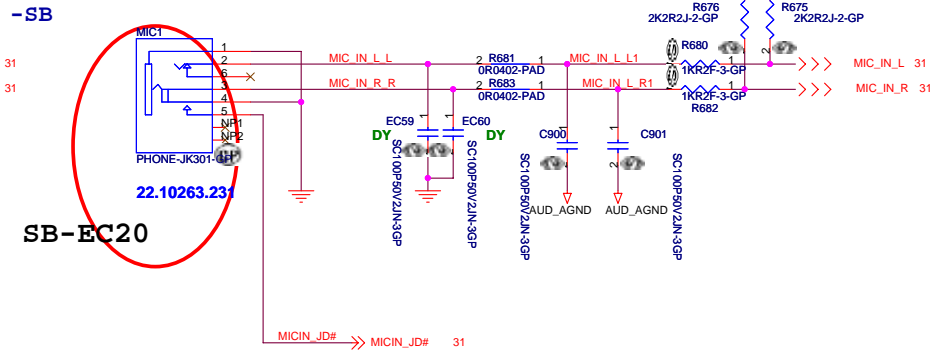


 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title AUDIO AMP/Subwoofer		
Size A3	Document Number X17	Rev SA
Date: Tuesday, February 19, 2008	Sheet 33	of 56

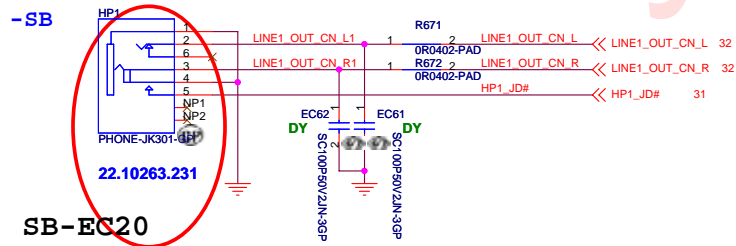
LINE In



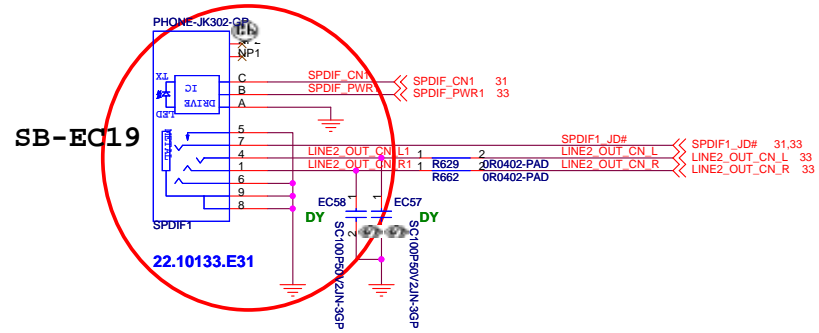
MIC In




Headphone / LINE1 OUT

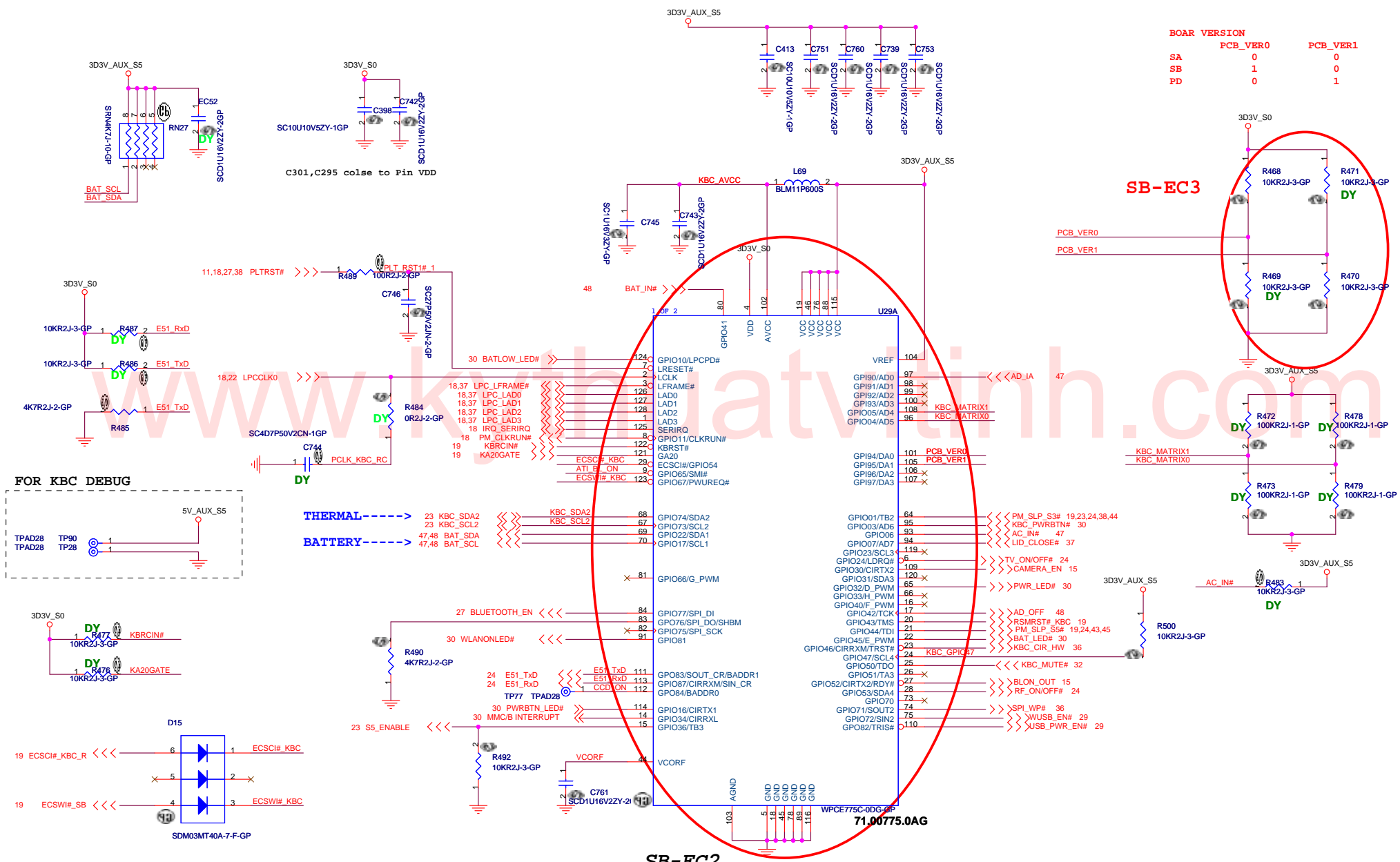


SPDIF OUT / LINE2 OUT



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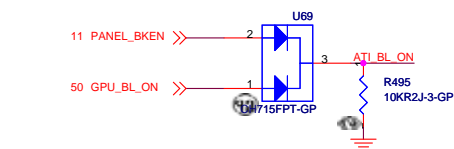
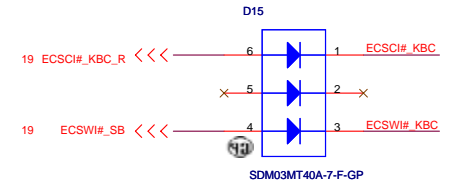
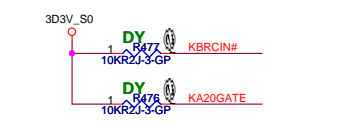
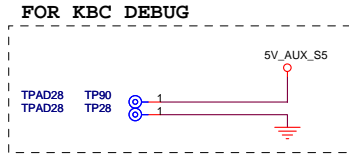
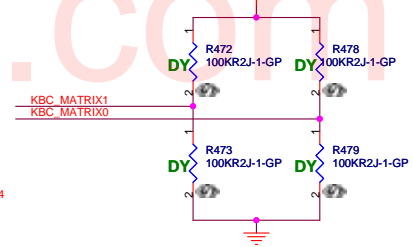
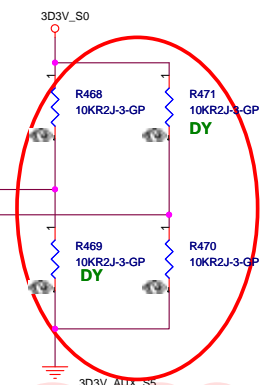
<Variant Name>	
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AUDIO CONN/SUBWOOFER	
Size A3	Document Number X17
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BOARD VERSION

	PCB_VER0	PCB_VER1
SA	0	0
SB	1	0
PD	0	1

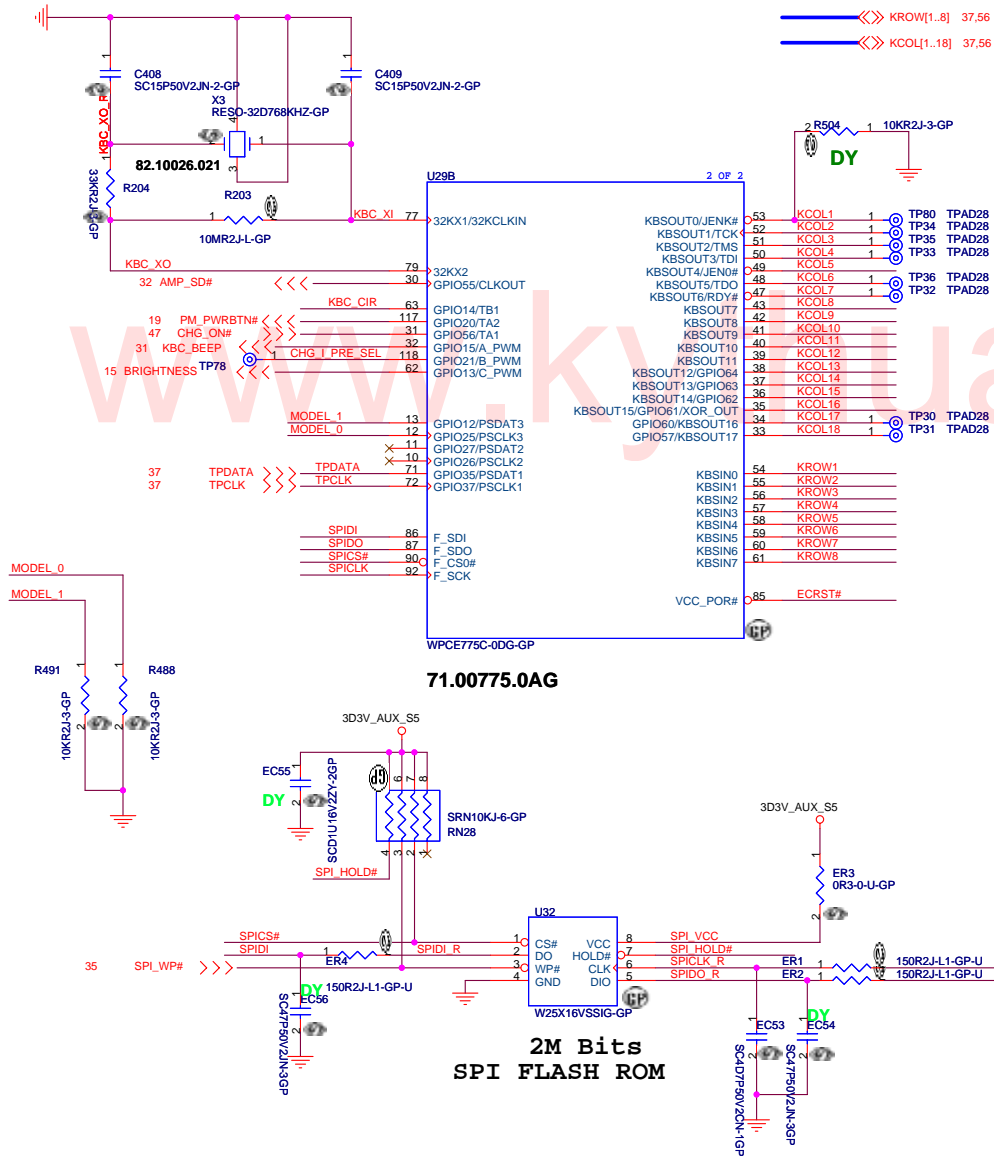
SB-EC3



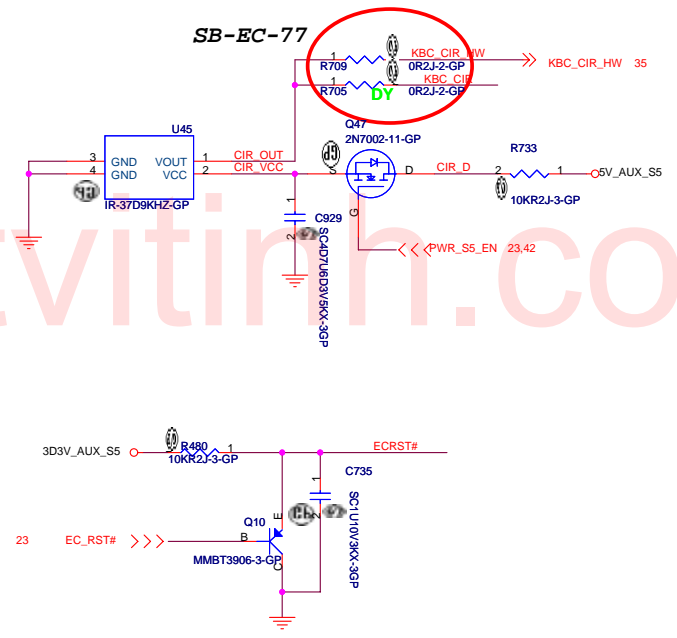
THERMAL-----> 23 KBC_SDA2
 23 KBC_SCL2
BATTERY-----> 47,48 BAT_SDA
 47,48 BAT_SCL

SB-EC2

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
KBC WPC775 / BIOS			
Size	Document Number		Rev
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CIR



<Variant Name>

緯創資通 Wistron Corporation
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Title: **KBC WPC775 / BIOS(2/2)**

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	X17	

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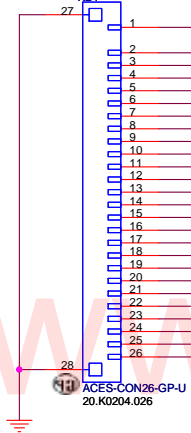
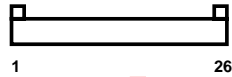
Internal KeyBoard Connector

— << KROW[1..8] 36.56
— << KCOL[1..18] 36.56

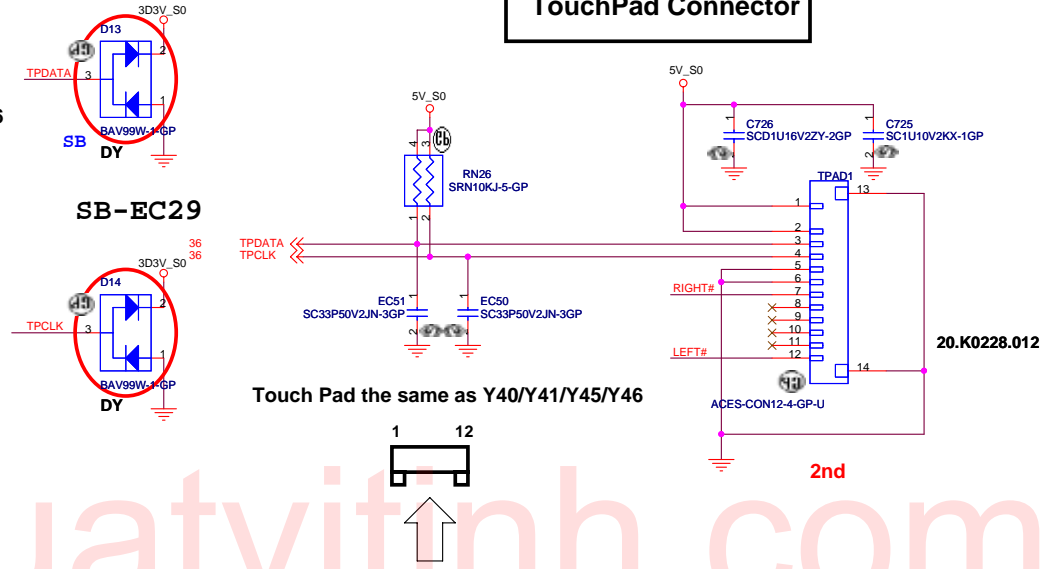
KEYBOARD MARTIX the same as Y40/Y41/Y45/Y46

Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



TouchPad Connector

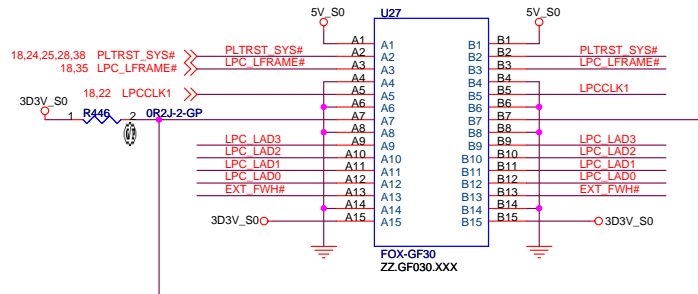


Touch Pad the same as Y40/Y41/Y45/Y46

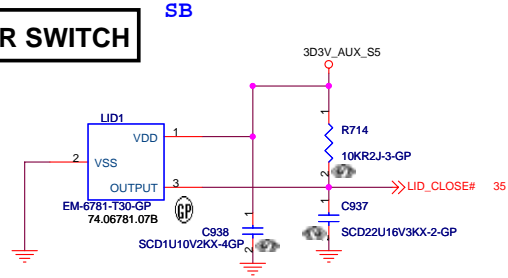
20.K0228.012

2nd

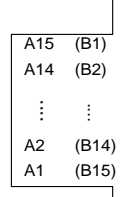
GOLDEN FINGER FOR DEBUG BOARD



COVER SWITCH

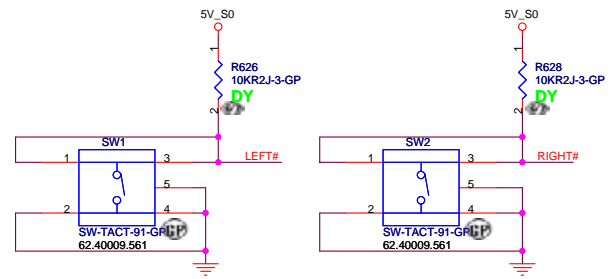


TOP VIEW



(BOTTOM VIEW)

17" TOUCHPAD BUTTON SWITCH

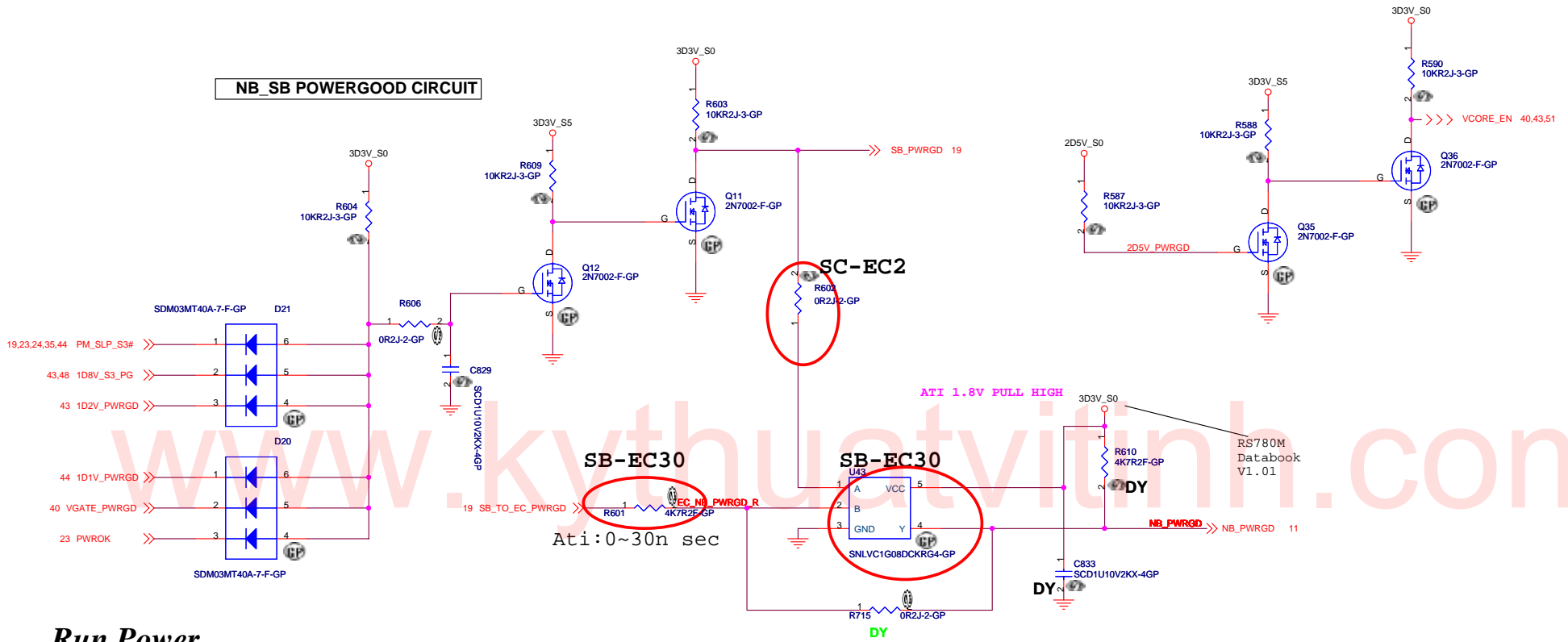


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

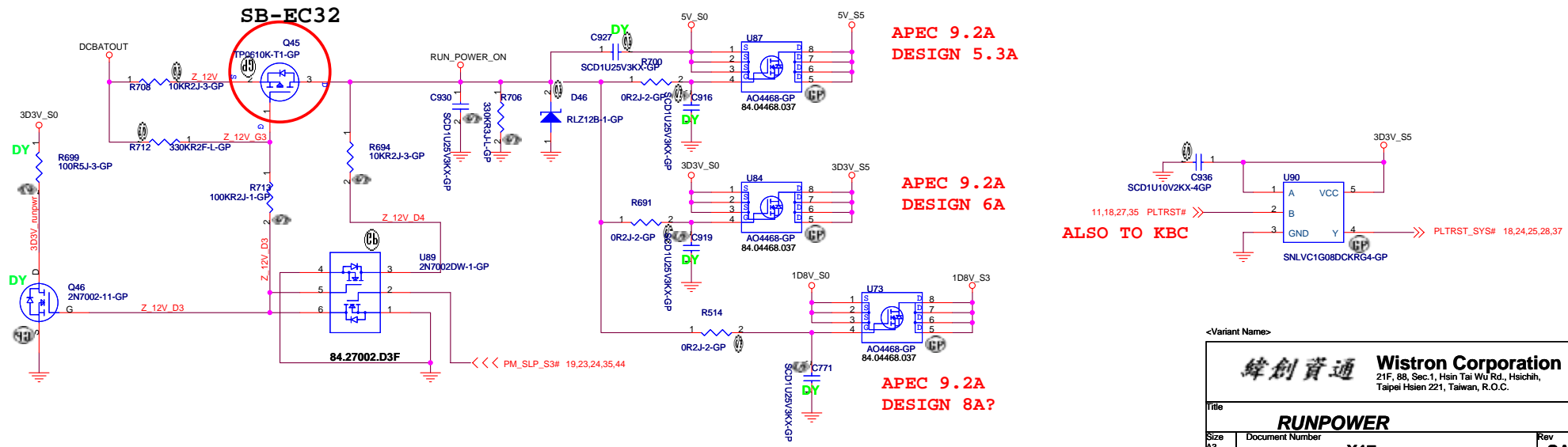
Title			KEYBOARD/TPAD/DEBUG/LID		
Size	Document Number		Rev		
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NB_SB POWERGOOD CIRCUIT



Run Power



<Variant Name>

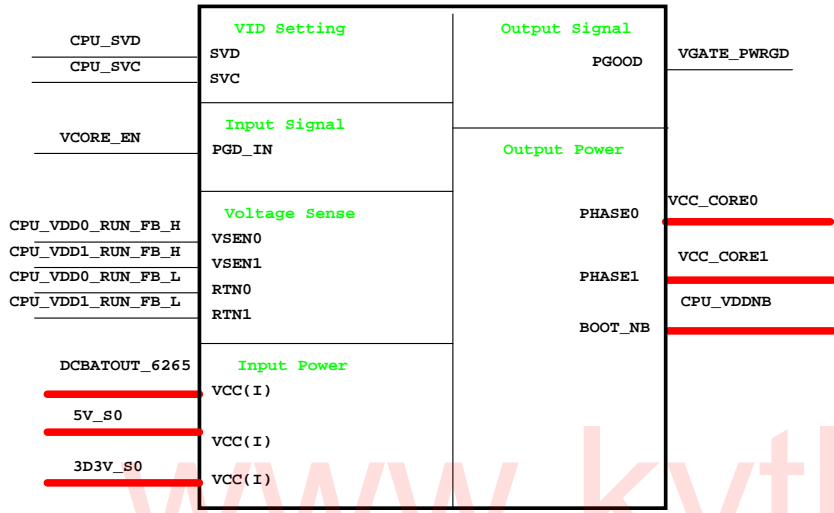
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUNPOWER**

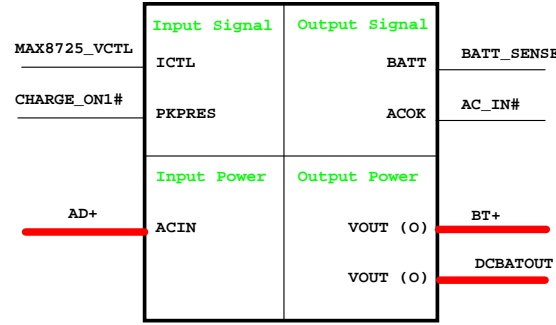
Size A3	Document Number	Rev SA
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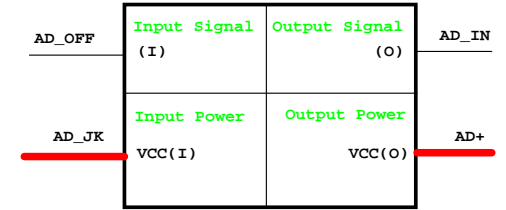
CPU_CORE
Intersil ISL6265



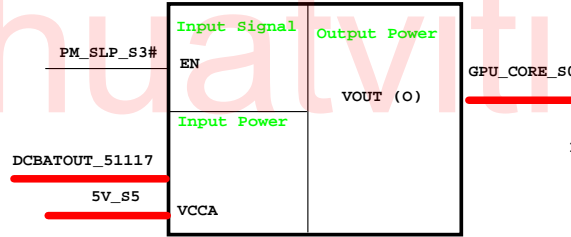
Charger Max8725



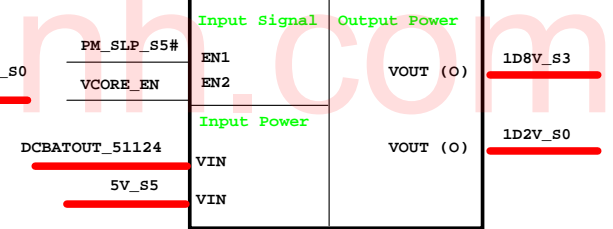
Adapter



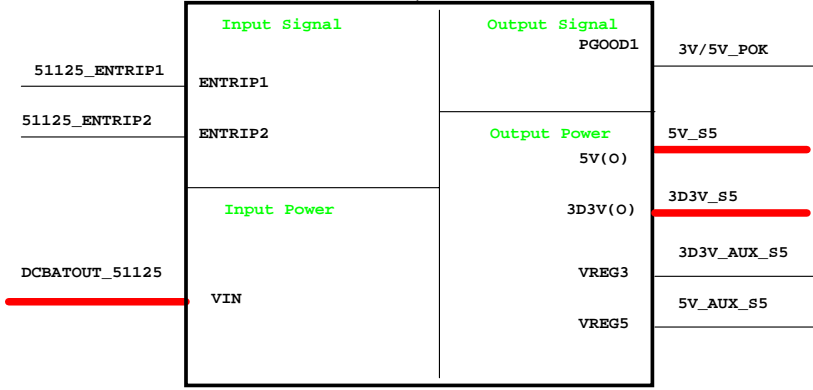
TPS51117
GPU_CORE



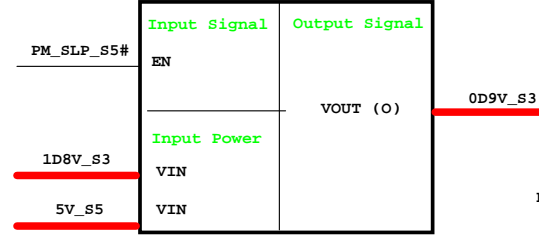
TPS51124
1D8V_S3
1D2V_S0



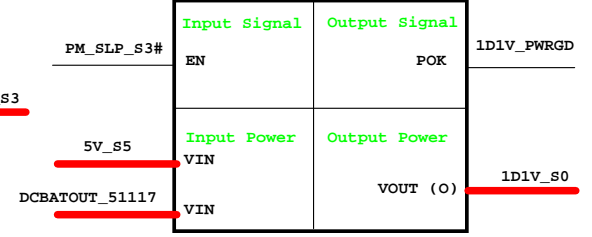
TPS51125
5V/3D3V



RT9026FPF
0D9V_S3



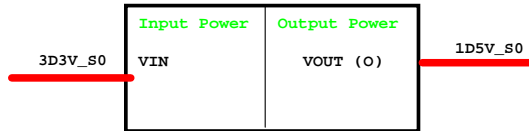
TPS51117
1D1V_S0



G9161
1D2V_S5



G957
1D5V_S0



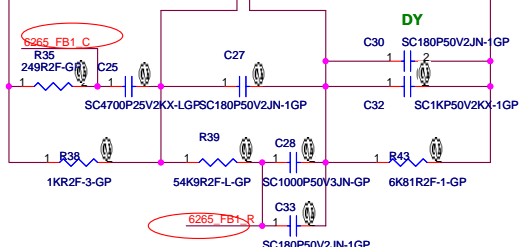
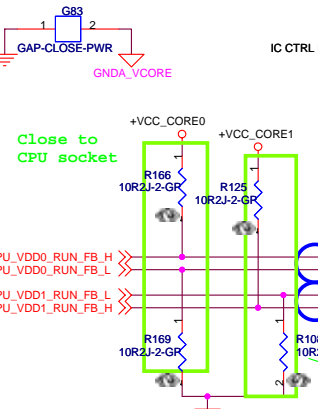
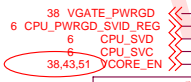
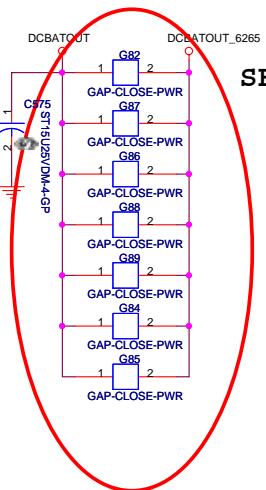
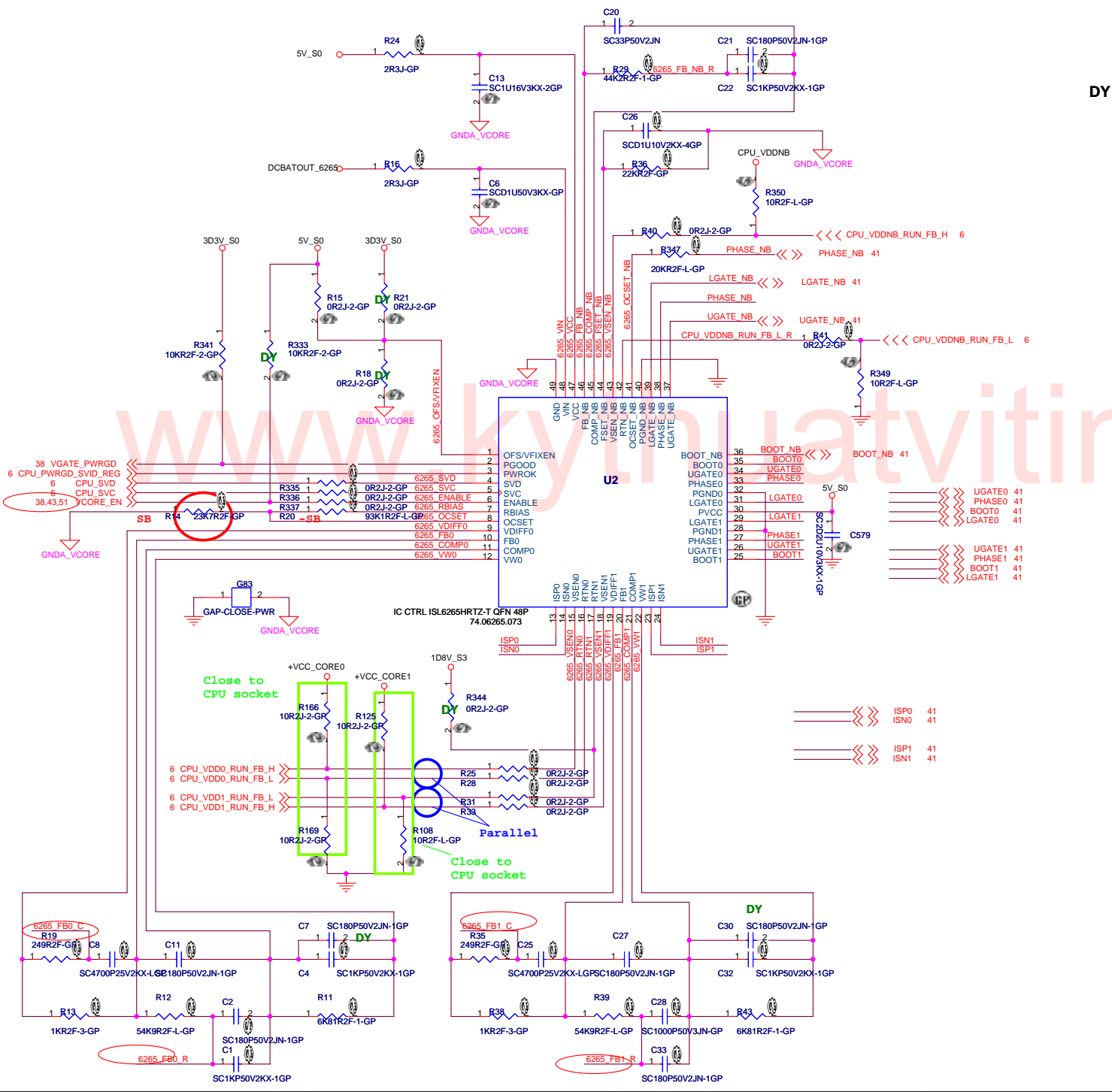
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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1	OFS/VFIXEN	36	BOOT_NB	<<<	BOOT_NB 41
2	PGOOD	35	BOOT0		
3	PWROK	34	UGATE0		
4	SVD	33	PHASE0		
5	SVC	32	PGND0		
6	ENABLE	31	LGATE0		
7	RBIAS	30	LGATE1		
8	OCSET	29	PHASE1		
9	VDIFF0	28	UGATE1		
10	VDIFF0	27	PHASE1		
11	COMP0	26	UGATE1		
12	VW0	25	BOOT1		
13	ISPO	24			
14	ISNO	23			
15	VSEN0	22			
16	RTN1	21			
17	VSEN1	20			
18	VDIFF1	19			
19	VDIFF1	18			
20	COMP1	17			
21	VW1	16			
22	ISP1	15			
23	ISN1	14			
24		13			
25		12			
26		11			
27		10			
28		9			
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35		2			
36		1			

<Variant Name>

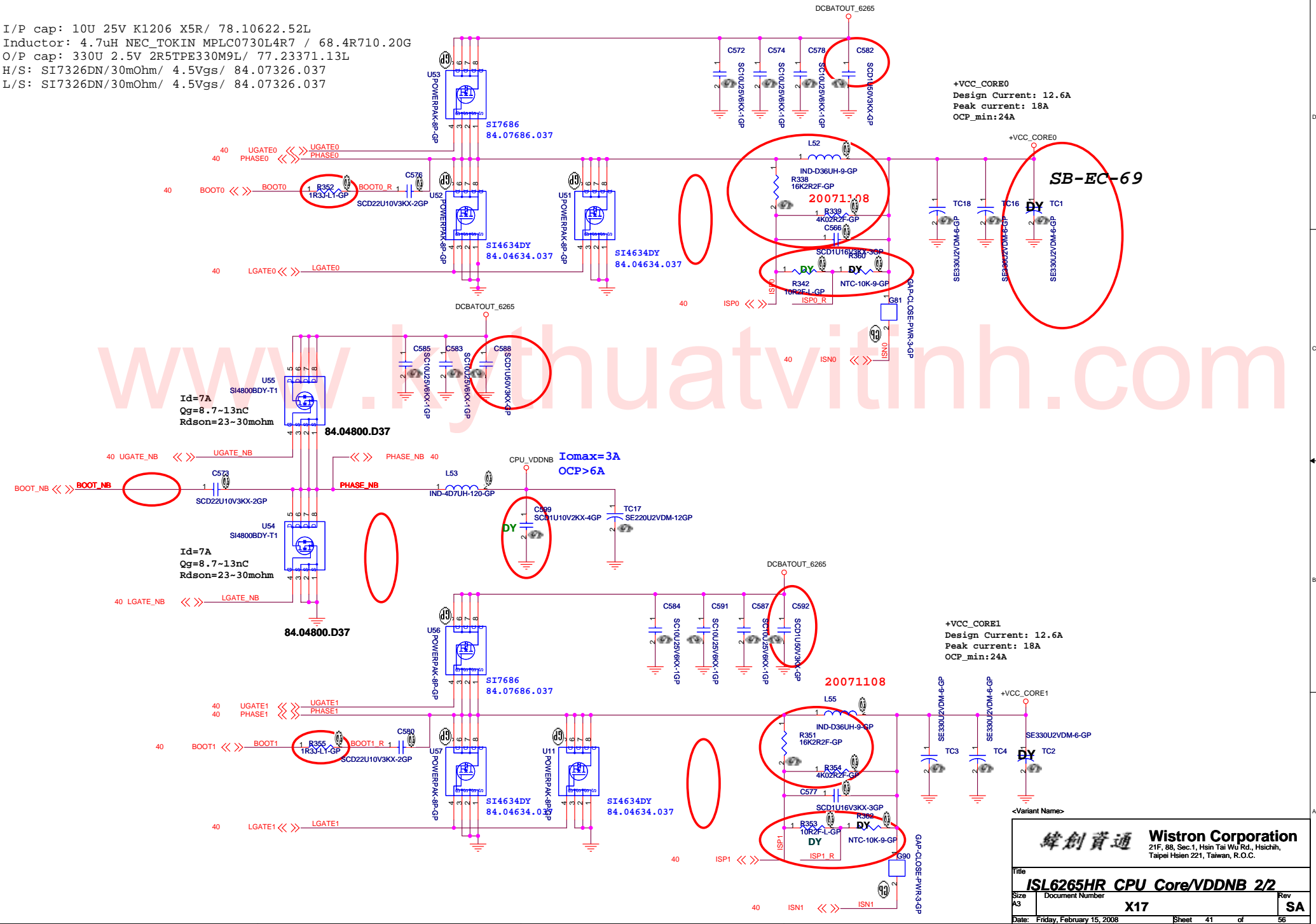
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6265HR CPU Core/VDDNB 1/2**

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I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
 O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
 H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
 L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037



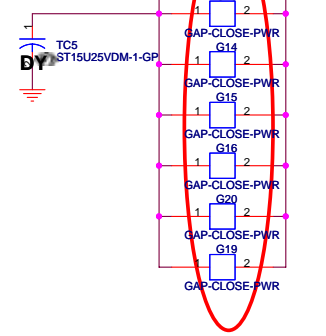
+VCC_CORE0
 Design Current: 12.6A
 Peak current: 18A
 OCP_min: 24A

+VCC_CORE1
 Design Current: 12.6A
 Peak current: 18A
 OCP_min: 24A

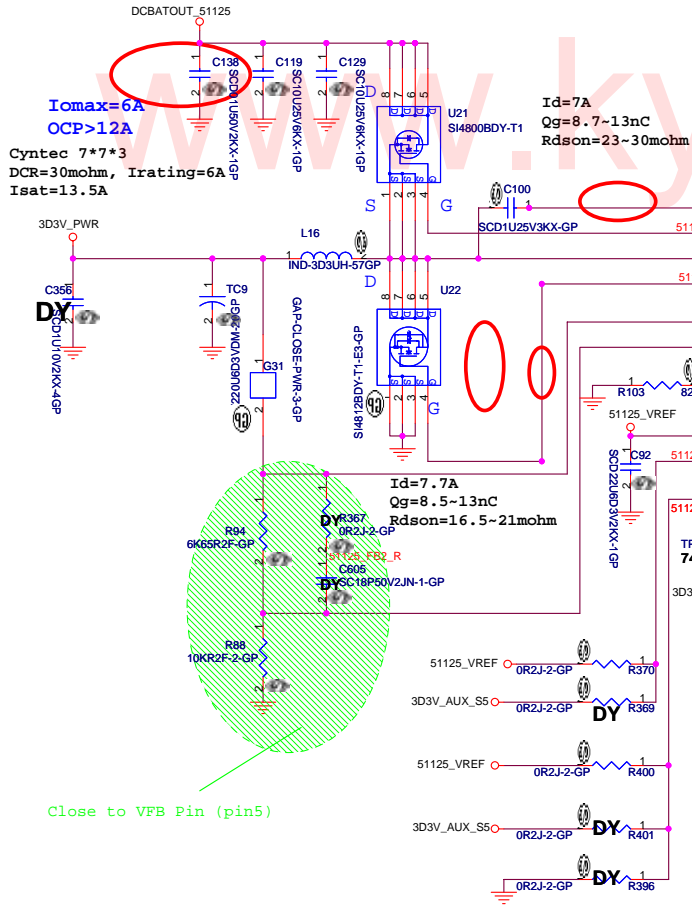
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		ISL6265HR CPU Core/VDDNB 2/2	
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SB-EC52



SB-EC53



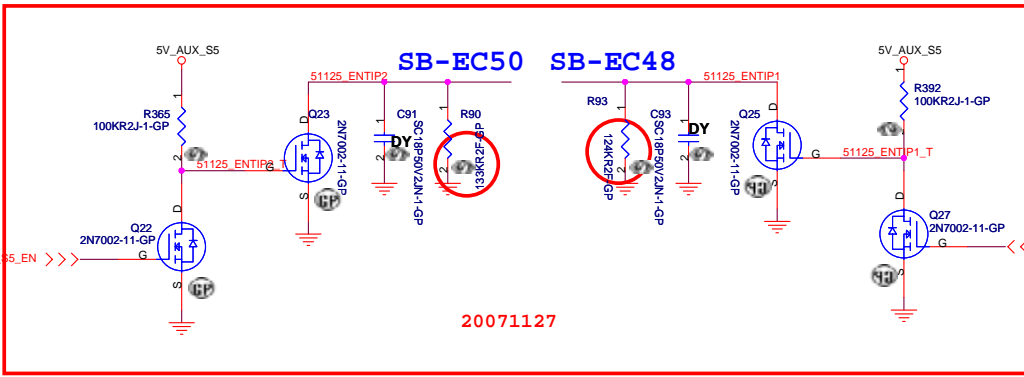
SB-EC4



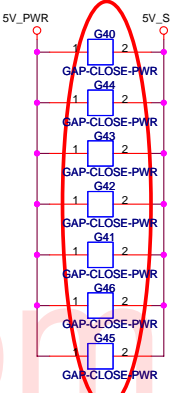
20071127

SB-EC50

SB-EC48



SB-EC54



Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

<Variant Name>

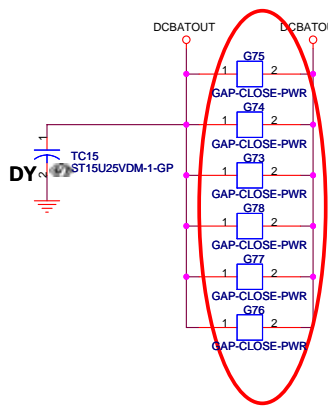
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51125 5V/3D3V**

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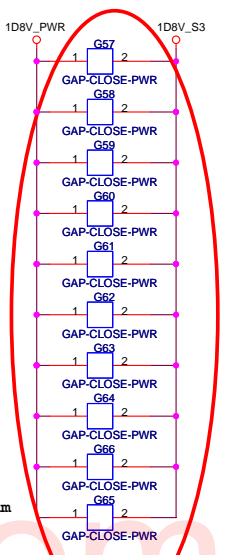
SB-EC55



Id=7.5A
Qg=4-5nC,
Rdson=26-30mohm

Cytec 10*10*4
DCR=3mohm, Irating=15A
Isat=40A

Iomax=12A
OCP>18A

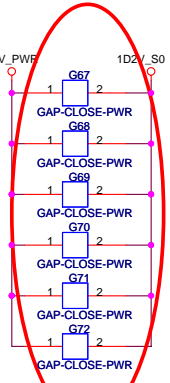


Id=14.5A
Qg=25-35nC,
Rdson=5.9-7.25mohm

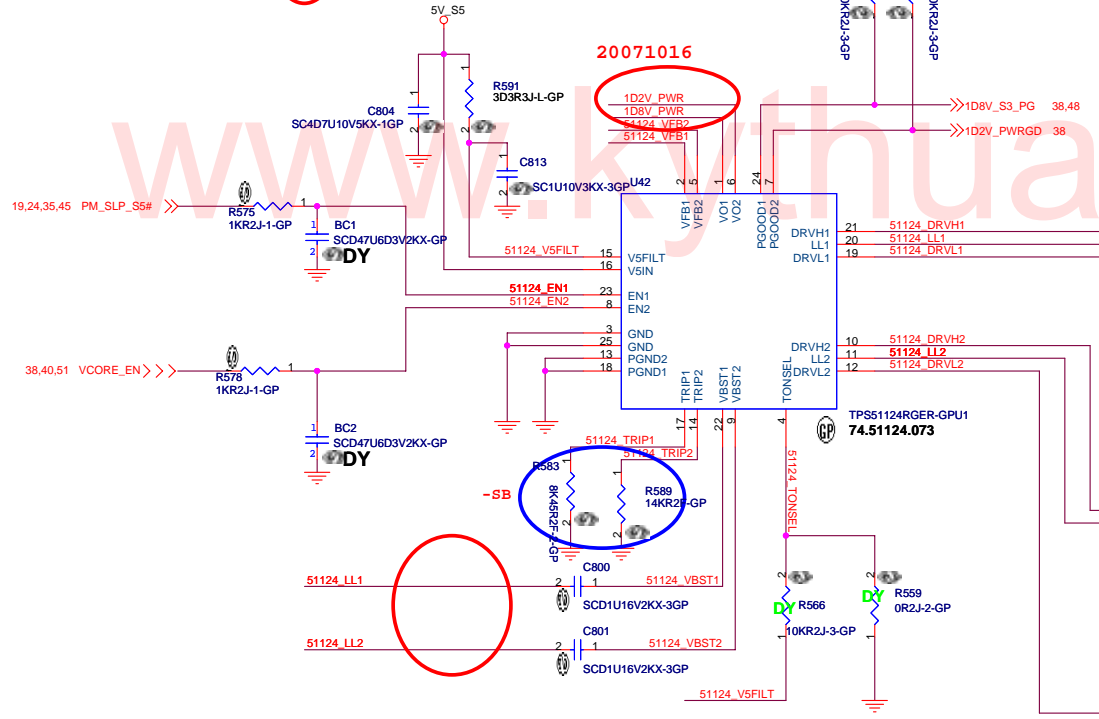
Vo(cal)=1.8046V

SB-EC56

1D2V Iomax=5A
OCP>10A



SB-EC57



20071016

1D2V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1

Id=5A
Qg=8.7-13nC,
Rdson=23-30mohm

Cytec 6*6*3
DCR=14mohm, Irating=9A
Isat=18A

Vo(cal)=1.2077V

SANYO
ESR=15mohm

Fujitsu
ESR=15mohm

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

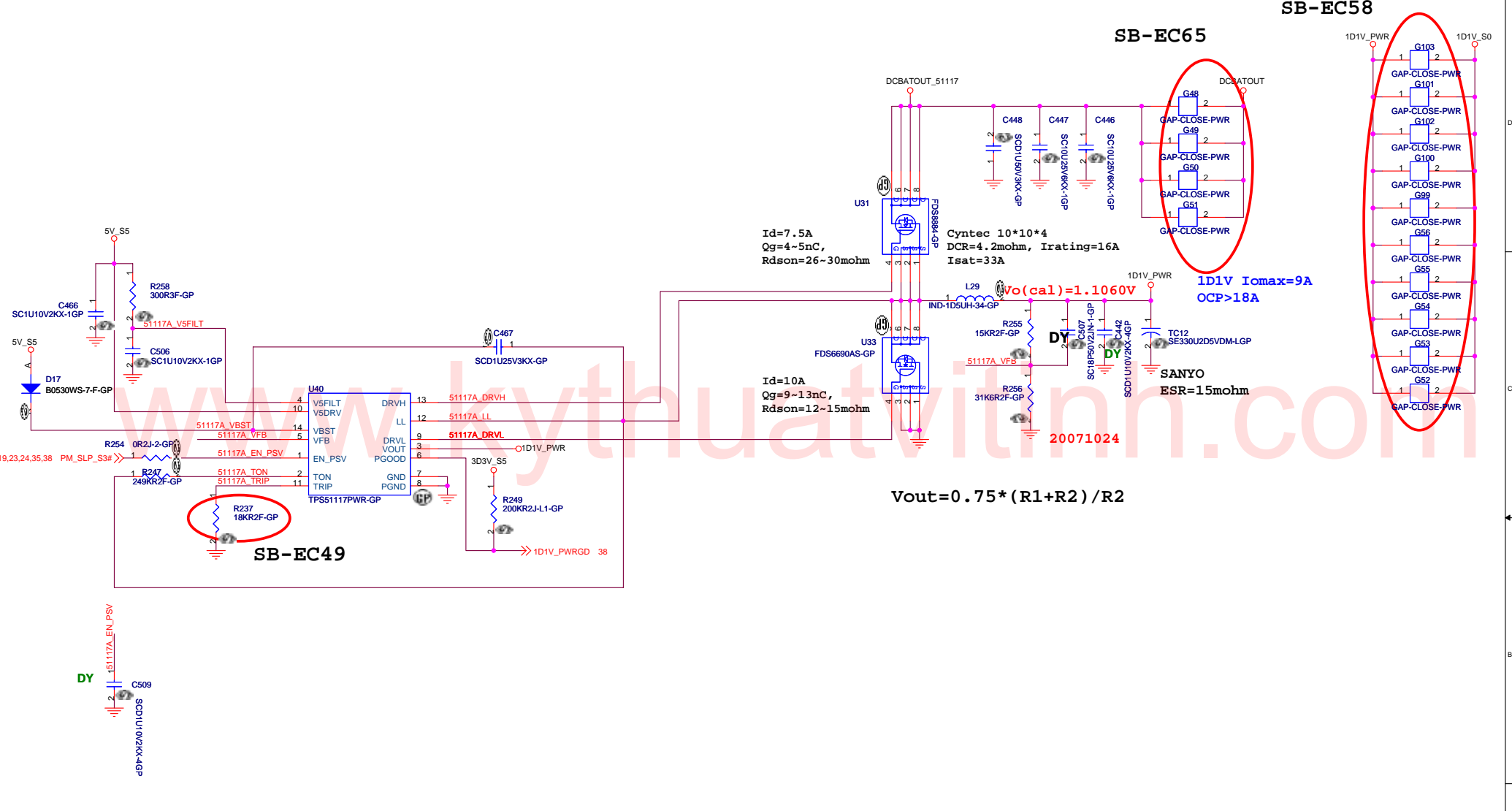
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D8V/1D2V**

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

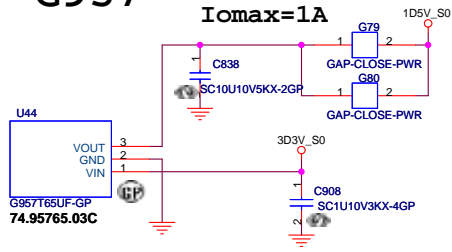
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TPS51117 1D1V

Size A3	Document Number X17	Rev SA
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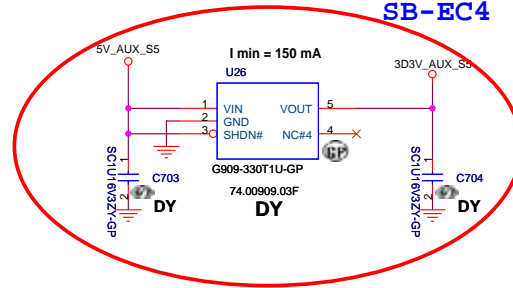
Date: Friday, February 15, 2008 Sheet 44 of 56

G957

1D5V_S0
I_{omax}=1A

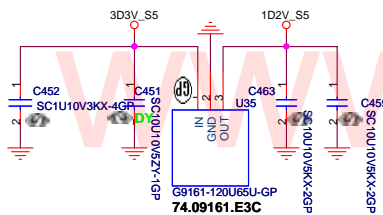


SB-EC4

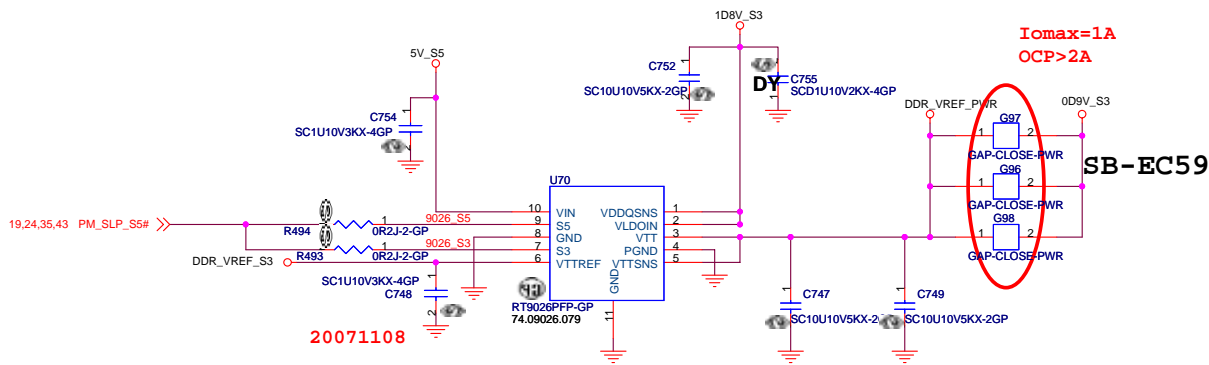


1D2V_S5

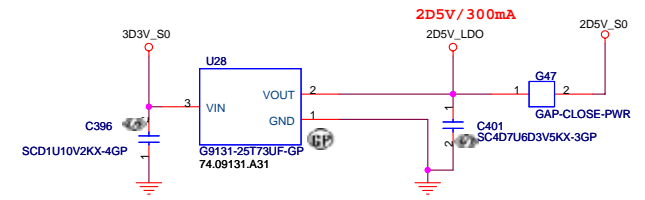
I_{omax}=400mA



Place near to SB700



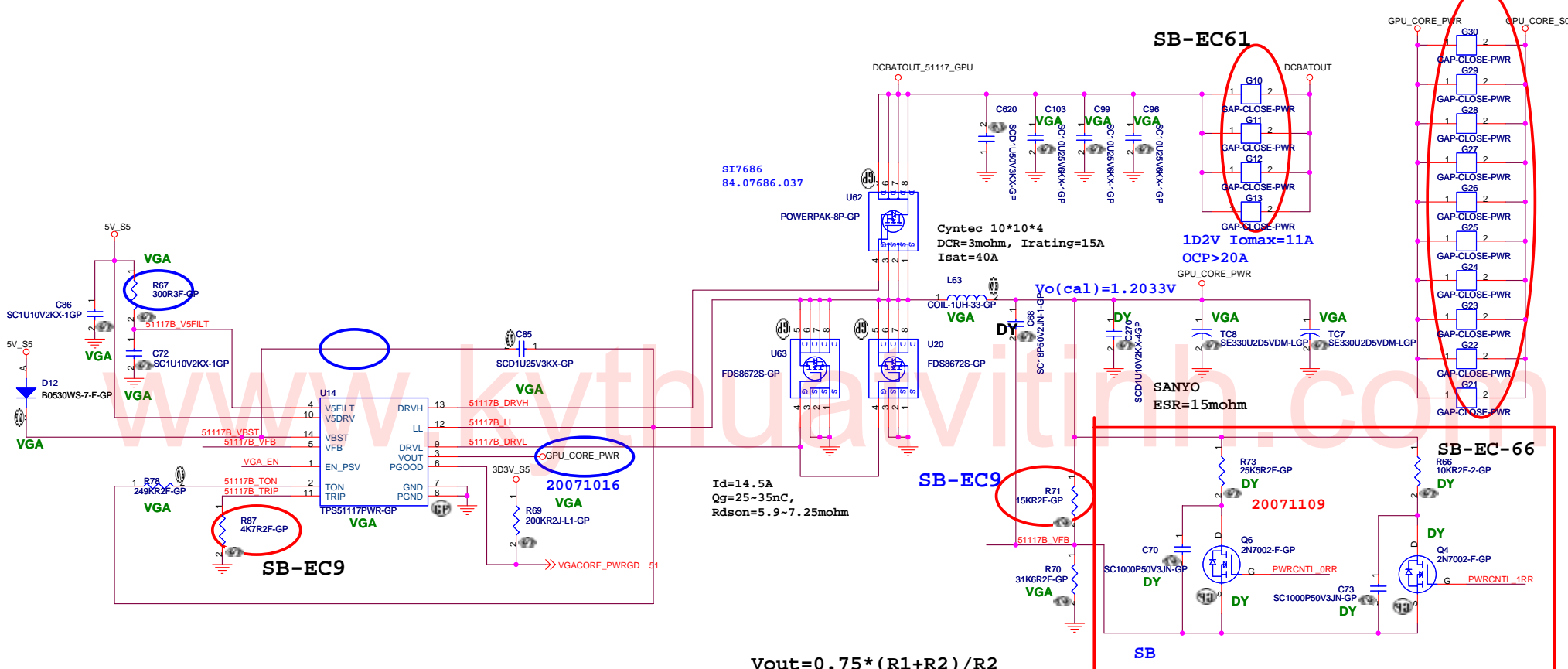
2D5V_S0
I_{omax}=0.3A



<Variant Name>

緯創資通 **Wistron Corporation**
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Title		
0D9V&2D5V&1D25V&1D5V		
Size	Document Number	Rev
A3	X17	SA
Date:	Friday, February 15, 2008	Sheet 45 of 56



SI7686
84.07686.037

Cyntec 10*10*4
DCR=3mohm, Irating=15A
Isat=40A

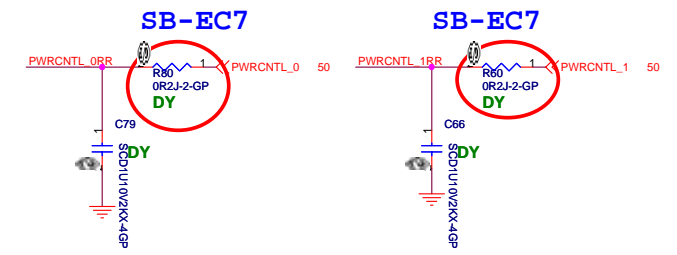
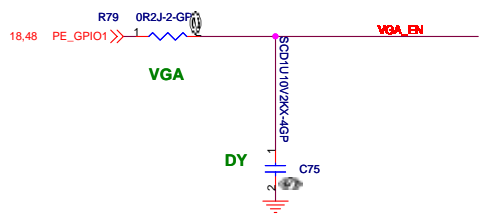
1D2V Iomax=11A
OCP>20A

Id=14.5A
Qg=25~35nC,
Rdson=5.9~7.25mohm

SANYO
ESR=15mohm

$$V_{out} = 0.75 * (R1 + R2) / R2$$

PWRCNTL_0	PWRCNTL_1	Vout(Default)	Vout(Cal.)
0	0	1.2V	1.2033V
1	0	1.0V	1.0091V
0	1	0.9V	0.9057V



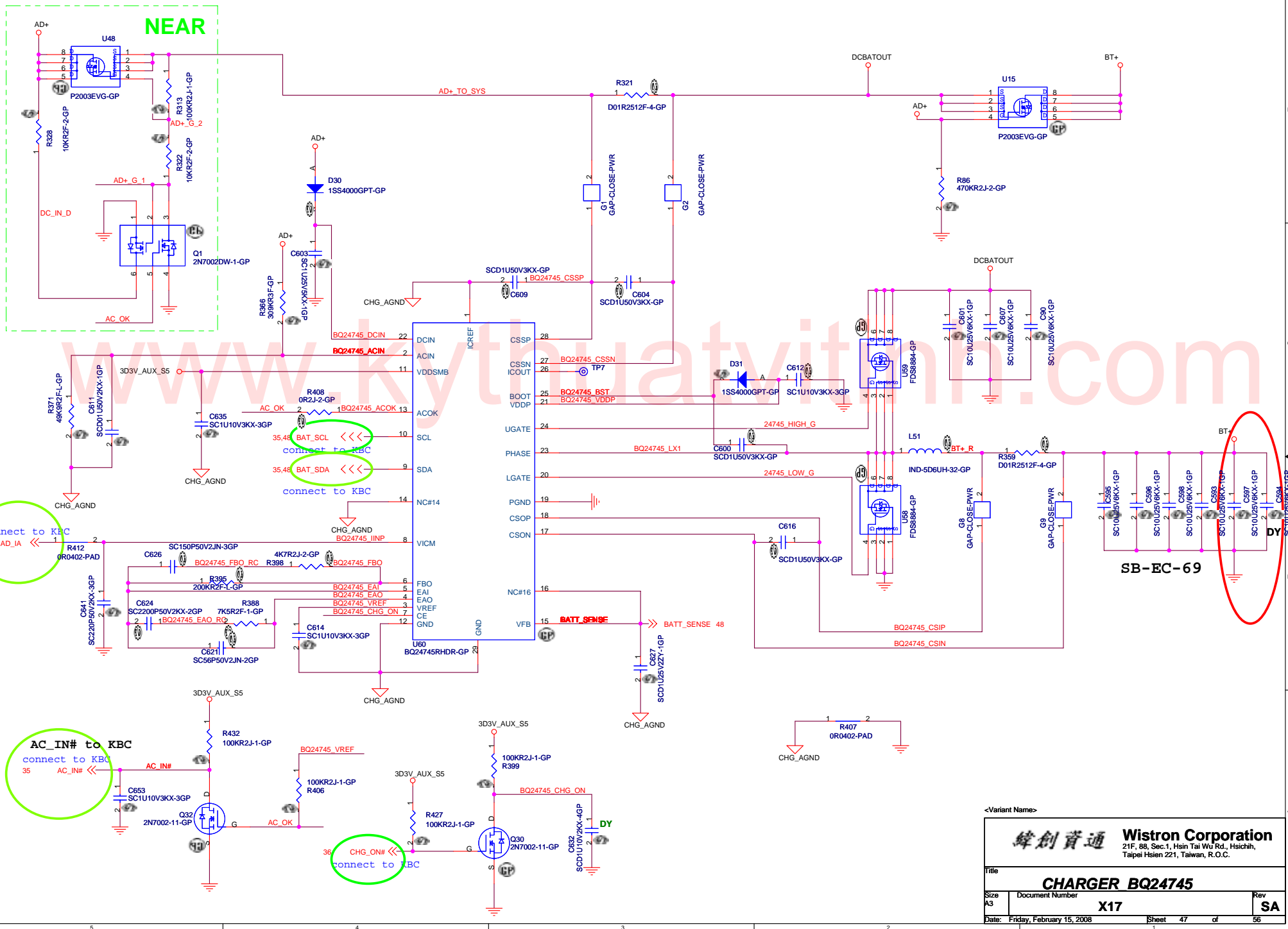
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51117 GPU Core

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<Variant Name>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

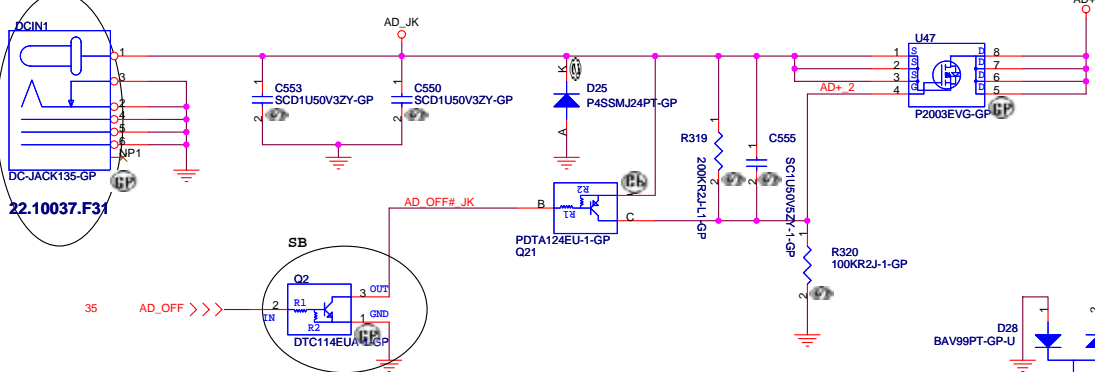
Title: **CHARGER BQ24745**

Size A3	Document Number	Rev SA
X17		

Date: Friday, February 15, 2008 Sheet 47 of 56

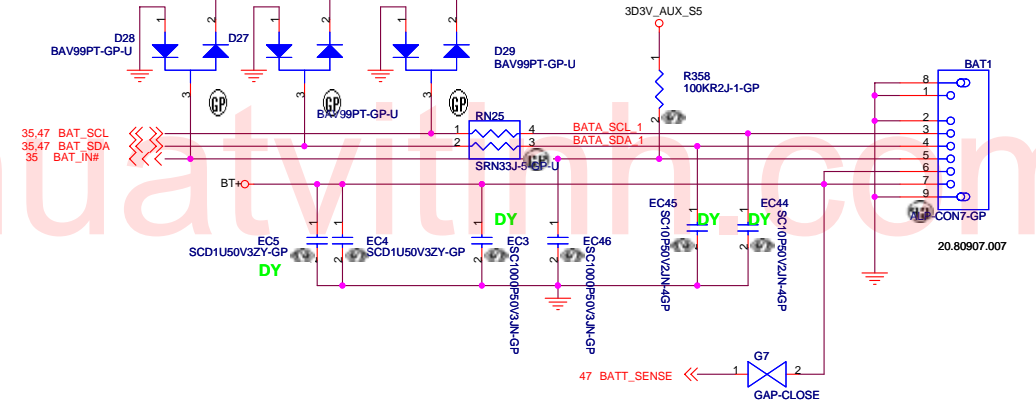
SB-EC21

Adaptor in to generate DCBATOUT

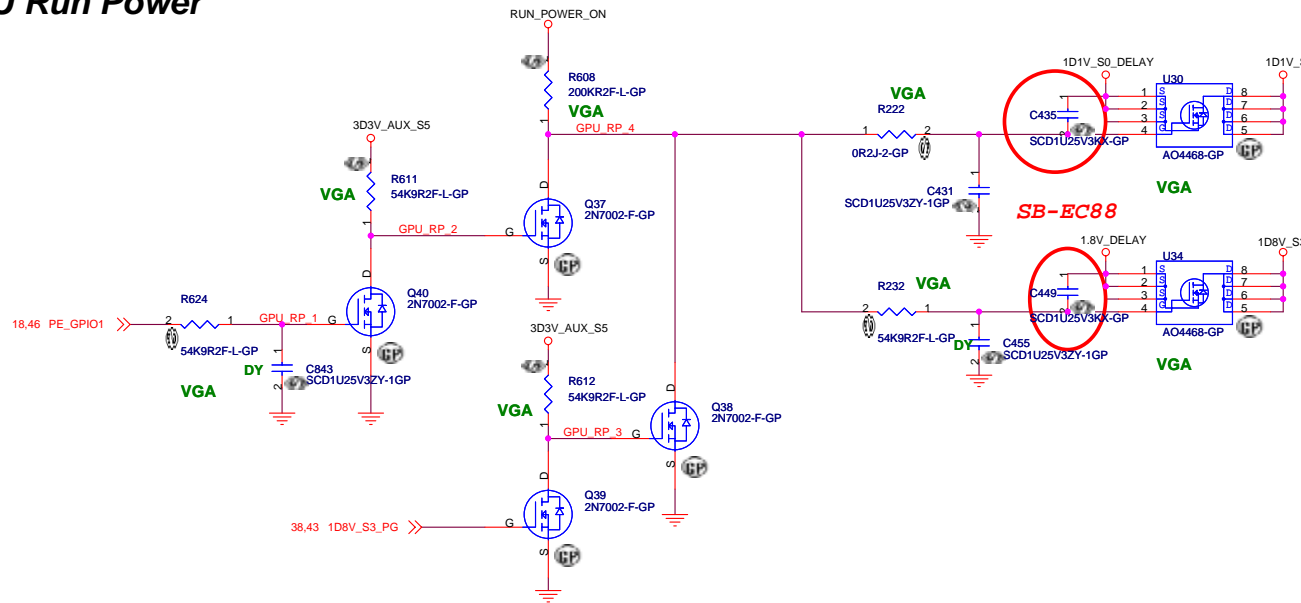


SB-EC31

BATTERY CONNECTOR



GPU Run Power



www.kythuratv.com

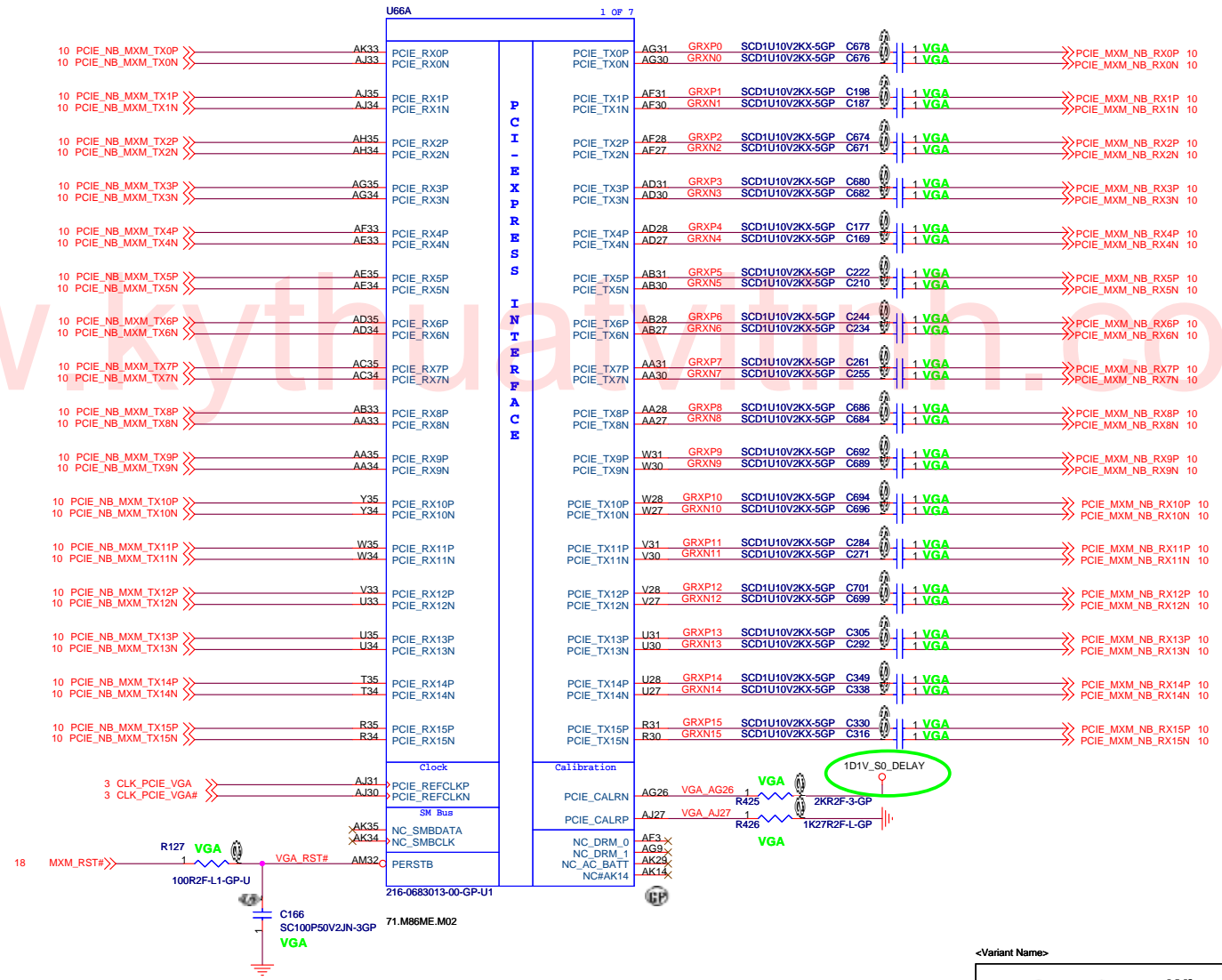
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
AD IN/ BTY SWITCH/GPURUN

Size A3 Document Number **X17** Rev SA

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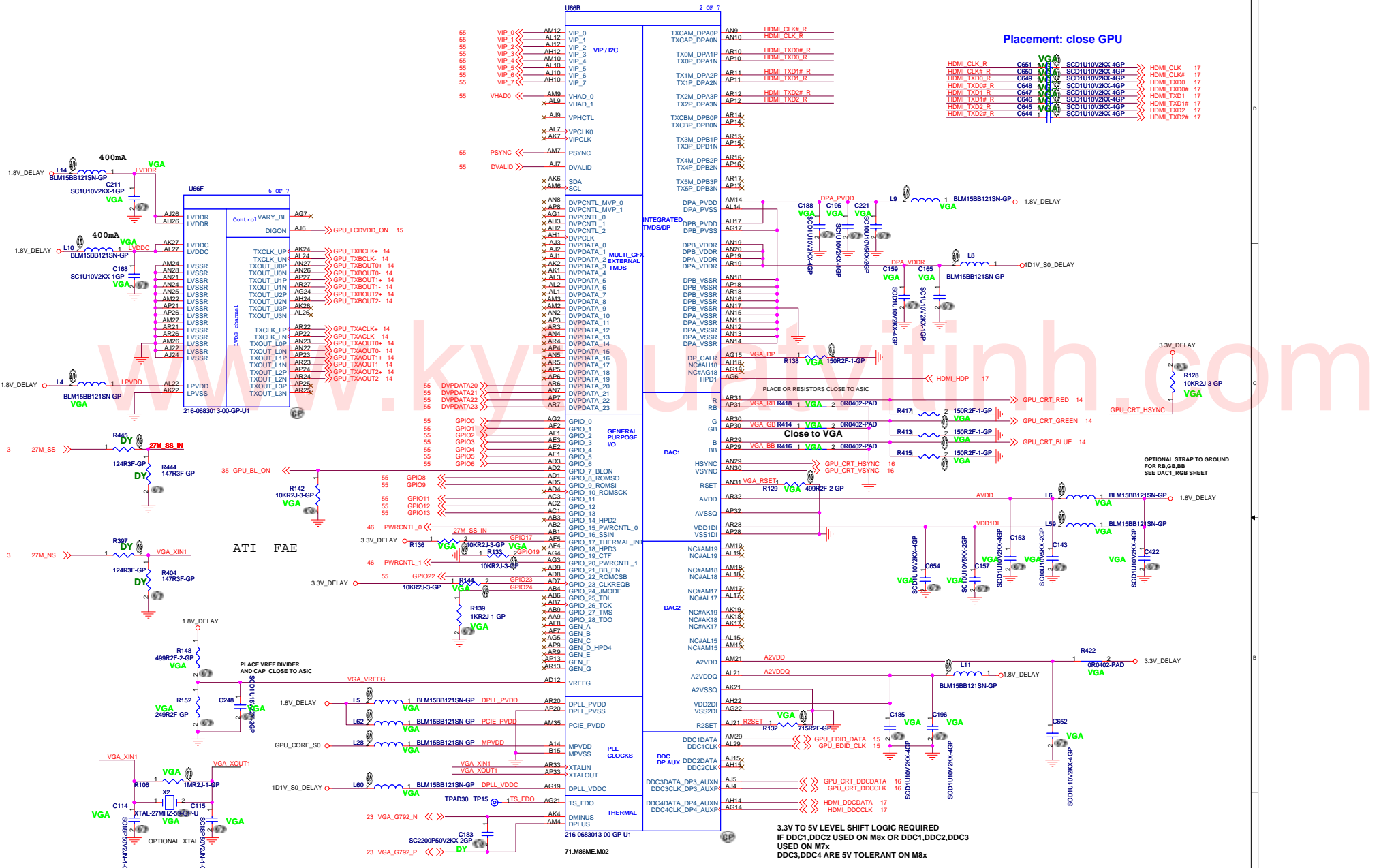
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **M8XM PCIE**

Size: A3 | Document Number: **X17** | Rev: SA

Date: Friday, February 15, 2008 | Sheet: 49 of 56

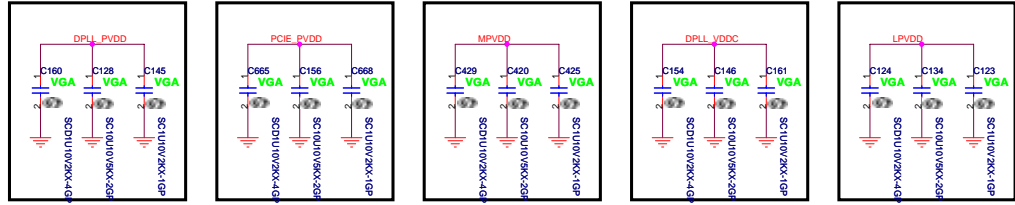


Placement: close GPU

INTEGRATED TMS/SDP

Close to VGA

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED IF DDC1, DDC2 USED ON M8x OR DDC1, DDC2, DDC3 USED ON M7x
 DDC3, DDC4 ARE 5V TOLERANT ON M8x

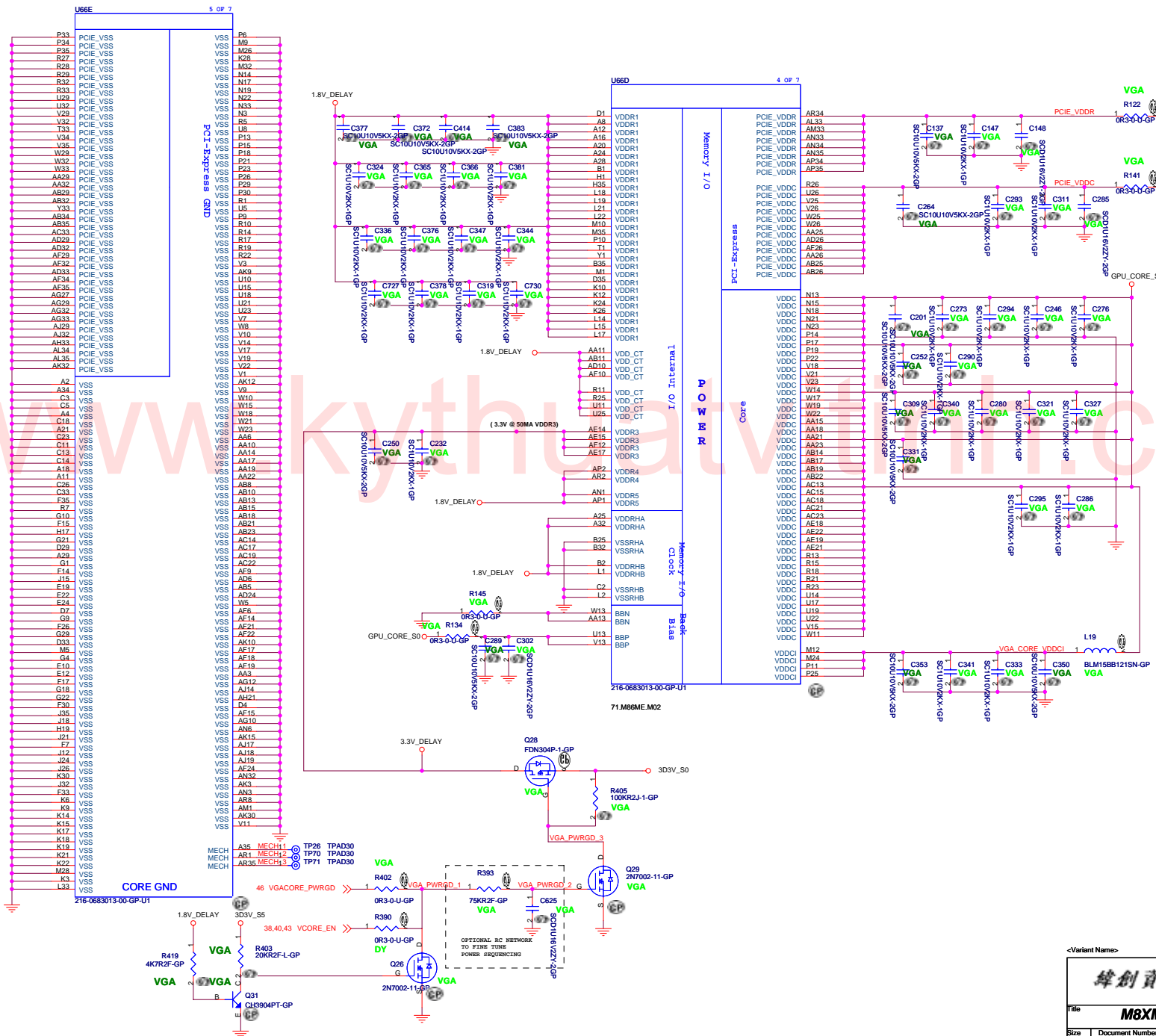


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Model: **M8XM IO**

Size: Custom
 Document Number: **X17**

Date: Friday, February 15, 2008
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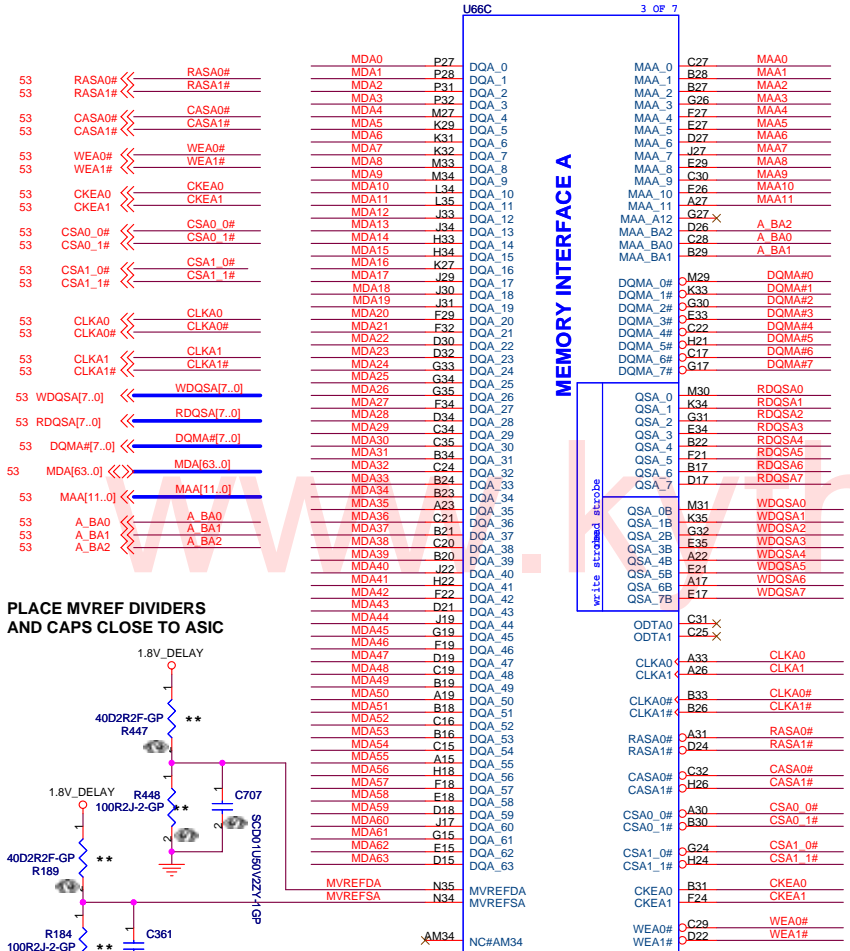
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

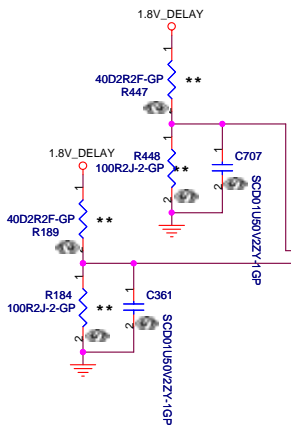
File: **M8XM_POWER**

Size: Custom Document Number: **X17** Rev: **SA**

Date: Friday, February 15, 2008 Sheet 51 of 56

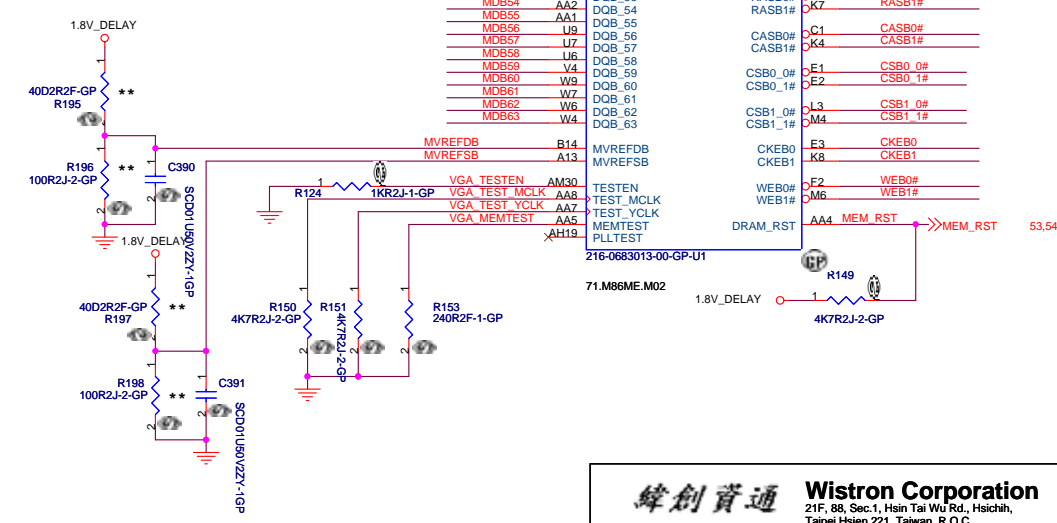


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

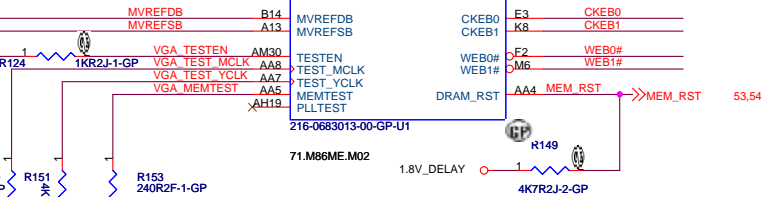
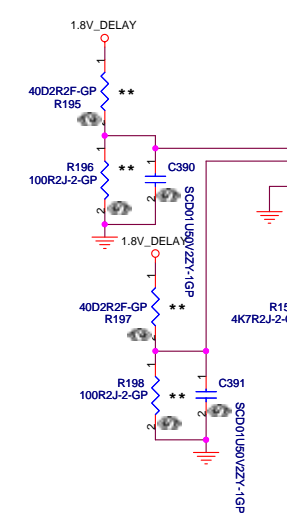


** DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

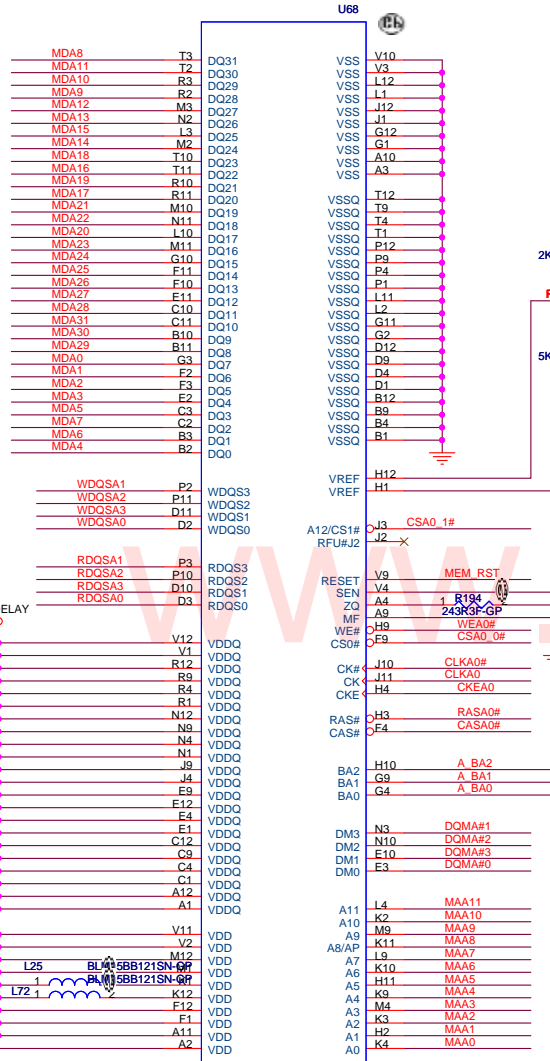


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

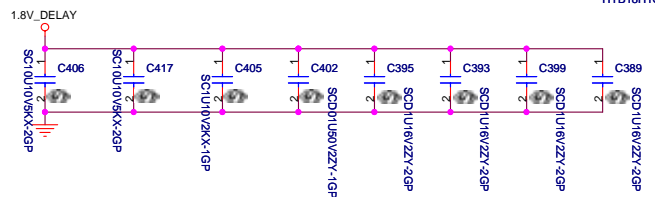
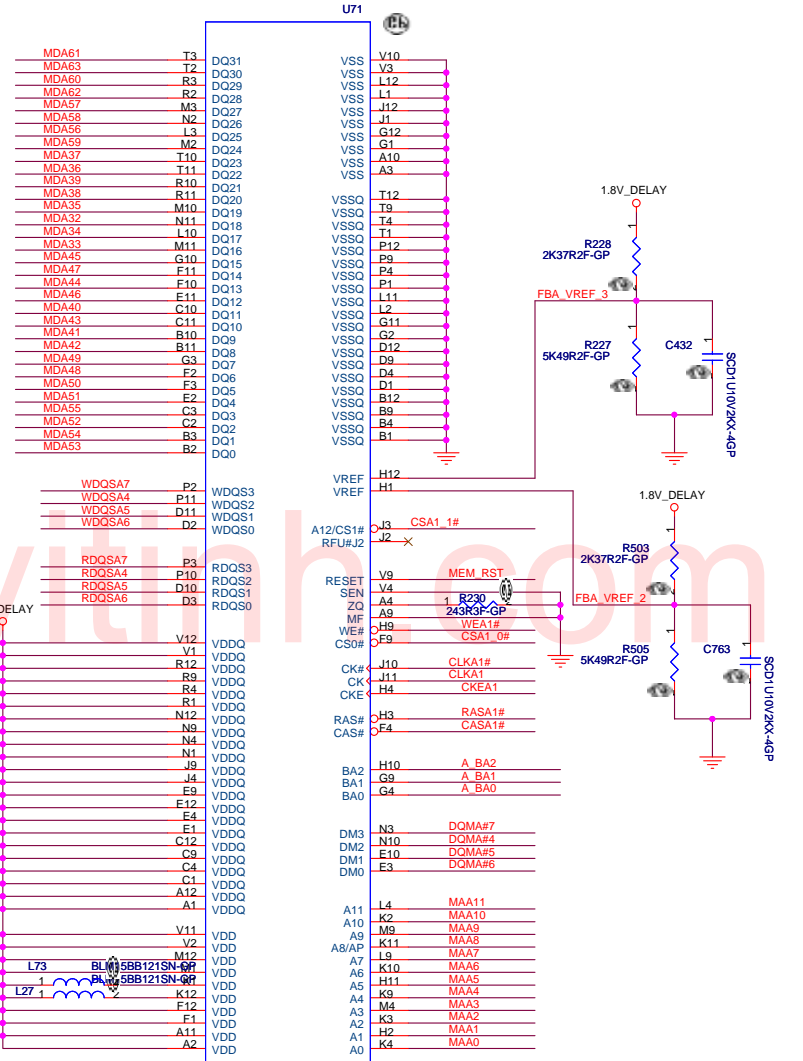
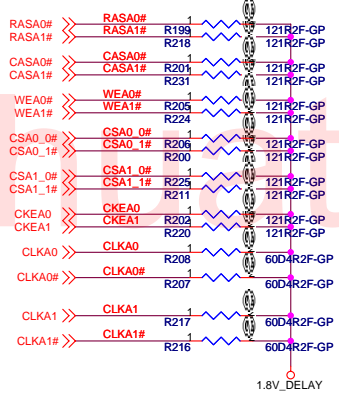
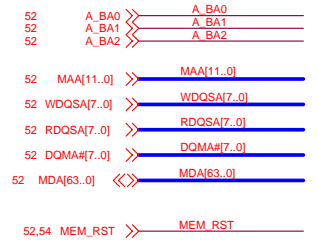


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Title			
M8XM MEMORY			
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Main source : 72.18321.00U(Qimonda 700M)
 2'nd source : 72.18321.A0U(Qimonda 900M)
 3'rd source : 72.41032.B0U(Samsung)

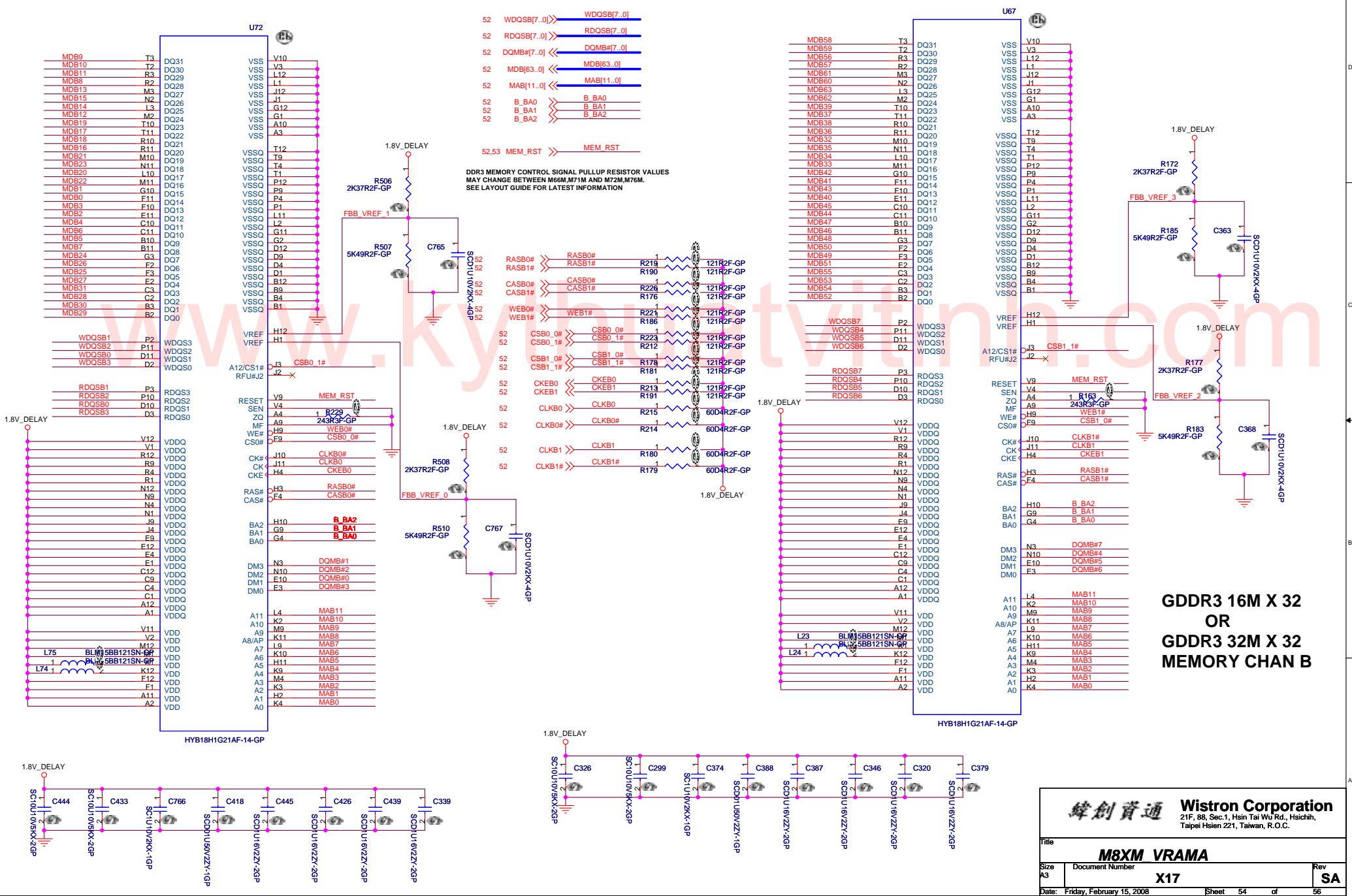


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Title: **M86ME VRAMA**

Size A3 Document Number **X17** Rev **SA**

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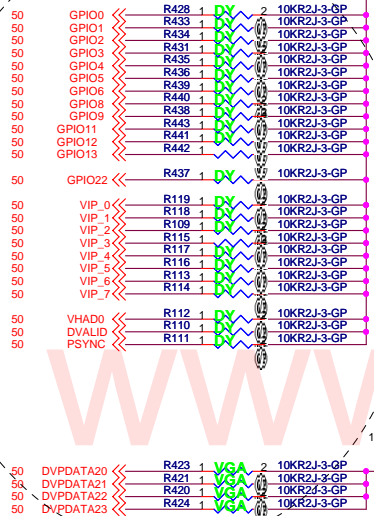


**GDDR3 16M X 32
OR
GDDR3 32M X 32
MEMORY CHAN B**

緯創資通 Wistron Corporation	
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Title: M8XM VRAMA	
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SB-EC7

3.3V_DELAY



Only populate the required straps, see table and databook

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE
 RSVd = ATI RESERVED
 (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x		M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA		0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7XM and M86M ONLY) Note:1	X	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA		0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X		X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X		X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0		0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82M ONLY) Note:2	X		RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X		0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA		X
ROMIDCFG(3:0)	GPIO(13:11,9)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X		XX X X
VIP_DEVICE_STRAP_ENA	VSYNc	IGNORE VIP DEVICE STRAPS	0		0
BIF_VGA_DIS	PSYNc	VGA ENABLED	0		0
BIF_HDMI_EN	HSYNc	HDMI ENABLE (SEE NOTE 2)	X		X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0		0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X		X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

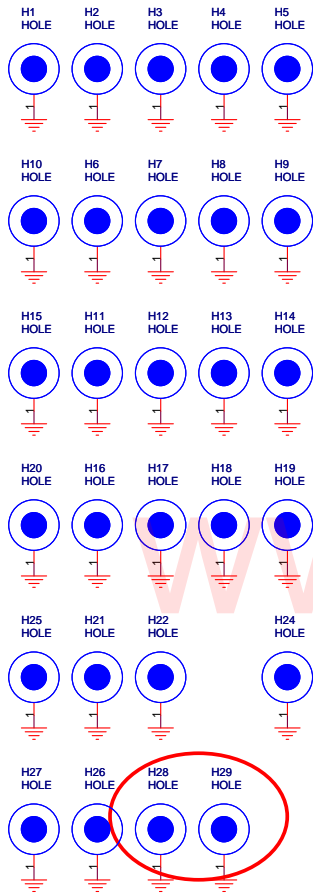
ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

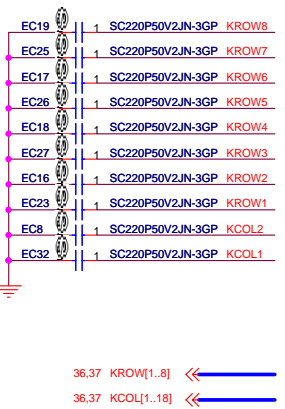
VHAD0	VIP0	VIP2	VIP4	VIP6	VIP7	GPIO2	GPIO3	H2SYNc
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET								
GPIO_28_TDO	GENERICc	GPIO21_BB_EN						

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
STRAPS			
Size A3	Document Number		Rev SA
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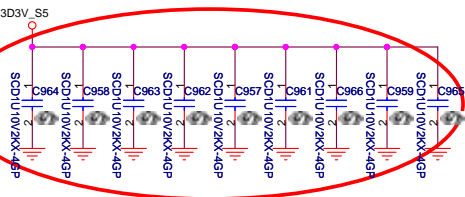
Keyboard EMI Caps



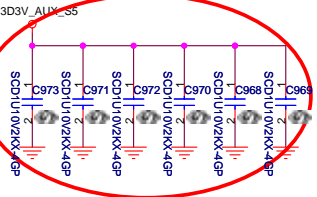
36.37 KROW[1..8] ←←
36.37 KCOL[1..18] ←←

EMI Power

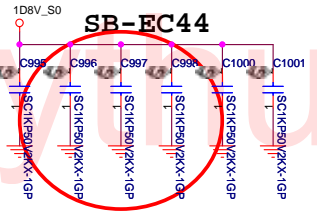
SB-EC37



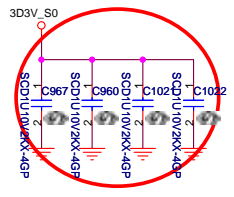
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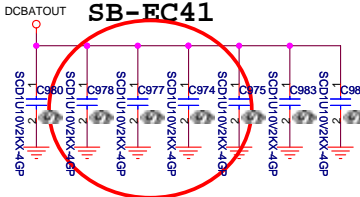
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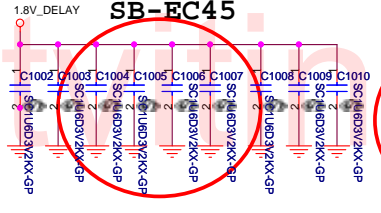
SB-EC39



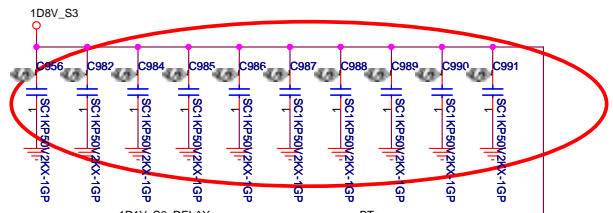
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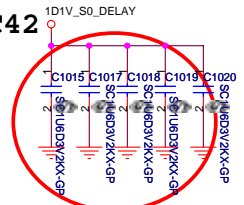
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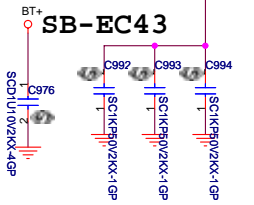
SB-EC38



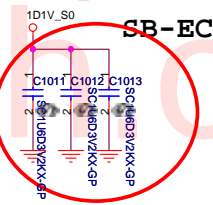
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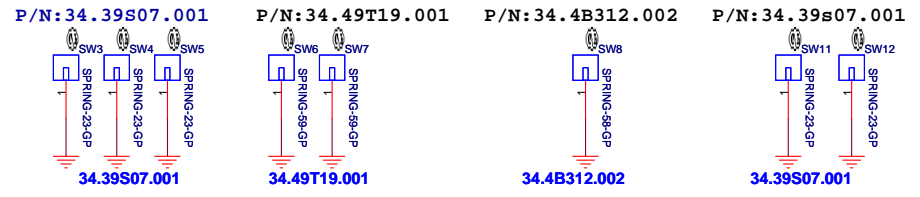
SB-EC43



SB-EC46



SB-EC36



- SB ME

<Variant Name>

緯創資通		Wistron Corporation	
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Title			
EMI			
Size	Document Number		Rev
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