Parker Block Diagram

Project code:91.4S701.001
PCB P/N :48.4S701.001
REVISION :06240-1

CPU
U1400 FW289
U1500 UP954
U2100
U7500 JW620
U7600 FW418

Clock Generator
ICS 951463 4

Intel Mobile CPU
Yonah / Merom ULV
FSB:533Mhz
5,6

HOST BUS FSB 533MHz

200-PIN DDR2 SODIMM
Support Aero Glass

12.1WXGA 17 — LVDS

RS600ME
DUAL DDR2 CHANNEL
INTEGRATED GRAPHICS
PCI-EXPRESS(4)
LVDS
7,8,9,10,11

DDRII 533/667MHz — ON-BOARD RAM 1G
CELL X 8 12,13,14

DDRII 533/667MHz — UNBUFFERED DDR2
SODIMM Socket 15

SDVO

CRT Port 16 — RGB CRT

CRT

PCI Express (4) — Power Switch 31

Express Card Slot 54mm PORT6 PCIE3 31

Mini-Card WWAN PORT9 PCIE1 32 — SIM CONN 32

Mini-Card 802.11a/g/n PCIE2 32

Biometric PORT5 17

Bluetooth PORT7 31

USB*2 PORT0.1
P-USB*1 PORT2 34

Digi Tizer PORT3 17

ALINK x4

Thermal Sensor EMC4001 23

PATA HDD 33 — IDE

ATI
SB600
USB 2.0/1.1 ports (10)
High Definition Audio
ATA 66/ 100/133
SATA2 (4)
LPC I/F
PCI/PCI BRIDGE
ACPI 2.0
SPI
18,19,20,21,22

1394 CONN 26 — 1394
SD card 26 — 8 in1
TI 7402
Card reader
1394 2 port 24,25
PCI BUS

USB2.0 (10)

AZALIA

MIC IN
Digital MIC Array
Azalia CODEC
STAC 9205 29

LINE OUT
INT.SPKR
Speaker AMP.
Headphone AMP.
TI TPA6040A4 30

SPI

LPC

BCM5756ME
Giga LAN
TPM 1.2 PCIE0 27

RJ45 CONN 28

BIOS
SPI FLASH
2MB 33 — SPI

EC
SMSC MEC5025 35

SIO Expander
SMSC ECE5021 36

SMBus

Touch Pad 37

KBC
SMSC ECE1077 37

Int. KB 37

DVI CRT S/PDIF SMBus USB 2.0 PORT8 RJ45

Media-Slice 38

08/14/2007

Battery Charger
ISL88731 39,40

INPUTS	OUTPUTS
+PWR_SRC	+PBATT

CPU DC/DC
ADP3207 42

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

System DC/DC
ISL6236/MAX8778 43

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO +5V_ALW +3.3V_ALW

LDO MAX8794 44

+1.8V_SUS	+1.5V_RUN

LDO TPS51100 44

+1.8V_SUS	+0.9V_DDR_VTT V_DDR_NB_REF

System DC/DC
ISL6236/MAX8778 45

+PWR_SRC	+1.8V_SUS +1.05V_VCCP

System DC/DC
ISL6236/MAX8778 46

+PWR_SRC	+NB_VCORE +1.2V_SUS

PCB LAYER

L1:TOP
L2:Signal
L3:GND
L4:Signal
L5:GND
L6:VCC
L7:Signal
L8:GND
L9:Signal
L10:BOTTON

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Parker | Rev: -1
Date: Wednesday, August 29, 2007 | Sheet 1 of 53

CLK-GEN ICS951463

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CLKREQA# B# C# MAP

CLKREQA#	CLKSRC 7 NB ALINK
	CLKSRC 5 EXPRESS CARD
	CLKSRC 6 SB ALINK
CLKREQB#	CLKSRC 2 WLAN
	CLKSRC 4 LOM
CLKREQC#	CLKSRC 0 WWAN
	ATIGCLK 1 NB-PCIEX16
	ATIGCLK 2 NO -USED

ATI NB-RS600ME STRAP PIN

Strap name	LOW 0	HIGH 1
NB_VSYNC (DAC_VSYNC: STRAP_MOBILE_GFX)	DESKTOP GRAPHICS DEVICE	MOBILE GRAPHICS DEVICE ★
NB_HSYNC (DAC_HSYNC: STRP_INTGFX_DISABLE)	ENABLE ★	DISABLE
NB_SDVO_CTRLDATA (DDC_DATA: STRAP_MEMVMODE)	DDR3	DDR2 ★
STRP_DATA (STRP_DATA: STRP_MEMSTRAPS)	SELECT MEMORY CHA A AS DEBUG BUS	NORMAL MODE ★

SR600ME PCIE route

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD

ATI SB-SB600 STRAP PIN

Strap name	LOW 0	HIGH 1
AC_SDOUT SB_AC_SDOUT	IGNORE DEBUG STRAPS ★	DEBUG STRAPS Default
RTC_CLK SB_RTCCLK	EXTERNAL RTC	INTERNAL RTC ★ Default
PCI_CLK4 CLK_SB_PCI4	EXTERNAL 48MHZ ★ Default	INTERNAL PLL48
PCI_CLK6 CLK_SB_PCI6	INTEL CPU ★ Default	AMD CPU

PCI_CLK0 CLK_SB_PCI0	PCI_CLK1 CLK_SB_PCI1	ROM TYPE
0	0	FWH
0	1	LPC Default
1	0	SPI
1	1	PCI

USB TABLE

USB0	Ext Side 1
USB1	Ext Side 2
USB2	POWER USB
USB3	Digi Tizer
USB4	
USB5	Biometric
USB6	Express Card
USB7	BLUETOOTH
USB8	Media Slice
USB9	MiniCard WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MEDIACARD	AD17	G H	1	1

PCI-CLK route

PCICLK 2	MEC5025
PCICLK 5	BCM5756ME
PCICLK 6	TI7402

TABLE OF CONTENTS

SMBUS TABLE

SMBUS TABLE

SOURCE	SIGNAL NAME	LINKED DEVICES
RS600ME	I2C_CLK/DAC_SDA	CRT/SLICE CRT
	I2C_CLK/I2C_DATA	LVDS
	I2C_CLK/DDC_SDA	DVI
SB600	SCL1/SDA1	LAN / WLAN / WWAN / EXPRESS CARD/SO-DIMM
MEC5025	AB1A_CLK/AB1A_DATA	SLICE CONN.
	AB1B_CLK/AB1B_DATA	INVERTER / LIGHT SENSOR
	AB1C_CLK/AB1C_DATA	BATTERY CONN.
	AB1D_CLK/AB1D_DATA	BATTERY-SLICE CONN.
	AB1E_CLK/AB1E_DATA	P-USB / CHARGER / THERMAL
	AB1H_CLK/AB1H_DATA	CLK-GEN
	IMCLK/IMDAA	TOUCH PAD

EMC4001 Thermal sensor mapping

D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

<Variant Name>

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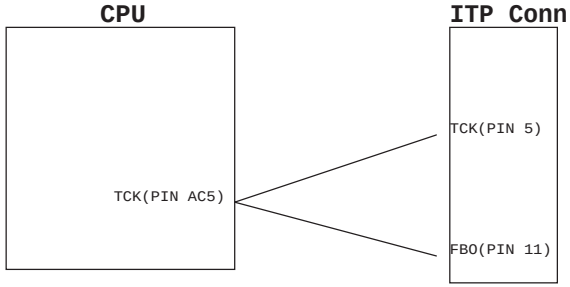
Title: Table Contsnt

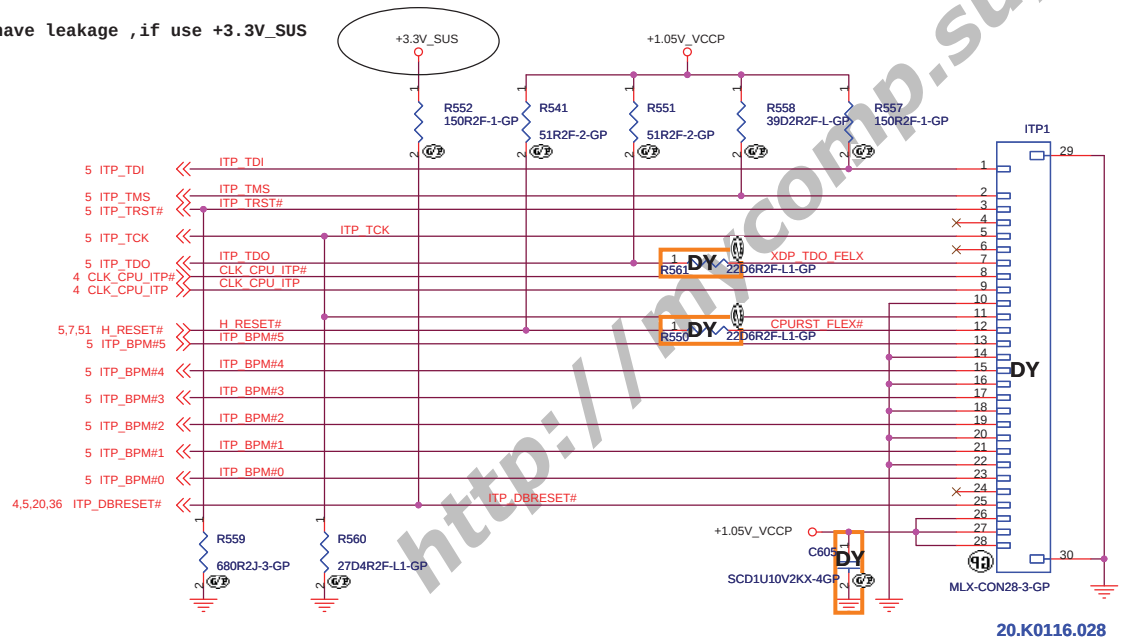
Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 2 of 53

SSID = CPU



clk-gen may have leakage ,if use +3.3V_SUS



20.K0116.028

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

<Variant Name>

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Title		
ITP Debug		
Size: A3	Document Number: Parker	Rev: -1
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1500mA

200mA

200mA

200mA

CLK-GEN XTAL

CLOSE TO PIN 14,23,26,33,36,48

CLOSE TO PIN 42

CLOSE TO PIN 4

CLOSE TO PIN 1

CLOSE TO PIN2 ,3

SSID = CLOCK

placed CAP closed CLK-GEN within 20 mm (80mil)

CLKREQA# B# C# INTERNAL 120K ohm PU

CLOSE TO PIN 40

placed CAP closed CLK-GEN within 20 mm (80mil)

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CLKREQA# B# C# MAP

CLKREQA#	CLKSRC 7 NB ALINK
	CLKSRC 5 EXPRESS CARD
	CLKSRC 6 SB ALINK
CLKREQB#	CLKSRC 2 WLAN
	CLKSRC 4 LOM
CLKREQC#	CLKSRC 0 WWAN
	ATIGCLK 1 NB-PCIEX16
	ATIGCLK 2 NO -USED

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size: Custom | Document Number: Parker | Rev: -1

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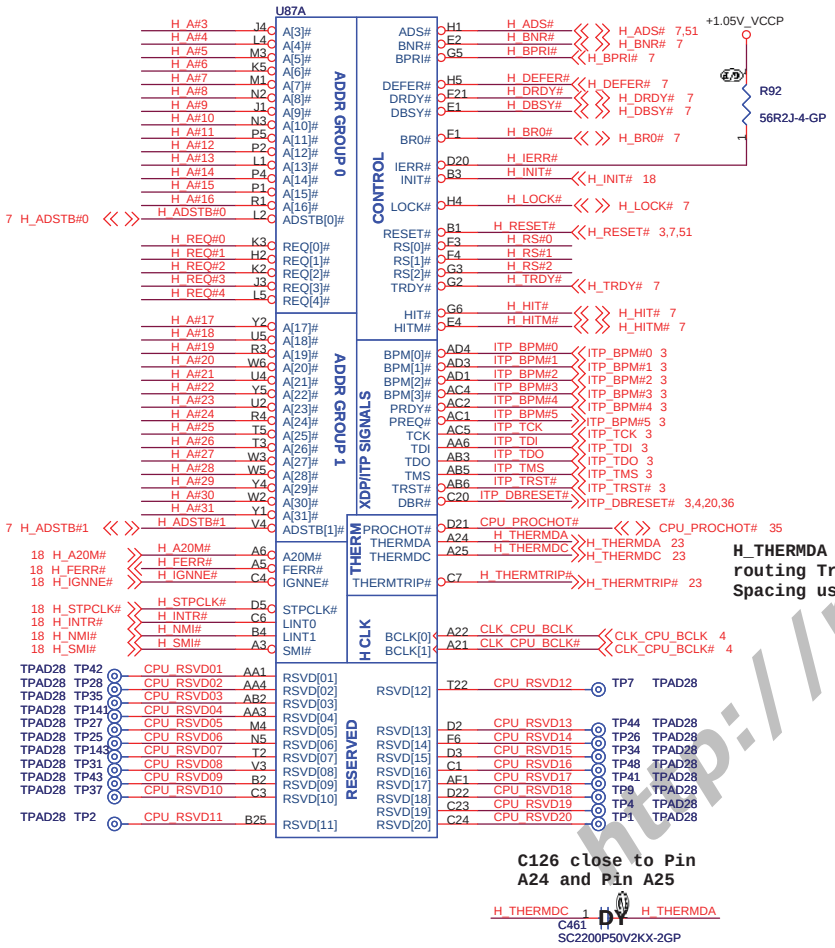
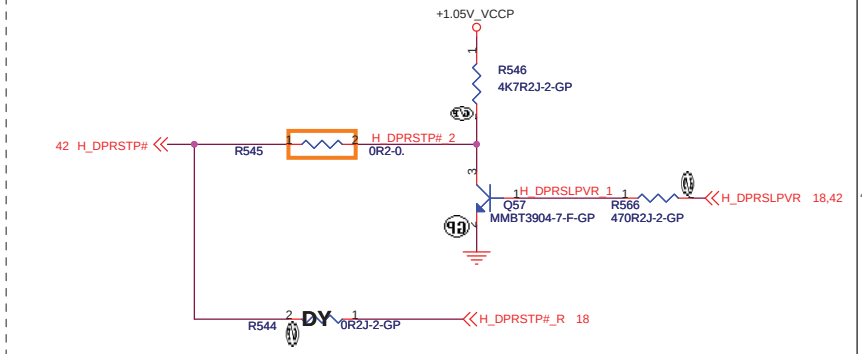
SSID = CPU

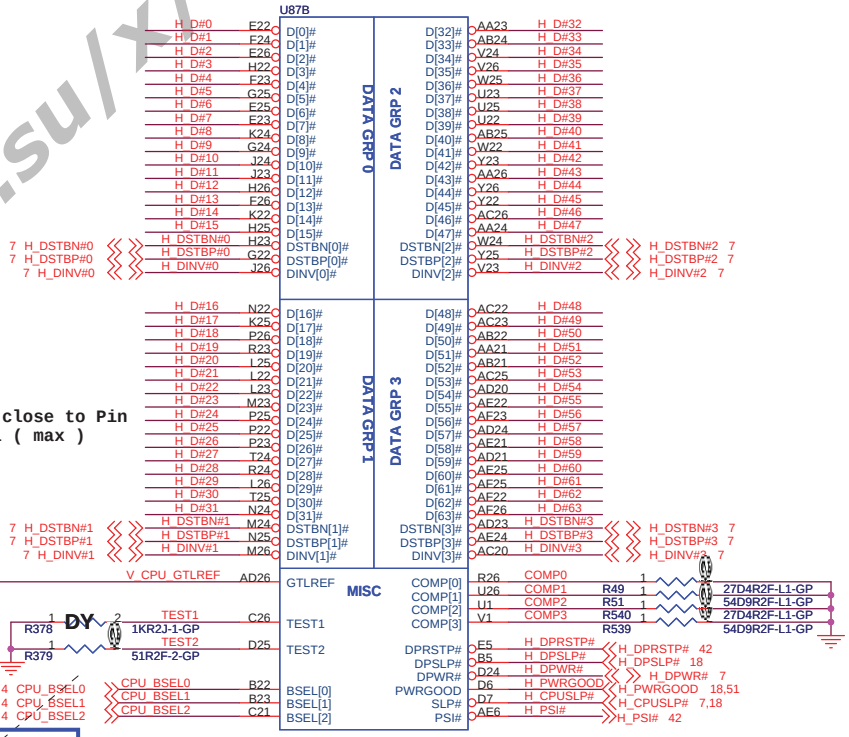
IC CPU YONAH U1500 1.33G BGA--P/N:UP954
IC CPU MEROM U7500 1.06G BGA--P/N:JW602
IC CPU YONAH U1400 1.2G BGA--P/N:FW289



H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

C126 close to Pin A24 and Pin A25





Yonah support

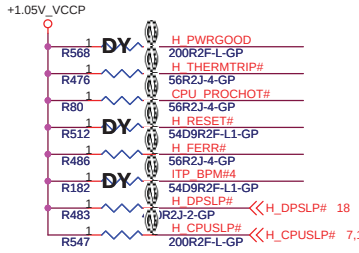
Change R846 to 51 ohm and Populate R843 for Yonah B0 Forward

Parker will use B0 version or later version

This resistor is needed for Yonah but not for Meorm.

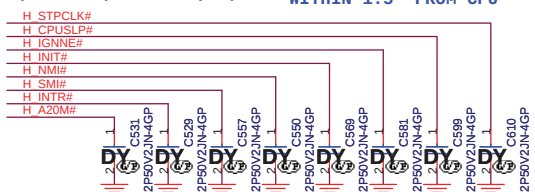
CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.Trace should be No Longer than 500 mils



place cap close cpu pin

THESE CAPS PLACE WITHIN 1.5" FROM CPU



<Variant Name>

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Title: CPU - 01 - Yonah - FSB

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 5 of 53

SSID = CPU

Merom (Dual Core)

All Pop

Yahon (Signal Core)

De-pop C91, 93, 123, 127, 166, 169, 191 and 193

22uF 0805 X5R -> 85 degree C ,
Or better such As X6S and X7R

U87D

U87C

+VCC_CORE

+1.05V_VCCP

+1.5V_RUN

TC7
SE220U2VDM-8GP

H_VID[6..0] 42

VCCSENSE 42

VSSSENSE 42

R473
100R2F-L1-GP-U

R475
100R2F-L1-GP-U

Place R50 and R51 near CPU
Routing VCC_SENSE and VSS_SENSE at
27.4 ohms,50 mils spacing,1 inch.

Please these inside socket cavity on L8 (North side Secondary)

<Variant Name>

Wistron Corporation
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Title: CPU - 02 - Yonah - POWER

Size: A3 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 6 of 53

SSID = N.B

+1.8V_RUN_NB_IOPLLVDD18

200mA

+1.8V_RUN — L20 BLM18BB221SN1D-GP — +1.8V_RUN_NB_IOPLLVDD18 — C168 SC2D2U6D3V3MX-1-GP

Place close pin AA35

+1.2V_RUN_NB_IOPLLVDD12

200mA

+1.2V_RUN — L13 BLM18BB221SN1D-GP — +1.2V_RUN_NB_IOPLLVDD12 — C133 SC2D2U6D3V3MX-1-GP

Place close pin V35

+1.05V_VCCP_NB_CPU_VREF

+1.05V_VCCP — R84 61D9R2F-GP — +1.05V_VCCP_NB_CPU_VREF — R76 127R2F-GP; C43 SC1U6D3V2KX-GP; C44 SC220P50V2JN-3GP

width/space: 10/10

Place close pin A32

NB_TEST_MODE

+3.3V_RUN_NB — R52 4K7R2J-2-GP (DY) — NB_TEST_MODE — R56 4K7R2J-2-GP

TESTMODE	RS600MODE
HIGH	TEST MODE
LOW	NORMAL MODE

NB THERMAL DIODE

CAP close to NB pin

NB_THERMDP — C239 SC2200P50V2KX-2GP (DY) — NB_THERMDN

H_RS#[2..0] — H_RS#[2..0] 5
H_D#[63..0] — H_D#[63..0] 5
H_A#[31..3] — H_A#[31..3] 5
H_REQ#[4..0] — H_REQ#[4..0] 5

U91A 1 0F 7

P-4 AGTL+I/F

ADDR GROUP 0: H_A#3 M42, H_A#4 K42, H_A#5 M44, H_A#6 T39, H_A#7 M38, H_A#8 P42, H_A#9 T43, H_A#10 P38, H_A#11 P44, H_A#12 P36, H_A#13 W39, H_A#14 V40, H_A#15 W42, H_A#16 V42, H_REQ#0 P39, H_REQ#1 M39, H_REQ#2 K44, H_REQ#3 H42, H_REQ#4 K40, H_ADSTB#0 T42 — CPU_A3 … CPU_A16, CPU_REQ0 … CPU_REQ4, CPU_ADSTB0#

5 H_ADSTB#0

ADDR GROUP 1: H_A#17 AC39, H_A#18 W43, H_A#19 V44, H_A#20 V36, H_A#21 AA40, H_A#22 AC43, H_A#23 V38, H_A#24 AA42, H_A#25 AA38, H_A#26 AC42, H_A#27 AD36, H_A#28 AD38, H_A#29 AA36, H_A#30 AD42, H_A#31 AD40, H_A#32 AD44, H_A#33 AD43, H_ADSTB#1 AA44, U46 — CPU_A17 … CPU_A33, CPU_ADSTB1, CPU_RESERVED

TPAD28 TP20, TPAD28 TP21

5 H_ADSTB#1

CONTROL: H_ADS# R46, H_BNR# M47, H_BPRI# H44, H_DEFER# K46, H_DRDY# P45, H_DBSY# M46, H_LOCK# M45, H_RESET# K25, H_RS#2 L45, H_RS#1 R47, H_RS#0 L47, H_BR0# T45, H_TRDY# R45, H_HIT# K47, H_HITM# P46, H_DPWR# T47 — CPU_ADS … CPU_DPWR

5,51 H_ADS#, 5 H_BNR#, 5 H_BPRI#, 5 H_DEFER#, 5 H_DRDY#, 5 H_DBSY#, 5 H_LOCK#, 3,5,51 H_RESET#, 5 H_BR0#, 5 H_TRDY#, 5 H_HIT#, 5 H_HITM#, 5 H_DPWR#

MISC: PM_SUS_STAT# AT9, PLTRST# D10, NB_POWERGOOD F10, NB_CPU_COMP_P B32, NB_CPU_COMP_N A31, NB_THERMDP AT5, NB_THERMDN AT4, IOPLLVDD18 AA35, IOPLLVDD12 V35, IOPLLVSS W35, CPU_SLP# C17, CPU_VREF A32, TESTMODE A20 — SUS_STAT#, SYSRESET#, POWERGOOD, CPU_COMP_P, CPU_COMP_N, THERMALDIODE_P, THERMALDIODE_N

RS600ME-GP

DATA GROUP 0: CPU_D0 H46 … CPU_D15 H45, CPU_DBI0 F47, CPU_DSTB0N E46, CPU_DSTB0P E45 — H_D#0 … H_D#15, H_DINV#0, H_DSTBN#0, H_DSTBP#0

DATA GROUP 1: CPU_D16 E40 … CPU_D31 E34, CPU_DBI1 K36, CPU_DSTB1N J38, CPU_DSTB1P J36 — H_D#16 … H_D#31, H_DINV#1, H_DSTBN#1, H_DSTBP#1

DATA GROUP 2: CPU_D32 J32 … CPU_D47 F25, CPU_DBI2 J30, CPU_DSTB2N H29, CPU_DSTB2P F29 — H_D#32 … H_D#47, H_DINV#2, H_DSTBN#2, H_DSTBP#2

DATA GROUP 3: CPU_D48 C37 … CPU_D63 A36, CPU_DBI3 C34, CPU_DSTB3N B41, CPU_DSTB3P C41 — H_D#48 … H_D#63, H_DINV#3, H_DSTBN#3, H_DSTBP#3

+1.8V_SUS — R170 4K7R2J-2-GP (DY)

+1.8V_RUN — Q18 2N7002-7-FP — R96 1KR2J-1-GP

20 PM_SUS_STAT#, 18,27,31,32,35,45,46,51 PLTRST# — R405 0R2-0.

35,48,51 NB_PWRGD — R99 0R2J-2-GP (DY)

+1.05V_VCCP — R81 53D6R3F-2-GP; R65 21R3F-GP

23 NB_THERMDP, 23 NB_THERMDN

+3.3V_RUN_NB — R82 20KR2J-L2-GP

+1.05V_VCCP — R108 4K7R2J-2-GP — NB_H_CPUSLP# 1 — Q11 MMBT3904-7-F-GP

5,18 H_CPUSLP# — NB_H_CPUSLP#

Q10 MMBT3904-7-F-GP

+1.05V_VCCP — R93 2K2R2J-2-GP — NB_H_CPUSLP# 2

+1.8V_RUN_NB_IOPLLVDD18, +1.2V_RUN_NB_IOPLLVDD12, +1.05V_VCCP_NB_CPU_VREF, NB_TEST_MODE

<Variant Name>

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Title: RS600ME-AGTL(1/5)

Size: A3 | Document Number: Parker | Rev: -1

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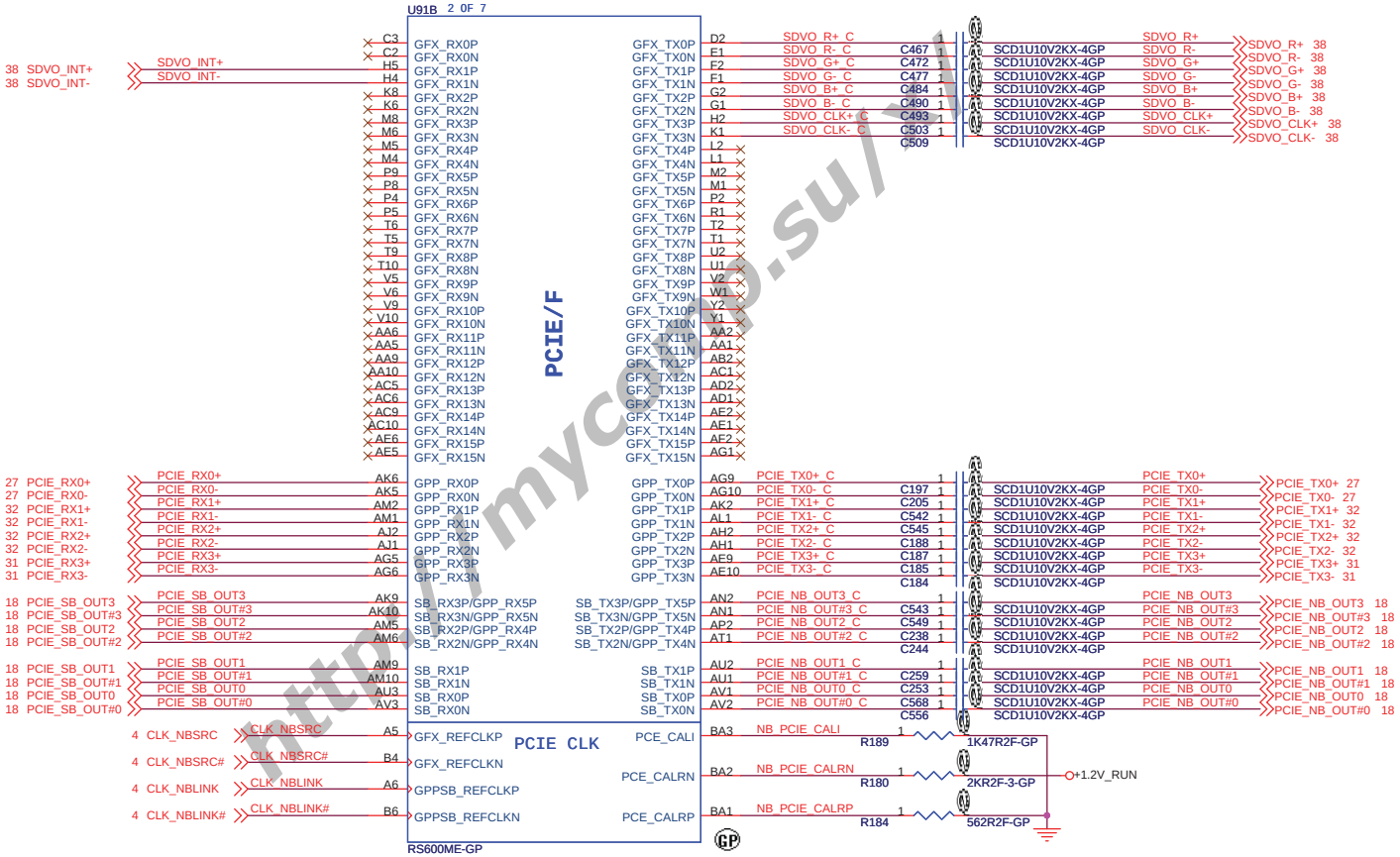
SSID = N.B

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD



<Variant Name>

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Title: RS600ME-ALINK/PCIE-2(2/5)

Size	Document Number	Rev
A3	Parker	-1

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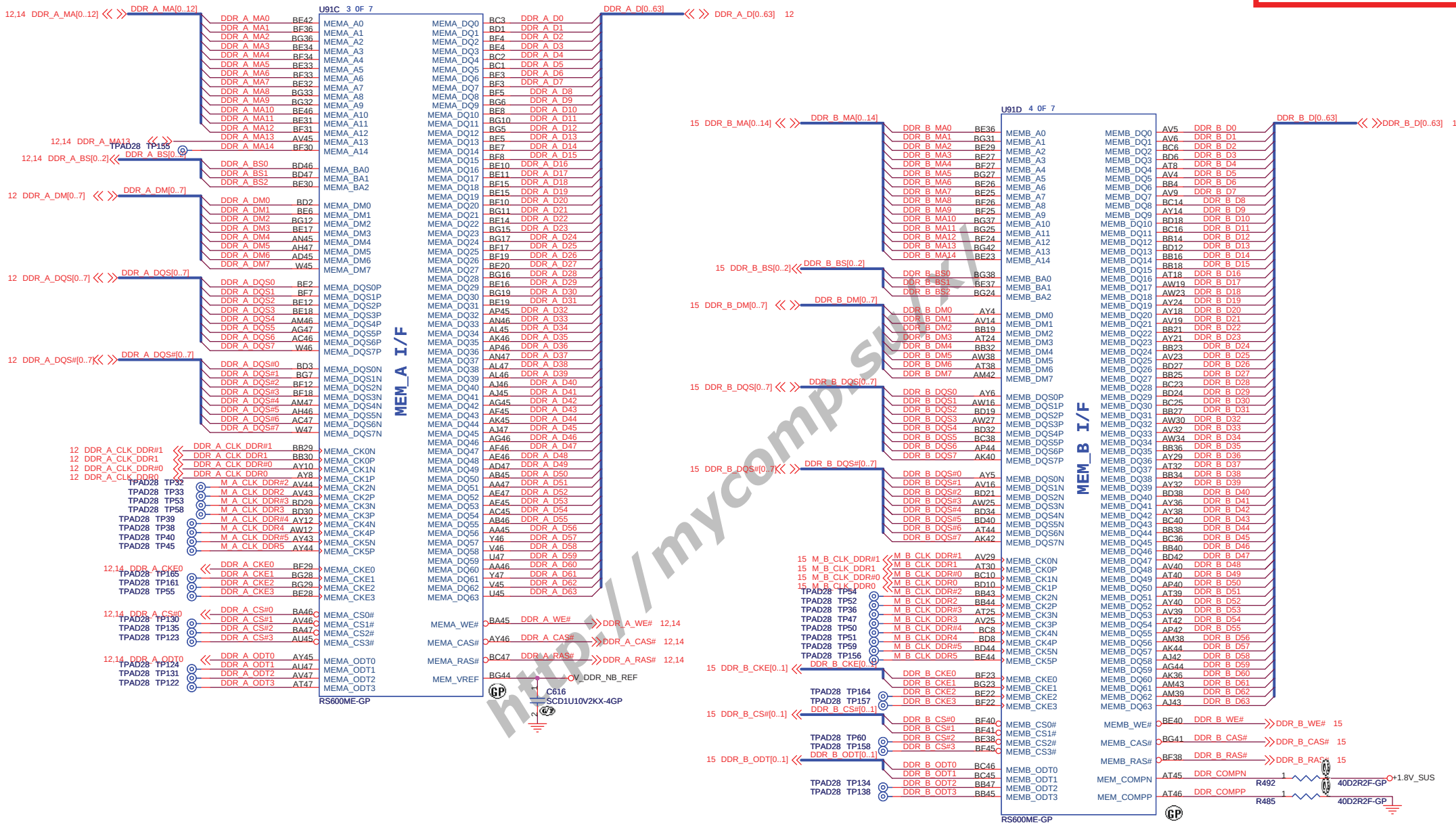
SSID = N.B



<Variant Name>

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Title: RS600ME-MEMORY I/F (3/5)

Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 Sheet 9 of 53

SSID = N.B

NB 3.3V are independent

PUT AT LEAST TWO VIAS
CLOSE TO VDDR3 TWO BALLS
FOR POWER DELIVERY

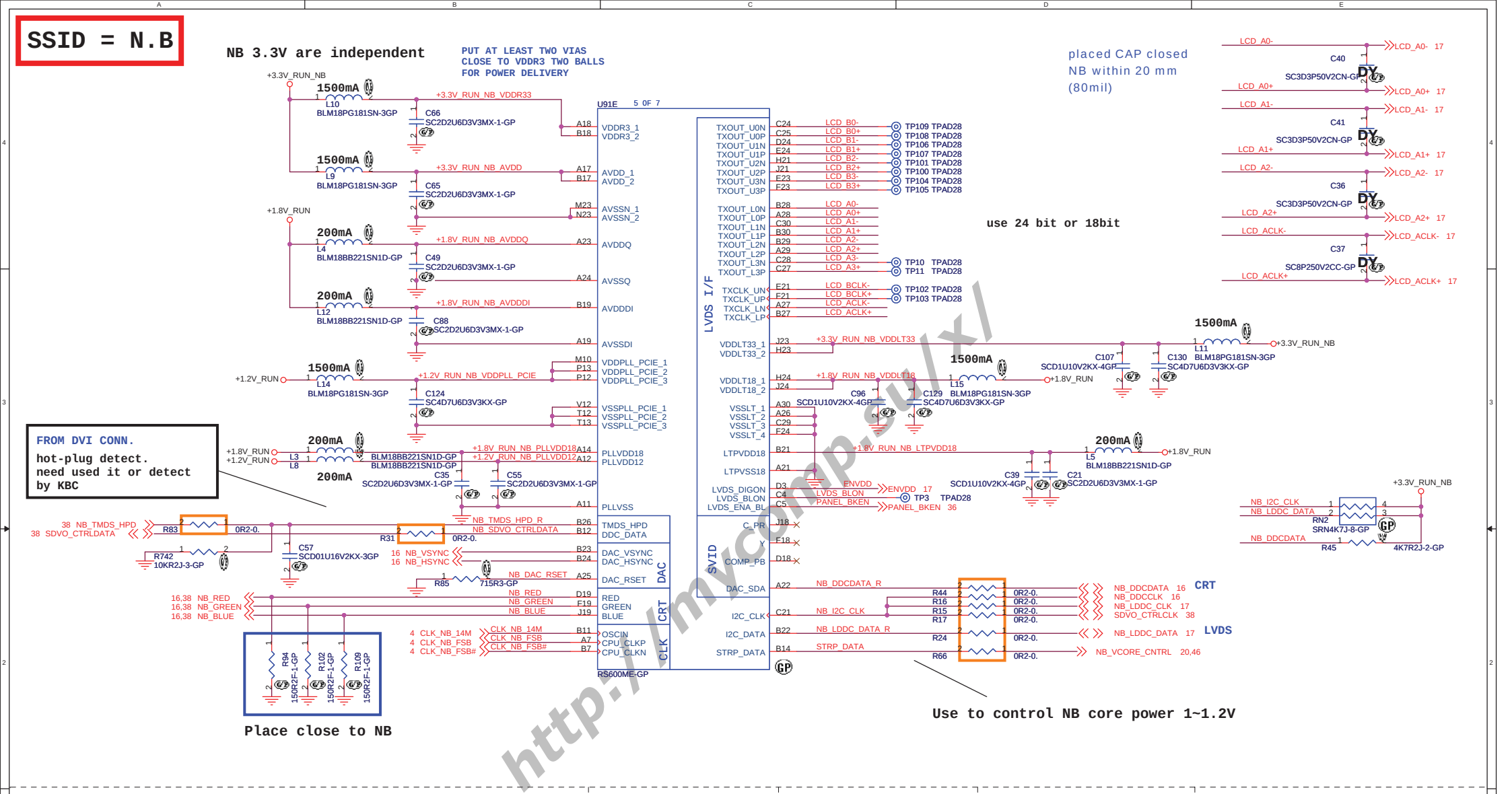
placed CAP closed
NB within 20 mm
(80mil)

use 24 bit or 18bit

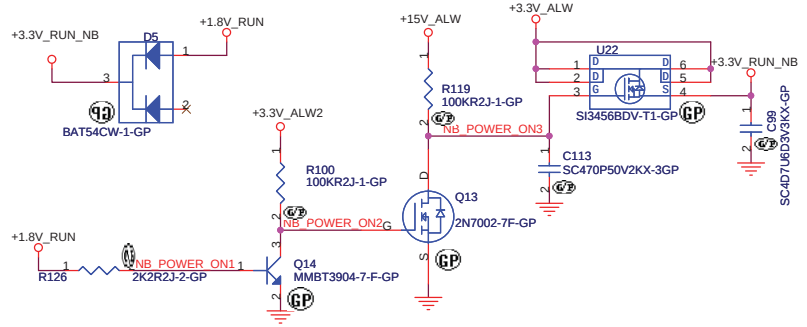
FROM DVI CONN.
hot-plug detect.
need used it or detect
by KBC

Place close to NB

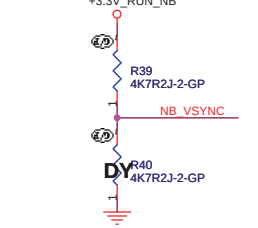
Use to control NB core power 1~1.2V



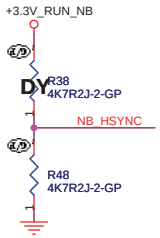
ONLY FOR NB 3.3V POWER



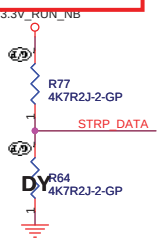
DAC_VSYNC: STRAP_MOBILE_GFX
DEFAULT: 1
0: DESKTOP GRAPHICS DEVICE
1: MOBILE GRAPHICS DEVICE



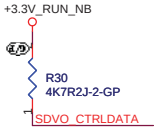
DAC_HSYNC: STRP_INTGFX_DISABLE
DEFAULT: 0
0: ENABLE
1: DISABLE



STRP_DATA: STRP_MEMSTRAPS
DEFAULT: 1
0: SELECT MEMORY CHA A AS DEBUG BUS
1: NORMAL MODE



DDC_DATA: STRAP_MEMVMODE
DEFAULT: 1
0: DDR3
1: DDR2



<Variant Name>

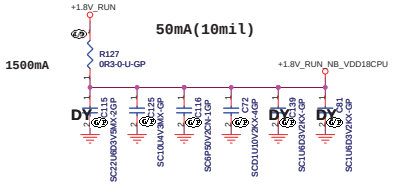
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS600ME-4(4/5)

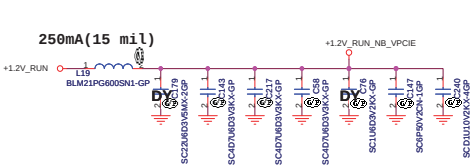
Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 10 of 53

NB-VDD18_CPU DE-COUPLING

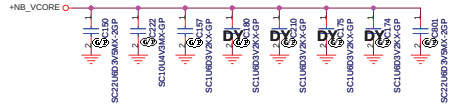


NB-VDD_PCIE DE-COUPLING

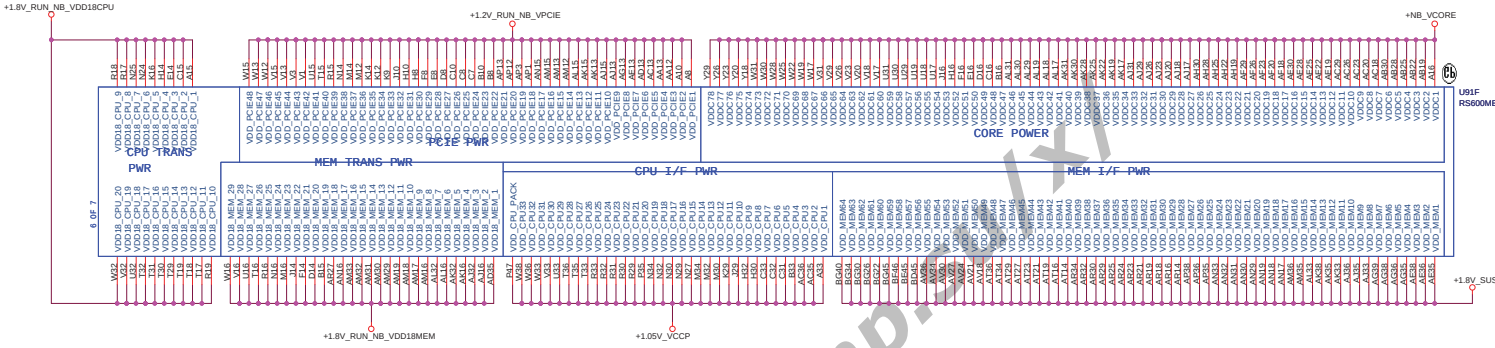


NB-VDDC DE-COUPLING

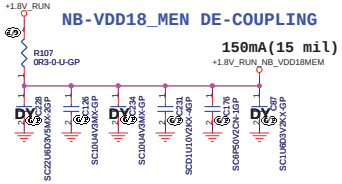
POWER 1V~1.2V 6A(240 mil)



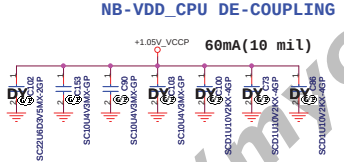
SSID = N.B



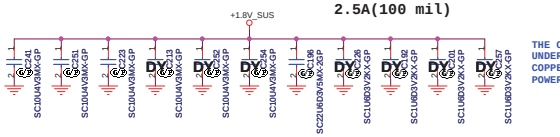
NB-VDD18_MEN DE-COUPLING



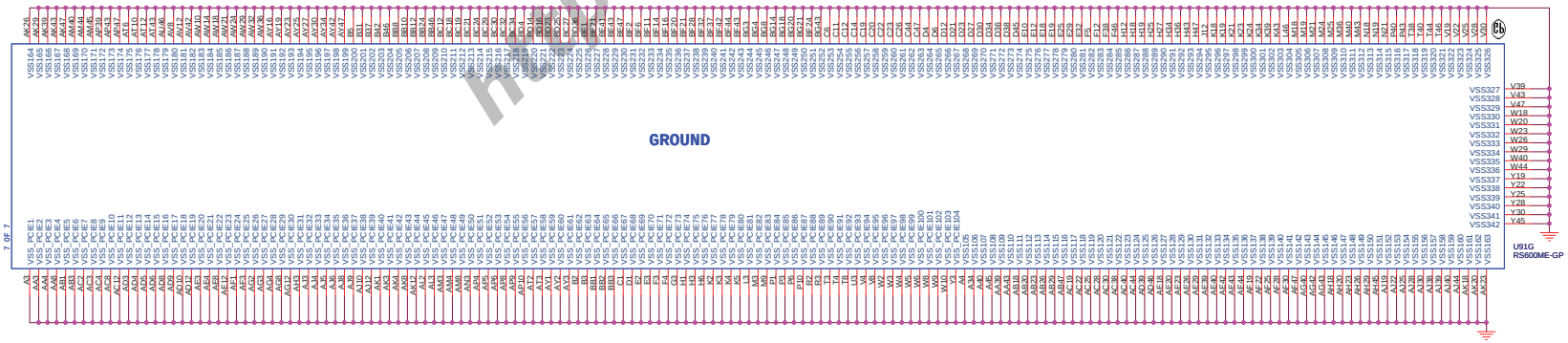
NB-VDD_CPU DE-COUPLING



NB-VDD_MEN DE-COUPLING



THE CAPS HAVE TO BE PLACED UNDER NB. ALL CAPS' GND USE COPPER FLOOD TOGETHER, AND POWER ALSO LIKE THIS WAY.



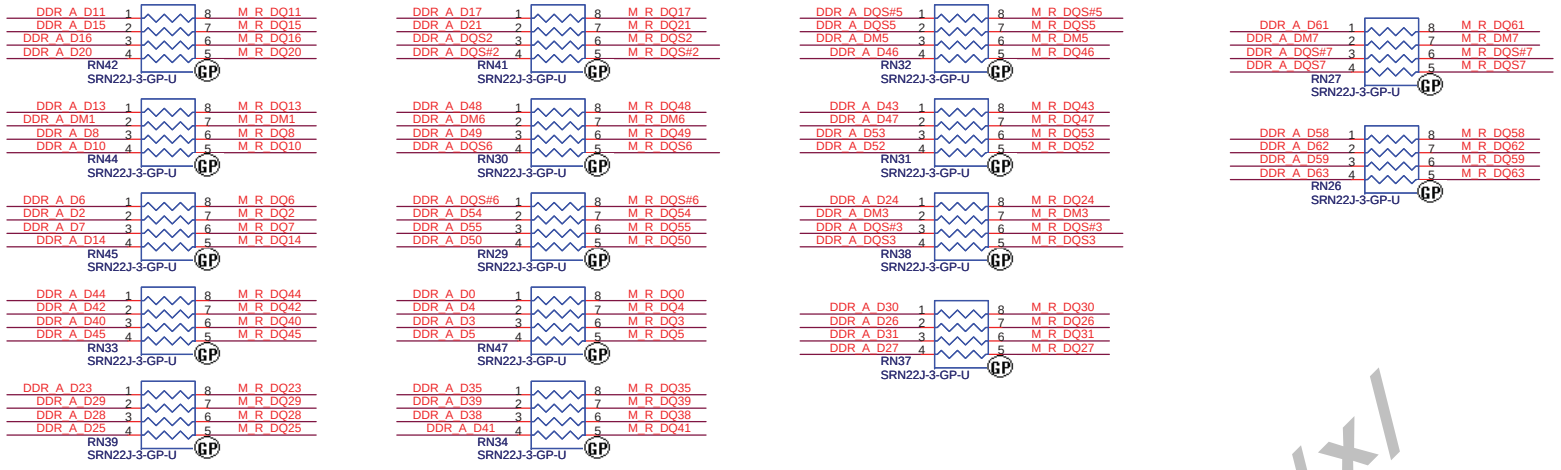
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

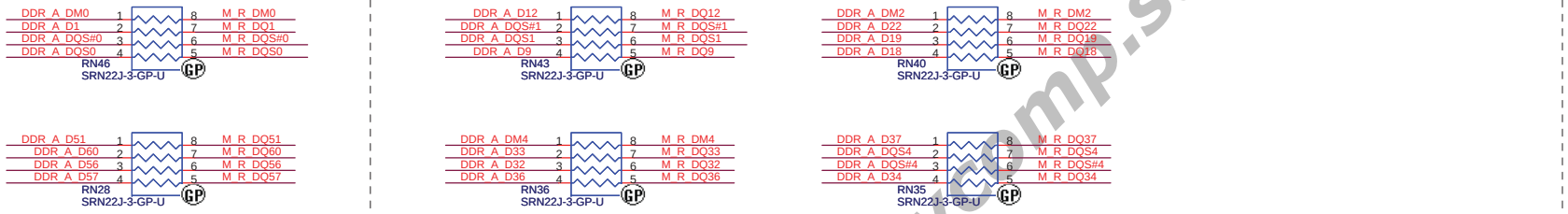
Title: RS600ME-5(5/5)

Size: A2 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 11 of 53



series resistor 22 ohm CHANNEL A DATA



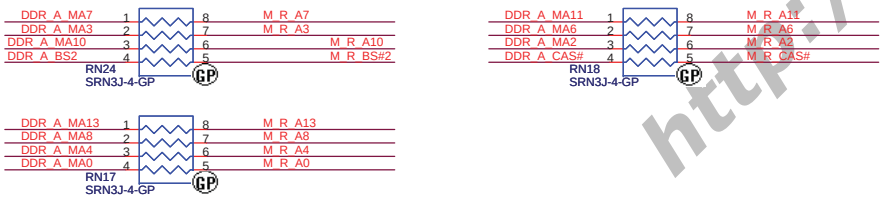
CHANNEL A DATA-MASK
series resistor 22 ohm

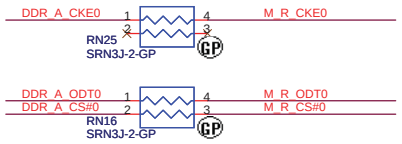
series resistor 22 ohm CHANNEL A DATA-STROBE

CHANNEL A ADDRESS

CHANNEL A COMMAND
RAM CELL ADDRESS 13

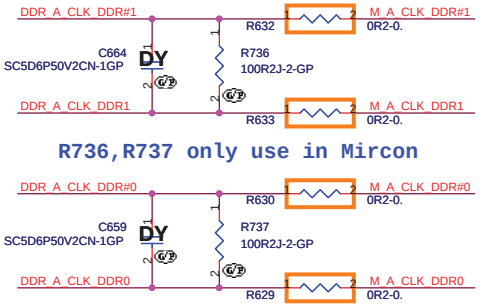
CHANNEL A BANK SELECT





series resistor 3 ohm

series resistor 3 ohm



FROM NB

DDR_A_D[0..63] DDR_A_D[0..63] 9
DDR_A_DM[0..7] DDR_A_DM[0..7] 9
DDR_A_DQS[0..7] DDR_A_DQS[0..7] 9
DDR_A_DQS#[0..7] DDR_A_DQS#[0..7] 9
DDR_A_MA[0..12] DDR_A_MA[0..12] 9,14
DDR_A_BS[0..2] DDR_A_BS[0..2] 9,14

DDR_A_CS#0 DDR_A_CS#0 9,14
DDR_A_RAS# DDR_A_RAS# 9,14
DDR_A_CAS# DDR_A_CAS# 9,14
DDR_A_WE# DDR_A_WE# 9,14
DDR_A_CKE0 DDR_A_CKE0 9,14
DDR_A_ODT0 DDR_A_ODT0 9,14
DDR_A_MA13 DDR_A_MA13 9,14

DDR_A_CLK_DDR#1 DDR_A_CLK_DDR#1 9
DDR_A_CLK_DDR1 DDR_A_CLK_DDR1 9
DDR_A_CLK_DDR#0 DDR_A_CLK_DDR#0 9
DDR_A_CLK_DDR0 DDR_A_CLK_DDR0 9

TO DIMM

M_R_DQ[63..0] M_R_DQ[63..0] 13
M_R_DM[7..0] M_R_DM[7..0] 13
M_R_DQS[7..0] M_R_DQS[7..0] 13
M_R_DQS#[7..0] M_R_DQS#[7..0] 13
M_R_A[12..0] M_R_A[12..0] 13
M_R_BS#[2..0] M_R_BS#[2..0] 13

M_R_CS#0 M_R_CS#0 13
M_R_CAS# M_R_CAS# 13
M_R_RAS# M_R_RAS# 13
M_R_ODT0 M_R_ODT0 13
M_R_CKE0 M_R_CKE0 13
M_R_WE# M_R_WE# 13
M_R_A13 M_R_A13 13

M_A_CLK_DDR#1 M_A_CLK_DDR#1 13
M_A_CLK_DDR1 M_A_CLK_DDR1 13
M_A_CLK_DDR#0 M_A_CLK_DDR#0 13
M_A_CLK_DDR0 M_A_CLK_DDR0 13

SSID = MEMORY

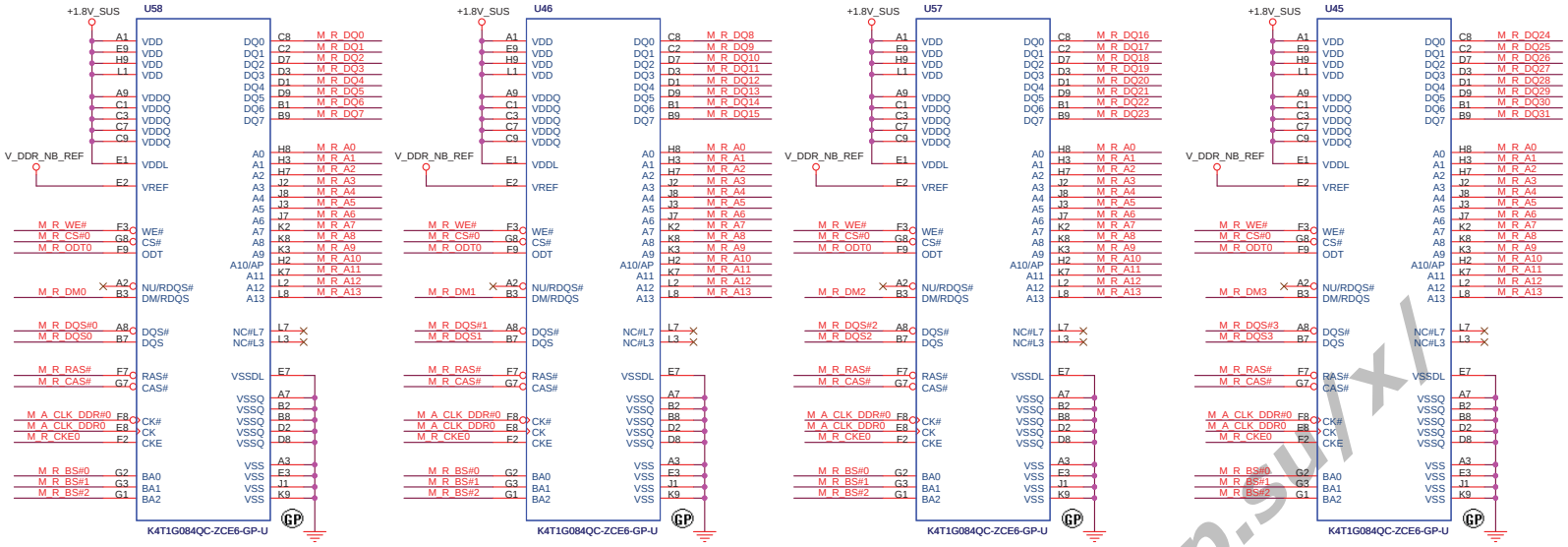
<Variant Name>

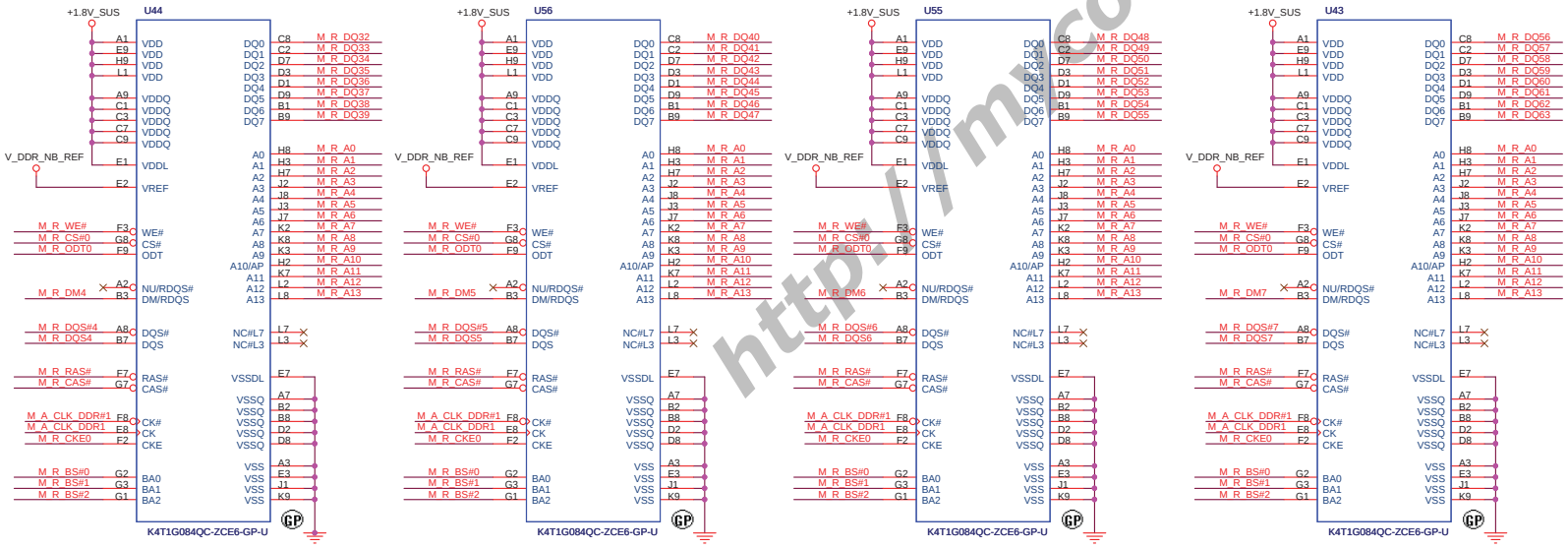
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANNEL A RESISTORS
Size: A3 | Document Number: Parker | Rev: -1
Date: Friday, August 03, 2007 | Sheet 12 of 53

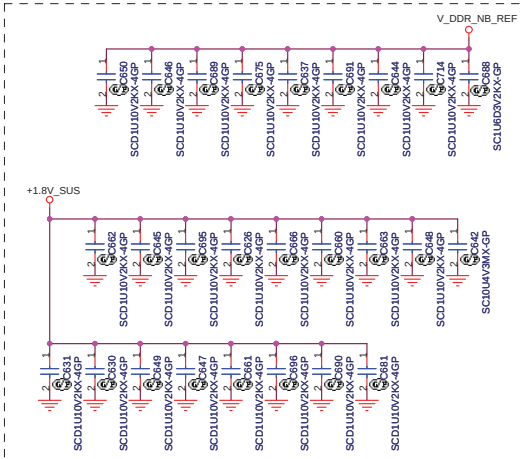
On-board DDR2 Memory

samsung





SSID = MEMORY



Place around the DDR2 chips

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ON BOARD MEMORY**

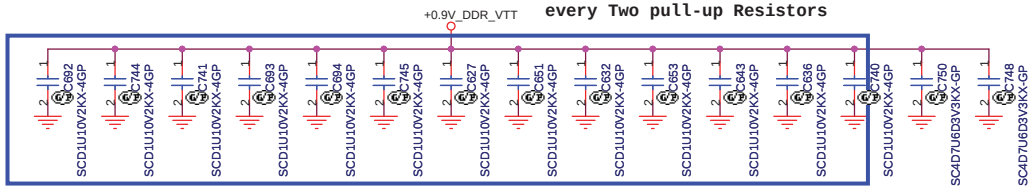
Size	Document Number	Rev
Custom	Parker	-1

Date: Friday, August 03, 2007 Sheet 13 of 53

SSID = MEMORY

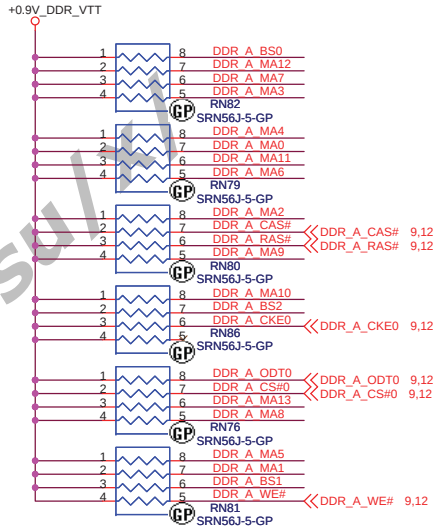
DIMMA-DDR +0.9V_DDR_VTT DE-COUPLING

Please use One Capacitor close to every Two pull-up Resistors



DDR_A_BS[0..2] DDR_A_BS[0..2] 9,12
DDR_A_MA[0..12] DDR_A_MA[0..12] 9,12
DDR_A_MA13 DDR_A_MA13 9,12

ON-BOARD MEMORY TERMINATION



<Variant Name>

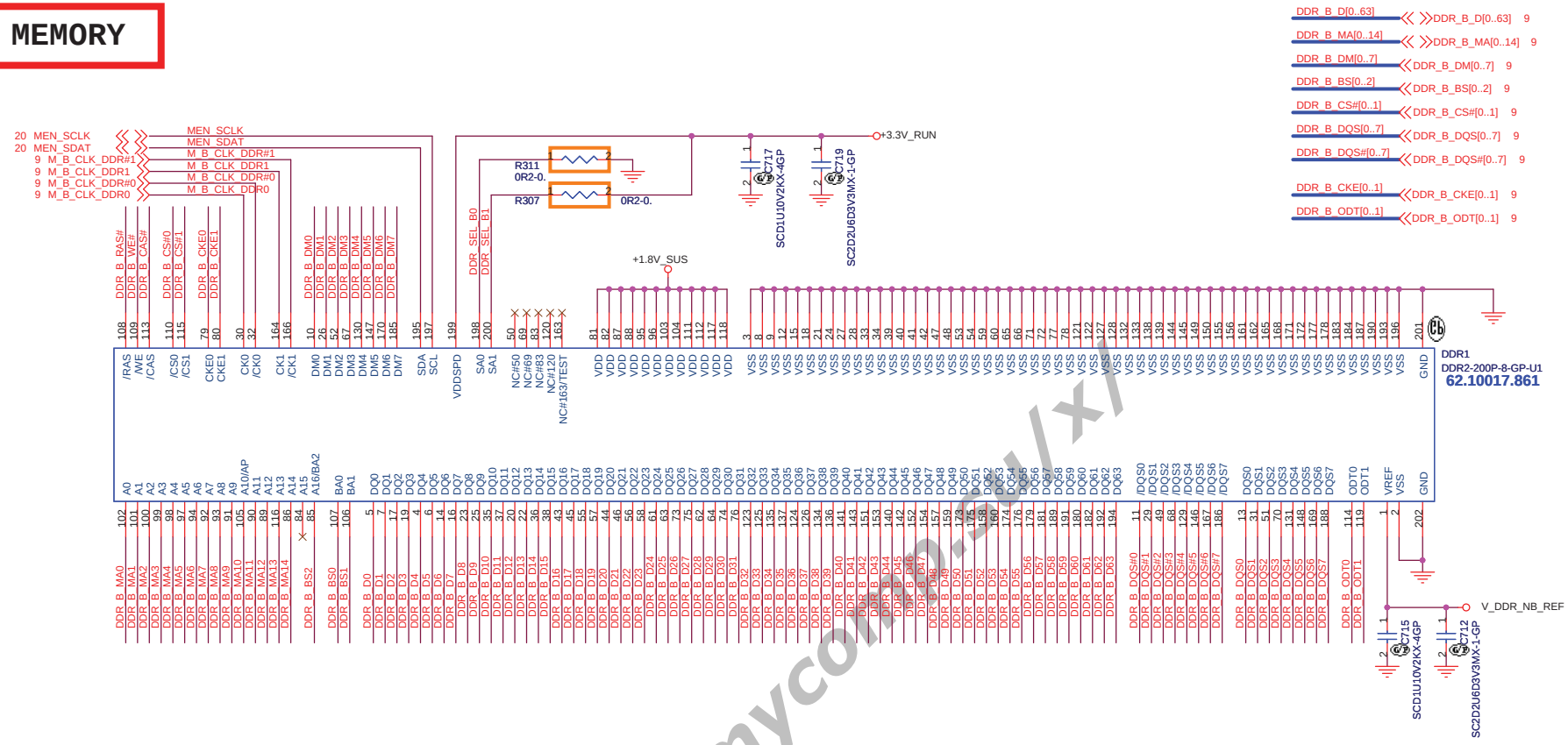
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ON-BOARD MEMORY TERMINATION

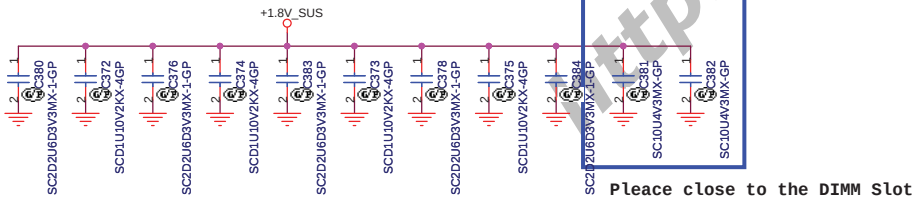
Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 14 of 53

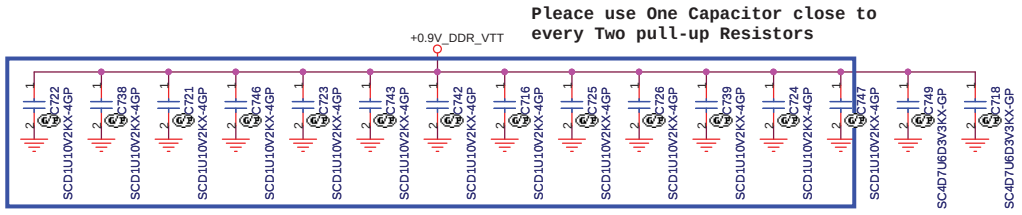
SSID = MEMORY

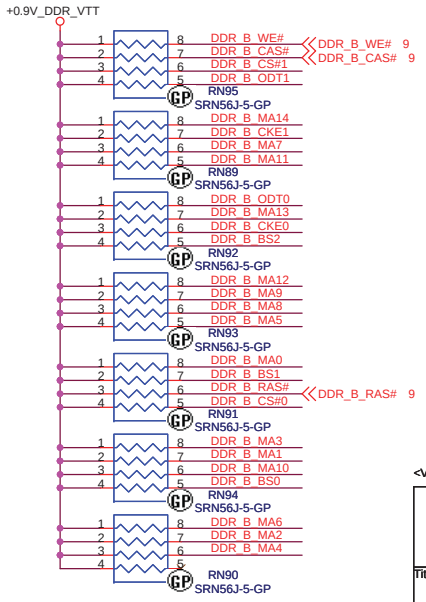


DIMMB-DDR +1.8V_SUS DE-COUPLING



DIMMB-DDR +0.9V_DDR_VTT DE-COUPLING



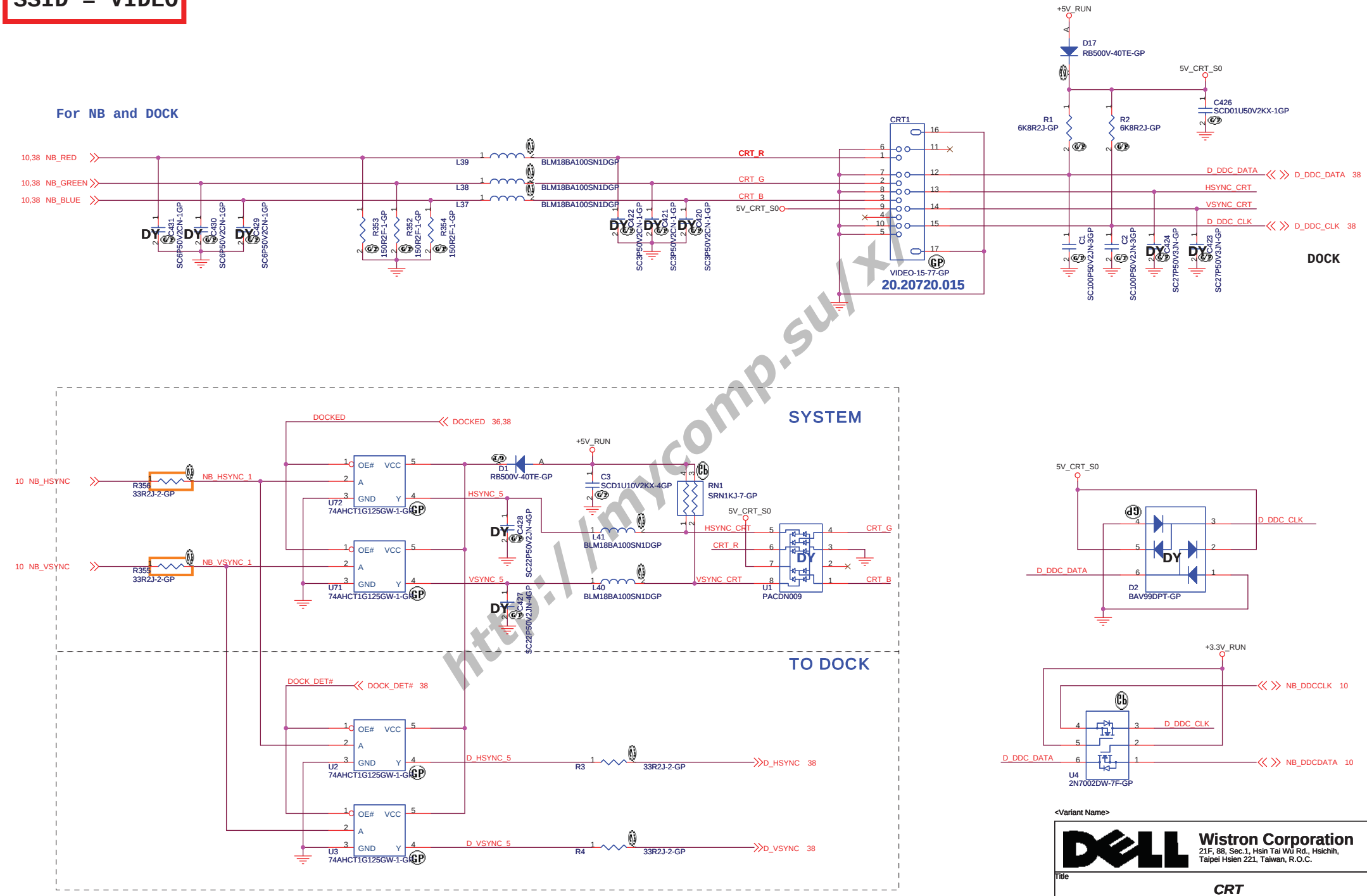


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR-B	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 15 of 53	

SSID = VIDEO

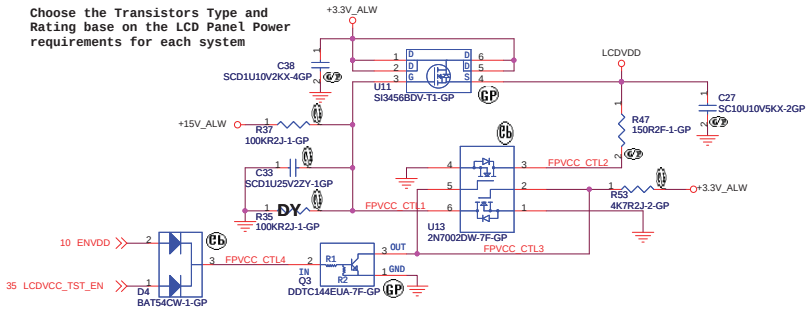


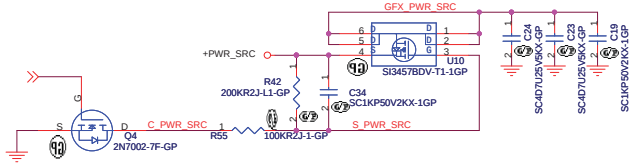
<Variant Name>

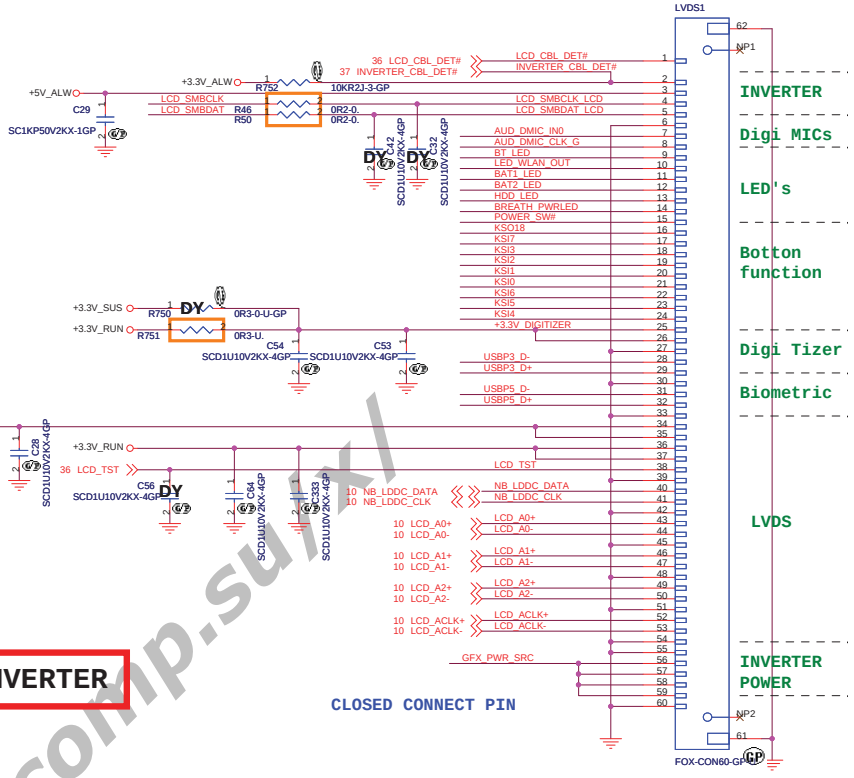
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 16 of 53	

Choose the Transistors Type and Rating base on the LCD Panel Power requirements for each system







SSID = INVERTER

CLOSED CONNECT PIN

20.F1015.060

Digi MICs +3.3V_RUN PLANE

750uA **3 PIN**

29 AUD_DMIC_CLK_G — AUD_DMIC_CLK_G
29 AUD_DMIC_IN0 — AUD_DMIC_IN0

Light Sensor +3.3V_RUN PLANE

2 PIN

35 LCD_SMBCLK — LCD_SMBCLK
35 LCD_SMBDAT — LCD_SMBDAT

maybe use the same SMBUS

Digi Tizer +3.3V_RUN PLANE

2 PIN

20 SB600_USBP3- — R75 0R2-0. — USBP3_D-

20 SB600_USBP3+ — R74 0R2-0. — USBP3_D+

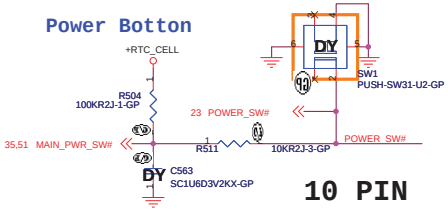
Biometric +3.3V_RUN PLANE

2 PIN

20 SB600_USBP5- — R73 0R2-0. — USBP5_D-

20 SB600_USBP5+ — R72 0R2-0. — USBP5_D+

Power Botton



10 PIN

Ctrl+Del+Alt Botton

37 KSI0 — KSI0

Mobility Center Botton

37 KSI1 — KSI1

User-Programmable Botton

37 KSI2 — KSI2

Screen Rotation Botton

37 KSI3 — KSI3

37 KSO18 — KSO18

Toggle Switch

37 KSI4 — KSI4 — R

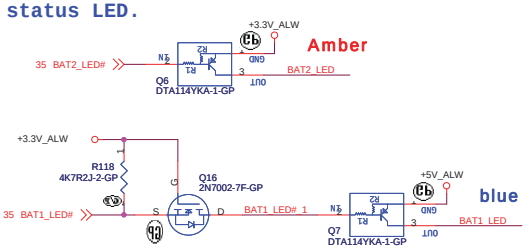
37 KSI5 — KSI5 — L

37 KSI6 — KSI6

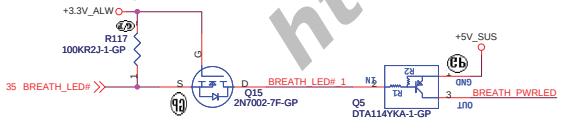
Forward Botton

37 KSI7 — KSI7

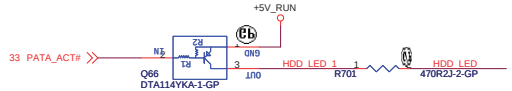
Battery status LED.



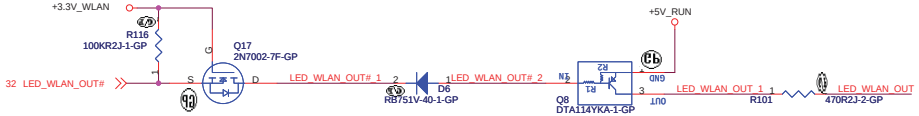
Power & Suspend LED.



HDD activity LED.

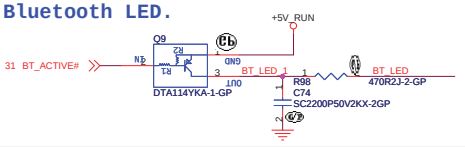


WLAN LED.



6 PIN

Bluetooth LED.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 17 of 53

SSID = S.B

U35A 1 of 4

SB600-GP

Place R160,R155,R156 Close to pin E29,E28,E27<100 mil

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

LPC

CPU

RTC

XTAL

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	G H	1	1

SSID =RBATT

SB_RTC

SB_Xtal

Place Close to pin D2,C1

AND Gate

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-CPU&LPC&PCI&PCIE(1/5)

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 18 of 53

<Variant Name> 20.F0693.003

SSID = S.B

If SATA I/F no used SATA_X1 directly to GND
AVDD_SATA directly to GND
PLLVDD_SATA directly to GND
XTLVDD_SATA directly to GND

U35B 2 of 4

SERIAL ATA

SATA_TX0+ AH21
SATA_TX0- AJ21
SATA_RX0- AH20
SATA_RX0+ AJ20
SATA_TX1+ AH18
SATA_TX1- AJ18
SATA_RX1- AH17
SATA_RX1+ AJ17
SATA_TX2+ AH13
SATA_TX2- AH14
SATA_RX2- AH16
SATA_RX2+ AJ16
SATA_TX3+ AJ11
SATA_TX3- AH11
SATA_RX3- AH12
SATA_RX3+ AJ13

SATA_CAL AE12
SATA_X1 AD16
SATA_X2 AD18
SATA_ACT#/GPIO67 AC12

R602 1KR2F-3-GP DY
SATA_CAL
SATA_XTAL1
SATA_XTAL2

ATA 66/100

IDE_IORDY AB29
IDE_IRQ AA28
IDE_A0 AA29
IDE_A1 AB27
IDE_A2 Y28
IDE_DACK# AB28
IDE_DRQ AC27
IDE_IOR# AC29
IDE_IOW# AC28
IDE_CS1# W28
IDE_CS3# W27

IDE_IORDY 33
INT_IRQ14 33
IDE_A0 33
IDE_A1 33
IDE_A2 33
IDE_DACK# 33
IDE_DREQ 33
IDE_IOR# 33
IDE_IOW# 33
IDE_CS1# 33
IDE_CS3# 33
IDE_D[0..15] 33

IDE_D0/GPIO15 AD28 IDE_D0
IDE_D1/GPIO16 AD26 IDE_D1
IDE_D2/GPIO17 AE29 IDE_D2
IDE_D3/GPIO18 AF27 IDE_D3
IDE_D4/GPIO19 AG29 IDE_D4
IDE_D5/GPIO20 AH28 IDE_D5
IDE_D6/GPIO21 AJ28 IDE_D6
IDE_D7/GPIO22 AJ27 IDE_D7
IDE_D8/GPIO23 AH27 IDE_D8
IDE_D9/GPIO24 AG27 IDE_D9
IDE_D10/GPIO25 AG28 IDE_D10
IDE_D11/GPIO26 AF28 IDE_D11
IDE_D12/GPIO27 AF29 IDE_D12
IDE_D13/GPIO28 AF28 IDE_D13
IDE_D14/GPIO29 AD25 IDE_D14
IDE_D15/GPIO30 AD29 IDE_D15

SB_EC_SPI_DIN_R
C776 SC22P50V2JN-4GP DY

SERIAL ATA POWER

VCC_SATA_PLL
VCC_RUN_SB
200mA
L35 BLM18BB221SN1D-GP
C628 SC1U6D3V2KX-GP DY
R738 0R2-0.

VCC_SATA_XTL
+3.3V_RUN
200mA
L34 BLM18BB221SN1D-GP
R739 0R2-0.

VCC_SATA_SB
VCC_RUN_SB
1500mA
L36 BLM18PG181SN-3GP
C634 SC22U6D3V5MX-2GP DY
C638 SC1U6D3V2KX-GP DY
C640 SC1U6D3V2KX-GP DY
R740 0R2-0.

AVDD_SATA AE14 AE16 AE18 AE19 AF19 AF21 AG22 AG23 AH22 AH23 AJ12 AJ14 AJ19 AJ22 AJ23
PLLVDD_SATA AD14 AJ10
XTLVDD_SATA AC16
AVSS_SATA AB14 AB16 AB18 AC14 AC18 AC19 AD12 AD19 AD21 AE12 AE21 AF11 AF14 AF16 AF18 AG11 AG12 AG13 AG14 AG16 AG17 AG18 AG19 AG20 AG21 AH10 AH19

SPI ROM

SPI_DI/GPIO12 J3
SPI_DO/GPIO11 J6
SPI_CLK/GPIO47 G3
SPI_HOLD#/GPIO31 G2
SPI_CS#/GPIO32 G6

SB_EC_SPI_DIN_R
SB_EC_SPI_DO_R R518 0R2-0.
SB_EC_SPI_CLK_R R529 47R2J-2-GP
SB_SPI_HOLD#_R R514 47R2J-2-GP DY
SB_SPI_CS# R509 0R2J-2-GP

SB_EC_SPI_DIN 35
SB_EC_SPI_DO 35
SB_EC_SPI_CLK 35
SB_SPI_HOLD# 33

LAN_RST#/GPIO13 C23
ROM_RST#/GPIO14 G5

SB_LAN_RST#
SB_ROM_RST#
TP126 TPAD28
TP132 TPAD28

HW MONITOR

FANOUT0/GPIO3 M4
FANOUT1/GPIO48 T3
FANOUT2/GPIO49 V4

PCIE_WLAN_DET#
USB_WLAN_DET#
PCIE_WLAN_DET# 32
USB_WLAN_DET# 32

WLAN

FANIN0/GPIO50 N3
FANIN1/GPIO51 P2
FANIN2/GPIO52 W4

PCIE_WWAN_DET#
USB_WWAN_DET#
PCIE_WWAN_DET# 32
USB_WWAN_DET# 32

WWAN

TEMP_COMM P5
TEMPIN0/GPIO61 P7
TEMPIN1/GPIO62 P8
TEMPIN2/GPIO63 T8
TEMPIN3/TALERT#/GPIO64 T7

SB_TEMP_COMM
TP151 TPAD28
AUD_SPK_DET#
AUD_SPK_DET# 30
RTC_BAT_DET# 18
MINI3_CLK_REQ#
R543 10KR2J-3-GP
+3.3V_RUN

VIN0/GPIO53 V5
VIN1/GPIO54 L7
VIN2/GPIO55 M8
VIN3/GPIO56 V6
VIN4/GPIO57 M6
VIN5/GPIO58 P4
VIN6/GPIO59 M7
VIN7/GPIO60 V7

SB_WWAN_PCIE_RST# 32
SB_WLAN_PCIE_RST# 32
SB_LOM_PCIE_RST# 27
NC_GPIO56
MEM_VEND_ID1
MEM_VEND_ID1 36
LBF_ID1
LBF_ID2
TP148 TPAD28
TP145 TPAD28
ALT_TP_DET#
R563 10KR2J-3-GP
+3.3V_RUN
R585 20KR2J-L2-GP
R533 20KR2J-L2-GP
R522 20KR2J-L2-GP
R589 20KR2J-L2-GP

BIOS should not enable the internal GPIO pull up resistor

+3.3V_RUN_HW
AVDD N1
AVSS M1
200mA
L27 BLM18BB221SN1D-GP
+3.3V_RUN
C276 SCD1U10V2KX-4GP
C275 SC2D2U6D3V3MX-1-GP
R186 0R3-U.
HW_AGND

Place R175 close to SB600
HWM AGND trace at least 10 mil wide

SB600-GP

SATA_Xtal

SATA_XTAL3 R247 0R2J-2-GP SATA_XTAL1
R244 10MR2J-L-GP SATA_XTAL2
X3 XTAL-25MHZ-72GP
C332 SC10P50V2JN-4GP DY
C323 SC10P50V2JN-4GP DY

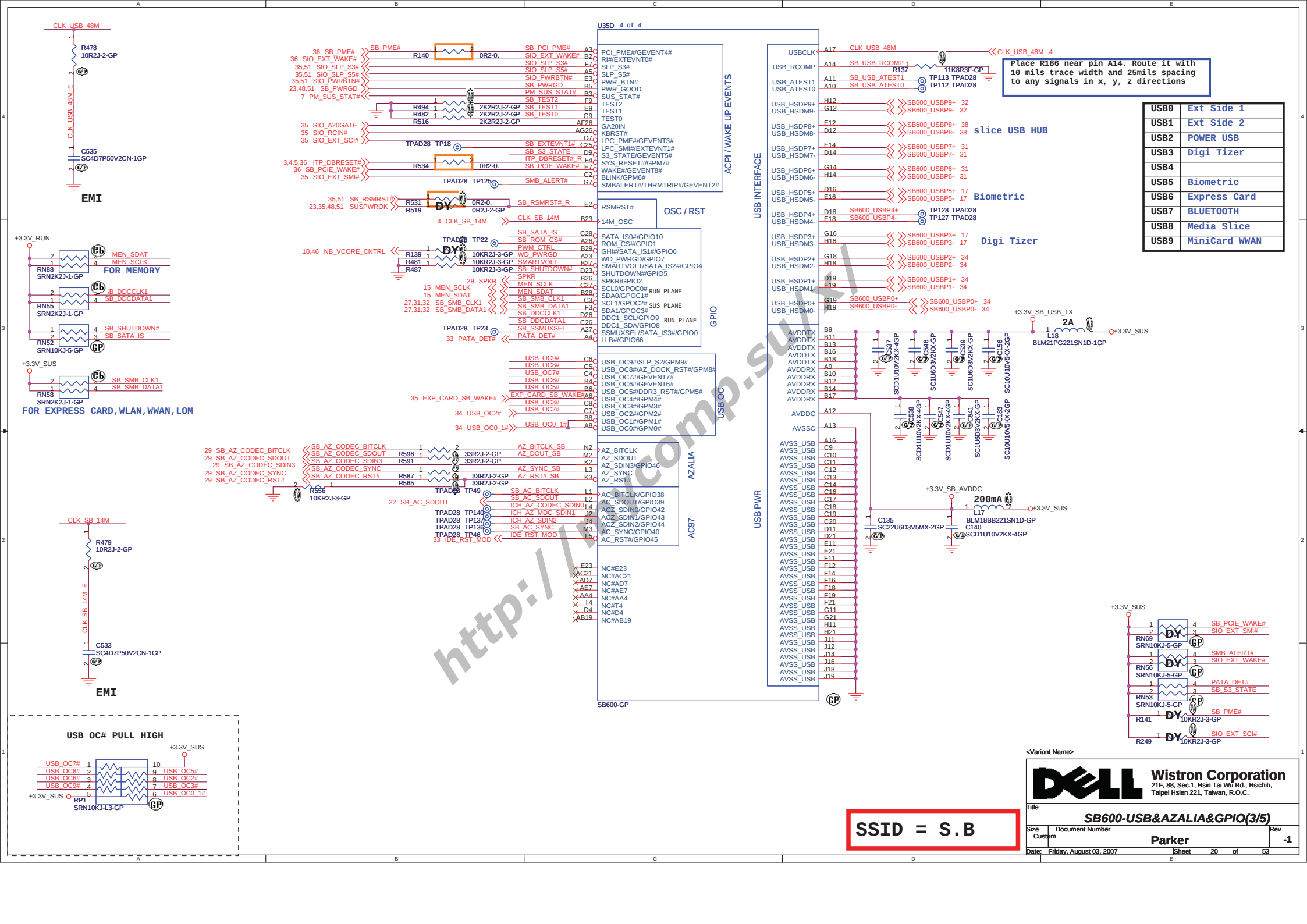
AND Gate

+3.3V_SUS
R484 1KR2J-1-GP
SB_SPI_CS#
35 SIO_SPI_CS#
R445 47R2J-2-GP
+3.3V_ALW
C499 SCD1U10V2KX-4GP DY
SPI_CS#_R
R436 15R2J-GP DY
SPI_CS# 33
U84 74AHC1G08GW-GP-U

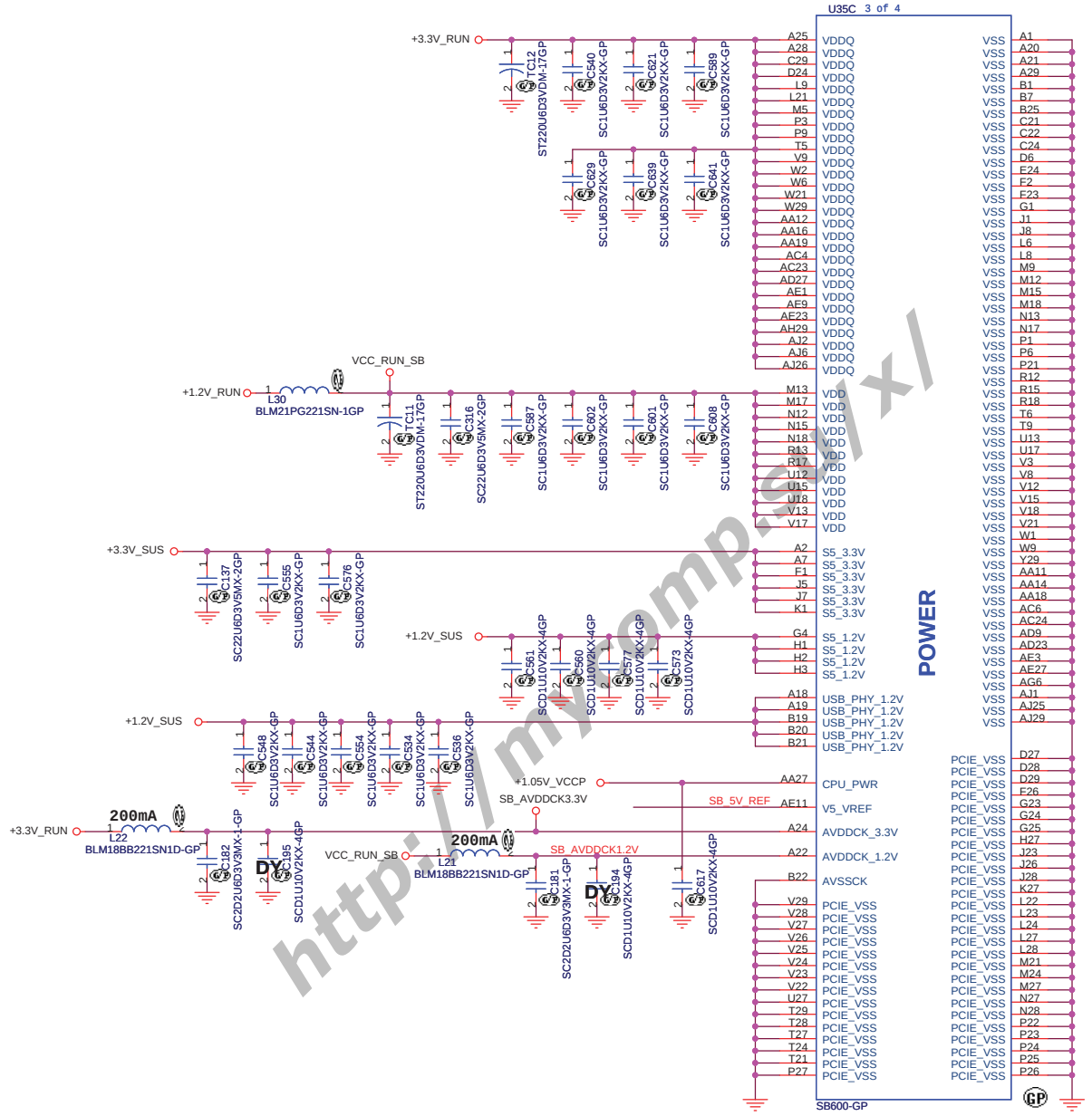
<Variant Name>

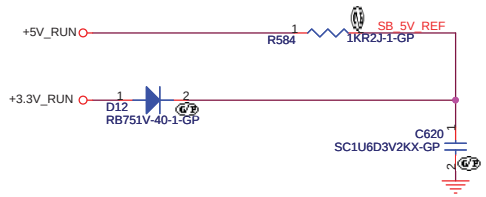
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-IDE&SATA$SPI(2/5)
Size: A3
Document Number: Parker
Rev: -1
Date: Tuesday, August 14, 2007
Sheet 19 of 53



SSID = S.B





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-Power(4/5)

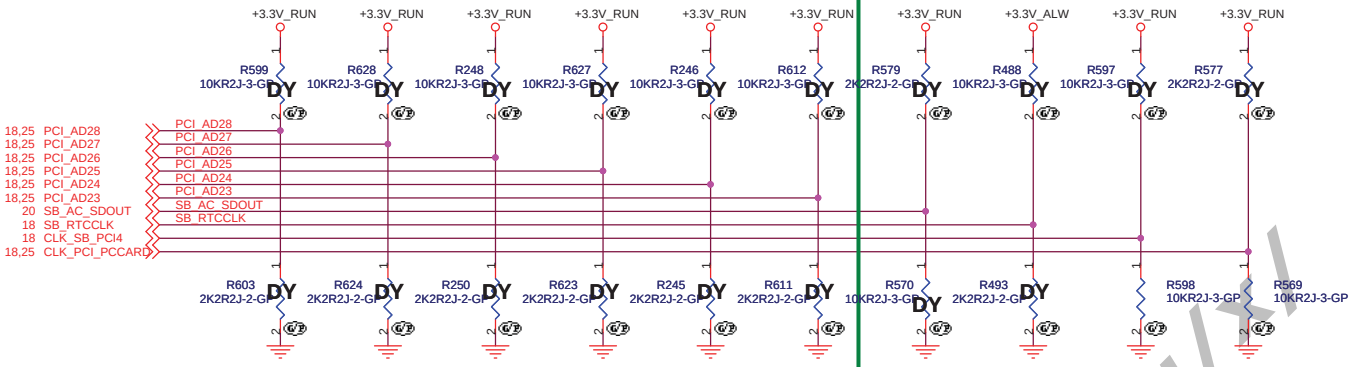
Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 21 of 53

Debug Straps

SSID = S.B

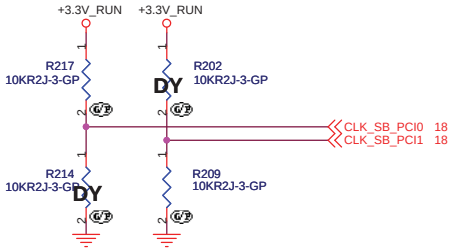
Standard Straps



CLK_SB_PCI4

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6
HIGH	LONG RESET Default	PCI PLL Default	ACPI BCLK Default	IDE PLL Default	DEFAULT PCIE STRAPS Default	BOOTFAIL TIMER DISABLED Default	DEBUG STRAPS	INTERNAL RTC Default	INTERNAL PLL48	AMD CPU
LOW	SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED	IGNORE DEBUG STRAPS Default	EXTERNAL RTC	EXTERNAL 48MHZ Default	INTEL CPU Default

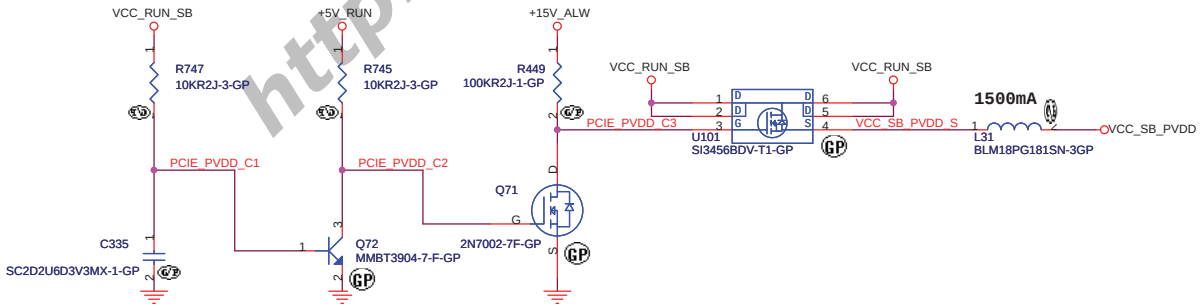
CLK_PCI_PCCARD



CLK_SB_PCI0

PCI_CLK0	PCI_CLK1	ROM TYPE	
0	0	FWH	
0	1	LPC	
1	0	SPI	Default
1	1	PCI	

CLK_SB_PCI1



<Variant Name>

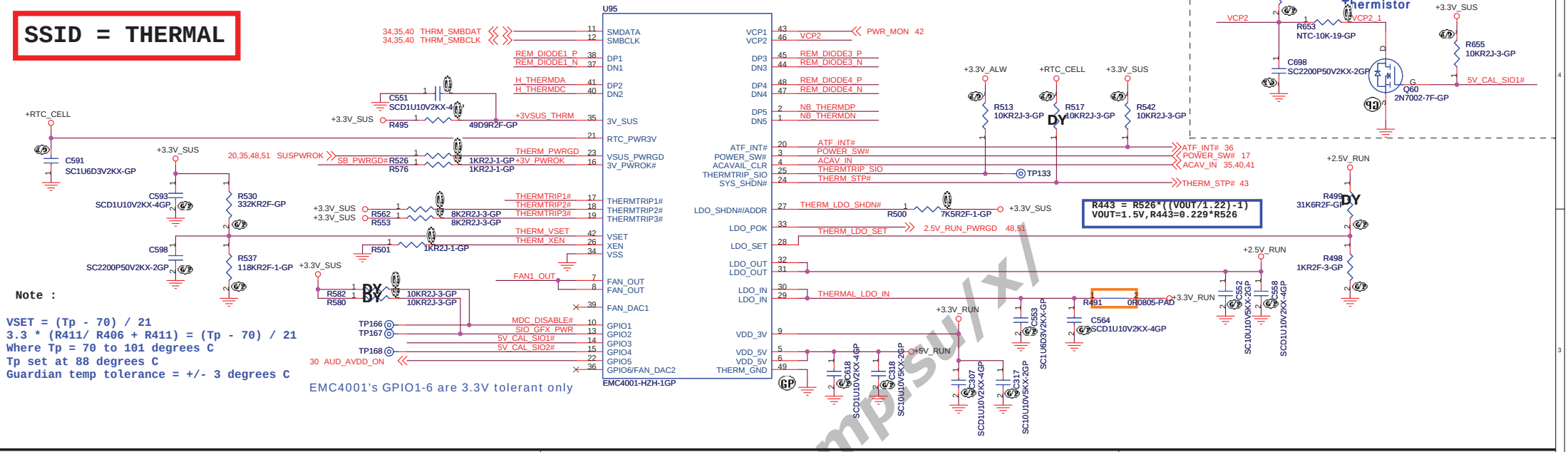
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *SB600-Strapping Pin(5/5)*

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 22 of 53

SSID = THERMAL



Note :

VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

EMC4001's GPIO1-6 are 3.3V tolerant only

R443 = R526*((VOUT/1.22)-1)
VOUT=1.5V,R443=0.229*R526

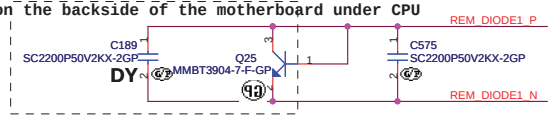
Placement should be near the WWAN minicard connector just under the inserted minicard.

Thermal sensor for CPU D1

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Locate C350 near Guardian

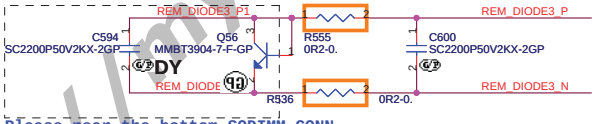
place on the backside of the motherboard under CPU



Thermal sensor for SODIMM D3

REM_DIODE3_N and REM_DIODE3_P routing Trace width and Spacing use 10 / 10 mil

Locate C351 near Guardian



Please near the bottom SODIMM CONN

Thermal sensor for RS600ME D5

NB_THERMDA and NB_THERMDC routing Trace width and Spacing use 10 / 10 mil

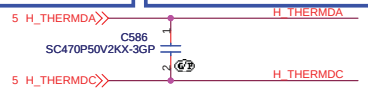
Locate C368 near Guardian

Reserve area near NB for a cap between DP4/DN4

Thermal sensor for CPU DIODE D2

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

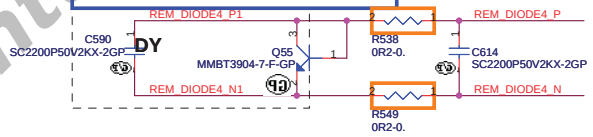
Locate C352 near Guardian



Thermal sensor for skin temp D4

REM_DIODE4_N and REM_DIODE4_P routing Trace width and Spacing use 10 / 10 mil

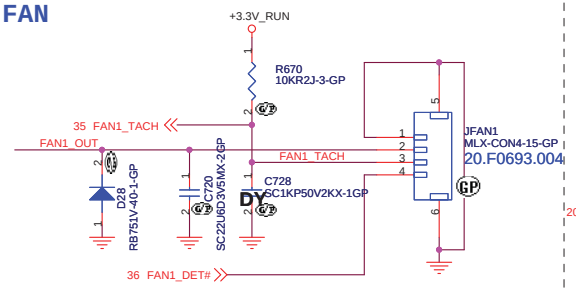
Locate C355 near Guardian



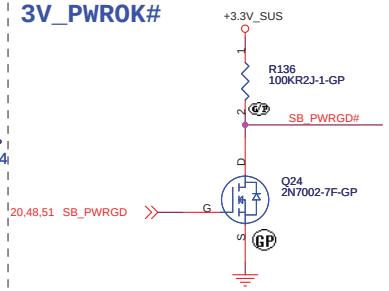
Thermal sensor mapping

D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

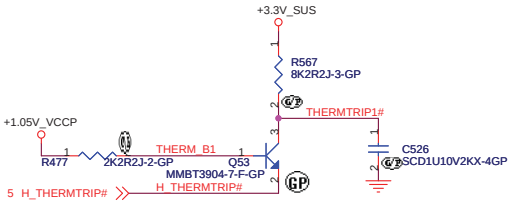
FAN



3V_PWROK#



CPU THERMALTRIP



<Variant Name>

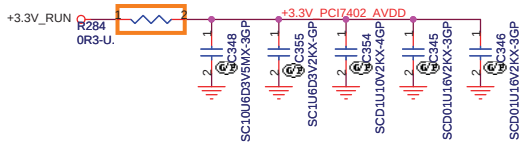
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN, EMC4001

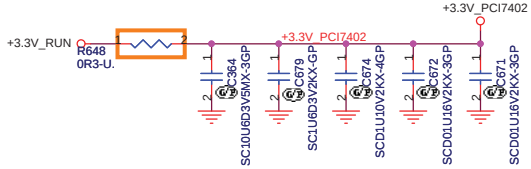
Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 23 of 53

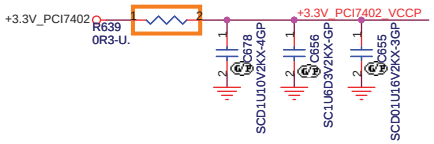
PCI7402_AVDD_33



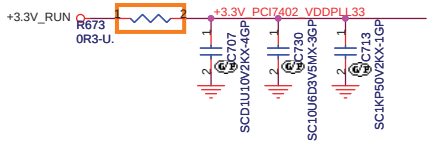
PCI7402_VCC



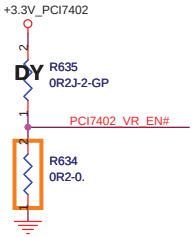
PCI7402_VCCP



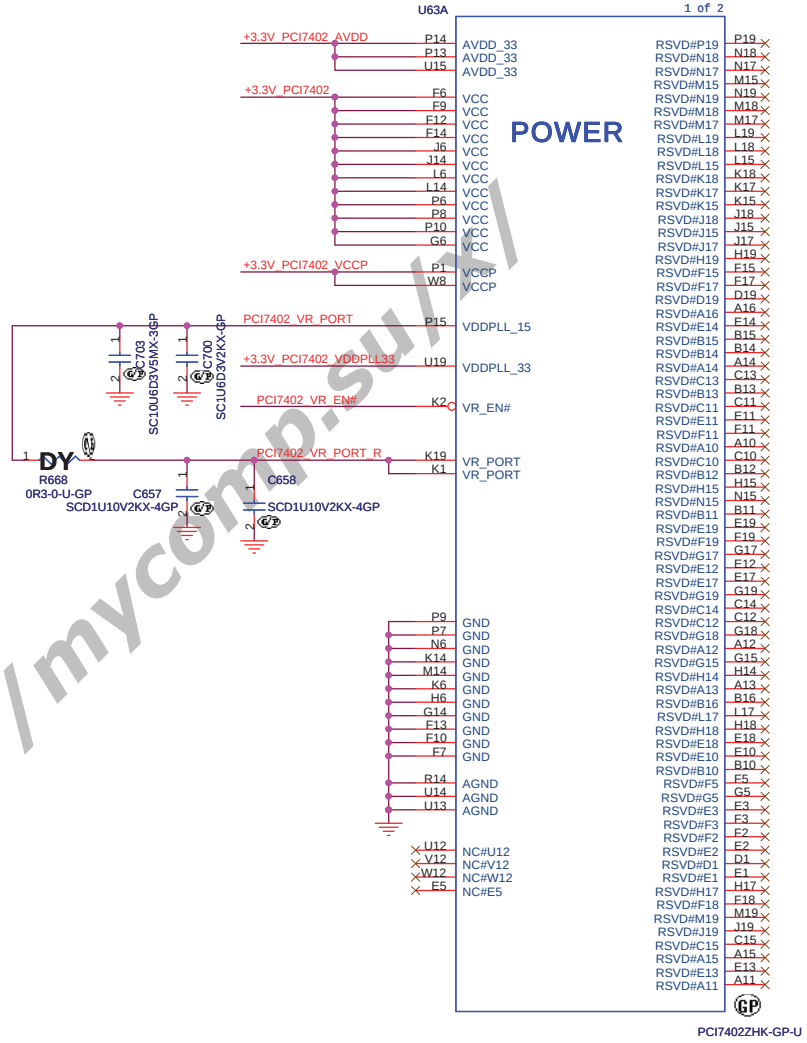
PCI7402_VDDPLL33



PCI7402_VR_EN#



SSID = 1394

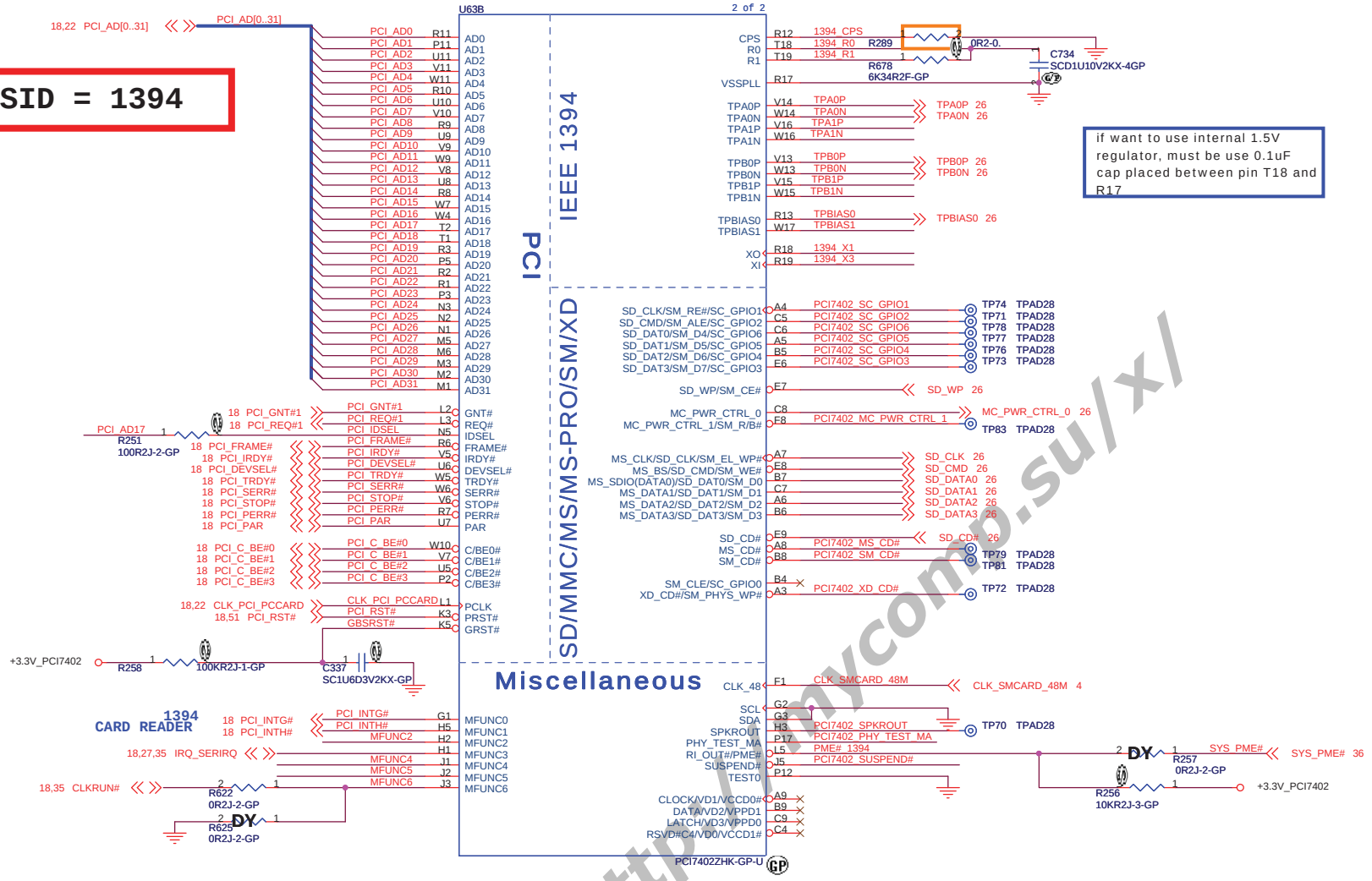


<Variant Name>

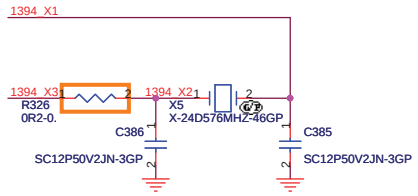
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCI7402-1	
Size: A3	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 24 of 53	

SSID = 1394

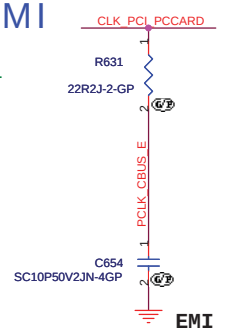


1394 Xtal



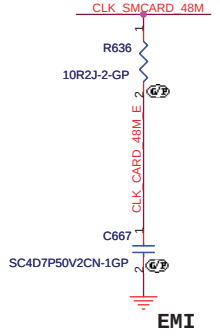
PCI-CLK EMI

CLOSE TO PIN L1



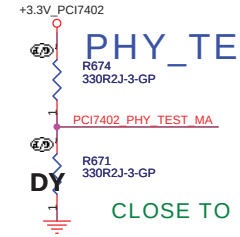
CLK 48M EMI

CLOSE TO PIN F1



MEDIA SLICE 1394

PHY_TEST_MA



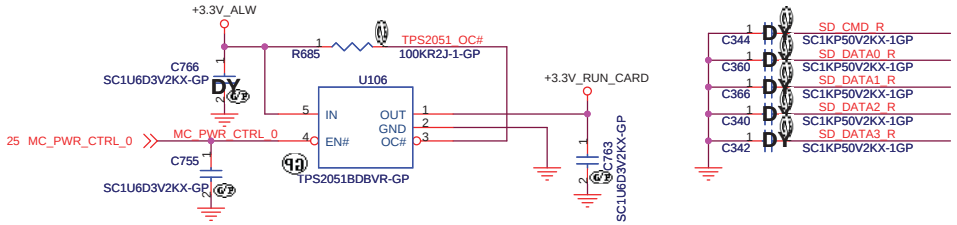
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

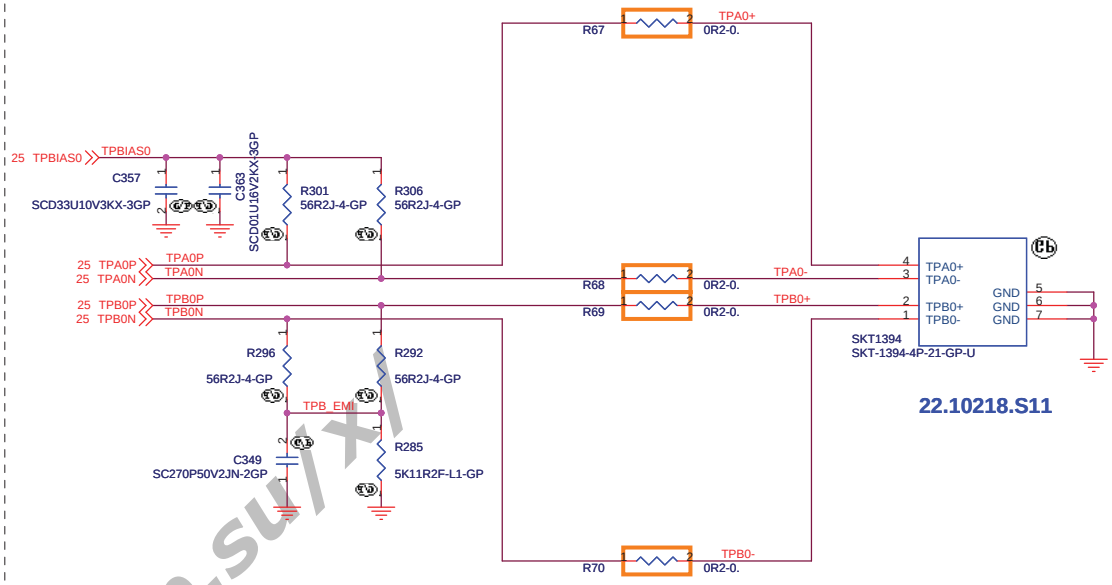
Title	PCI7402-2	
Size A3	Document Number Parker	Rev -1
Date: Tuesday, August 14, 2007	Sheet 25 of 53	

SD POWER-SWITCH

SSID = 1394

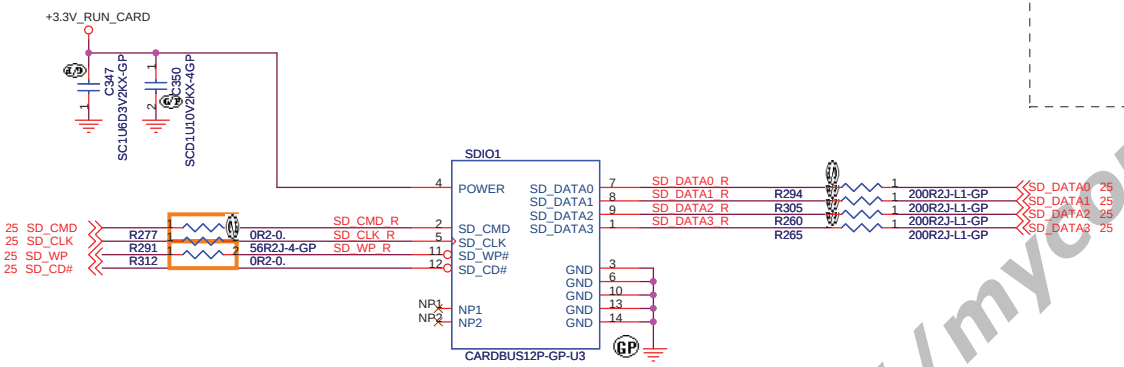


M/B 1394



22.10218.S11

SD SOCKET



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMART CARD/SD/1394(3/3)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 26 of 53

SSID = LOM

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Closed to pin E4, J3, D6, G8

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Monitor GPHY PLL Clk

Populate resister for debug

Place resister as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for bath footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

Place crystal less than 0.75" (~1.9cm) from LAN Controller

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

Logic High Voltage must be 0.7V to 2.75V

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.

VDDIOPower Decoupling

Core Power Decoupling

VDDP Power Decoupling

place C937 near U91 pin L11

Place high-freqency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side ofthe cap to the ground via should also be minimized.

Reserve for EMI

<Variant Name>

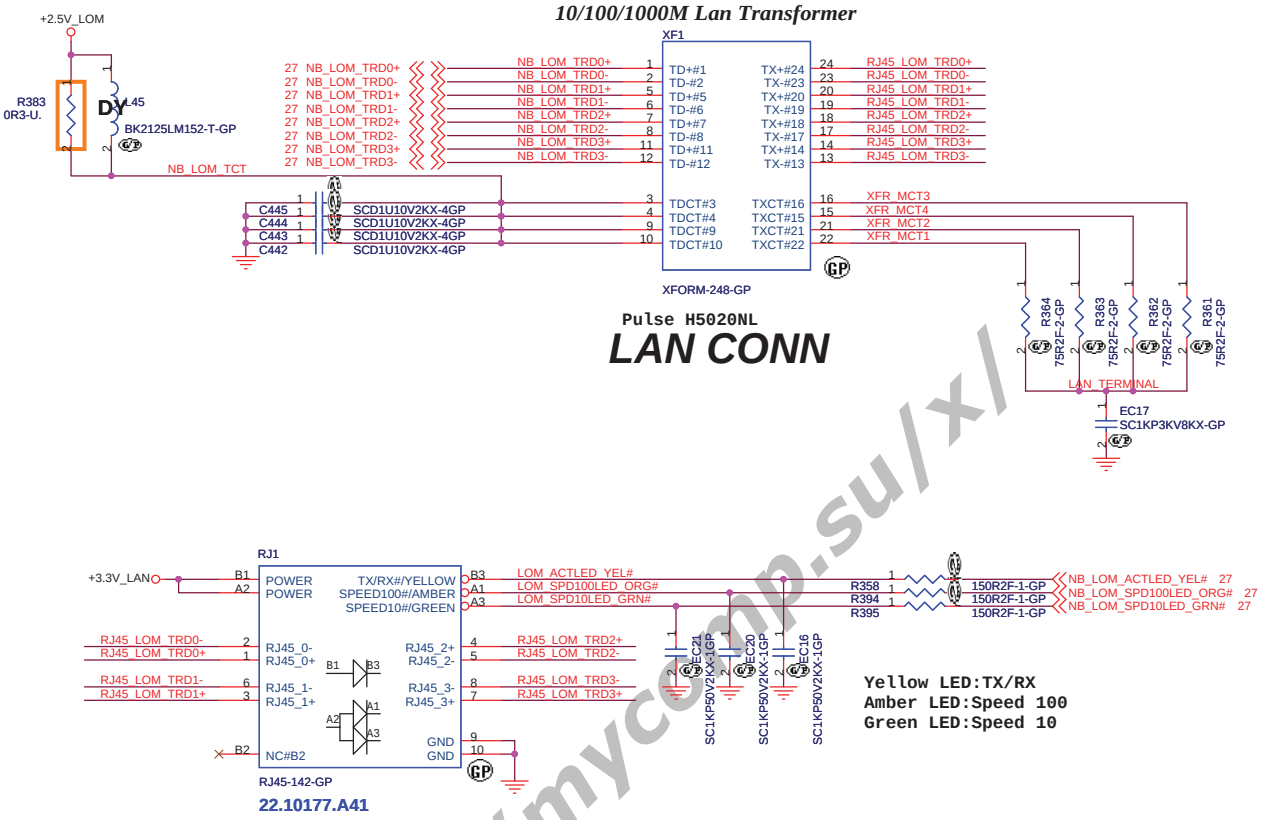
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN BCM5756ME

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 27 of 53

SSID = LOM



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

<Variant Name>

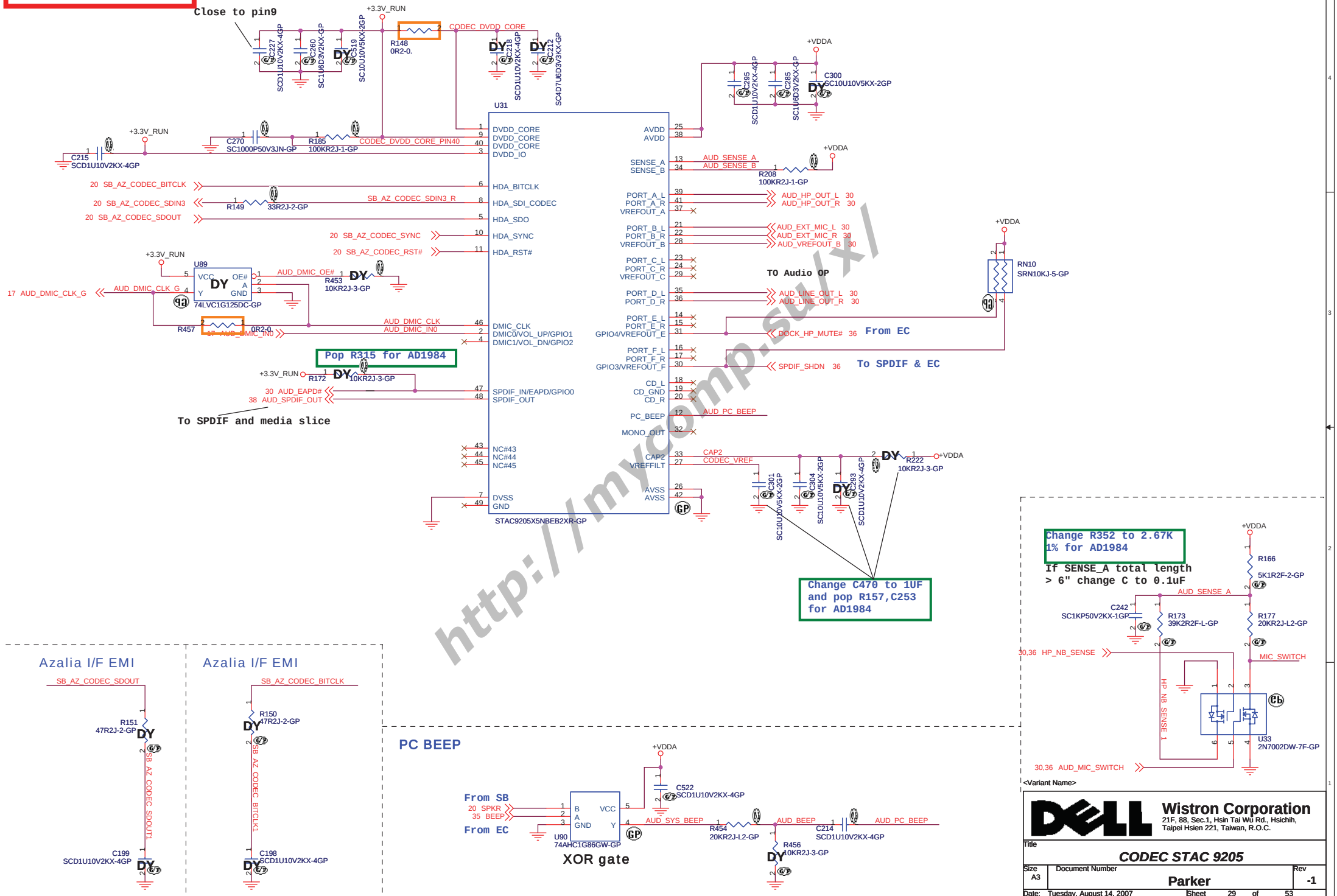
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN Connector*

Size: A3 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 28 of 53

SSID = AUDIO



Azalia I/F EMI

Azalia I/F EMI

PC BEEP

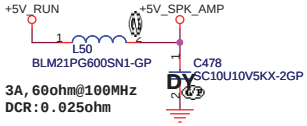
Change R352 to 2.67K 1% for AD1984

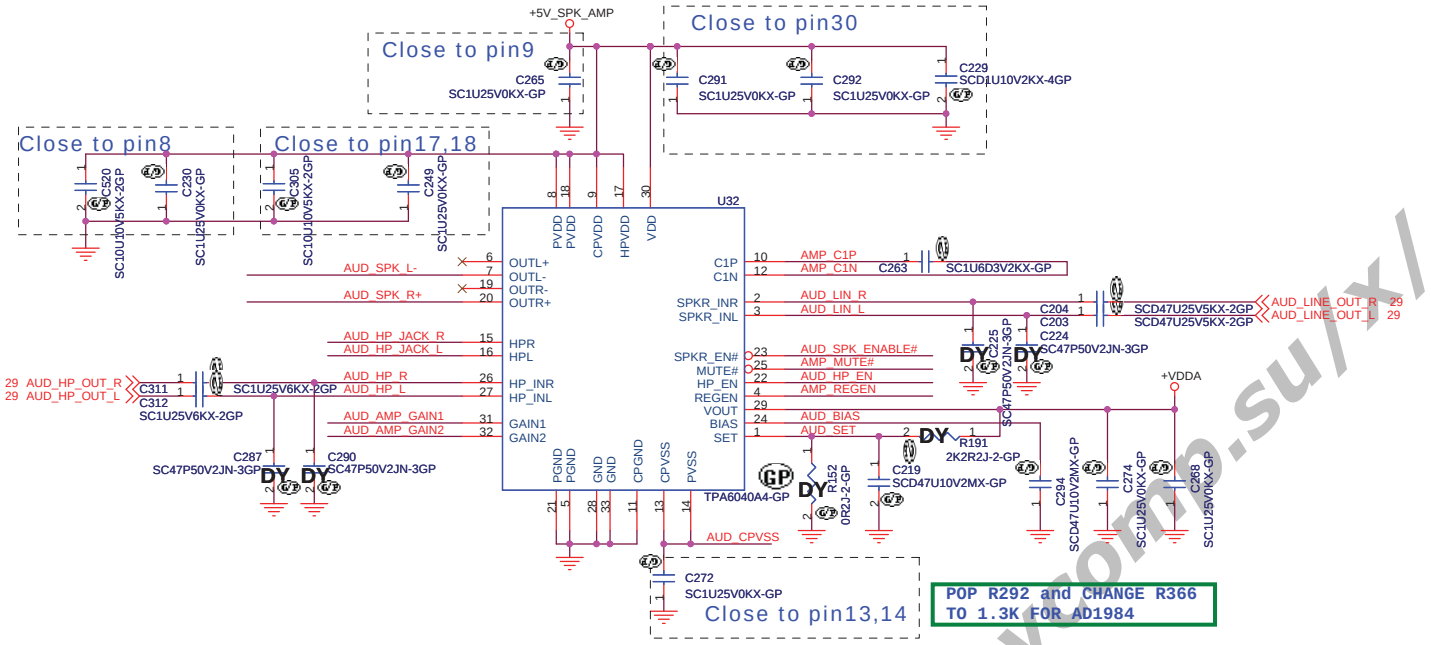
If SENSE_A total length > 6" change C to 0.1uF

<Variant Name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CODEC STAC 9205		
Size: A3	Document Number: Parker	Rev: -1
Date: Tuesday, August 14, 2007	Sheet 29 of 53	

SSID = AUDIO

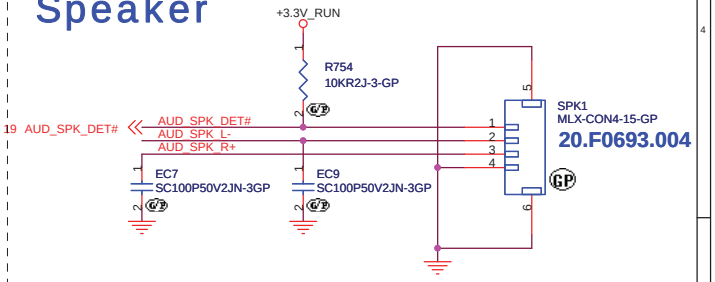




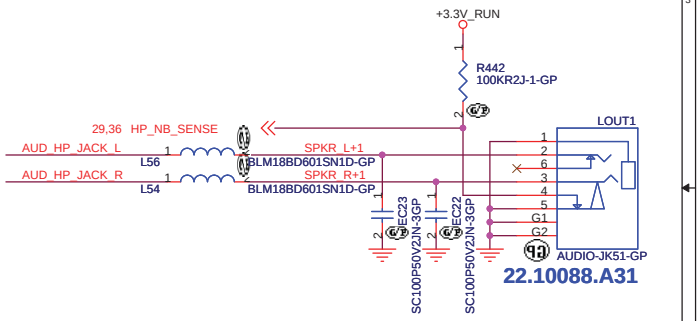
POP R292 and CHANGE R366
TO 1.3K FOR AD1984

U32 for TPA6040A4
Pop R746,C219,C220, Depop R152,R153,R210, Change C203,C204,C294 to 0.47UF
U32 for MAX9789A
Pop R152,R153,R210, Depop R746,C219,C220, Change C203,C204,C294 to 0.033UF

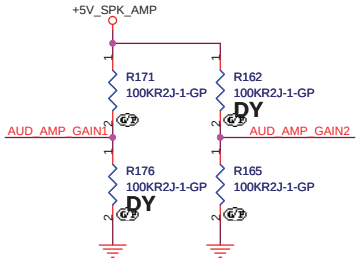
Speaker



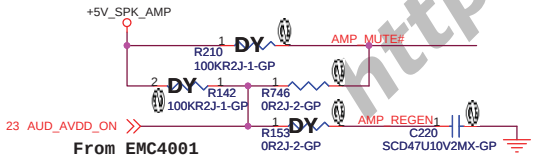
LINE OUT



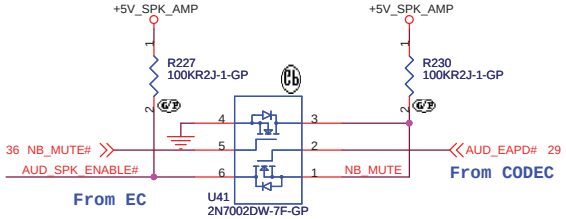
GAIN SETTING

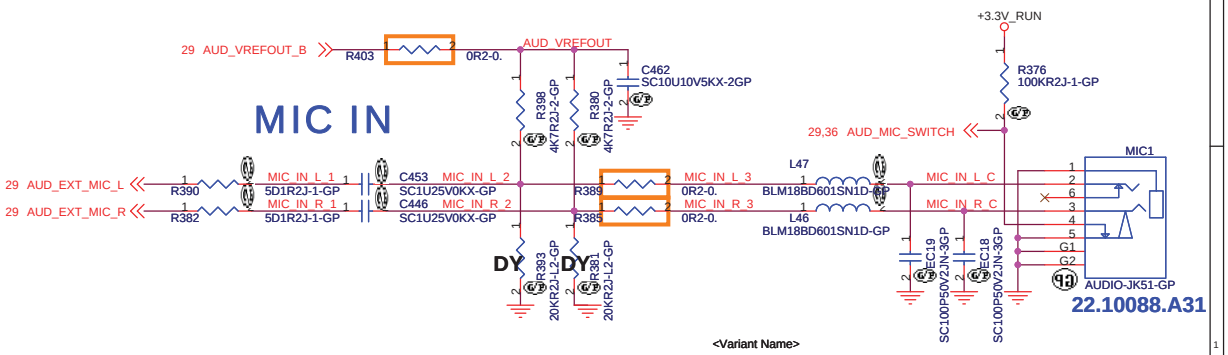


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

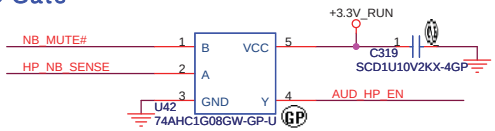


Signal inverter for speaker shutdown





AND Gate



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

Size	Document Number	Rev
A3	Parker	-1

Date: Thursday, August 09, 2007 Sheet 30 of 53

EXPRESS CARD POWER SWITCH

SSID = ExpressCard

Please Near the U32

+3.3V_SUS: C762 SCD1U10V2KX-4GP
+3.3V_RUN: C391 SCD1U10V2KX-4GP
+1.5V_RUN: C402 SCD1U10V2KX-4GP
+3.3V_CARDSUS: C403 SCD1U10V2KX-4GP
+3.3V_CARD: C390 SCD1U10V2KX-4GP
+1.5V_CARD: C765 SCD1U10V2KX-4GP

STBY# — R703 0R2J-2-GP — EXPRCRD_STDBY# — EXPRCRD_STDBY# 36

EC5018

U65 TPS2231RGP-GP

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

SHDN#	R704	100KR2J-1-GP	+3.3V_SUS
CARD_RESET#			
CPUSB#	R705	100KR2J-1-GP	+3.3V_SUS
EXPRCRD_PWREN#	R702	100KR2J-1-GP	PLTRST#
NRST	R680	0R2-0.	PLTRST# 7,18,27,32,35,45,46,51

+1.5V_RUN, +1.5V_CARD, +3.3V_CARD, +3.3V_RUN

Test circuit
Use Card and No Card

+3.3V_CARDSUS, +3.3V_SUS, +1.5V_CARD, +3.3V_RUN, +3.3V_CARD, +1.5V_RUN

20 SB600_USBP6+ — R657 0R2-0. — USBP6D+
20 SB600_USBP6- — R658 0R2-0. — USBP6D-

Close EPR1

Geometry : 1759714-1
ERPSKT1
NP1
CARDBUS-SKT92-GP-U2
For Newcard socket

EXPRESS CARD
USB-PORT6

ERP1

8 PCIE_TX3+ — PCIE_TX3+
8 PCIE_TX3- — PCIE_TX3-
8 PCIE_RX3+ — PCIE_RX3+
8 PCIE_RX3- — PCIE_RX3-
4 CLK_PCIE_EXPCARD — CLK_PCIE_EXPCARD
4 CLK_PCIE_EXPCARD# — CLK_PCIE_EXPCARD#
36 EXPRCRD_PWREN# — EXPRCRD_PWREN#
4 CARD_CLK_REQ# — CARD_CLK_REQ#
+3.3V_CARD — CARD_RESET#
+3.3V_CARDSUS — PCIE_WAKE# C
27,32,36 PCIE_WAKE# — PCIE_WAKE# — R649 0R2-0.
+1.5V_CARD
20,27,32 SB_SMB_DATA1 — SB_SMB_DATA1
20,27,32 SB_SMB_CLK1 — SB_SMB_CLK1
CPUSB#
USBP6D+
USBP6D-

CARDBUS26P-9GP-U
62.10024.891

EXPRESS PIN	
26	GND
25	PCIE_TXP4
24	PCIE_TXN4
23	GND
22	PCIE_RXP4
21	PCIE_RXN4
20	GND
19	CLK_PCIE_NEW
18	CLK_PCIE_NEW#
17	CPPE#
16	CONN_CLKREQ#
15	+3VRUN_NEW
14	+3VRUN_NEW
13	PERST#
12	+3VAUX_NEW
11	PCIE_WAKE#
10	+1.5VRUN_NEW
9	+1.5VRUN_NEW
8	SMB_DATA
7	SMB_CLK
6	TP1
5	TP2
4	CPUSTB#
3	USB+
2	USB-
1	GND

+3.3V_CARD: C668 SC10U10V5KX-2GP
+3.3V_CARD: C665 SCD1U10V2KX-4GP
+1.5V_CARD: C697 SC10U10V5KX-2GP
+1.5V_CARD: C680 SCD1U10V2KX-4GP

Please Near the EPR1

USB-PORT7

SSID = User.interface

Bluetooth Module conn.

BT1

20 SB600_USBP7+
20 SB600_USBP7-
32 COEX1_BT_ACTIVE
36 BT_RADIO_DIS#
32 COEX2_WLAN_ACTIVE
BT_ACTIVITY

+3.3V_RUN
C756 SCD1U10V2KX-4GP
C760 SC4D7U6D3V3KX-GP
R679 10KR2J-3-GP

MLX-CON10-7-GP
20.D0183.110

Note:Place R310 near CN13.

This circuit is only needed if the platform has the SNIFFER

+5V_RUN
R707 10KR2J-3-GP
33,36 LED_MASK#
17 BT_ACTIVE# — BT_ACTIVE#
Q65 2N7002-7F-GP
R697 DY 0R2J-2-GP
BT_ACTIVITY 1# — BT_ACTIVITY 1# 32
Q64 MMBT3904-7-F-GP
1 BT_ACTIVITY

SSID = User.interface

Sniffer LED.

yellow
+3.3V_SUS
35 SNIFFER_YELLOW#
Q35 DTA114YKA-1-GP
SNIFFER_Y

blue
+3.3V_SUS
R297 100KR2J-1-GP
Q34 2N7002-7F-GP
35 SNIFFER_BLUE#
SNIFFER_BLUE# 1
+5V_SUS
Q33 DTA114YKA-1-GP
SNIFFER_B
R309 470R2J-2-GP

25 SNIFFER_DET#
R308 470R2J-2-GP
SNIFFER_DET#
RSNIFFER_Y
RSNIFFER_B
SNIFFER1
HRS-CON6-3-GP
20.K0267.006

Sniffer Switch

+3.3V_RUN
R313 100KR2J-1-GP
36 WIRELESS_ON/OFF#
R318 0R2-0.
SNIFFER1
C367 SC1U6D3V2KX-GP
SNIFFER2

+RTC_CELL
R317 100KR2J-1-GP
35 SNIFFER_PWR_SW#
R319 0R2-0.
C371 SC1U6D3V2KX-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXPRESS CARD/BT/SNIFFER
Size: A3
Document Number: Parker
Rev: -1
Date: Friday, August 03, 2007
Sheet 31 of 53

SSID = WWAN

MiniCard WWAN connector

USB-PORT9

Close MINICARD2(WWAN)

C593 Please Near the MINICARD2/Pin24

Place caps closest to the SIM connector

Layout Note: Place resistors close to choke as possible to minimize stubs.

62.10024.841

62.10043.481

62.10043.491

SSID = WLAN

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

MiniCard WLAN connector

C587 Please Near the MINICARD1/Pin24

Prevent backdrive when WoW is enabled.

For Debug card used only.

62.10043.481

62.10043.491

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN/WWAN

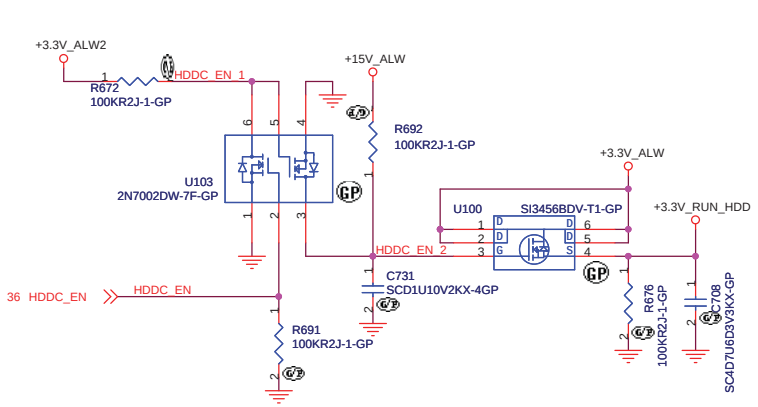
Size: Custom | Document Number: Parker | Rev: -1

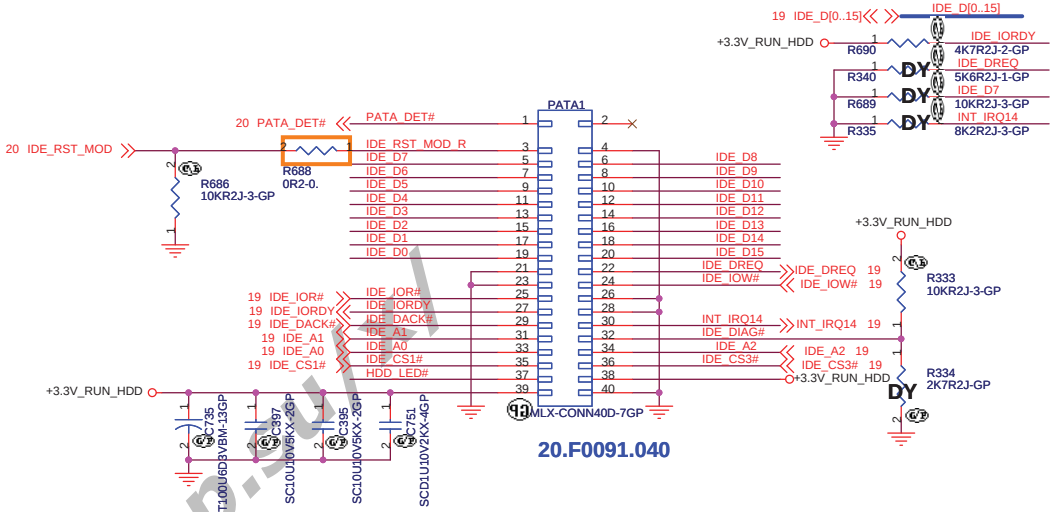
Date: Tuesday, August 14, 2007 | Sheet 32 of 53

SSID = PATA

PATA HDD conn.

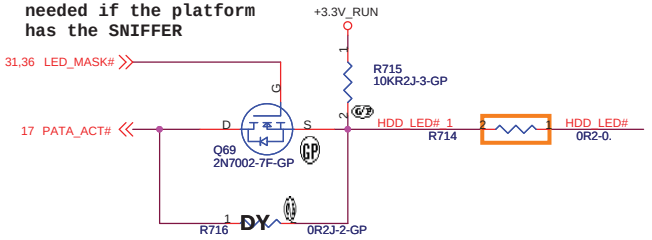
SSID = PATA





20.F0091.040

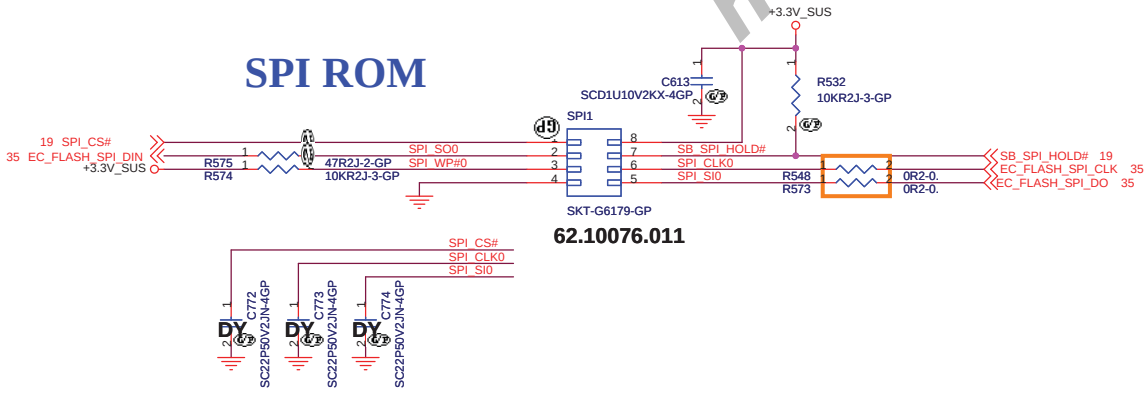
This circuit is only needed if the platform has the SNIFFER



SSID = Flash.ROM

SPI BIOS :SST FEROM 25VF016B
P/N:72.25016.A01
SPI BIOS socket :62.10076.011

SPI ROM

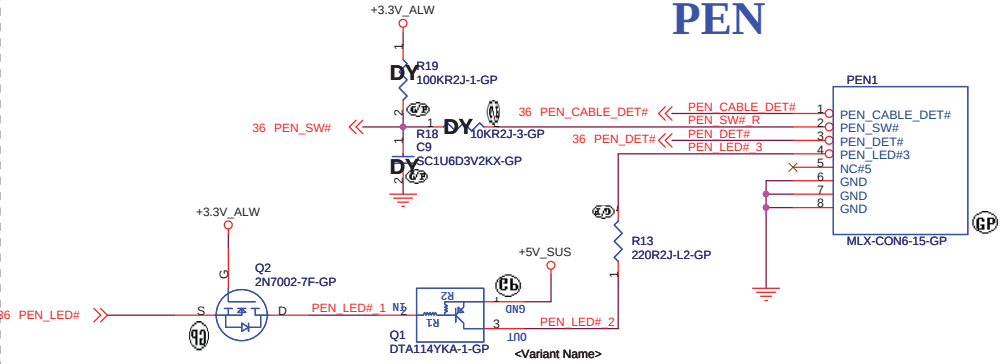


62.10076.011

SSID = User.interface

JUST SUPPORT S3 WAKE UP,CHANGE TO SUS POWER

PEN



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/SPI ROM/PEN

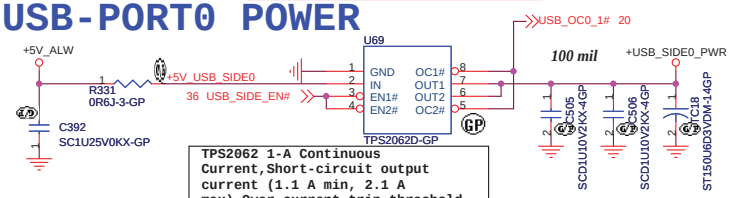
Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 Sheet 33 of 53

USB POWER

SSID = USB

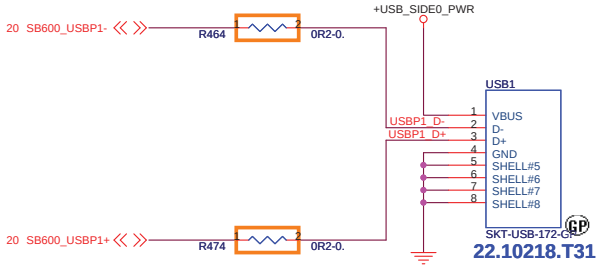
USB-PORT0 POWER



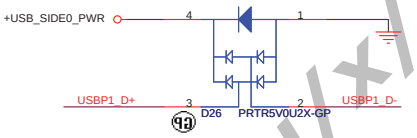
TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.

ESD Cap must near USB connector

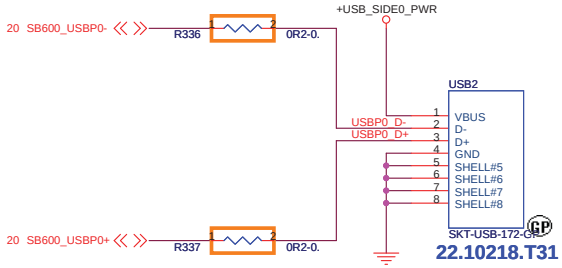
USB-PORT1



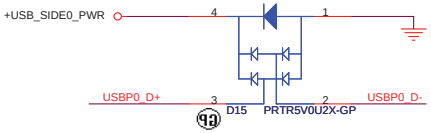
22.10218.T31



USB-PORT0



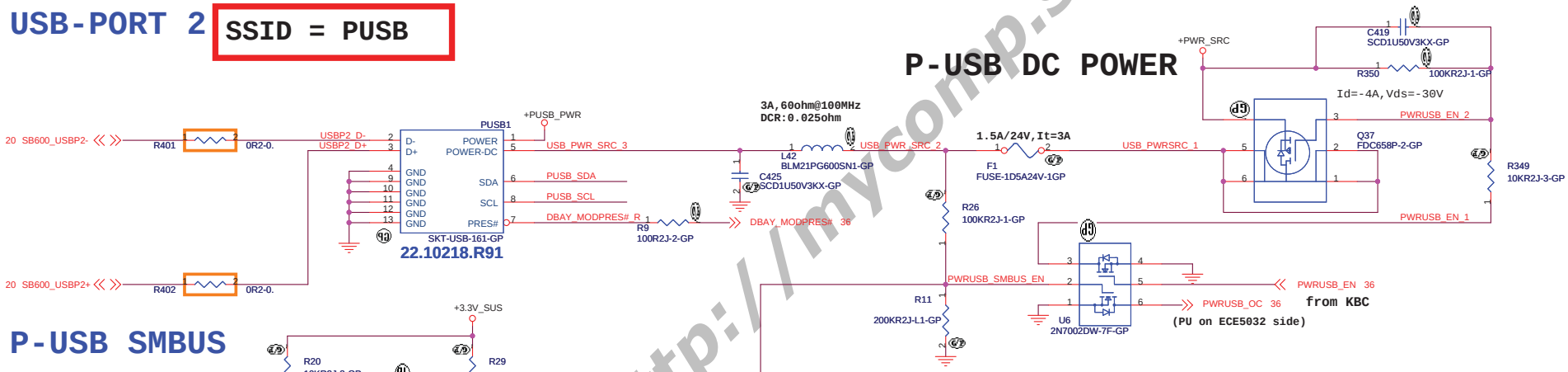
22.10218.T31



USB-PORT 2

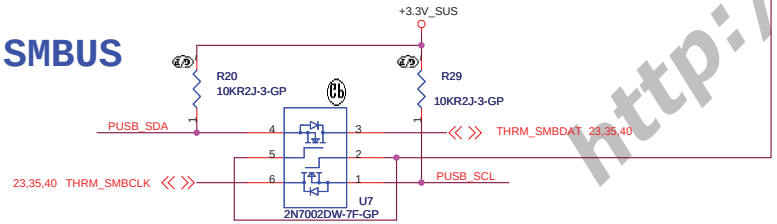
SSID = PUSB

P-USB DC POWER



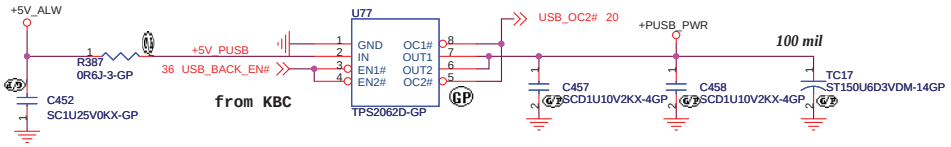
22.10218.R91

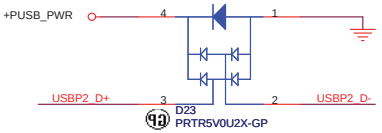
P-USB SMBUS



P-USB POWER

TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: P-USB/USB

Size: Custom | Document Number: Parker | Rev: -1

Date: Thursday, August 09, 2007 | Sheet 34 of 53

SSID = KBC

ATI versus Intel chipset to allow power sequence differences.
ATI is Logic High.
Intel is Logic Low.

Place cap close to pin 121

Place these caps close to MEC5025.

Note: MEC5025 KSO3/GPIOC3 pin 29 was 3V_5V_SUS_PWRGD, M08 platforms already had 3V_5V_SUS_PWRGD from the discrete component.

ECE1077 BC bus

ECE5021 BC bus

TP

To KBC 5025

Flash Recovery.
1=Enabled
0=Disabled

Low=
Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

Not Stuff R921 0 ohm when doing Flash recovery.

Debug Serial Port
Flash Recovery port.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

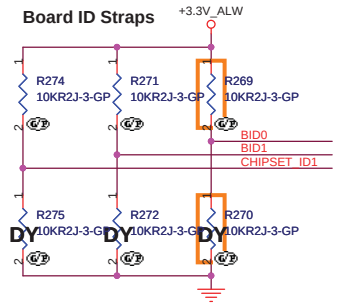
<variant_name>

Title: KBC MEC5025

Size: A3 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 35 of 53

Board ID Straps

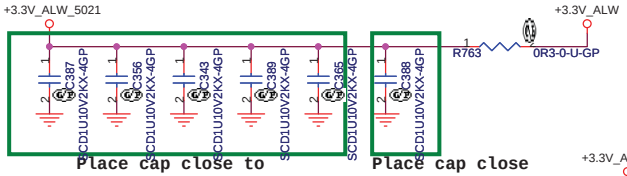


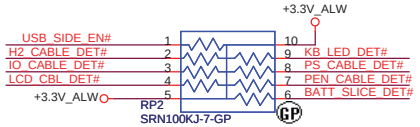
BID1	BID0	Board Rev.
0	0	SST(X00)
0	1	PT(X01)
1	0	ST(X02)
1	1	X-B(A00)

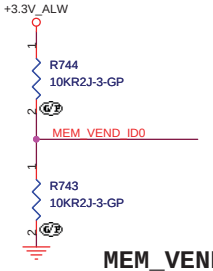
CHIPSET_ID1

This resistor strapping will not change and is used to identify parker chipset as ATI

SSID = SIO

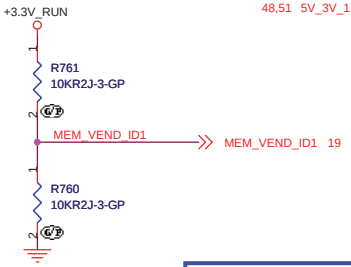






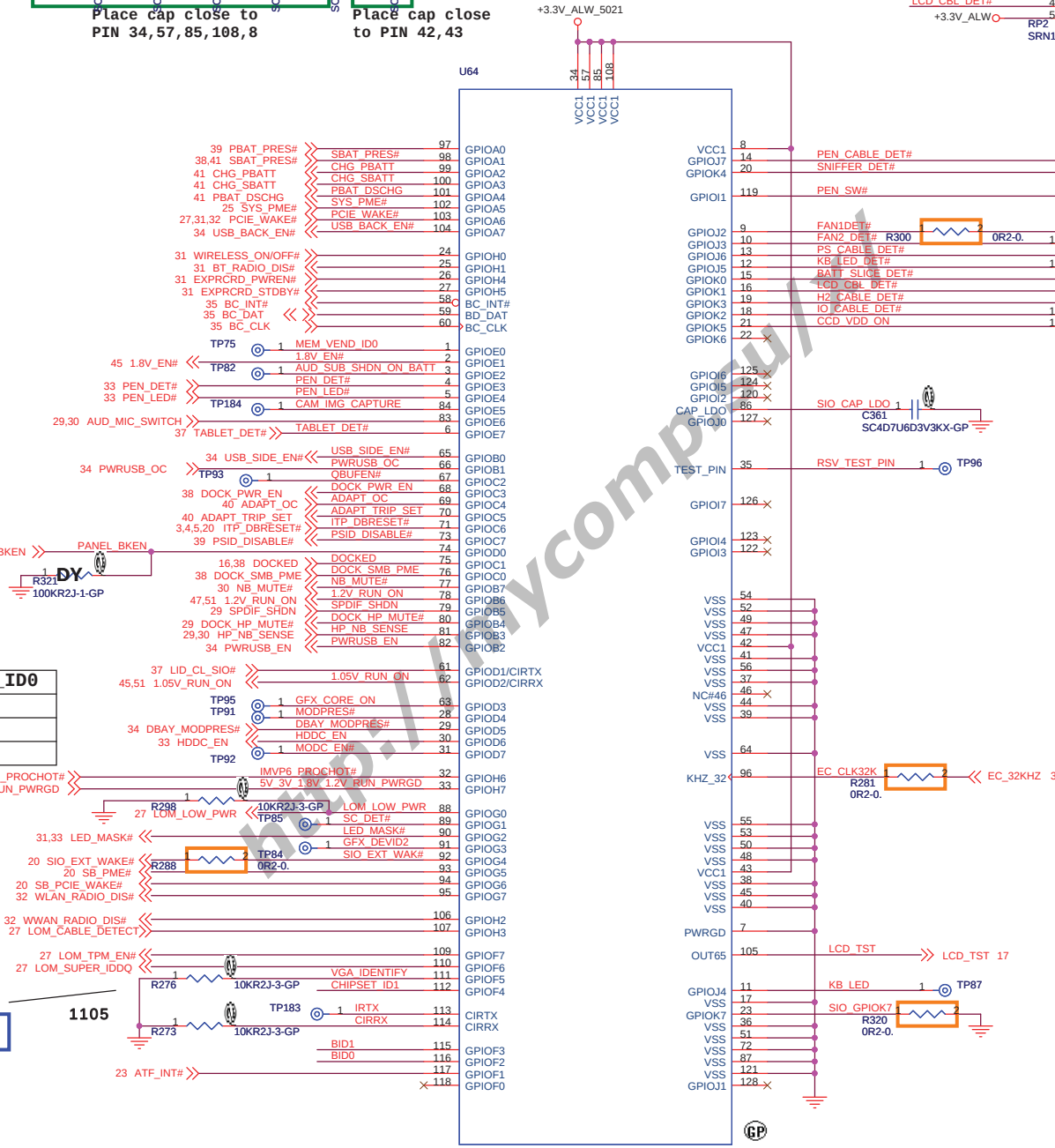
MEM_VEND_ID support

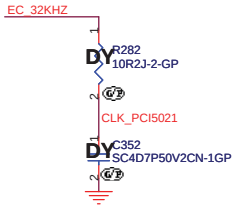
	MEM_VEND_ID1	MEM_VEND_ID0
Sansung	H	L
Hynix	L	H
Mircon	L	H

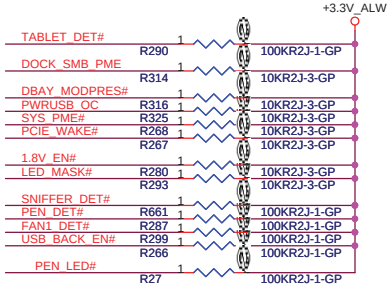


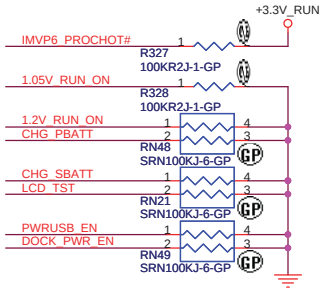
VGA_IDENTIFY
Low=UMA, High=Discrete

1105









Parker

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

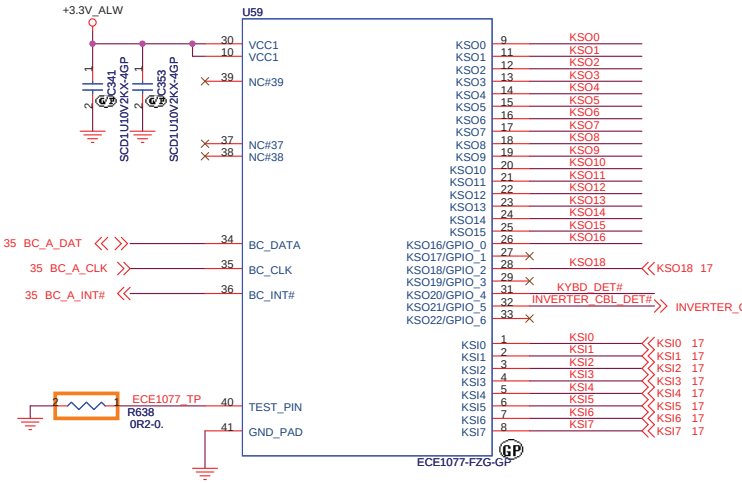
Title: SIO ECE5021

Size	Document Number	Rev
A3	Parker	-1

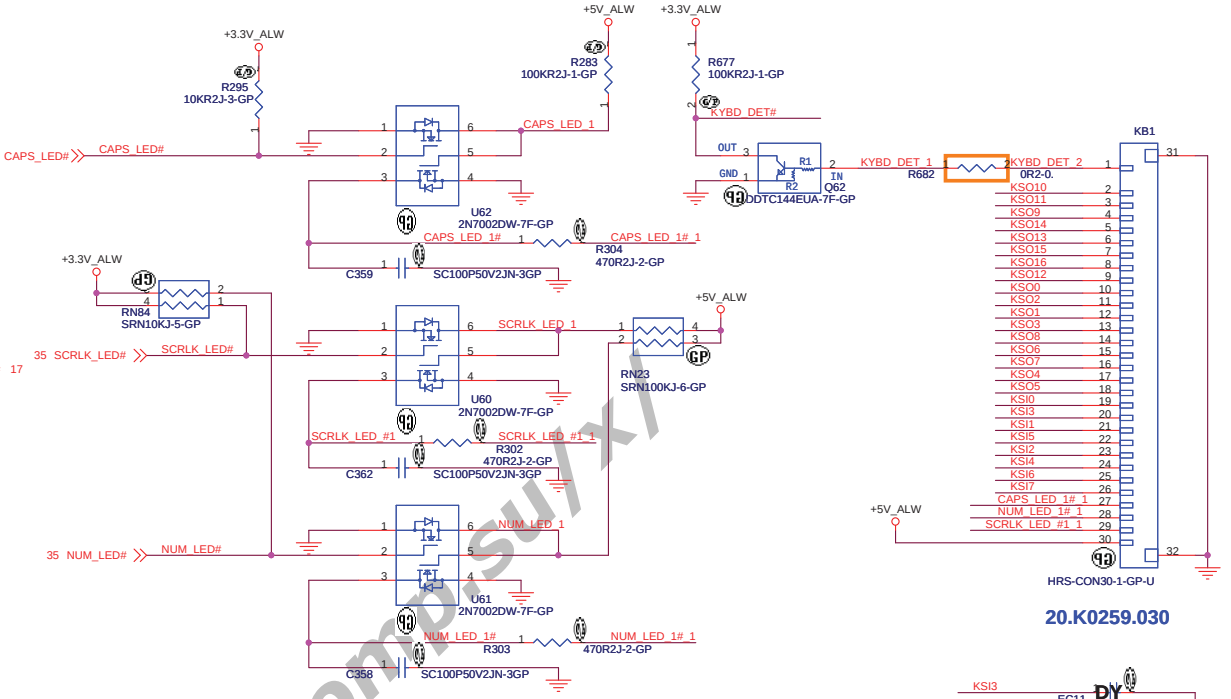
Date: Friday, August 03, 2007 Sheet 36 of 53

K/B CONN.

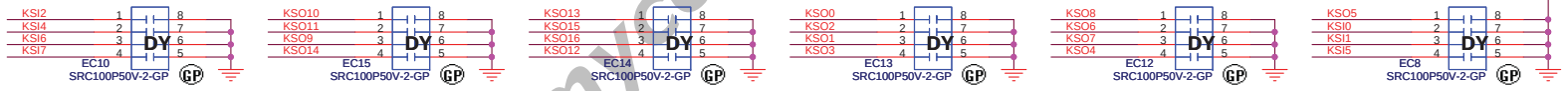
SSID = User.interface



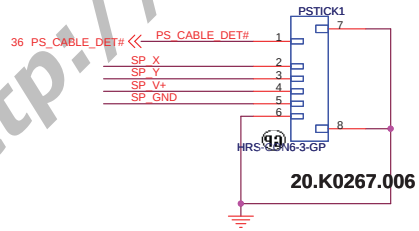
KB LEDs



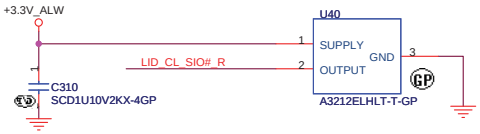
PLACE HOLDER



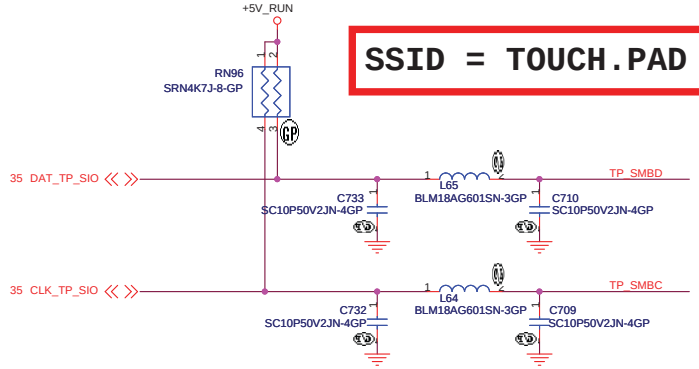
POINT-STICK CONN.



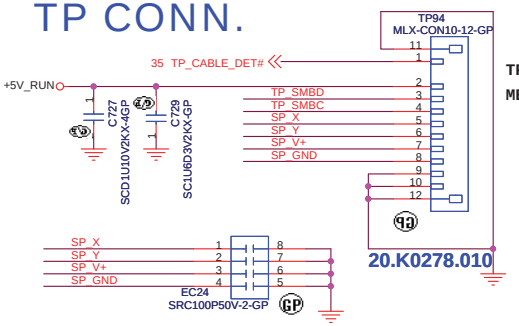
hall switch



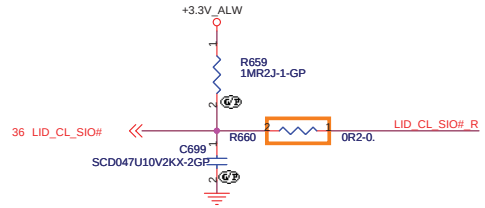
SSID = TOUCH.PAD

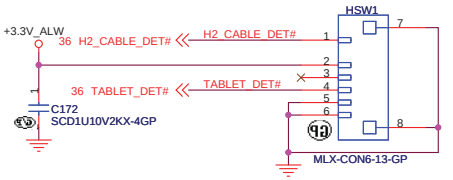


TP CONN.



TP AND POWER
MEC5025 CONNECT





<Variant Name>

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Title: ECE1077

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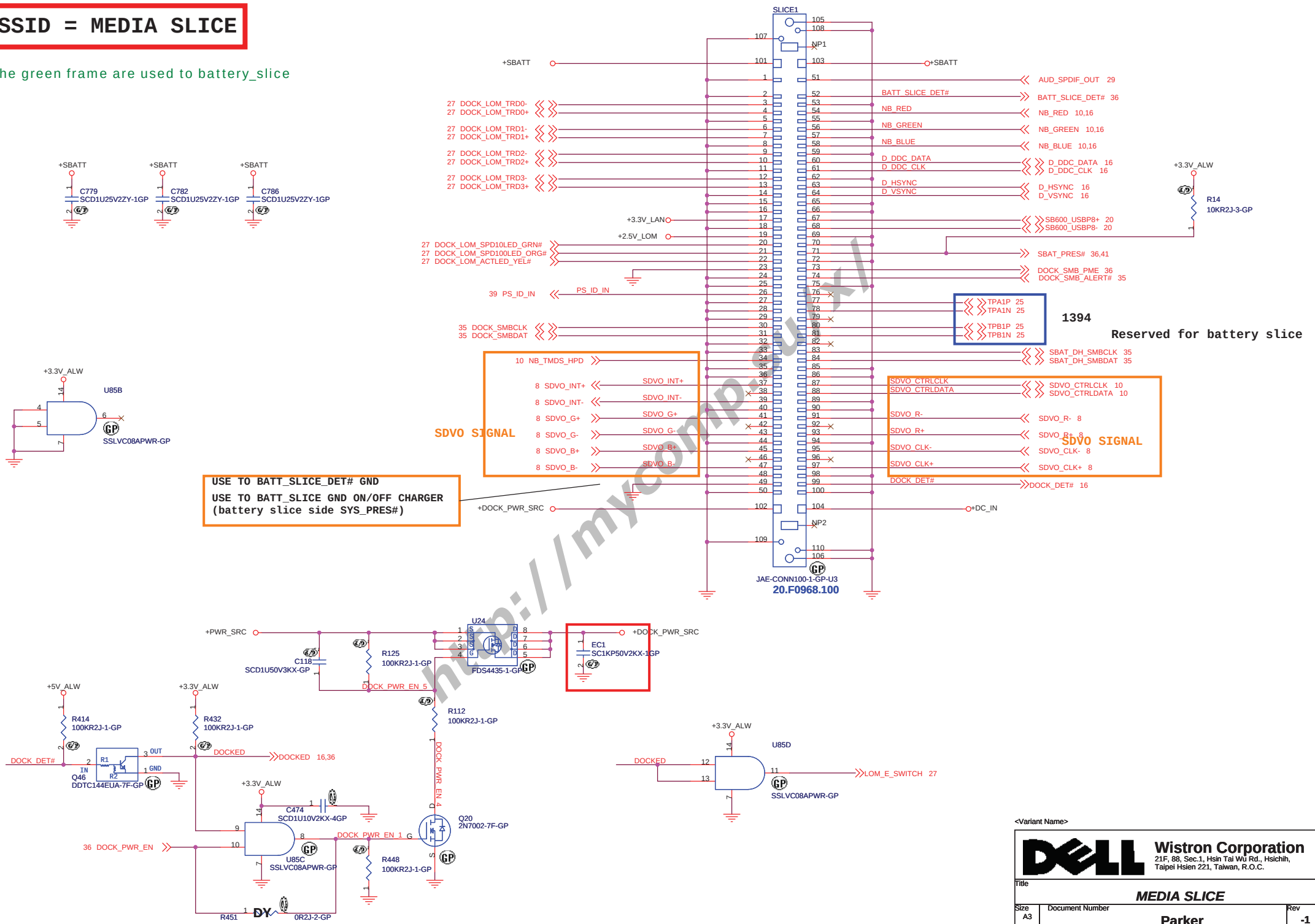
SSID = MEDIA SLICE

The green frame are used to battery_slice



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: MEDIA SLICE

Size	Document Number	Rev
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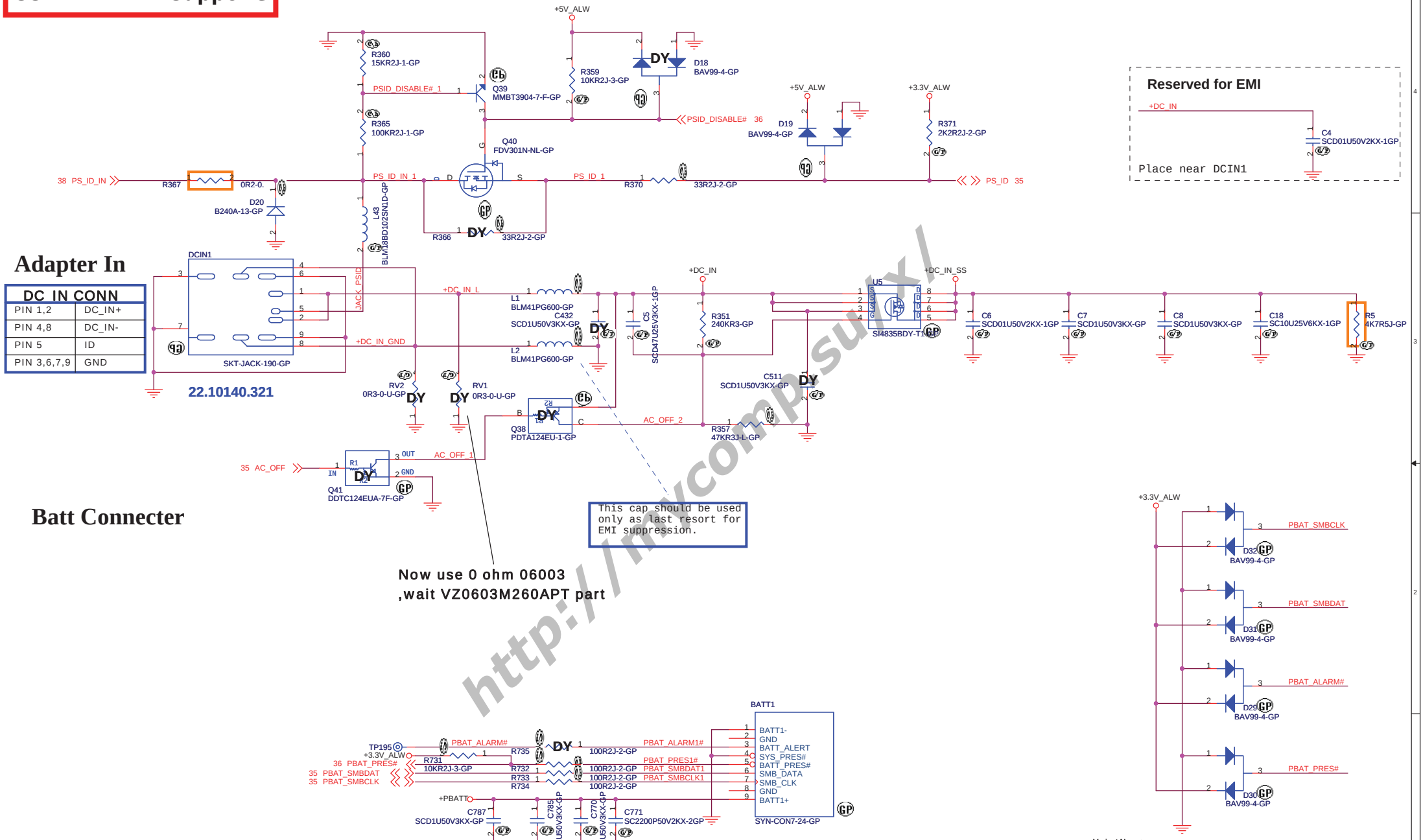
SSID = PWR.Support



<Variant Name>

Wistron Corporation
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Title: **DCIN / BATT CONN.**

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SSID = CHARGER

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

Adapter (W)	Trip Current (A)	R1620	R1621	R1622	R1623
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R23 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

This Resistor must be 1% tolerance.

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
R1610	8.45K 1%	DUMMY
C1412	0.01uF	0.1uF
C1404	0.1uF 10V	DUMMY
C1408	1uF 10V	DUMMY
R1602	365K 1%	215K 1%
R1609	0 5%	10 5%
R1601	0 5%	10 5%
C1402	DUMMY	0.22uF
C1388	DUMMY	0.22uF
C1406	0.01uF	DUMMY
C1409	0.1uF 10V	DUMMY
C1399	220pF 50V	DUMMY
D36	RB751V-40	DUMMY
C1398	3.3nF	DUMMY
R1607	1 1%	0 5%
R1612	100 5%	0 5%
R1759	0 5%	8.45K 1%
R1611	10K 5%	2.2K 5%
C1405	0.01uF	0.01uF
C1407	0.01uF	0.01uF
R1606	1K 5%	DUMMY
D35	ISS355	DUMMY

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Title: Charger
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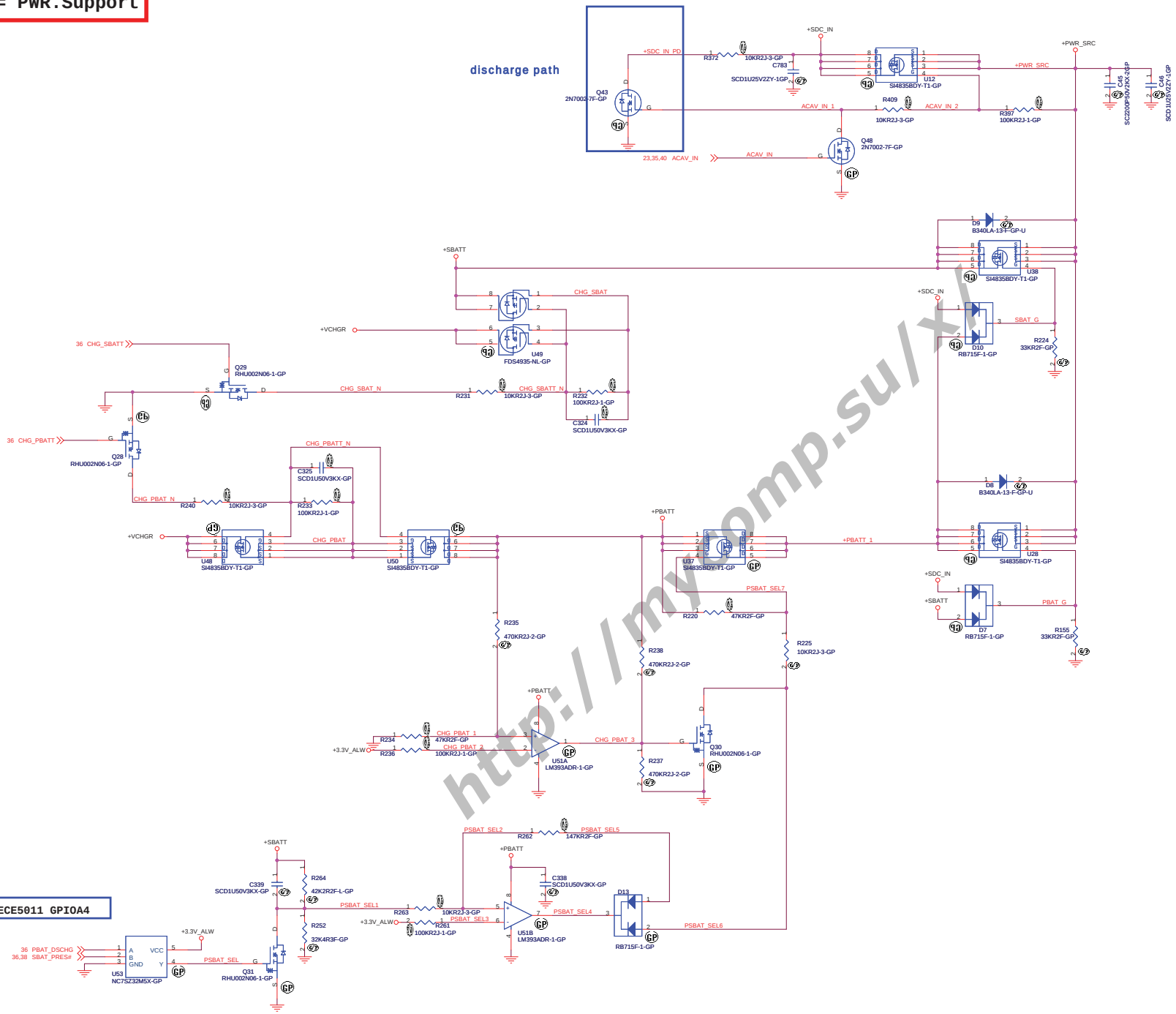
SSID = PWR.Support



In M07,use ECE5011 GPIOA4

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY SELECT

Size	Document Number	Rev
A2	Parker	-1

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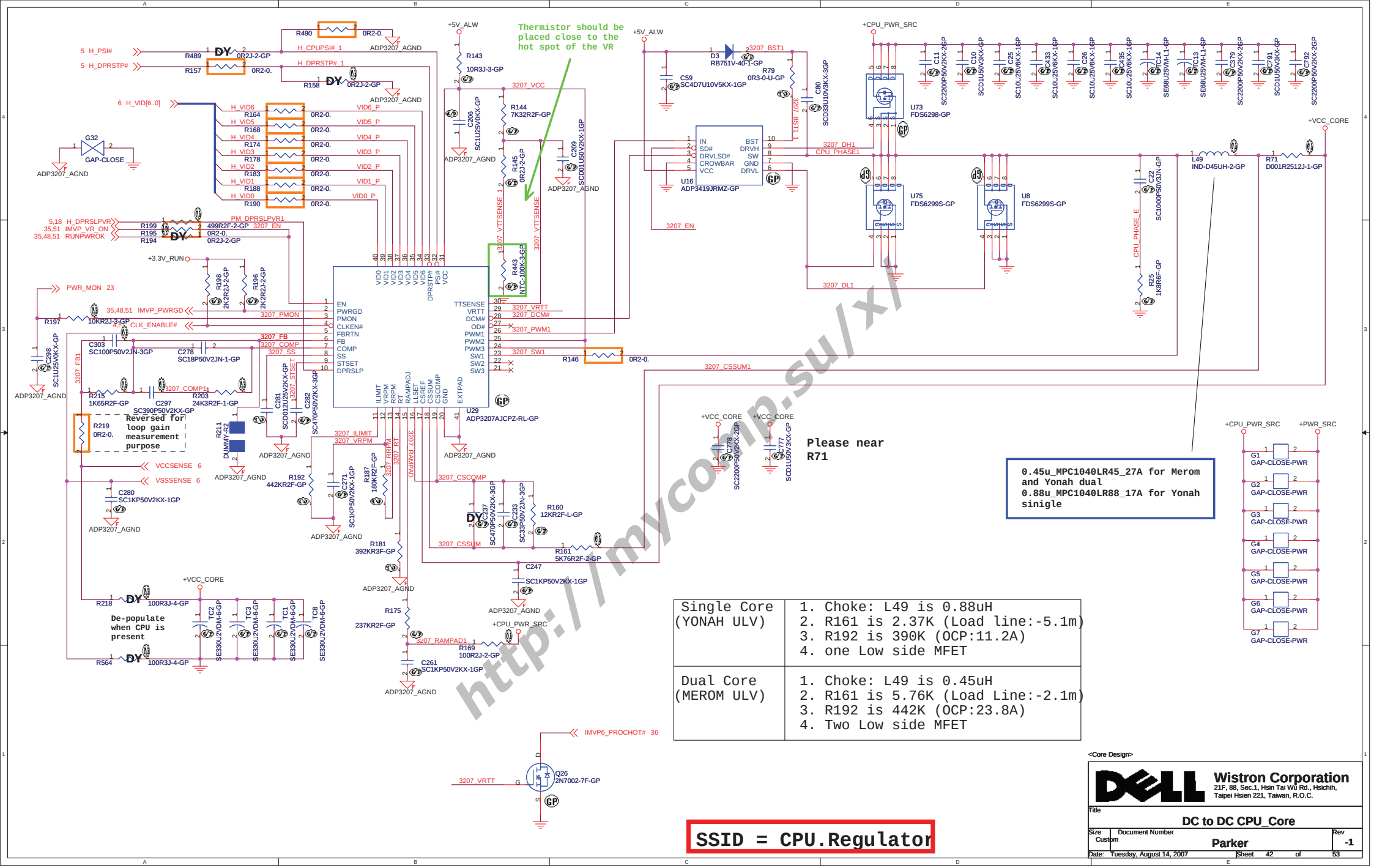

Single Core (YONAH ULV)	1. Choke: L49 is 0.88uH 2. R161 is 2.37K (Load line:-5.1m) 3. R192 is 390K (OCP:11.2A) 4. one Low side MFET
Dual Core (MEROM ULV)	1. Choke: L49 is 0.45uH 2. R161 is 5.76K (Load Line:-2.1m) 3. R192 is 442K (OCP:23.8A) 4. Two Low side MFET

<Core Design>

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Title	DC to DC CPU_Core	
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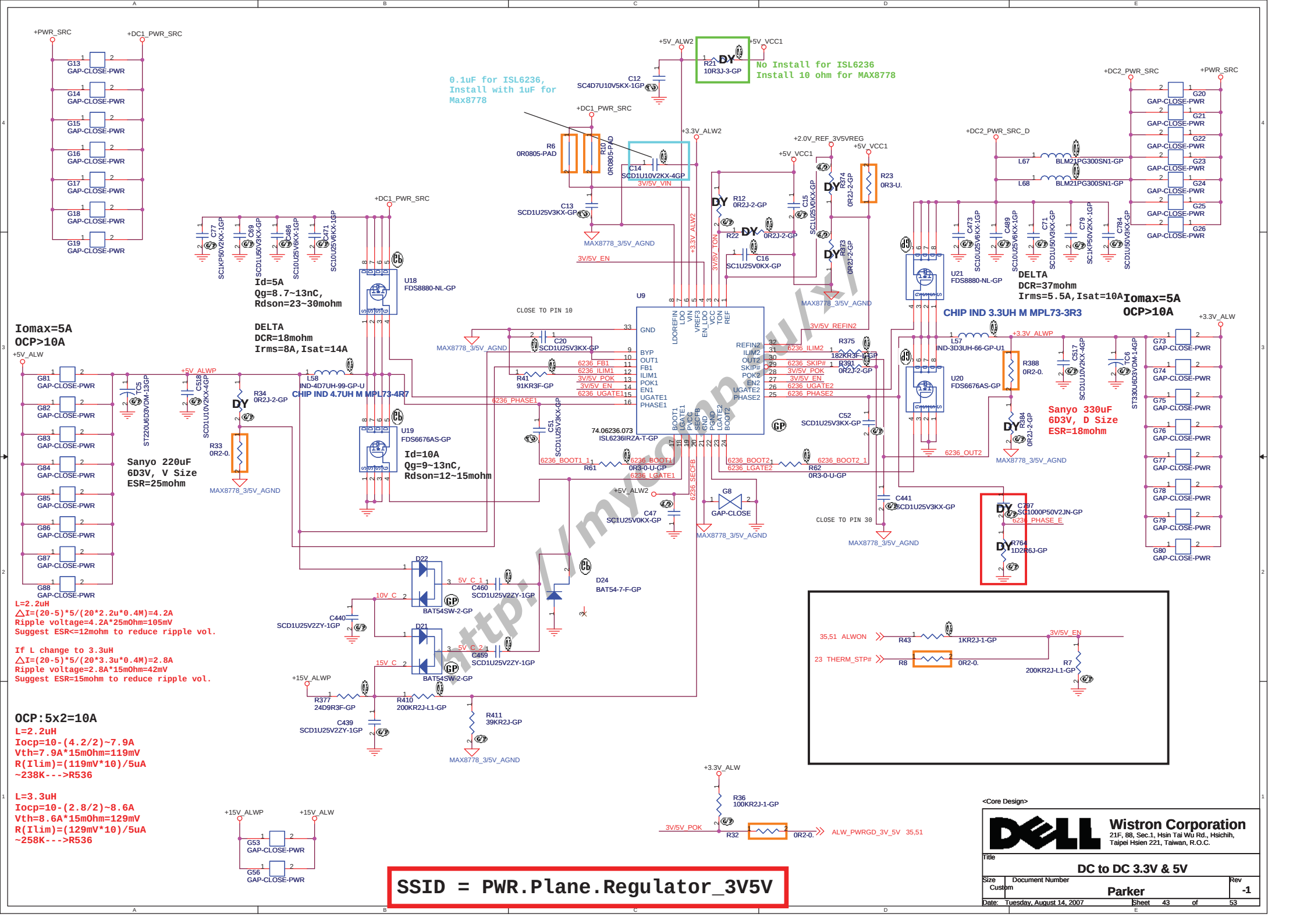
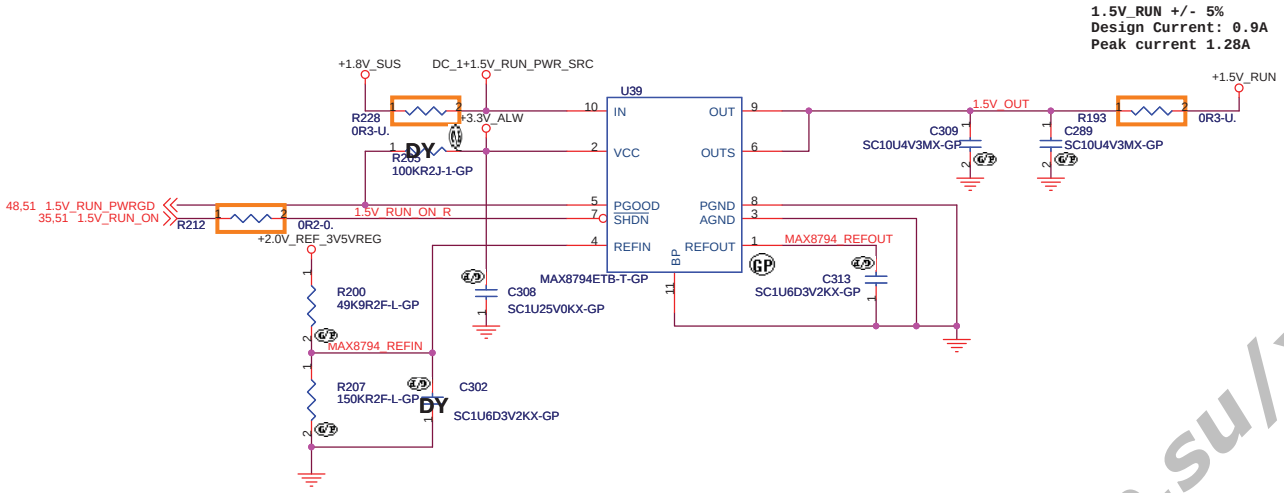
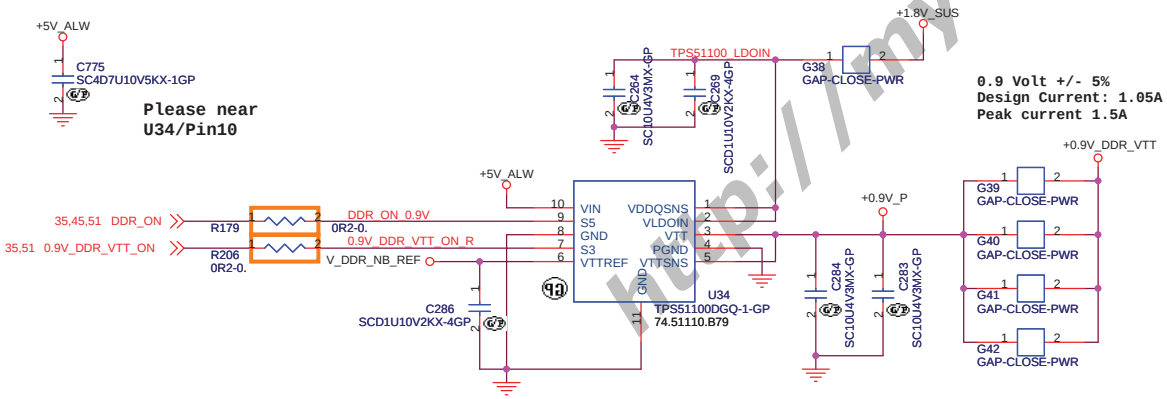


SSID = PWR.Plane.Regulator_1.5V



SSID = PWR.Plane.Regulator_0.9V



<Core Design>

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Title: DC to DC 1D5V / 0D9V

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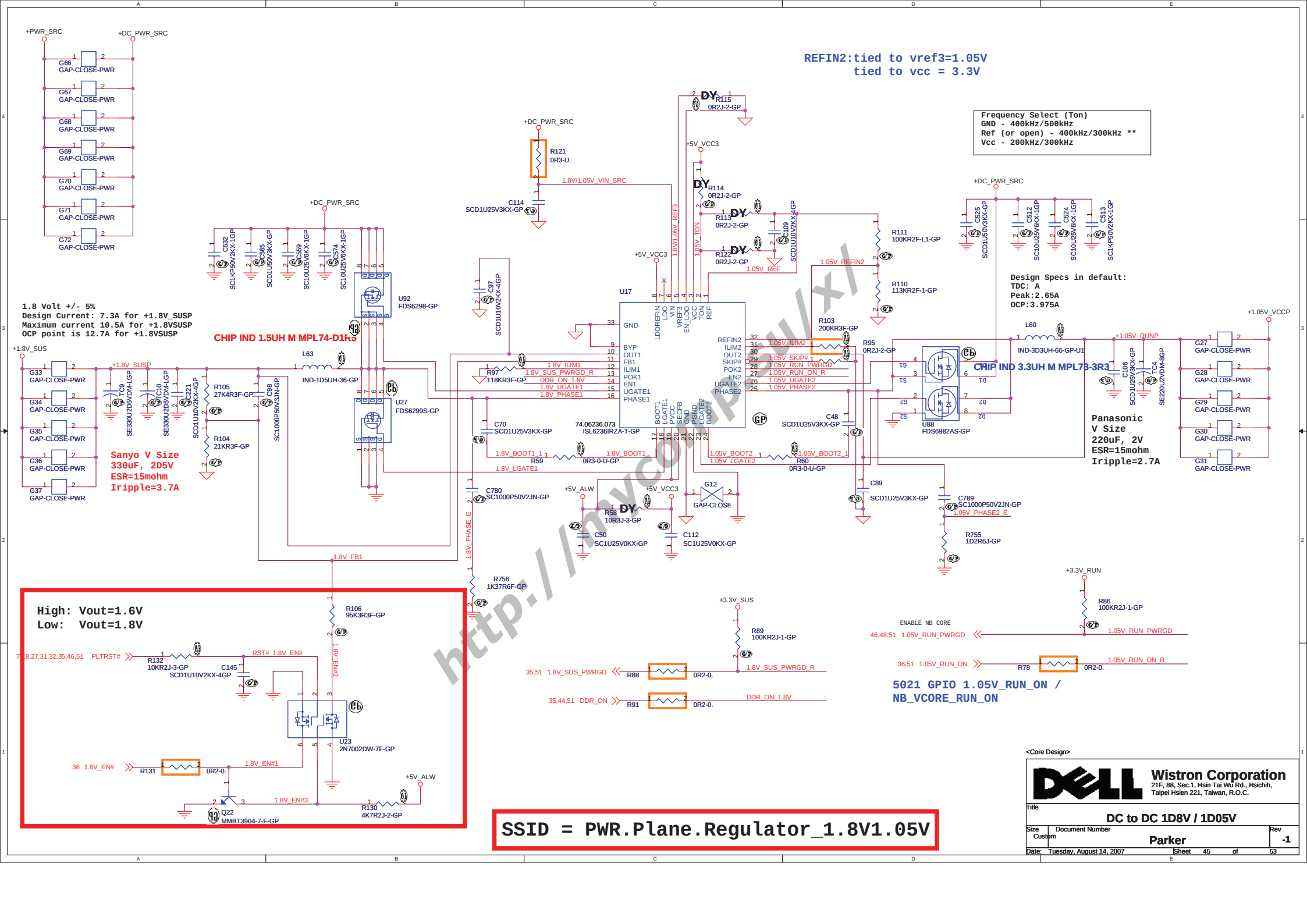

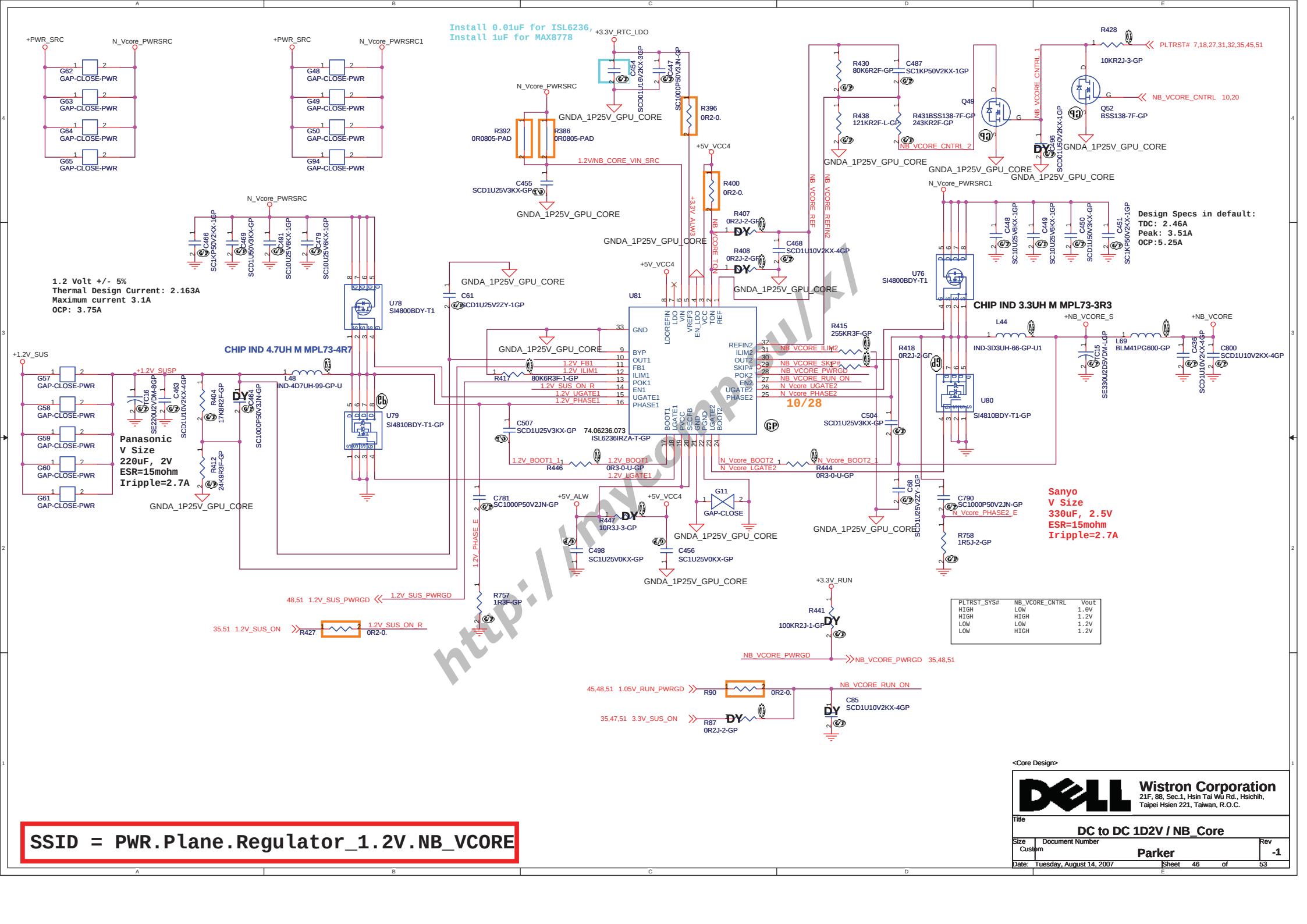
Install 0.01uF for ISL6236,
Install 1uF for MAX8778
1.2 Volt +/- 5%
Thermal Design Current: 2.163A
Maximum current 3.1A
OCP: 3.75A
CHIP IND 4.7UH M MPL73-4R7
Panasonic
V Size
220uF, 2V
ESR=15mohm
Iripple=2.7A
CHIP IND 3.3UH M MPL73-3R3
Design Specs in default:
TDC: 2.46A
Peak: 3.51A
OCP:5.25A
Sanyo
V Size
330uF, 2.5V
ESR=15mohm
Iripple=2.7A
10/28
SSID = PWR.Plane.Regulator_1.2V.NB_VCORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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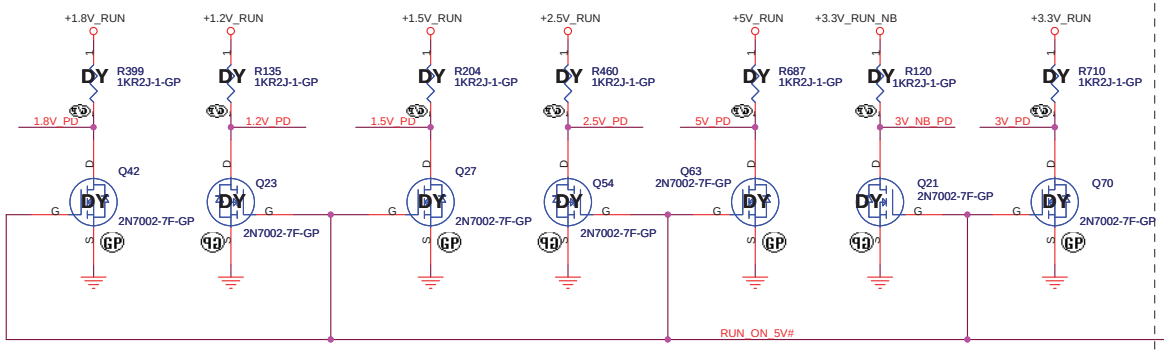
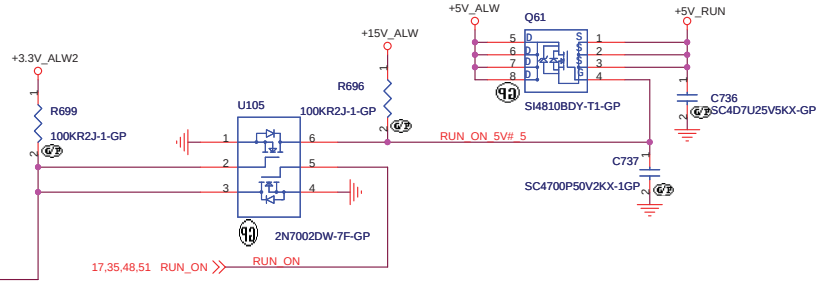
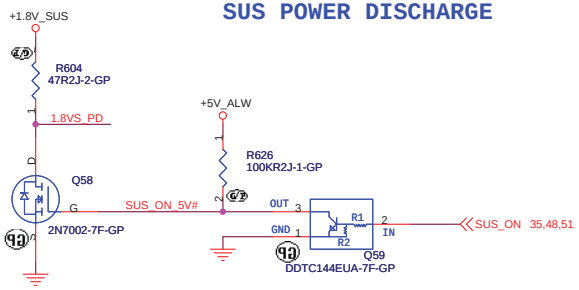
DC to DC 1D2V / NB_Core
Parker
Tuesday, August 14, 2007
http://mycomp.ru/xi

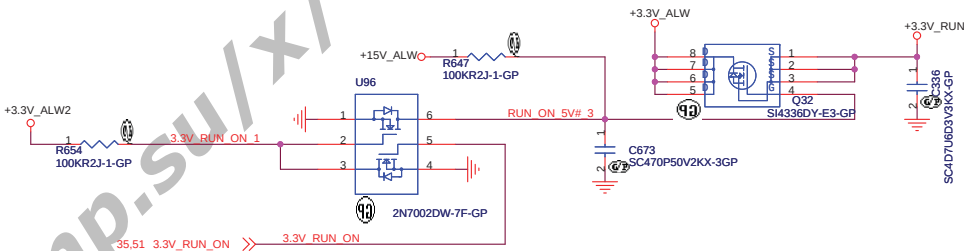
RUN POWER DISCHARGE



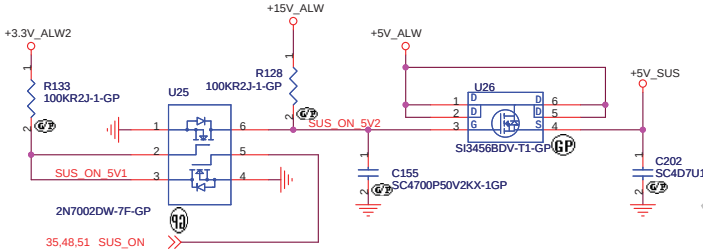


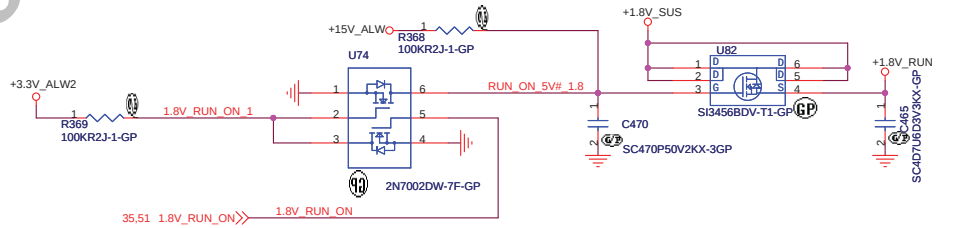
SUS POWER DISCHARGE



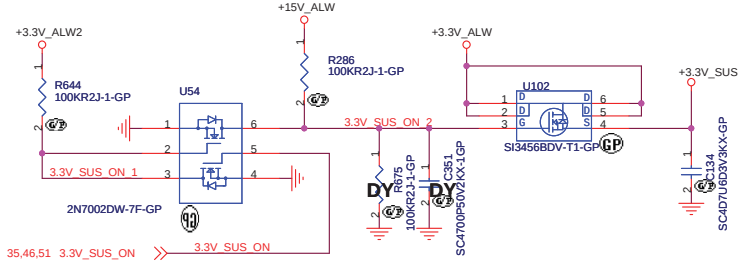


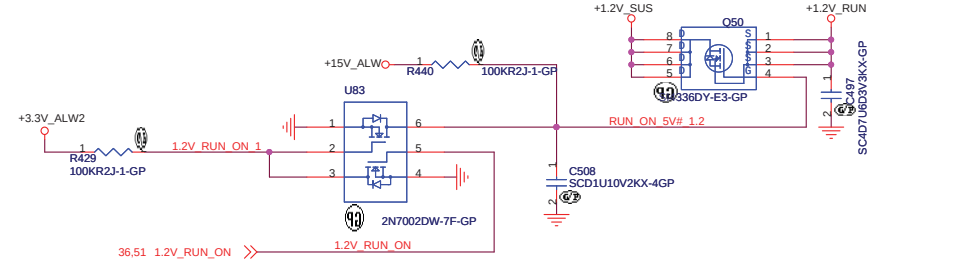
+5V_SUS POWER ENABLE





+3.3V_SUS POWER ENABLE





SSID = Reset.Suspend

<Variant Name>

Wistron Corporation
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Title: POWER ENABLE

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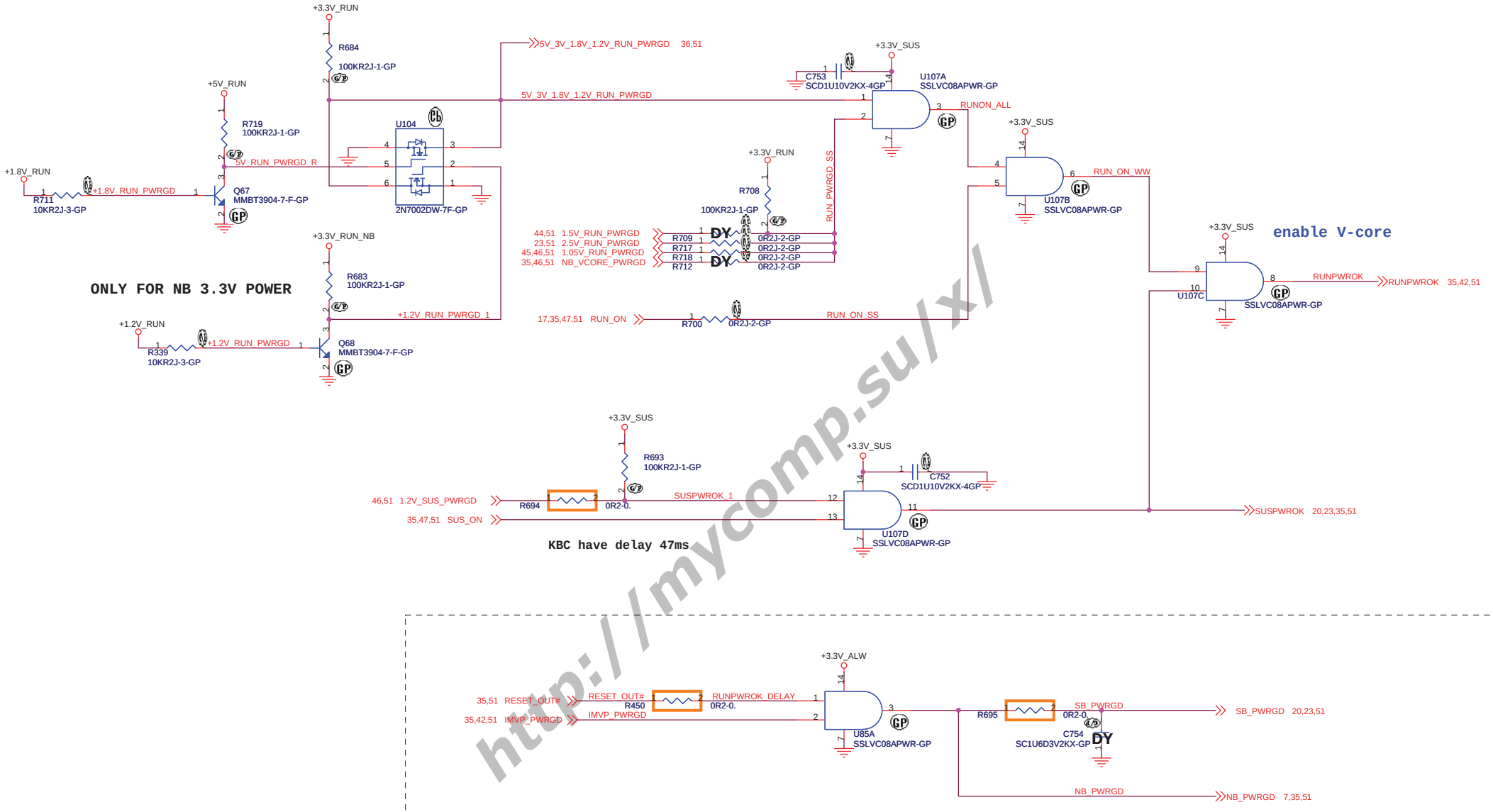

SSID = Reset.Suspend

<Variant Name>

Wistron Corporation
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Title: **POWER ON LOGIC**

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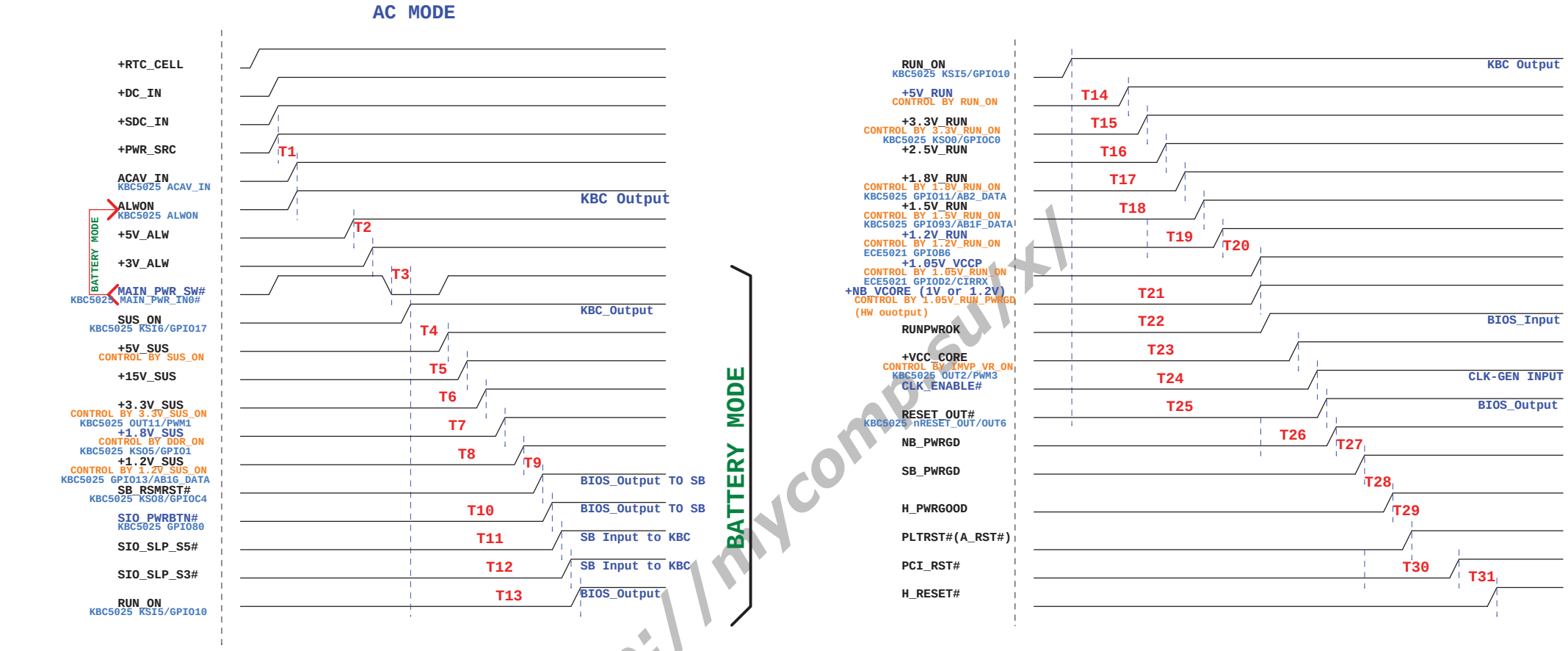
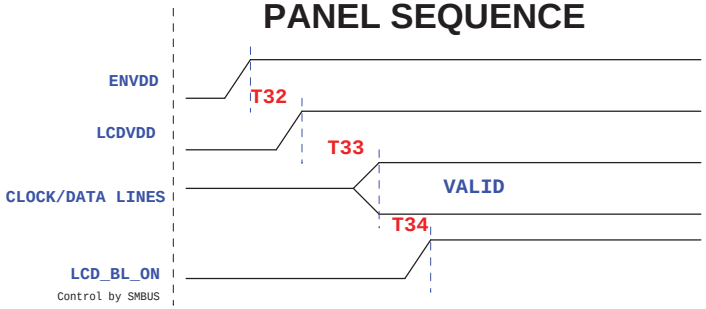
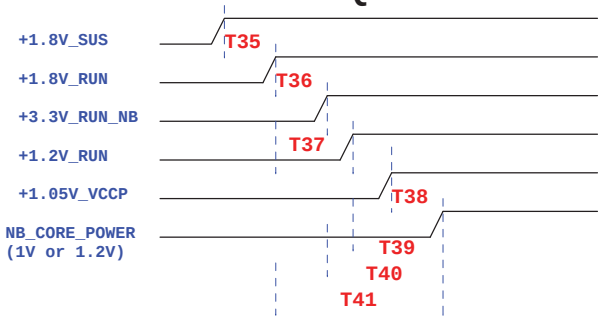
DP2 PLATFORMS POWER UP



PANEL SEQUENCE



NB SEQUENCE



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Title: POWER ON SEQUENCE

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Custom	Parker	-1

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Power

Signal Name	Test Position	Signal Name	Test Position
+DC_IN	U5.1;Page 39	GFX_PWR_SRC	U10.1;Page 17
+DC_IN_SS	U5.8;Page 39	+RTC_CELL	C266.1;Page 18
+SDC_IN	U12.8;Page 41	VCC_RUN_SB	L31.1;Page 18
+VCHGR	U48.8;Page 41	VCC_SB_PVDD	C315.1;Page 18
+PBATT	U37.1;Page 41	VCC_SB_VDDR	C245.1;Page 18
+SBATT	U38.8;Page 41	SB_AVDDCK1.2	C181.1;Page 21
+DOCK_PWR_SRC	U24.8;Page 38	+3.3V_RUN_HW	C275.1;Page 19
+PWR_SRC	U12.1;Page 41	+3.3V_SB_USB_TX	C156.1;Page 20
+VCC_CORE	TC2.1;Page 42	+3.3V_SB_USB_RX	C183.1;Page 20
+15V_ALW	R696.1;Page 47	+3.3V_SB_AVDDC	C135.1;Page 20
+5V_ALW	R413.1;Page 18	+SB_AVDDCK3.3	C182.1;Page 21
+3.3V_ALW	U11.1;Page 17	SB_5V_REF	C620.1;Page 21
+3.3V_ALW2	C14.2;Page 43	+2.5V_RUN	C552.1;Page 23
+1.5V_RUN	R193.2;Page 44	THERMAL_LDO_IN	C553.1;Page 23
+0.9V_DDR_VTT	C718.1;Page 15	+3.3V_PCI7402_AVDD	C348.1;Page 24
+1.8V_SUS	R170.1;Page 7	+3.3V_PCI7402	C364.1;Page 24
+1.05V_VCCP	C102.1;Page 11	+3.3V_PCI7402_VCCP	C656.1;Page 24
+1.2V_SUS	Q50.8;Page 47	+3.3V_PCI7402_VDDPLL33	C730.1;Page 24
+NB_VCORE	U26.6;Page 47	PCI7402_VR_PORT	C703.1;Page 24
+5V_SUS	U26.6;Page 47	+3.3V_RUN_CARD	C763.1;Page 26
+3.3V_SUS	U102.6;Page 47	+3.3V_LAN	U93.4;Page 27
+5V_RUN	Q61.1;Page 41	+2.5V_LOM	C62.1;Page 27
+3.3V_RUN	Q32.1;Page 47	+2.5V_BIASVDD	L51.1;Page 27
+1.8V_RUN	U82.6;Page 47	+2.5V_XTALVDD	L53.1;Page 27
+1.2V_RUN	Q50.1;Page 47	+2.5V_AVDD	L59.1;Page 27
CLK_VDDREF	C331.1;Page 4	+1.2V_LOM	C492.1;Page 27
CLK_VDD48	C330.1;Page 4	+1.2V_AVDDL	L55.2;Page 27
CLK_VDDA	C248.1;Page 4	+1.2V_GPHY_PLLVDD	L52.2;Page 27
+3.3V_RUN_CLK	C246.1;Page 4	+1.2V_PCIE_PLLVDD	L61.2;Page 27
V_CPU_GTLREF	R54.1;Page 5	+1.2V_PCIE_SDVDD	L16.2;Page 27
+1.05V_VCCP_NB_CPU_VREF	C43.1;Page 7	CODEC_DVDD_CORE	U31.1;Page 29
V_DDR_NB_REF	C616.1;Page 9	CODEC_DVDD_CORE_PIN40	U31.40;Page 29
+1.8V_RUN_NB_IOPLLVDD18	C168.1;Page 7	+5V_SPK_AMP	L50.2;Page 30
+1.2V_RUN_NB_IOPLLVDD12	C133.1;Page 7	+VDDA	C268.1;Page 30
+1.8V_RUN_NB_PLLVDD18	C35.1;Page 10	+3.3V_CARDSUS	C403.1;Page 31
+1.2V_RUN_NB_PLLVDD12	C55.1;Page 10	+1.5V_CARD	C765.1;Page 31
+1.2V_NB_VDDPLL_PCIE	C124.1;Page 10	+3.3V_CARD	C390.1;Page 31
+1.8V_RUN_NB_AVDDD	C88.1;Page 10	+3.3V_WLAN	U98.6;Page 32
+1.8V_RUN_NB_AVDDQ	C49.1;Page 10	+3.3V_RUN_HDD	U100.6;Page 33
+1.8V_RUN_NB_VDDLT18	C129.1;Page 10		
+1.8V_RUN_NB_LTP18VDD	C21.1;Page 10		
+3.3V_RUN_NB_AVDD	C65.1;Page 10		
+3.3V_RUN_NB_VDDR33	C66.1;Page 10		
+3.3V_RUN_NB_VDDLT33	C130.1;Page 10		
+3.3V_RUN_NB	U22.6;Page 10		
+1.8V_RUN_NB_VDD18CPU	C115.1;Page 11		
+1.8V_RUN_NB_VDD18MEN	C228.1;Page 11		
+1.2V_RUN_NB_VPCIE	C179.1;Page 11		
5V_CRT_S0	C426.1;Page 16		
LCDVDD	U11.4;Page 17		

Power Sequence

Signal Name	Test Position	Signal Name	Test Position
+RTC_CELL	C258/1 ; Page 18	+NB_VCORE	C150/1 ; Page 11
+DC_IN	U5/1 ; Page 41	RUNPWROK	U107/8 ; Page 48
+SDC_IN	U12/8 ; Page 41	+VCC_CORE	TC2/1 ; Page 42
+PWR_SRC	U12/1 ; Page 41	CLK_ENABLE#	R572/1 ; Page 4
ACAV_IN	R329/2 ; Page 40	RESET_OUT#	U30/53 ; Page 35
ALWON	R43/1 ; Page 43	NB_PWRGD	R695/1 ; Page 48
+3.3V_ALW	C314/1 ; Page 35	SB_PWRGD	R695/2 ; Page 48
+5V_ALW	Q61/5 ; Page 47	H_PWRGOOD	R568/2 ; Page 5
MAIN_PWR_SW#	R511/2 ; Page 17	PLTRST#	R664/1 ; Page 18
SUS_ON	U30/34 ; Page 35	PCI_RST#	R621/2 ; Page 18
+5V_SUS	U26/4 ; Page 47	H_RESET#	R512/2 ; Page 5
+15V_ALWP	R377/1 ; Page 43	ENVDD	D4/2 ; Page 17
+3.3V_SUS	RN50/3 ; Page 35	LCDVDD	U11/4 ; Page 17
+1.8V_SUS	U82/1 ; Page 47		
+1.2V_SUS	Q50/8 ; Page 47		
SB_RSMRST#	U30/23 ; Page 35		
SIO_PWRBTN#	U30/109 ; Page 35		
SIO_SLP_S5#	U30/31 ; Page 35		
SIO_SLP_S3#	U30/30 ; Page 35		
RUN_ON	U30/35 ; Page 35		
+5V_RUN	Q61/1 ; Page 47		
+3.3V_RUN	Q32/1 ; Page 47		
+2.5V_RUN	R460/1 ; Page 47		
+1.8V_RUN	U82/4 ; Page 47		
+1.5V_RUN	R193/2 ; Page 44		
+1.2V_RUN	Q50/1 ; Page 47		
+1.05V_VCCP	R108/2 ; Page 7		

<Variant Name>

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SSID=EMI

SPR2 SPRING-24-GP 34.45T31.001
SPR1 SPRING-24-GP 34.45T31.001
SPR6 SPRING-24-GP 34.45T31.001
SPR4 SPRING-24-GP 34.45T31.001
SPR3 SPRING-24-GP 34.45T31.001
SPR5 SPRING-24-GP 34.45T31.001
SPR8 SPRING-48-GP 34.43G01.002
SPR7 SPRING-48-GP 34.43G01.002
SW3 SPRING-17 34.45V09.001
SW2 SPRING-17 34.45V09.001
SW4 SPRING-17 34.45V09.001

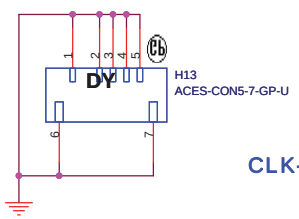
SSID=Mechanical

H5 HOLE
H7 HOLE
H11 HOLE
H3 HOLE
H14 HOLE
H16 HOLE
H8 HOLE
ZZ.0HOLE.XXX

H7,BOSS
34.4S701.001

H1 HOLE
H18 HOLE
H12 HOLE
H17 HOLE
H2 HOLE
H19 HOLE
ZZ.0HOLE.XXX

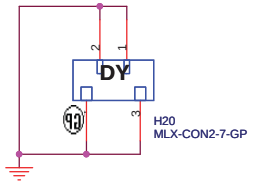
CLK-GEN Shading BOX



H6 HOLE
H15 HOLE
ZZ.0HOLE.XXX

CLK-GEN Shading-Lock
34.4S712.001
34.4S713.001

LAN Shading BOX



H10 HOLE
H9 HOLE
ZZ.0HOLE.XXX

LAN Shading-Lock
34.4S710.001
34.4S711.001

35,43	ALWON	ALWON	TP29 TPAD28
17,35	MAIN_PWR_SW#	MAIN_PWR_SW#	TP120 TPAD28
35,43	ALW_PWRGD_3V_5V	ALW_PWRGD_3V_5V	TP17 TPAD28
35,47,48	SUS_ON	SUS_ON	TP99 TPAD28
35,46,47	3.3V_SUS_ON	3.3V_SUS_ON	TP80 TPAD28
35,44,45	DDR_ON	DDR_ON	TP129 TPAD28
35,45	1.8V_SUS_PWRGD	1.8V_SUS_PWRGD	TP8 TPAD28
35,46	1.2V_SUS_ON	1.2V_SUS_ON	TP110 TPAD28
46,48	1.2V_SUS_PWRGD	1.2V_SUS_PWRGD	TP186 TPAD28
20,23,35,48	SUSPWROK	SUSPWROK	TP191 TPAD28
20,35	SB_RSMRST#	SB_RSMRST#	TP139 TPAD28
20,35	SIO_PWRBTN#	SIO_PWRBTN#	TP119 TPAD28
20,35	SIO_SLP_S5#	SIO_SLP_S5#	TP16 TPAD28
20,35	SIO_SLP_S3#	SIO_SLP_S3#	TP14 TPAD28
17,35,47,48	RUN_ON	RUN_ON	TP190 TPAD28
35,47	3.3V_RUN_ON	3.3V_RUN_ON	TP177 TPAD28
23,48	2.5V_RUN_PWRGD	2.5V_RUN_PWRGD	TP98 TPAD28
35,47	1.8V_RUN_ON	1.8V_RUN_ON	TP175 TPAD28
35,44	0.9V_DDR_VTT_ON	0.9V_DDR_VTT_ON	TP56 TPAD28
35,44	1.5V_RUN_ON	1.5V_RUN_ON	TP150 TPAD28
44,48	1.5V_RUN_PWRGD	1.5V_RUN_PWRGD	TP192 TPAD28

36,47	1.2V_RUN_ON	1.2V_RUN_ON	TP111 TPAD28
36,48	5V_3V_1.8V_1.2V_RUN_PWRGD	5V_3V_1.8V_1.2V_RUN_PWRGD	TP97 TPAD28
36,45	1.05V_RUN_ON	1.05V_RUN_ON	TP6 TPAD28
45,46,48	1.05V_RUN_PWRGD	1.05V_RUN_PWRGD	TP194 TPAD28
35,46,48	NB_VCORE_PWRGD	NB_VCORE_PWRGD	TP193 TPAD28
35,42,48	RUNPWROK	RUNPWROK	TP189 TPAD28
35,42	IMVP_VR_ON	IMVP_VR_ON	TP149 TPAD28
4,42	CLK_ENABLE#	CLK_ENABLE#	TP160 TPAD28
35,42,48	IMVP_PWRGD	IMVP_PWRGD	TP118 TPAD28
35,48	RESET_OUT#	RESET_OUT#	TP144 TPAD28
7,35,48	NB_PWRGD	NB_PWRGD	TP187 TPAD28
20,23,48	SB_PWRGD	SB_PWRGD	TP188 TPAD28
5,18	H_PWRGOOD	H_PWRGOOD	TP169 TPAD28
7,18,27,31,32,35,45,46	PLTRST#	PLTRST#	TP185 TPAD28
18,25	PCI_RST#	PCI_RST#	TP5 TPAD28
3,5,7	H_RESET#	H_RESET#	TP12 TPAD28
5,7	H_ADS#	H_ADS#	TP13 TPAD28

<Variant Name>

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/11/03	X00	1	18	REMOVE DVI CHIP TO MEDIA SLICE SIDE	Change SPEC	EE
		2	3	Dummy ITP1		EE
		3	4	Add R616,R617, Dummy R607,R610	Ext Clock Frequency select to 133MHz	EE , SW
		4	4	Change R221,R595 to 15 ohm , RN14 to 22 ohm	EA report fail issues	EE
		5	8	Change PCI-E GPP_TX	PCI-E GPP error	EE
		6	10	Add R742 10K ohm in NB_TMDS_HPD_R	BIT issues	EE
		7	11	Change +1.8V_RUN_NB_VDD18MEN TO +1.8V_RUN_NB_VDD18MEM	BIT issues	EE
		8	12	Change R629,R630,R632,R633 to 0 ohm and Add R736,R737 100 ohm	DDR clock driver issues	EE
		9	13	Change Onboard memory to Hynix and Mircon	Sansung memory can't support issues	EE
		10	16	Change L37, L38, L39, L40, L41 to BLM18BA100SN1D	EA report fail issues	EE
		11	17	Change R47 to 150 ohm	EA report fail issues	EE
		12	17	Change LVDS1 Power circuit	LCD Power issues	EE
		13	19	Add R738,R739,R740 0 ohm connect SATA power and GND	No support SATA HDD issues	EE
		14	19	Add C776 22pF De-pop and Change R445,R514,R529 to 47 ohm	SPI ROM issues	RF
		15	20	Change Memory SMBus support to SB SMBus 0 and Del U101,RN58	Memory controller issues	SW
		16	20	Del L23 and Change AVDDRX power to +3.3V_SB_USB_TX	ATI Desgin check issues	EE
		17	25	Change signal IRQ_SERIRQ to U63/Pin H1;Change U63/Pin H2 to signal MFUNC2	TI multi function setting issues	EE , SW
		18	25	Change C385,C386 to 12PF	Crytal result issues	EE
		19	26	Change R260,R265,R294,R305 to 200 ohm , R291 to 75 ohm	SDIO Rise time fall issues	EE
		20	27	Change C510 to 33PF	Crytal result issues	EE
		21	27	Change R420 to 1.18K ohm	LOM Driver issues	EE
		22	29	Change U31/Pin 4 AUD_SPK_DET signal to U35/Pin P8	Audio detect issues	SW
		23	30	Change U32 to TI TPA6040A4 and setting	AMP Main source change issues	EE
		24	30	Change U40/Pin 5 Power to +3.3V_RUN	BIT issues	EE
2007/03/21	X01	25	30	Change C446, C453 to 1uF 25V 0603	Audio issues	EE
		26	32	Swap ESD1 and De-pop C369, C377	WWAN's SIM error	EE
		27	32	Change U98 to Vishay SI3424DV	WLAN Power issues	Power
		28	33	Change R548,R573 to 0 ohm , R575 to 47 ohm and Add C772,C773, C774 22pF De-pop	SPI ROM issues	EE
		29	35	Dummy DBG1, DBG2		EE
		30	35	Change R641 to 1M ohm	BIT issues	EE
		31	35	Change RN54,RN61,RN65,RN78 to 2.2K ohm	SUS and RUN power open two time issues	EE , SW
		32	35	Change C173 to 12PF ,C200 to 15PF	Crytal result issues	EE
		33	35	De-pop R321	BIT issues	EE
		34	35	Add R749 10K ohm to +RTL_CELL	Pen switch issues	EE , SW
		35	36	Add R269 10K ohm, Dummy R270	Board ID issues	EE , SW
		36	36	Add MEM_VEND_I Detect in U64 Pin 1	Memory controller for SPD issues	SW
		37	36	Change U64 Pin 7 signal connect GND	BIT issues	EE
		38	36	Add PEN_SW# connector to U64/Pin 119	Pen switch issues	EE , SW
		39	37	Change KB1 signal	Keyboard issues	EE , KBC
		40	37	Change LID_CL_SIO#_R to U40/Pin 2 , TABLET_DET# to HSW1/Pin 4	Hall switch support change issues	ME
		41	38	Change U85 power source to +3.3V_ALW	BIT issues	EE
		42	38	Add DOCKED signal use U85 to LOM and Change U86/Pin E3 signal to LOM_E_SWITCH	LOM Docking switch issues	EE
		43	40	Add 1K8 ohm 1206 De-pop in +VCHGR to GND	BIT issues	EE
		44	43	Change TC5 to 220U6D3V	BIT issues	EE
		45	44	Add C775 near U34/Pin 10	BIT issues	EE
		46	45	Change L63 to IND-1D5UH , TC9,TC10 to SE330U2D5VVD , R97 to 118K , R103 to 93.1K	Power issues	Power
		47	46	Change R417 to 80.6K ohm , R415 to 255K ohm , TC15 to 330U2D5V	Power issues	Power
		48	48	Change R695 to 0 ohm , Del R666, C730	Power sequence issues	Power
		49		Change Power use Gap to Clise Gap		Power

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Del C570,582,585,592,595,604,606,609,611,622	RF noise issues	RF
		2	4	Change C615,623,635 to 15pF	RF noise issues	RF
		3	11	Change C116,147,176 to 6pF, C72,231,240 to 0.1uF and ADD C801 22uF	RF noise issues	RF
		4	13	Add C802,803,804 to 4.7uF	+1.8_SUS, +0.9V_DDR_VTT, V_DDR_NB_REF ripple issues	EE
		5	17	Change C563 to Dummy	Power switch issues	EE
		6	17	Add R752 10K ohm	Cable detect setting issues	SW
		7	17	Change LCD Lunch Board Power support	Digitizer Power support	EE
		8	17	Change R98,101,701 to 470 ohm	Battery life issues	EE
		9	18	Add R753 10K ohm	Cable detect setting issues	SW
		10	19	Change Net LBF_ID0 to MEM_VEND_ID1	Onboard memory vendor support issues	EE,SW
		11	20	Change R478,479 to 10 ohm, C533,535 to 4.7pF	EMI issues	EMI
		12	22	Add SB power delay circuit	ATI power issues	EE
		13	25	Change R631 to 22 ohm, R636 to 10 ohm, C654 to 10pF and C667 to 4.7pF	EMI issues	EMI
		14	27	Add R485 0 ohm	Cable detect setting issues	SW
		15	27	Change R462 to 22 ohm and C527 to 4.7pF	EMI issues	EMI
		16	28	Change R383 to 0 ohm and L45 to Dummy	EMI issues	EMI
		17	30	Add R754 10K ohm	Cable detect setting issues	SW
		18	31	Change R308,309 to 470 ohm	Battery life issues	EE
		19	32	Add +1.5V_RUN_WLAN switching circuit	Power switch issues	EE
		20	33	Change R18,19 and C9 to Dummy	Pen detect setting issues	SW
		21	34	Add C793,794,795,796 EMI Capacitor Pad and D15,23,26 EMI Diode	EMI issues	EMI
		22	35	Add R762 0 ohm	RF noise issues	RF
		23	35	Change Net AC_OFF ti pull down	AC_OFF setting issues	EE,SW
		24	35	Change R223 to 22 ohm and C321 to 10pF	EMI issues	EMI
2007/06/25	X02	25	36	Change Board ID to X02	Board ID setting issues	SW
		26	36	Add R763 0 ohm	RF noise issues	RF
		27	37	Change R302,303 and 304 to 470 ohm	Battery life issues	EE
		28	37	Change R682 to 0 ohm	Cable detect setting issues	SW
		29	38	Add C779,782 and 786 0.1uF	RF noise issues	RF
		30	39	Add C511,785 and 787 0.1uF	RF noise issues	RF
		31	40	Change L66 part to SIL104R	Charge issues	POWER
		32	40	Add C788 to 0.1uF	RF noise issues	RF
		33	40	Add ACAV_IN detect circuit	ACAV_IN setting issues	SW
		34	42	Change C297 to 390pF, R203 to 24.3K ohm, R192 to 442K ohm, R175 to 237K ohm and C233 to 33pF	CPU power issues	POWER
		35	42	Add C777,791 0.1uF, C22,379,778,792 2200pF and R25 1 ohm	RF noise issues	RF
		36	43	Change C77,79 to 1000pF and Add C784 0.1uF	RF noise issues	RF
		37	43	Add L67,68 30 ohm Bead	RF noise issues	RF
		38	45	Change C513,532 to 1000pF and Add C780,789 1000pF, R755,756 1.2 ohm	RF noise issues	RF RF
		39	46	Add L69 60 ohm	RF noise issues	RF
		40	46	Change C451,466 to 1000pF and Add C781,790 1000pF, R757,758 1 ohm	RF noise issues	RF
		41				
		42				
		43				
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		45				
		46				
		47				
		48				

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