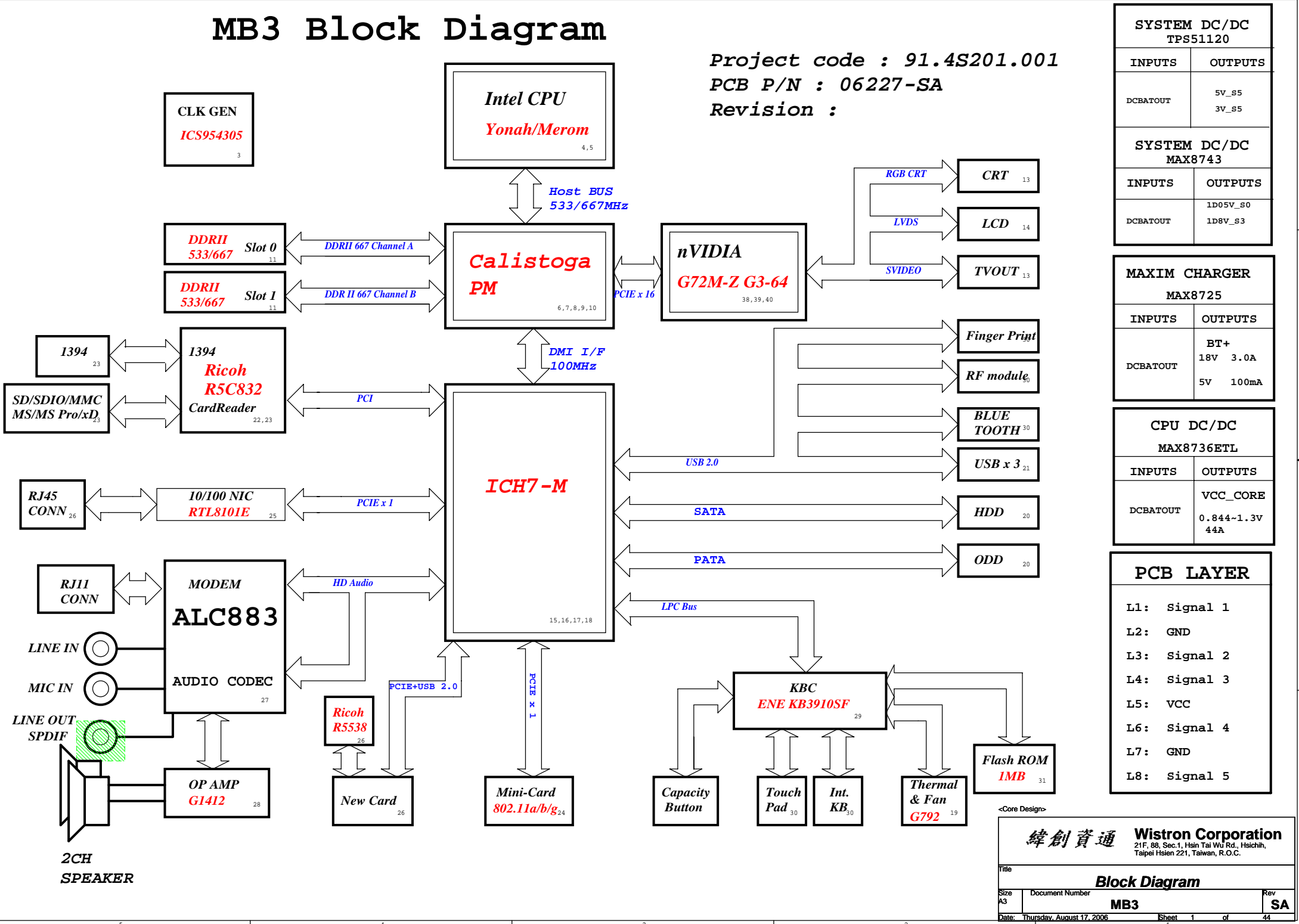


MB3 Block Diagram

Project code : 91.4S201.001
 PCB P/N : 06227-SA
 Revision :



| SYSTEM DC/DC TPS51120 | |
|--------------------------|----------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_S5 3V_S5 |

| SYSTEM DC/DC MAX8743 | |
|-------------------------|---------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0 1D8V_S3 |

| MAXIM CHARGER MAX8725 | |
|--------------------------|-----------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | BT+ 18V 3.0A 5V 100mA |

| CPU DC/DC MAX8736ETL | |
|-------------------------|-------------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE 0.844~1.3V 44A |

| PCB LAYER | |
|-----------|----------|
| L1: | Signal 1 |
| L2: | GND |
| L3: | Signal 2 |
| L4: | Signal 3 |
| L5: | VCC |
| L6: | Signal 4 |
| L7: | GND |
| L8: | Signal 5 |

<Core Design>

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| | | |
|---------------------------------|----------------------|---------------|
| Title | Block Diagram | |
| Size A3 | Document Number | Rev SA |
| Date: Thursday, August 17, 2006 | MB3 | Sheet 1 of 44 |

Calistoga Strapping Signals and Configuration

page 7

| Pin Name | Strap Description | Configuration |
|---------------|-------------------------------------|--|
| CFG[2:0] | FSB Frequency Select | 001 = FSB533 011 = FSB667 others = Reserved |
| CFG[4:3] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | | 0=Moby Dick 1=Calistoga |
| CFG7 | CPU Strap | 0 = Reserved 1 =Mobile CPU(Default) |
| CFG8 | Reserved | |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order |
| CFG[11:10] | Reserved | |
| CFG[13:12] | Reserved | |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG17 | Global R-comp Disable (All R-comps) | 0 = All R-comp Disable 1 = Normal Operation (Default) |
| CFG18 | VCC Select | 0 = 1.05V (Default) 1 = 1.5V |
| CFG19 | DMI Lane Reversal | 0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect... |
| CFG20 | SDVO/PCIE Concurrent | 0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port |
| SDVOCRTL_DATA | SDVO Present | 0 = No SDVO device present (Default) 1 = SDVO device present |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORCK In signal.

ICS954305 Spread Spectrum Select

page 3

| SS3 | SS2 | SS1 | SS0 | Spread Amount% |
|-----|-----|-----|-----|----------------|
| 0 | 0 | 0 | 0 | -0.5 |
| 0 | 0 | 0 | 1 | -1.0 |
| 0 | 0 | 1 | 0 | -1.5 |
| 0 | 0 | 1 | 1 | -2.0 |
| 0 | 1 | 0 | 0 | -0.75 |
| 0 | 1 | 0 | 1 | -1.25 |
| 0 | 1 | 1 | 0 | -1.75 |
| 0 | 1 | 1 | 1 | -2.25 |
| 1 | 0 | 0 | 0 | +/-0.25 |
| 1 | 0 | 0 | 1 | +/-0.5 |
| 1 | 0 | 1 | 0 | +/-0.75 |
| 1 | 0 | 1 | 1 | +/-1.0 |
| 1 | 1 | 0 | 0 | +/-0.25 |
| 1 | 1 | 0 | 1 | +/-0.5 |
| 1 | 1 | 1 | 0 | +/-0.75 |
| 1 | 1 | 1 | 1 | +/-1.0 |

PCI Routing

| | IDSEL | IRQ | REQ/GNT |
|--------|-------|-----|---------|
| R5C832 | 25 | | 0 |

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

| | |
|---|--------------------------------|
| ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3] | ICH6 internal 20K pull-ups |
| LAN_RXD[2:0] | ICH6 internal 10K pull-ups |
| ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS, | ICH6 internal 20K pull-downs |
| USB[7:0][P,N] | ICH6 internal 15K pull-downs |
| DD[7], SDDRQ | ICH6 internal 11.5K pull-downs |
| LAN_CLK | ICH6 internal 100K pull-downs |

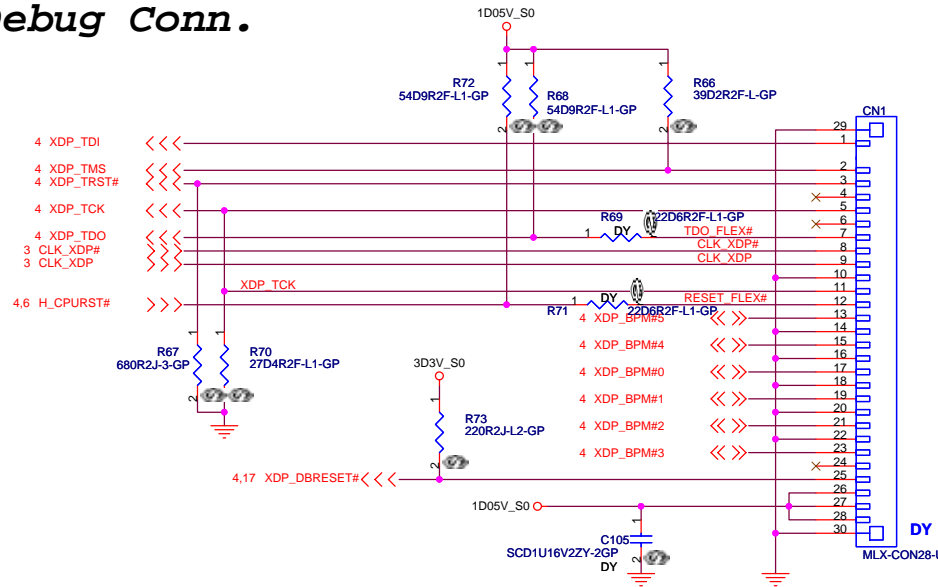
ICH7M IDE Integrated Series Termination Resistors

| | |
|--|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | approximately 33 ohm |
|--|----------------------|

History

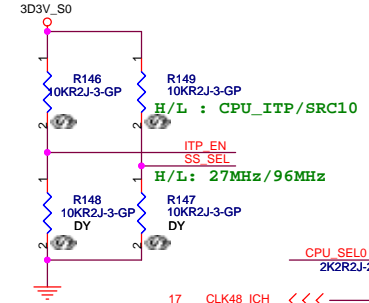
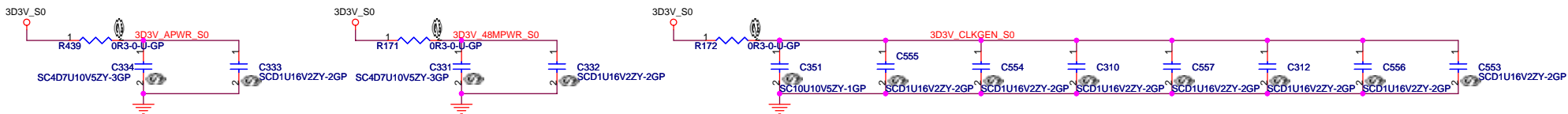
U19----->71.945PM.B0U
U27----->71.ICH7M.C0U
CHECK NEW CARD p/n for BOM

ITP Debug Conn.

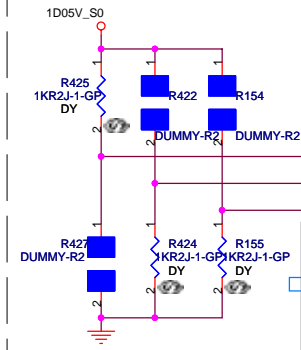
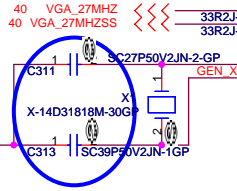
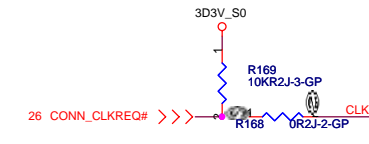


<Core Design>

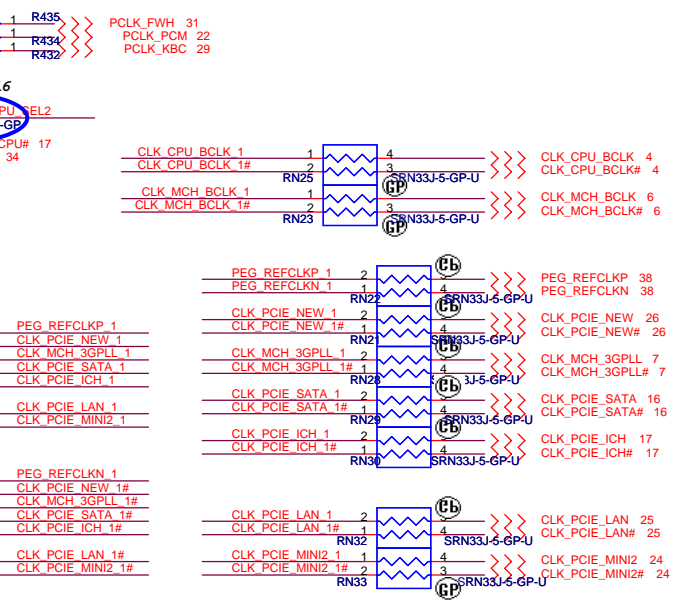
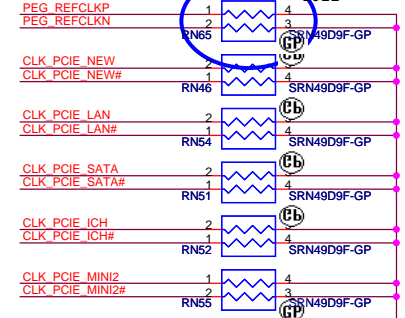
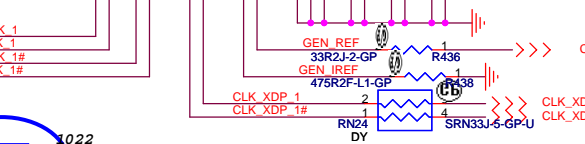
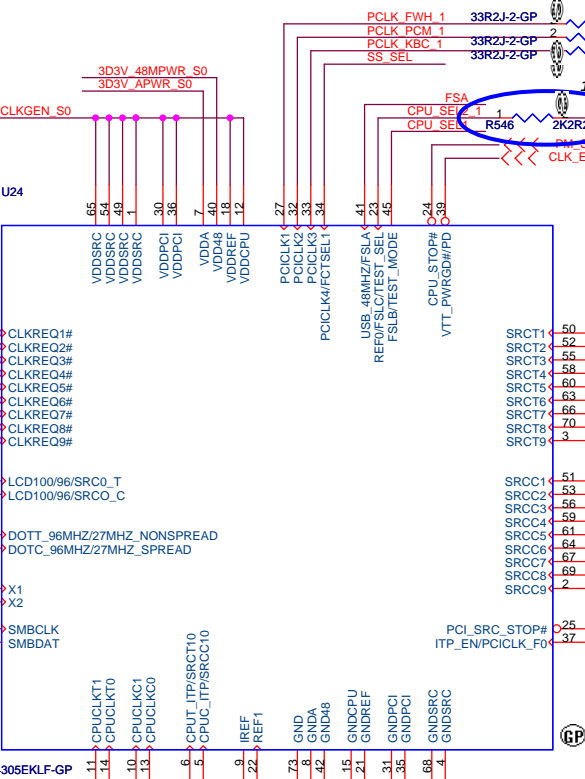
| | | | |
|---------------------------------|-----------------|--|-----------|
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| ITP | | | |
| Title | Document Number | | Rev |
| Size A3 | MB3 | | SA |
| Date: Thursday, August 24, 2006 | Sheet 2 | of 44 | |



| IN (3D3V_S0) | EN (6218_PGOOD) | OUT (VTT_PWRGD#) |
|-----------------|--------------------|---------------------|
| H | L | H |
| X | H | Hi - Z |



| FS_C | FS_B | FS_A | CPU |
|------|------|------|----------|
| 0 | 0 | 0 | 266M |
| 0 | 0 | 1 | 133M |
| 0 | 1 | 0 | 200M |
| 0 | 1 | 1 | 166M |
| 1 | 0 | 0 | 333M |
| 1 | 0 | 1 | 100M |
| 1 | 1 | 0 | 400M |
| 1 | 1 | 1 | Reserved |



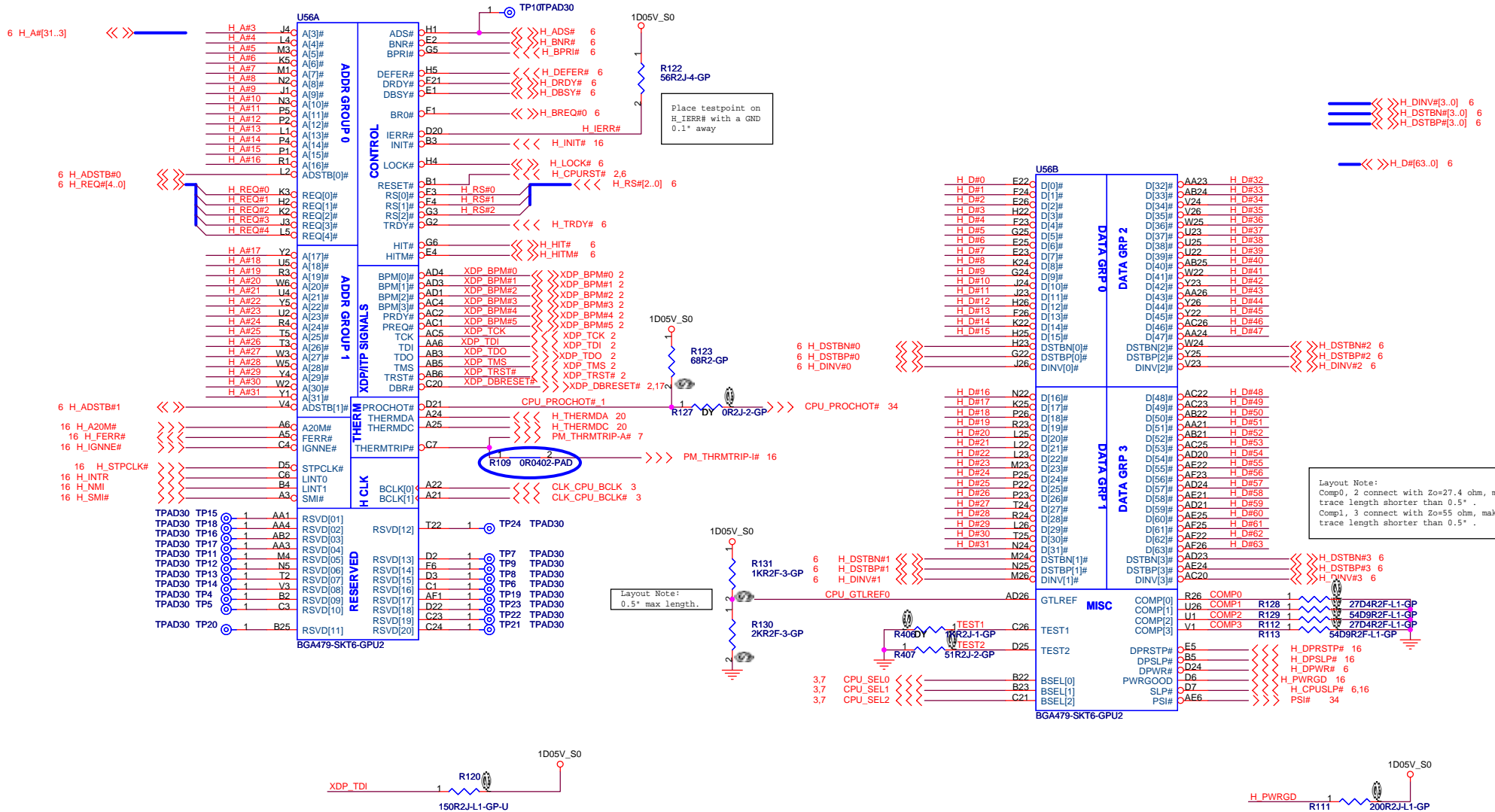
<Core Design>

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Title: **Clock Generator**

Size A3 Document Number **MB3** Rev SA

Date: Thursday, August 24, 2006 Sheet 3 of 44



<<<>>> H_DINV#[3..0] 6
 <<<>>> H_DSTBN#[3..0] 6
 <<<>>> H_DSTBP# [3..0] 6

<<<>>> H_D#[63..0] 6

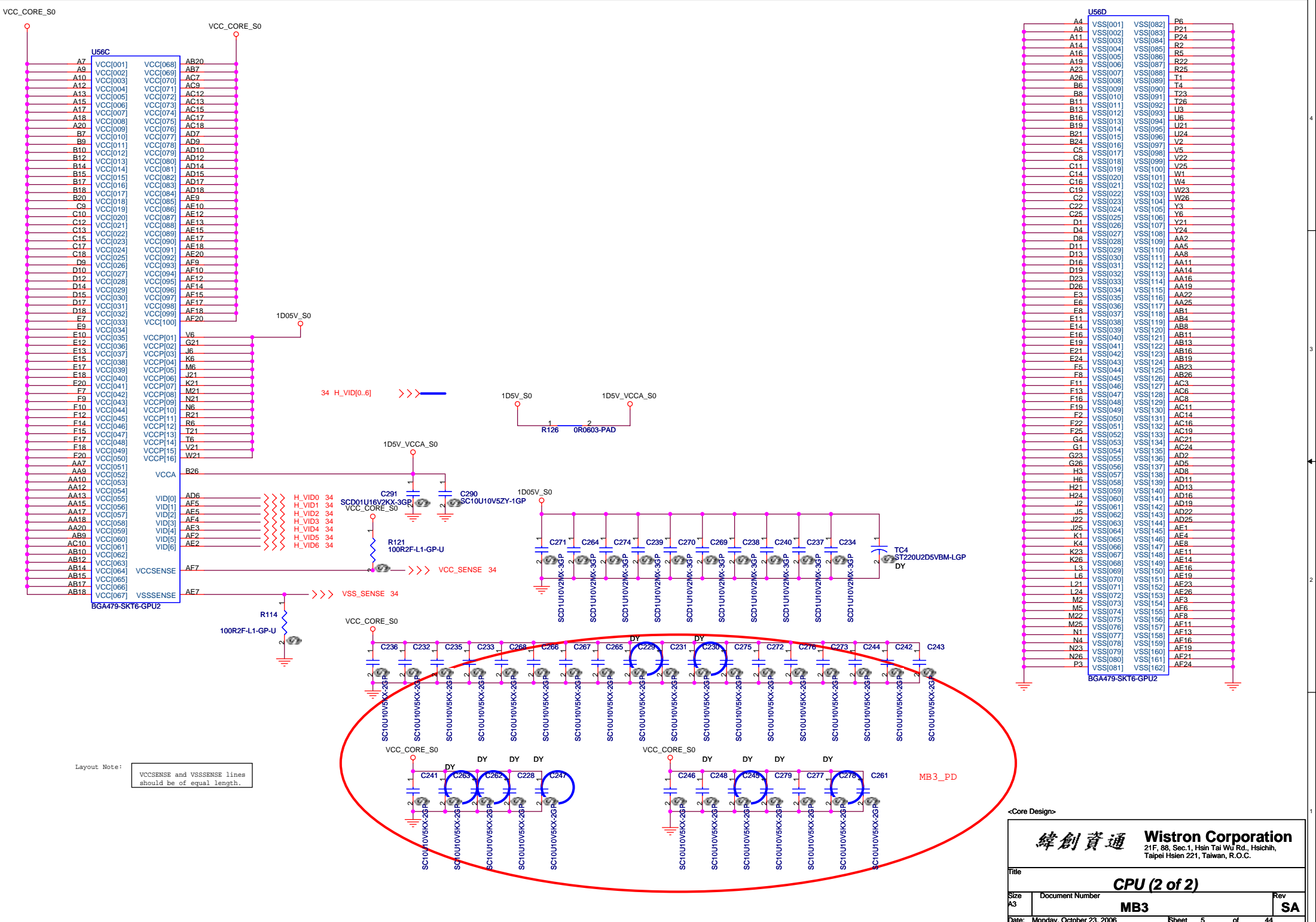
Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

<Core Design>

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Title: **CPU (1 of 2)**

| | | |
|---------------------------------|----------------------------|---------------|
| Size A3 | Document Number MB3 | Rev SA |
| Date: Thursday, August 24, 2006 | Sheet 4 of 44 | |

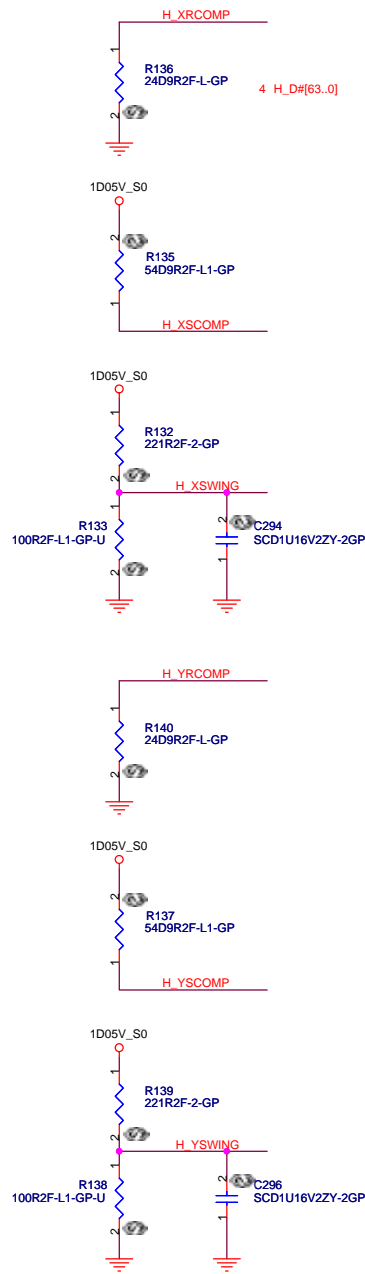


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File: **CPU (2 of 2)**

Size: A3
 Document Number: **MB3**
 Date: Monday, October 23, 2006
 Sheet: 5 of 44

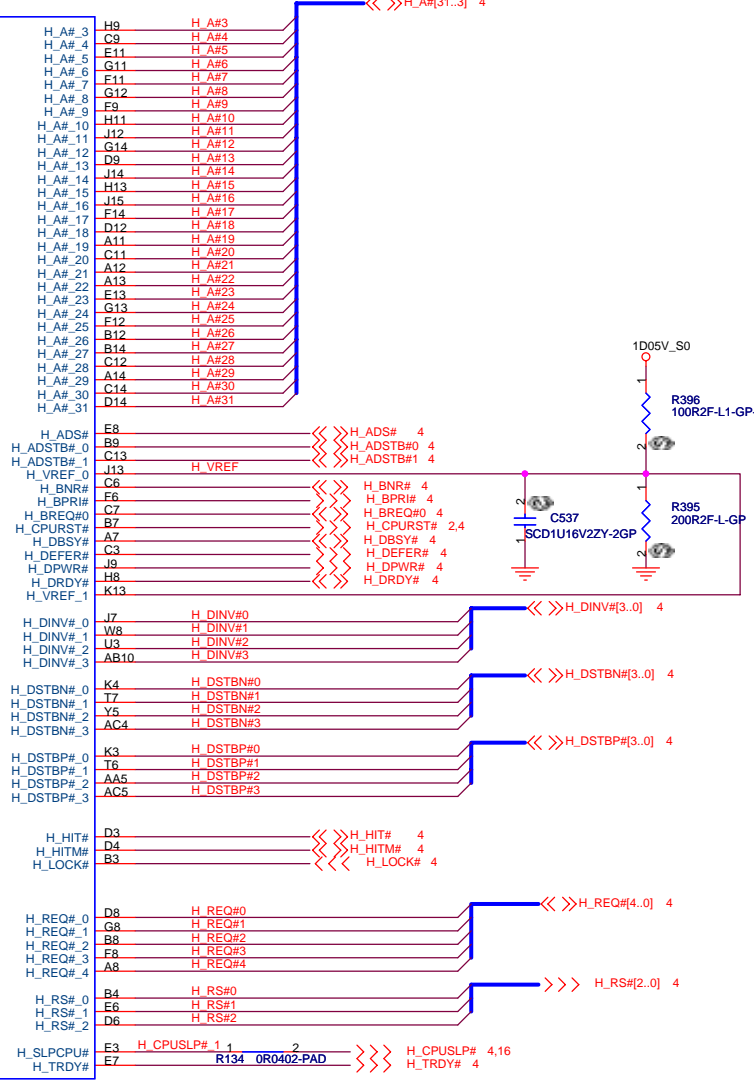
Rev: SA



Place them near to the chip

| U19A | |
|-----------------|------|
| H_D#0 | F1 |
| H_D#1 | J1 |
| H_D#2 | H1 |
| H_D#3 | J6 |
| H_D#4 | H3 |
| H_D#5 | K2 |
| H_D#6 | G1 |
| H_D#7 | G2 |
| H_D#8 | K9 |
| H_D#9 | K1 |
| H_D#10 | K7 |
| H_D#11 | J8 |
| H_D#12 | H4 |
| H_D#13 | J3 |
| H_D#14 | K11 |
| H_D#15 | G4 |
| H_D#16 | T10 |
| H_D#17 | W11 |
| H_D#18 | T3 |
| H_D#19 | U7 |
| H_D#20 | U9 |
| H_D#21 | U11 |
| H_D#22 | T11 |
| H_D#23 | W9 |
| H_D#24 | T1 |
| H_D#25 | T8 |
| H_D#26 | T4 |
| H_D#27 | W7 |
| H_D#28 | U5 |
| H_D#29 | T9 |
| H_D#30 | W6 |
| H_D#31 | T5 |
| H_D#32 | AB7 |
| H_D#33 | AA9 |
| H_D#34 | W4 |
| H_D#35 | W3 |
| H_D#36 | Y3 |
| H_D#37 | Y7 |
| H_D#38 | W5 |
| H_D#39 | Y10 |
| H_D#40 | AB8 |
| H_D#41 | W2 |
| H_D#42 | AA4 |
| H_D#43 | AA7 |
| H_D#44 | AA2 |
| H_D#45 | AA6 |
| H_D#46 | AA10 |
| H_D#47 | Y8 |
| H_D#48 | AA1 |
| H_D#49 | AB4 |
| H_D#50 | AC9 |
| H_D#51 | AB11 |
| H_D#52 | AC11 |
| H_D#53 | AB3 |
| H_D#54 | AC2 |
| H_D#55 | AD1 |
| H_D#56 | AD9 |
| H_D#57 | AC1 |
| H_D#58 | AD7 |
| H_D#59 | AC6 |
| H_D#60 | AB5 |
| H_D#61 | AD10 |
| H_D#62 | AD4 |
| H_D#63 | AC8 |
| H_XRCOMP | E1 |
| H_XSCOMP | E2 |
| H_XSWING | E4 |
| H_YRCOMP | Y1 |
| H_YSCOMP | U1 |
| H_YSWING | W1 |
| 3 CLK_MCH_BCLK | AG2 |
| 3 CLK_MCH_BCLK# | AG1 |

HOST



100mils or less from GMCH pin

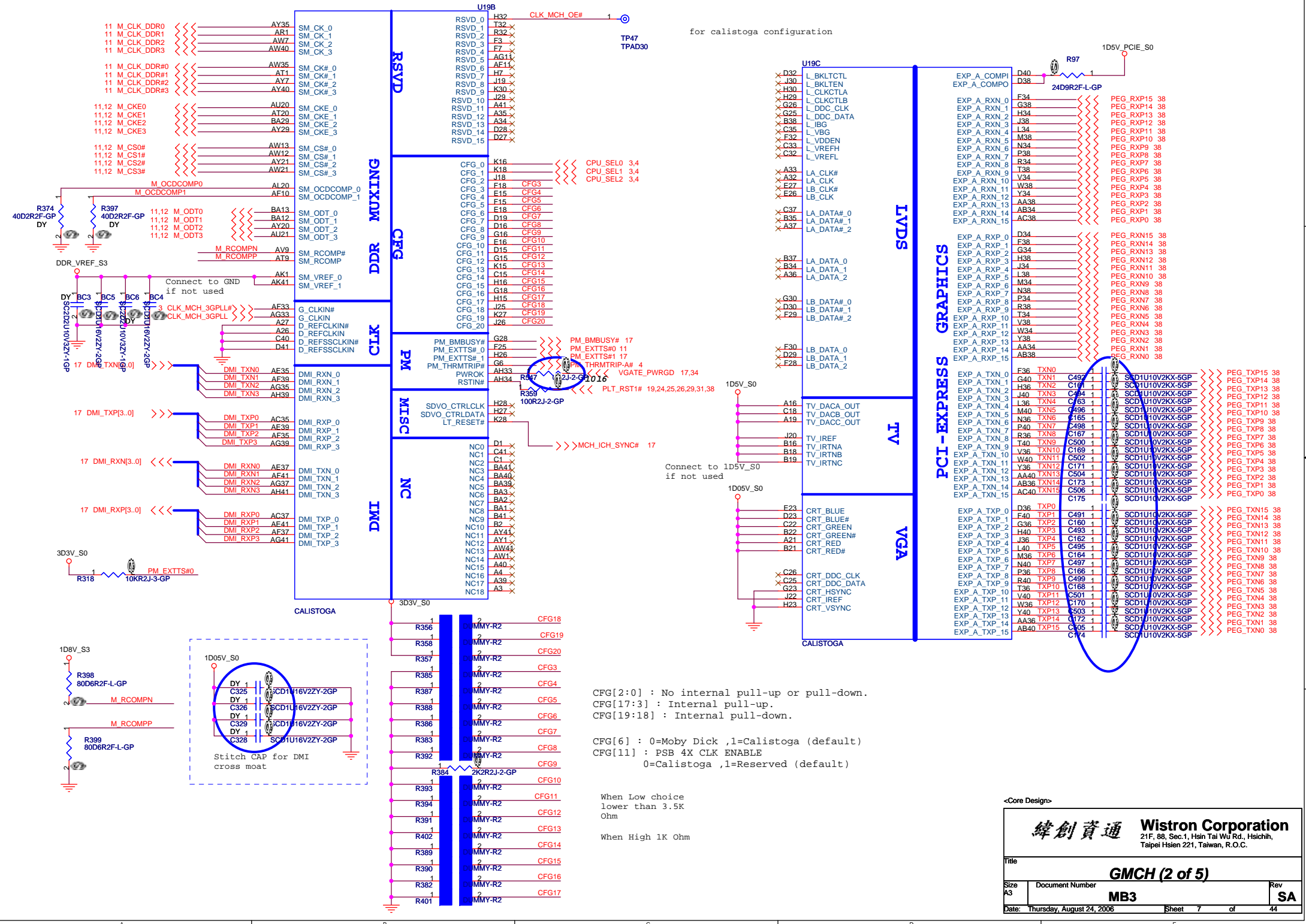
<Core Design>

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Title: **GMCH (1 of 5)**

Size: A3 Document Number: **MB3** Rev: **SA**

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for calistoga configuration

CPU_SEL0 3,4
CPU_SEL1 3,4
CPU_SEL2 3,4

PM_EXTTSS#0 11
PM_EXTTSS#1 17
THRMTRIP# 4
VGA_PWRGD 17,34
PLT_RST#1 19,24,25,26,29,31,38

MCH_ICH_SYNC# 17

Connect to 1D05V_S0 if not used

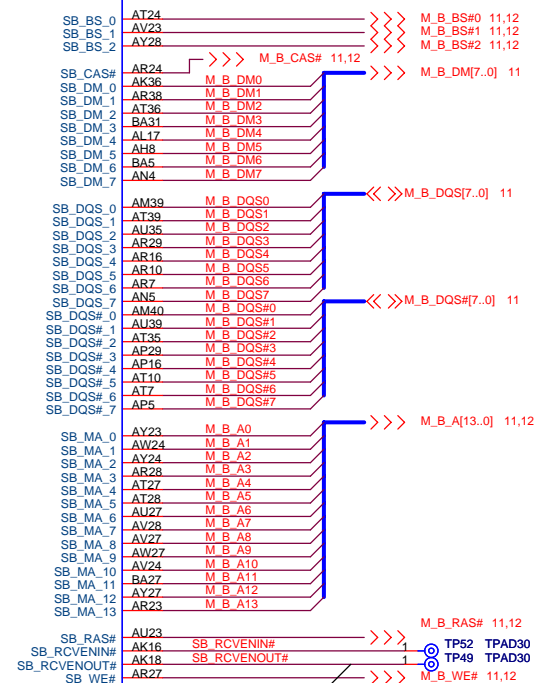
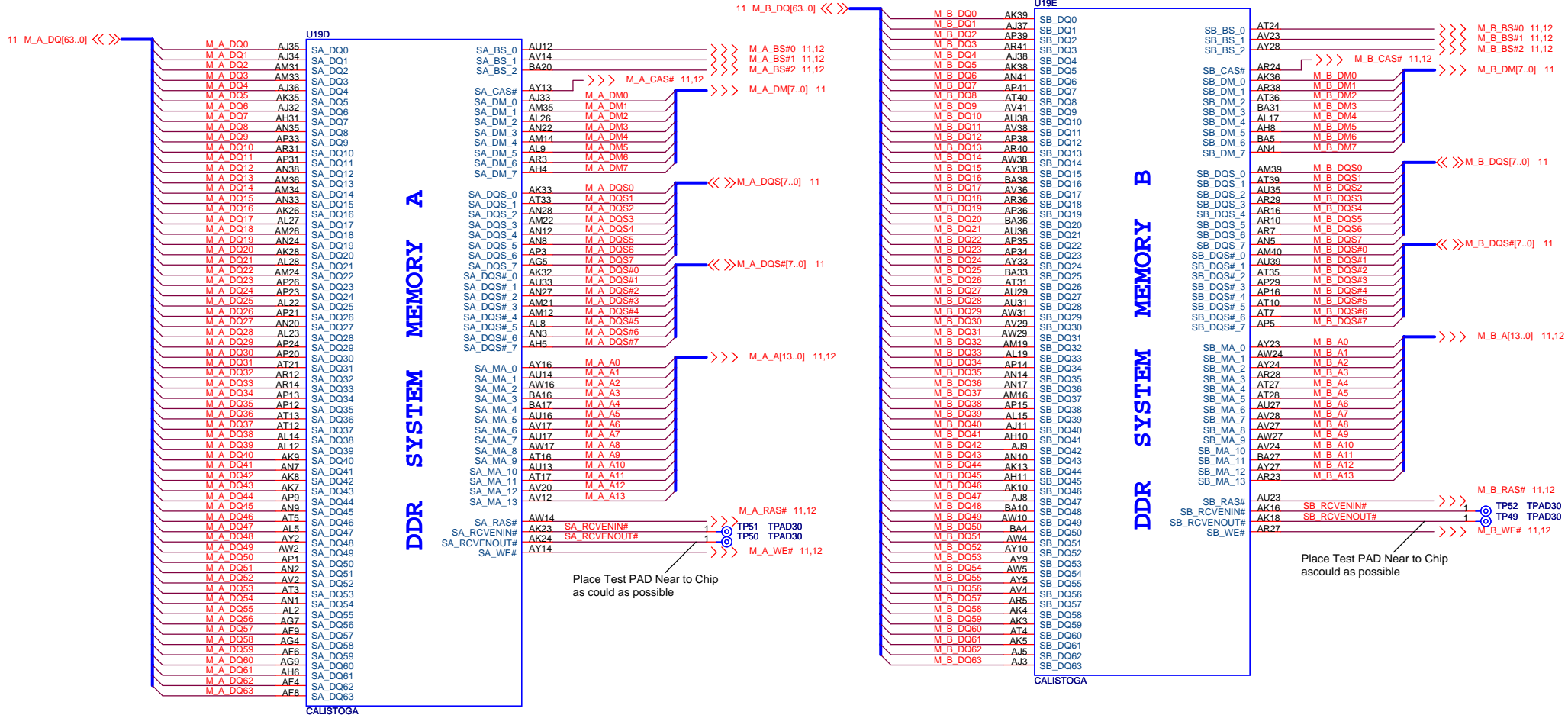
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)

When Low choice lower than 3.5K Ohm
When High 1K Ohm

<Core Design>

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| | | | |
|---------------------------------|----------------------|------------|---------------|
| Title | GMCH (2 of 5) | | |
| Size A3 | Document Number | MB3 | Rev SA |
| Date: Thursday, August 24, 2006 | Sheet 7 | of 44 | |



Place Test PAD Near to Chip
as could as possible

Place Test PAD Near to Chip
ascould as possible

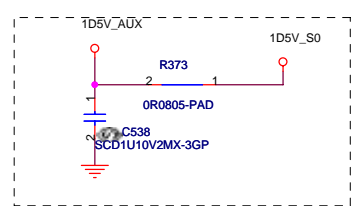
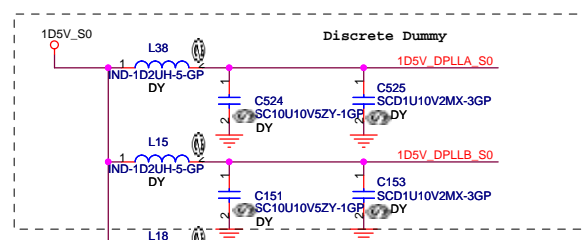
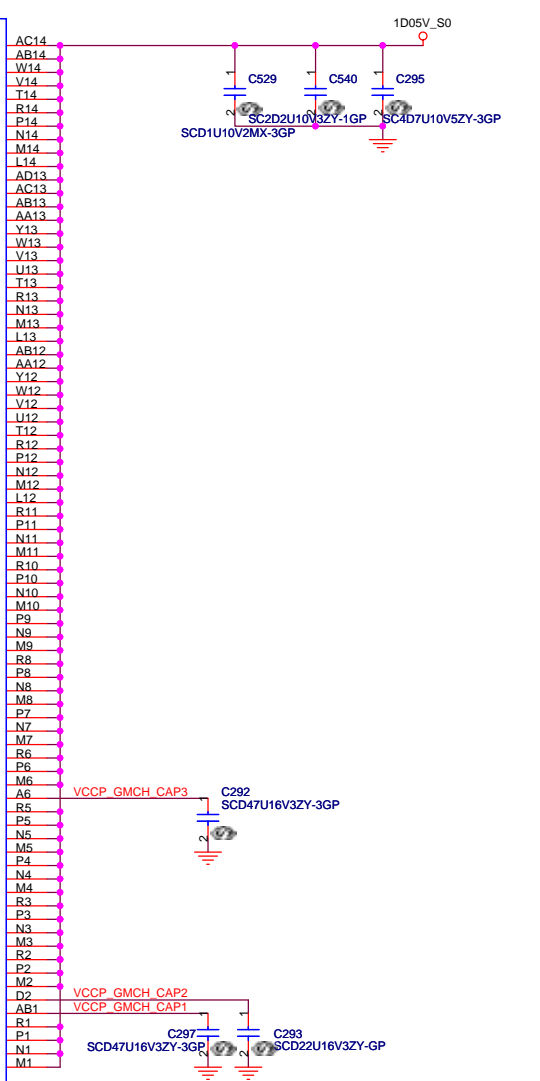
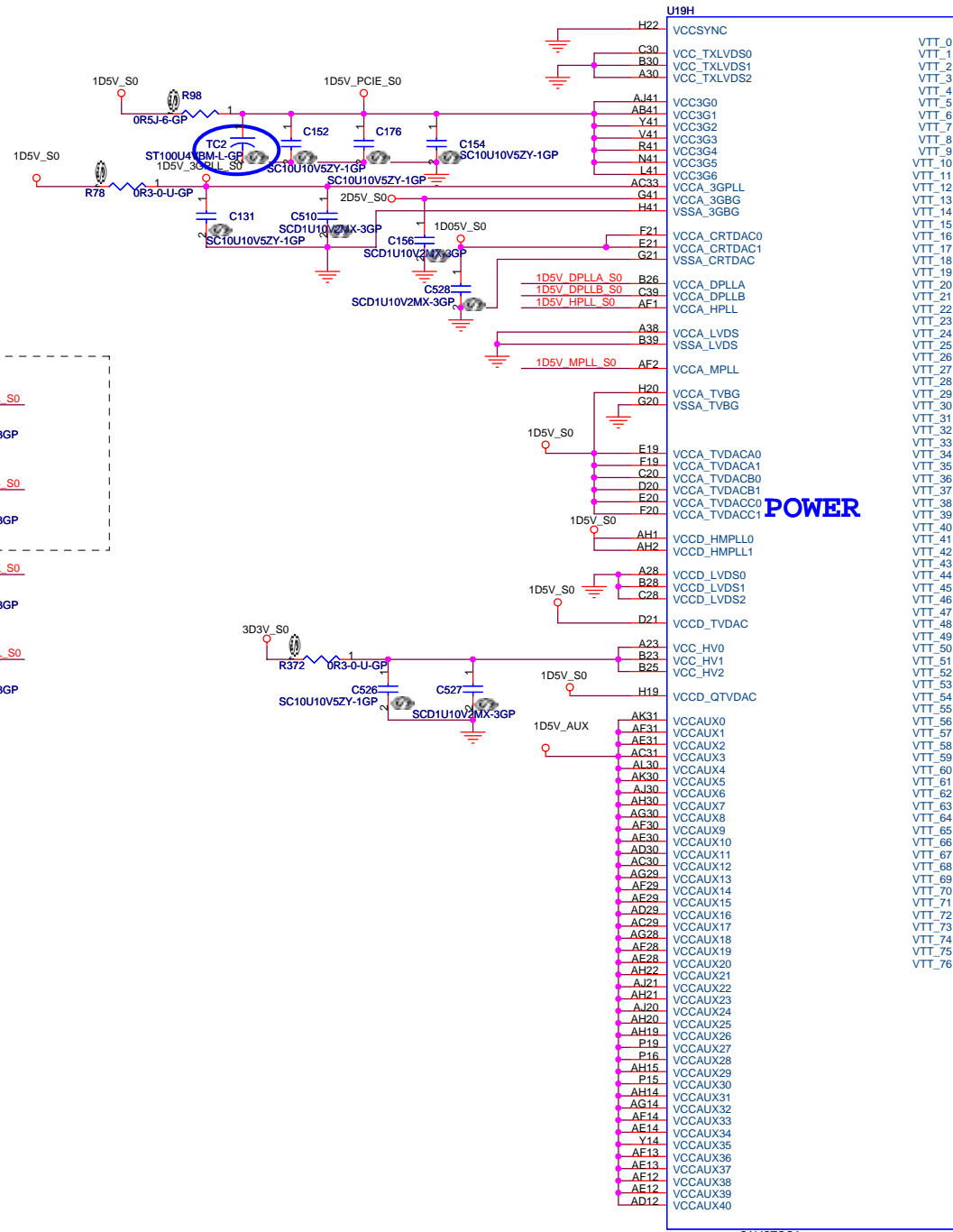
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Title: **GMCH (3 of 5)**

Size: A3 Document Number: **MB3** Rev: **SA**

Date: Thursday, August 24, 2006 Sheet: 8 of 44

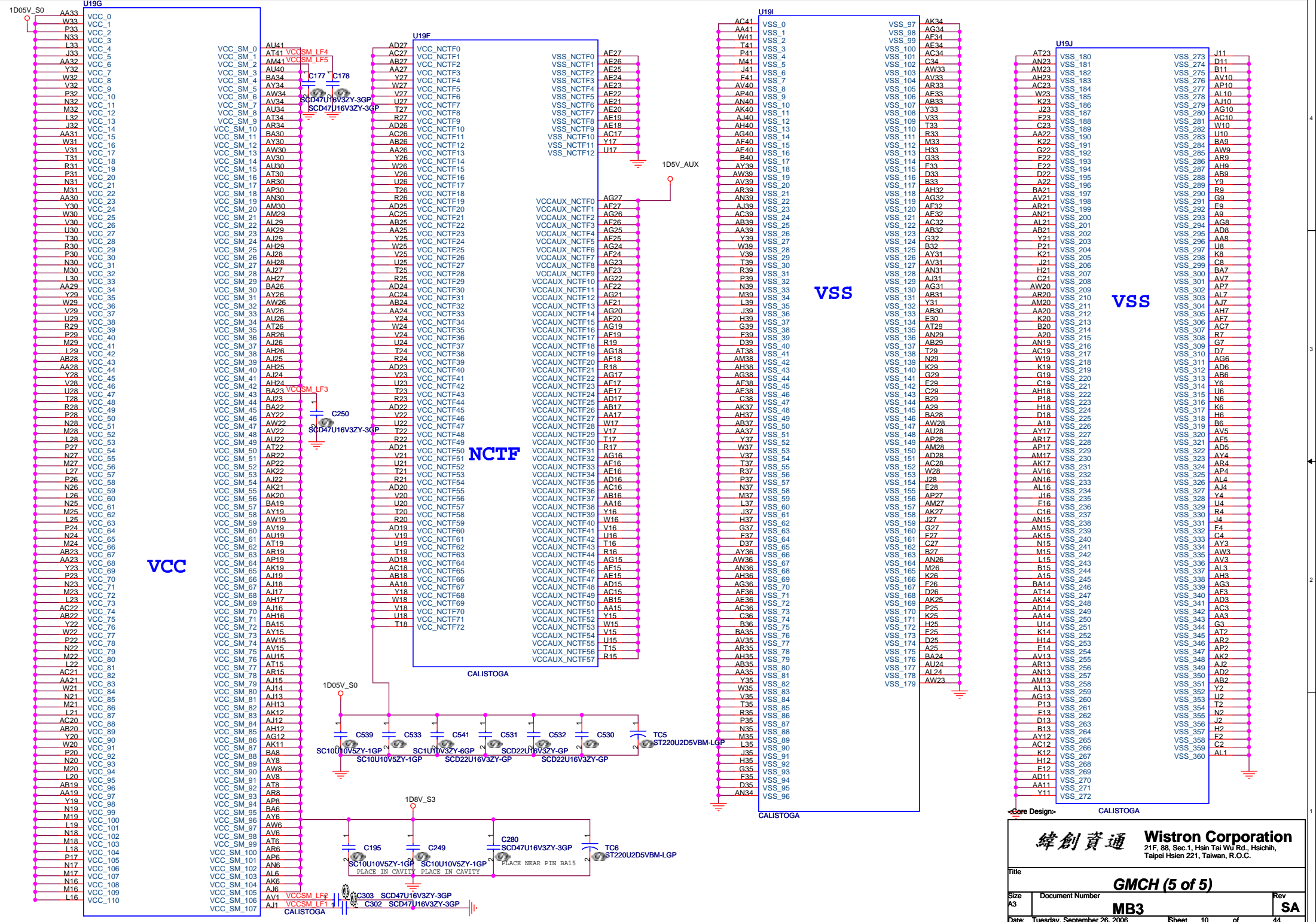


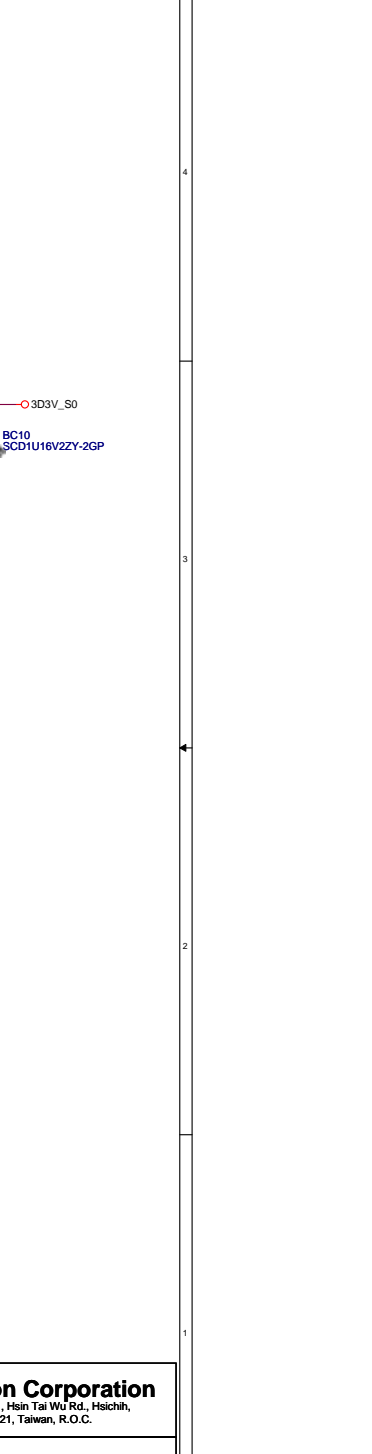
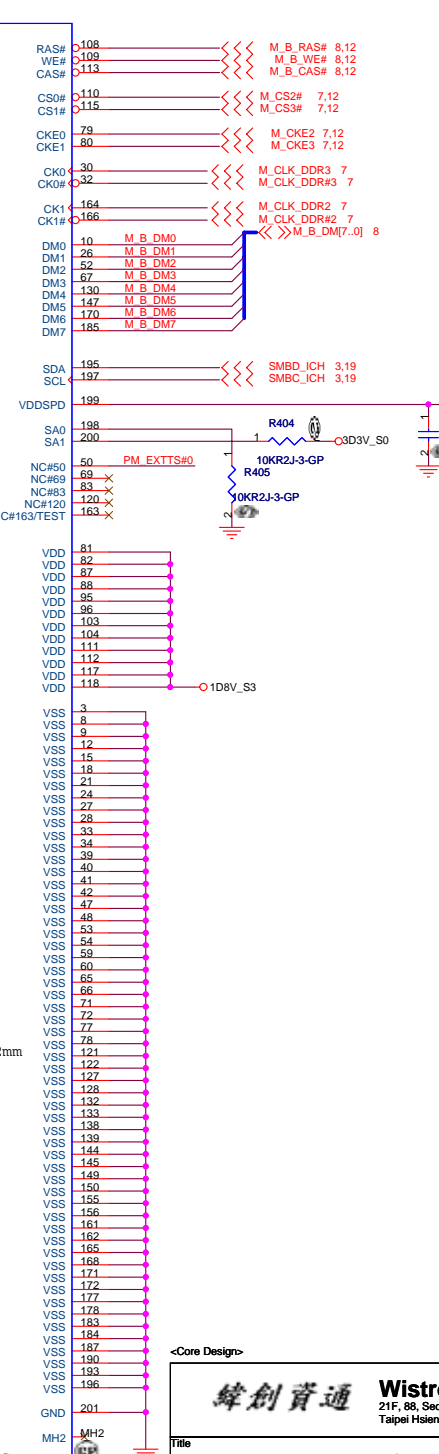
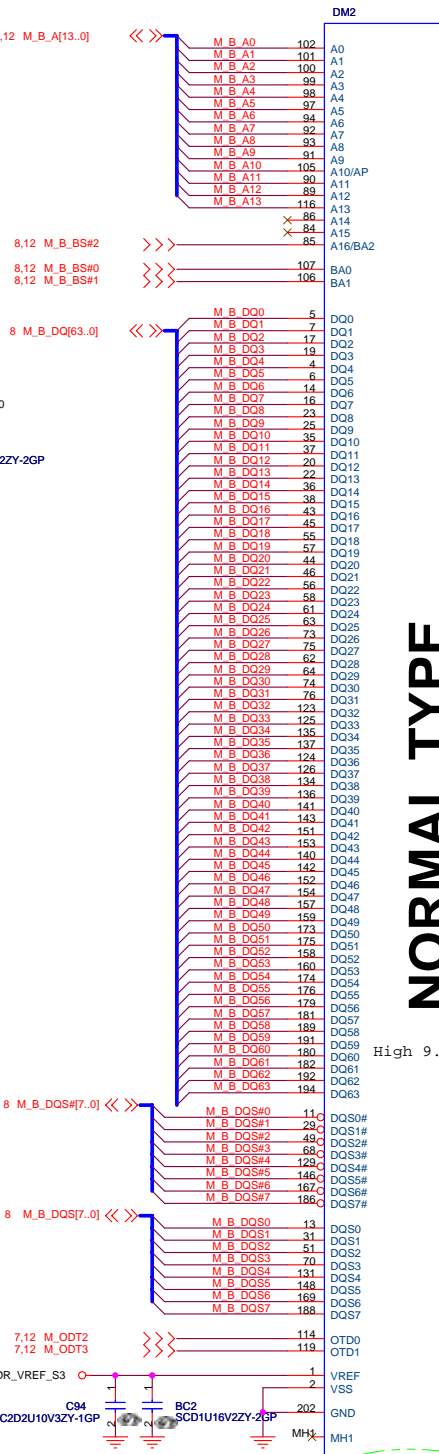
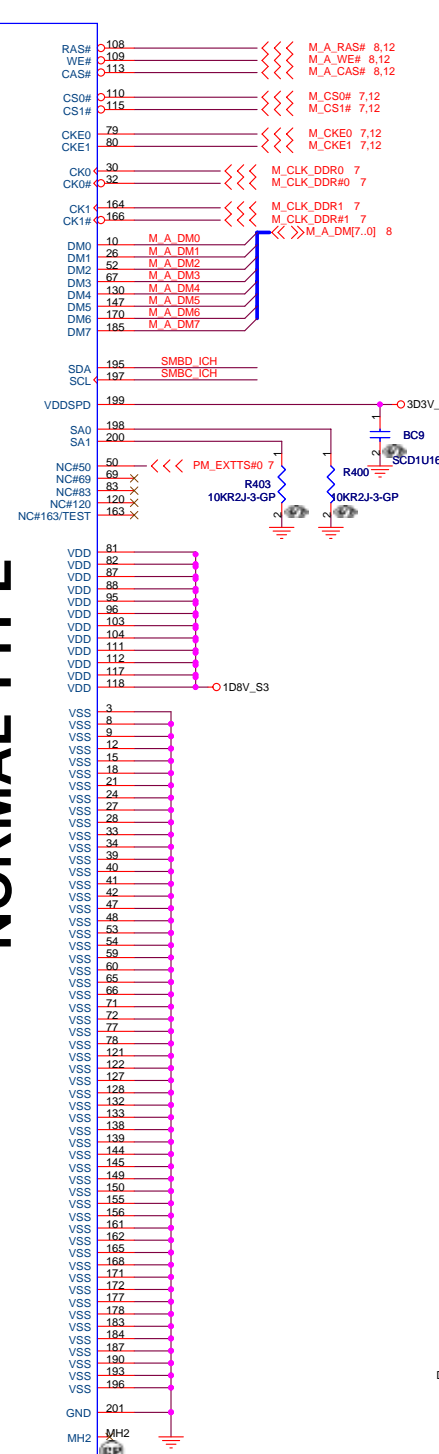
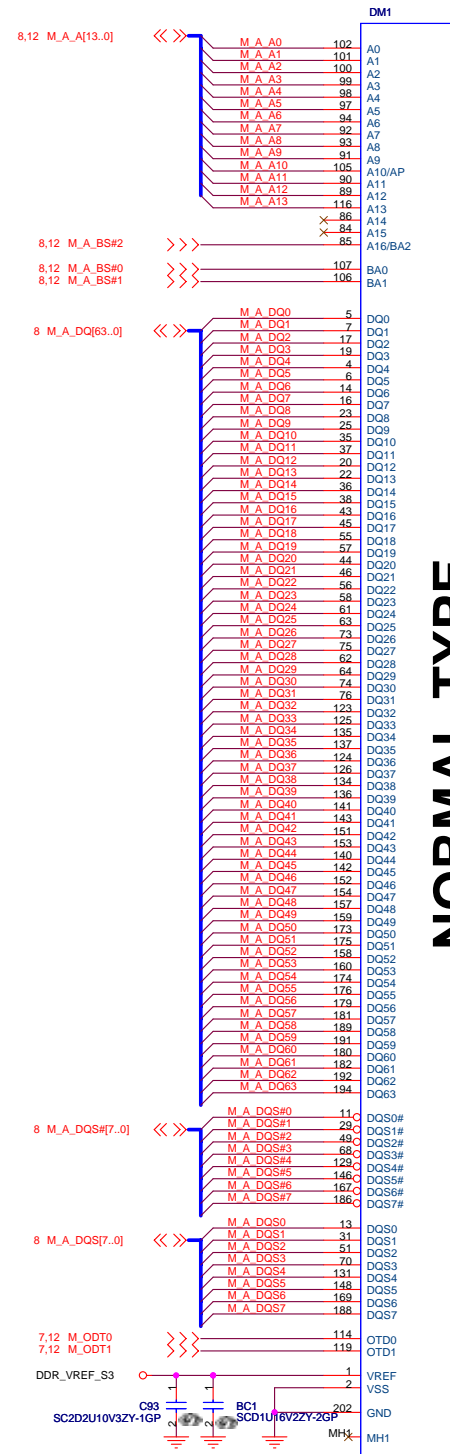
<Core Design>

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Title: **GMCH (4 of 5)**

| | | |
|---------------------------------|-----------------------------|----------------|
| Size: A3 | Document Number: MB3 | Rev: SA |
| Date: Thursday, August 17, 2006 | Sheet: 9 of 44 | |





NORMAL TYPE

NORMAL TYPE

High 9.2mm

DDR2-200P-20-GP-U1
62.10017.A41

Main Source : 62.10017.661
Second Source : 62.10017.A41

DDR2-200P-22-GP-U1
62.10017.A61 MB3-SA

<Core Design>

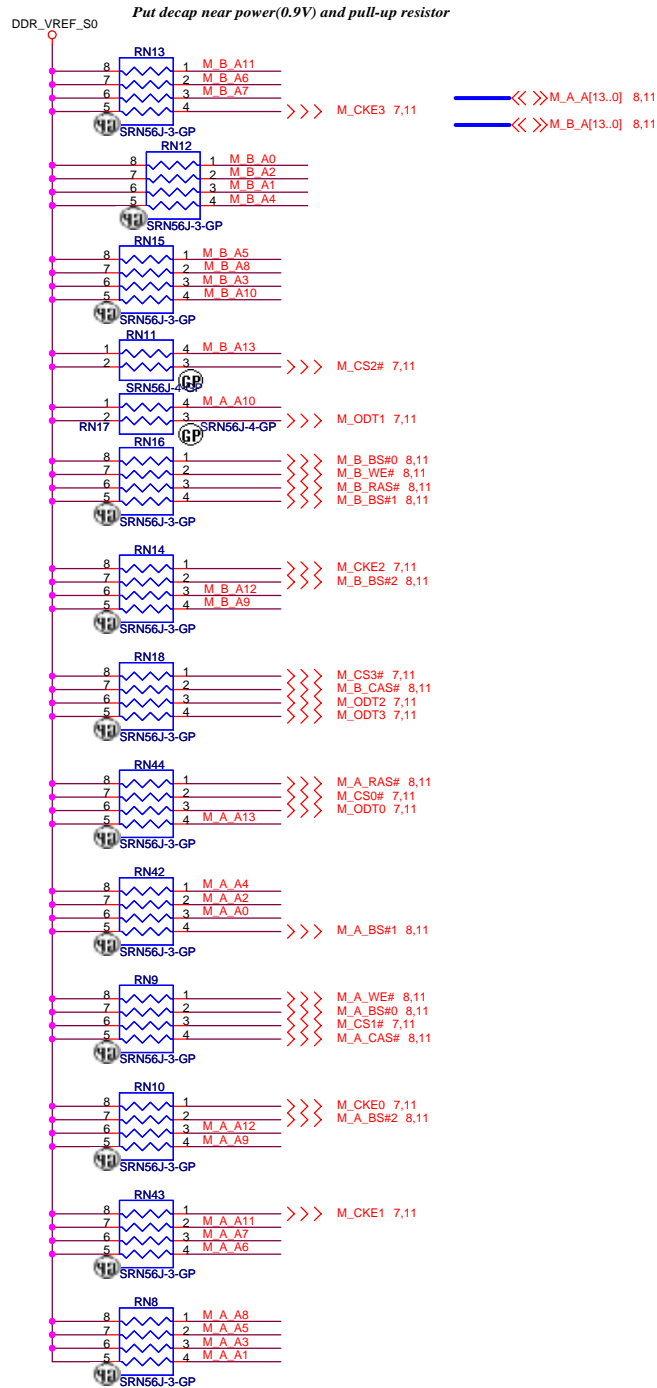
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Title: **DDR2 Socket**

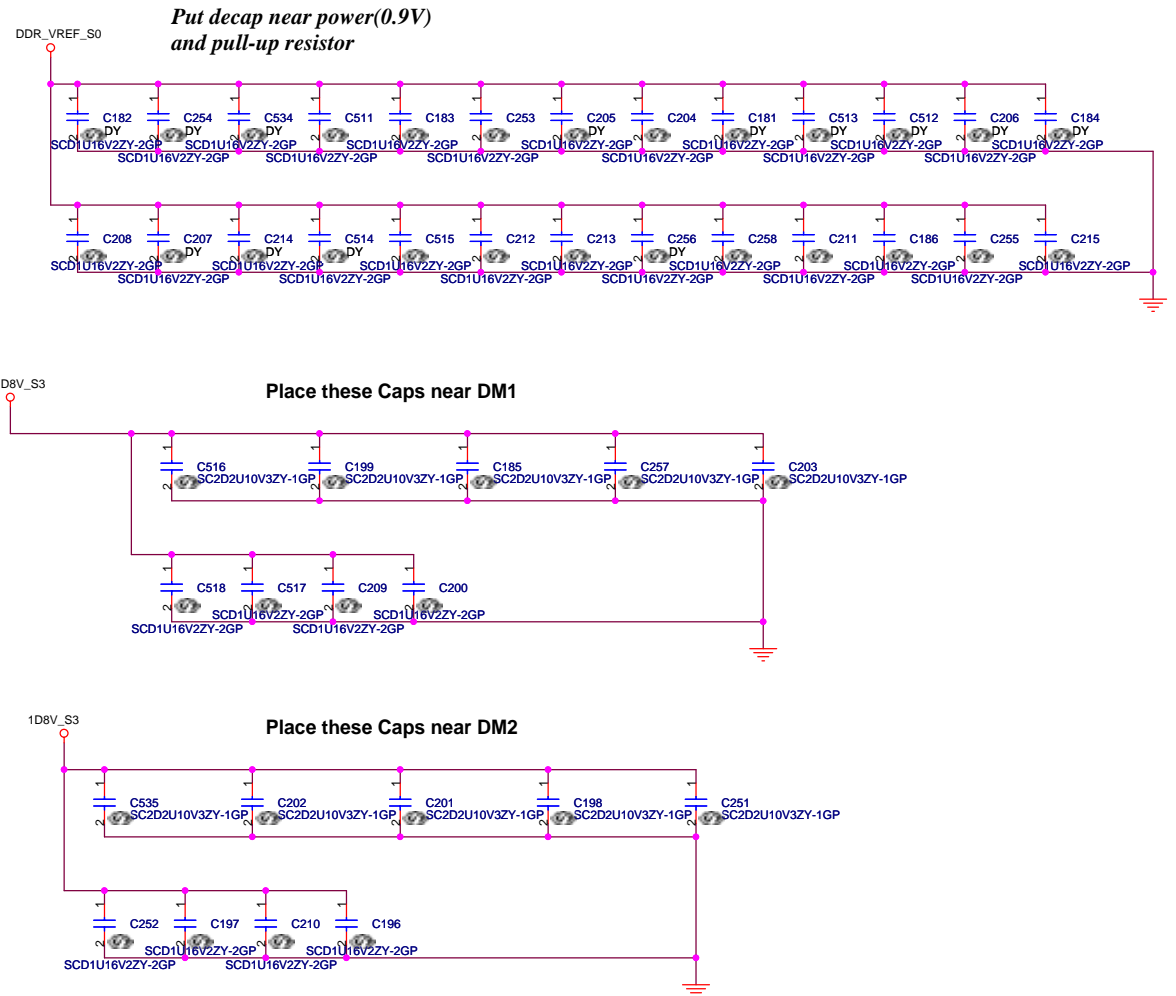
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|--------|-----------------|-----------|
| Size | Document Number | Rev |
| Custom | MB3 | SA |

Date: Thursday, August 24, 2006 Sheet 11 of 44

PARALLEL TERMINATION

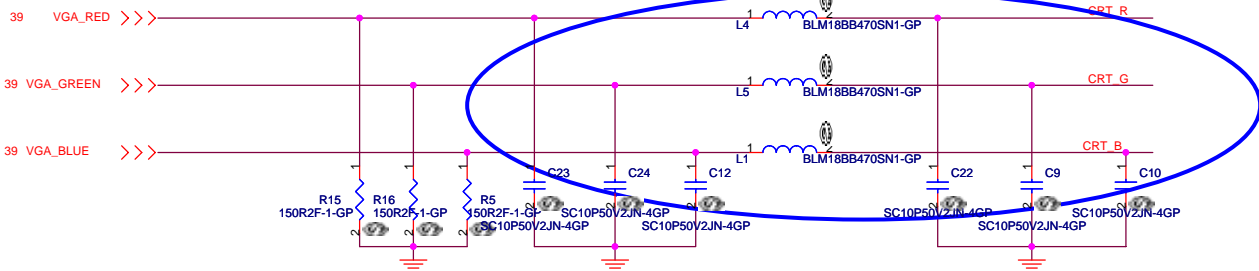


Decoupling Capacitor



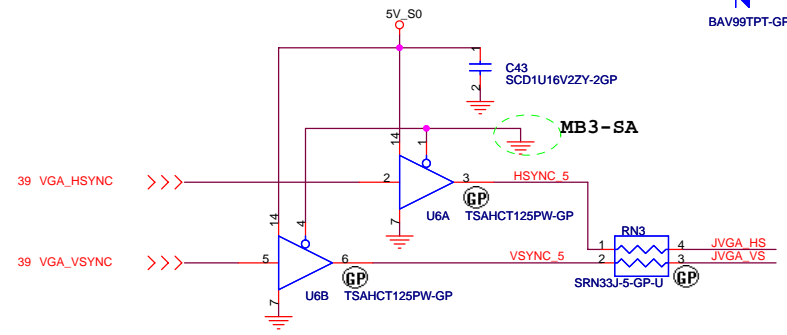
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



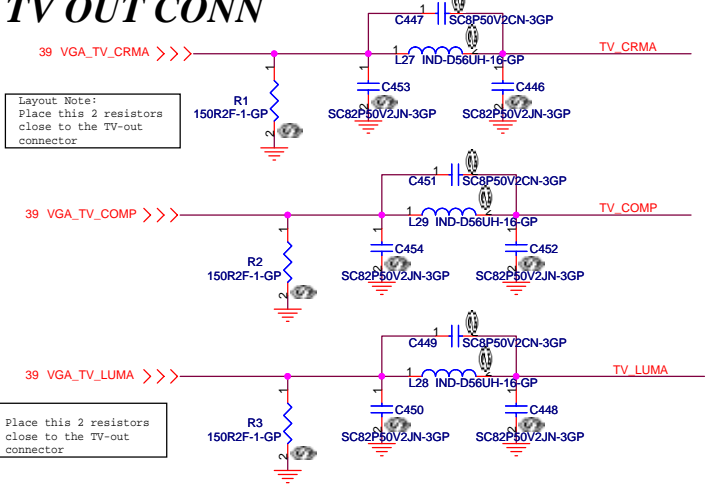
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

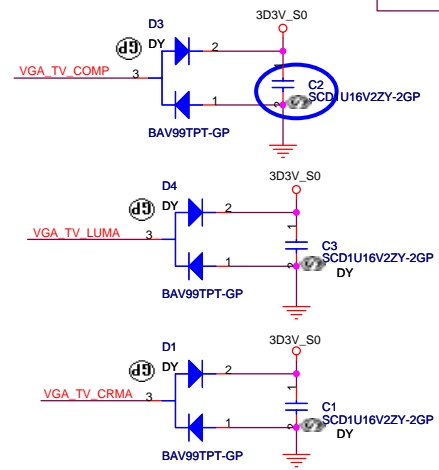
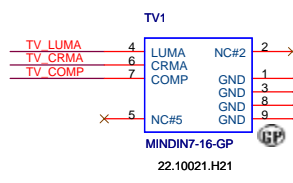
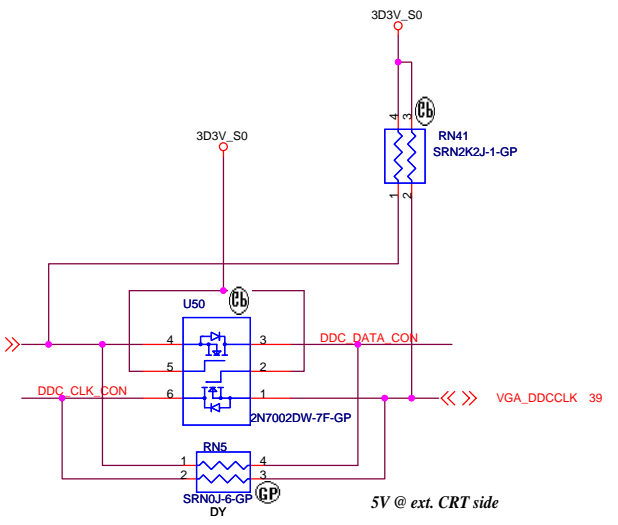
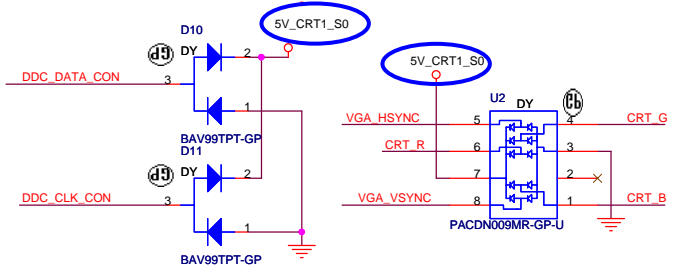
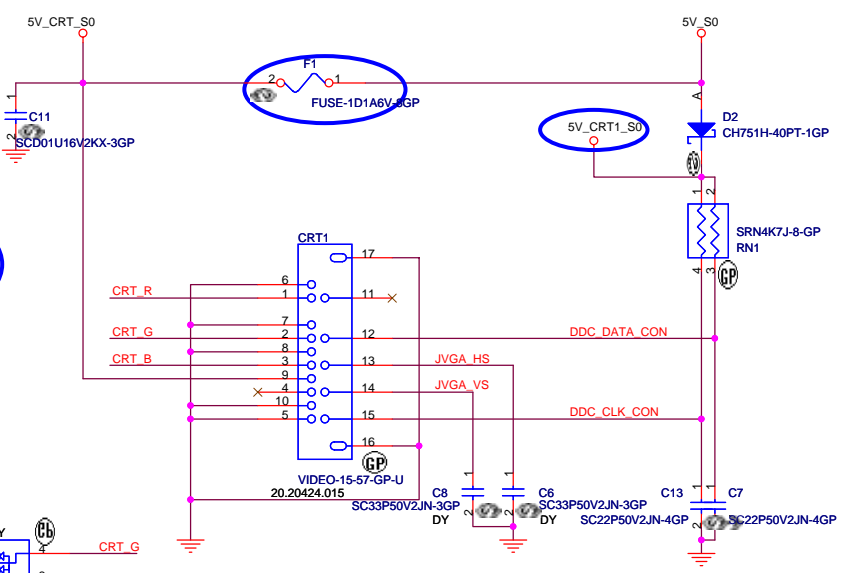


TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



Place this 2 resistors
close to the TV-out
connector



<Core Design>

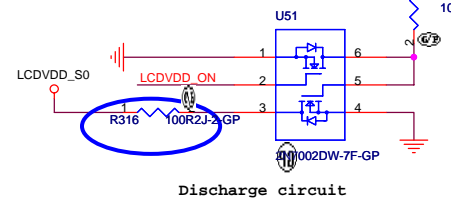
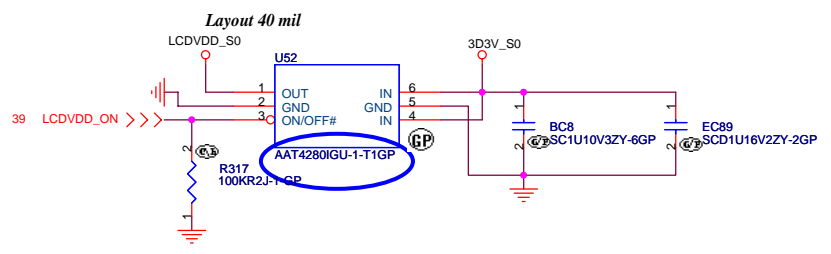
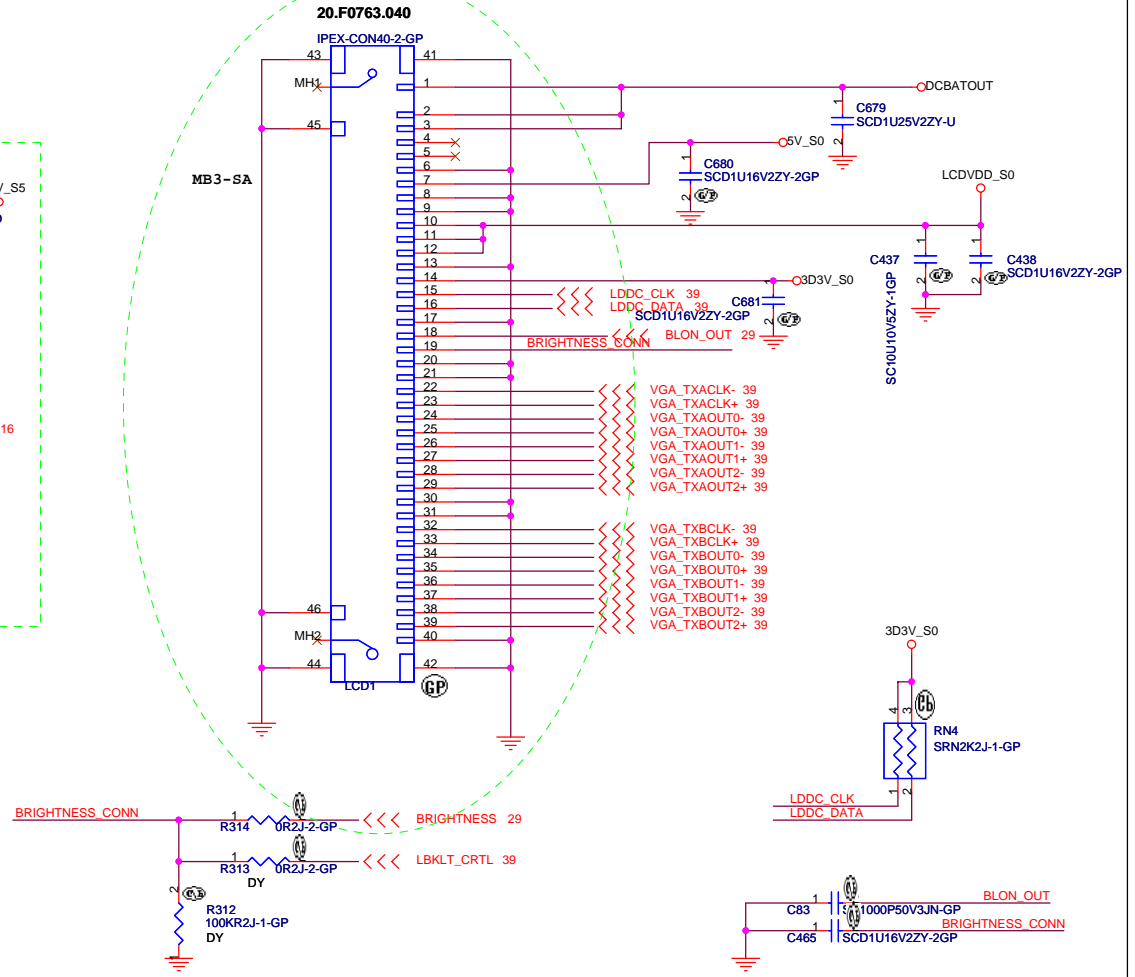
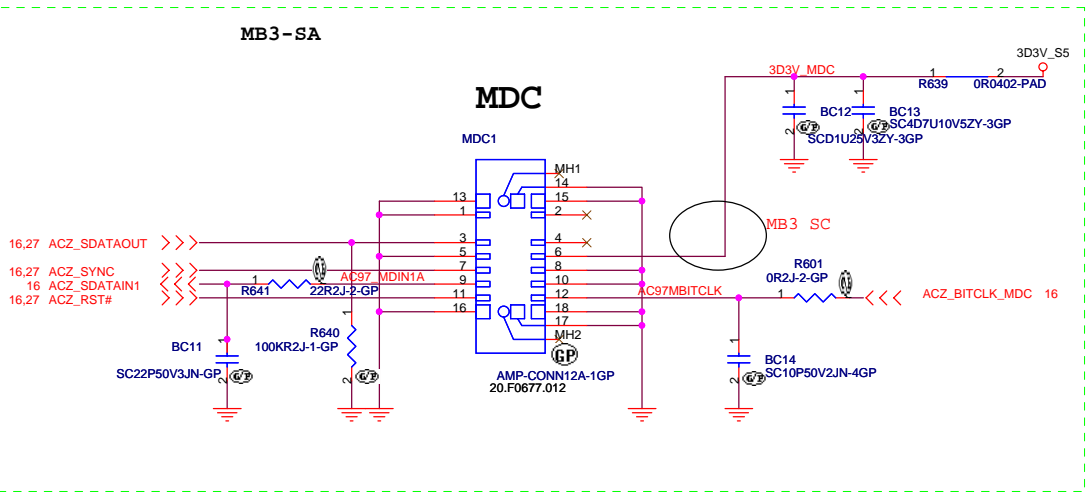
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Title: **CRT/TV Connector**

Size: A3 Document Number: **MB3** Rev: **SA**

Date: Thursday, August 24, 2006 Sheet 13 of 44

LED / INVERTER INTERFACE LCD/INV CONN



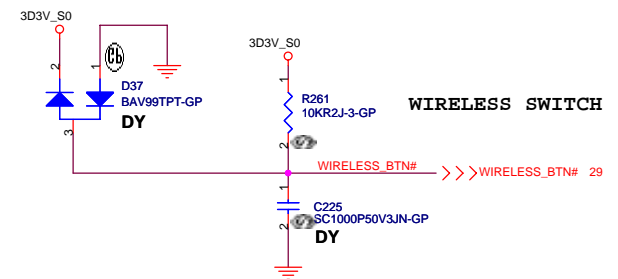
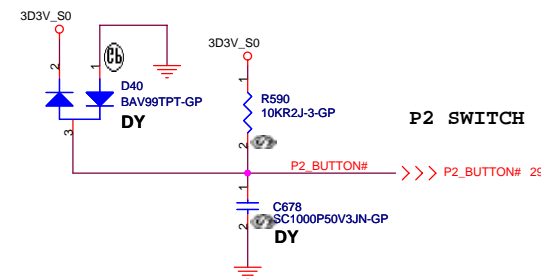
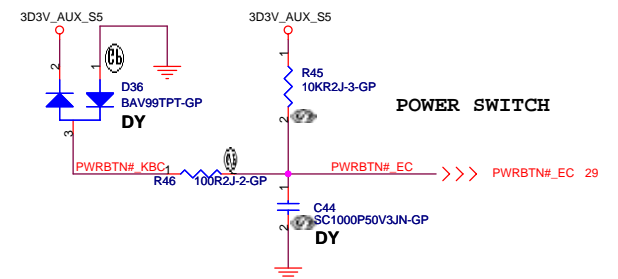
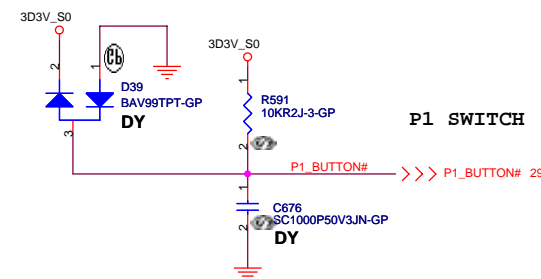
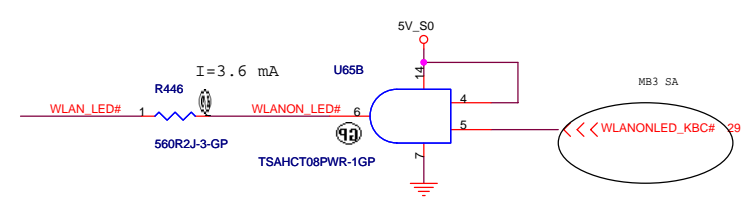
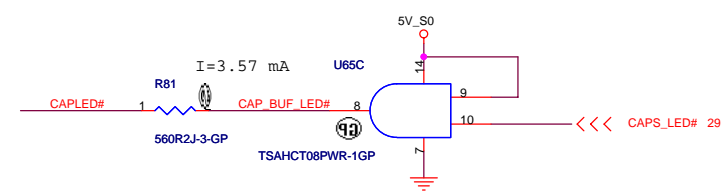
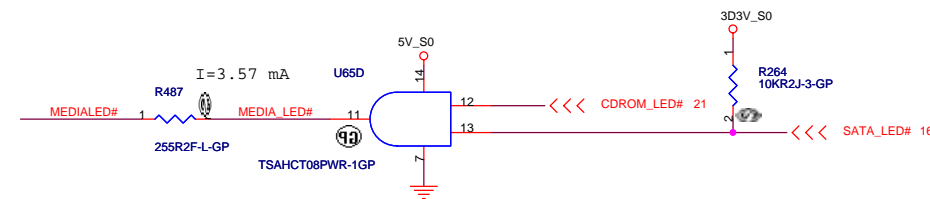
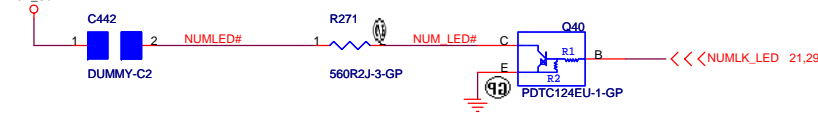
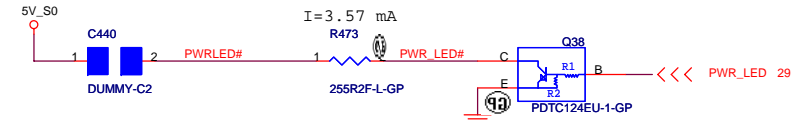
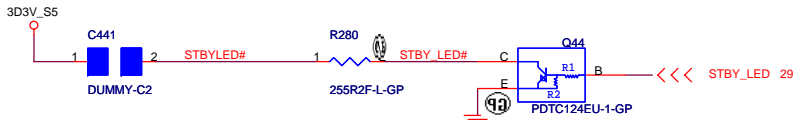
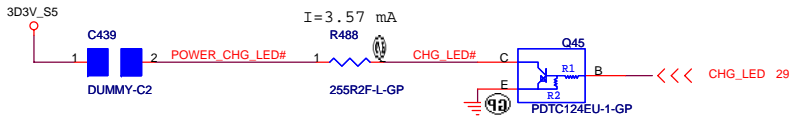
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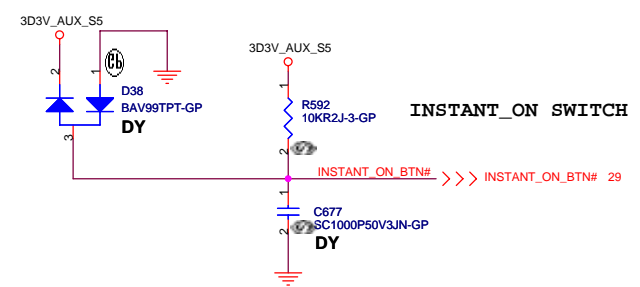
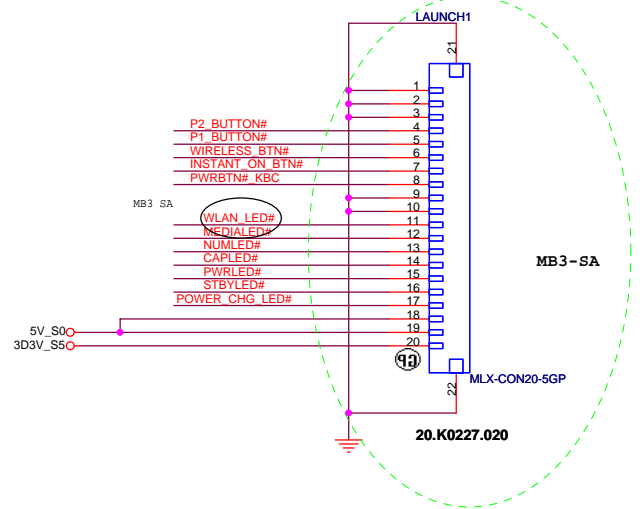
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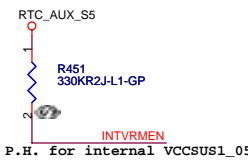
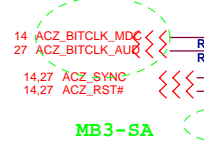
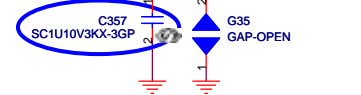
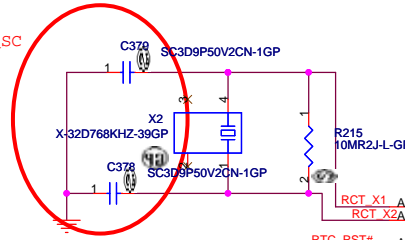
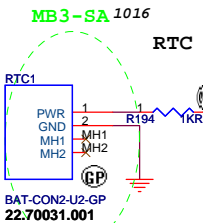
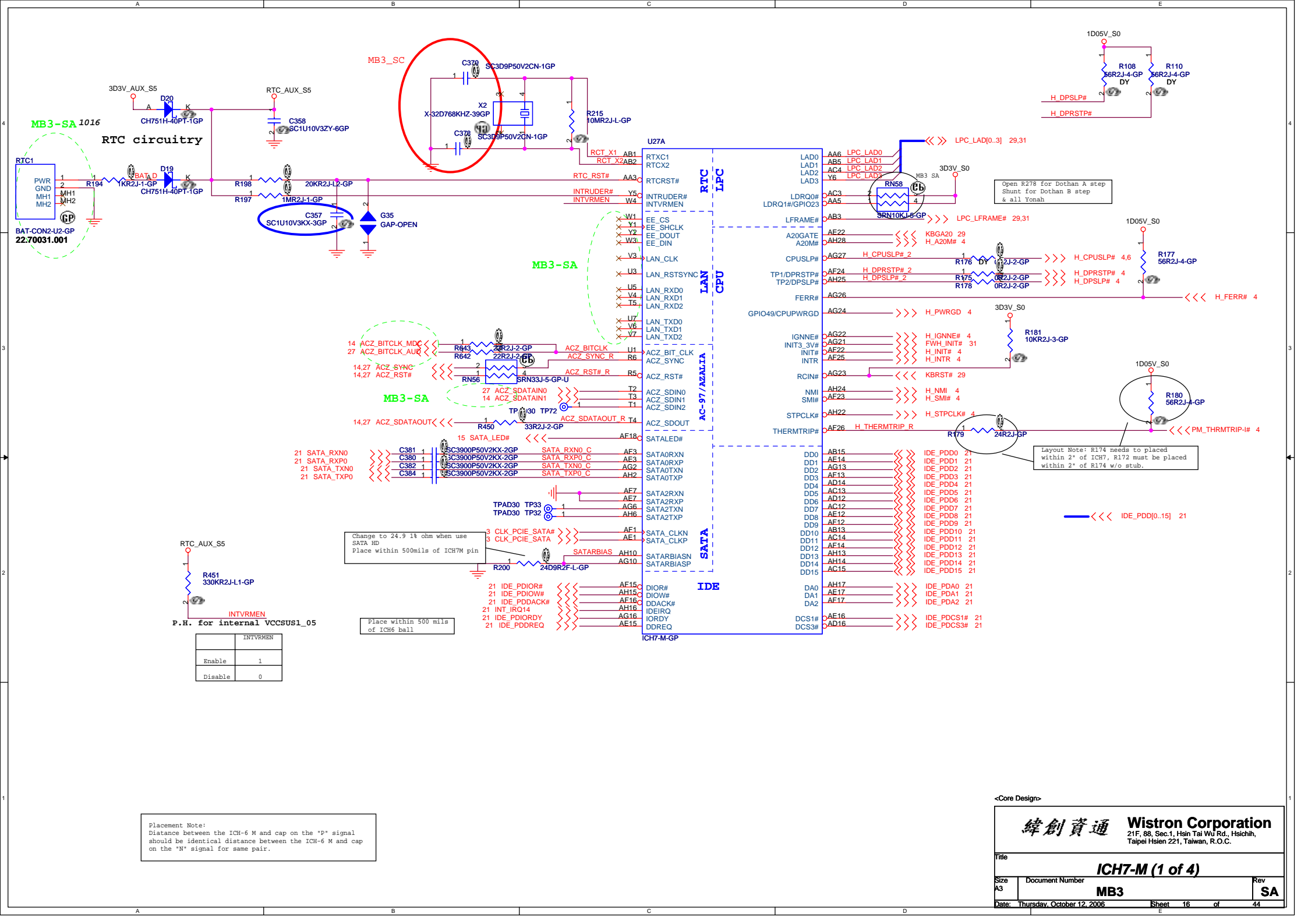
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| Size | Document Number | Rev |
| Custom | MB3 | SA |
| Date: Wednesday, October 18, 2006 | Sheet 14 of 44 | |

all page is for MB3-SA



Launch Board CNN



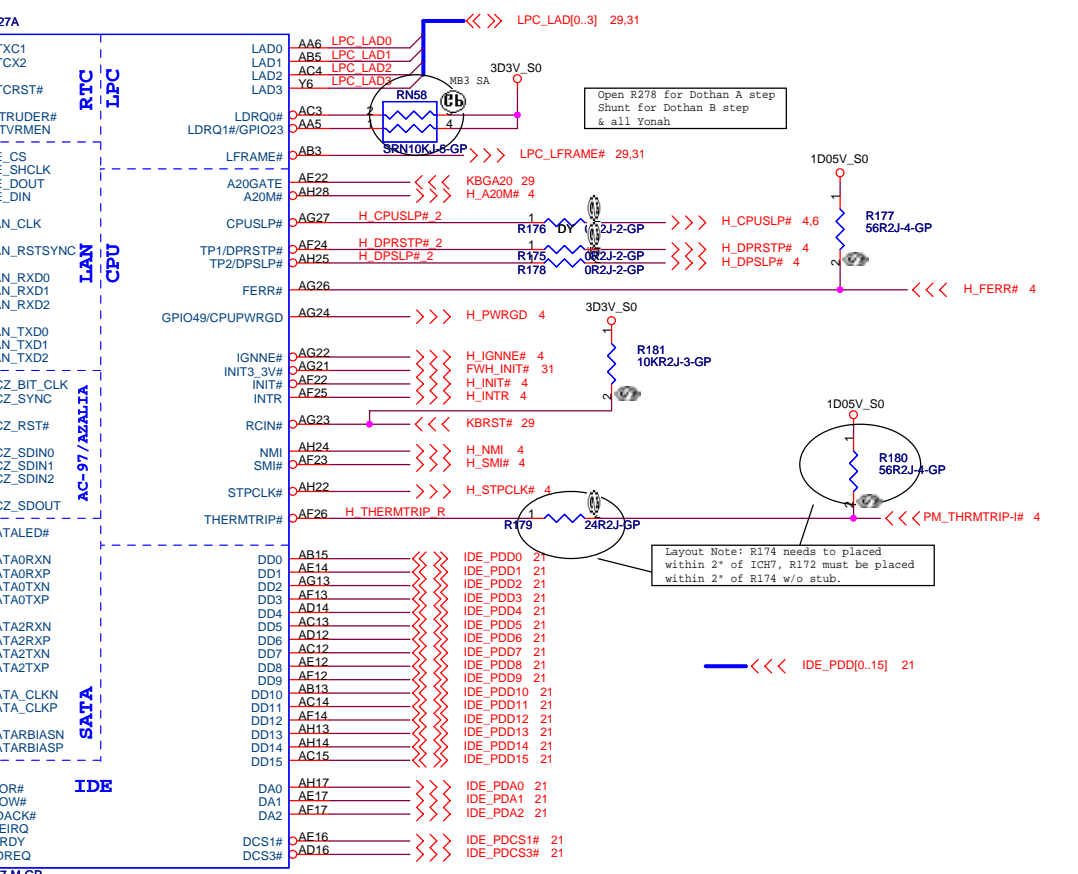


Change to 24.9 1% ohm when use SATA HD
Place within 500mils of ICH7M pin



| | INTVRMEN |
|---------|----------|
| Enable | 1 |
| Disable | 0 |

Placement Note:
Distance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



<Core Design>

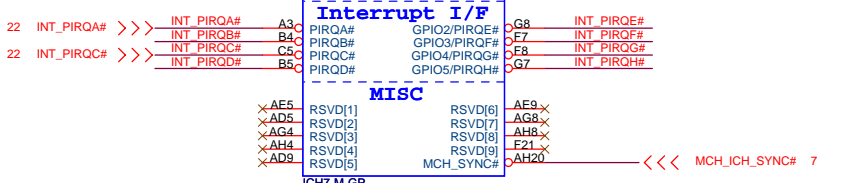
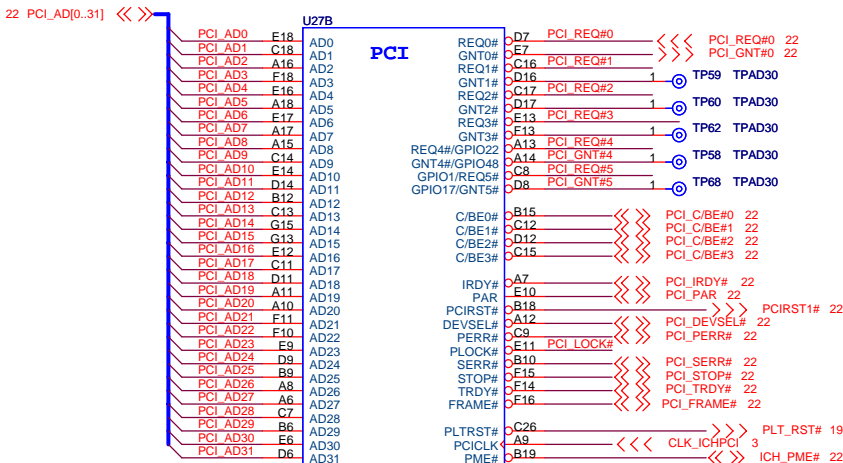
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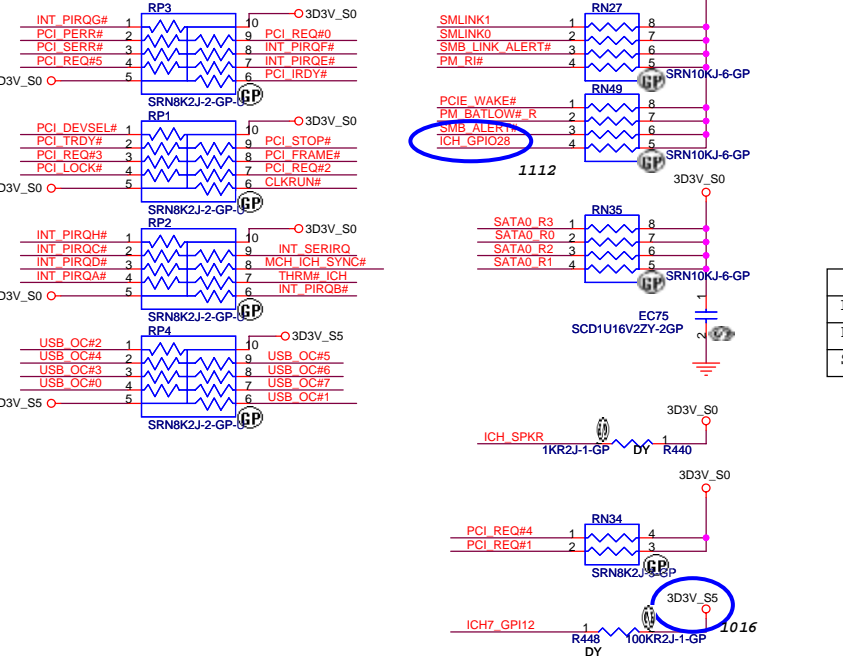
Title: **ICH7-M (1 of 4)**

Size A3 Document Number **MB3** Rev **SA**

Date: Thursday, October 12, 2006 Sheet 16 of 44

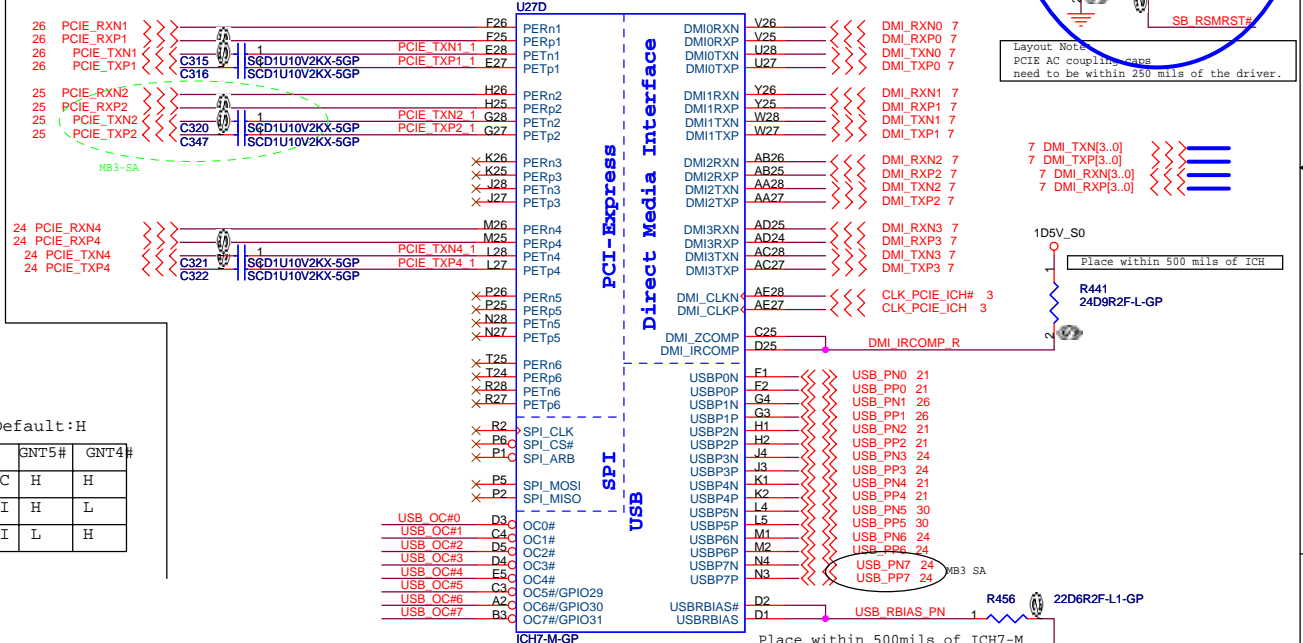
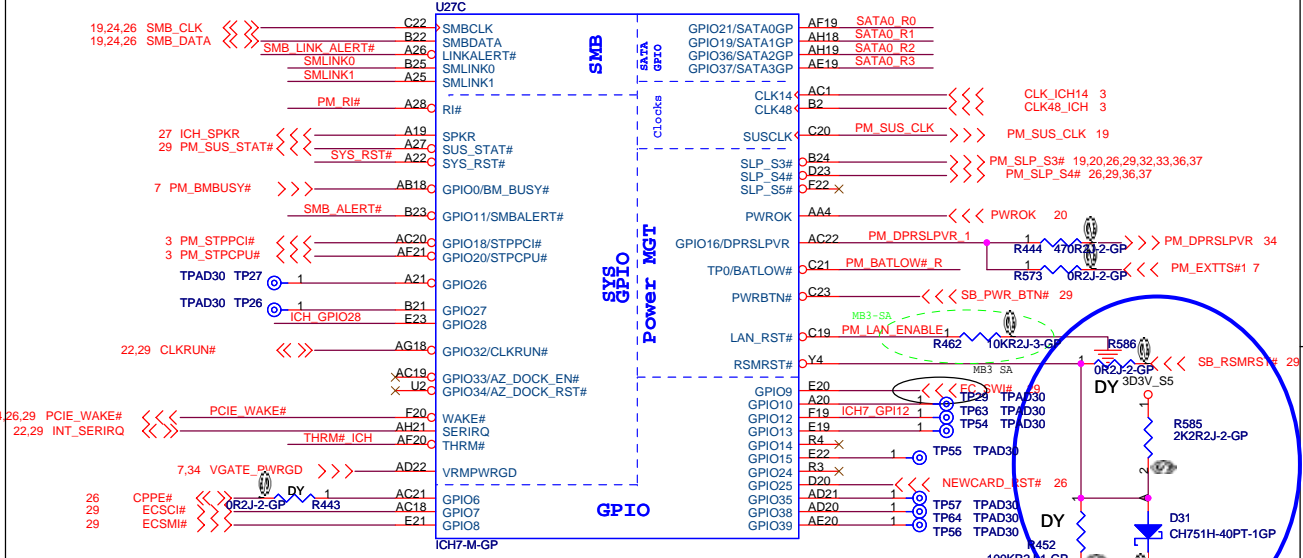


ICH7 Pullups



Default: H

| | | |
|-----|---|---|
| LPC | H | H |
| PCI | H | L |
| SPI | L | H |



Layout Note: PCB AC coupling capacitors need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500mils of ICH7-M

USB0---->JUSB2 USB1-->NEW CARD
 USB2/3---->JUSB1 USB4-->RF
 USB5-->blue tooth USB6-->finger print
 USB7-->Mini card

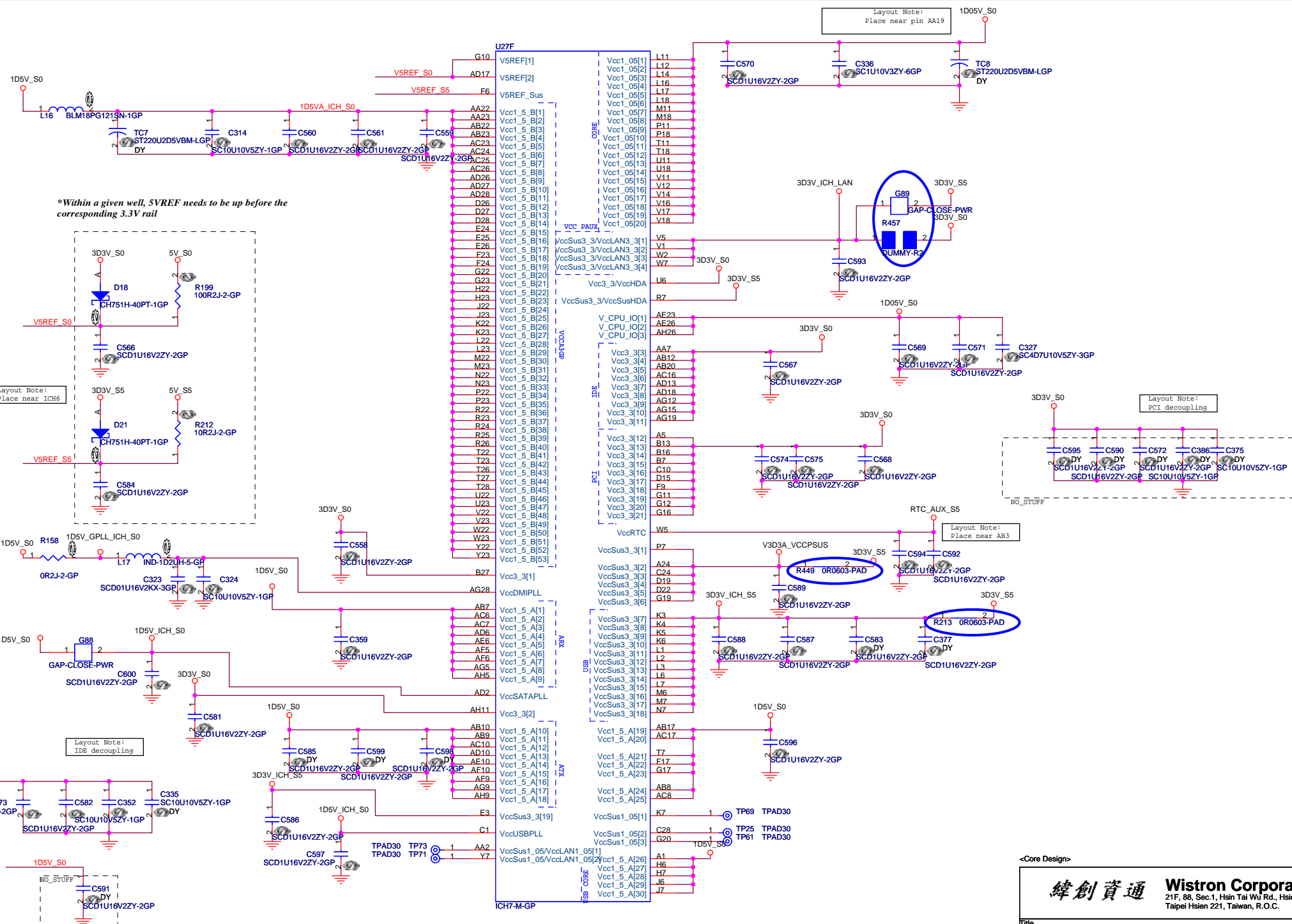
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Title: **ICH7-M (2 of 4)**

Size: A3 Document Number: MB3 Rev: SA

Date: Wednesday, August 30, 2006 Sheet: 17 of 44



*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note:
Place near ICH6

Layout Note:
PCI decoupling

Layout Note:
Place near AB3

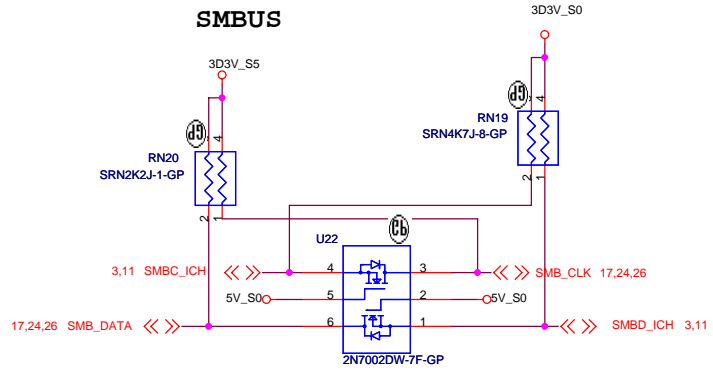
Layout Note:
IDS decoupling

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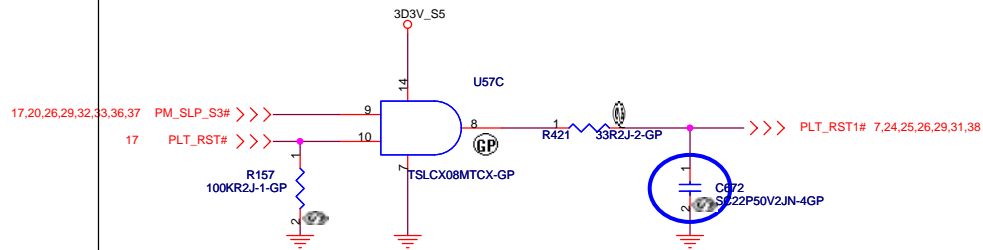
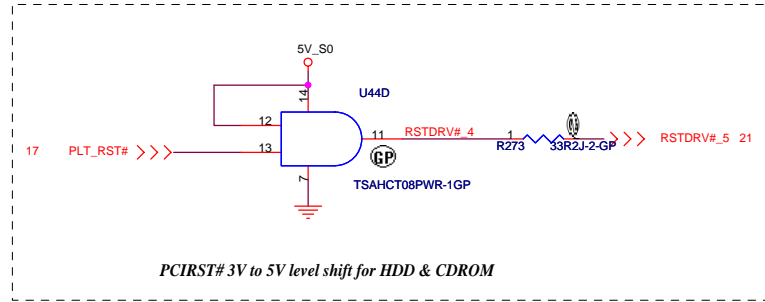
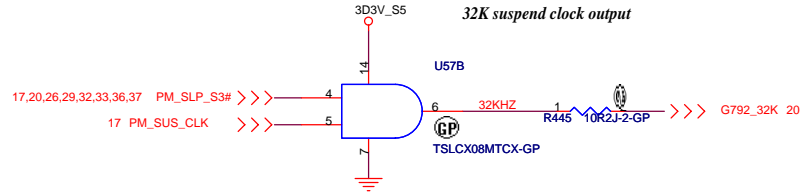
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (3 of 4)**

| | | |
|----------------------------------|-----------------|-----------|
| Size A3 | Document Number | Rev |
| | MB3 | SA |
| Date: Thursday, October 26, 2006 | Sheet 18 of 44 | |



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance



| | | | |
|-----|---------|----------|------|
| A4 | VSS1[1] | VSS[98] | P28 |
| A23 | VSS[2] | VSS[99] | R1 |
| B1 | VSS[3] | VSS[100] | R11 |
| B8 | VSS[4] | VSS[101] | R12 |
| B11 | VSS[5] | VSS[102] | R13 |
| B14 | VSS[6] | VSS[103] | R14 |
| B17 | VSS[7] | VSS[104] | R15 |
| B20 | VSS[8] | VSS[105] | R16 |
| B28 | VSS[9] | VSS[106] | R17 |
| B28 | VSS[10] | VSS[107] | R18 |
| C2 | VSS[11] | VSS[108] | T6 |
| C6 | VSS[12] | VSS[109] | T12 |
| C27 | VSS[13] | VSS[110] | T13 |
| D10 | VSS[14] | VSS[111] | T14 |
| D13 | VSS[15] | VSS[112] | T15 |
| D18 | VSS[16] | VSS[113] | T16 |
| D21 | VSS[17] | VSS[114] | T17 |
| D24 | VSS[18] | VSS[115] | U4 |
| E1 | VSS[19] | VSS[116] | U12 |
| E2 | VSS[20] | VSS[117] | U13 |
| E4 | VSS[21] | VSS[118] | U14 |
| E8 | VSS[22] | VSS[119] | U15 |
| E15 | VSS[23] | VSS[120] | U16 |
| F3 | VSS[24] | VSS[121] | U17 |
| F4 | VSS[25] | VSS[122] | U24 |
| F5 | VSS[26] | VSS[123] | U25 |
| F12 | VSS[27] | VSS[124] | U26 |
| F27 | VSS[28] | VSS[125] | V2 |
| F28 | VSS[29] | VSS[126] | V13 |
| G1 | VSS[30] | VSS[127] | V15 |
| G2 | VSS[31] | VSS[128] | V24 |
| G5 | VSS[32] | VSS[129] | V27 |
| G6 | VSS[33] | VSS[130] | V28 |
| G9 | VSS[34] | VSS[131] | W6 |
| G14 | VSS[35] | VSS[132] | W24 |
| G18 | VSS[36] | VSS[133] | W25 |
| G21 | VSS[37] | VSS[134] | W26 |
| G24 | VSS[38] | VSS[135] | Y3 |
| G25 | VSS[39] | VSS[136] | Y24 |
| G26 | VSS[40] | VSS[137] | Y28 |
| H3 | VSS[41] | VSS[138] | AA1 |
| H4 | VSS[42] | VSS[139] | AA24 |
| H5 | VSS[43] | VSS[140] | AA25 |
| H24 | VSS[44] | VSS[141] | AA26 |
| H27 | VSS[45] | VSS[142] | AB4 |
| H28 | VSS[46] | VSS[143] | AB6 |
| J1 | VSS[47] | VSS[144] | AB11 |
| J2 | VSS[48] | VSS[145] | AB14 |
| J5 | VSS[49] | VSS[146] | AB16 |
| J24 | VSS[50] | VSS[147] | AB19 |
| J25 | VSS[51] | VSS[148] | AB21 |
| J26 | VSS[52] | VSS[149] | AB24 |
| K24 | VSS[53] | VSS[150] | AB27 |
| K27 | VSS[54] | VSS[151] | AB28 |
| K28 | VSS[55] | VSS[152] | AC2 |
| L13 | VSS[56] | VSS[153] | AC5 |
| L15 | VSS[57] | VSS[154] | AC9 |
| L24 | VSS[58] | VSS[155] | AC11 |
| L25 | VSS[59] | VSS[156] | AD1 |
| L26 | VSS[60] | VSS[157] | AD3 |
| M3 | VSS[61] | VSS[158] | AD4 |
| M4 | VSS[62] | VSS[159] | AD7 |
| M5 | VSS[63] | VSS[160] | AD8 |
| M12 | VSS[64] | VSS[161] | AD11 |
| M13 | VSS[65] | VSS[162] | AD15 |
| M14 | VSS[66] | VSS[163] | AD19 |
| M15 | VSS[67] | VSS[164] | AD23 |
| M16 | VSS[68] | VSS[165] | AE2 |
| M17 | VSS[69] | VSS[166] | AE4 |
| M24 | VSS[70] | VSS[167] | AE8 |
| M27 | VSS[71] | VSS[168] | AE11 |
| M28 | VSS[72] | VSS[169] | AE13 |
| N1 | VSS[73] | VSS[170] | AE18 |
| N2 | VSS[74] | VSS[171] | AE21 |
| N6 | VSS[75] | VSS[172] | AE24 |
| N11 | VSS[76] | VSS[173] | AE25 |
| N12 | VSS[77] | VSS[174] | AF2 |
| N13 | VSS[78] | VSS[175] | AF4 |
| N14 | VSS[79] | VSS[176] | AF8 |
| N15 | VSS[80] | VSS[177] | AF11 |
| N16 | VSS[81] | VSS[178] | AF27 |
| N17 | VSS[82] | VSS[179] | AF28 |
| N18 | VSS[83] | VSS[180] | AG1 |
| N24 | VSS[84] | VSS[181] | AG3 |
| N25 | VSS[85] | VSS[182] | AG7 |
| N26 | VSS[86] | VSS[183] | AG11 |
| P3 | VSS[87] | VSS[184] | AG14 |
| P4 | VSS[88] | VSS[185] | AG17 |
| P12 | VSS[89] | VSS[186] | AG20 |
| P13 | VSS[90] | VSS[187] | AG25 |
| P14 | VSS[91] | VSS[188] | AH1 |
| P15 | VSS[92] | VSS[189] | AH3 |
| P16 | VSS[93] | VSS[190] | AH7 |
| P17 | VSS[94] | VSS[191] | AH12 |
| P24 | VSS[95] | VSS[192] | AH23 |
| P24 | VSS[96] | VSS[193] | AH27 |
| P27 | VSS[97] | VSS[194] | |

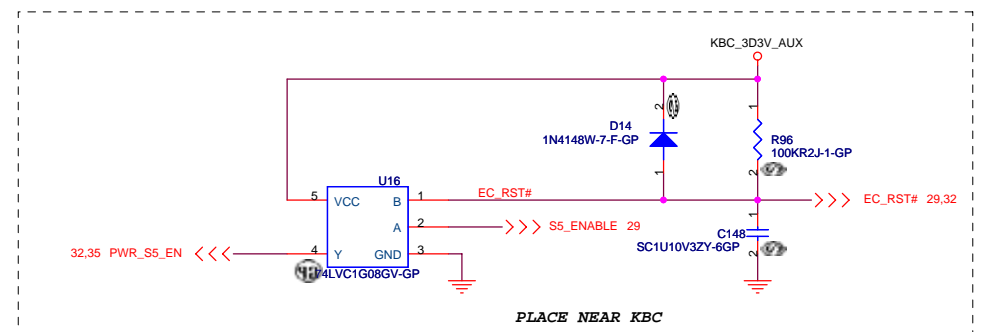
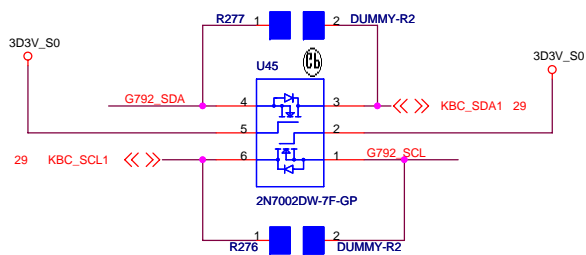
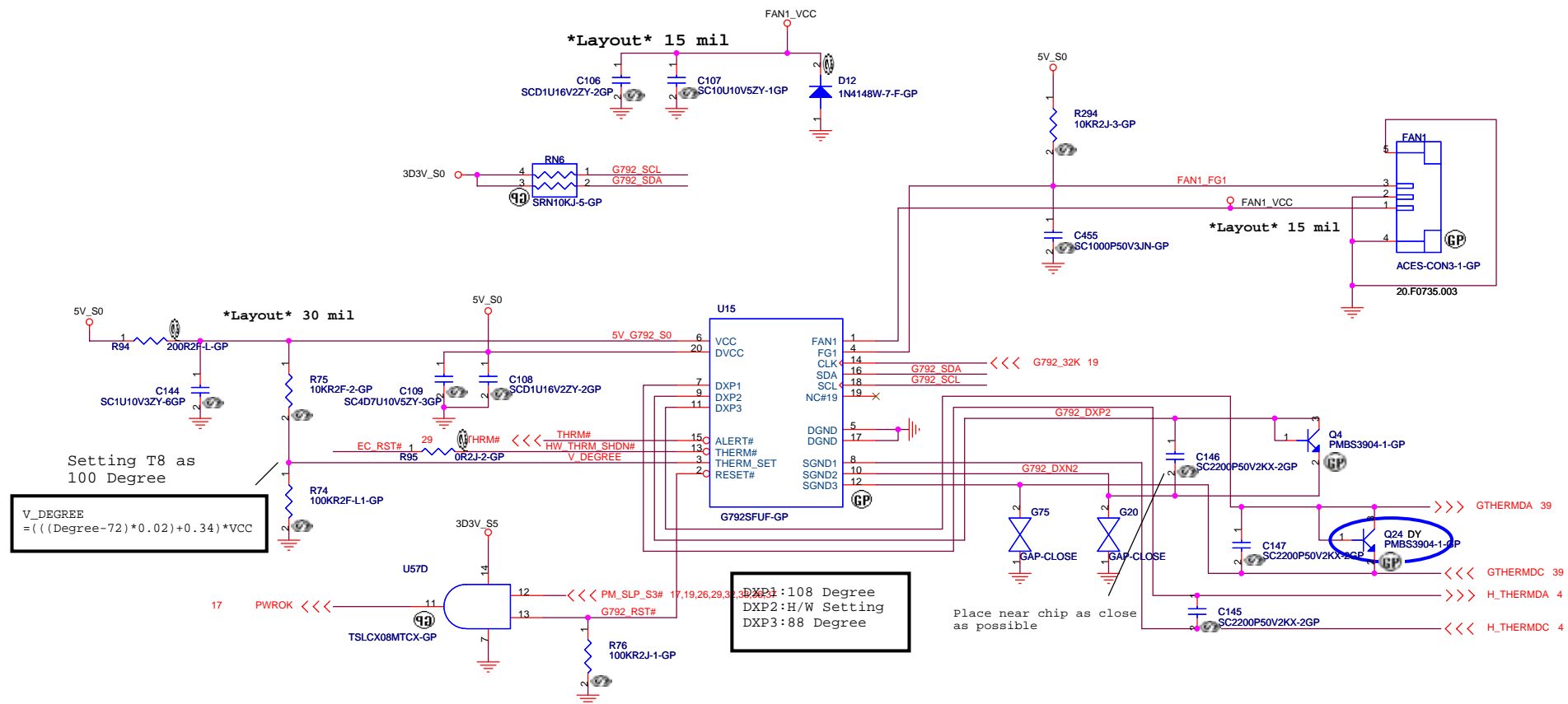
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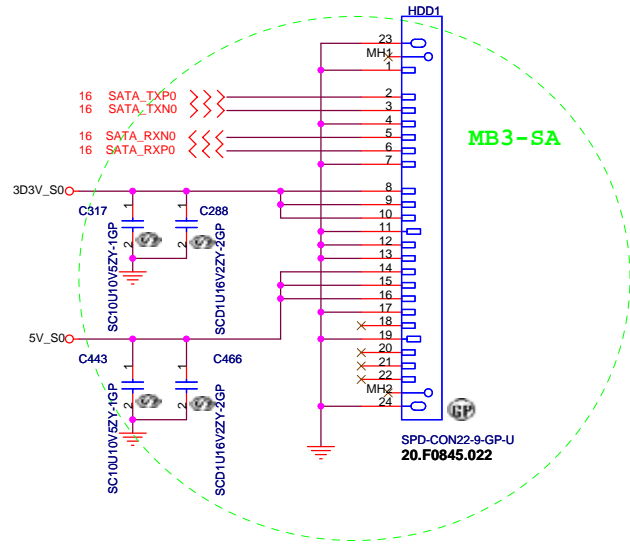
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Size A3 Document Number **MB3** Rev **SA**

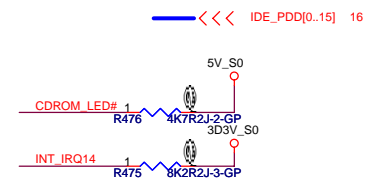
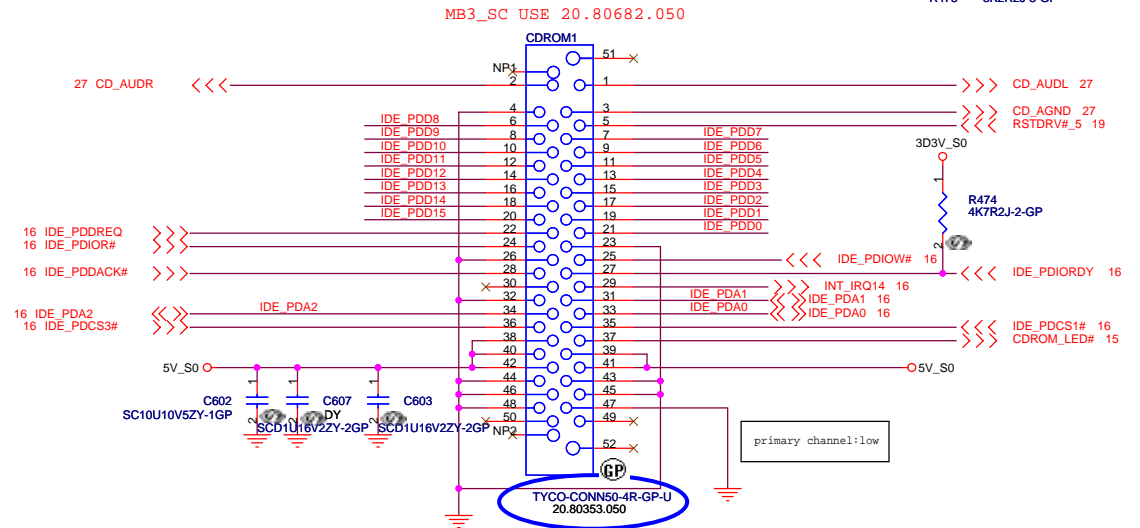
Date: Thursday, August 24, 2006 Sheet 19 of 44



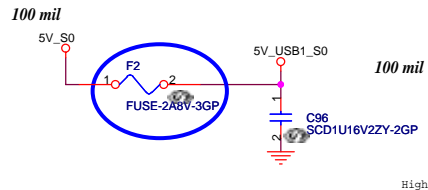
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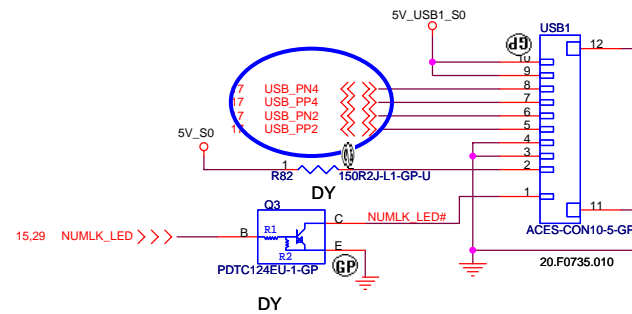
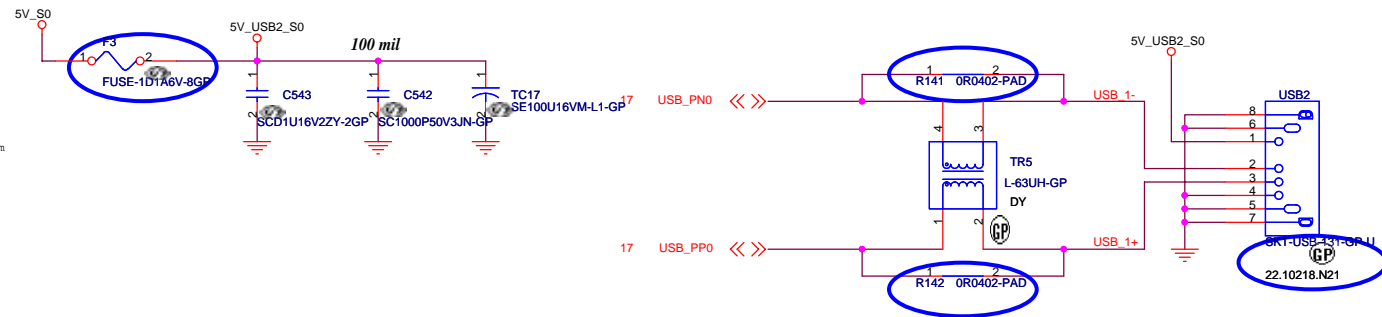
CD-ROM CONNECTOR



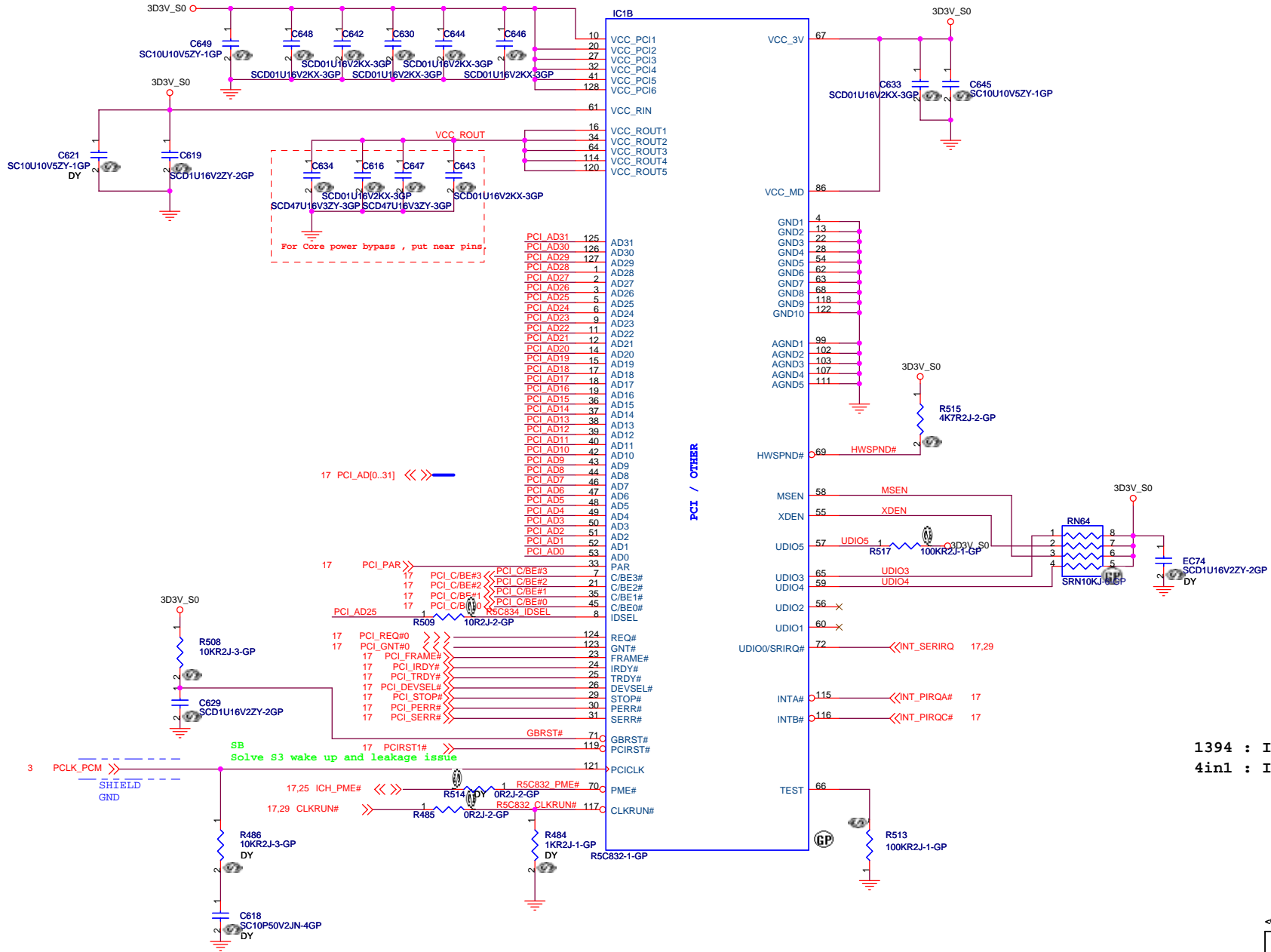
USB PORT



High limit under 2.5 mm



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17 PCI_PAR <<>

SB solve s3 wake up and leakage issue

17,25 ICH_PME# <<>

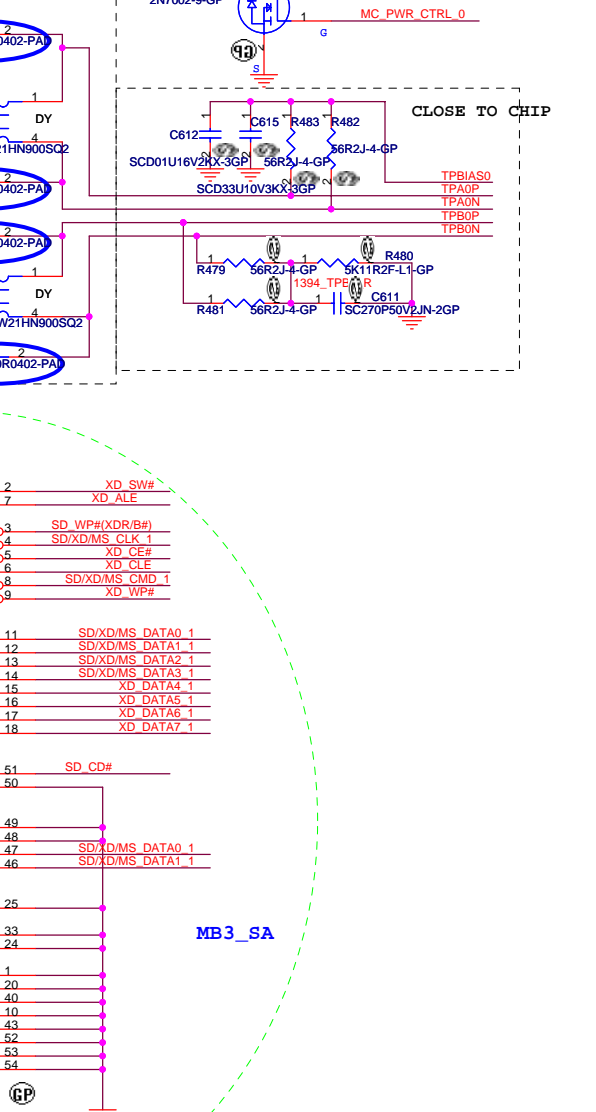
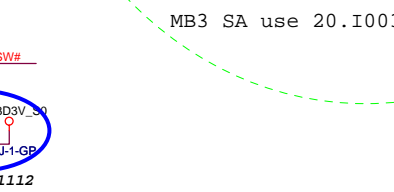
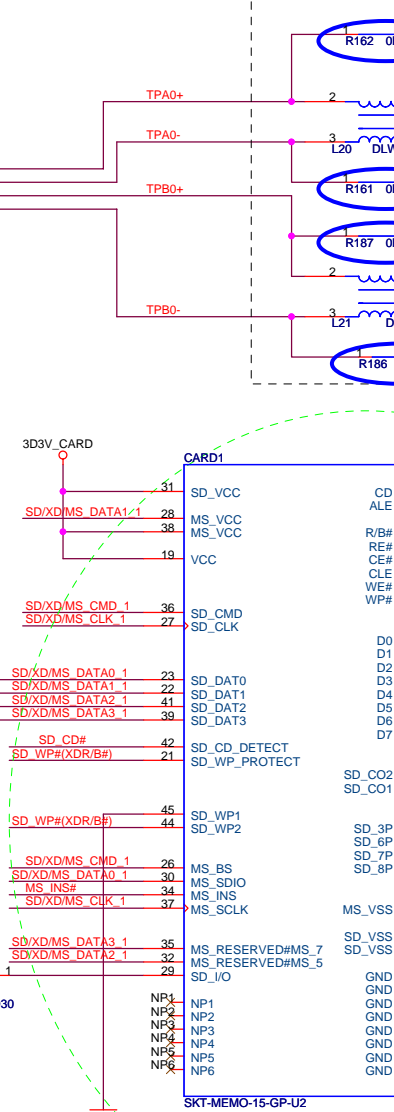
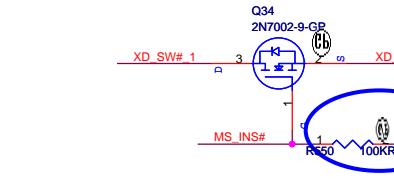
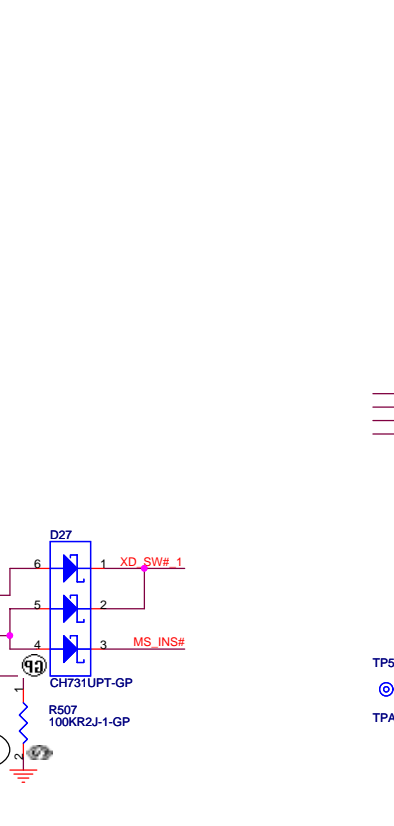
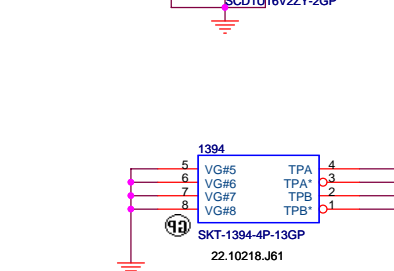
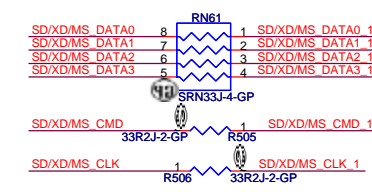
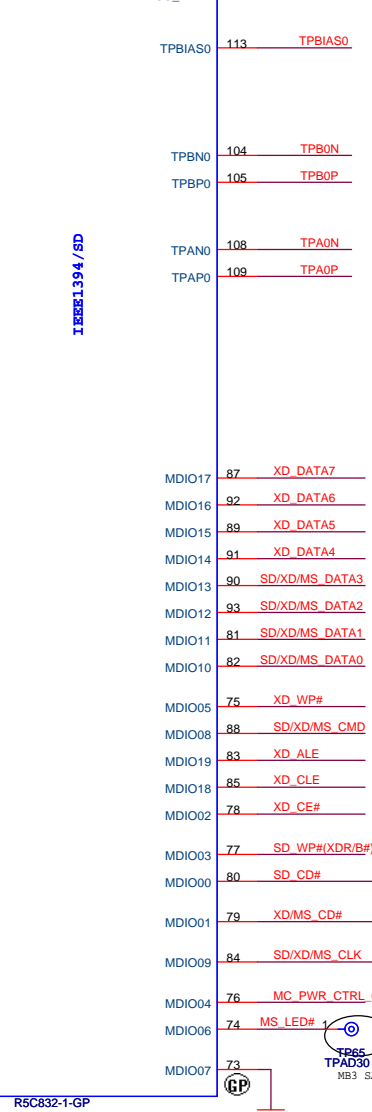
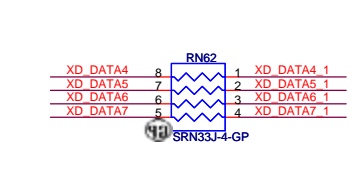
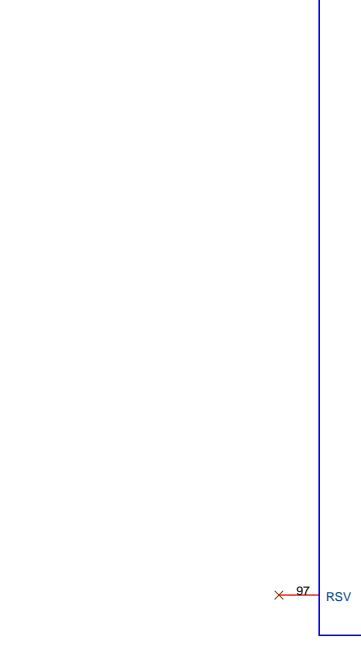
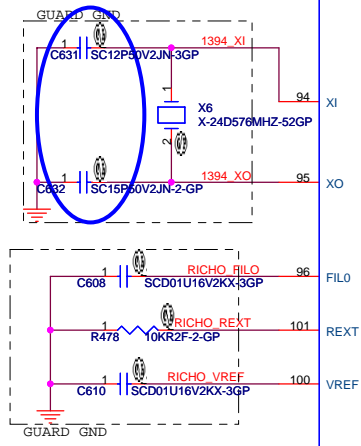
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PCI / OTHER

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4in1 : INTB#

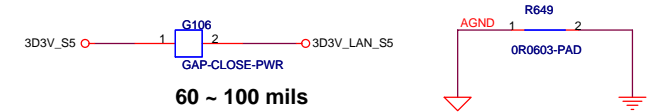
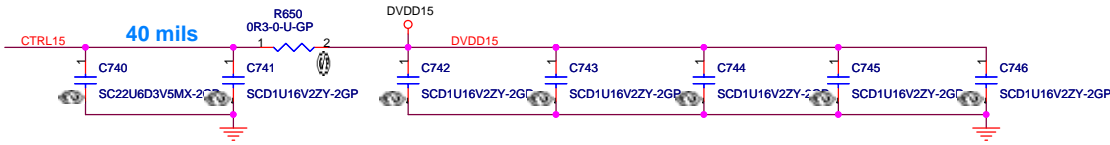
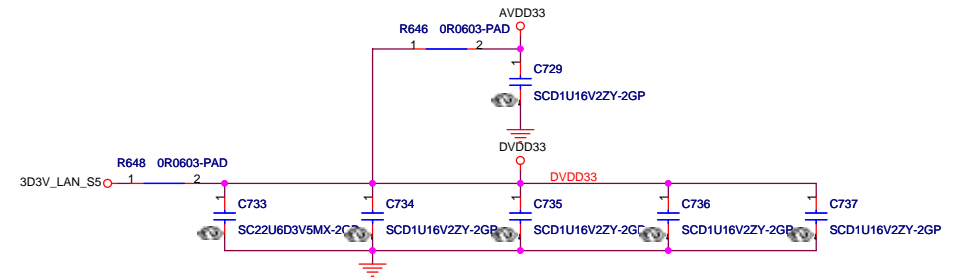
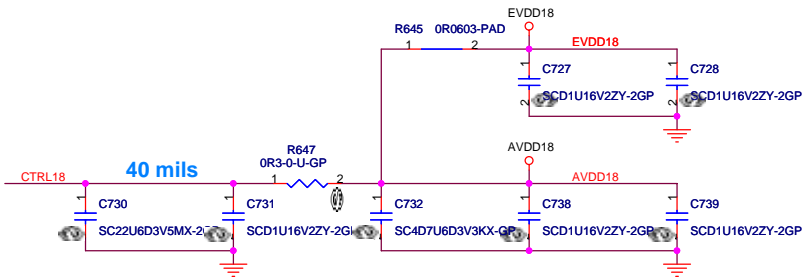
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| | |
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| R5C832/PCI | |
| Title | SA |
| Size A3 | Date: Thursday, August 24, 2006 |
| Document Number | Sheet 22 of 44 |
| MB3 | Rev |

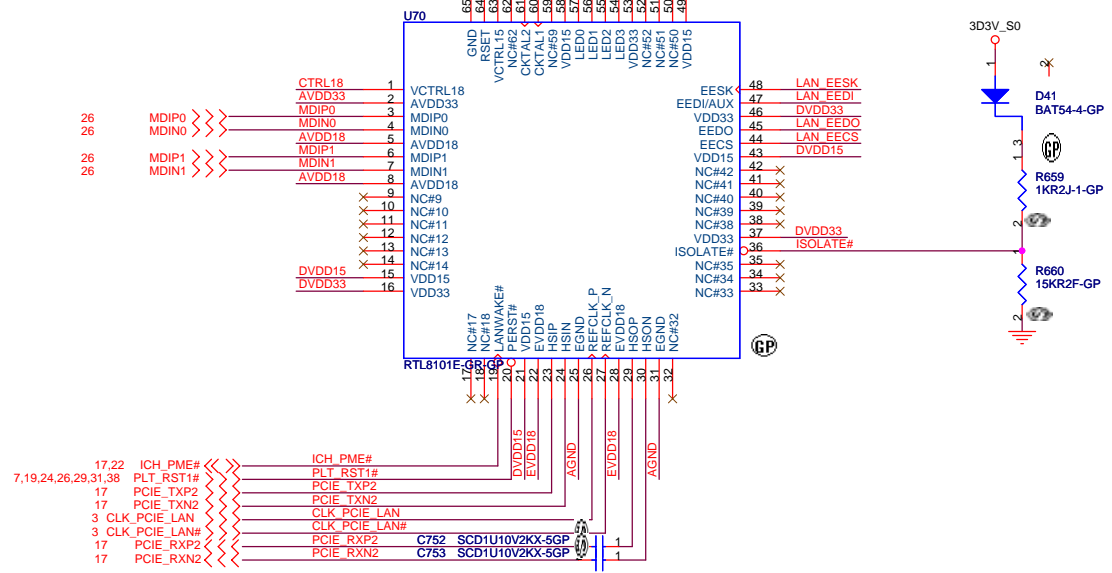
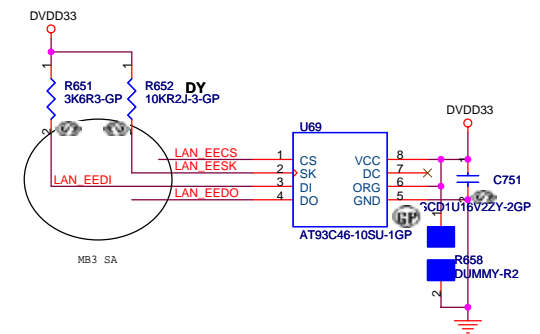
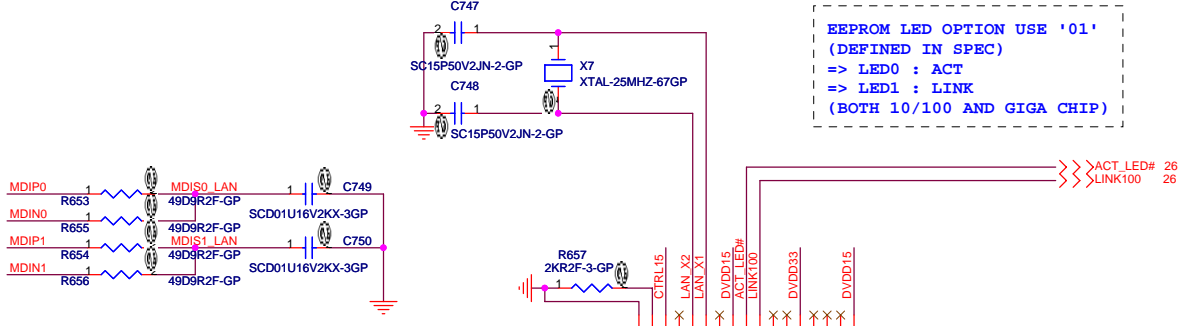


For SD Card Power

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 Title: **R5C832/IEEE1394/SD**
 Size: A3 Document Number: **MB3** Rev: **SA**
 Date: Thursday, August 17, 2006 Sheet 23 of 44



EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)



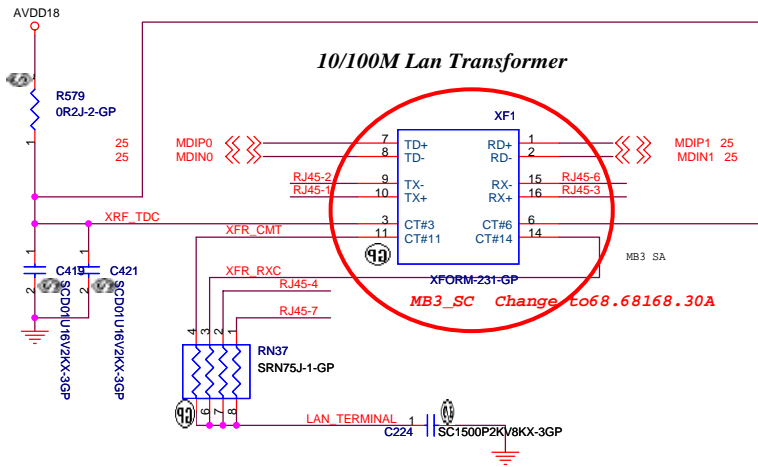
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緯創資通 Wistron Corporation
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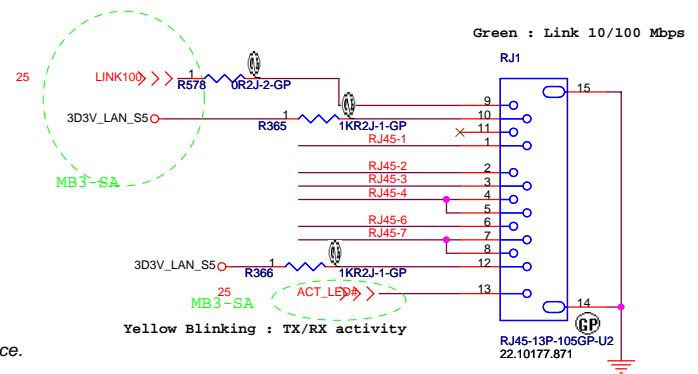
Title: **RTL8101E**

Size: Document Number: **MB3** Rev: **SA**

Date: Thursday, August 24, 2006 Sheet 25 of 44



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

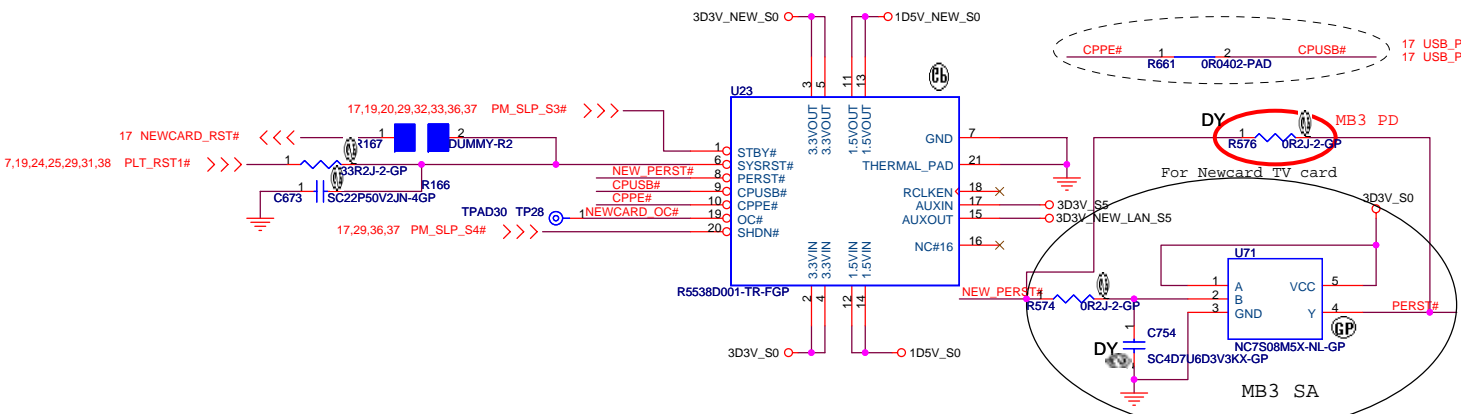
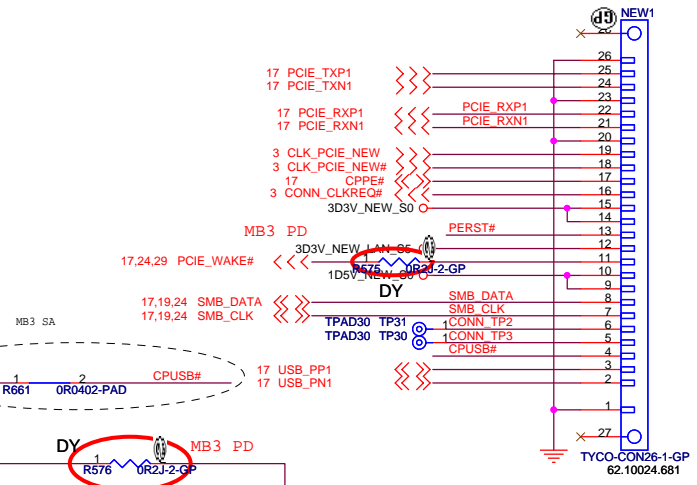
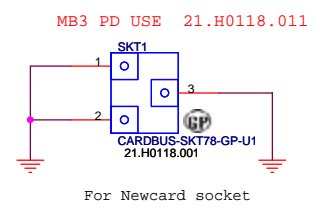
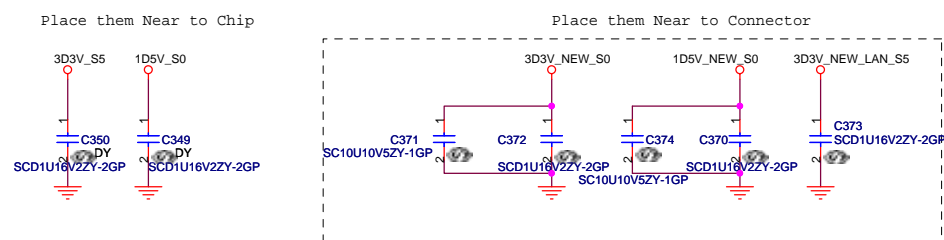


Green : Link 10/100 Mbps
 Yellow Blinking : TX/RX activity

Pin10(+)Pin9(-) Green
 Pin10(+)Pin11(-) Orange
 Pin12(+) Pin13(-) Yellow

PIN09 : GREEN
 PIN11 : ORANGE
 PIN13 : YELLOW

NEWCARD Connector



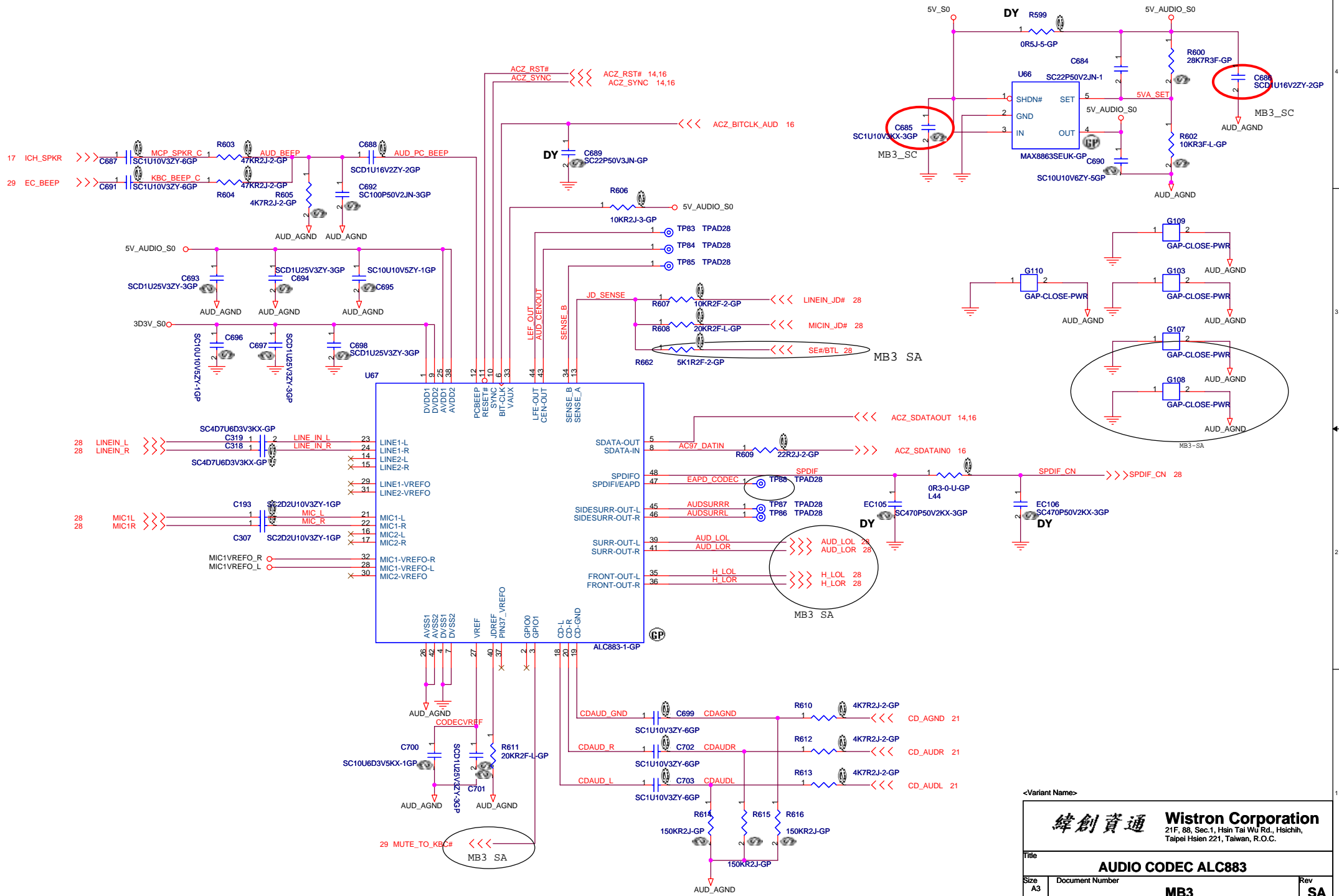
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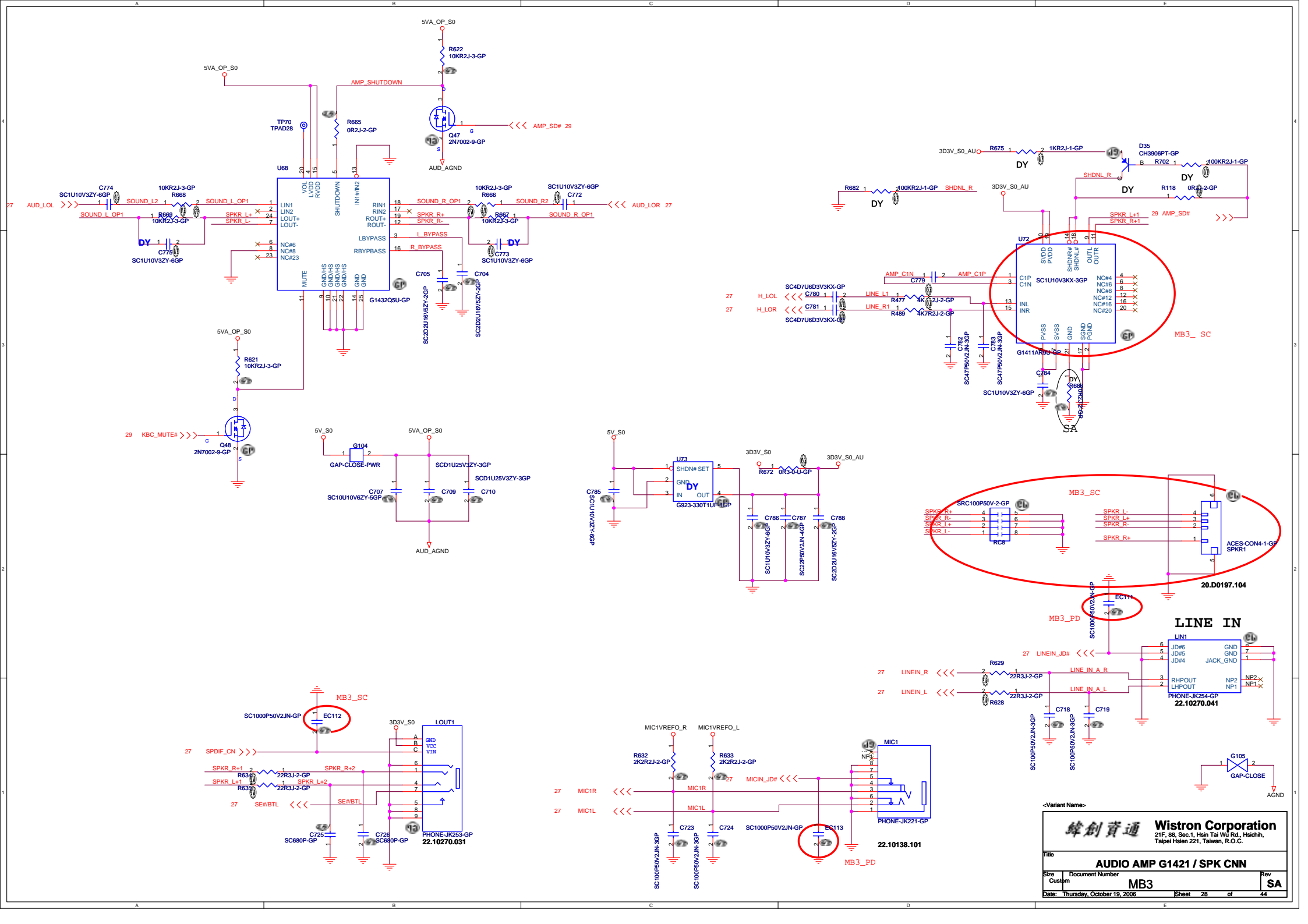
緯創資通 Wistron Corporation
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Title: **New Card**

Size: A3 Document Number: **MB3** Rev: **SA**

Date: Wednesday, October 18, 2006 Sheet: 26 of 44

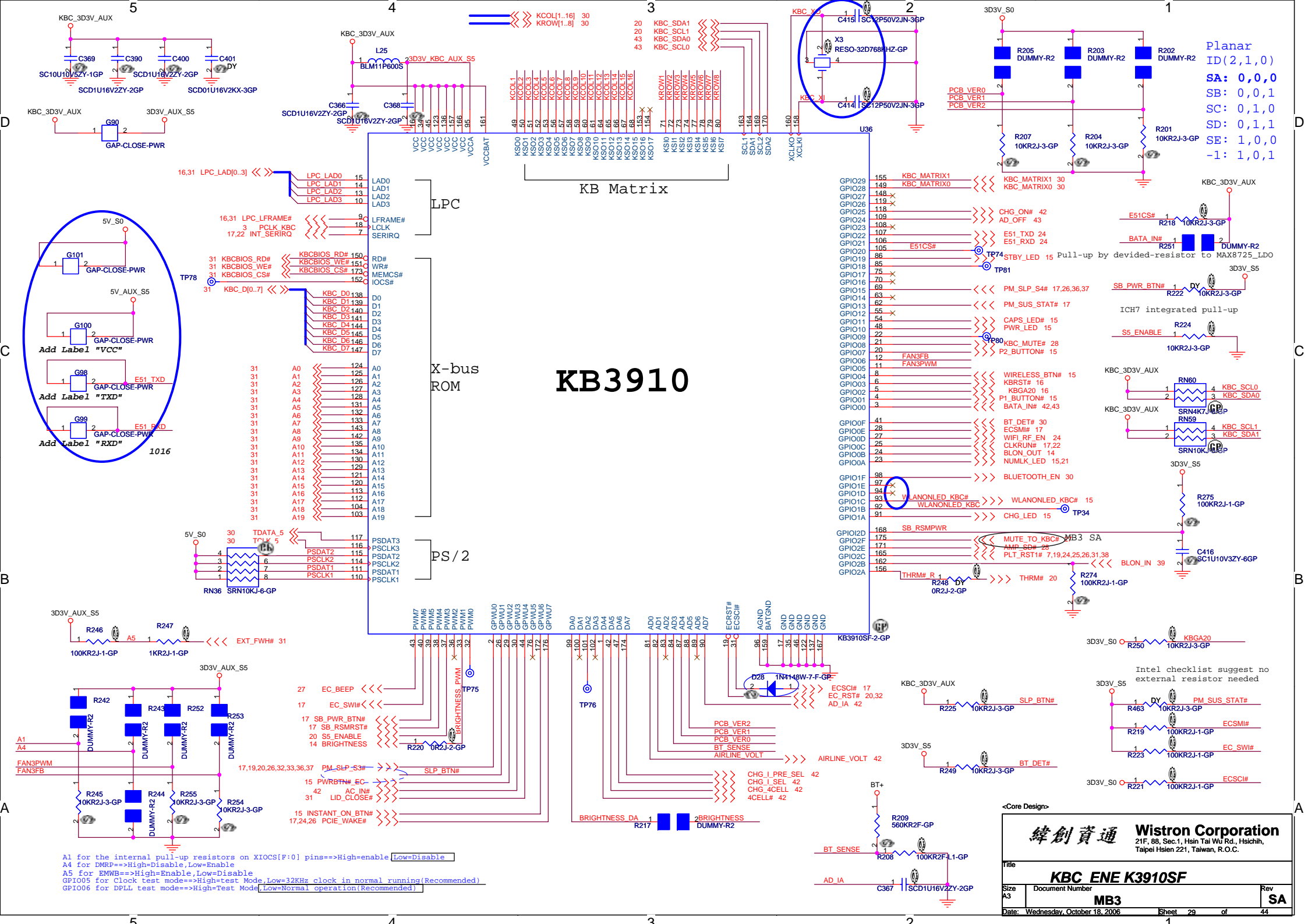




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 Taipei Hsien 221, Taiwan, R.O.C.

AUDIO AMP G1421 / SPK CNN

| | | | |
|-------|----------------------------|----------------|-----|
| Title | CUSTOMER NAME | | Rev |
| Size | Document Number | MB3 | SA |
| Date: | Thursday, October 19, 2006 | Sheet 28 of 44 | |



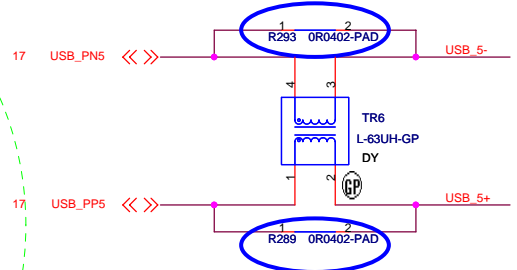
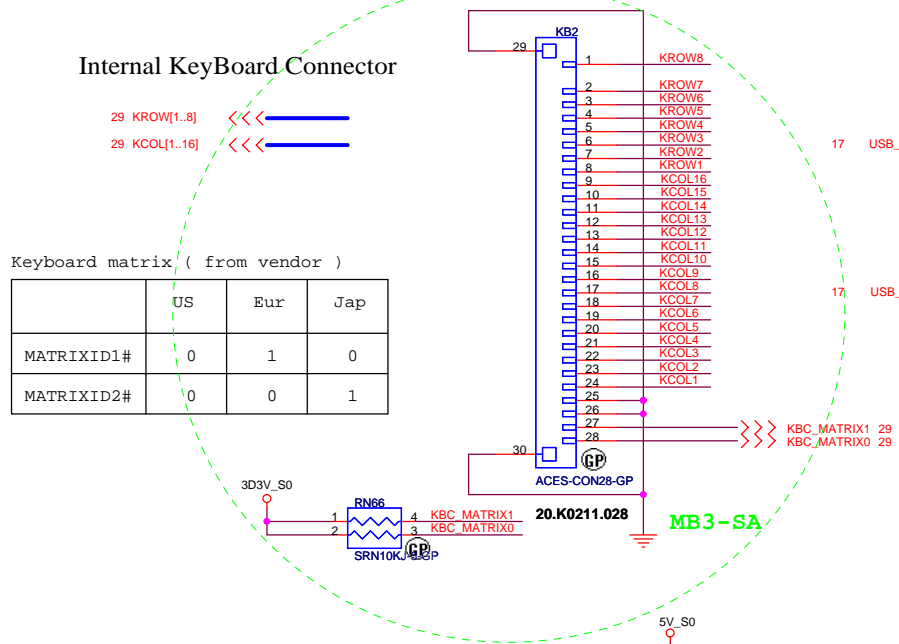
Internal Keyboard Connector

Internal Keyboard Connector

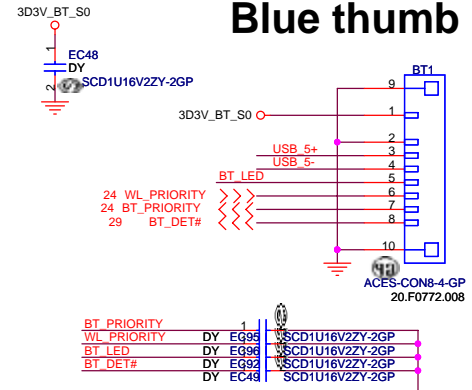
29 KROW[1..8] <<<<
29 KCOL[1..16] <<<<

Keyboard matrix (from vendor)

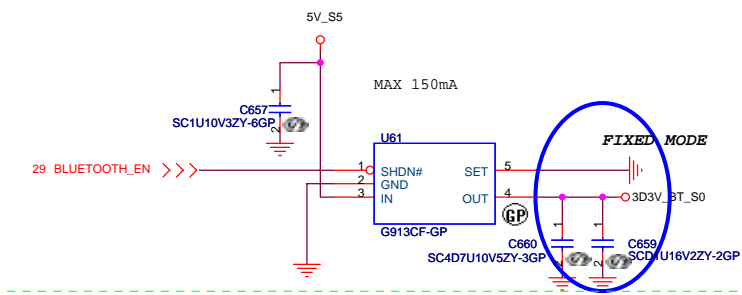
| | US | Eur | Jap |
|------------|----|-----|-----|
| MATRIXID1# | 0 | 1 | 0 |
| MATRIXID2# | 0 | 0 | 1 |



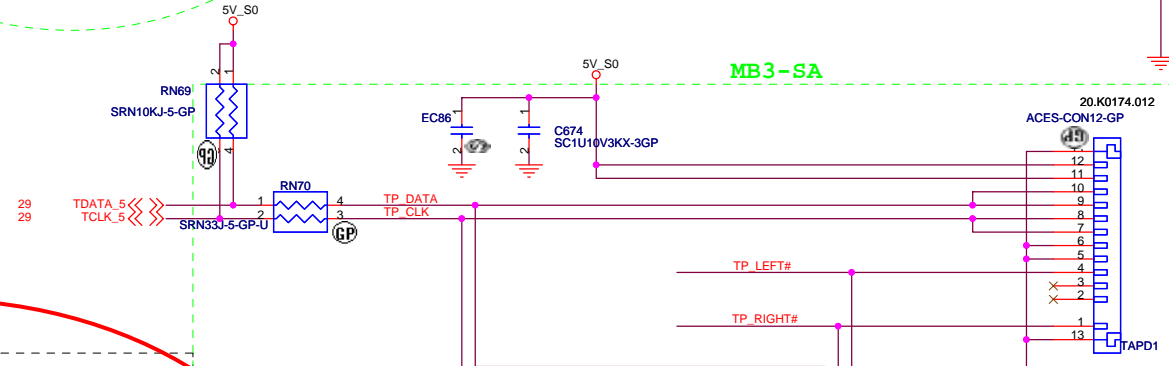
Blue thumb



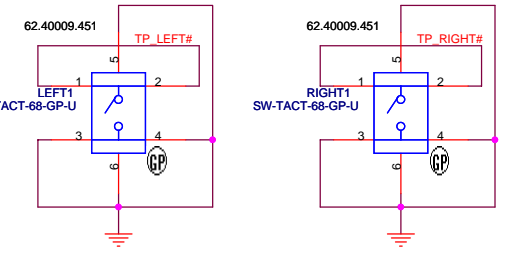
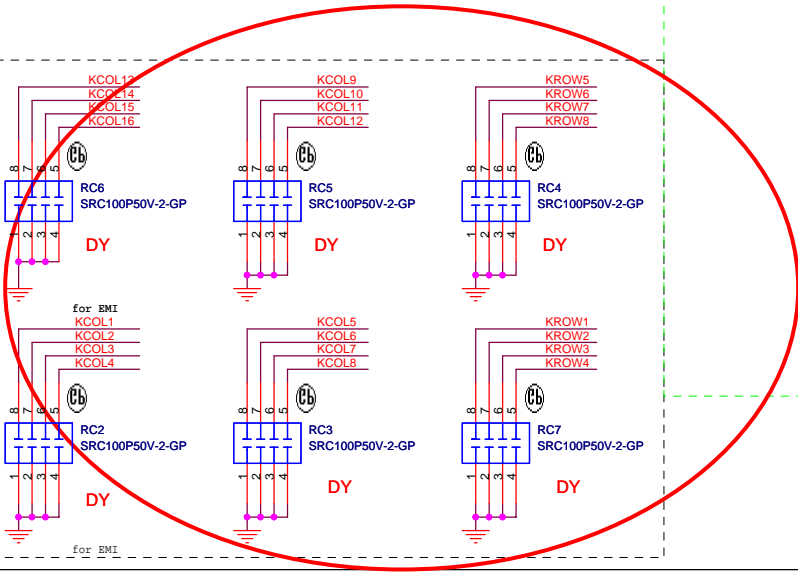
Close to BT1



MB3-SA



TOUCH PAD



<Core Design>

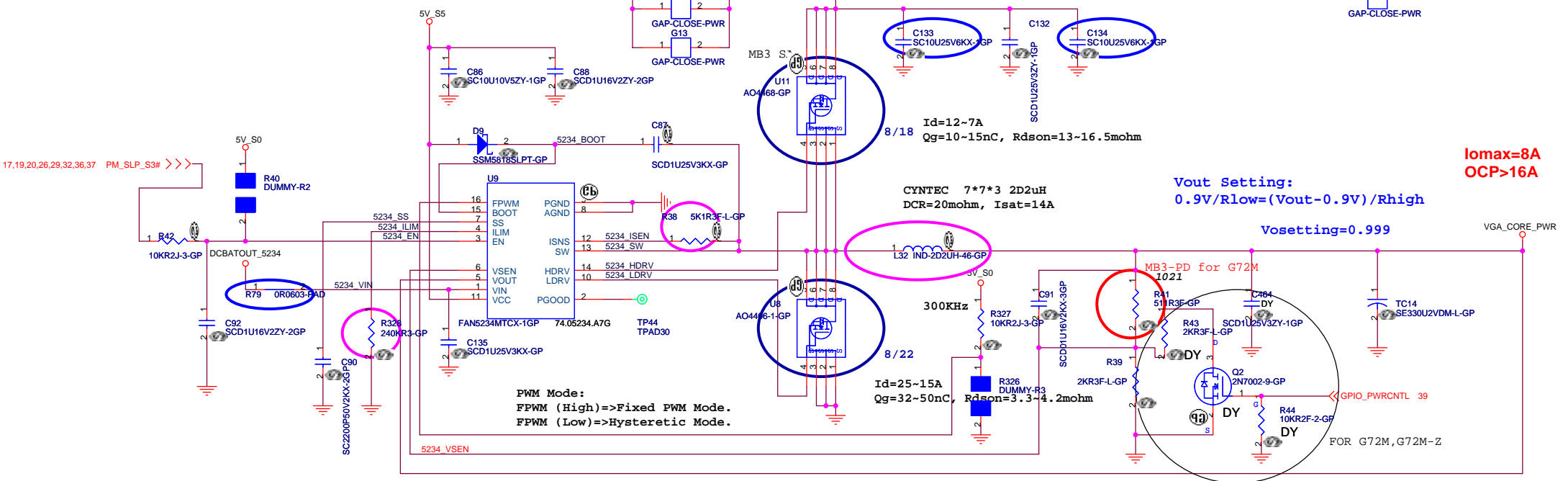
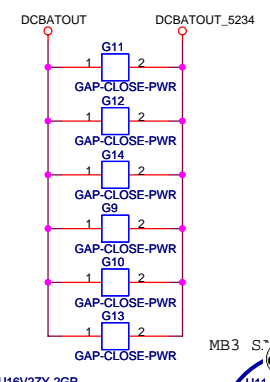
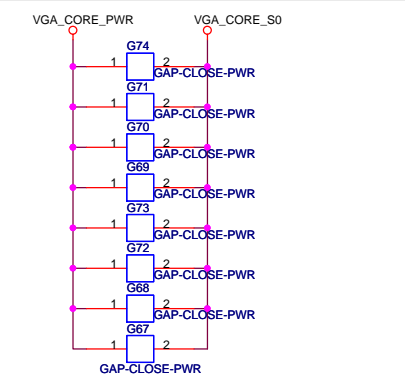
緯創資通 Wistron Corporation
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Title: **KeyBoard-CONN**

Size A3 | Document Number: **MB3** | Rev: **SA**

Date: Friday, October 20, 2006 | Sheet 30 of 44

FAN5234 FOR VGA_Core



Iomax=8A
OCP>16A

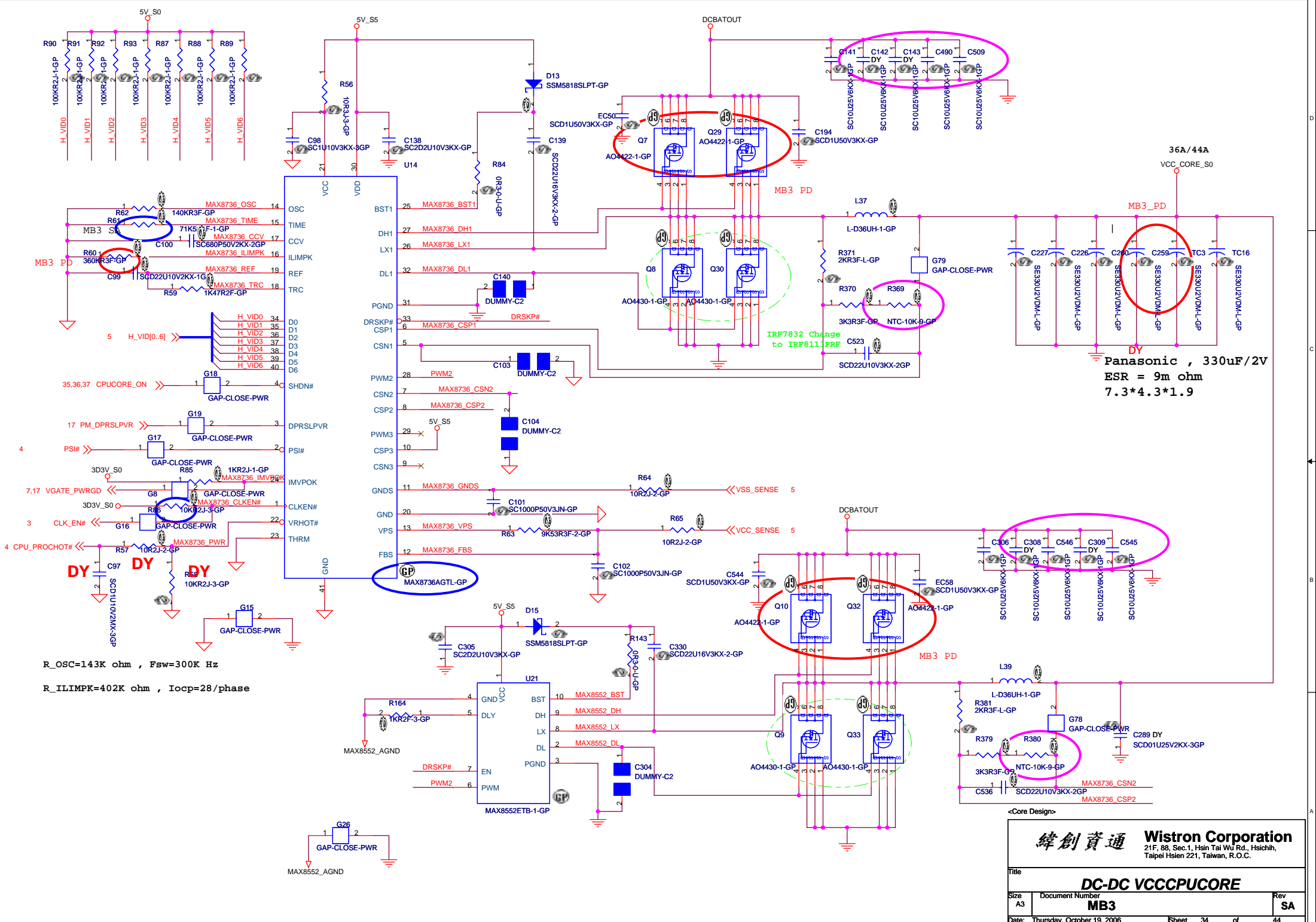
Vout Setting:
 $0.9V/R_{low} = (V_{out} - 0.9V) / R_{high}$

Vosetting=0.999

PWM Mode:
FPWM (High) => Fixed PWM Mode.
FPWM (Low) => Hysteretic Mode.

$$R_{ilim} = (11.2 / I_{ilim}) * ((100 + R_{sense}) / R_{dson})$$

Low (0V) => Vo=1.01V
High (3.3V) => Vo=1.11V



Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9

R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase

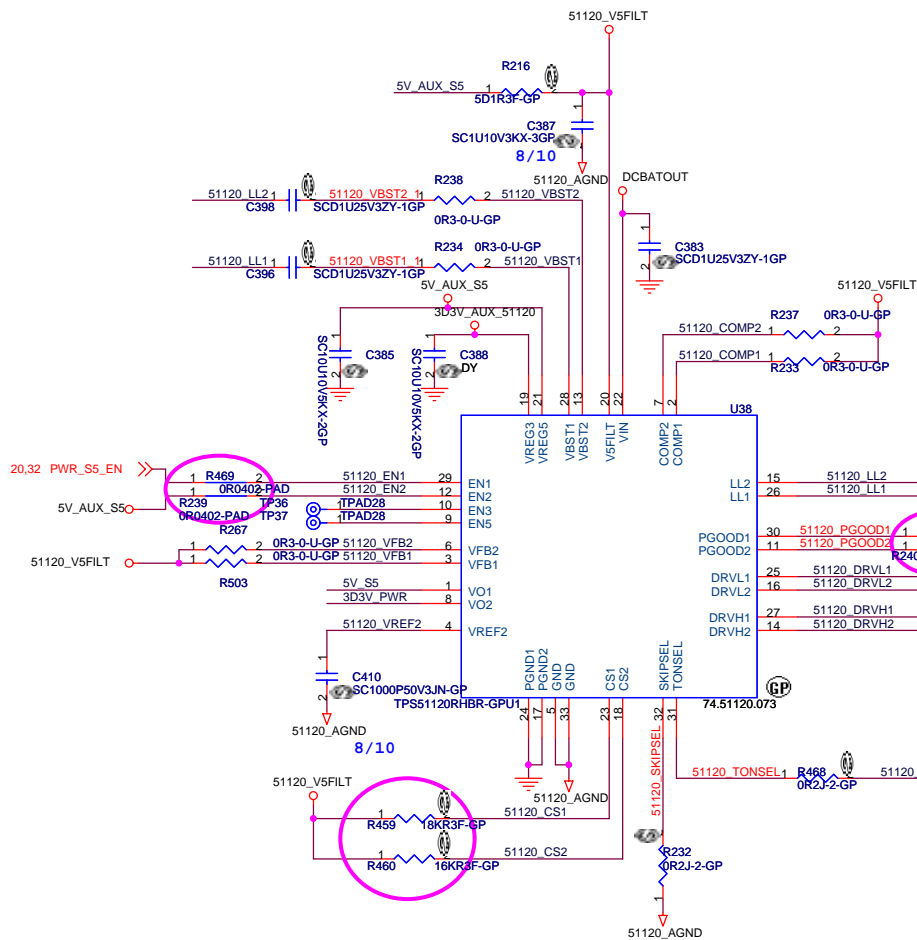
<Core Design>

緯創資通 Wistron Corporation
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Title: **DC-DC VCCPUCORE**

Size: A3 Document Number: **MB3** Rev: **SA**

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I_{omax}=11A
Q_g=9.8nC,
R_{dson}=20~25mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=20~25mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

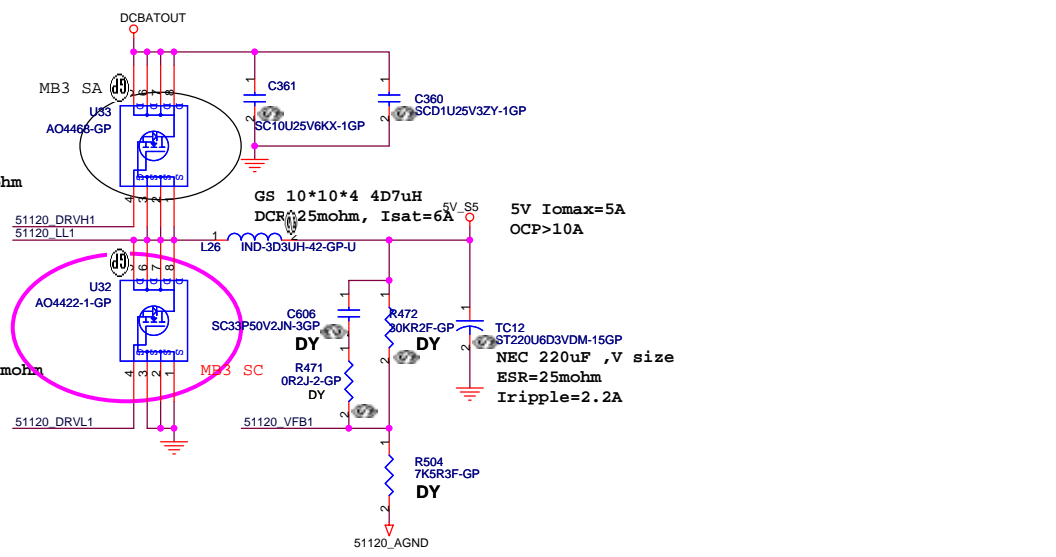
$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
V_{out}=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

V_{out}=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.



I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=20~25mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=20~25mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

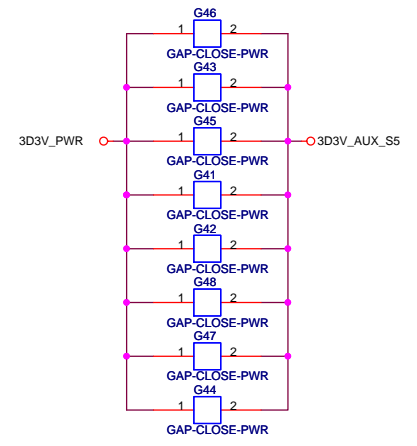
I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

I_{omax}=11A
Q_g=9.8nC,
R_{dson}=19.6~24mohm

| | GND | VREF2 | FLOAT | V5FILT |
|----------|----------------------|-----------------------|----------------------|----------------------|
| SKIPSEL | AUTOSKIP | AUTOSKIP / FAULTS OFF | PWM | PWM |
| COMP | N/A | N/A | CURRENT MODE | D-Cap MODE |
| TONSEL | 380k/CH1 590k/CH2 | 290k/CH1 440k/CH2 | 220k/CH1 330k/CH2 | 180k/CH1 280k/CH2 |
| VFB1 | N/A | not use | ADJ. | 5V Fixed Output |
| VFB2 | N/A | not use | ADJ. | 3.3V Fixed Output |
| EN1, EN2 | switcher OFF | not use | Switchchr ON | switcher ON |
| EN3, EN5 | LDO OFF | not use | LDO ON | VREG3 on |



<Core Design>

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Title: **5V_S5/3D3V_S5**

Size A3 Document Number **MB3** Rev SA

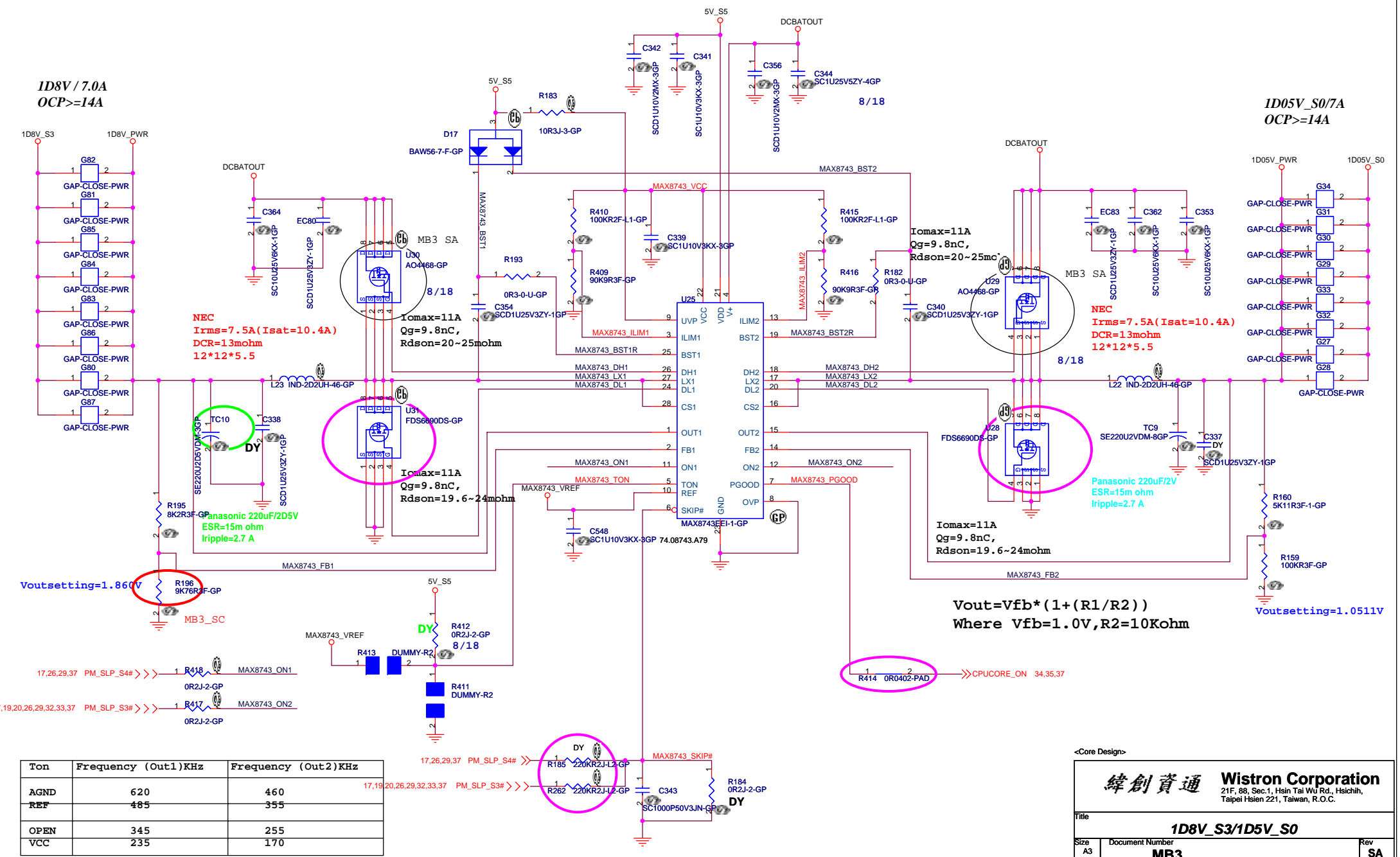
Date: Wednesday, October 18, 2006 Sheet 35 of 44

$I_{ocp}=7.0*2=14A$
 $R_{ds,on}=17m\ \Omega$
 $V_{cs1}=I_{ocp}*R_{ds,on}=238mV$
 $V_{ILIM}=V_{cs1}/0.1=2.38V$

$I_{ocp}=7.0*2=14A$
 $R_{ds,on}=17m\ \Omega$
 $V_{cs2}=I_{ocp}*R_{ds,on}=28mV$
 $V_{ILIM2}=V_{cs2}/0.1=2.38V$

ID8V / 7.0A
OCP>=14A

ID05V_S0/7A
OCP>=14A



NEC
 $I_{rms}=7.5A (I_{sat}=10.4A)$
 $DCR=1.3m\ \Omega$
 $12*12*5.5$

NEC
 $I_{rms}=7.5A (I_{sat}=10.4A)$
 $DCR=13m\ \Omega$
 $12*12*5.5$

$V_{out}=V_{fb} * (1 + (R1/R2))$
 Where $V_{fb}=1.0V, R2=10K\ \Omega$

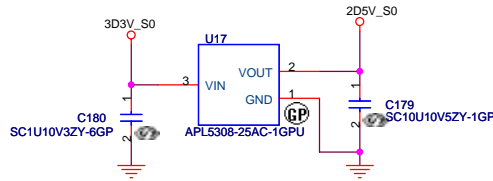
| Ton | Frequency (Out1)KHz | Frequency (Out2)KHz |
|------|---------------------|---------------------|
| AGND | 620 | 460 |
| REF | 485 | 355 |
| OPEN | 345 | 255 |
| VCC | 235 | 170 |

<Core Design>

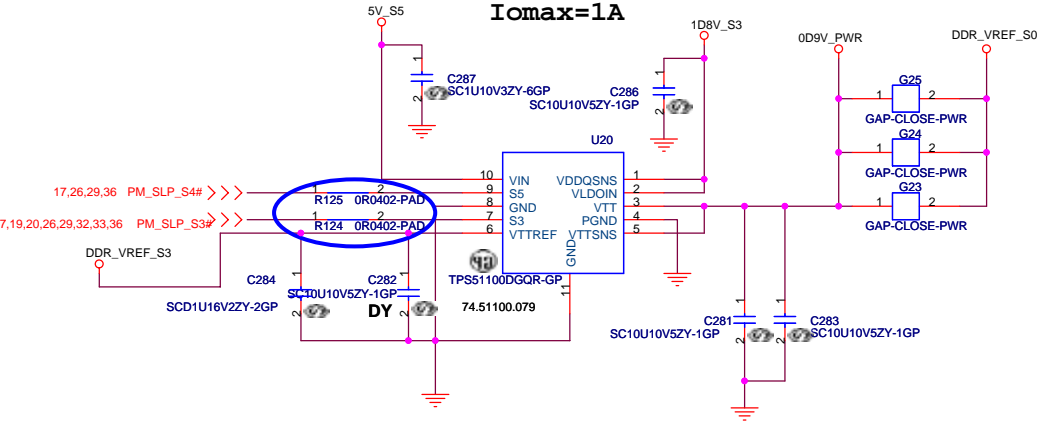
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **1D8V_S3/1D5V_S0**
 Size A3 | Document Number **MB3** | Rev **SA**
 Date: Wednesday, October 18, 2006 | Sheet 36 of 44

2D5V_S0
I_{omax}=300mA

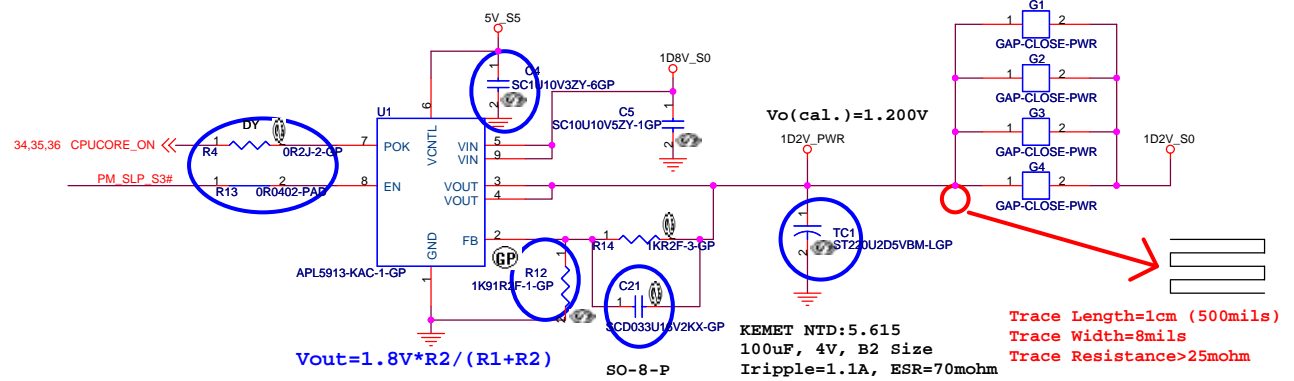


0D9V
I_{omax}=1A



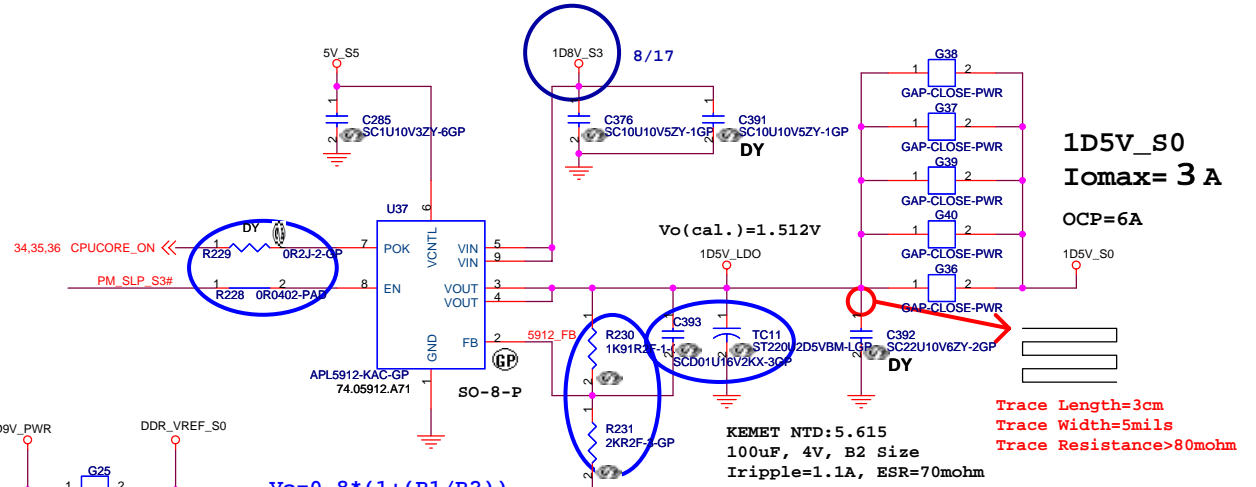
$$V_o = 0.8 * (1 + (R1/R2))$$

1D2V_S0
I_{omax}=3A



$$V_{out} = 1.8V * R2 / (R1 + R2)$$

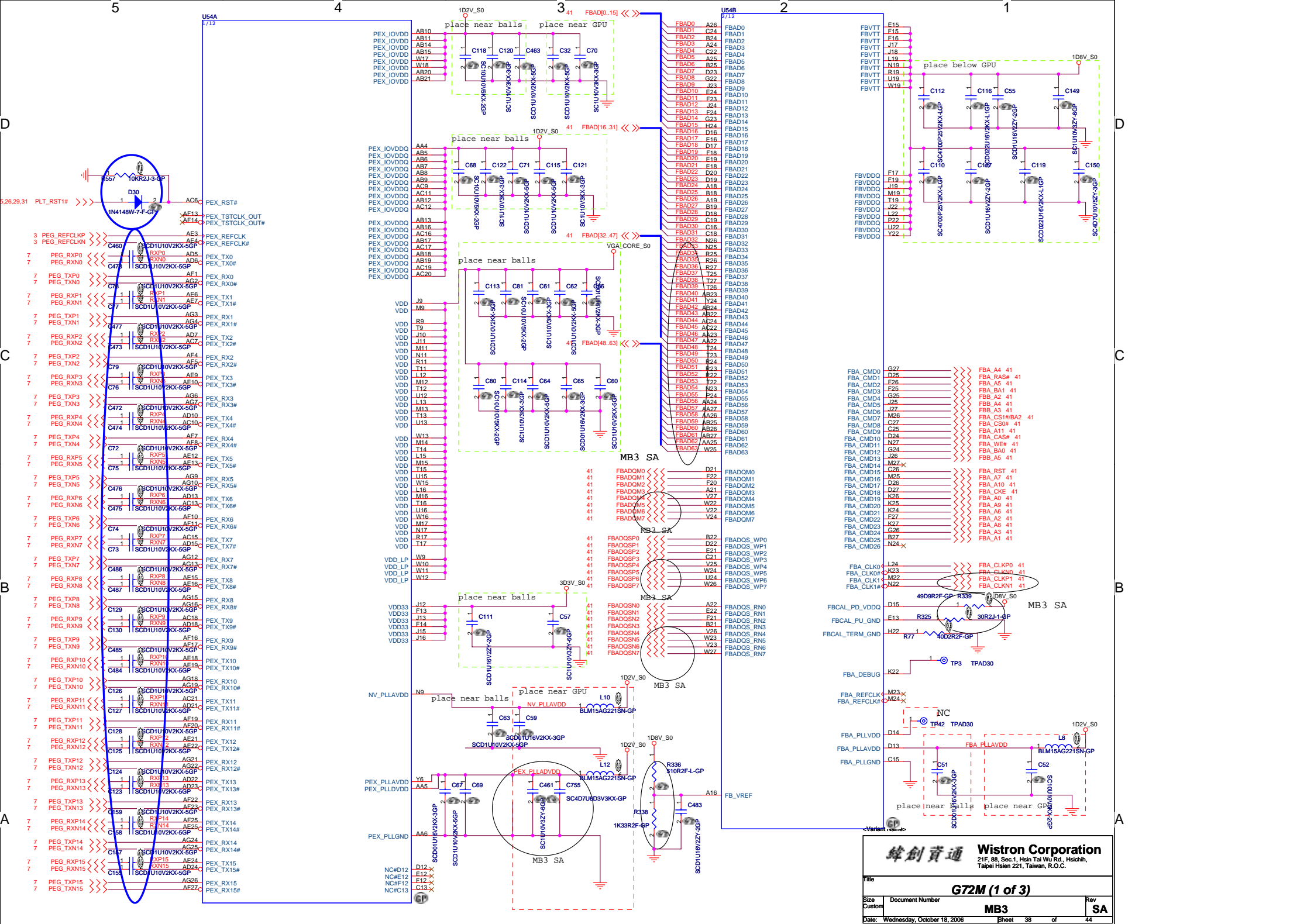
1D5V_S0
I_{omax}=3A
OCP=6A



Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

<Core Design>

| | | | |
|--|-----------------|----------------------------|----|
| 緯創資通 | | Wistron Corporation | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | | |
| Title | | | |
| 0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO | | | |
| Size | Document Number | Rev | |
| A3 | MB3 | SA | |
| Date: Wednesday, October 18, 2006 | | Sheet | of |
| | | 37 | 44 |



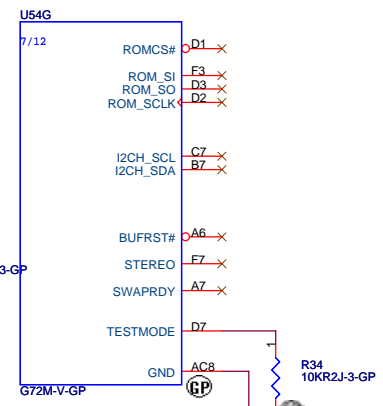
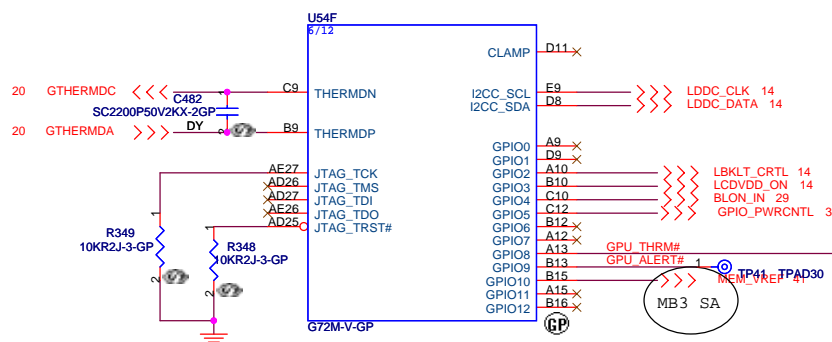
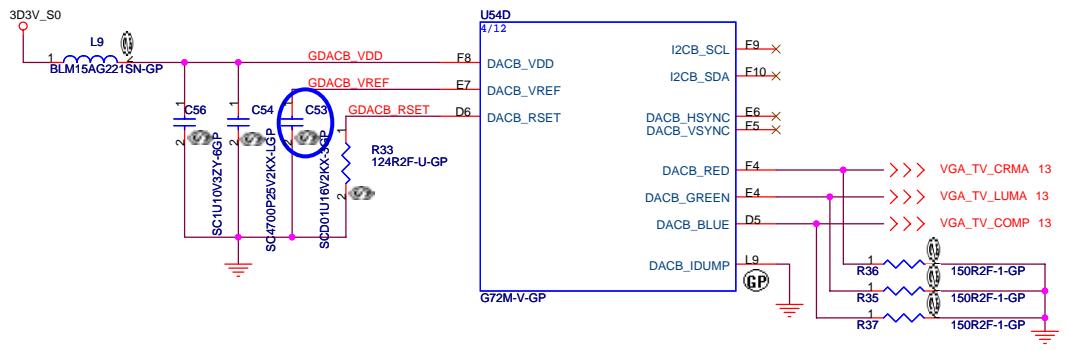
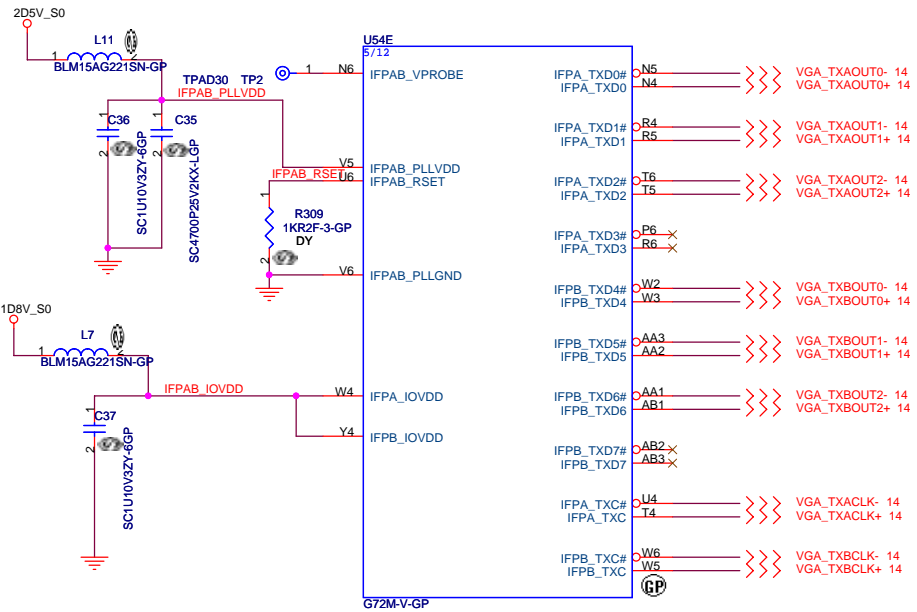
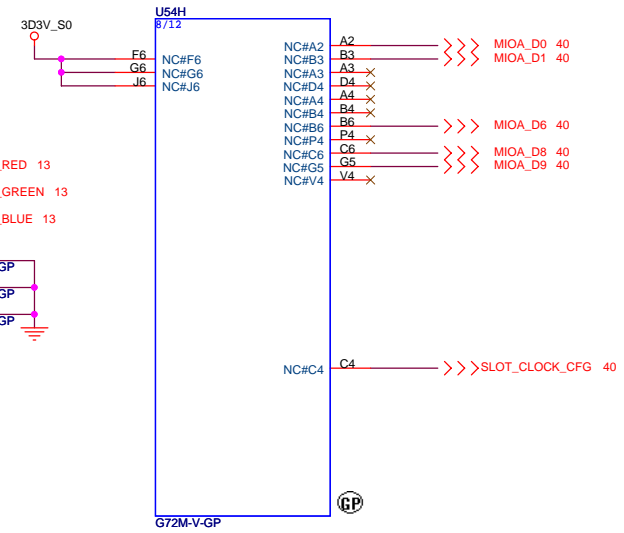
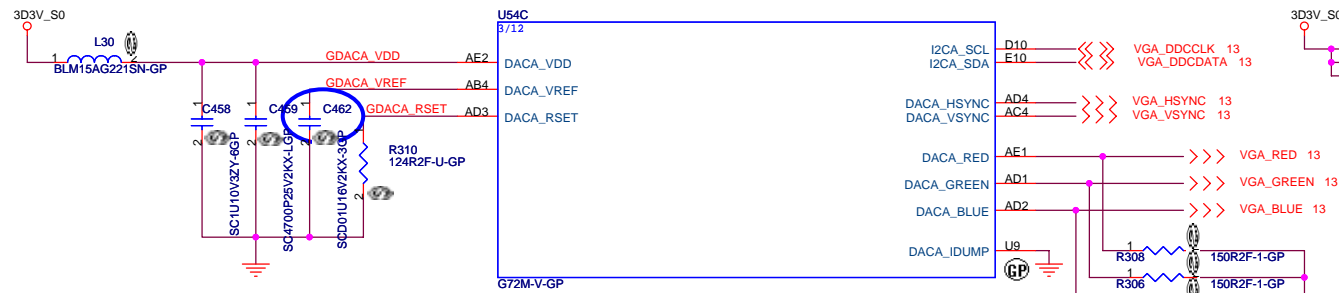
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 Taipei Hsien 221, Taiwan, R.O.C.

G72M (1 of 3)

MB3

Rev SA

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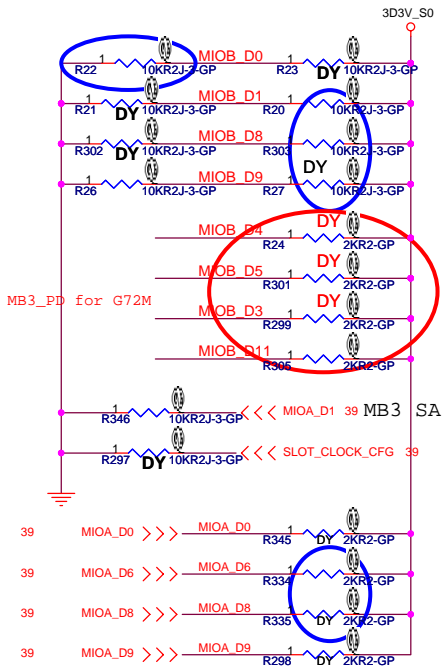
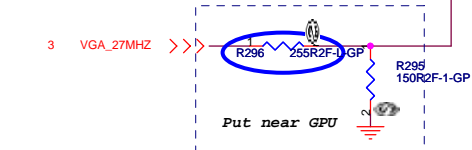
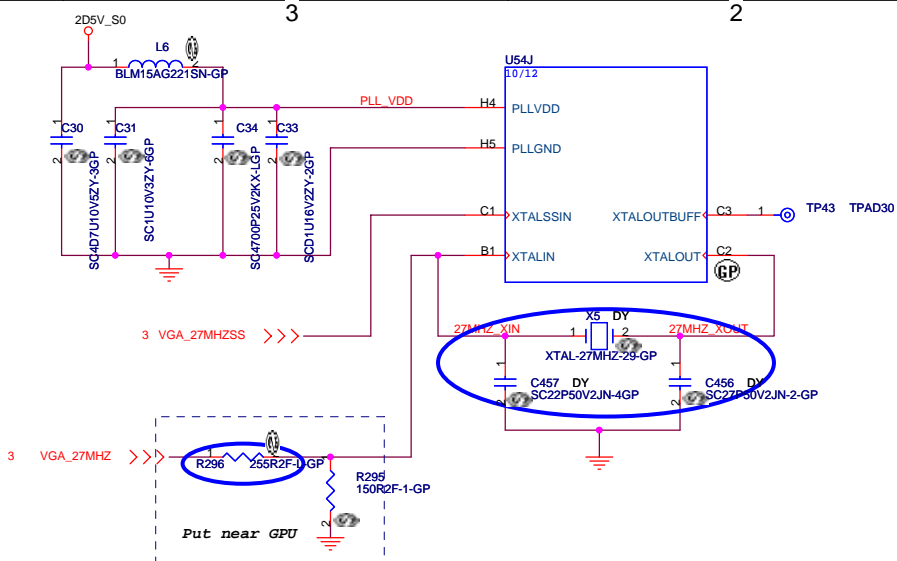
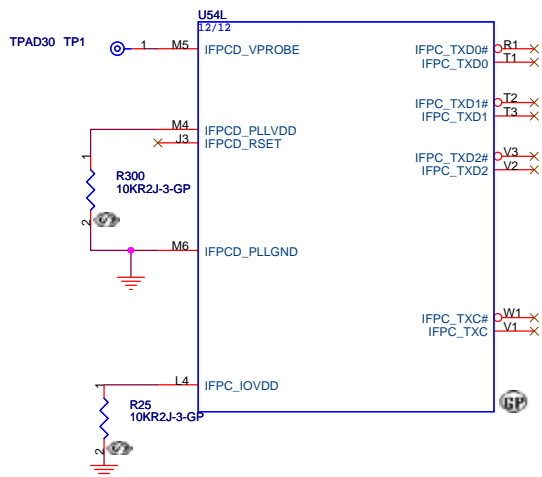
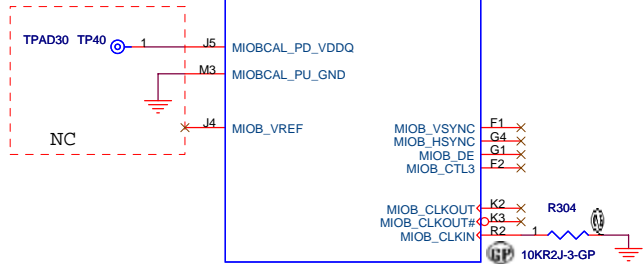
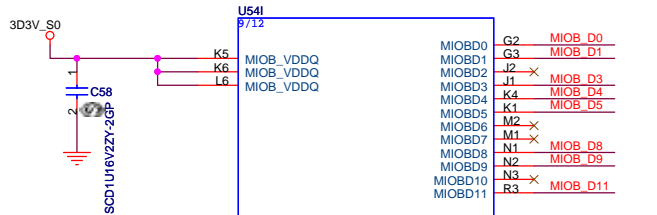


<Variant Name>

緯創資通 Wistron Corporation
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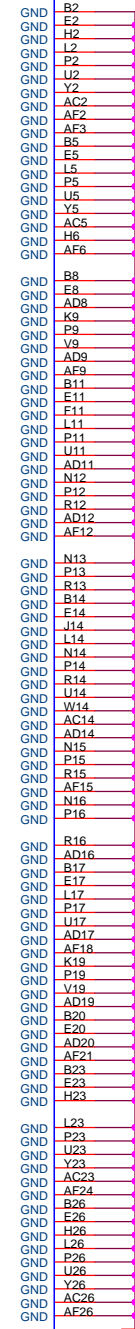
Title: **G72M (2 of 3)**

| | | |
|-----------------------------------|-----------------|-----------|
| Size A3 | Document Number | Rev |
| | MB3 | SA |
| Date: Wednesday, October 18, 2006 | Sheet 39 of 44 | |



1 means 1 pic, 0 means 2 pic

| Bit Signal | Values |
|----------------------------------|---|
| MIOB_D0: RAM_CFG_0 | GDDR3 8Mx32 64bit |
| MIOB_D1: RAM_CFG_1 | 1101 Infineon |
| MIOB_D8: RAM_CFG_2 | 1110 Hynix |
| MIOB_D9: RAM_CFG_3 | 1111 Samsung |
| MIOB_D4: PCL_DEVID_0 | G72M 1000 |
| MIOB_D5: PCL_DEVID_1 | G72M-V 0111 |
| MIOB_D3: PCL_DEVID_2 | G72M=2 0110 |
| MIOB_D11: PCL_DEVID_3 | |
| MIOA_D1: SUB_VENDOR | 0 SYSTEM BIOS 1 ADAPTER BIOS (DEFAULT) |
| MIOA_D0: PEX_PLL_EN_TERM100 | 0 ENABLED (DEFAULT) 1 DISABLED |
| MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0] | 0 DESKTOP (DEFAULT) 1 MOBILE |
| MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1] | |
| MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2] | |



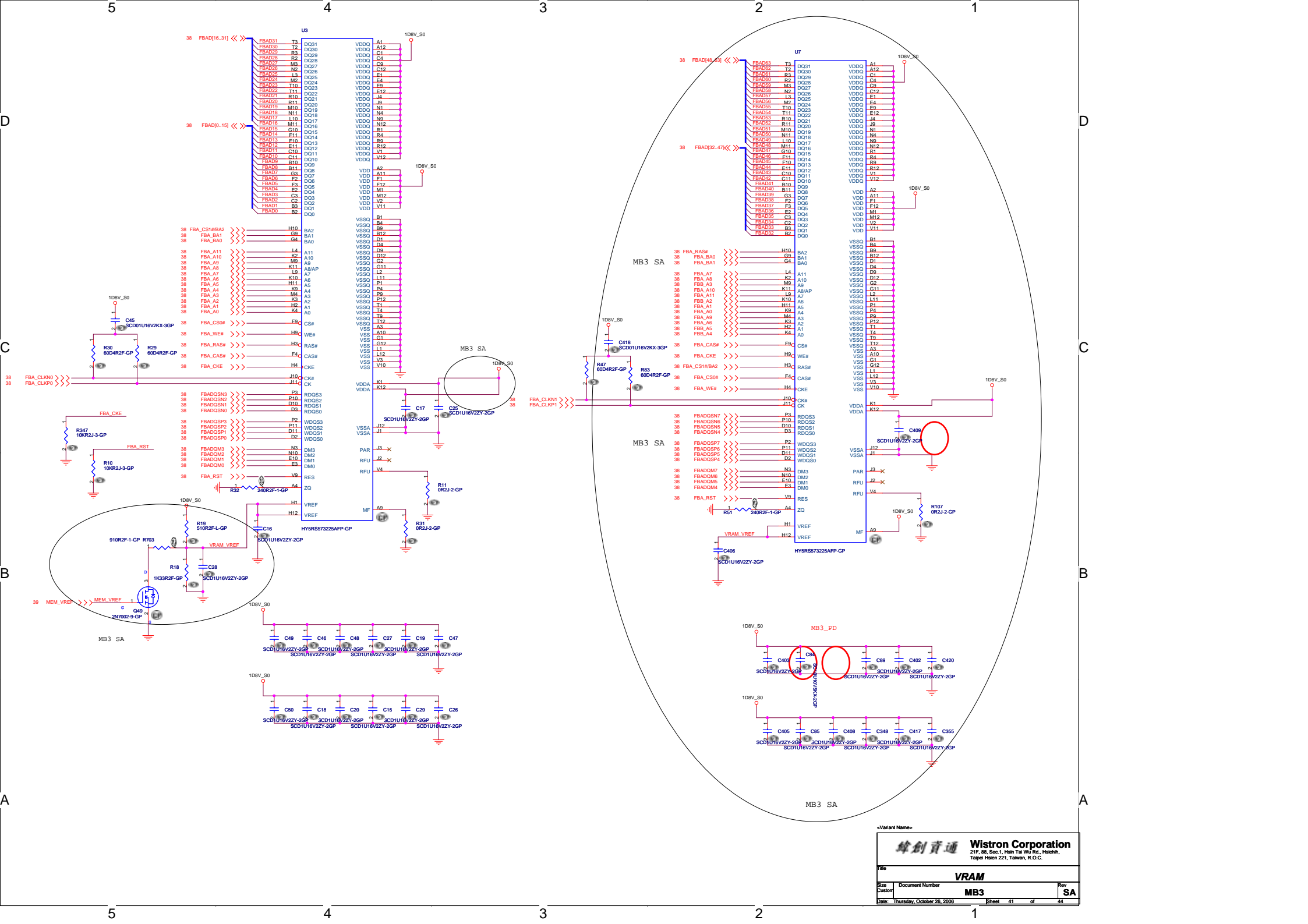
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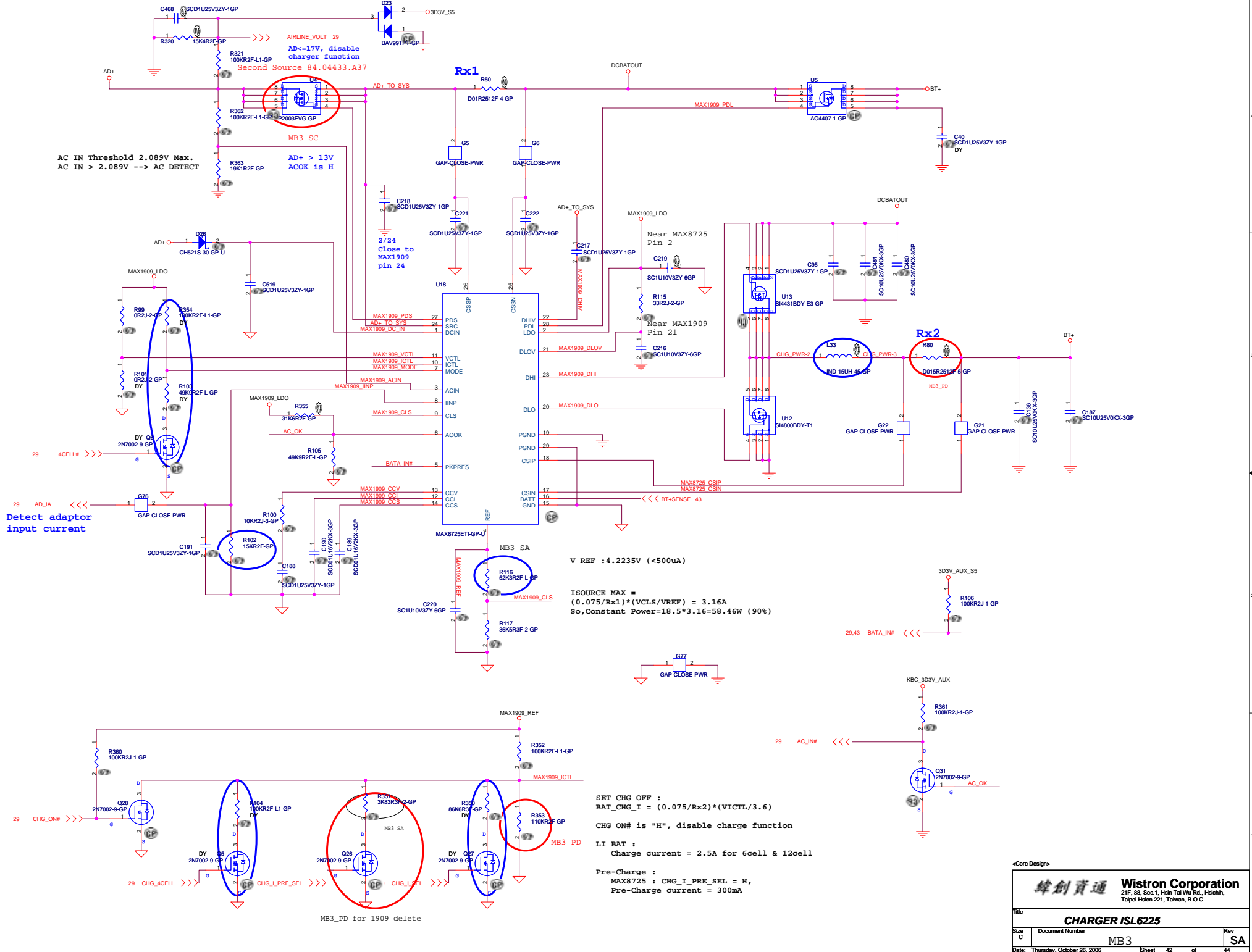
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G72M (3 of 3)**

Size A3 Document Number **MB3** Rev **SA**

Date: Wednesday, October 25, 2006 Sheet 40 of 44

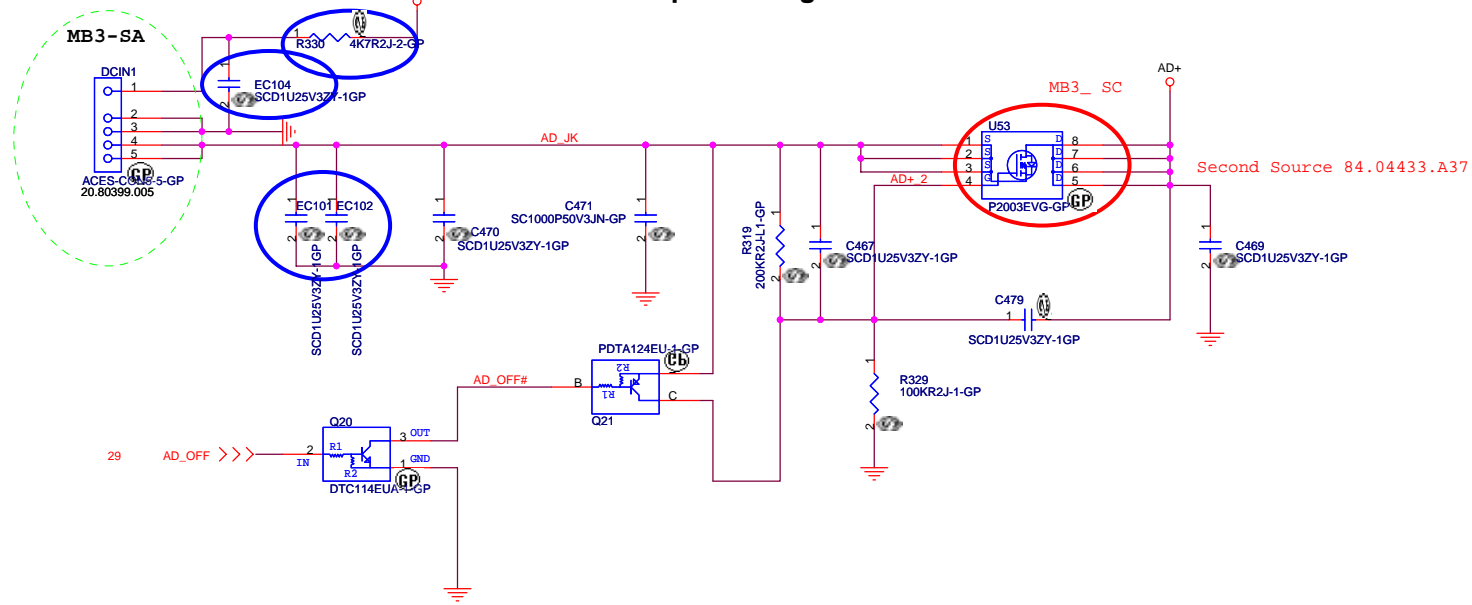




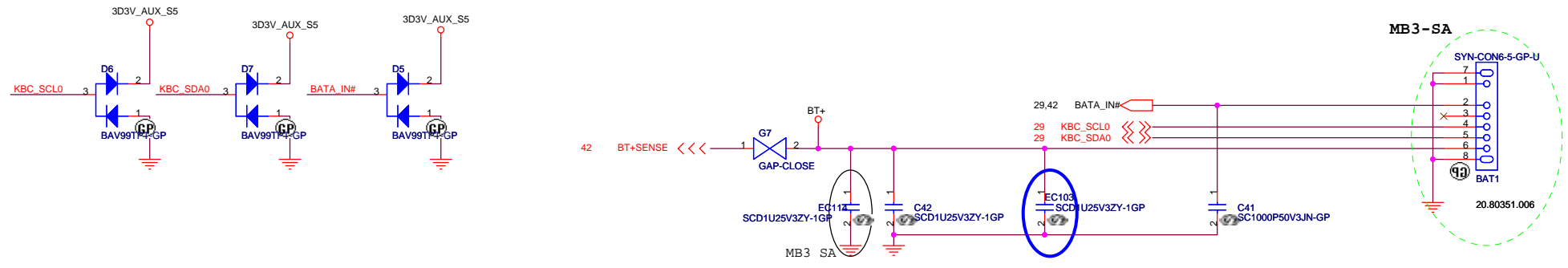
V_REF : 4.2235V (<500uA)
 ISOURCE_MAX =
 (0.075/Rx1)*(VCLS/VREF) = 3.16A
 So, Constant Power=18.5*3.16=58.46W (90%)

SET CHG OFF :
 BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
 CHG_ON# is "H", disable charge function
 LI BAT :
 Charge current = 2.5A for 6cell & 12cell
 Pre-Charge :
 MAX8725 : CHG_I_PRE_SEL = H,
 Pre-Charge current = 300mA

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

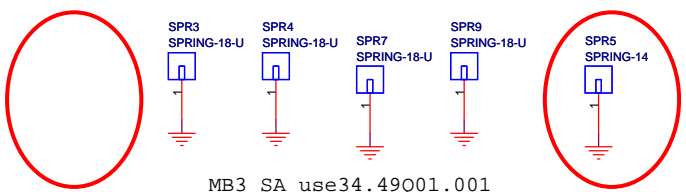
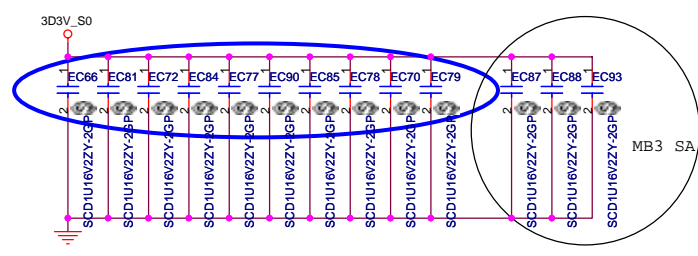
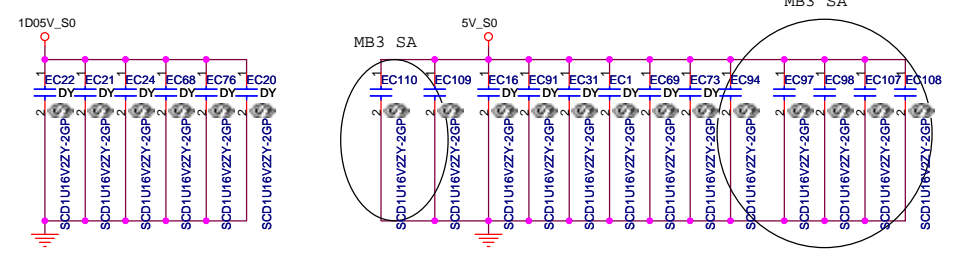
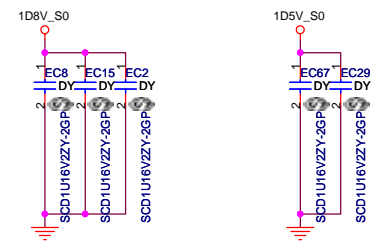
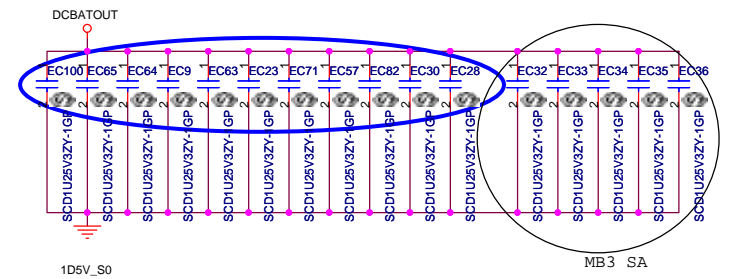
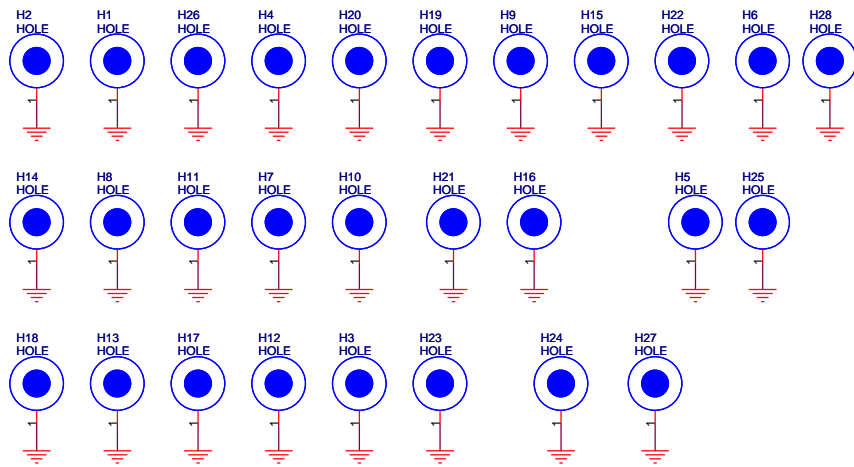


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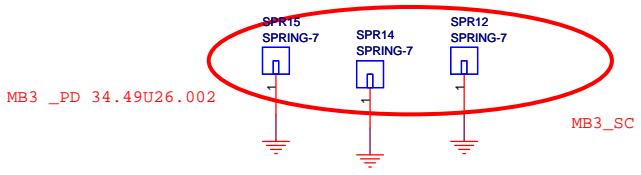
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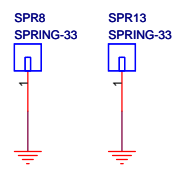
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MB3_PD 34.49U26.002

MB3_SC

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all of the parts followed MB2.

check them later

<Core Design>

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| Size | Document Number | Rev | |
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