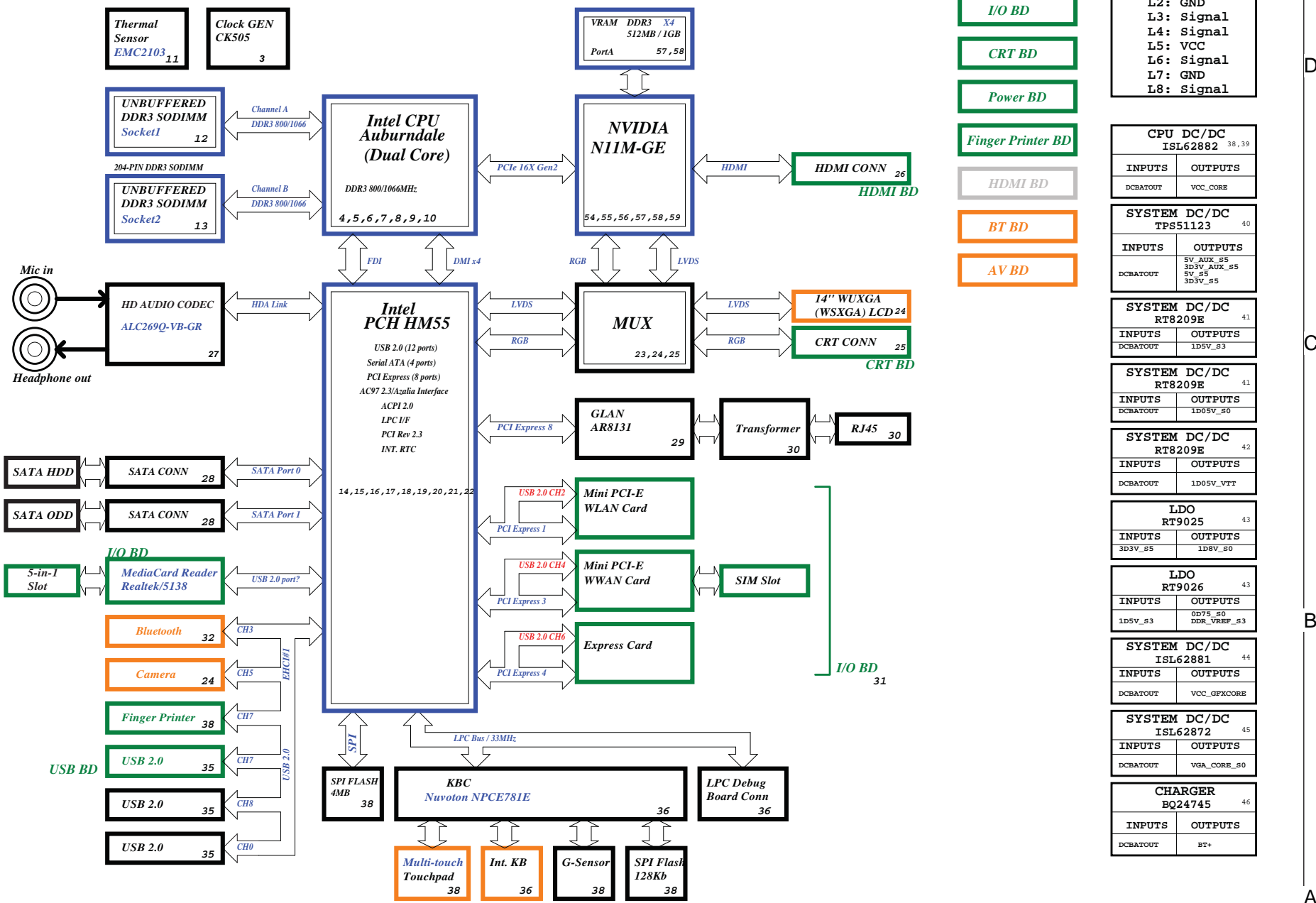


LA46 Switchable Graphics System Schematics

<http://hobi-elektronika.net>

Project Code: 91.4GV01.001
PCB(Raw Card): 09911-1



- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- HDMI BD
- BT BD
- AV BD

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC ISL62882 38,39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC ISL62872 45	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

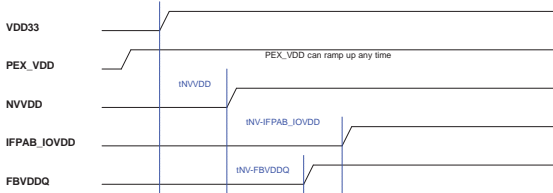
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

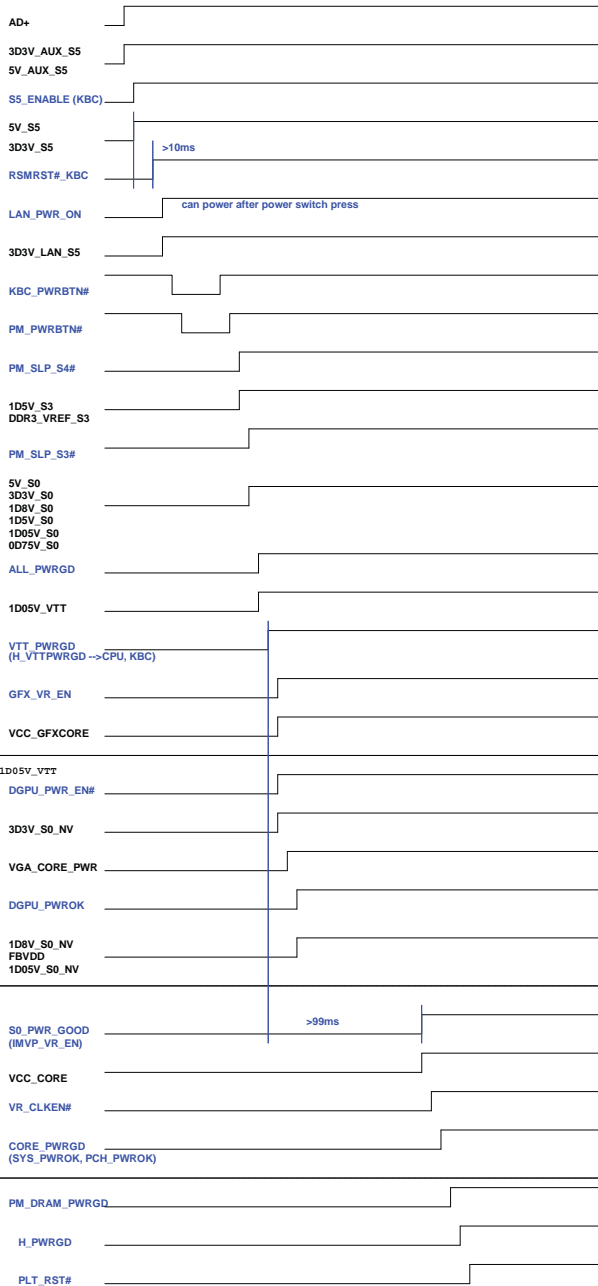
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence

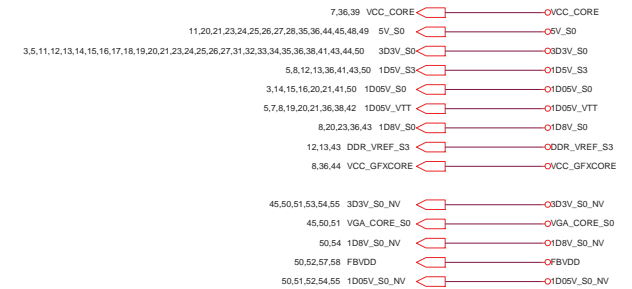


Sequence AC



PLANAR_ID[1..0]

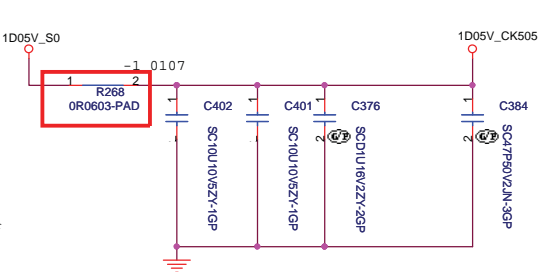
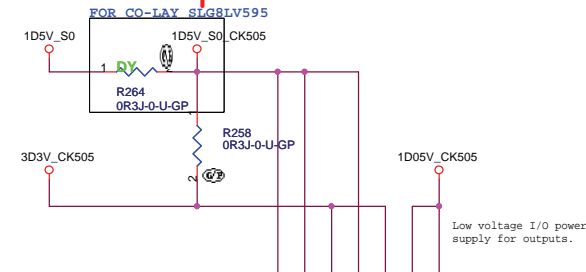
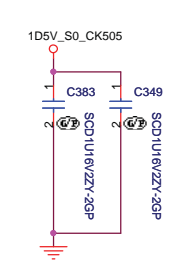
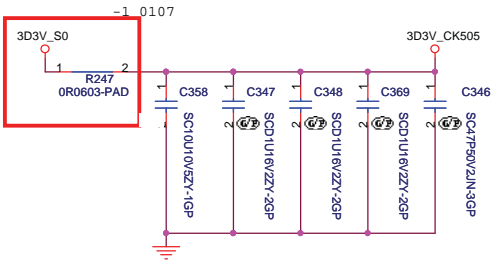
KBC GPIn	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0	LA46 - SA	SA
	0	0	LA46 - SB	SB
	0	1	LA46 - SB	SC
	1	0	LA46 - SB	SC
	1	1		-1



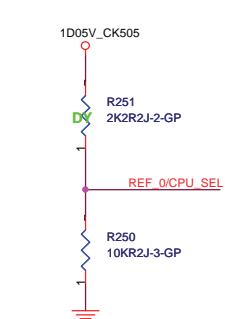
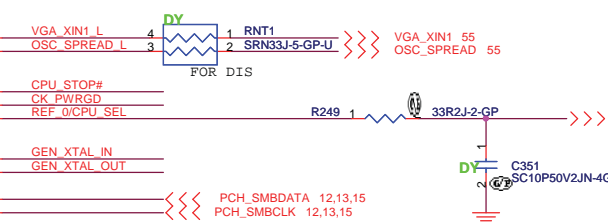
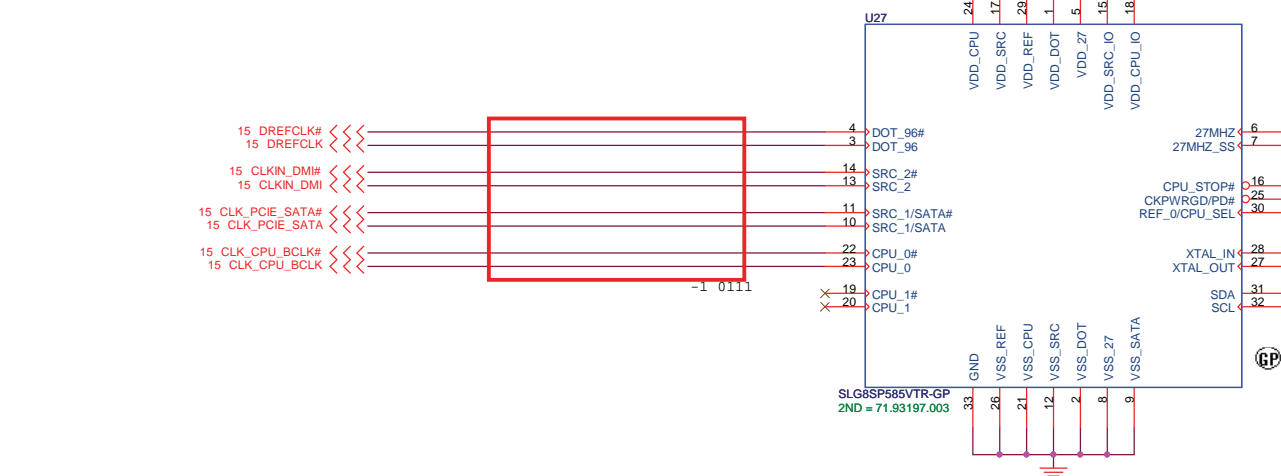
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

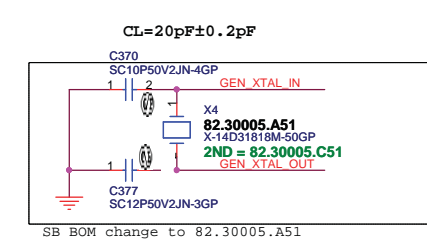
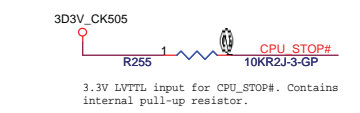
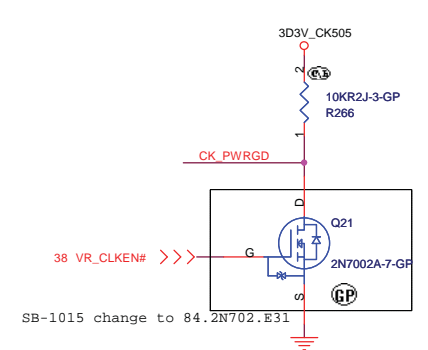
File	02 Reference	Rev
Size	Document Number	Rev
A2	LA46 MB	-1
Date:	Wednesday, January 27, 2010	Sheet 2 of 58



VGA 27M	RNT1	R75	X1	R79	R80	C107	C131
Crystal	DY	DY	Mount	Mount	Mount	Mount	Mount
CLK GEN	Mount	Mount	DY	DY	DY	DY	DY

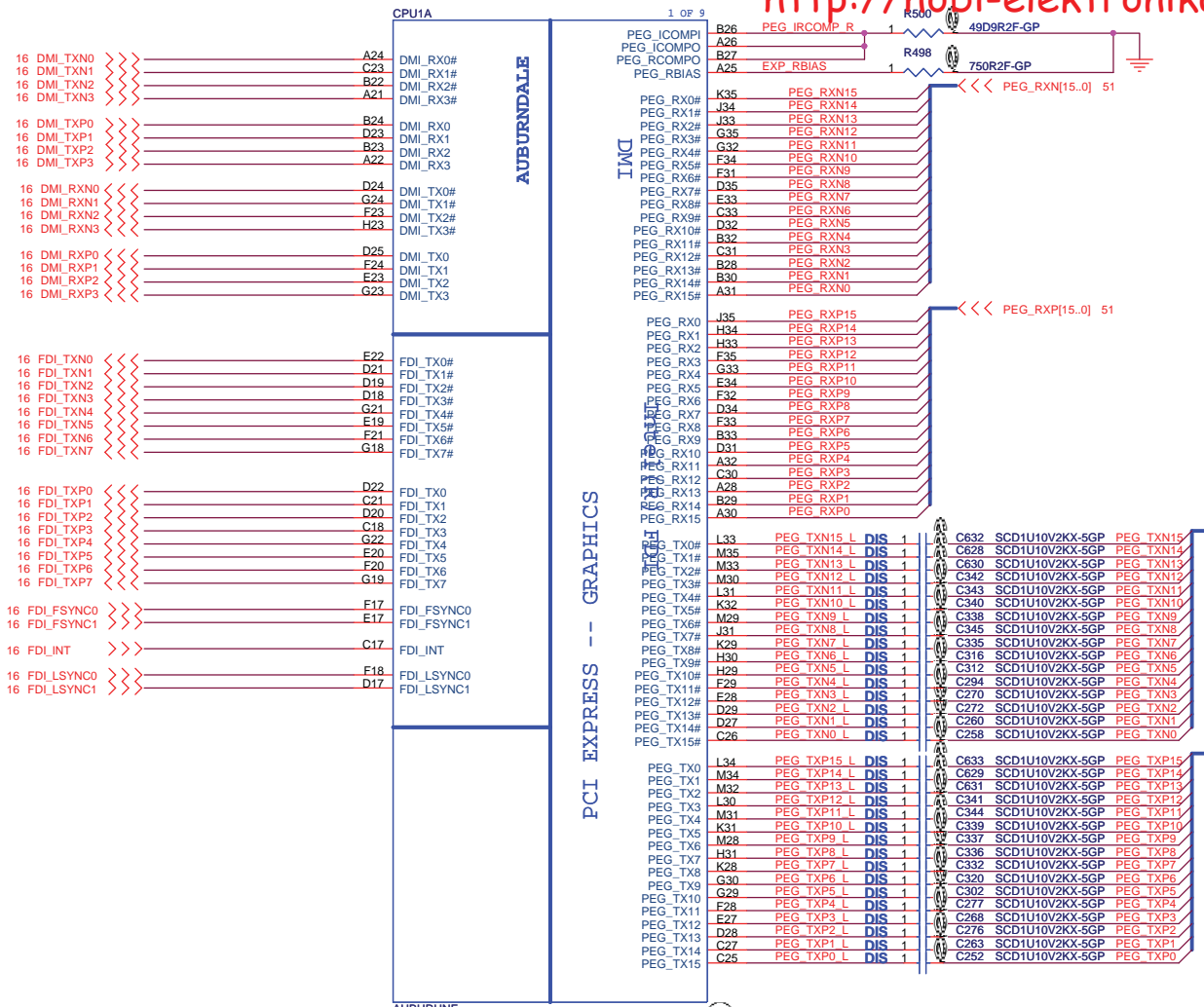


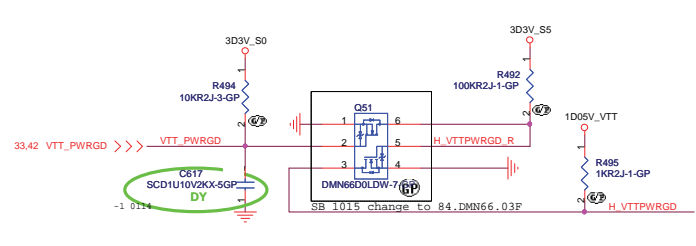
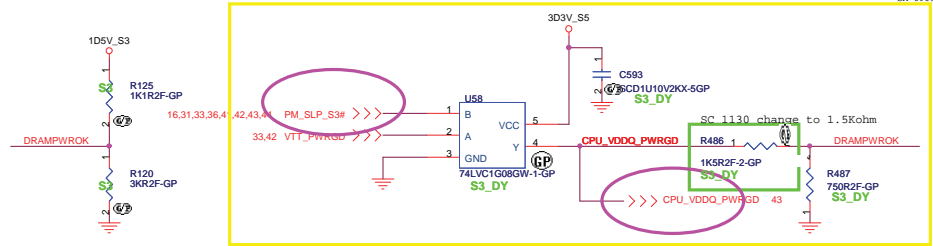
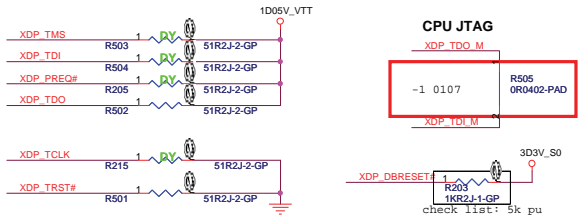
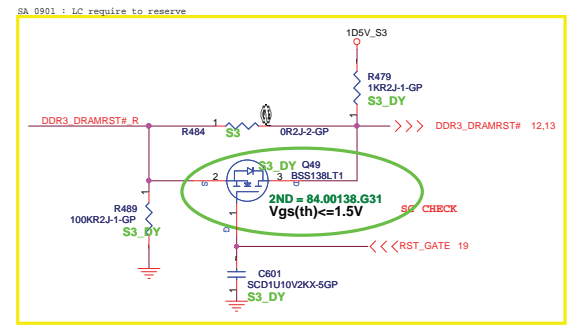
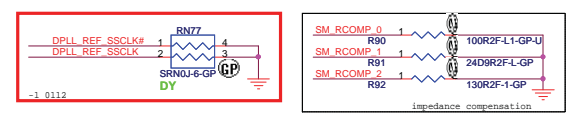
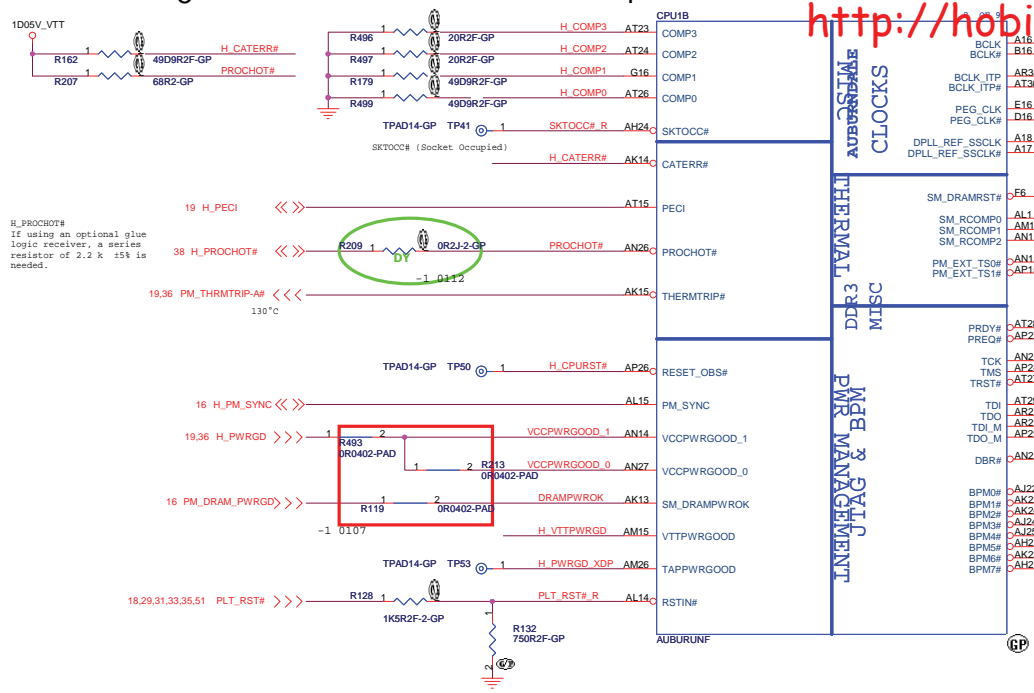
FSC	0	1
SPEED	133MHz (Default)	100MHz



Layout Notes:

Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.





<Core Design>

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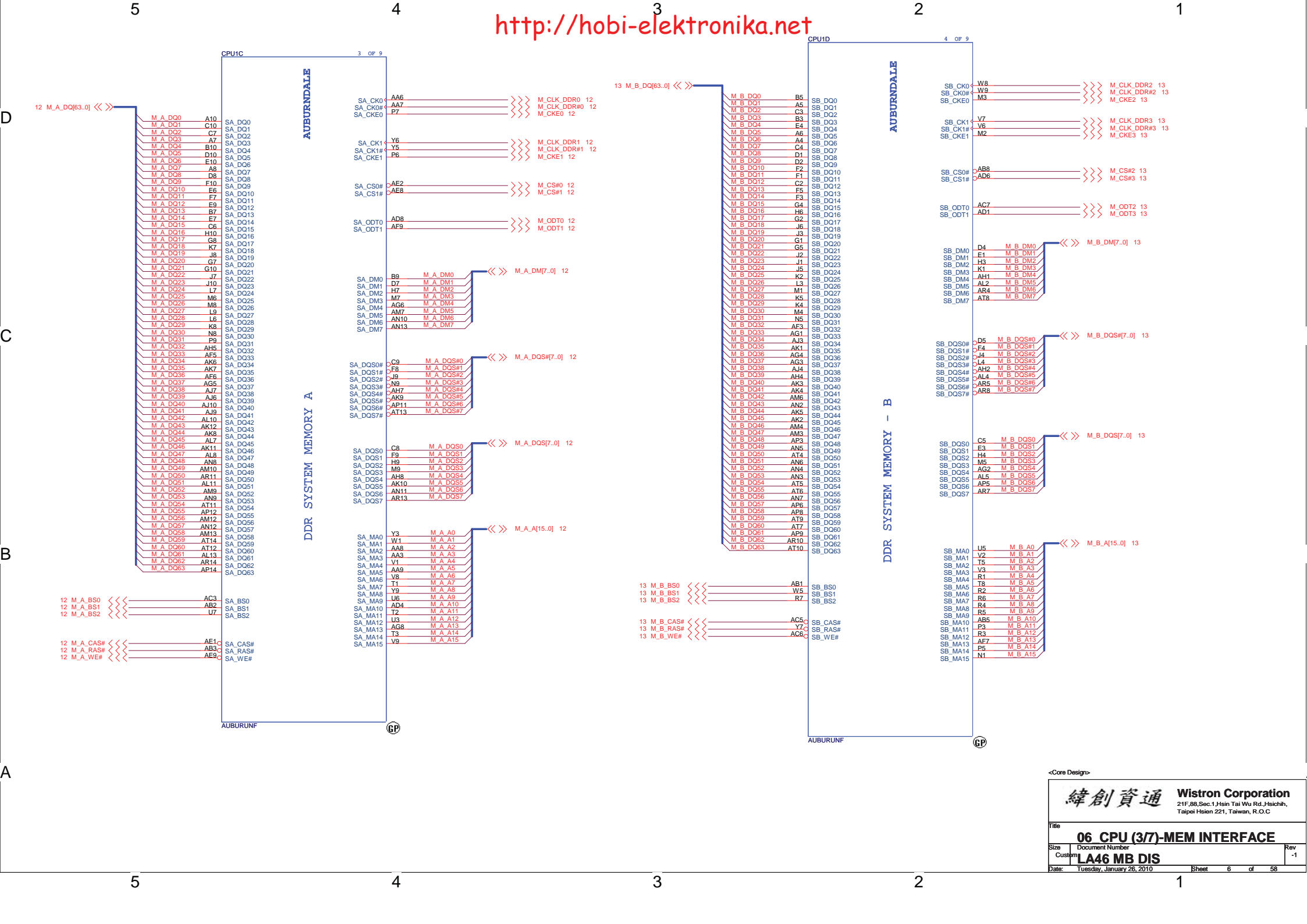
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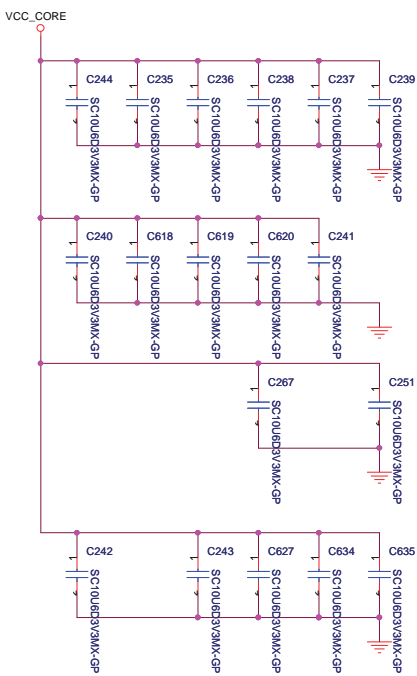
Size: Document Number **LA46 MB DIS** Rev: 1

Customer: **LA46 MB DIS**

Date: Tuesday, January 26, 2010 Sheet 5 of 58



PROCESSOR CORE POWER
48A -->Arrandale



- VCC_CORE
- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
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- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
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- P26 VCC

AUBURNDALE

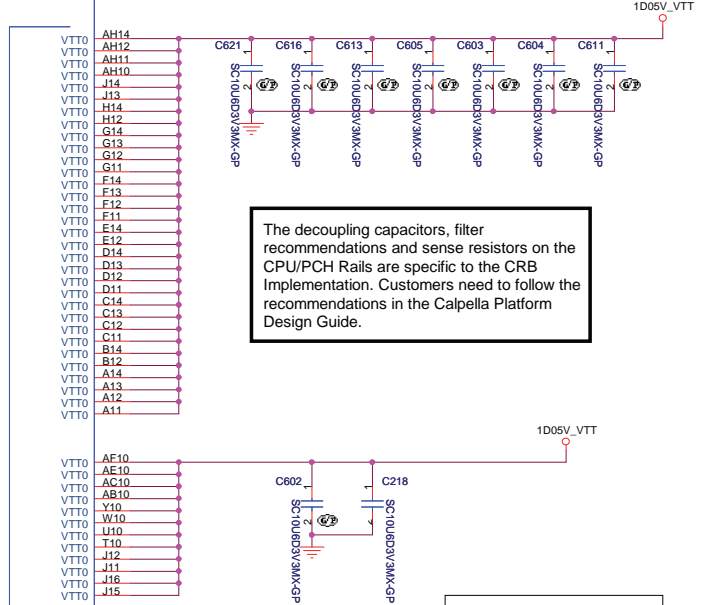
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

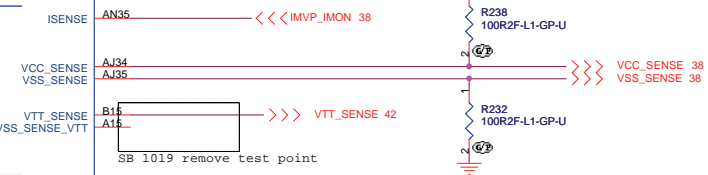
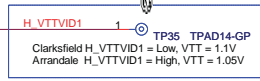
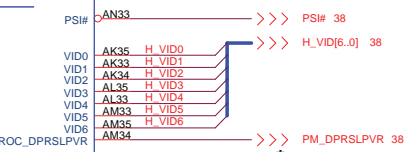
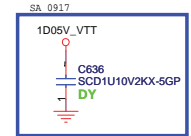
CPU VIDS

SENSE LINES

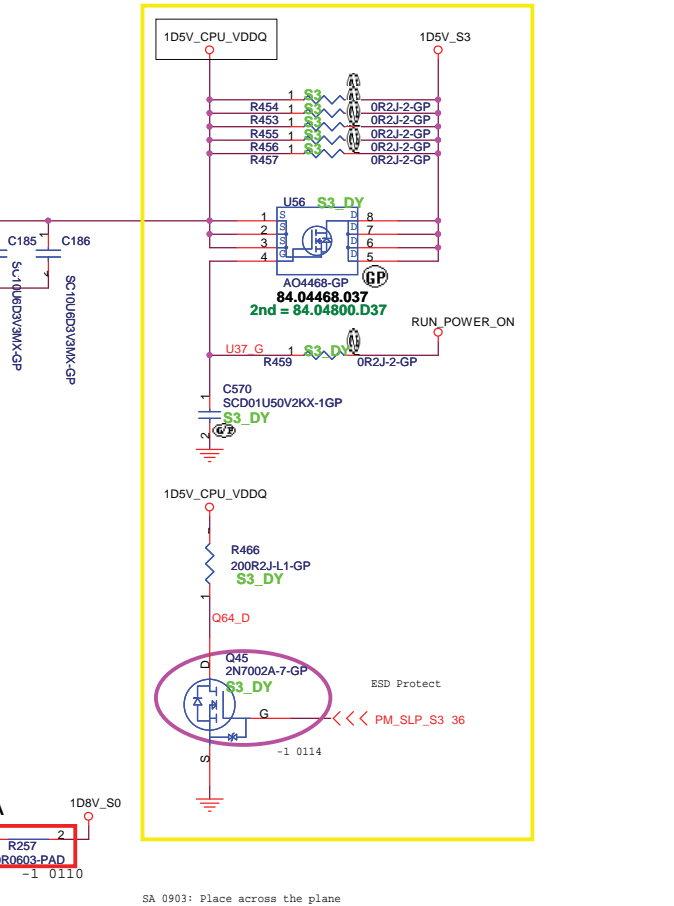
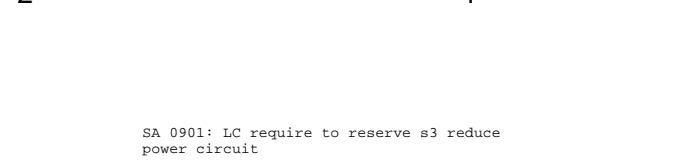
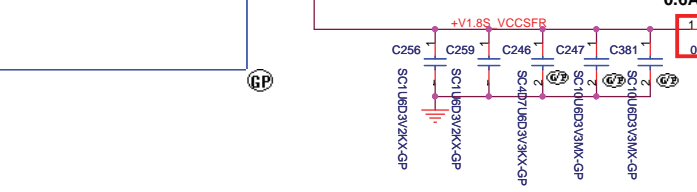
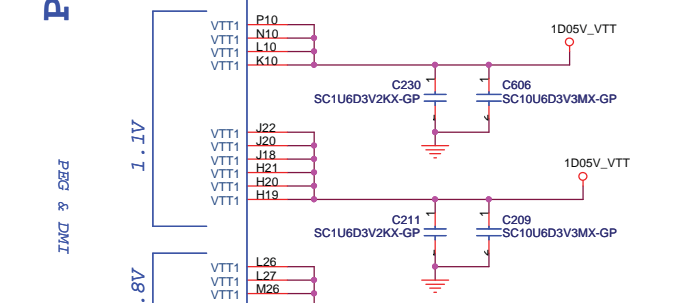
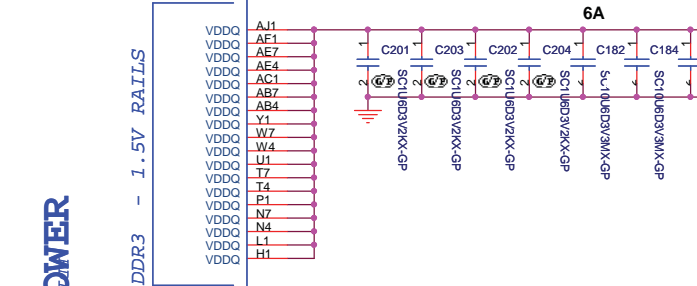
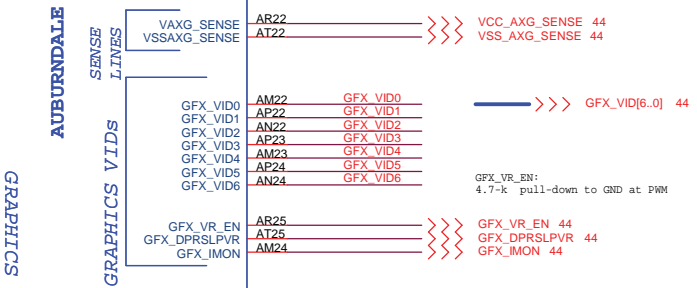
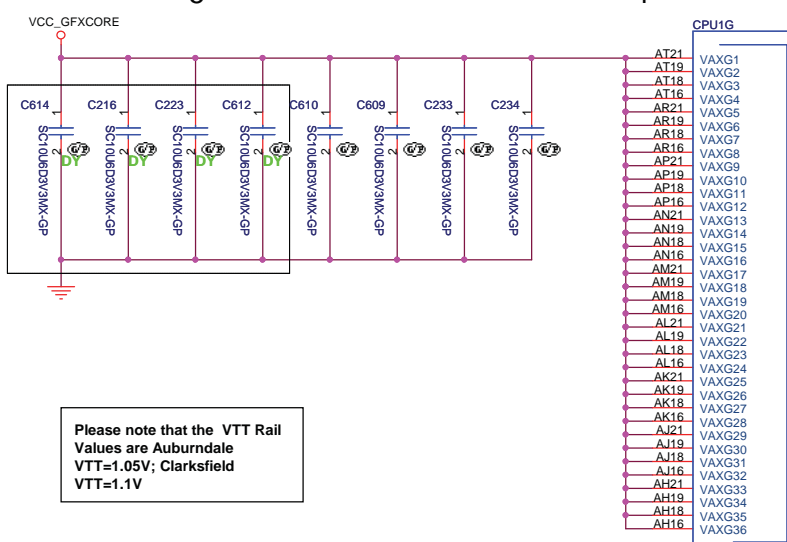


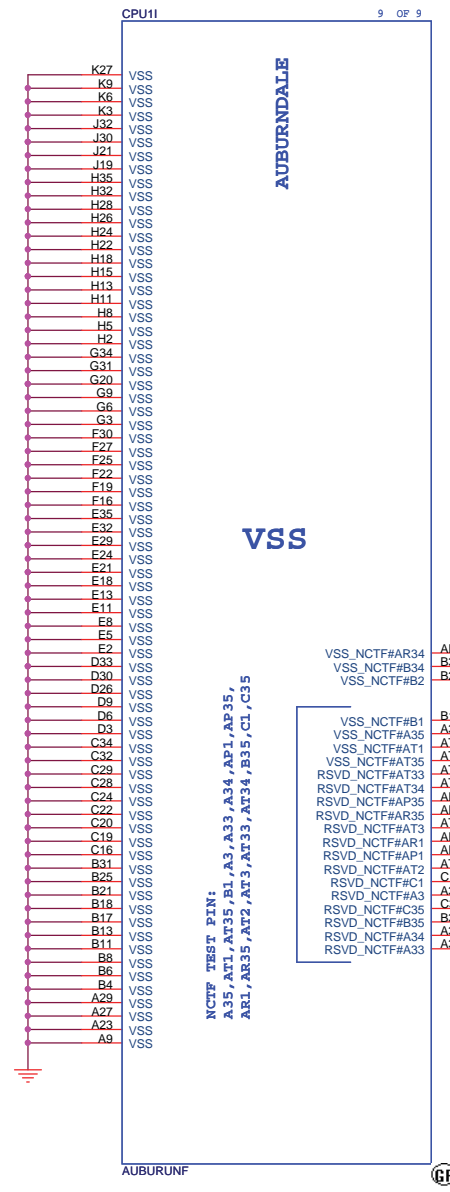
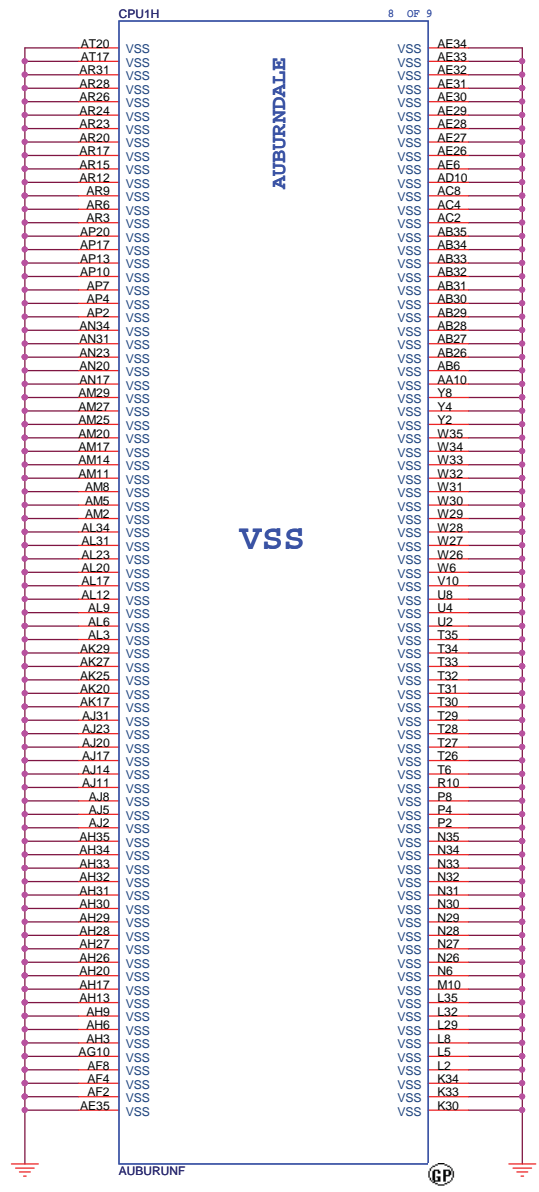
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



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21F,88,Sec.1,Hsin Tai Wu Rd.,Hsiehchih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 07 CPU (4/7)-POWER
Size: Custom LA46 MB DIS
Date: Wednesday, January 27, 2010 Sheet 7 of 88

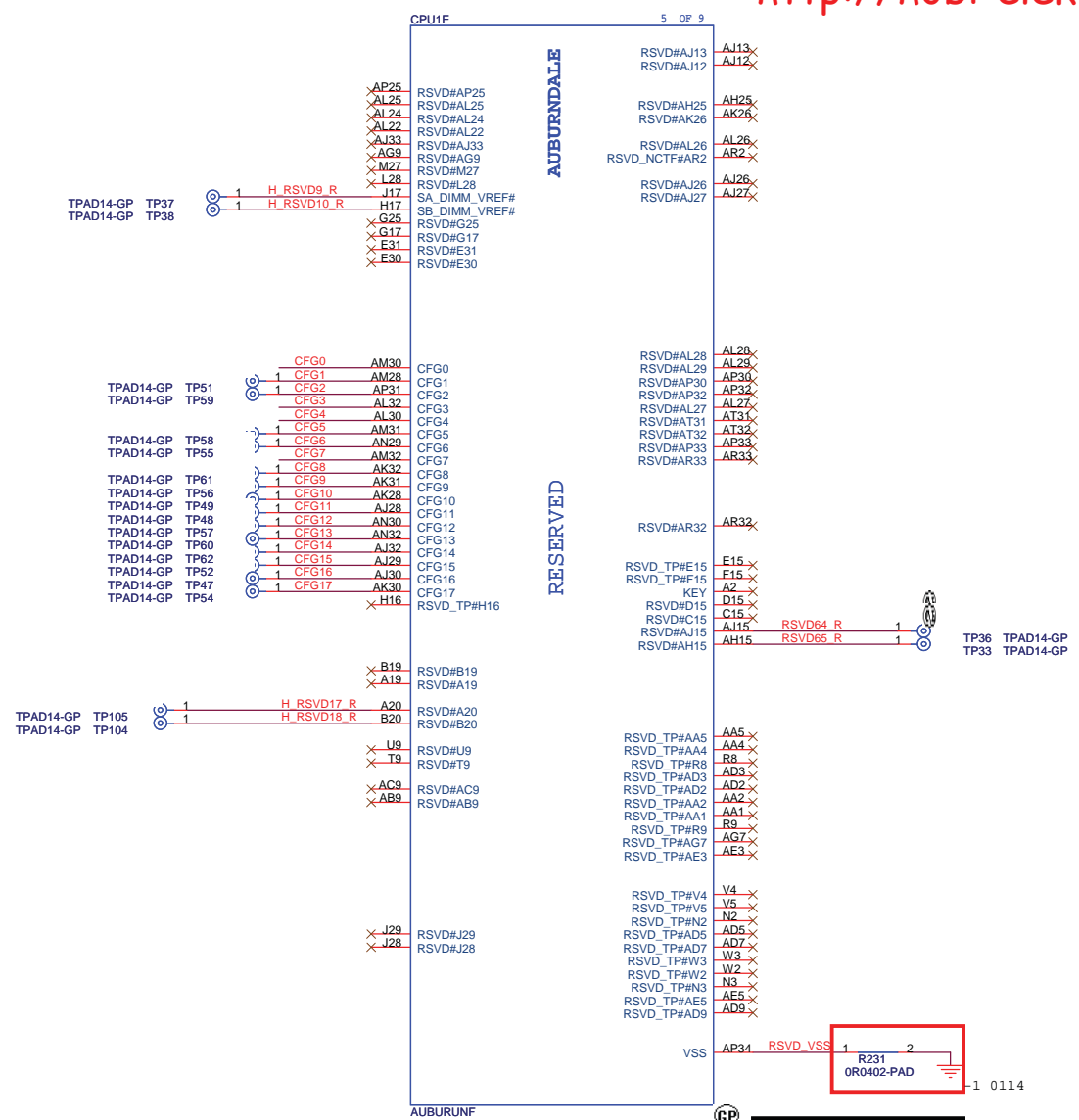




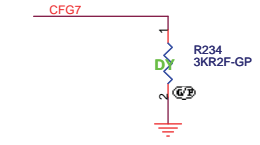
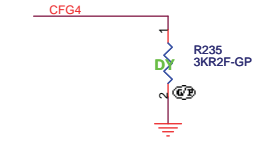
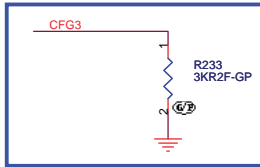
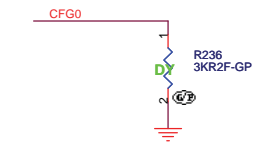
NCTF TEST PIN:
A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,
AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35

VSS_NCTF#AR34	AR34				
VSS_NCTF#B34	B34				
VSS_NCTF#B2	B2				
VSS_NCTF#B1	B1	TP	MCP	VSS	NCTF6
VSS_NCTF#A35	A35	TP	MCP	VSS	NCTF1
VSS_NCTF#AT1	AT1	TP	MCP	VSS	NCTF2
VSS_NCTF#AT35	AT35	TP	MCP	VSS	NCTF7
RSVD_NCTF#AT33	AT33				
RSVD_NCTF#AT34	AT34				
RSVD_NCTF#AP35	AP35				
RSVD_NCTF#AR35	AR35				
RSVD_NCTF#AT3	AT3				
RSVD_NCTF#AR1	AR1				
RSVD_NCTF#AP1	AP1				
RSVD_NCTF#AT2	AT2				
RSVD_NCTF#C1	C1				
RSVD_NCTF#A3	A3				
RSVD_NCTF#C35	C35				
RSVD_NCTF#B35	B35				
RSVD_NCTF#A34	A34				
RSVD_NCTF#A33	A33				





VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



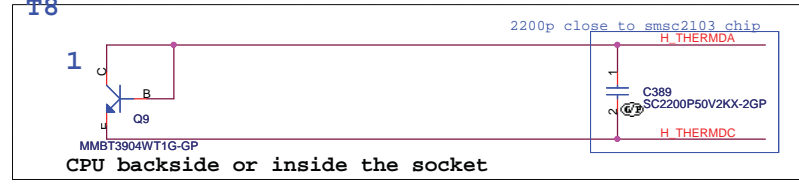
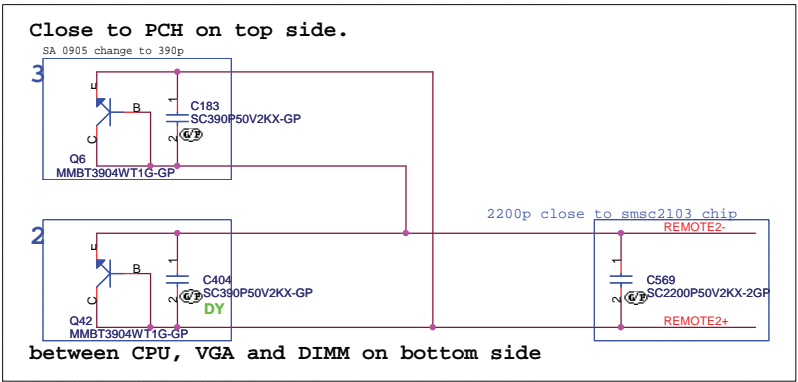
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

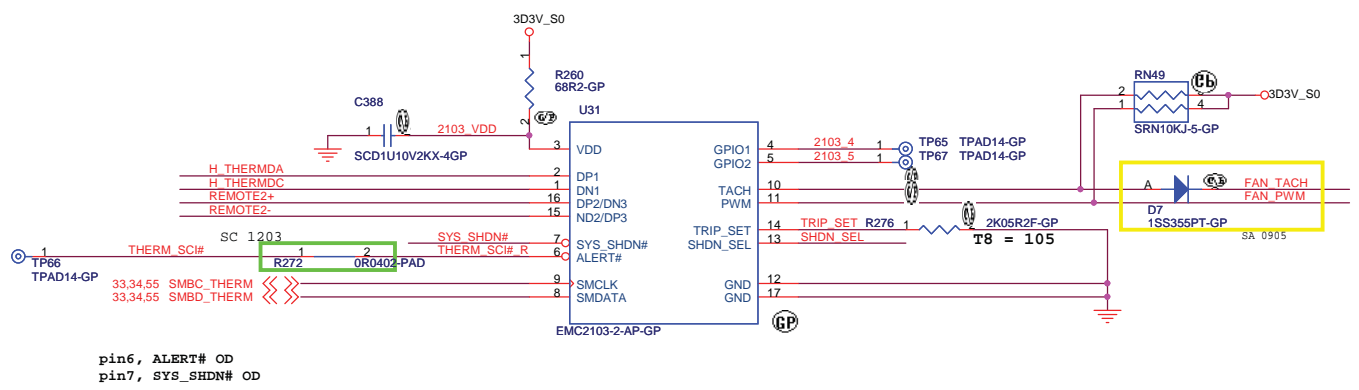
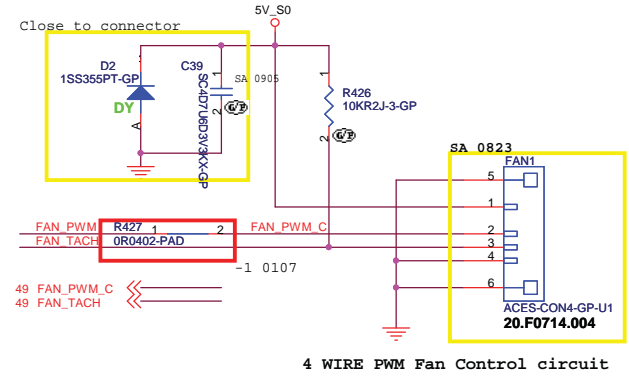
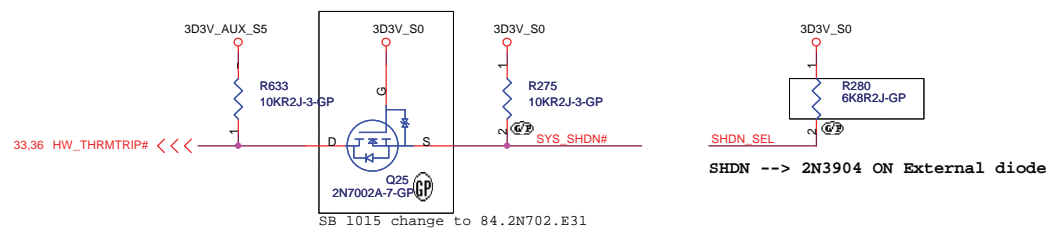
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

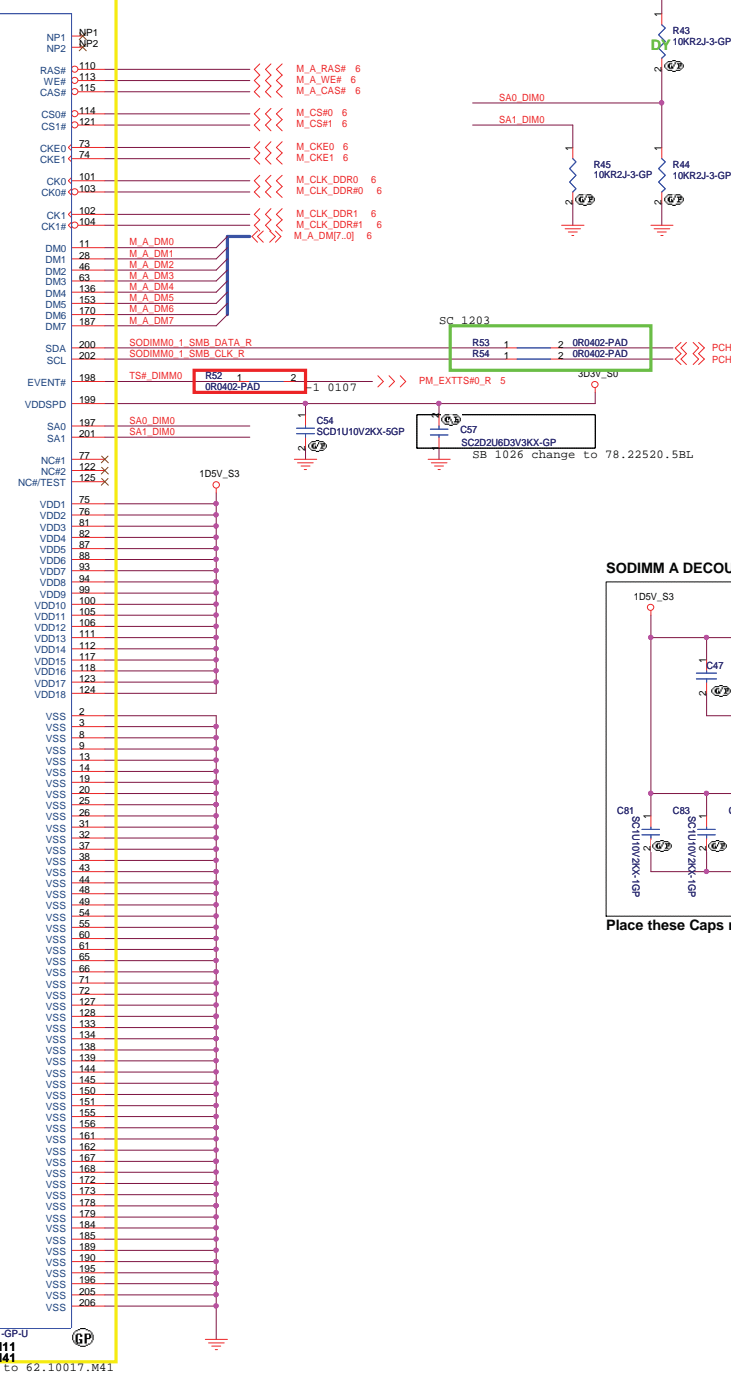
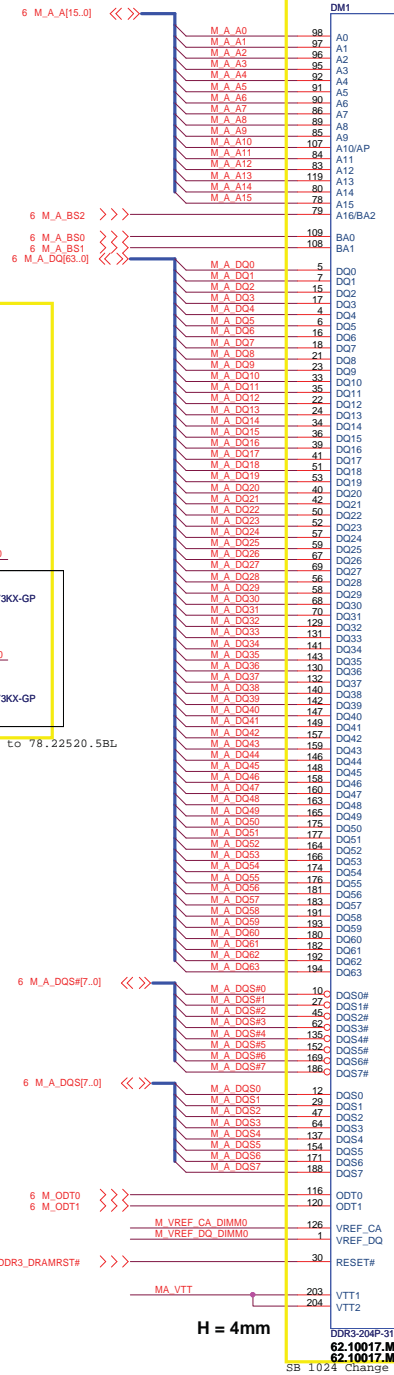
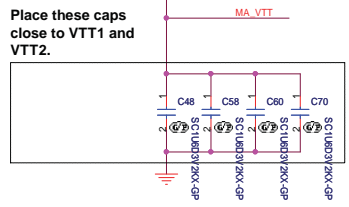
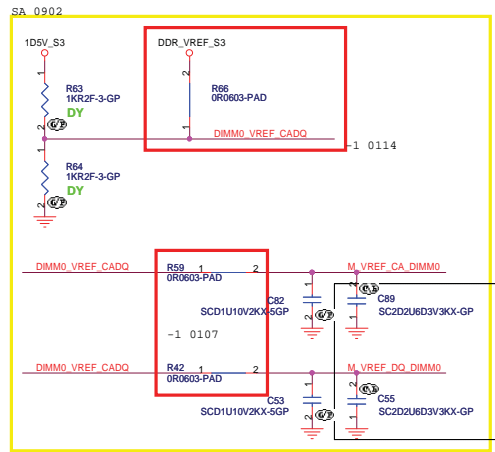
CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

<Core Design>

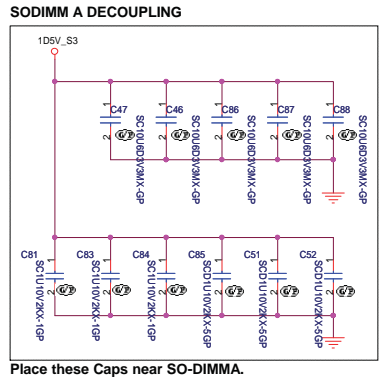


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

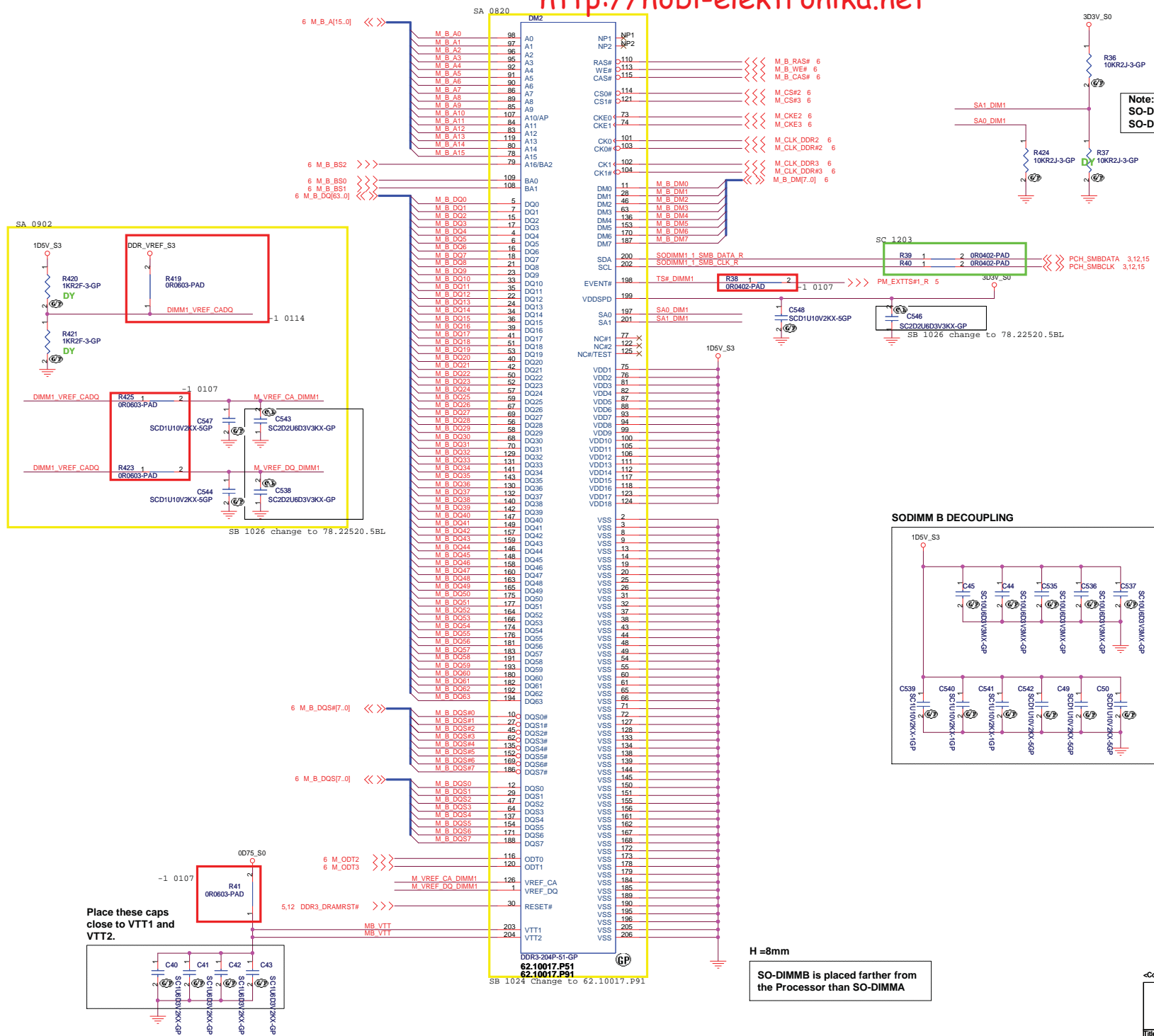




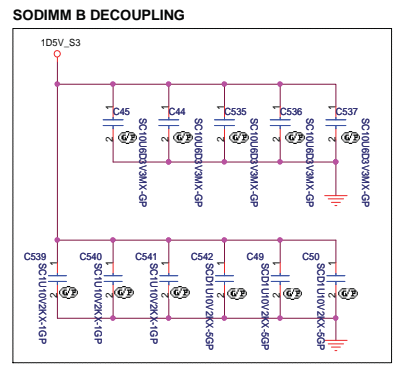
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



H = 4mm
 62-10017.M11
 62-10017.M41
 SB 1024 Change to 62.10017.M41



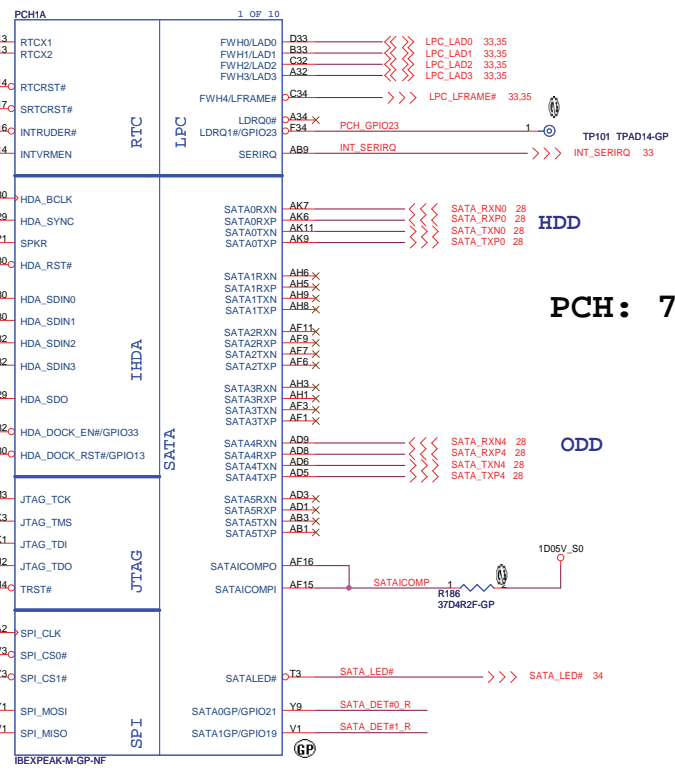
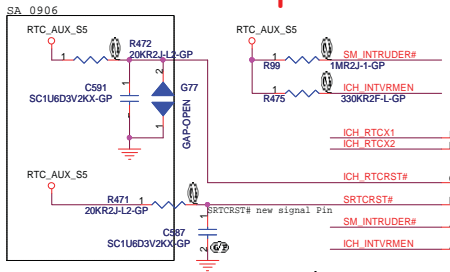
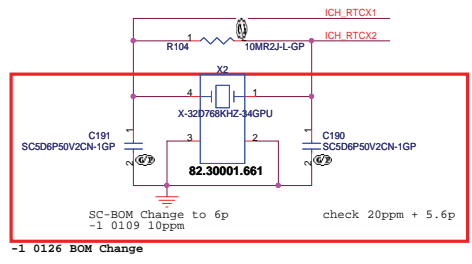
Note:
SO-DIMMB SPD Address is 0x44
SO-DIMMB TS Address is 0x34



H = 8mm
SO-DIMMB is placed farther from the Processor than SO-DIMMA

Place these caps close to VTT1 and VTT2.

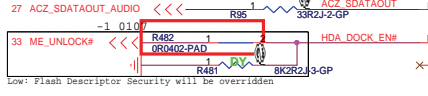
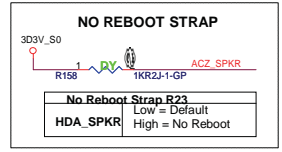
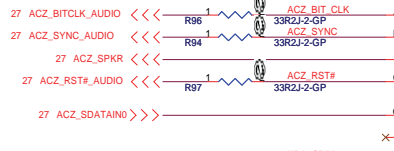
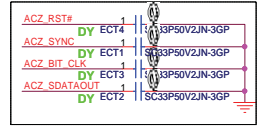
integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable



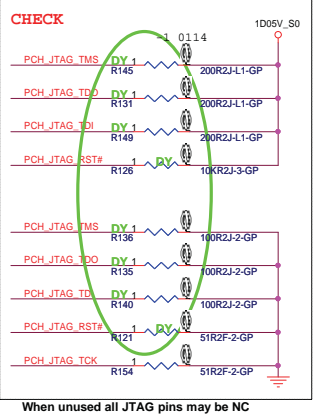
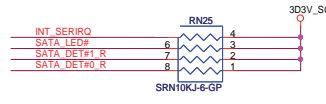
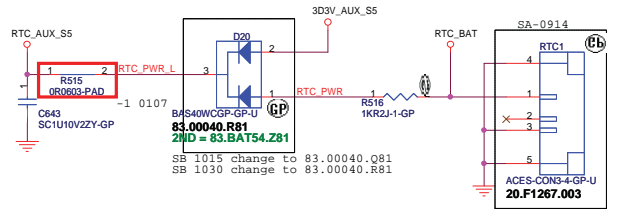
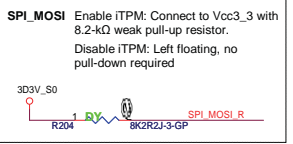
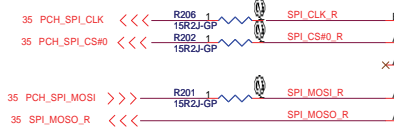
PCH: 71.0IBEX.G0U

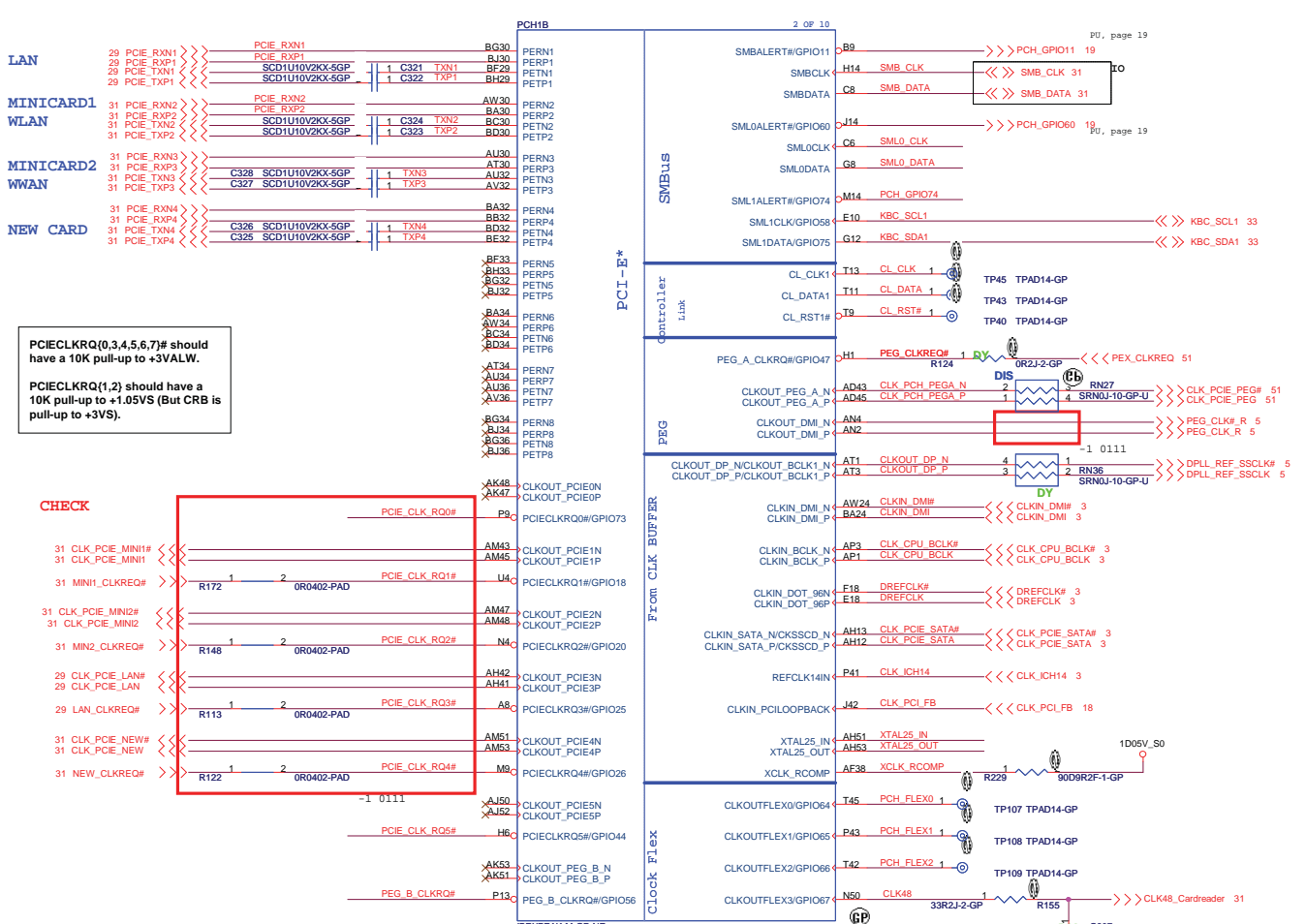
HDD

ODD



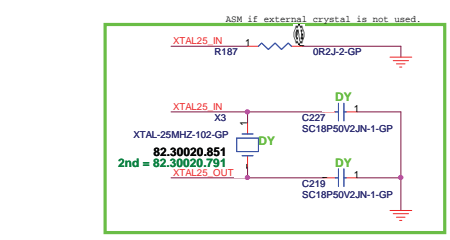
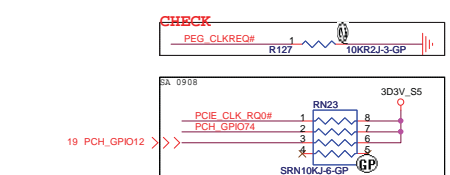
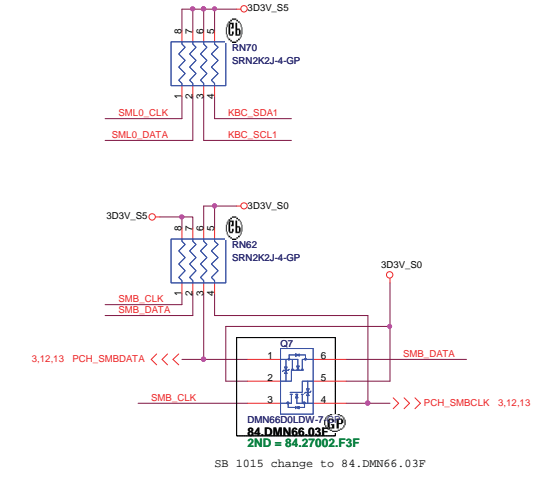
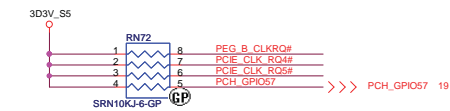
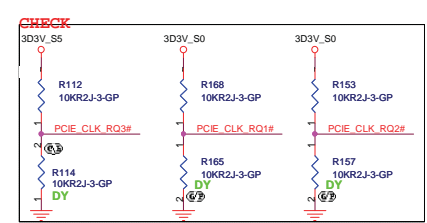
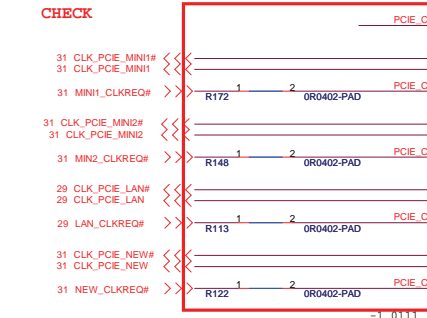
SPI_CS#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

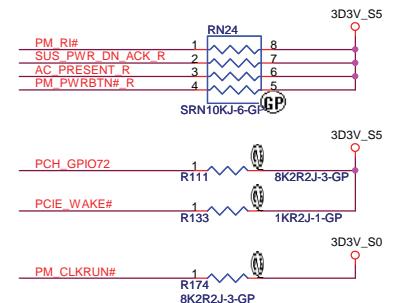
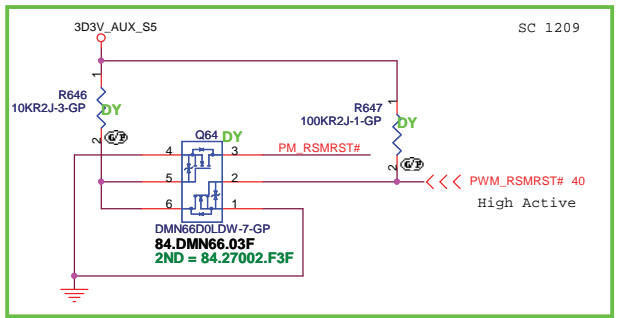
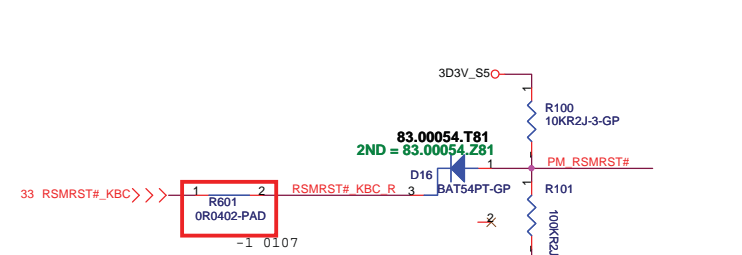
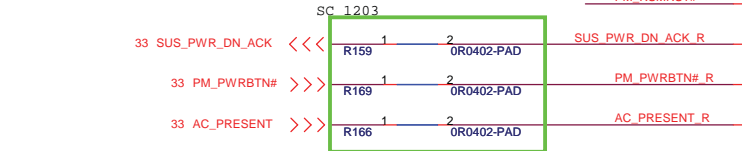
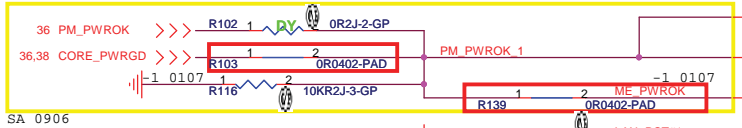




PCIECLKRQ(0,3,4,5,6,7)# should have a 10K pull-up to +3VALW.

PCIECLKRQ(1,2) should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).





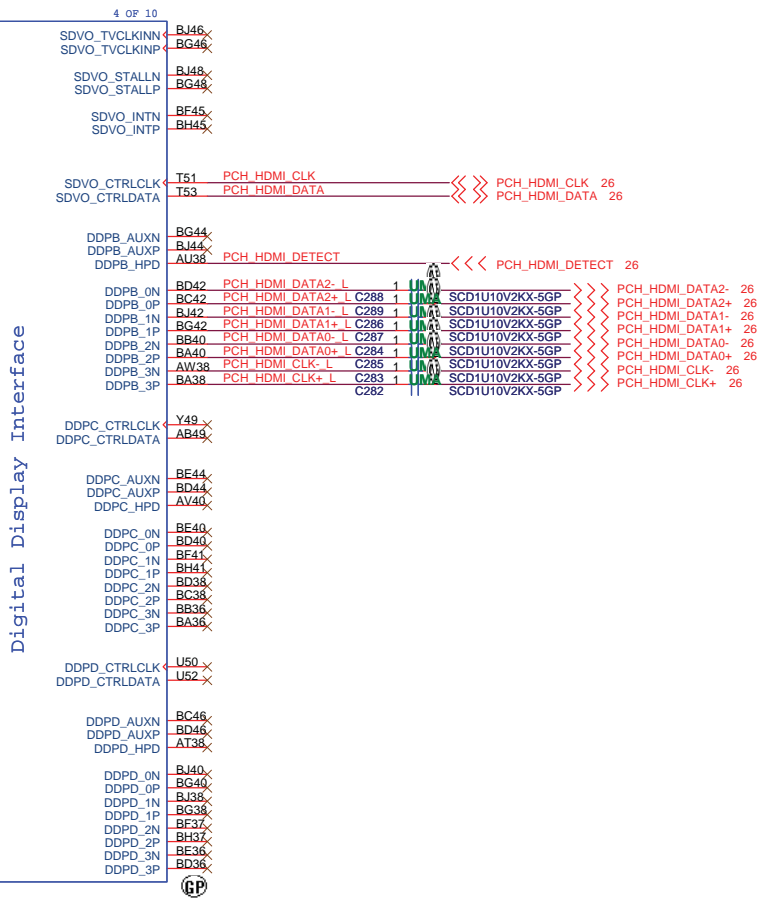
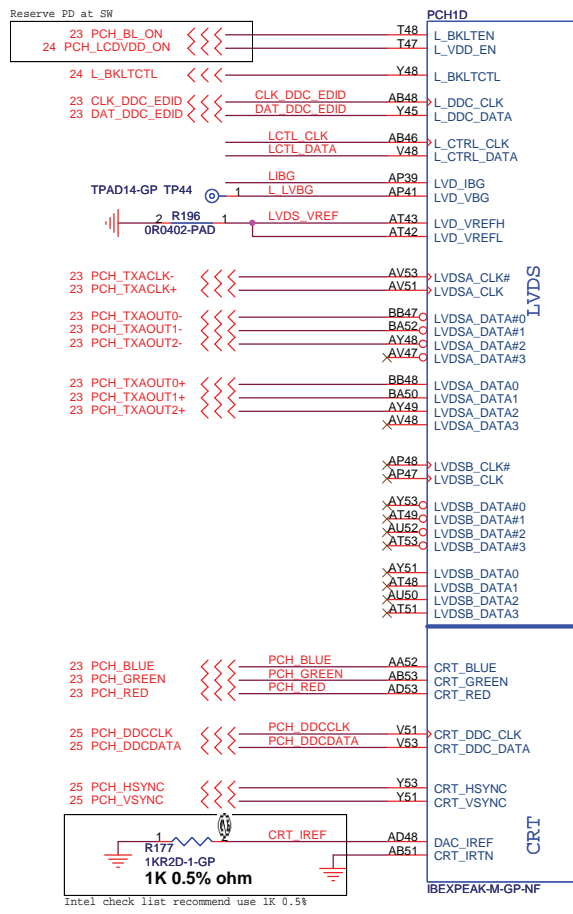
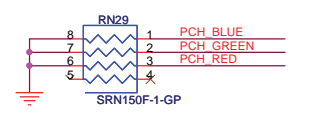
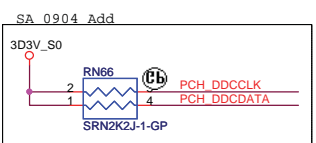
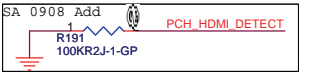
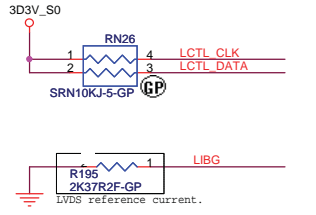
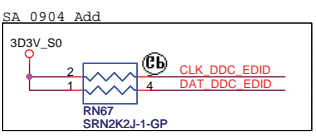
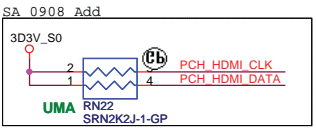
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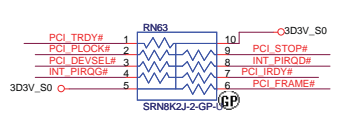
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Title: **16 PCH (3/9)-DMI / FDI / PM**

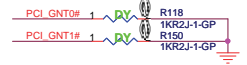
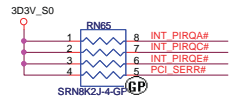
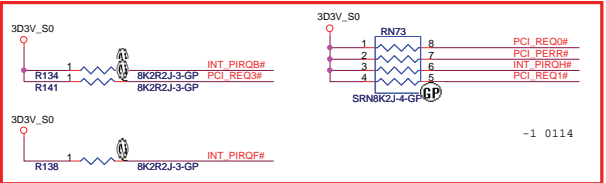
Size: Custom Document Number: **LA46 MB DIS**

Date: Tuesday, January 26, 2010 Sheet 16 of 58

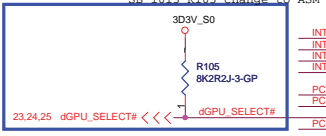




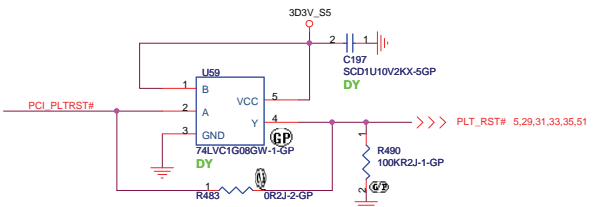
These pins are left as NC, because the function is disabled.



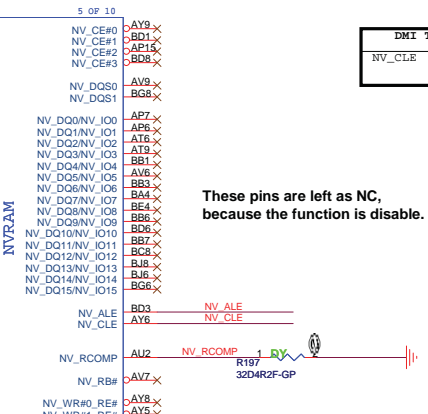
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



24 dGPU_PWM_SELECT# <<<< dGPU_PWM_SELECT#



- >H40 AD0
- >N34 AD1
- >C44 AD2
- >A38 AD3
- >C38 AD4
- >J34 AD5
- >A40 AD6
- >M45 AD7
- >E36 AD8
- >H48 AD9
- >E40 AD10
- >C40 AD11
- >M48 AD12
- >M45 AD13
- >E53 AD14
- >M40 AD15
- >M43 AD16
- >AD17
- >E40 AD18
- >AD19
- >C42 AD20
- >M48 AD21
- >J52 AD22
- >M51 AD23
- >E48 AD24
- >L34 AD25
- >E42 AD26
- >J40 AD27
- >E44 AD28
- >M47 AD29
- >M47 AD30
- >H36 AD31
- >J50 C/BE0#
- >G42C C/BE1#
- >H47C C/BE2#
- >G34C C/BE3#
- >C38C PIRQA#
- >H51C PIRQB#
- >B37C PIRQC#
- >A44C PIRQD#
- >E51C REQ0#
- >A46C REQ1#/GPIO50
- >B45C REQ2#/GPIO52
- >M53C REQ3#/GPIO54
- >F48C GNT0#
- >K45C GNT1#
- >E36C GNT2#/GPIO53
- >H53C GNT3#/GPIO55
- >B41C INT_PIRQA#
- >K53C INT_PIRQB#
- >A36C INT_PIRQC#
- >A48C INT_PIRQD#
- >K6C PCI_RST#
- >E44C SERR#
- >E50C PERR#
- >A42C IRDY#
- >H44 PAR
- >F46C DEVSEL#
- >C46C FRAME#
- >D49C PLOCK#
- >D41C STOP#
- >C48C TRDY#
- >M7C PME#
- >D5C PLTRST#
- >N52 CLKOUT_P0
- >P53 CLKOUT_P1
- >P46 CLKOUT_P2
- >P51 CLKOUT_P3
- >P48 CLKOUT_P4

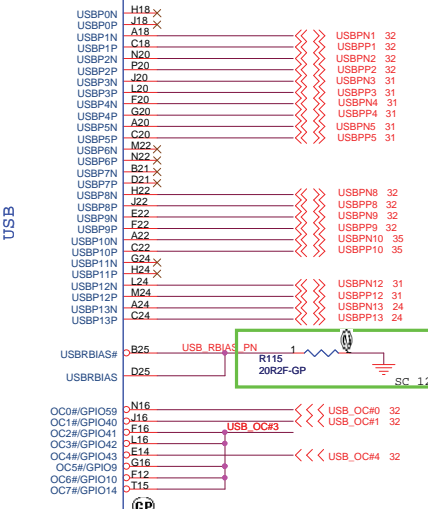


These pins are left as NC, because the function is disabled.

DMI Termination Voltage	
NV_CLE	Set to V _{as} when low. Set to V _{ec} when high.

Danbury Technology:
Disabled when Low.
Enable when High.

Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera



Change to 20ohm for fine tune USB signal

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

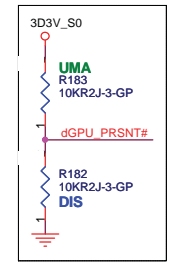
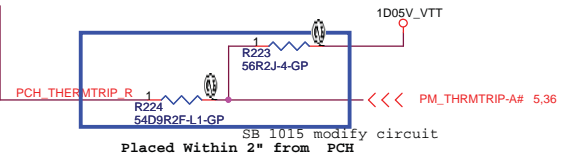
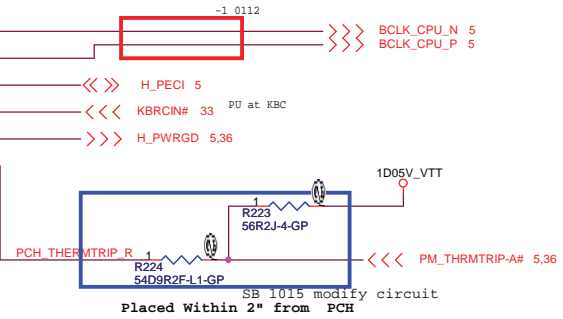
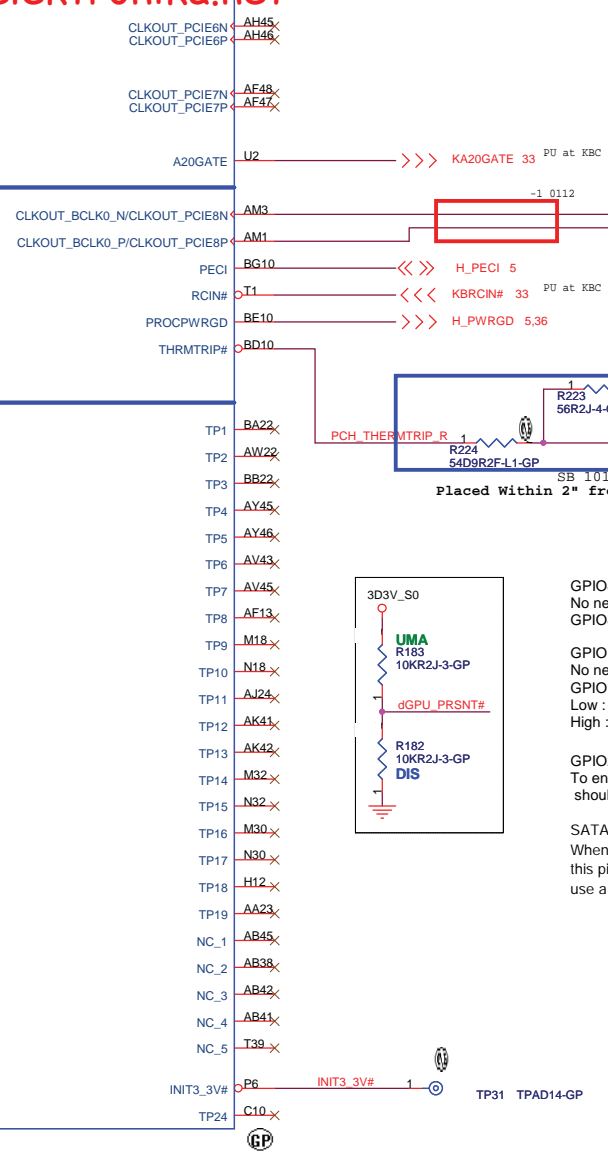
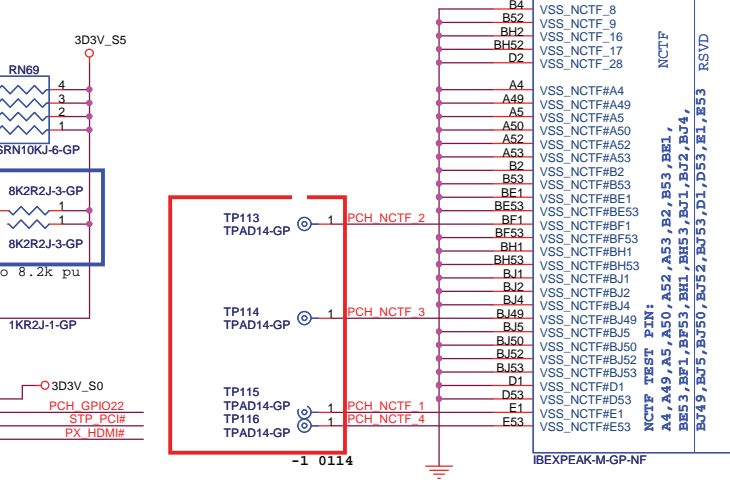
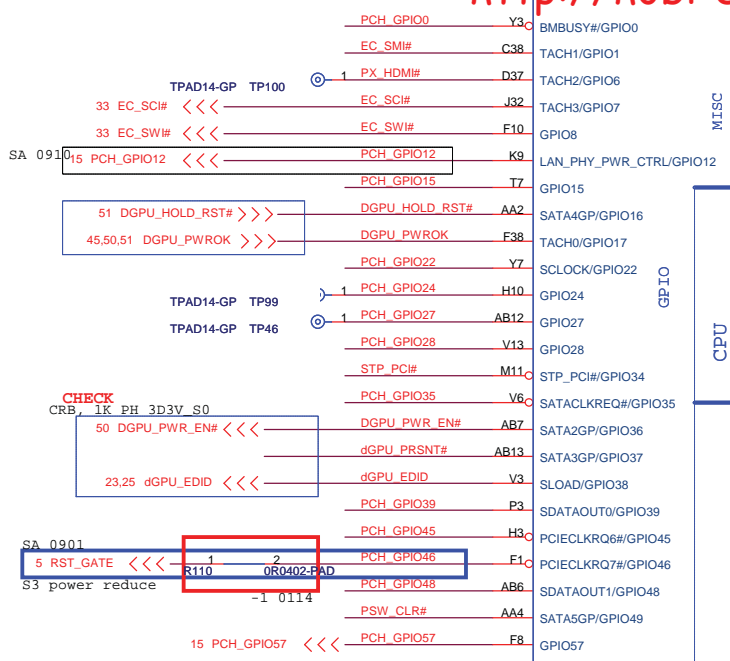
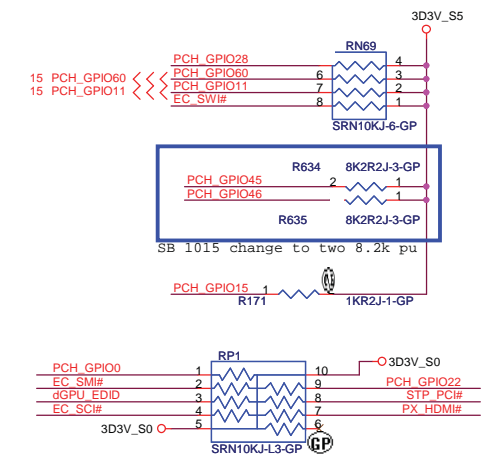
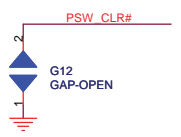
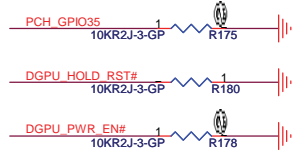
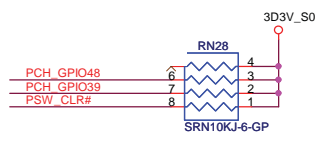
OC#0	Port 0 & 1	
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	EHCI 1
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	EHCI 2
OC#7	Floater OC# (not used)	

<Core Design>

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Title: **18 PCH (5/9)-PCI / USB**

Size: Document Number
Customer: **LA46 MB DIS**
Date: Tuesday, January 26, 2010 Sheet 18 of 58 Rev -1



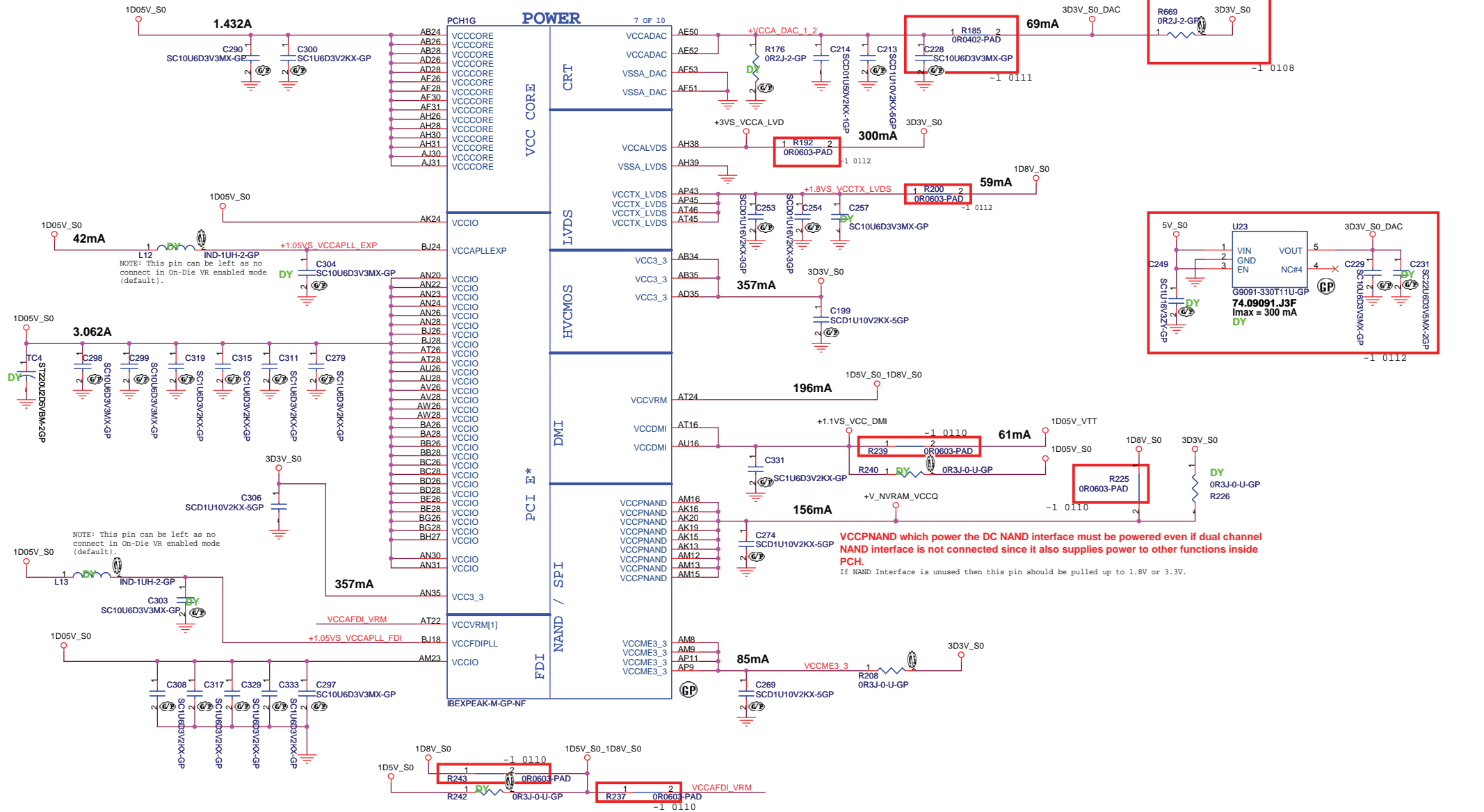
GPIO8 has a weak[20K] internal pull up. No need to have external pull down/up. GPIO8 pin set to high at reset.

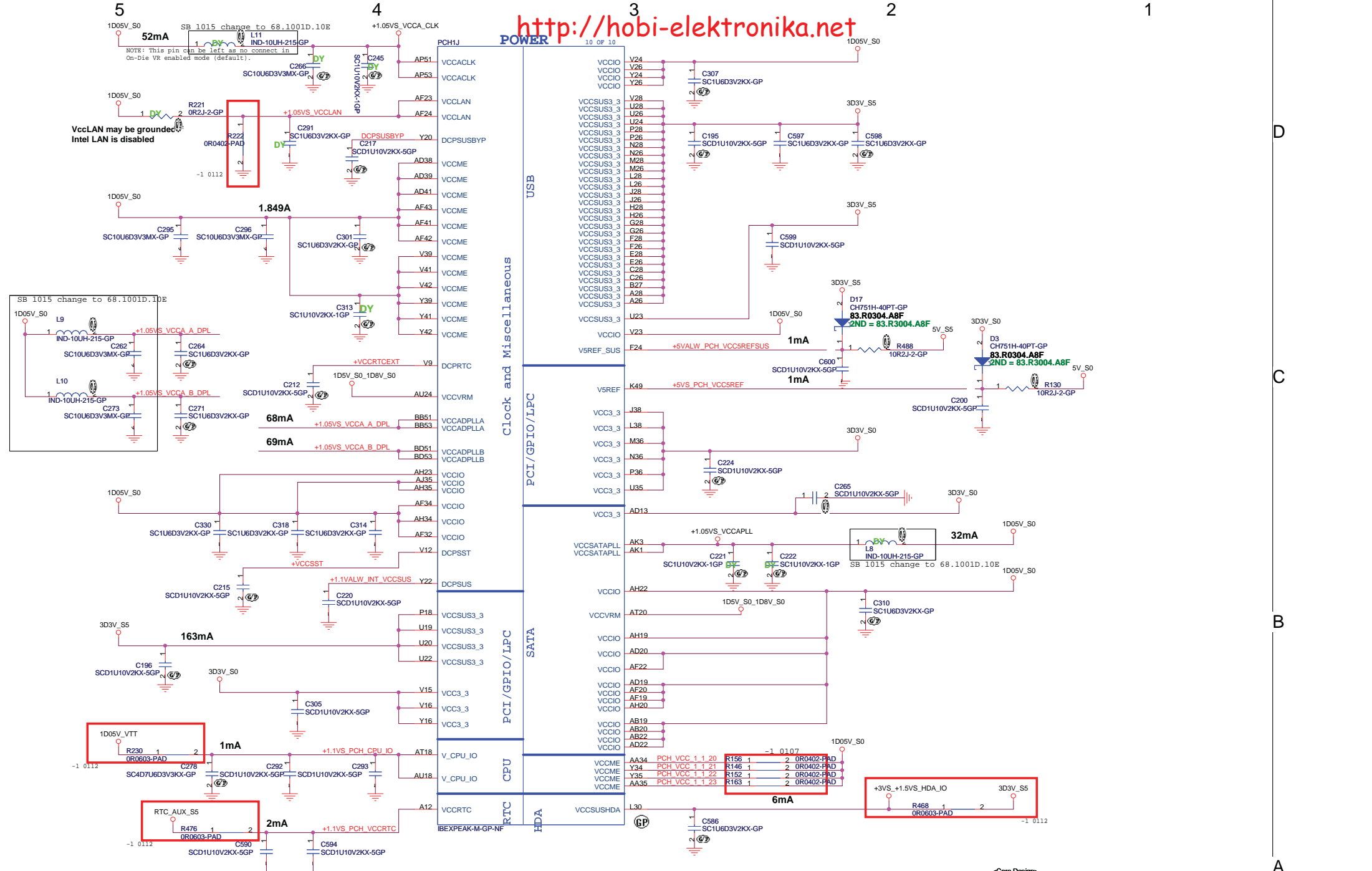
GPIO15 has a weak[20K] internal pull down. No need to have external pull up/down. GPIO 15 pin is set to low at reset. Low : ME Crypto TLS with no confidentiality High : ME Crypto TLS with confidentiality

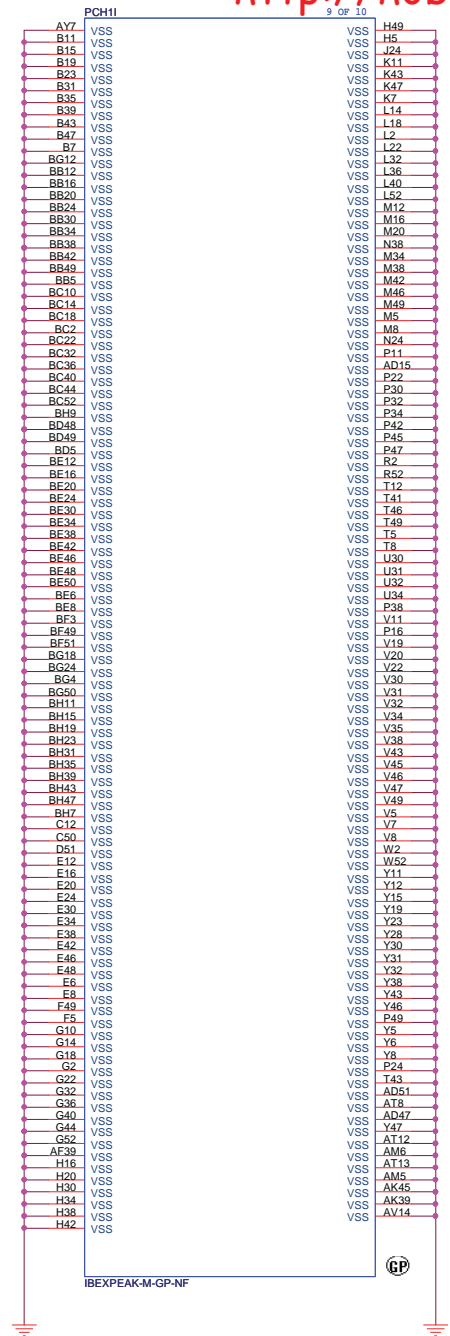
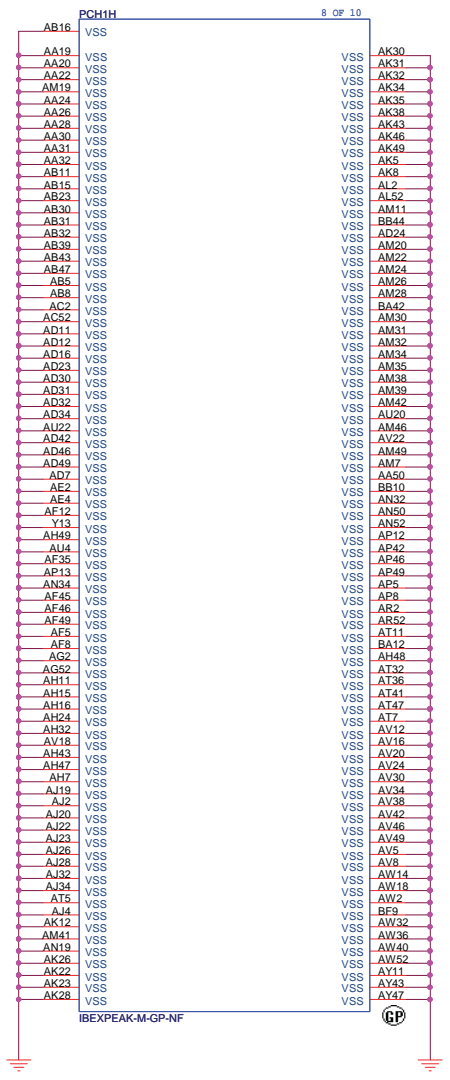
GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regulator, should not place external pull down.

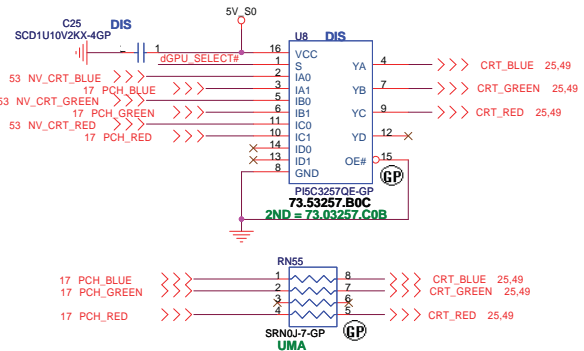
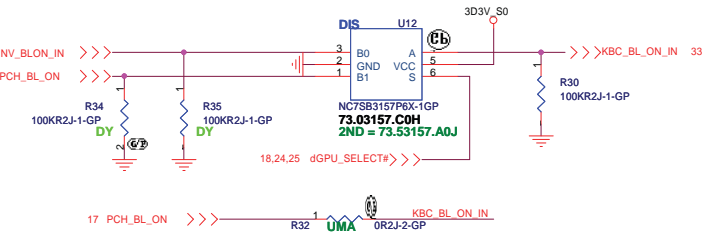
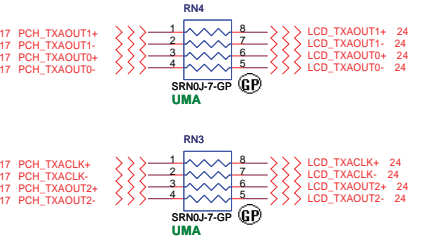
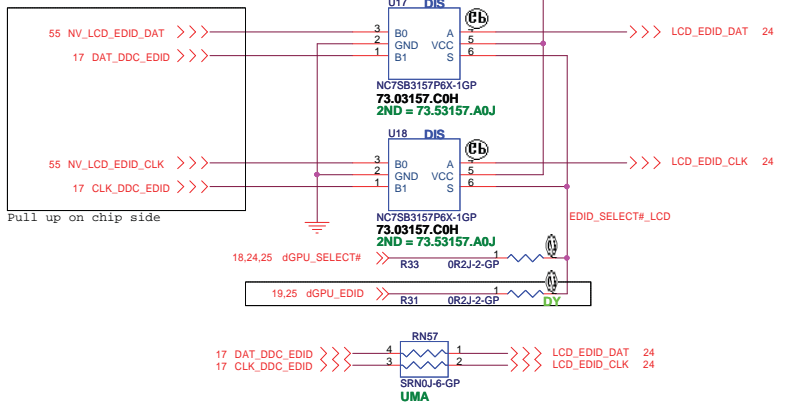
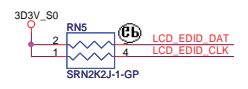
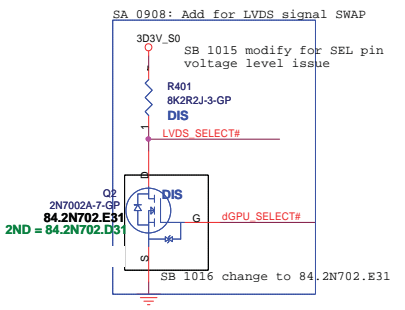
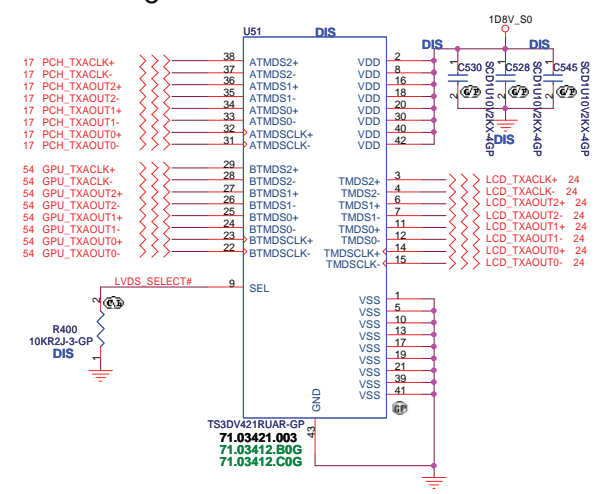
SATACLKREQ#: When used as SATACLKREQ#, this pin is open drain and should use a pull-up resistor.

<Core Design>









FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

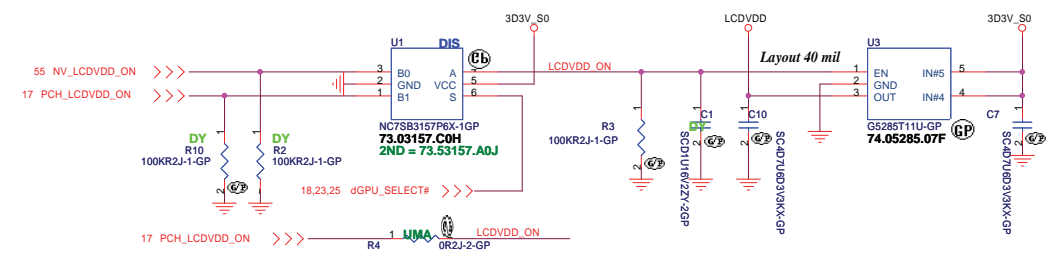
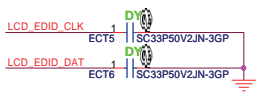
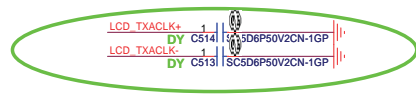
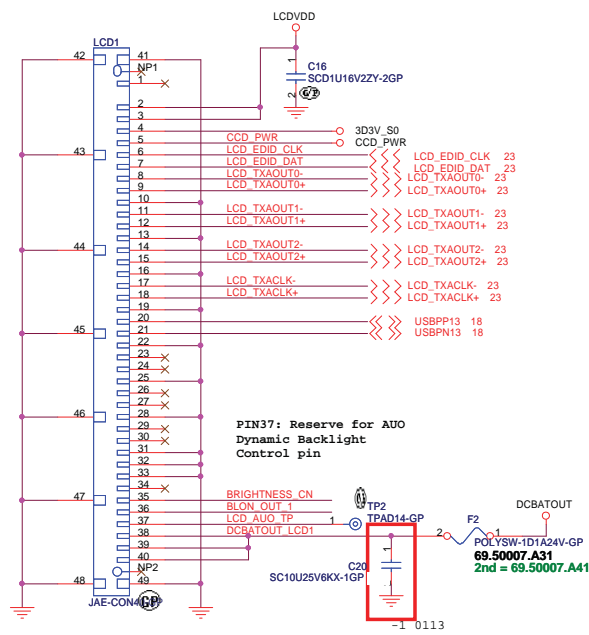
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

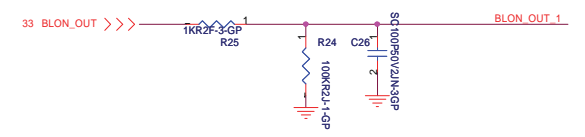
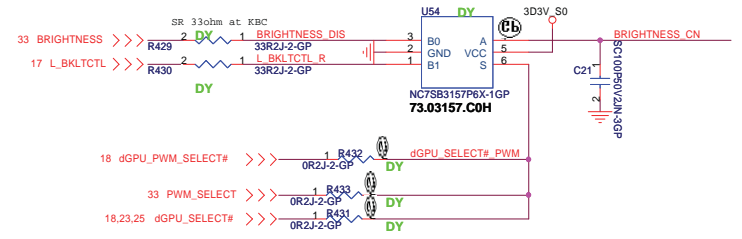
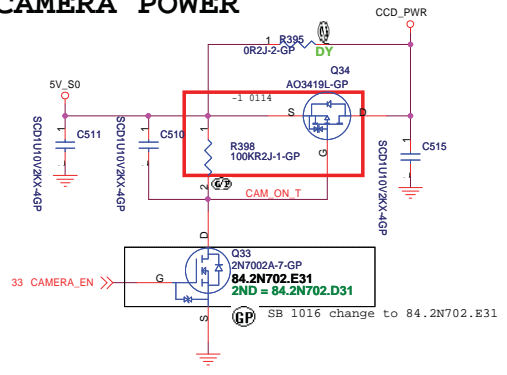
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 Taipei Hsein 221, Taiwan, R.O.C

Title: **23 Display MUX**
 Size: **LA46 MB DIS**
 Date: Tuesday, January 26, 2010 Sheet 23 of 58

LCD/INVERTER/CCD CONN



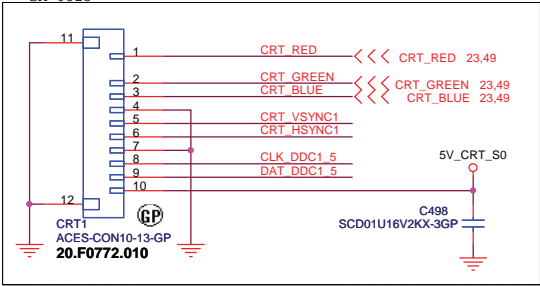
CAMERA POWER



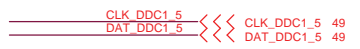
<Core Design>

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		21F,88,Sec.1,Hsin Tai Wu Rd.,Hschih, Taipei Hsein 221, Taiwan, R.O.C	
Title			
24 LCD & CCD			
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
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SA-0820 Move pi filter to CRT board.
SA-0823

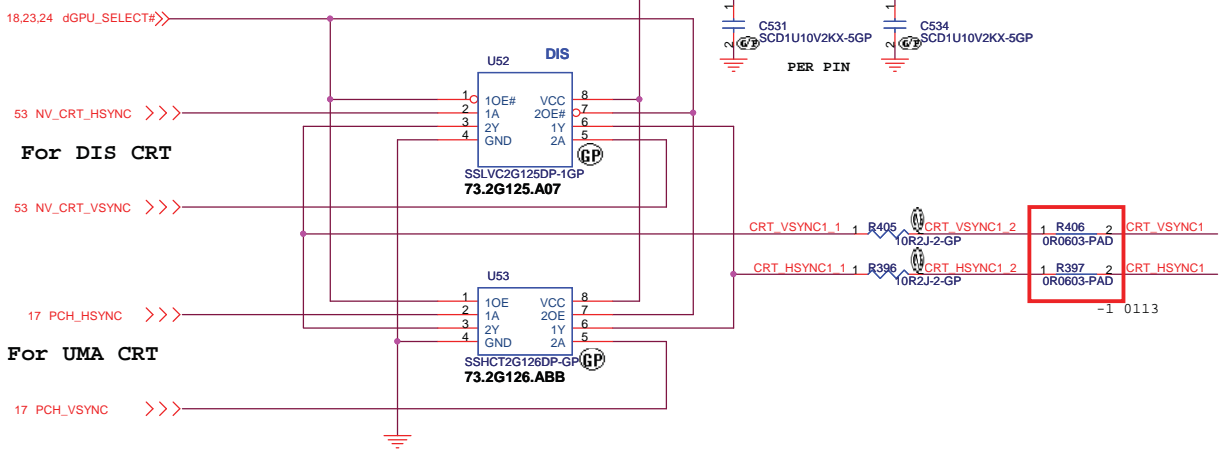


SB 1024 Add pin to GND (EMI)

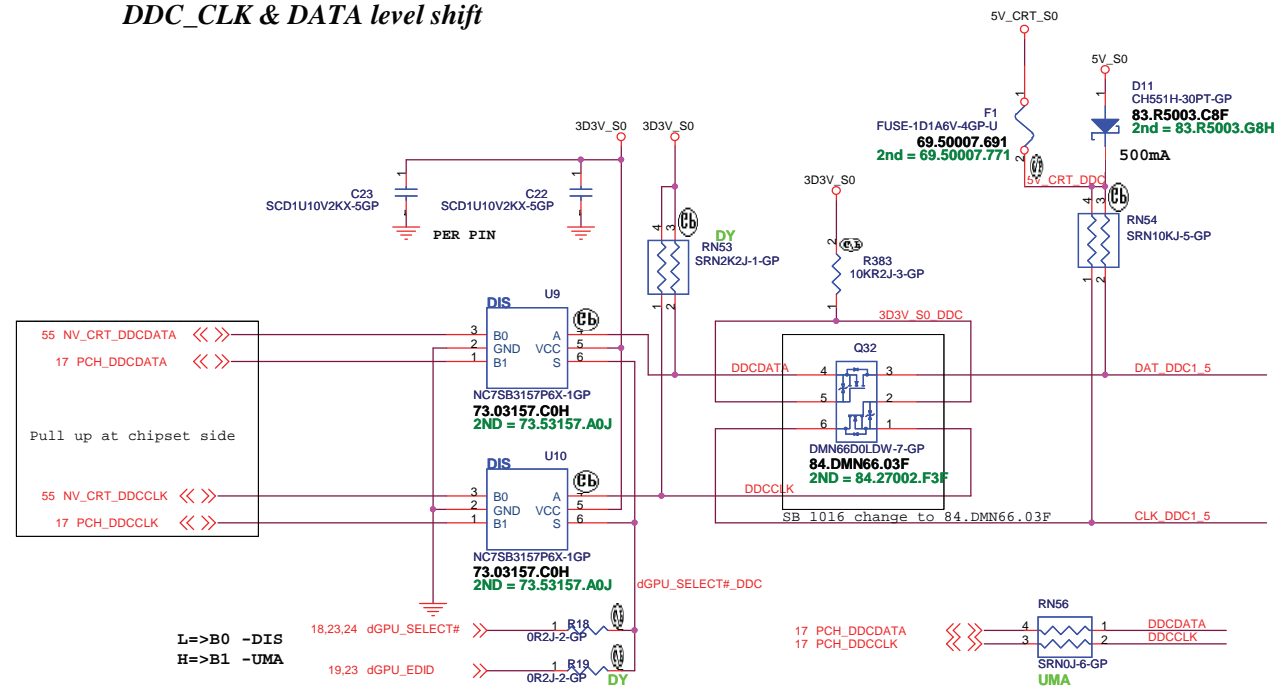


L=>B0 -DIS
H=>B1 -UMA

Hsync & Vsync level shift



DDC_CLK & DATA level shift

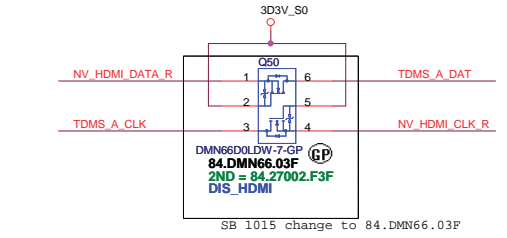
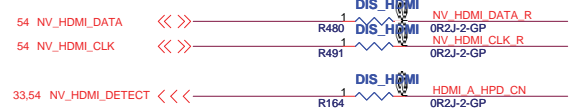
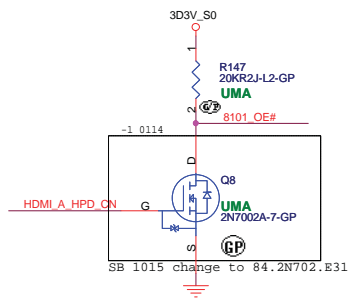
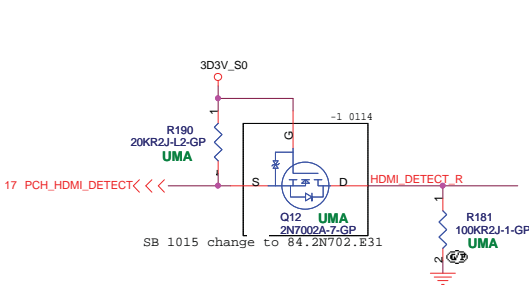
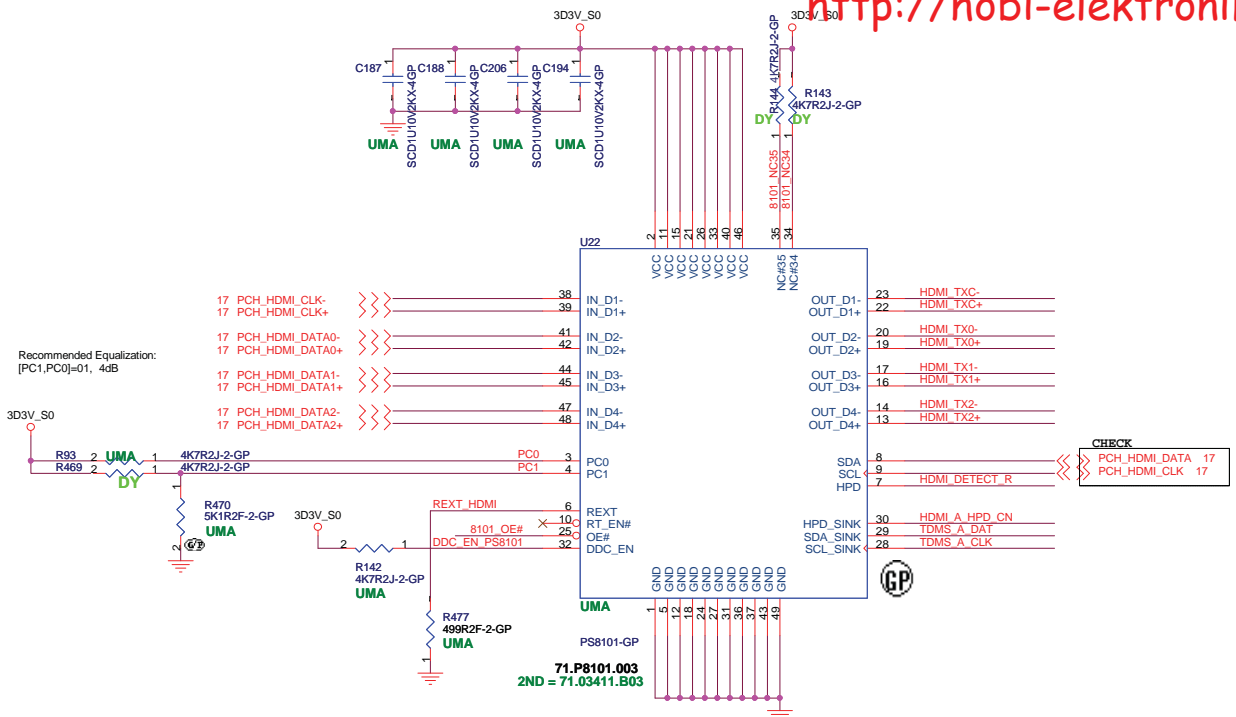
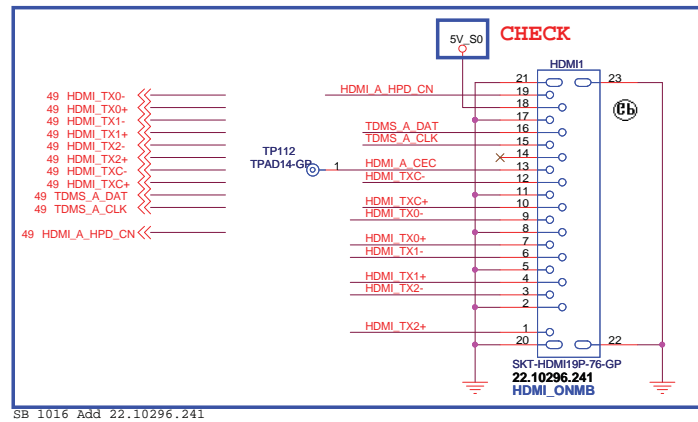
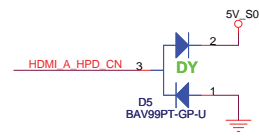
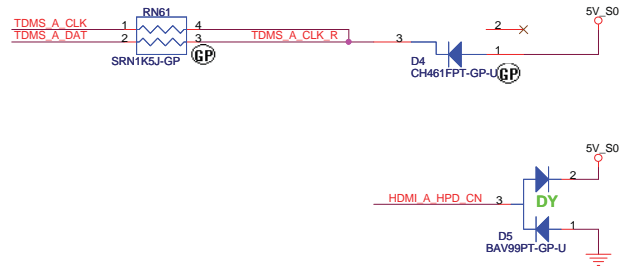
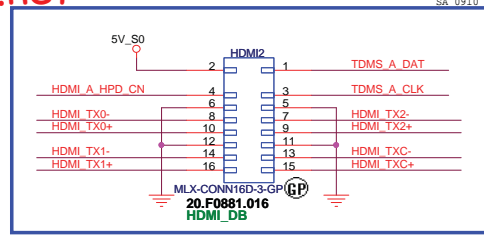


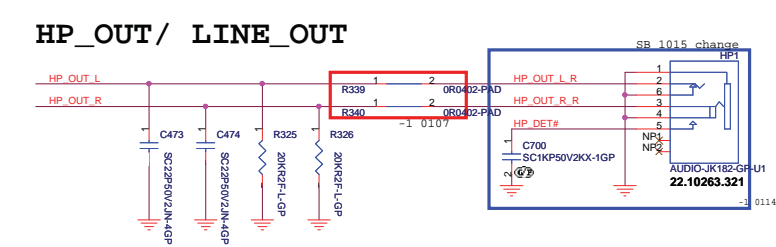
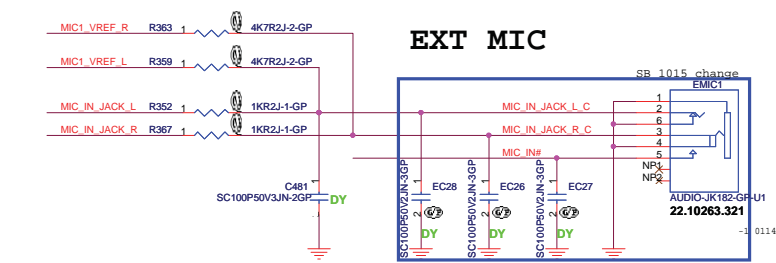
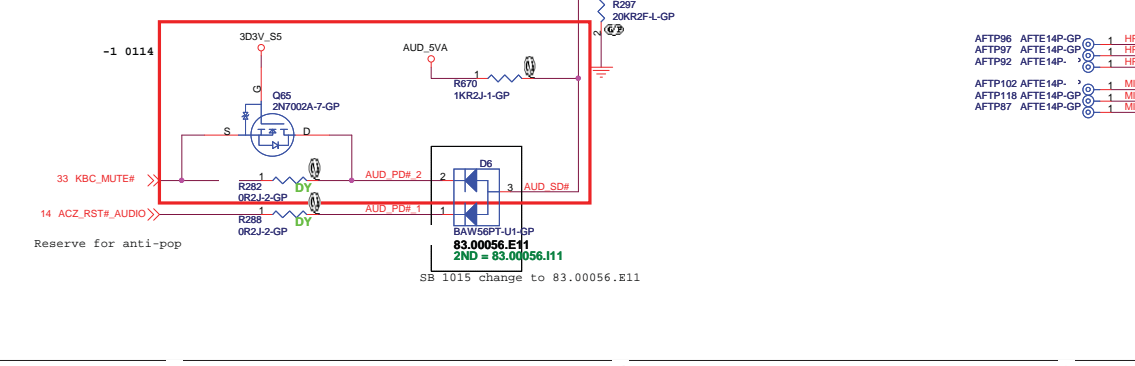
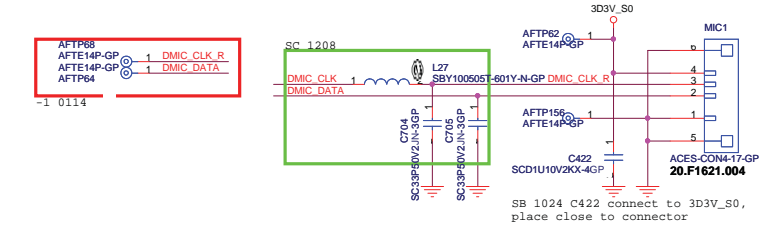
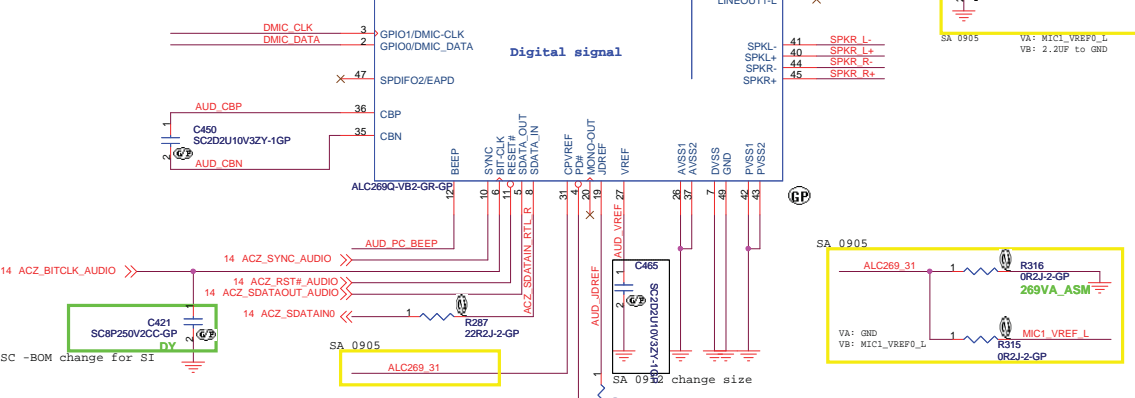
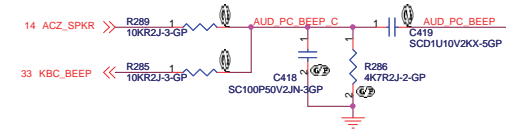
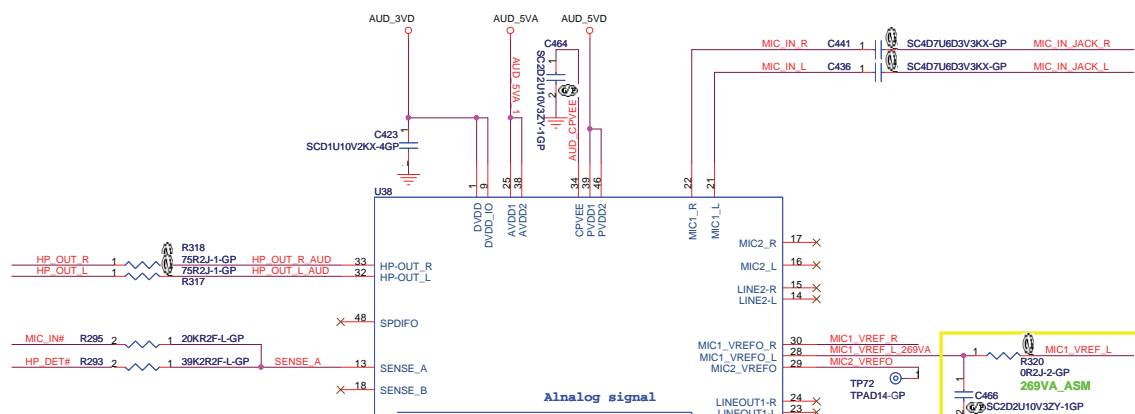
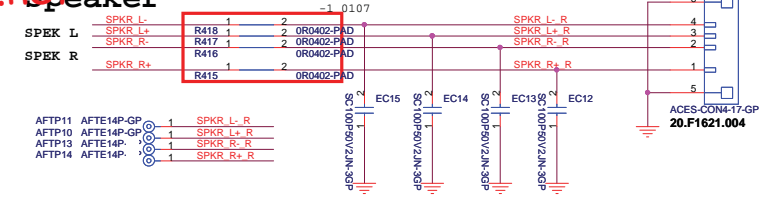
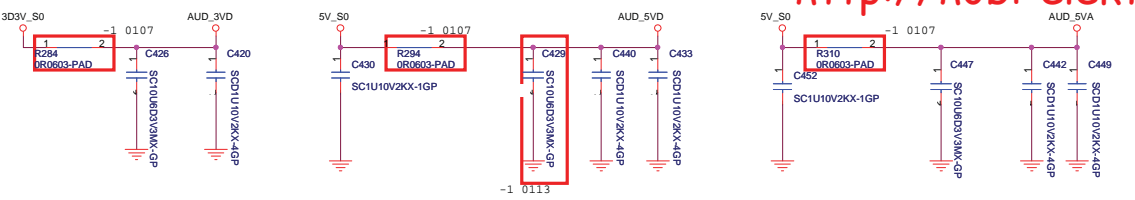
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H=>B1 -UMA

<Core Design>

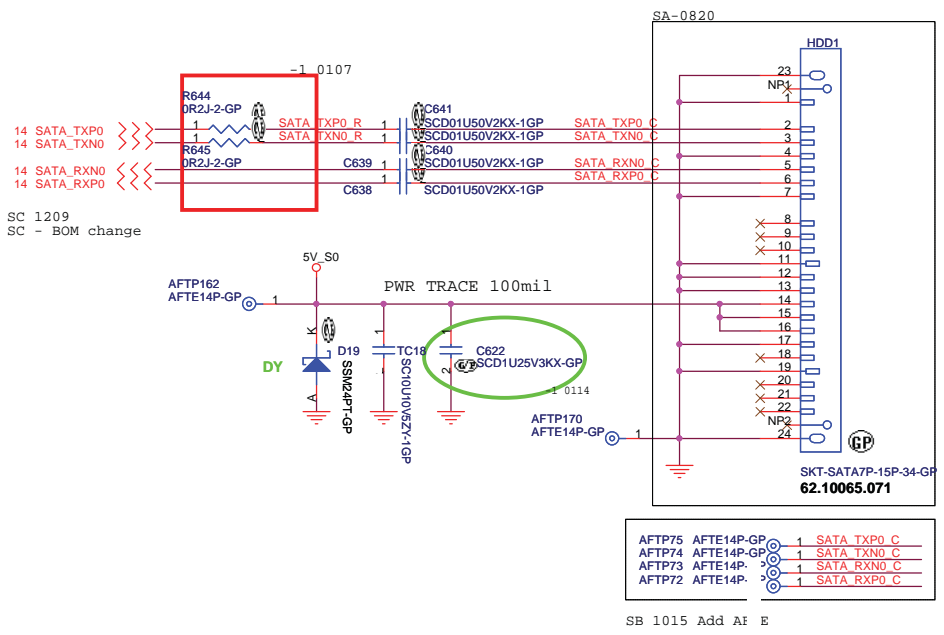
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	25 CRT	
Size	Document Number	Rev
A3	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 25 of 58

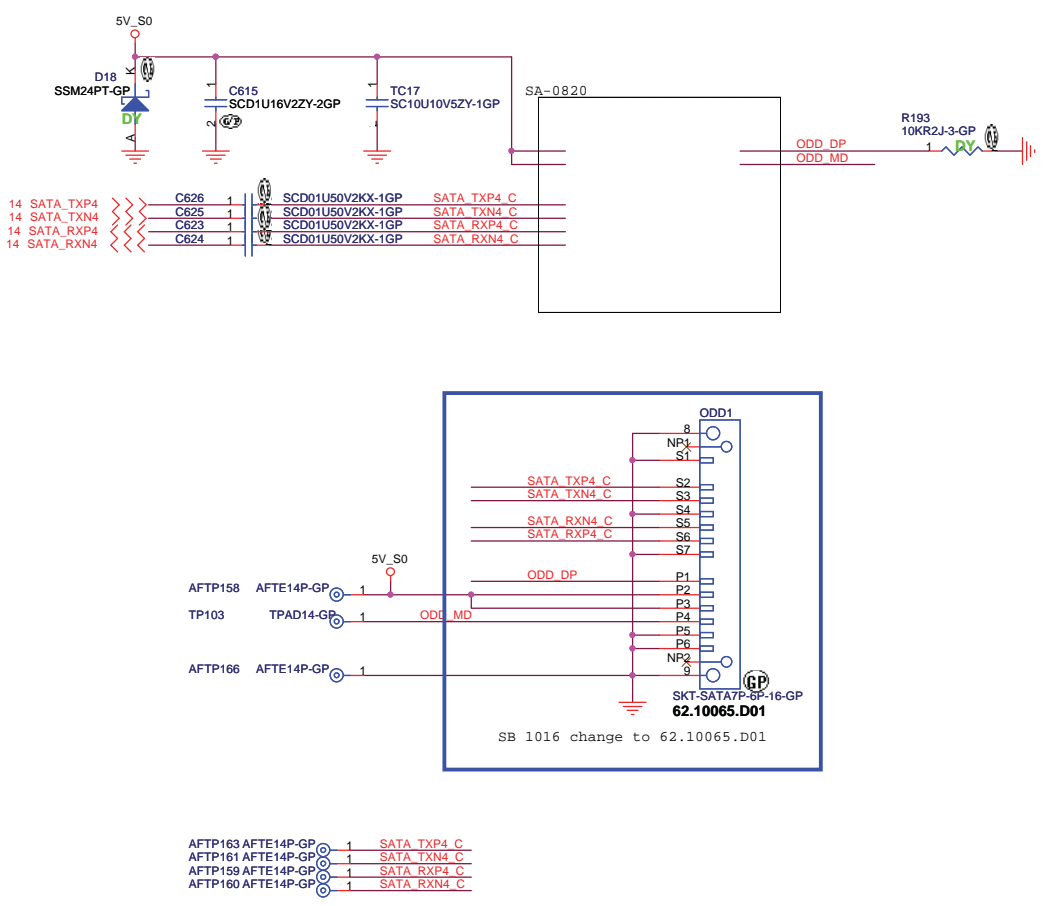


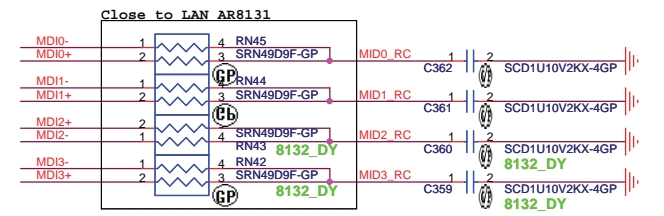
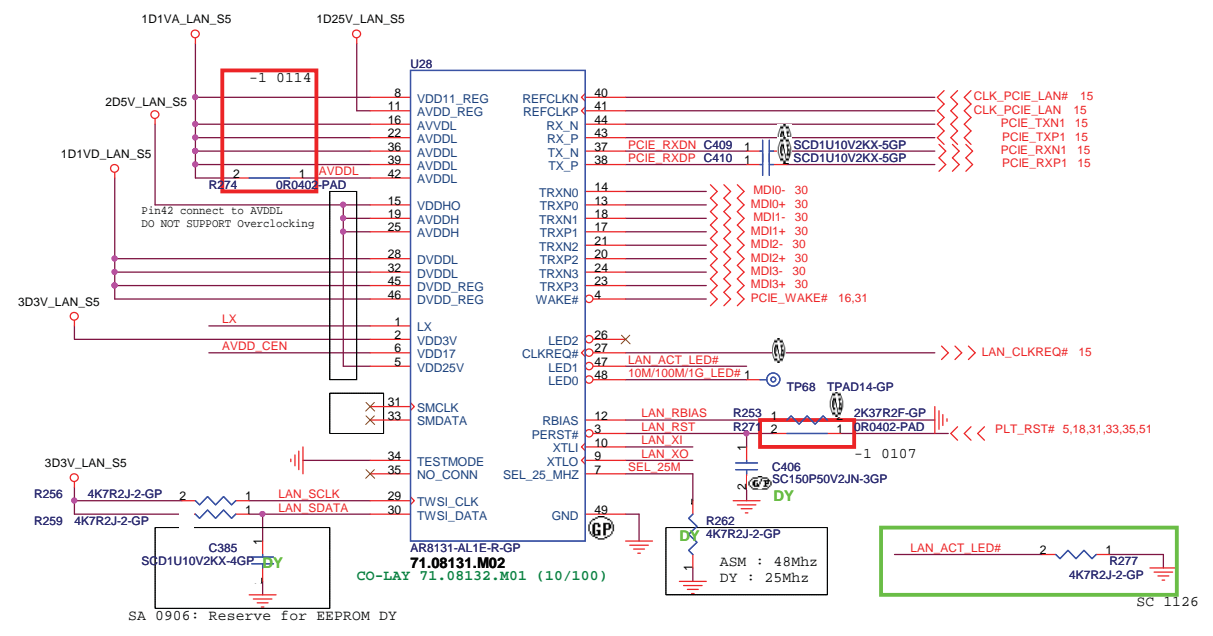
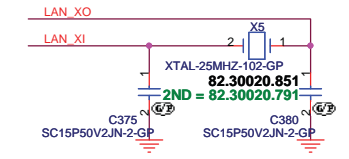
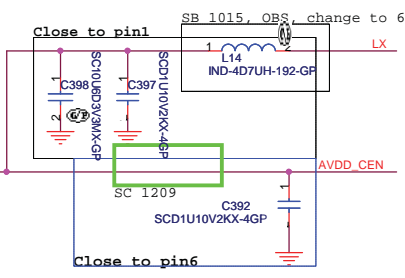
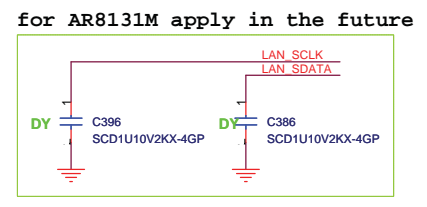
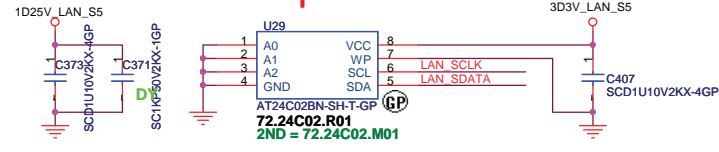
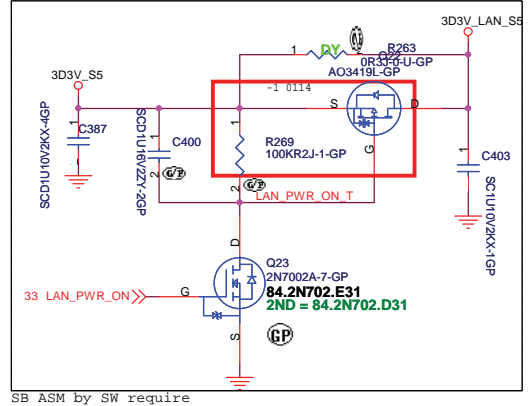
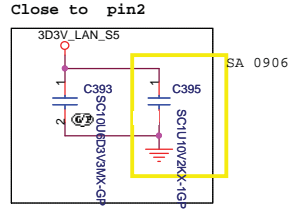
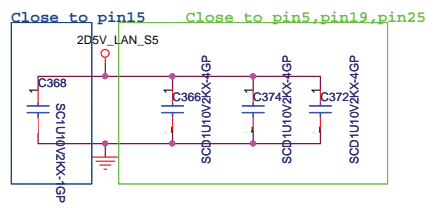
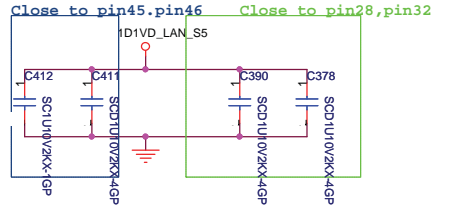
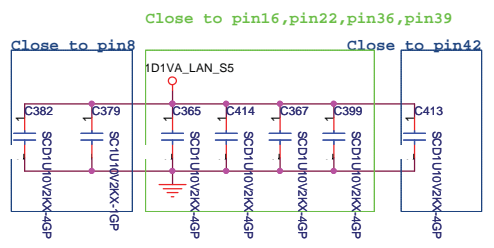


SATA Connector

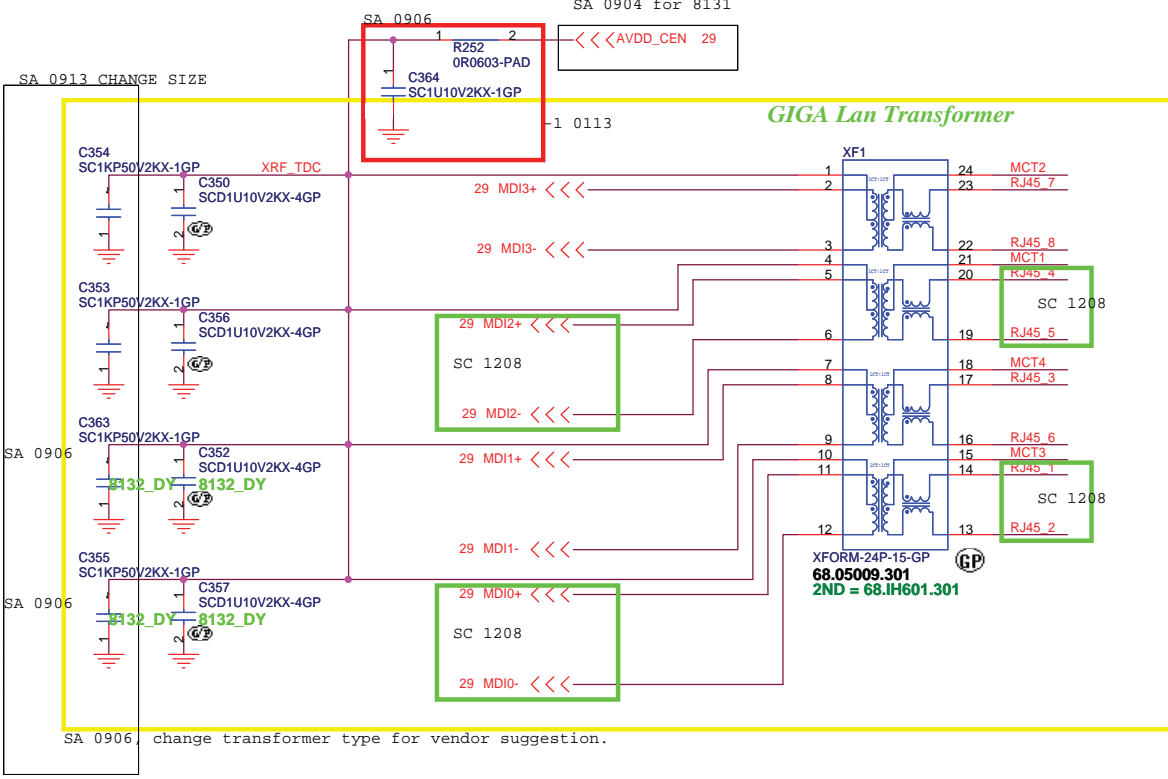


ODD Connector

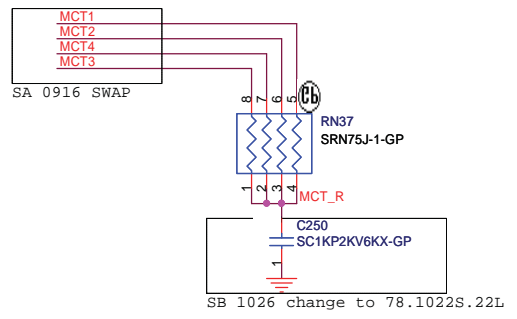
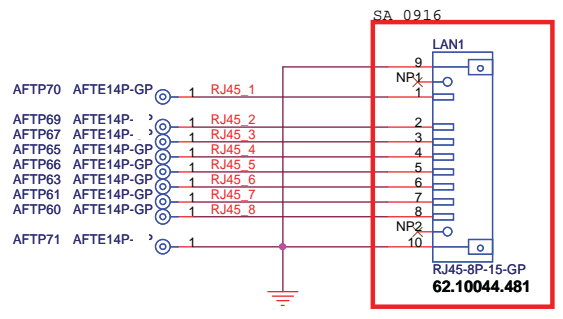




- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



LAN Connector



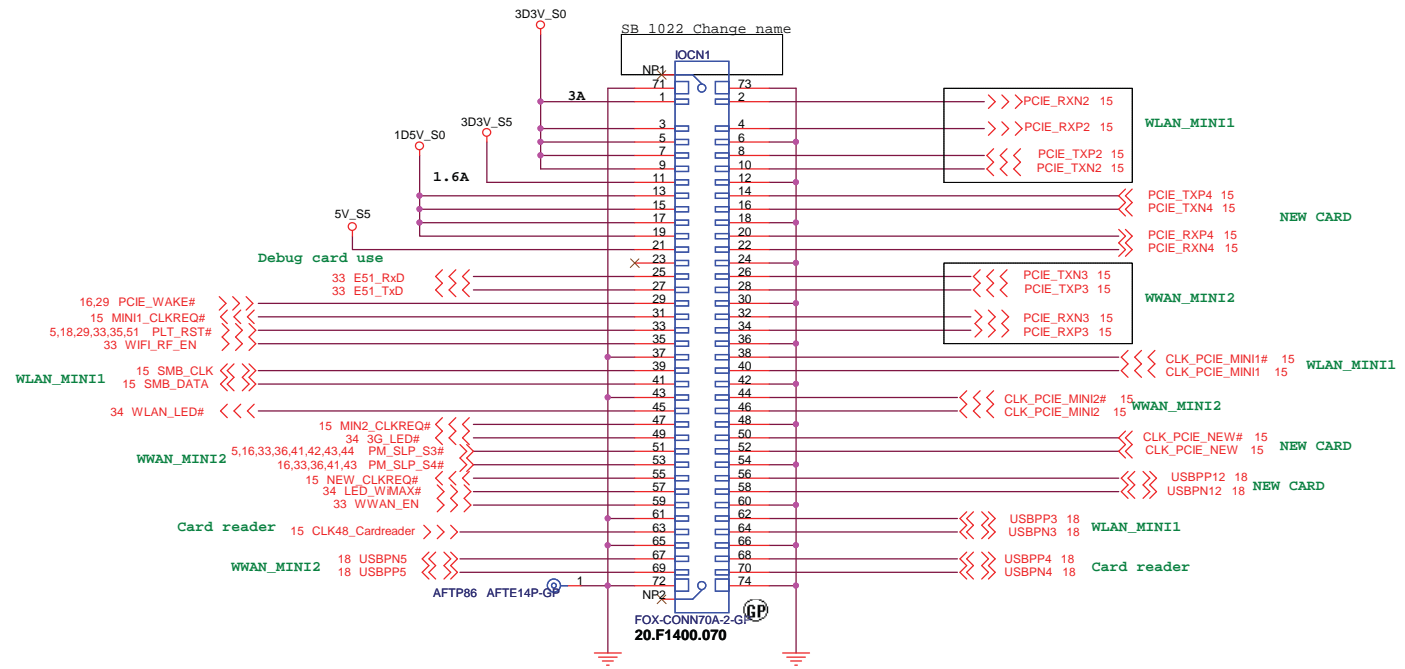
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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: **30 LAN CONN**

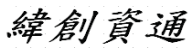
Size: Custom Document Number: **LA46 MB DIS** Rev: -1

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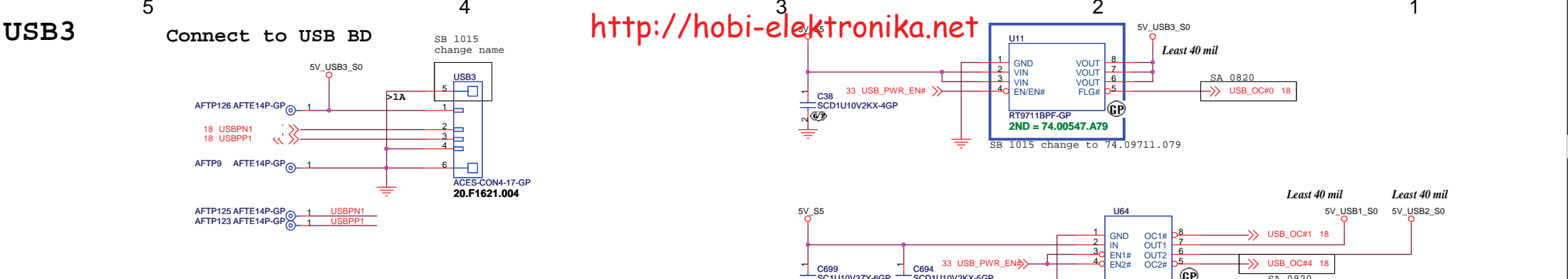


- | | | |
|--------------------|---|---------|
| AFTP107 AFTE14P-GP | 1 | 3D3V_S0 |
| AFTP103 AFTE14P | 1 | 3D3V_S5 |
| AFTP104 AFTE14P-GP | 1 | 1D5V_S0 |
| AFTP99 AFTE14P | 1 | 5V_S5 |
-
- | | | |
|--------------------|---|-----------------|
| AFTP98 AFTE14P-GP | 1 | E51_RxD |
| AFTP93 AFTE14P-GP | 1 | E51_TxD |
| AFTP91 AFTE14P | 1 | PCI_E_WAKE# |
| AFTP84 AFTE14P | 1 | MINI1_CLKREQ# |
| AFTP180 AFTE14P-GP | 1 | CLK_PCIE_MINI1# |
| AFTP188 AFTE14P | 1 | CLK_PCIE_MINI1 |
| AFTP109 AFTE14P | 1 | PCI_E_RXN2 |
| AFTP108 AFTE14P | 1 | PCI_E_RXP2 |
| AFTP105 AFTE14P | 1 | PCI_E_TXN2 |
| AFTP106 AFTE14P-GP | 1 | PCI_E_TXP2 |
| AFTP185 AFTE14P | 1 | PLT_RST# |
| AFTP184 AFTE14P | 1 | WIFI_RF_EN |
| AFTP182 AFTE14P-GP | 1 | SMB_CLK |
| AFTP181 AFTE14P | 1 | SMB_DATA |
| AFTP180 AFTE14P | 1 | WLAN_LED# |
| AFTP178 AFTE14P | 1 | MIN2_CLKREQ# |
| AFTP187 AFTE14P | 1 | USBPN3 |
| AFTP189 AFTE14P-GP | 1 | USBPP3 |
| AFTP177 AFTE14P | 1 | CLK_PCIE_MINI2# |
| AFTP179 AFTE14P | 1 | CLK_PCIE_MINI2 |
-
- | | | |
|--------------------|---|------------------|
| AFTP194 AFTE14P-GP | 1 | USBPP4 |
| AFTP193 AFTE14P-GP | 1 | USBPN4 |
| AFTP176 AFTE14P-GP | 1 | CLK48_Cardreader |
| AFTP101 AFTE14P-GP | 1 | PCI_E_TXP4 |
| AFTP100 AFTE14P | 1 | PCI_E_TXN4 |
| AFTP95 AFTE14P | 1 | PCI_E_RXP4 |
| AFTP94 AFTE14P-GP | 1 | PCI_E_RXN4 |
| AFTP174 AFTE14P-GP | 1 | CLK_PCIE_NEW |
| AFTP173 AFTE14P | 1 | CLK_PCIE_NEW# |
| AFTP80 AFTE14P | 1 | USBPP12 |
| AFTP79 AFTE14P | 1 | USBPN12 |
| AFTP81 AFTE14P-GP | 1 | 3G_LED# |
| AFTP78 AFTE14P | 1 | PM_SLP_S3# |
| AFTP82 AFTE14P | 1 | PM_SLP_S4# |
| AFTP93 AFTE14P | 1 | NEW_CLKREQ# |
| AFTP89 AFTE14P | 1 | PCI_E_TXN3 |
| AFTP88 AFTE14P-GP | 1 | PCI_E_TXP3 |
| AFTP90 AFTE14P | 1 | PCI_E_RXN3 |
| AFTP85 AFTE14P | 1 | PCI_E_RXP3 |
| AFTP192 AFTE14P | 1 | USBPN5 |
| AFTP191 AFTE14P | 1 | USBPP5 |
| AFTP77 AFTE14P-GP | 1 | LED_WMAX# |
| AFTP76 AFTE14P | 1 | WWAN_EN |

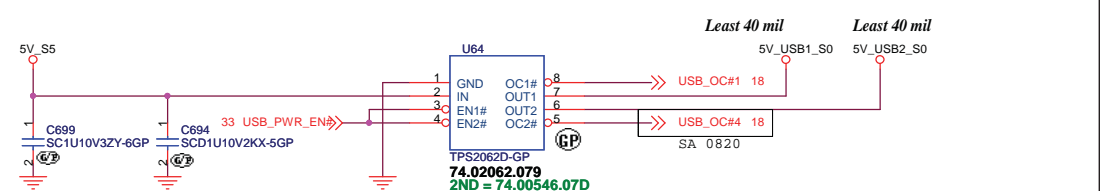
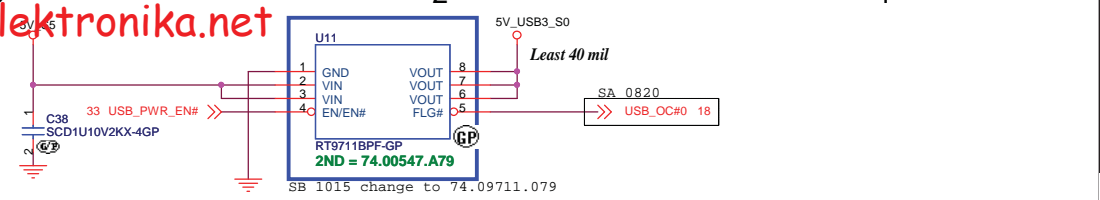
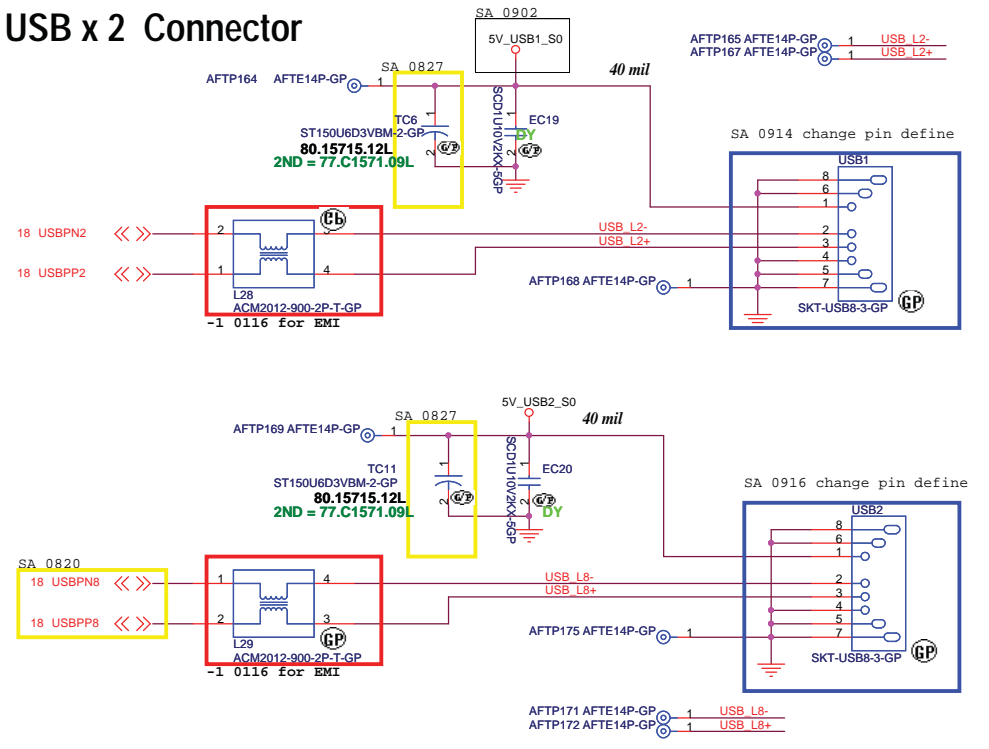
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 Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
31 IO CONN	
Title 31 IO CONN	Document Number LA46 MB DIS
Size A3	Rev -1
Date: Tuesday, January 26, 2010	
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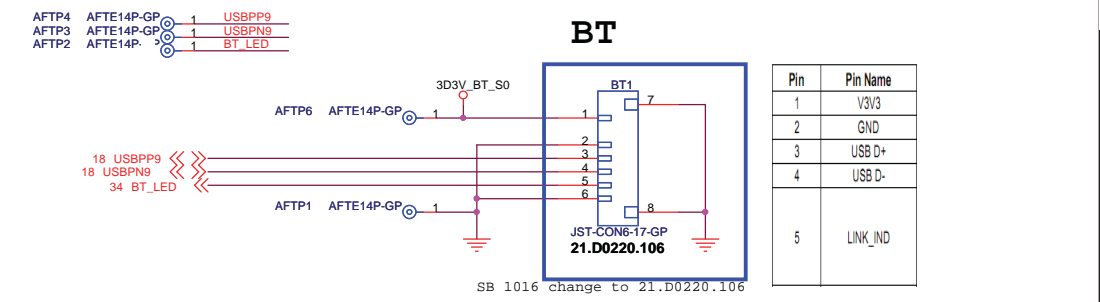
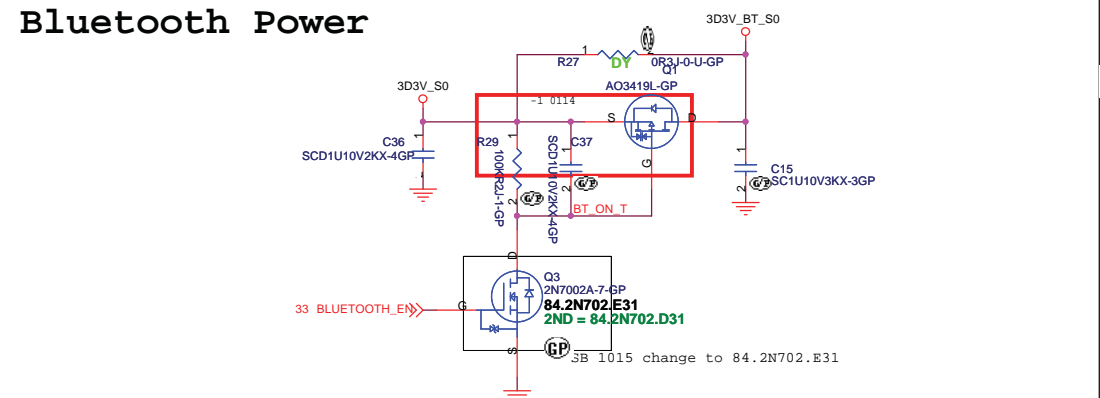
USB3

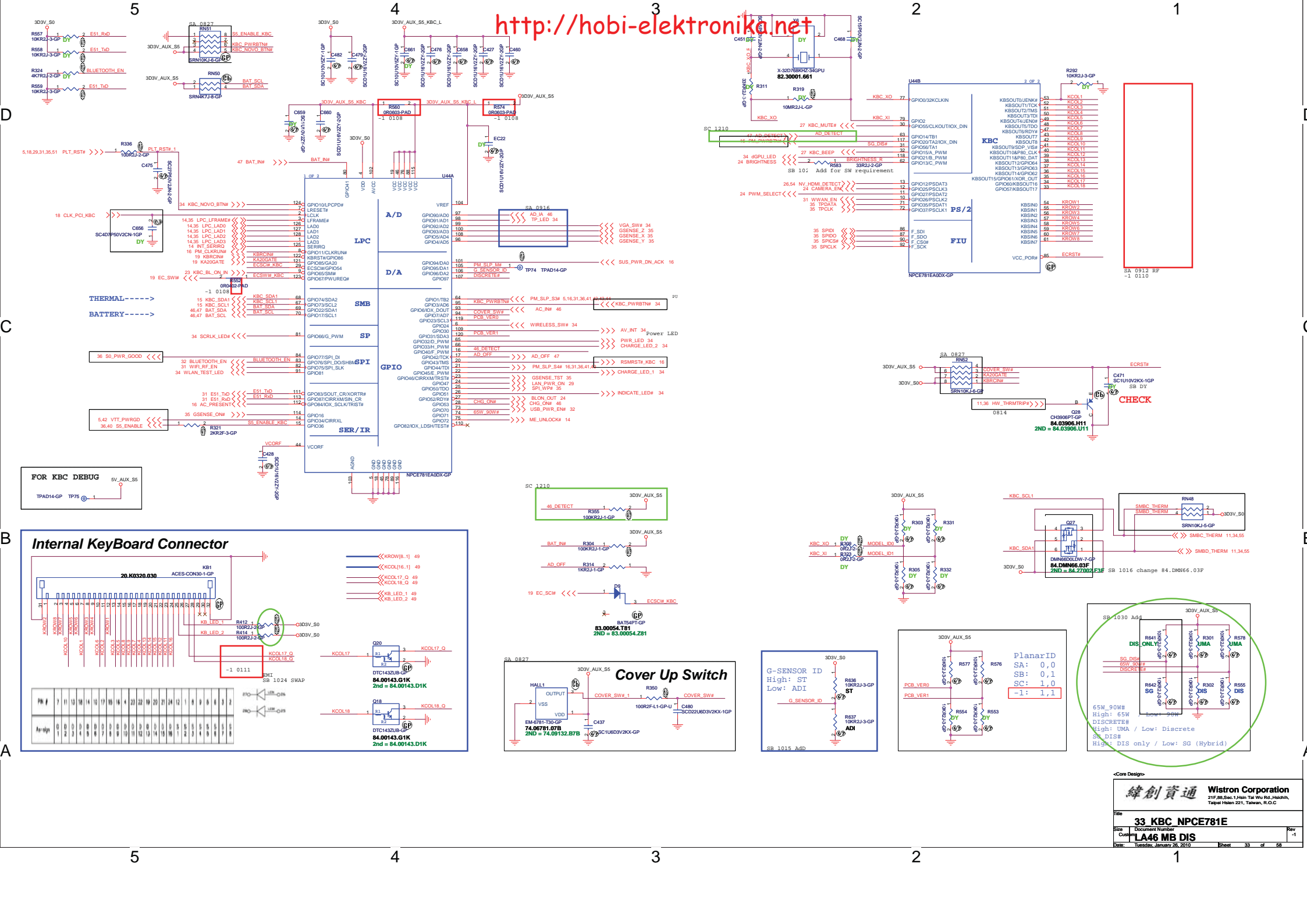


USB x 2 Connector



Bluetooth Power





D

C

B

A

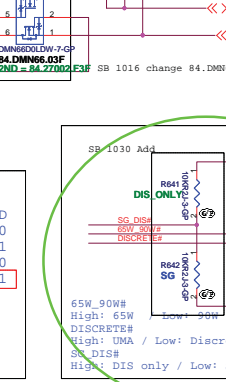
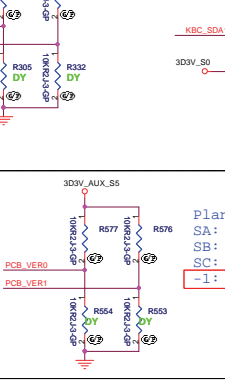
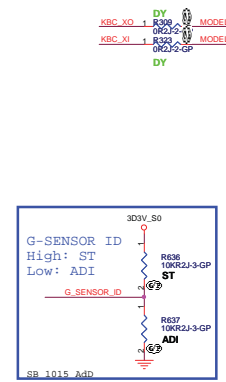
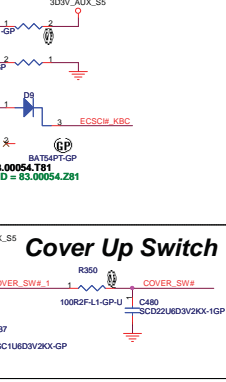
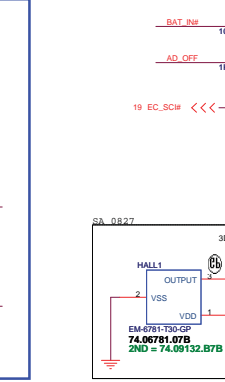
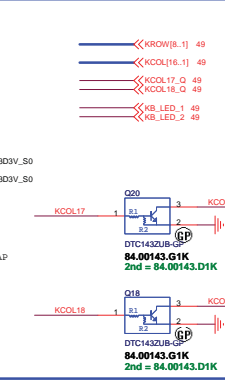
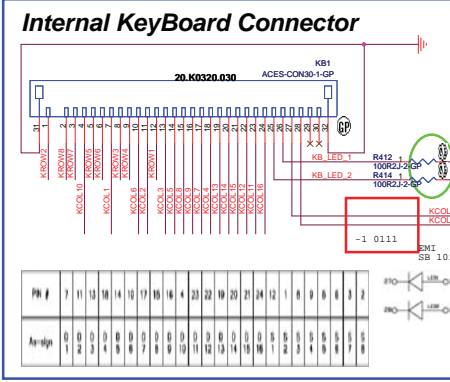
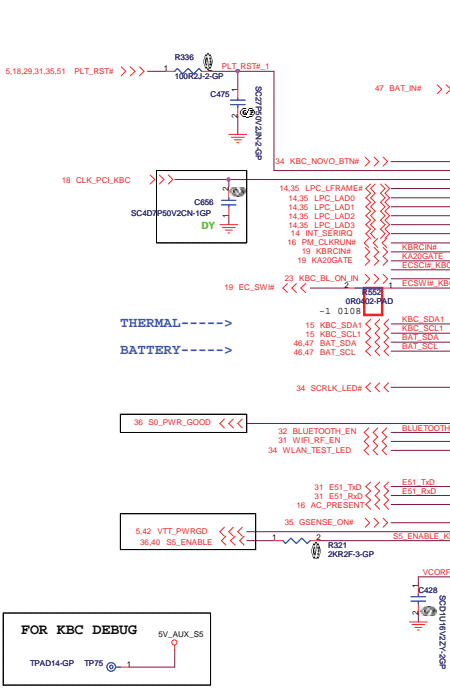
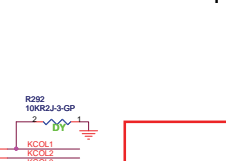
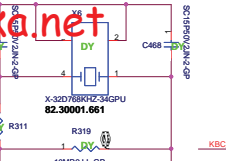
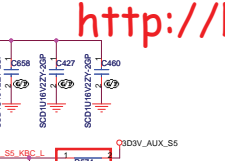
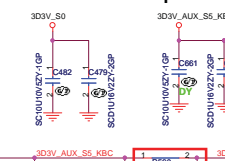
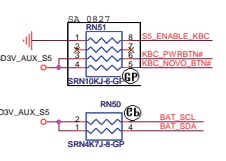
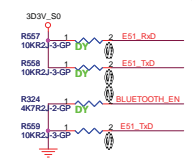


Table with 2 columns: Pin # and Pin 1-20. It lists pin numbers and their corresponding functions or connections.

Table with 2 columns: Pin # and Pin 1-20. It lists pin numbers and their corresponding functions or connections.

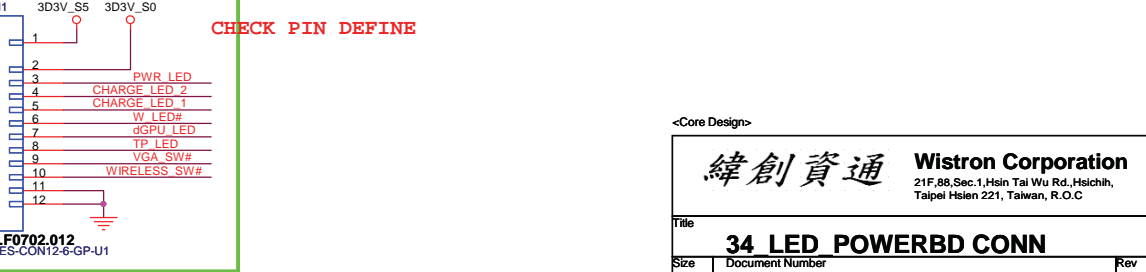
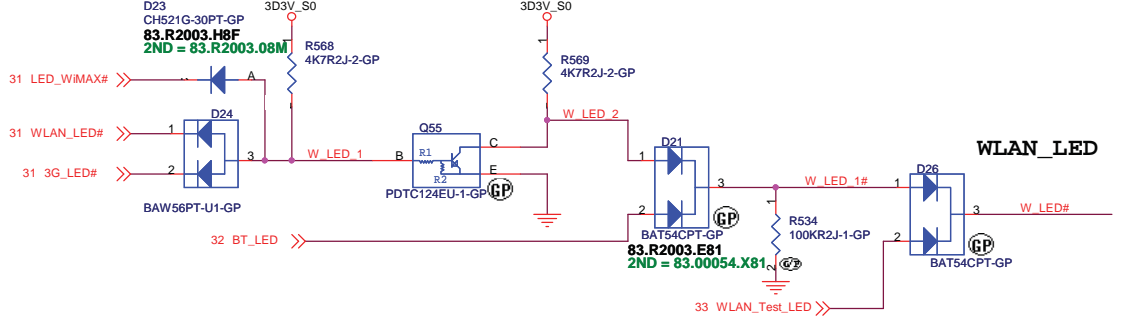
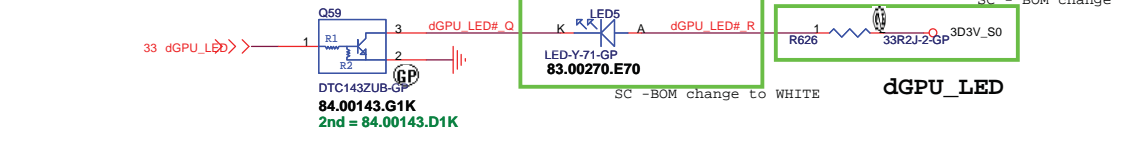
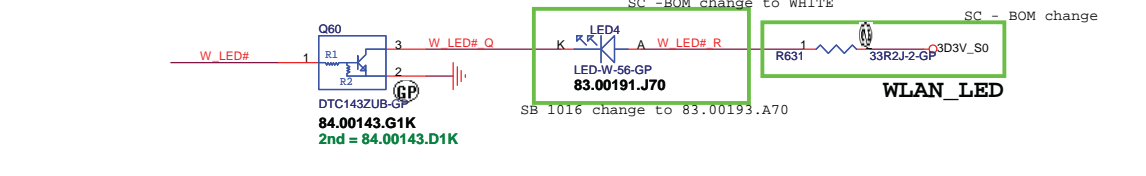
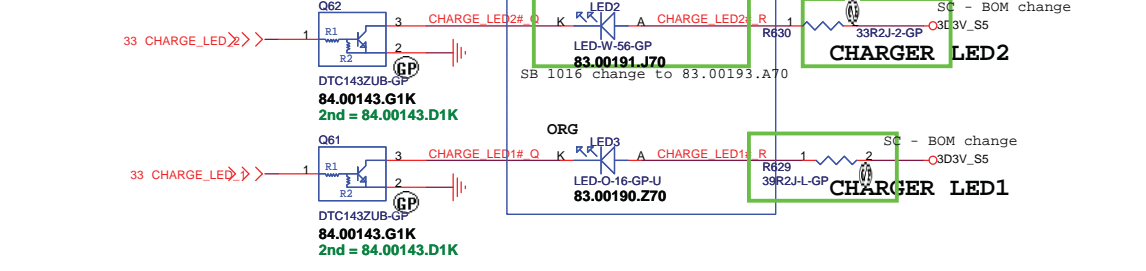
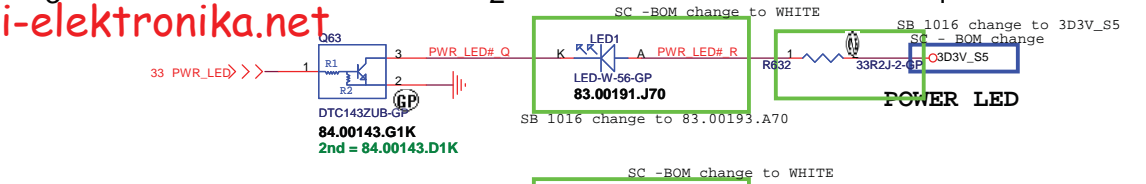
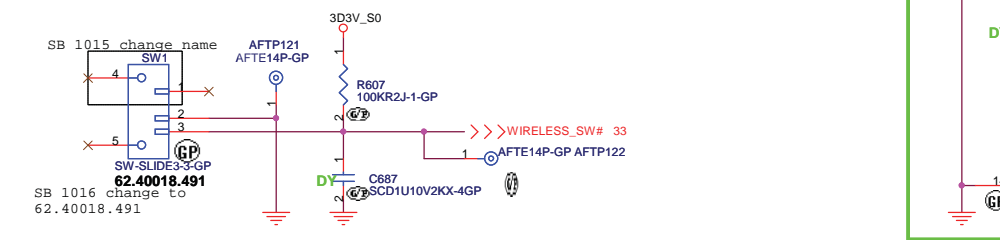
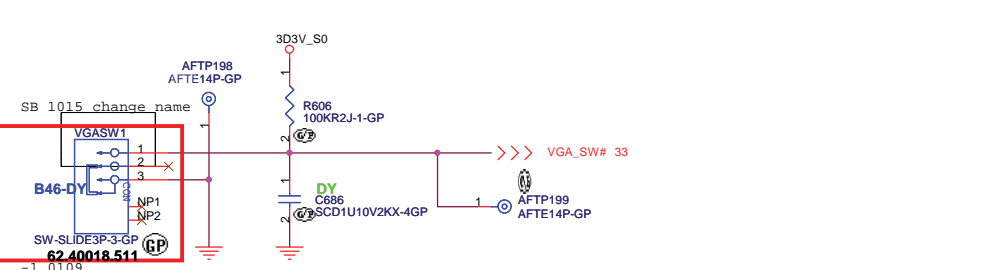
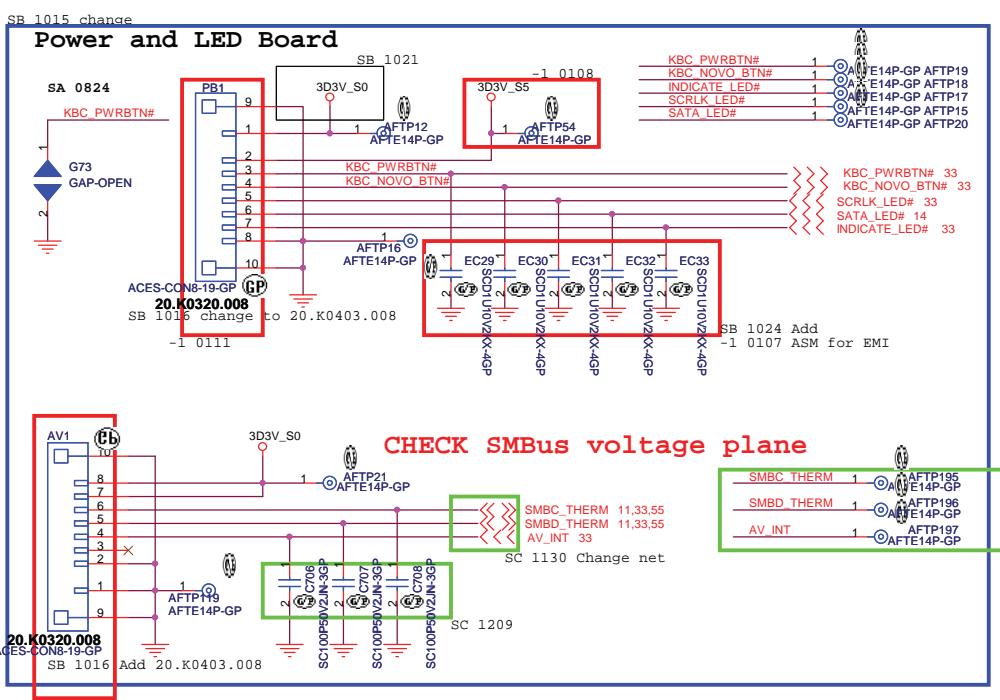
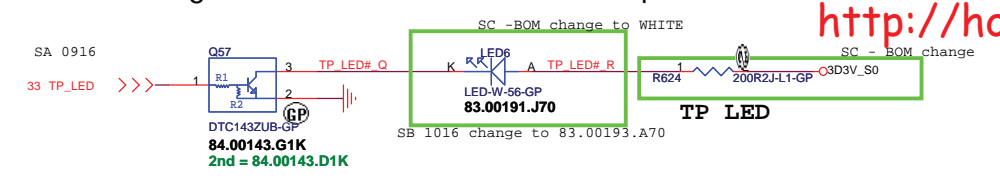
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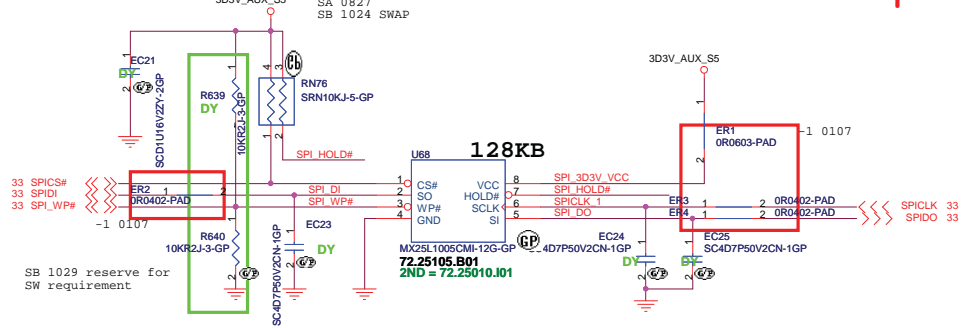
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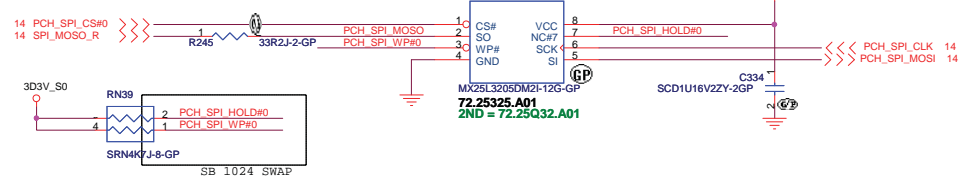
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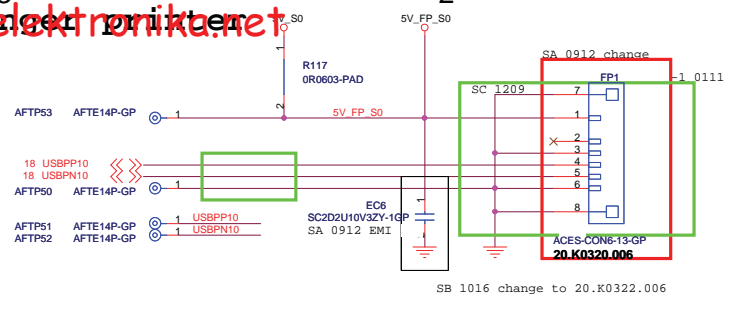
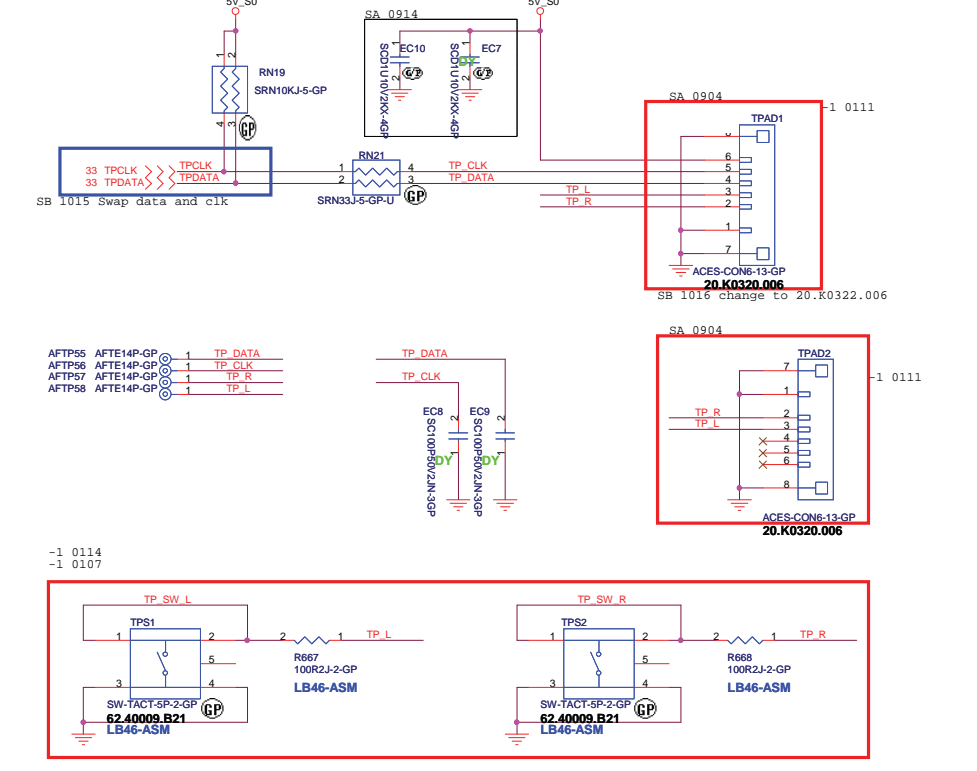
EC BIOS Flash ROM



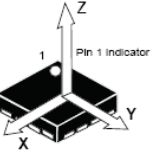
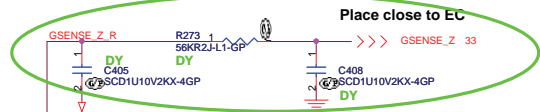
System BIOS Flash ROM



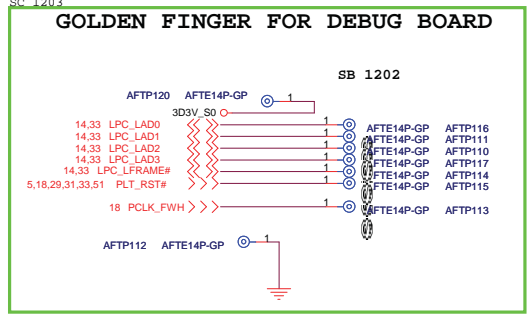
TOUCH PAD



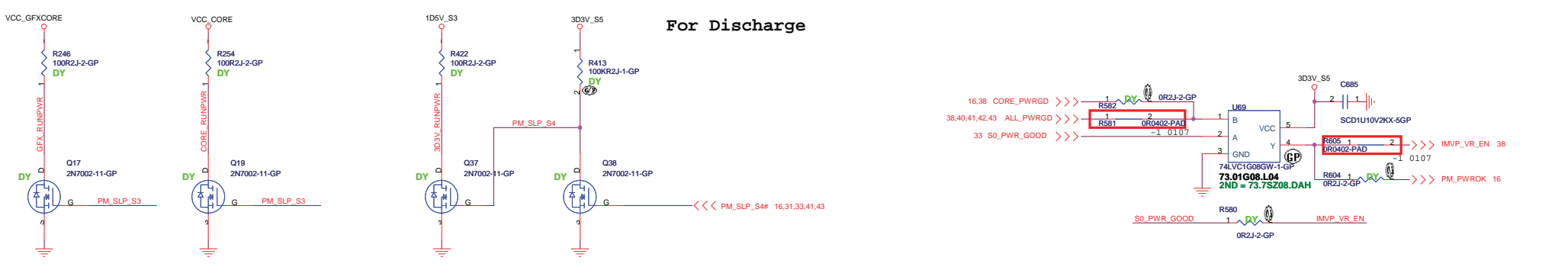
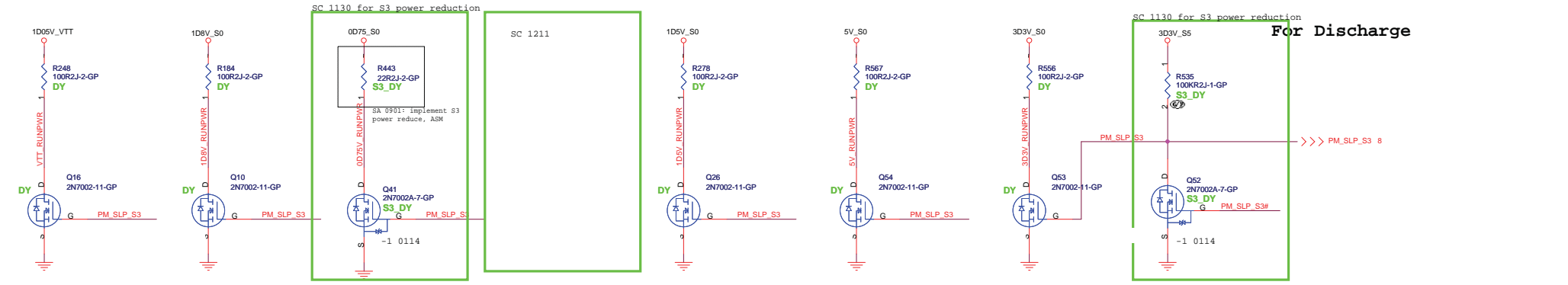
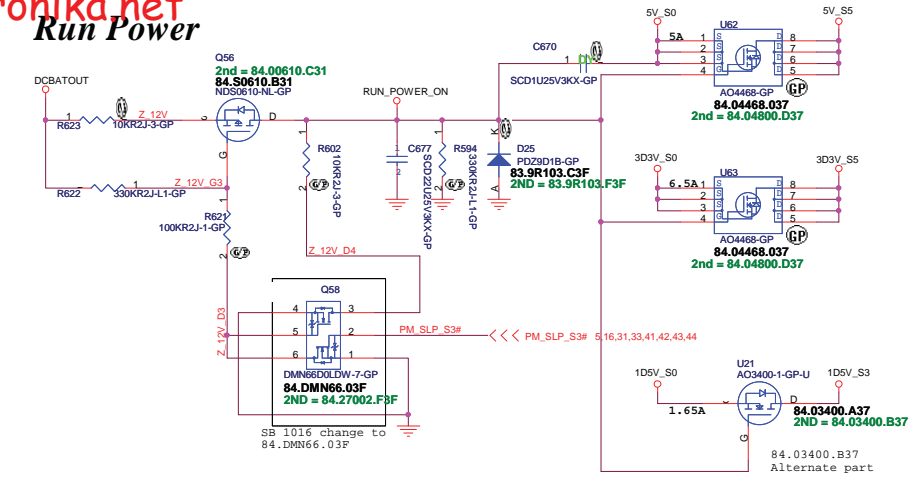
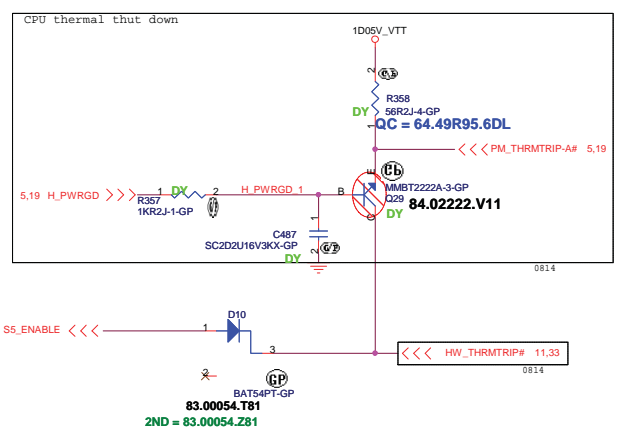
G-Sensor



STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00035.0BZ



Run Power



<Core Design>

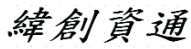
緯創資通 **Wistron Corporation**
 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichn, Taipei Hsien 221, Taiwan, R.O.C

Title	36 Run PWR		
Size	Document Number		Rev
Customer	LA46 MB DIS		
Date:	Tuesday, January 26, 2010	Sheet	36 of 58

D
C
B
A

D
C
B
A

<Core Design>

		Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title			
37 BLANK			
Size	Document Number	Rev	
A3	LA46 MB	SA	
Date:	Tuesday, January 26, 2010	Sheet	37 of 58

5

4

3

2

1

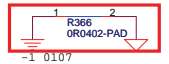
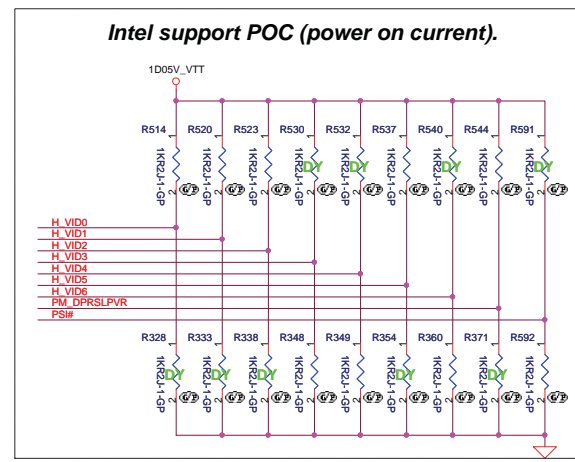
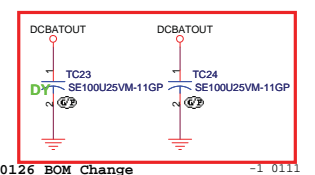
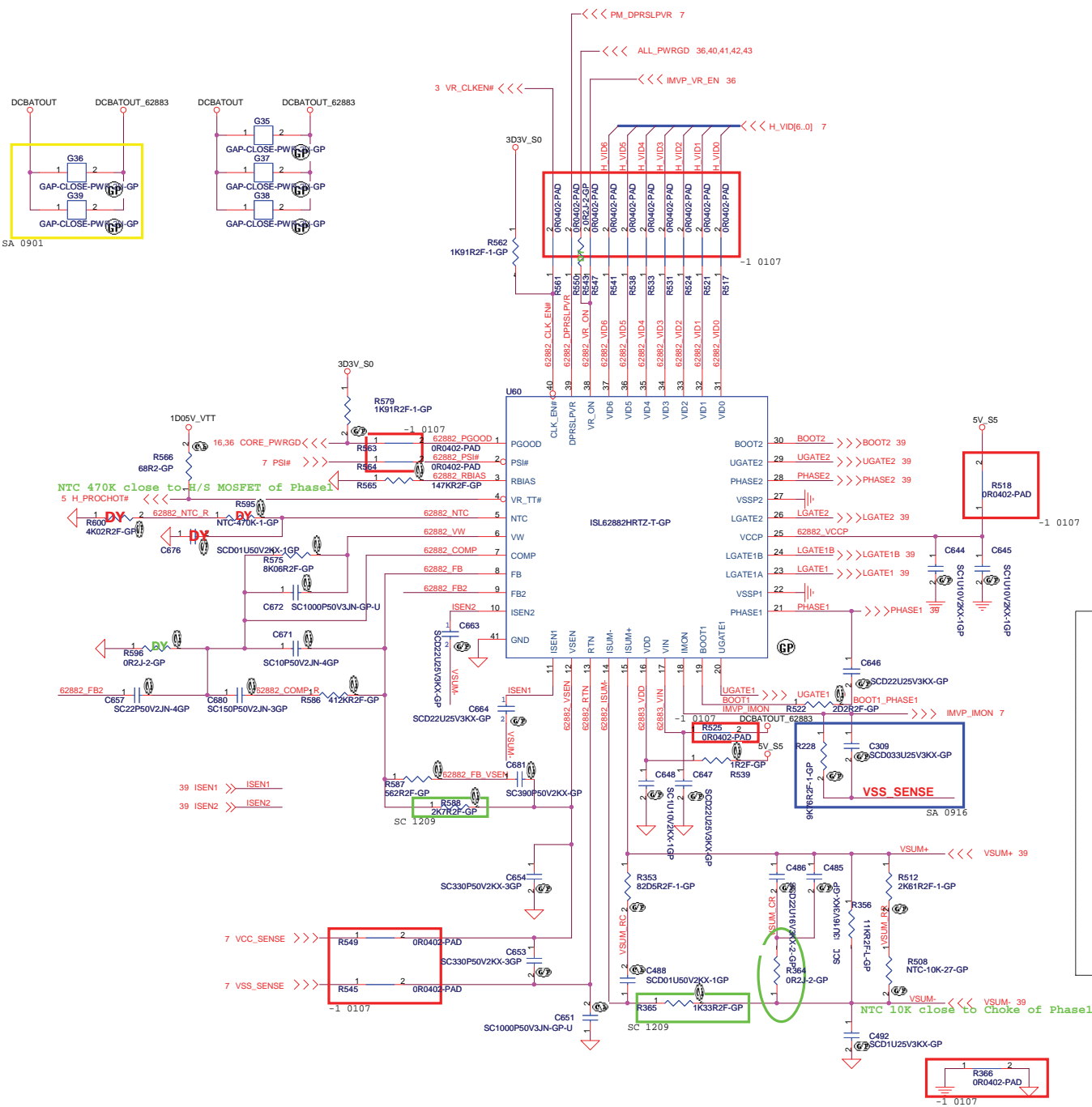
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4

3

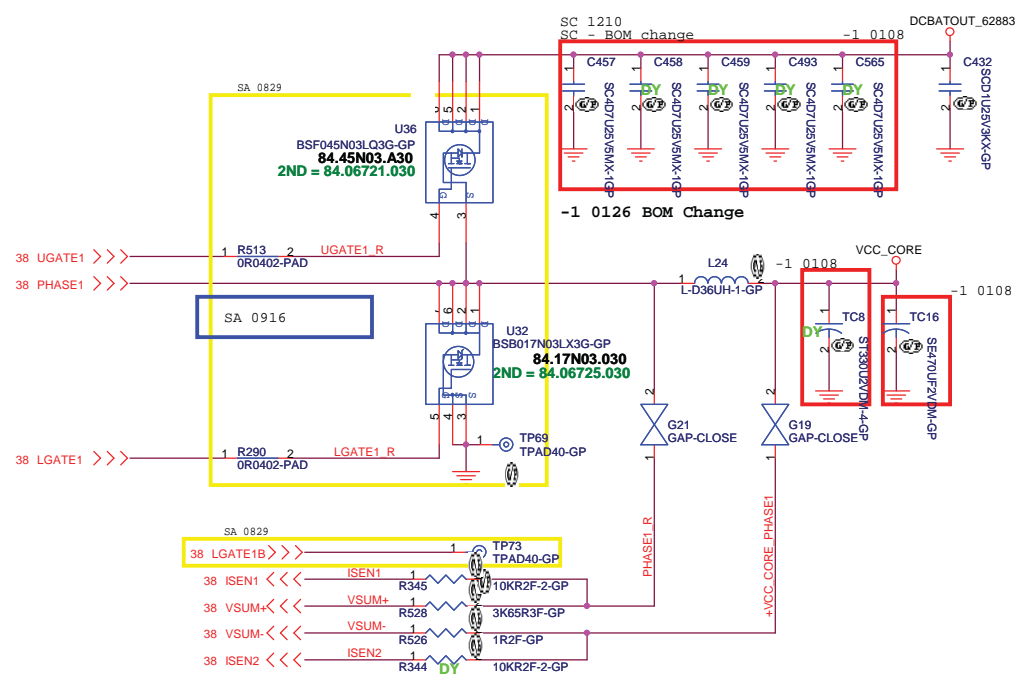
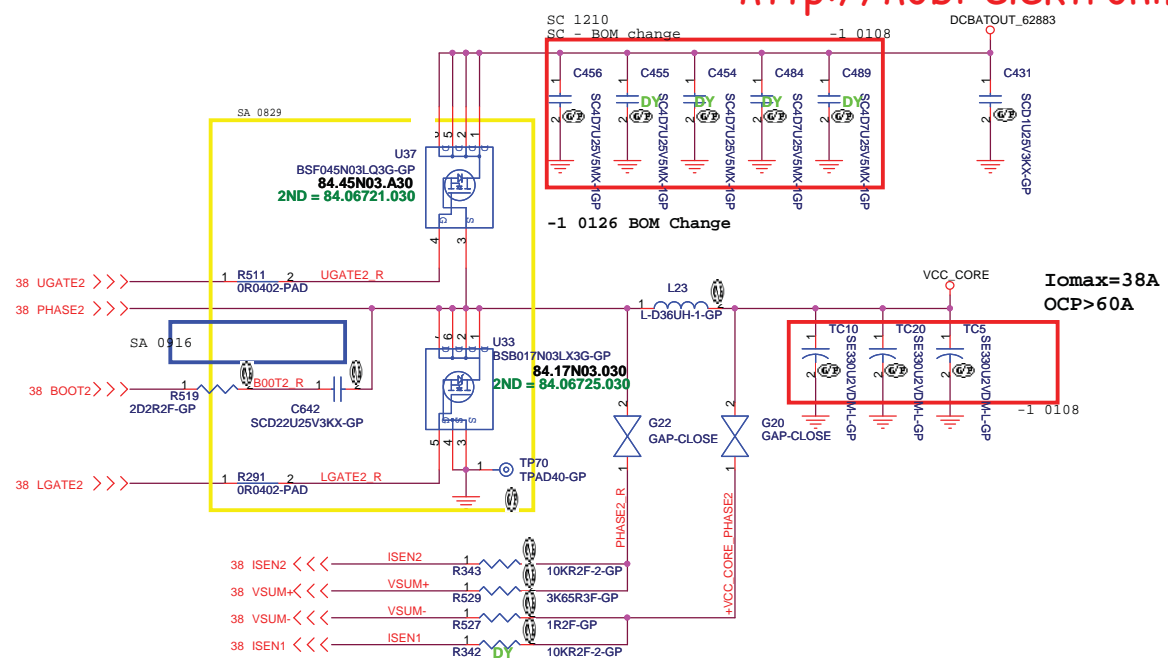
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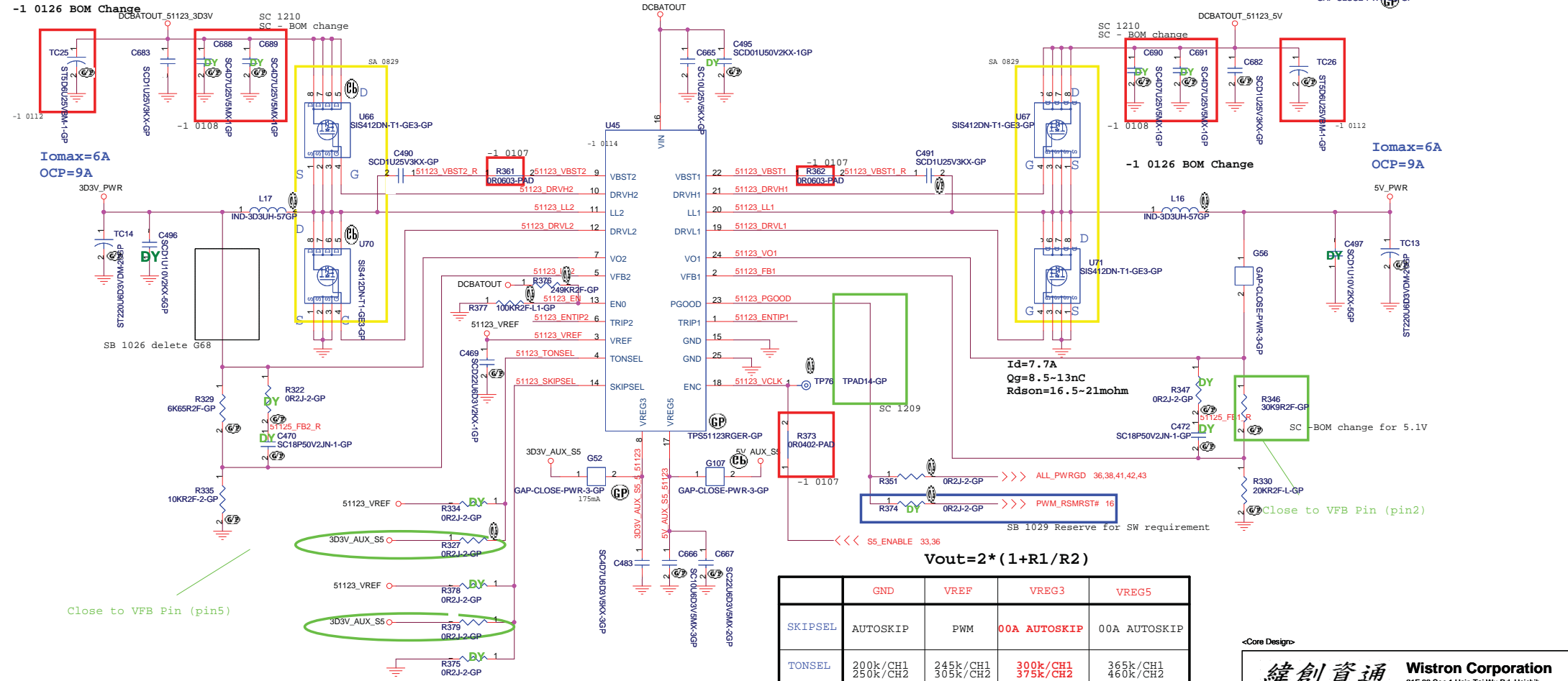
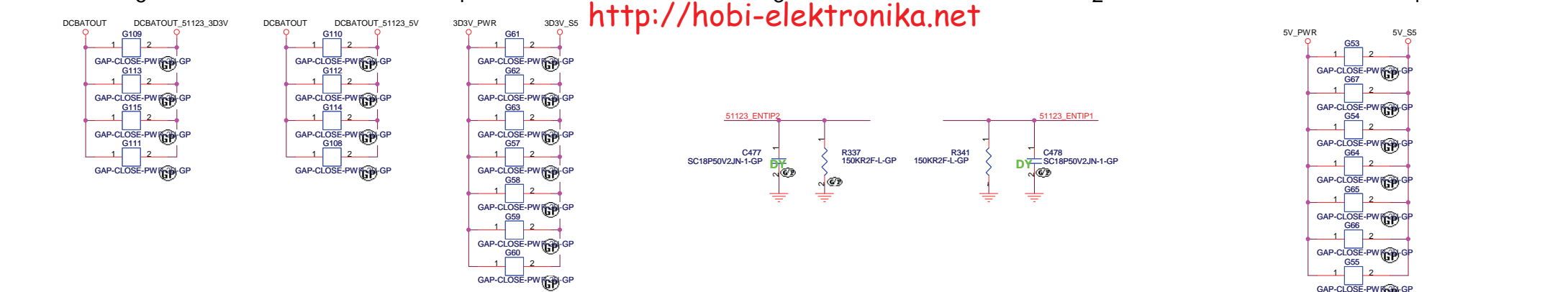
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<Core Design>
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title		38 ISL62882 CPU CORE (1 of 2)	
Size	Document Number	LA46 MB DIS	Rev
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	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

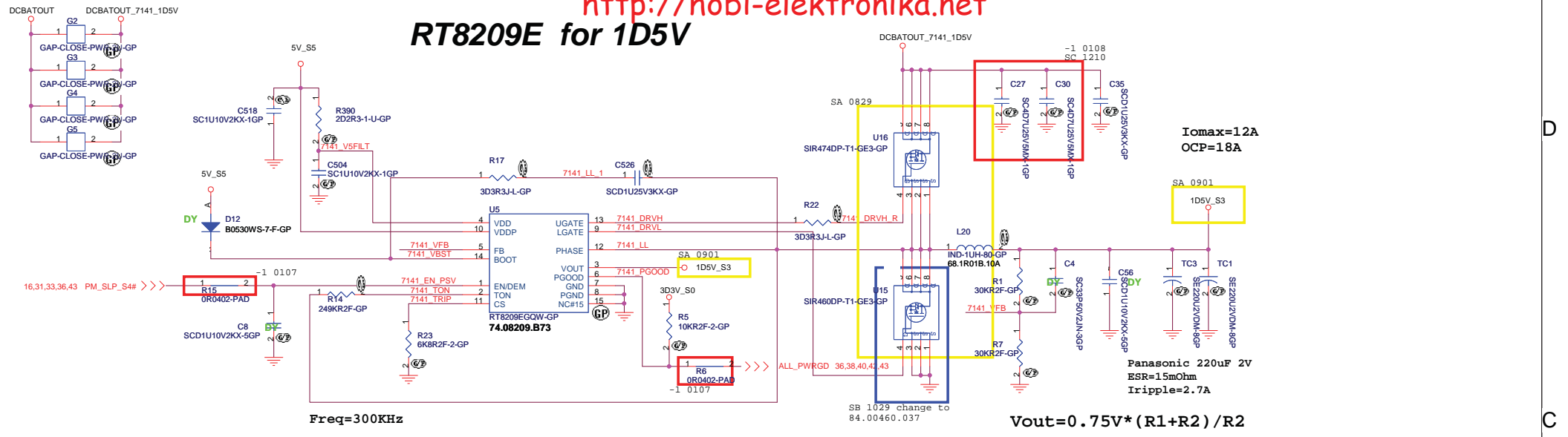
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **40 TPS51123 5V/3D3V**

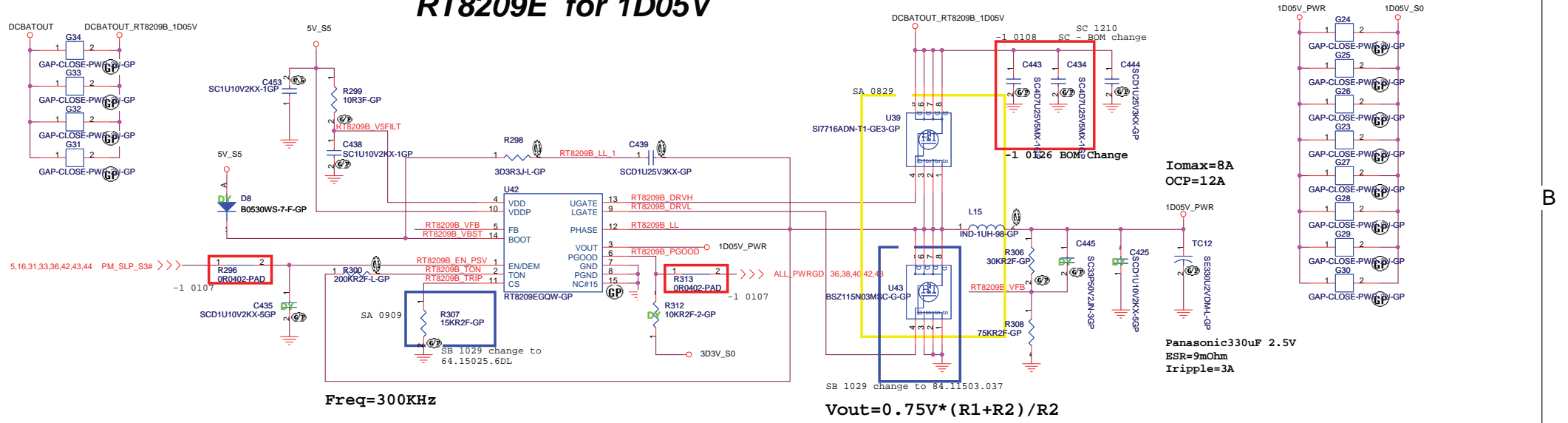
Size: Document Number
Custom: **LA46 MB DIS**

Date: Wednesday, January 27, 2010 Sheet 40 of 58 Rev -1

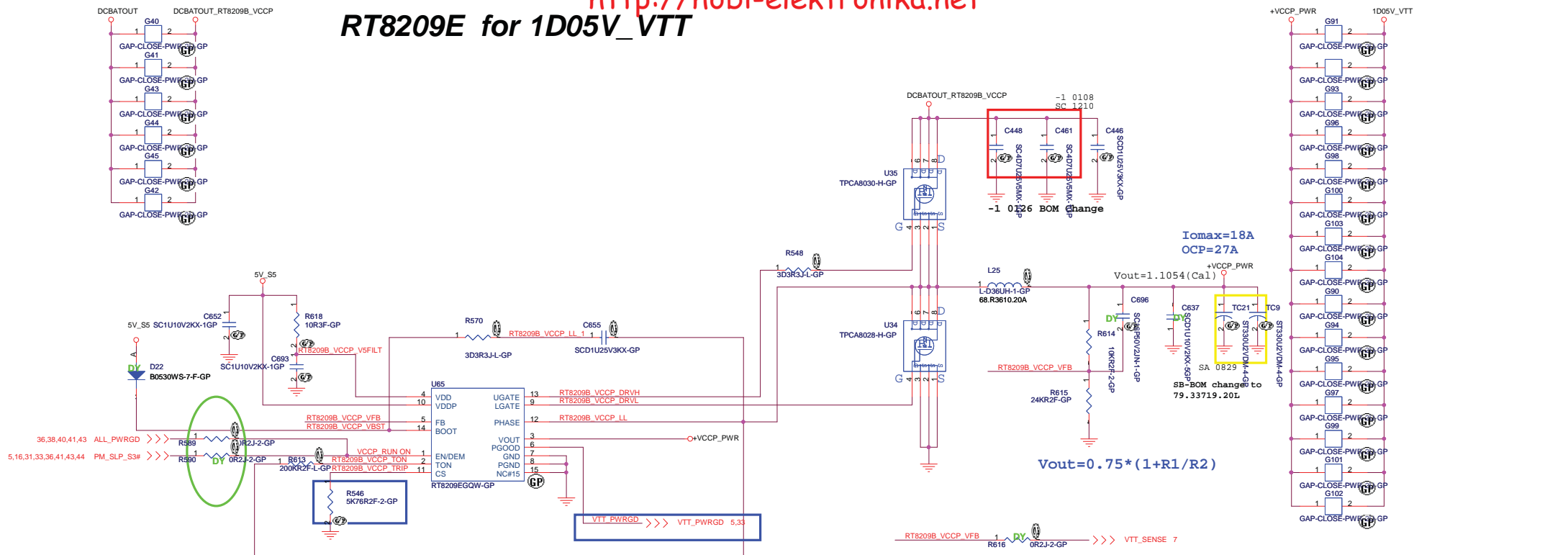
RT8209E for 1D5V



RT8209E for 1D05V



RT8209E for 1D05V_VTT



Freq=360KHz

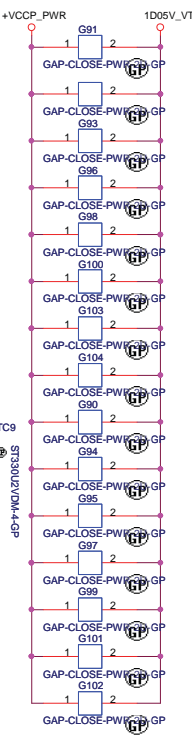
$$V_{out} = 0.75 * (1 + R1/R2)$$

I_{omax}=18A
OCP=27A

V_{out}=1.1054 (Cal)

SB-BOM changed to
79.33719.20L

-1 0108
SC 1210
BOM change



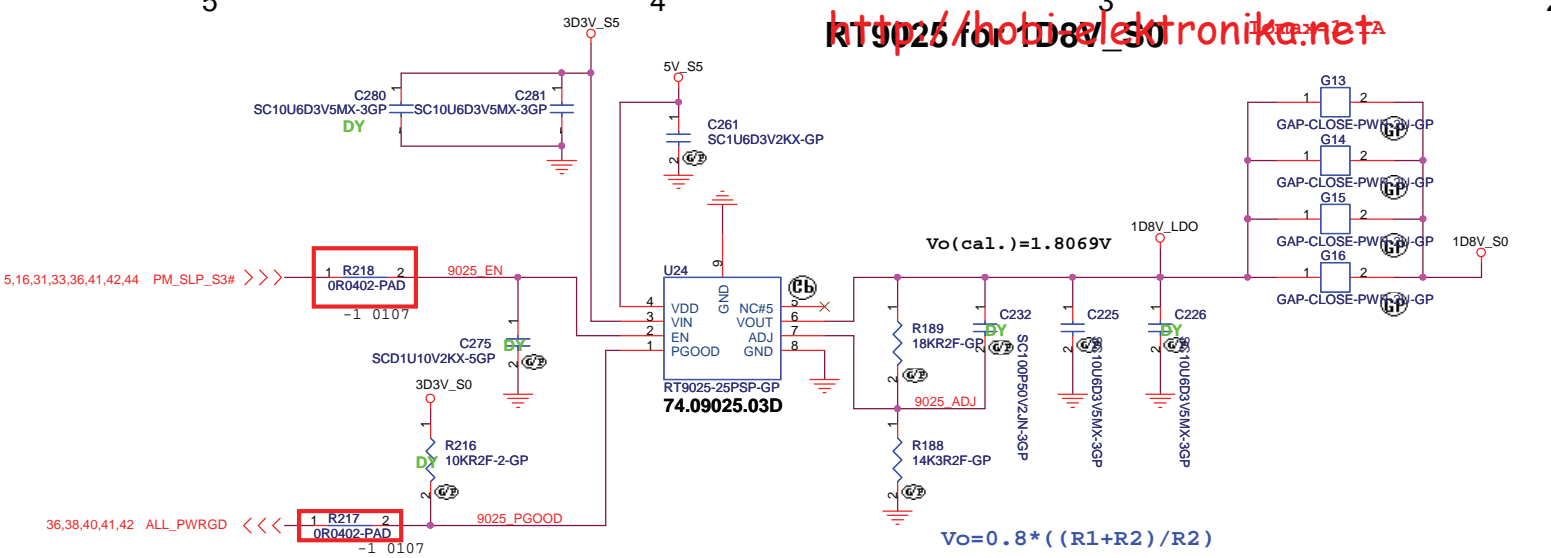
<-Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei 305, Taiwan, R.O.C

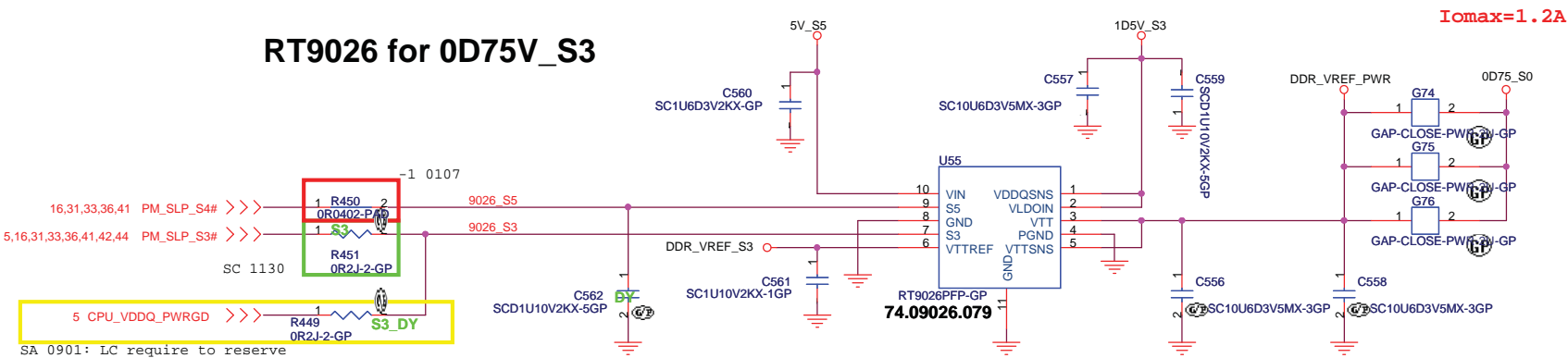
File: **42 RT8209E 1D05V VTT**

Size: Document Number
Custom: **LA46 MB DIS** Rev: -1

Date: Wednesday, January 27, 2010 Sheet 42 of 58



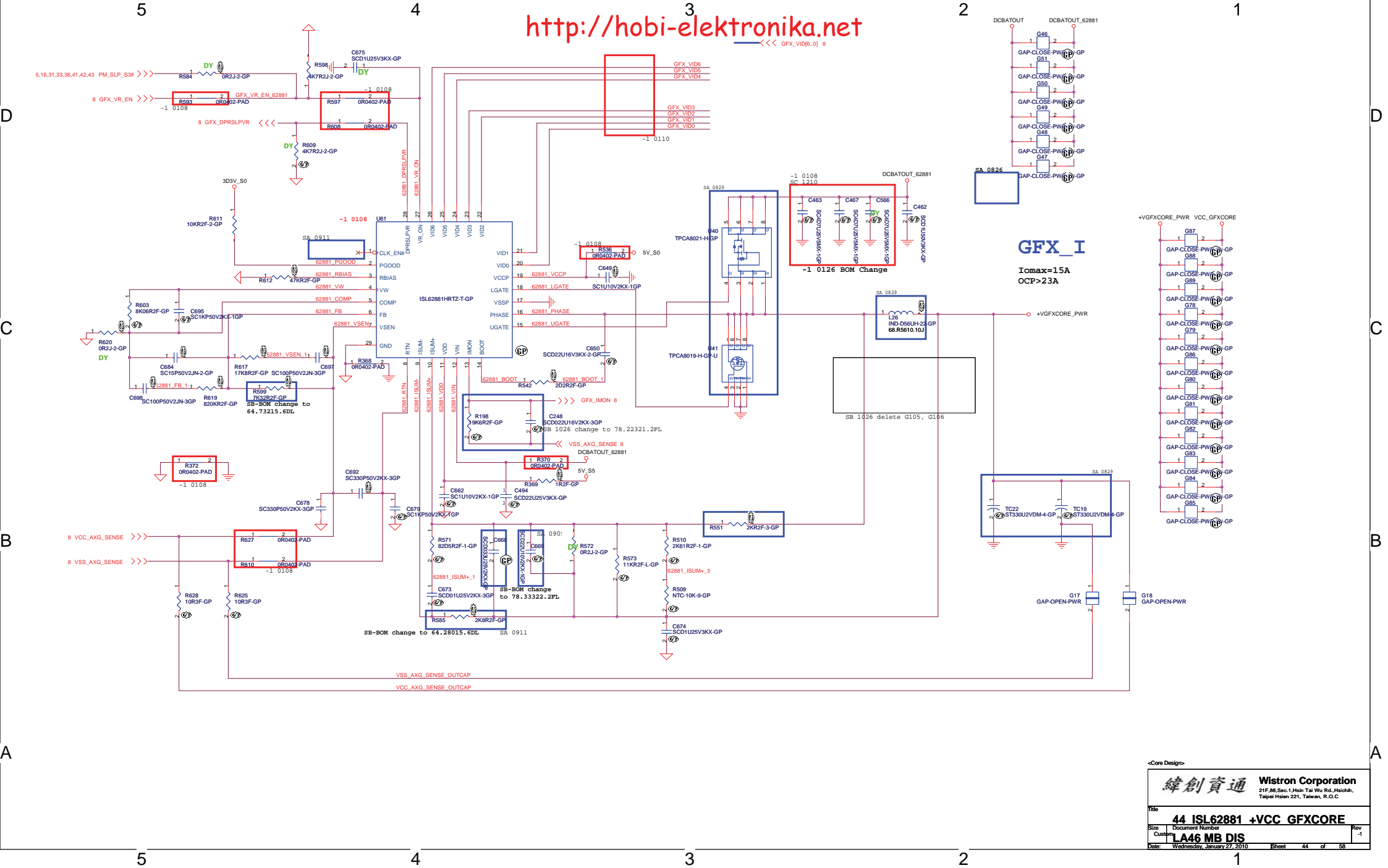
RT9026 for 0D75V_S3



<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		43 RT9025 1D8V/ RT9026 0D75	
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
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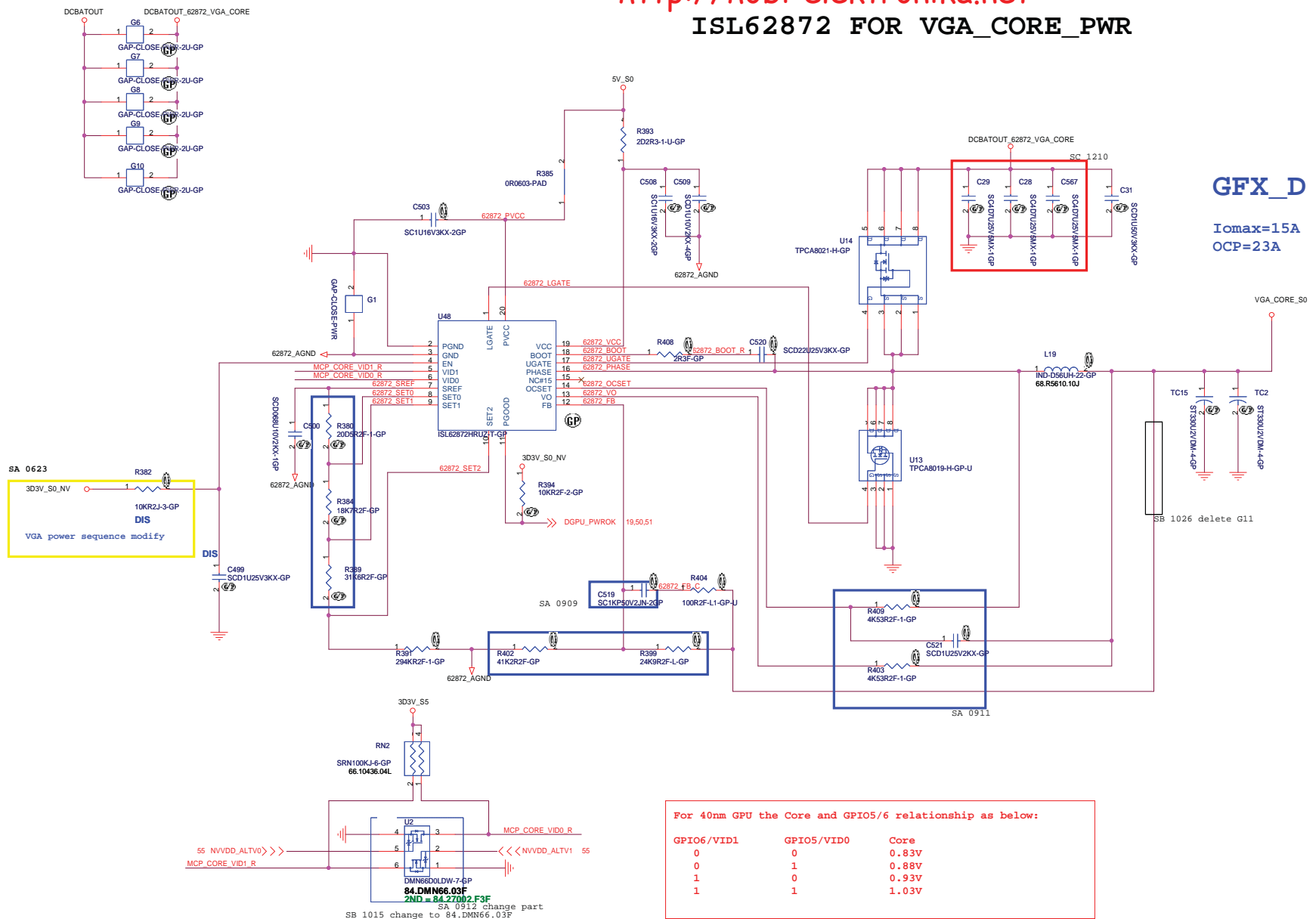
http://hobi-elektronika.net

GFX_I

I_{omax}=1.5A
OCP>2.3A

<Core Design>
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

Title	44 ISL62881 +VCC GFXCORE	
Size	Document Number	Rev
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For 40nm GPU the Core and GPIO5/6 relationship as below:

GPIO6/VID1	GPIO5/VID0	Core
0	0	0.83V
0	1	0.88V
1	0	0.93V
1	1	1.03V

SB 1031 R380 Change to 64.20R55.6DL
 R384 Change to 64.18725.6DL
 R389 Change to 64.31625.6DL
 to rise up VGA voltage for NV suggestion.

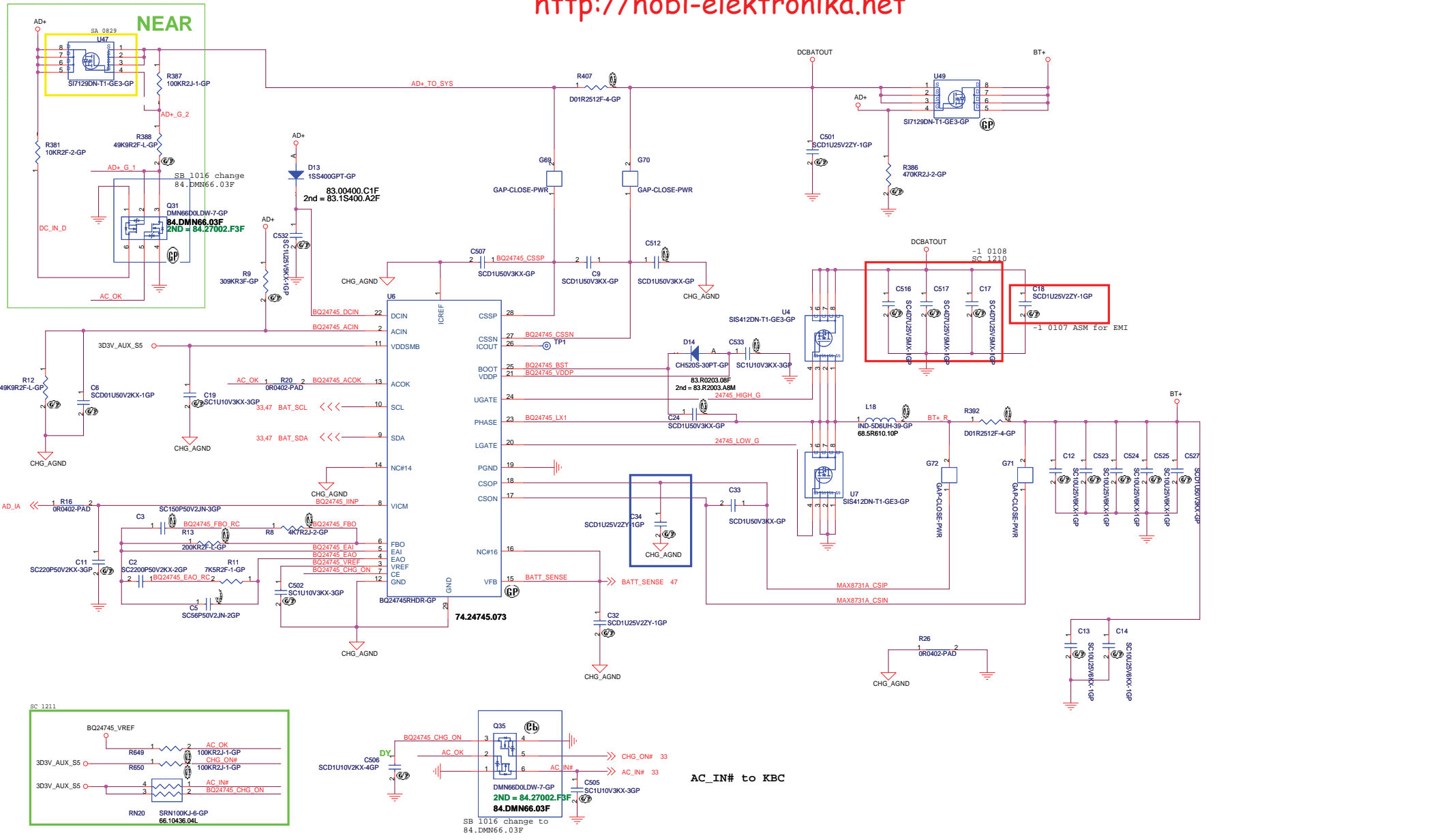
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

Title: **45 ISL62872 VGA CORE**

Size: Customer Document Number: **LA46 MB DIS** Rev: -1

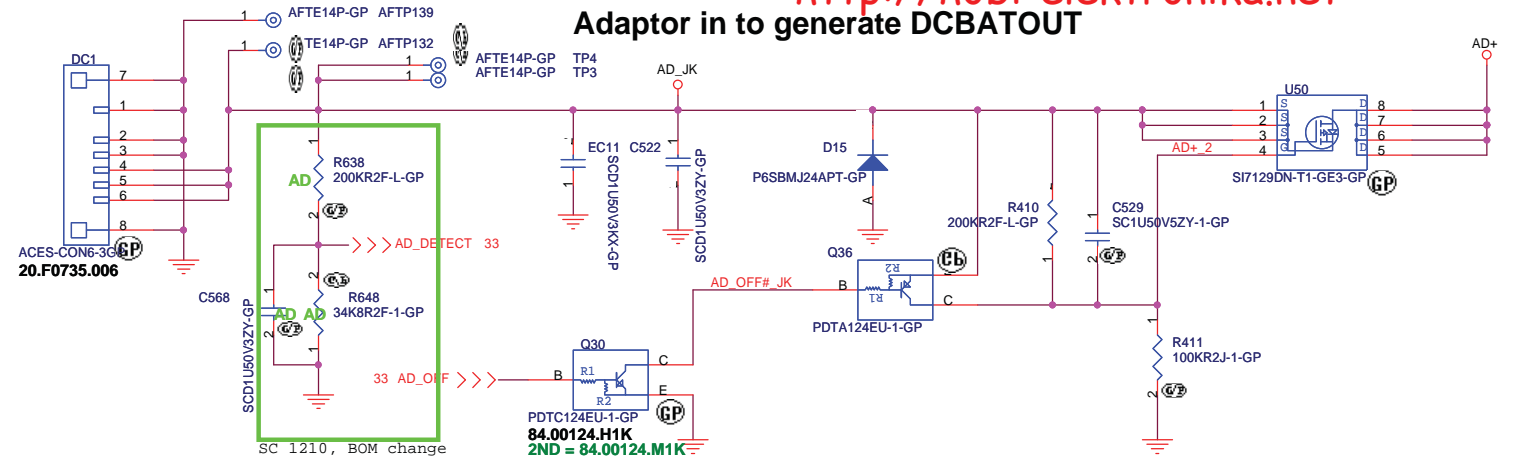
Date: Tuesday, January 26, 2010 Sheet: 45 of 58



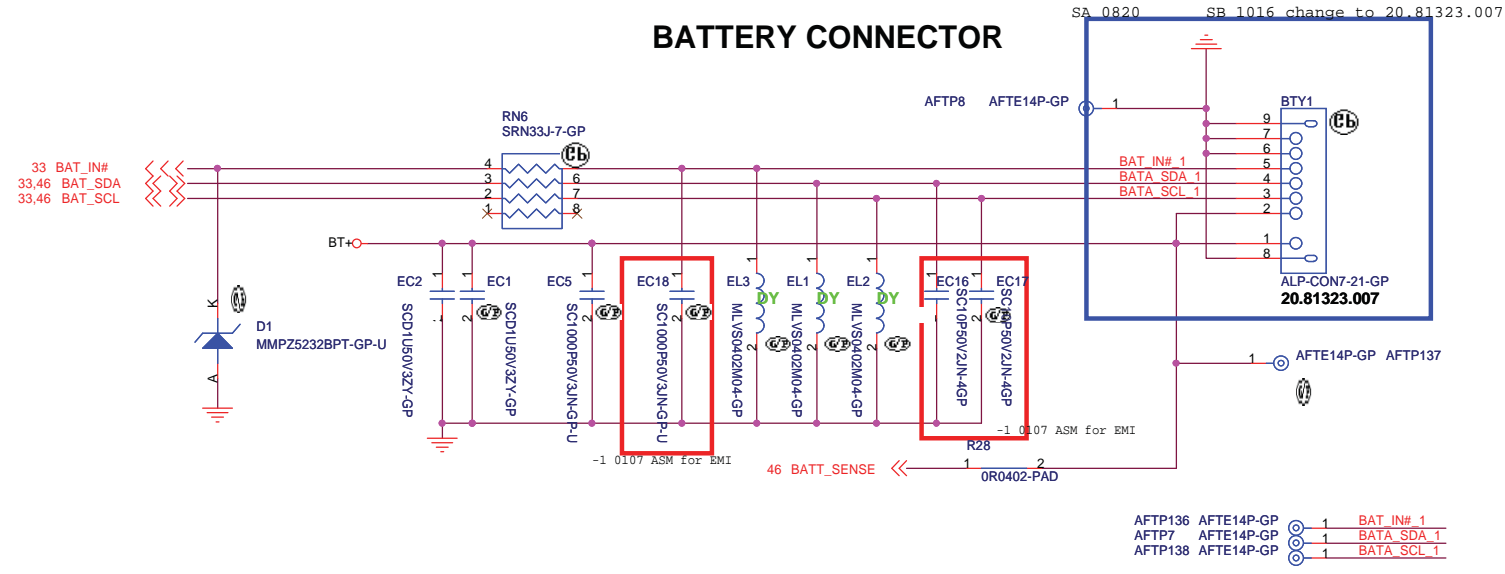
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緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		46 BQ24745 CHARGER	
Size	Customer	Document Number	Rev
		LA46 MB DIS	-1
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Adaptor in to generate DCBATOUT

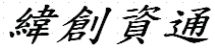


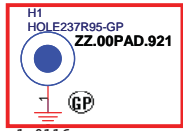
BATTERY CONNECTOR



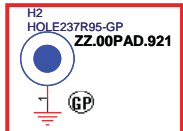
- AFTP136 AFTE14P-GP 1 BAT_IN# 1
- AFTP7 AFTE14P-GP 1 BATA_SDA 1
- AFTP138 AFTE14P-GP 1 BATA_SCL 1

<Core Design>

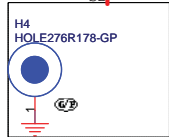
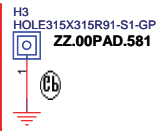
 Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title 47 AD/BATT CONN	
Size	Document Number
Custom	LA46 MB DIS
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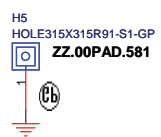
-1 0116



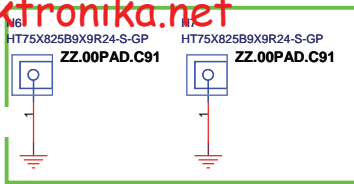
SC 1130 Remove H2
-1 0110



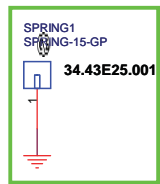
ZZ.00PAD.N11



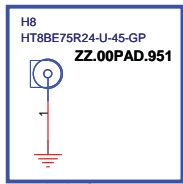
ZZ.00PAD.581



SC 1130 CHECK, H6, H7 change to ZZ.00PAD.C91



SC 1209



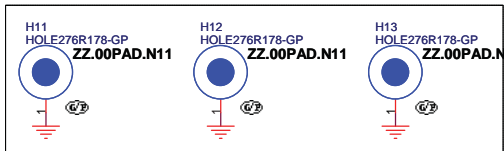
SB 1016 change to
ZZ.00PAD.951



ZZ.00PAD.951



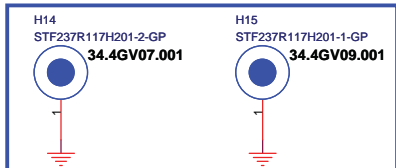
SB 1016 change to
34.4Y702.101



ZZ.00PAD.N11

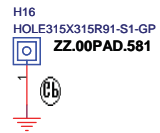
ZZ.00PAD.N11

ZZ.00PAD.N11

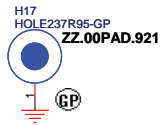


SB 1016 change to
34.4GV07.001

SB 1016 change to
34.4GV09.001



ZZ.00PAD.581



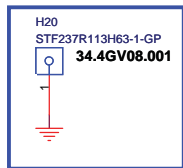
ZZ.00PAD.921



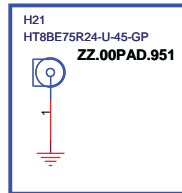
ZZ.00PAD.921



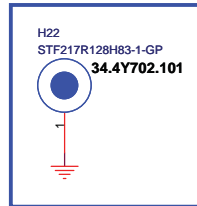
ZZ.00PAD.921



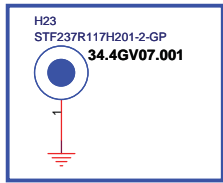
SB 1016 change to
34.4GV08.001



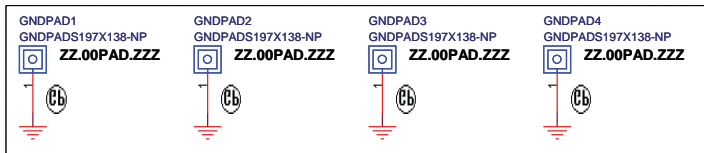
SB 1016 change
to ZZ.00PAD.951



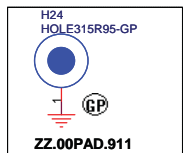
SB 1016 change to
34.4Y702.101



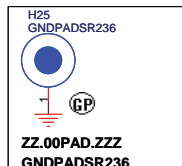
SB 1016 Add 34.4GV07.001



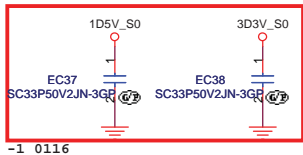
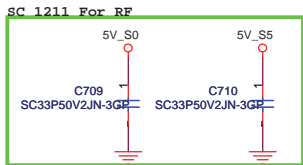
SB 1019 Add GND PAD



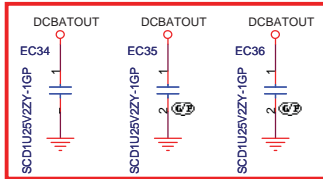
SB 1021 Add ZZ.00PAD.911



SB 1021 Add GNDPADSR236

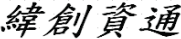


-1 0116

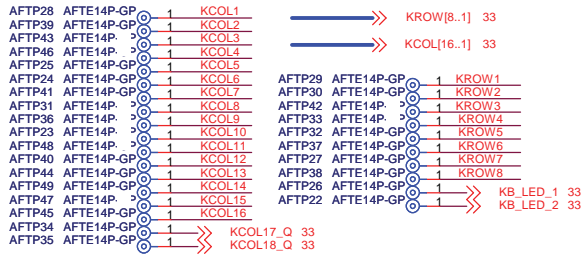


-1 0107 ASM for EMI

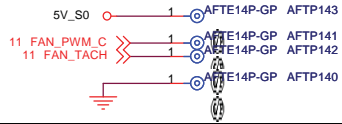
<Core Design>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	48_EMI/Spring/Boss
Size	Document Number
A3	LA46 MB DIS
Date:	Tuesday, January 26, 2010
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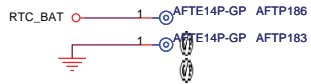
Near KB1 Keyboard



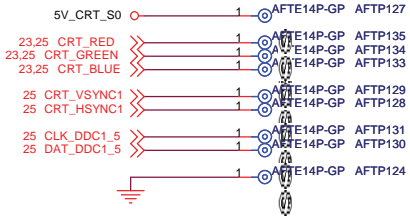
Near FAN1



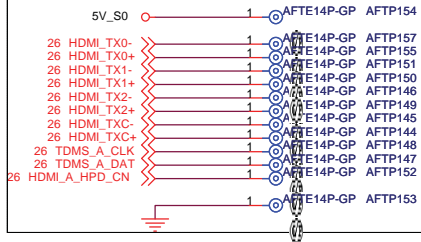
Near RTC1



Near CRT_CN1



Near HDMI_CN1

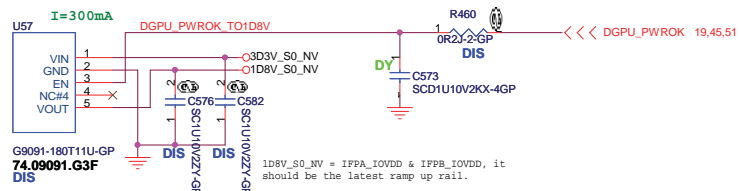


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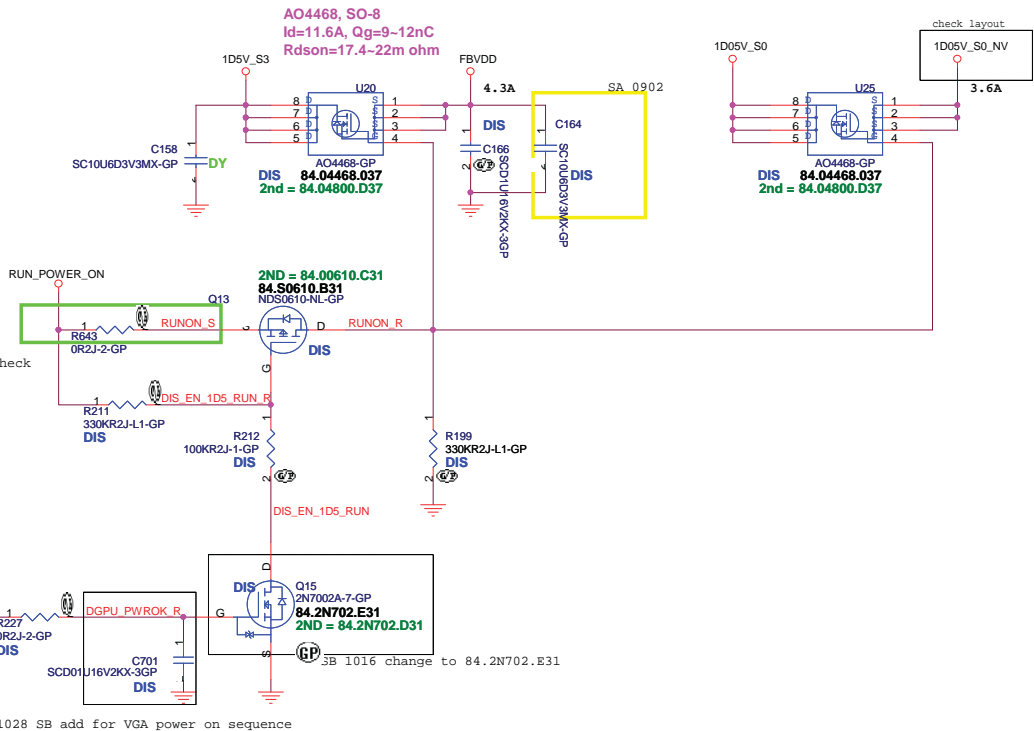
緯創資通 **Wistron Corporation**
 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

Title		
49 AFTE TP		
Size	Document Number	Rev
A3	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 49 of 58

+3VS to 1.8V Transfer



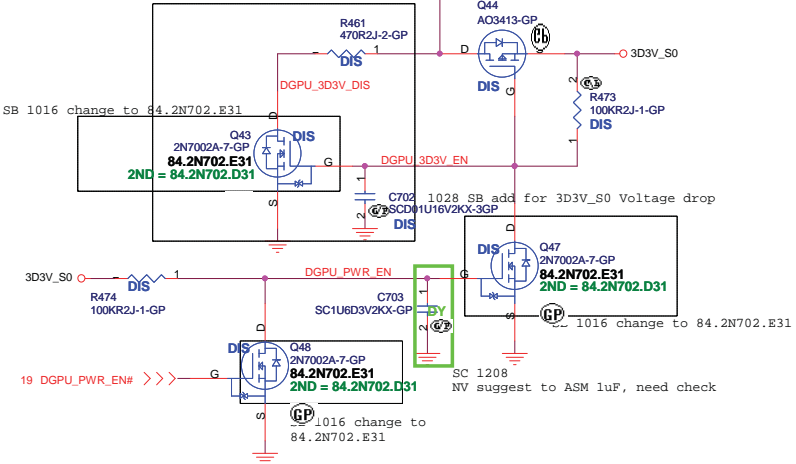
SC 1208 NV suggest to use 200K, need check



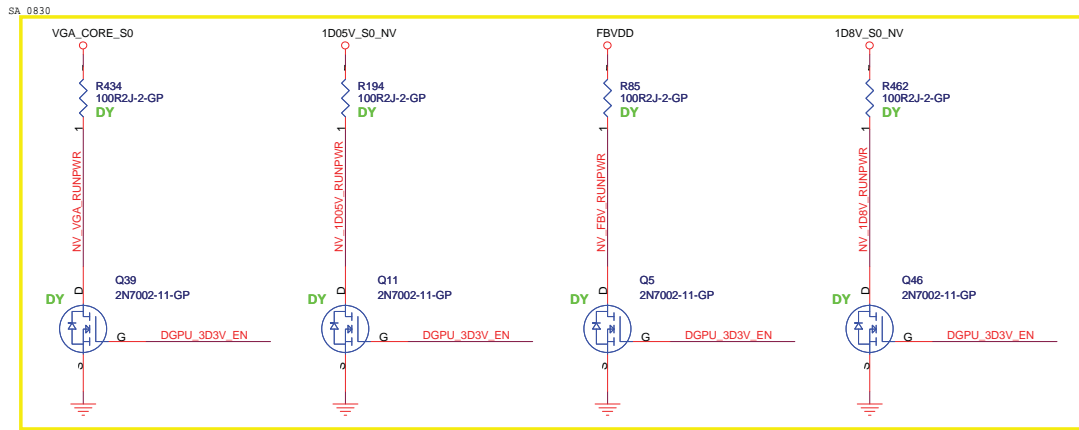
+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT



SC 1208 NV suggest to ASM 1uF, need check

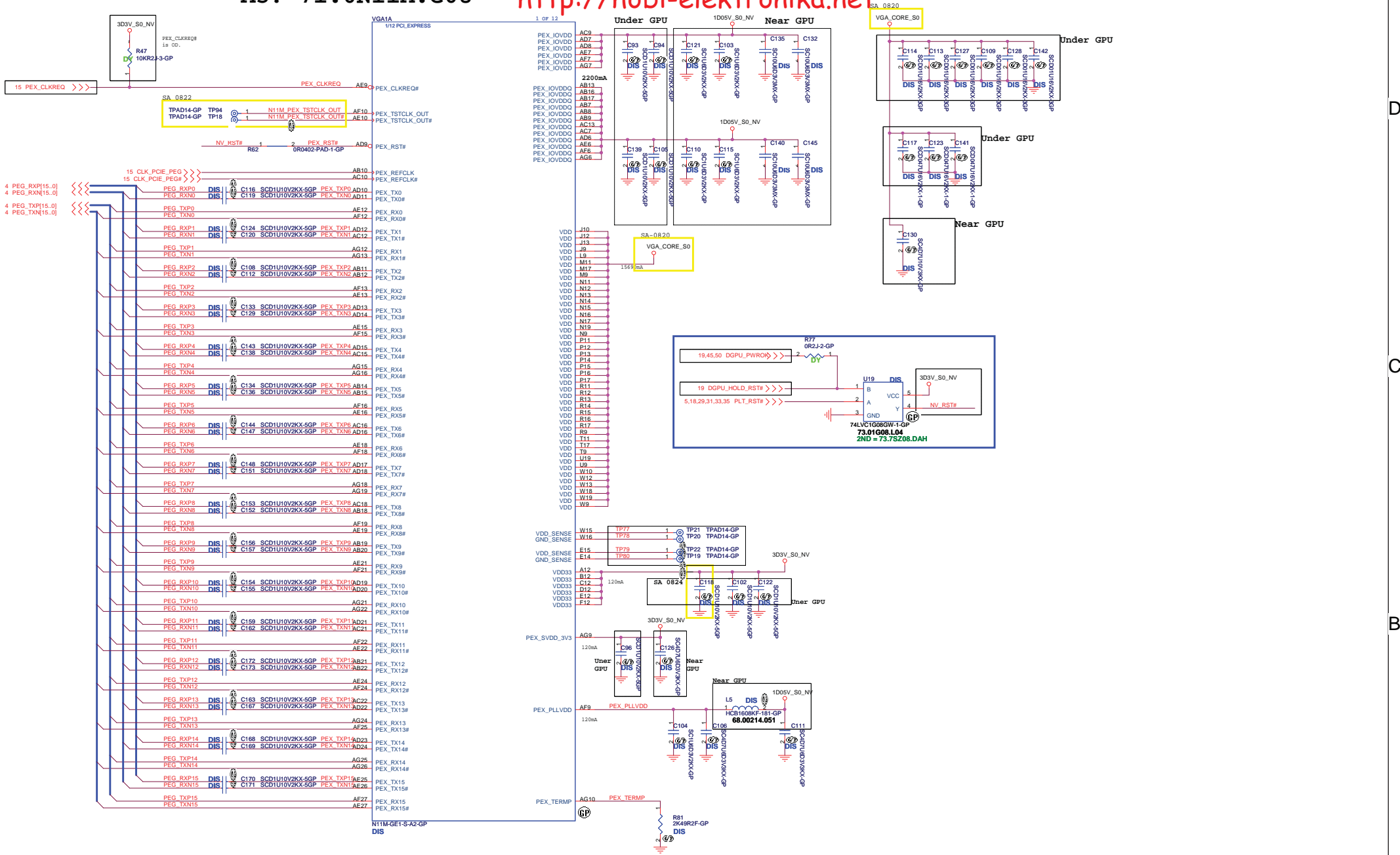


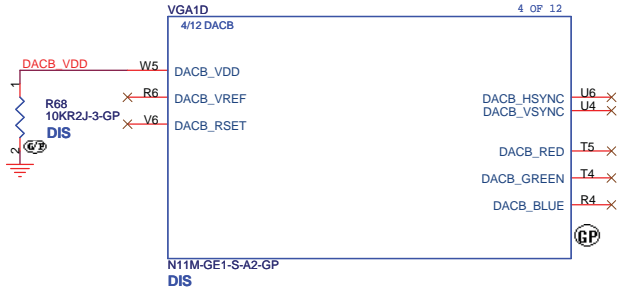
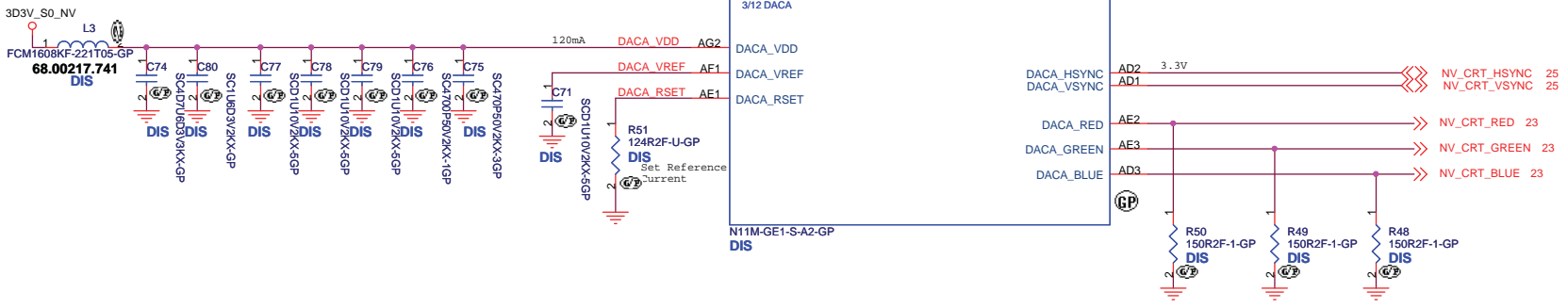
system turn on 3D3V_S0_NV --> VGA_CORE_S0
DGPU_PWROK --> FBVDD, 1D05V_S0_NV, 1D8V_S0_NV

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

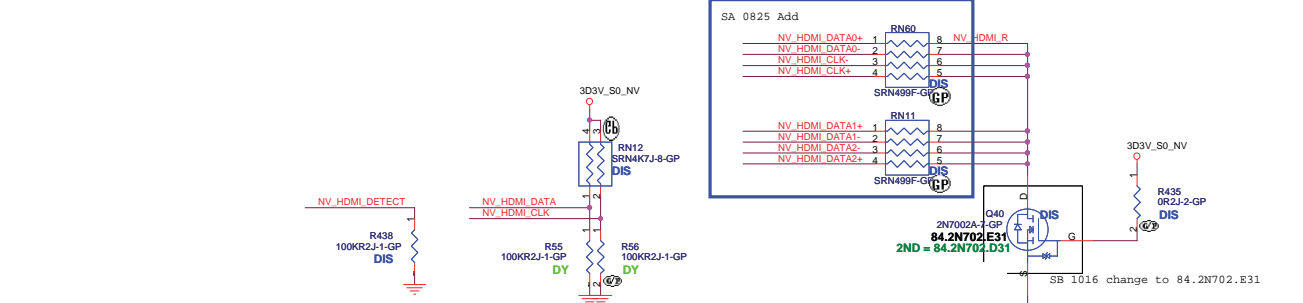
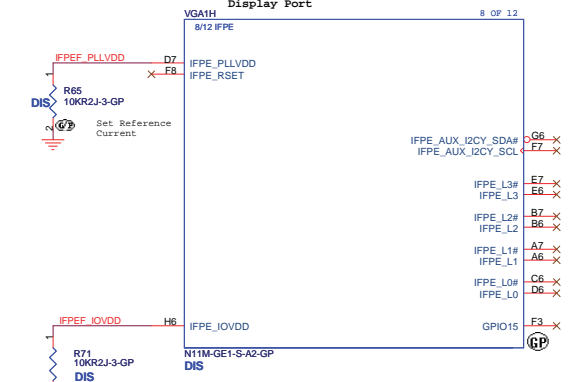
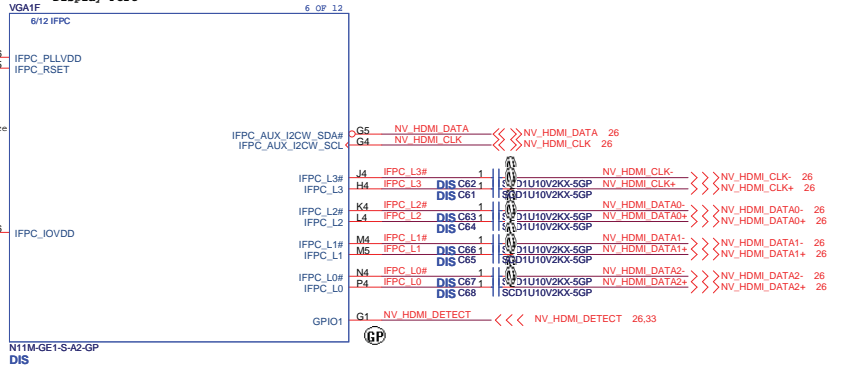
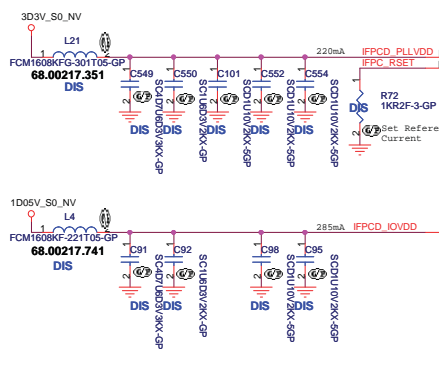
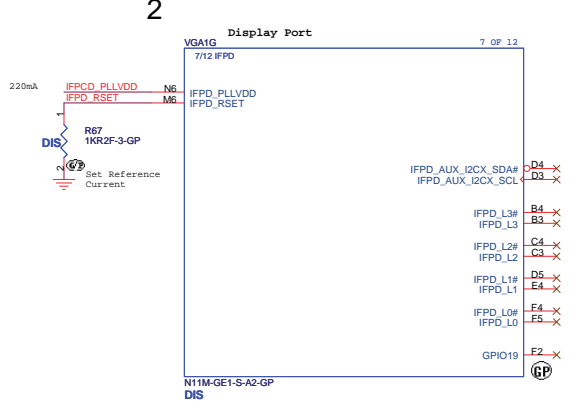
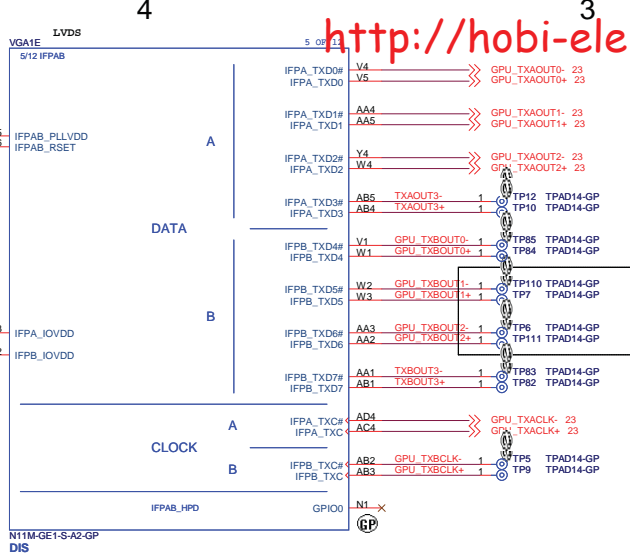
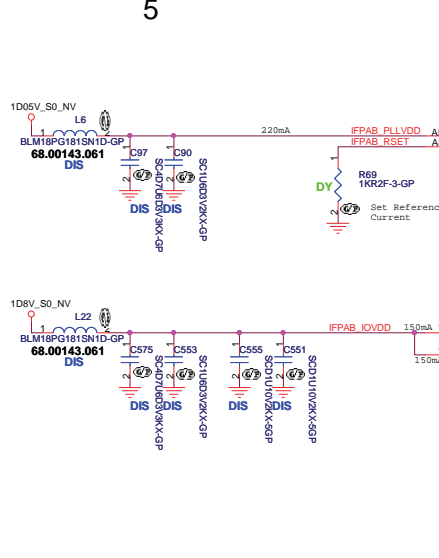
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Size	Document Number	Customer	Rev
	LA46 MB DIS		-1
Date:	Tuesday, January 26, 2010	Sheet	50 of 58



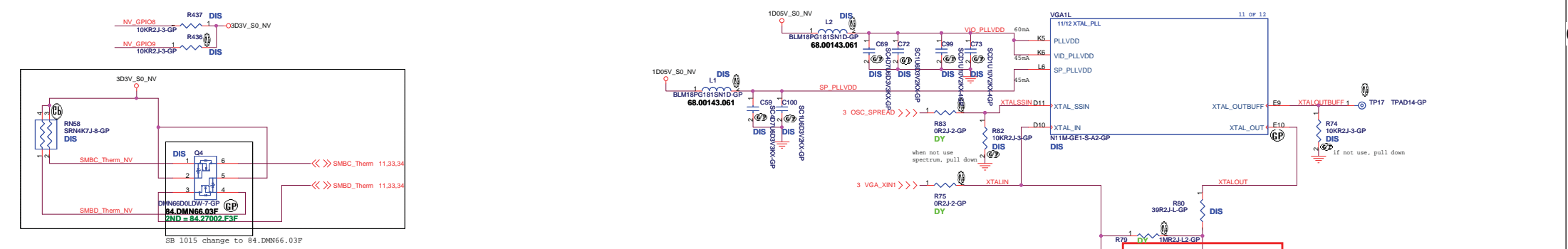
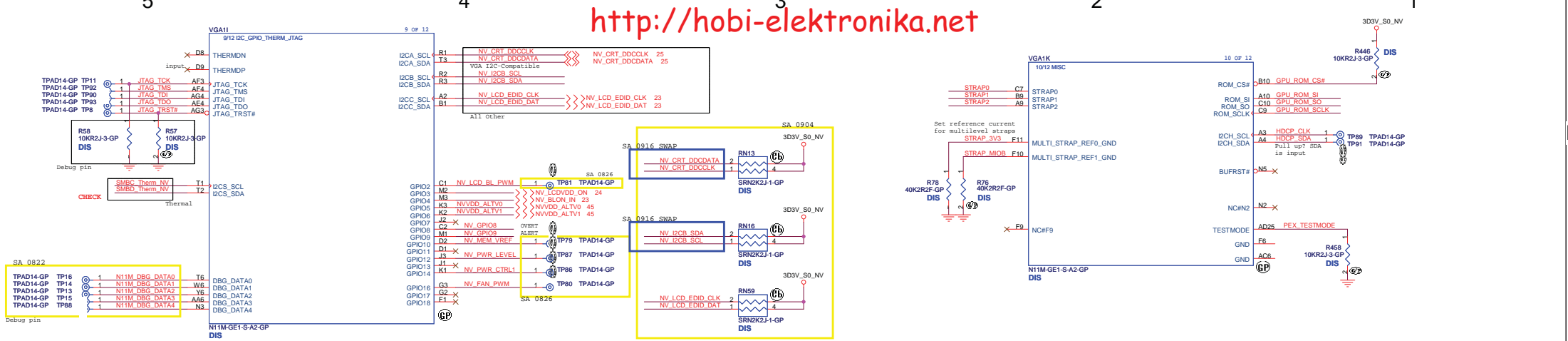


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Title 53 N11M(3/6) DAC		
Size	Document Number	Rev
Custom	LA46 MB DIS	-1
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Direct HDMI Connection



DeviceID

N11P-LM1 (0x0A2B) ?

N11M-GE1 (0x0A75) 1-0101

GPU_ROM_SI for Hynix VRAM

GPU_ROM_SI for Samsung VRAM

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

GPU_ROM_SI

GPU_ROM_SO

GPU_ROM_SCLK

GPU_ROM_SCLK

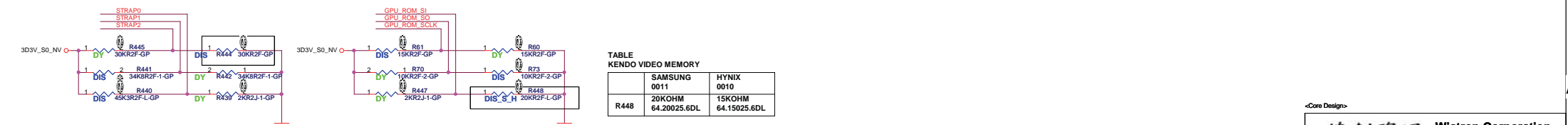


TABLE KENDO VIDEO MEMORY

	SAMSUNG	HYNIX
R448	64.20025.6DL	64.15025.6DL

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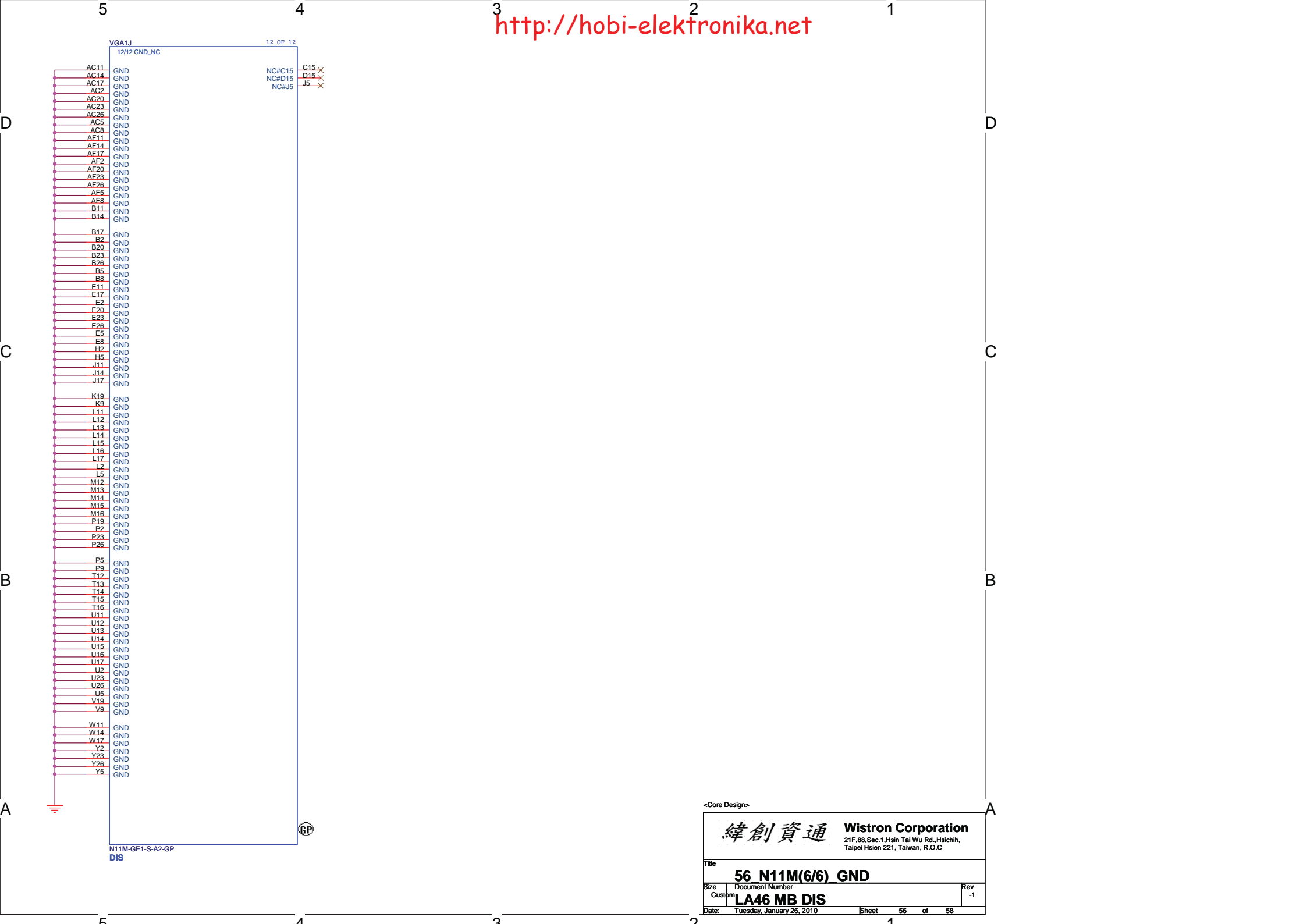
55 N11M(5/6) STRAP/ GPIO

LA46 MB DIS

Rev -1

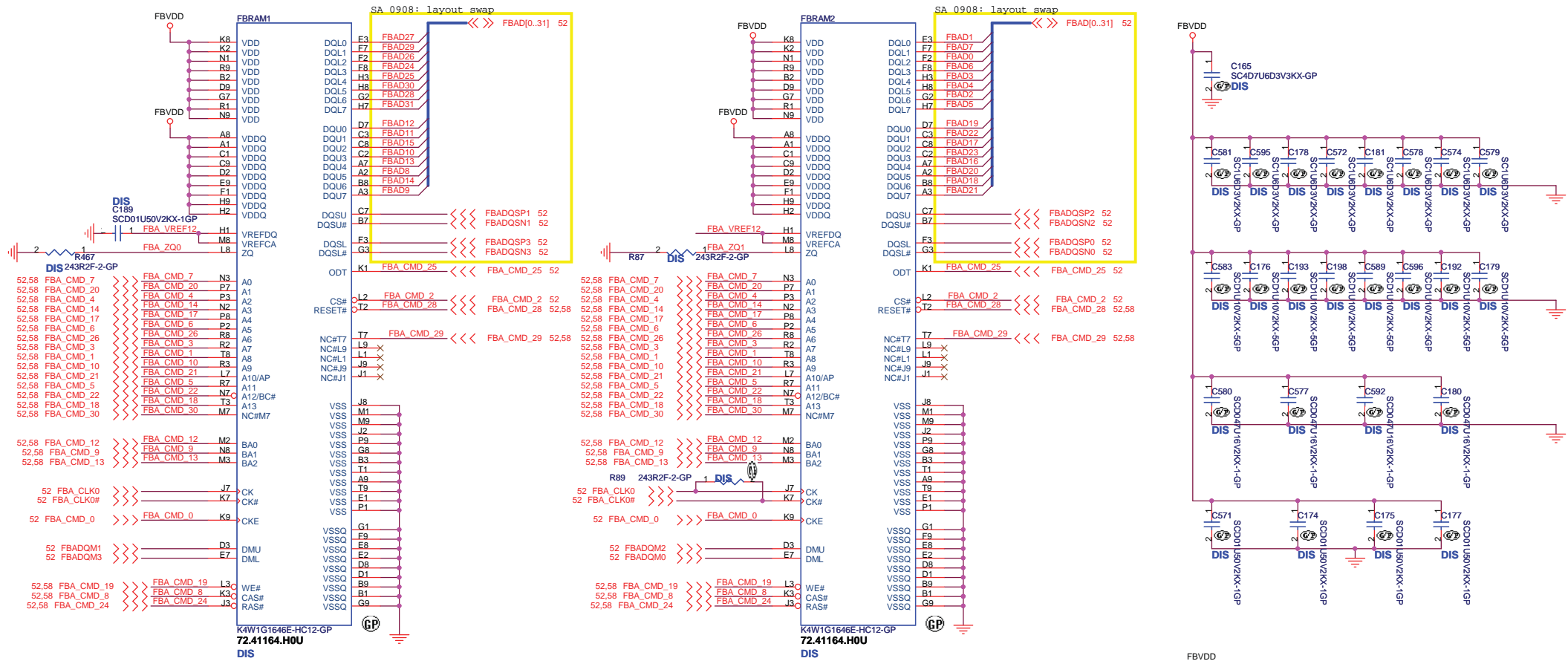
Date: Wednesday, January 27, 2010

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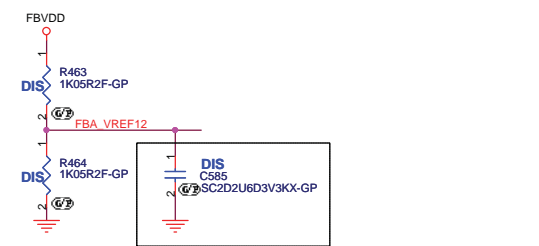


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緯創資通		Wistron Corporation	
		21F,88,Sec.1,Hsin,Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title			
56 N11M(6/6) GND			
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Custom	LA46 MB DIS		-1
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2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)



SB 1031 change to 78.22520.5BL

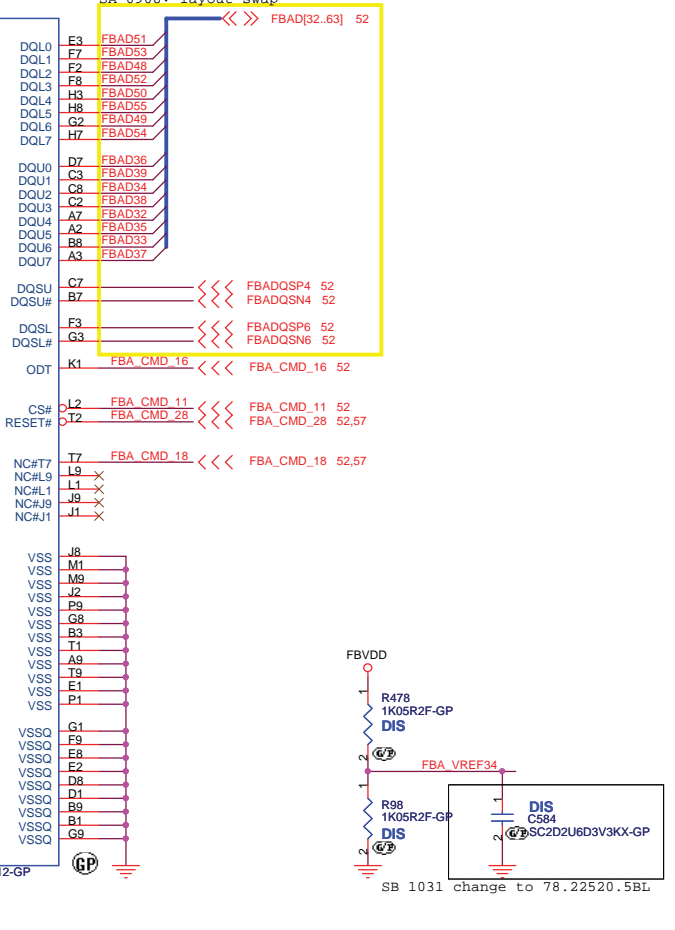
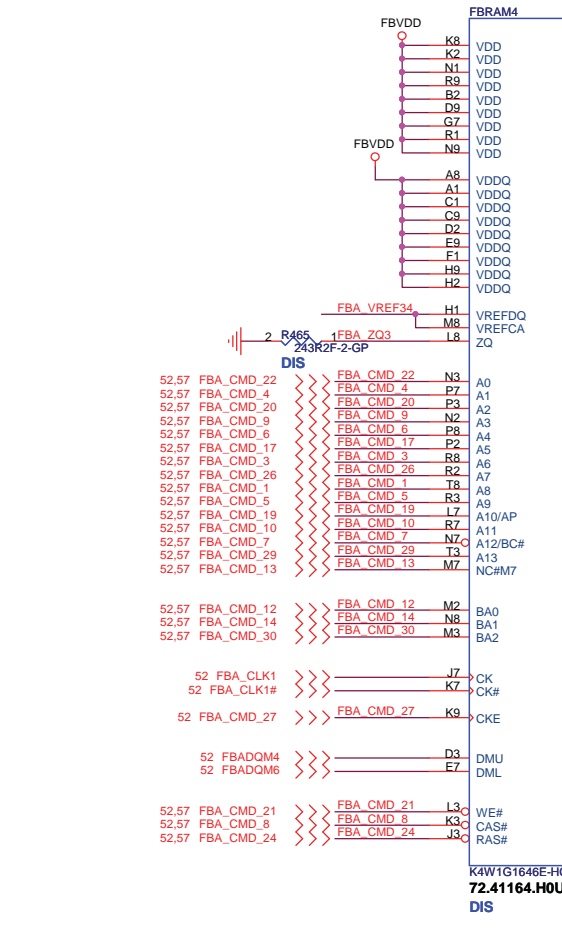
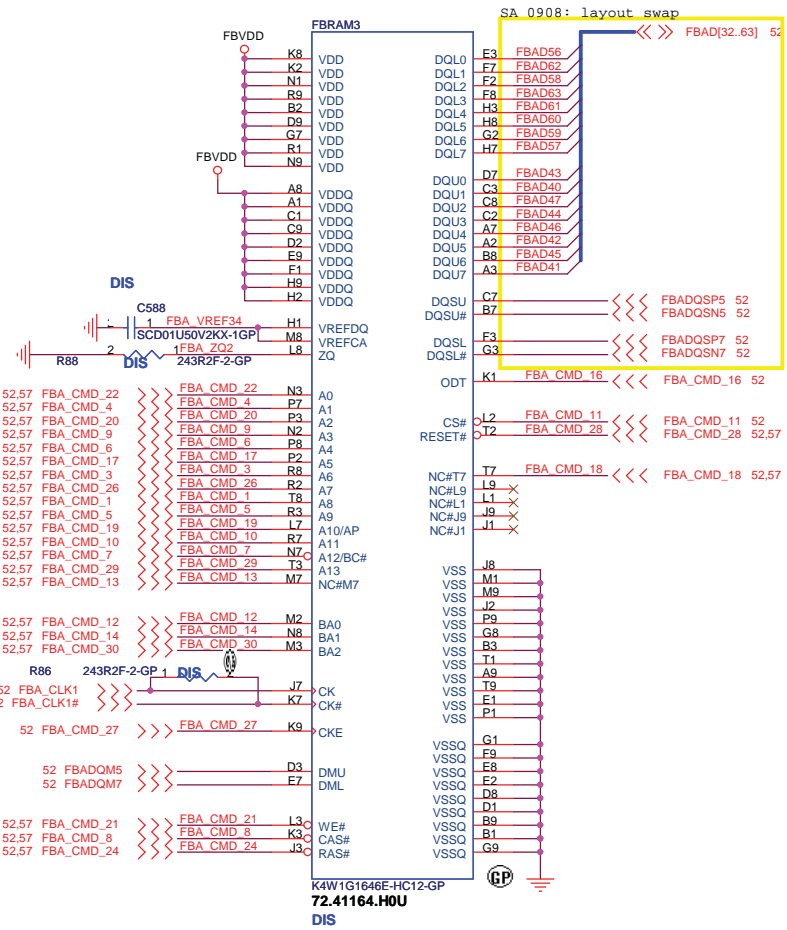
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緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C

Title: **57 VRAM(1/2)**

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

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File: **58 VRAM(2/2)**

Size: Custom Document Number
Customer: **LA46 MB DIS** Rev: -1

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