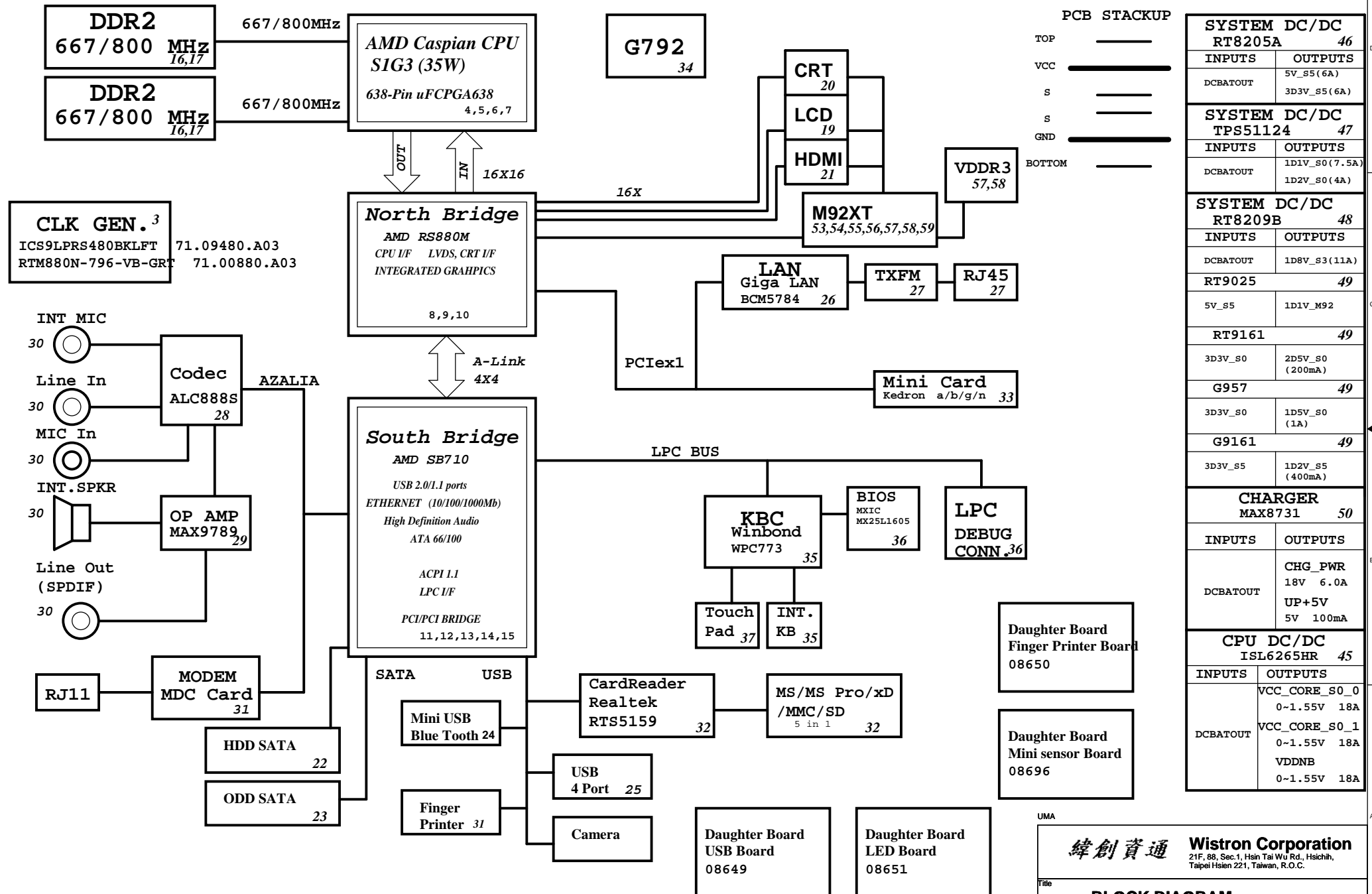


JV71-TR Block Diagram

Project code: 91.4FP01.001

PCB P/N : 48.4FP02.0SB

REVISION : 09243-SB



PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A)
	3D3V_S5(6A)
SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A)
	1D2V_S0(4A)
SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
RT9025 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0(200mA)
G957 49	
3D3V_S0	1D5V_S0(1A)
G9161 49	
3D3V_S5	1D2V_S5(400mA)
CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
	VCC_CORE_S0_0
	0~1.55V 18A
DCBATOUT	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A

5

4

3

2

1

D

D

C

C

B

B

A

A

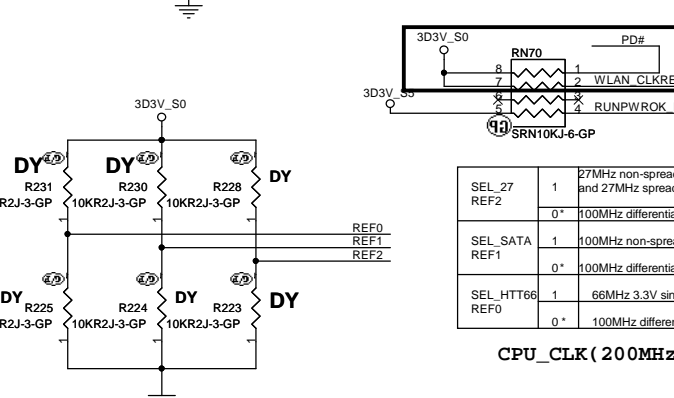
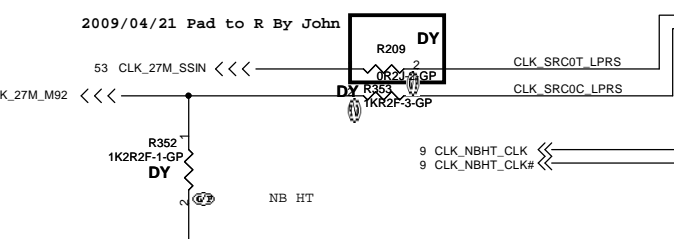
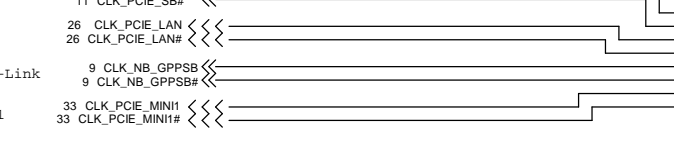
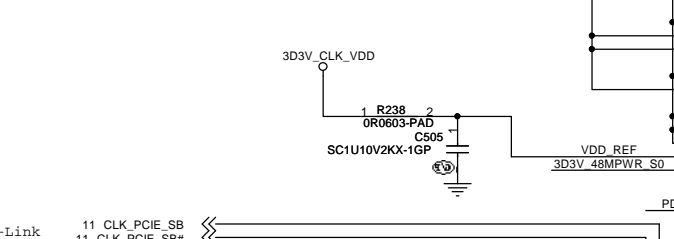
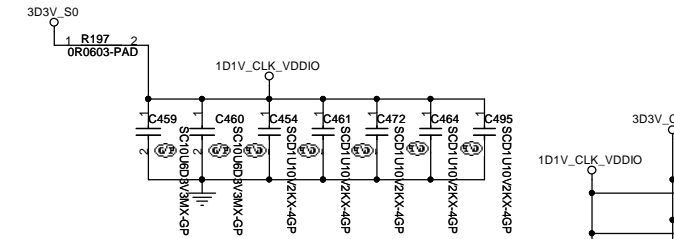
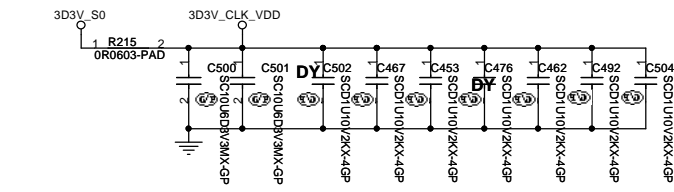
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Title
USB/PCIE Routing

Size A3	Document Number JV71-TR	Rev SA
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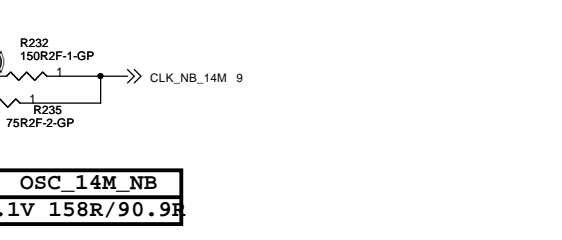
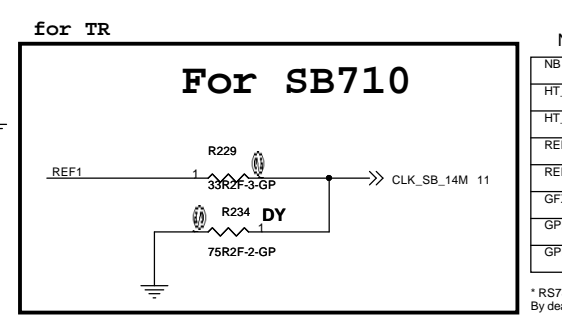
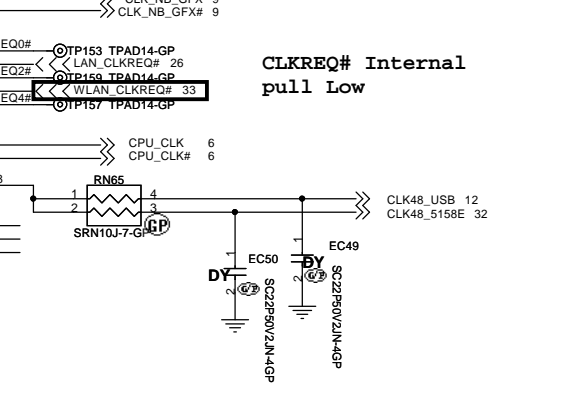
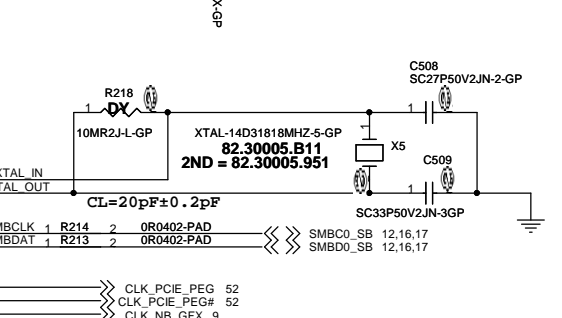
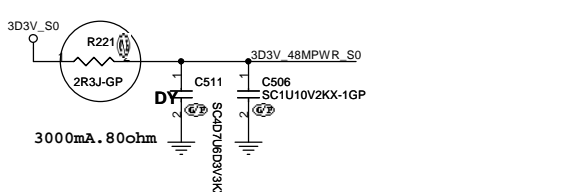
Date: Monday, July 06, 2009 Sheet 2 of 61



SEL_27	REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
		0*	100MHz differential spreading SRC clock
SEL_SATA	REF1	1	100MHz non-spreading differential SATA clock
		0*	100MHz differential spreading SRC clock
SEL_HTT66	REF0	1	66MHz 3.3V single ended HTT clock
		0*	100MHz differential HTT clock

CPU_CLK (200MHz)

OSC_14M_NB
RS780M 1.1V 158R/90.9R



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

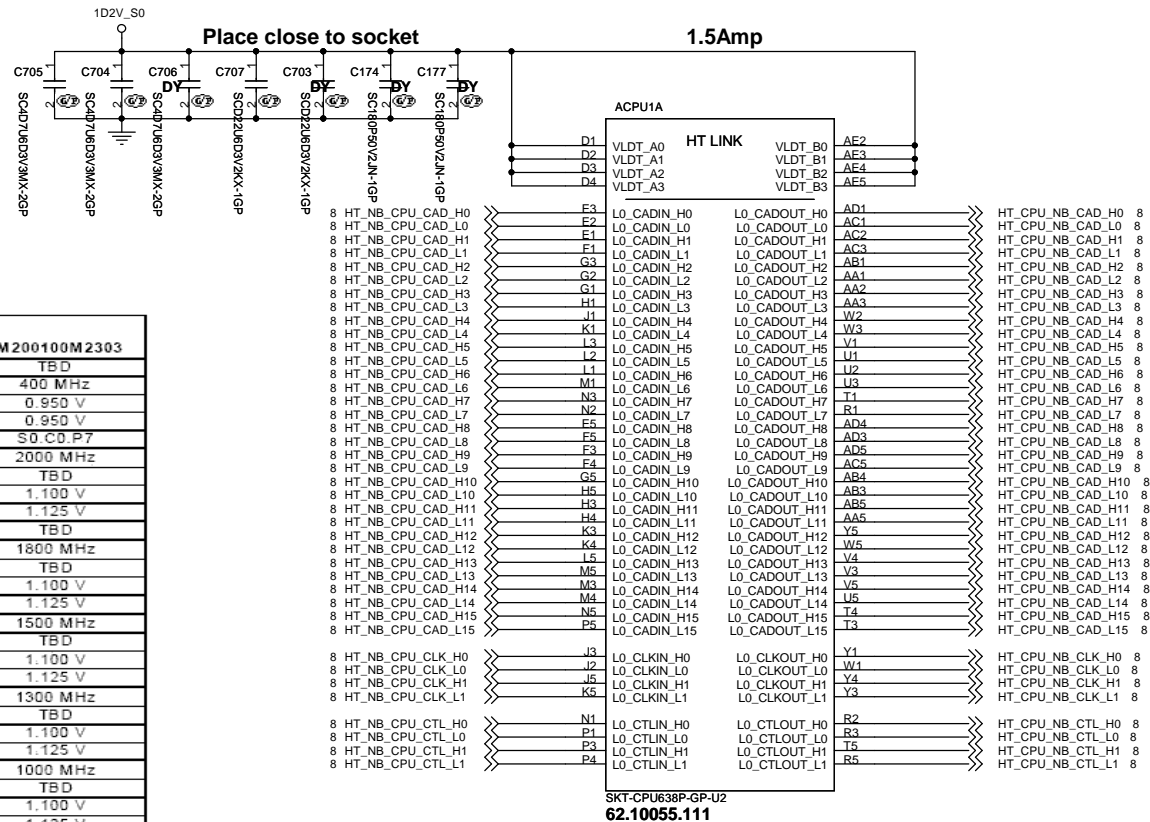
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Title: **CLKGEN ICS9LPRS480**

Size: **A3** Document Number: **JV71-TR** Rev: **SB**

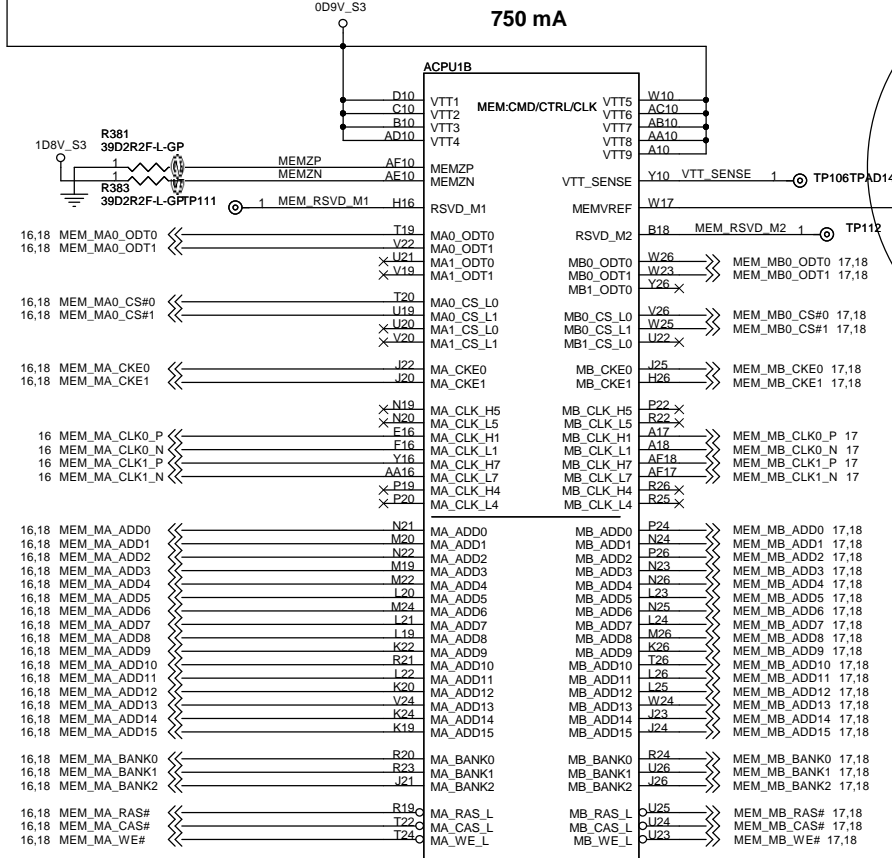
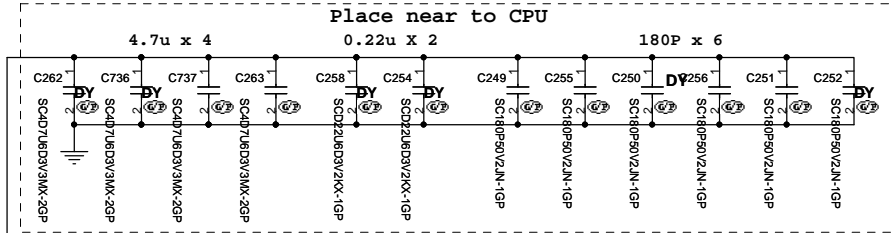
Date: **Monday, July 06, 2009** Sheet: **3** of **61**



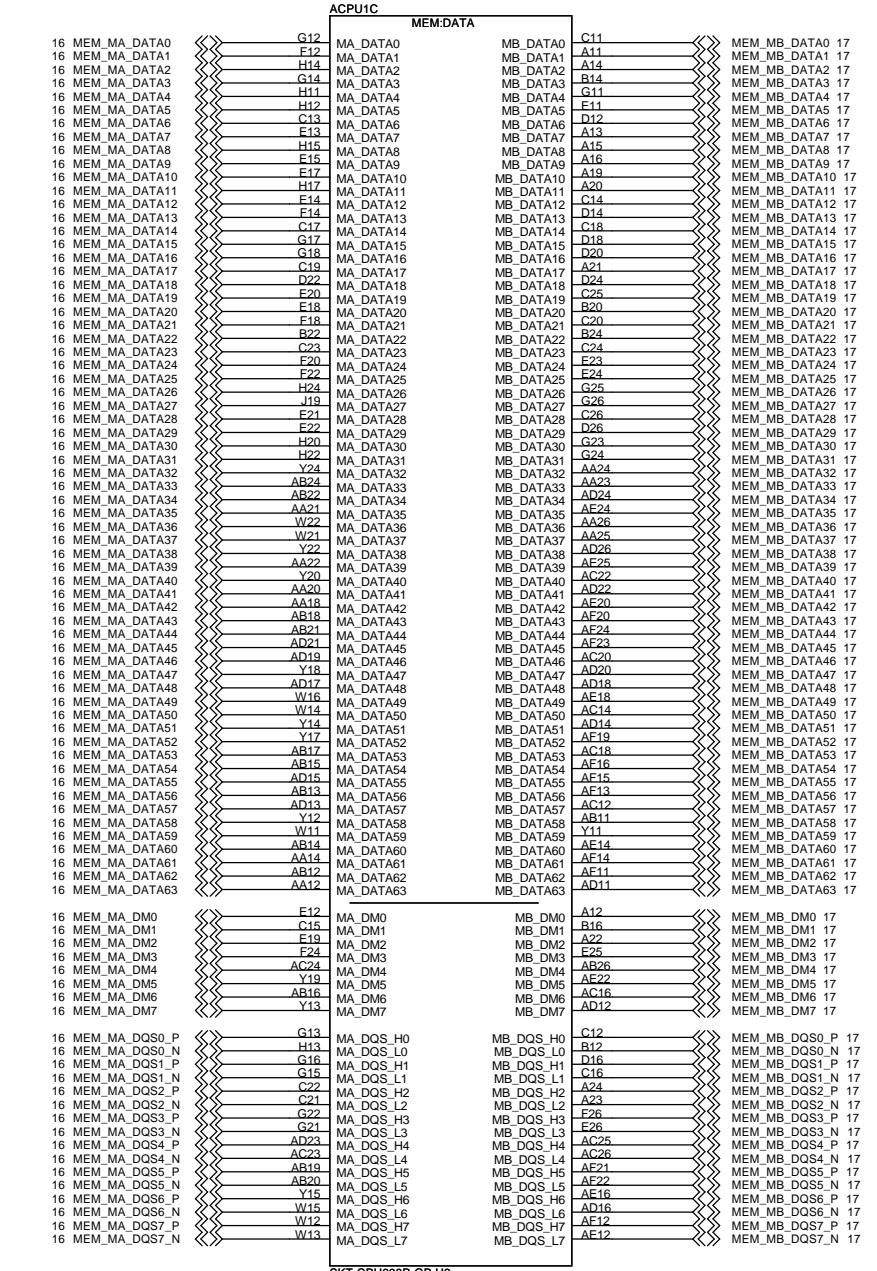
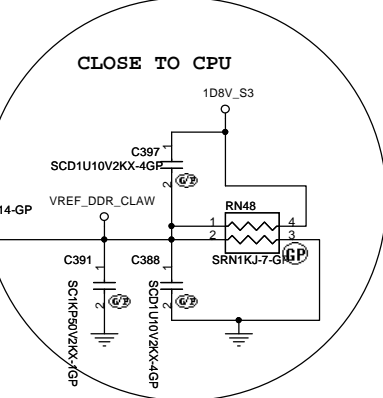
State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

- | | | | | | | |
|---------------------|----|--------------|---------------|-----|-------------------|---|
| 8 HT_NB_CPU_CAD_H0 | E3 | L0_CADIN_H0 | L0_CADOUT_H0 | AD1 | HT_CPU_NB_CAD_H0 | 8 |
| 8 HT_NB_CPU_CAD_L0 | E2 | L0_CADIN_L0 | L0_CADOUT_L0 | AC1 | HT_CPU_NB_CAD_L0 | 8 |
| 8 HT_NB_CPU_CAD_H1 | E1 | L0_CADIN_H1 | L0_CADOUT_H1 | AC2 | HT_CPU_NB_CAD_H1 | 8 |
| 8 HT_NB_CPU_CAD_L1 | F1 | L0_CADIN_L1 | L0_CADOUT_L1 | AC3 | HT_CPU_NB_CAD_L1 | 8 |
| 8 HT_NB_CPU_CAD_H2 | G3 | L0_CADIN_H2 | L0_CADOUT_H2 | AB1 | HT_CPU_NB_CAD_H2 | 8 |
| 8 HT_NB_CPU_CAD_L2 | G2 | L0_CADIN_L2 | L0_CADOUT_L2 | AA1 | HT_CPU_NB_CAD_L2 | 8 |
| 8 HT_NB_CPU_CAD_H3 | G1 | L0_CADIN_H3 | L0_CADOUT_H3 | AA2 | HT_CPU_NB_CAD_H3 | 8 |
| 8 HT_NB_CPU_CAD_L3 | H1 | L0_CADIN_L3 | L0_CADOUT_L3 | AA3 | HT_CPU_NB_CAD_L3 | 8 |
| 8 HT_NB_CPU_CAD_H4 | J1 | L0_CADIN_H4 | L0_CADOUT_H4 | W2 | HT_CPU_NB_CAD_H4 | 8 |
| 8 HT_NB_CPU_CAD_L4 | K1 | L0_CADIN_L4 | L0_CADOUT_L4 | W3 | HT_CPU_NB_CAD_L4 | 8 |
| 8 HT_NB_CPU_CAD_H5 | L3 | L0_CADIN_H5 | L0_CADOUT_H5 | V1 | HT_CPU_NB_CAD_H5 | 8 |
| 8 HT_NB_CPU_CAD_L5 | L2 | L0_CADIN_L5 | L0_CADOUT_L5 | U1 | HT_CPU_NB_CAD_L5 | 8 |
| 8 HT_NB_CPU_CAD_H6 | L1 | L0_CADIN_H6 | L0_CADOUT_H6 | U2 | HT_CPU_NB_CAD_H6 | 8 |
| 8 HT_NB_CPU_CAD_L6 | M1 | L0_CADIN_L6 | L0_CADOUT_L6 | U3 | HT_CPU_NB_CAD_L6 | 8 |
| 8 HT_NB_CPU_CAD_H7 | N3 | L0_CADIN_H7 | L0_CADOUT_H7 | T1 | HT_CPU_NB_CAD_H7 | 8 |
| 8 HT_NB_CPU_CAD_L7 | N2 | L0_CADIN_L7 | L0_CADOUT_L7 | R1 | HT_CPU_NB_CAD_L7 | 8 |
| 8 HT_NB_CPU_CAD_H8 | E5 | L0_CADIN_H8 | L0_CADOUT_H8 | AD4 | HT_CPU_NB_CAD_H8 | 8 |
| 8 HT_NB_CPU_CAD_L8 | E6 | L0_CADIN_L8 | L0_CADOUT_L8 | AD3 | HT_CPU_NB_CAD_L8 | 8 |
| 8 HT_NB_CPU_CAD_H9 | E3 | L0_CADIN_H9 | L0_CADOUT_H9 | AC5 | HT_CPU_NB_CAD_H9 | 8 |
| 8 HT_NB_CPU_CAD_L9 | F4 | L0_CADIN_L9 | L0_CADOUT_L9 | AB4 | HT_CPU_NB_CAD_L9 | 8 |
| 8 HT_NB_CPU_CAD_H10 | G5 | L0_CADIN_H10 | L0_CADOUT_H10 | AB3 | HT_CPU_NB_CAD_H10 | 8 |
| 8 HT_NB_CPU_CAD_L10 | H5 | L0_CADIN_L10 | L0_CADOUT_L10 | AB5 | HT_CPU_NB_CAD_L10 | 8 |
| 8 HT_NB_CPU_CAD_H11 | H3 | L0_CADIN_H11 | L0_CADOUT_H11 | AA5 | HT_CPU_NB_CAD_H11 | 8 |
| 8 HT_NB_CPU_CAD_L11 | H4 | L0_CADIN_L11 | L0_CADOUT_L11 | AA6 | HT_CPU_NB_CAD_L11 | 8 |
| 8 HT_NB_CPU_CAD_H12 | K3 | L0_CADIN_H12 | L0_CADOUT_H12 | W5 | HT_CPU_NB_CAD_H12 | 8 |
| 8 HT_NB_CPU_CAD_L12 | K4 | L0_CADIN_L12 | L0_CADOUT_L12 | W4 | HT_CPU_NB_CAD_L12 | 8 |
| 8 HT_NB_CPU_CAD_H13 | L5 | L0_CADIN_H13 | L0_CADOUT_H13 | V3 | HT_CPU_NB_CAD_H13 | 8 |
| 8 HT_NB_CPU_CAD_L13 | M3 | L0_CADIN_L13 | L0_CADOUT_L13 | V5 | HT_CPU_NB_CAD_L13 | 8 |
| 8 HT_NB_CPU_CAD_H14 | M5 | L0_CADIN_H14 | L0_CADOUT_H14 | U5 | HT_CPU_NB_CAD_H14 | 8 |
| 8 HT_NB_CPU_CAD_L14 | M4 | L0_CADIN_L14 | L0_CADOUT_L14 | U6 | HT_CPU_NB_CAD_L14 | 8 |
| 8 HT_NB_CPU_CAD_H15 | N5 | L0_CADIN_H15 | L0_CADOUT_H15 | T4 | HT_CPU_NB_CAD_H15 | 8 |
| 8 HT_NB_CPU_CAD_L15 | P5 | L0_CADIN_L15 | L0_CADOUT_L15 | T3 | HT_CPU_NB_CAD_L15 | 8 |
| 8 HT_NB_CPU_CLK_H0 | J3 | L0_CLKIN_H0 | L0_CLKOUT_H0 | Y1 | HT_CPU_NB_CLK_H0 | 8 |
| 8 HT_NB_CPU_CLK_L0 | J2 | L0_CLKIN_L0 | L0_CLKOUT_L0 | W1 | HT_CPU_NB_CLK_L0 | 8 |
| 8 HT_NB_CPU_CLK_H1 | J5 | L0_CLKIN_H1 | L0_CLKOUT_H1 | Y4 | HT_CPU_NB_CLK_H1 | 8 |
| 8 HT_NB_CPU_CLK_L1 | K5 | L0_CLKIN_L1 | L0_CLKOUT_L1 | Y3 | HT_CPU_NB_CLK_L1 | 8 |
| 8 HT_NB_CPU_CTL_H0 | N1 | L0_CTLIN_H0 | L0_CTLOUT_H0 | R2 | HT_CPU_NB_CTL_H0 | 8 |
| 8 HT_NB_CPU_CTL_L0 | P1 | L0_CTLIN_L0 | L0_CTLOUT_L0 | R3 | HT_CPU_NB_CTL_L0 | 8 |
| 8 HT_NB_CPU_CTL_H1 | P3 | L0_CTLIN_H1 | L0_CTLOUT_H1 | T5 | HT_CPU_NB_CTL_H1 | 8 |
| 8 HT_NB_CPU_CTL_L1 | P4 | L0_CTLIN_L1 | L0_CTLOUT_L1 | R5 | HT_CPU_NB_CTL_L1 | 8 |

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62.10055.111
SKT-BGA638H176



SKT-CPU638P-GP-U2
62.10055.111



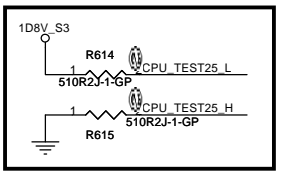
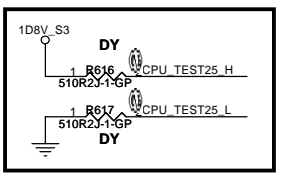
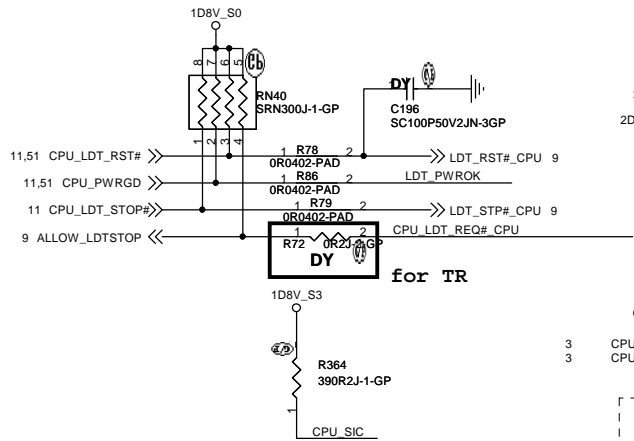
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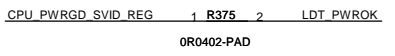
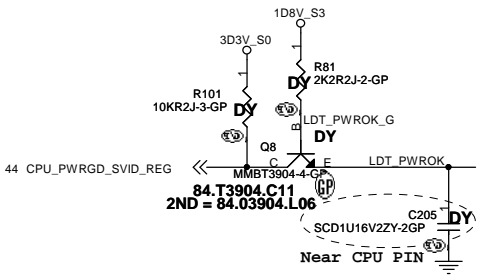
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Title			CPU DDR (2/4)		
Size	Document Number	Rev			
A3	JV71-TR	SA			
Date:	Monday, July 06, 2009	Sheet	5	of	61

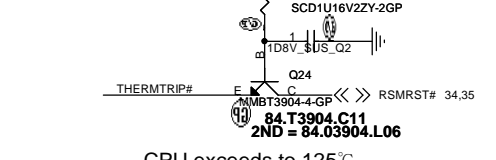
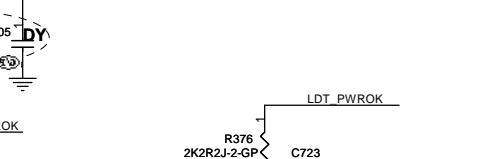
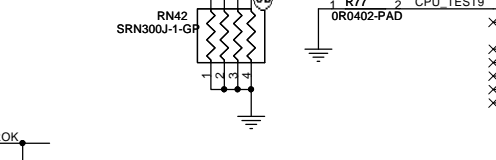
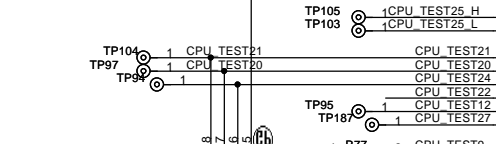
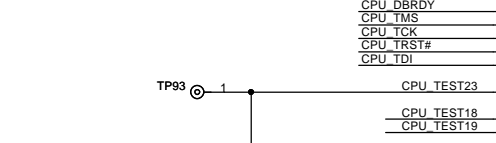
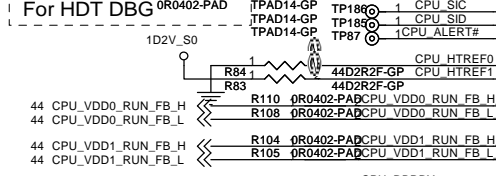
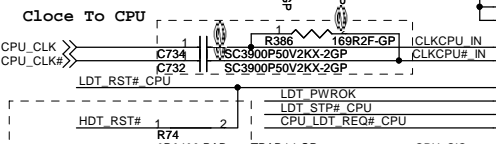
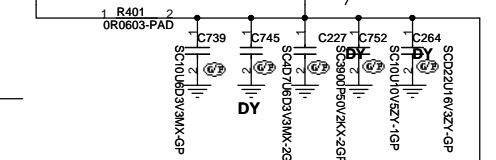
The Processor has reached a preset maximum operating temperature. 100°C
 I=Active HTC
 O=FAN



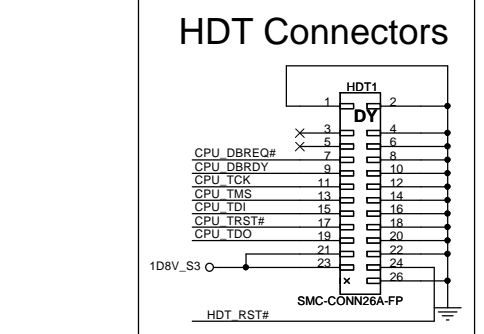
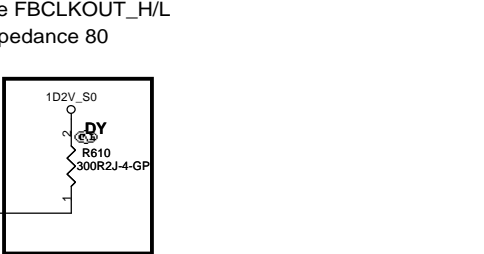
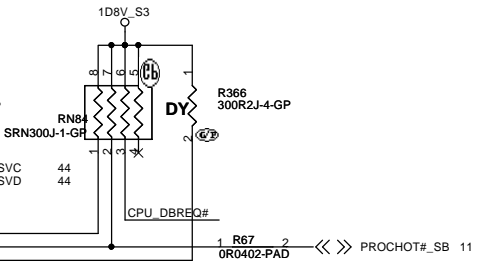
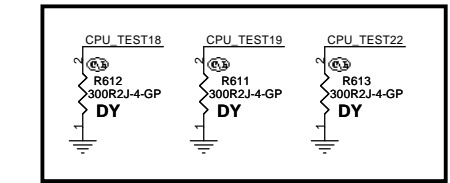
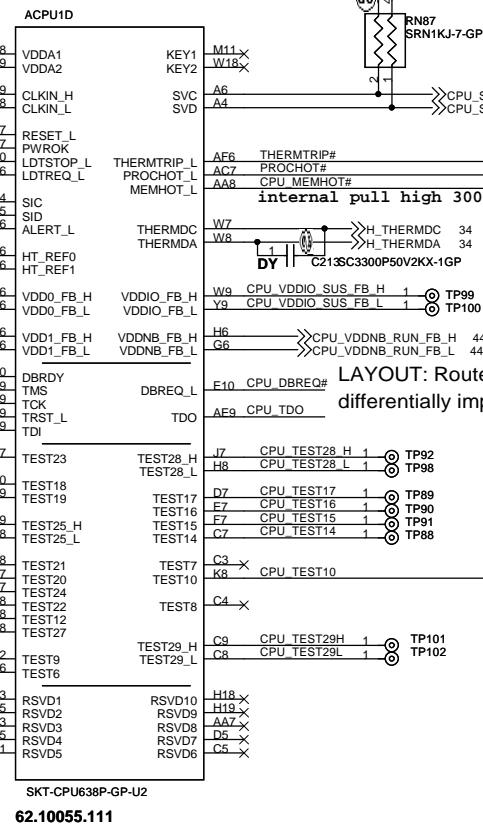
for TR



IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
 LAYOUT:ROUTE VDDA TRACE APPROX.
 50mils WIDE(USE 2X25 mil TRACES TO
 EXIT BALL FIELD) AND 500 mils LONG.



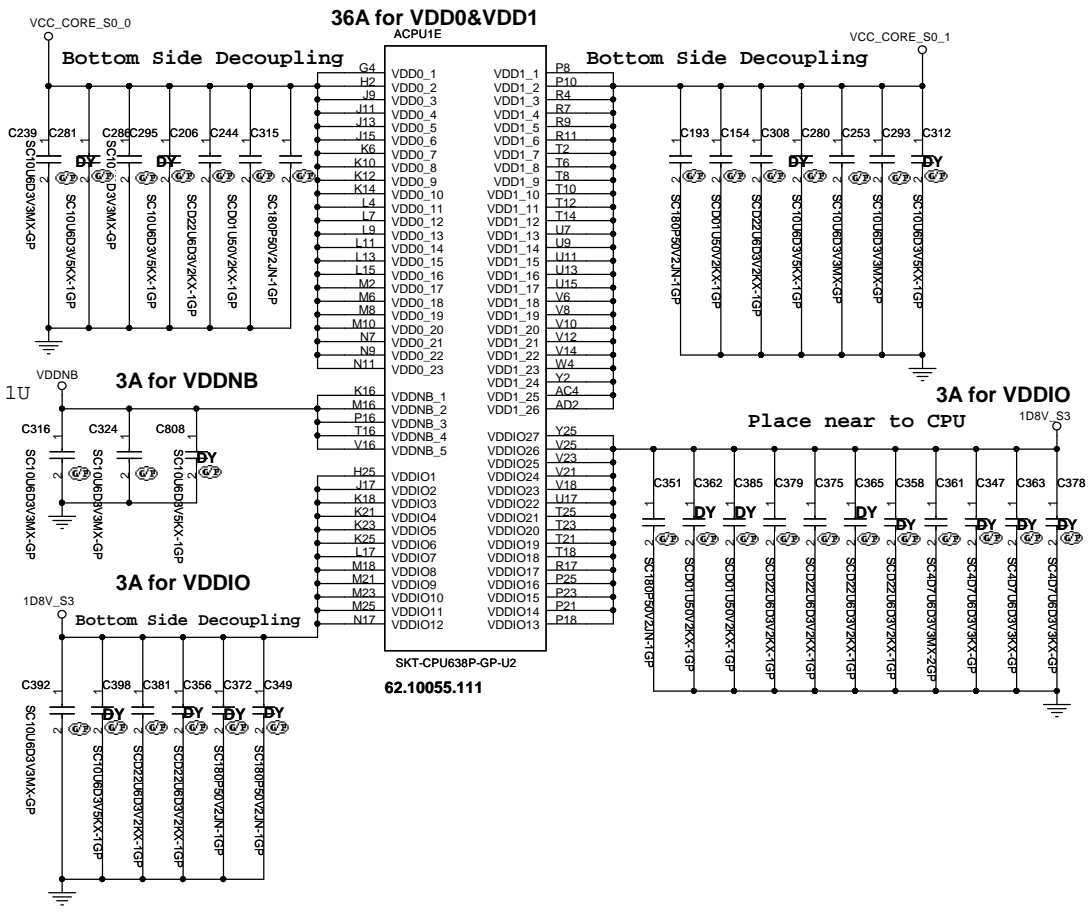
CPU exceeds to 125°C

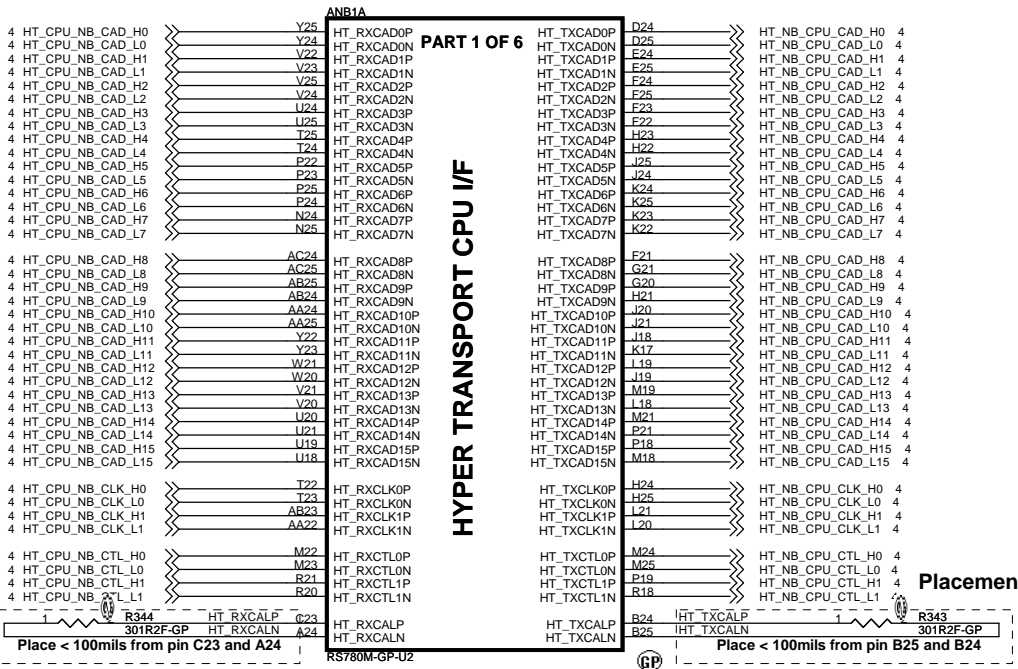


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ACPU1F		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA13	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB2	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AB25	VSS11	VSS76
AC11	VSS12	VSS77
AC13	VSS13	VSS78
AC15	VSS14	VSS79
AC19	VSS15	VSS80
AC21	VSS16	VSS81
AC17	VSS17	VSS82
AD6	VSS18	VSS83
AD8	VSS19	VSS84
AD25	VSS20	VSS85
AE11	VSS21	VSS86
AE13	VSS22	VSS87
AE15	VSS23	VSS88
AE17	VSS24	VSS89
AE19	VSS25	VSS90
AE21	VSS26	VSS91
AE23	VSS27	VSS92
AE11	VSS28	VSS93
B6	VSS29	VSS94
BR	VSS30	VSS95
B9	VSS31	VSS96
B11	VSS32	VSS97
B12	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B19	VSS36	VSS101
B21	VSS37	VSS102
B23	VSS38	VSS103
B25	VSS39	VSS104
D6	VSS40	VSS105
D8	VSS41	VSS106
D9	VSS42	VSS107
D11	VSS43	VSS108
D13	VSS44	VSS109
D15	VSS45	VSS110
D17	VSS46	VSS111
D19	VSS47	VSS112
D21	VSS48	VSS113
D23	VSS49	VSS114
D25	VSS50	VSS115
E4	VSS51	VSS116
E2	VSS52	VSS117
E11	VSS53	VSS118
E13	VSS54	VSS119
F15	VSS55	VSS120
F17	VSS56	VSS121
F19	VSS57	VSS122
F21	VSS58	VSS123
F23	VSS59	VSS124
F25	VSS60	VSS125
H7	VSS61	VSS126
H9	VSS62	VSS127
H21	VSS63	VSS128
H23	VSS64	VSS129
J4	VSS65	

SKT-CPU638P-GP-U2
62.10055.111

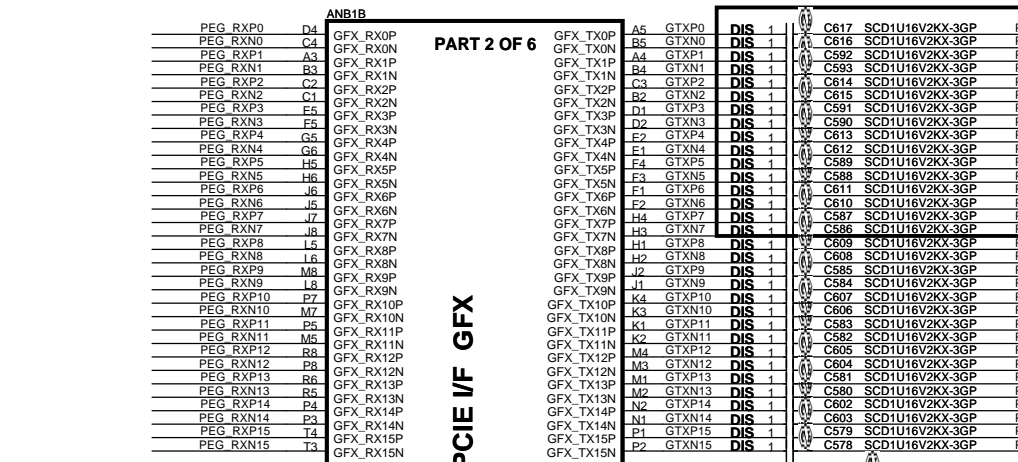




RS780 SYMBOL

Placement: close RS780

Placement: close RS780



PEG_TXP[15..0] 52
PEG_TXN[15..0] 52

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

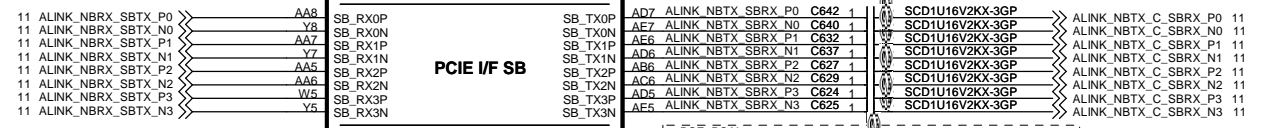
GTXP0	LIMA	C30	1	SCD1U16V2KX-3GP	HDMI DATA2+	2
GTXP0	LIMA	C29	1	SCD1U16V2KX-3GP	HDMI DATA1+	2
GTXP1	LIMA	C27	1	SCD1U16V2KX-3GP	HDMI DATA1-	2
GTXP1	LIMA	C26	1	SCD1U16V2KX-3GP	HDMI DATA1-	2
GTXP2	LIMA	C25	1	SCD1U16V2KX-3GP	HDMI DATA0+	2
GTXP2	LIMA	C22	1	SCD1U16V2KX-3GP	HDMI DATA0-	2
GTXP3	LIMA	C21	1	SCD1U16V2KX-3GP	HDMI_CLK+	21
GTXP3	LIMA	C19	1	SCD1U16V2KX-3GP	HDMI_CLK-	21

for TR

LAN 26
MINICARD1 33

LAN 26
MINICARD1 33

A-LINK

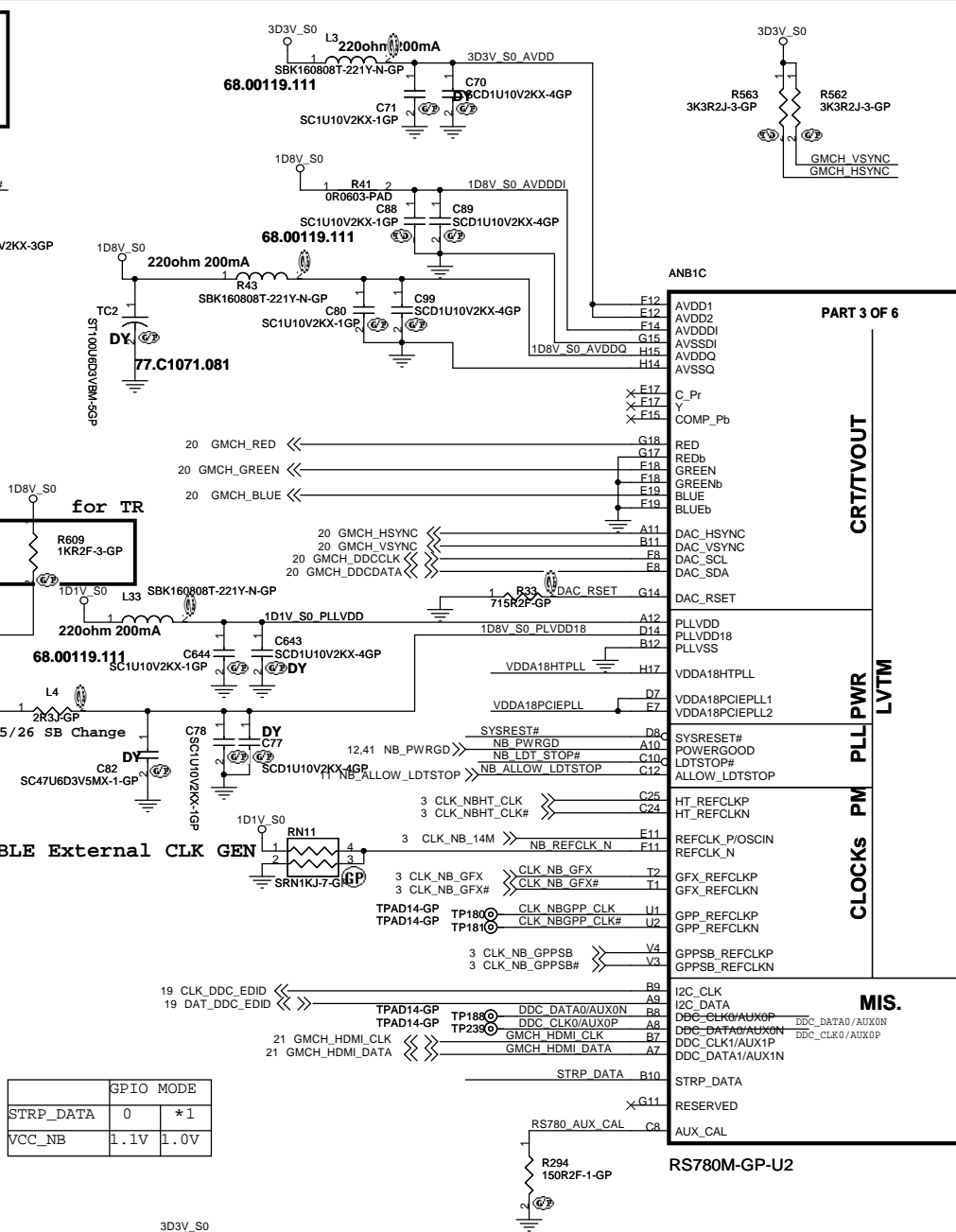
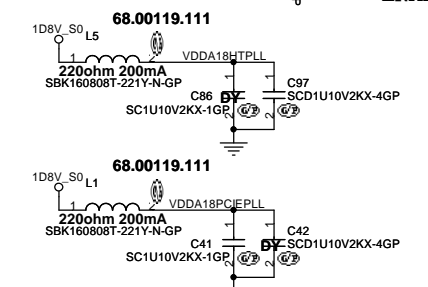
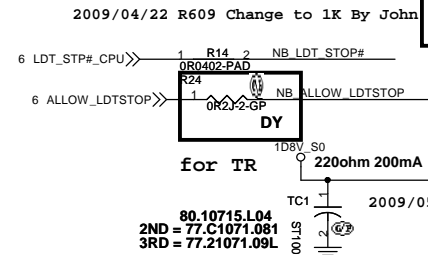
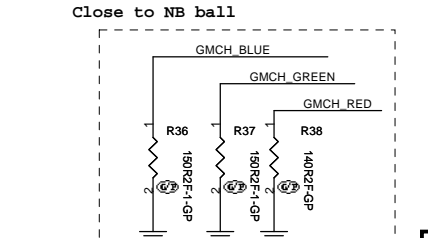
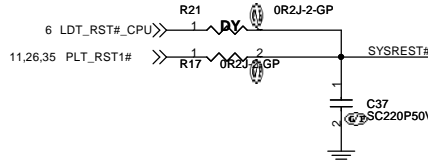


Place < 100mils from pin AC8 and AB8

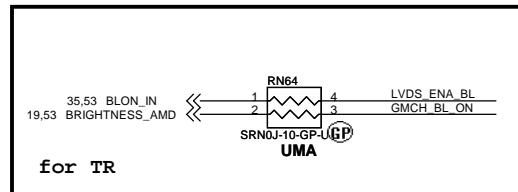
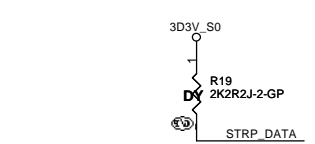
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title ATI-RS880M_HT LINK&PCIE(1/3)		
Size A3	Document Number JV71-TR	Rev SA
Date Monday, July 06, 2009	Sheet 8	of 61

NB_PWRGD
Reserve for DY
EMI
0408



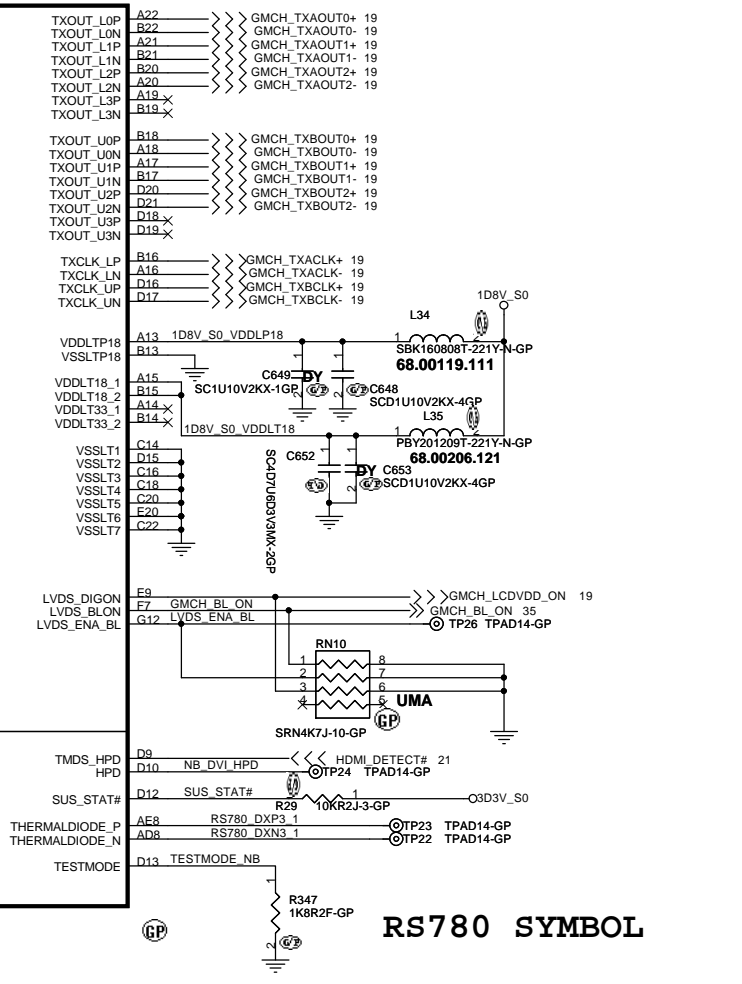
GPIO MODE	
STRP_DATA	*1
VCC_NB	1.1V 1.0V



STRAP_DEBUG_BUS_GPIO_ENABLEB
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS from EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected



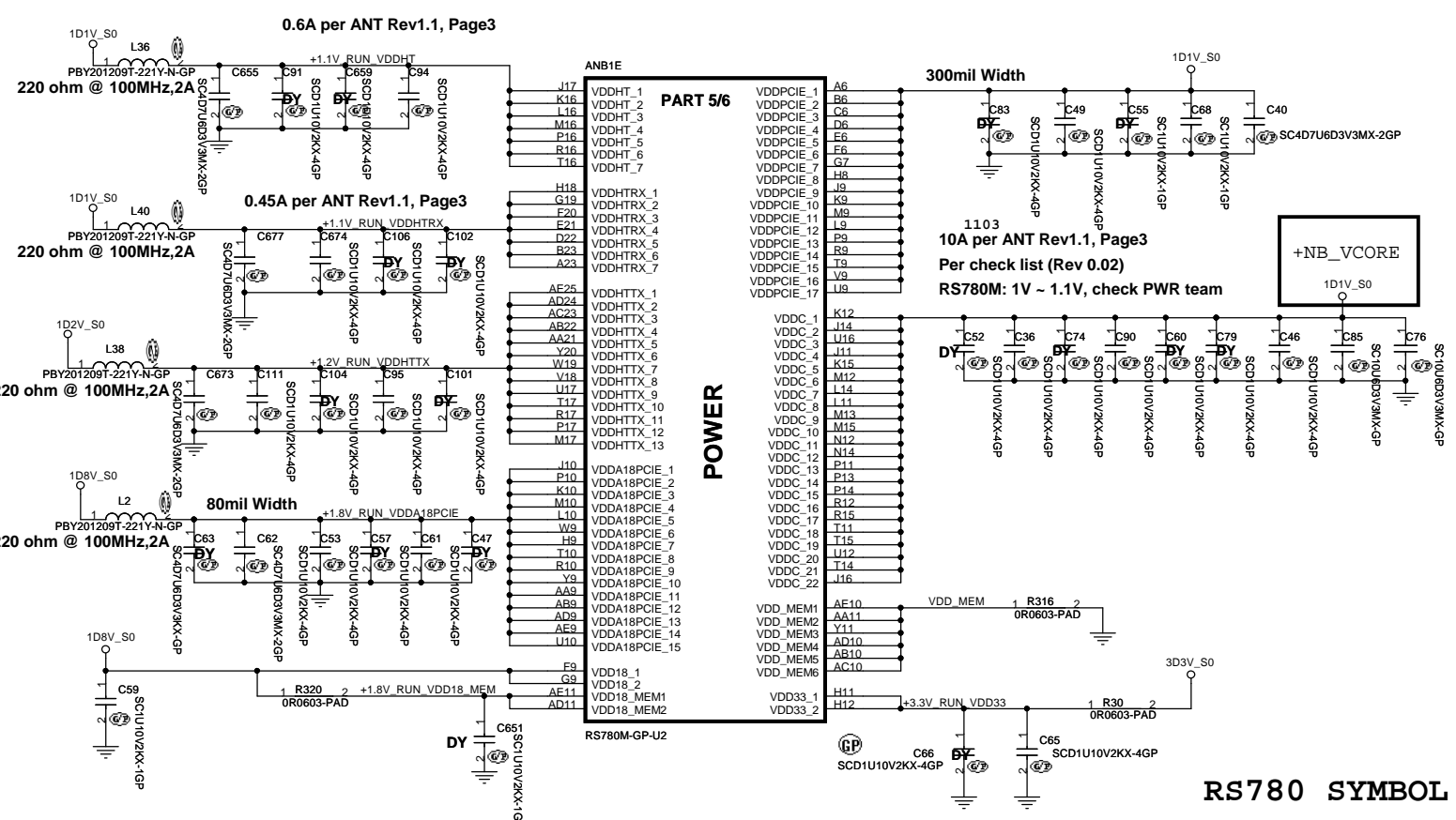
UMA

緯創資通 Wistron Corporation
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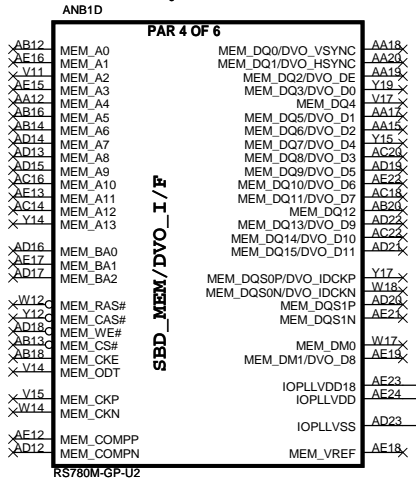
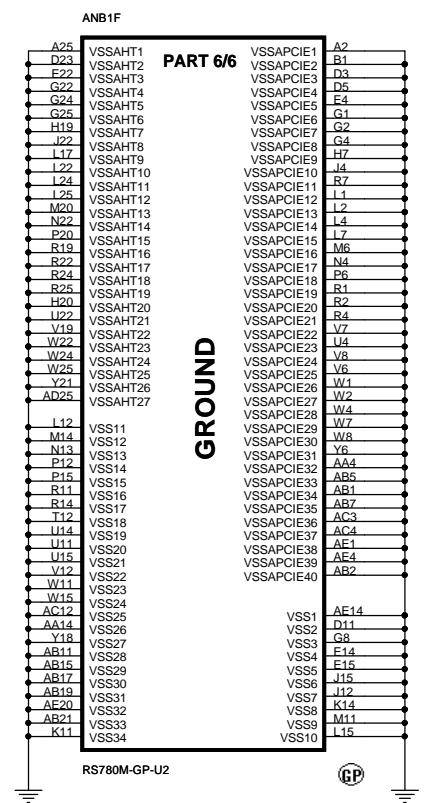
Title: **ATI-RS880M LVDS&CRT (2/3)**

Size A3 Document Number **JV71-TR** Rev SA

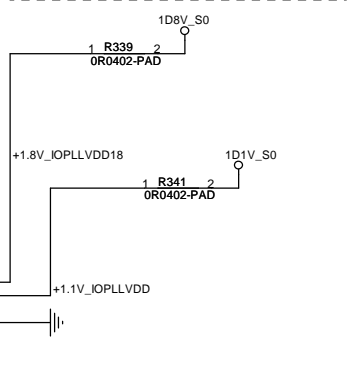
Date: Monday, July 06, 2009 Sheet 9 of 61



RS780 SYMBOL



MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions



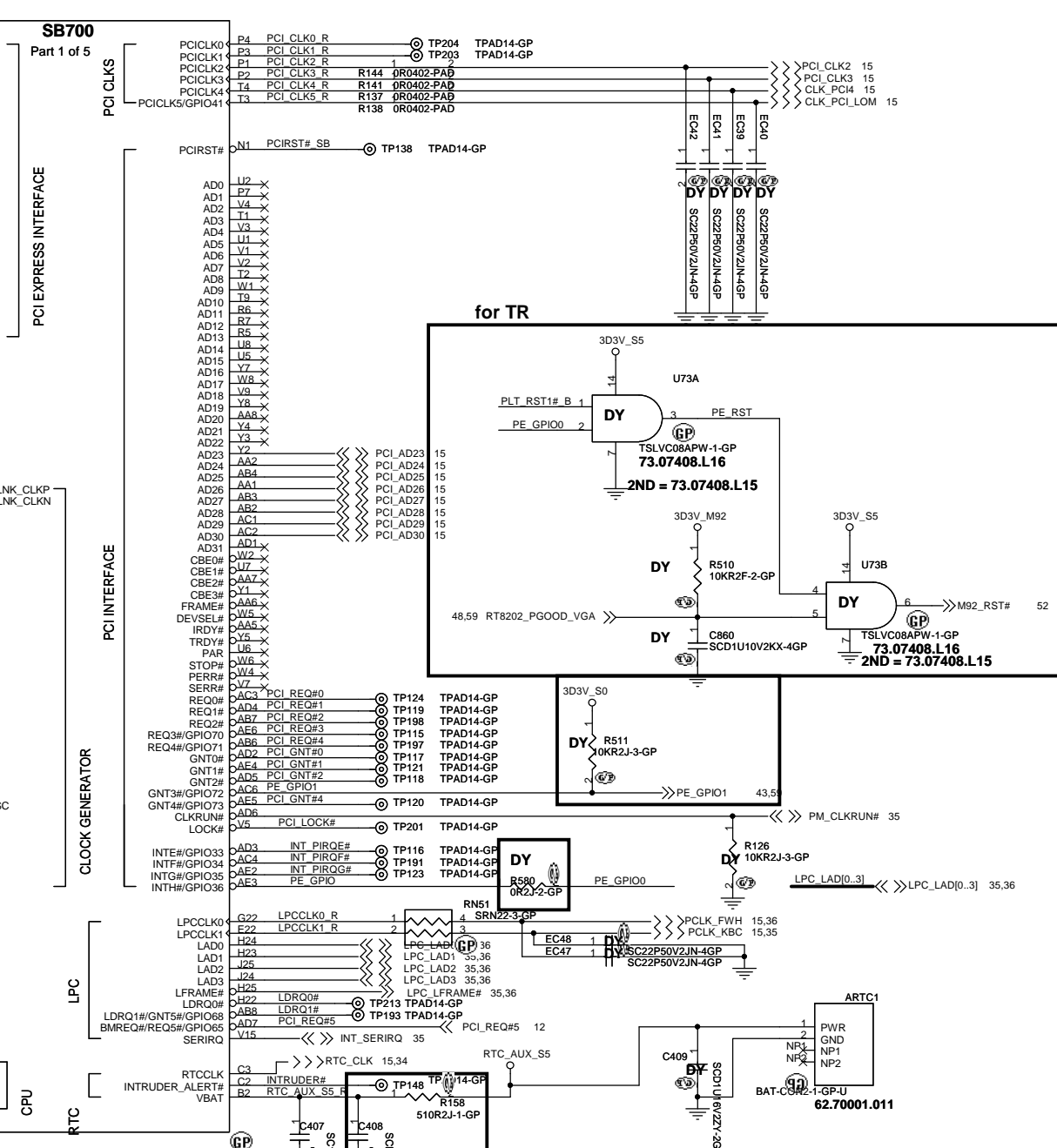
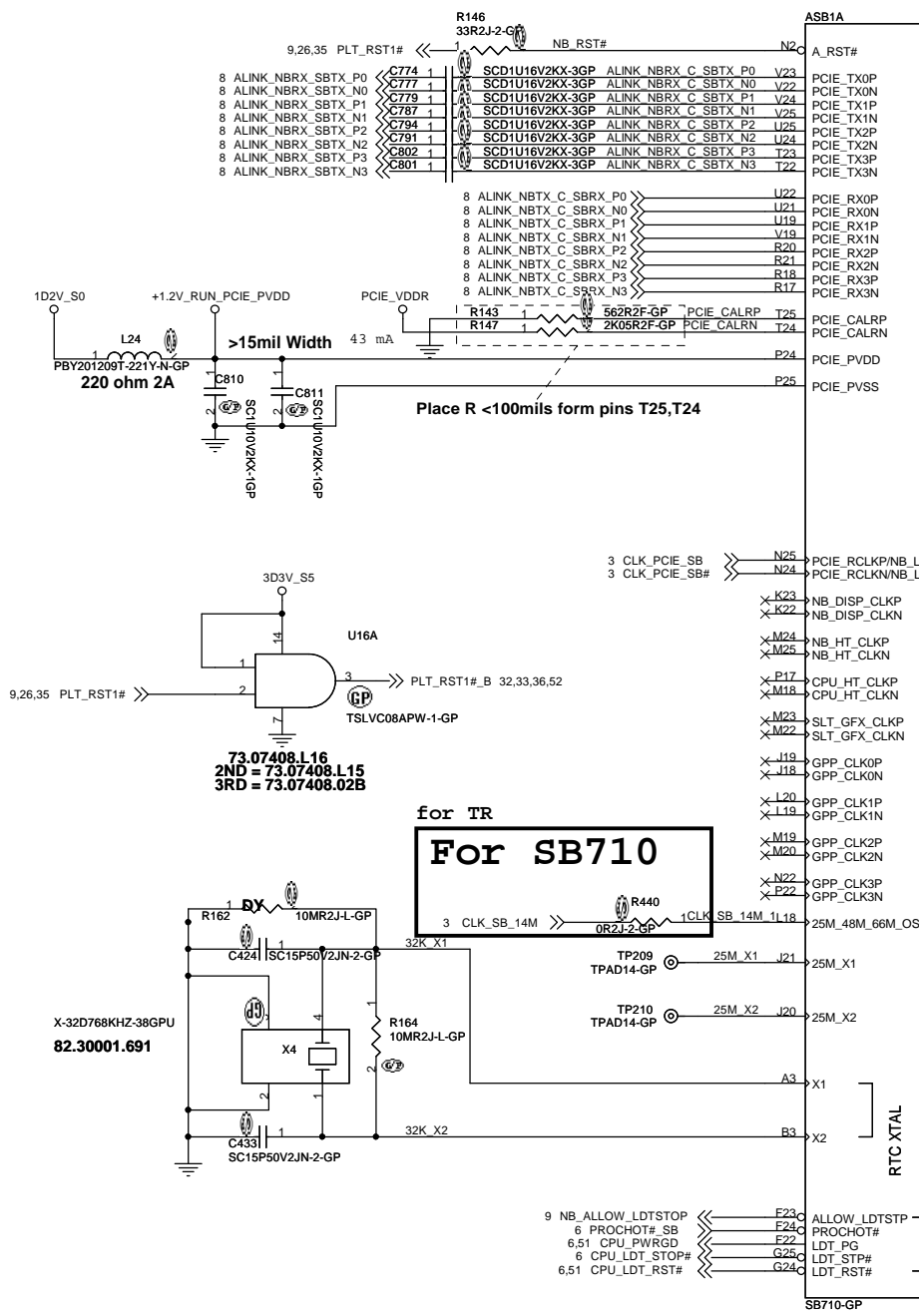
UMA

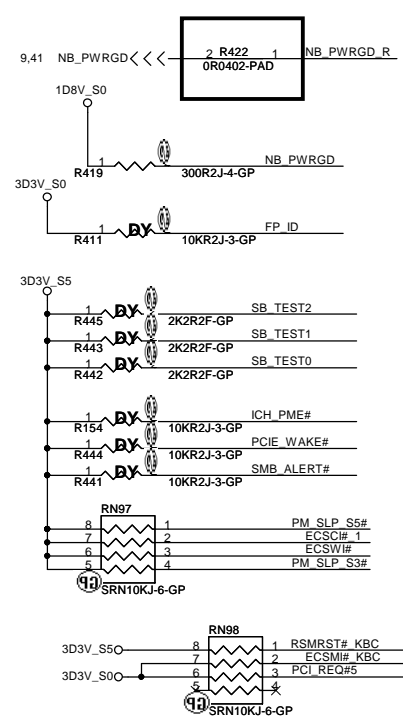
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Ati-RS880M Side Port&PWR&GND(3/3)**

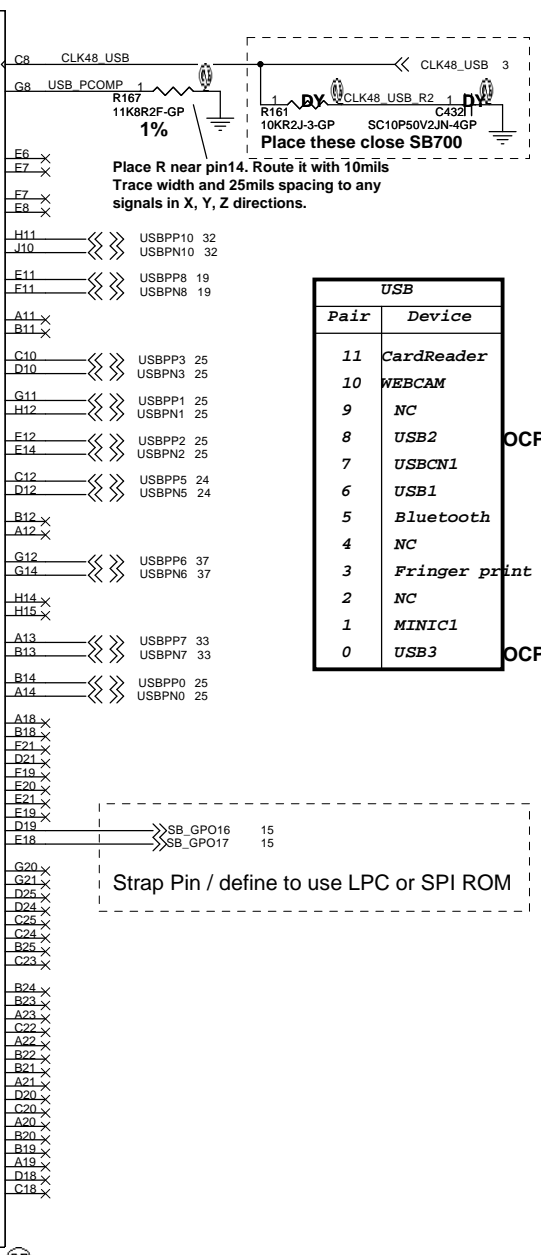
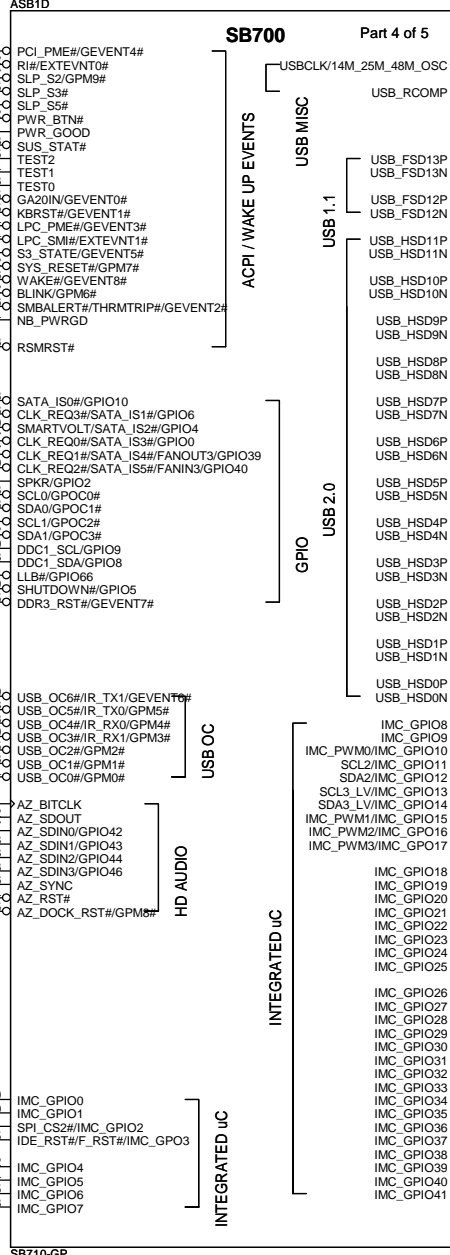
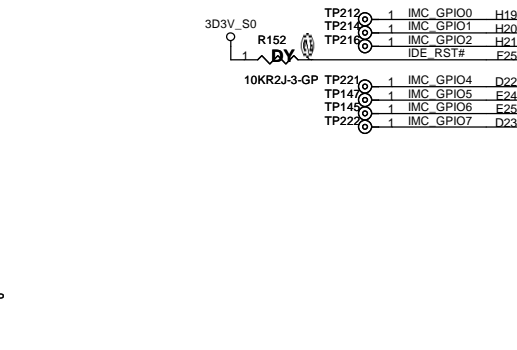
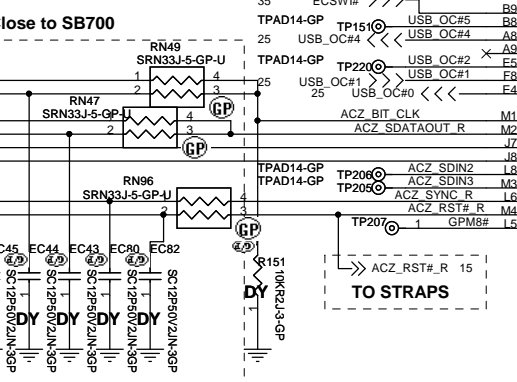
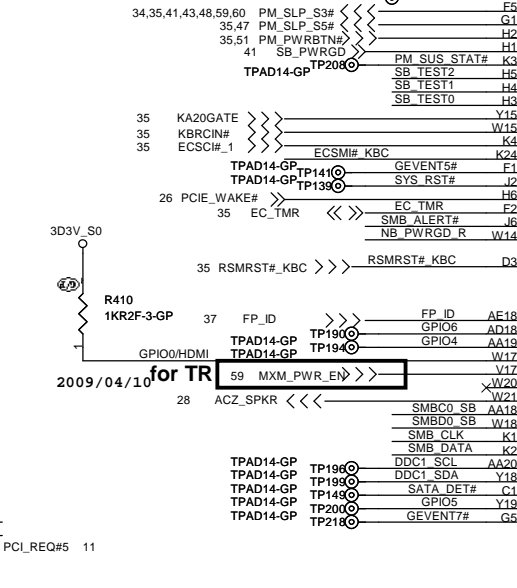
Size: A3 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 06, 2009 Sheet 10 of 61





Reserve for DY
EMI
0408

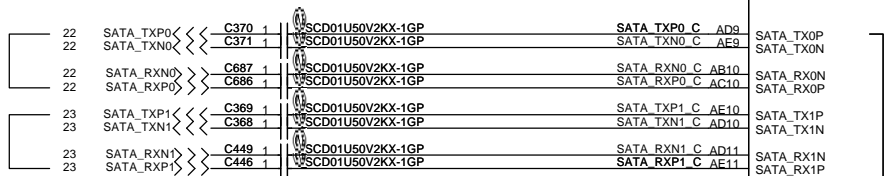


USB	
Pair	Device
11	CardReader
10	WEBCAM
9	NC
8	USB2
7	USBCN1
6	USB1
5	Bluetooth
4	NC
3	Fringier print
2	NC
1	MINIC1
0	USB3

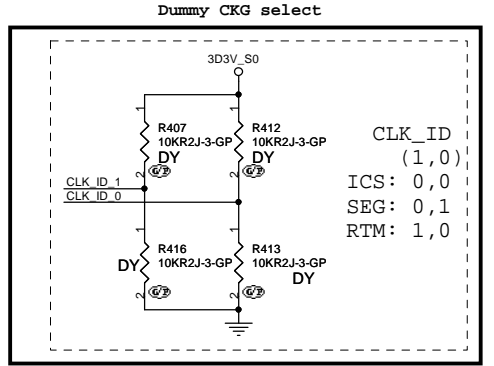
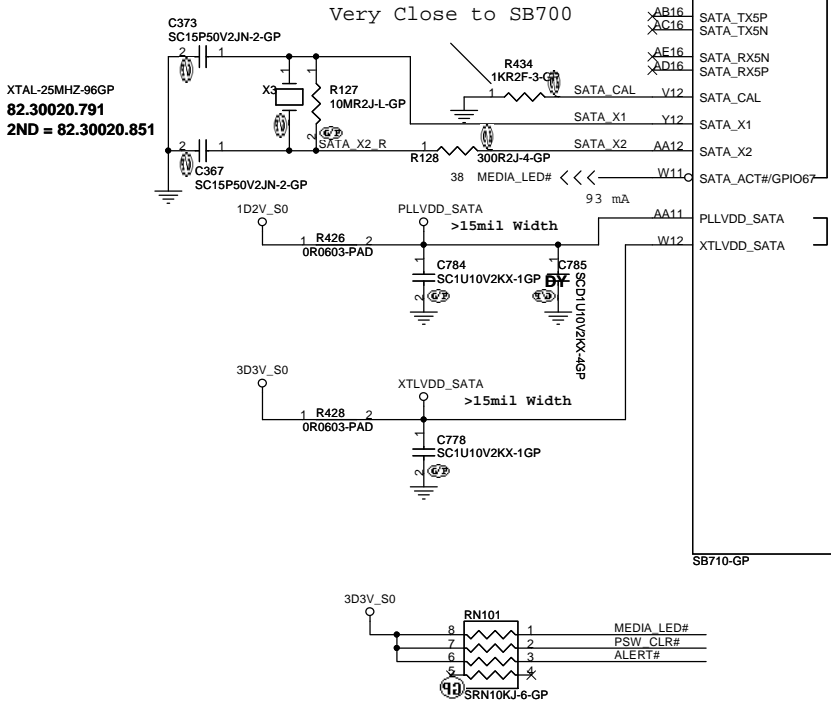
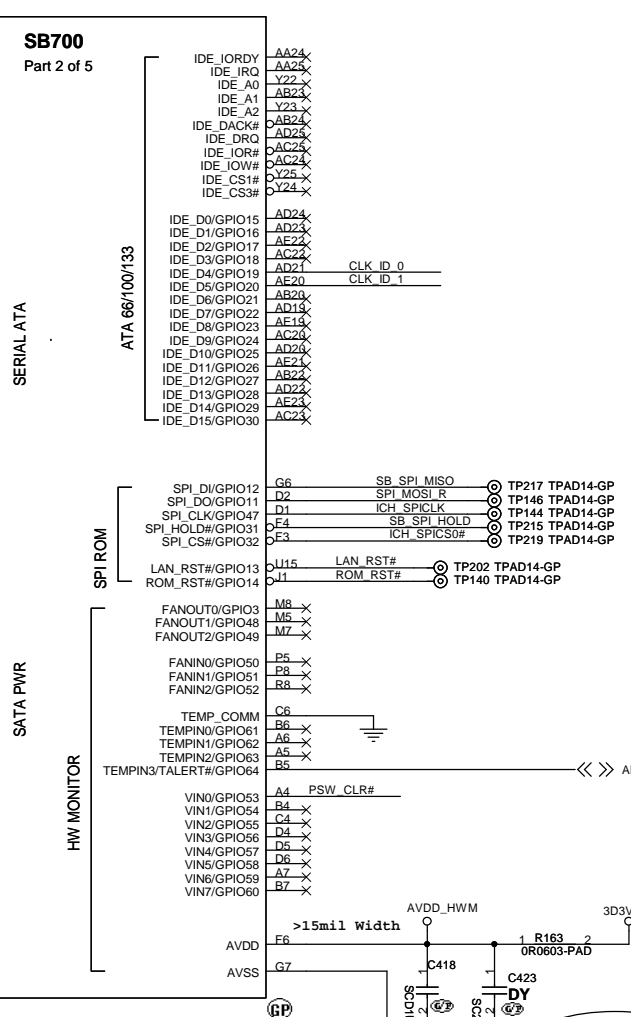
OCP1#
OCP0#

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700

SATA HDD
SATA ODD



ASB1B
SB700
Part 2 of 5
SERIAL ATA
SATA PWR
HW MONITOR
SB710-GP



2009/04/09 ALL DY

Layout connect to Cap then GND

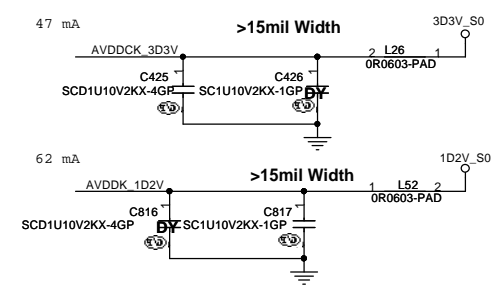
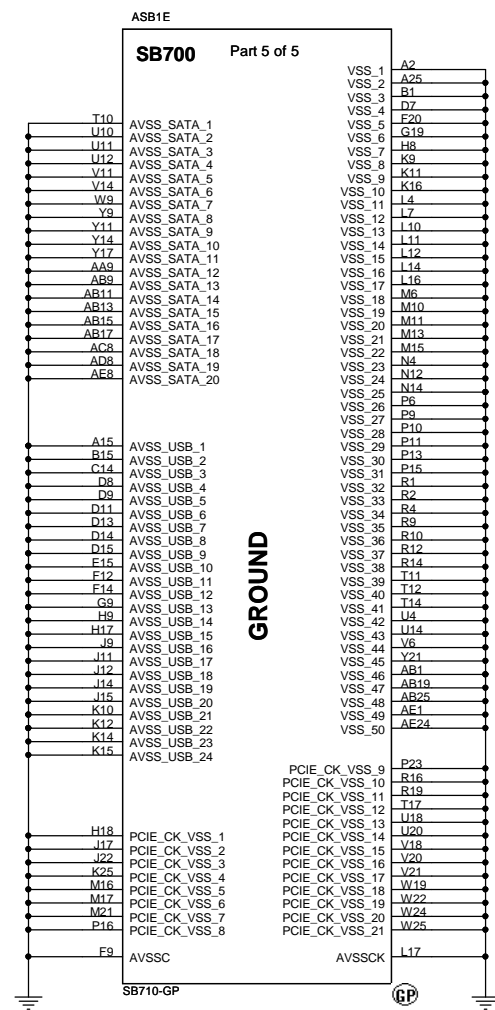
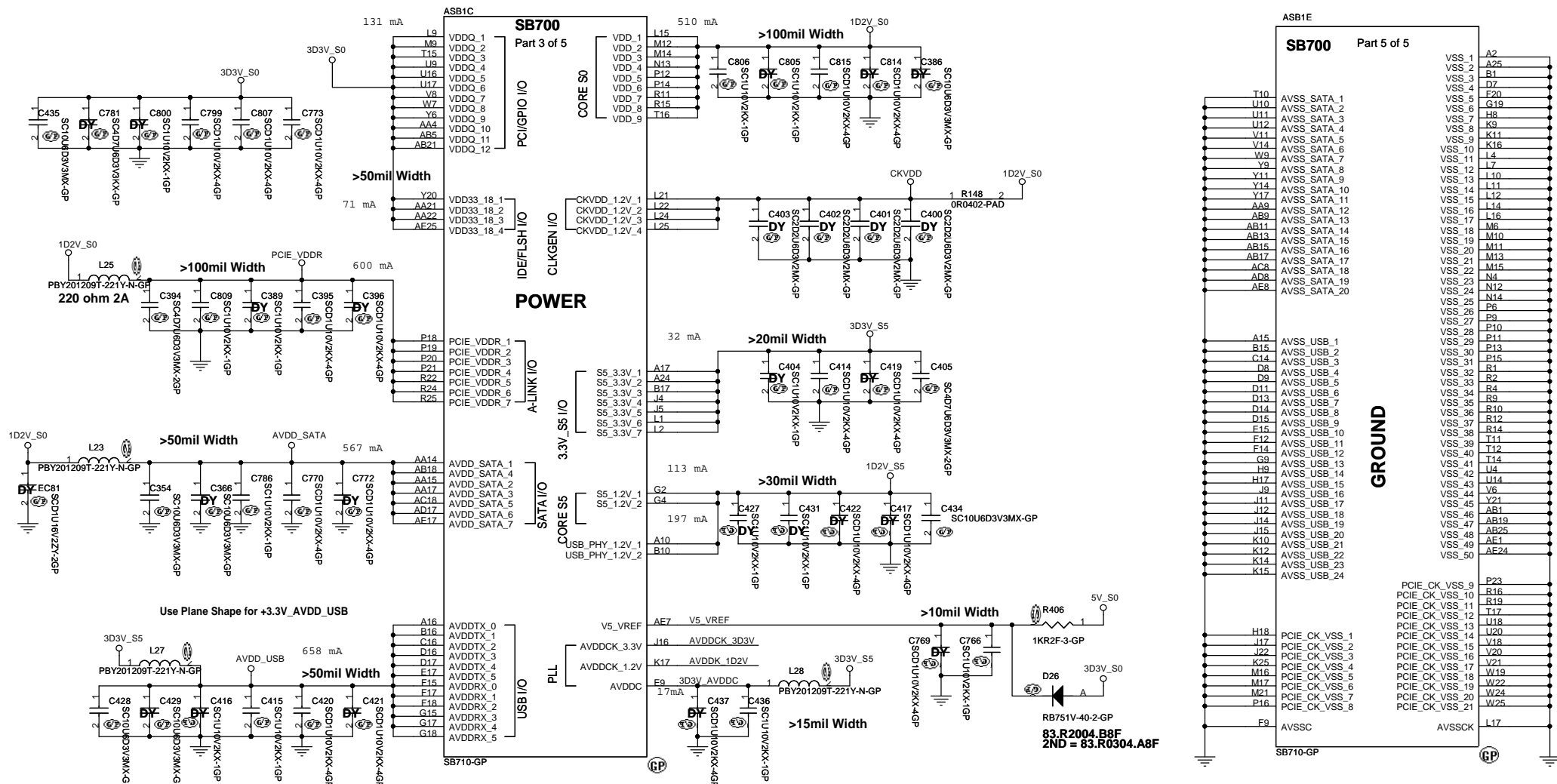
UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 SATA-IDE (3/5)**

Size: A3 Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 13 of 61



UMA

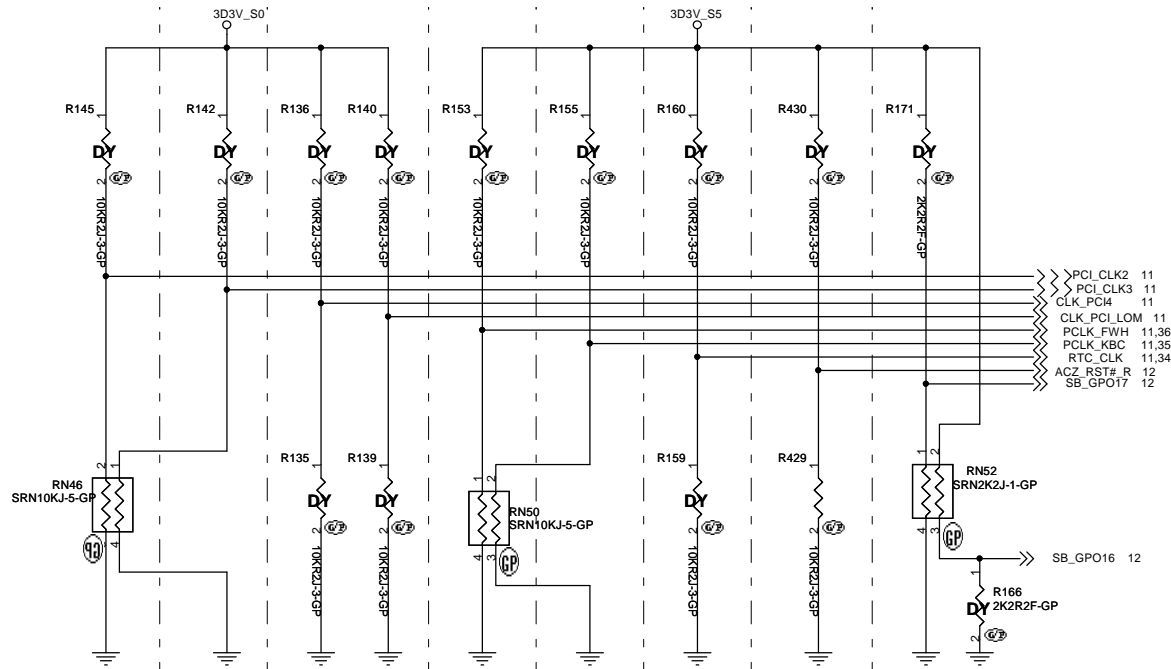
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 POWER&GND (4/5)**

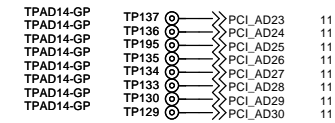
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet: 14	of: 61

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

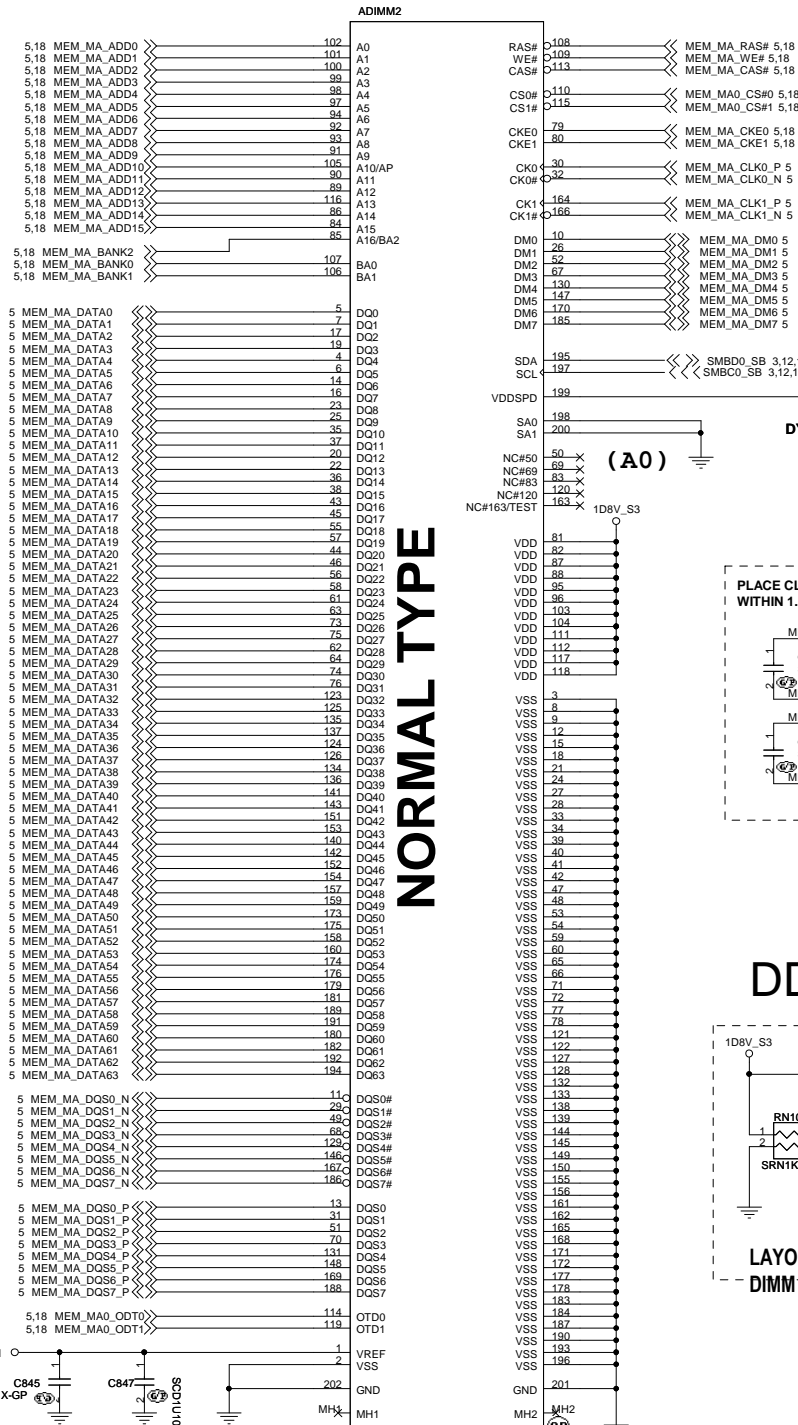
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

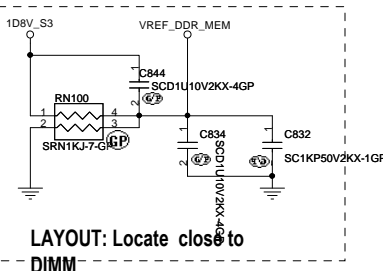
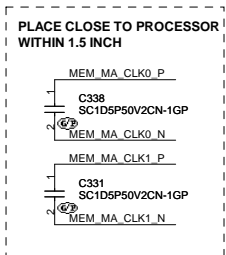
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

UMA

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ATi-SB710 STRAPPING (5/5)			
Size	Document Number		Rev
A3	JV71-TR		SA
Date:	Monday, July 06, 2009		Sheet 15 of 61



NORMAL TYPE



Place C2.2uF and 0.1uF < 500mils from DDR connector

SKT-SODIMM20020U4GP
62.10017.661
 2ND = 62.10017.A41
 3RD = 62.10017.G81

LOW 5.2 mm

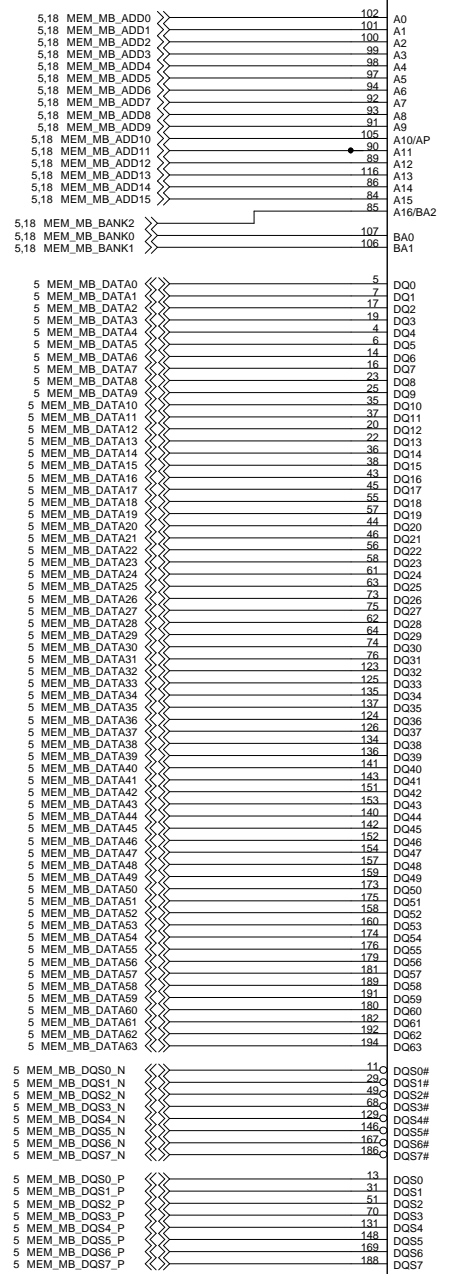
UMA

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

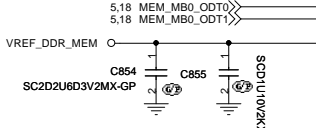
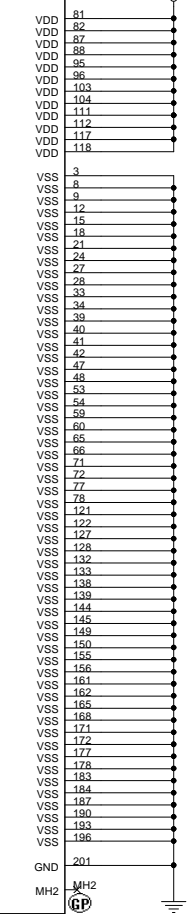
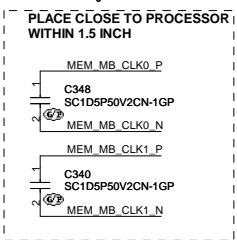
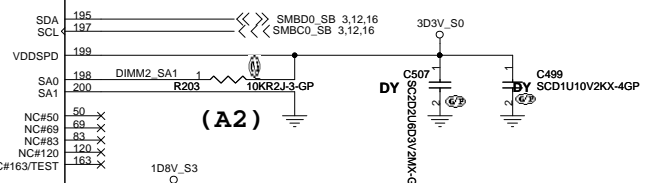
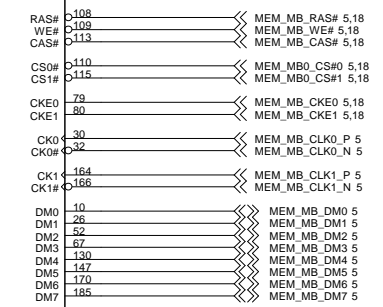
Title: **DDR SO-DIMM SKT_1**

Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet: 16 of 61



NORMAL TYPE



SKT-SODIMM200-37GP

62-10017.E21
2ND = 62-10017.A51
3RD = 62-10017.G71

HI 9.2mm

Place C2.2uF and 0.1uF < 500mils from DDR connector

UMA

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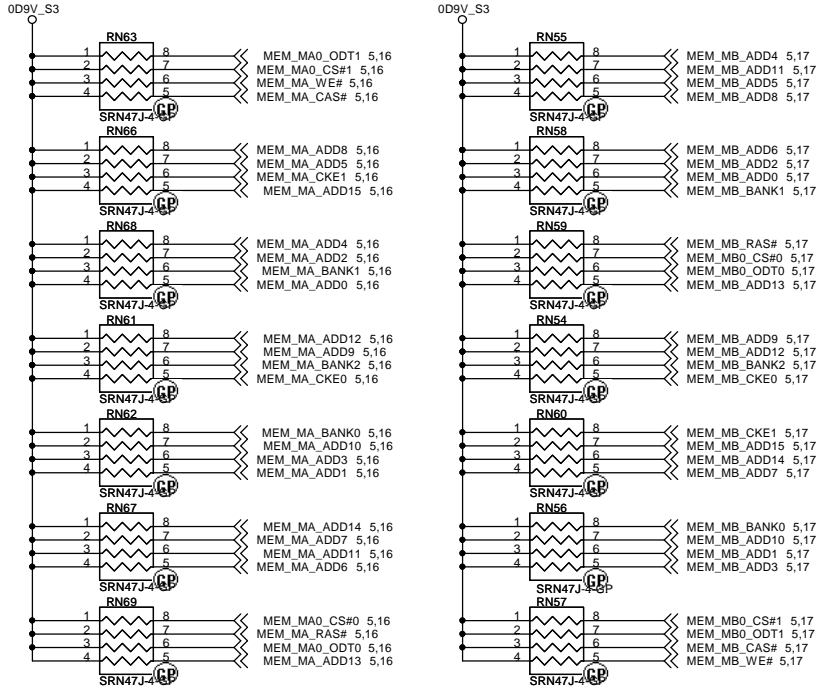
Title: **DDR SO-DIMM SKT 2**

Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 17 of 61

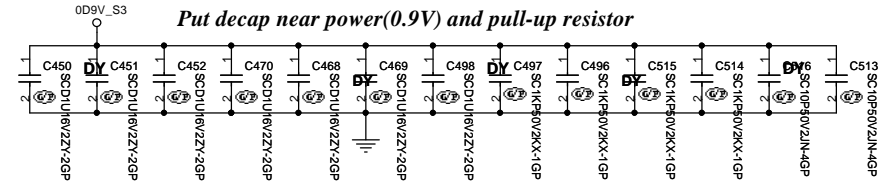
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

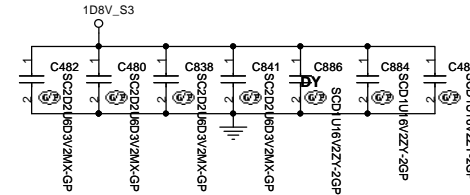


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

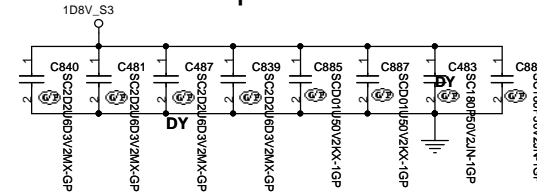


Place these Caps near DM1



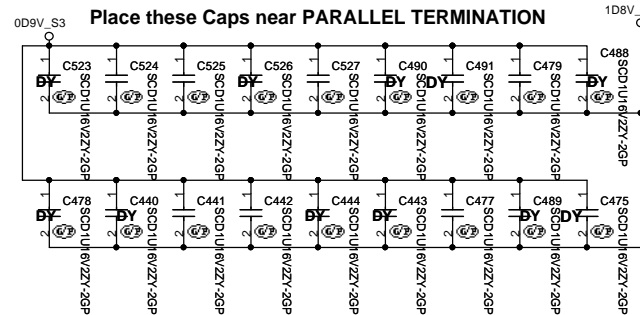
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



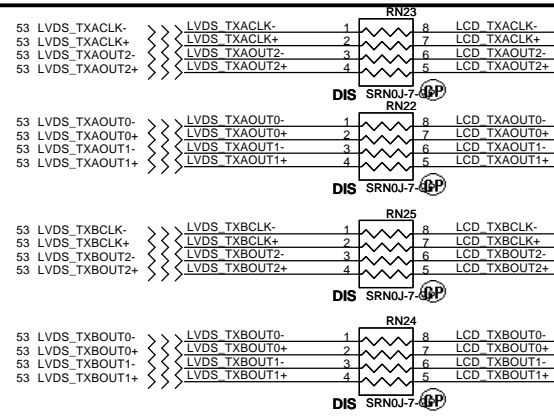
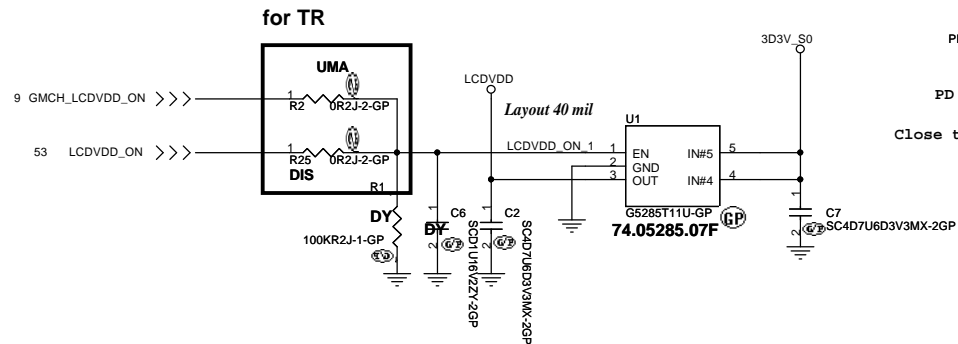
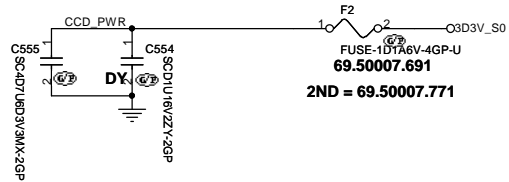
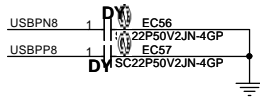
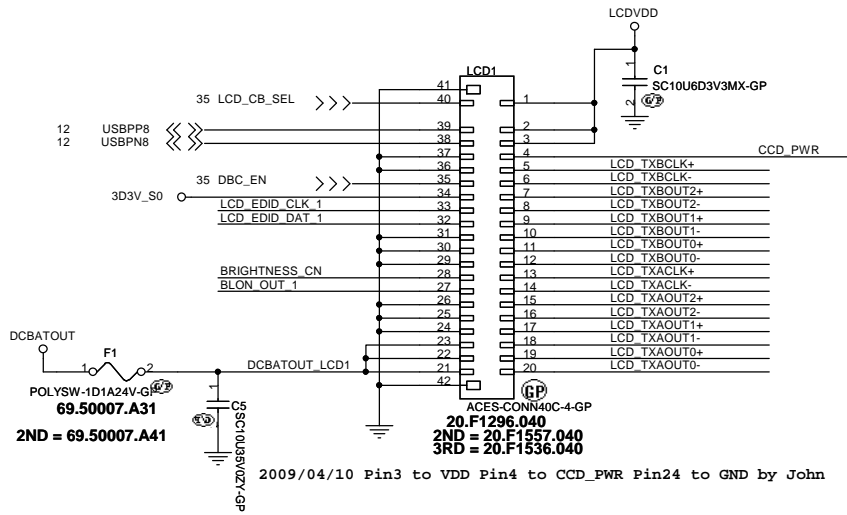
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



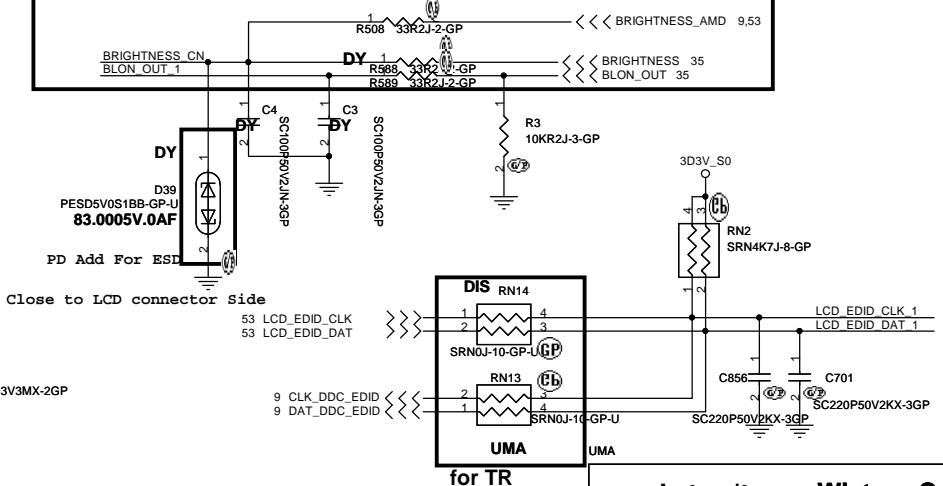
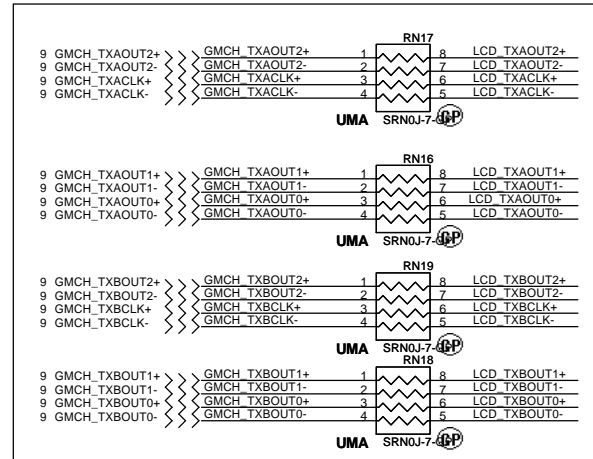
LCD/INVERTER/CCD CONN

for TR

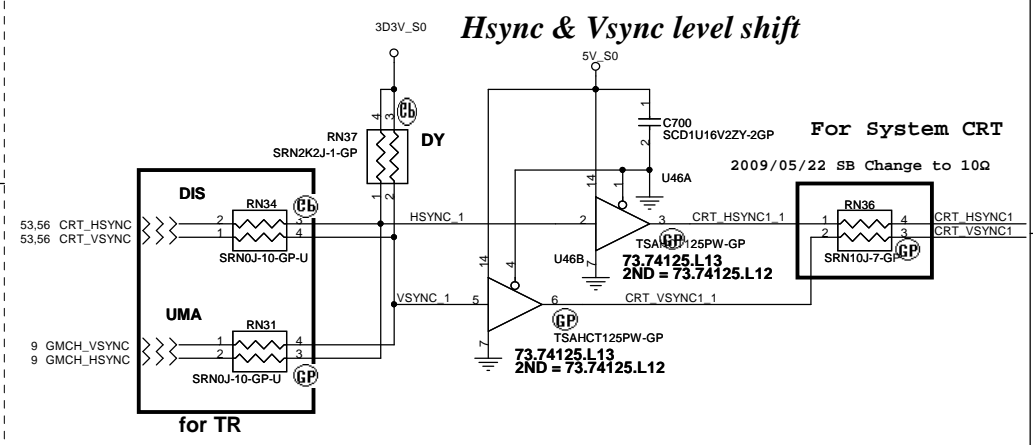
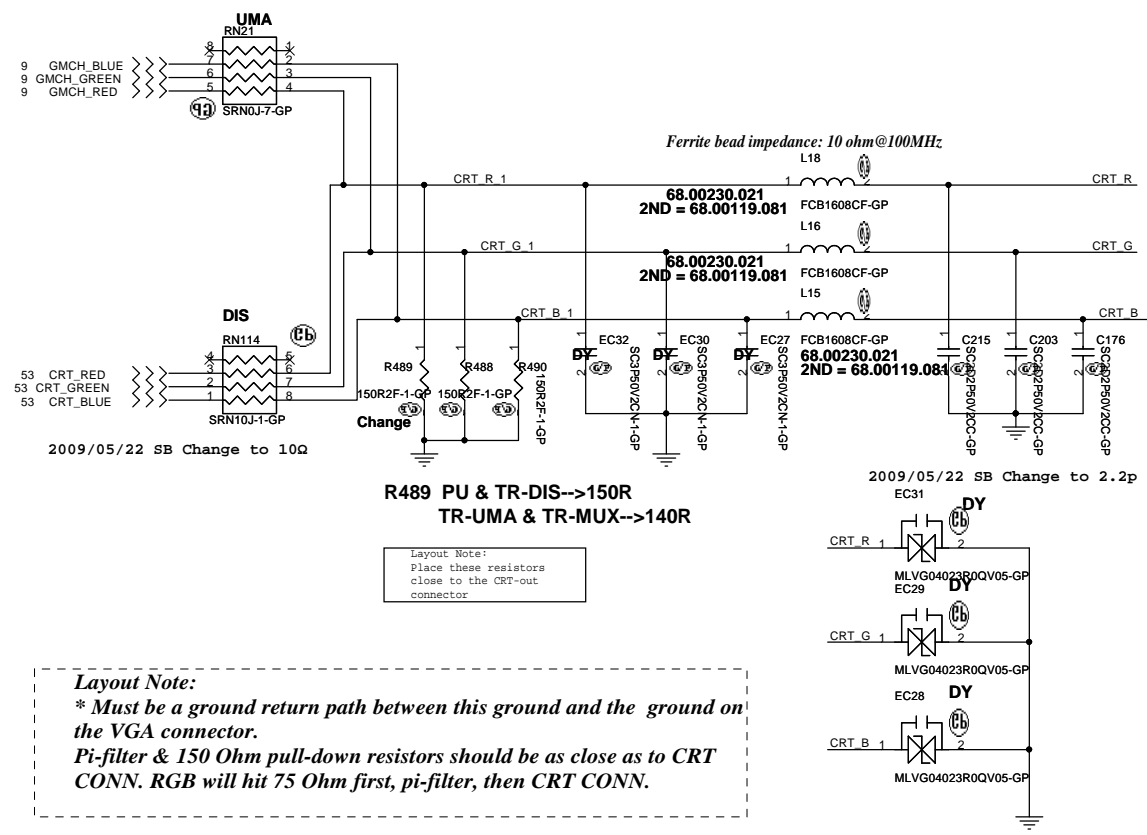


Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

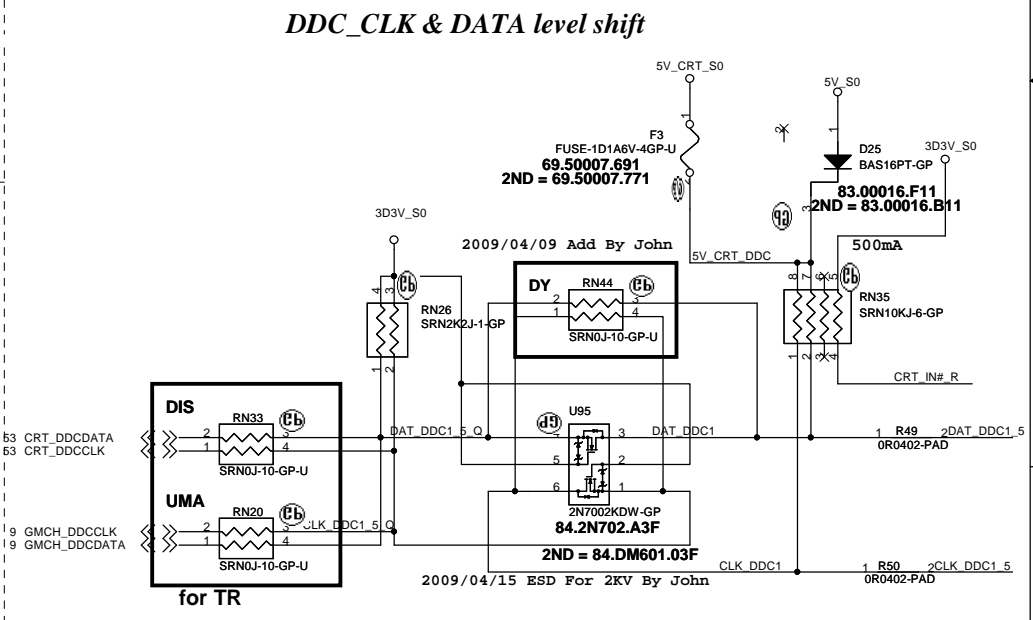
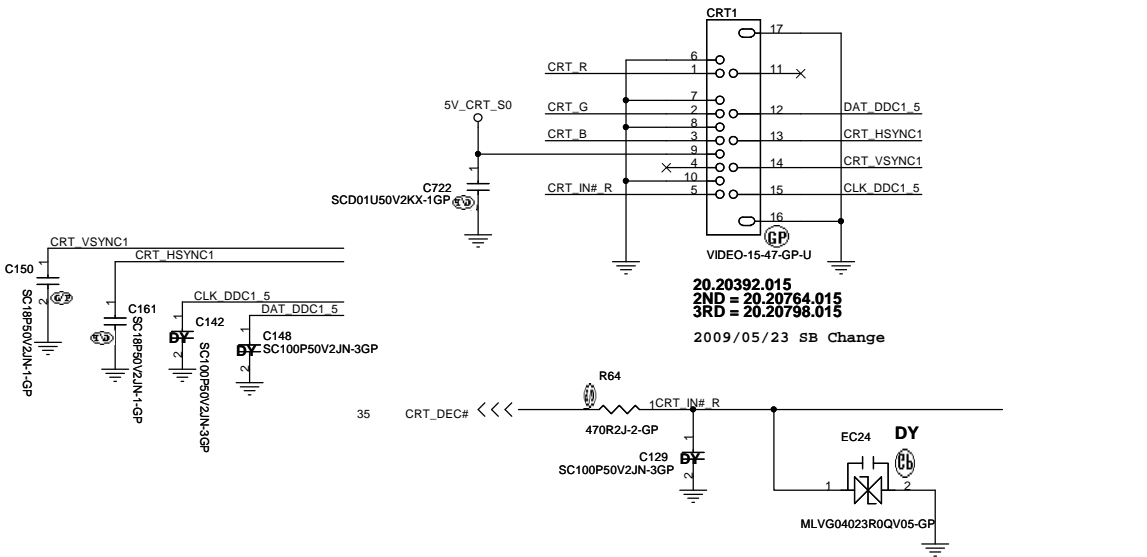
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



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 Taipei Hsien 221, Taiwan, R.O.C.



CRT I/F & CONNECTOR



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

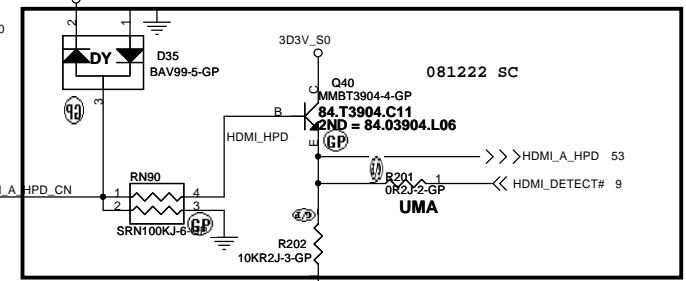
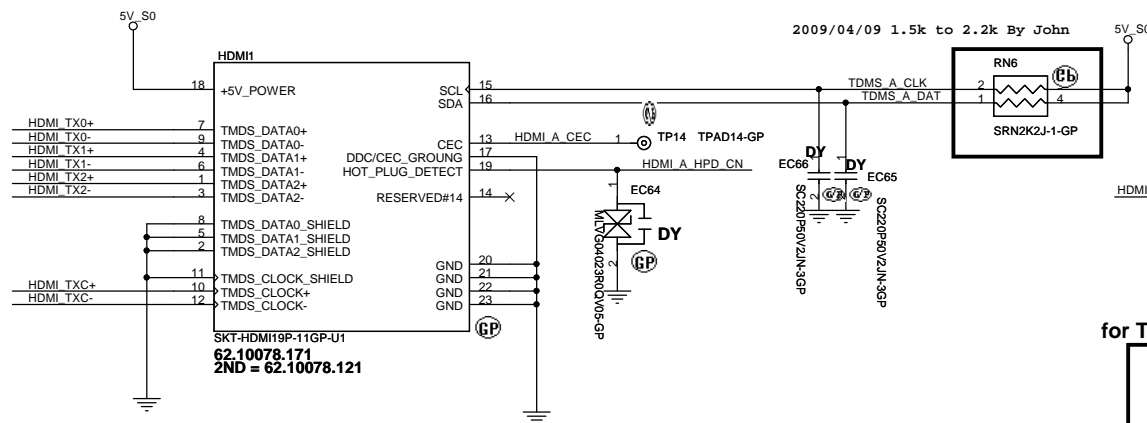
Size: Document Number

Date: Monday, July 06, 2009

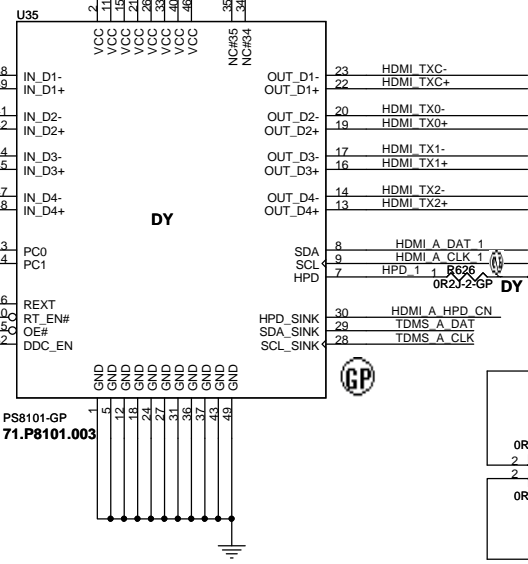
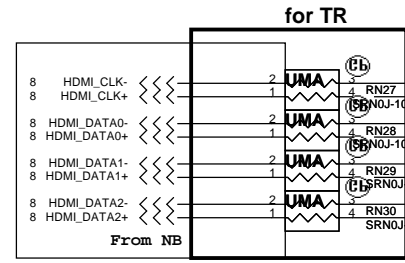
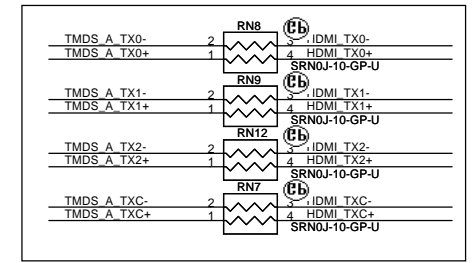
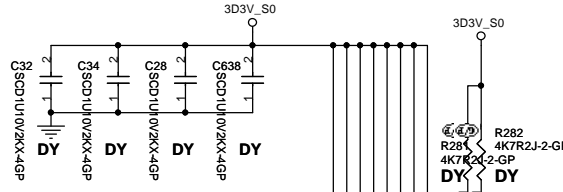
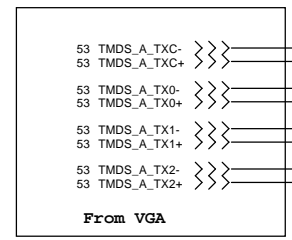
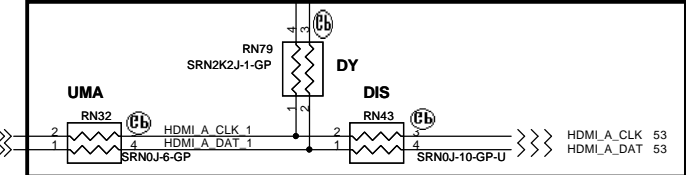
Sheet 20 of 61

Rev: **SB**

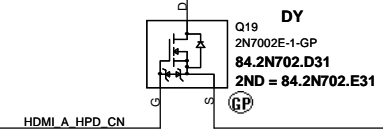
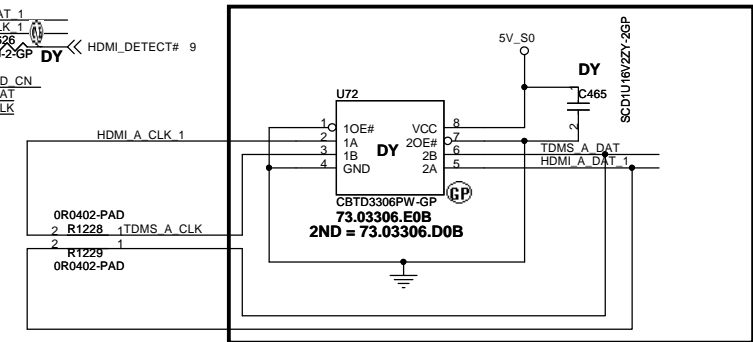
Part Number: **JV71-TR**



for TR



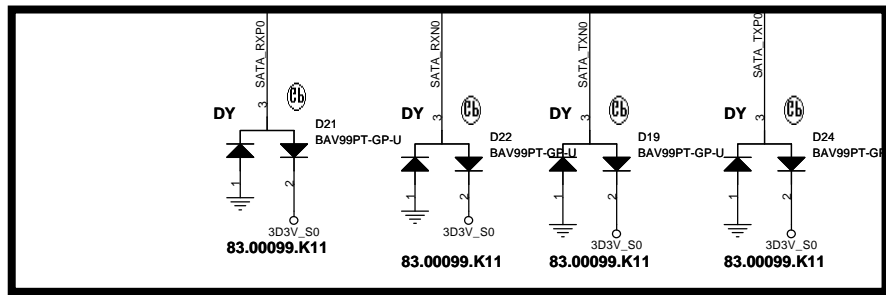
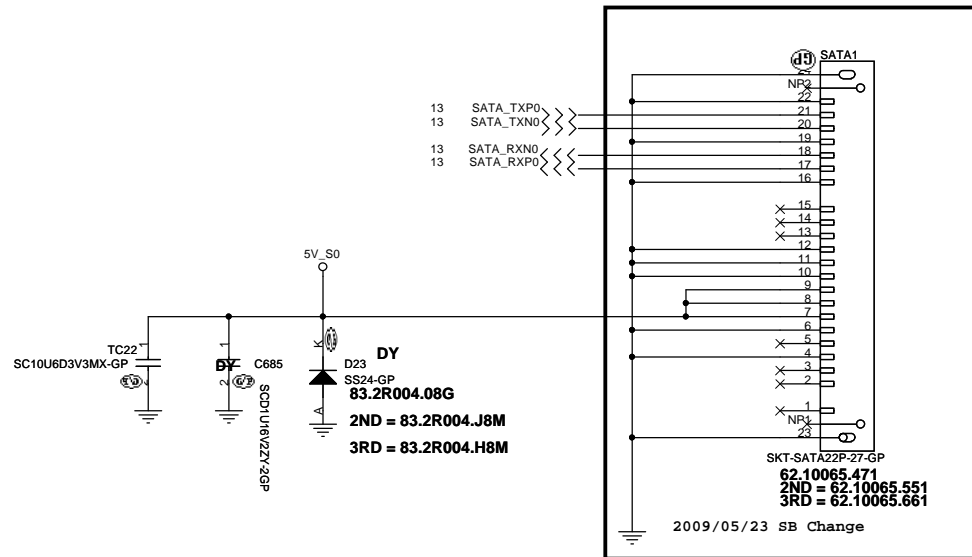
2009/04/14 Follow JM70 By John



緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

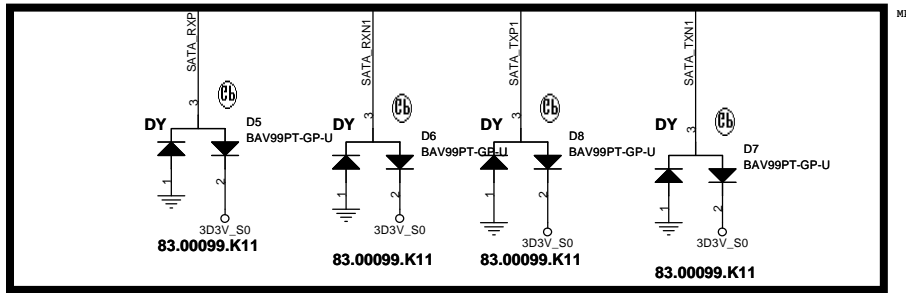
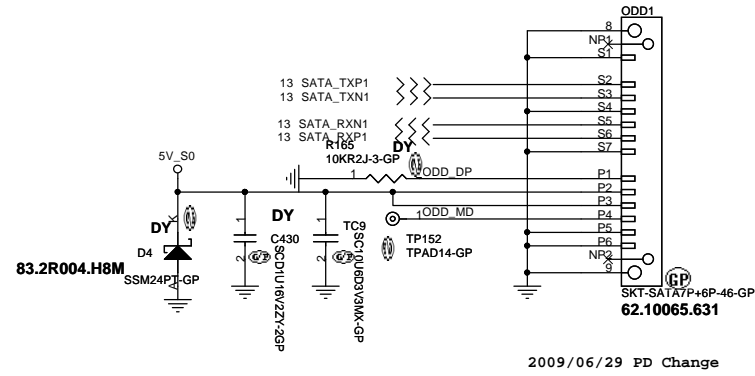
SATA Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD	
Size	Document Number
JV71-TR	
Date: Monday, July 06, 2009	Sheet 22 of 61
Rev SB	

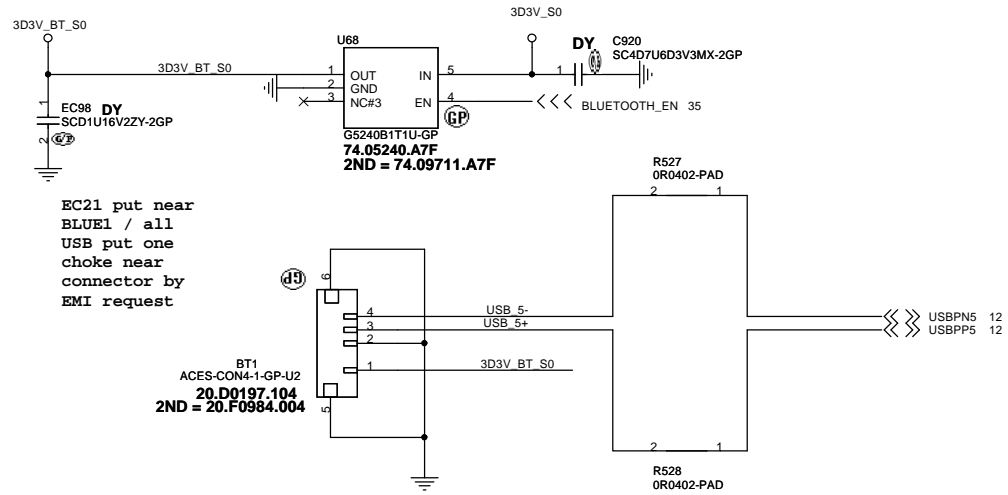
SATA ODD Connector



UMA

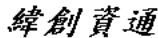
BLUETOOTH MODULE

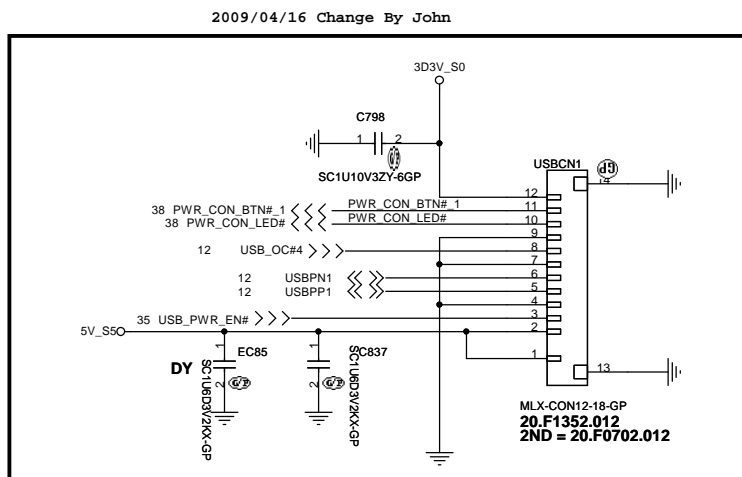
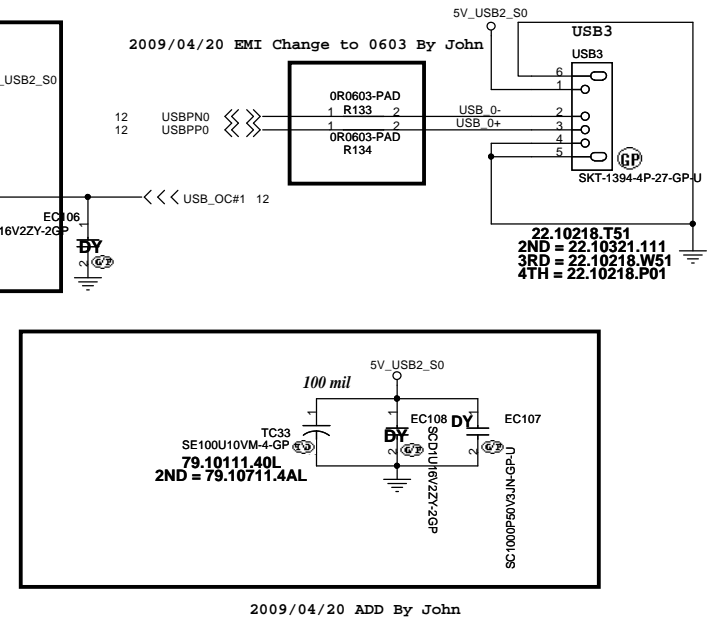
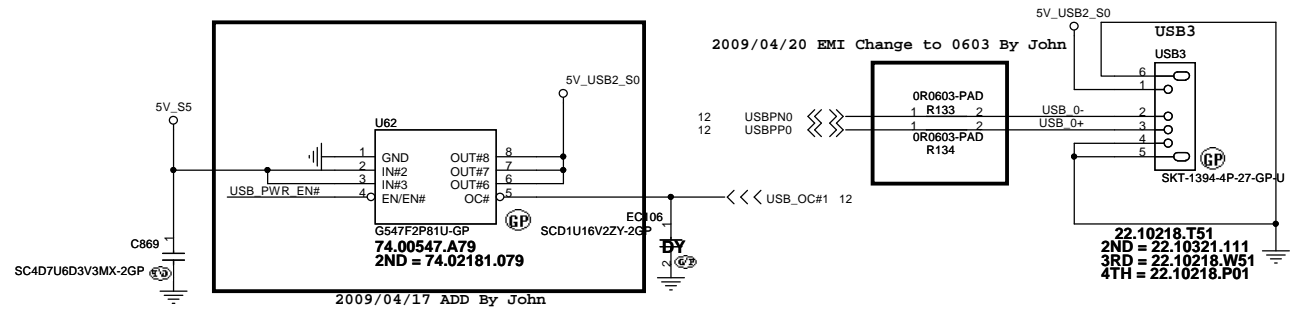
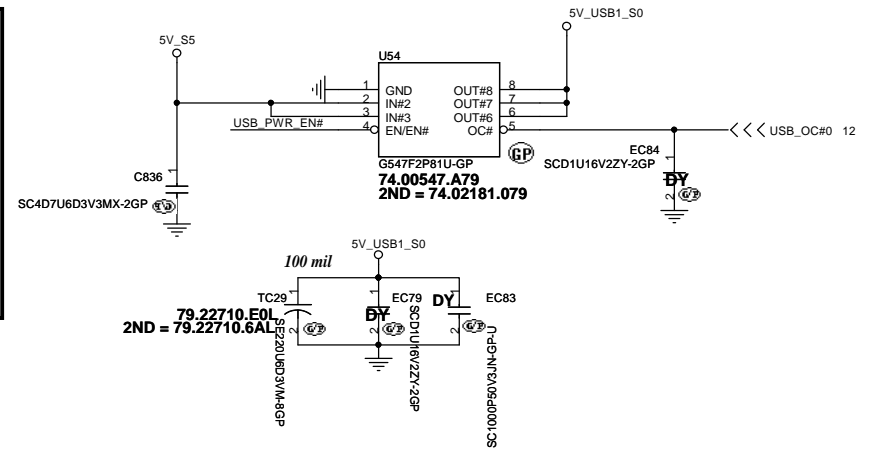
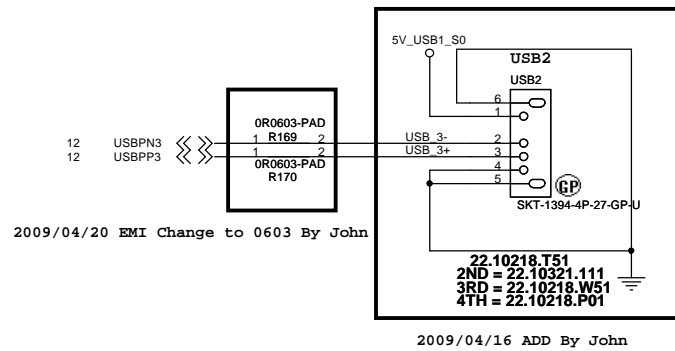
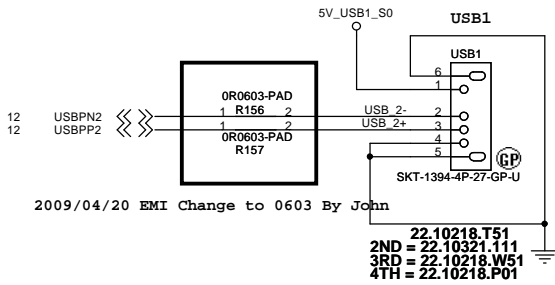
1.5A / High Active Voltage 2V



EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BLUETOOTH	
Size	Document Number
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SA	



- USB_OC#4 1 AFTE14P-GP
- USBPN1 1 AFTE14P-GP
- USBPP1 1 AFTE14P-GP
- USB_PWR_EN# 1 AFTE14P-GP
- 5V_S5 1 TP179 AFTE14P-GP

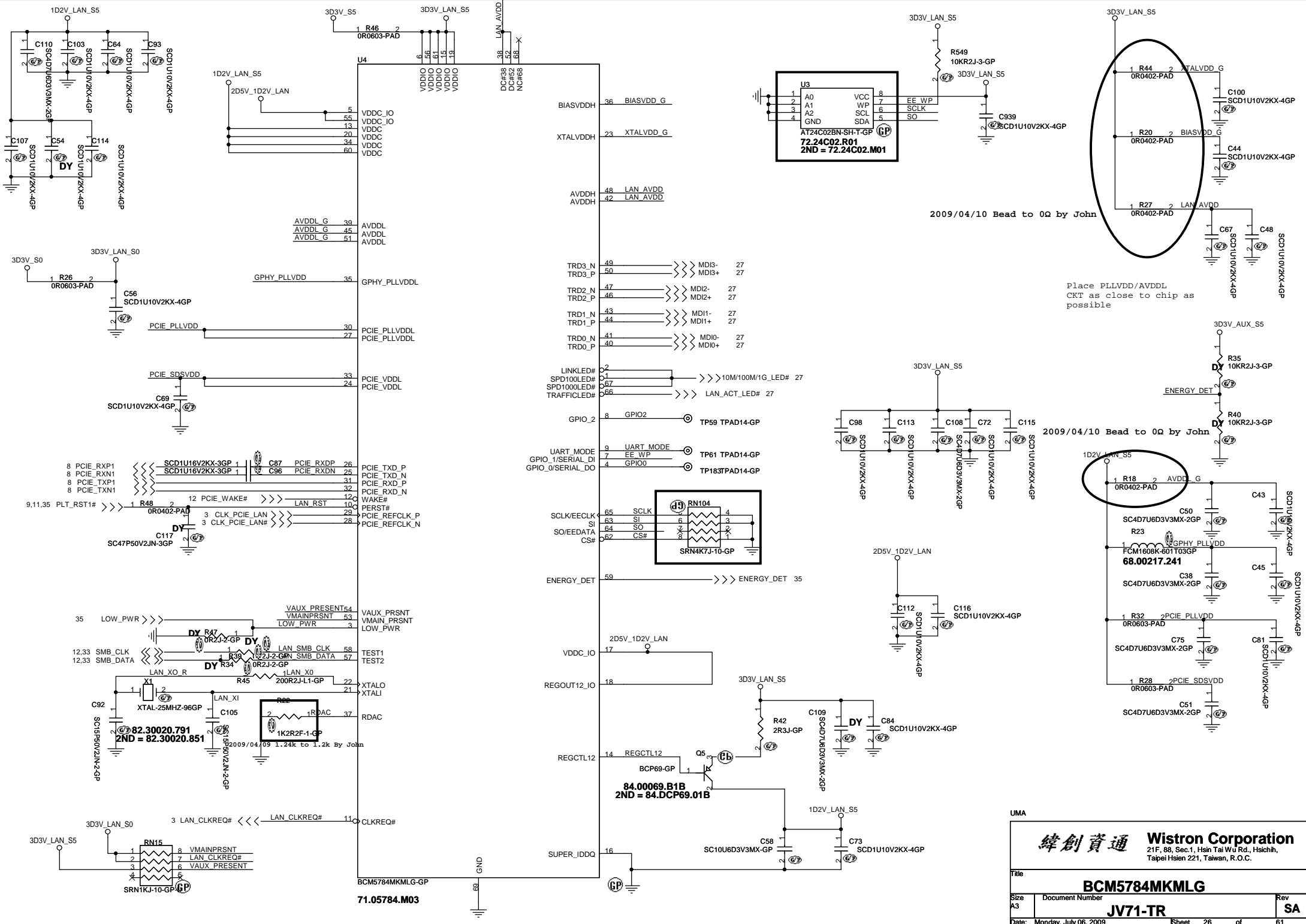
UMA

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Title: **USB**

Size: Document Number **JV71-TR** Rev: **SA**

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UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM5784M KMLG**

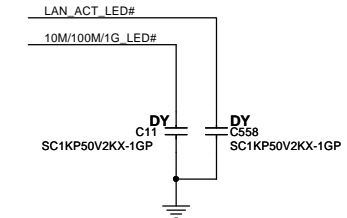
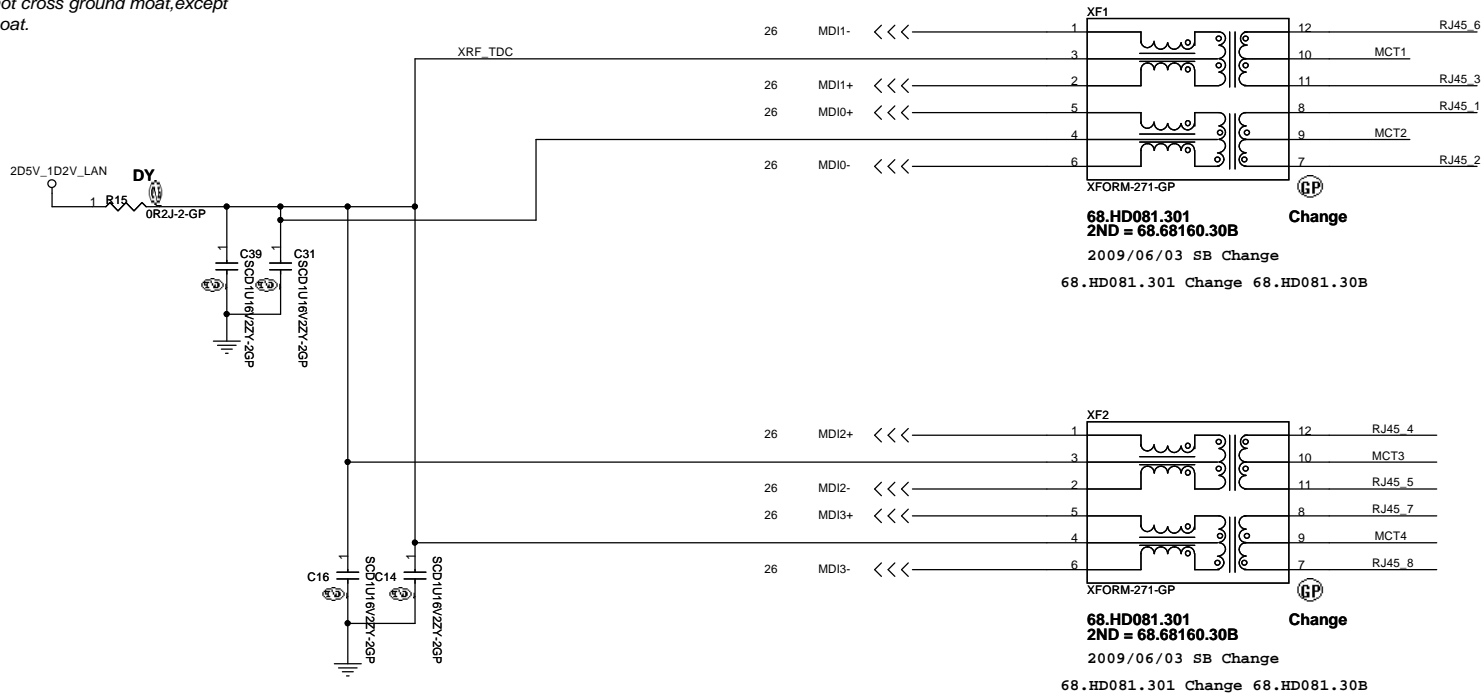
Size A3 Document Number **JV71-TR** Rev **SA**

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LAN Connector

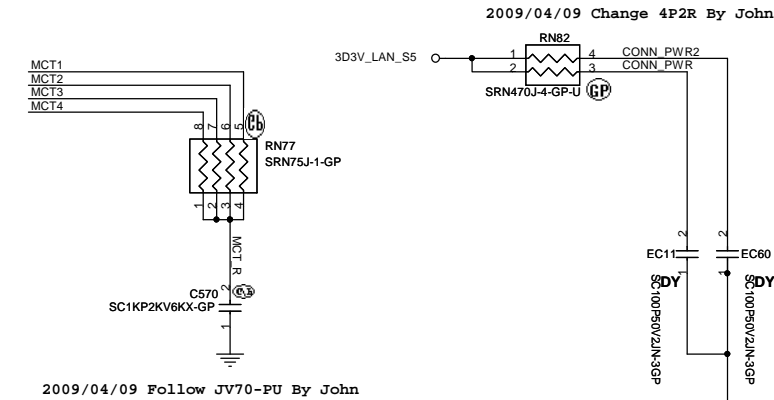
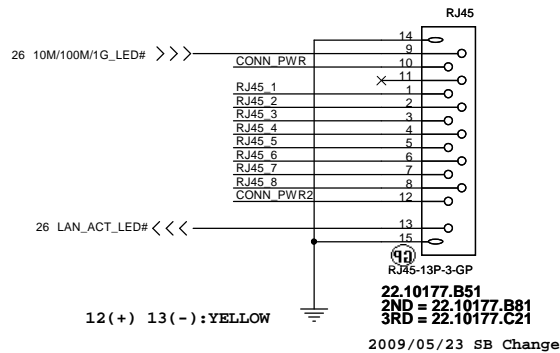
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

GIGA Lan Transformer



10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

LAN Connector



DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

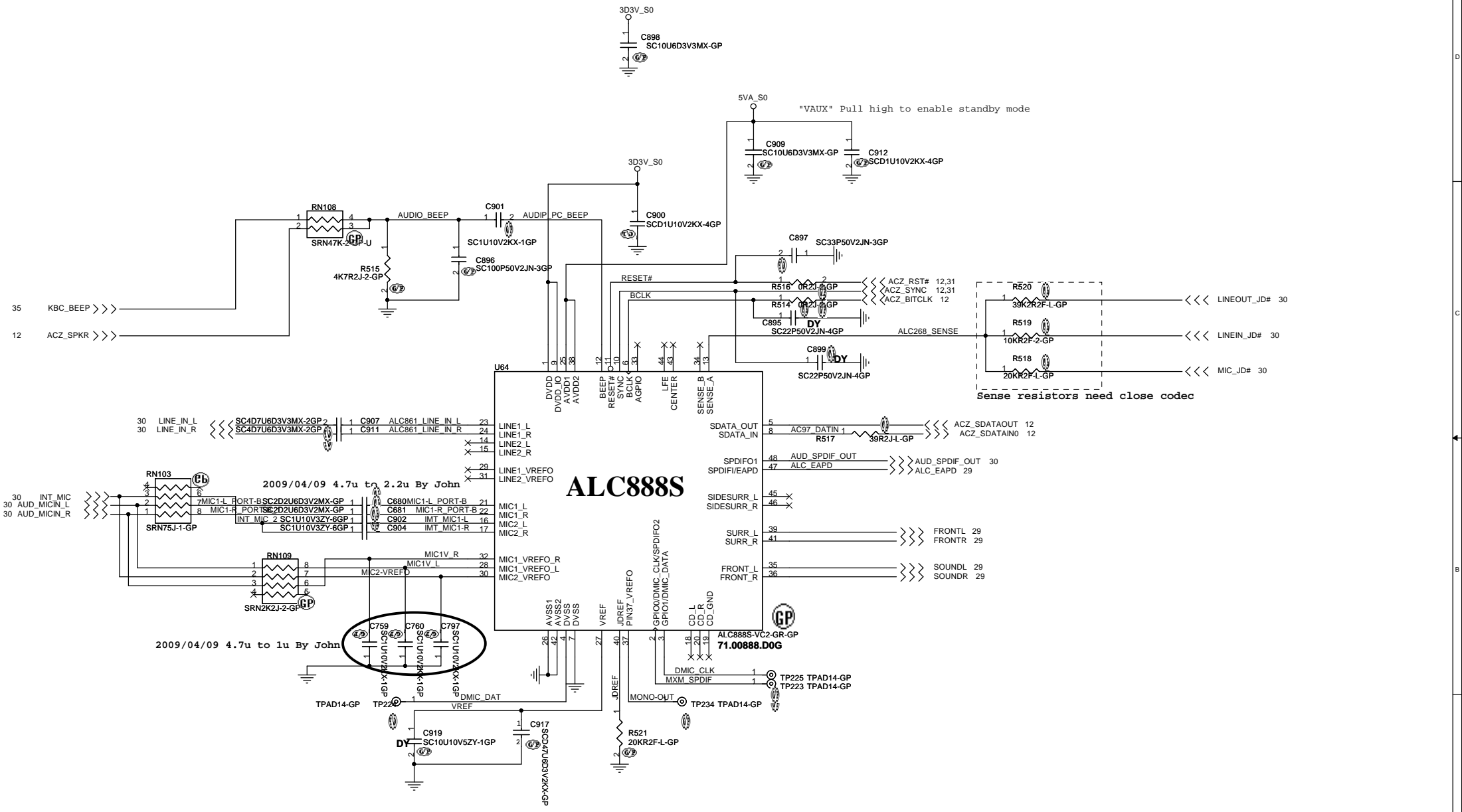
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN CONN

Size A3 Document Number **JV71-TR** Rev **SB**

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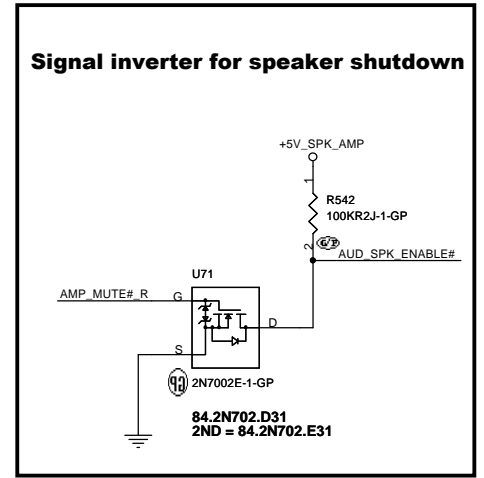
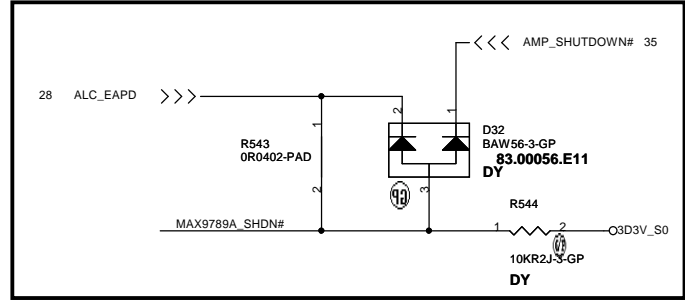
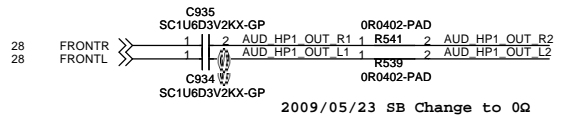
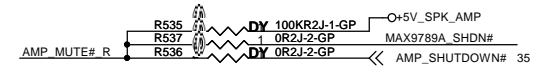
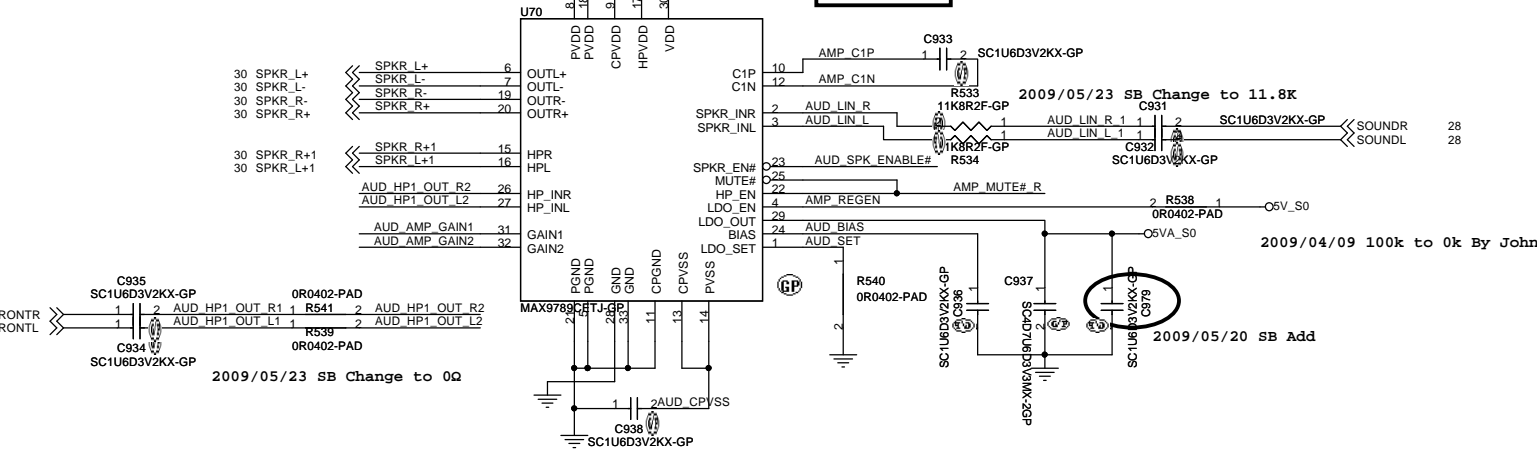
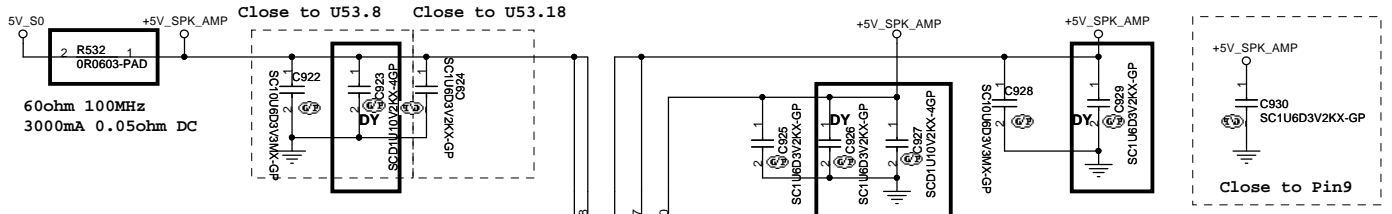
UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC888**

Size A3	Document Number JV71-TR	Rev SB
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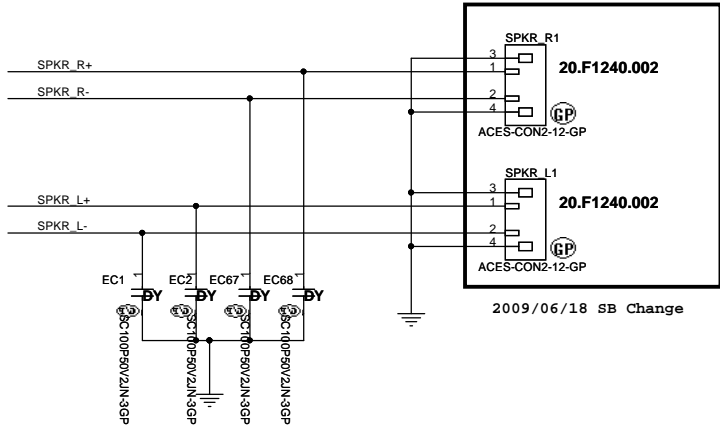
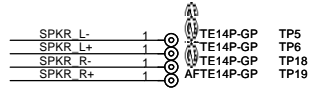
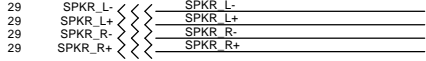
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GAIN SETTING

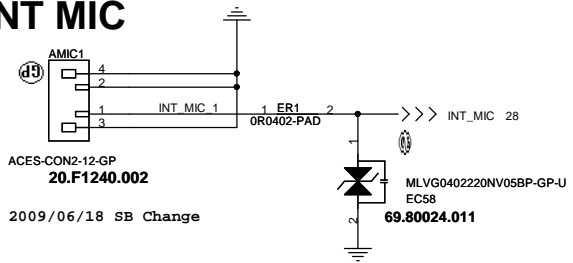
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Internal Speaker

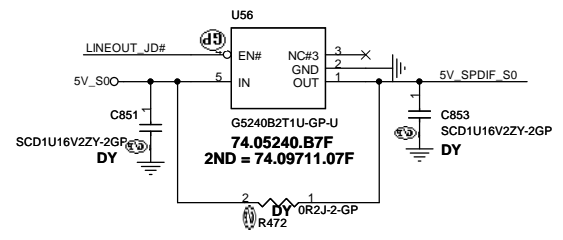


2009/06/18 SB Change

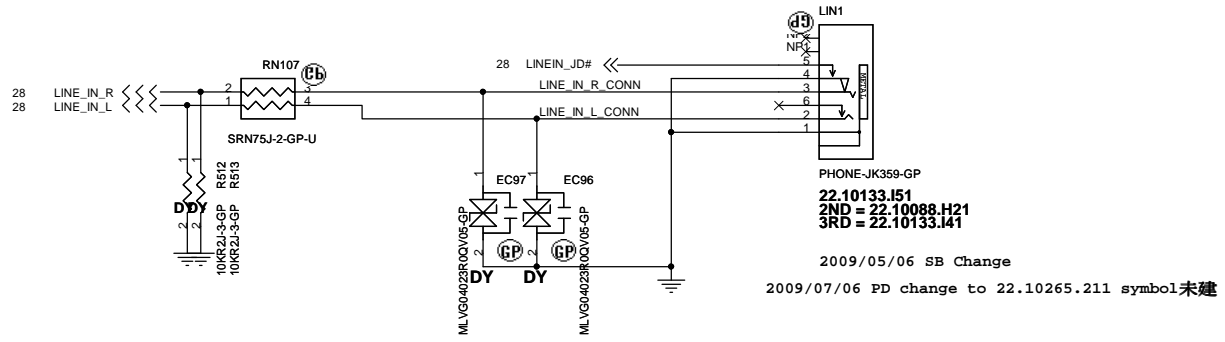
INT MIC



2009/06/18 SB Change

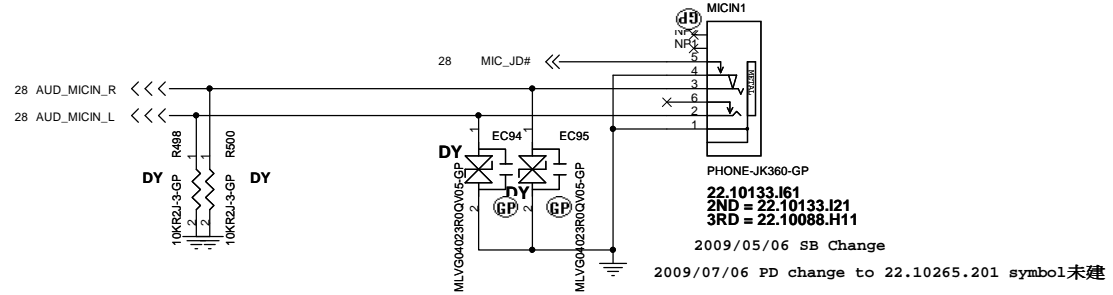


LINE IN



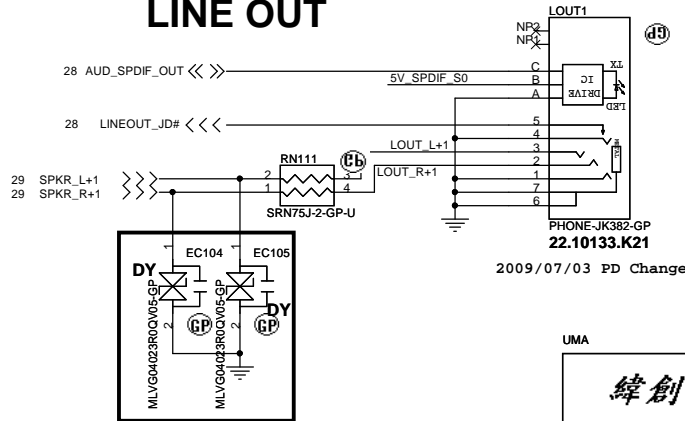
2009/05/06 SB Change
2009/07/06 PD change to 22.10265.211 symbol未建

MIC IN



2009/05/06 SB Change
2009/07/06 PD change to 22.10265.201 symbol未建

LINE OUT



2009/07/03 PD Change

UMA

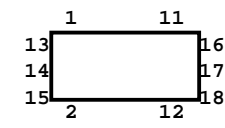
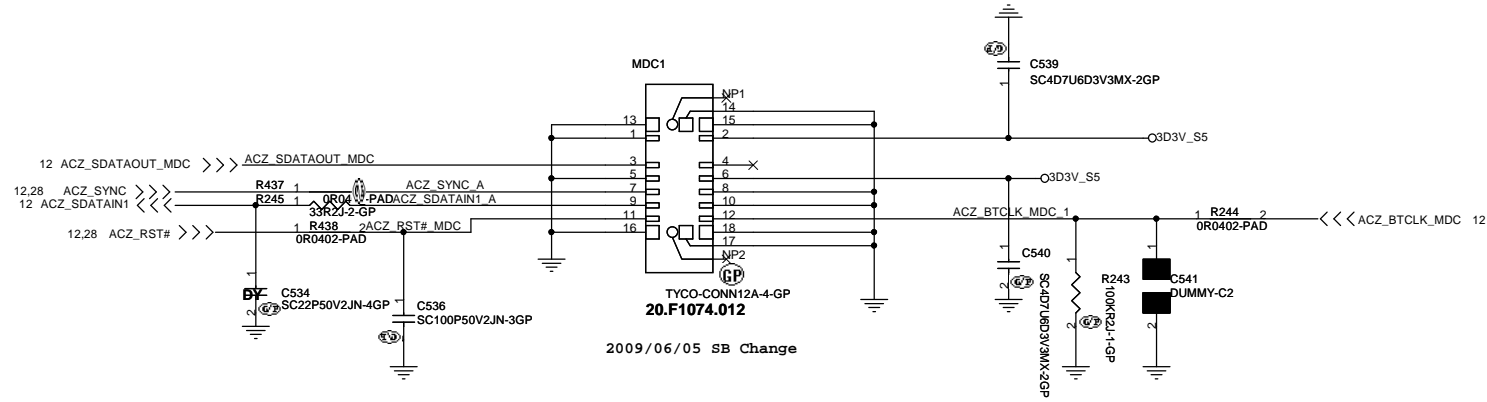
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

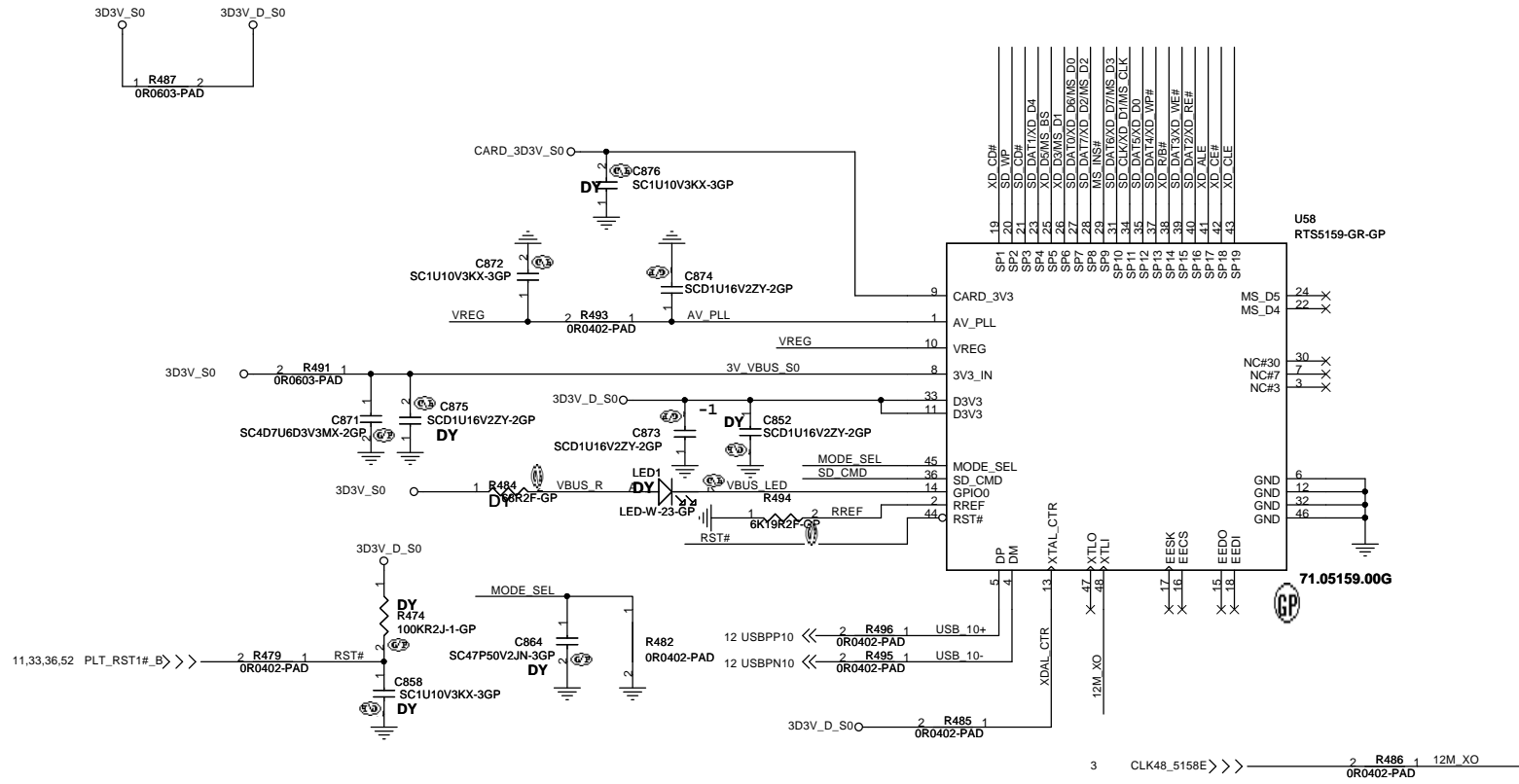
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Size: Document Number **JV71-TR** Rev: **SB**

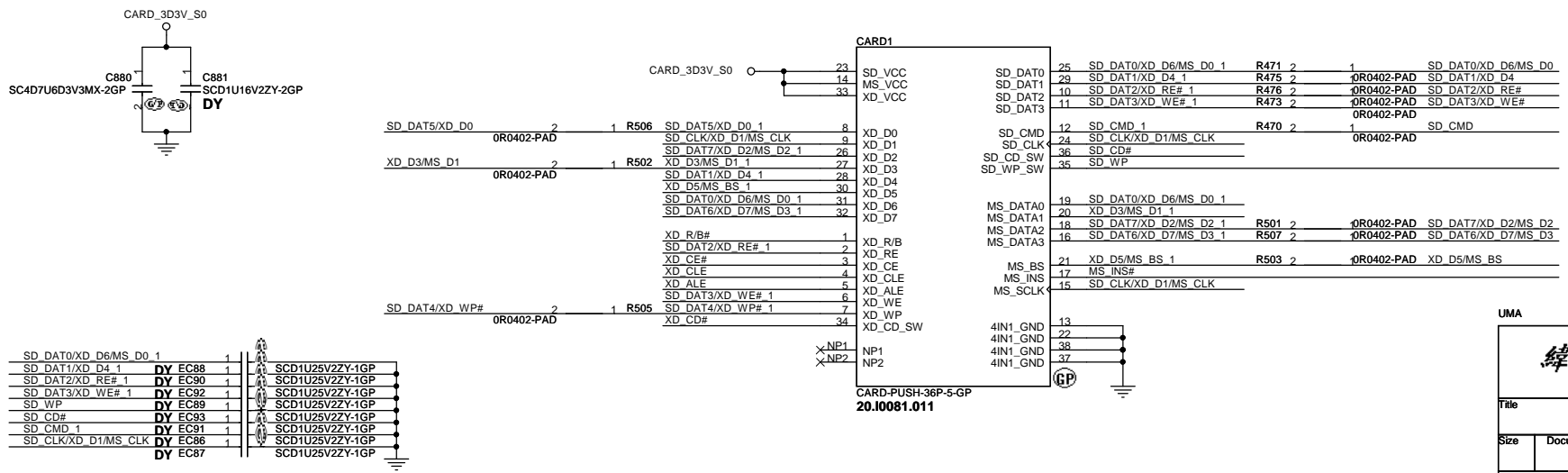
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MDC 1.5 CONN





5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

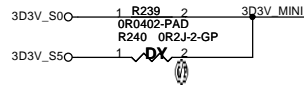
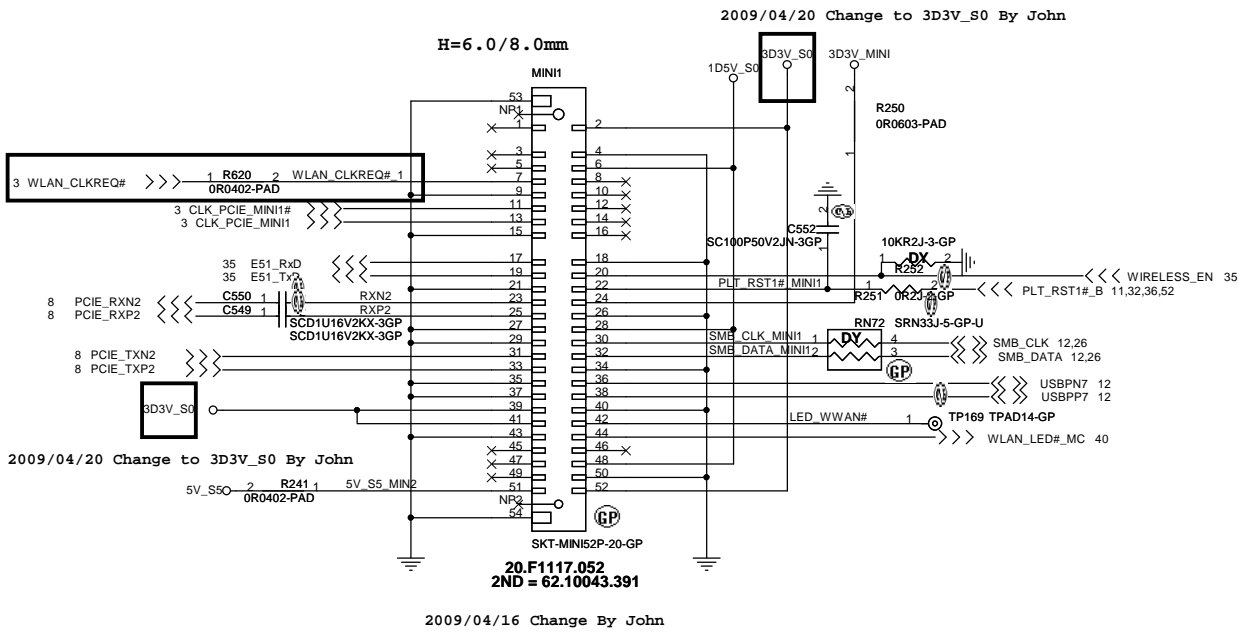
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CARDREADER- RTS5159**

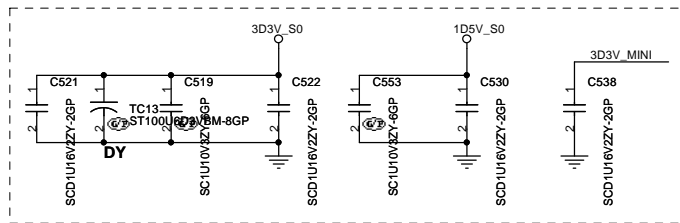
Size Document Number **JV71-TR** Rev **SB**

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Mini Card Connector(WLAN)

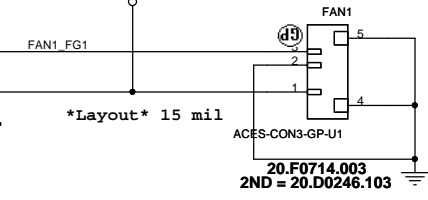
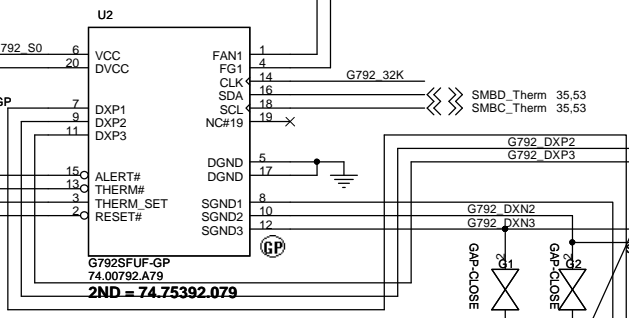
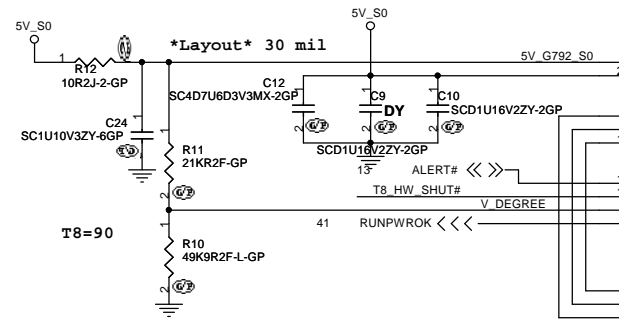
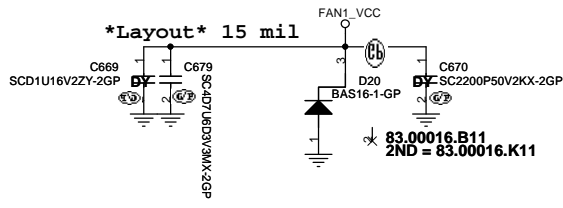


Place near MINI1

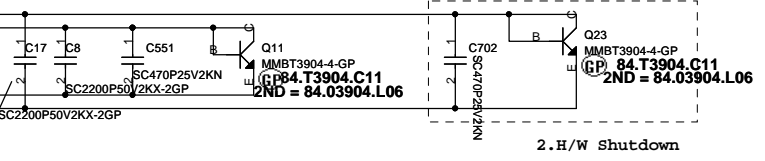


UMA

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MINI CARD	
File	Rev
Size	Document Number
JV71-TR	
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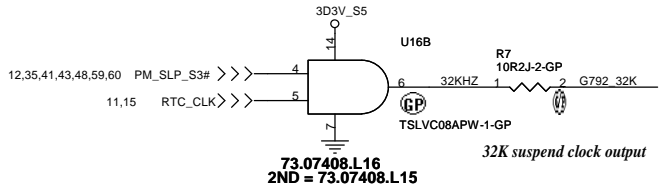


3.System Sensor, Put Plamrest.



DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

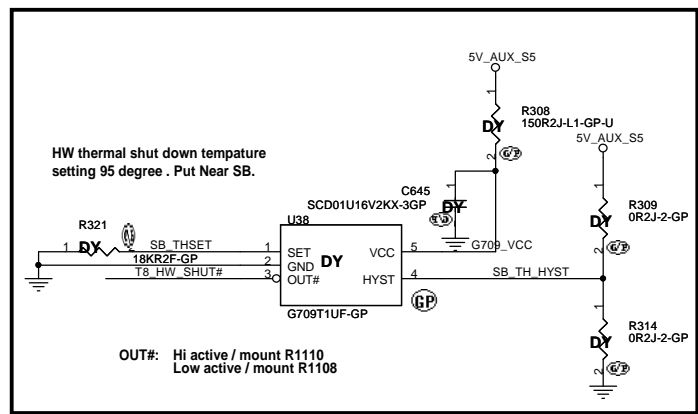
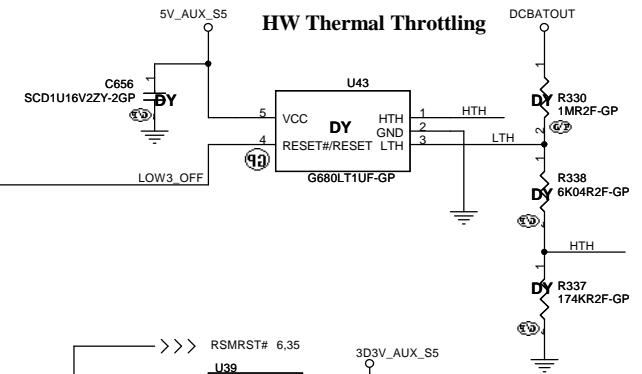


73.07408.L16
2ND = 73.07408.L15

32K suspend clock output

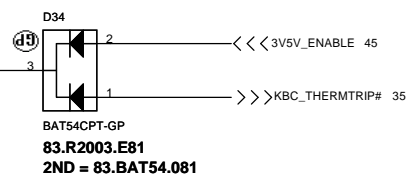
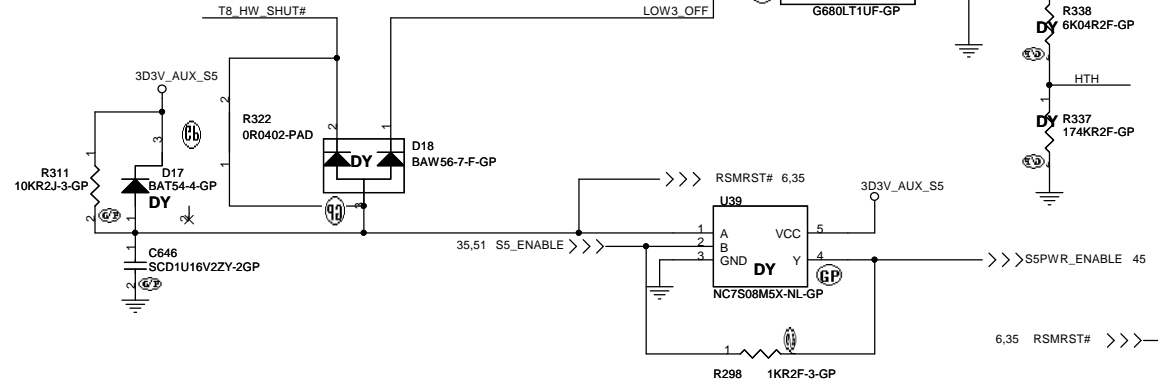
BL3#

HW Thermal Throttling



HW thermal shut down temperature setting 95 degree . Put Near SB.

OUT#: Hi active / mount R1110
Low active / mount R1108



UMA

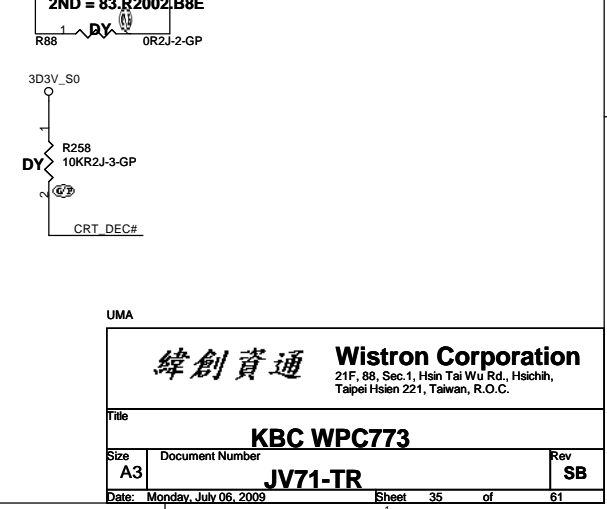
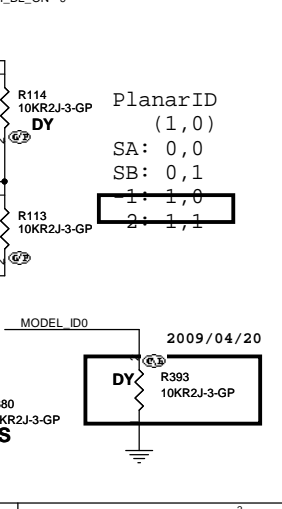
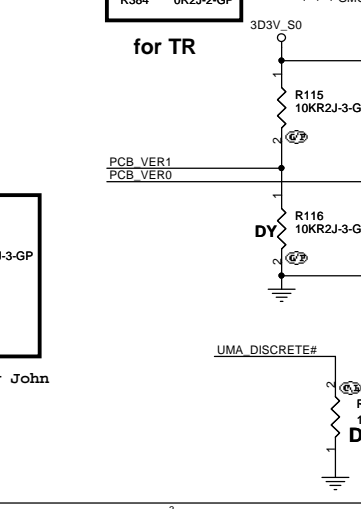
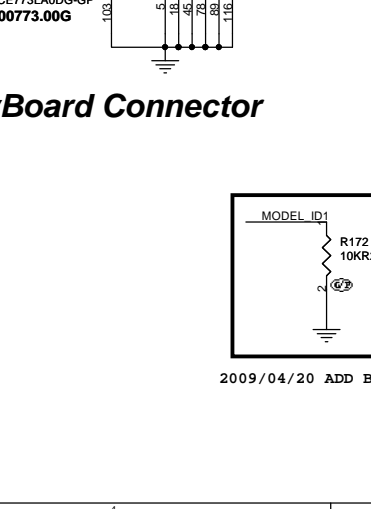
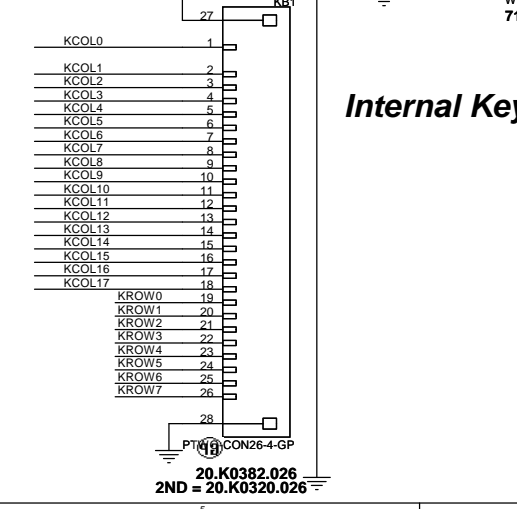
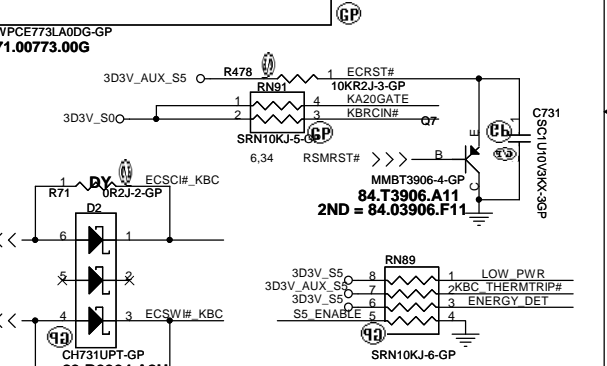
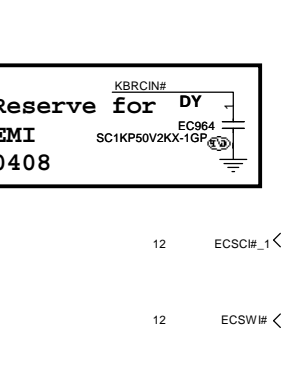
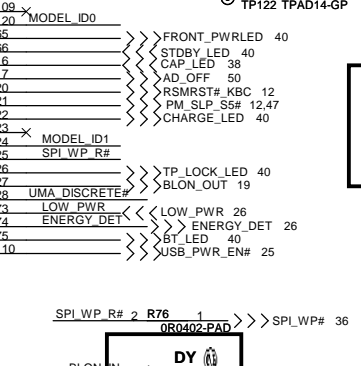
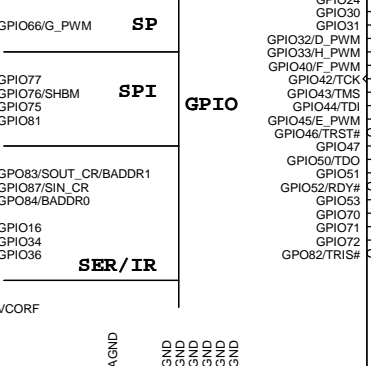
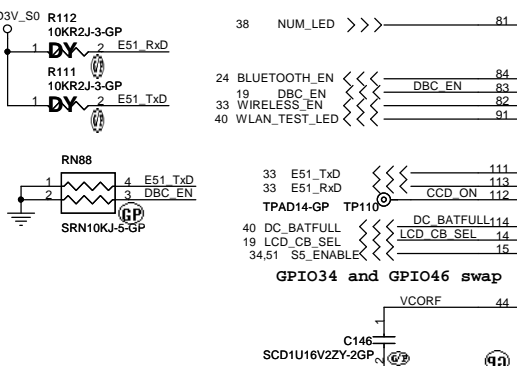
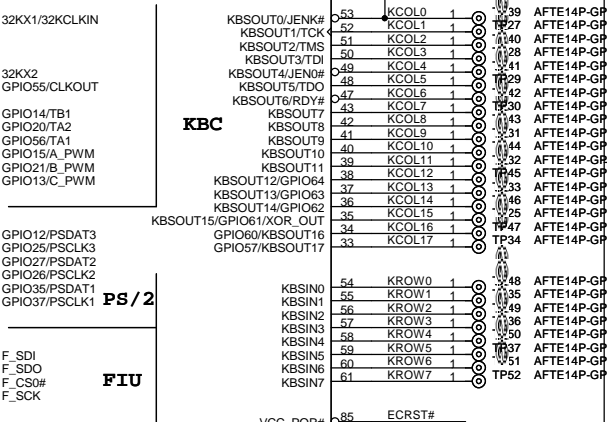
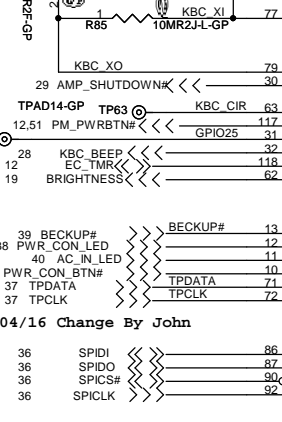
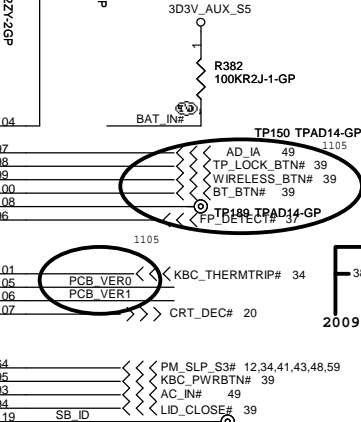
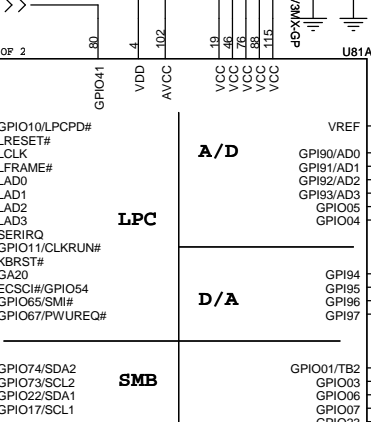
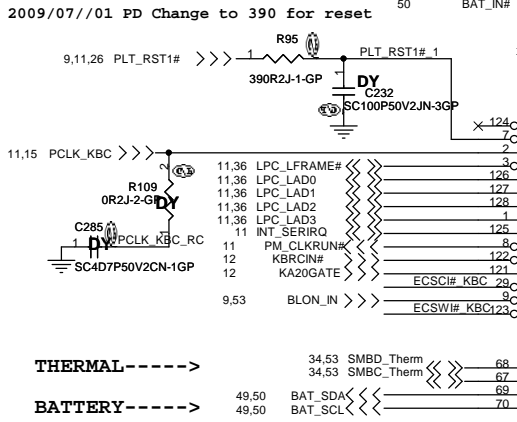
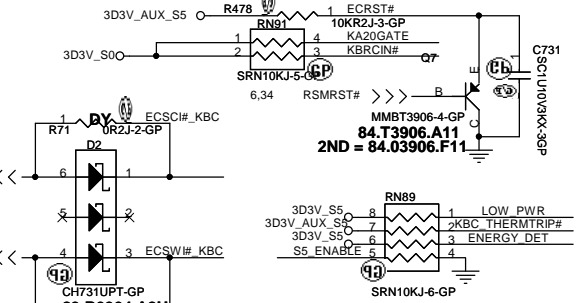
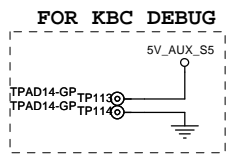
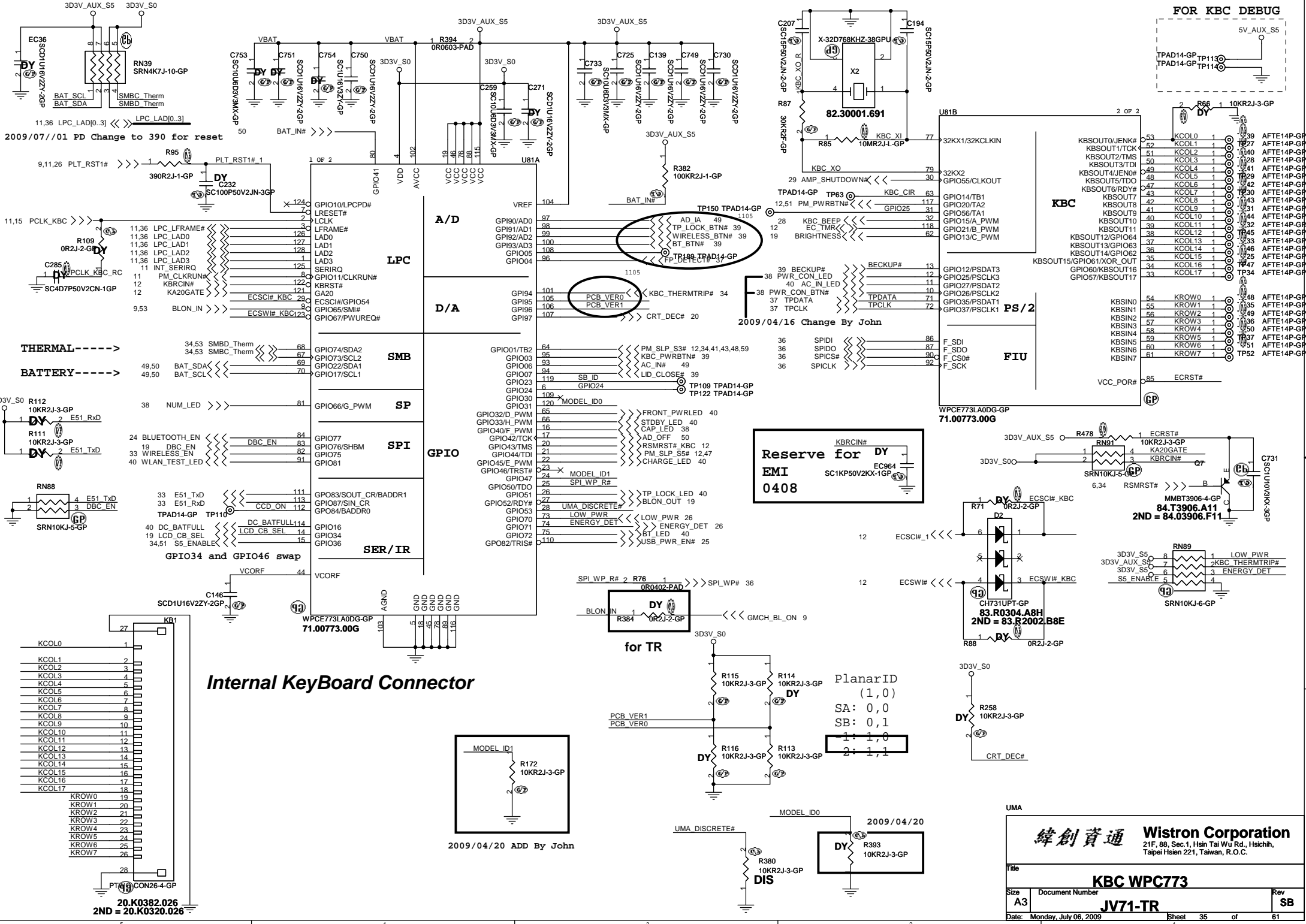
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G792**

Size: A3	Document Number: JV71-TR	Rev: SB
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BAT54CPT-GP
83.R2003.EB1
2ND = 83.BAT54.081



20.K0382.026
2ND = 20.K0320.026

2009/04/20 ADD By John

2009/04/20
R393
10KR2J-3-GP

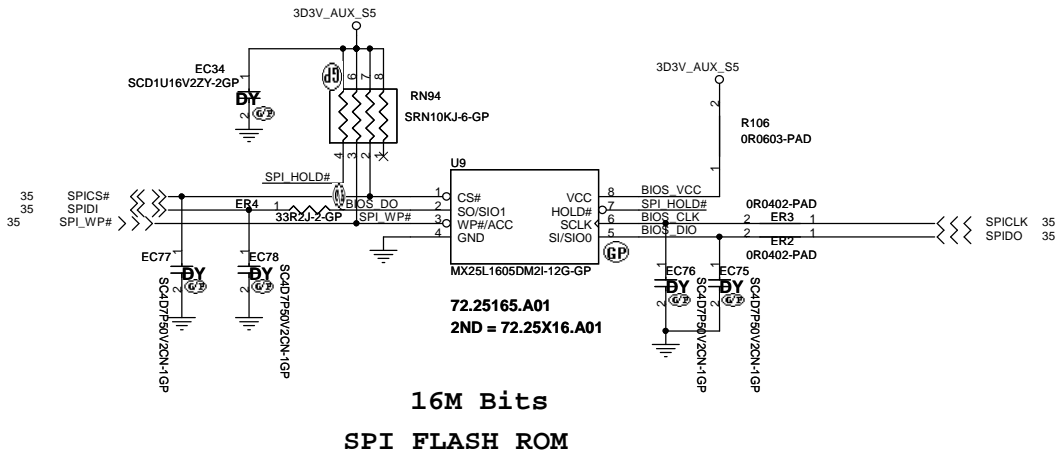
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

KBC WPC773

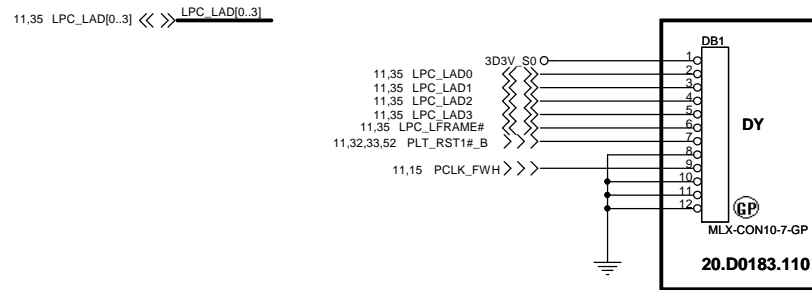
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Size: A3 Document Number: **JV71-TR** Rev: **SB**

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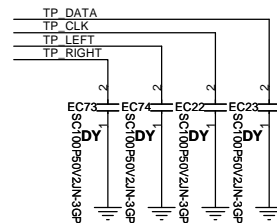
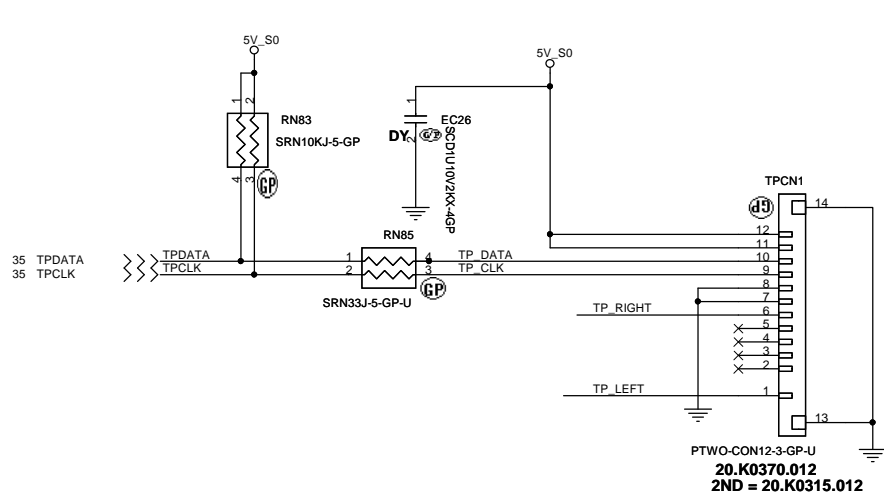
GOLDEN FINGER FOR DEBUG BOARD



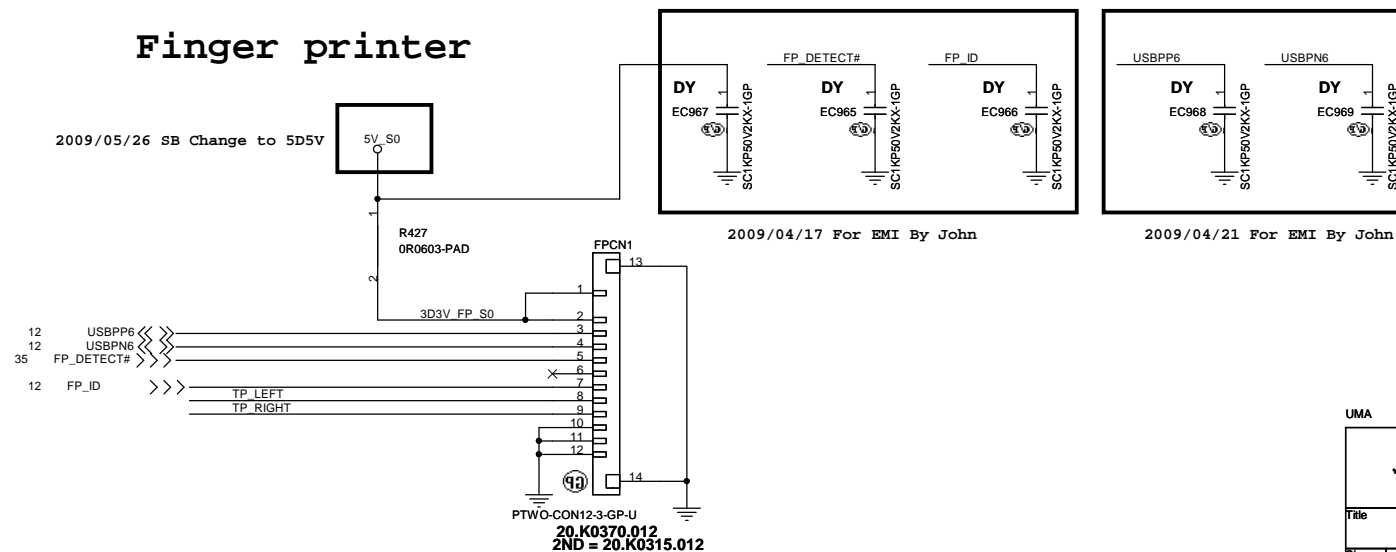
UMA

緯創資通 Wistron Corporation		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
BIOS			
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TOUCH PAD



Finger printer



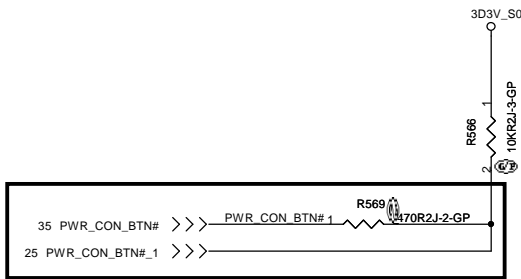
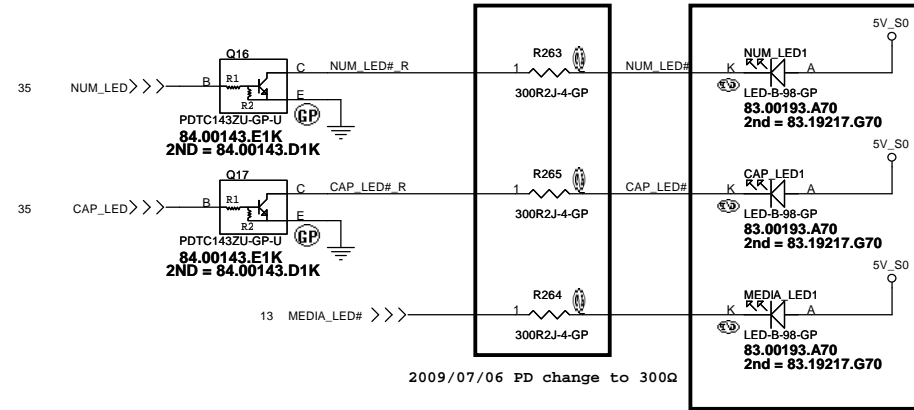
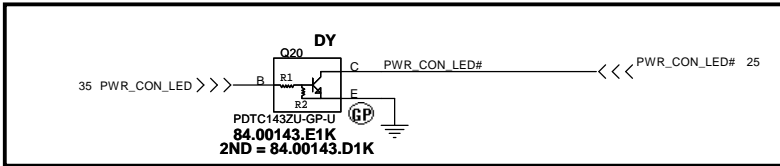
UMA

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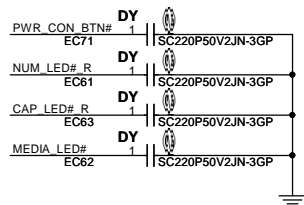
Title: **Touch PAD/Finger printer**

Size: A3	Document Number: JV71-TR	Rev: SB
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2009/04/16 Change By John

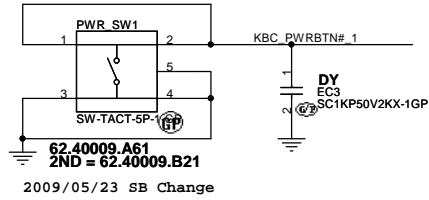


2009/04/16 Change By John

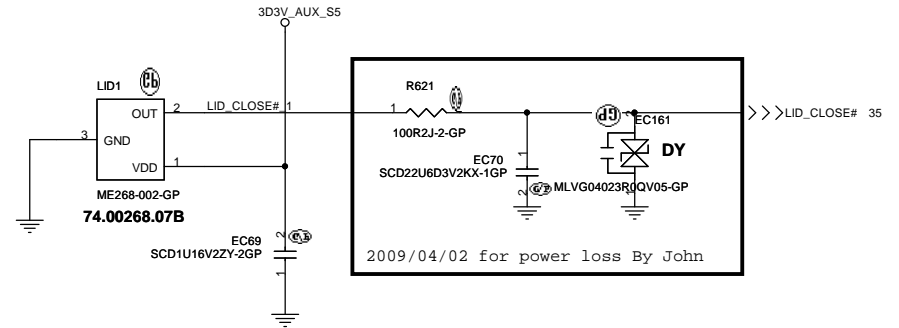


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LAUNCH BOARD	
Title Size A3	Document Number JV71-TR
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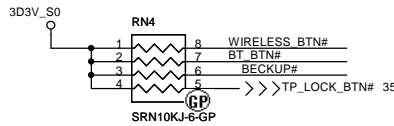
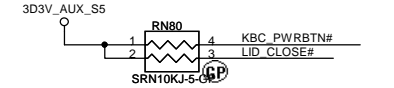
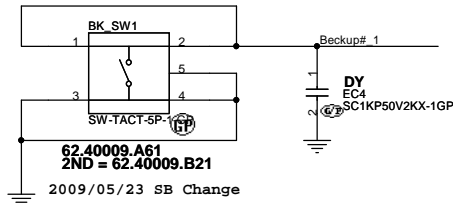
Power Button



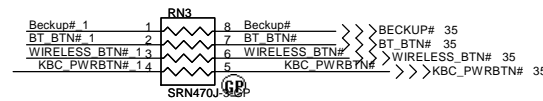
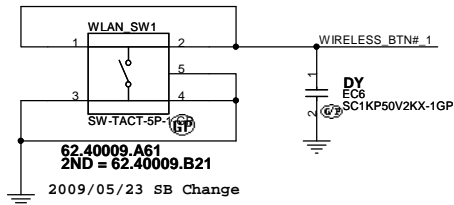
Cover Up Switch



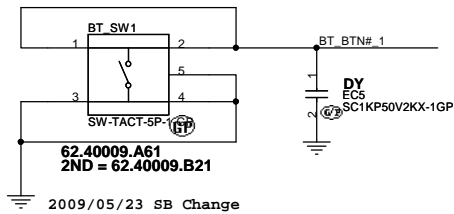
Beckup Button



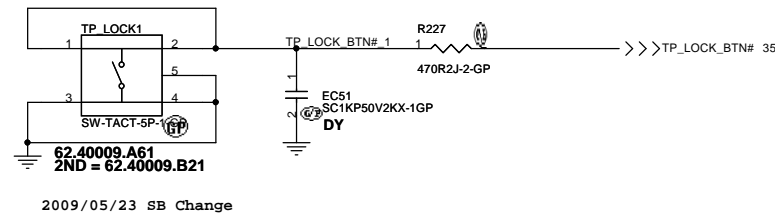
WIRELESS Button

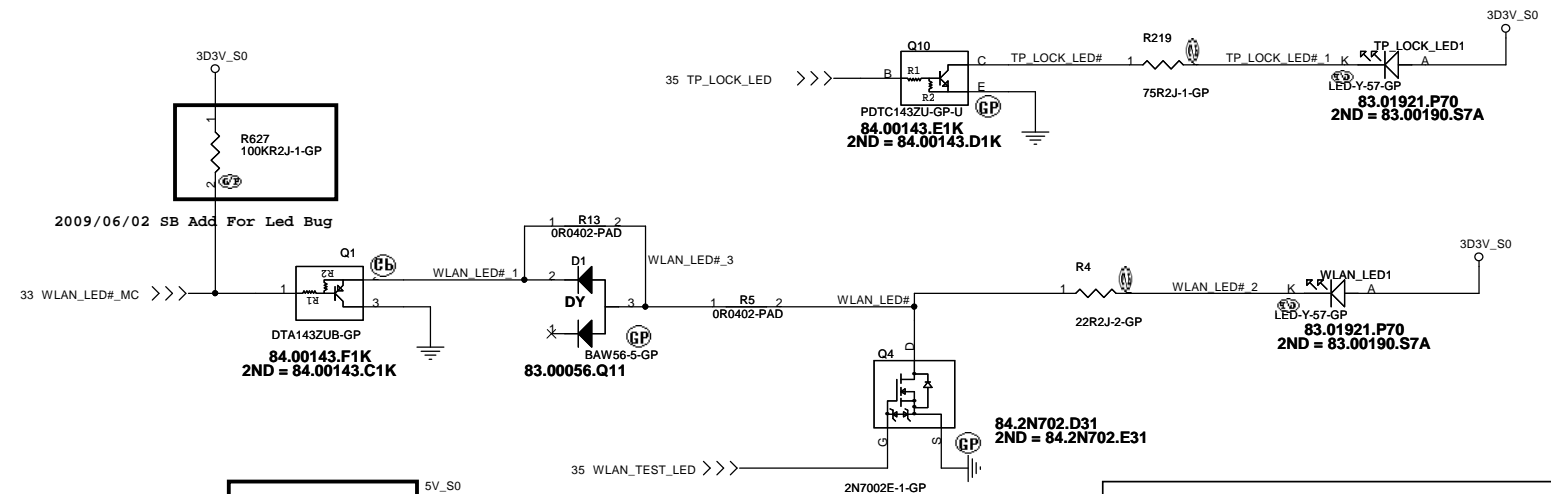
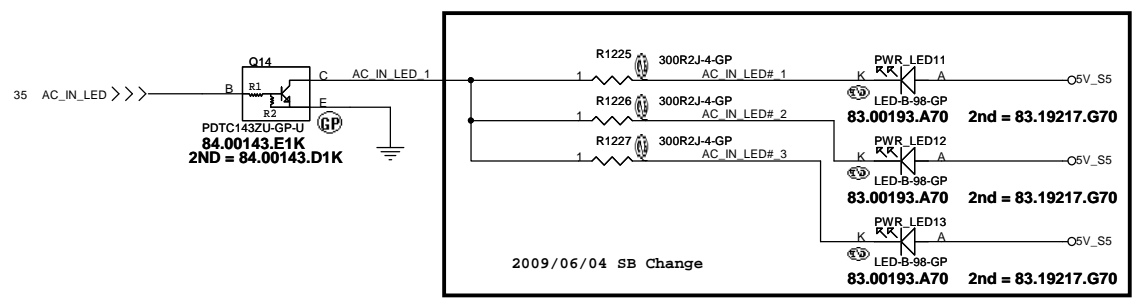
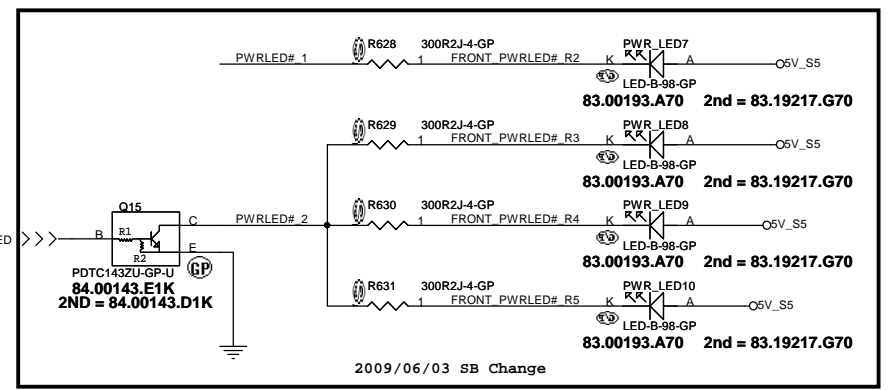
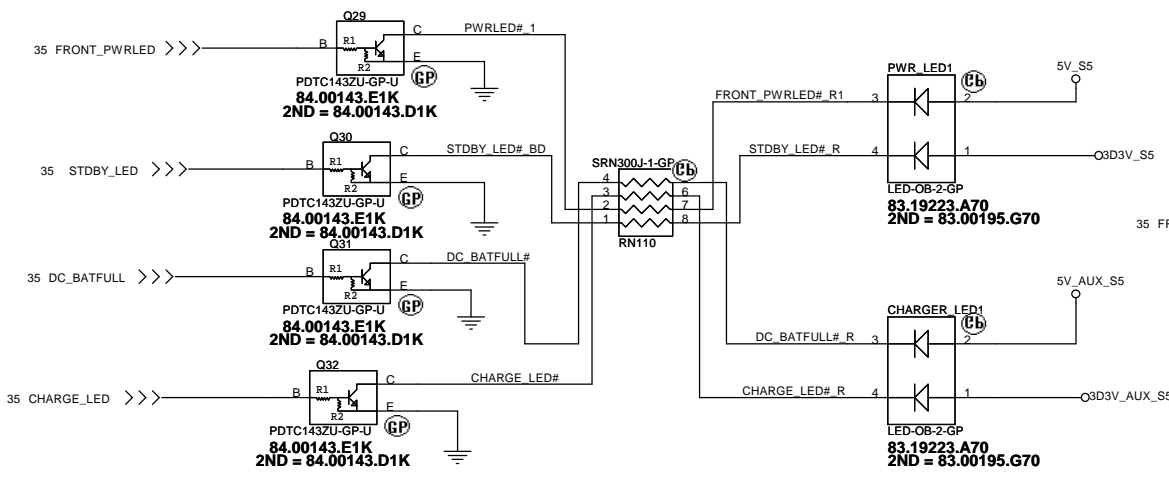


BT/3G Button



T/P lock Button



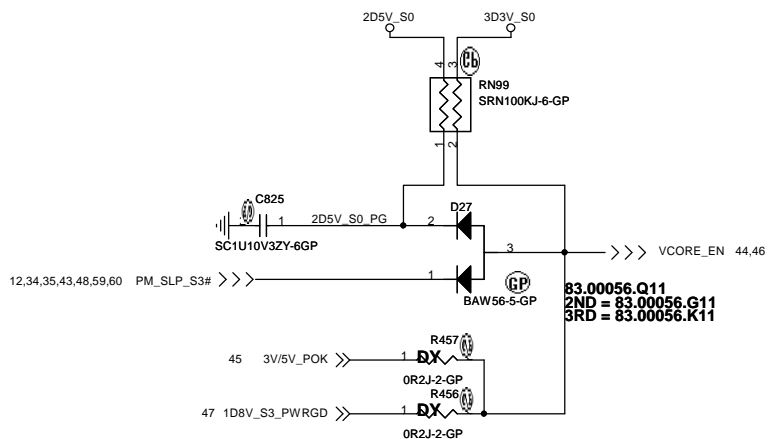


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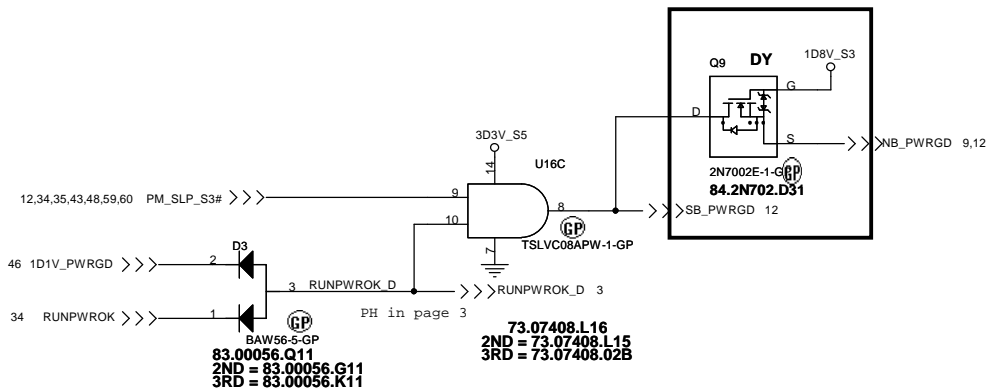
Title: **LED**

Size: A3
 Document Number: **JV71-TR**
 Date: Wednesday, July 08, 2009
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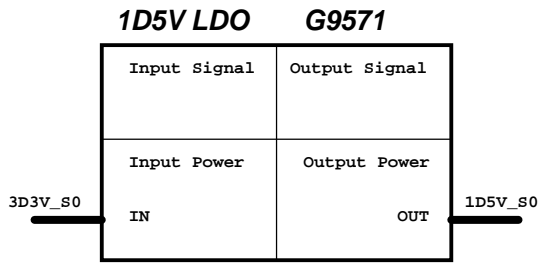
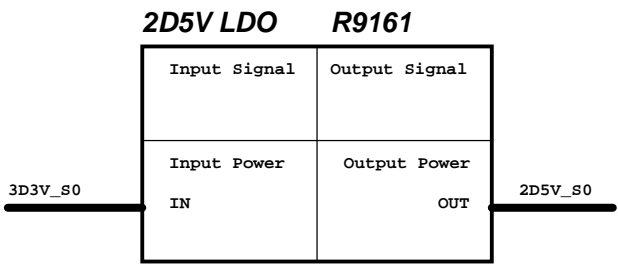
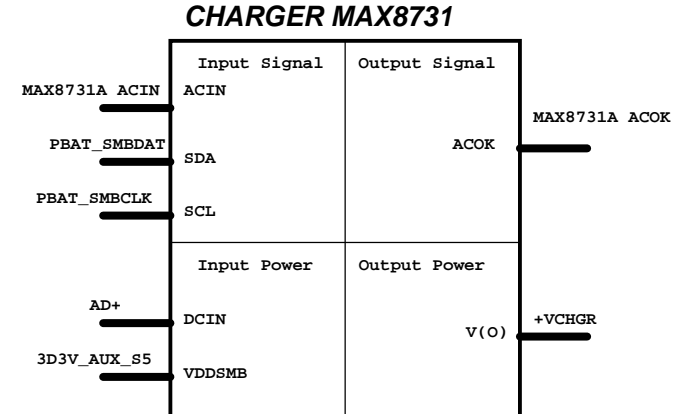
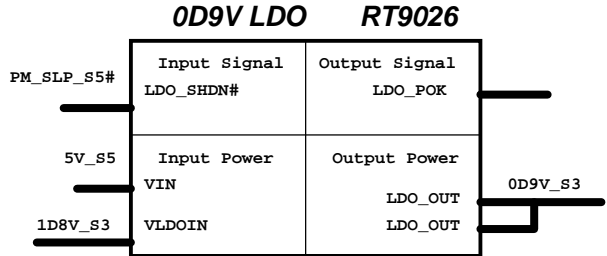
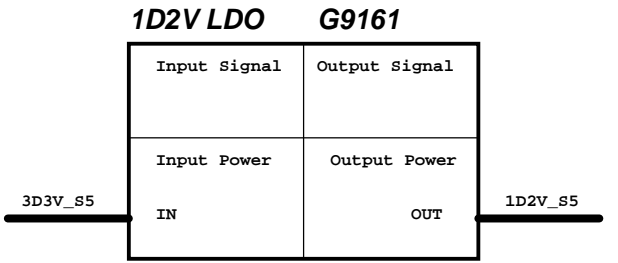
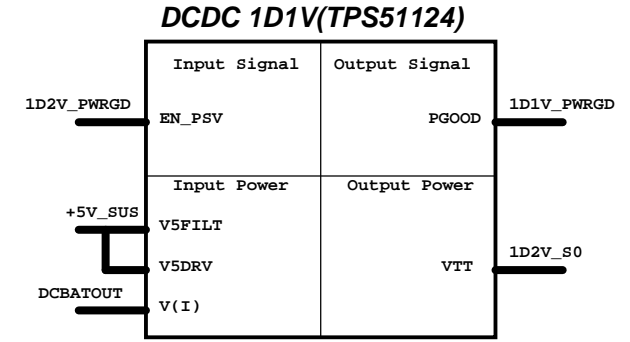
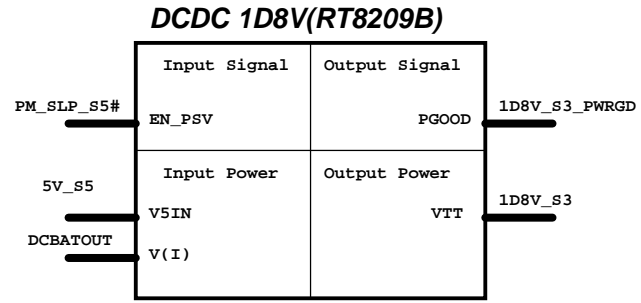
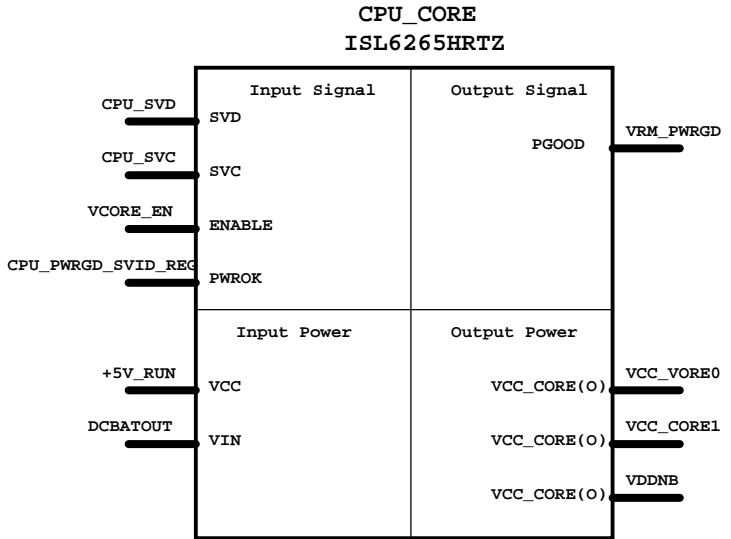
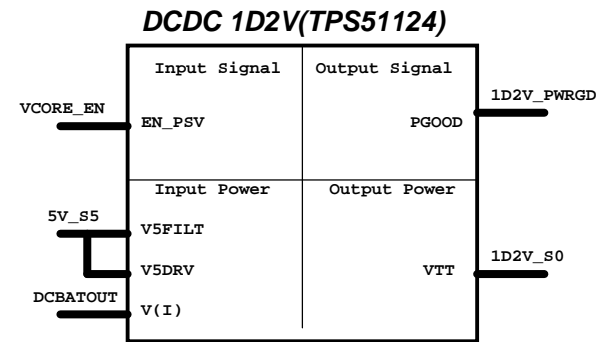
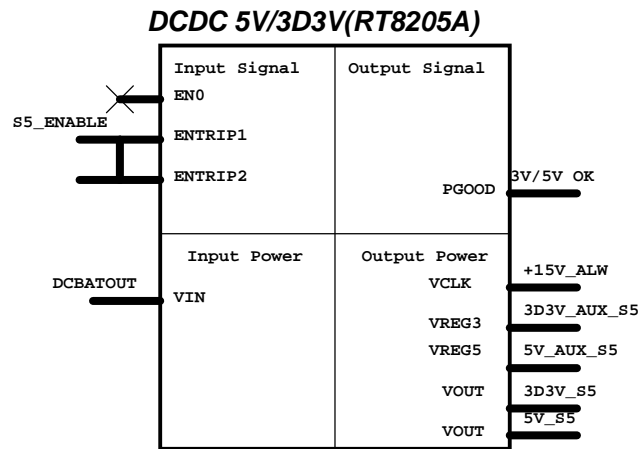
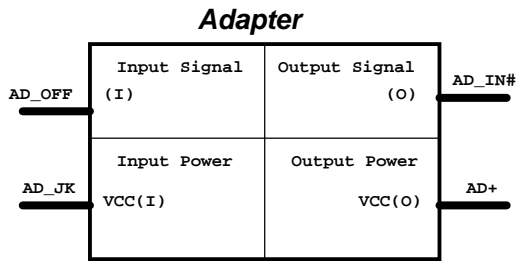
Rev: **SB**



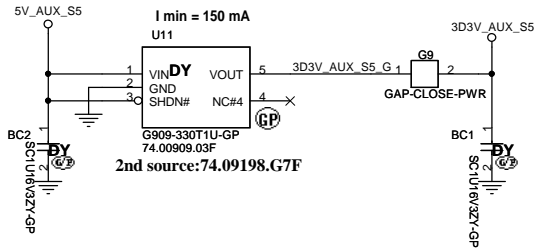
P/H @ 1D8V_S3 PAGE



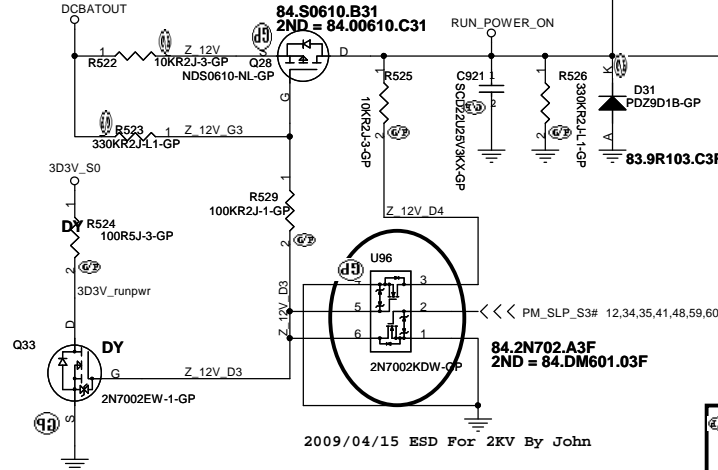
UMA



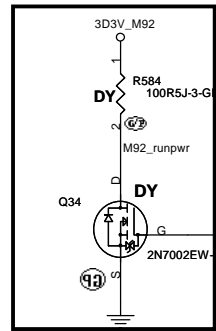
Aux Power 3D3V_AUX_S5



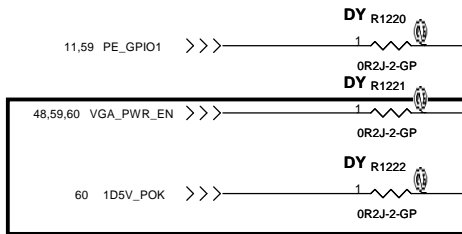
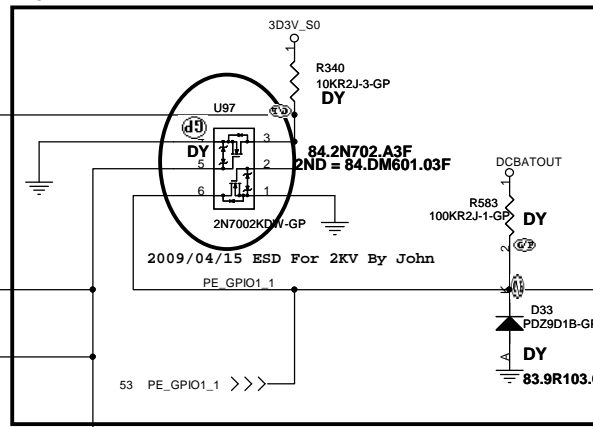
Run Power



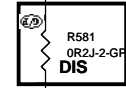
for TR



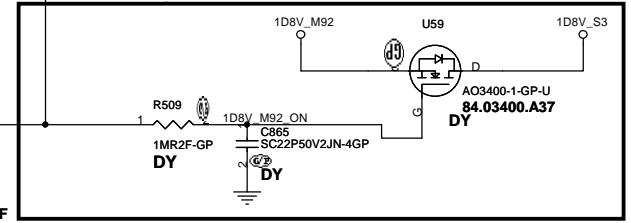
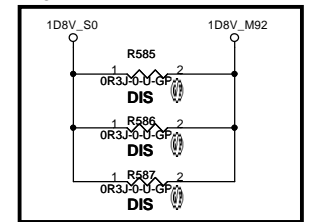
for TR



2009/04/21 ADD By John



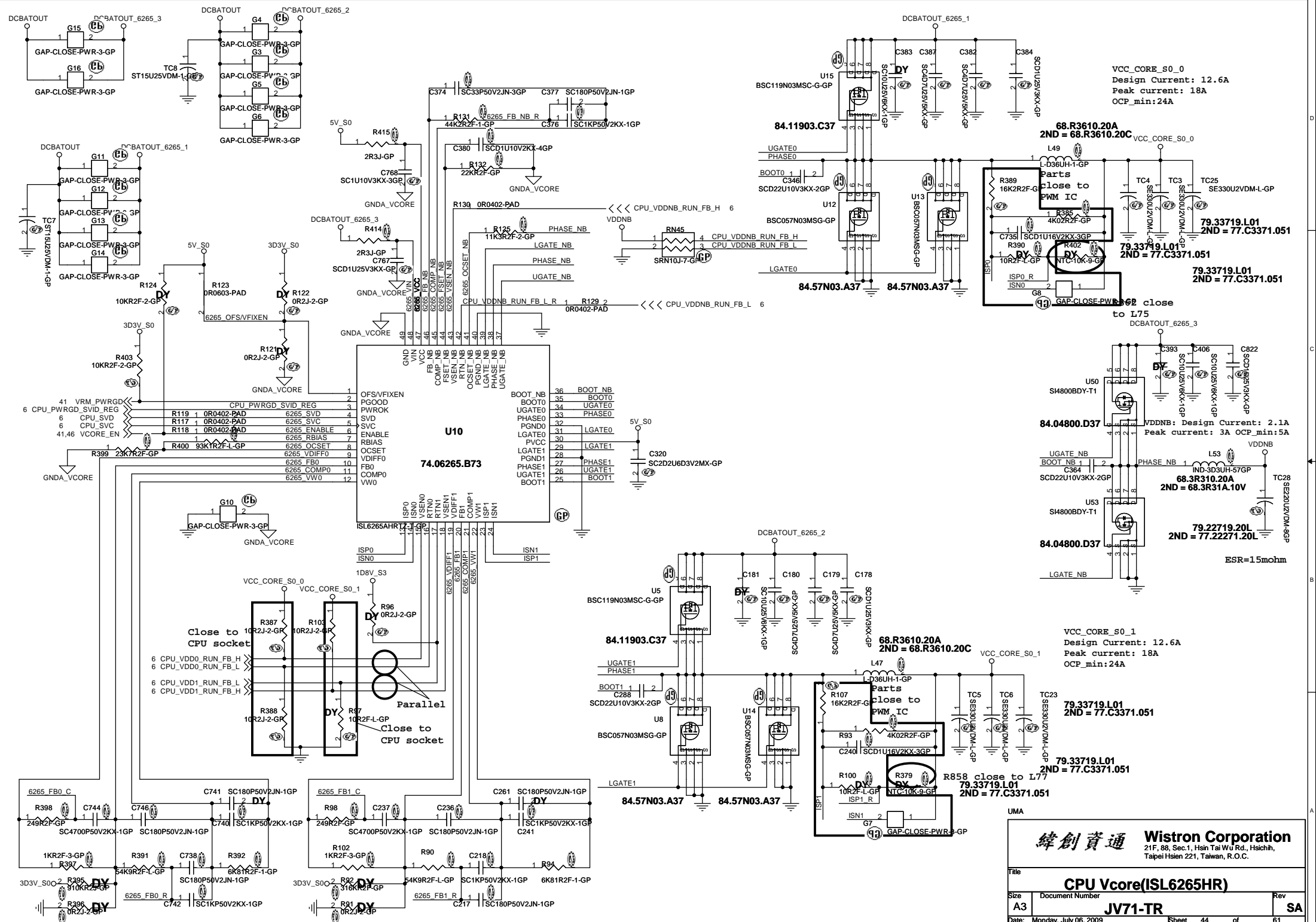
for TR



R509, R342 - 10MΩ
 C865 - 22pF
 C675 - 1000pF
 For VGA sequence issue

UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TITLE	
RUN AND AUX POWER	
Size A3	Document Number JV71-TR
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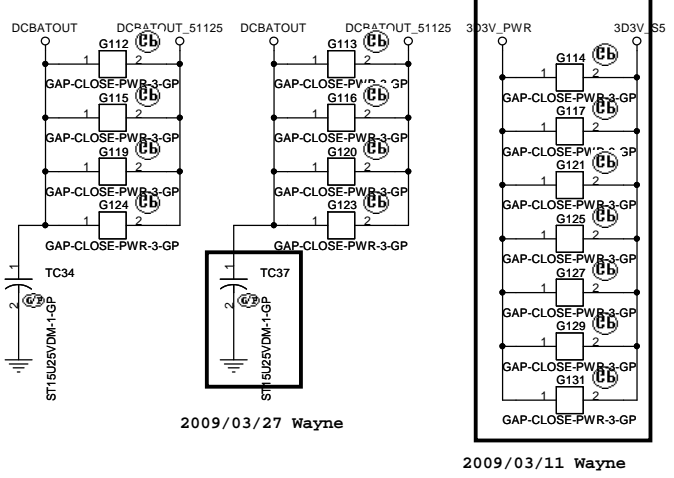


VCC_CORE_S0_0
 Design Current: 12.6A
 Peak current: 18A
 OCP_min:24A

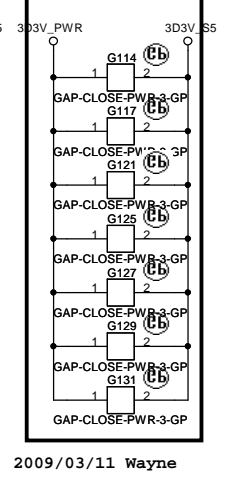
VDDNB: Design Current: 2.1A
 Peak current: 3A OCP_min:5A

VCC_CORE_S0_1
 Design Current: 12.6A
 Peak current: 18A
 OCP_min:24A

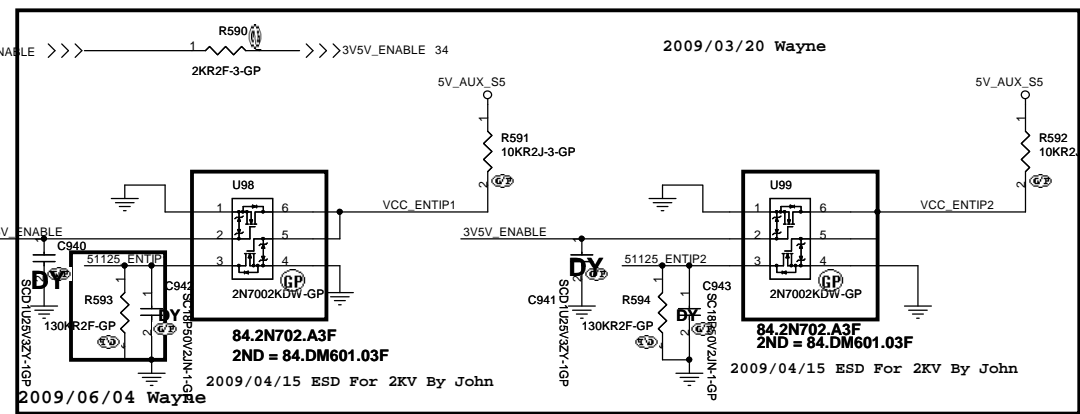
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU Vcore(ISL6265HR)	
File	Rev
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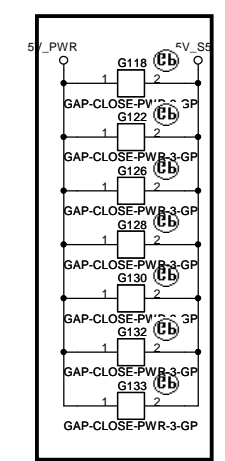
2009/03/27 Wayne



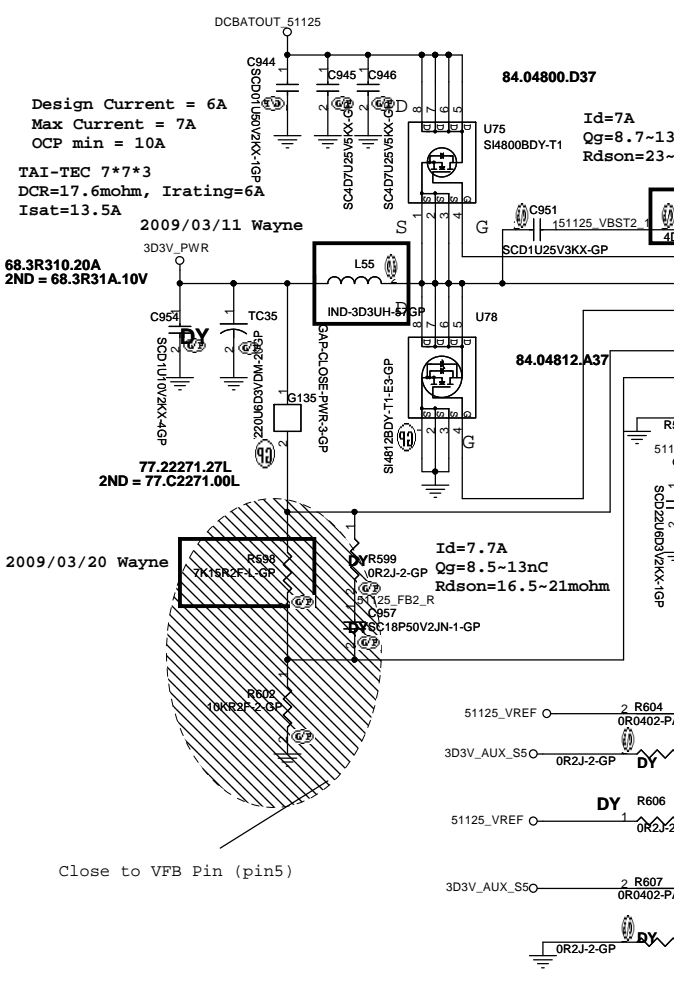
2009/03/11 Wayne



2009/06/04 Wayne
2009/04/15 ESD For 2KV By John



2009/03/11 Wayne



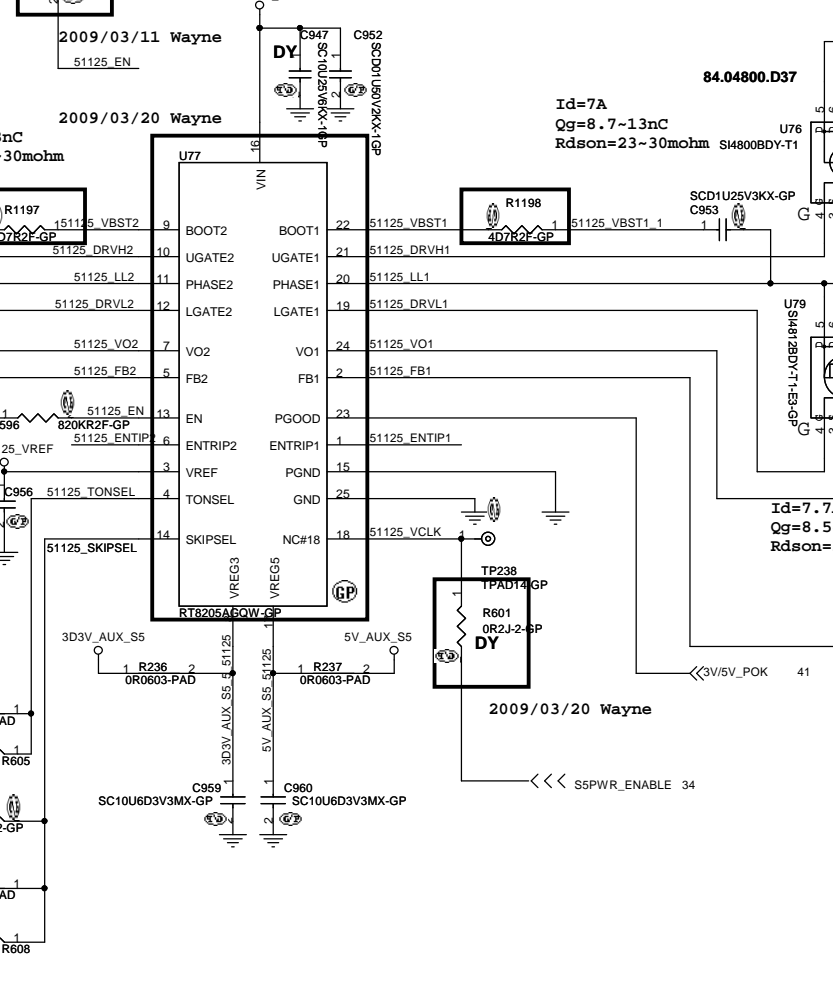
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A

2009/03/11 Wayne

68.3R310.20A
2ND = 68.3R31A.10V

2009/03/20 Wayne

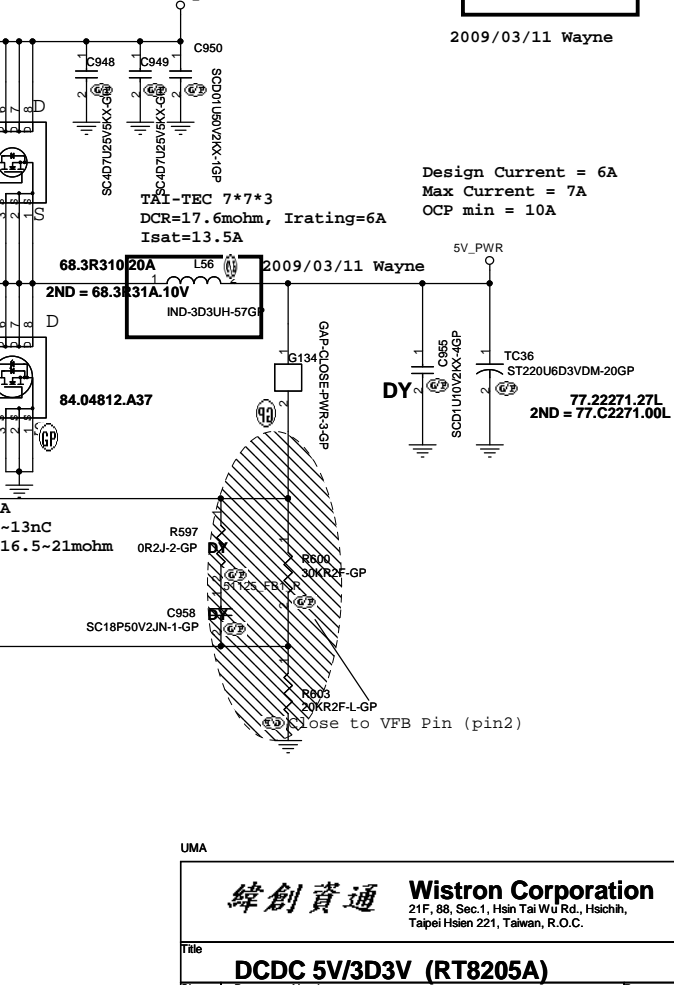
Close to VFB Pin (pin5)



2009/03/20 Wayne

Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

2009/03/20 Wayne



Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

68.3R310.20A
2ND = 68.3R31A.10V

2009/03/20 Wayne

Close to VFB Pin (pin2)

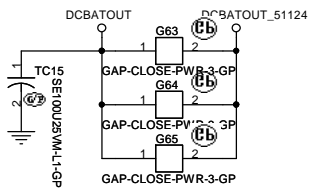
UMA

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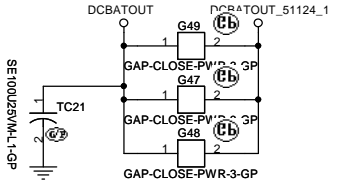
Title: **DCDC 5V/3D3V (RT8205A)**

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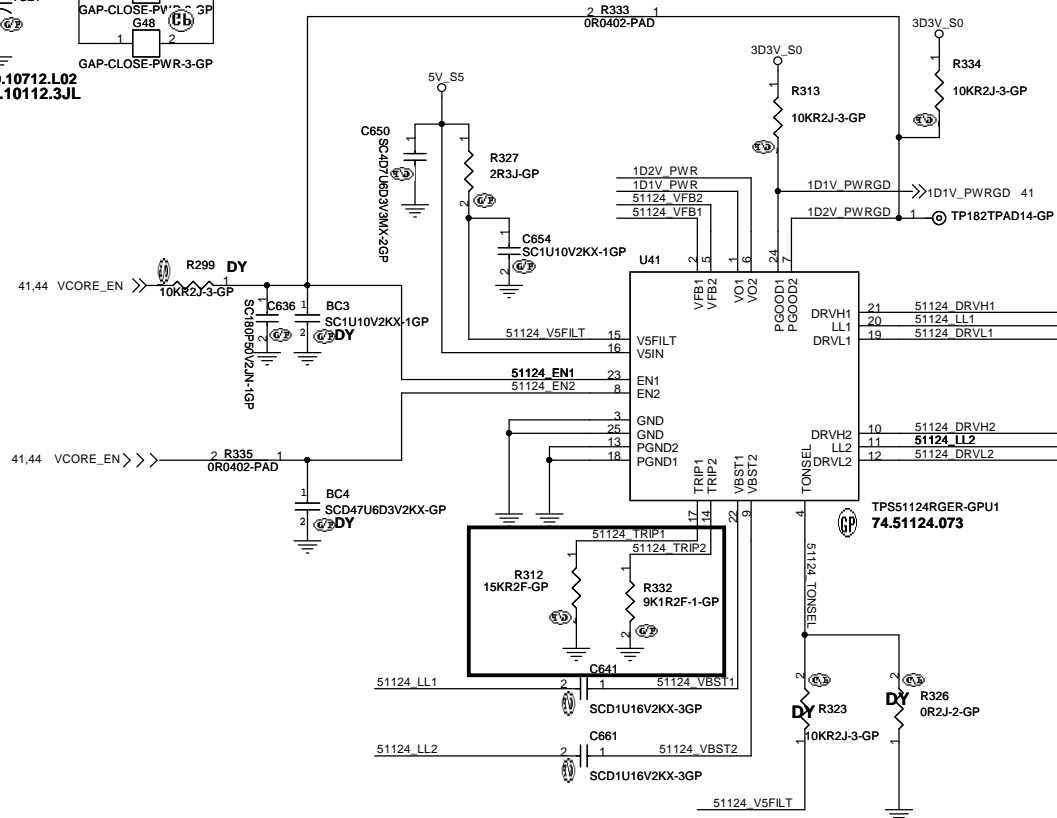
79.10712.L02
2ND = 79.10112.3JL



79.10712.L02
2ND = 79.10112.3JL

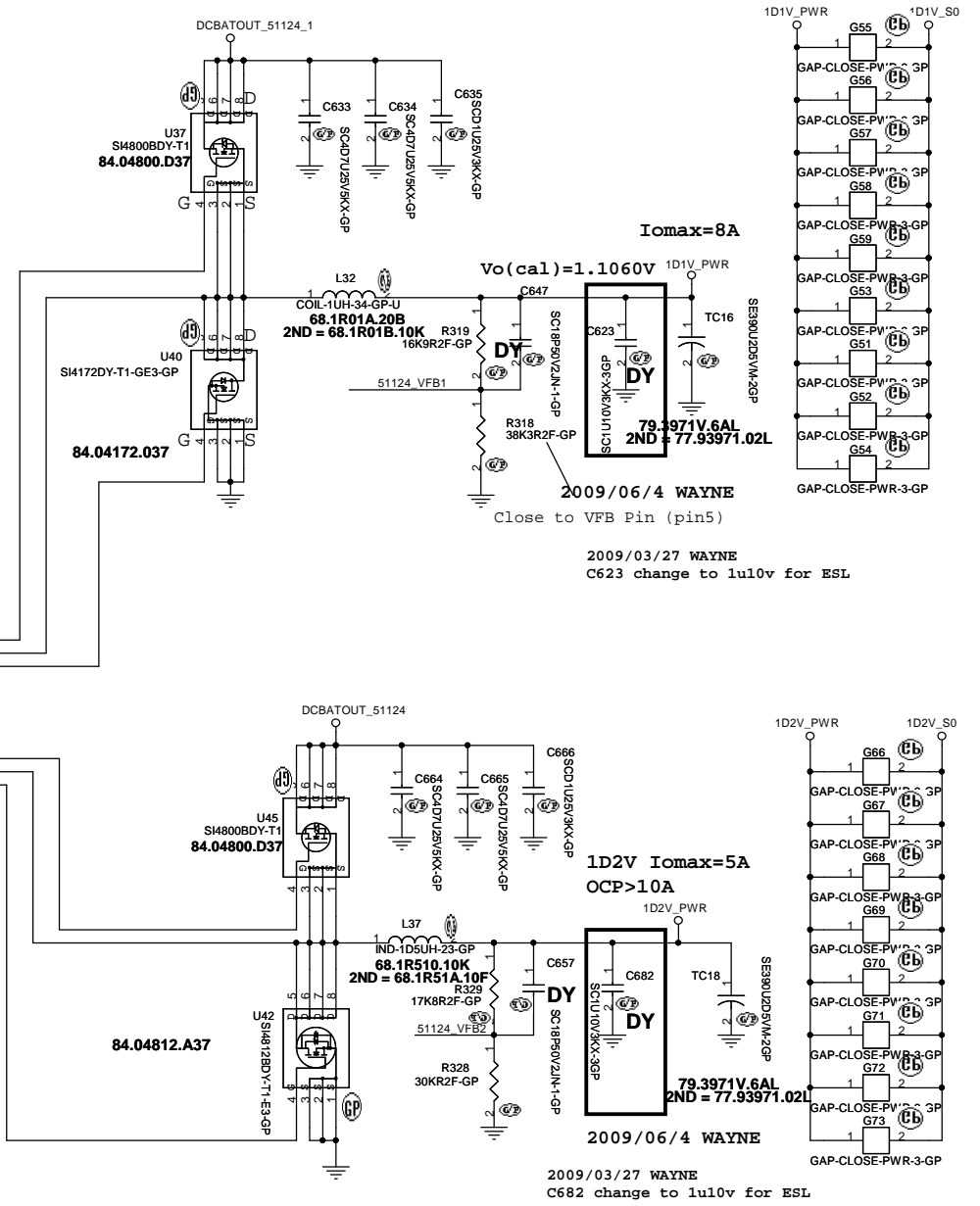
$$V_{trip}(mV) = R_{trip}(Kohm) * I_0(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



$V_o(cal) = 1.1060V$

$I_{omax} = 8A$

79.3971V.6AL
2ND = 77.93971.02L

2009/06/4 WAYNE
Close to VFB Pin (pin5)

2009/03/27 WAYNE
C623 change to 1u10v for ESL

1D2V $I_{omax} = 5A$
OCP > 10A

79.3971V.6AL
2ND = 77.93971.02L

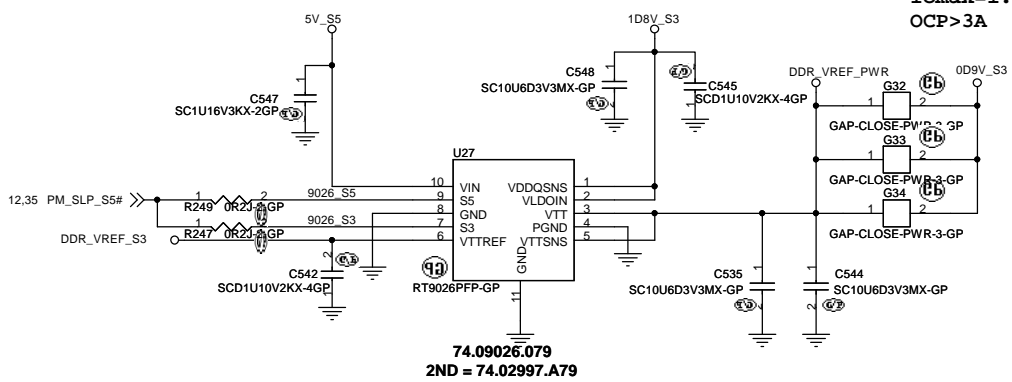
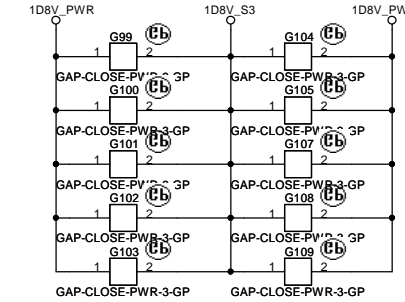
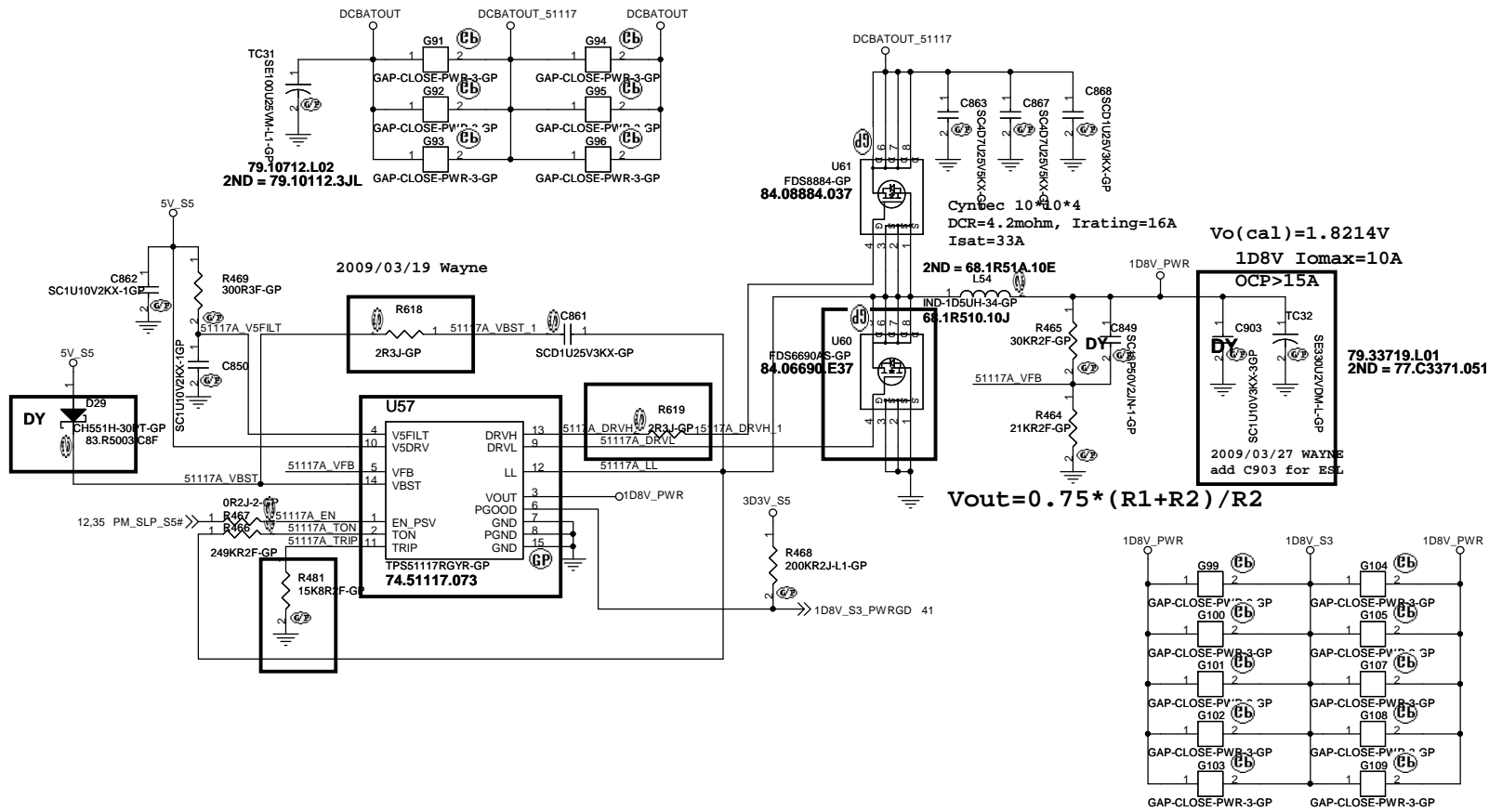
2009/06/4 WAYNE
2009/03/27 WAYNE
C682 change to 1u10v for ESL

UMA

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Title: **TPS51124 1D1V 1D2V**

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UMA

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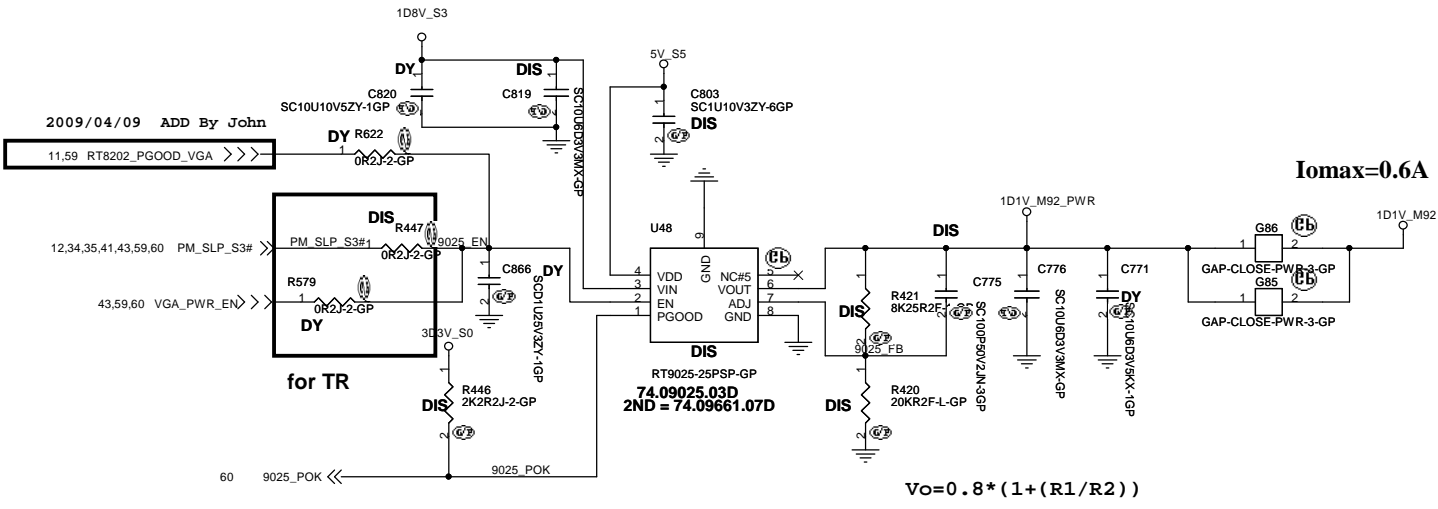
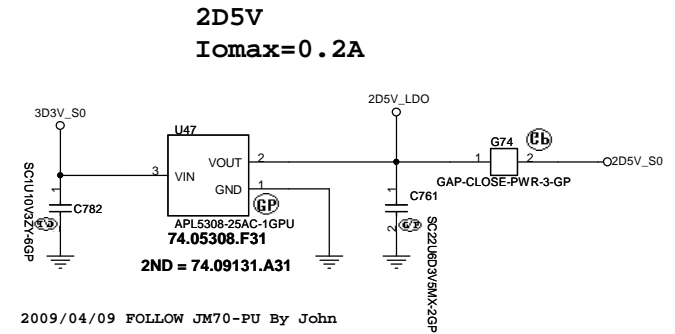
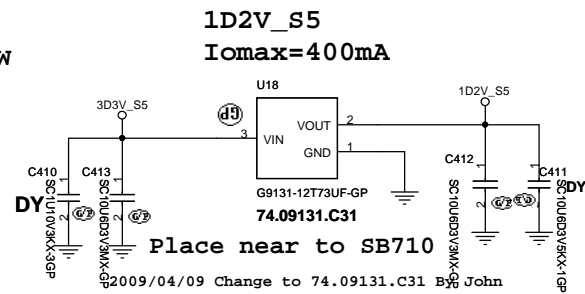
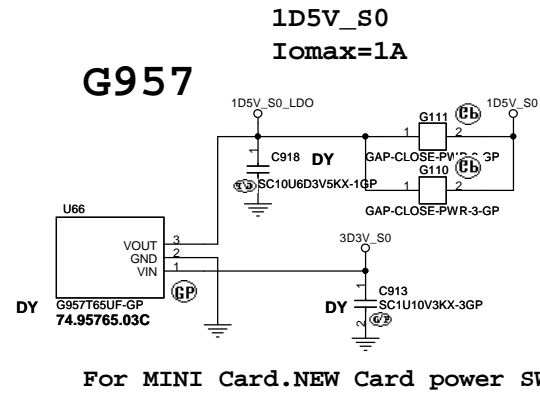
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Size: A3
Date: Monday, July 06, 2009

Document Number: **JV71-TR**

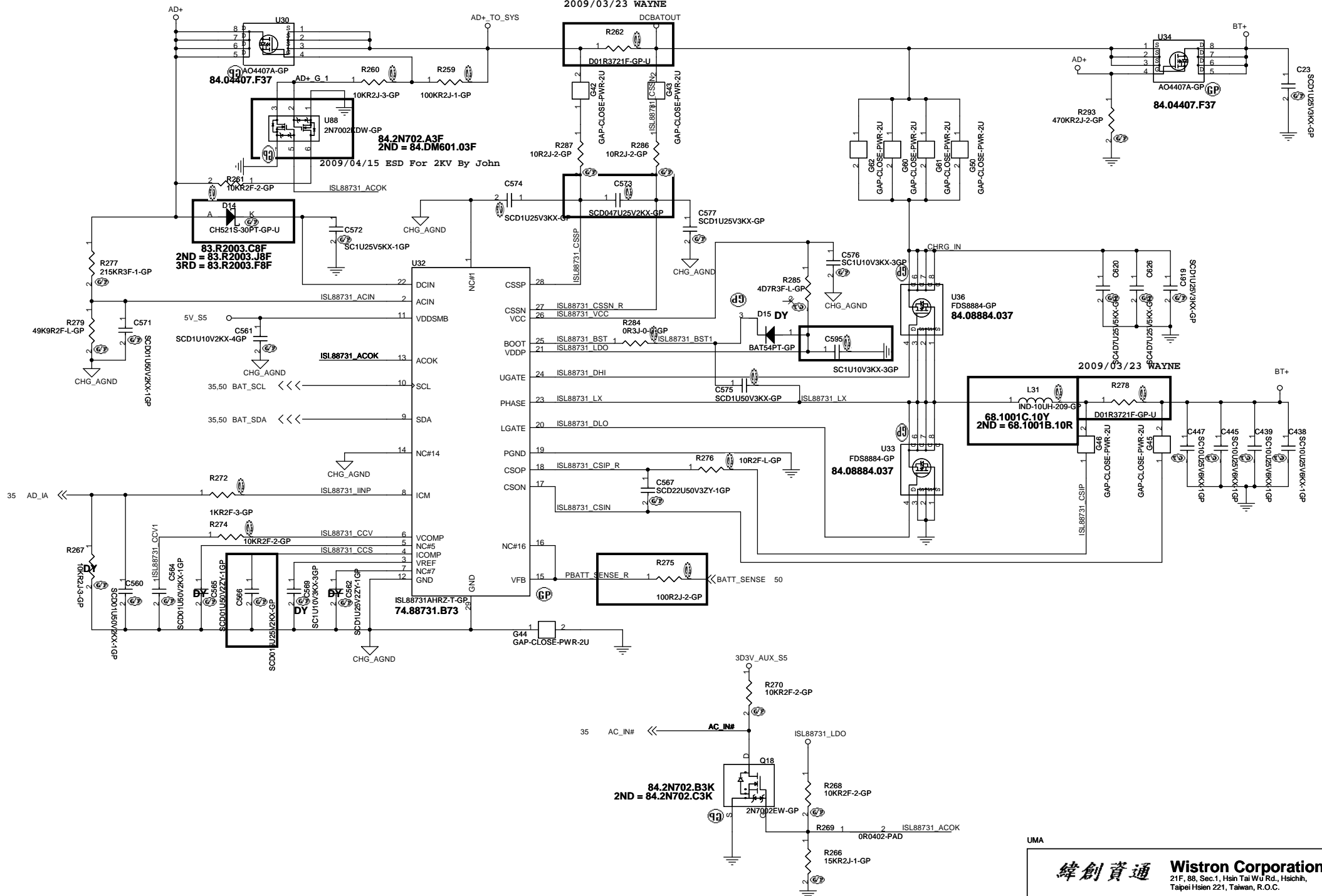
Rev: **SA**

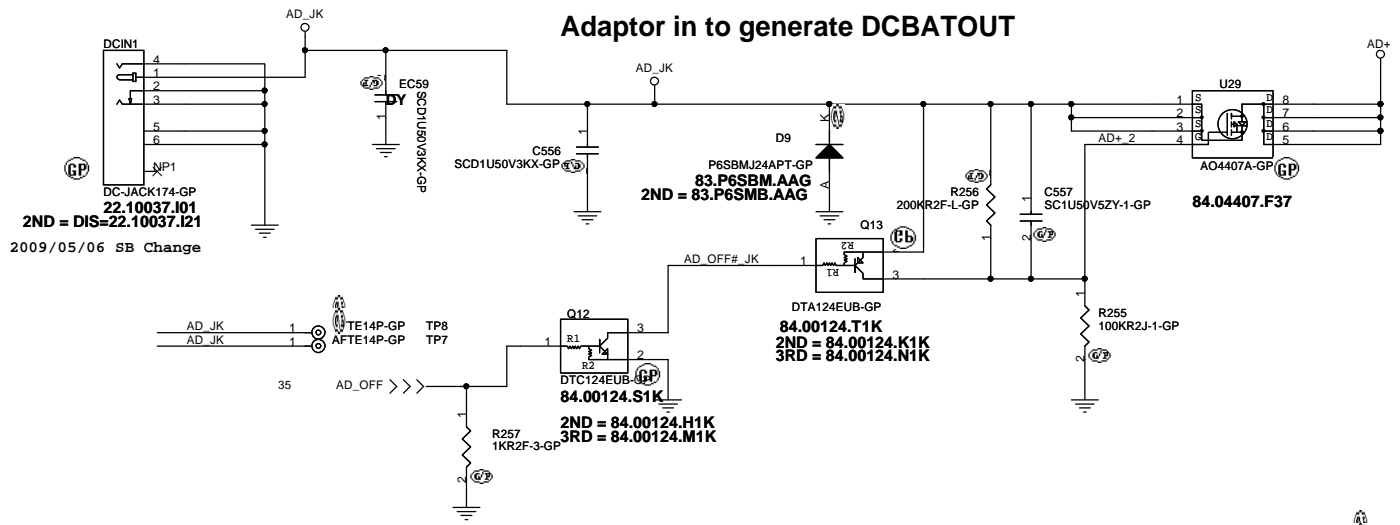
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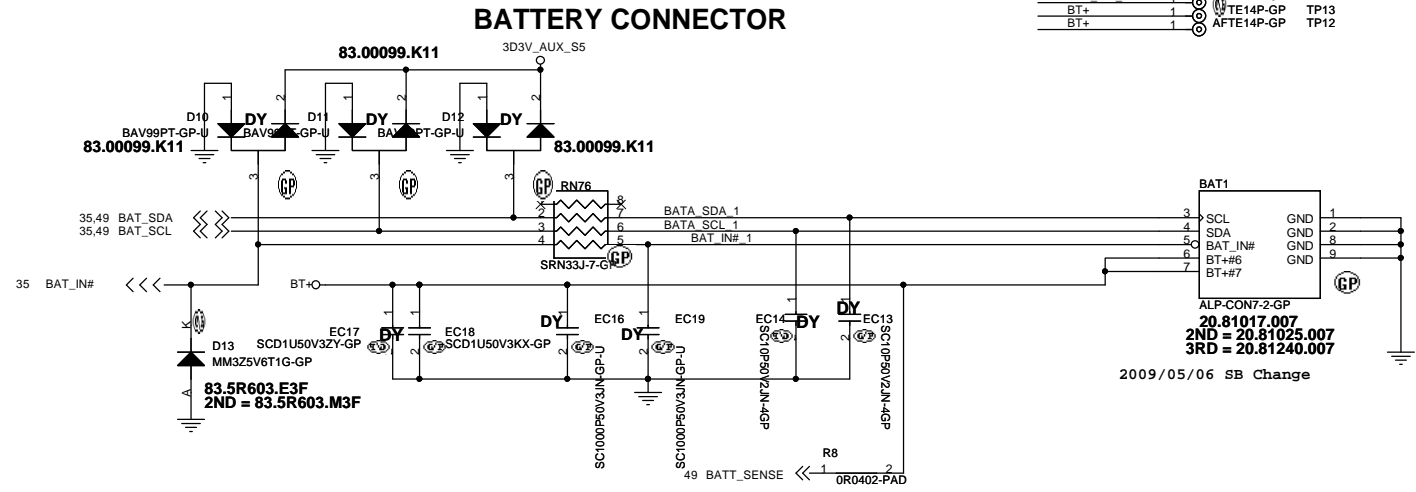
UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LDO 2D5V/1D5V/1D2V S5/1D1V M92			
Size	Document Number	Rev	
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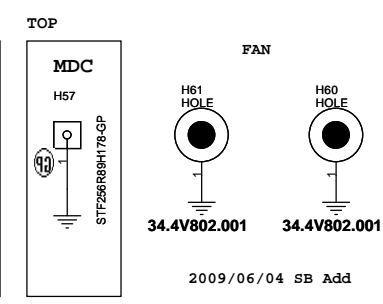
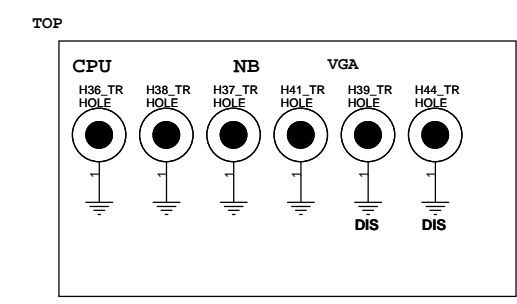
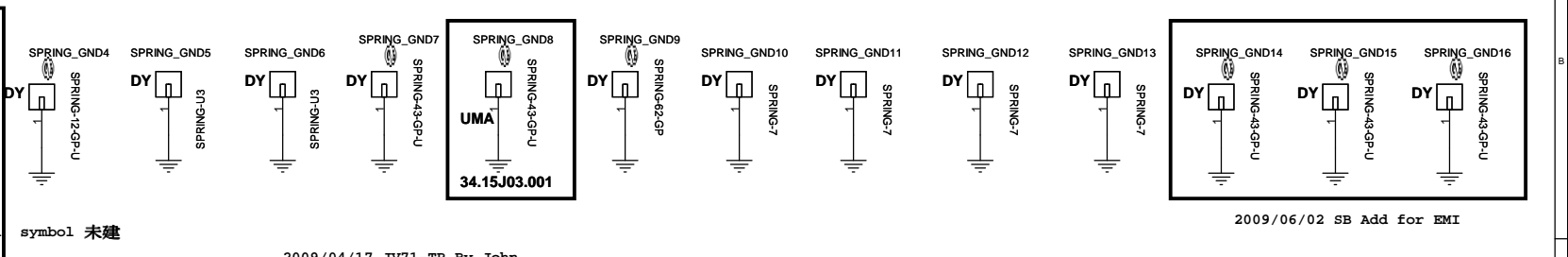
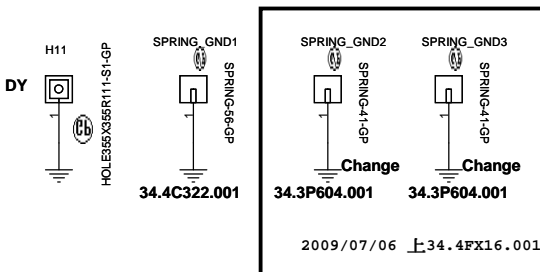
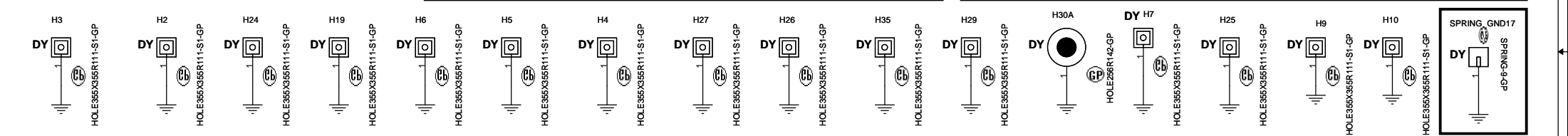
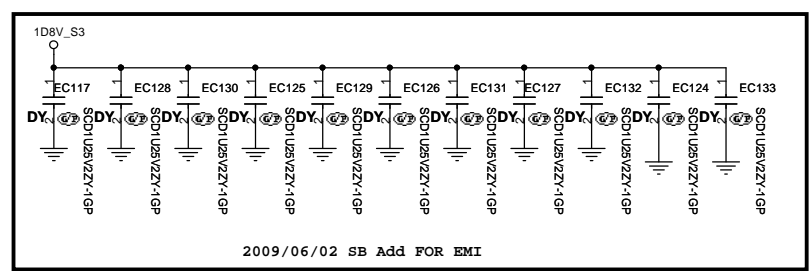
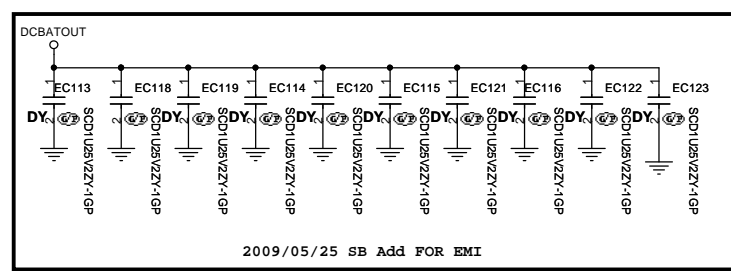
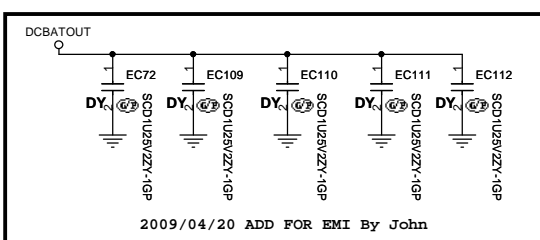
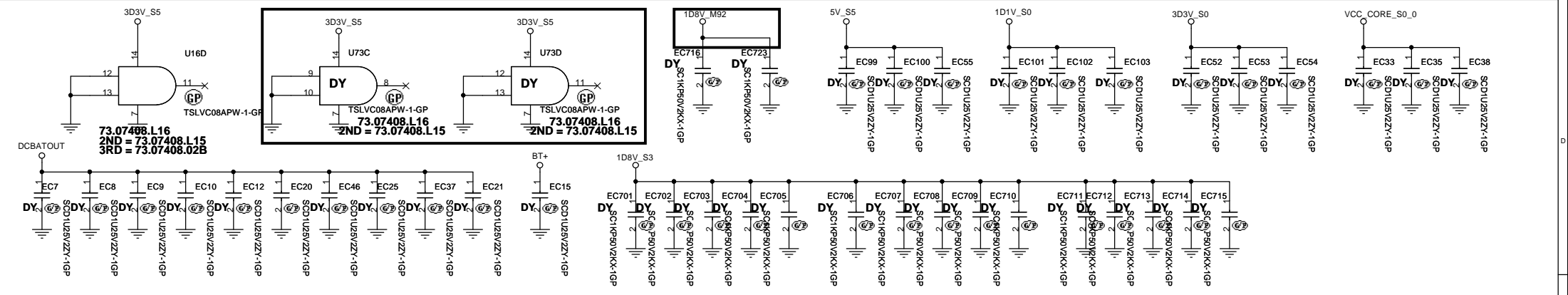
2009/03/23 WAYNE





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BATA_SCL_1	1	TE14P-GP	TP10
BAT_IN#_1	1	TE14P-GP	TP11
BT+	1	TE14P-GP	TP13
BT+	1	AFTE14P-GP	TP12

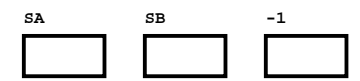




Check test point

3D3V_S0	TP233	TPAD14-GP
3D3V_AUX_S5	TP232	TPAD14-GP
3D3V_S50	TP231	TPAD14-GP
5V_S5	TP230	TPAD14-GP
12,35 PM_PWRBTN#	TP229	TPAD14-GP
6,11 CPU_PWRGD	TP228	TPAD14-GP
34,35 S5_ENABLE	TP227	TPAD14-GP
6,11 CPU_LDT_RST#	TP226	TPAD14-GP

Test Point放在Dimm Door打開可量測處



UMA

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File: **EMI/Spring/Boss**

Size: Document Number **JV71-TR** Rev **SB**

Date: Friday, July 10, 2009 Sheet 51 of 61

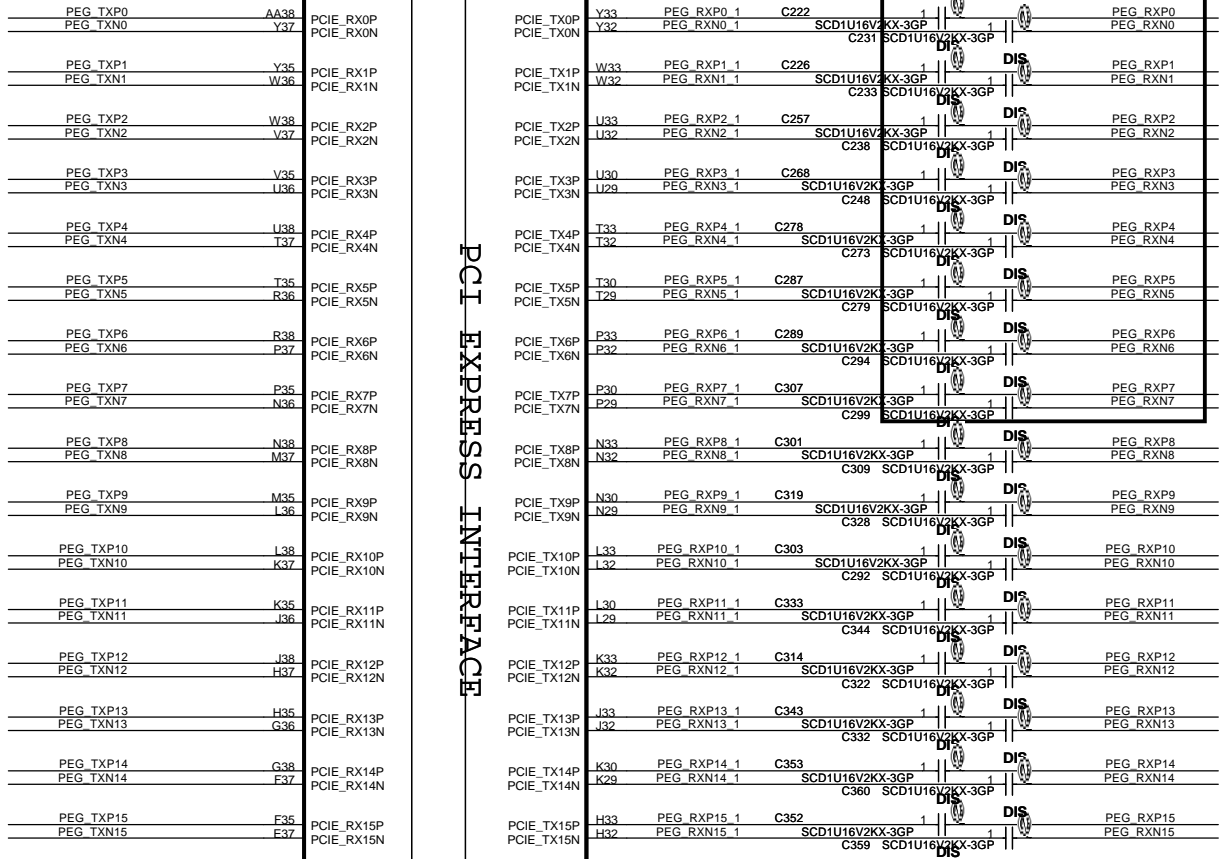
8 PEG_TXP[15..0] << PEG_TXP[15..0]
 8 PEG_TXN[15..0] << PEG_TXN[15..0]

8 PEG_RXP[15..0] << PEG_RXP[15..0]
 8 PEG_RXN[15..0] << PEG_RXN[15..0]

AVGA1A 1 OF 8

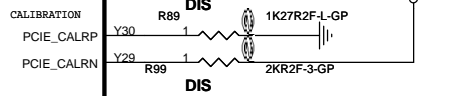
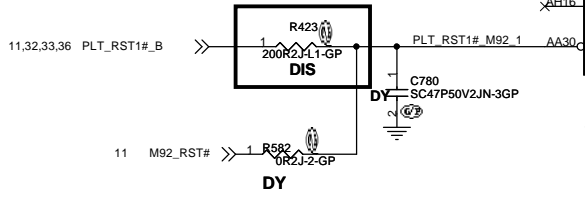
PCI EXPRESS INTERFACE

for TR



3 CLK_PCIE_PEG << AB35
 3 CLK_PCIE_PEG# << AA36

2009/07/01 PD Change to 200 for reset



UMA

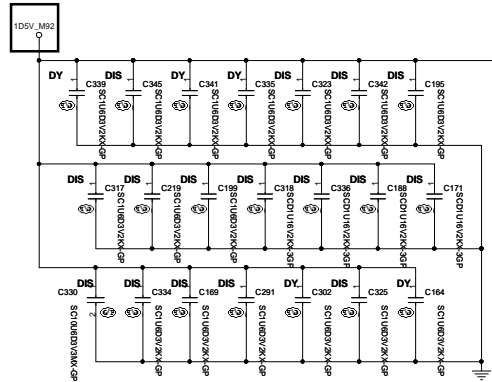
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **M92 PCIE**

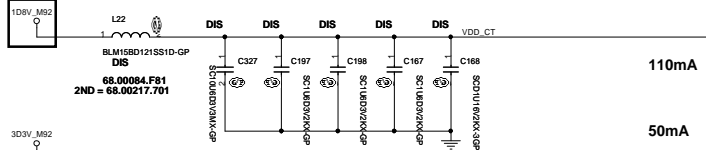
Size: A3 Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 52 of 61

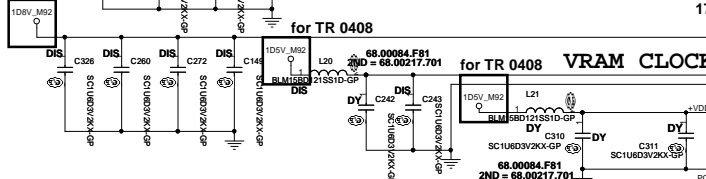
for TR 0408 VDDR1+VDDRHX 1.50 V (DDR3 700 Mhz) 0.93 A (RMS) / 1.2 A (peak)



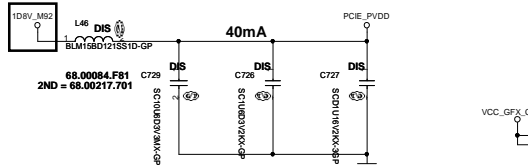
for TR



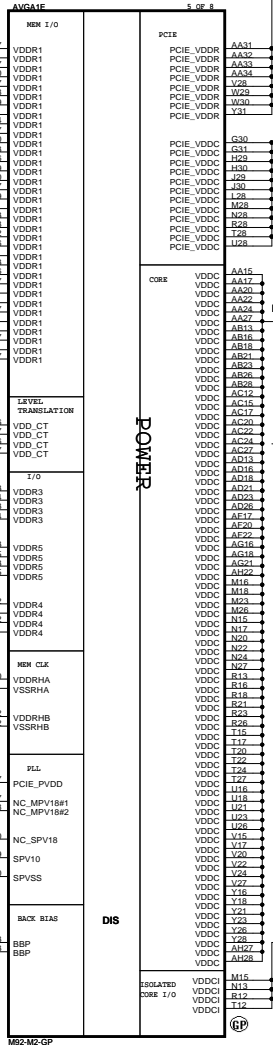
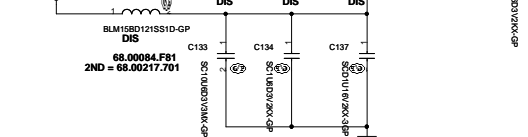
for TR



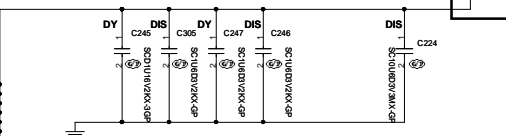
for TR



for TR



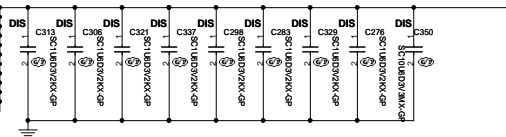
362mA



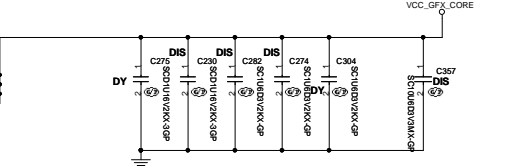
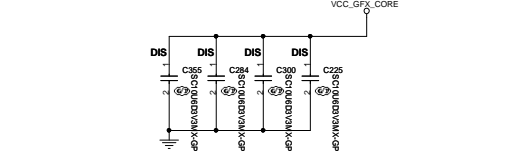
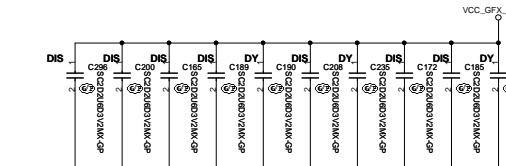
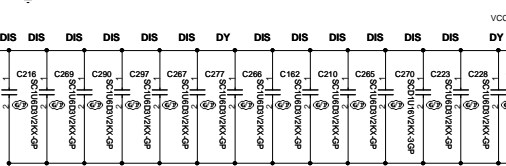
for TR



1400mA



108V_M92



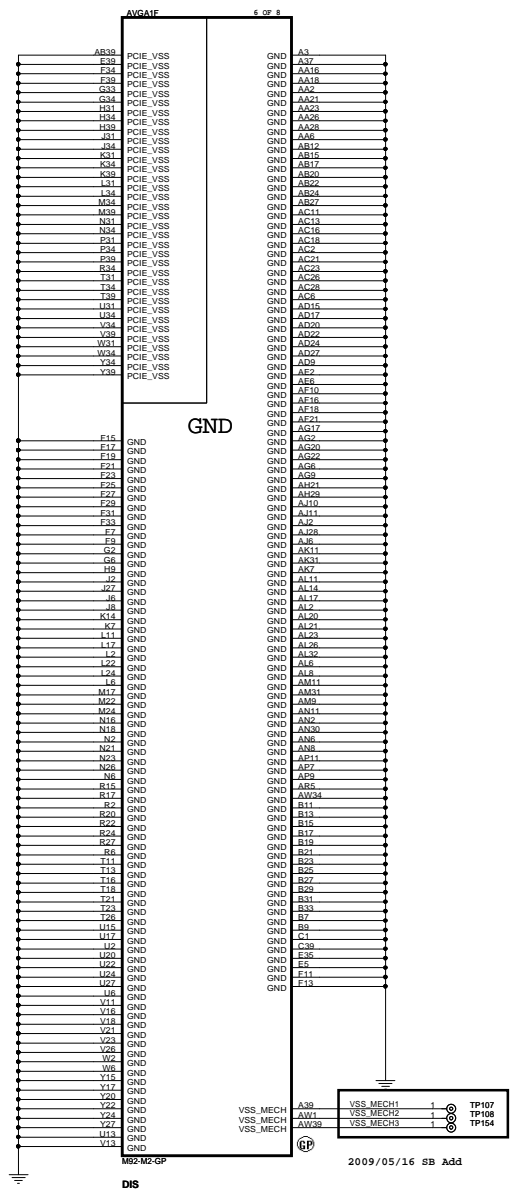
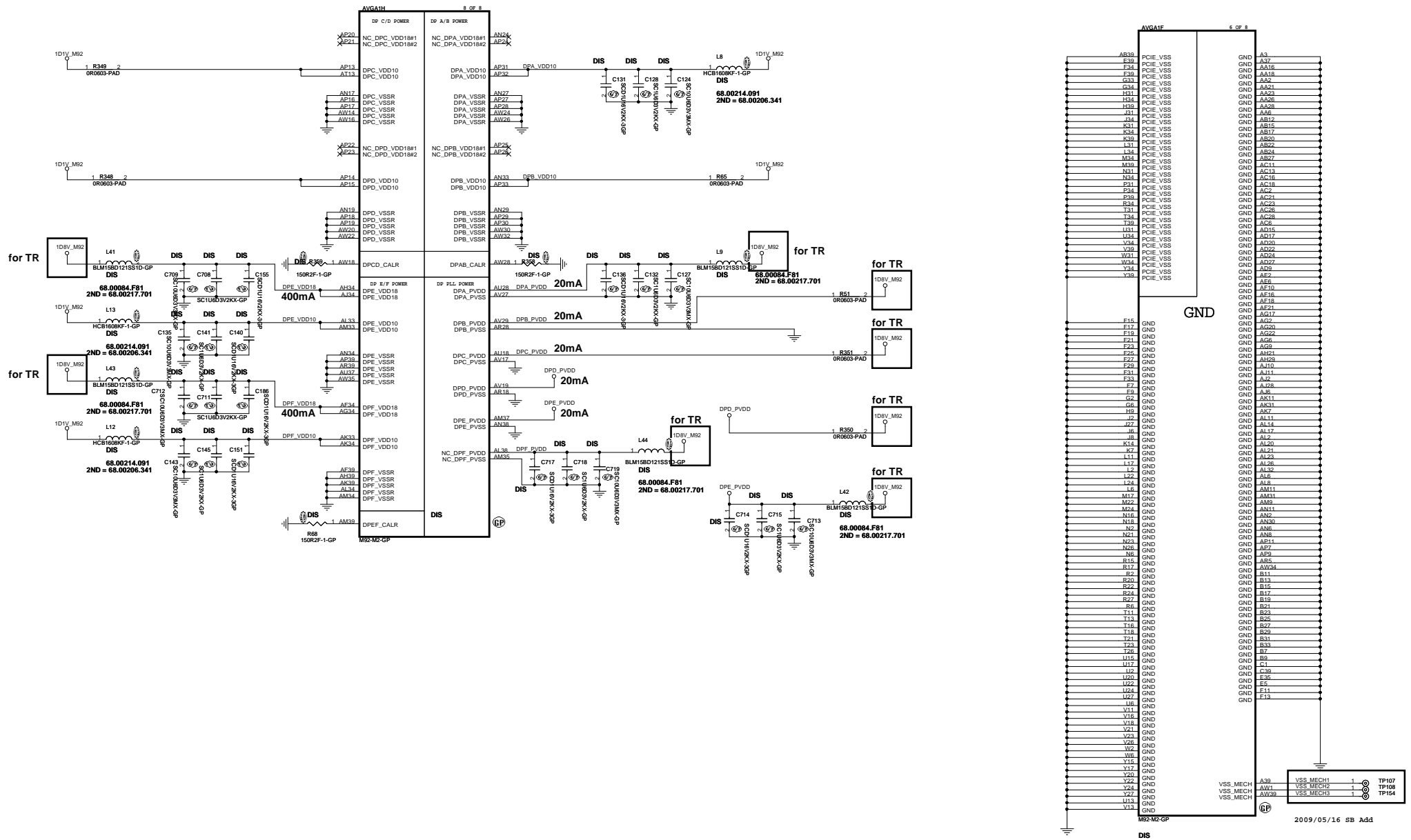
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M92 POWER

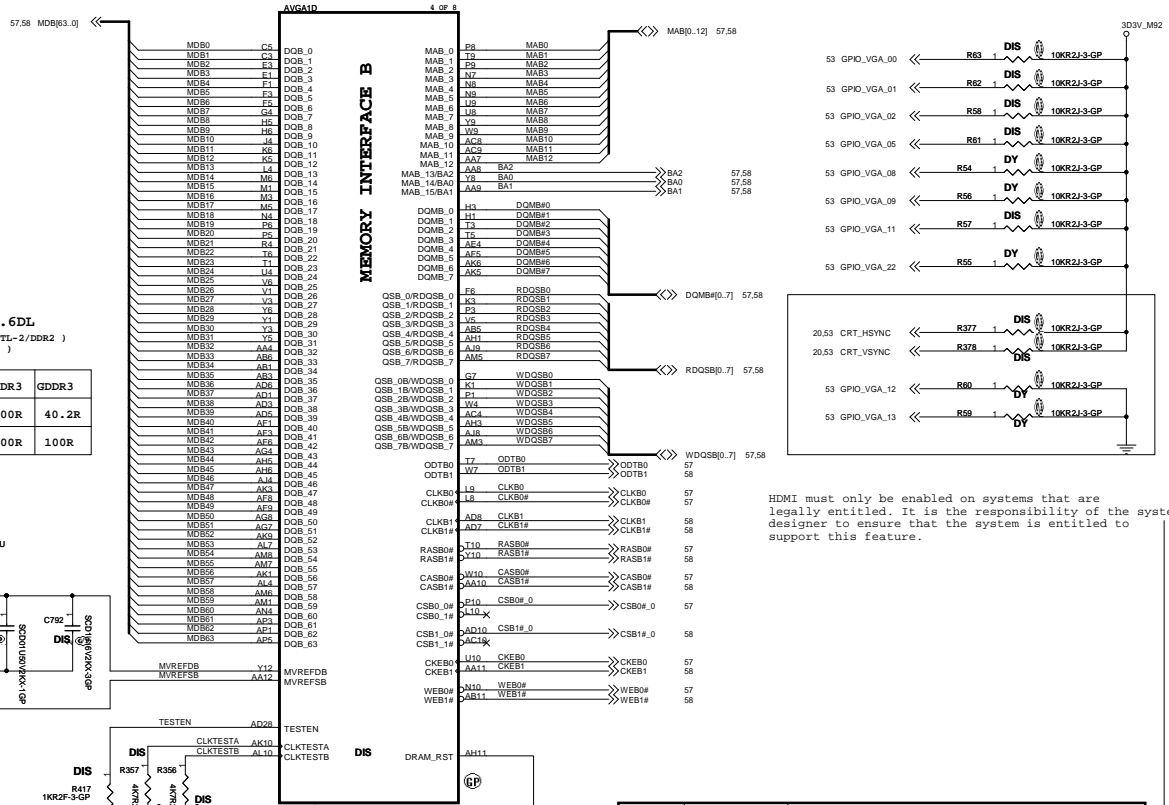
File: **JV71-TR**

Size: A2 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 08, 2009 Sheet: 54 of 61

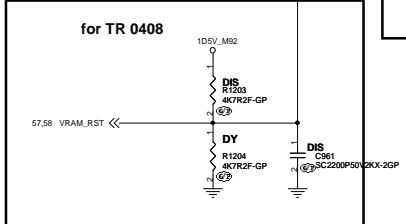
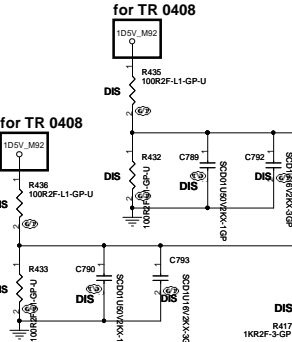


M92-M2 uses memory group B only



40.2R PN:64, 40R25, 6DL
 (0.5 * VDDR1) (for SST1-1, 8/SST1-2/DDR2)
 (0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R



STRAPS	PIN	DESCRIPTION
GPIO	DVPPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

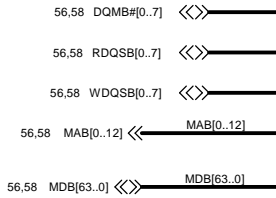
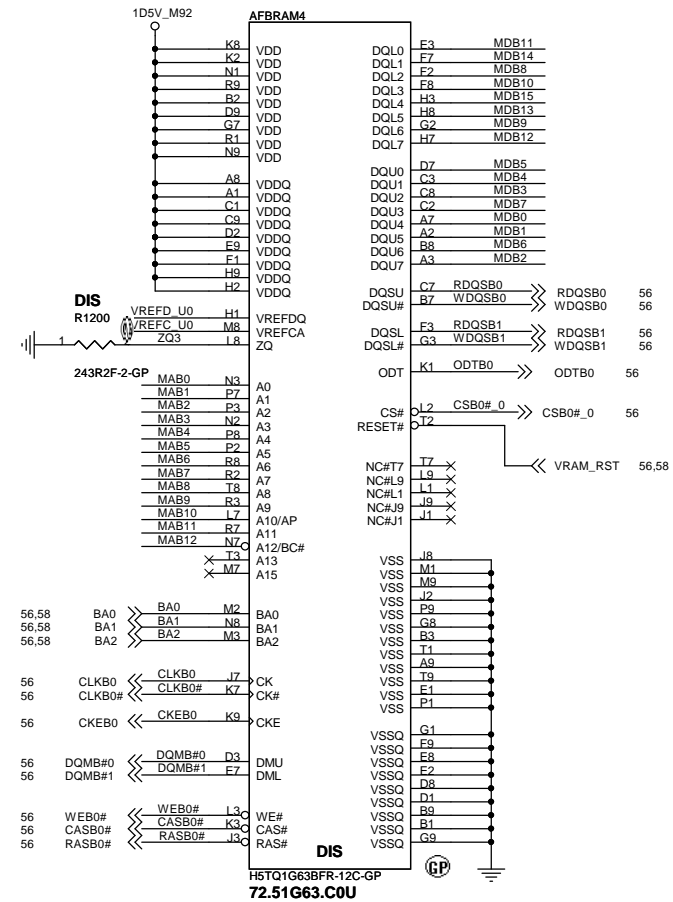
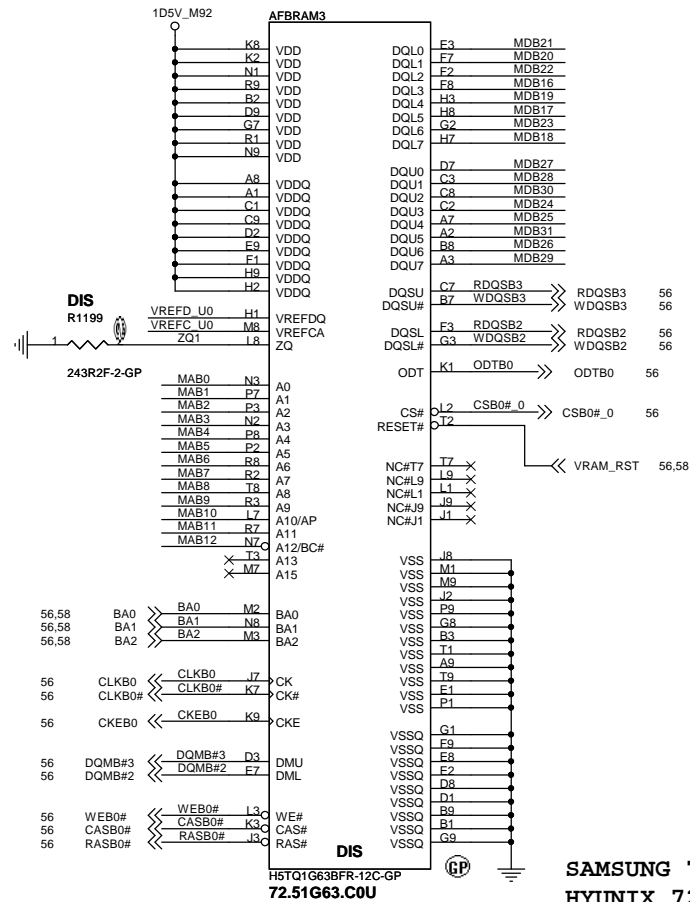
HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC, GENERIC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO , GPIO21_BB_EN	

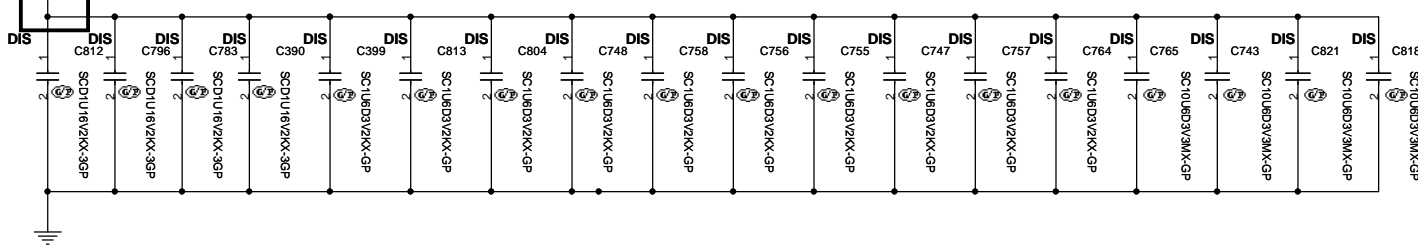
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
1GB	x	Chingis (formerly FMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR x = DESIGN DEFENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50k Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
PWRCNTL[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBPASS	GENERIC		0

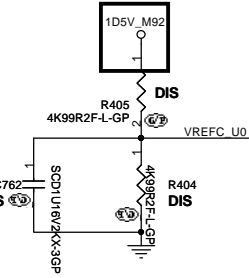
DDR3



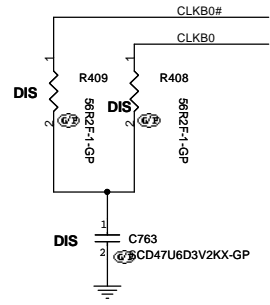
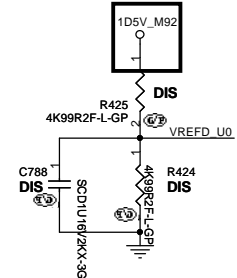
1D5V_M92 for TR



for TR



for TR



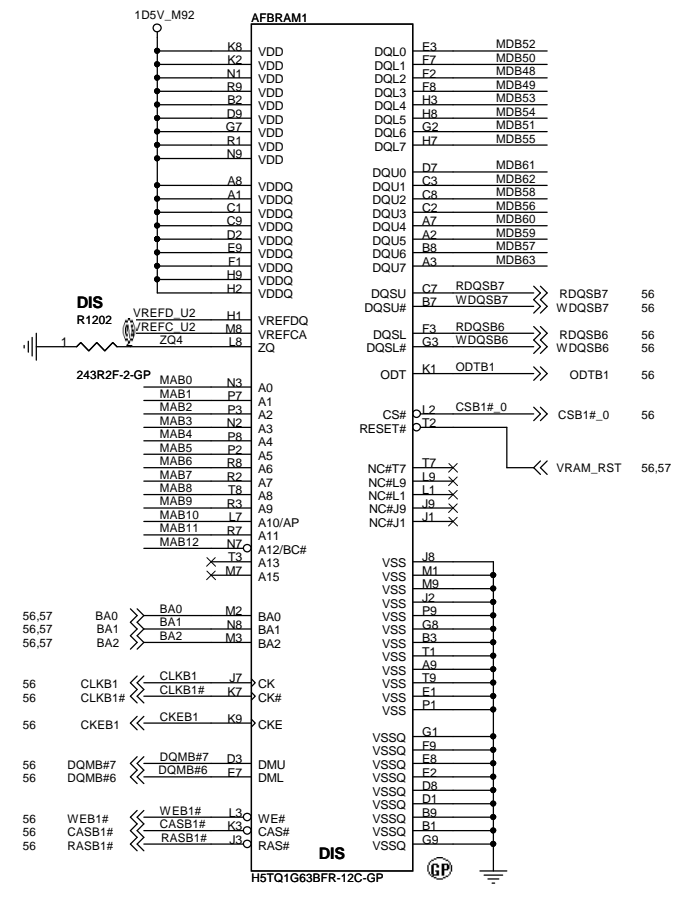
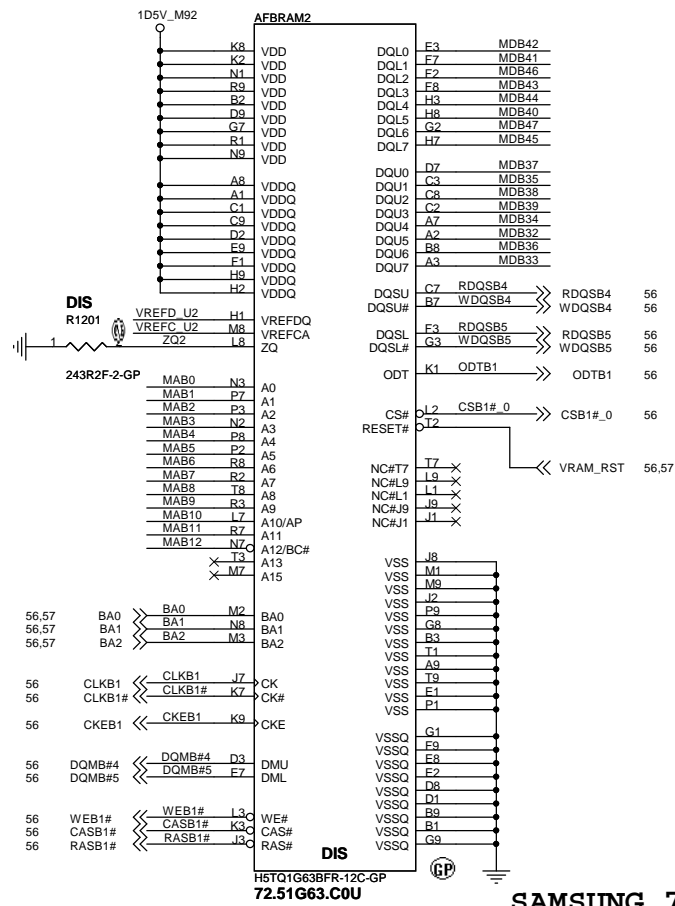
UMA

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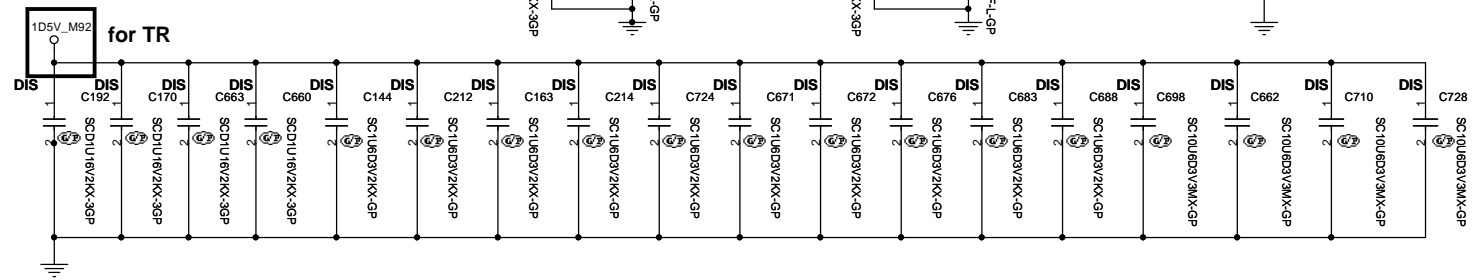
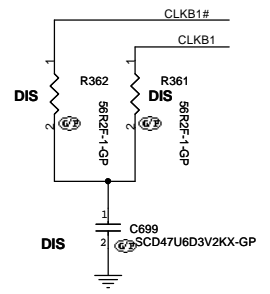
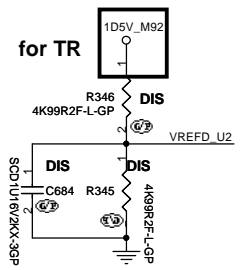
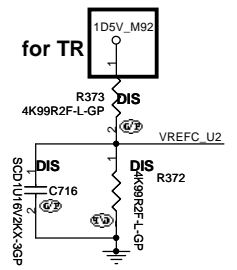
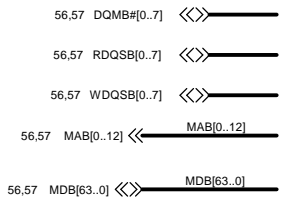
Title: **DDR3 B0**

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SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.COU



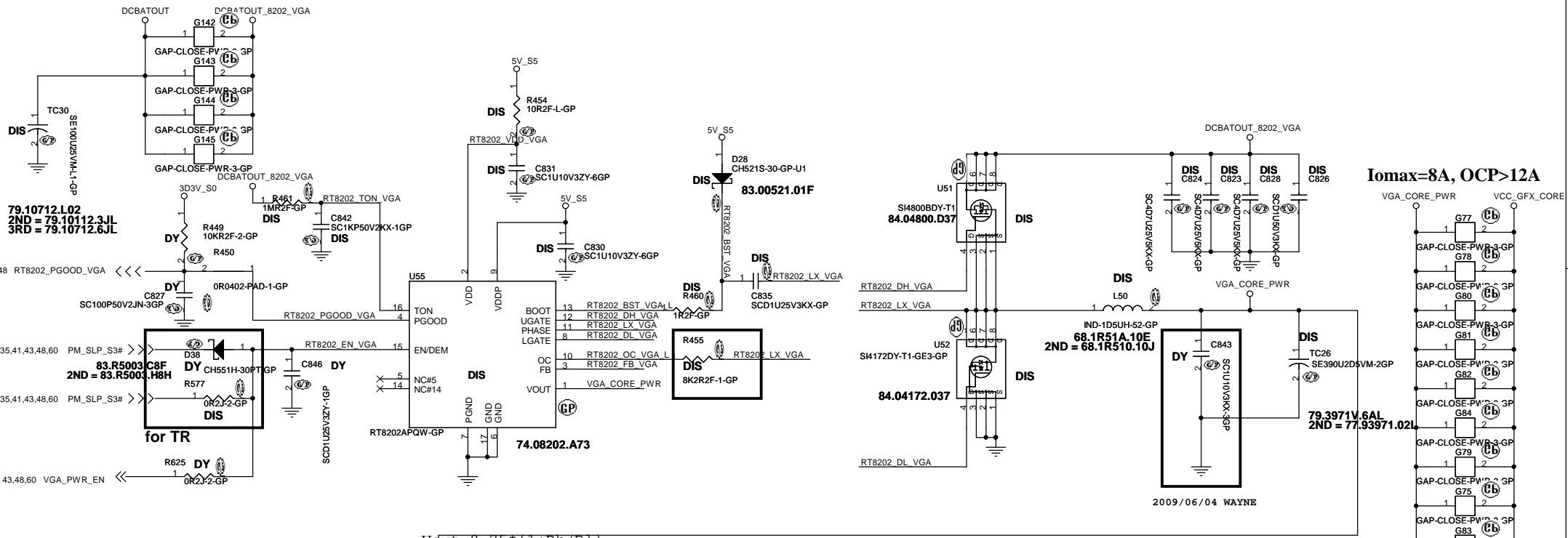
UMA

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Title: **M92 DDR3 B1**

Size: A3 Document Number: **JV71-TR** Rev: **SB**

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Iomax=8A, OCP>12A

79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL

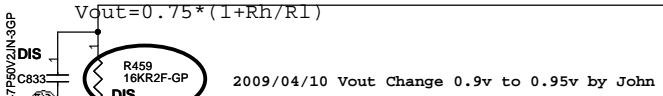
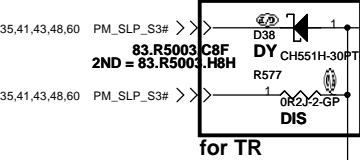
83.00521.01F

SI4800BDY-T1
84.04800.D37

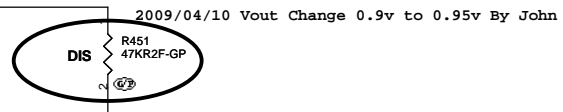
IND-1D5UH-52-GP
68.1R51A.10E
2ND = 68.1R510.10J

79.3971V.6AL
2ND = 77.93971.02L

2009/06/04 WAYNE

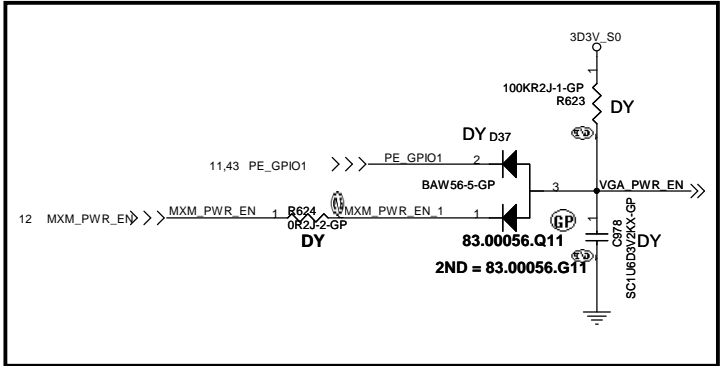


2009/04/10 Vout Change 0.9v to 0.95v by John

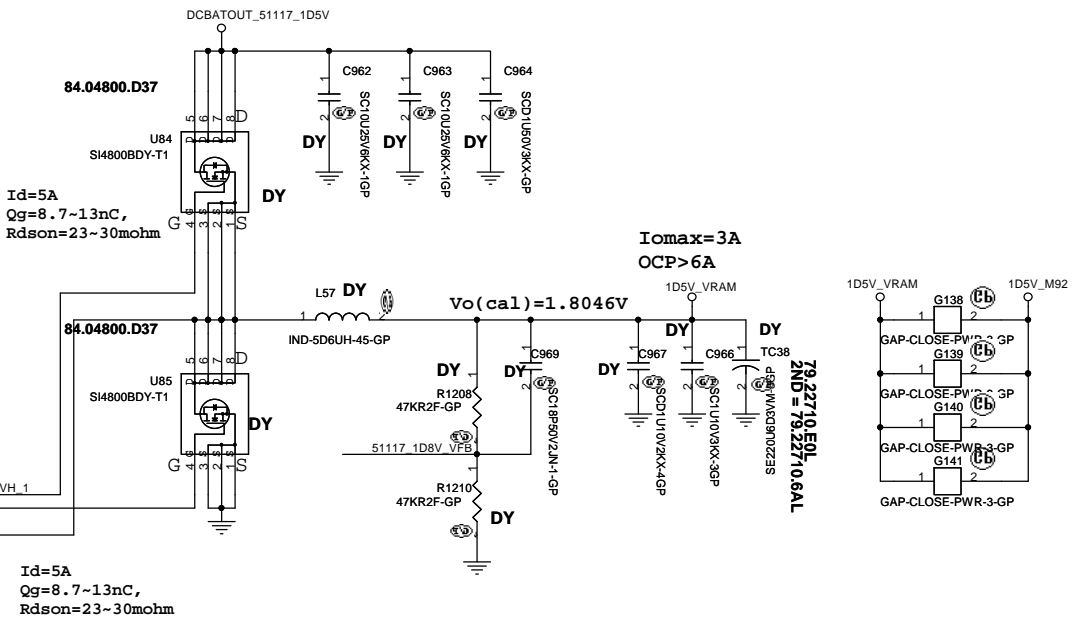
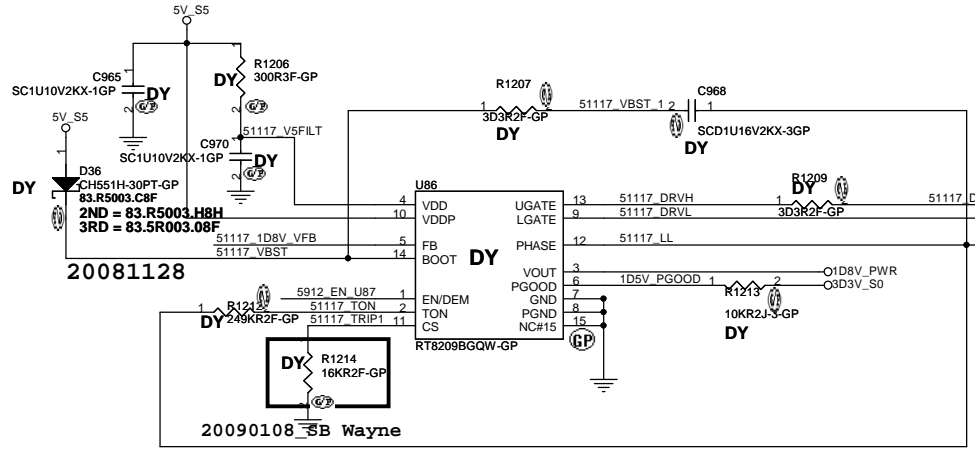
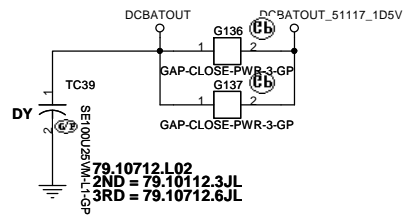


2009/04/10 Vout Change 0.9v to 0.95v By John

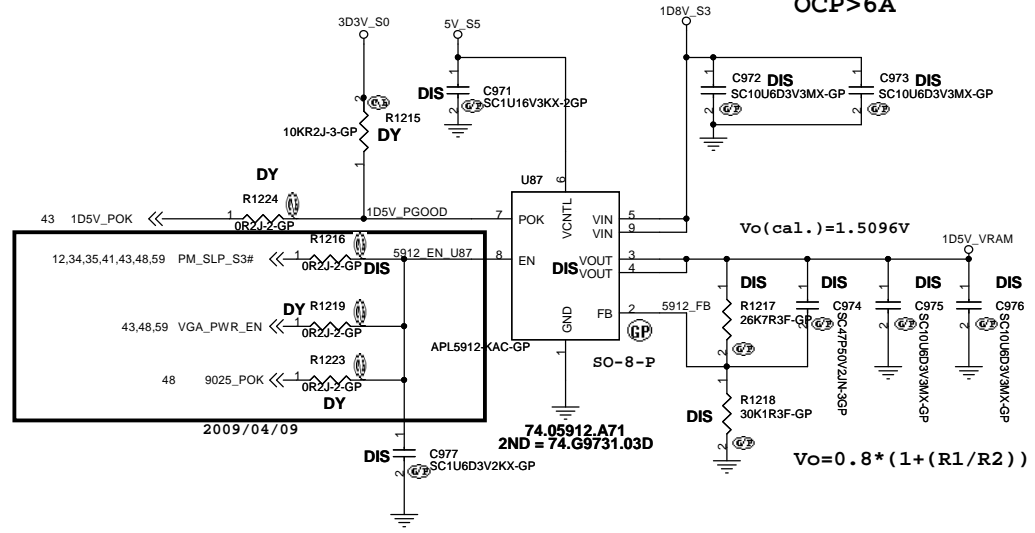
2009/04/10 FOLLW SJM50-TR for TR DIS



VGA_PWR_EN 43,48,60



1D5V_S0
Iomax=3.16A
OCP>6A



5

4

3

2

1

D

D

C

C

B

B

A

A

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Title **HISTORY**

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