JV10-CS Block Diagram

Project code:91.4GS01.001
PCB P/N :48.4GS01.0SA
REVISION :09918-1

Clock Generator
ICS9LRS3197AKLFT 3

DDRIII Slot 0
800/1066/1333 21

DDRIII Slot 1
800/1066/1333 22

DDRIII Channel A

DDRIII Channel B

Intel CPU
SFF
4,5,..,10,11

FDIx8

DMIx4

Mini-Card
WLAN & 3G 33

PCIE+USB 2.0

RJ45
CONN 32

Giga LAN
AR8151 31

PCIE

INTEL
PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
12,13,...,19,20

RGB CRT

LVDS 2CH

Digital Display

CRT 24

LCD
WXGA+ 23

HDMI 25

35 MIC IN

23 INT MIC

HD AUDIO
CODEC
ALC271X 34

AZALIA

35 LINE OUT

2CH SPEAKER
35

WEBCAM 23

BLUETOOTH 38

USB 2.0

USB x 3
29,38

Card Reader
RTS5138 30

SD/MMC
MS/MS Pro/xD 31

SATA

SATA HDD 28

SPI

Flash ROM
4MB 37

LPC Bus

LPC debug 37

KBC
NPCE781B 36

SPI

Flash ROM
128KB 36

Thermal
Sensor
G795 26

Touch
PAD 38

Int.
KB

26 CPU FAN

SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 42

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 43

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 44

SYSTEM DC/DC RT9026	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 43

CPU DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 41

INTERSIL CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 45

PCB STACKUP

TOP
Power
S
S
GND
BOTTOM

JV10 CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

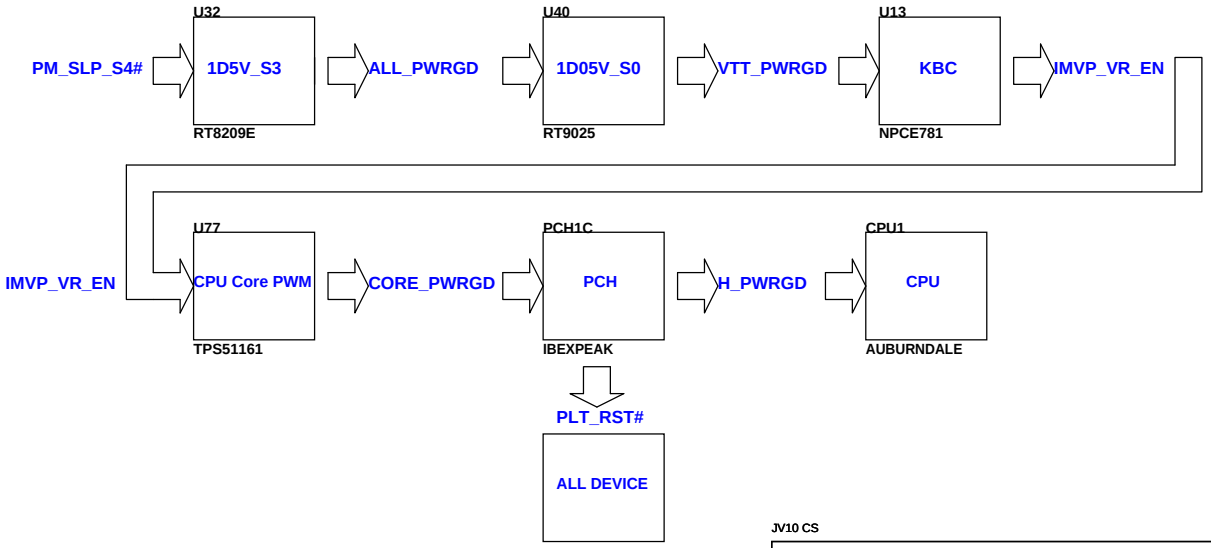
PCIE Routing

LANE1	LAN
LANE2	MiniCard1

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

Power Sequence



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Title: **Table of Content**

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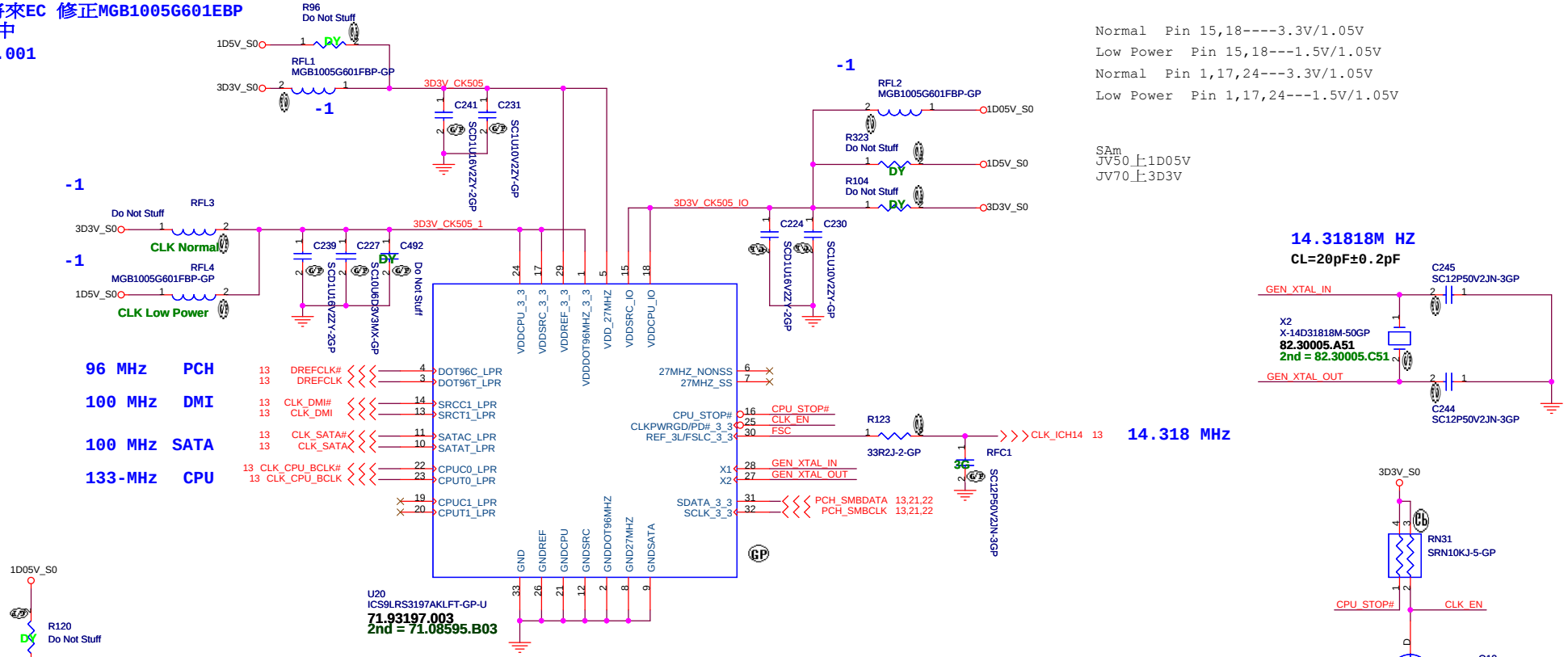
RFL1~4 將來EC 修正MGB1005G601EBP
料號申請中
68.00373.001

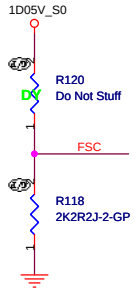
Normal Pin 15,18----3.3V/1.05V
Low Power Pin 15,18---1.5V/1.05V
Normal Pin 1,17,24---3.3V/1.05V
Low Power Pin 1,17,24---1.5V/1.05V

SAm
JV50上1D05V
JV70上3D3V



CLK Lower Power ICS:71.93197.B03,SILEGO:71.08595.003

FSC	0	1
SPEED	133MHz (Default)	100MHz



14.31818M HZ
CL=20pF±0.2pF

14.318 MHz

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Title: Clock Generator
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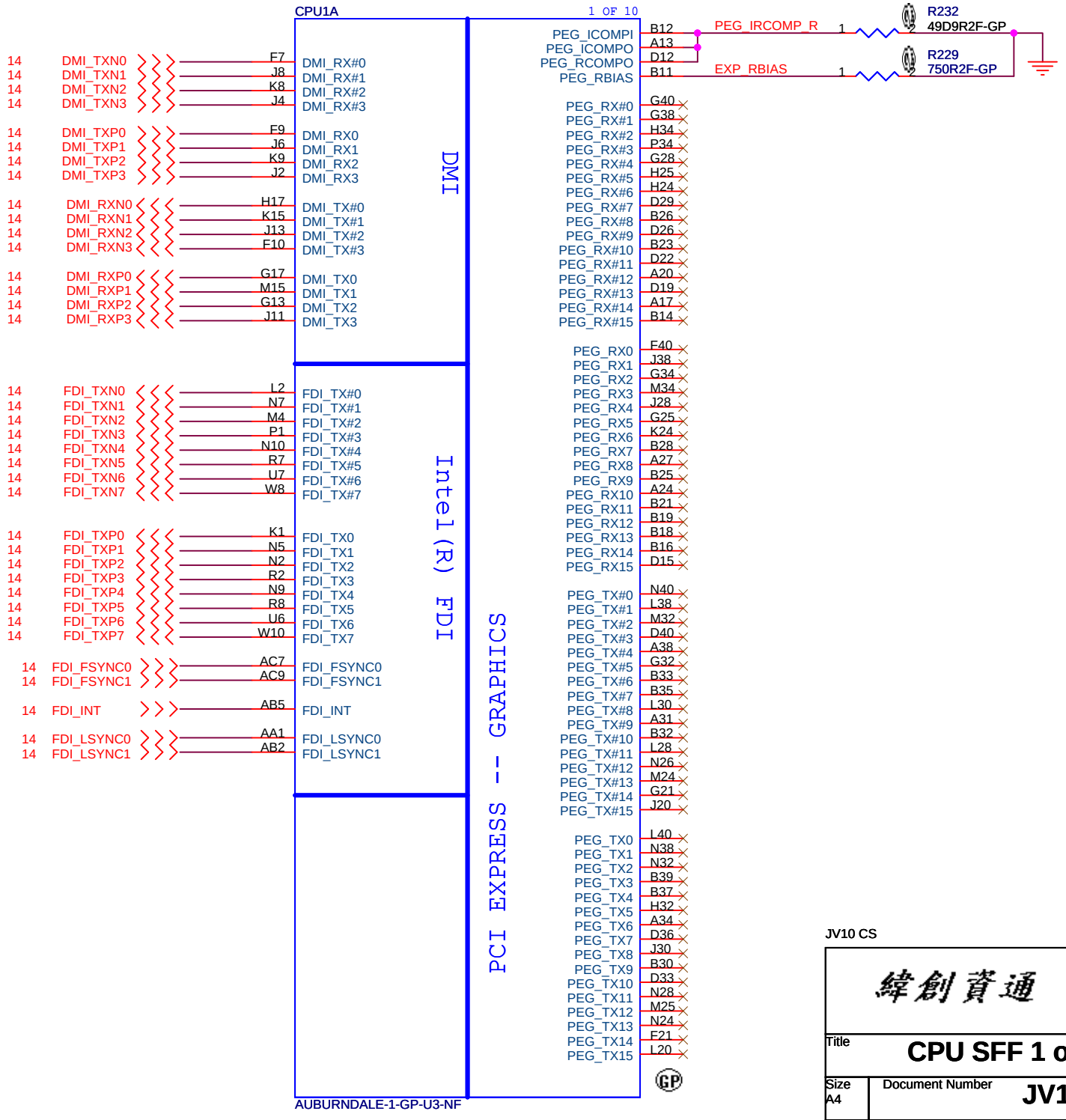

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Title: **CPU SFF 1 of 8(DMI/FDI/PEG)**

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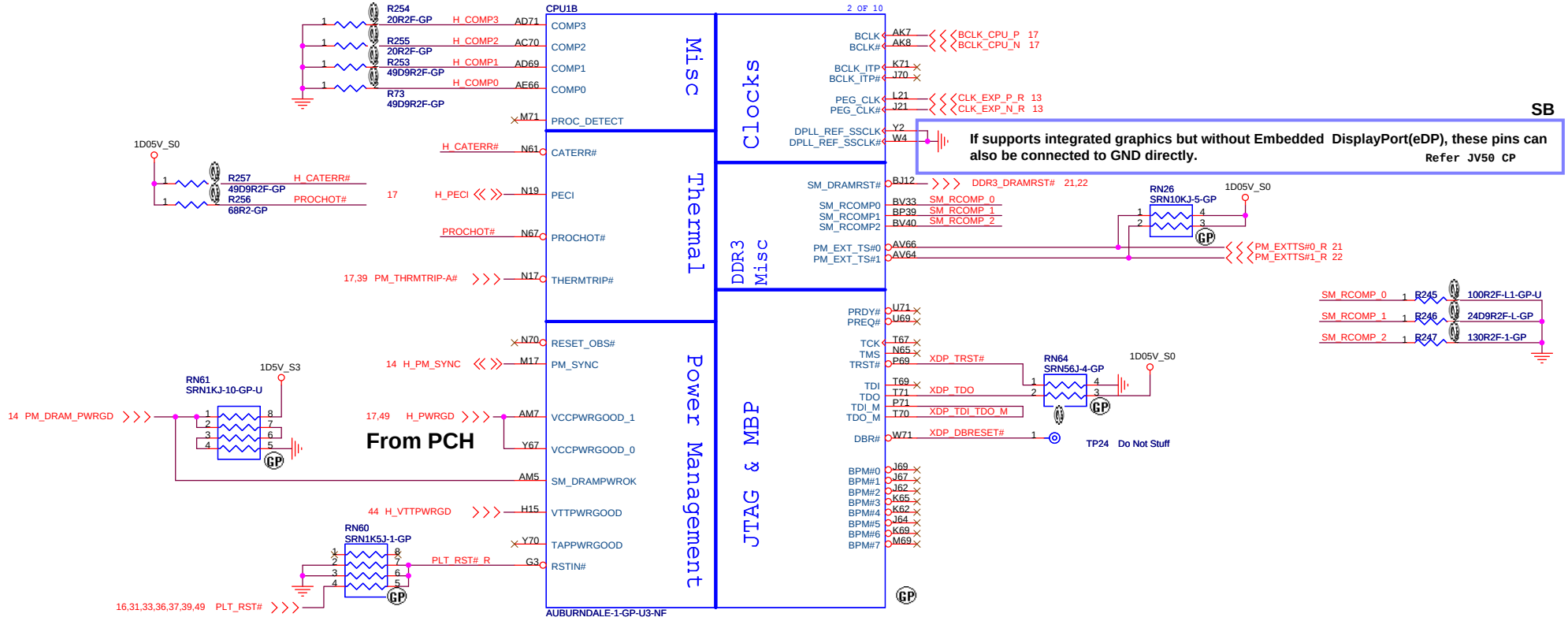

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Title: CPU SFF 2 of 8(CLK/Thermal)

Size	Document Number	Rev
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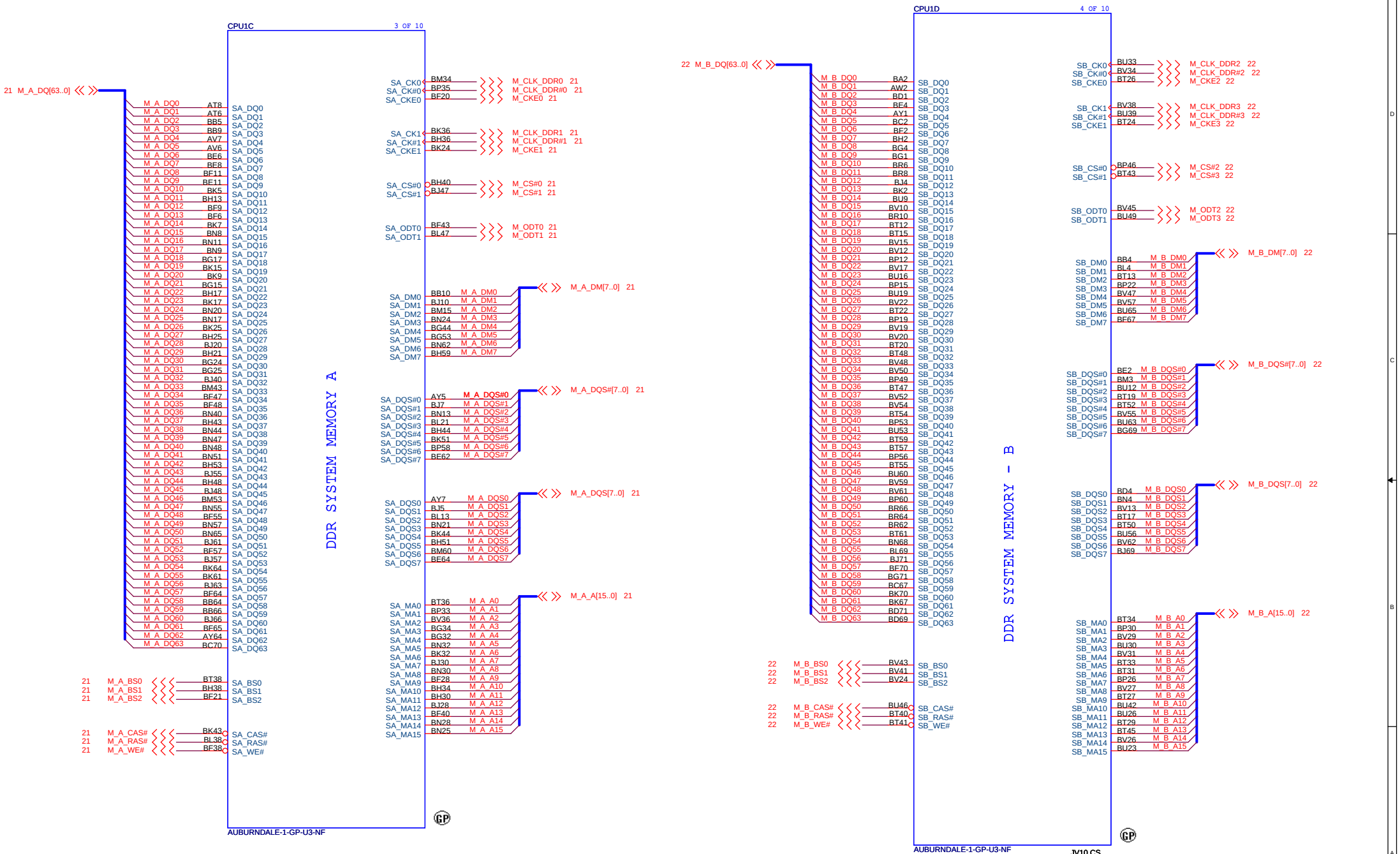
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3 OF 10
DDR SYSTEM MEMORY A
AUBURNDALE-1-GP-U3-NF
21 M_A_DQ[63..0]
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M_A_DQ1 AT6 SA_DQ1
M_A_DQ2 BB5 SA_DQ2
M_A_DQ3 BB9 SA_DQ3
M_A_DQ4 AV7 SA_DQ4
M_A_DQ5 AV6 SA_DQ5
M_A_DQ6 BE6 SA_DQ6
M_A_DQ7 BE8 SA_DQ7
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M_A_DQ15 BN8 SA_DQ15
M_A_DQ16 BN11 SA_DQ16
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M_A_DQ20 BK9 SA_DQ20
M_A_DQ21 BG15 SA_DQ21
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M_A_DQ27 BH25 SA_DQ27
M_A_DQ28 BJ20 SA_DQ28
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M_A_DQ44 BH48 SA_DQ44
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M_A_DQ47 BN55 SA_DQ47
M_A_DQ48 BF55 SA_DQ48
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M_A_DQ60 BJ66 SA_DQ60
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M_A_DQ62 AY64 SA_DQ62
M_A_DQ63 BC70 SA_DQ63
21 M_A_BS0 BT38 SA_BS0
21 M_A_BS1 BH38 SA_BS1
21 M_A_BS2 BF21 SA_BS2
21 M_A_CAS# BK43 SA_CAS#
21 M_A_RAS# BL38 SA_RAS#
21 M_A_WE# BF38 SA_WE#
SA_CK0 BM34 M_CLK_DDR0 21
SA_CK#0 BP35 M_CLK_DDR#0 21
SA_CKE0 BF20 M_CKE0 21
SA_CK1 BK36 M_CLK_DDR1 21
SA_CK#1 BH36 M_CLK_DDR#1 21
SA_CKE1 BK24 M_CKE1 21
SA_CS#0 BH40 M_CS#0 21
SA_CS#1 BJ47 M_CS#1 21
SA_ODT0 BF43 M_ODT0 21
SA_ODT1 BL47 M_ODT1 21
SA_DM0 BB10 M_A_DM0
SA_DM1 BJ10 M_A_DM1
SA_DM2 BM15 M_A_DM2
SA_DM3 BN24 M_A_DM3
SA_DM4 BG44 M_A_DM4
SA_DM5 BG53 M_A_DM5
SA_DM6 BN62 M_A_DM6
SA_DM7 BH59 M_A_DM7
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SA_DQS#1 BJ7 M_A_DQS#1
SA_DQS#2 BN13 M_A_DQS#2
SA_DQS#3 BL21 M_A_DQS#3
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SA_DQS#5 BK51 M_A_DQS#5
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SA_DQS5 BH51 M_A_DQS5
SA_DQS6 BM60 M_A_DQS6
SA_DQS7 BE64 M_A_DQS7
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SA_MA4 BG32 M_A_A4
SA_MA5 BN32 M_A_A5
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SA_MA14 BN28 M_A_A14
SA_MA15 BN25 M_A_A15
M_A_A[15..0] 21
CPU1D
4 OF 10
DDR SYSTEM MEMORY - B
AUBURNDALE-1-GP-U3-NF
22 M_B_DQ[63..0]
M_B_DQ0 BA2 SB_DQ0
M_B_DQ1 AW2 SB_DQ1
M_B_DQ2 BD1 SB_DQ2
M_B_DQ3 BE4 SB_DQ3
M_B_DQ4 AY1 SB_DQ4
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M_B_DQ61 BK67 SB_DQ61
M_B_DQ62 BD71 SB_DQ62
M_B_DQ63 BD69 SB_DQ63
22 M_B_BS0 BV43 SB_BS0
22 M_B_BS1 BV41 SB_BS1
22 M_B_BS2 BV24 SB_BS2
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22 M_B_RAS# BT40 SB_RAS#
22 M_B_WE# BT41 SB_WE#
SB_CK0 BU33 M_CLK_DDR2 22
SB_CK#0 BV34 M_CLK_DDR#2 22
SB_CKE0 BT26 M_CKE2 22
SB_CK1 BV38 M_CLK_DDR3 22
SB_CK#1 BU39 M_CLK_DDR#3 22
SB_CKE1 BT24 M_CKE3 22
SB_CS#0 BP46 M_CS#2 22
SB_CS#1 BT43 M_CS#3 22
SB_ODT0 BV45 M_ODT2 22
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SB_DM3 BP22 M_B_DM3
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SB_DM6 BU65 M_B_DM6
SB_DM7 BF67 M_B_DM7
M_B_DM[7..0] 22
SB_DQS#0 BE2 M_B_DQS#0
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SB_DQS#2 BU12 M_B_DQS#2
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SB_MA3 BU30 M_B_A3
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SB_MA13 BT45 M_B_A13
SB_MA14 BV26 M_B_A14
SB_MA15 BU23 M_B_A15
M_B_A[15..0] 22
JV10 CS
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Wistron Corporation
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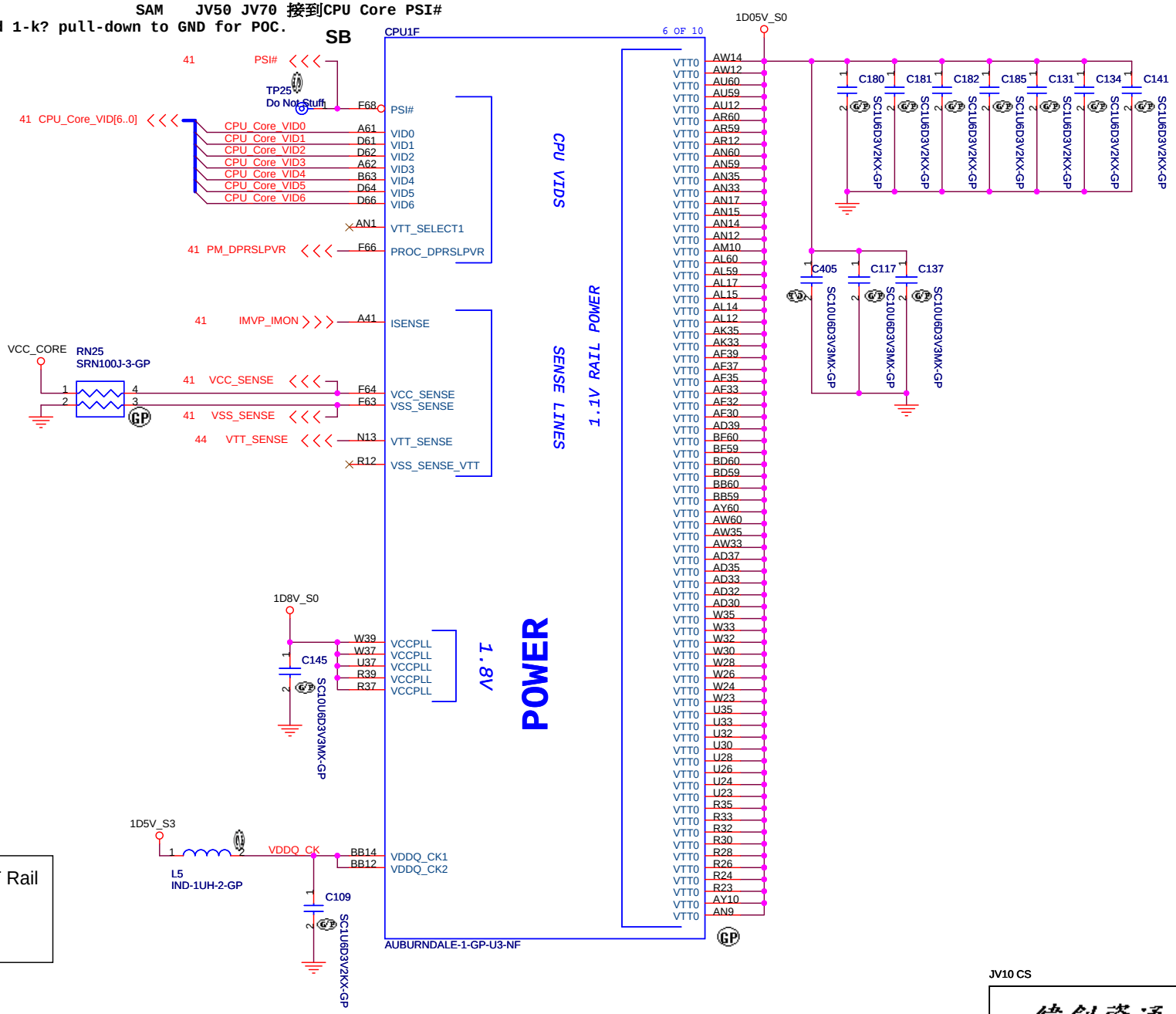
check list
1-k? pull-up to VTT and 1-k? pull-down to GND for POC.
1D05V_VTT

SAM JV50 JV70 接到CPU Core PSI#

SB



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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Title: CPU SFF 4 of 8(POWER/VTT)		
Size: Custom	Document Number: JV10-CS	Rev: -1
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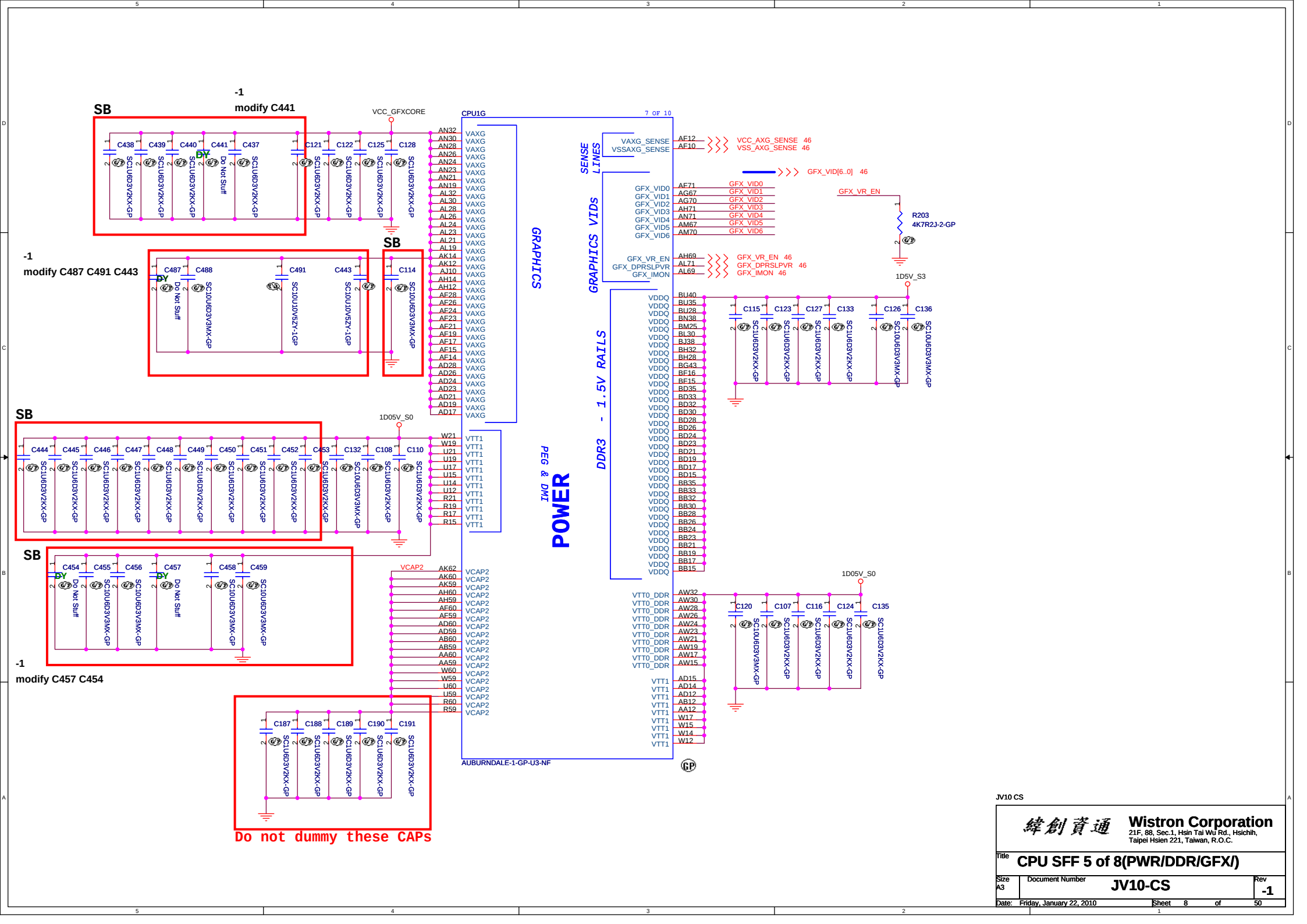

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Title	CPU SFF 5 of 8(PWR/DDR/GFX/)	
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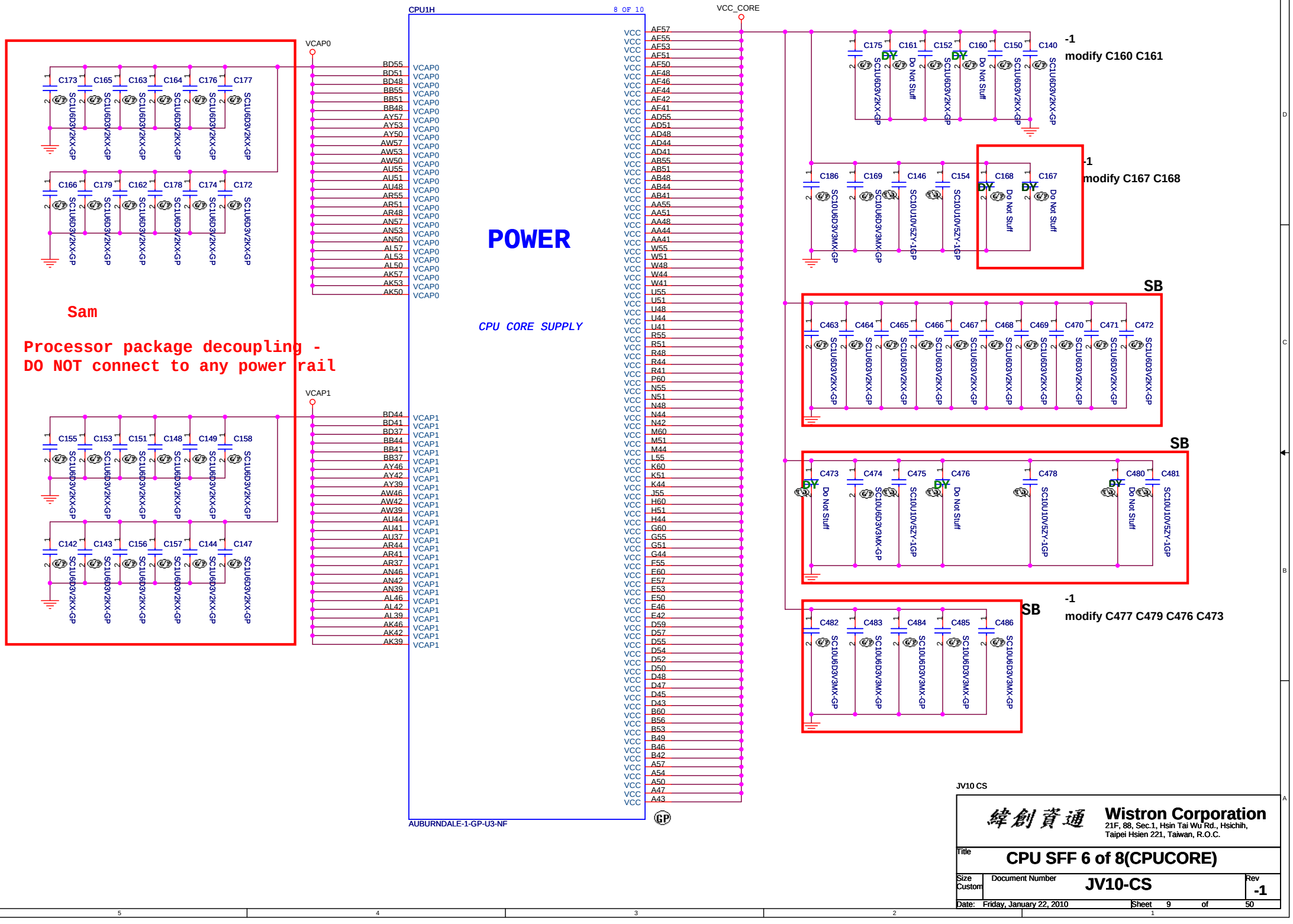

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Title: CPU SFF 6 of 8(CPUCORE)		
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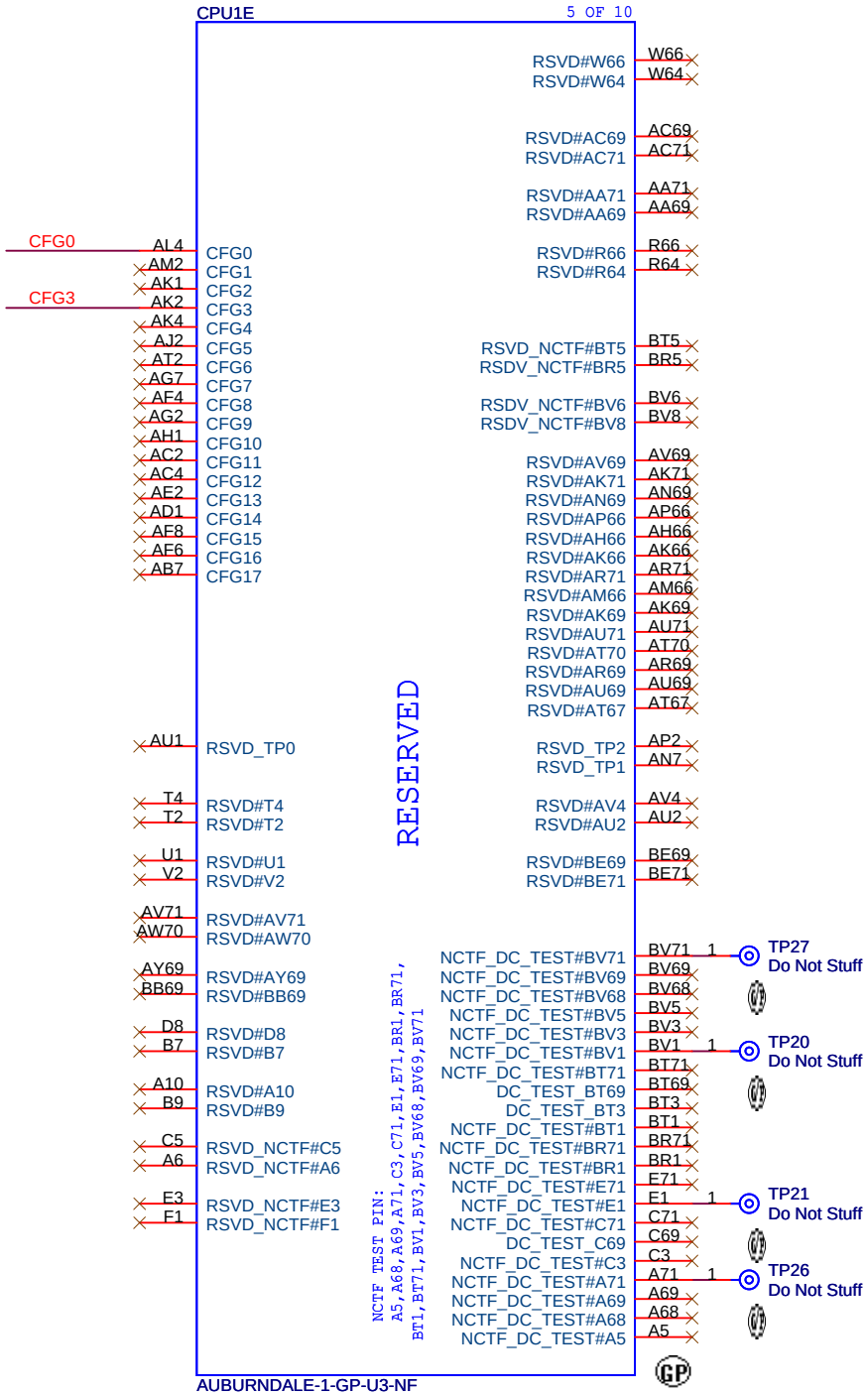
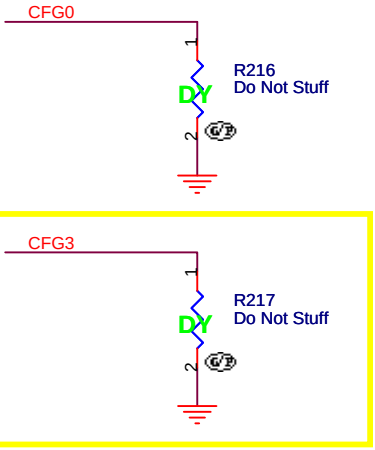




PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

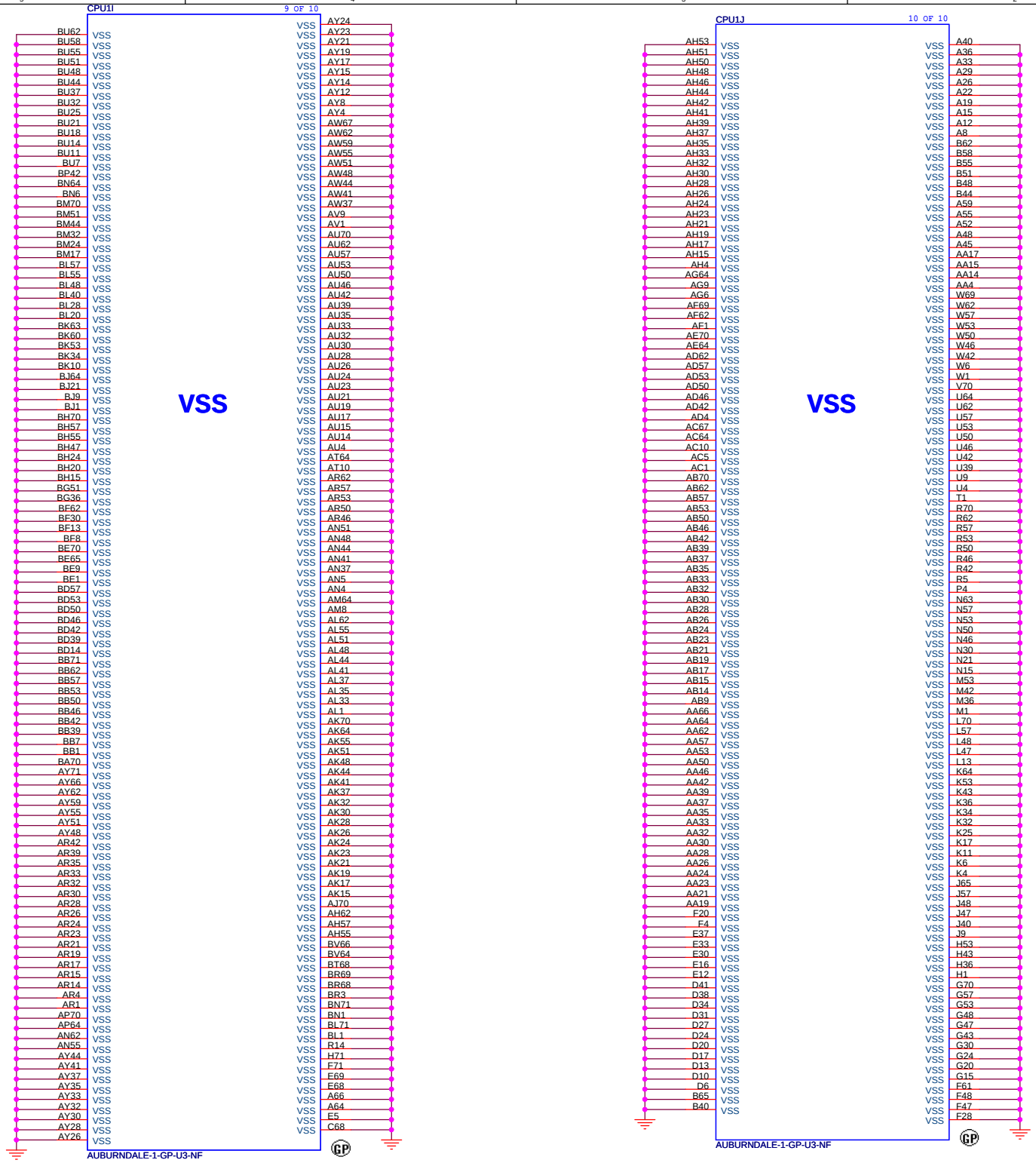
JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU SFF 7 of 8(RESERVED)**

Size	Document Number	Rev
A4	JV10-CS	-1

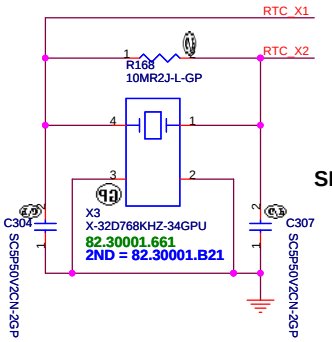
Date: Friday, January 22, 2010 Sheet 10 of 50

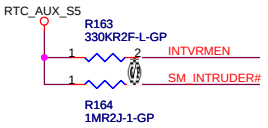


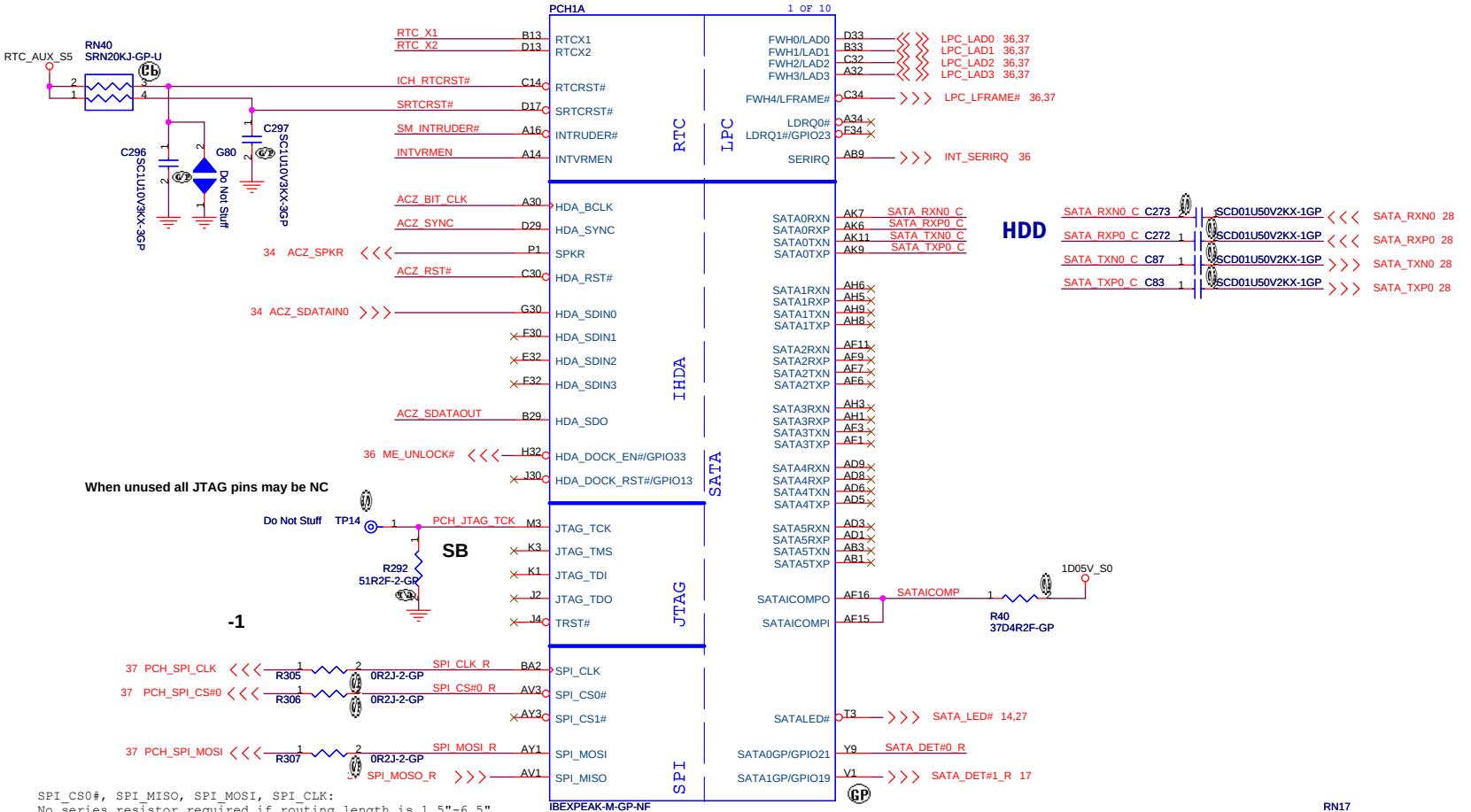
JV10 CS

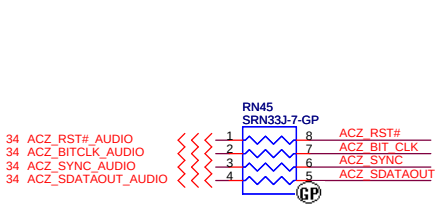
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU SFF 8 of 8(VSS)**	
Size A3	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 11 of 50	

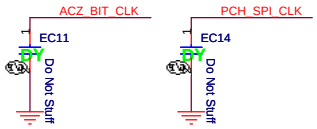
integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

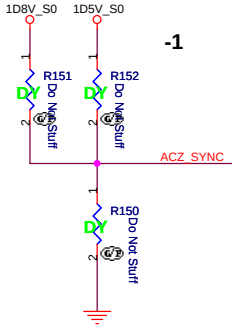


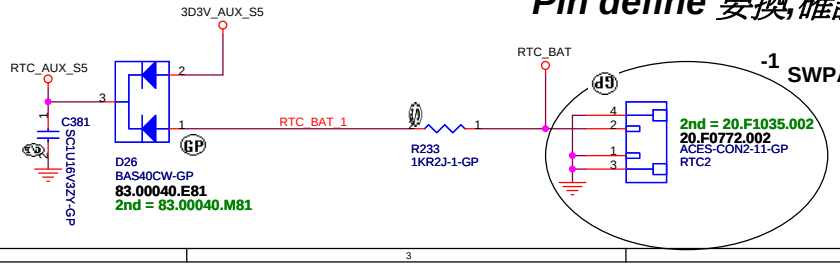












If reserve 1.5/1.8V option for VCCVRM.Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

RTC CONN

23.25218.001

Pin define 要換,確認connector part number

JV10 CS

Wistron Corporation
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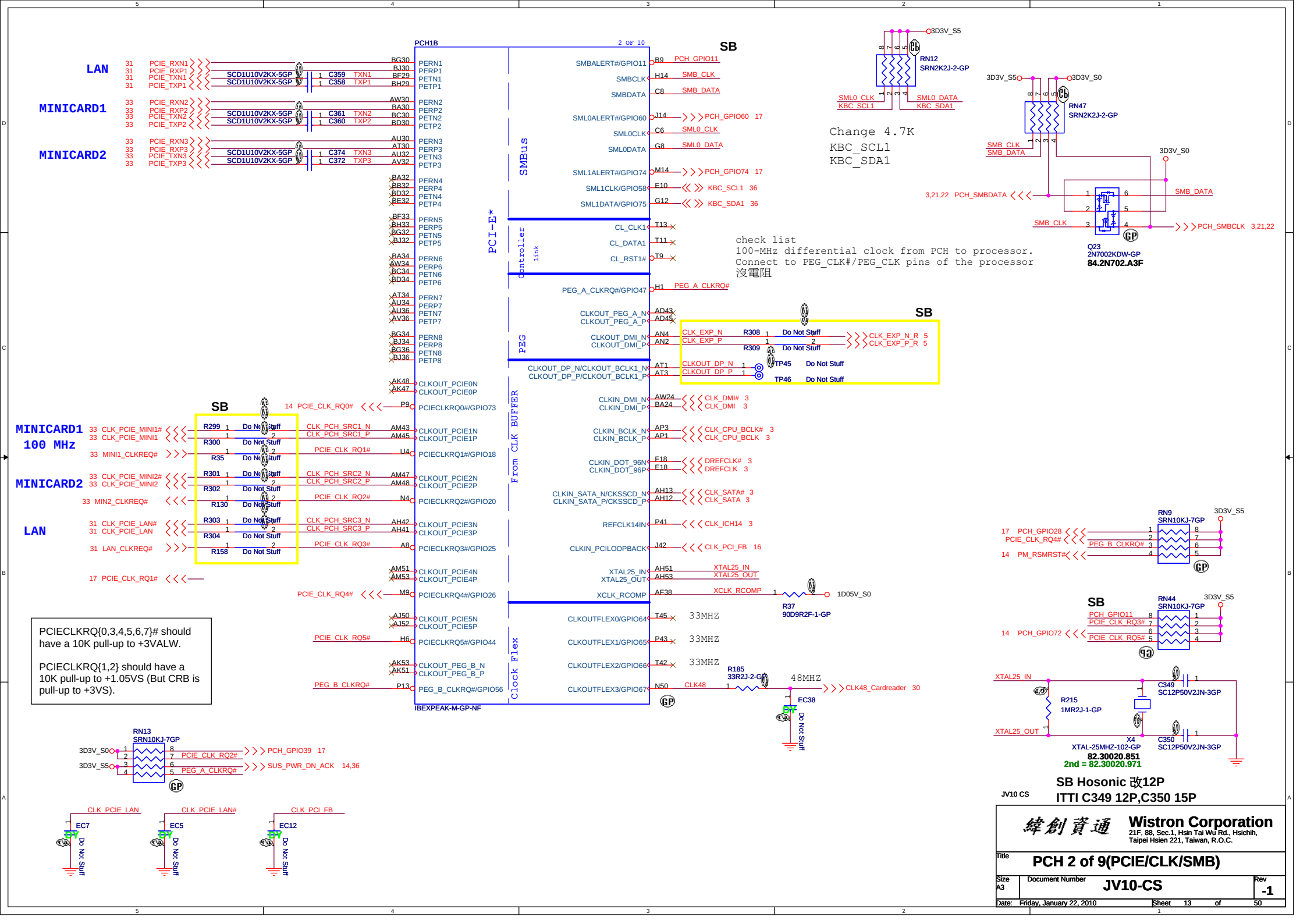
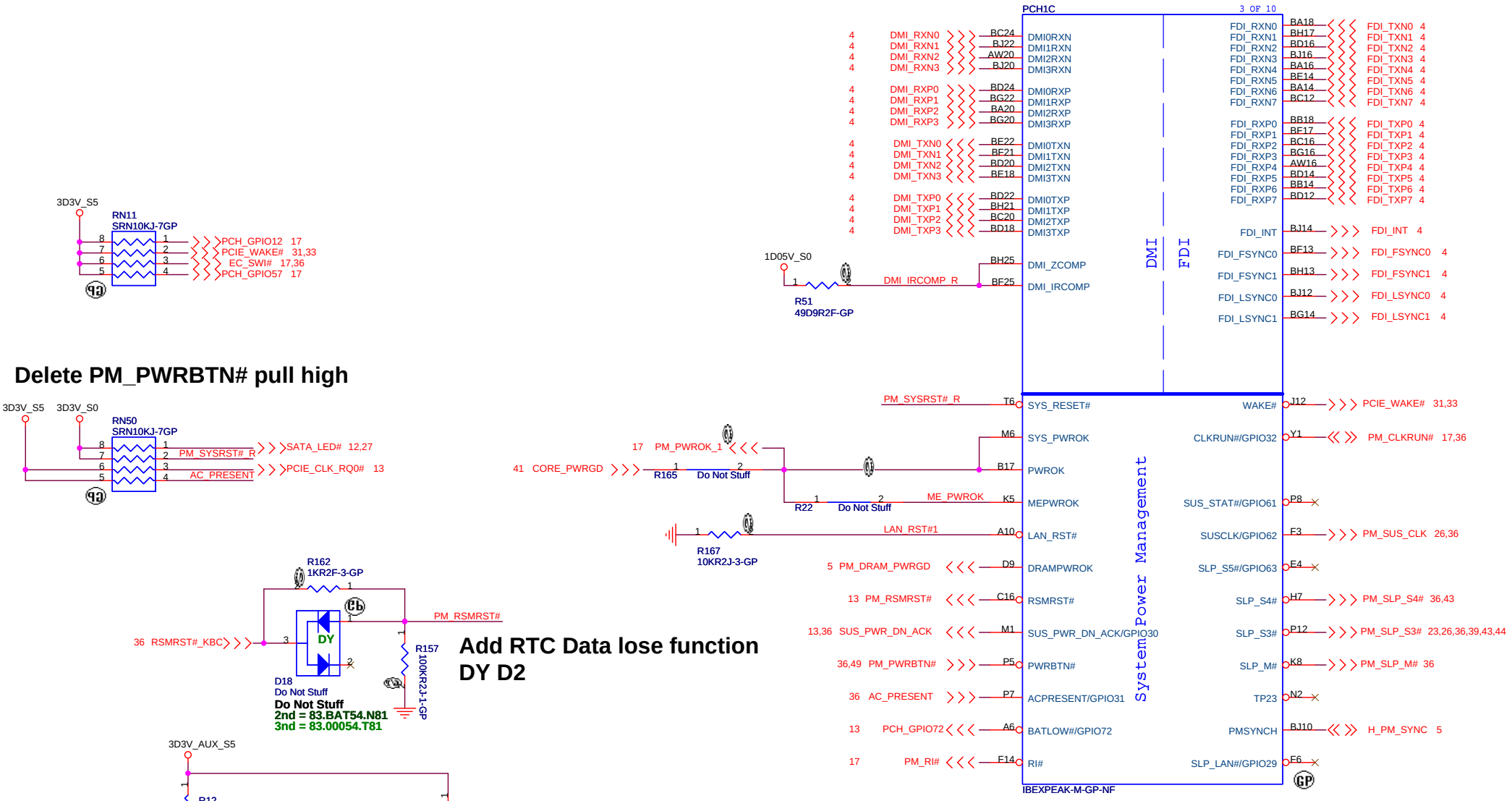
Title	PCH 1 of 9(SATA/RTC/HDA)	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 12 of 50	


LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
SB
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
Change 4.7K
KBC_SCL1
KBC_SDA1
check list
100-MHz differential clock from PCH to processor.
Connect to PEG_CLK#/PEG_CLK pins of the processor
沒電阻
MINICARD1
100 MHz
MINICARD2
LAN
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
RN12 SRN2K2J-2-GP
RN47 SRN2K2J-2-GP
Q23 2N7002KDW-GP
84.2N702.A3F
RN9 SRN10KJ-7GP
RN44 SRN10KJ-7GP
RN13 SRN10KJ-7GP
R37 90D9R2F-1-GP
R185 33R2J-2-GP
R215 1MR2J-1-GP
X4 XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.971
SB Hosonic 改12P
ITTI C349 12P,C350 15P
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 2 of 9(PCIE/CLK/SMB)
Size A3
Document Number
JV10-CS
Rev -1
Date: Friday, January 22, 2010
Sheet 13 of 50



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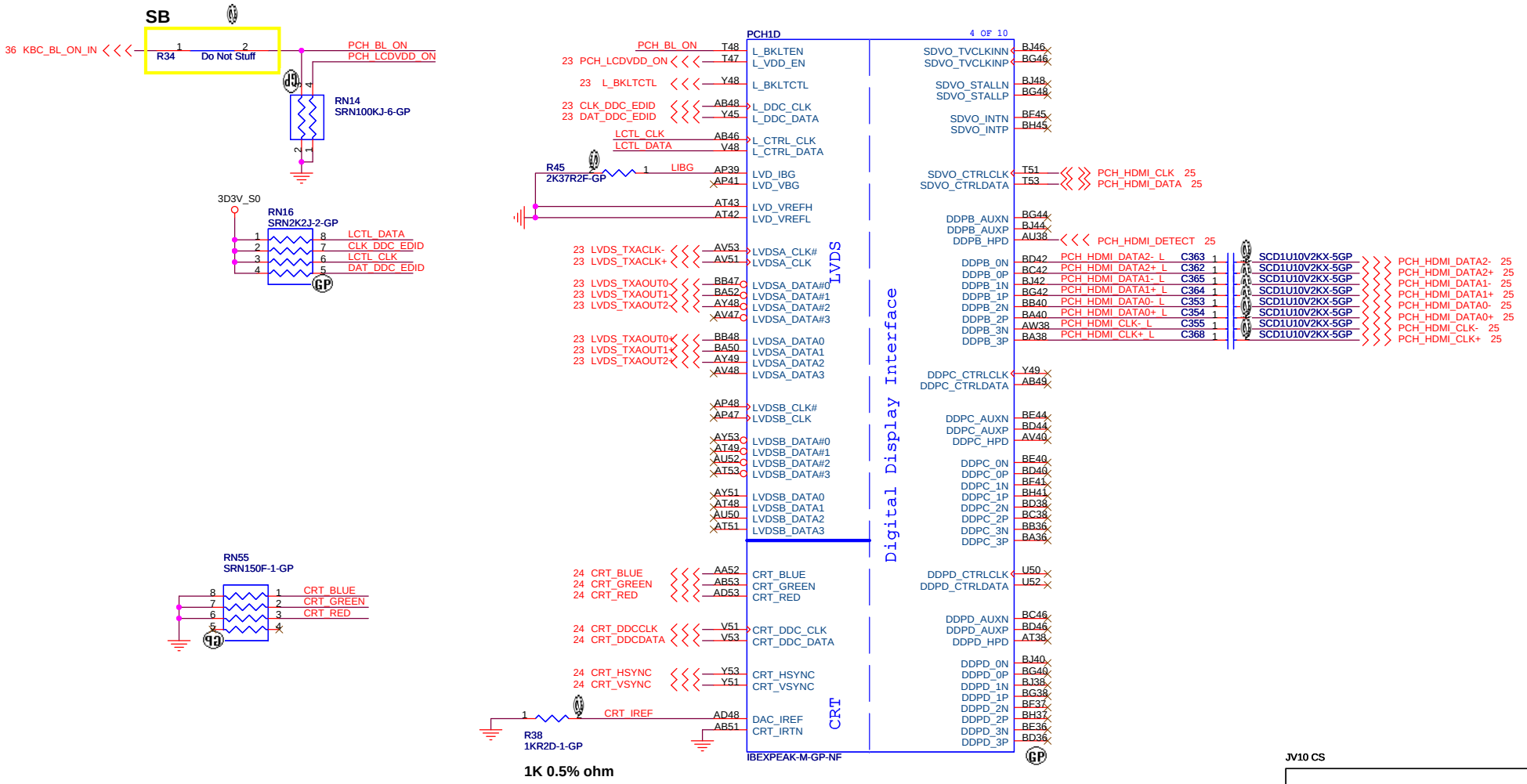
Title: **PCH 3 of 9(DMI/FDI)**

Size	Document Number	Rev
Custom	JV10-CS	-1

Date: Friday, January 22, 2010 Sheet 14 of 50

Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



JV10 CS

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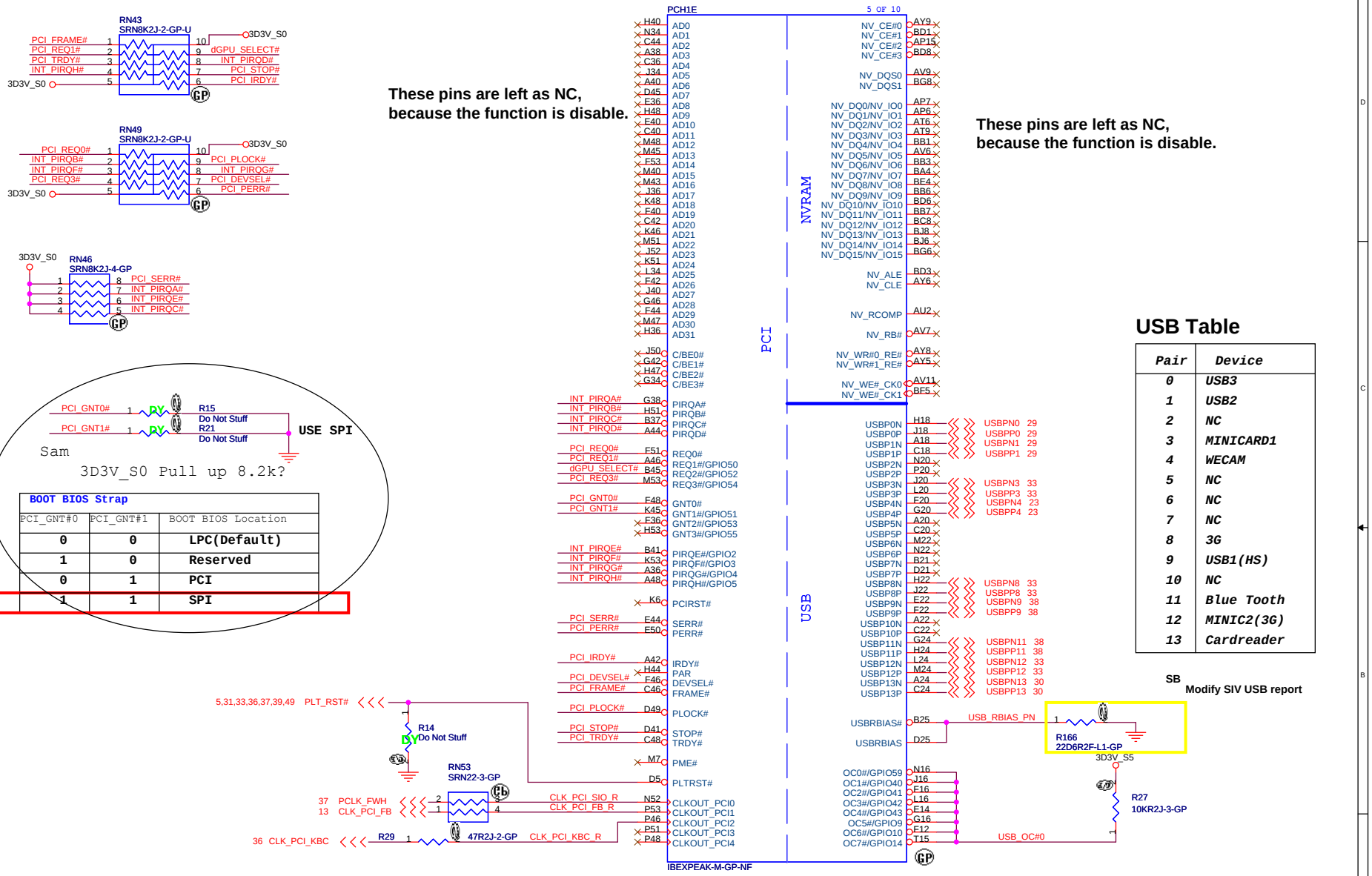
Title: PCH 4 of 9(LVDS/CRT/DP)

Size	Document Number	Rev
Custom	JV10-CS	-1

Date: Friday, January 22, 2010 Sheet 15 of 50



USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	3G
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2(3G)
13	Cardreader

SB
Modify SIV USB report

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Title: PCH 5 of 9(PCI/USB)

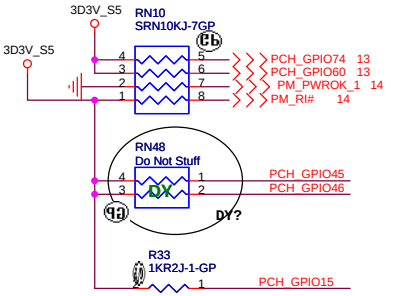
Size: A3 | Document Number: JV10-CS | Rev: -1

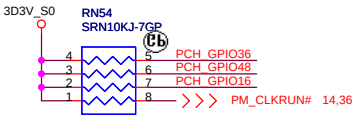
Date: Friday, January 22, 2010 | Sheet 16 of 50

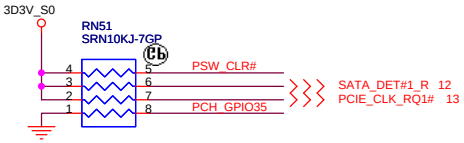
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

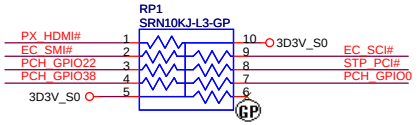
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

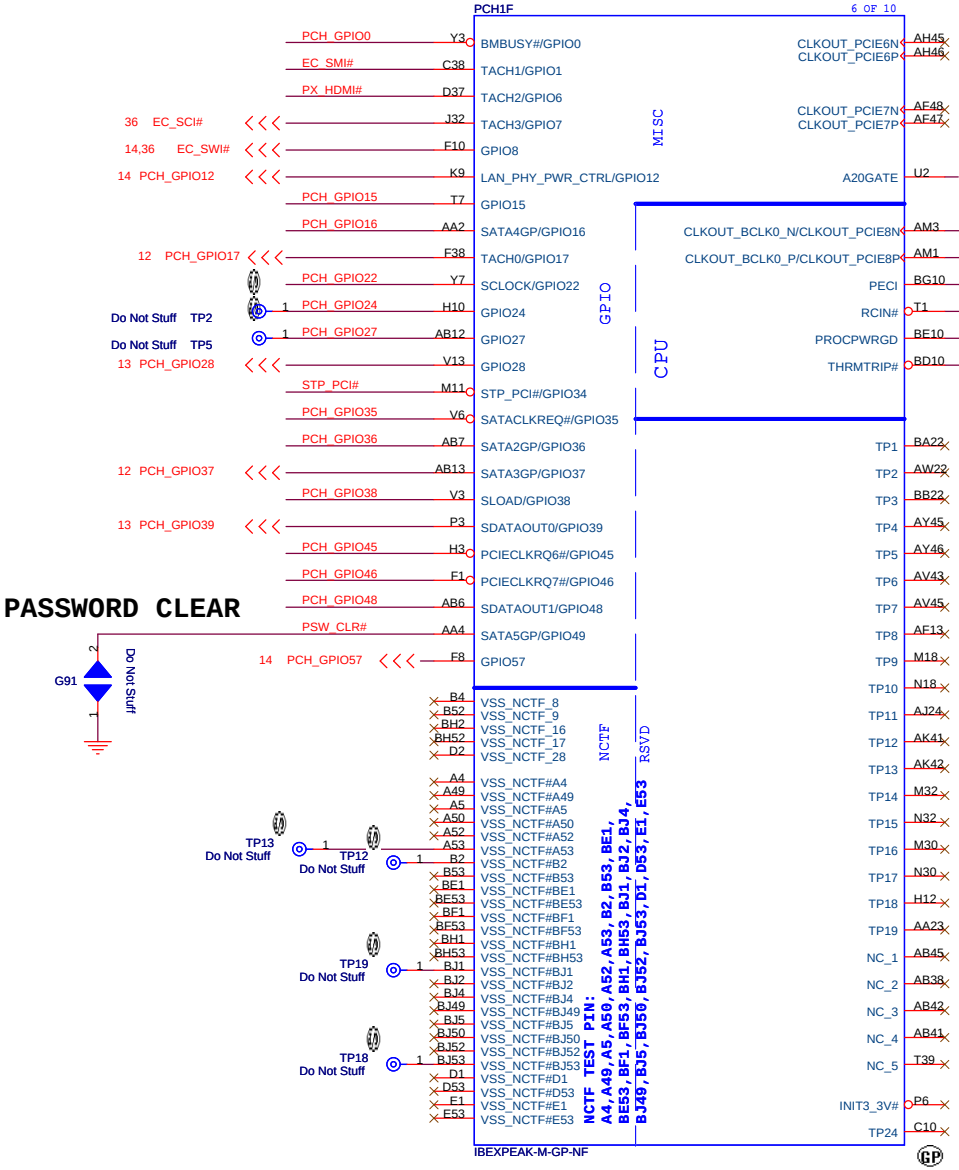
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.









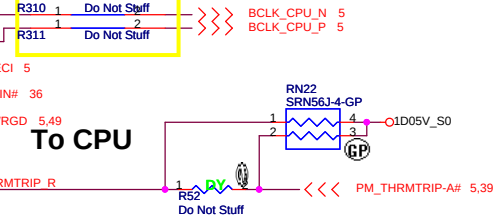


PASSWORD CLEAR

G91 Do Not Stuff

TP13 Do Not Stuff
TP12 Do Not Stuff
TP19 Do Not Stuff
TP18 Do Not Stuff

SB



JV10 CS

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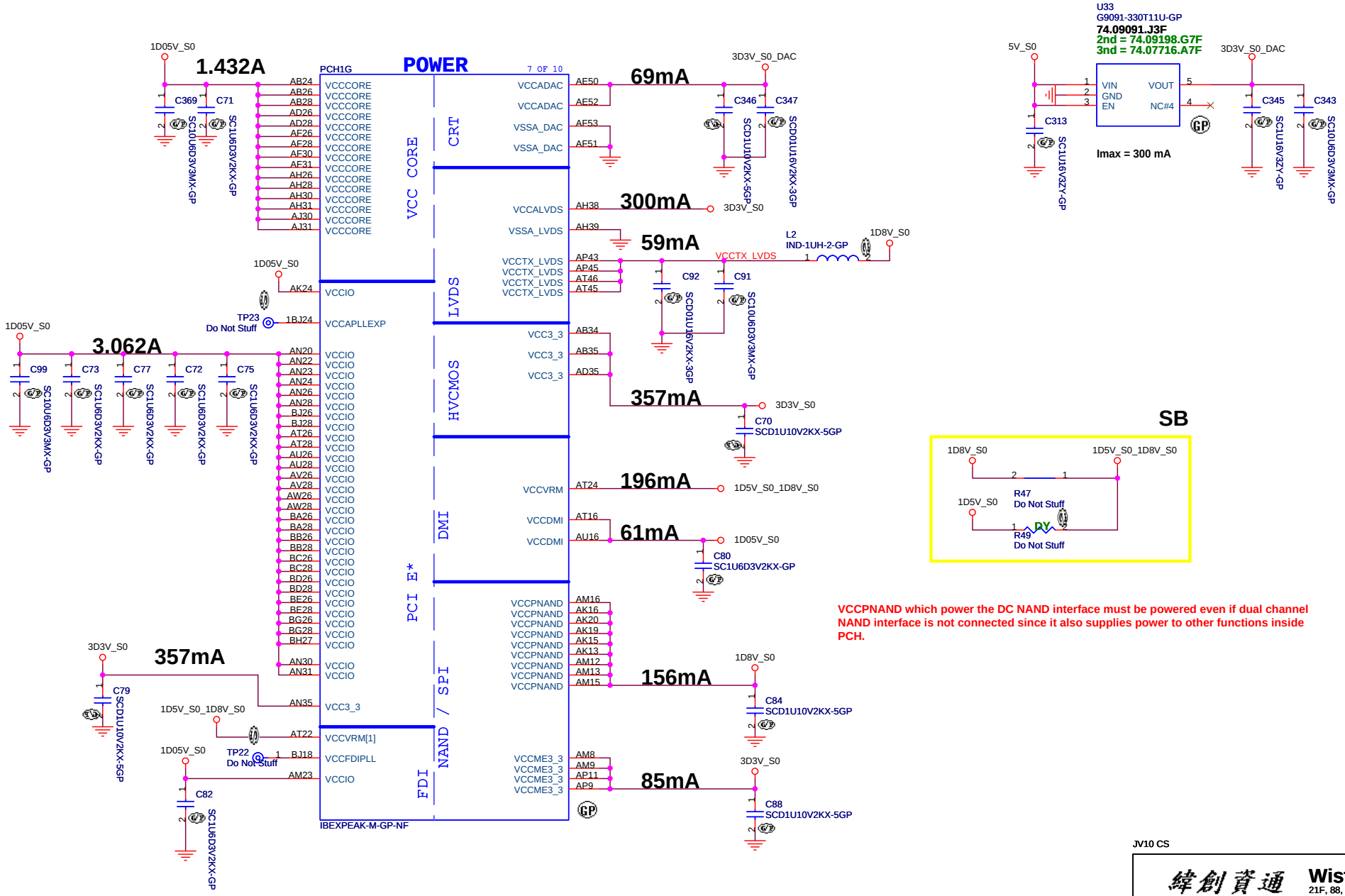
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 6 of 9(GPIO/RSVD)	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 17 of 50	



JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 7 of 9(PWR/VCORE/LVDS)**

Size	Document Number	Rev
Custom	JV10-CS	-1

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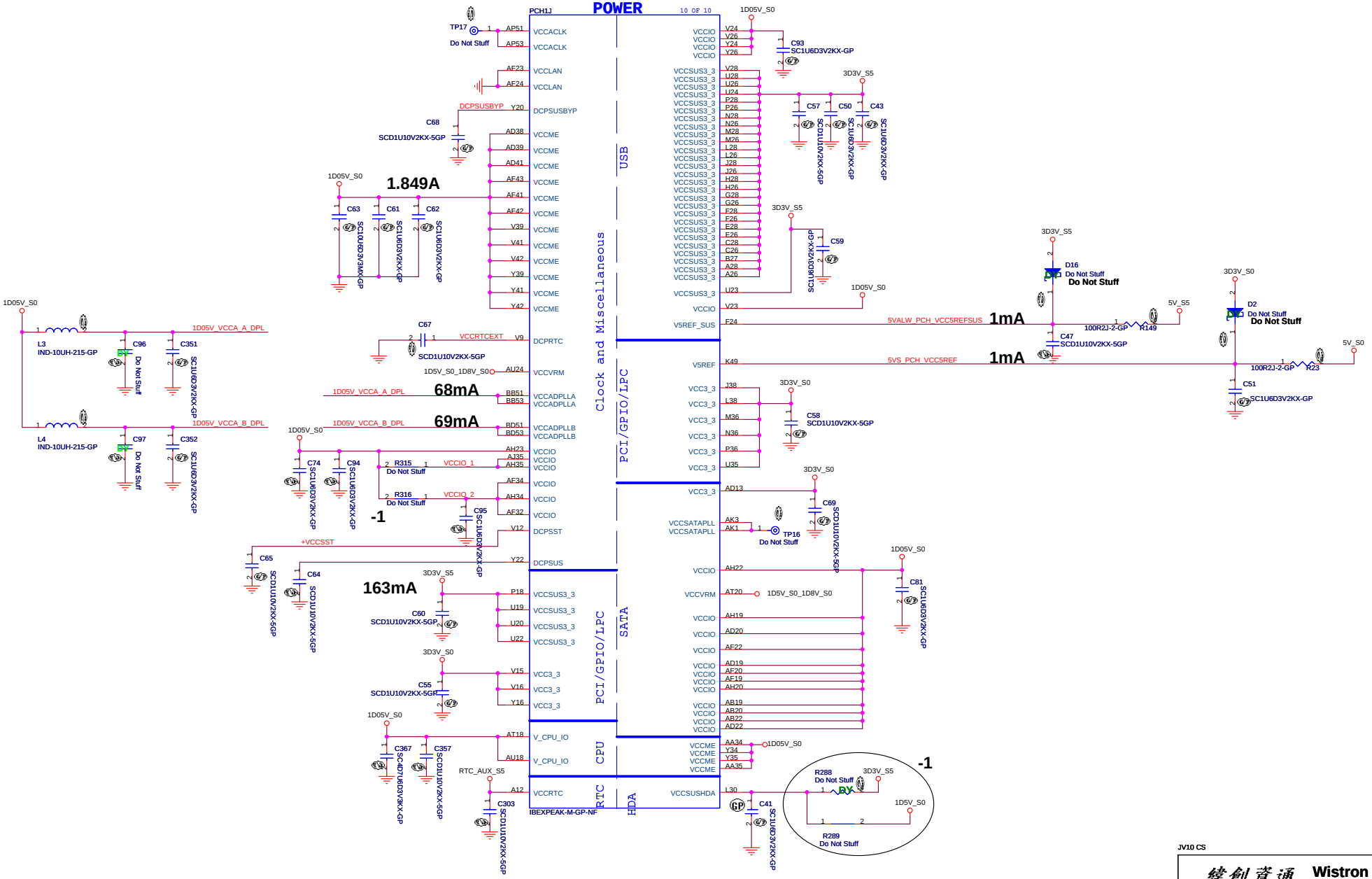
POWER
PCH1J
10 OF 10
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
1.849A
68mA
69mA
163mA
1mA
1mA
-1
-1
Do Not Stuff
1D05V_S0
3D3V_S5
3D3V_S0
5V_S5
5V_S0
1D05V_VCCA_A_DPL
1D05V_VCCA_B_DPL
+VCCSST
RTC_AUX_S5
1D05V_S0_1D8V_S0
5VALW_PCH_VCC5REFSUS
5VS_PCH_VCC5REF
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH 8 of 9(PWR\SATA\USB)
JV10-CS
Rev -1
Date: Friday, January 22, 2010
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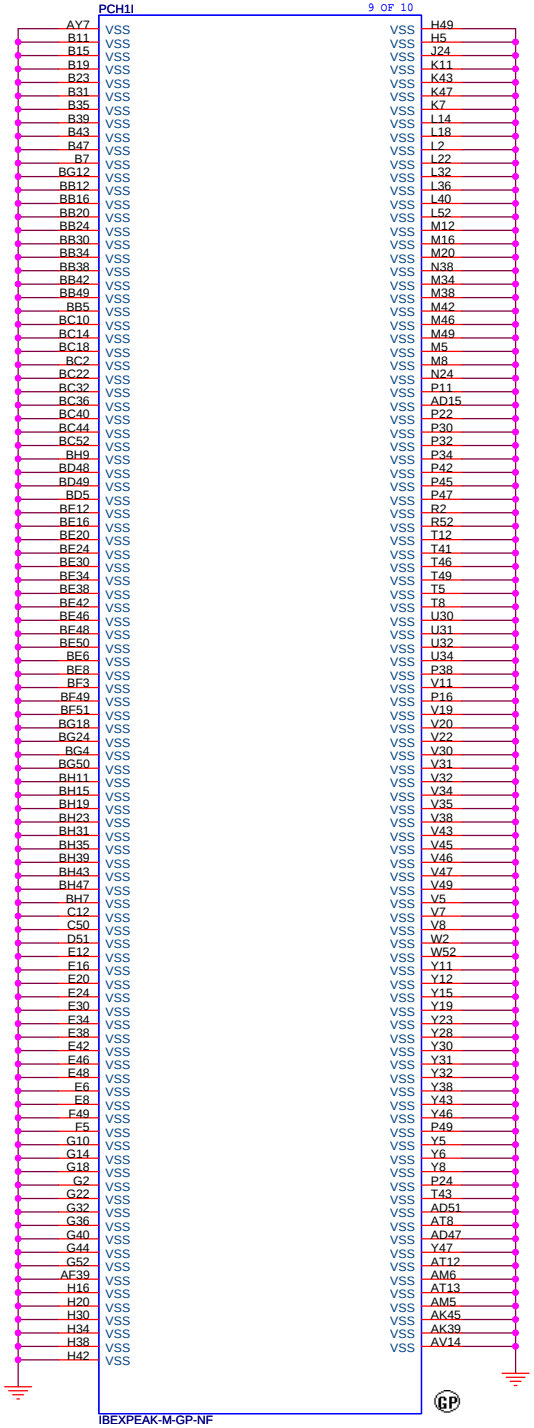

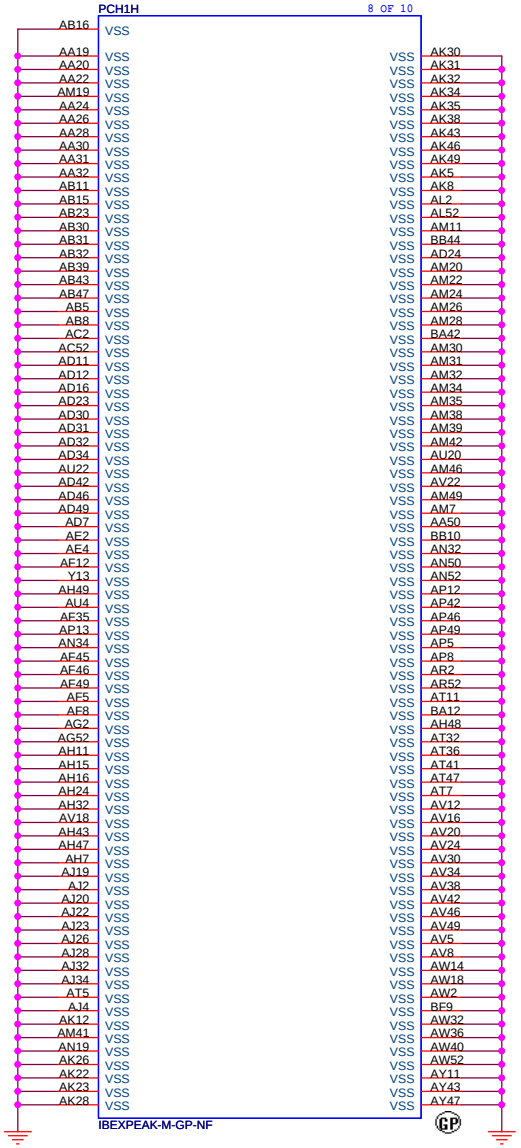

JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 9 of 9(VSS)**

Size	Document Number	Rev
A3	JV10-CS	-1

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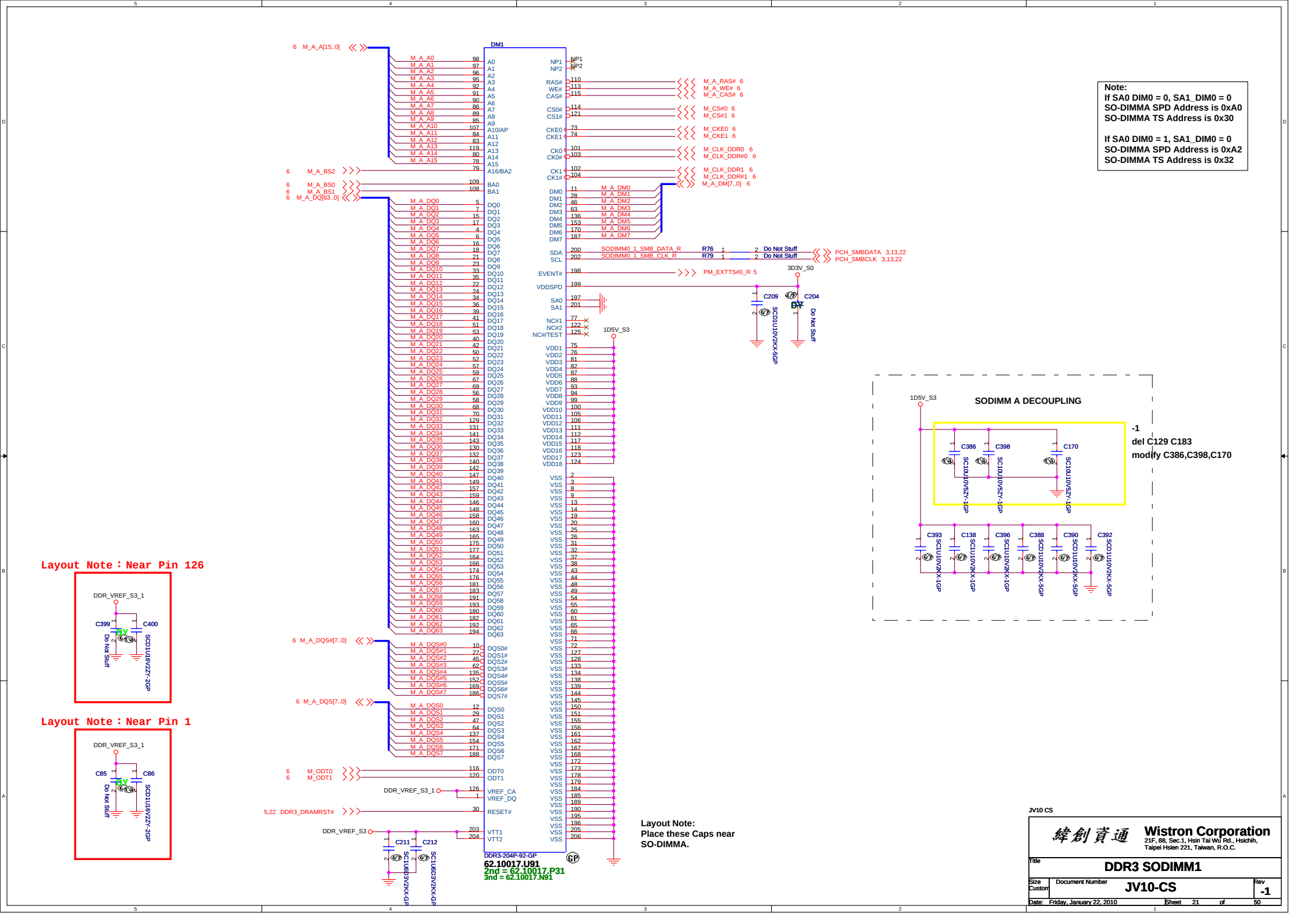
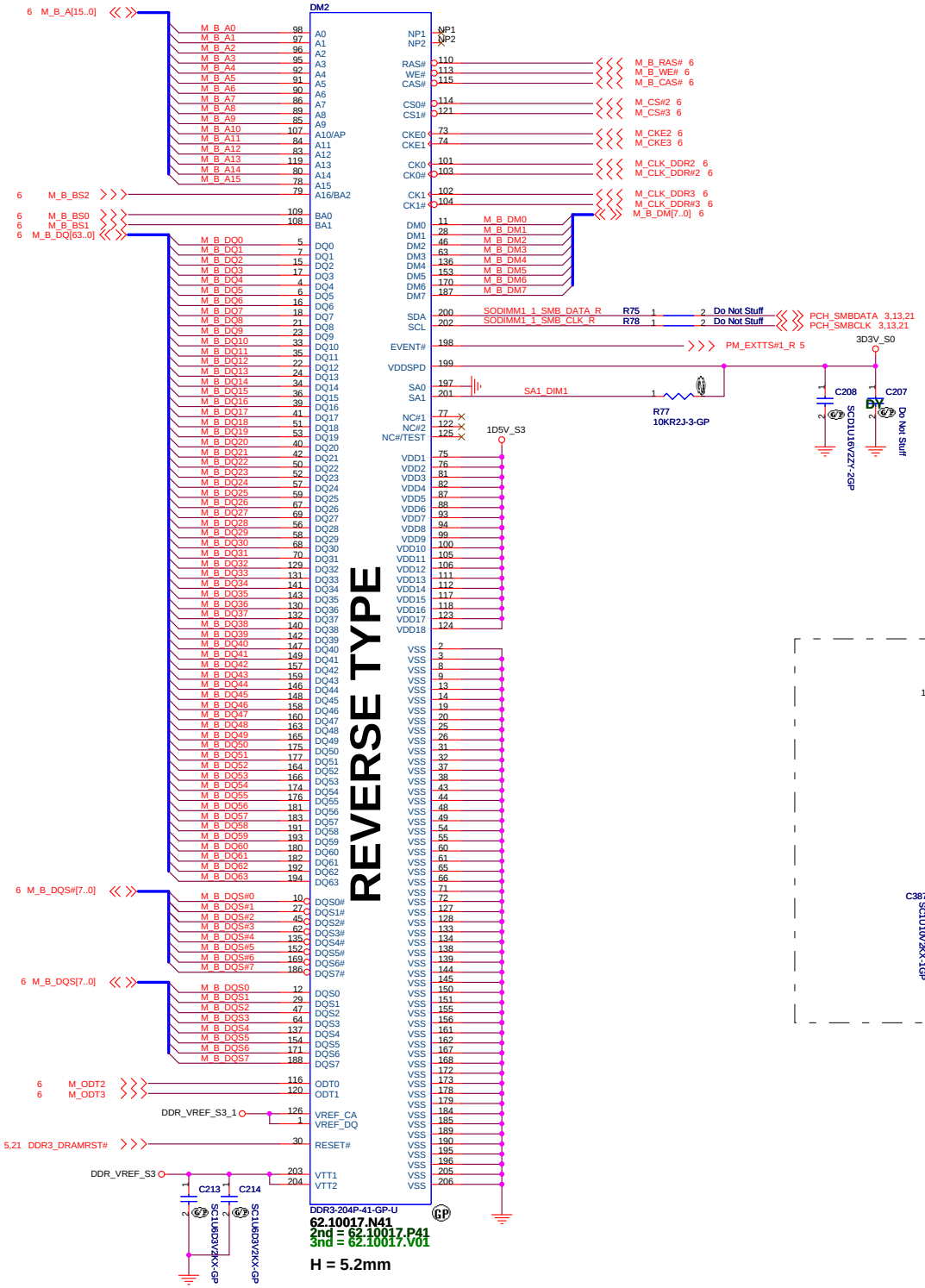
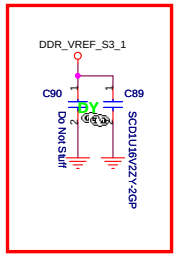
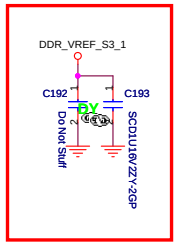

DM1
DDR3-204P-92-GP
62.10017.U91
2nd = 62.10017.P31
3nd = 62.10017.N91
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SODIMM A DECOUPLING
-1
del C129 C183
modify C386,C398,C170
Layout Note：Near Pin 126
Layout Note：Near Pin 1
Layout Note:
Place these Caps near
SO-DIMMA.
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3 SODIMM1
JV10-CS
-1
Date: Friday, January 22, 2010
Sheet 21 of 50

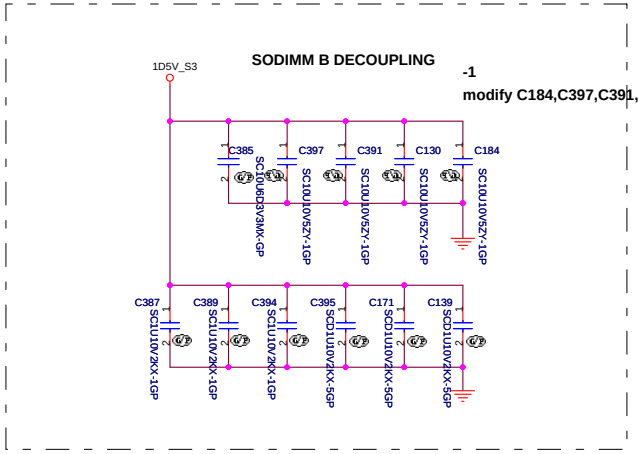


Layout Note : Near Pin 1



Layout Note : Near Pin 126





JV10 CS

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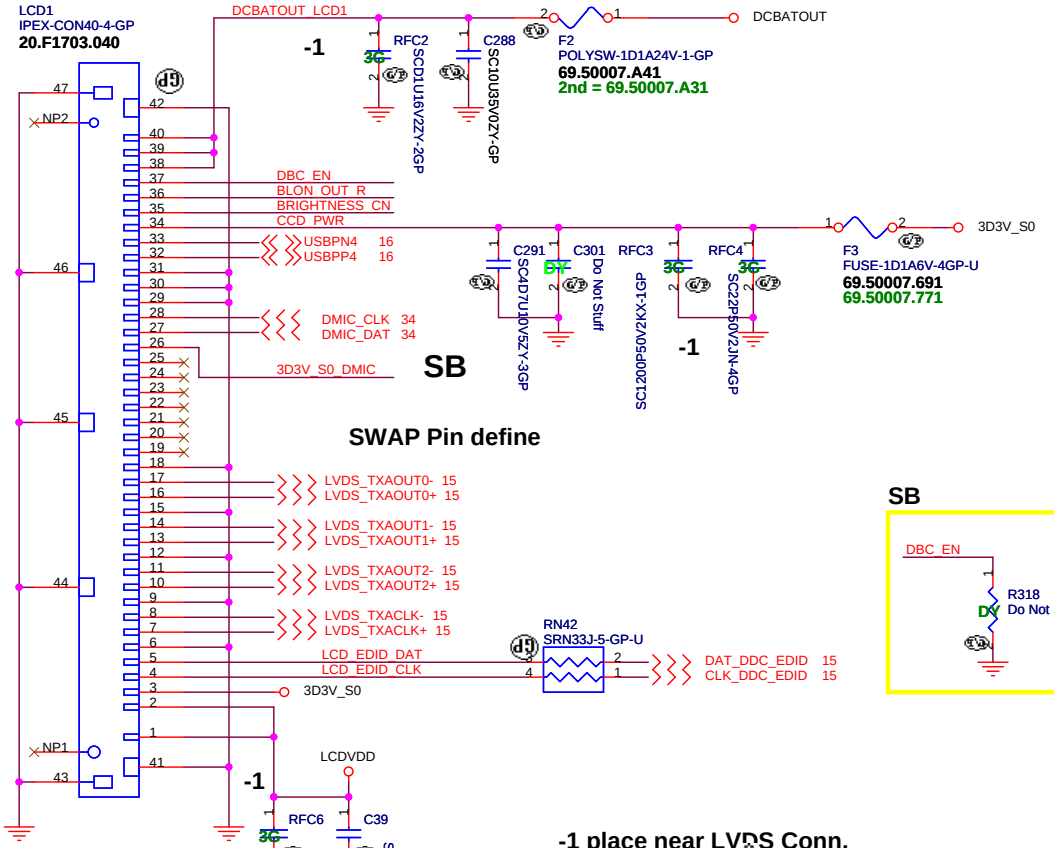
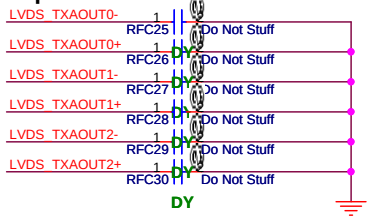
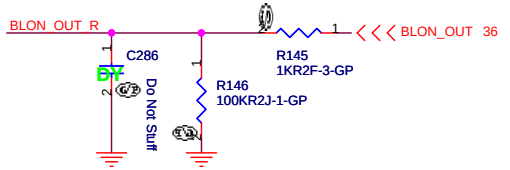
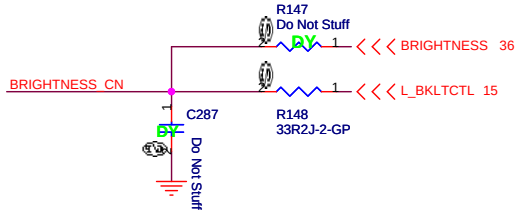
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3 SODIMM2		
Size: Custom	Document Number: JV10-CS		Rev: -1
Date: Friday, January 22, 2010	Sheet 22 of 50		





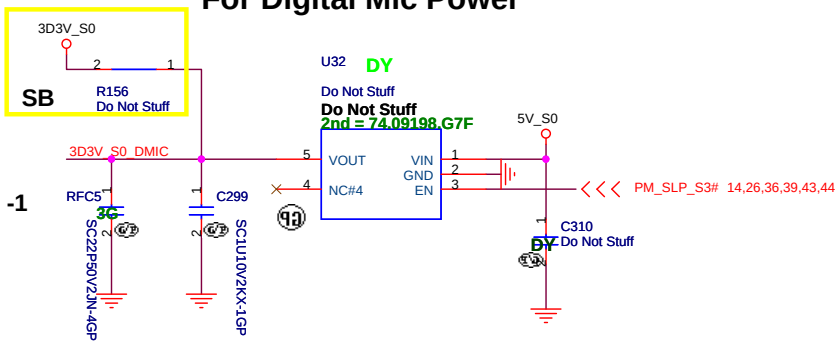




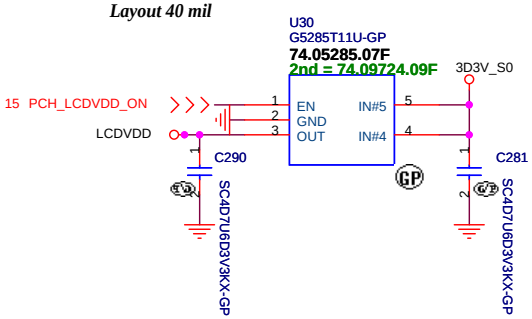
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND

For Digital Mic Power



Layout 40 mil

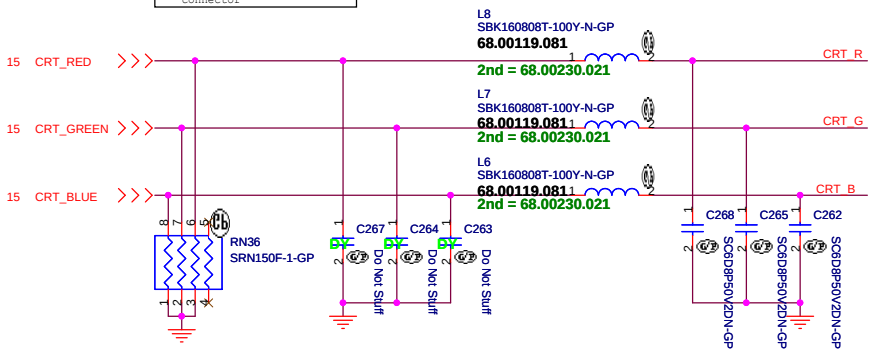


JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CCD CONN	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 23 of 50	

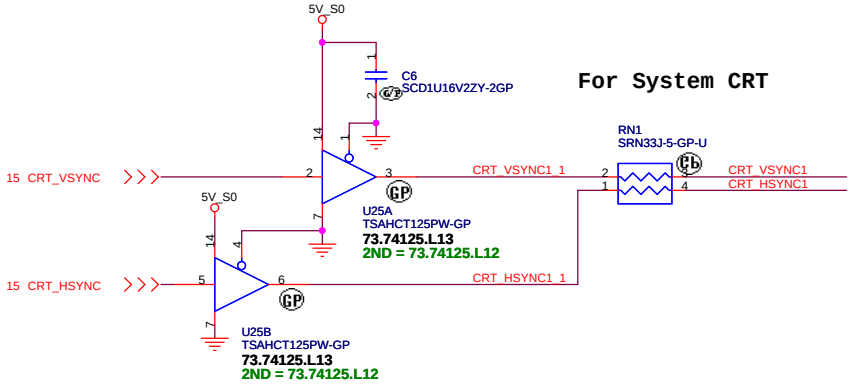
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

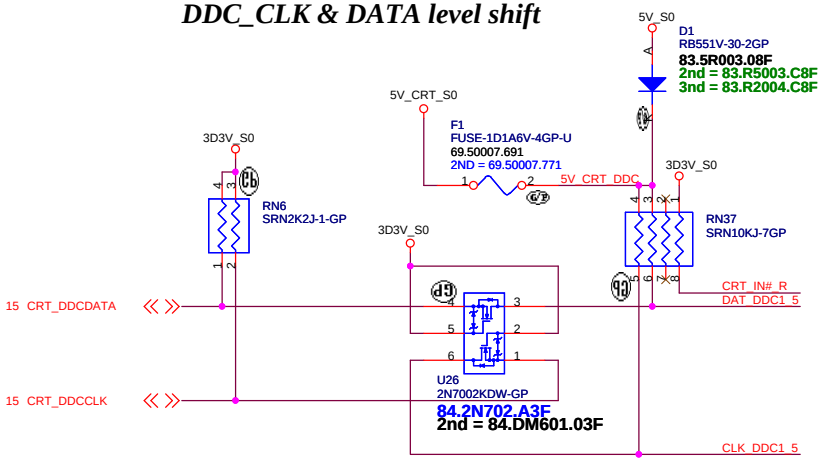


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

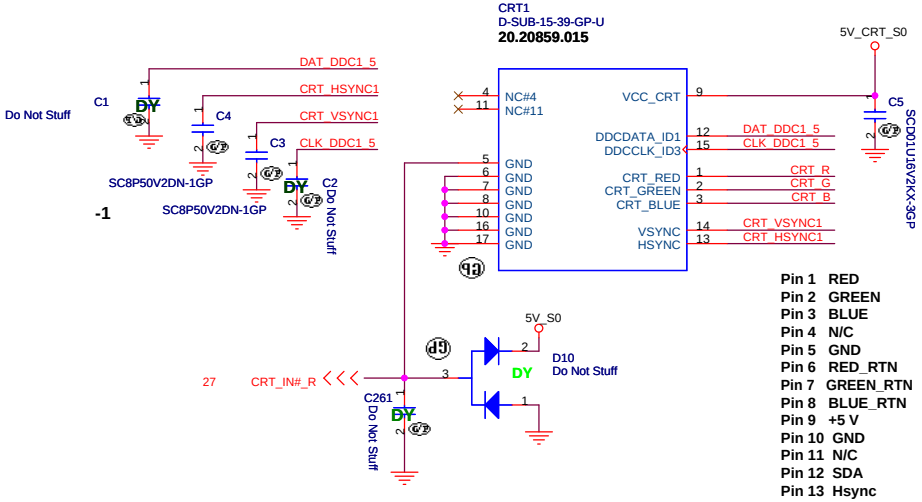
Hsync & Vsync level shift



DDC_CLK & DATA level shift



CRT I/F & CONNECTOR



Pin 1 RED
Pin 2 GREEN
Pin 3 BLUE
Pin 4 N/C
Pin 5 GND
Pin 6 RED_RTN
Pin 7 GREEN_RTN
Pin 8 BLUE_RTN
Pin 9 +5 V
Pin 10 GND
Pin 11 N/C
Pin 12 SDA
Pin 13 Hsync
Pin 14 VSync
Pin 15 SCL

JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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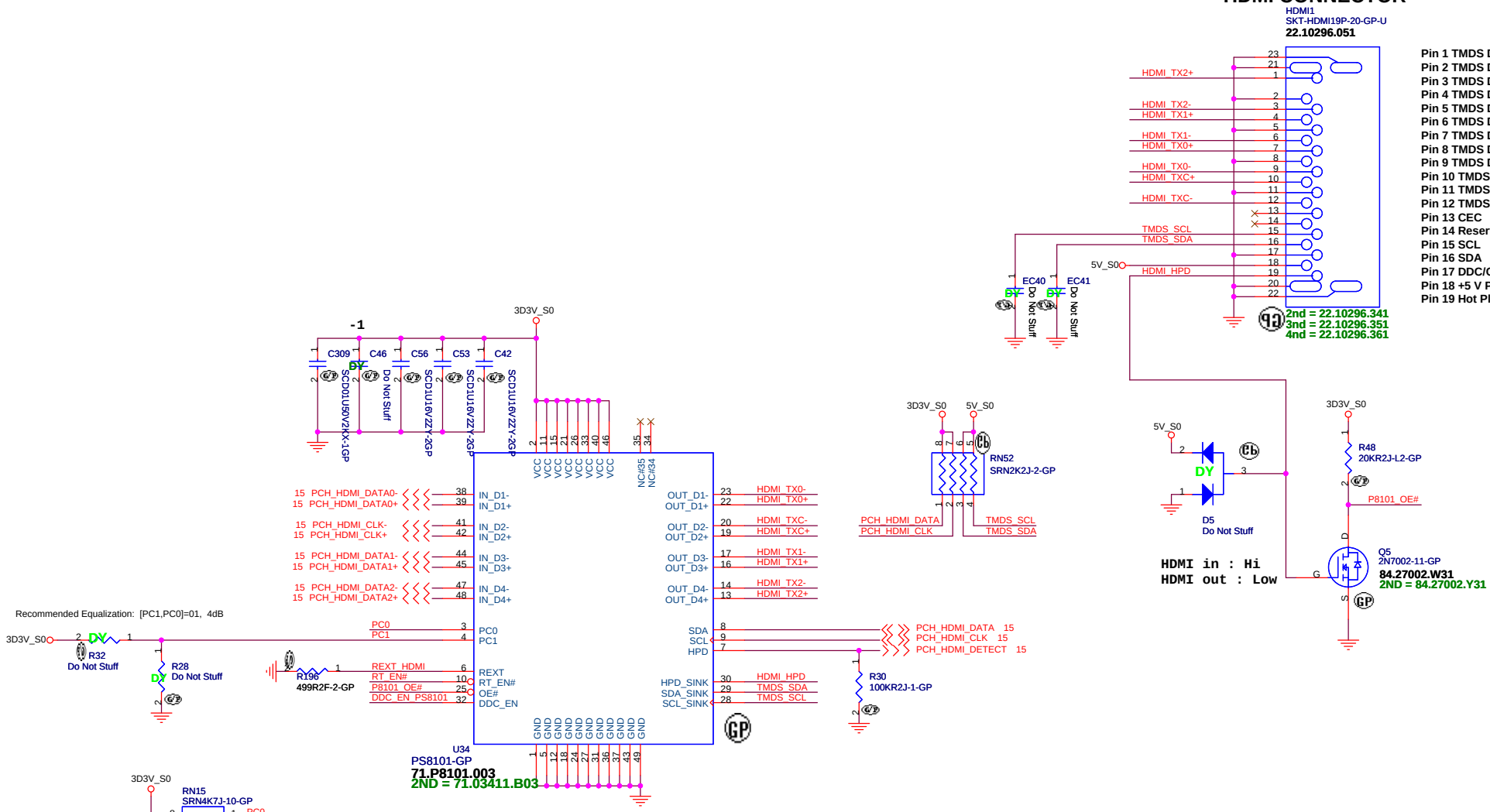
Title: **CRT conn**		
Size: A3	Document Number: **JV10-CS**	Rev: **-1**
Date: Friday, January 22, 2010	Sheet 24 of 50	

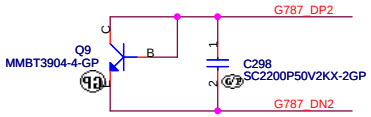
HDMI CONNECTOR



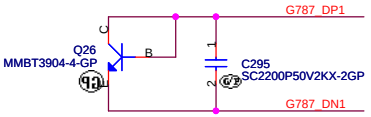
JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **HDMI conn**		
Size: Custom	Document Number: **JV10-CS**	Rev: **-1**
Date: Friday, January 22, 2010	Sheet 25 of 50	

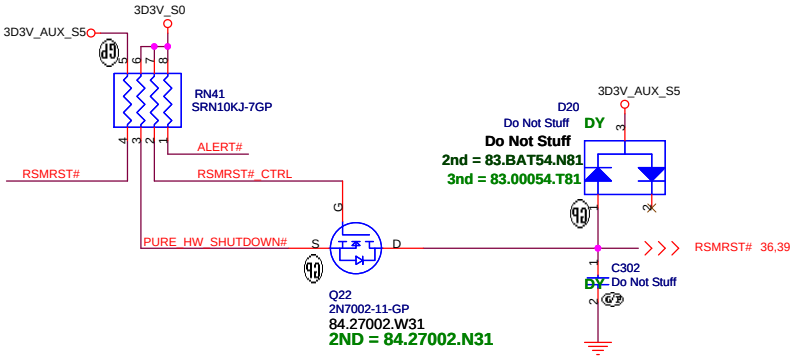
For T8 thermal diode



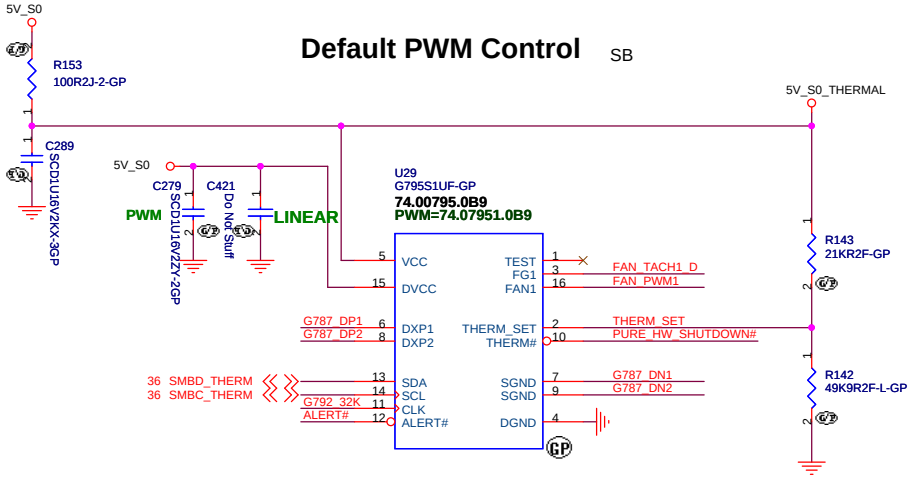
For System thermal diode



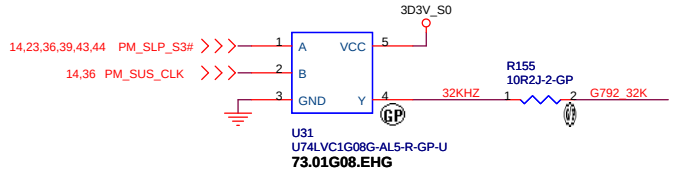
C298& C295 CLOSE to G795



Default PWM Control SB



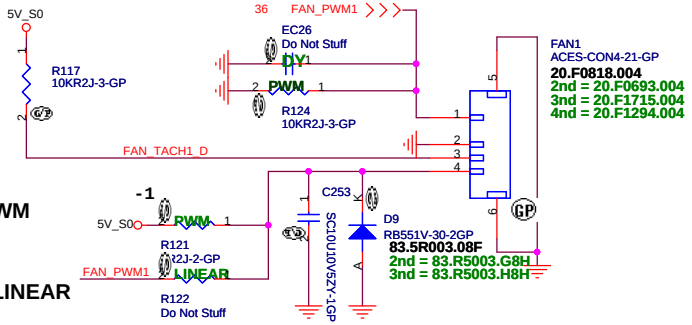
T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC



CPU FAN Connector

PWM FAN		LINEAR FAN	
PIN1	PWM	PIN1	NC
PIN2	GND	PIN2	GND
PIN3	FG	PIN3	FG
PIN4	VCC	PIN4	VCC

PWM FOR EC



JV10 CS

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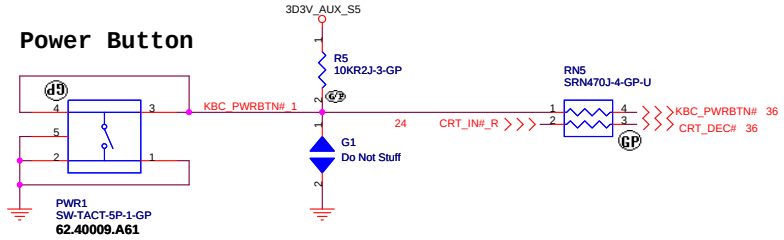
Taipei Hsien 221, Taiwan, R.O.C.

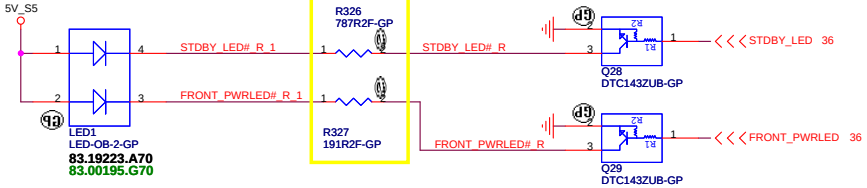
Title	**Thermal/Fan Conn**	
Size A3	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 26 of 50	

Power Button

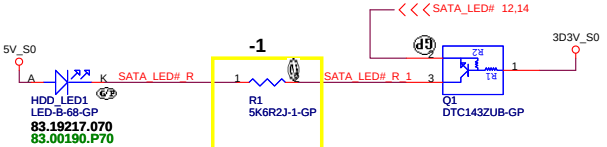


Power Button LED
(BLUE/ORANGE)

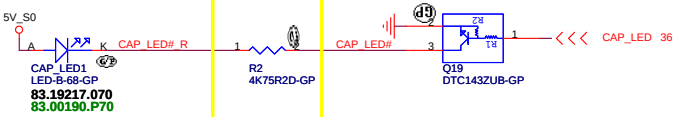
-1



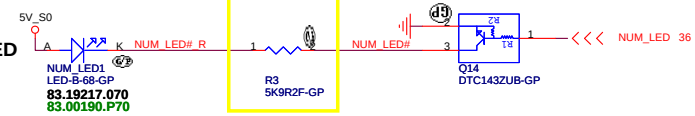
HDD LED (BLUE)



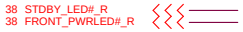
CAP LED (BLUE)



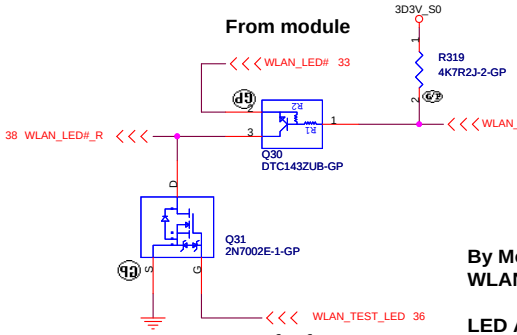
NUM LED (BLUE)



To USBCN1 Connector



From module



for factory test

From KBC

Delete ALL LED OFF

ALL LED OFF GPIO14 change WLAN_LED
WLAN_LED GPIO81 change WLAN_TEST_LED

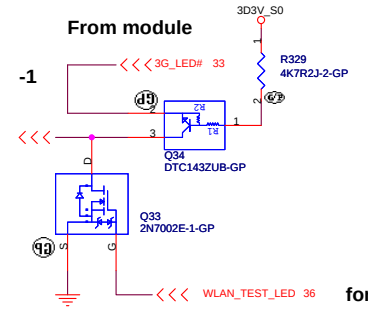
By Module (LED Flash)
WLAN_LED_OFF# High

LED Always On
WLAN_LED_OFF# Low
WLAN_TEST_LED High

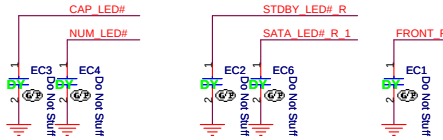
Factory test use
WLAN_TEST_LED High

From module

-1



for factory test



JV10 CS

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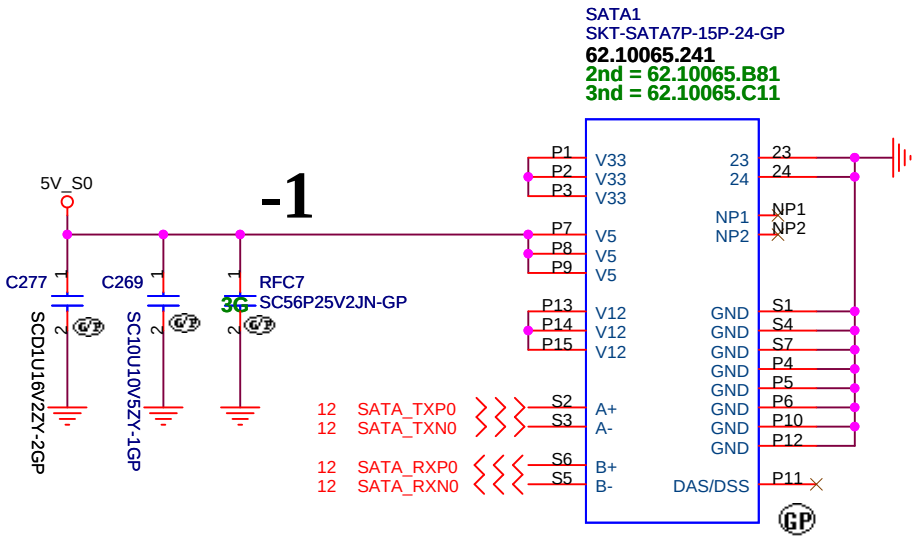
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LED**	
Size: Custom	Document Number: **JV10-CS**	Rev: **-1**
Date: Friday, January 22, 2010	Sheet 27 of 50	

SATA Connector



JV10 CS

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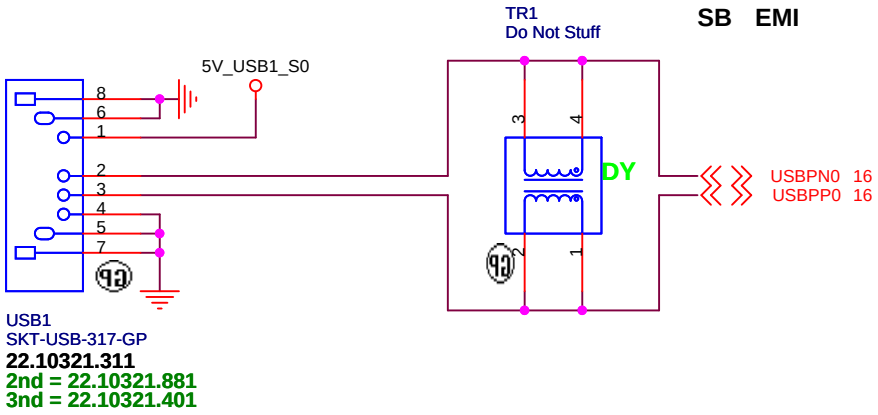
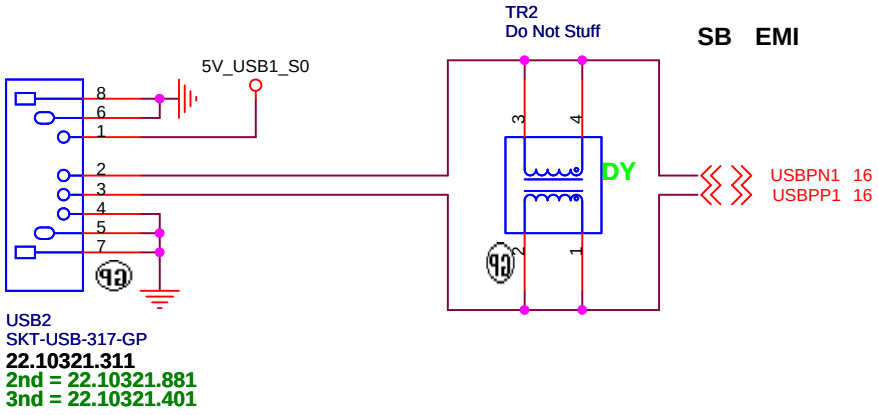
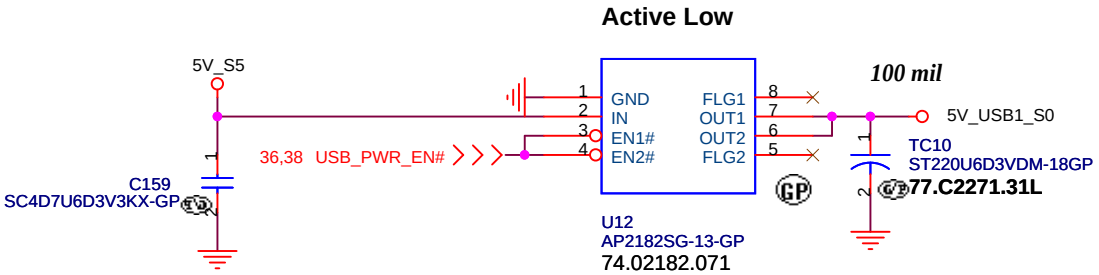
Title: *HDD*		
Size: A4	Document Number: JV10-CS	Rev: *-1*
Date: Friday, January 22, 2010	Sheet 28 of 50	

USB MODULE







JV10 CS

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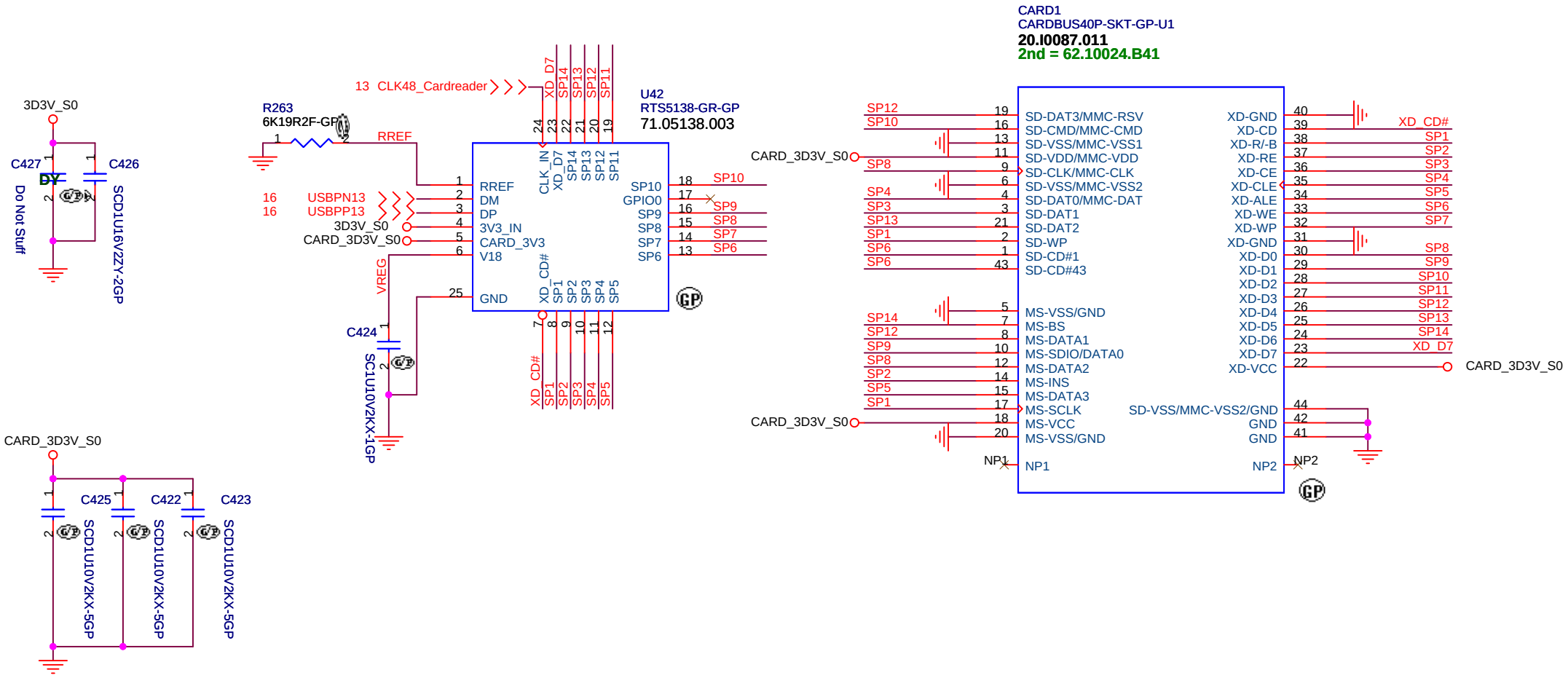
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB Port*	
Size A4	Document Number JV10-CS	Rev *-1*
Date: Friday, January 22, 2010	Sheet 29 of 50	

5 IN1 CARD-READER

SB
與 ALPS Co-Layout



Near CARD1 Pin11, Pin18, Pin22

JV10 CS

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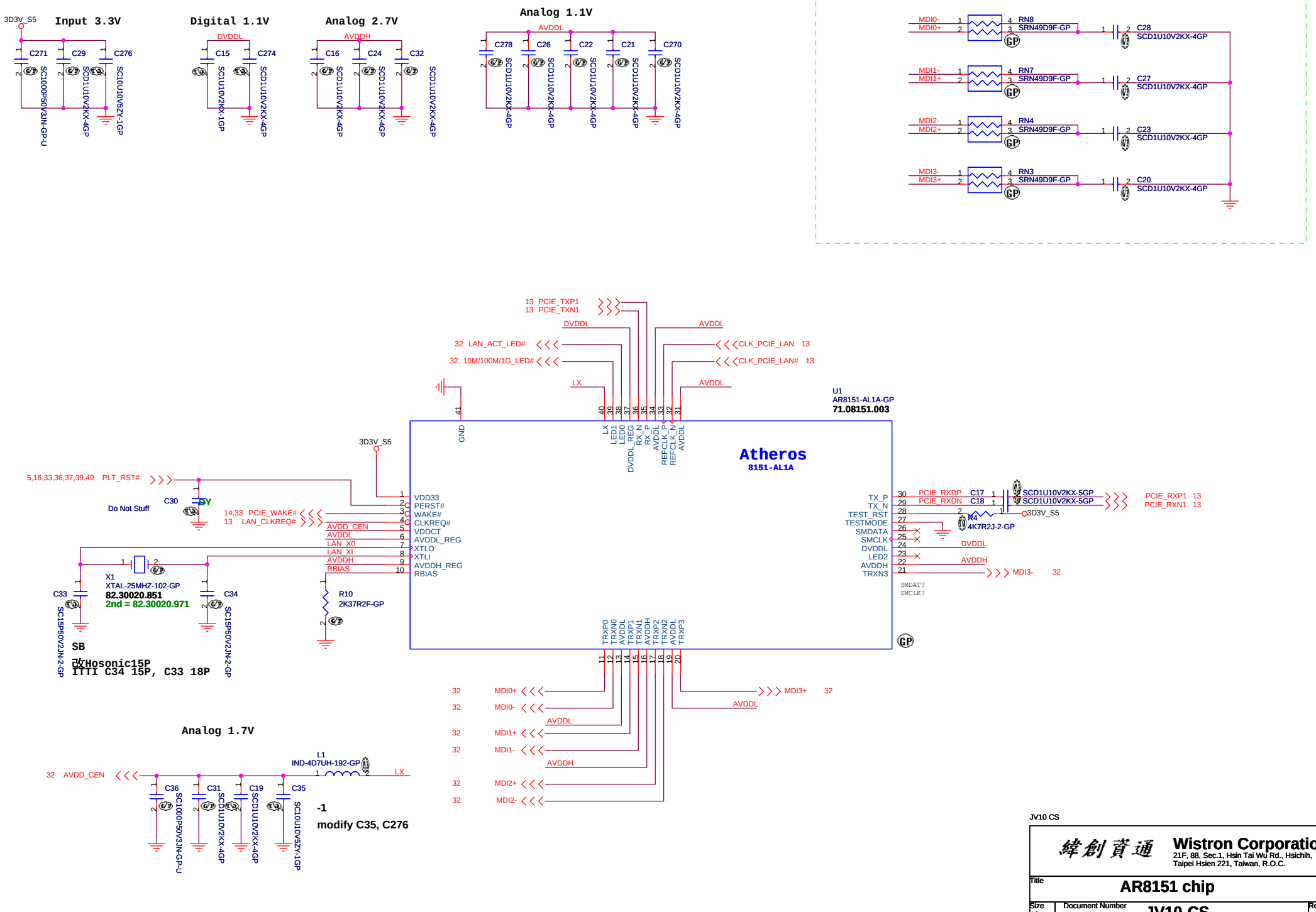
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CARDREADER***	
Size A4	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 30 of 50	



JV10 CS

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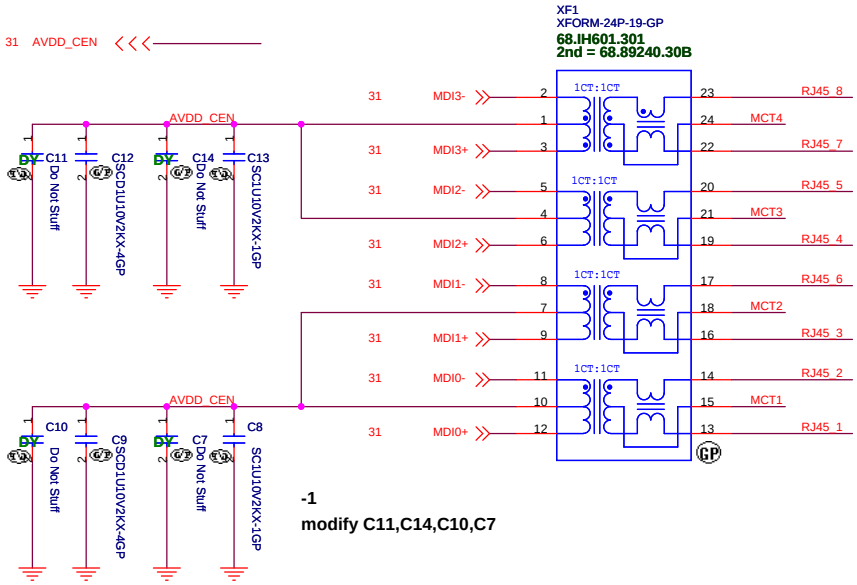
Title: AR8151 chip		
Size: A3	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 31 of 50	

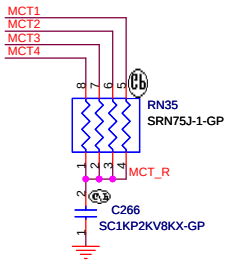
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

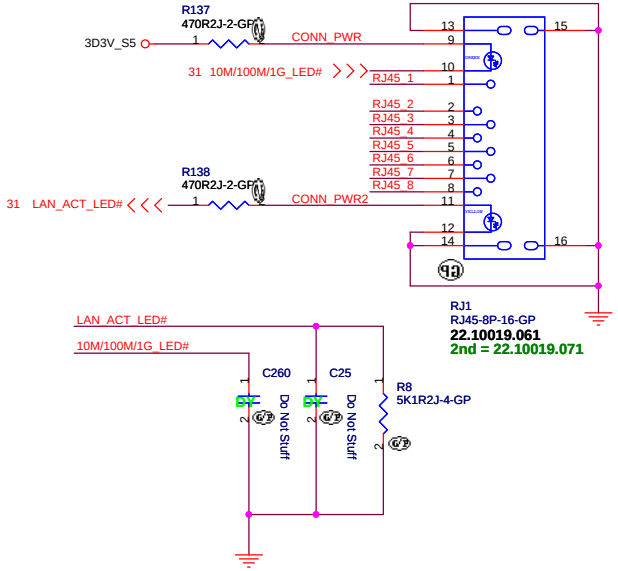
LAN Connector

GIGA Lan Transformer



-1
modify C11,C14,C10,C7





LED COLOR

B1(+) B2(-)::GREEN

A1(+) A2(-):YELLOW

Green(A3), behavior is the same for 10/100/1000 bits

Yellow(B2), when LAN is transfering data.

JV10 CS

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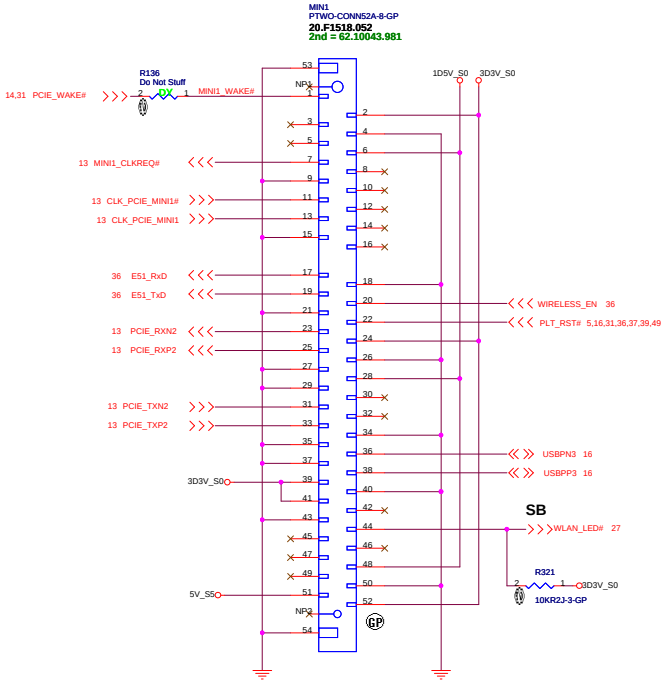
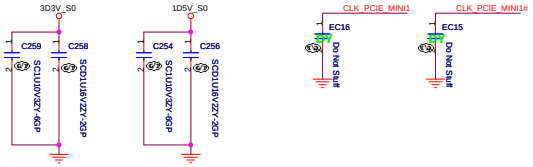
Title: LAN Connector		
Size: A3	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 32 of 50	

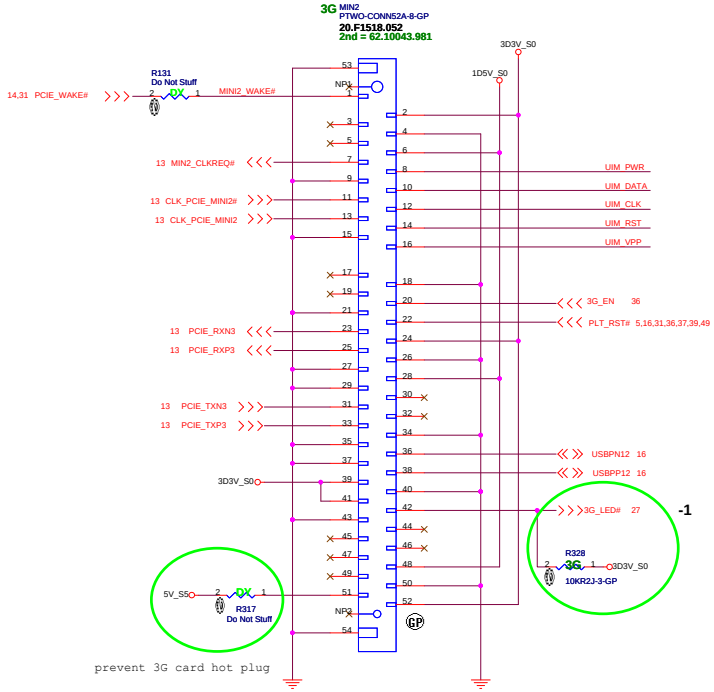
Mini Card Connector(WLAN)
Support debug-card



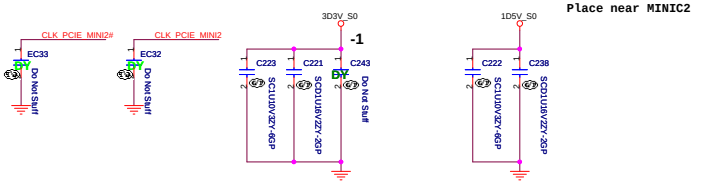
Place near MINI1



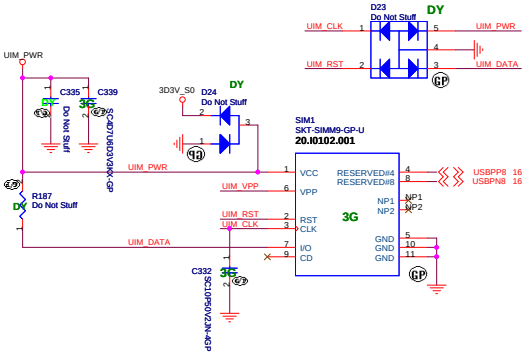
Mini Card Connector(3G)



Place near MINIC2

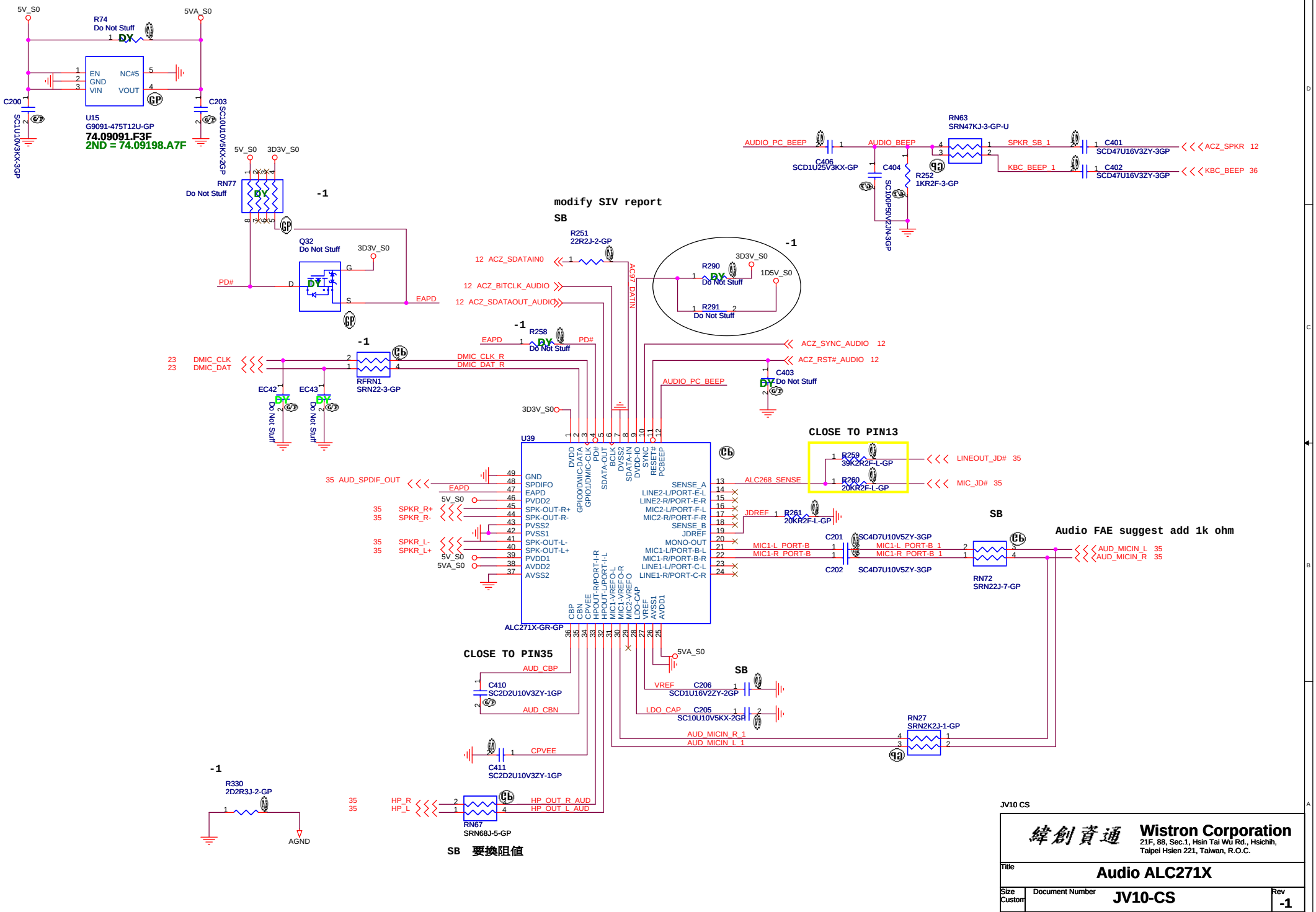


SIM Card



JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI Conn	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 33 of 50	



JV10 CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Audio ALC271X		
Size: Custom	Document Number: JV10-CS	Rev: -1
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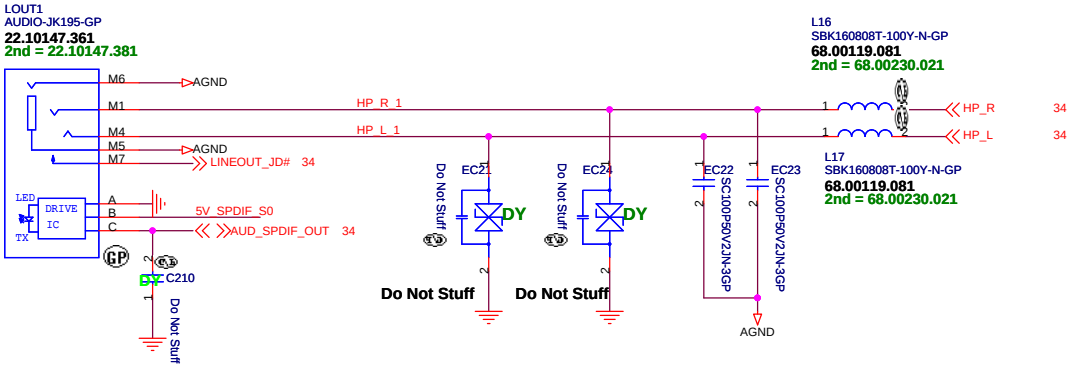
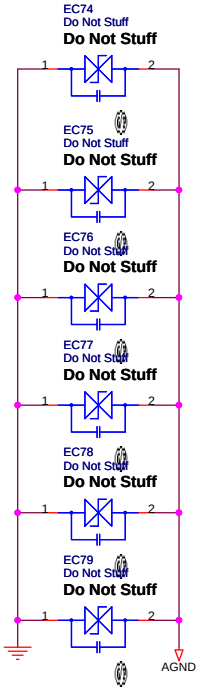
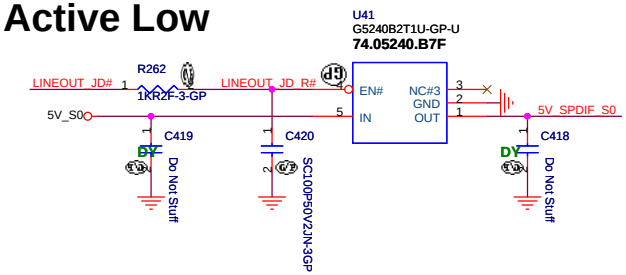
LINE OUT

SB

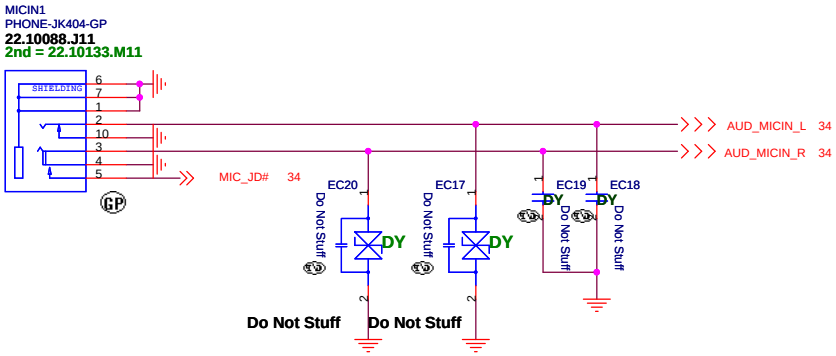




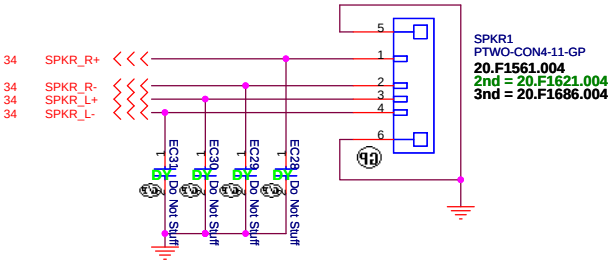
Active Low



MIC IN



Internal Speaker



JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio Jack/Mic In/ SPKR*

Size	Document Number	Rev
A3	JV10-CS	-1

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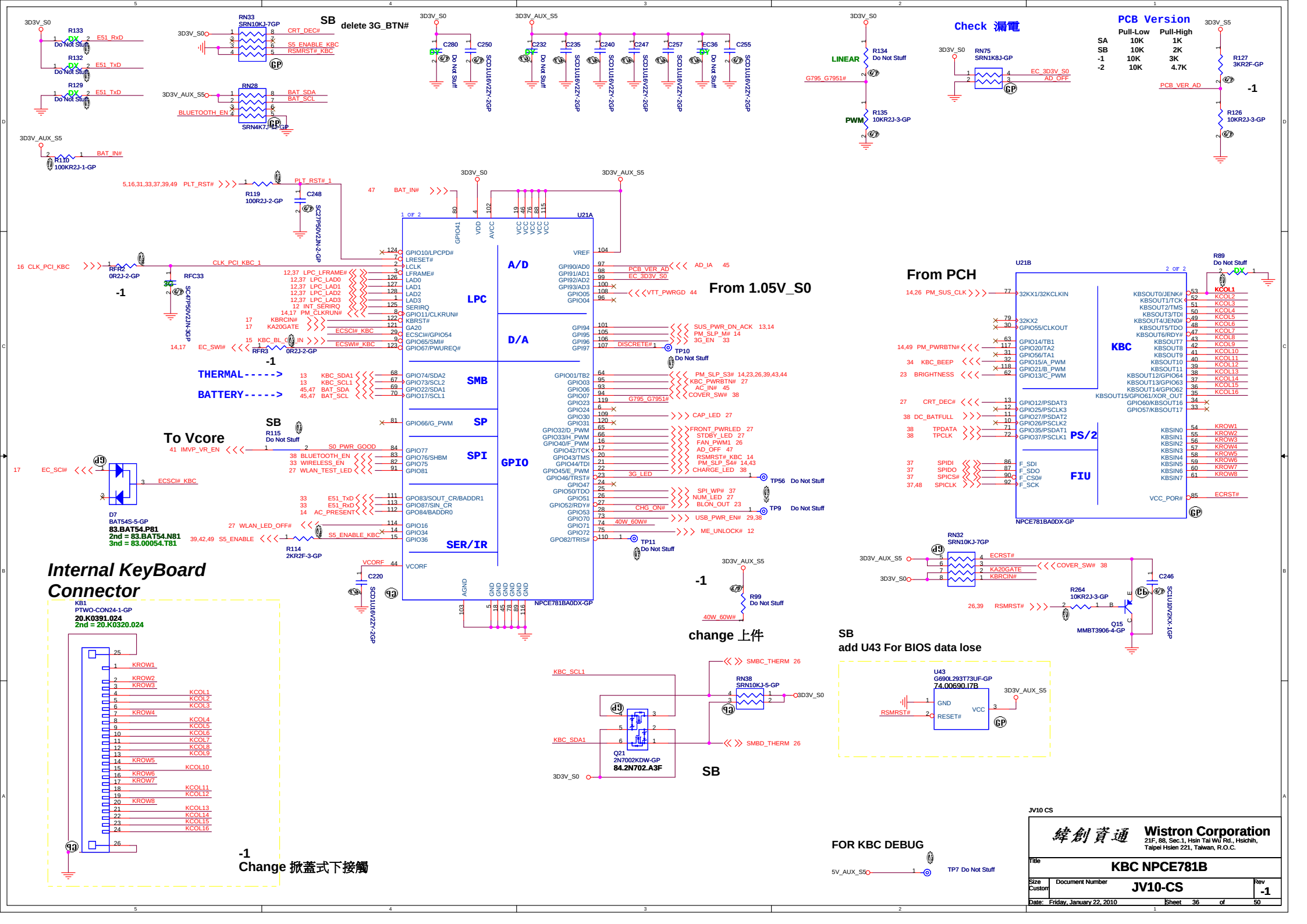
SB
delete 3G_BTN#
PCB Version
Pull-Low Pull-High
SA 10K 1K
SB 10K 2K
-1 10K 3K
-2 10K 4.7K
Check 漏電
LINEAR
PWM
From 1.05V_S0
From PCH
To Vcore
THERMAL----->
BATTERY----->
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
U21A
U21B
NPCE781BA0DX-GP
Internal KeyBoard Connector
KB1
PTWO-CON24-1-GP
20.K0391.024
2nd = 20.K0320.024
-1
Change 掀蓋式下接觸
change 上件
SB
add U43 For BIOS data lose
U43
G690L293T73UF-GP
74.00690.I7B
FOR KBC DEBUG
Q21
2N7002KDW-GP
84.2N702.A3F
D7
BAT54S-5-GP
83.BAT54.P81
2nd = 83.BAT54.N81
3nd = 83.00054.T81
Do Not Stuff
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
JV10-CS
Rev -1
Date: Friday, January 22, 2010
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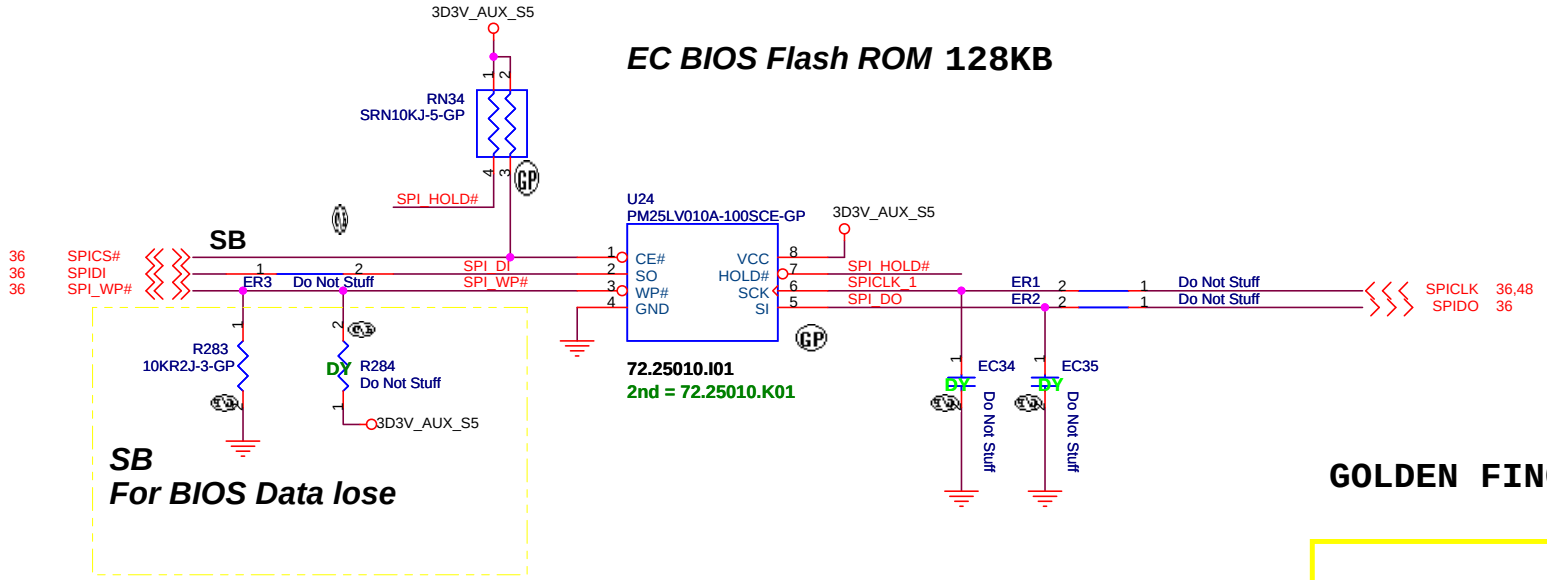

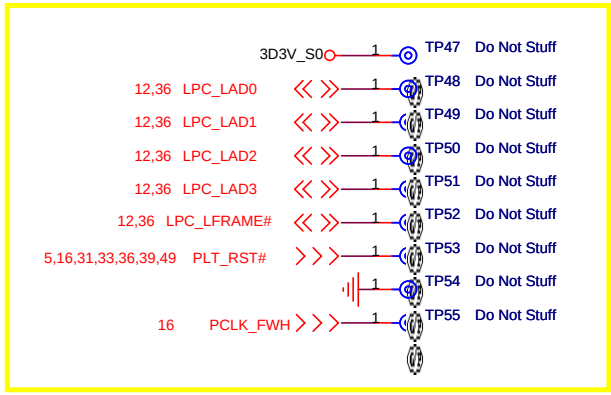

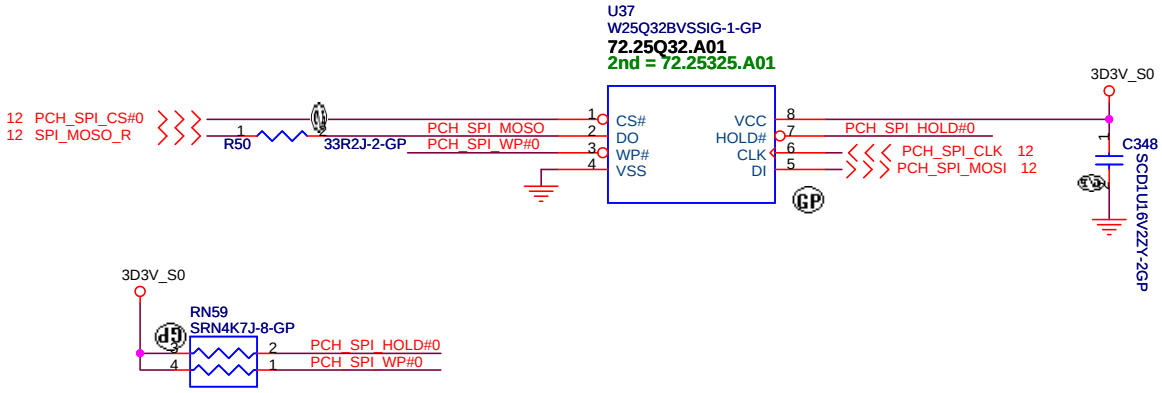

JV10 CS

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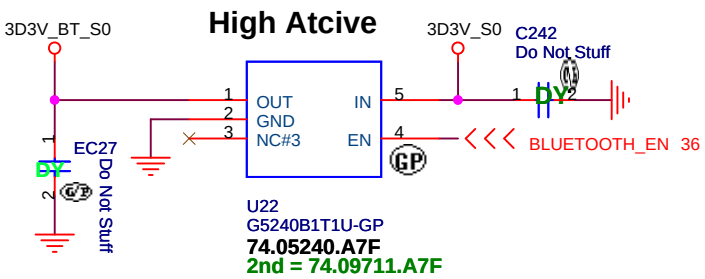
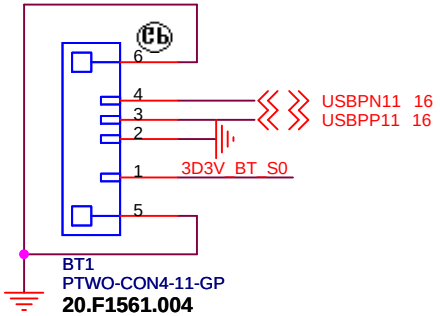
Title	**BIOS**	
Size: Custom	Document Number: **JV10-CS**	Rev: **-1**
Date: Friday, January 22, 2010	Sheet 37 of 50	

BLUETOOTH Connector

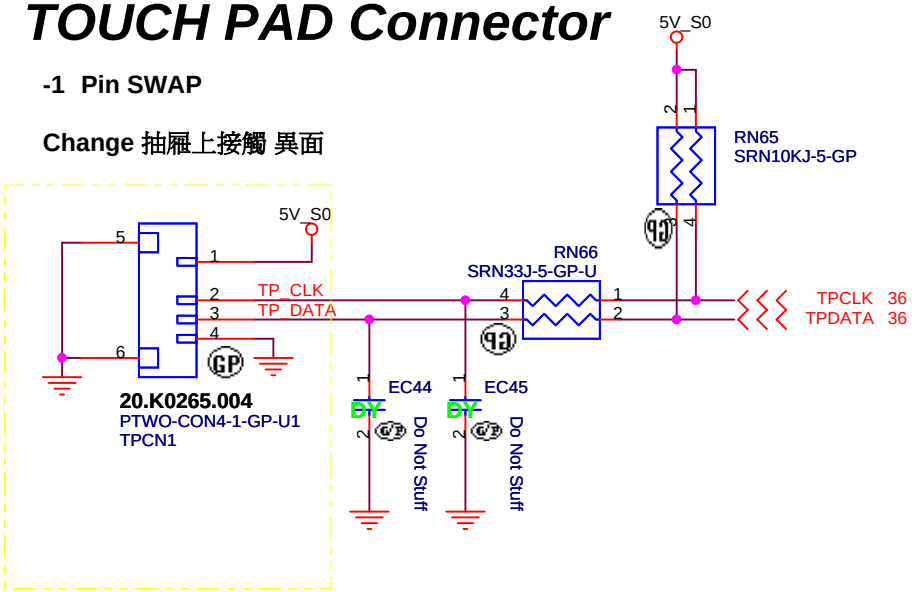




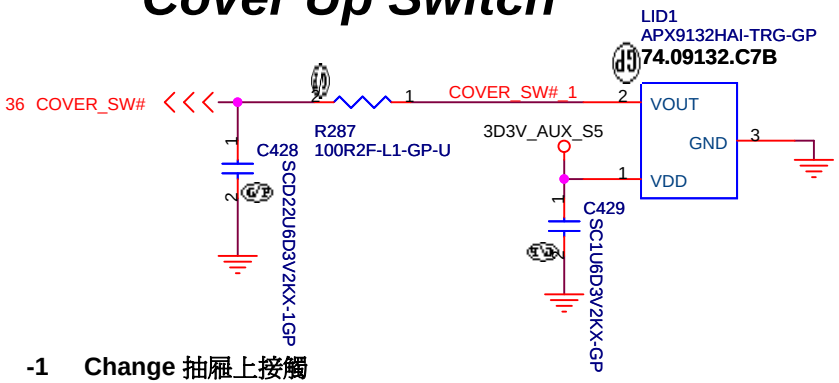
TOUCH PAD Connector

-1 Pin SWAP

Change 抽屜上接觸 異面

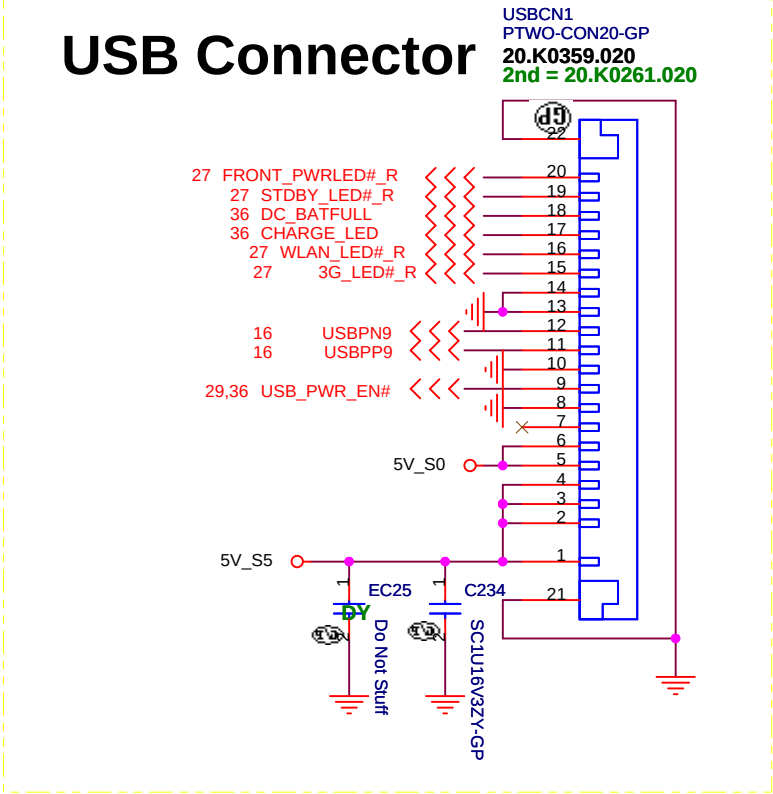


Cover Up Switch



-1 Change 抽屜上接觸

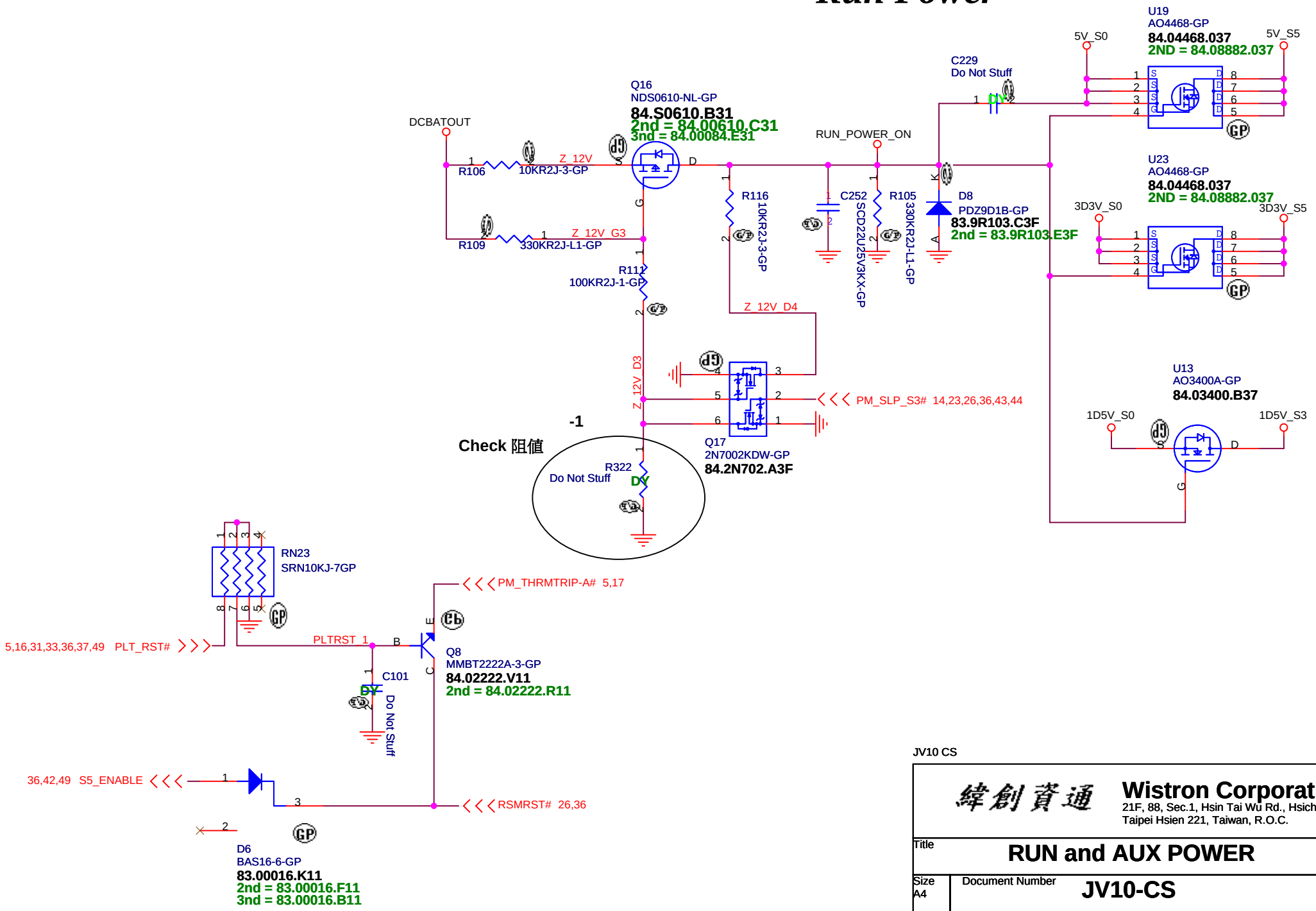
USB Connector



JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CONNECTOR**	
Size A4	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 38 of 50	

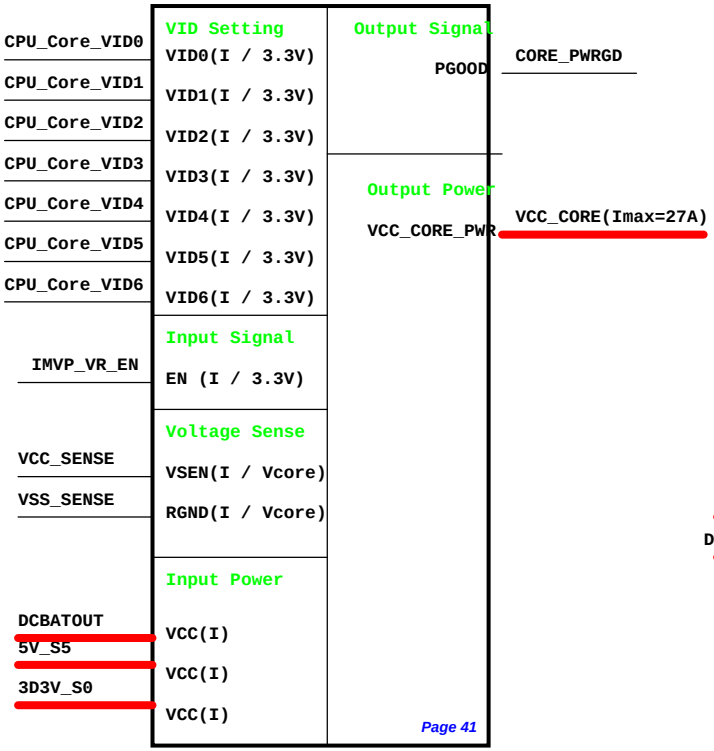
Run Power



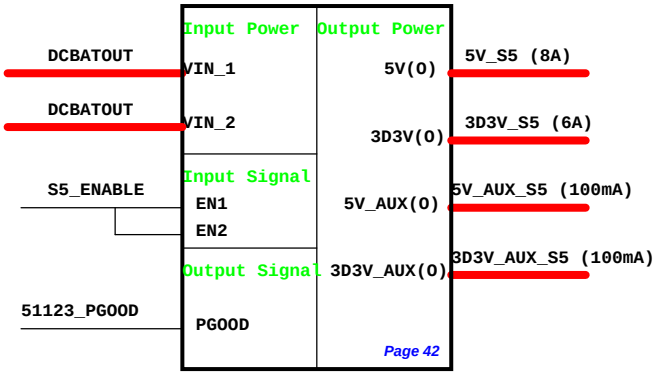
JV10 CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: RUN and AUX POWER			
Size: A4	Document Number: JV10-CS		Rev: -1
Date: Friday, January 22, 2010	Sheet 39 of 50		

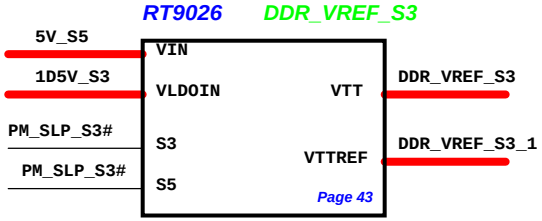
TPS51611 VCC_CORE



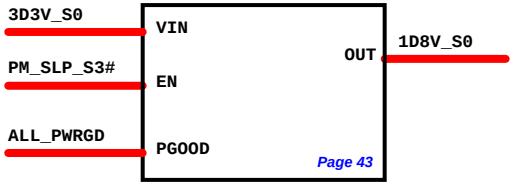
RT8223 5V/3D3V_S5



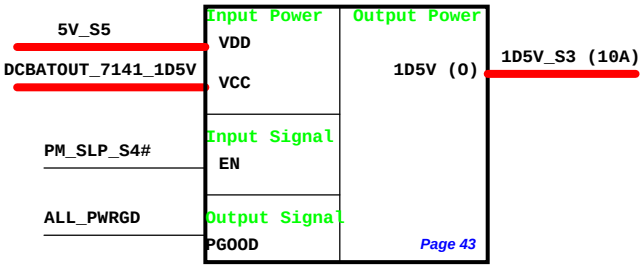
RT9026 DDR_VREF_S3



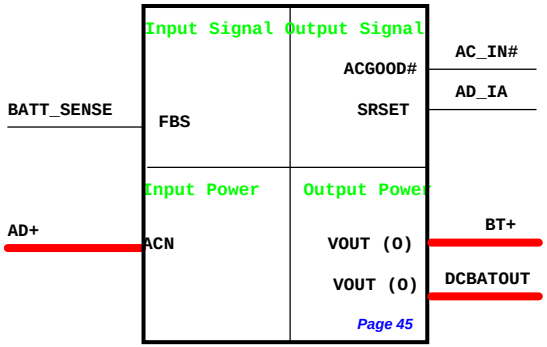
RT9025 1D8V_S0



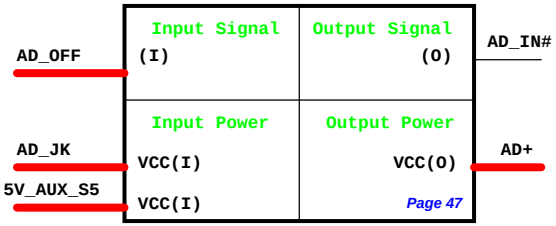
RT8209E 1D5V_S3



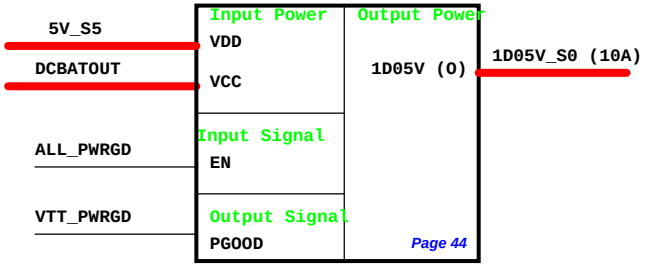
Charger ISL88731A



Adapter

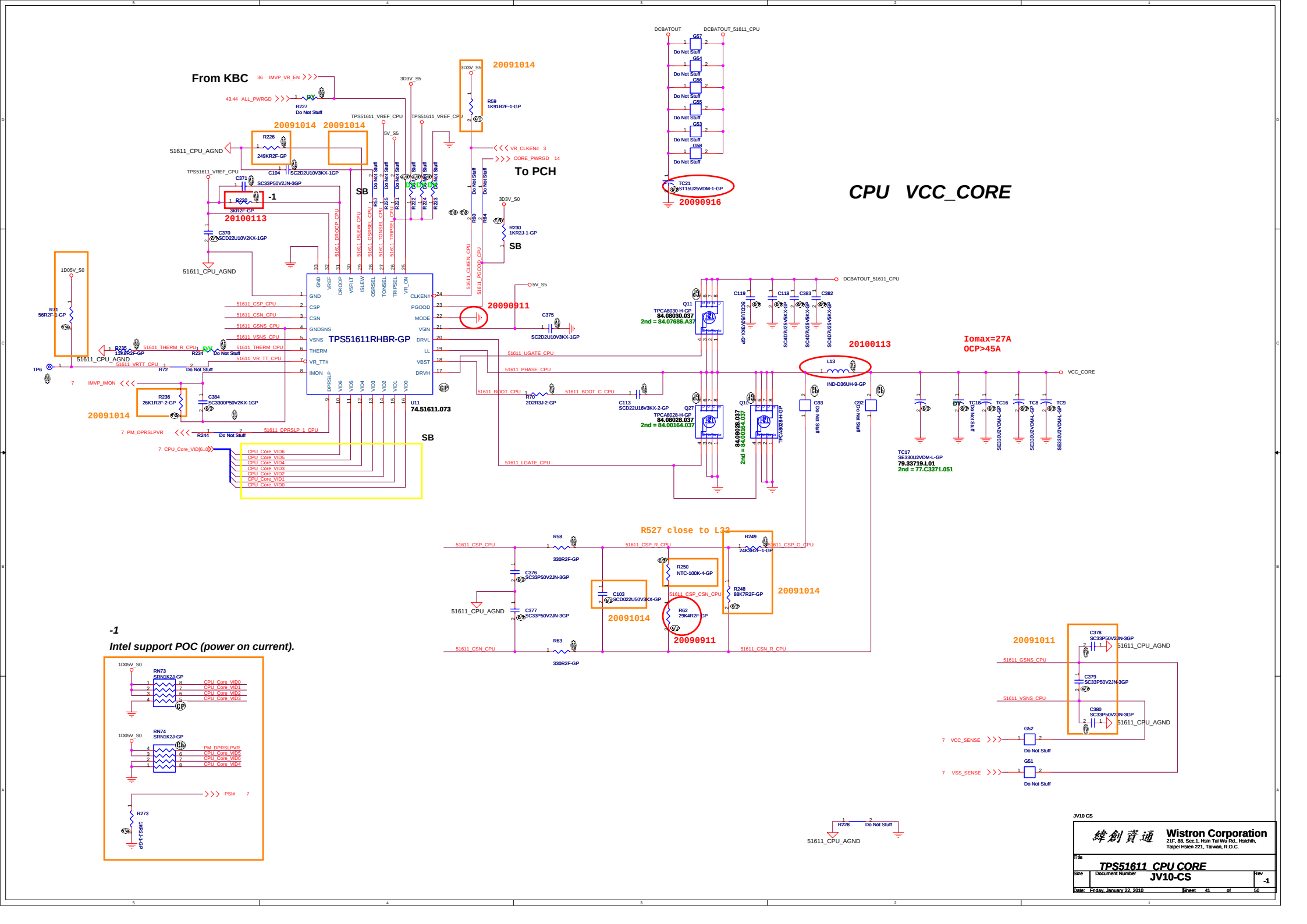


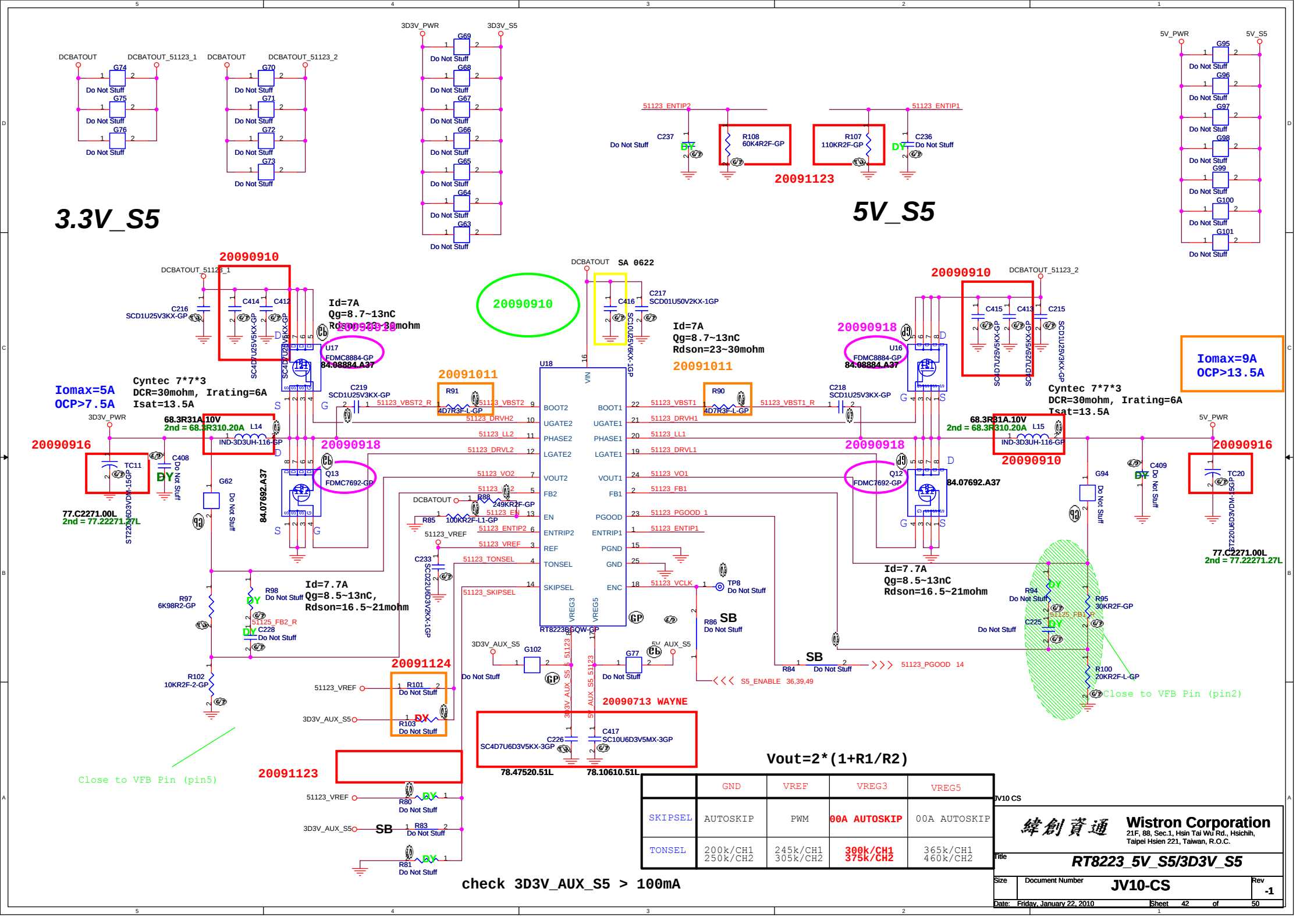
RT8209B 1D05V



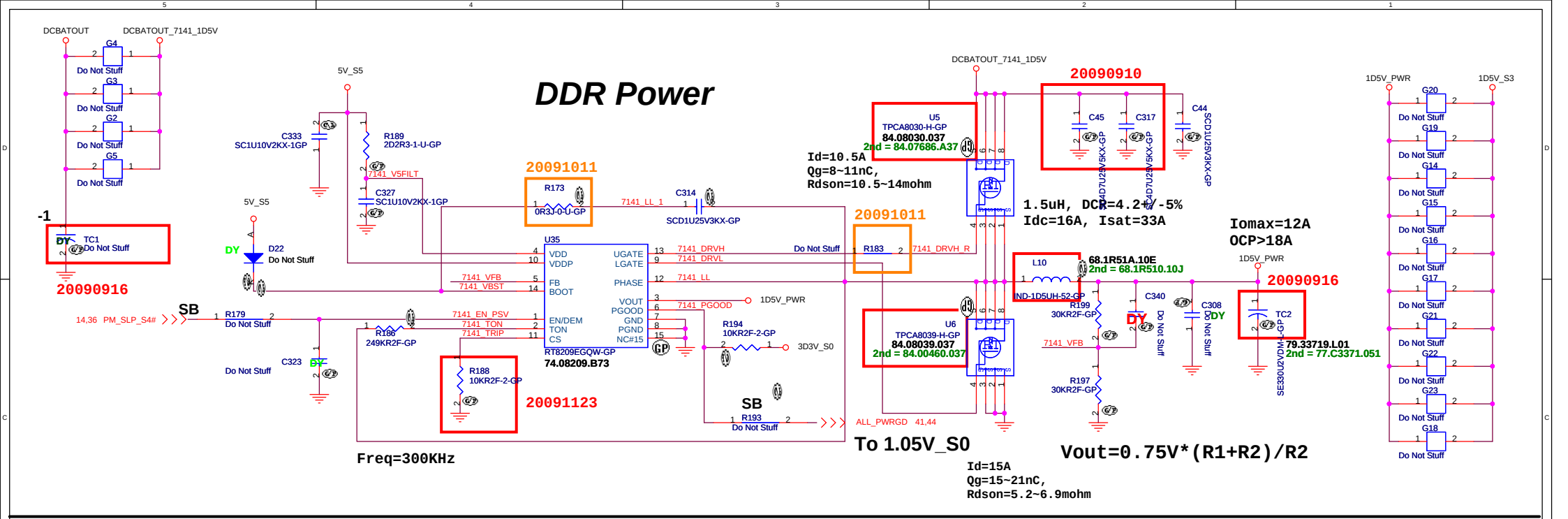
JV10 CS

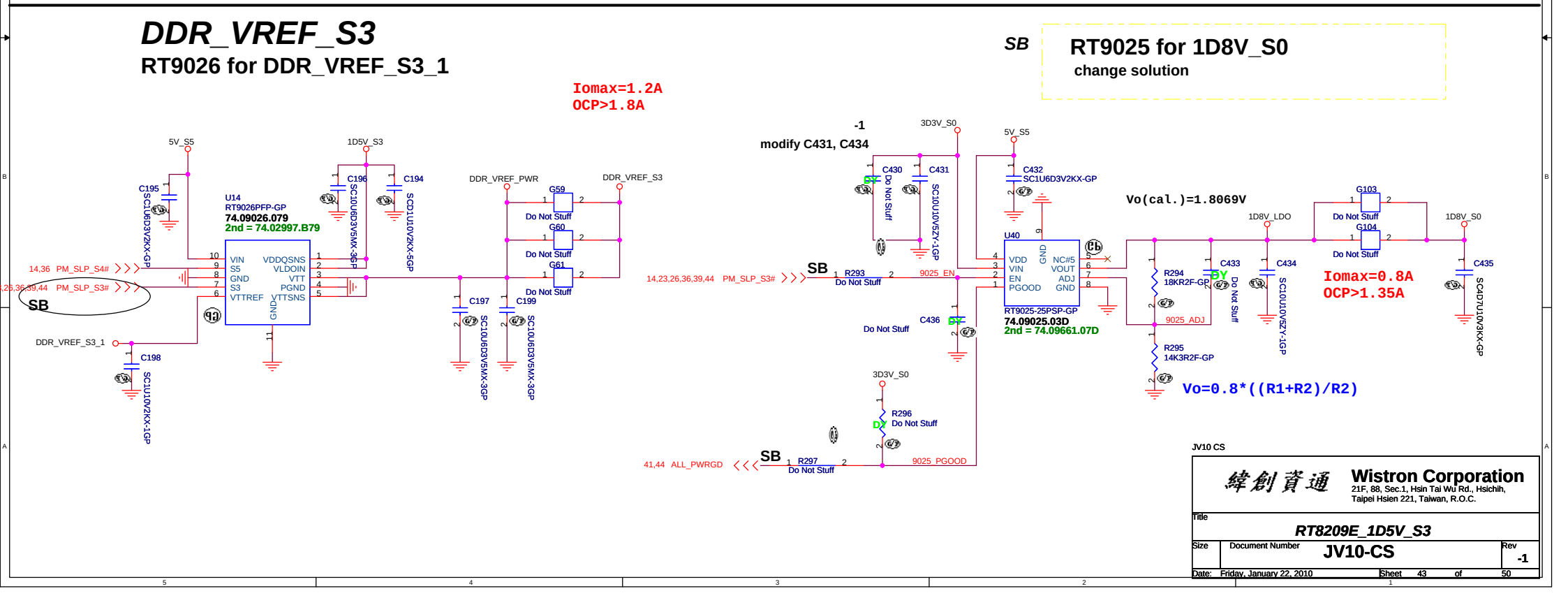
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Power Block Diagram**		
Size	Document Number: **JV10-CS**	Rev: -1
Date: Friday, January 22, 2010	Sheet 40 of 50	


CPU VCC_CORE
From KBC
To PCH
TPS51611RHBR-GP
U11
74.51611.073
SB
-1
Intel support POC (power on current).
R527 close to L32
Iomax=27A
OCP>45A
20091014
20091011
20090916
20090911
20100113
VCC_CORE
DCBATOUT
DCBATOUT_51611_CPU
51611_CPU_AGND
1D05V_S0
3D3V_S5
5V_S5
3D3V_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51611_CPU CORE
JV10-CS
Rev -1
Date: Friday, January 22, 2010
Sheet 41 of 50



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

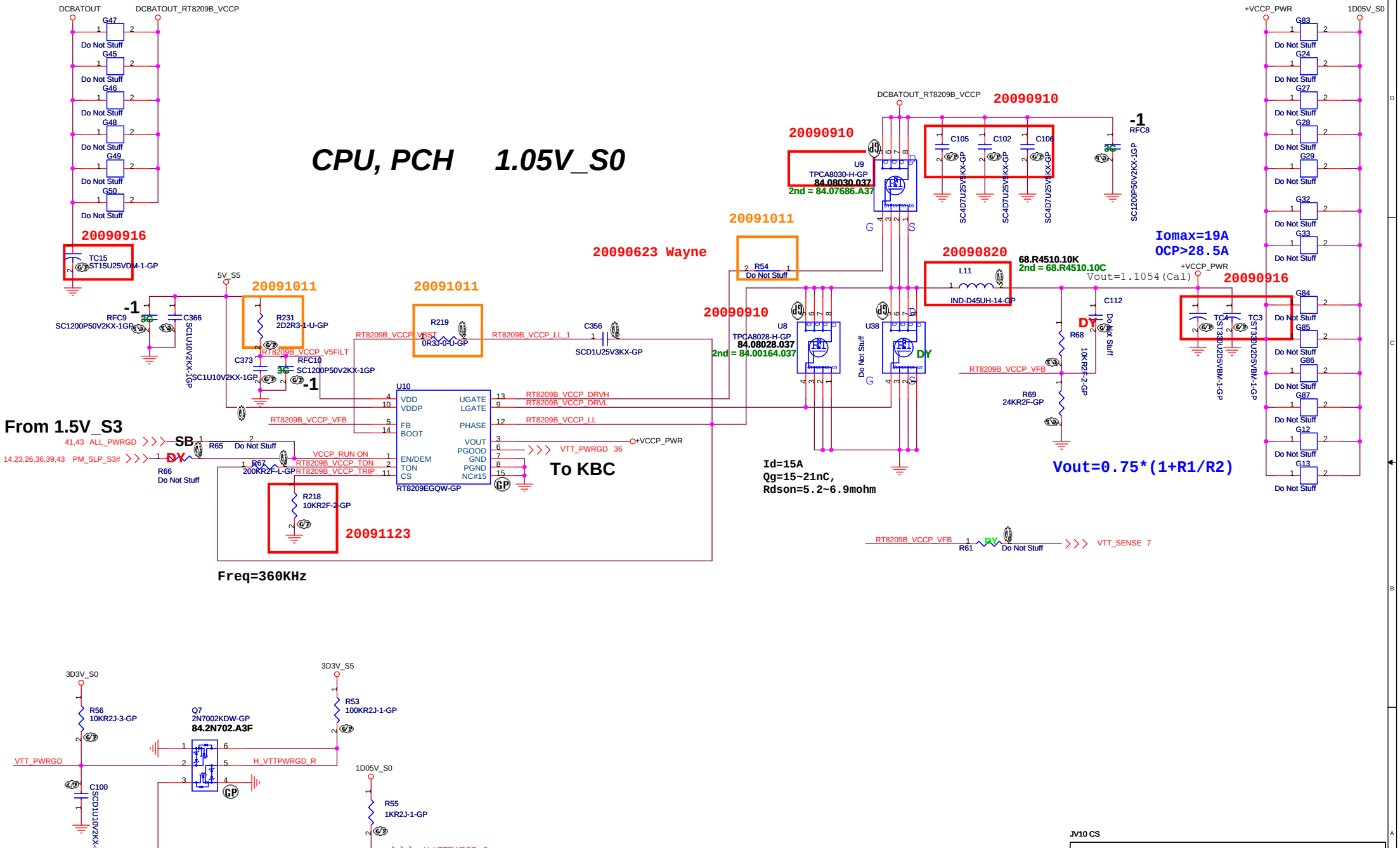




JV10 CS

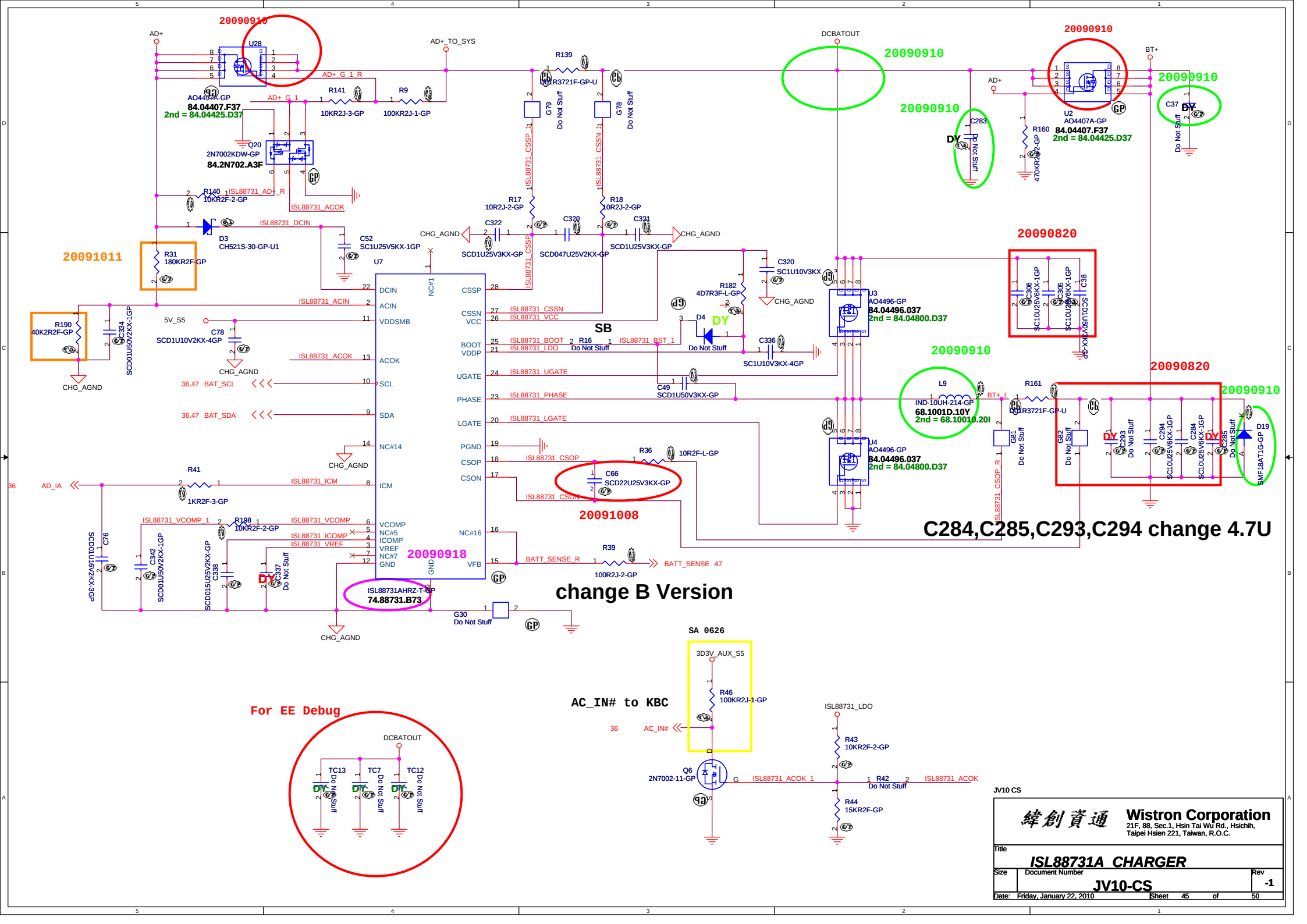
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*RT8209E_1D5V_S3*	
Size	Document Number **JV10-CS**	Rev -1
Date: Friday, January 22, 2010	Sheet 43 of 50	

CPU, PCH 1.05V_S0



JV10 CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209B_1D05V_S0		
Size	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 44 of 50	


20090910
AD+
U28
AO4407A-GP
84.04407.F37
2nd = 84.04425.D37
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R141
10KR2J-3-GP
R9
100KR2J-1-GP
Q20
2N7002KDW-GP
84.2N702.A3F
R140
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
ISL88731_DCIN
D3
CH521S-30-GP-U1
20091011
R31
180KR2F-GP
C52
SC1U25V5KX-1GP
U7
R190
40K2R2F-GP
C334
SCD01U50V2KX-1GP
CHG_AGND
5V_S5
C78
SCD1U10V2KX-4GP
ISL88731_ACIN
ISL88731_ACOK
36,47 BAT_SCL
36,47 BAT_SDA
NC#14
R41
AD_IA
1KR2F-3-GP
ISL88731_ICM
ISL88731_VCOMP_1
R198
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C76
SCD01U16V2KX-3GP
C342
SCD01U50V2KX-1GP
C338
SCD015U25V2KX-GP
C337
DY
Do Not Stuff
20090918
ISL88731AHRZ-T-GP
74.88731.B73
G30
Do Not Stuff
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#16
VFB
R139
0UR3721F-GP-U
G79
G78
ISL88731_CSSP_1
ISL88731_CSSN_1
R17
10R2J-2-GP
R18
10R2J-2-GP
C322
C328
C321
SCD1U25V3KX-GP
SCD047U25V2KX-GP
CHG_AGND
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
R16
Do Not Stuff
ISL88731_BST_1
SB
R182
4D7R3F-L-GP
D4
DY
Do Not Stuff
C336
SC1U10V3KX-4GP
C49
SCD1U50V3KX-GP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
R36
10R2F-L-GP
C66
SCD22U25V3KX-GP
ISL88731_CSON
20091008
R39
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 47
change B Version
For EE Debug
DCBATOUT
TC13
TC7
TC12
Do Not Stuff
SA 0626
3D3V_AUX_S5
R46
100KR2J-1-GP
AC_IN# to KBC
AC_IN#
Q6
2N7002-11-GP
ISL88731_ACOK_1
R42
Do Not Stuff
ISL88731_ACOK
ISL88731_LDO
R43
10KR2F-2-GP
R44
15KR2F-GP
20090820
U3
AO4496-GP
84.04496.037
2nd = 84.04800.D37
U4
AO4496-GP
84.04496.037
2nd = 84.04800.D37
C320
SC1U10V3KX
C306
C305
SCD1U16V3KX-GP
L9
IND-10UH-214-GP
68.1001D.10Y
2nd = 68.10010.20I
BT+_L
R161
0UR3721F-GP-U
G81
G82
C294
C293
C284
C285
SC10U25V6KX-1GP
D19
SMF18AT1G-GP
C283
R160
470KR2J-2-GP
U2
AO4407A-GP
84.04407.F37
2nd = 84.04425.D37
C37
BT+
C284,C285,C293,C294 change 4.7U
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
Size
Document Number
JV10-CS
Rev
-1
Date: Friday, January 22, 2010
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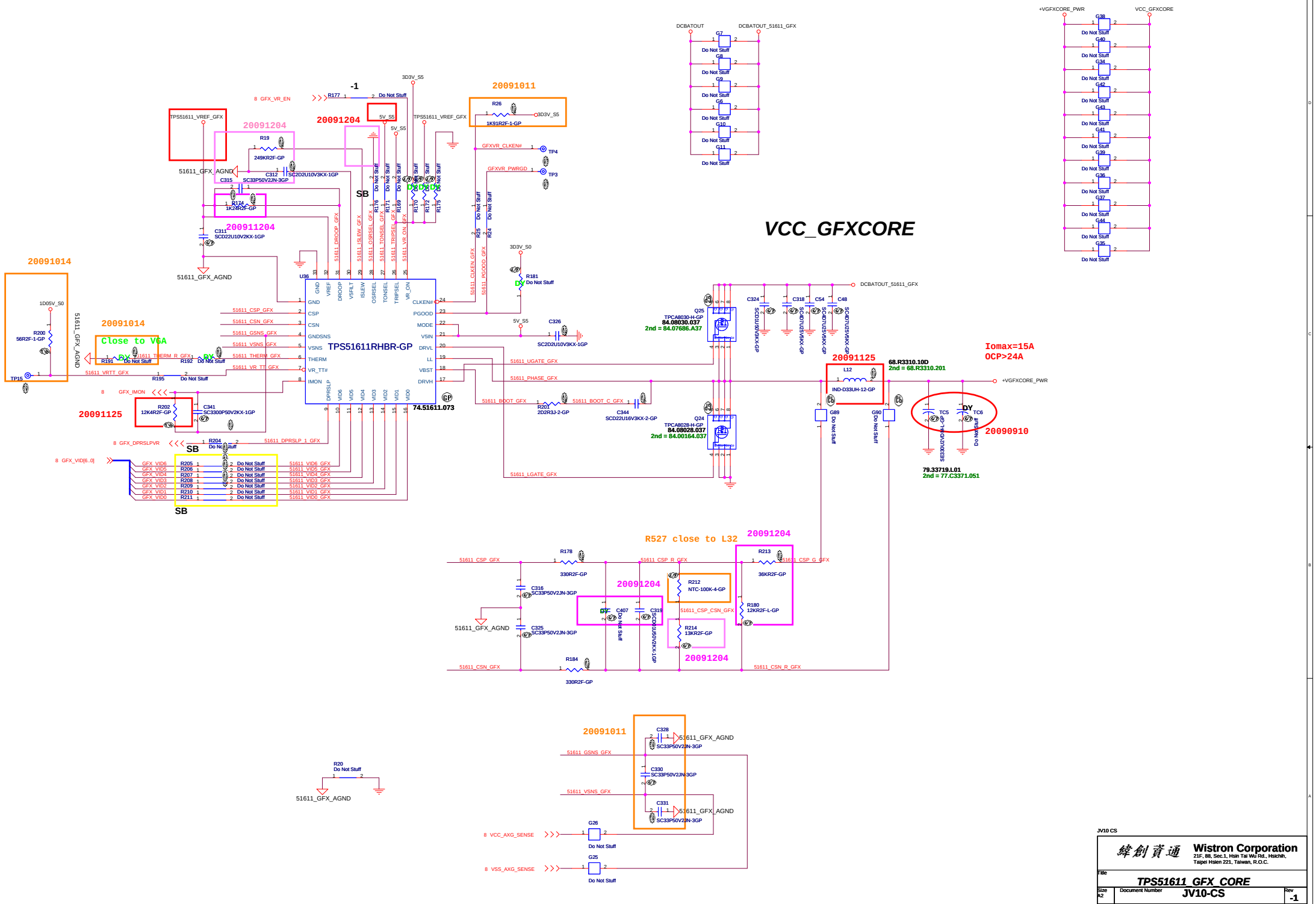
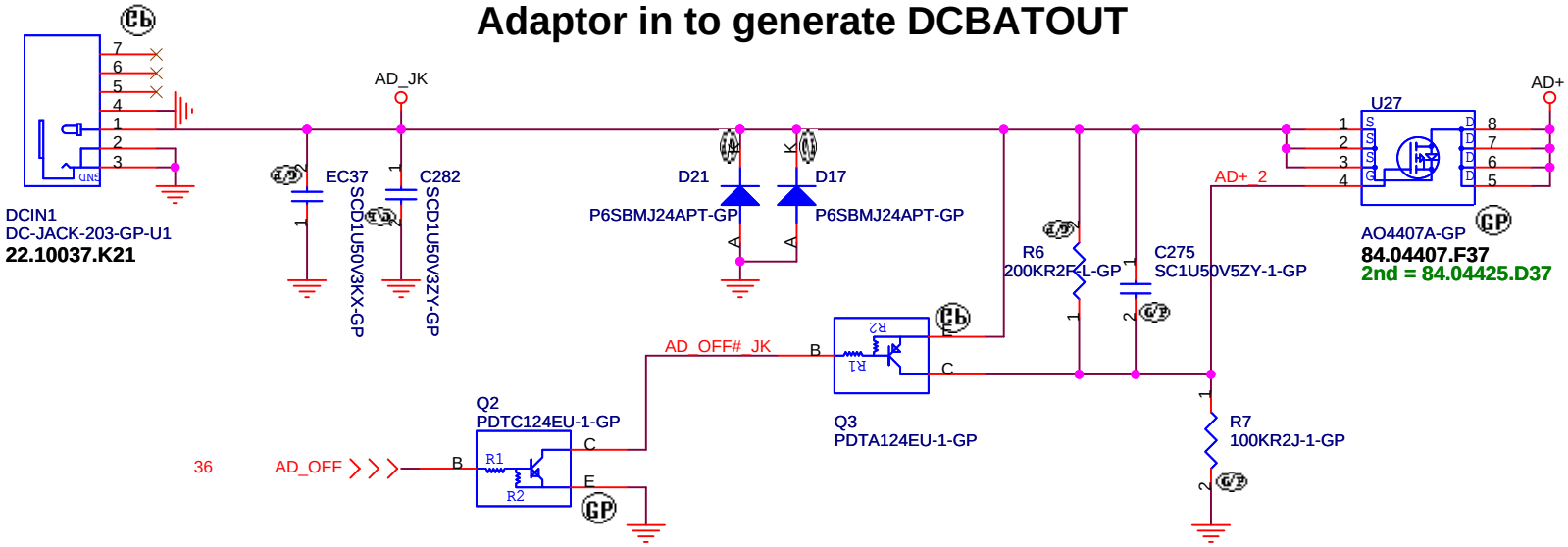
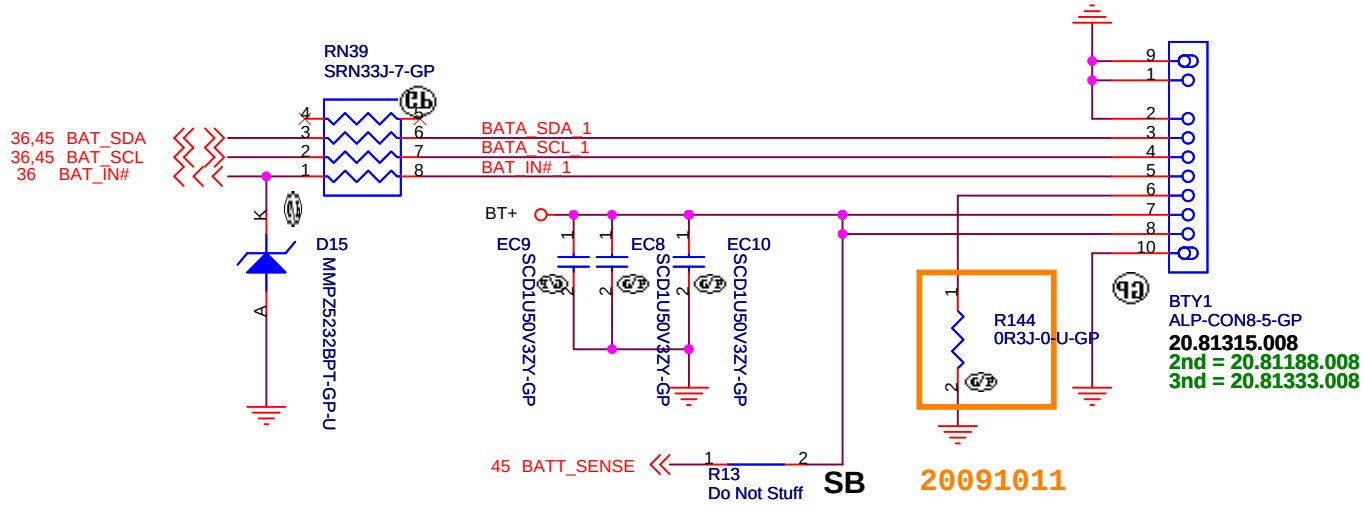

VCC_GFXCORE
TPS51611RHBR-GP
74.51611.073
Close to VGA
Iomax=15A
OCP>24A
R527 close to L32
20091011
20091204
20091014
20091125
20090910
SB
Do Not Stuff
51611_GFX_AGND
+VGFXCORE_PWR
VCC_GFXCORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51611_GFX_CORE
JV10-CS
Friday, January 22, 2010

Adaptor in to generate DCBATOUT



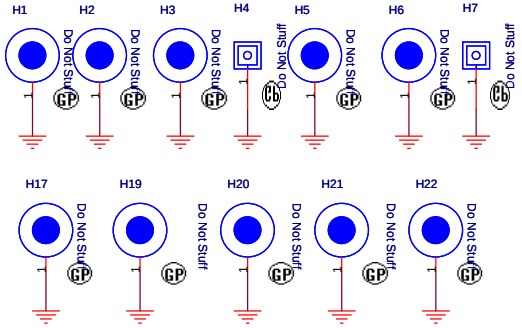
BATTERY CONNECTOR



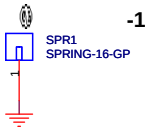
JV10 CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD/BATT CONN		
Size	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 47 of 50	

MB HOLE

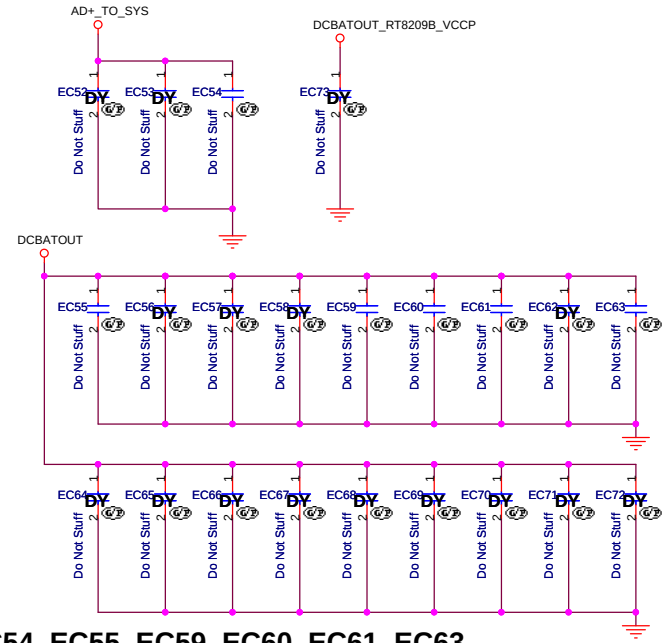


SPRING



SB

EMI

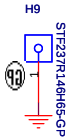


EC54, EC55, EC59, EC60, EC61, EC63

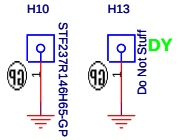
MINI CARD BOSS

(BTN Side)

HALF MINI CARD

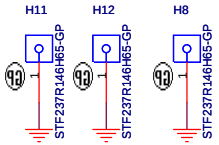


FULL MINI CARD

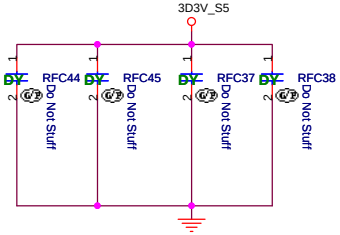


CPU PCH BOSS

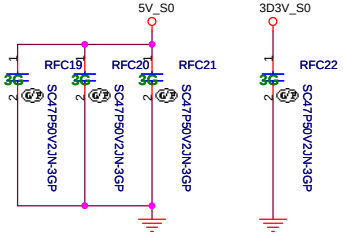
(BTN Side)



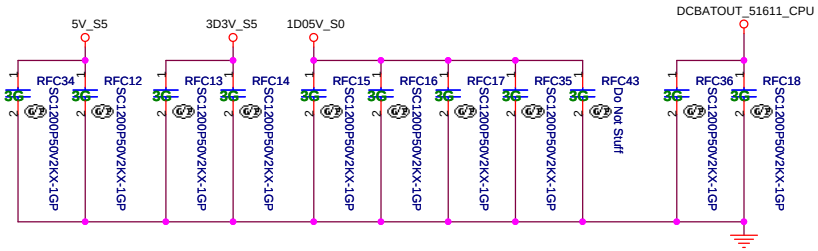
For RF power point Page 26



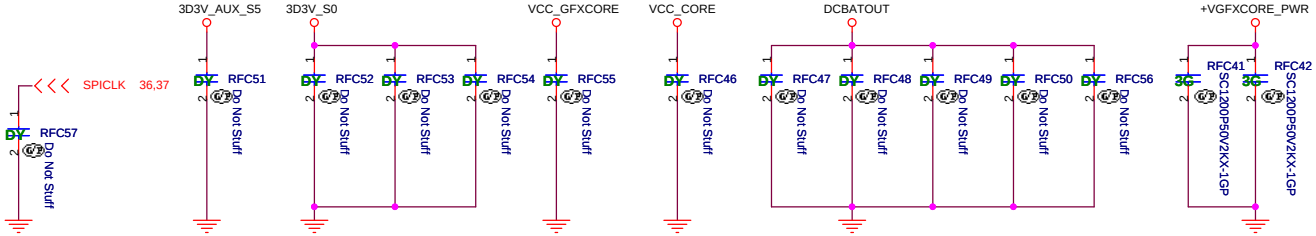
For RF power point Page 12



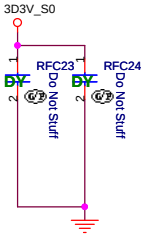
For RF power point Page 4

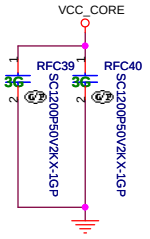


For RF power point Page 17



For RF power point Page 13

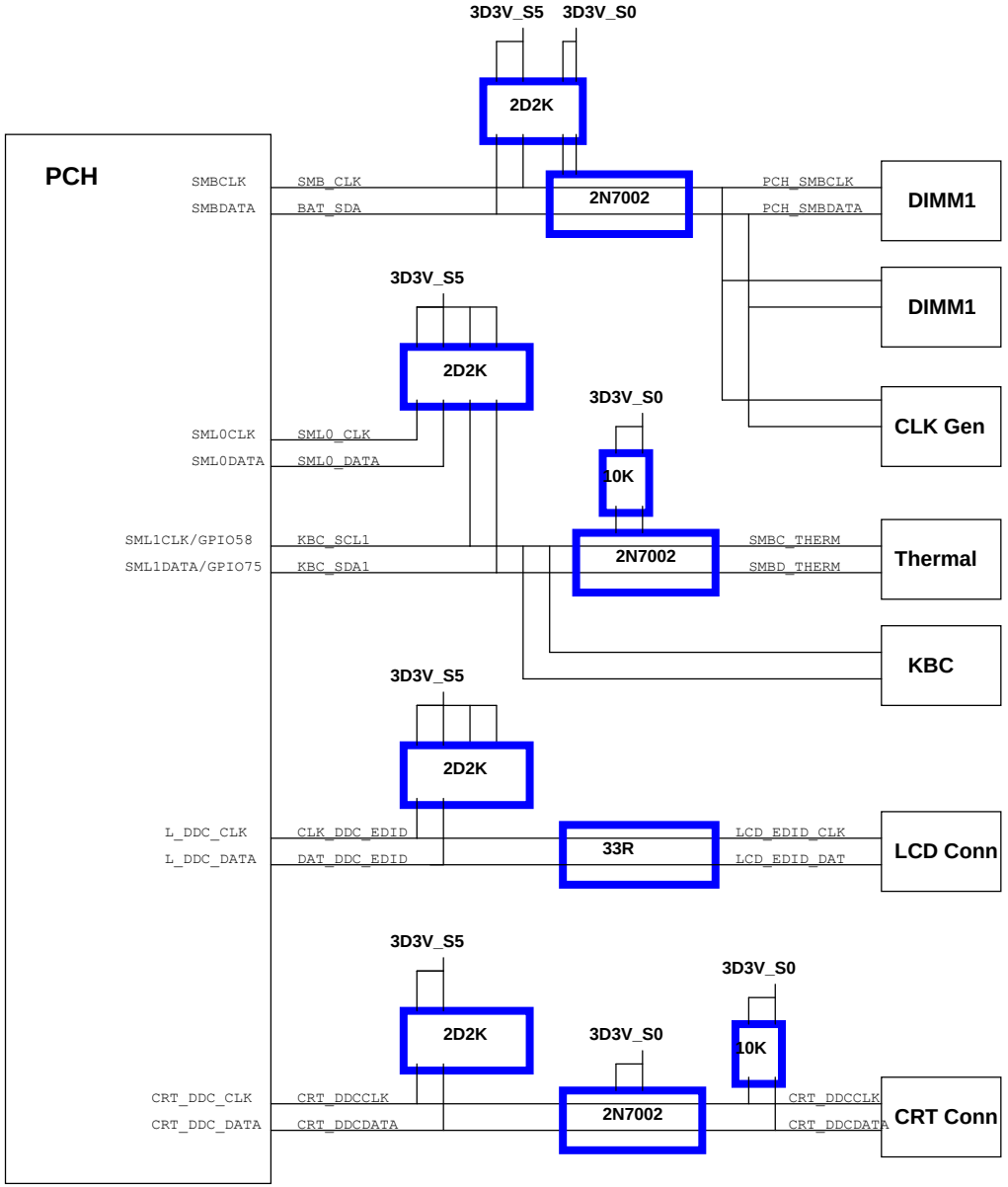




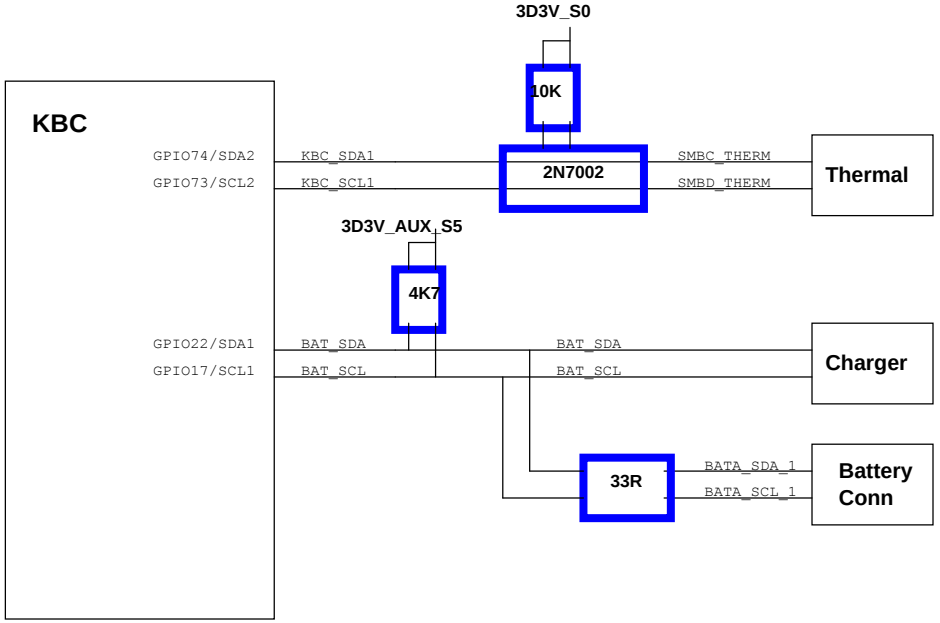
JV10 CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: EMI/Spring/Boss		
Size	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 48 of 50	

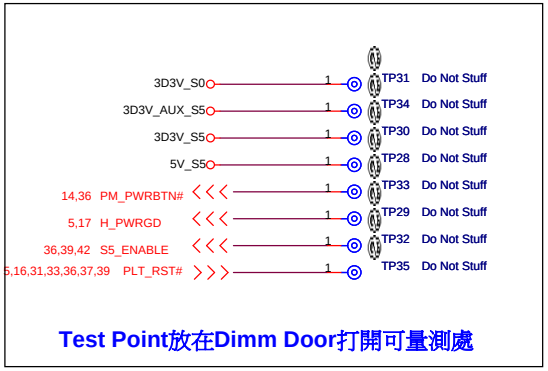
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Check test point



Test Point放在Dimm Door打開可量測處

JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AFTE_TP/SMB Diagram***	
Size	Document Number: **JV10-CS**	Rev: **-1**
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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

EC SB11/04 add Intel support POC Function(power on current).
EC SB11/04 SWAP Touch Pad Pin define
EC SB11/04 R230 add 1K
EC SB11/04 change LOUT1 part number
EC SB11/11 SWAP Digital Mic DATA/CLK Pin define
EC SB11/11 Delete 3G_BTN#,Wireless_BTN#, function
EC SB11/11 add Cover switch to MB
EC SB11/11 add RN72 22ohm for Mic in
EC SB11/16 change U40 1D8V_S0 power solution
EC SB11/19 modify all LED off Function
EC SB11/19 change HDD Connector Type
EC SB11/19 Close Powert team Gap
EC PD 01/11 modify keyborad connector KB1
EC PD 01/11 modify USB Touch pad connector TPCN1 USBCN1
EC PD 01/11 add 3G module LED Function
EC PD 01/11 EMI add EC54, EC55, EC59, EC60, EC61, EC63, C37
EC PD 01/11 TPCN1 SWAP Pin define

JV10 CS

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Title: **Modify History**

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