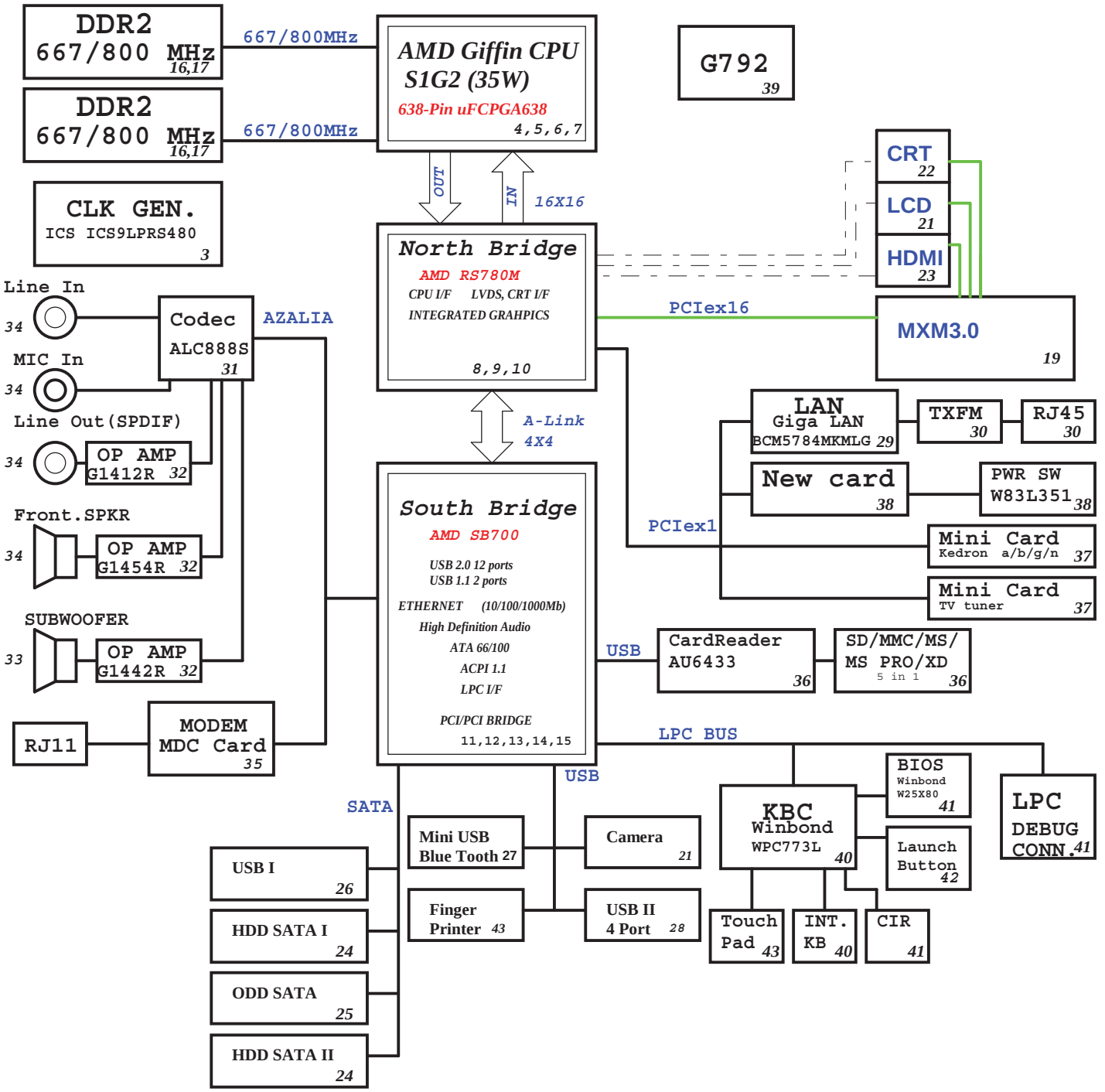
JM70-PU (AS 17") Block Diagram

Project code: 91.4CE01.001
PCB P/N : 48.4CE01.0SC
REVISION : 08255-SC



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 49

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 50

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 52

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 51

1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)

RT9166 51

3D3V_S0	2D5V_S0 (300mA)

G957 51

3D3V_S0	1D5V_S0(1A)

G9161(UMA) 51

3D3V_S5	1D2V_S5 (400mA)

G9131(DIS) 51

3D3V_S5	1D2V_S5 (300mA)

CHARGER MAX8731A 53

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 48

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JM70-PU | Rev: -2
Date: Monday, March 02, 2009 | Sheet 1 of 56

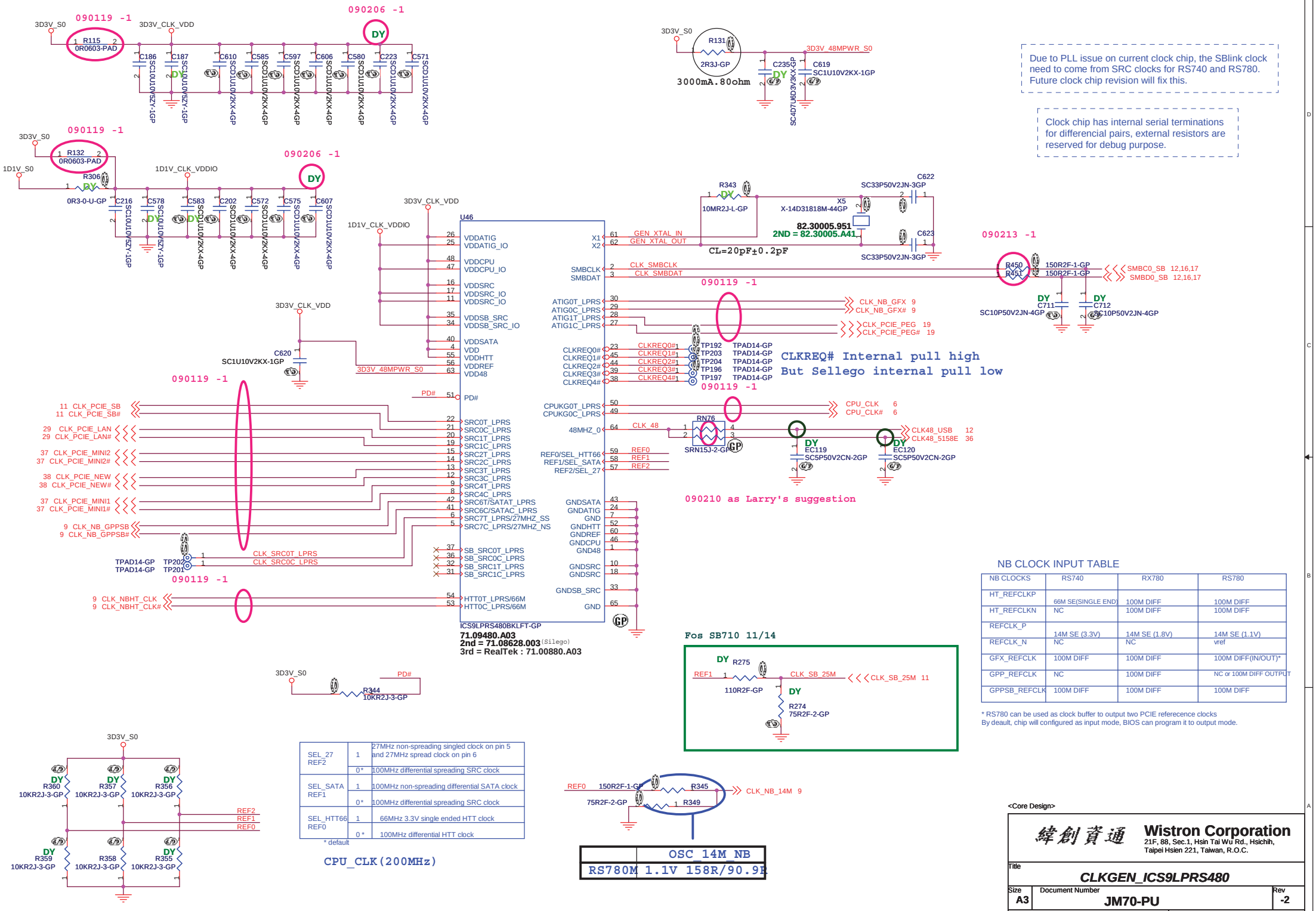
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Monday, March 02, 2009 Sheet 2 of 56



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

<Core Design>

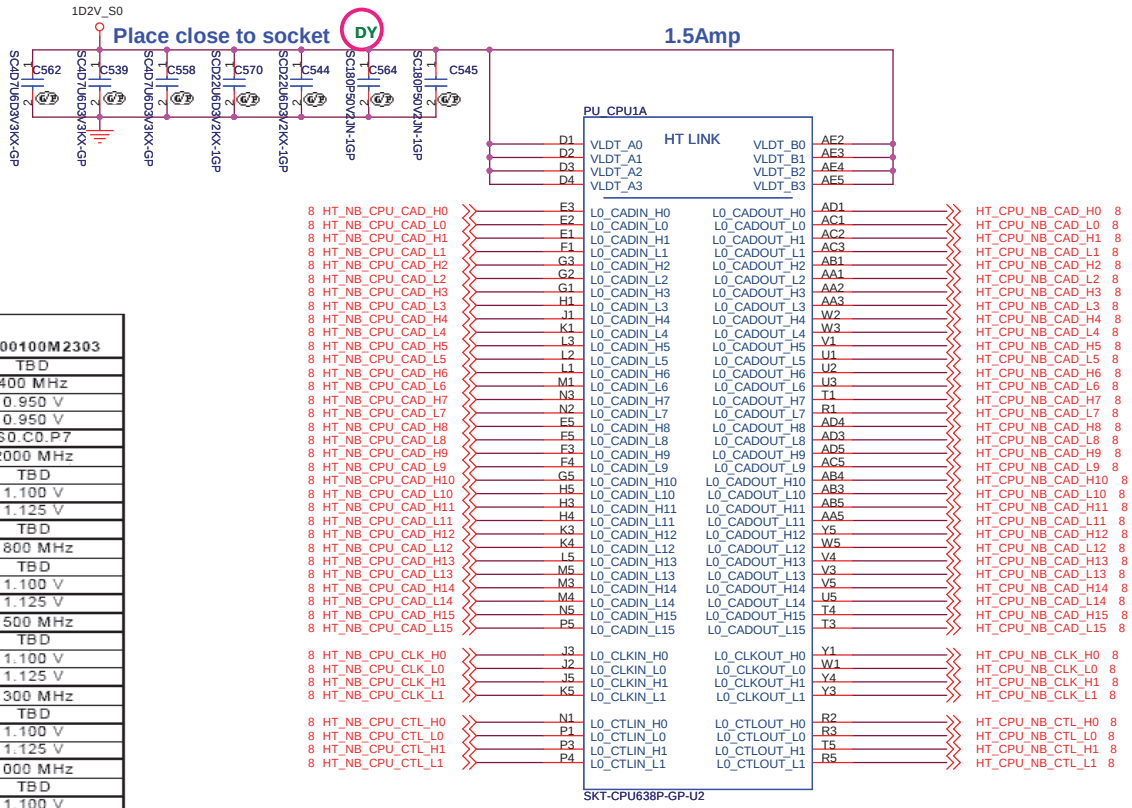
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 3 of 56

090206 -1



62.10055.111
2ND = 62.10055.251

090109 SC

SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 4 of 56

090206 -1

Place near to CPU

4.7u x 4 | 0.22u X 2 | 180P x 6

DY

C215 SC4D7U6D3V3KX-GP
C600 SC4D7U6D3V3KX-GP
C203 SC4D7U6D3V3KX-GP
C204 SC4D7U6D3V3KX-GP
C212 SCD22U6D3V2KX-1GP
C208 SCD22U6D3V2KX-1GP
C210 SC180P50V2JN-1GP
C211 SC180P50V2JN-1GP
C206 SC180P50V2JN-1GP
C213 SC180P50V2JN-1GP
C209 SC180P50V2JN-1GP
C207 SC180P50V2JN-1GP

0D9V_S3

CLOSE TO CPU

1D8V_S3

C250 SCD1U10V2KX-4GP
VREF_DDR_CLAW
RN20 SRN1KJ-7-GP
C246 SC1KP50V2KX-1GP
C240 SCD1U10V2KX-4GP

R376 39D2R2F-L-GP
R379 39D2R2F-L-GPTP137

MEMZP
MEMZN
MEM_RSVD_M1
VTT_SENSE → TP132TPAD14-GP
MEM_RSVD_M2 → TP138

PU_CPU1B

MEM:CMD/CTRL/CLK

MA0_ODT0	MB0_ODT0	MEM_MB0_ODT0	17,18
MA0_ODT1	MB0_ODT1	MEM_MB0_ODT1	17,18
MA0_CS_L0	MB0_CS_L0	MEM_MB0_CS#0	17,18
MA0_CS_L1	MB0_CS_L1	MEM_MB0_CS#1	17,18
MA_CKE0	MB_CKE0	MEM_MB_CKE0	17,18
MA_CKE1	MB_CKE1	MEM_MB_CKE1	17,18
MA_CLK_H0	MB_CLK_H0	MEM_MB_CLK0_P	17
MA_CLK_H1	MB_CLK_H1	MEM_MB_CLK0_N	17
MA_CLK_H7	MB_CLK_H7	MEM_MB_CLK1_P	17
MA_CLK_L7	MB_CLK_L7	MEM_MB_CLK1_N	17
MA_ADD0	MB_ADD0	MEM_MB_ADD0	17,18
MA_ADD1	MB_ADD1	MEM_MB_ADD1	17,18
MA_ADD2	MB_ADD2	MEM_MB_ADD2	17,18
MA_ADD3	MB_ADD3	MEM_MB_ADD3	17,18
MA_ADD4	MB_ADD4	MEM_MB_ADD4	17,18
MA_ADD5	MB_ADD5	MEM_MB_ADD5	17,18
MA_ADD6	MB_ADD6	MEM_MB_ADD6	17,18
MA_ADD7	MB_ADD7	MEM_MB_ADD7	17,18
MA_ADD8	MB_ADD8	MEM_MB_ADD8	17,18
MA_ADD9	MB_ADD9	MEM_MB_ADD9	17,18
MA_ADD10	MB_ADD10	MEM_MB_ADD10	17,18
MA_ADD11	MB_ADD11	MEM_MB_ADD11	17,18
MA_ADD12	MB_ADD12	MEM_MB_ADD12	17,18
MA_ADD13	MB_ADD13	MEM_MB_ADD13	17,18
MA_ADD14	MB_ADD14	MEM_MB_ADD14	17,18
MA_ADD15	MB_ADD15	MEM_MB_ADD15	17,18
MA_BANK0	MB_BANK0	MEM_MB_BANK0	17,18
MA_BANK1	MB_BANK1	MEM_MB_BANK1	17,18
MA_BANK2	MB_BANK2	MEM_MB_BANK2	17,18
MA_RAS_L	MB_RAS_L	MEM_MB_RAS#	17,18
MA_CAS_L	MB_CAS_L	MEM_MB_CAS#	17,18
MA_WE_L	MB_WE_L	MEM_MB_WE#	17,18

SKT-CPU638P-GP-U2

62.10055.111
2ND = 62.10055.251
090109 SC

PU_CPU1C

MEM:DATA

MA_DATA0	MB_DATA0	MEM_MB_DATA0	17
MA_DATA1	MB_DATA1	MEM_MB_DATA1	17
MA_DATA2	MB_DATA2	MEM_MB_DATA2	17
MA_DATA3	MB_DATA3	MEM_MB_DATA3	17
MA_DATA4	MB_DATA4	MEM_MB_DATA4	17
MA_DATA5	MB_DATA5	MEM_MB_DATA5	17
MA_DATA6	MB_DATA6	MEM_MB_DATA6	17
MA_DATA7	MB_DATA7	MEM_MB_DATA7	17
MA_DATA8	MB_DATA8	MEM_MB_DATA8	17
MA_DATA9	MB_DATA9	MEM_MB_DATA9	17
MA_DATA10	MB_DATA10	MEM_MB_DATA10	17
MA_DATA11	MB_DATA11	MEM_MB_DATA11	17
MA_DATA12	MB_DATA12	MEM_MB_DATA12	17
MA_DATA13	MB_DATA13	MEM_MB_DATA13	17
MA_DATA14	MB_DATA14	MEM_MB_DATA14	17
MA_DATA15	MB_DATA15	MEM_MB_DATA15	17
MA_DATA16	MB_DATA16	MEM_MB_DATA16	17
MA_DATA17	MB_DATA17	MEM_MB_DATA17	17
MA_DATA18	MB_DATA18	MEM_MB_DATA18	17
MA_DATA19	MB_DATA19	MEM_MB_DATA19	17
MA_DATA20	MB_DATA20	MEM_MB_DATA20	17
MA_DATA21	MB_DATA21	MEM_MB_DATA21	17
MA_DATA22	MB_DATA22	MEM_MB_DATA22	17
MA_DATA23	MB_DATA23	MEM_MB_DATA23	17
MA_DATA24	MB_DATA24	MEM_MB_DATA24	17
MA_DATA25	MB_DATA25	MEM_MB_DATA25	17
MA_DATA26	MB_DATA26	MEM_MB_DATA26	17
MA_DATA27	MB_DATA27	MEM_MB_DATA27	17
MA_DATA28	MB_DATA28	MEM_MB_DATA28	17
MA_DATA29	MB_DATA29	MEM_MB_DATA29	17
MA_DATA30	MB_DATA30	MEM_MB_DATA30	17
MA_DATA31	MB_DATA31	MEM_MB_DATA31	17
MA_DATA32	MB_DATA32	MEM_MB_DATA32	17
MA_DATA33	MB_DATA33	MEM_MB_DATA33	17
MA_DATA34	MB_DATA34	MEM_MB_DATA34	17
MA_DATA35	MB_DATA35	MEM_MB_DATA35	17
MA_DATA36	MB_DATA36	MEM_MB_DATA36	17
MA_DATA37	MB_DATA37	MEM_MB_DATA37	17
MA_DATA38	MB_DATA38	MEM_MB_DATA38	17
MA_DATA39	MB_DATA39	MEM_MB_DATA39	17
MA_DATA40	MB_DATA40	MEM_MB_DATA40	17
MA_DATA41	MB_DATA41	MEM_MB_DATA41	17
MA_DATA42	MB_DATA42	MEM_MB_DATA42	17
MA_DATA43	MB_DATA43	MEM_MB_DATA43	17
MA_DATA44	MB_DATA44	MEM_MB_DATA44	17
MA_DATA45	MB_DATA45	MEM_MB_DATA45	17
MA_DATA46	MB_DATA46	MEM_MB_DATA46	17
MA_DATA47	MB_DATA47	MEM_MB_DATA47	17
MA_DATA48	MB_DATA48	MEM_MB_DATA48	17
MA_DATA49	MB_DATA49	MEM_MB_DATA49	17
MA_DATA50	MB_DATA50	MEM_MB_DATA50	17
MA_DATA51	MB_DATA51	MEM_MB_DATA51	17
MA_DATA52	MB_DATA52	MEM_MB_DATA52	17
MA_DATA53	MB_DATA53	MEM_MB_DATA53	17
MA_DATA54	MB_DATA54	MEM_MB_DATA54	17
MA_DATA55	MB_DATA55	MEM_MB_DATA55	17
MA_DATA56	MB_DATA56	MEM_MB_DATA56	17
MA_DATA57	MB_DATA57	MEM_MB_DATA57	17
MA_DATA58	MB_DATA58	MEM_MB_DATA58	17
MA_DATA59	MB_DATA59	MEM_MB_DATA59	17
MA_DATA60	MB_DATA60	MEM_MB_DATA60	17
MA_DATA61	MB_DATA61	MEM_MB_DATA61	17
MA_DATA62	MB_DATA62	MEM_MB_DATA62	17
MA_DATA63	MB_DATA63	MEM_MB_DATA63	17
MA_DM0	MB_DM0	MEM_MB_DM0	17
MA_DM1	MB_DM1	MEM_MB_DM1	17
MA_DM2	MB_DM2	MEM_MB_DM2	17
MA_DM3	MB_DM3	MEM_MB_DM3	17
MA_DM4	MB_DM4	MEM_MB_DM4	17
MA_DM5	MB_DM5	MEM_MB_DM5	17
MA_DM6	MB_DM6	MEM_MB_DM6	17
MA_DM7	MB_DM7	MEM_MB_DM7	17
MA_DQS_H0	MB_DQS_H0	MEM_MB_DQS0_P	17
MA_DQS_L0	MB_DQS_L0	MEM_MB_DQS0_N	17
MA_DQS_H1	MB_DQS_H1	MEM_MB_DQS1_P	17
MA_DQS_L1	MB_DQS_L1	MEM_MB_DQS1_N	17
MA_DQS_H2	MB_DQS_H2	MEM_MB_DQS2_P	17
MA_DQS_L2	MB_DQS_L2	MEM_MB_DQS2_N	17
MA_DQS_H3	MB_DQS_H3	MEM_MB_DQS3_P	17
MA_DQS_L3	MB_DQS_L3	MEM_MB_DQS3_N	17
MA_DQS_H4	MB_DQS_H4	MEM_MB_DQS4_P	17
MA_DQS_L4	MB_DQS_L4	MEM_MB_DQS4_N	17
MA_DQS_H5	MB_DQS_H5	MEM_MB_DQS5_P	17
MA_DQS_L5	MB_DQS_L5	MEM_MB_DQS5_N	17
MA_DQS_H6	MB_DQS_H6	MEM_MB_DQS6_P	17
MA_DQS_L6	MB_DQS_L6	MEM_MB_DQS6_N	17
MA_DQS_H7	MB_DQS_H7	MEM_MB_DQS7_P	17
MA_DQS_L7	MB_DQS_L7	MEM_MB_DQS7_N	17

SKT-CPU638P-GP-U2

62.10055.111
2ND = 62.10055.251
<Core Design>
090109 SC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 5 of 56

LYAOUT:ROUTE VDDA TRACE APPROX.
40 mils WIDE
(USE 2X25 mil TRACES TO EXIT BALL FIELD)
& 500 mils LONG.

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

SB with 0402 PAD

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

081223 SC

CPU exceeds to 125℃

090119 -1

090206 -1

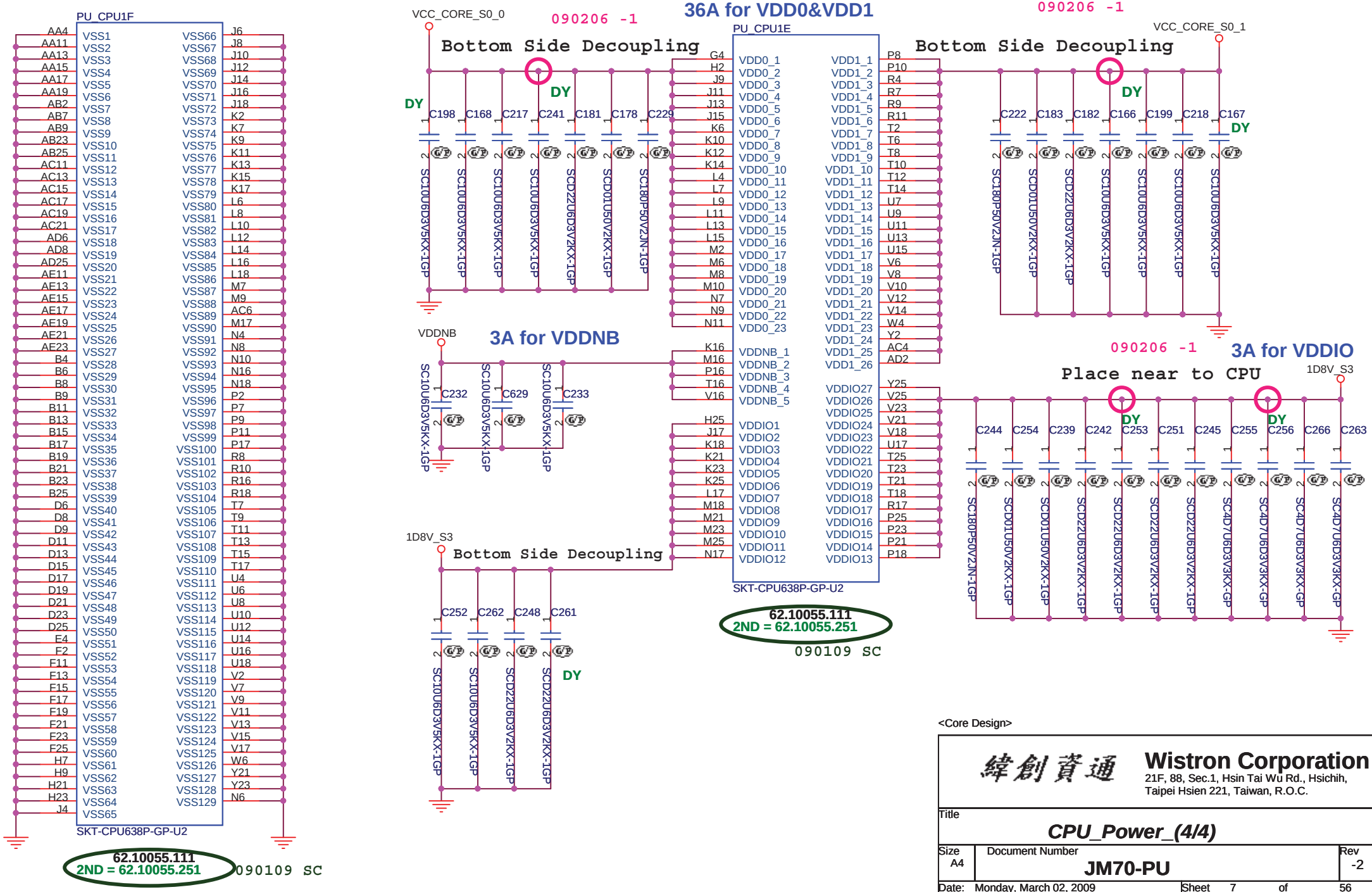
090113 -1

090109 SC

HDT Connectors

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***CPU_Control&Debug_(3/4)***		
Size: A3	Document Number: **JM70-PU**	Rev: -2
Date: Friday, March 06, 2009	Sheet 6 of 56	


PU_CPU1F
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251
090109 SC
VCC_CORE_S0_0
090206 -1
Bottom Side Decoupling
DY
C198 C168 C217 C241 C181 C178 C229
SC10U6D3V5KX-1GP
SCD22U6D3V2KX-1GP
SCD01U50V2KX-1GP
SC180P50V2JN-1GP
36A for VDD0&VDD1
PU_CPU1E
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251
090109 SC
VCC_CORE_S0_1
090206 -1
Bottom Side Decoupling
C222 C183 C182 C166 C199 C218 C167
VDDNB
3A for VDDNB
C232 C629 C233
1D8V_S3
Bottom Side Decoupling
C252 C262 C248 C261
090206 -1
3A for VDDIO
Place near to CPU
C244 C254 C239 C242 C253 C251 C245 C255 C256 C266 C263
SC4D7U6D3V3KX-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_Power_(4/4)
Size A4
Document Number
JM70-PU
Rev -2
Date: Monday, March 02, 2009
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PU_NB1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U2

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

PU_NB1B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780M-GP-U2

Place < 100mils from pin AC8 and AB8

PCIE As SW request 11/17
Port 1 => Onboard LAN
Port 2 => Mini Card WLAN
Port 3 => Mini Card#2
Port 4 => New Card
Port 5,6 => NC

090119 -1

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

LAN
MINICARD
MINICARD TV
NEW CARD

A-LINK

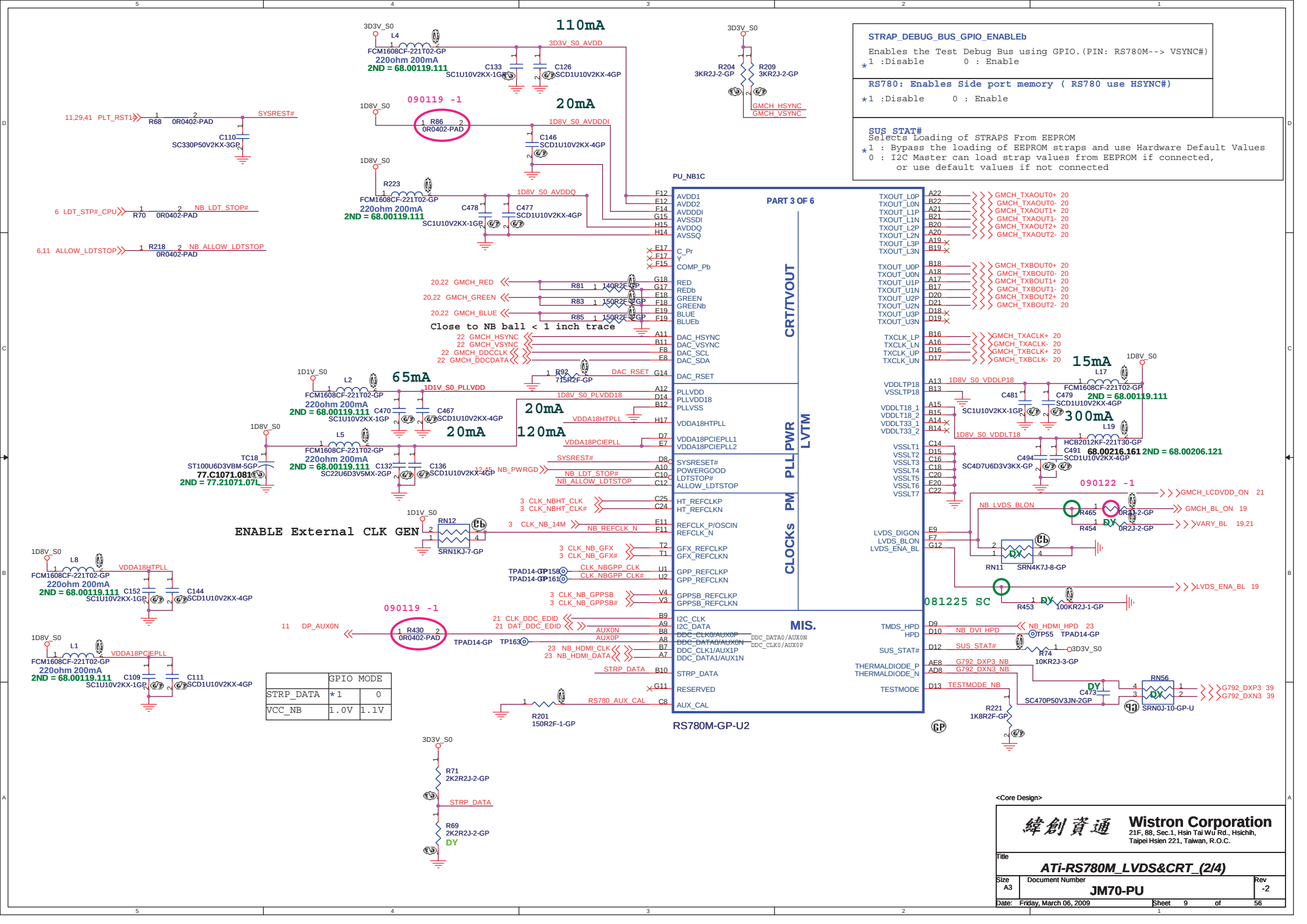
<Core Design>

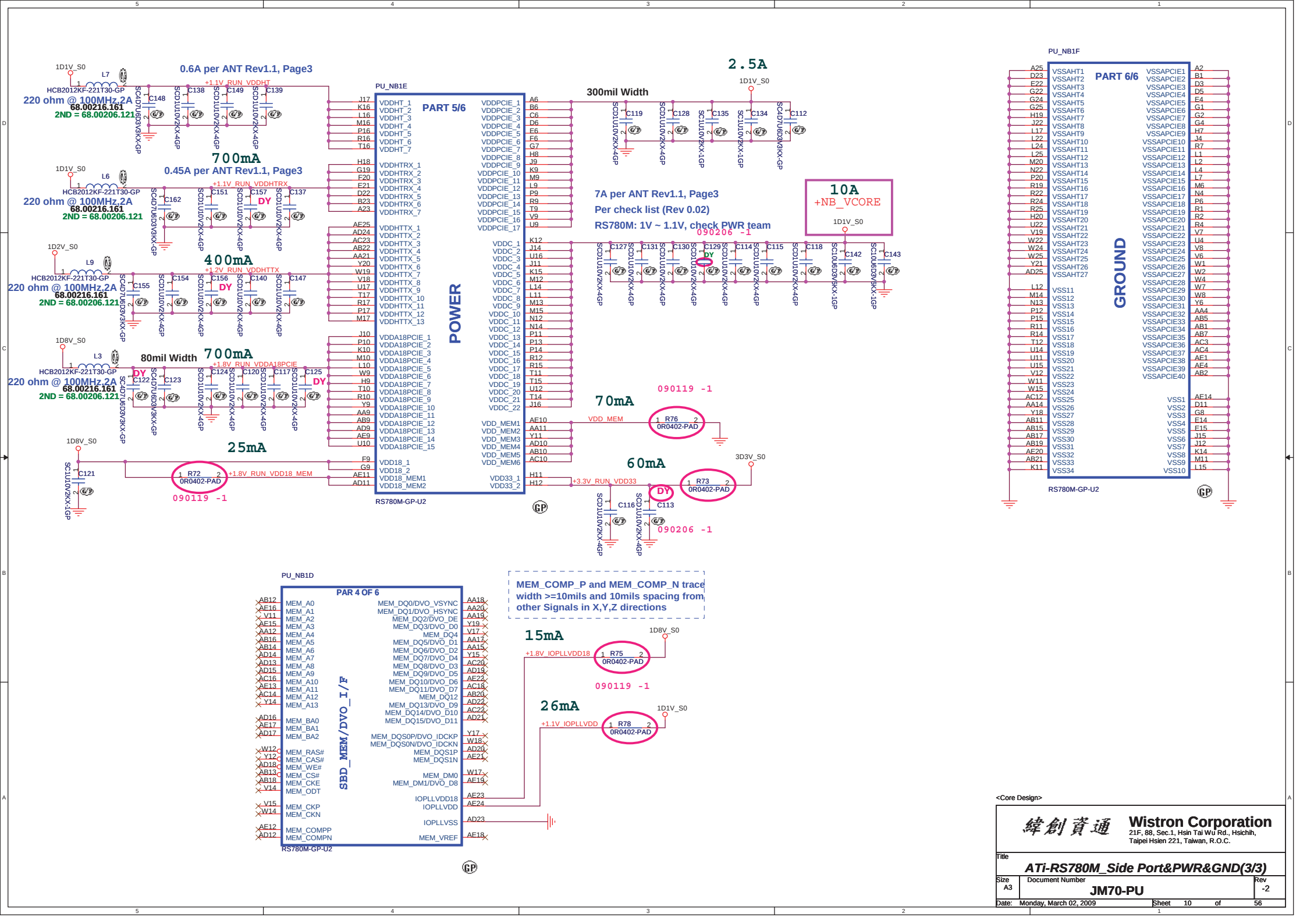
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_HT LINK&PCIe(1/3)

Size: A3 | Document Number: JM70-PU | Rev: -2

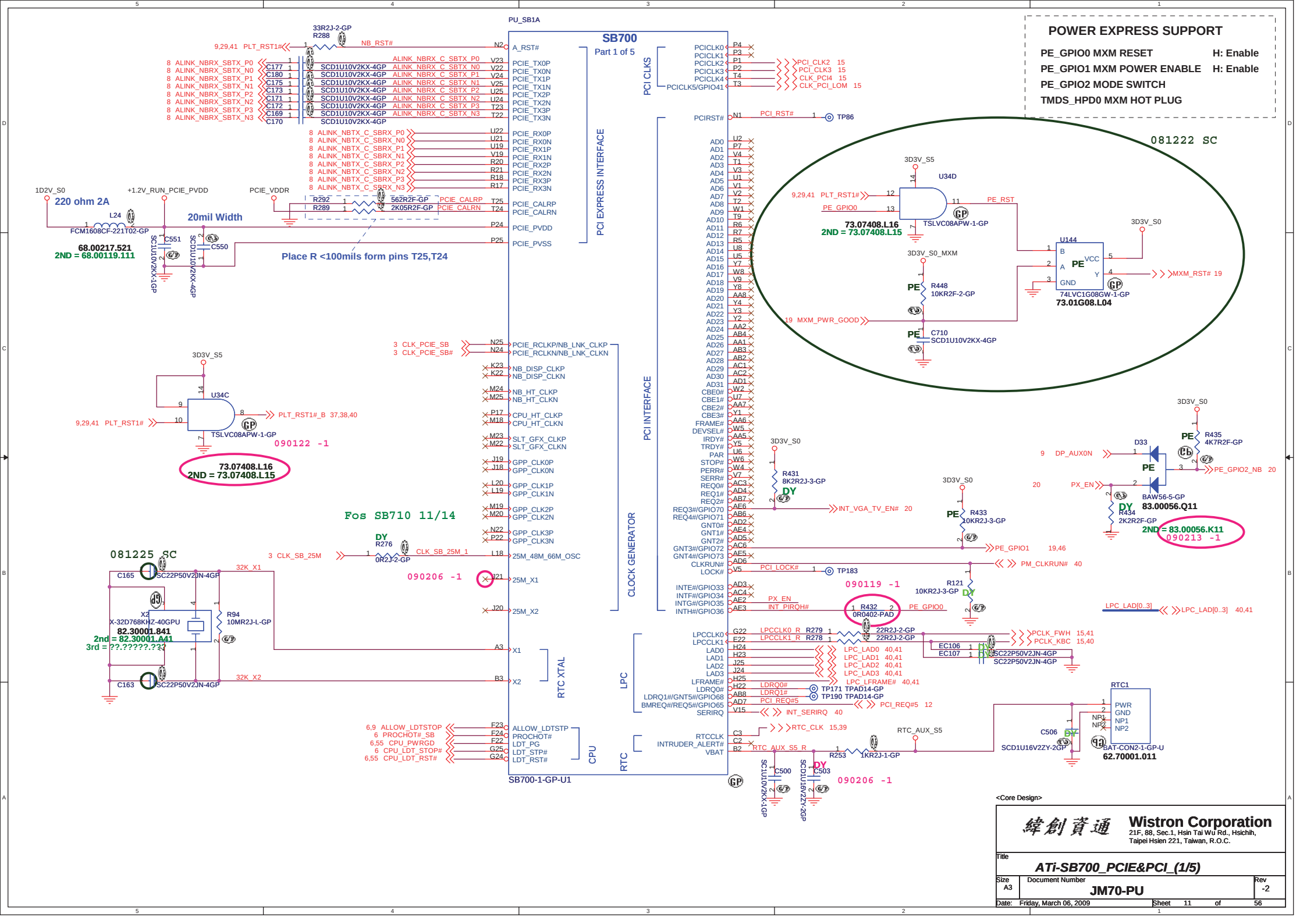
Date: Friday, March 06, 2009 | Sheet 8 of 56

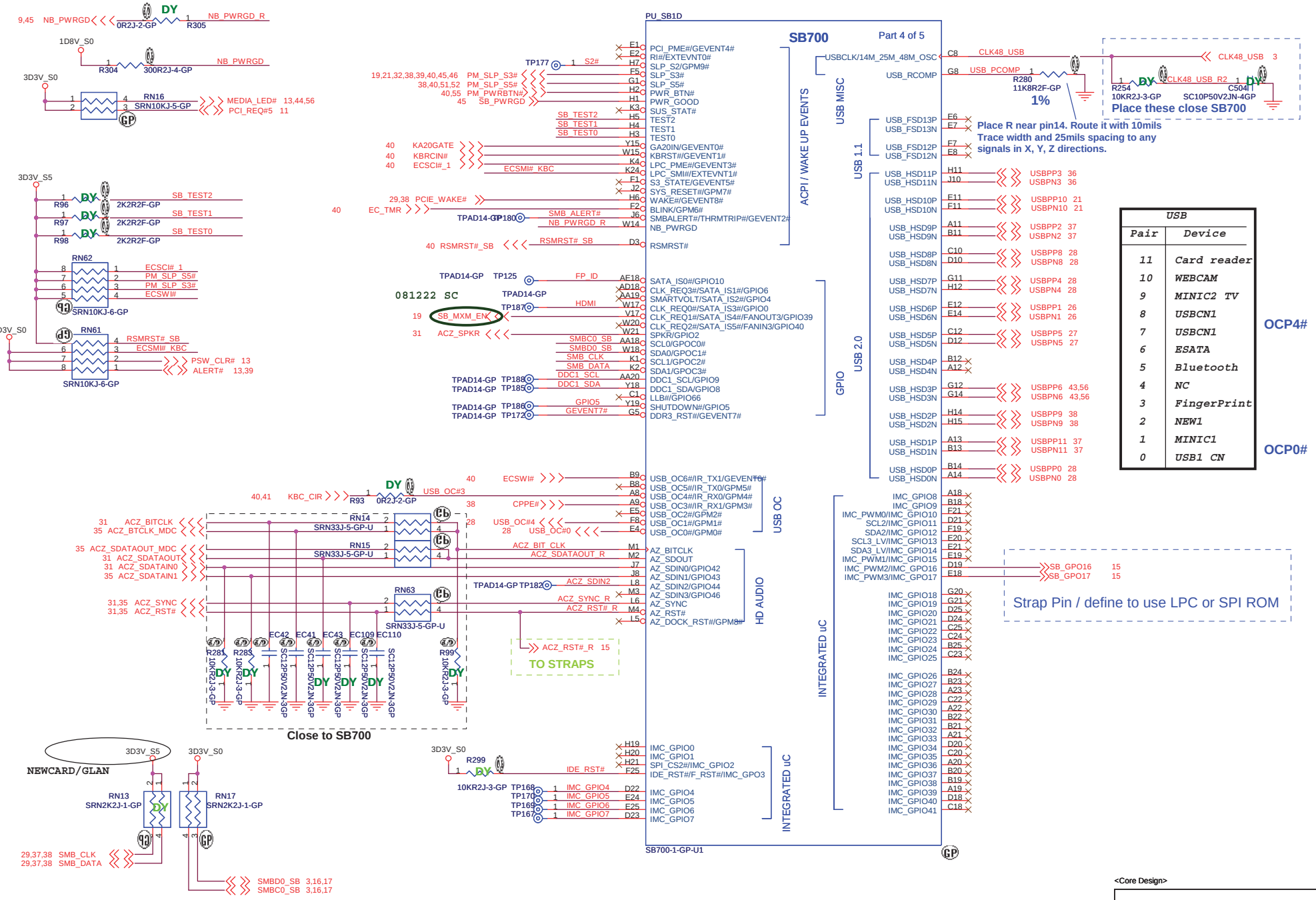

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
PU_NB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
Close to NB ball < 1 inch trace
ENABLE External CLK GEN
110mA
20mA
65mA
120mA
15mA
300mA
090119 -1
090122 -1
081225 SC
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_LVDS&CRT_(2/4)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 9 of 56



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ATi-RS780M_Side Port&PWR&GND(3/3)***
Size: A3	Document Number: **JM70-PU**
Rev: -2	
Date: Monday, March 02, 2009	Sheet 10 of 56


POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
SB700
Part 1 of 5
PU_SB1A
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
081222 SC
081225 SC
Fos SB710 11/14
220 ohm 2A
20mil Width
Place R <100mils form pins T25,T24
68.00217.521
2ND = 68.00119.111
73.07408.L16
2ND = 73.07408.L15
82.30001.841
2nd = 82.30001.A41
3rd = ??.?????.???
62.70001.011
83.00056.Q11
2ND = 83.00056.K11
090122 -1
090206 -1
090119 -1
090213 -1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_PCIE&PCI_(1/5)
JM70-PU
Size A3
Rev -2
Date: Friday, March 06, 2009
Sheet 11 of 56


SB700
Part 4 of 5
PU_SB1D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
CLK48_USB
USB_PCOMP
R280 11K8R2F-GP 1%
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
CLK48_USB_R2
R254 10KR2J-3-GP
C504 SC10P50V2JN-4GP
Place these close SB700
USB
Pair | Device
11 Card reader
10 WEBCAM
9 MINIC2 TV
8 USBCN1
7 USBCN1
6 ESATA
5 Bluetooth
4 NC
3 FingerPrint
2 NEW1
1 MINIC1
0 USB1 CN
OCP4#
OCP0#
Strap Pin / define to use LPC or SPI ROM
SB_GPO16
SB_GPO17
TO STRAPS
ACZ_RST#_R
Close to SB700
NEWCARD/GLAN
RN13 SRN2K2J-1-GP
RN17 SRN2K2J-1-GP
SMB_CLK
SMB_DATA
SMBD0_SB
SMBC0_SB
RN16 SRN10KJ-5-GP
RN62
RN61
SRN10KJ-6-GP
RN14 SRN33J-5-GP-U
RN15 SRN33J-5-GP-U
RN63 SRN33J-5-GP-U
TP177 S2#
TP180 SMB_ALERT#
TP125 FP_ID
TP187 HDMI
TP188 DDC1_SCL
TP185 DDC1_SDA
TP186 GPIO5
TP172 GEVENT7#
TP182 ACZ_SDIN2
TP168 IMC_GPIO4
TP170 IMC_GPIO5
TP169 IMC_GPIO6
TP167 IMC_GPIO7
R299 10KR2J-3-GP
R96 R97 R98 2K2R2F-GP
R93 0R2J-2-GP
R305 0R2J-2-GP
R304 300R2J-4-GP
R281 R283 R99 10KR2J-3-GP
EC42 EC41 EC43 EC109 EC110 SC12P50V2JN-3GP
081222 SC
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 12 of 56

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD
SATA ODD
E-SATA
2nd HDD

C190 C191 C594 C593 C193 C192 C591 C592 C590 C589 C194 C195 C197 C196 C587 C588
SCD01U50V2KX-1GP
090119 -1

PU_SB1B

SB700
Part 2 of 5

SERIAL ATA
SATA_TX0P SATA_TX0N SATA_RX0N SATA_RX0P SATA_TX1P SATA_TX1N SATA_RX1N SATA_RX1P SATA_TX2P SATA_TX2N SATA_RX2N SATA_RX2P SATA_TX3P SATA_TX3N SATA_RX3N SATA_RX3P SATA_TX4P SATA_TX4N SATA_RX4N SATA_RX4P SATA_TX5P SATA_TX5N SATA_RX5N SATA_RX5P SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67

SATA PWR
PLLVDD_SATA XTLVDD_SATA

ATA 66/100/133
IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#
IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30
SB_DIS/UMA# → TP191 TPAD14-GP
CLK_ID_0
CLK_ID_1

SPI ROM
SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32
SB_SPI_MISO → TP175 TPAD14-GP
LAN_RST#/GPIO13 ROM_RST#/GPIO14
LAN_RST# → TP184 TPAD14-GP

HW MONITOR
FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49
FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52
TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64
ALERT# 12,39
VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60
PSW_CLR# → PSW_CLR# 12
G62 GAP-OPEN

AVDD AVSS
AVDD_HWM 3D3V_S5
R273 0R0402-PAD
C524 SCD1U10V2KX-4GP

SB700-1-GP-U1

Very Close to SB700
C581 SC15P50V2JN-2-GP
X3 XTAL-25MHZ-96GP
82.30020.791
2ND = 82.30020.971
R303 10MR2J-L-GP
R298 1KR2F-3-GP
SATA_X2_R
R302 300R2J-4-GP
C569 SC15P50V2JN-2-GP
12,44,56 MEDIA_LED#

1D2V_S0
PLLVDD_SATA
20mil Width
R293 0R0402-PAD
C560 SC1U10V2KX-1GP
C561 SCD1U10V2KX-4GP
Close to SB700

3D3V_S0
XTLVDD_SATA
20mil Width
R294 0R0402-PAD
C557 SC1U10V2KX-1GP
Close to SB700

3D3V_S0
R317 10KR2J-3-GP
R316 10KR2J-3-GP
R324 10KR2J-3-GP
R323 10KR2J-3-GP
CLK_ID_1
CLK_ID_0

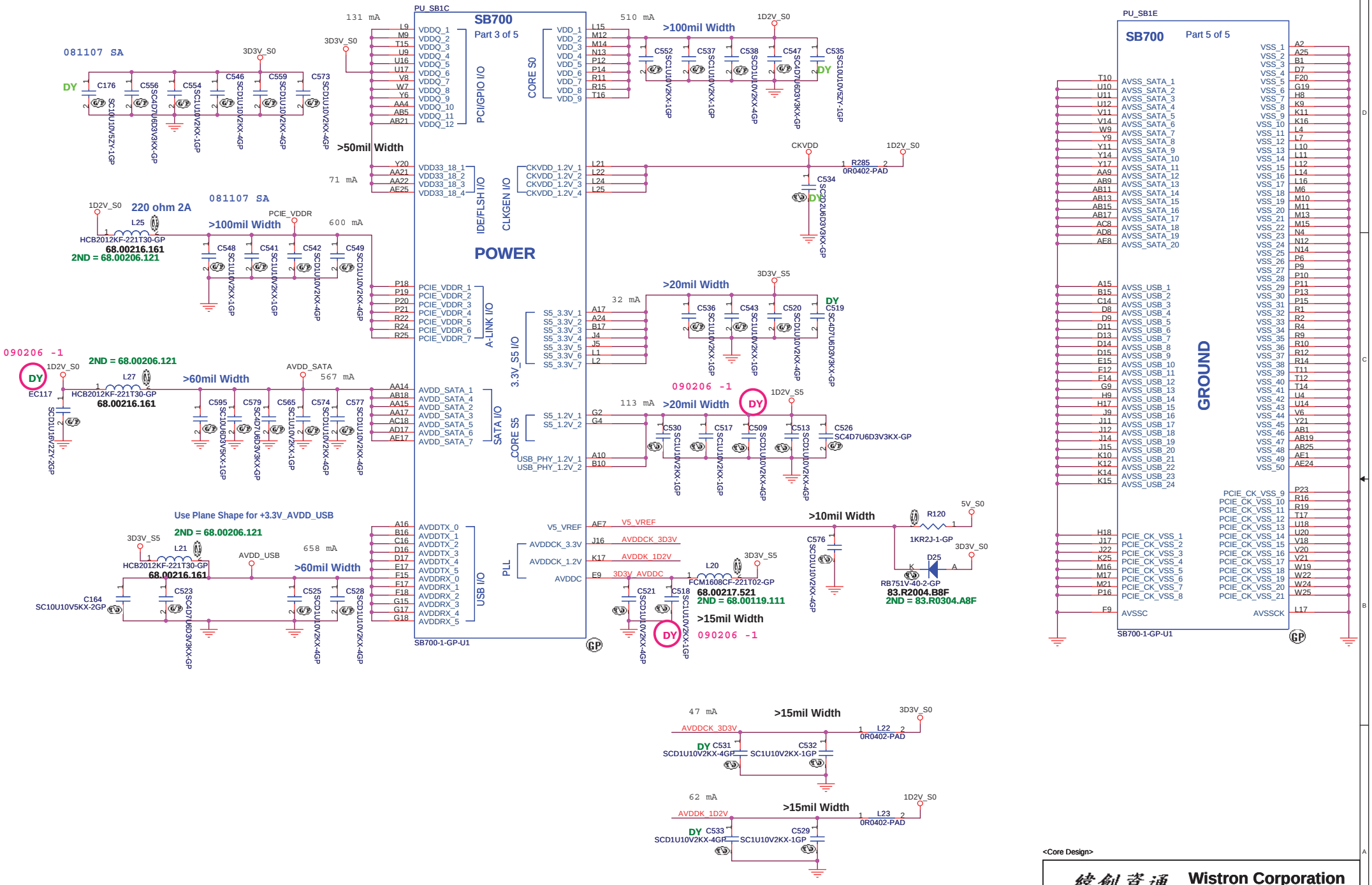
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)
Size: A3
Document Number: JM70-PU
Rev: -2
Date: Friday, March 06, 2009
Sheet 13 of 56



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

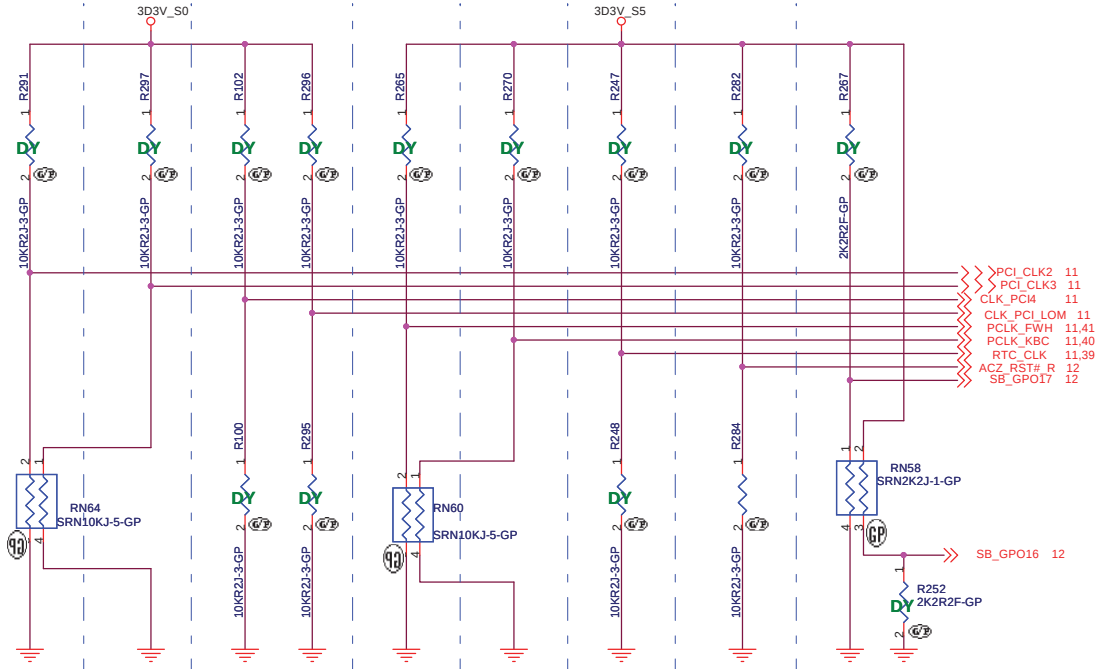
Title: ATi-SB700_POWER&GND_(4/5)

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Monday, March 02, 2009 Sheet 14 of 56

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved; H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM; L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

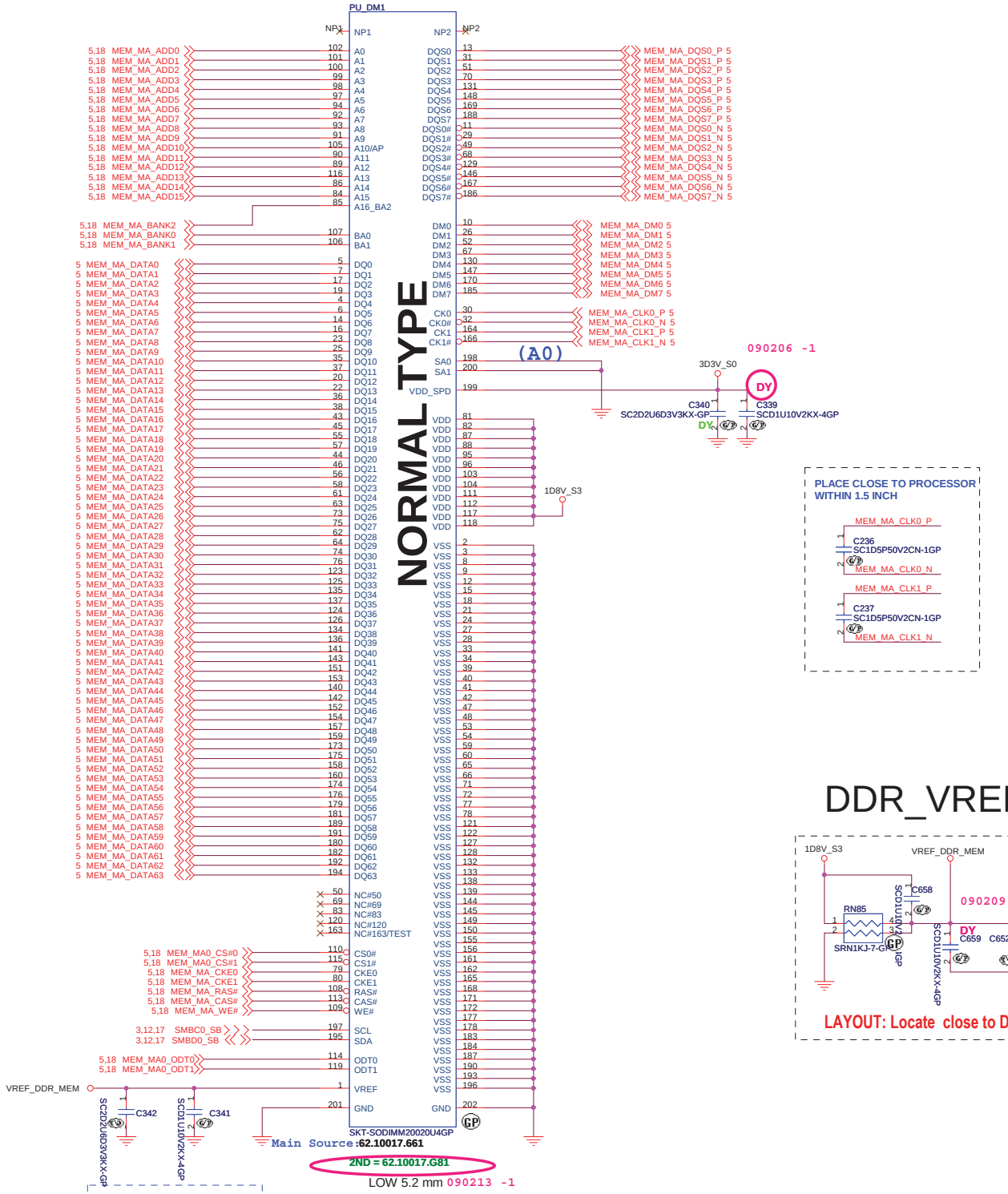
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 15 of 56



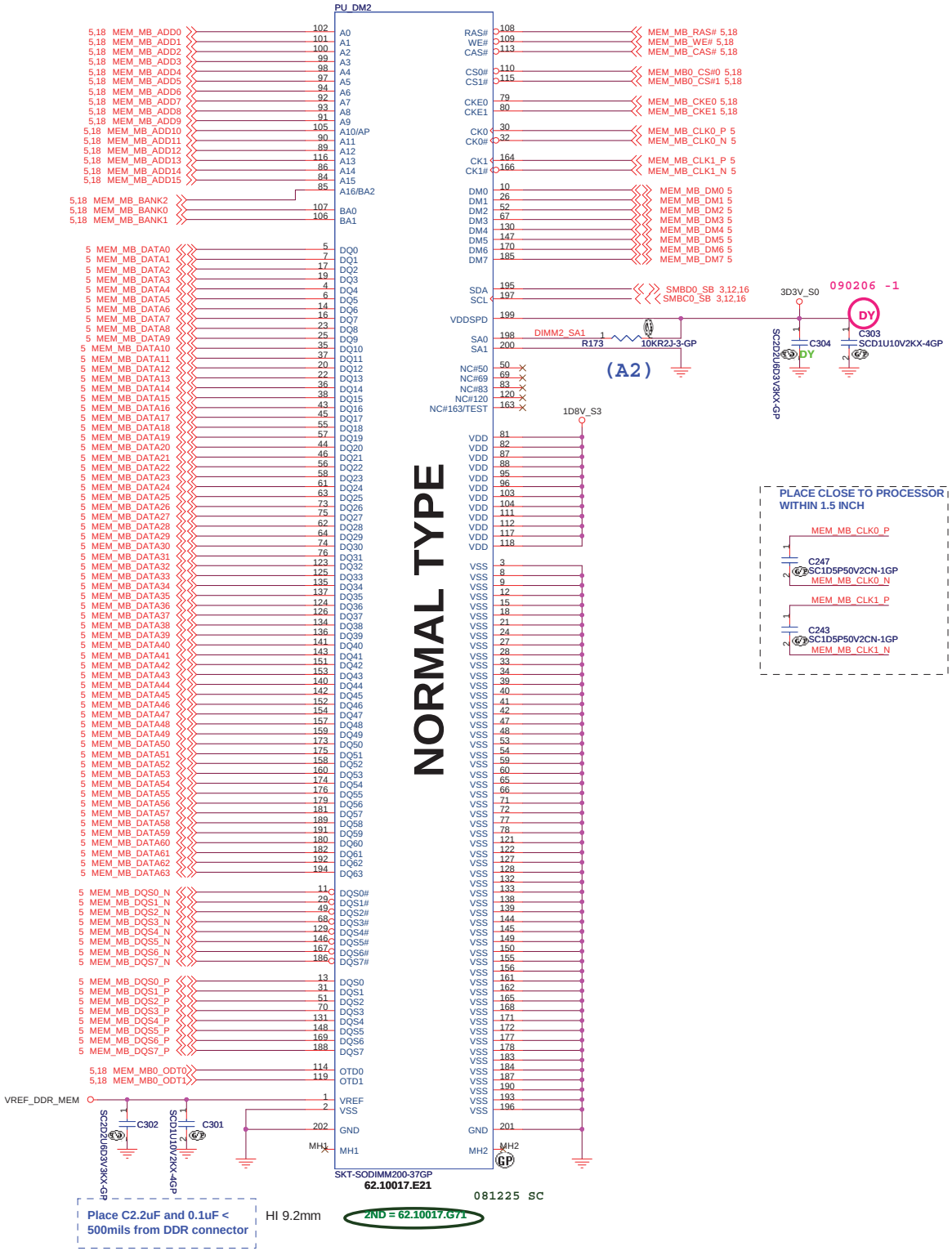
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 16 of 56



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_2

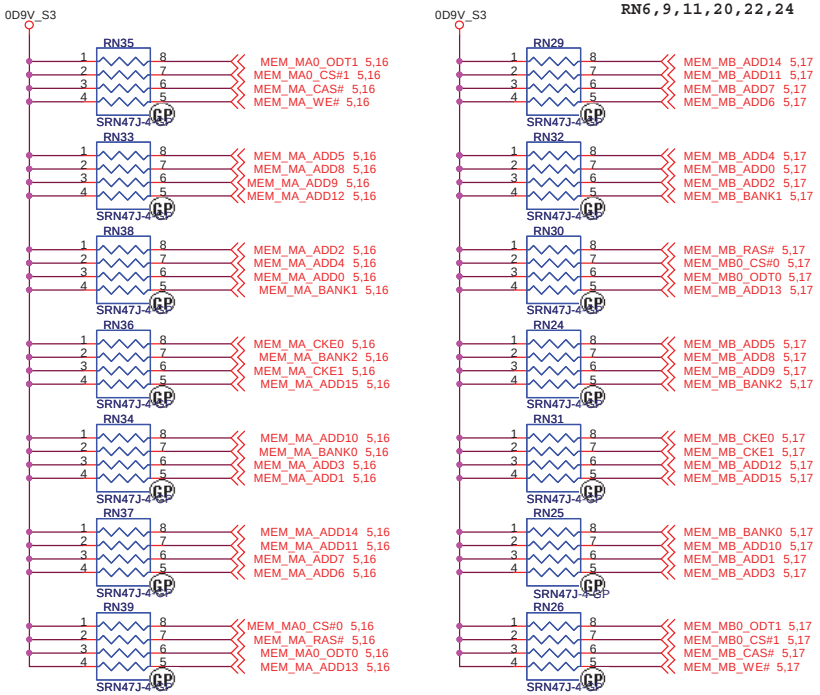
Size	Document Number	Rev
Custom	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 17 of 56

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Net swap 11/14
RN6,9,11,20,22,24

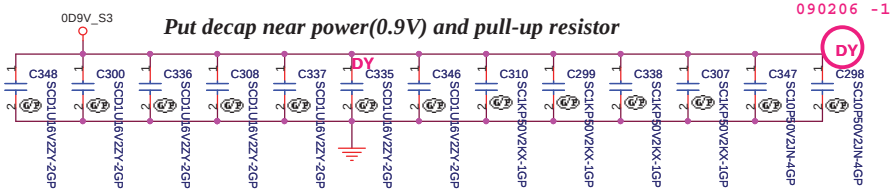


Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

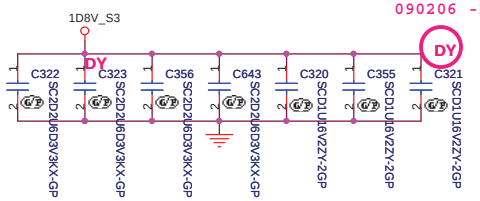
Put decap near power(0.9V) and pull-up resistor

090206 -1



Place these Caps near DM1

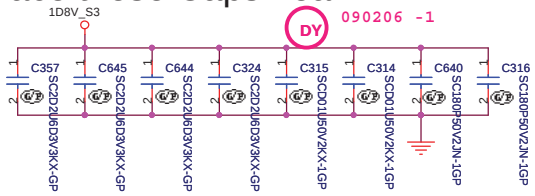
090206 -1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2

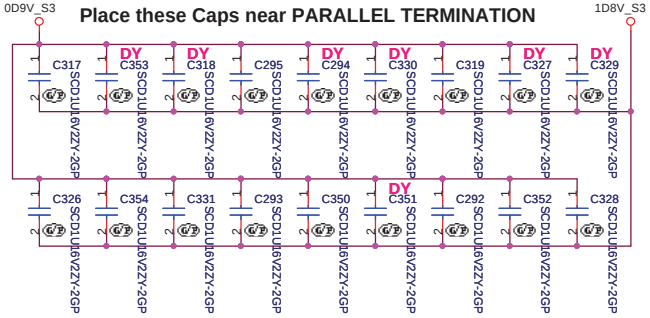
090206 -1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

090209 -1

Place these Caps near PARALLEL TERMINATION



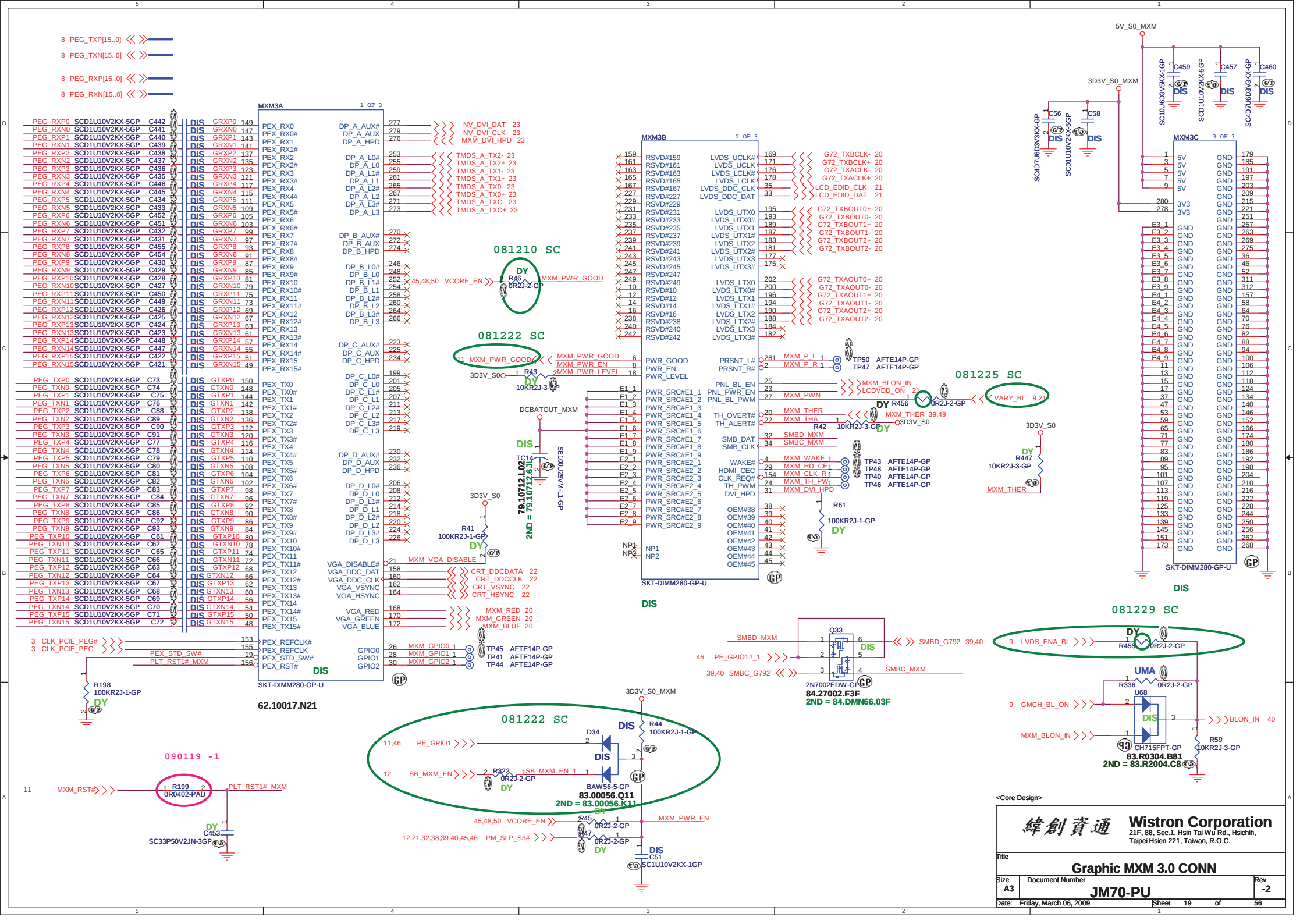
<Core Design>

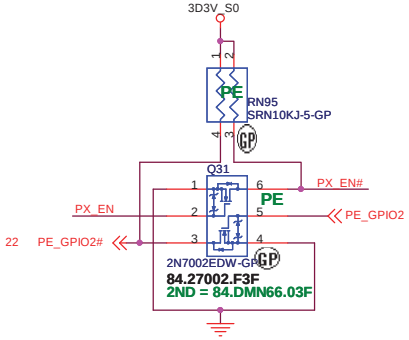
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

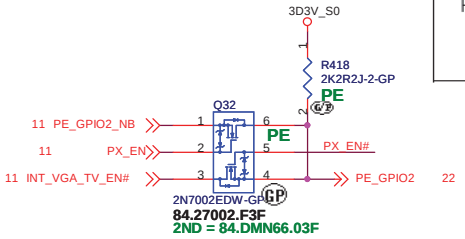
Title: ***DDR_DAMPING & TERMINATION***

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 18 of 56

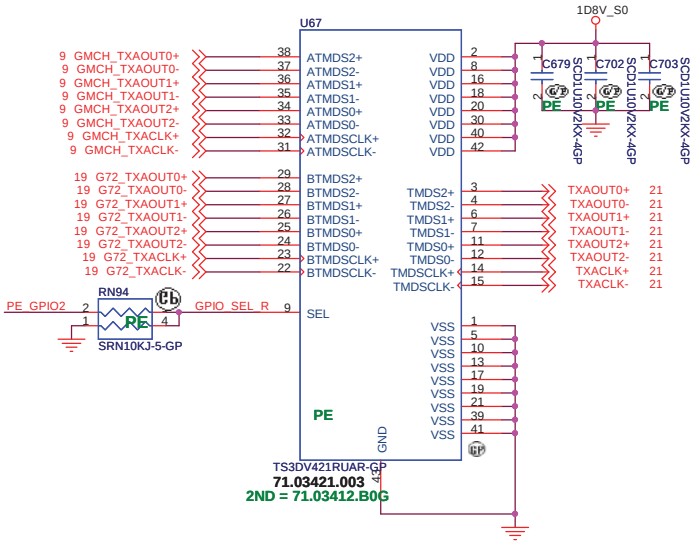

8 PEG_TXP[15..0]
8 PEG_TXN[15..0]
8 PEG_RXP[15..0]
8 PEG_RXN[15..0]
MXM3A
1 OF 3
SKT-DIMM280-GP-U
62.10017.N21
MXM3B
2 OF 3
SKT-DIMM280-GP-U
MXM3C
3 OF 3
SKT-DIMM280-GP-U
081210 SC
081222 SC
081225 SC
081229 SC
090119 -1
5V_S0_MXM
3D3V_S0_MXM
3D3V_S0
DCBATOUT_MXM
MXM_PWR_GOOD
MXM_PWR_EN
MXM_PWR_LEVEL
VCORE_EN
PM_SLP_S3#
MXM_RST#
PLT_RST1#_MXM
MXM_VGA_DISABLE
CRT_DDCDATA
CRT_DDCCLK
CRT_VSYNC
CRT_HSYNC
MXM_RED
MXM_GREEN
MXM_BLUE
MXM_GPIO0
MXM_GPIO1
MXM_GPIO2
PEX_STD_SW#
CLK_PCIE_PEG#
CLK_PCIE_PEG
NV_DVI_DAT
NV_DVI_CLK
MXM_DVI_HPD
TMDS_A_TX2-
TMDS_A_TX2+
TMDS_A_TX1-
TMDS_A_TX1+
TMDS_A_TX0-
TMDS_A_TX0+
TMDS_A_TXC-
TMDS_A_TXC+
G72_TXBCLK-
G72_TXBCLK+
G72_TXACLK-
G72_TXACLK+
LCD_EDID_CLK
LCD_EDID_DAT
G72_TXBOUT0+
G72_TXBOUT0-
G72_TXBOUT1+
G72_TXBOUT1-
G72_TXBOUT2+
G72_TXBOUT2-
G72_TXAOUT0+
G72_TXAOUT0-
G72_TXAOUT1+
G72_TXAOUT1-
G72_TXAOUT2+
G72_TXAOUT2-
MXM_P_L
MXM_P_R
MXM_BLON_IN
LCDVDD_ON
MXM_PWN
MXM_THER
MXM_THA
MXM_WAKE
MXM_HD_CE
MXM_CLK_R
MXM_TH_PW
MXM_DVI_HPD
SMBD_MXM
SMBC_MXM
LVDS_ENA_BL
GMCH_BL_ON
MXM_BLON_IN
BLON_IN
VARY_BL
SMBD_G792
SMBC_G792
PE_GPIO1#_1
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
83.00056.Q11
2ND = 83.00056.K11
83.R0304.B81
2ND = 83.R2004.C8
79.10712.L03
2ND = 79.10712.L01
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Graphic MXM 3.0 CONN
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 19 of 56

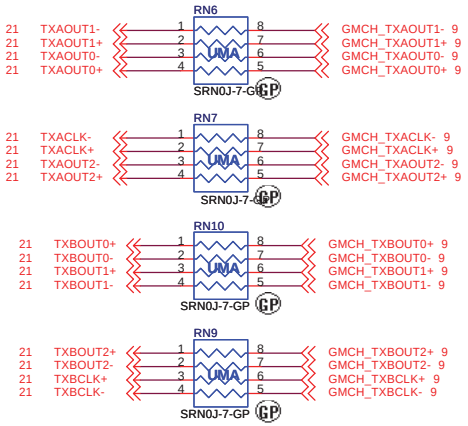


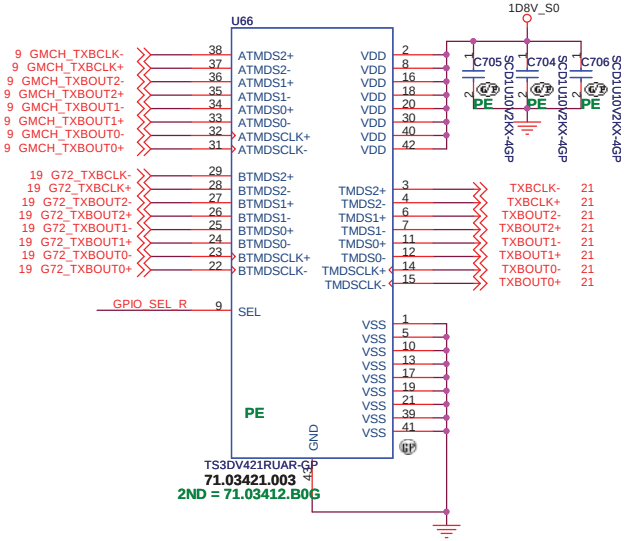


FUNCTION TABLE

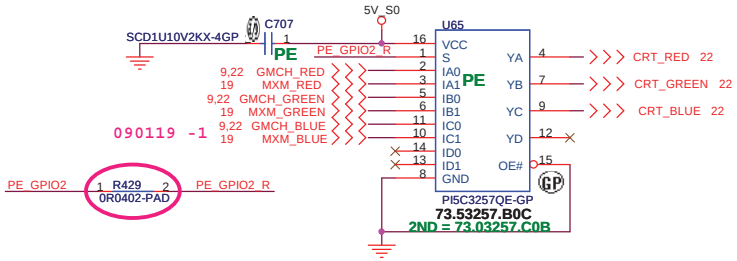
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DISPLAY SUPPORT TABLE

	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)

<Core Design>

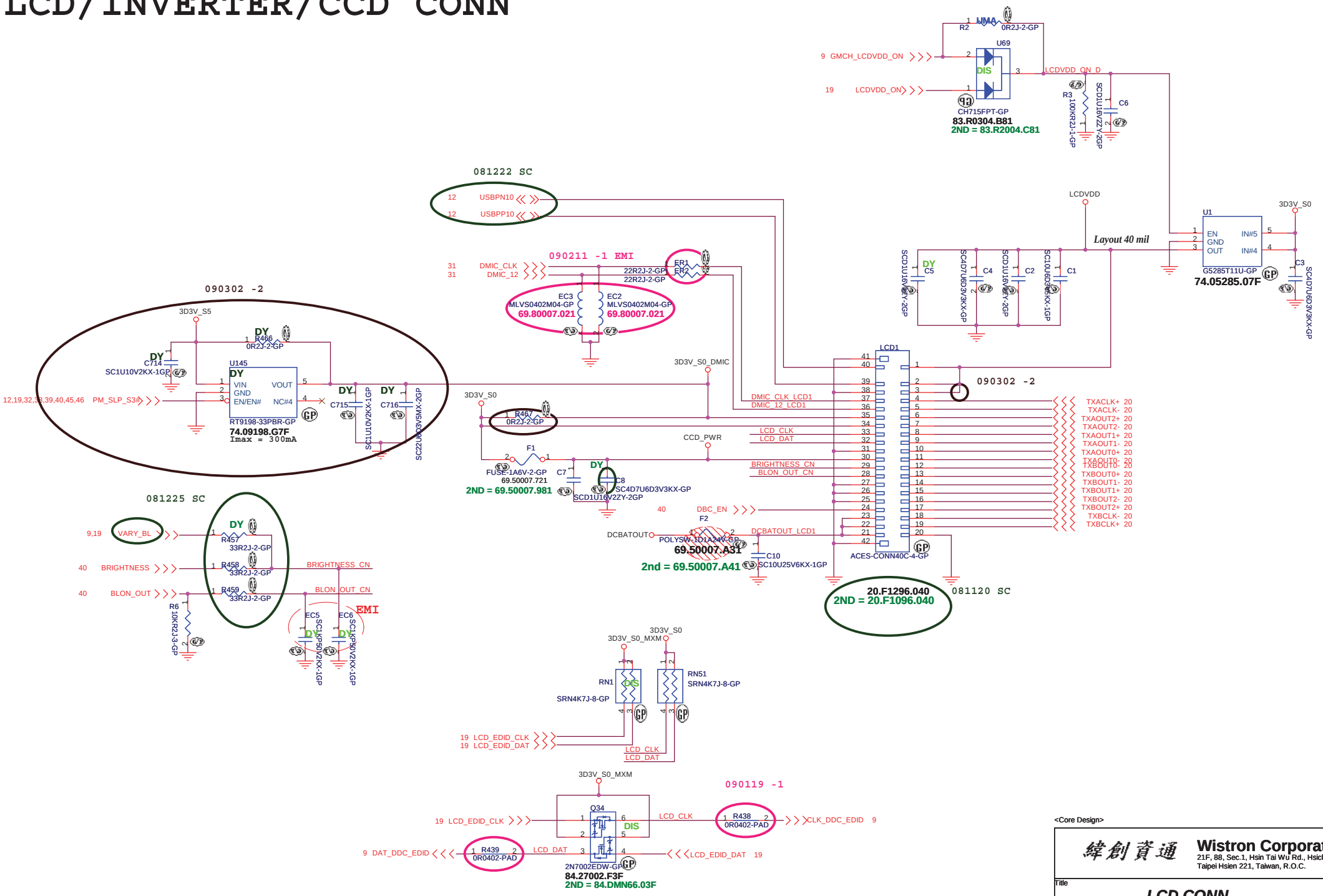
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SWITCH

Size | Document Number: JM70-PU | Rev: -2

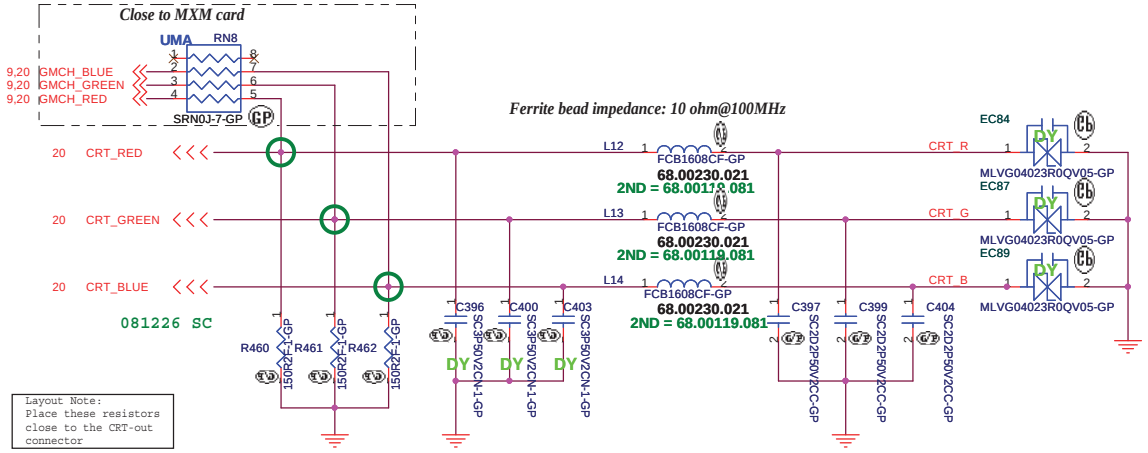
Date: Friday, March 06, 2009 | Sheet 20 of 56

LCD/INVERTER/CCD CONN



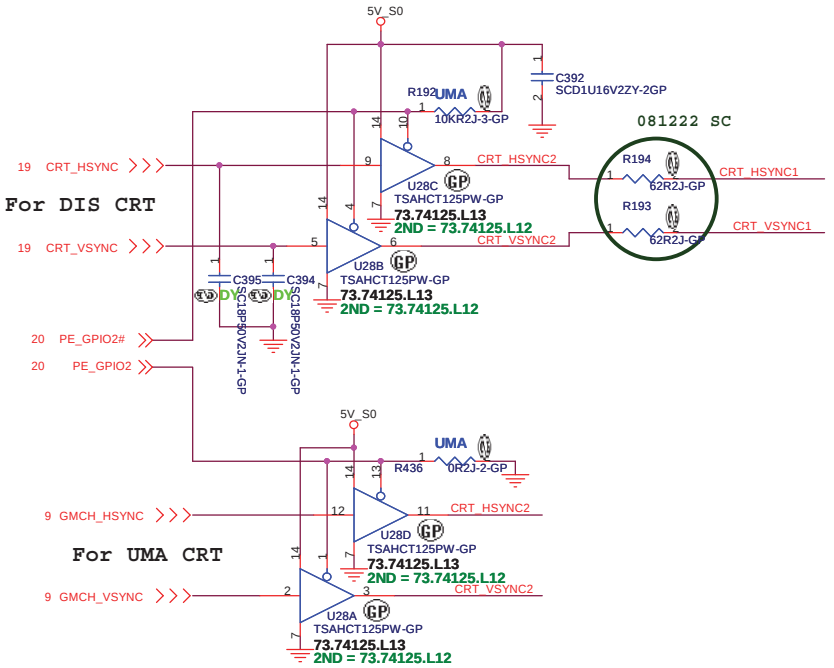
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CONN	
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 21 of 56	

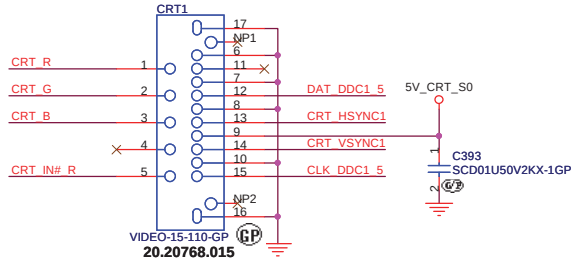


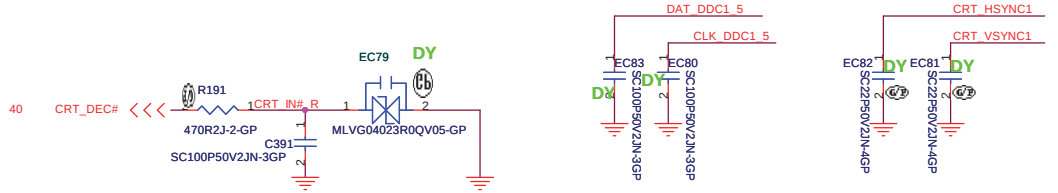
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

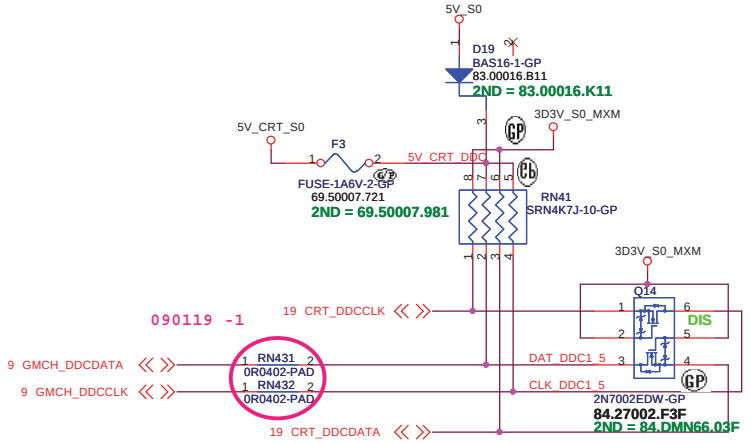


CRT I/F & CONNECTOR





DDC_CLK & DATA level shift



<Core Design>

緯創資通 **Wistron Corporation**
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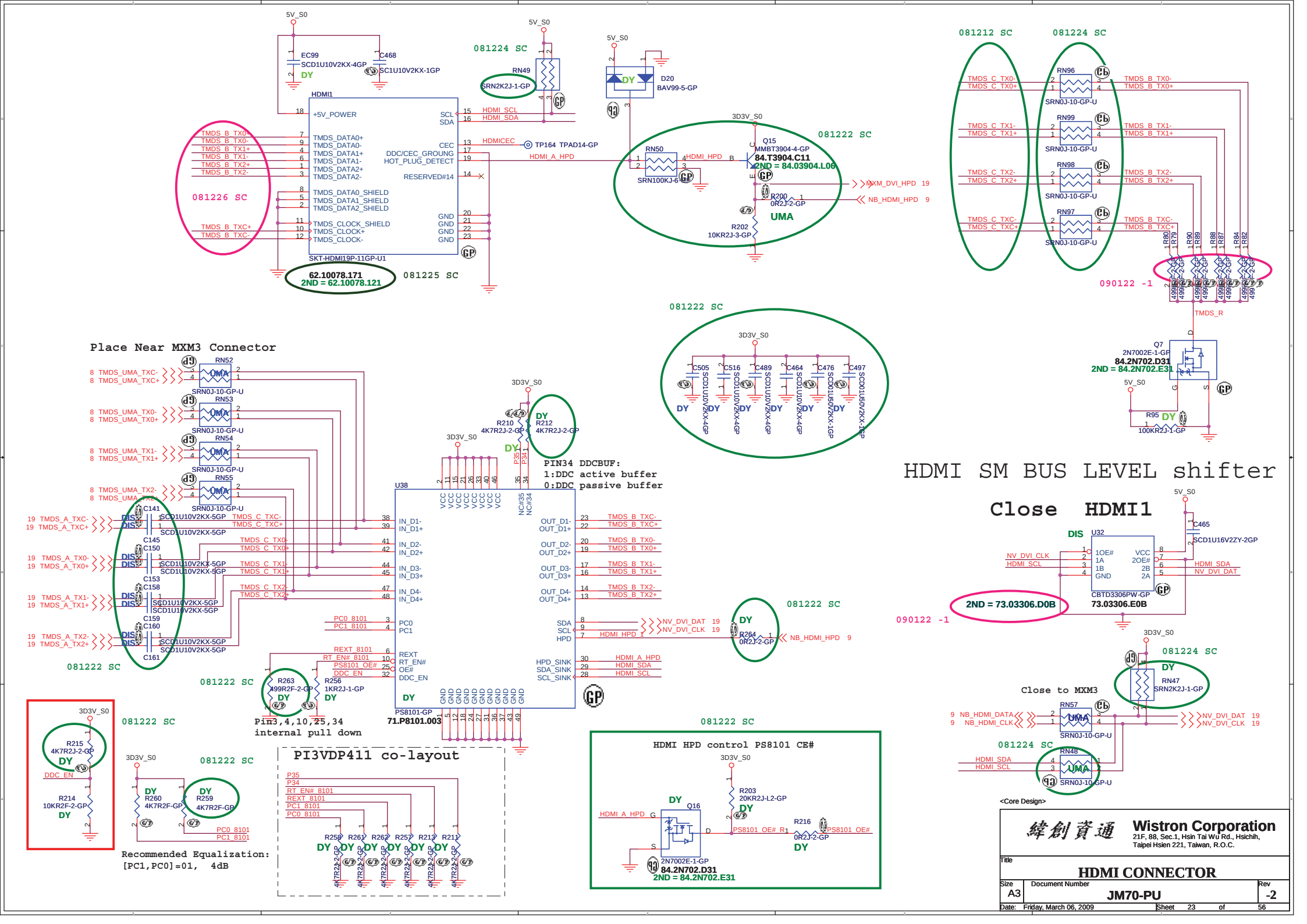
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CRT Connector**	
Size	Document Number: **JM70-PU**	Rev: -2
Date: Friday, March 06, 2009	Sheet 22 of 56	


HDMI SM BUS LEVEL shifter
Close HDMI1
Place Near MXM3 Connector
PI3VDP411 co-layout
HDMI HPD control PS8101 CE#
Close to MXM3
Recommended Equalization:
[PC1,PC0]=01, 4dB
Pin3,4,10,25,34
internal pull down
PIN34 DDCBUF:
1:DDC active buffer
0:DDC passive buffer
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
081225 SC
081226 SC
081224 SC
081222 SC
081212 SC
090122 -1
U38
PS8101-GP
71.P8101.003
U32
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
Q15
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
Q16
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Q7
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
D20
BAV99-5-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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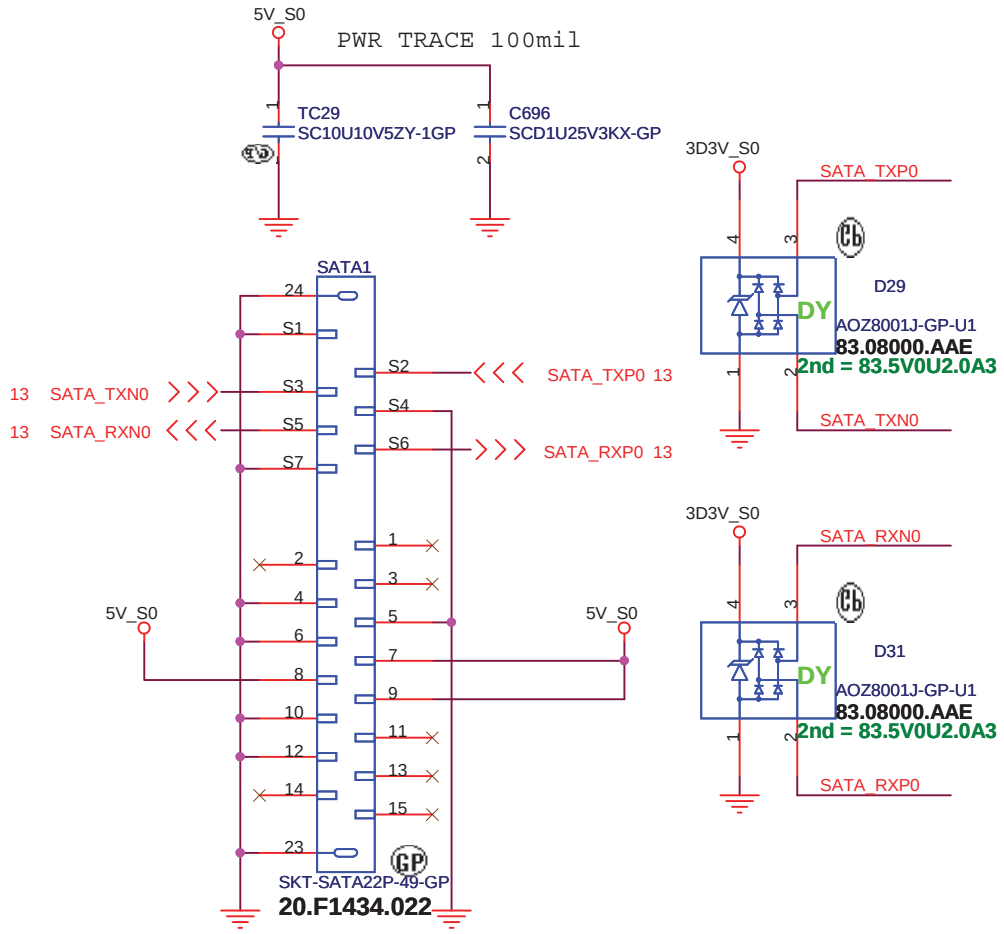
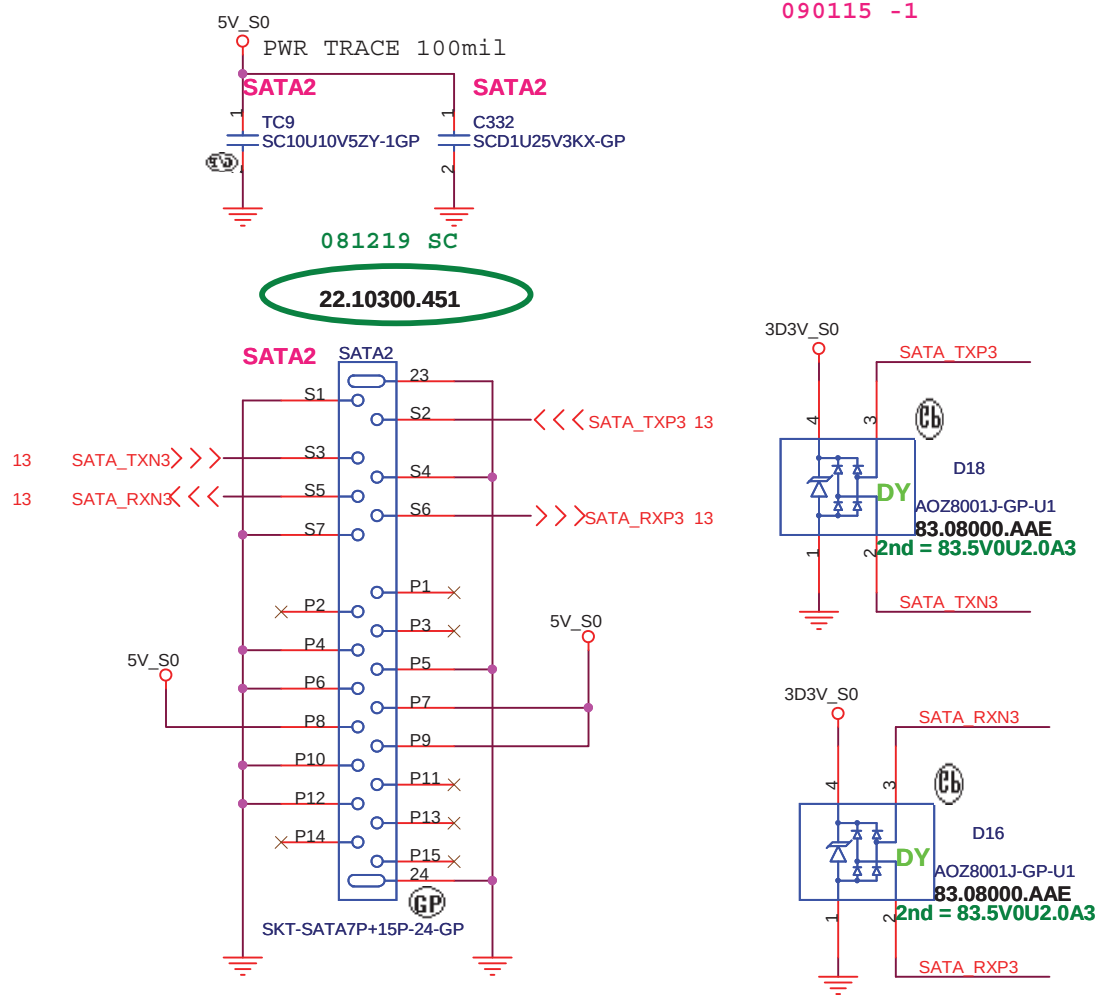
HDMI CONNECTOR
JM70-PU
Size A3
Rev -2
Date: Friday, March 06, 2009
Sheet 23 of 56

SATA HDD Connector



2ND SATA HDD Connector

090115 -1



<Core Design>

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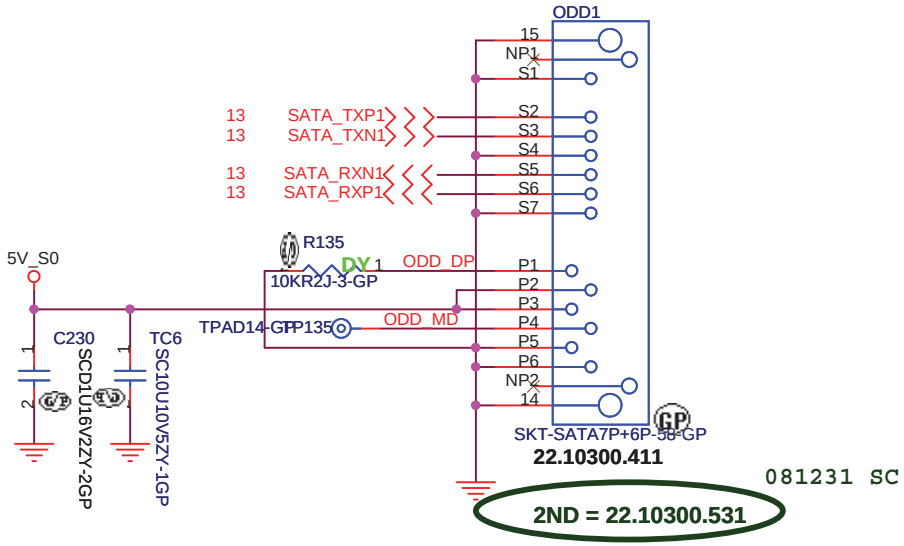
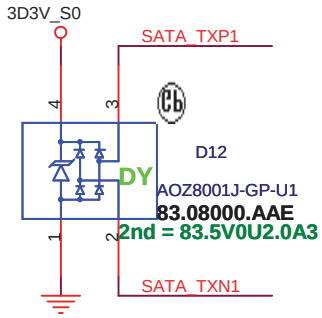
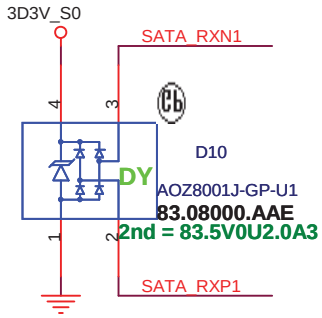
Title	HDD	
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 24 of 56	

ODD Connector







<Core Design>

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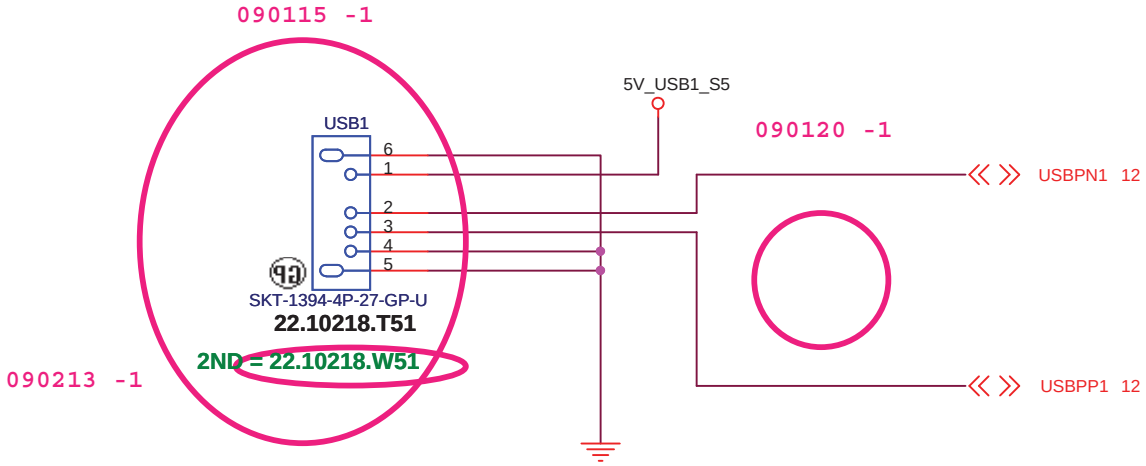
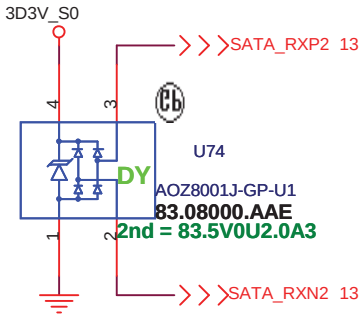
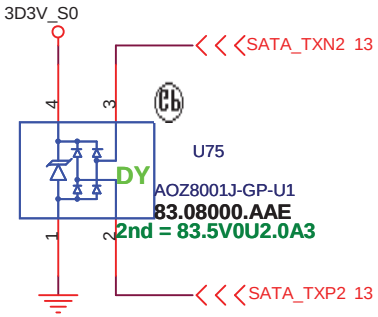
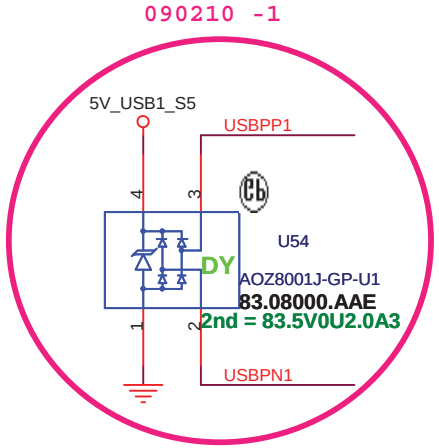
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM		
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 25 of 56	









<Core Design>

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Title: ***USB1***		
Size: **A4**	Document Number: **JM70-PU**	Rev: **-2**
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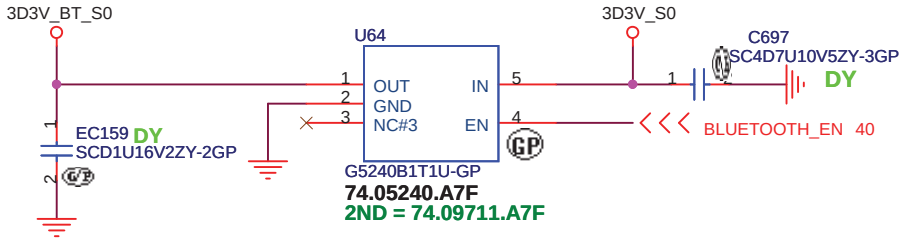
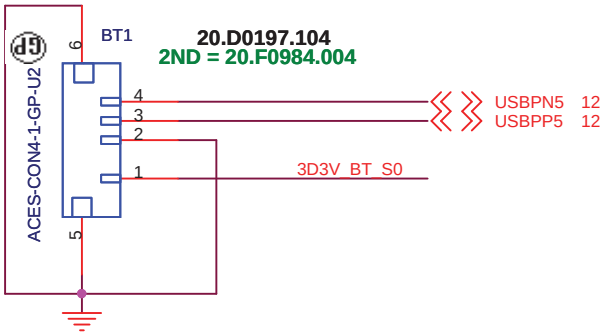
BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request



<Core Design>

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Title	BLUETOOTH	
Size: A4	Document Number: JM70-PU	Rev: -2
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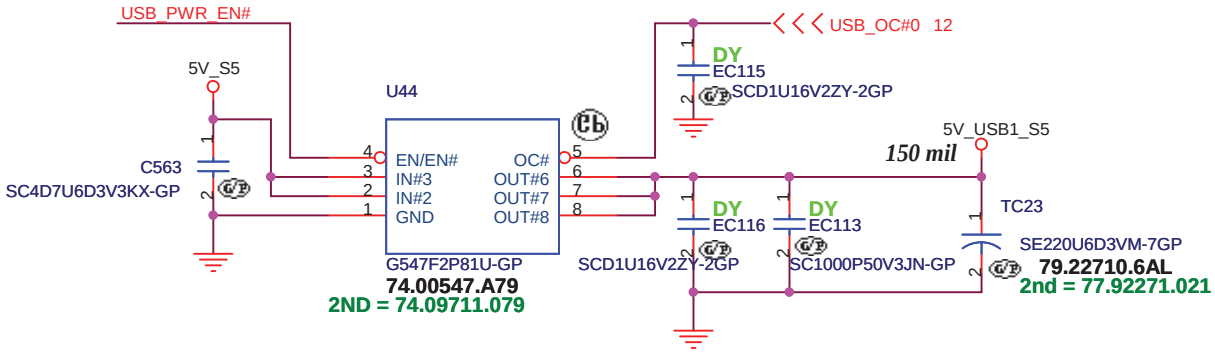
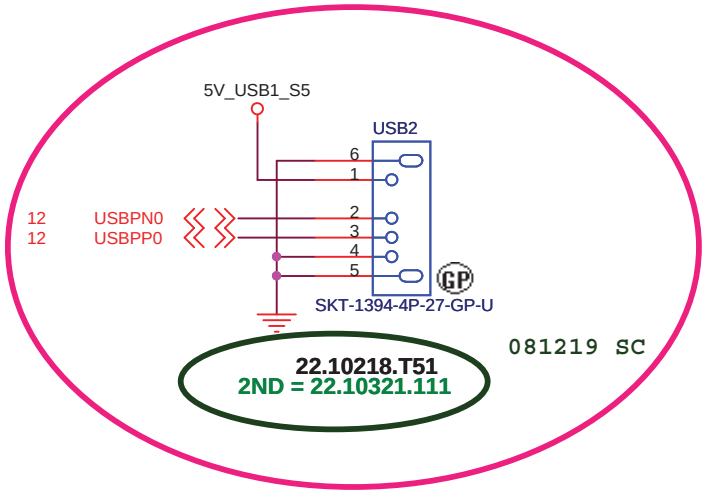
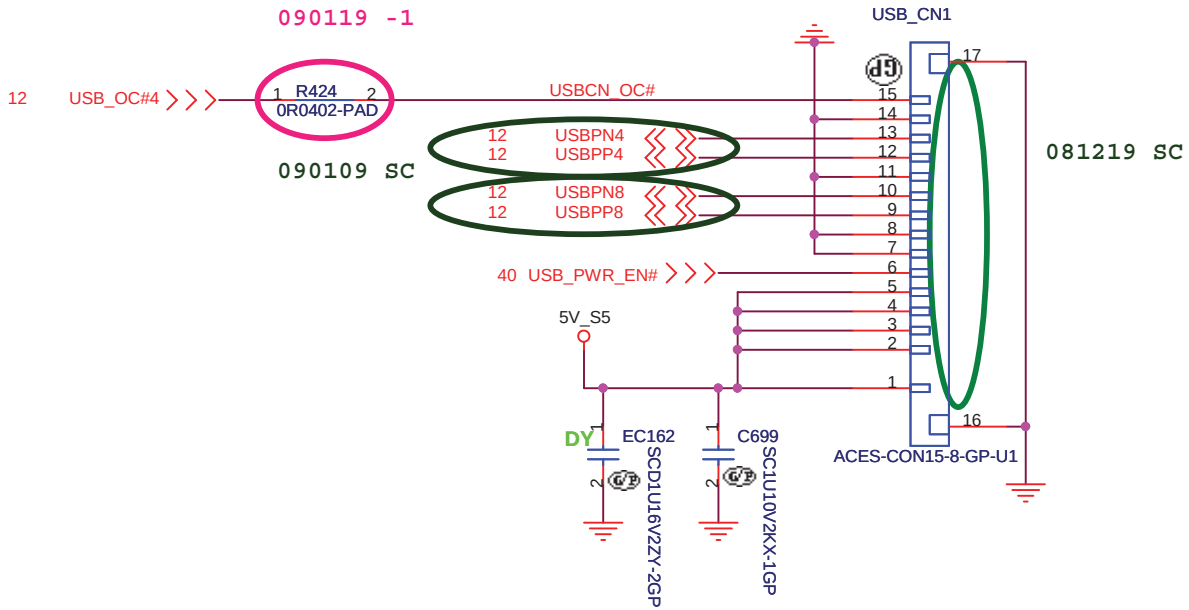


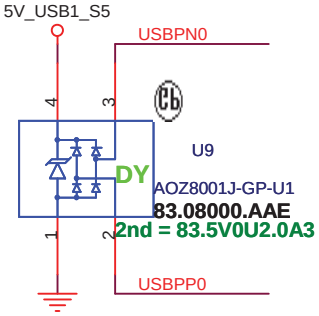
090115 -1



20.F1290.015
2ND = 21.D0214.115

090119 -1





<Core Design>

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Title: ***USB2***		
Size: A4	Document Number: **JM70-PU**	Rev: -2
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Note: SI, SO, CS, and SCLK have internal pull-ups.

Table 7: NVRAM Pin Strapping (EEPROM)

NVRAM Type	SO	SI	CS	SCLK
EEPROM—24c64–376 KHz	1	1	0	1
EEPROM—24c512–376 KHz	1	1	0	1
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0

U4

BCM5784MKMLG-GP

71.05784.M03

U27 AT24C02BN-SH-T-GP

72.24C02.R01

2ND = 72.24C02.M01

Q13 BCP69-GP

84.00069.B1B

2ND = 84.DCP69.01B

X1 XTAL-25MHZ-96GP

82.30020.791

2ND = 82.30020.971

FCM1608K-601T03GP

68.00217.241

2ND = 68.00248.011

RN4 SRN1KJ-10-GP

081222 SC

081223 SC

Place PLLVDD/AVDDL CKT as close to chip as possible

R349 change to Bead for Transmitter Distortion

<Core Design>

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Title: BCM5784MKMLG

Size: A3 | Document Number: JM70-PU | Rev: -2

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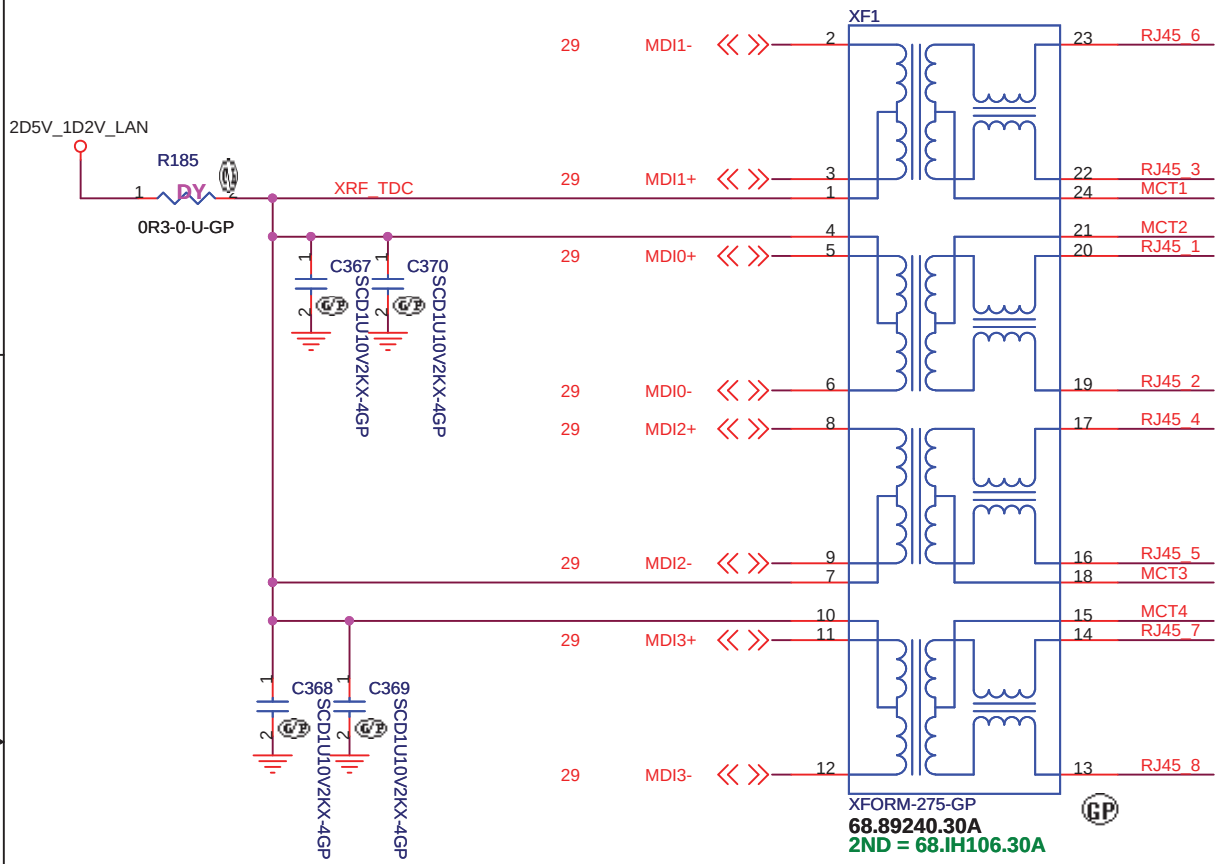
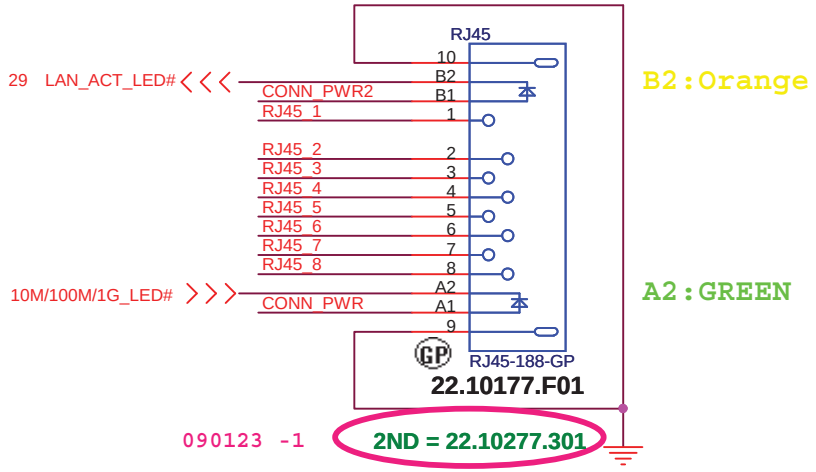
LAN Connector

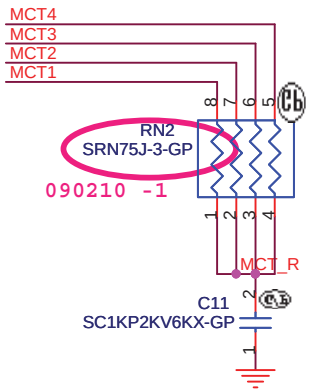


Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

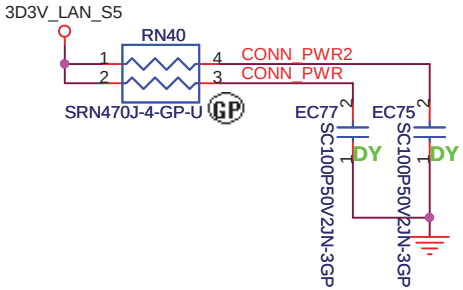


LAN Link: Green(A2), behavior is the same for 10/100/1000 bits

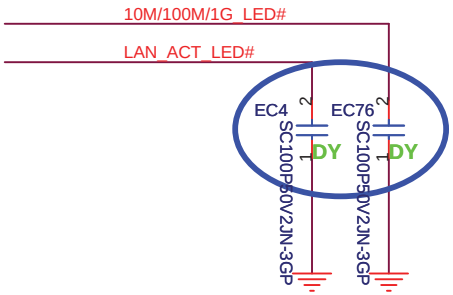
LAN Data: Yellow(B2), when LAN is transfering data.



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



For EMI Near LAN1 CONN



<Core Design>

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Title: **LAN CONN**

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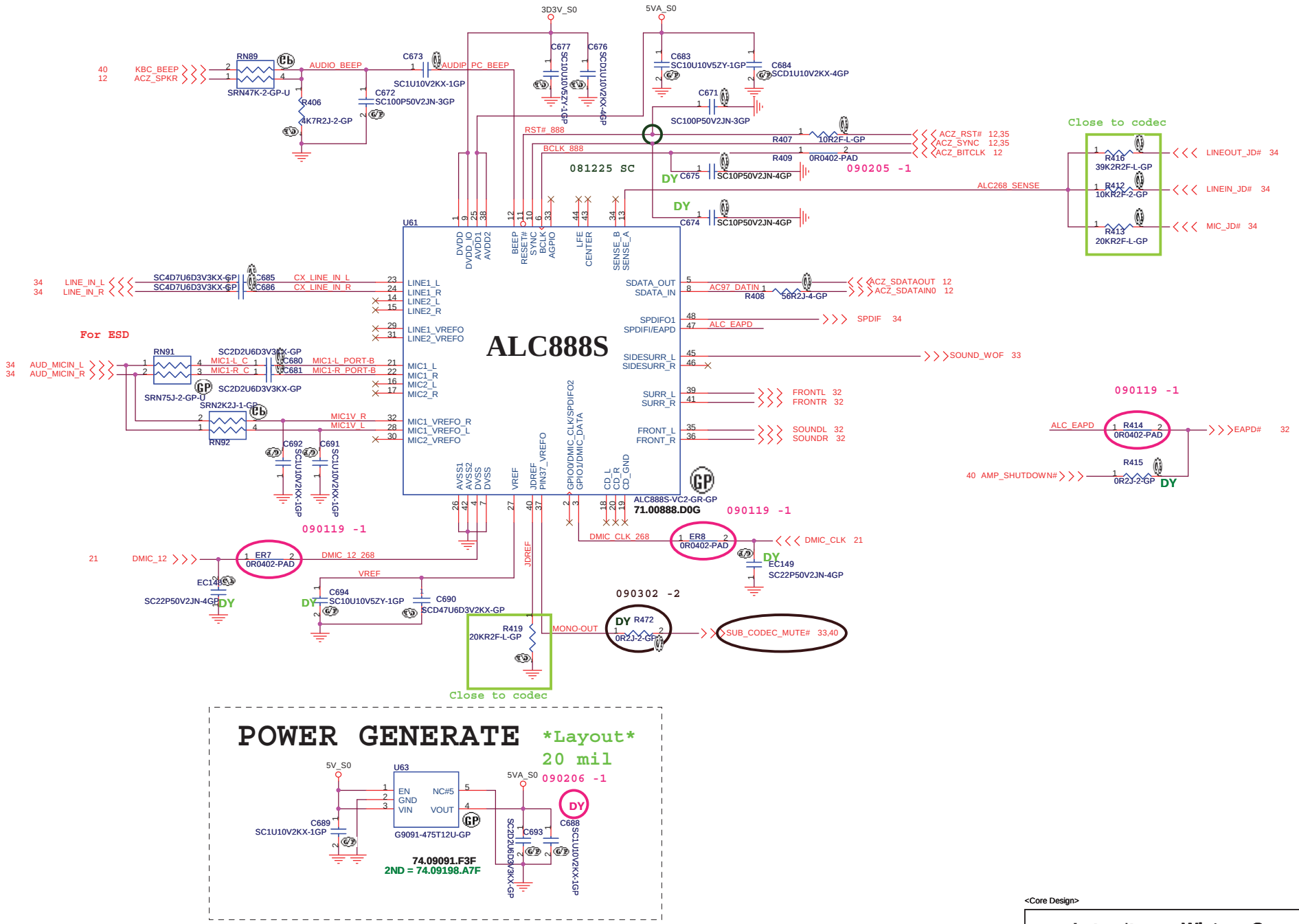

<Core Design>

緯創資通 Wistron Corporation
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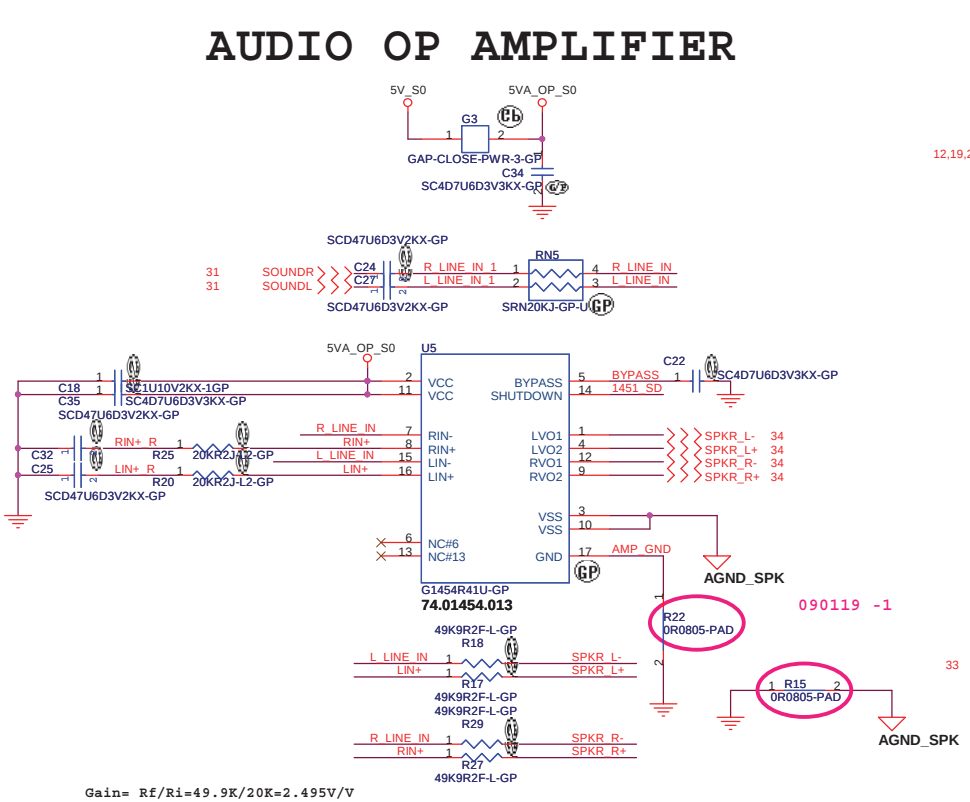
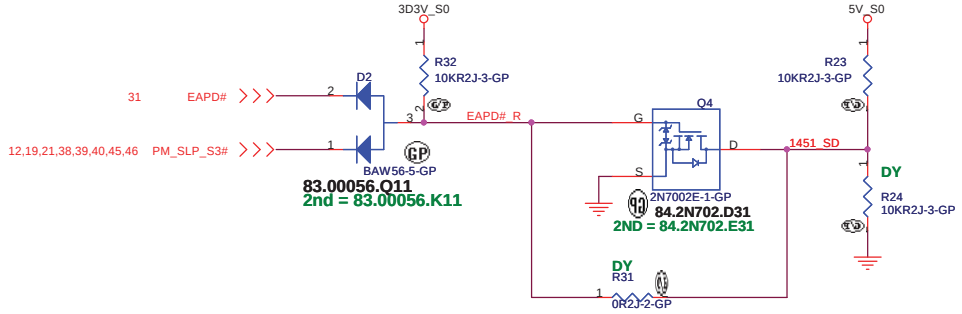
Taipei Hsien 221, Taiwan, R.O.C.

Title	Azalia codec ALC268	
Size: A3	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 31 of 56	

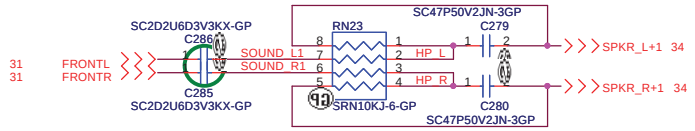
AUDIO OP AMPLIFIER

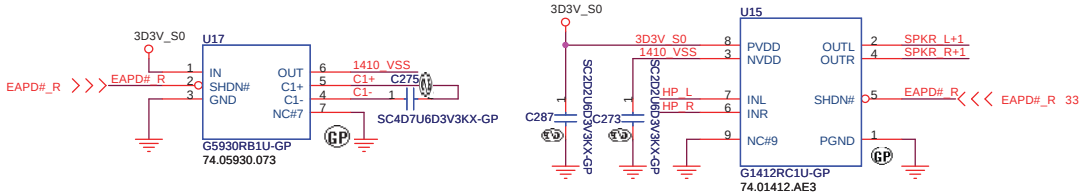


Gain= Rf/Ri=49.9K/20K=2.495V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V
V(rms)=2.828V
Power= 2.828^2/4=1.999W



090101 SC





Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?

<Core Design>

緯創資通 **Wistron Corporation**
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Title: AUDIO AMP		
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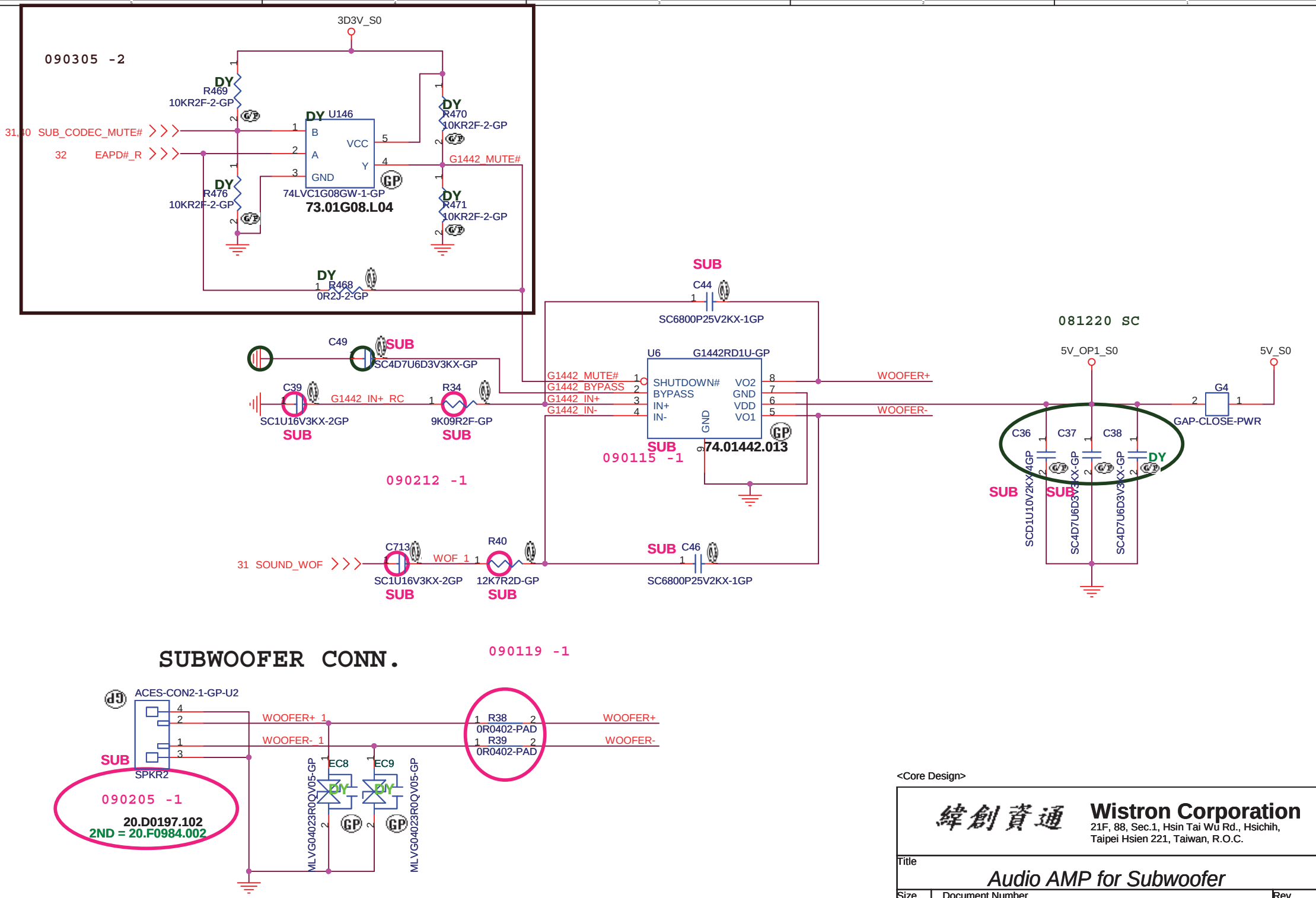

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio AMP for Subwoofer*

Size	Document Number	Rev
A4	JM70-PU	-2

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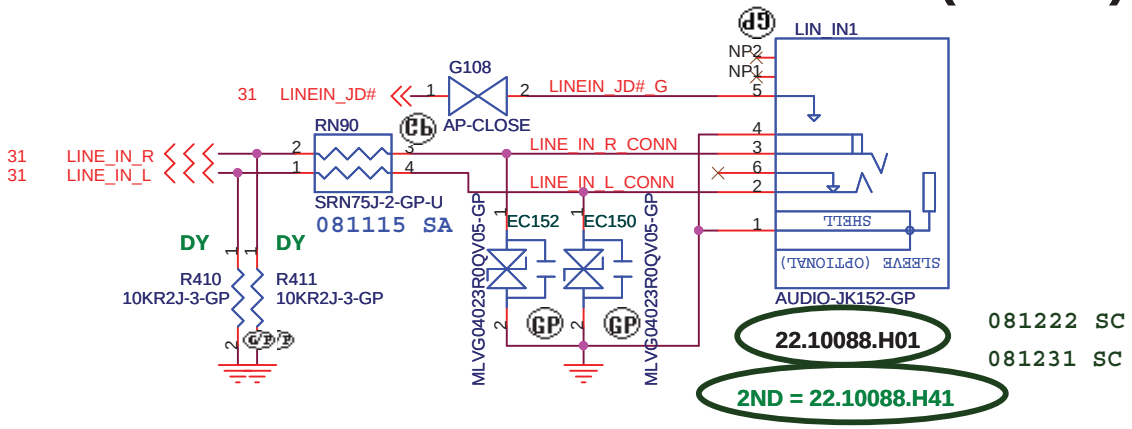
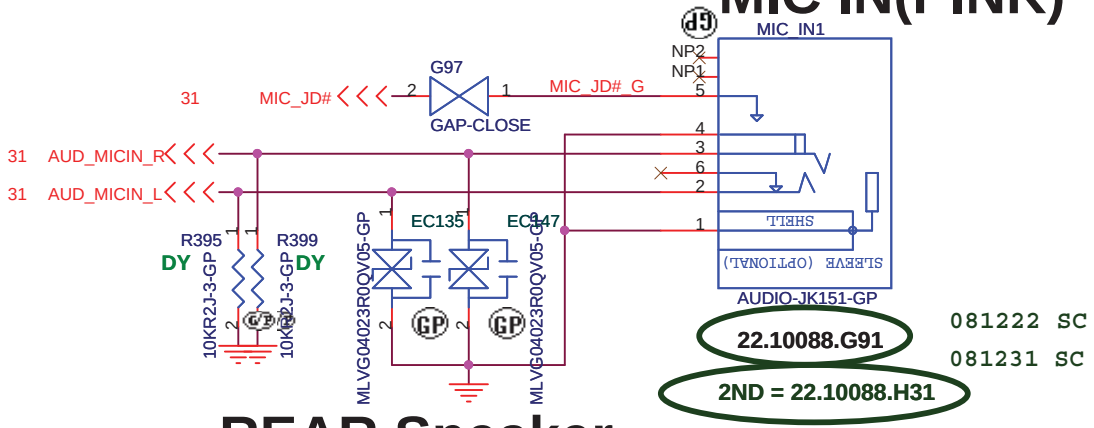
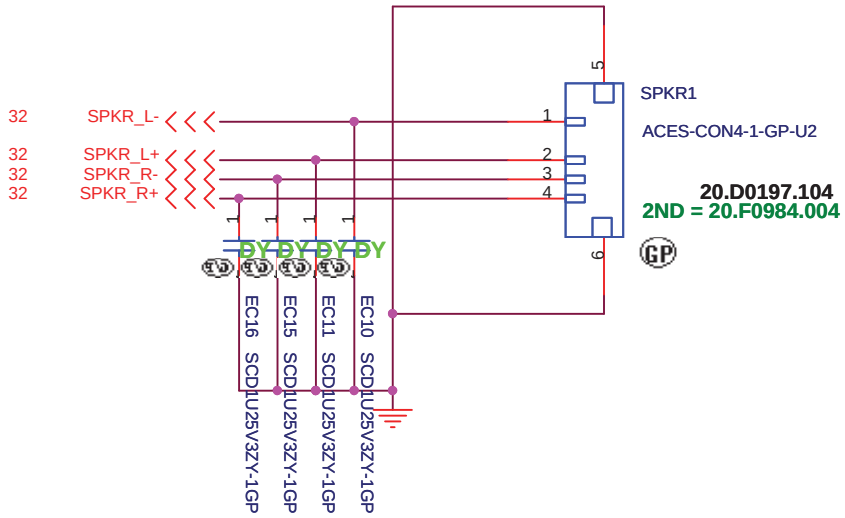
LINE IN(BLUE)



MIC IN(PINK)

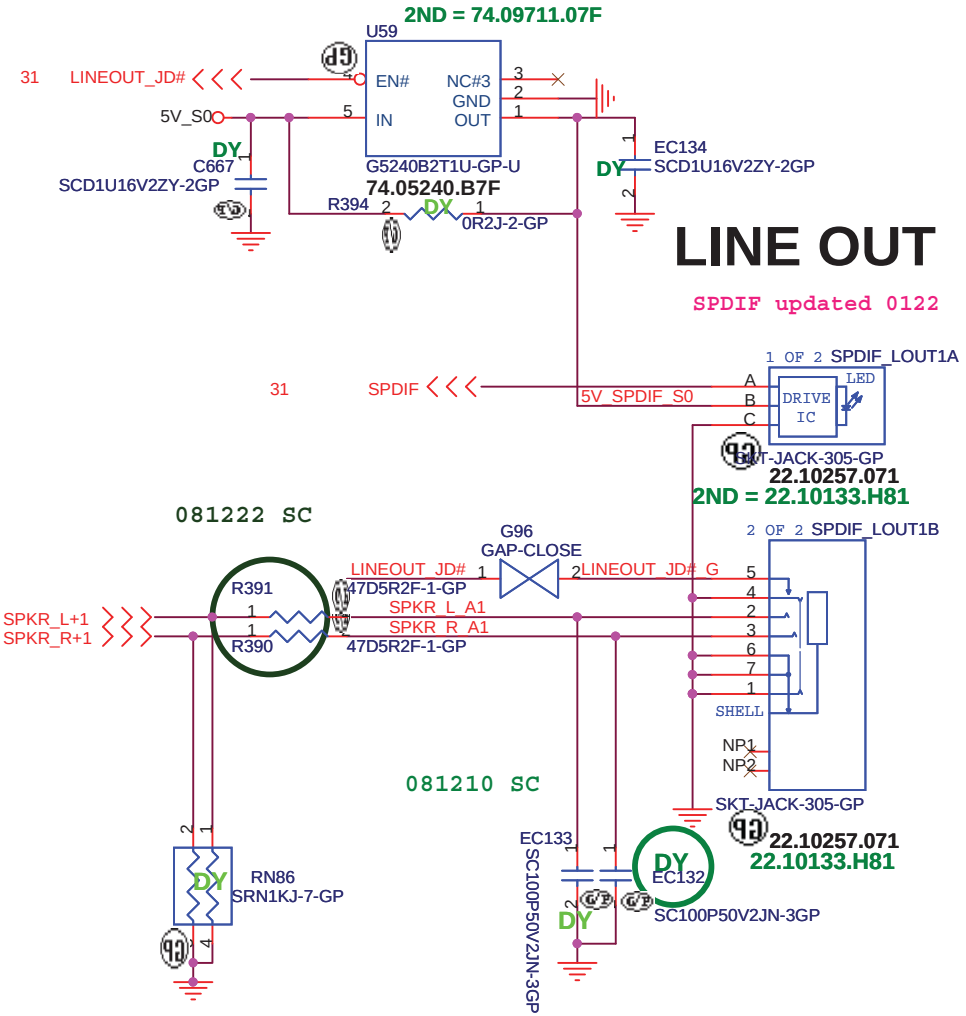


REAR Speaker



LINE OUT

SPDIF updated 0122



<Core Design>

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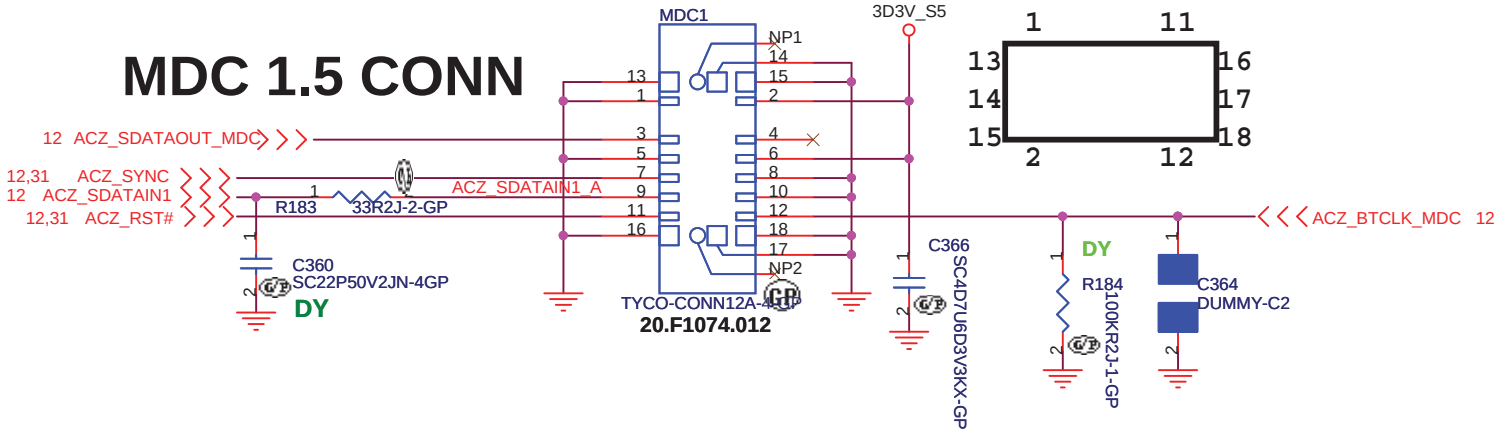
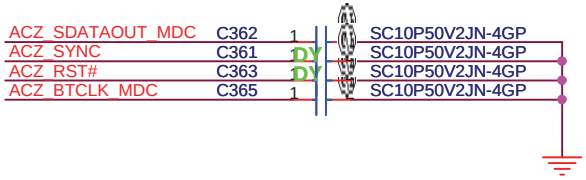
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 34 of 56	

MDC 1.5 CONN



090211 -1 EMI
Stuff C362,C365(10P)



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC		
Size: A4	Document Number: JM70-PU	Rev: -2
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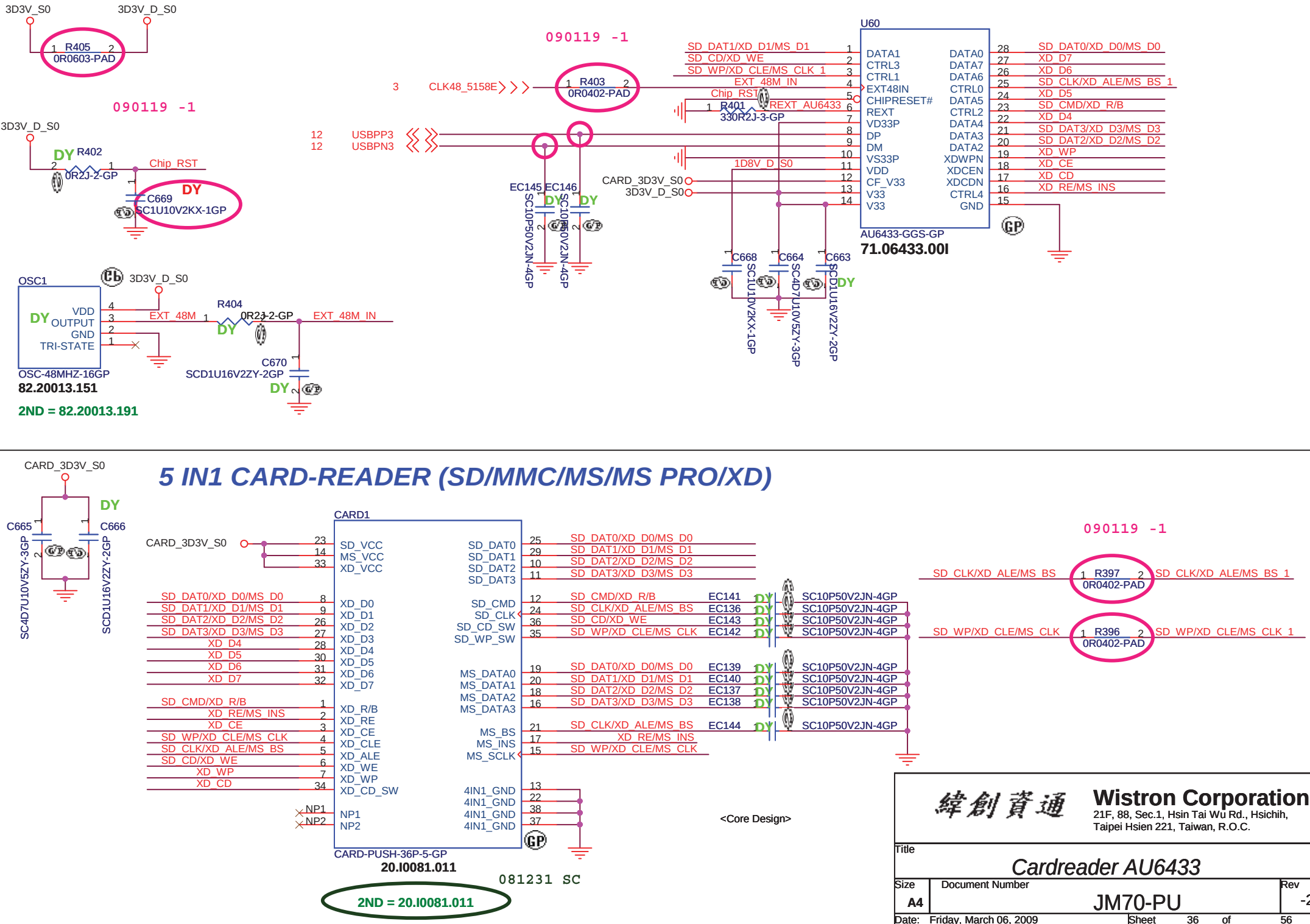
3D3V_S0
3D3V_D_S0
R405
0R0603-PAD
090119 -1
3D3V_D_S0
DY R402
0R2J-2-GP
Chip_RST
DY
C669
SC1U10V2KX-1GP
CLK48_5158E
R403
0R0402-PAD
USBPP3
USBPN3
SD_DAT1/XD_D1/MS_D1
SD_CD/XD_WE
SD_WP/XD_CLE/MS_CLK_1
EXT_48M_IN
Chip_RST
R401
330R2J-3-GP
REXT_AU6433
1D8V_D_S0
CARD_3D3V_S0
3D3V_D_S0
EC145 EC146
DY
SC10P50V2JN-4GP
U60
DATA1
CTRL3
CTRL1
EXT48IN
CHIPRESET#
REXT
VD33P
DP
DM
VS33P
VDD
CF_V33
V33
V33
DATA0
DATA7
DATA6
CTRL0
DATA5
CTRL2
DATA4
DATA3
DATA2
XDWPN
XDCEN
XDCDN
CTRL4
GND
SD_DAT0/XD_D0/MS_D0
XD_D7
XD_D6
SD_CLK/XD_ALE/MS_BS_1
XD_D5
SD_CMD/XD_R/B
XD_D4
SD_DAT3/XD_D3/MS_D3
SD_DAT2/XD_D2/MS_D2
XD_WP
XD_CE
XD_CD
XD_RE/MS_INS
AU6433-GGS-GP
71.06433.00I
C668
SC1U10V2KX-1GP
C664
SC4D7U10V5ZY-3GP
C663
DY
SCD1U16V2ZY-2GP
OSC1
DY
VDD
OUTPUT
GND
TRI-STATE
OSC-48MHZ-16GP
82.20013.151
2ND = 82.20013.191
3D3V_D_S0
R404
0R2J-2-GP
EXT_48M
EXT_48M_IN
C670
SCD1U16V2ZY-2GP
DY
CARD_3D3V_S0
DY
C665
C666
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)
CARD1
CARD_3D3V_S0
SD_VCC
MS_VCC
XD_VCC
SD_DAT0/XD_D0/MS_D0
SD_DAT1/XD_D1/MS_D1
SD_DAT2/XD_D2/MS_D2
SD_DAT3/XD_D3/MS_D3
XD_D4
XD_D5
XD_D6
XD_D7
SD_CMD/XD_R/B
XD_RE/MS_INS
XD_CE
SD_WP/XD_CLE/MS_CLK
SD_CLK/XD_ALE/MS_BS
SD_CD/XD_WE
XD_WP
XD_CD
NP1
NP2
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_CD_SW
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_CD_SW
SD_WP_SW
MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3
MS_BS
MS_INS
MS_SCLK
4IN1_GND
CARD-PUSH-36P-5-GP
20.I0081.011
081231 SC
2ND = 20.I0081.011
EC141
EC136
EC143
EC142
EC139
EC140
EC137
EC138
EC144
SC10P50V2JN-4GP
090119 -1
SD_CLK/XD_ALE/MS_BS
R397
0R0402-PAD
SD_CLK/XD_ALE/MS_BS_1
SD_WP/XD_CLE/MS_CLK
R396
0R0402-PAD
SD_WP/XD_CLE/MS_CLK_1
<Core Design>
綽創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cardreader AU6433
Size
A4
Document Number
JM70-PU
Rev
-2
Date: Friday, March 06, 2009
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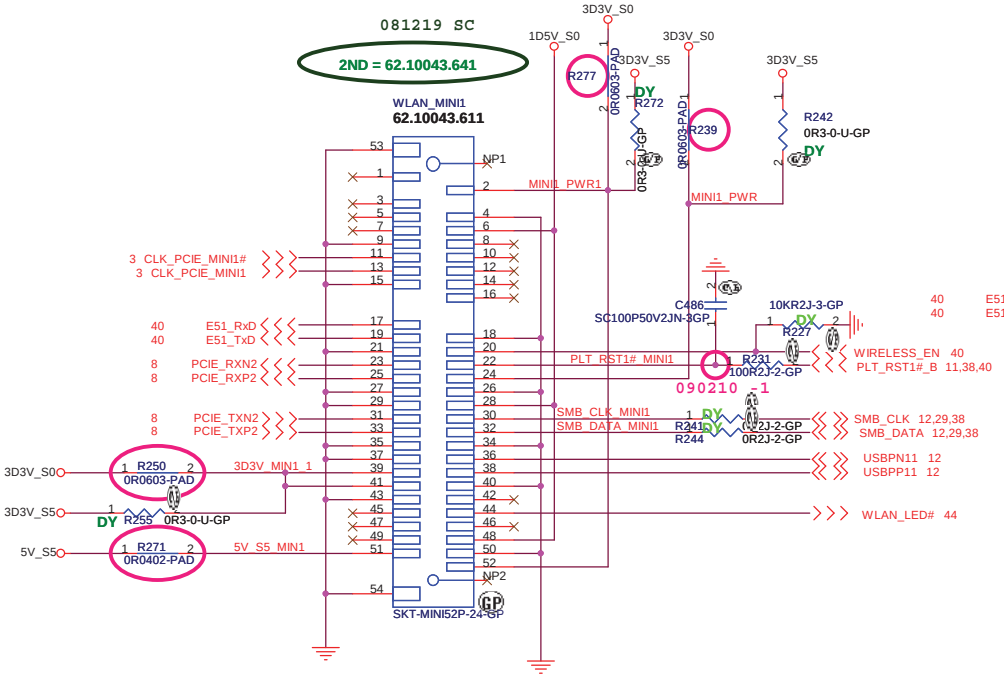
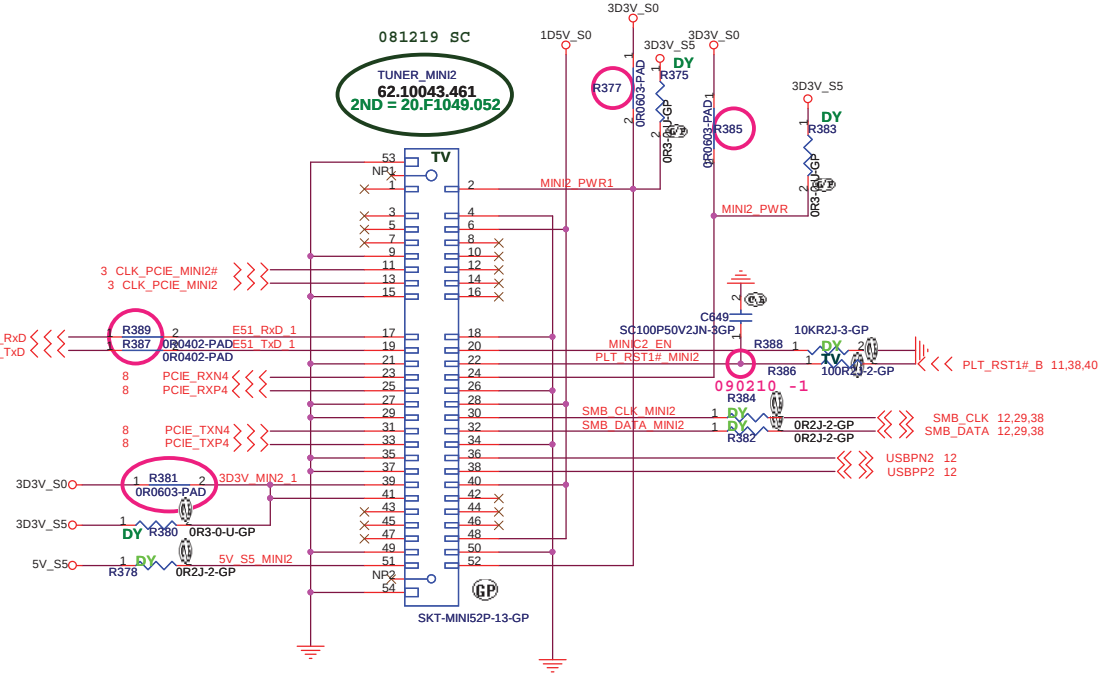
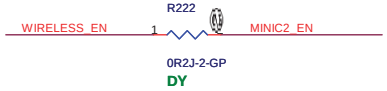
Mini1 Card Connector(WLAN)
Support debug-card

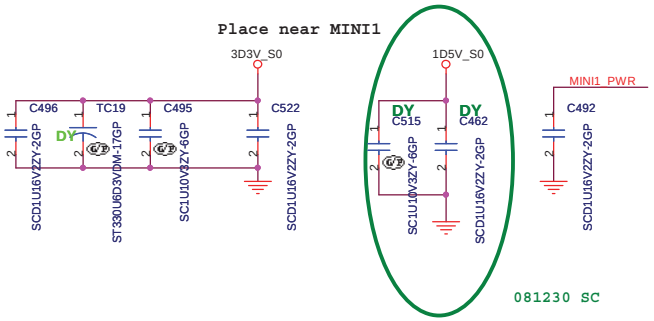
090119 -1

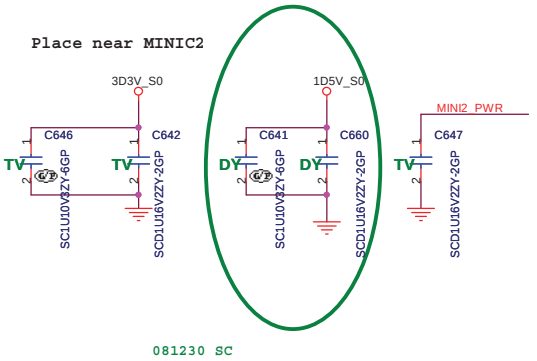


Mini2 Card Connector(TV tuner)









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Title: Mini Card

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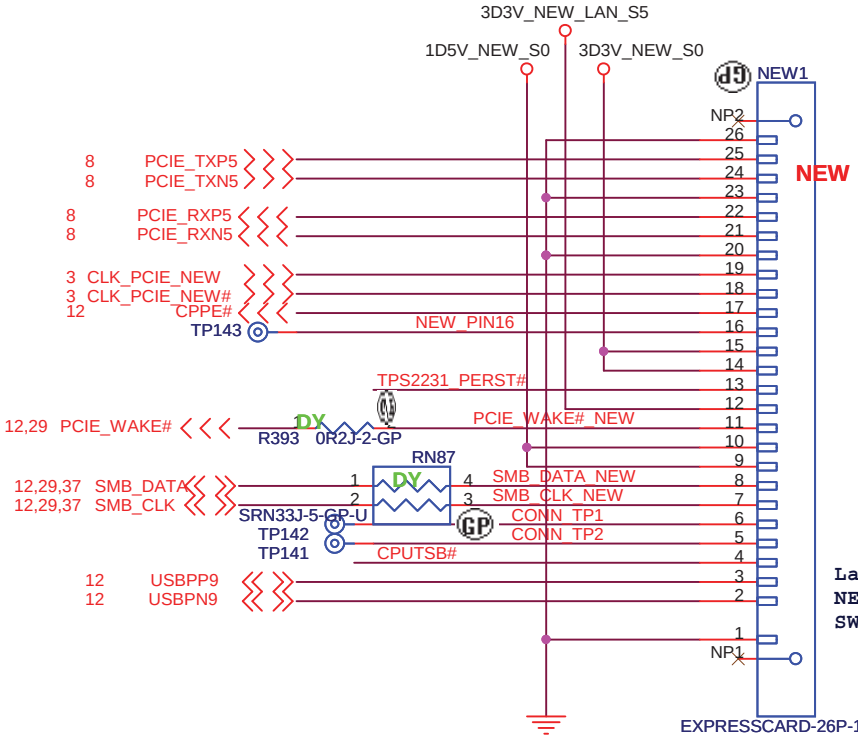
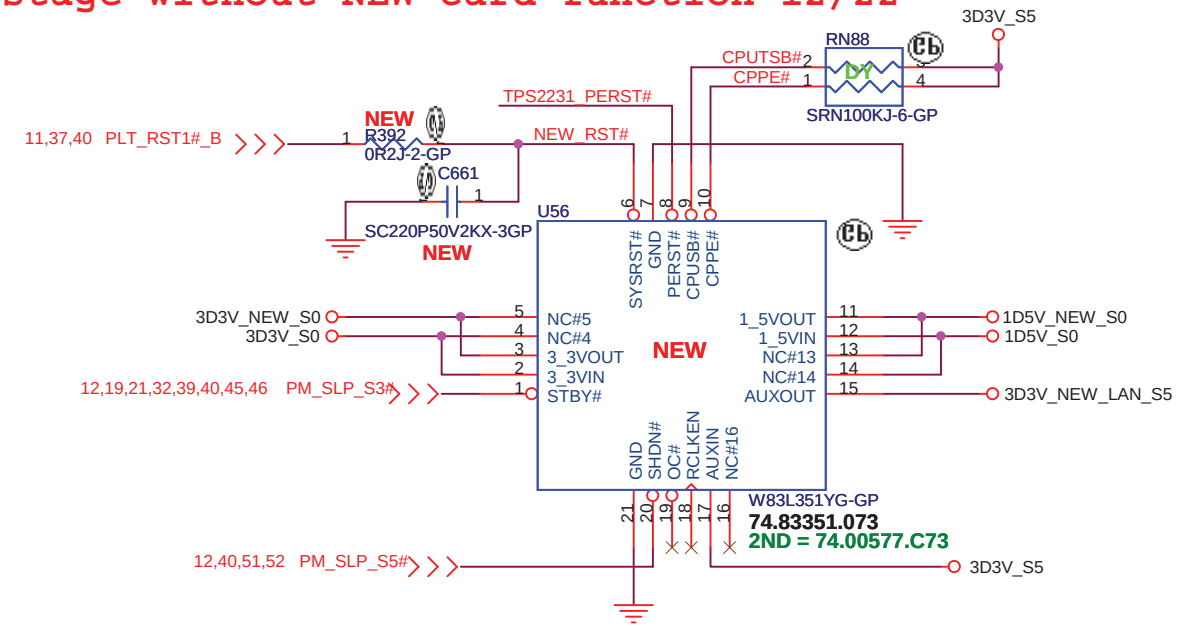
NEWCARD Connector

ENG stage without NEW card function 12/22

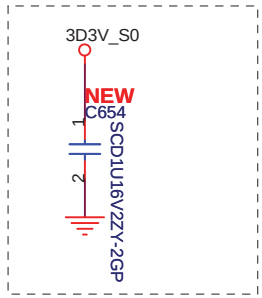




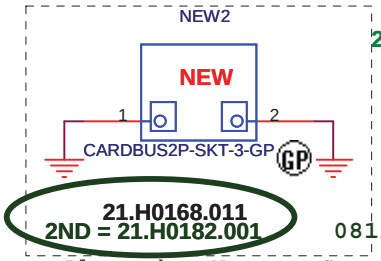
Layout Request 1226
NEW1 & NEW2
SWAP 1st & 2nd

74.00577.C73
new card power switch
GMT cost down solution

Place them Near to Chip



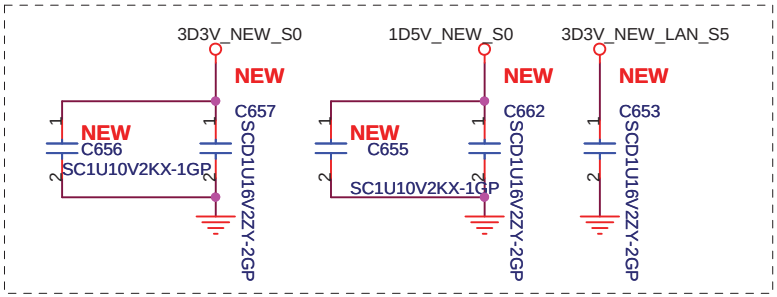
TOP VIEW



62.10081.151 081219 SC
2ND = 62.10081.131

21.H0168.011
2ND = 21.H0182.001 081219 SC

Place them Near to Connector



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **NEW CARD**		
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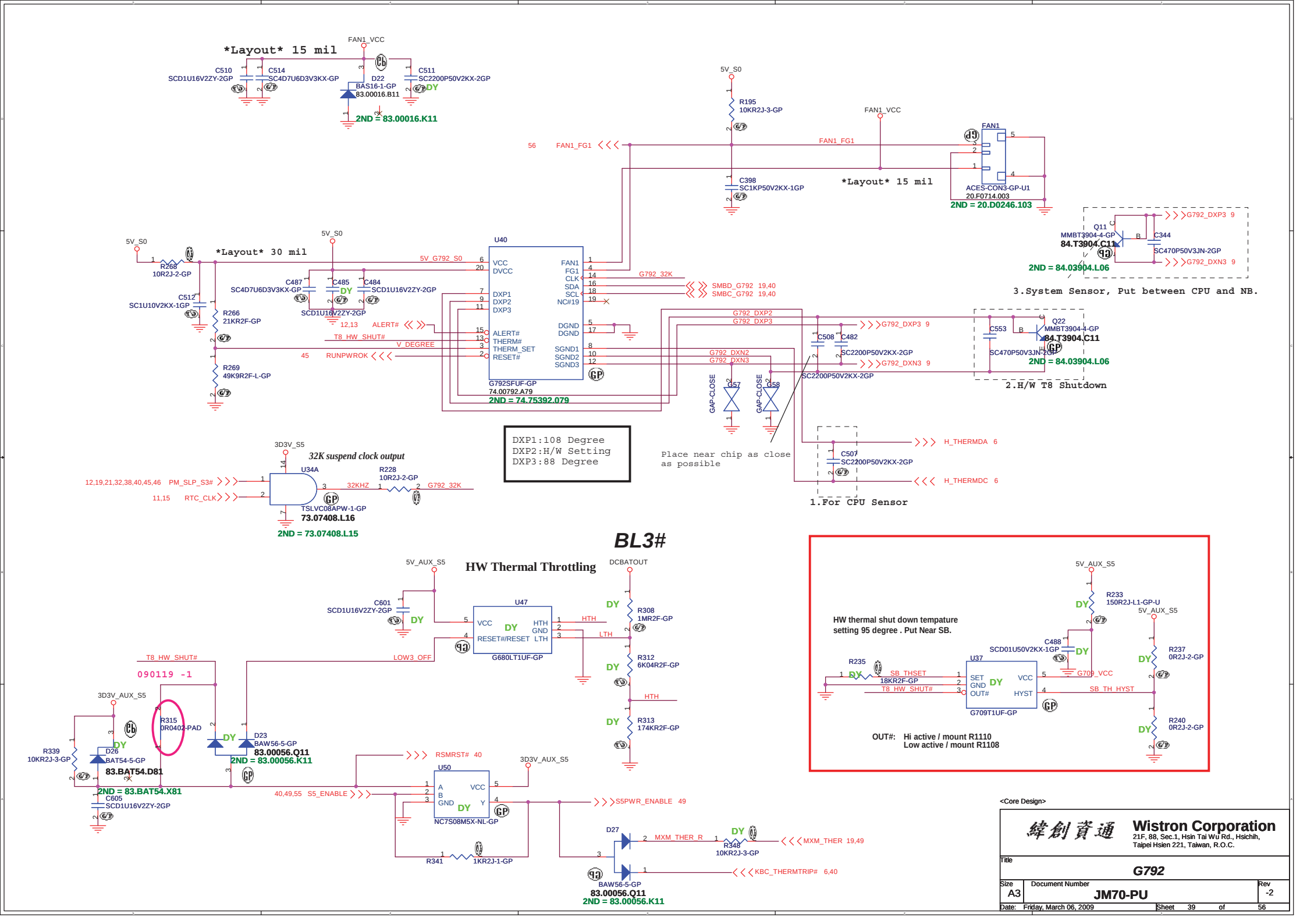

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Taipei Hsien 221, Taiwan, R.O.C.

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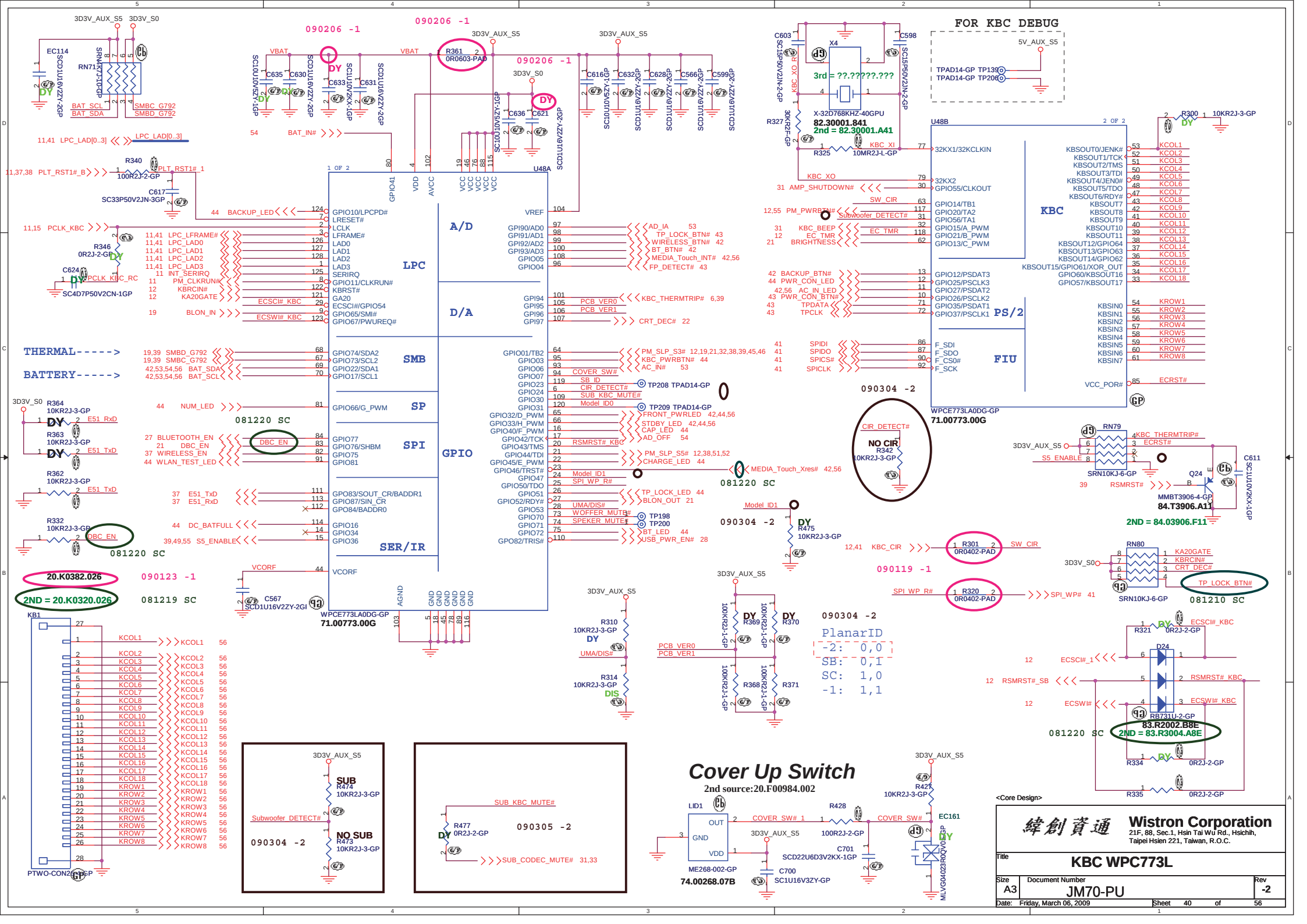
FOR KBC DEBUG
U48A
U48B
KBC
PS/2
FIU
GPIO
A/D
LPC
D/A
SMB
SP
SPI
SER/IR
THERMAL----->
BATTERY----->
Cover Up Switch
2nd source:20.F00984.002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
JM70-PU
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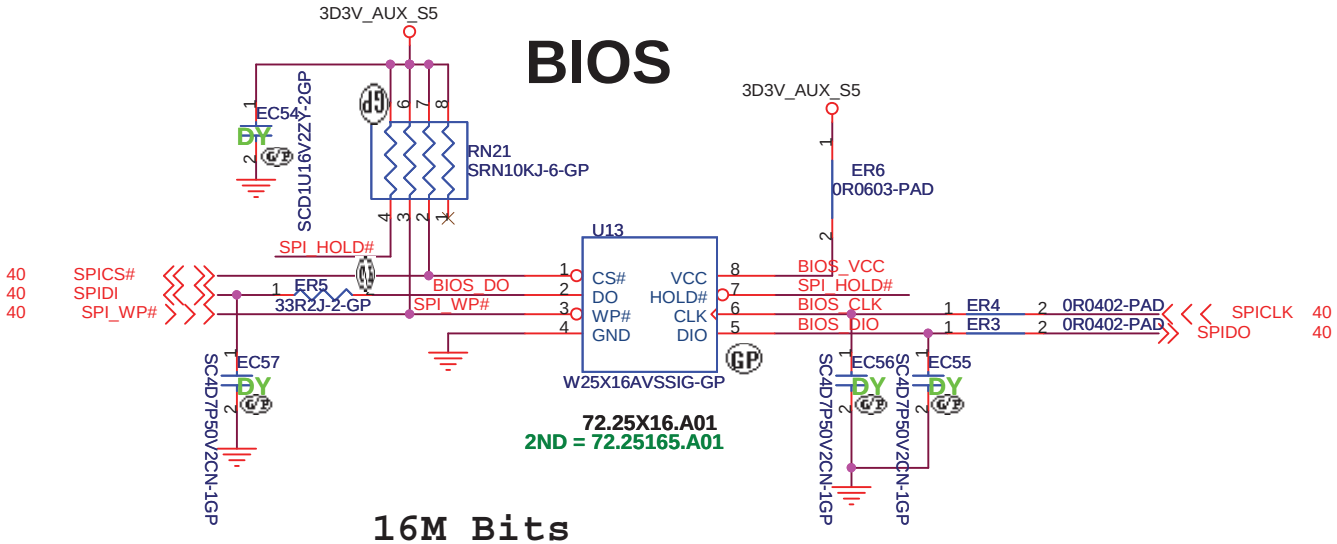
<Core Design>

BIOS

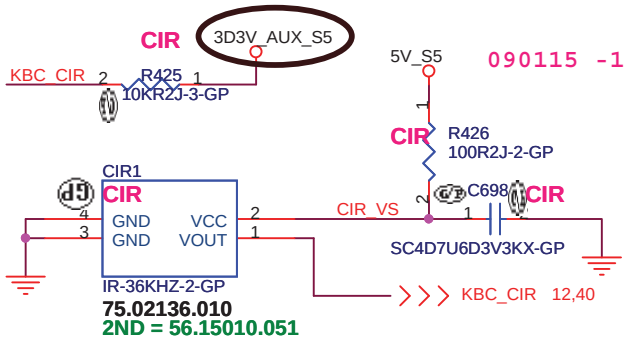


16M Bits

SPI FLASH ROM

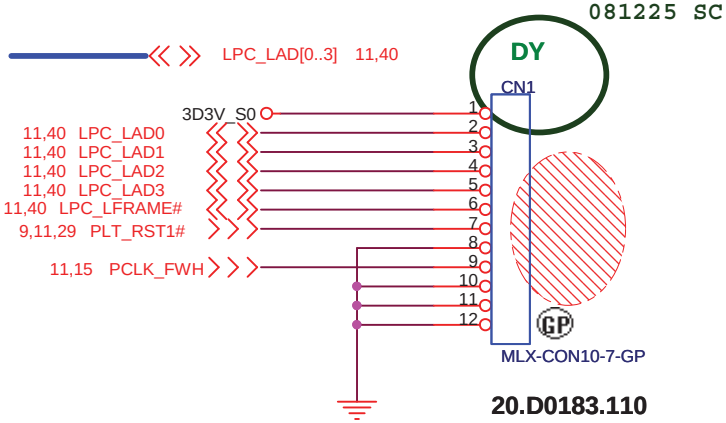
CIR Module

090304 -2



GOLDEN FINGER FOR DEBUG BOARD

081225 SC



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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS & CIR

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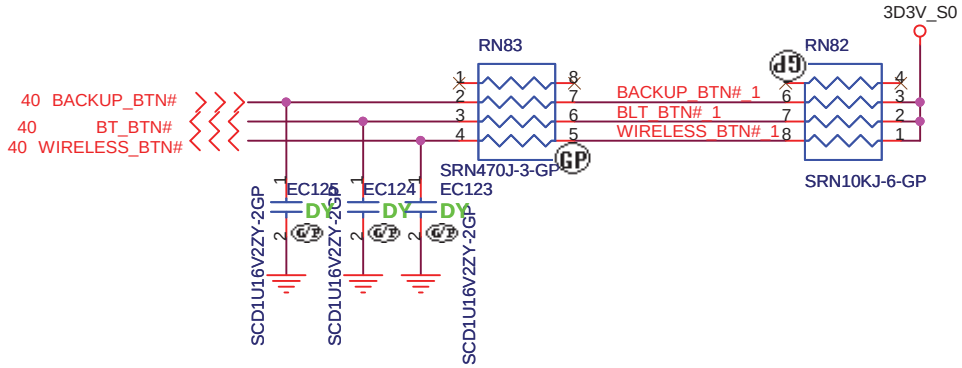
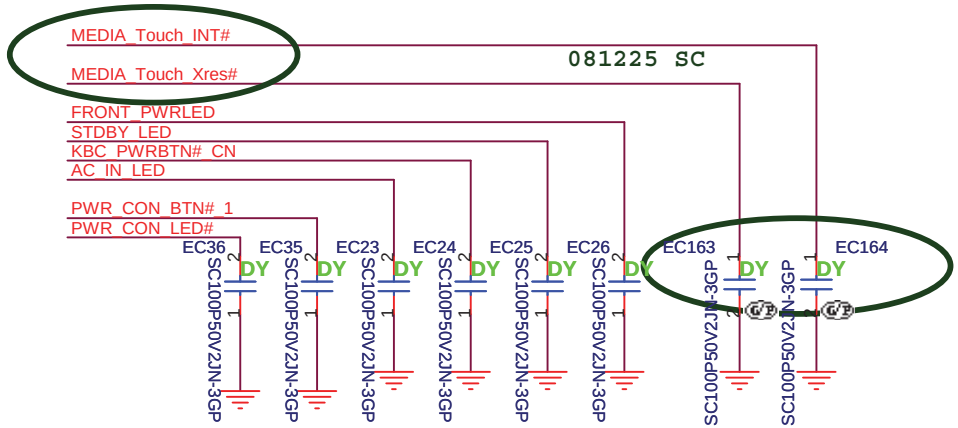
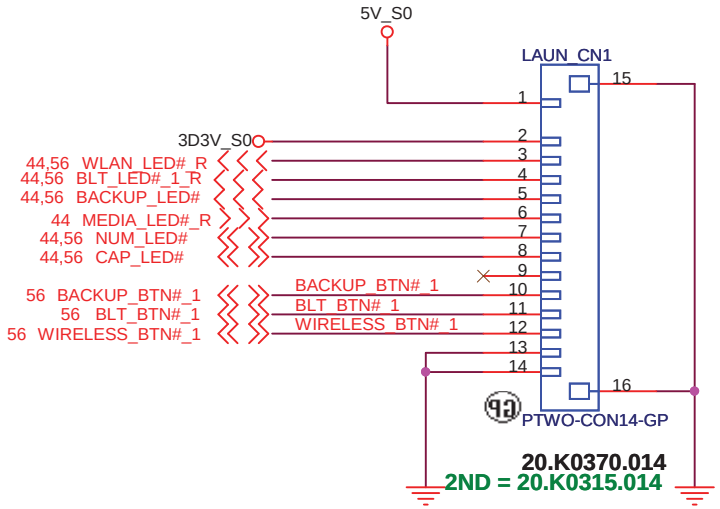
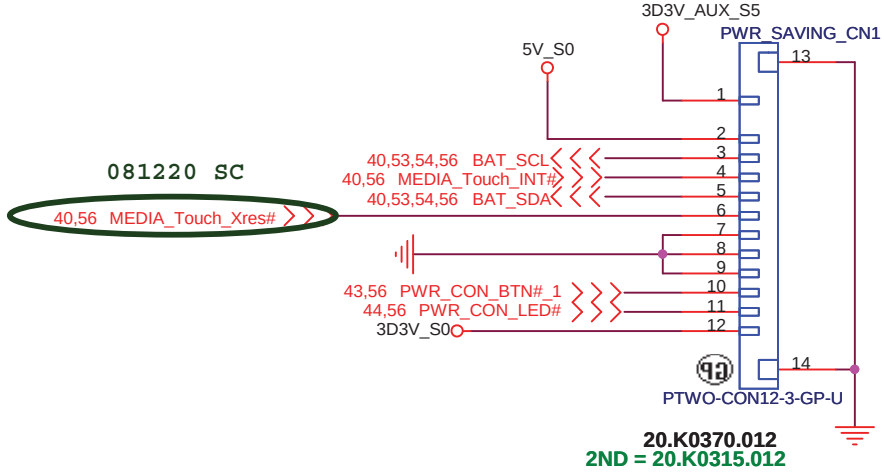
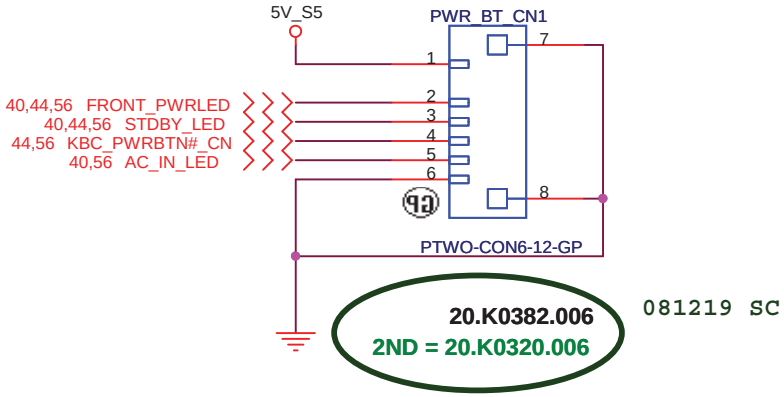
LAUNCH











<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	LAUNCH & LID	
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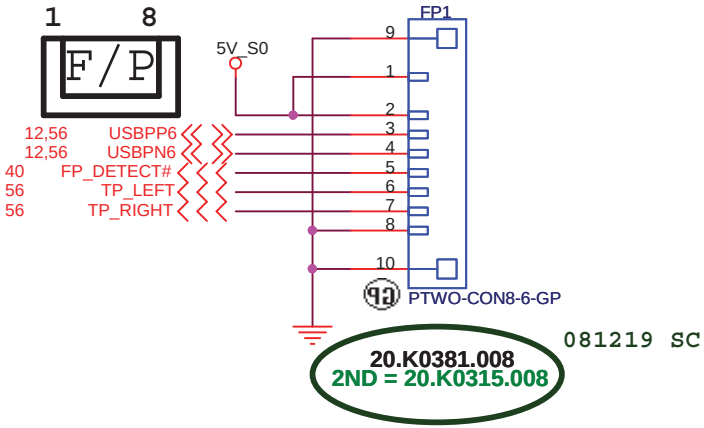
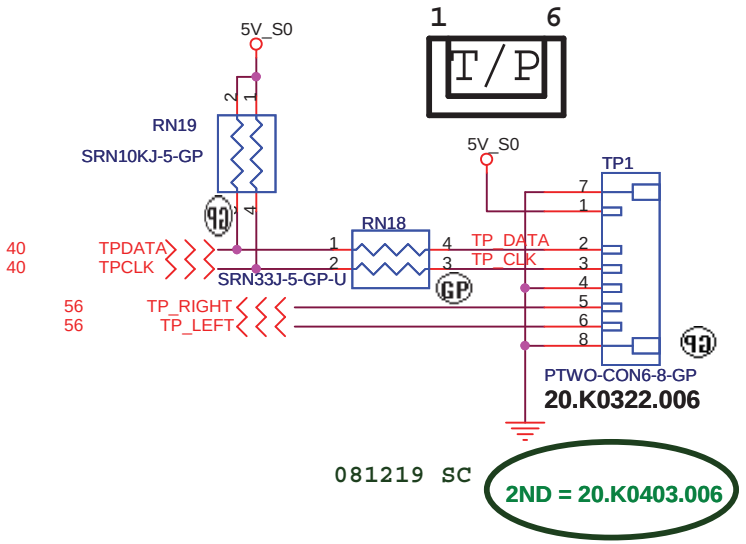
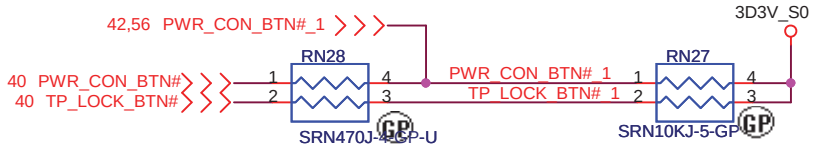
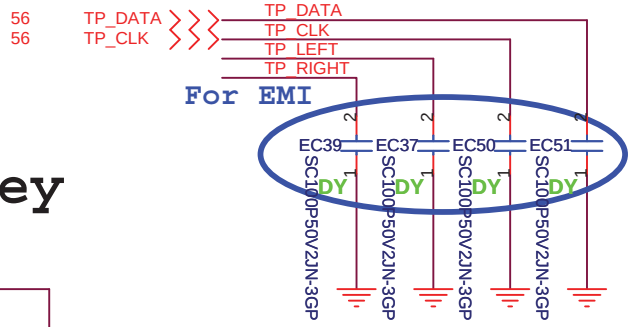
Finger printer



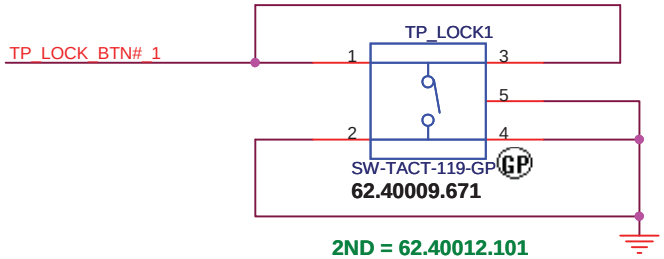
TOUCH PAD







TP_LOCK key



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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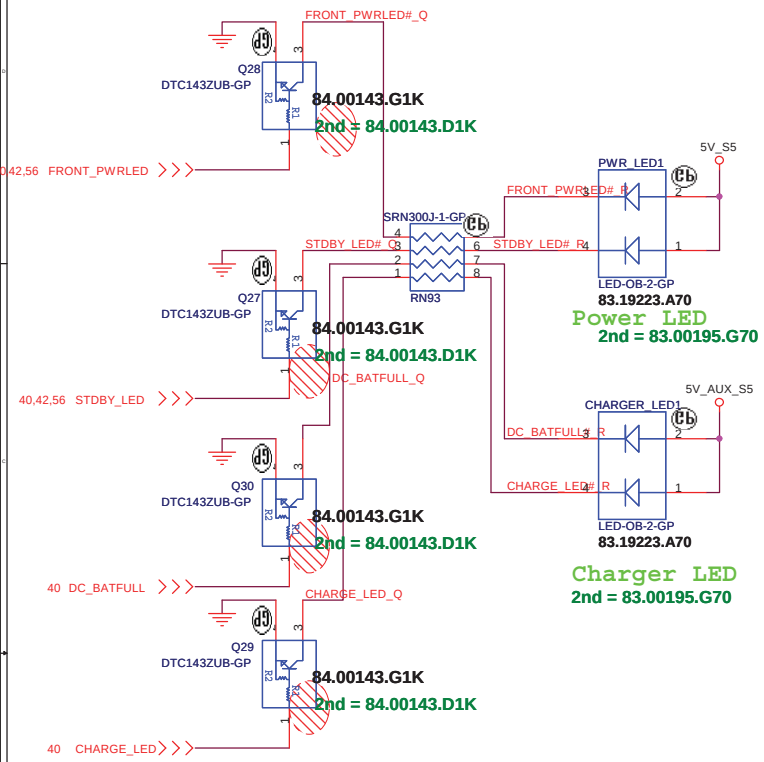
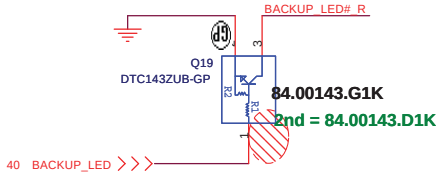
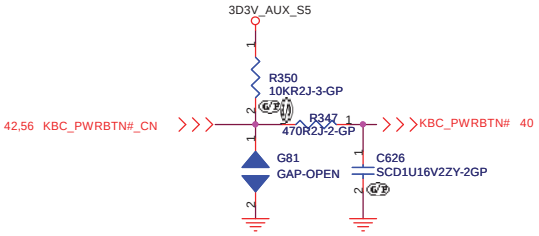
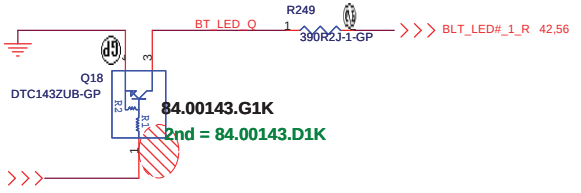
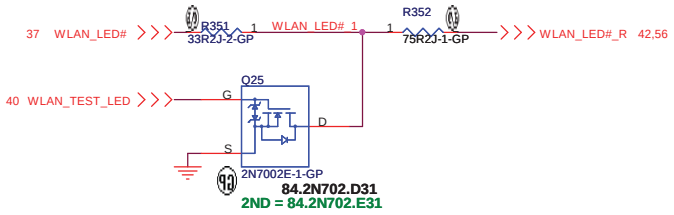
LED

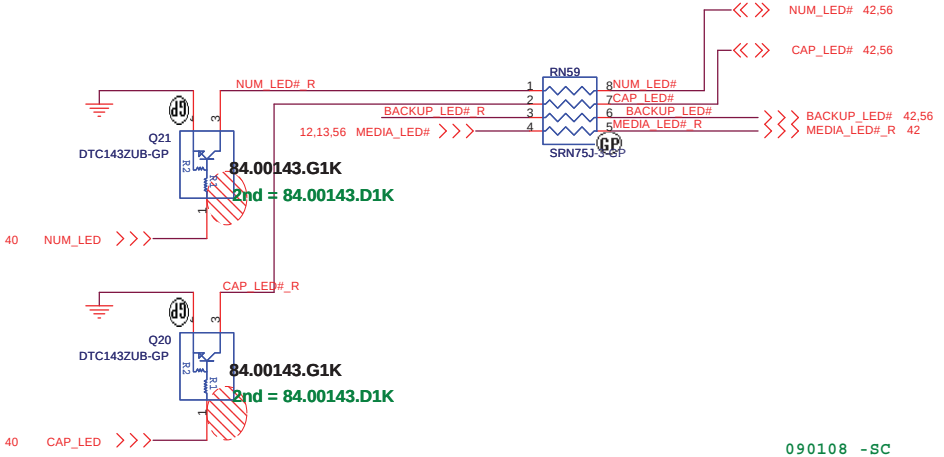


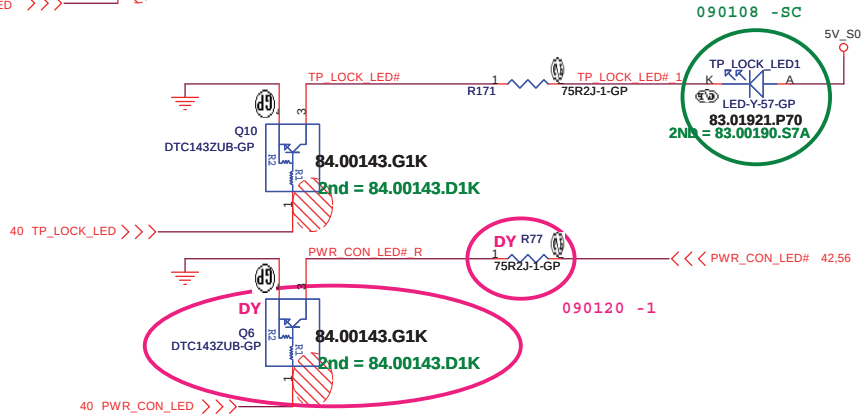












緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED & LAUNCH	
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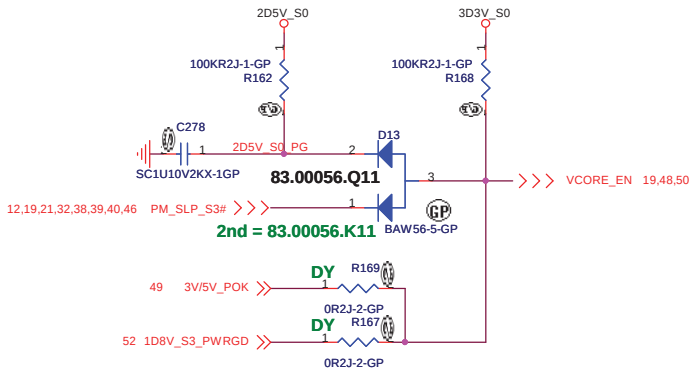
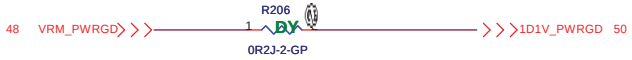
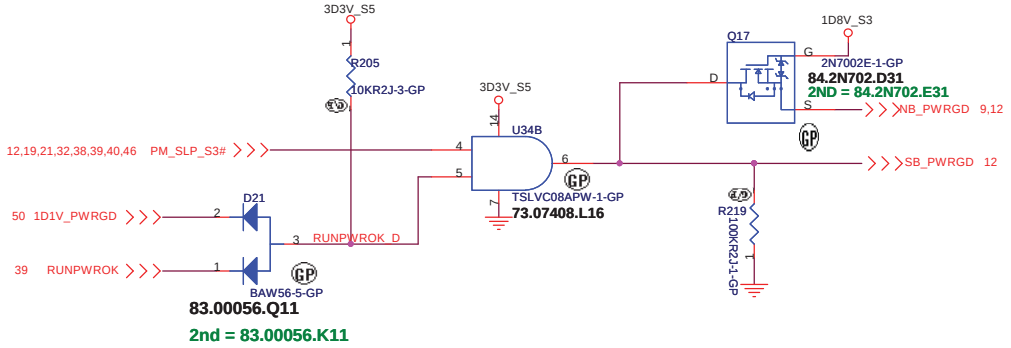


P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON LOGIC***

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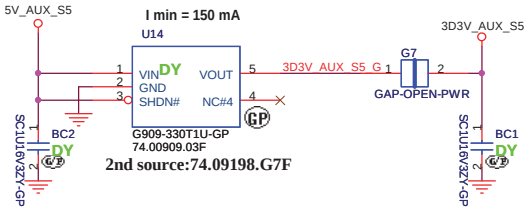
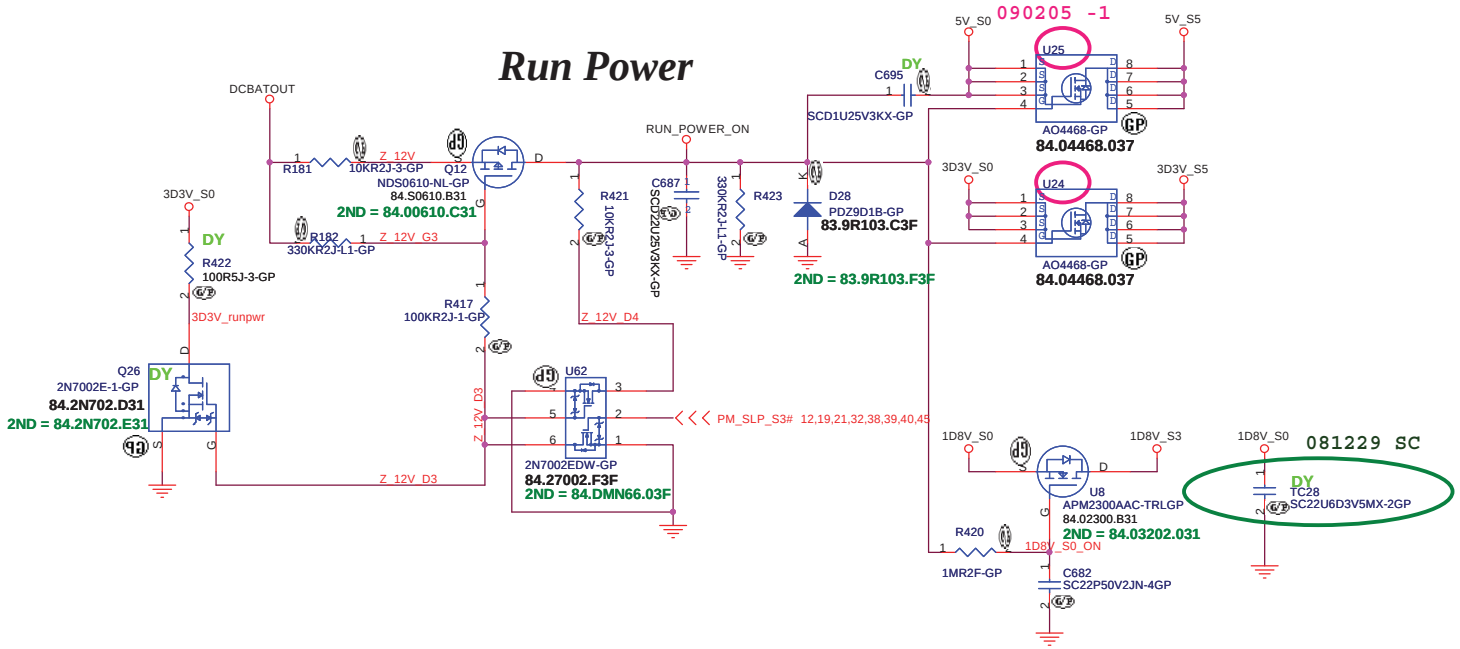
Aux Power

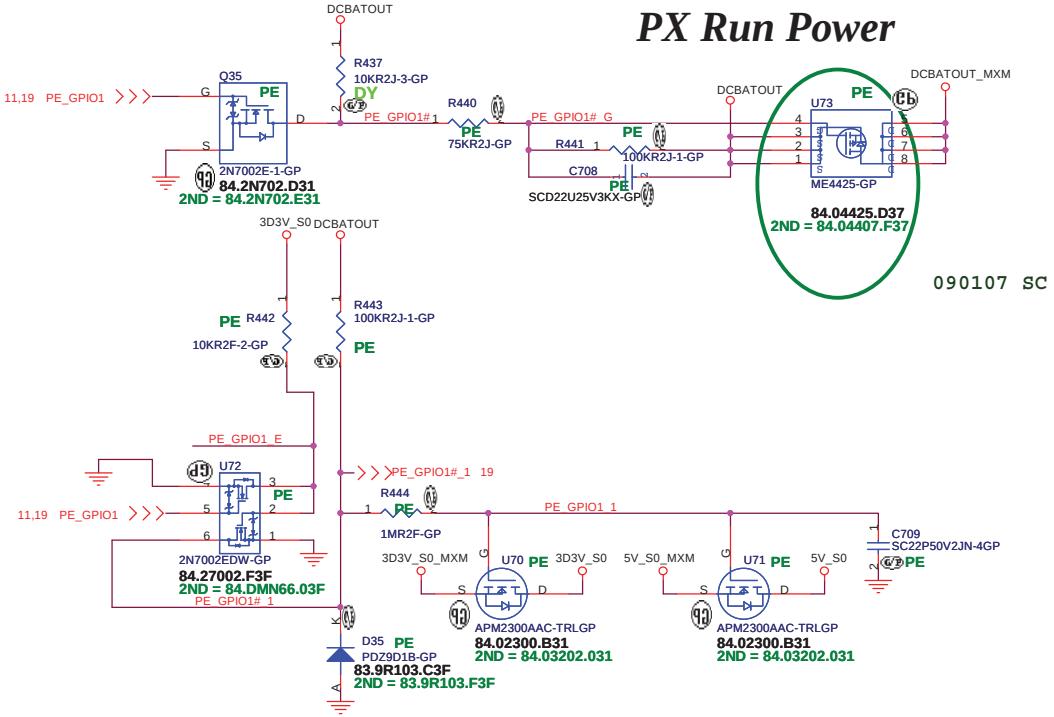
3D3V_AUX_S5



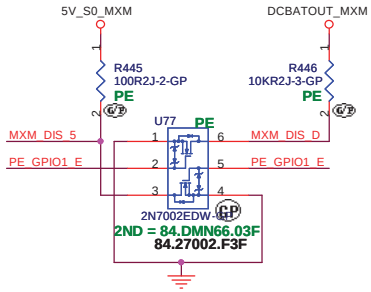
Run Power



PX Run Power



PX Run Power Discharge circuit



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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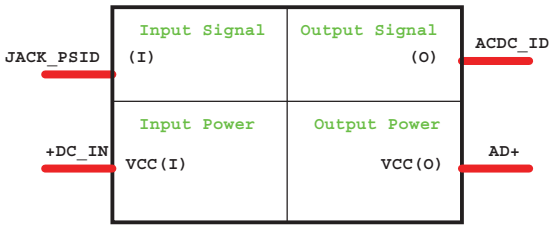
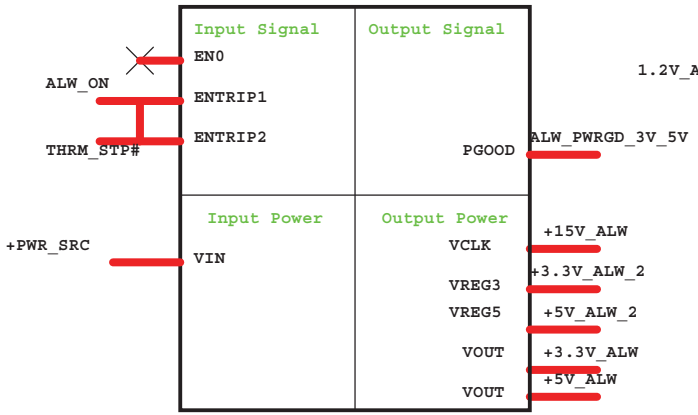
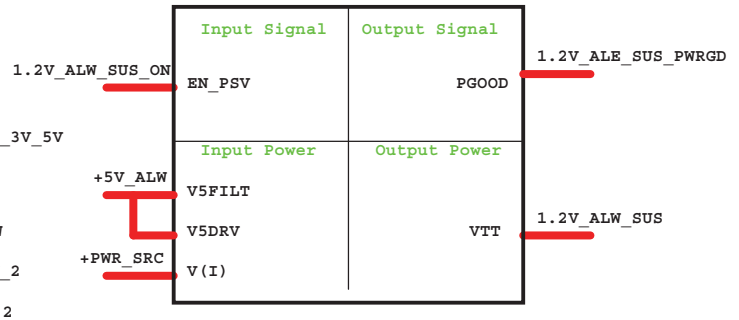
Adapter



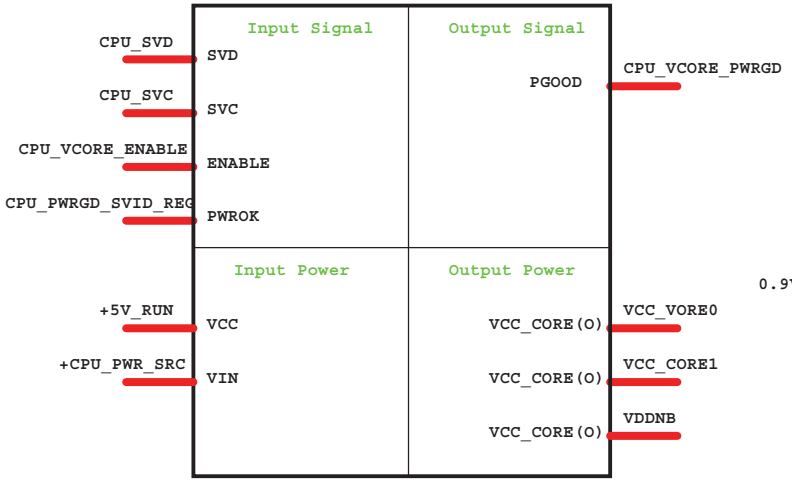
SN0608098



DCDC 1D2V(TPS5117)

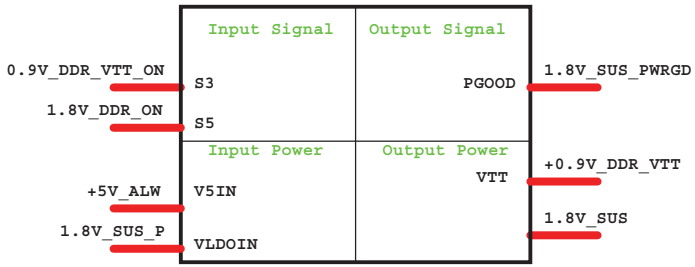


CPU_CORE
ISL6265HRTZ

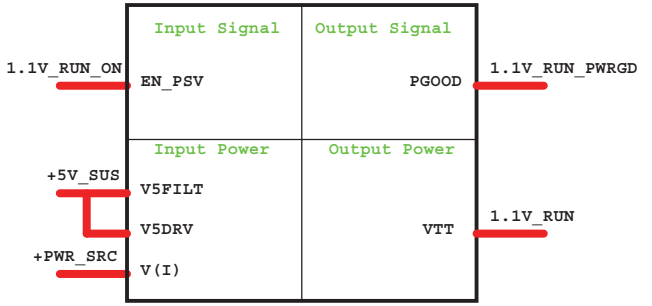


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

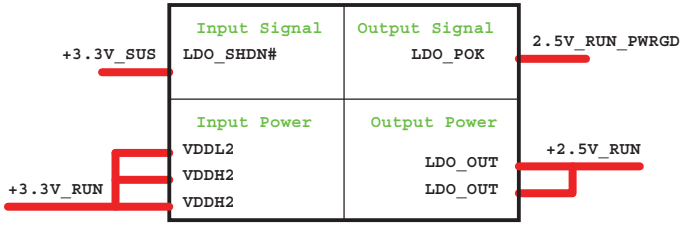
1D8V/0D9V(TPS5116)



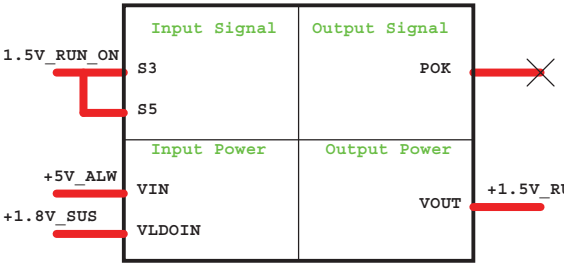
1D1V(TPS5117)



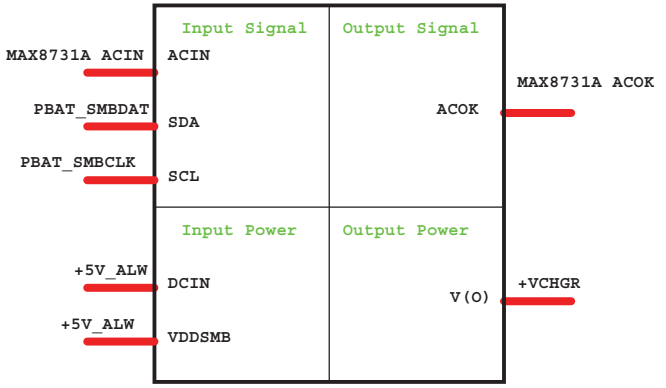
2.5V LDO
EMC4002



1.5V_LDO



CHARGER BQ24745



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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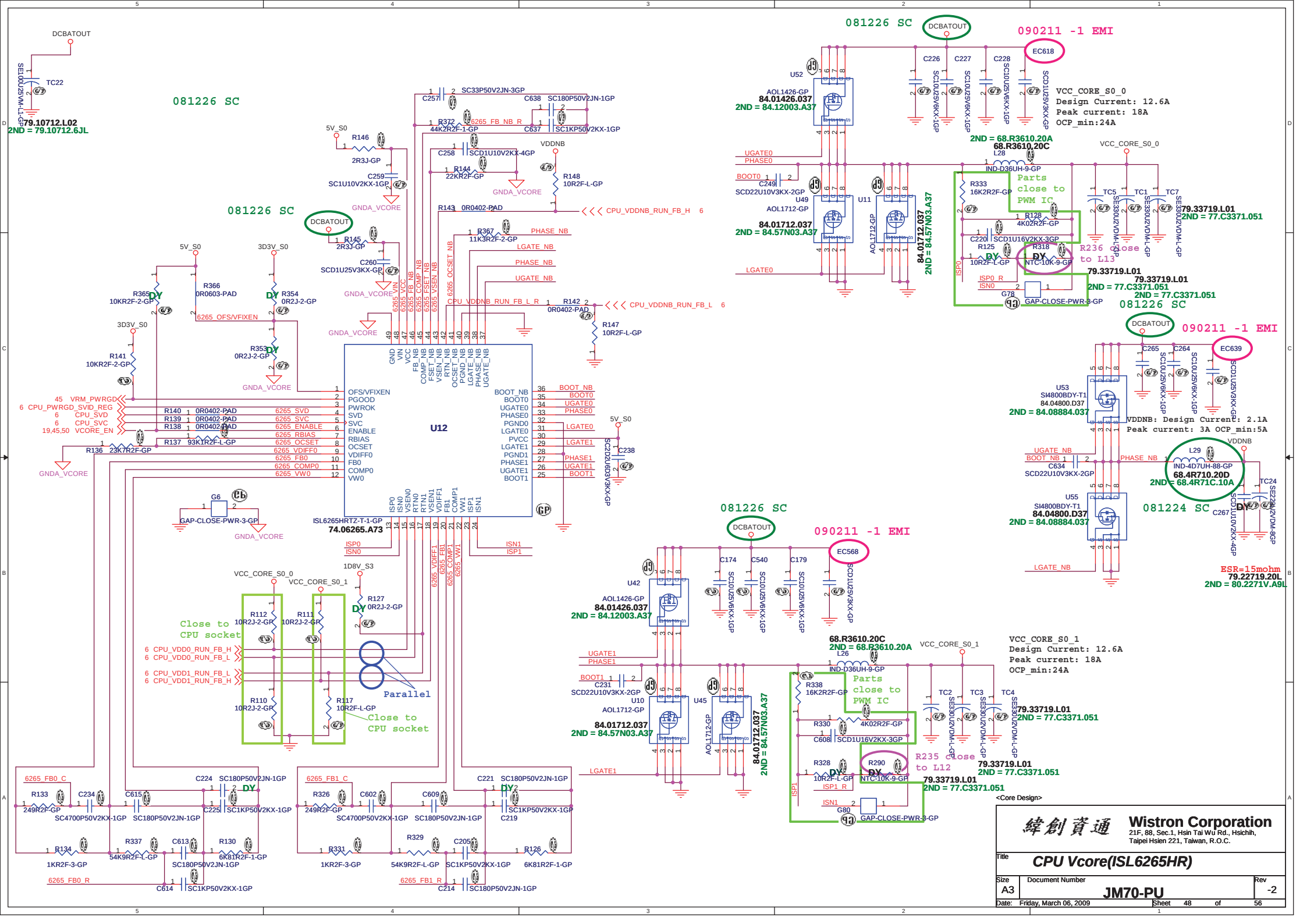
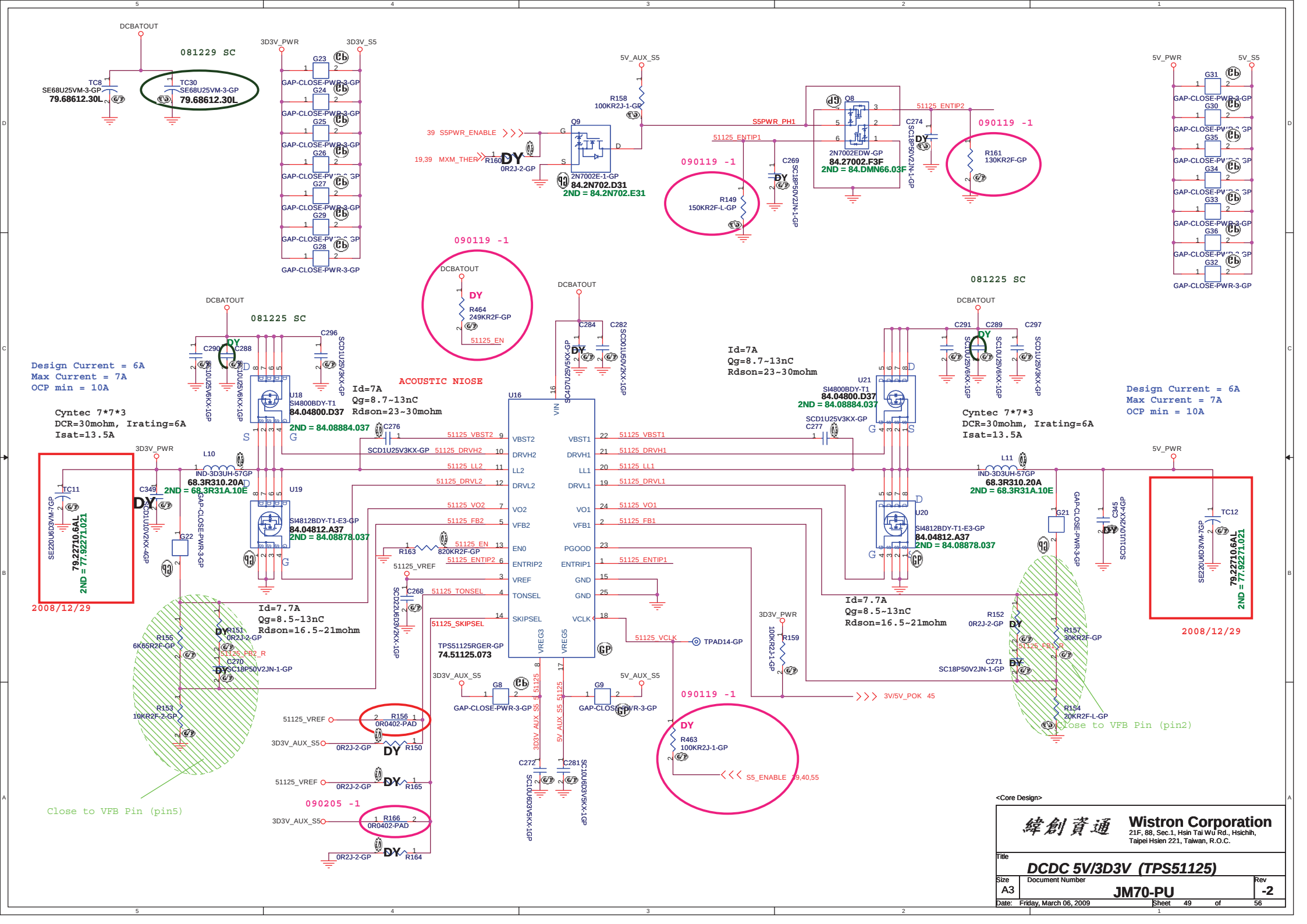

081226 SC
090211 -1 EMI
DCBATOUT
U12
ISL6265HRTZ-T-1-GP
74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
Parts close to PWM IC
R236 Close to L13
R235 close to L12
Close to CPU socket
Parallel
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
081224 SC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JM70-PU
Date: Friday, March 06, 2009
Sheet 48 of 56


DCBATOUT
081229 SC
TC8
SE68U25VM-3-GP
79.68612.30L
TC30
SE68U25VM-3-GP
79.68612.30L
3D3V_PWR
3D3V_S5
G23
G24
G25
G26
G27
G29
G28
GAP-CLOSE-PWR-3-GP
5V_AUX_S5
R158
100KR2J-1-GP
39 S5PWR_ENABLE
19,39 MXM_THER
R160
0R2J-2-GP
Q9
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
S5PWR_PH1
Q8
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
51125_ENTIP1
51125_ENTIP2
C274
SC18P50V2JN-1-GP
090119 -1
R161
130KR2F-GP
R149
150KR2F-L-GP
C269
SC18P50V2JN-1-GP
5V_PWR
5V_S5
G31
G30
G35
G34
G33
G36
G32
090119 -1
DCBATOUT
R464
249KR2F-GP
51125_EN
081225 SC
DCBATOUT
C290
C288
C296
SCD1U25V3KX-GP
SCD10U25V6KX-1GP
U18
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
ACOUSTIC NIOSE
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
C276
SCD1U25V3KX-GP
U16
TPS51125RGER-GP
74.51125.073
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_ENTIP1
51125_VCLK
TPAD14-GP
SCD47U25V5KX-GP
SCD01U50V2KX-1GP
SCD22U6D3V2KX-1GP
3D3V_PWR
L10
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
C349
SCD1U10V2KX-4GP
U19
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
TC11
SE220U6D3VM-7GP
79.22710.6AL
2ND = 77.92271.021
2008/12/29
G22
GAP-CLOSE-PWR-3-GP
R163
820KR2F-GP
C268
R155
6K65R2F-GP
R151
0R2J-2-GP
C270
SC18P50V2JN-1-GP
R153
10KR2F-2-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
R156
0R0402-PAD
R150
0R2J-2-GP
R165
0R2J-2-GP
090205 -1
R166
0R0402-PAD
R164
0R2J-2-GP
G8
G9
3D3V_AUX_S5
5V_AUX_S5
C272
C281
SC10U6D3V5KX-1GP
090119 -1
R463
100KR2J-1-GP
S5_ENABLE 19,40,55
3V/5V_POK 45
R159
100KR2J-1-GP
081225 SC
DCBATOUT
C291
C289
C297
SCD10U25V6KX-1GP
SCD1U25V3KX-GP
U21
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
SCD1U25V3KX-GP
C277
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Design Current = 6A
Max Current = 7A
OCP min = 10A
L11
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
U20
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
G21
GAP-CLOSE-PWR-3-GP
C345
SCD1U10V2KX-4GP
TC12
SE220U6D3VM-7GP
79.22710.6AL
2ND = 77.92271.021
2008/12/29
R152
0R2J-2-GP
51125_FB1_R
R157
30KR2F-GP
C271
SC18P50V2JN-1-GP
R154
20KR2F-L-GP
Close to VFB Pin (pin2)
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size
A3
Document Number
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-2
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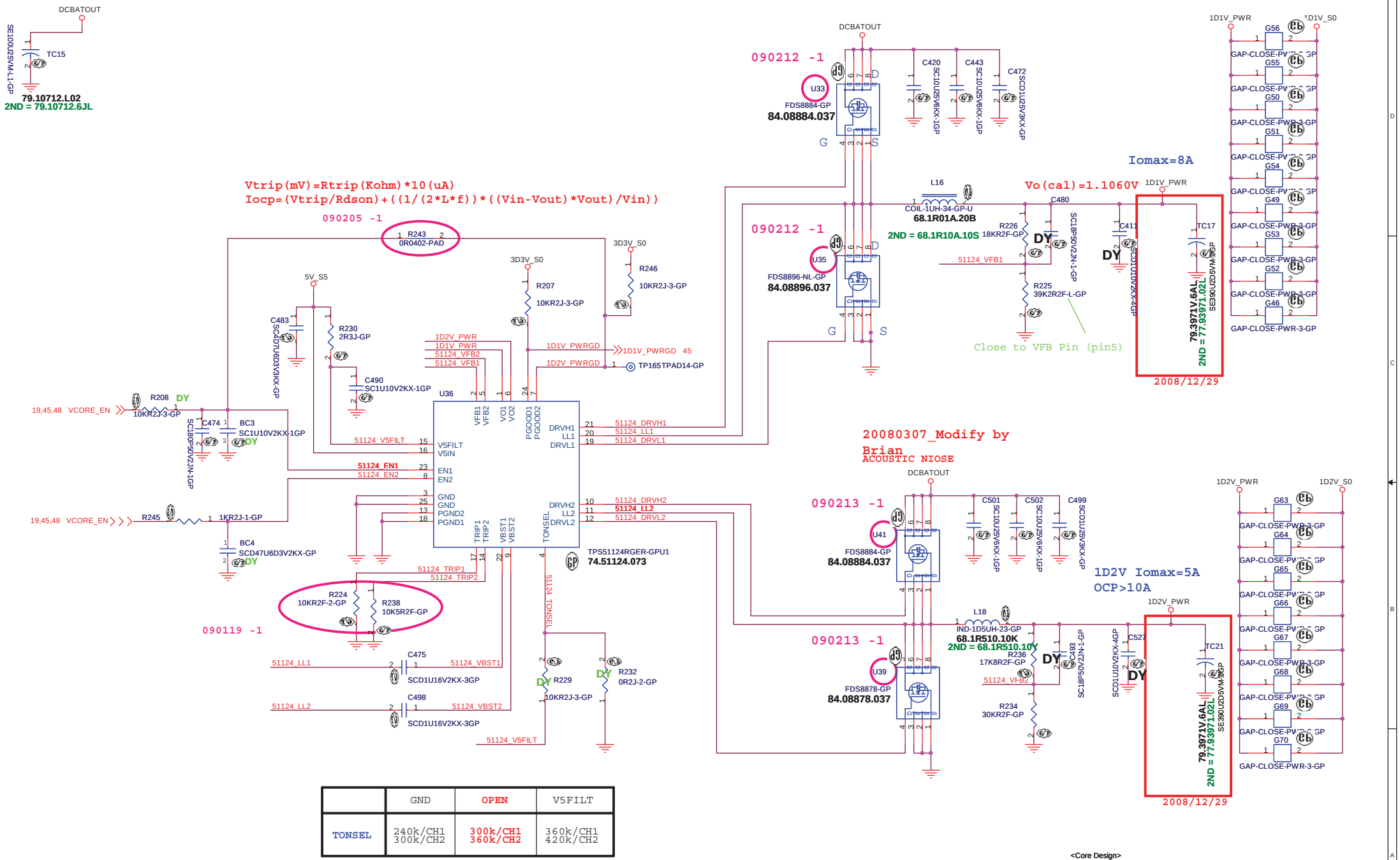

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

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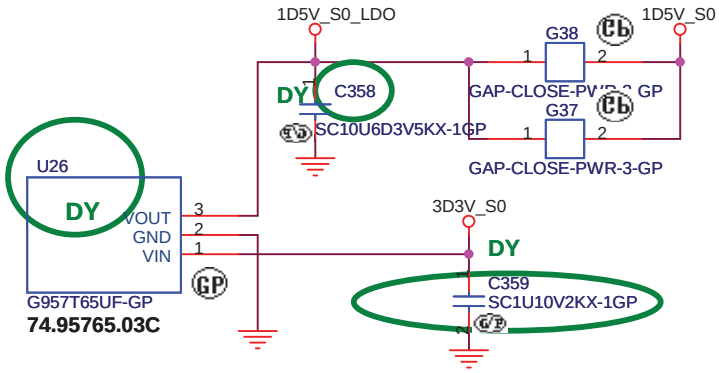
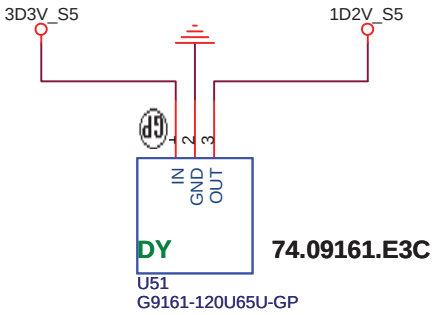
G957

1D5V_S0
Iomax=1A

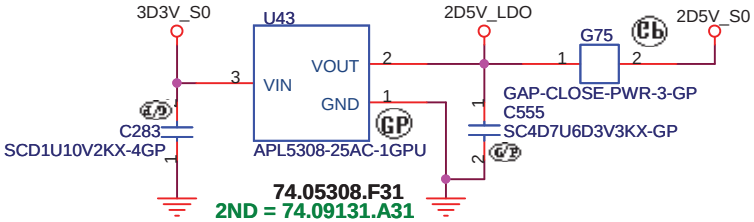


081230 SC

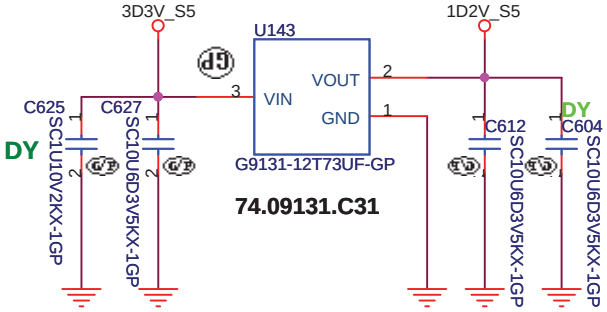
1D2V_S5
Iomax=400mA

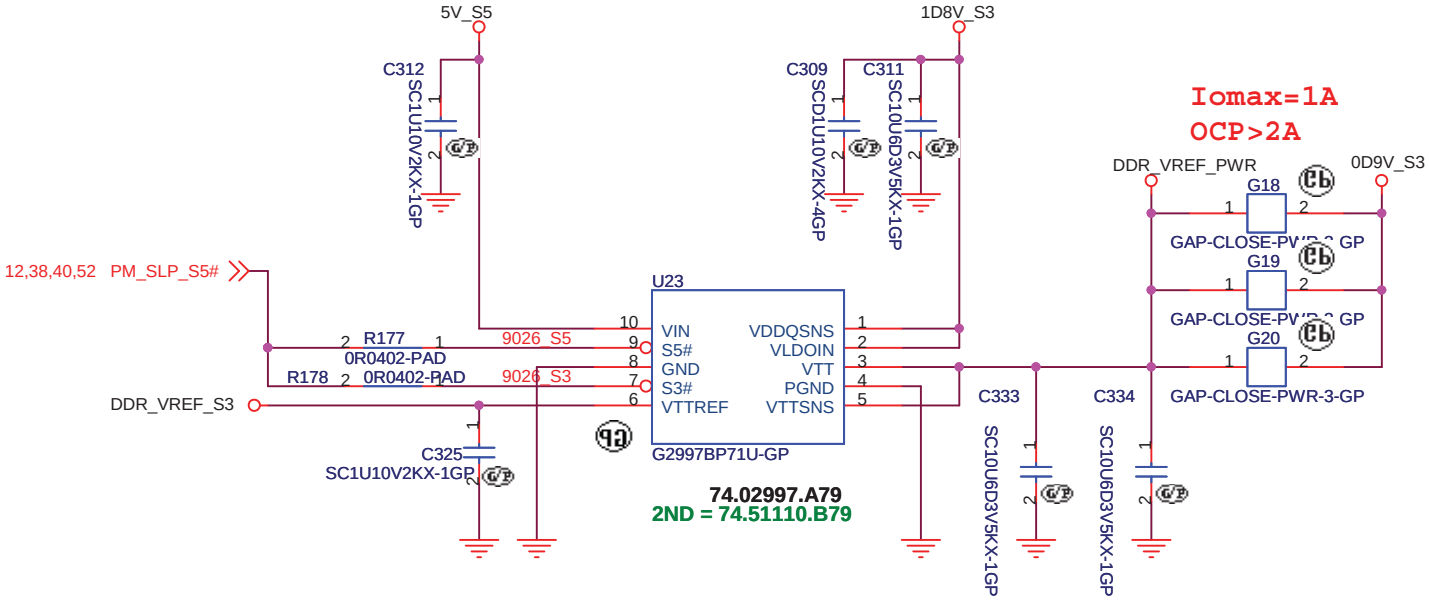


2D5V_S0
Iomax=0.3A 2D5V/300mA



Place near to SB700





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V&2D5V&1D25V&1D5V

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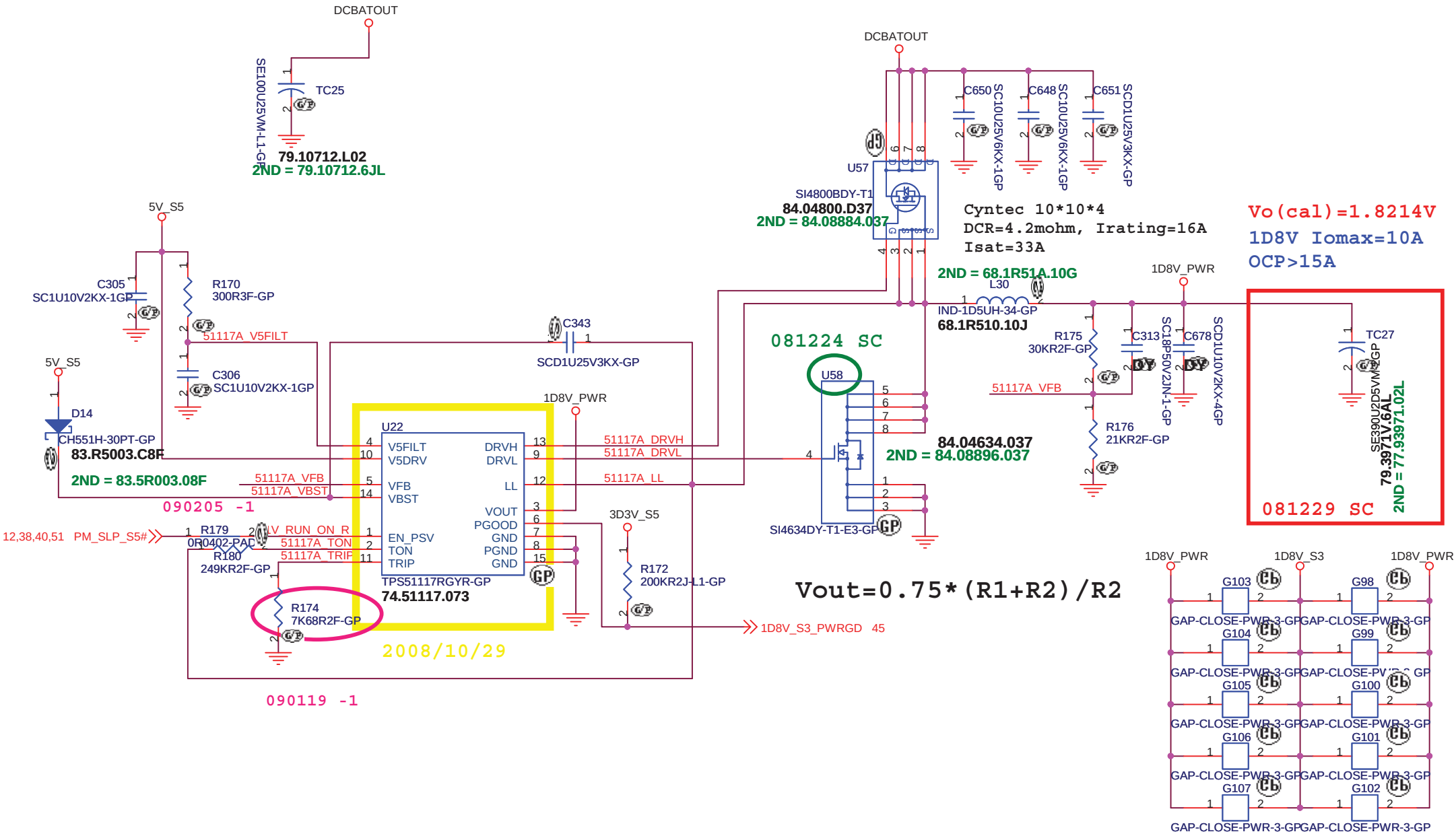

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***1D8V(TPS5117)***	
Size: A4	Document Number: **JM70-PU**	Rev: **-2**
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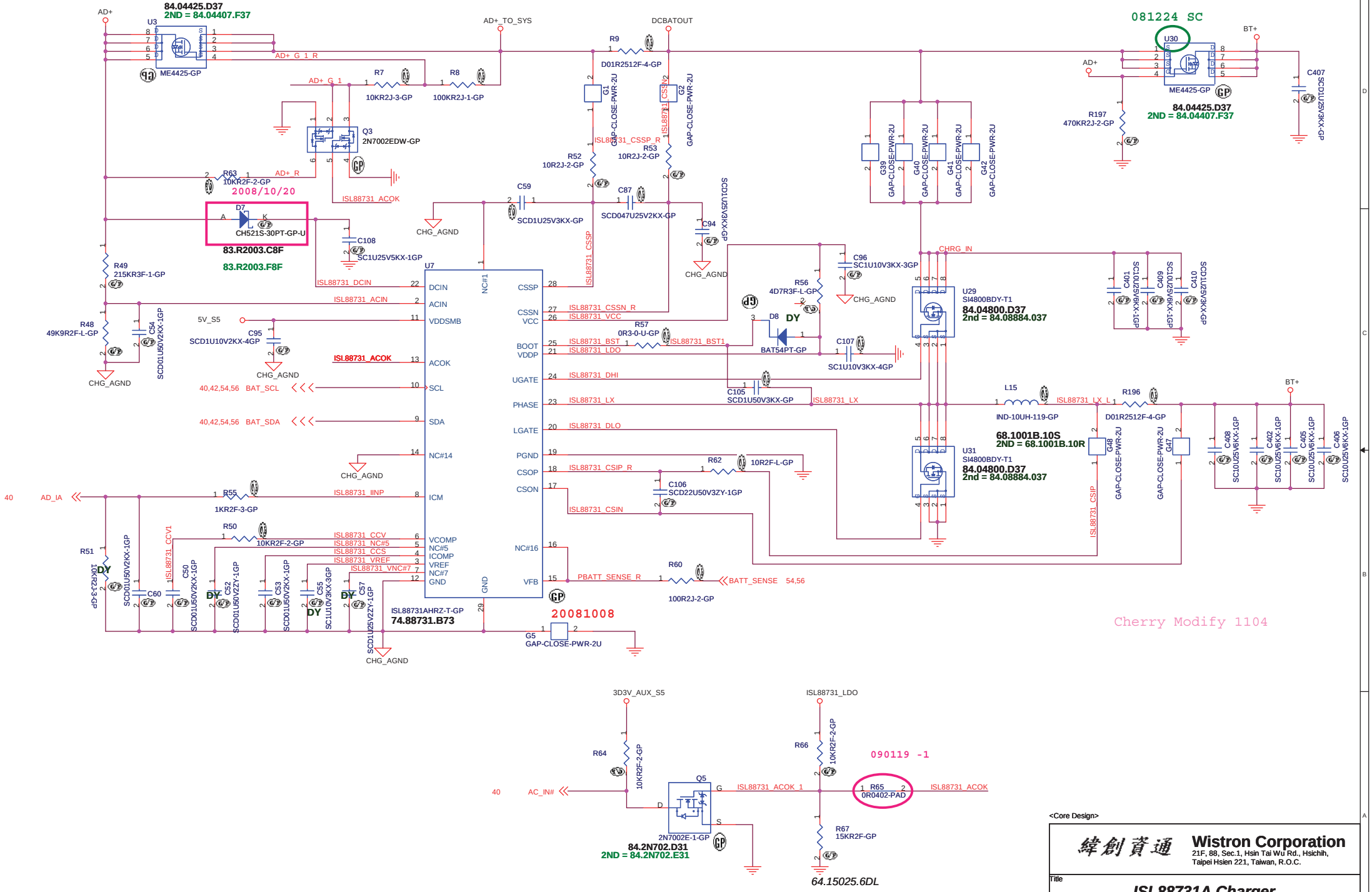
AD+
84.04425.D37
2ND = 84.04407.F37
U3
ME4425-GP
AD+_G_1_R
AD+_G_1
R7
10KR2J-3-GP
R8
100KR2J-1-GP
AD+_TO_SYS
DCBATOUT
R9
D01R2512F-4-GP
Q3
2N7002EDW-GP
R63
10KR2F-2-GP
AD+_R
2008/10/20
D7
CH521S-30PT-GP-U
83.R2003.C8F
83.R2003.F8F
C108
SC1U25V5KX-1GP
ISL88731_ACOK
CHG_AGND
C59
SCD1U25V3KX-GP
C87
SCD047U25V2KX-GP
C94
SCD1U25V3KX-GP
R52
10R2J-2-GP
R53
10R2J-2-GP
ISL88731_CSSP_R
ISL88731_CSSN_R
G1
G2
GAP-CLOSE-PWR-2U
G39
G40
G41
G42
081224 SC
U30
ME4425-GP
84.04425.D37
2ND = 84.04407.F37
R197
470KR2J-2-GP
C407
SCD1U25V3KX-GP
BT+
CHRG_IN
R49
215KR3F-1-GP
R48
49K9R2F-L-GP
C54
SCD01U50V2KX-1GP
5V_S5
C95
SCD1U10V2KX-4GP
U7
ISL88731_DCIN
ISL88731_ACIN
ISL88731_ACOK
40,42,54,56 BAT_SCL
40,42,54,56 BAT_SDA
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#1
NC#14
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
GND
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
R57
0R3-0-U-GP
R56
4D7R3F-L-GP
D8
BAT54PT-GP
DY
C96
SC1U10V3KX-3GP
C107
SC1U10V3KX-4GP
C105
SCD1U50V3KX-GP
U29
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
U31
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
L15
IND-10UH-119-GP
68.1001B.10S
2ND = 68.1001B.10R
R196
D01R2512F-4-GP
C401
C409
C410
C408
C402
C405
C406
SC10U25V6KX-1GP
R62
10R2F-L-GP
C106
SCD22U50V3ZY-1GP
40
AD_IA
R55
1KR2F-3-GP
ISL88731_IINP
ISL88731_CCV
ISL88731_NC#5
ISL88731_CCS
ISL88731_VREF
ISL88731_VNC#7
ISL88731_CCV1
R50
10KR2F-2-GP
R51
10KR2J-3-GP
C60
SCD01U50V2KX-1GP
C50
SCD01U50V2KX-1GP
C52
SCD01U50V2ZY-1GP
C53
SCD01U50V2KX-1GP
C55
SC1U10V3KX-3GP
C57
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ISL88731AHRZ-T-GP
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20081008
G5
GAP-CLOSE-PWR-2U
R60
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE 54,56
Cherry Modify 1104
3D3V_AUX_S5
ISL88731_LDO
R64
10KR2F-2-GP
R66
10KR2F-2-GP
090119 -1
Q5
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
40
AC_IN#
ISL88731_ACOK_1
R65
0R0402-PAD
ISL88731_ACOK
R67
15KR2F-GP
64.15025.6DL
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
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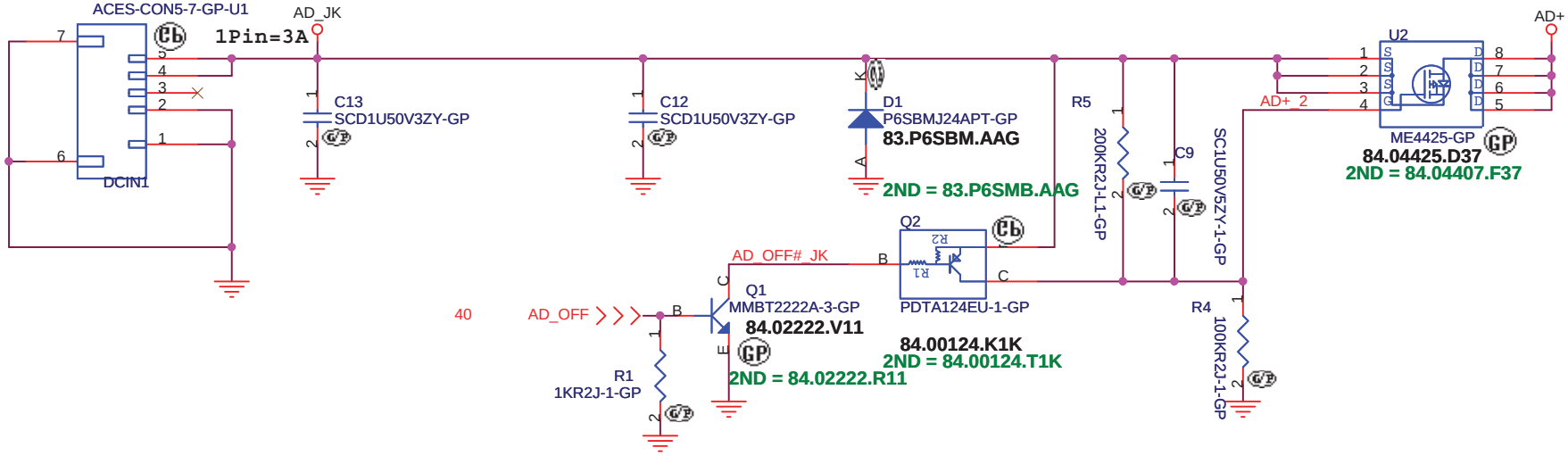
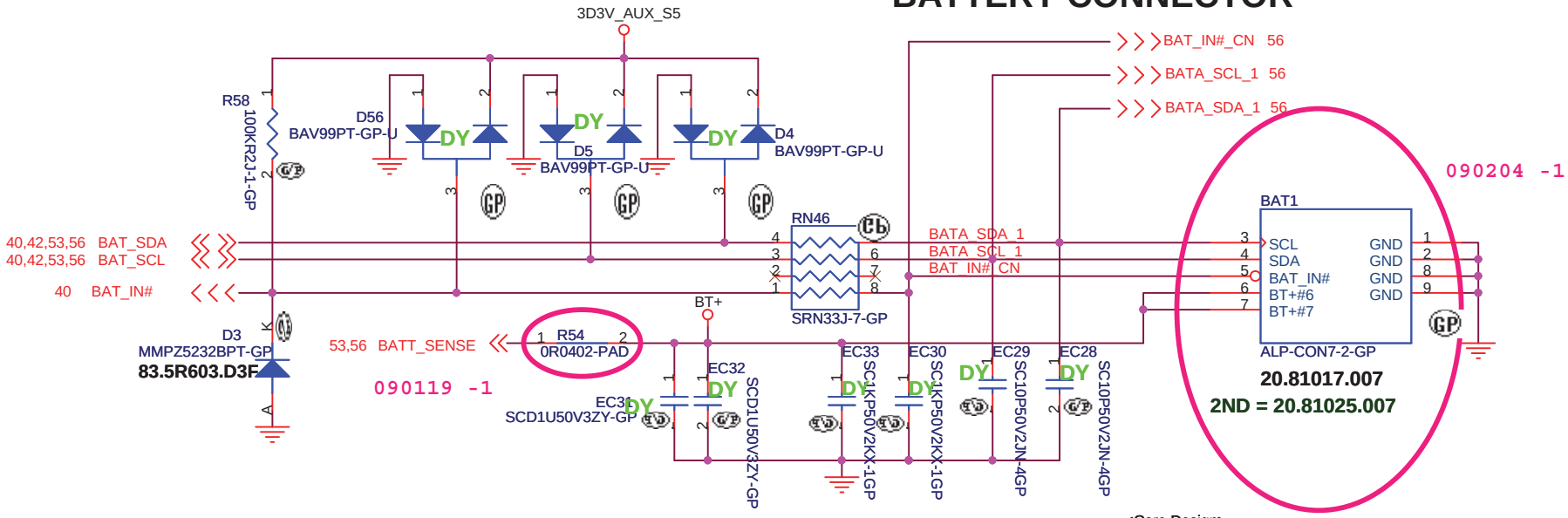
20.F1002.005

Adaptor in to generate DCBATOUT

2ND = 20.F1170.005

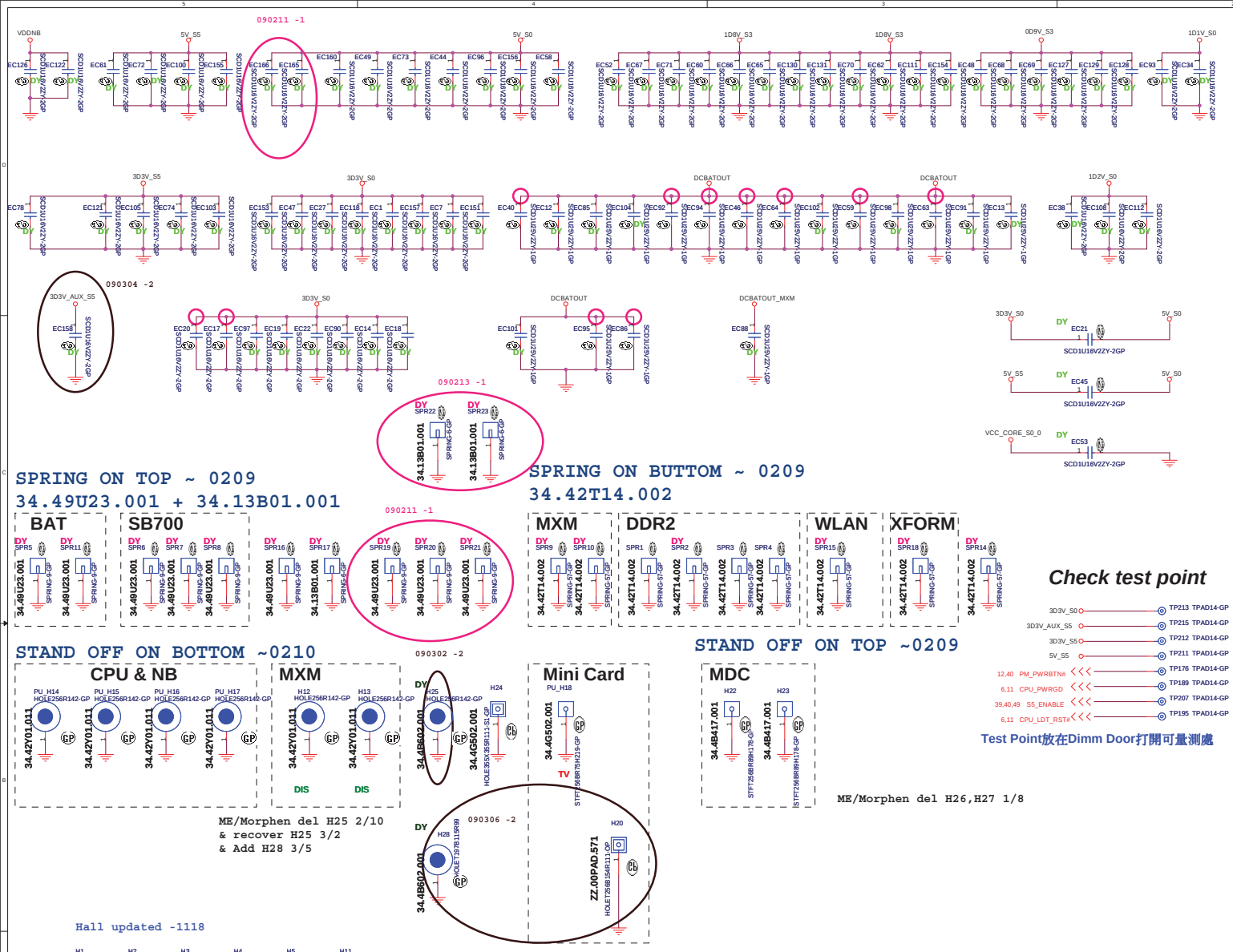


BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size: **A4**	Document Number: **JM70-PU**	Rev: -2
Date: Friday, March 06, 2009	Sheet 54 of 56	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size	Document Number	Rev
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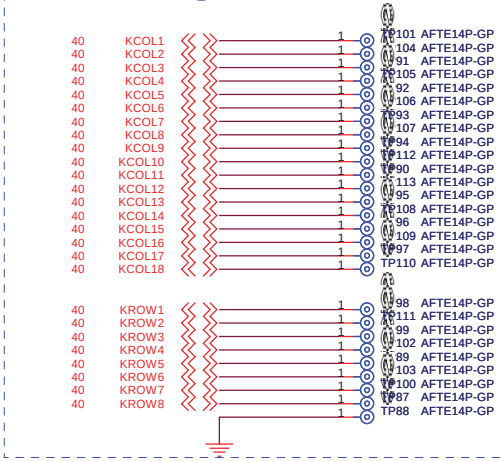
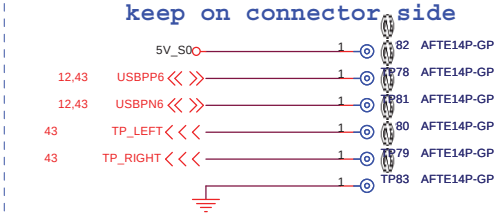
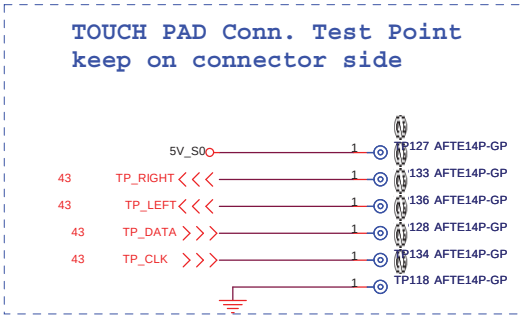
KB1 Conn. Test Point keep on connector side



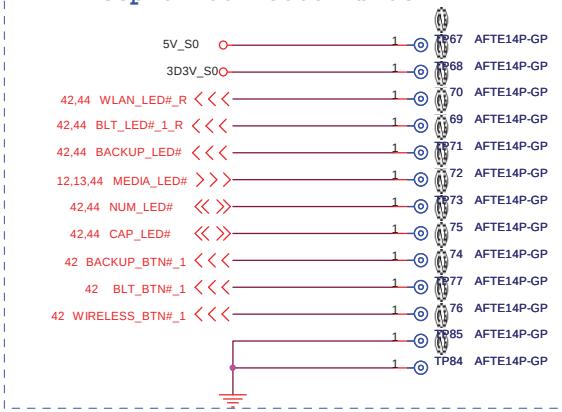
FP test Point keep on connector side



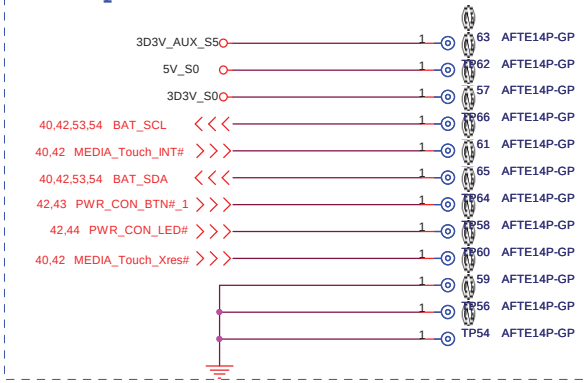
TOUCH PAD Conn. Test Point keep on connector side



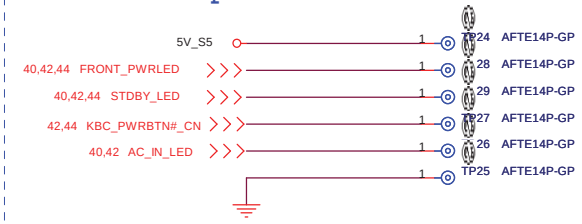
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side

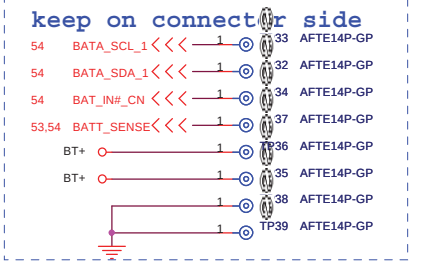


PWR_BT_CN1 Conn. Test Point keep on connector side

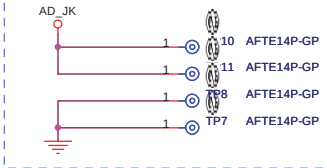


FAN1

BAT1 Conn. Test Point keep on connector side



DC1 Test Point keep on connector side



<Core Design>

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Title: **AFTE**

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