

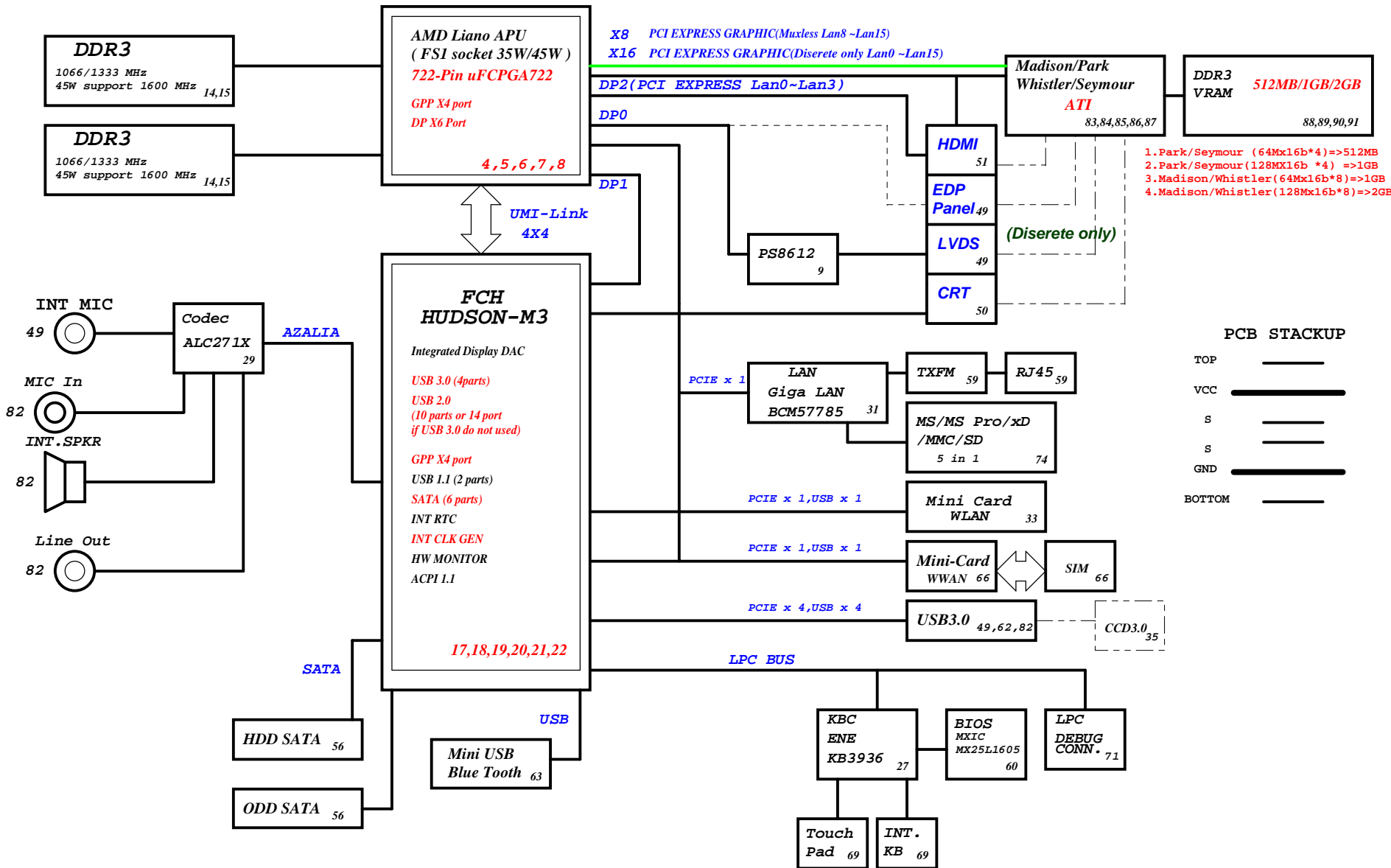
**Discrete/UMA /Muxless Schematics Document**  
**AMD LIANO CPU FS1**  
**AMD GPU Manhattan(Park/Madison M2)**  
**and Vancouver(Seymour/Whistler M2)**

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Cover Page</b>			
Size A4	Document Number <b>JE40-SB</b>		Rev <b>SB</b>
Date: Friday, March 25, 2011	Sheet	1	of 102

# JE40-SB Block Diagram

JE40-SB Project code: 91.4PQ01.001  
 SJV40\_SBM Project code:  
 SJV40\_SBP Project code:



1. Park/Seymour (64Mx16b\*4) => 512MB
2. Park/Seymour (128Mx16b \*4) => 1GB
3. Madison/Whistler (64Mx16b\*8) => 1GB
4. Madison/Whistler (128Mx16b\*8) => 2GB



SYSTEM DC/DC		RT8239		41
INPUTS	OUTPUTS			
DCBATOUT	5V_S5 (5.5A)	3D3V_S5 (5A)		
SYSTEM DC/DC		RT8207		44
5V_S5	1D5V_S3 (15A)			
SYSTEM DC/DC		RT8207		44
5V_S5	0D75_S0 (1.2A)			
SYSTEM DC/DC		RT8238		46
INPUTS	OUTPUTS			
5V_S5	1D1V_S5 (1.4A)			
SYSTEM DC/DC		RT8238		45
5V_S5	1D2V_S0 (5.2A)			
SYSTEM DC/DC		RT9025		93
3D3V_S5	1D8V_VGA_S0			
1D5V_S3	1V_VGA_S0			
SYSTEM DC/DC		RT9025		48
3D3V_S0	2D5V_S0 (200mA)			
SYSTEM DC/DC		RT8208		92
5V_S5	VGA_CORE			
CHARGER		BQ24745		40
INPUTS	OUTPUTS			
DCBATOUT	CHG_PWR	18V 6.0A		
	UP+5V	5V 100mA		
CPU DC/DC		ISL6267		42,43
INPUTS	OUTPUTS			
DCBATOUT	VCC_CORE_S0	0~1.55V 18A		
	VDDNB	0~1.55V 4A		

<Variant Name>

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Title: **Block Diagram**

Size A3	Document Number	Rev
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# Strapping

## REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH_GPO199	PCL_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	SS_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	SS_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

## USB Table

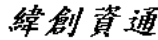
USB	
Pair	Device
0	USB 2.0(For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	USB 2.0 Small BD
7	CCD
8	NC
9	NC
10	USB 3.0 CCD(Reserve)
11	USB 3.0 (M/B USB1)
12	NC
13	NC

## PCIE Routing

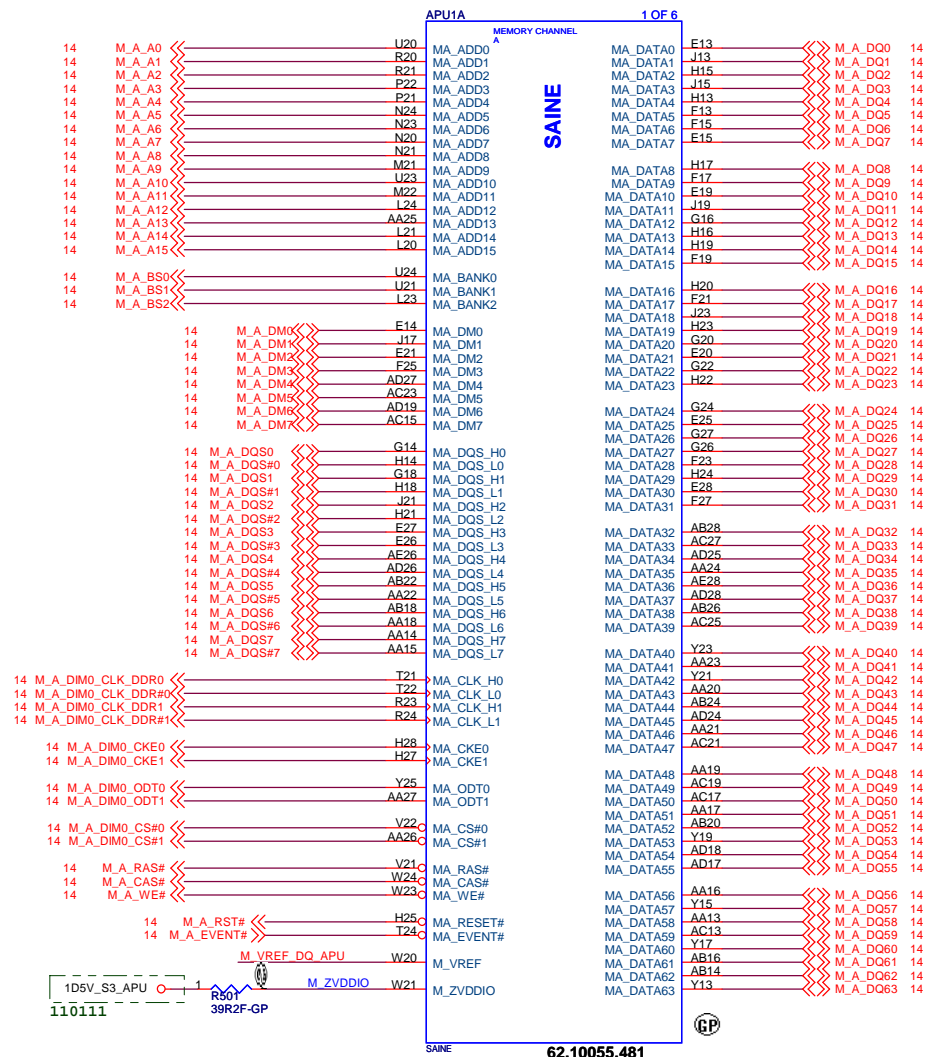
APU	
LANE0	LAN + Cardreader
LANE1	WWAN
LANE2	WLAN
LANE3	

FCH	
LANE0	
LANE1	
LANE2	
LANE3	

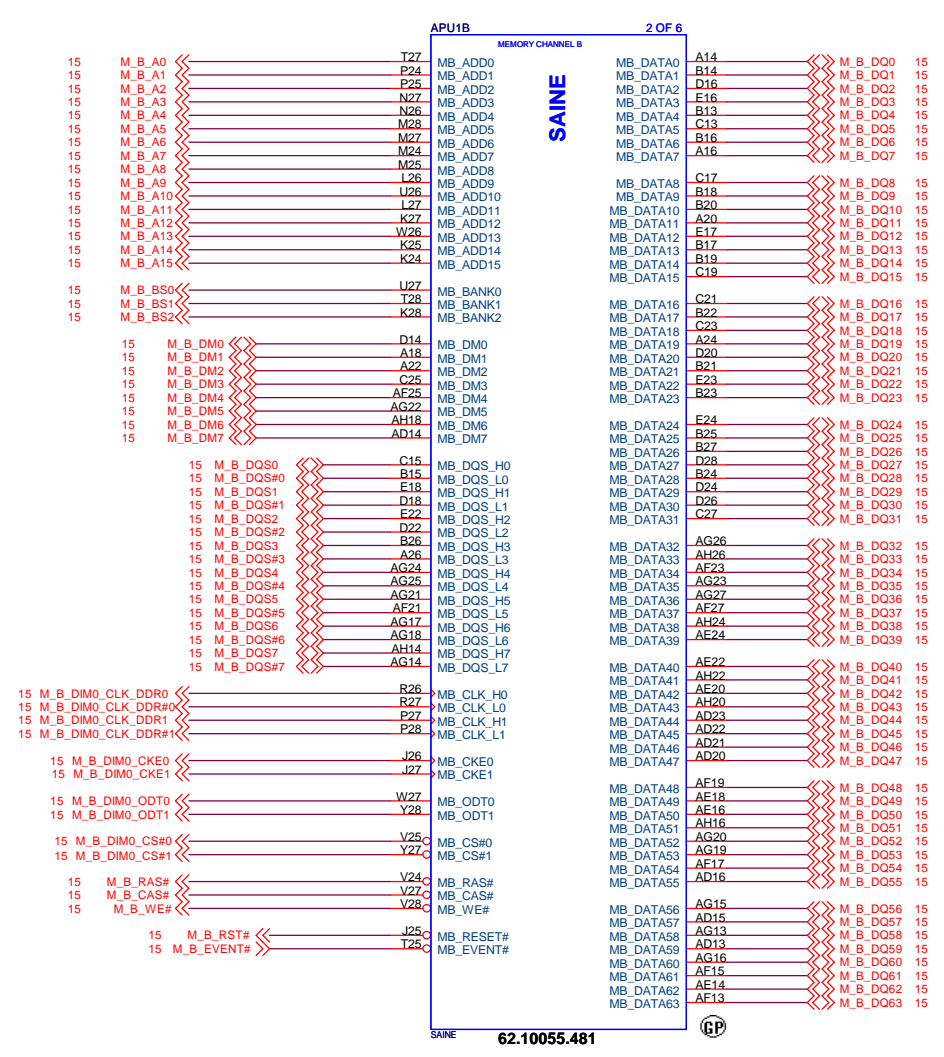
<Variant Name>

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Title		
<b>Table of Content</b>		
Size A3	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
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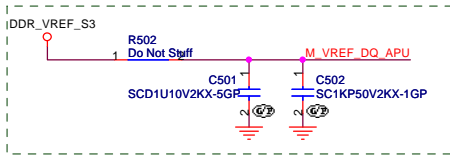


62.10055.481

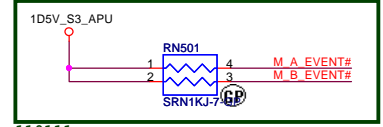


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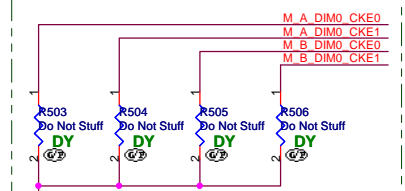
**APU\_VREF\_DQ**



LAYOUT: place them close to APU



110111



110110

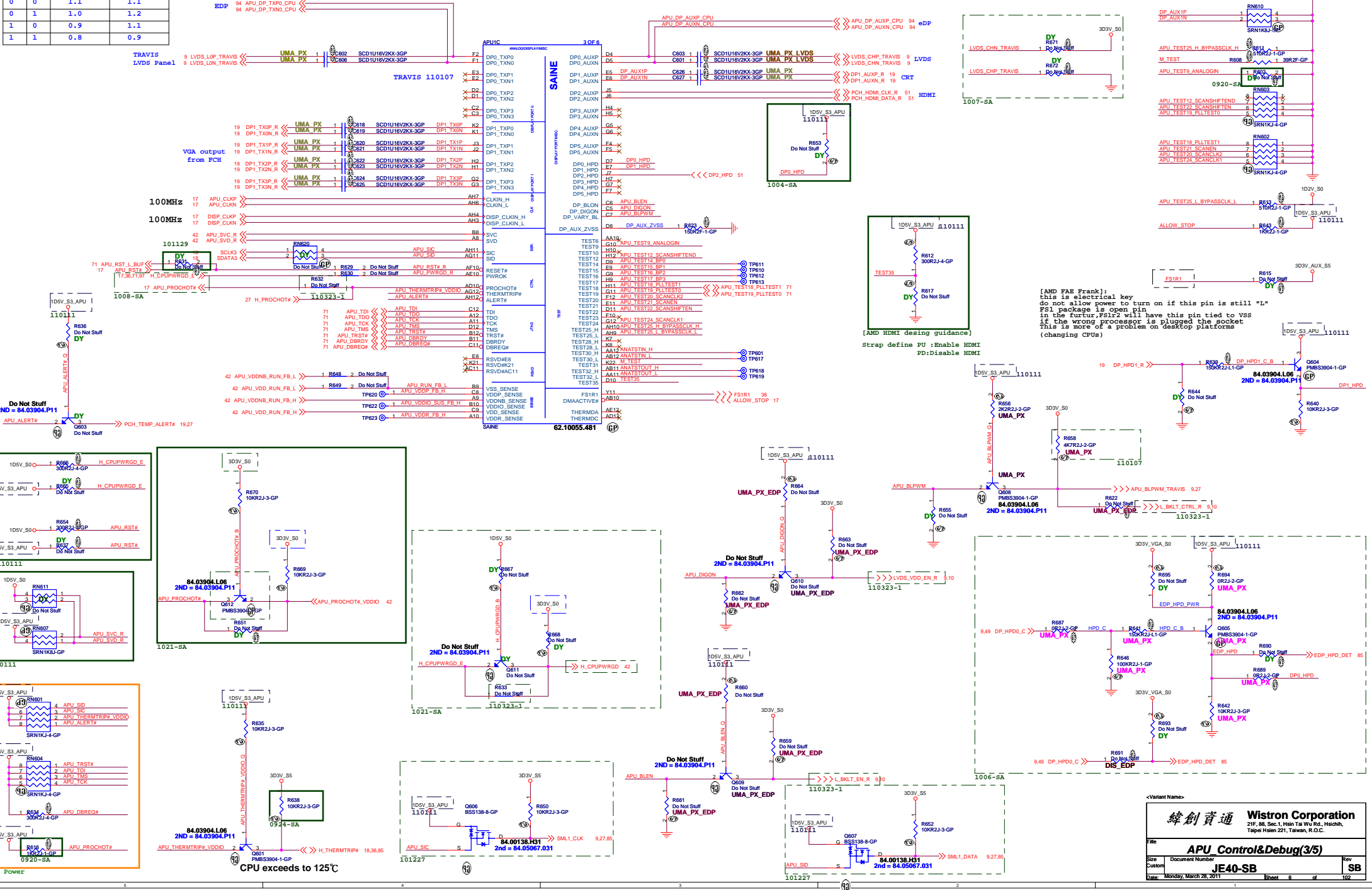
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Title: **APU DDR(2/5)**

Size A3	Document Number	Rev
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SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9



SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9

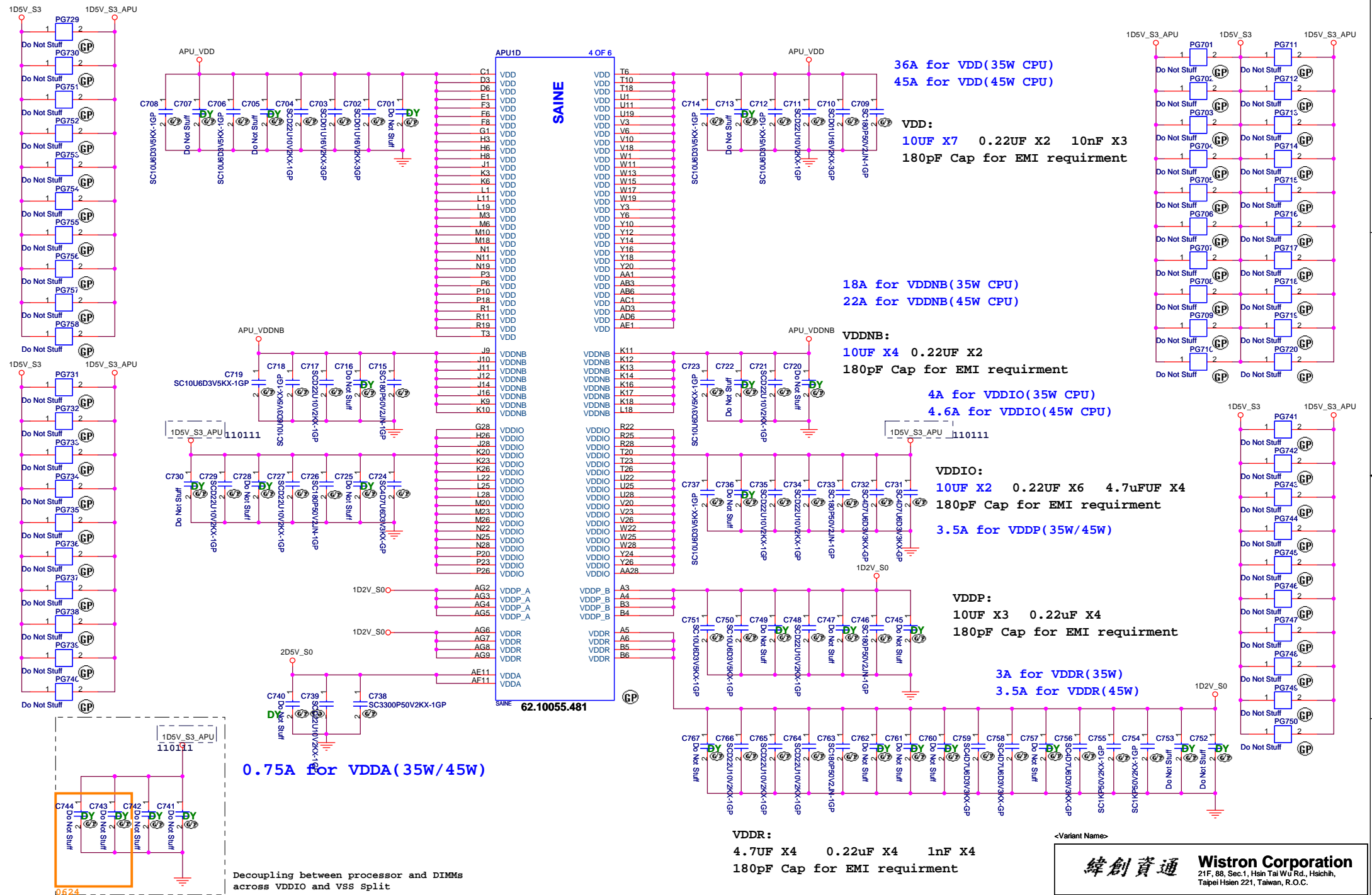
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

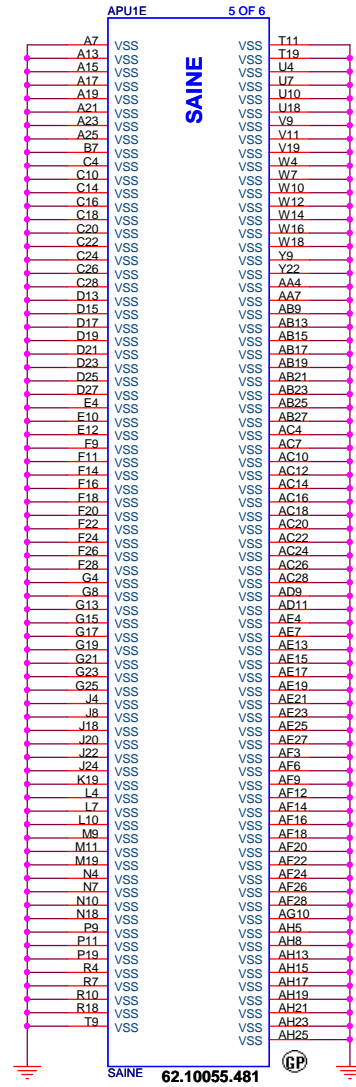
APU Control&Debug(3/5)

JE40-SB

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<Variant Name>

緯創資通

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Title

**APU VSS(5/5)**

Size  
A3

Document Number

**JE40-SB**

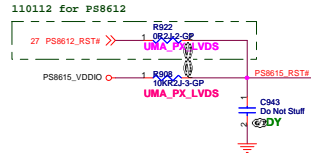
Rev

**SB**

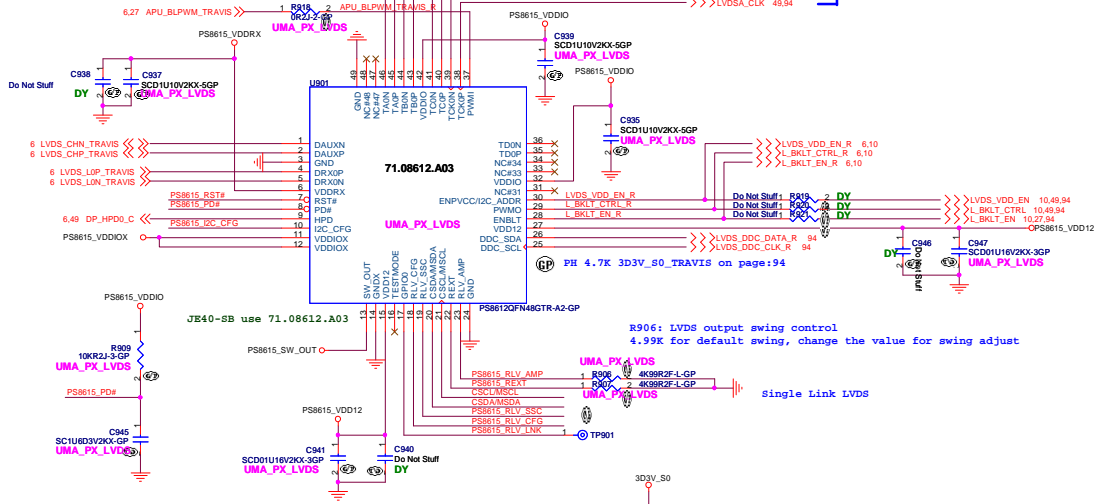
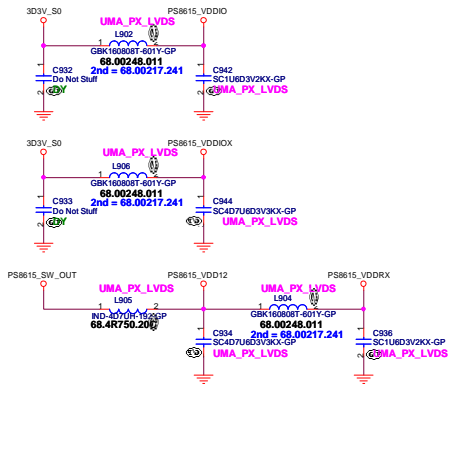
Date: Friday, March 25, 2011

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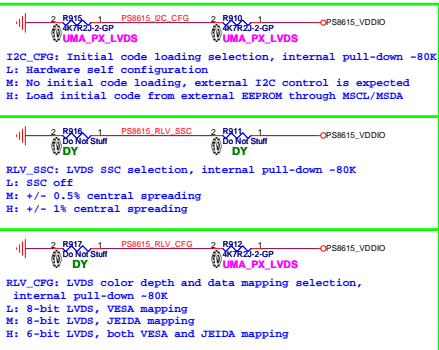




PWMI: 0-100KHz,  
0-100% duty cycle



R906: LVDS output swing control  
4.99K for default swing, change the value for swing adjust

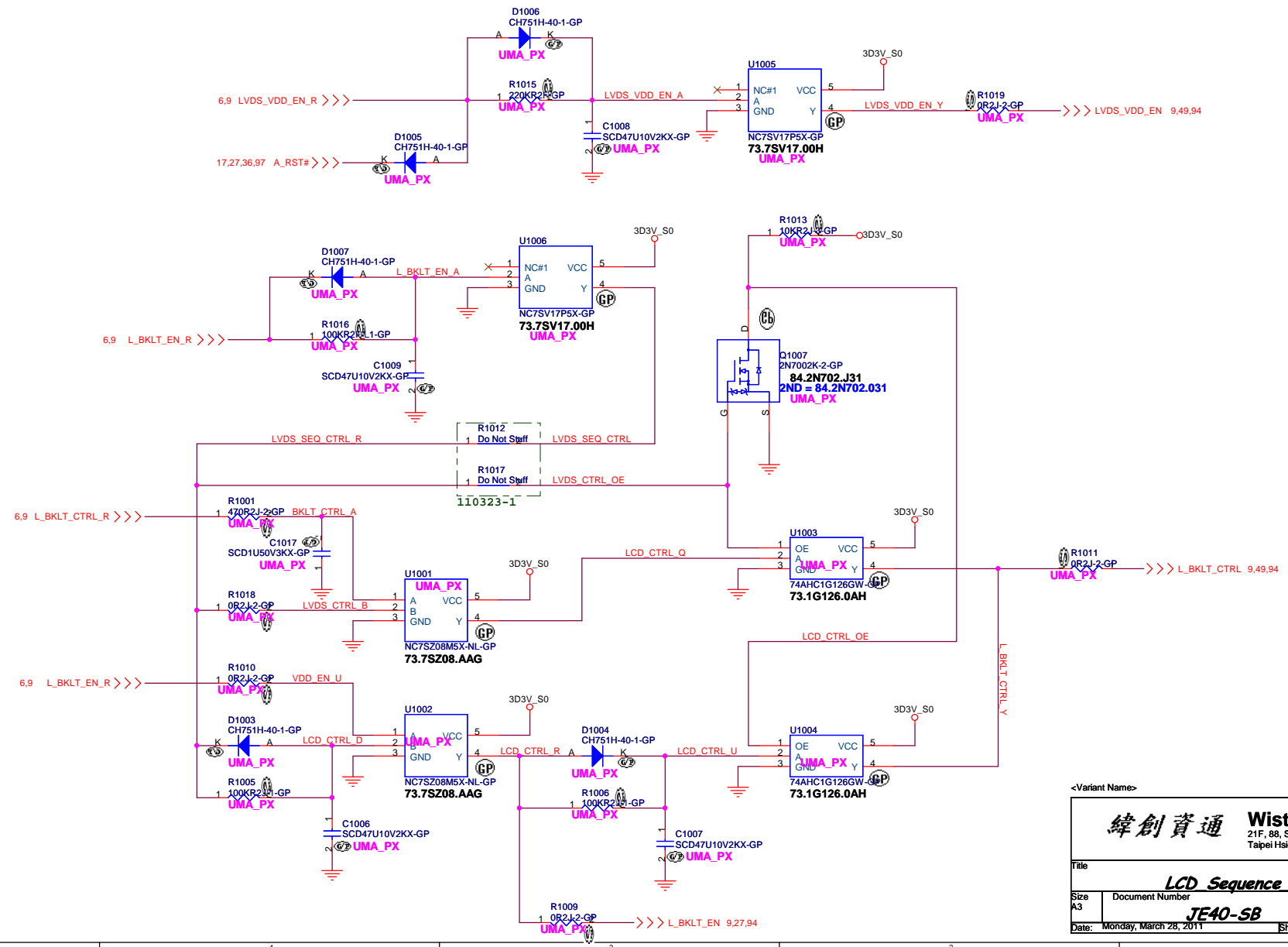


Default setting

I2C\_CFG: Initial code loading selection, internal pull-down -80K  
L: Hardware self configuration  
M: No initial code loading, external I2C control is expected  
H: Load initial code from external EPROM through NSCL/MSDA

RLV\_SSC: LVDS SSC selection, internal pull-down -80K  
L: SSC off  
M: +/- 0.5% central spreading  
H: +/- 1% central spreading

RLV\_CFG: LVDS color depth and data mapping selection, internal pull-down -80K  
L: 8-bit LVDS, VESA mapping  
M: 8-bit LVDS, JEIDA mapping  
H: 6-bit LVDS, both VESA and JEIDA mapping



(Blanking)

<Variant Name>

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Title		
<b>Reserved</b>		

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>Reserved</b>			
Size	Document Number		Rev
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( Blanking )

<Variant Name>

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Title

**Reserved**

Size

A4

Document Number

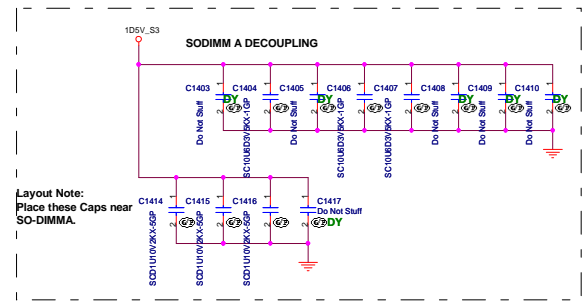
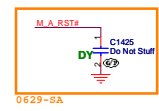
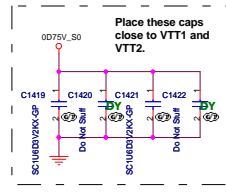
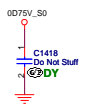
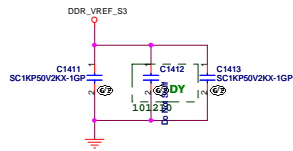
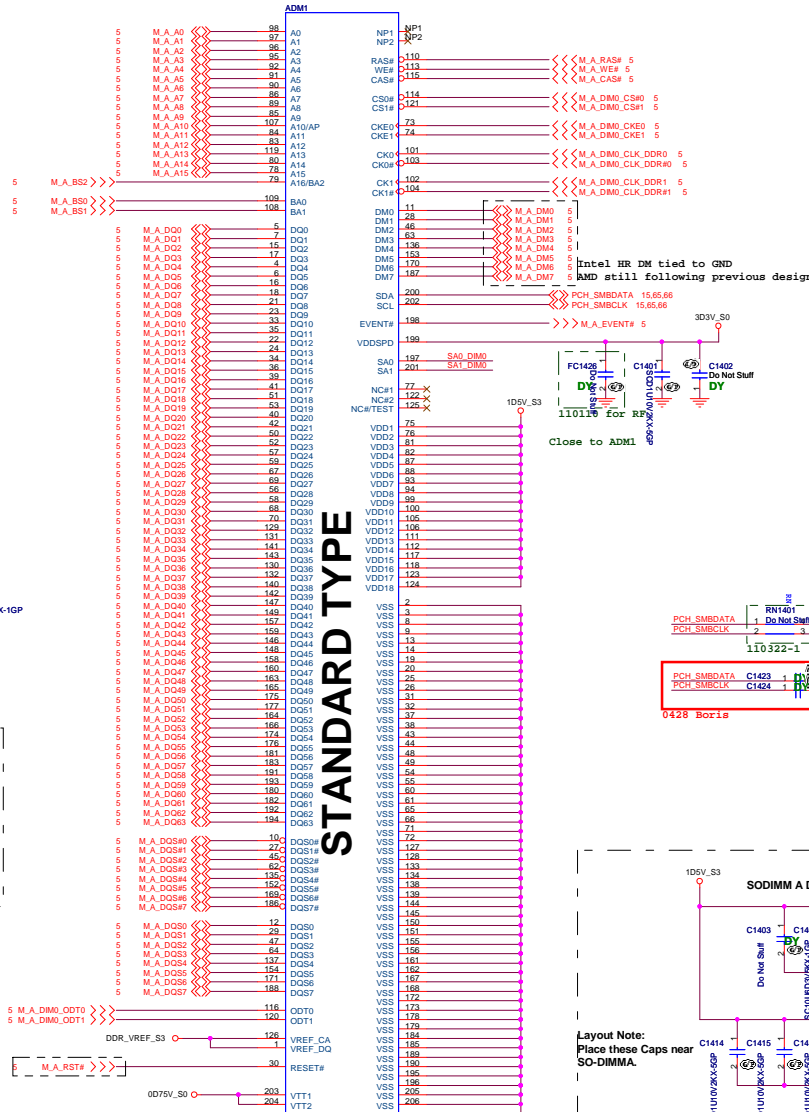
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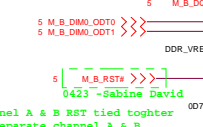
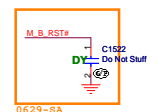
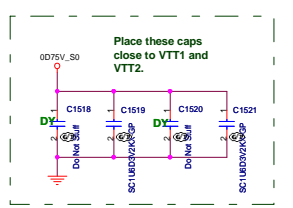
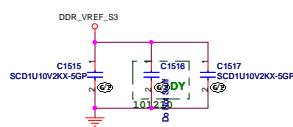
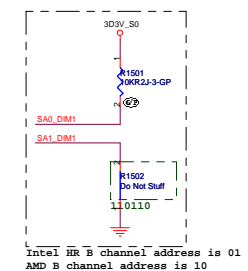
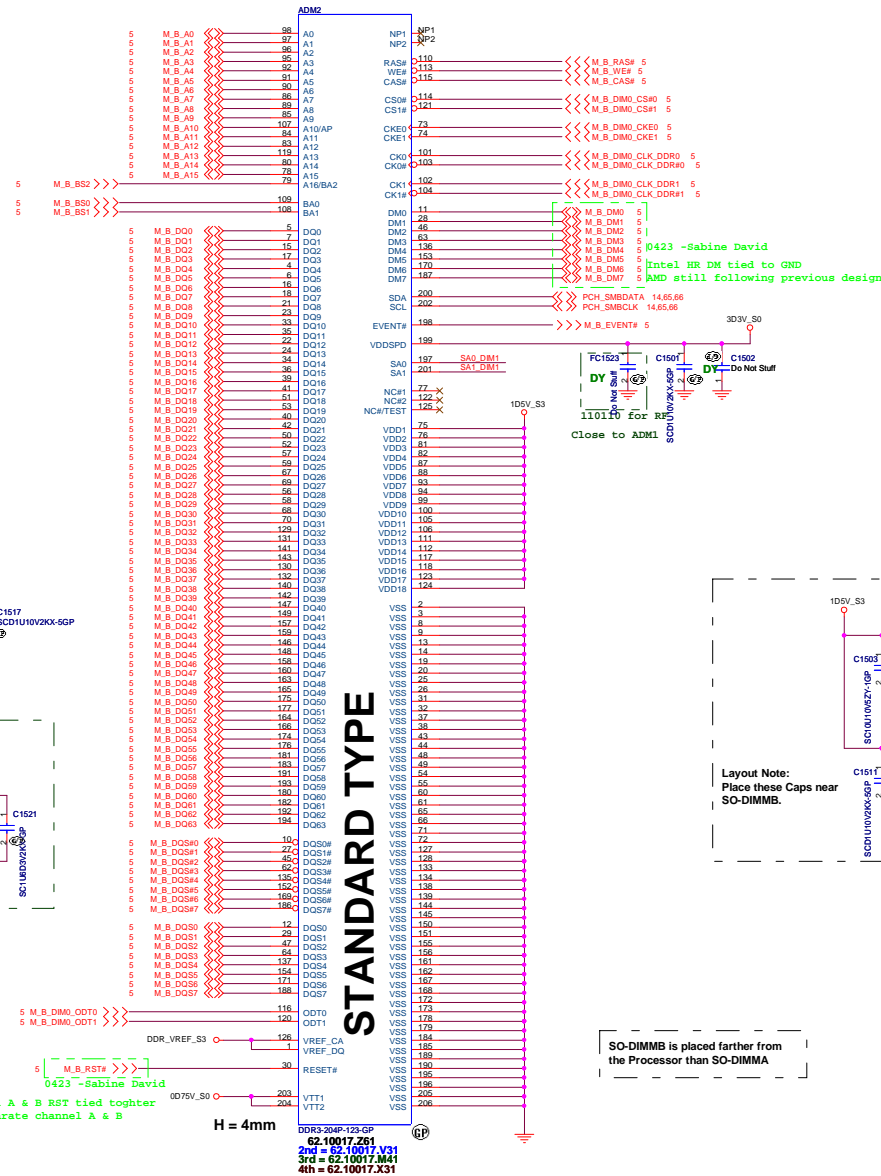
Rev

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Date: Friday, March 25, 2011

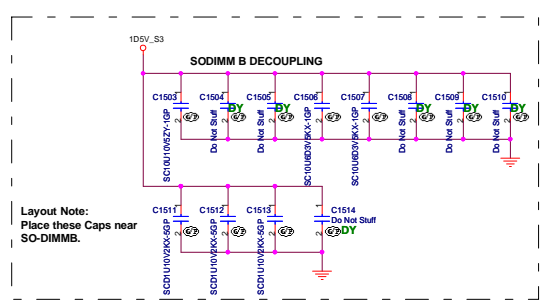
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**STANDARD TYPE**

H = 4mm  
 DDR3-204P-123-GP  
 62.10017.Z61  
 2nd = 62.10017.V31  
 3rd = 62.10017.M41  
 4th = 62.10017.X31



SO-DIMMB is placed farther from the Processor than SO-DIMMA

(Blanking)

<Variant Name>

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Title

**Reserved**

Size  
A4

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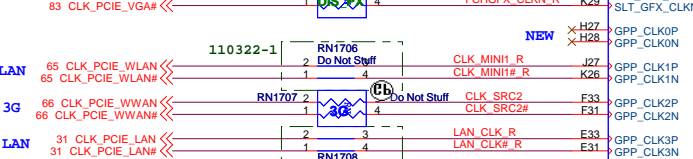
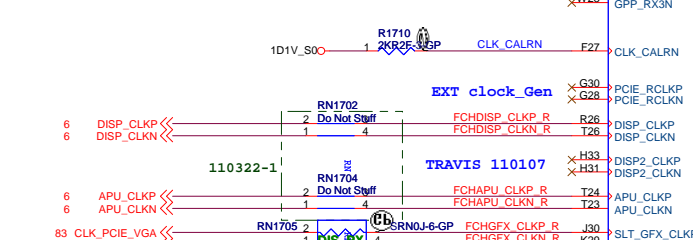
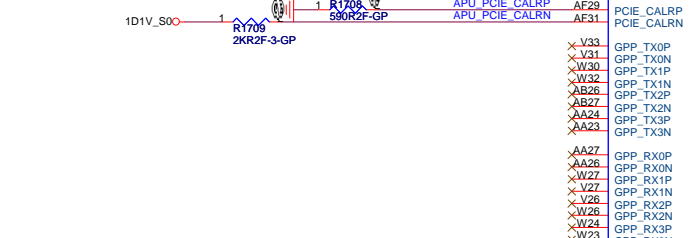
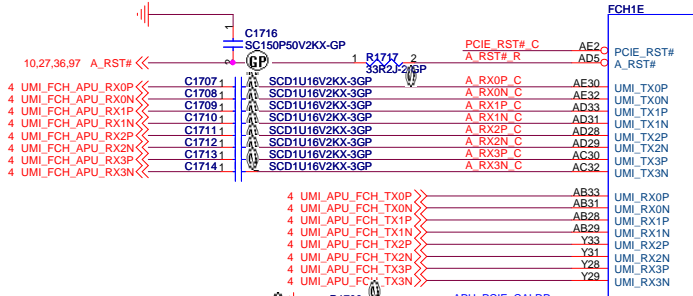
**JE40-SB**

Rev  
**SB**

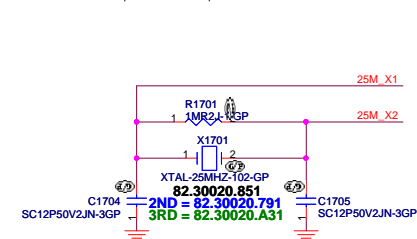
Date: Friday, March 25, 2011

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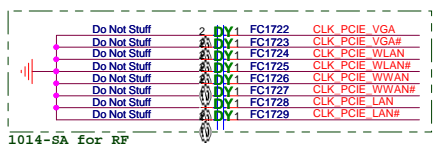




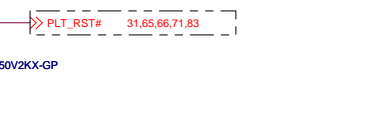
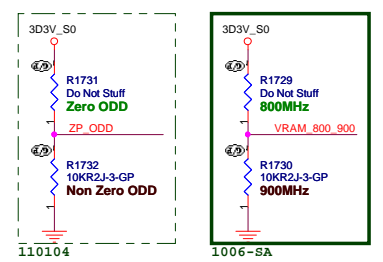
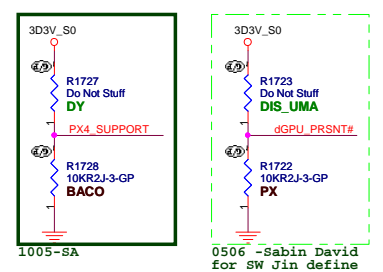
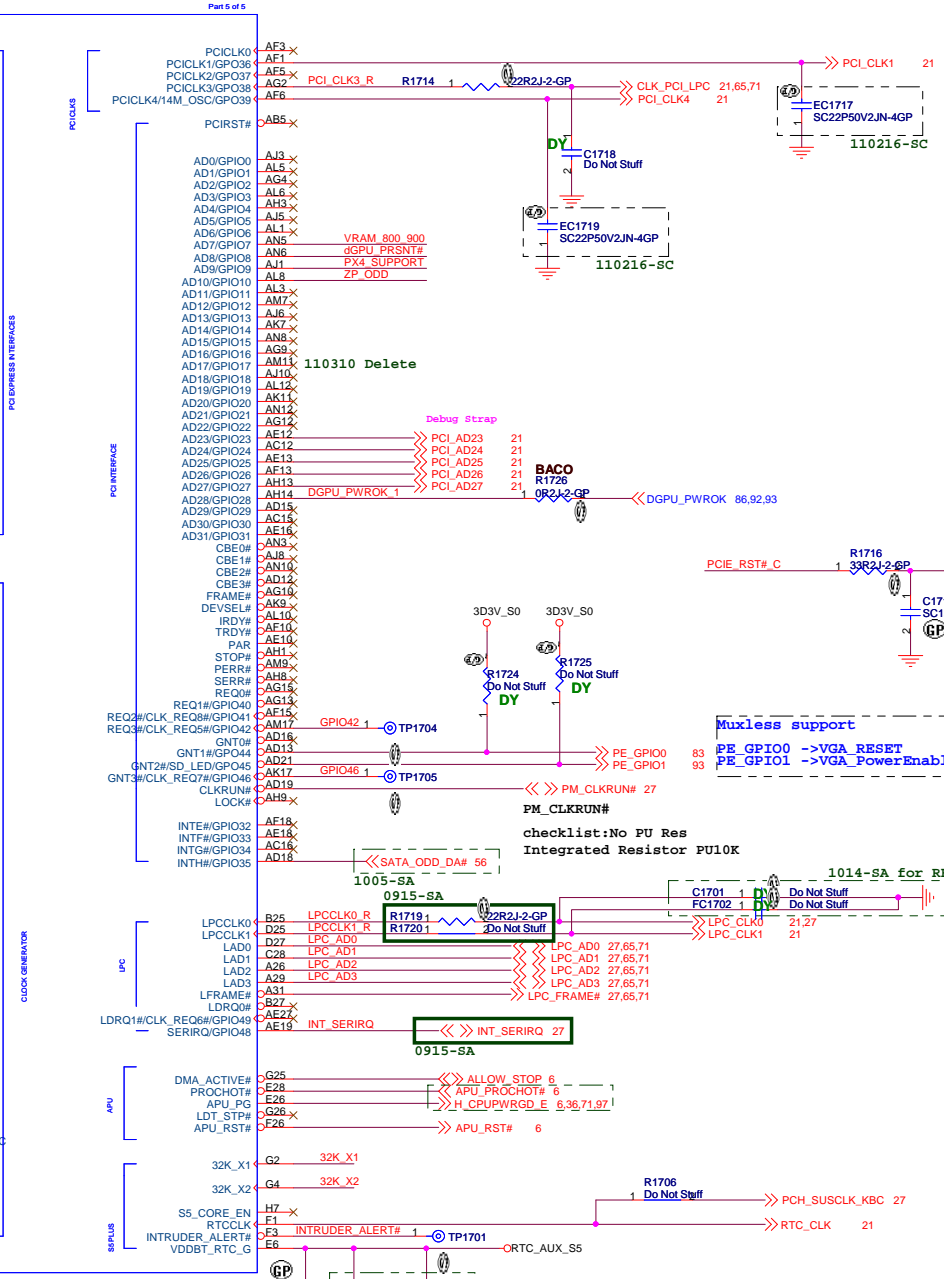
GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WWAN	2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	



CL = 12pF  
Freq tolerance : +/- 30ppm



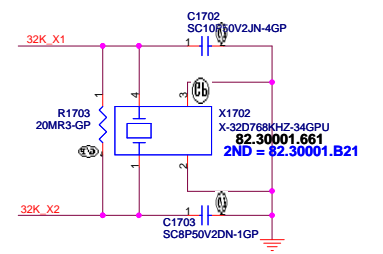
1014-SA for RF



LDT\_STP# connection is just for chipset automation purpose. It is an automatic test for AMD validation team only

Muxless support  
PE\_GPIO0 ->VGA\_RESET  
PE\_GPIO1 ->VGA\_PowerEnable

PM\_CLKRUN#  
checklist:No PU Res  
Integrated Resistor PU10K



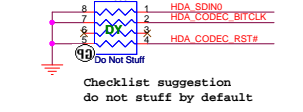
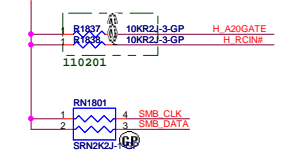
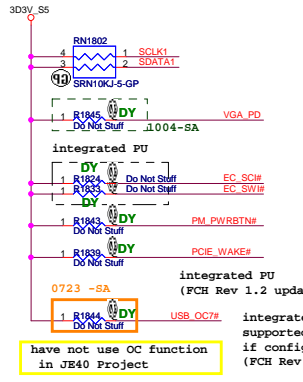
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Freq tolerance : +/- 20 ppm

-Variant Name-

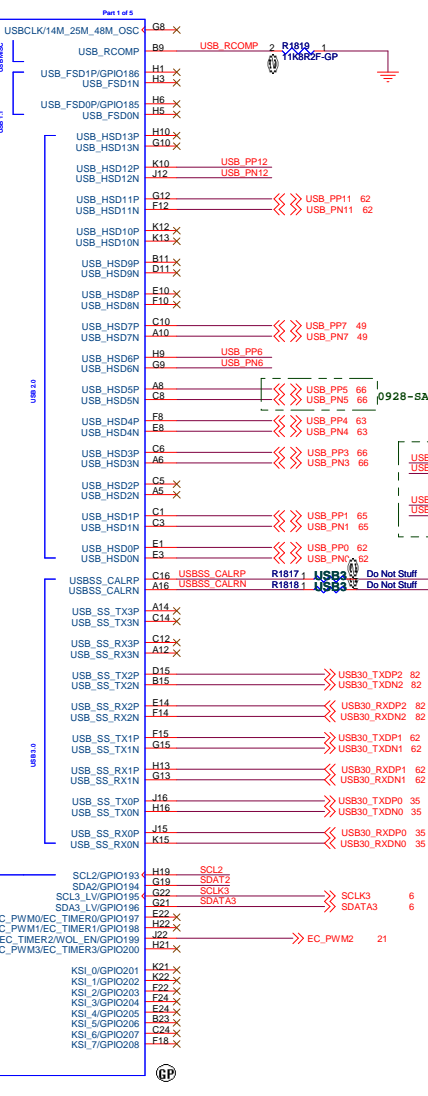
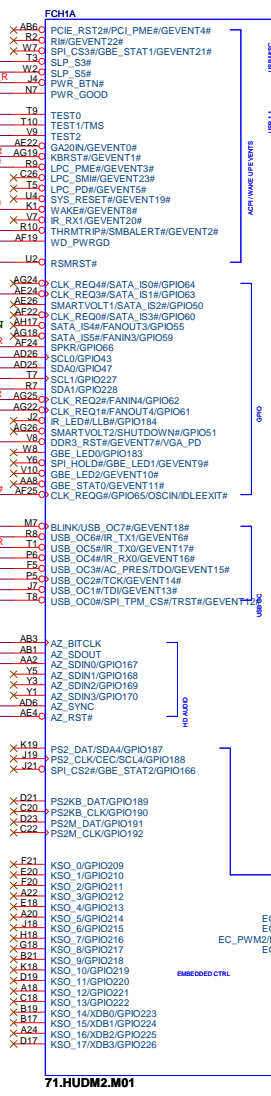
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Title: **HUDSON-M2(1/6)**

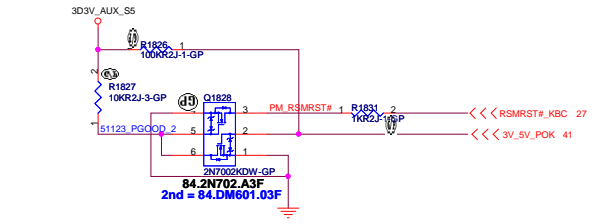
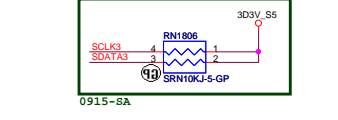
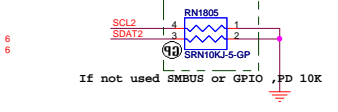
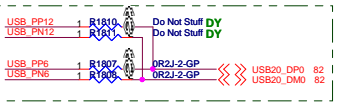
Size	Document Number	Rev
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Function	Name	Integrated Resistor	External Resistor
GA20IN	H_A20GATE	8.2K PU	10K PU 3.3_80 DY
KBRST#	H_RCIN#	8.2K PU	10K PU 3.3_80 DY
PME#	EC_SCI#	10K PU	10K PU 3.3_85 DY
THRIPTRIP#	H_THERMTRIP#	10K PU	10K PU 3.3_85 DY
PCIE_RST2#	FCH_PCIE_RST#	10K PU	
Gevent5	MEM_Hot#	10K PU	
Gevent6	EC_SWI#	10K PU	10K PU 3.3_85 DY
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_85 DY
USB_OC0#	USB_OC0#	10K PU	
USB_OC1#	USB_OC1#	10K PU	
USB_OC2#	USB_OC2#	10K PU	
Gevent15#	SATA_ODD_PRSNT#	10K PU	
Gevent16#	ODD_DA	10K PU	
USB_OC5#	ODD_C5#	10K PU	
Gevent17#	EC_SWI#	10K PU	10K PU 3.3_80 DY
USB_OC7#	USB_OC7#	10K PU	
LPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_85 DY
GPIO35	SATA_ODD_DA#	8.2K PU	
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_80 DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU	
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU	
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU	
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU	
CLK_REQ0	PEG_CLKREQ#	8.2K PU	



Pair	Device
0	USB 2.0 (For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	USB 2.0 Small BD
7	CCD
8	NC
9	NC
10	USB 3.0 CCD (Reserve)
11	USB 3.0 (M/B USB1)
12	USB 3.0 (Small BD Reserved)
13	NC



<Variant Name>

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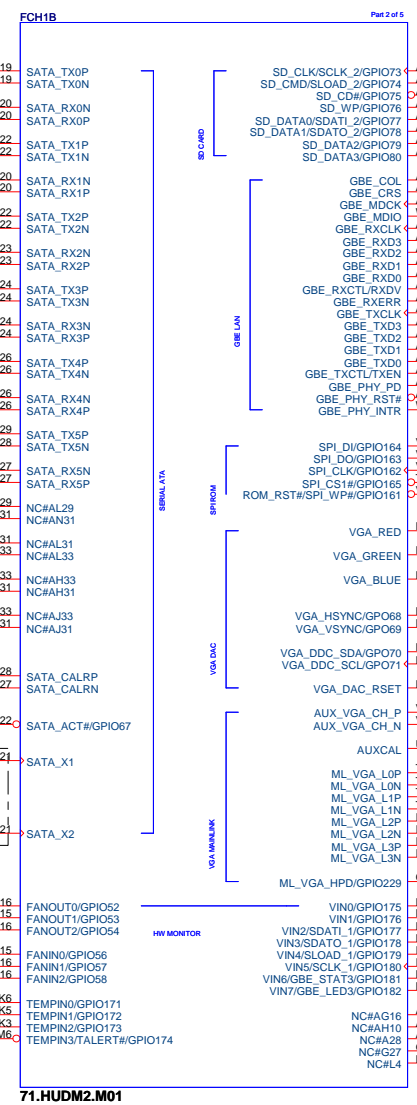
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Size: Document Number

Customer: **JE40-SB** Rev: **SB**

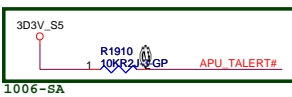
Date: Monday, March 26, 2011 Sheet: 18 of 102

1st SATA HDD  
SATA ODD  
E-SATA  
2nd SATA HDD



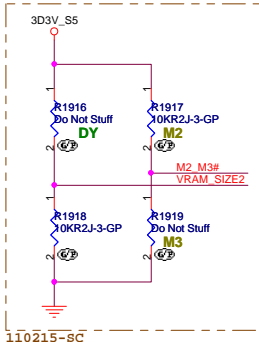
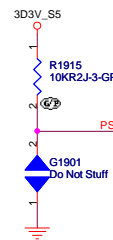
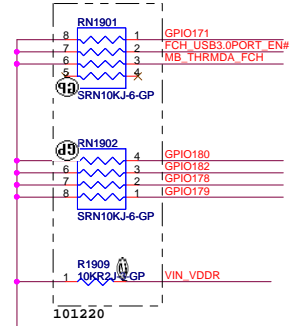
1D1V\_S0C follow AMD design guide

[checklist]: Integrated Clock Mode => Left unconnected



VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

VRAM size	GPIO176	GPIO177
512MB	L	L
1GB	H	H
2GB	H	L
Undefine	L	H



<Variant Name>

**緯創資通 Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

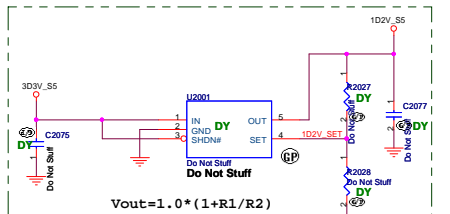
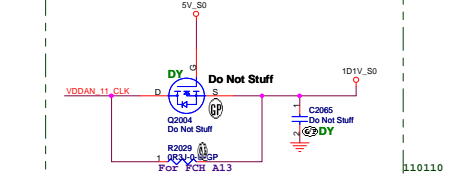
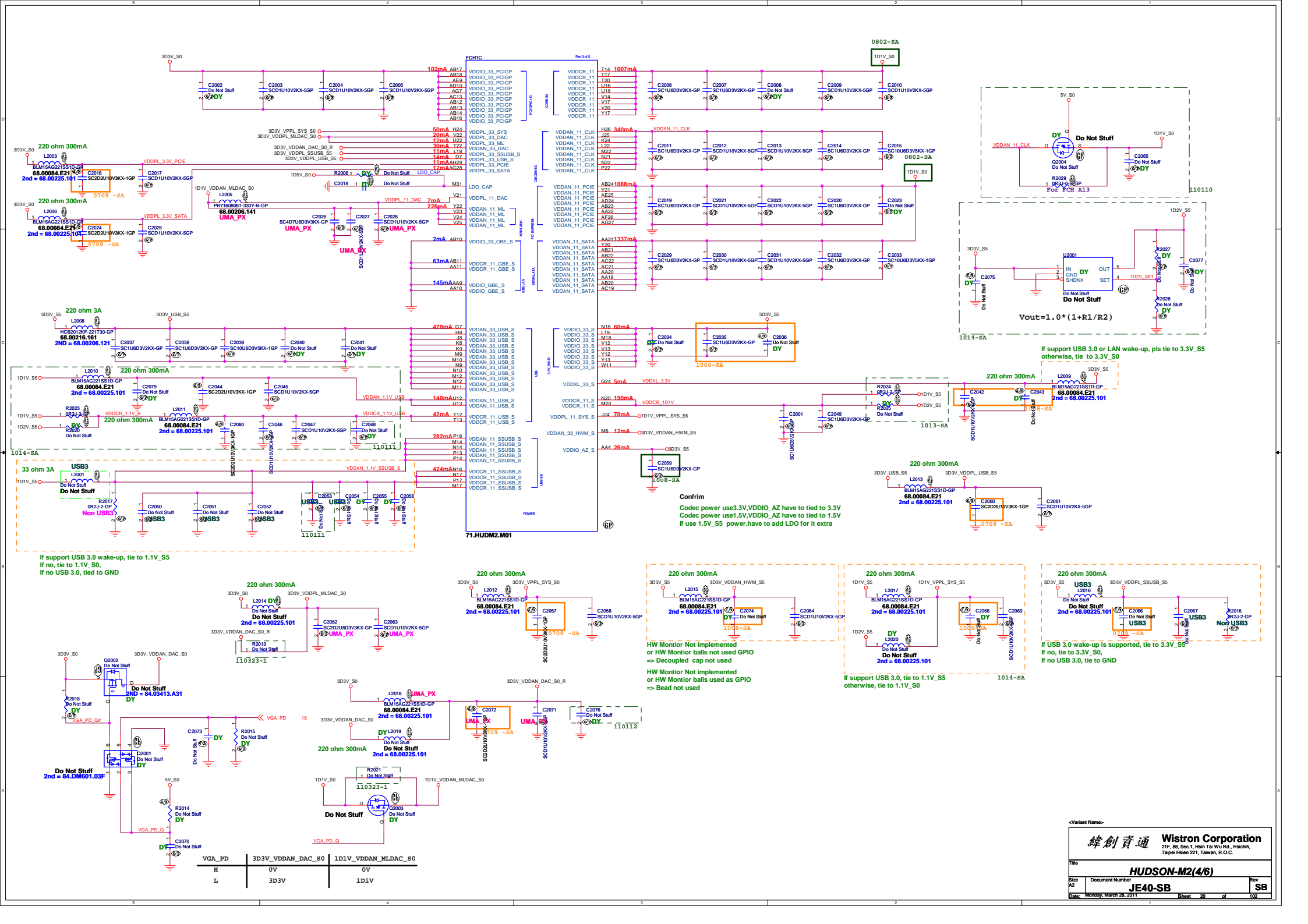
Title: **HUDSON-M2(3/6)**

Size: **JE40-SB**

Document Number: **SB**

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If not used HWM or GPIO ,PD 10K



If support USB 3.0 or LAN wake-up, pls tie to 3.3V\_S5 otherwise, tie to 3.3V\_S0

Confirm  
 Codec power use 3.3V\_VDDIO\_AZ have to tied to 3.3V  
 Codec power use 1.5V\_VDDIO\_AZ have to tied to 1.5V  
 If use 1.5V\_S5 power, have to add LDO for it extra

If support USB 3.0 wake-up, tie to 1.1V\_S5  
 If no, tie to 1.1V\_S0  
 If no USB 3.0, tied to GND

HW Monitor Not implemented or HW Monitor balls not used GPIO  
 => Decoupled cap not used

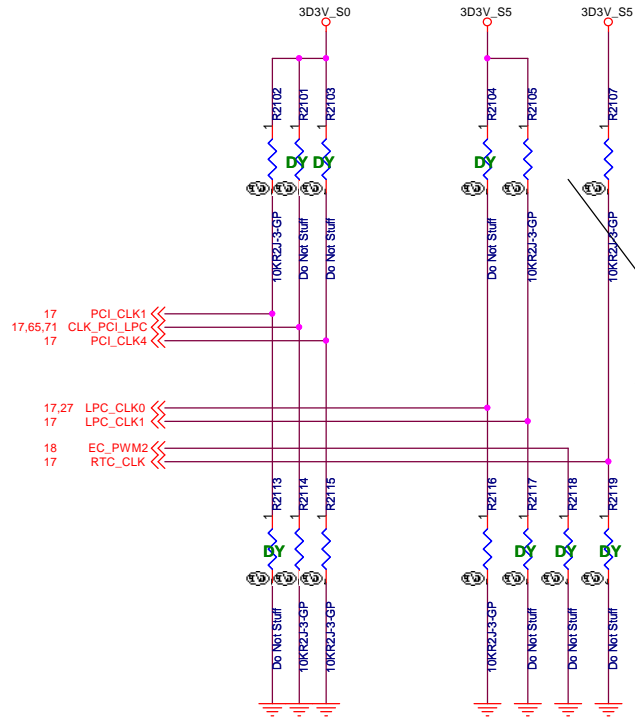
HW Monitor Not implemented or HW Monitor balls used as GPIO  
 => Bead not used

If USB 3.0 wake-up is supported, tie to 3.3V\_S5  
 If no, tie to 3.3V\_S0  
 If no USB 3.0, tie to GND

VGA_PD	3D3V_VDDAN_DAC_S0	1D1V_VDDAN_MLDAC_S0
H	0V	0V
L	3D3V	1D1V

**SSID = S.B**

## REQUIRED STRAPS



CRB:PU 3.3V\_AUX\_S5  
checklist:PU 3.3V\_S5  
no support S5 PLUS function,PU 3.3V\_S5

## REQUIRED SYSTEM STRAPS

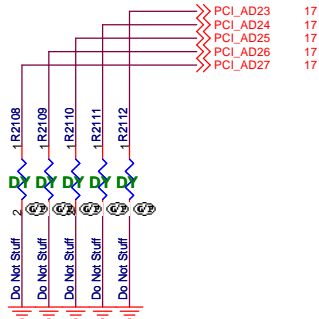
USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

LPC ROM implemented  
checklistsuggestion:  
no PU or PD required  
(integrated PU 10K)  
CRB: do not stuff PU Res

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

## DEBUG STRAPS

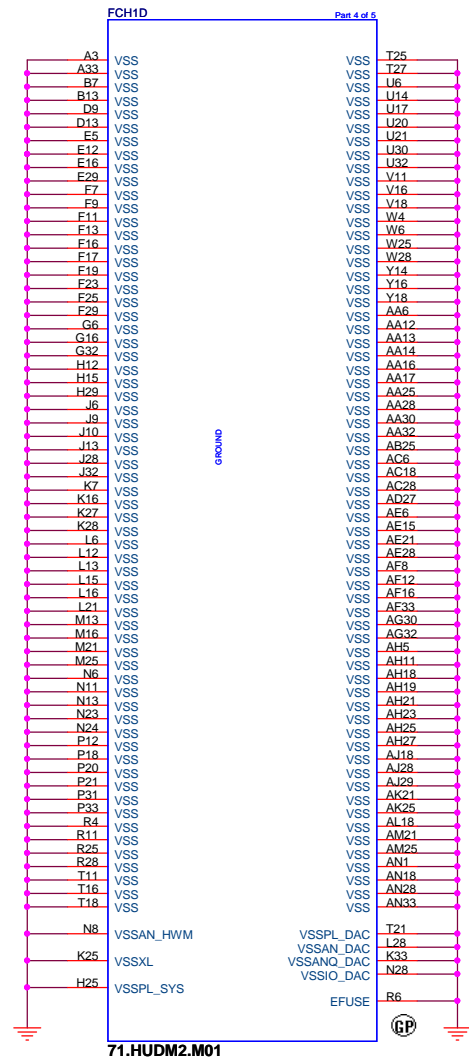


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI\_AD[27:23]

<Variant Name>

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<b>HUDSON-M2(5/6)</b>			
Title	Document Number		Rev
Size A3	<b>JE40-SB</b>		<b>SB</b>
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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>JE40-SB</b>		<b>SB</b>
Date:	Friday, March 25, 2011	Sheet 23	of 102

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<Variant Name>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**JE40-SB**

Rev  
**SB**

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<Variant Name>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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A3	<b>JE40-SB</b>	<b>SB</b>	
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<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

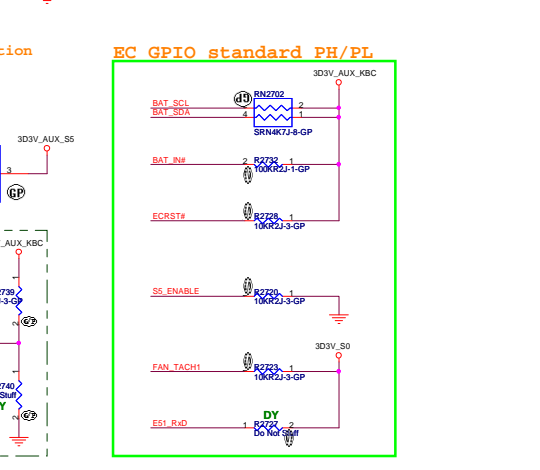
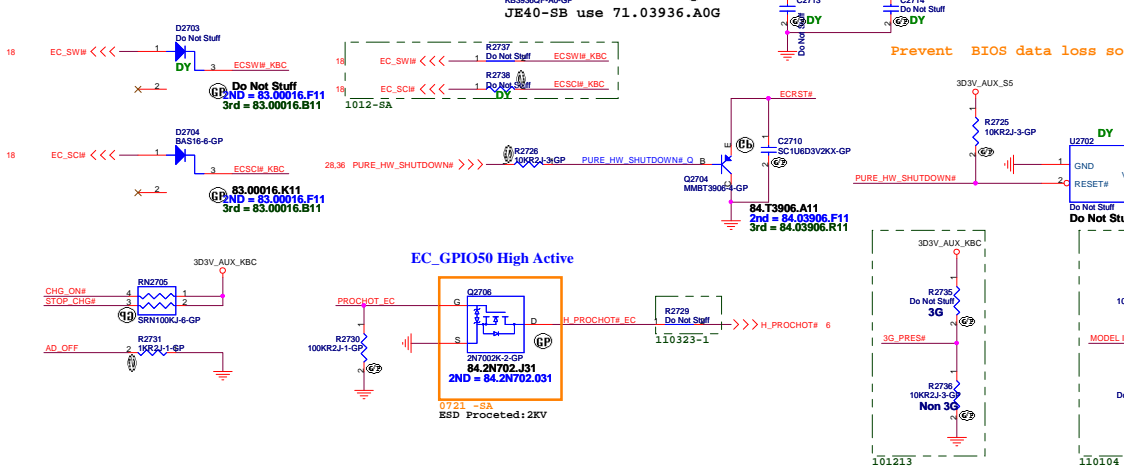
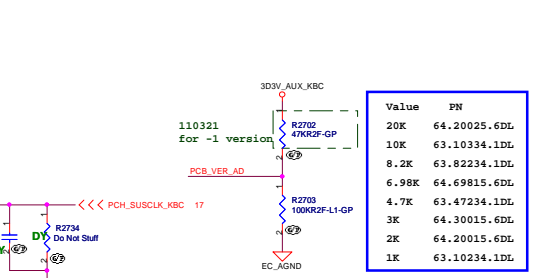
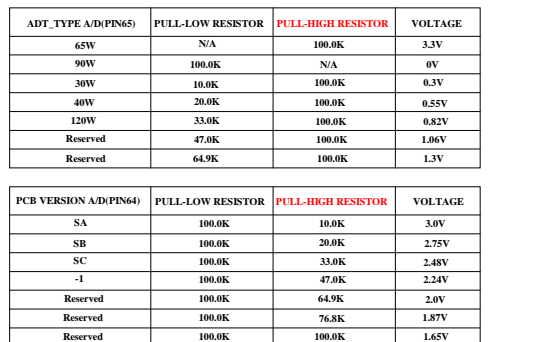
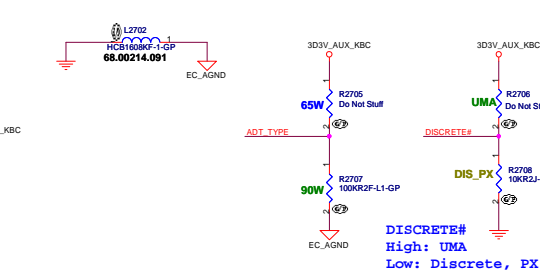
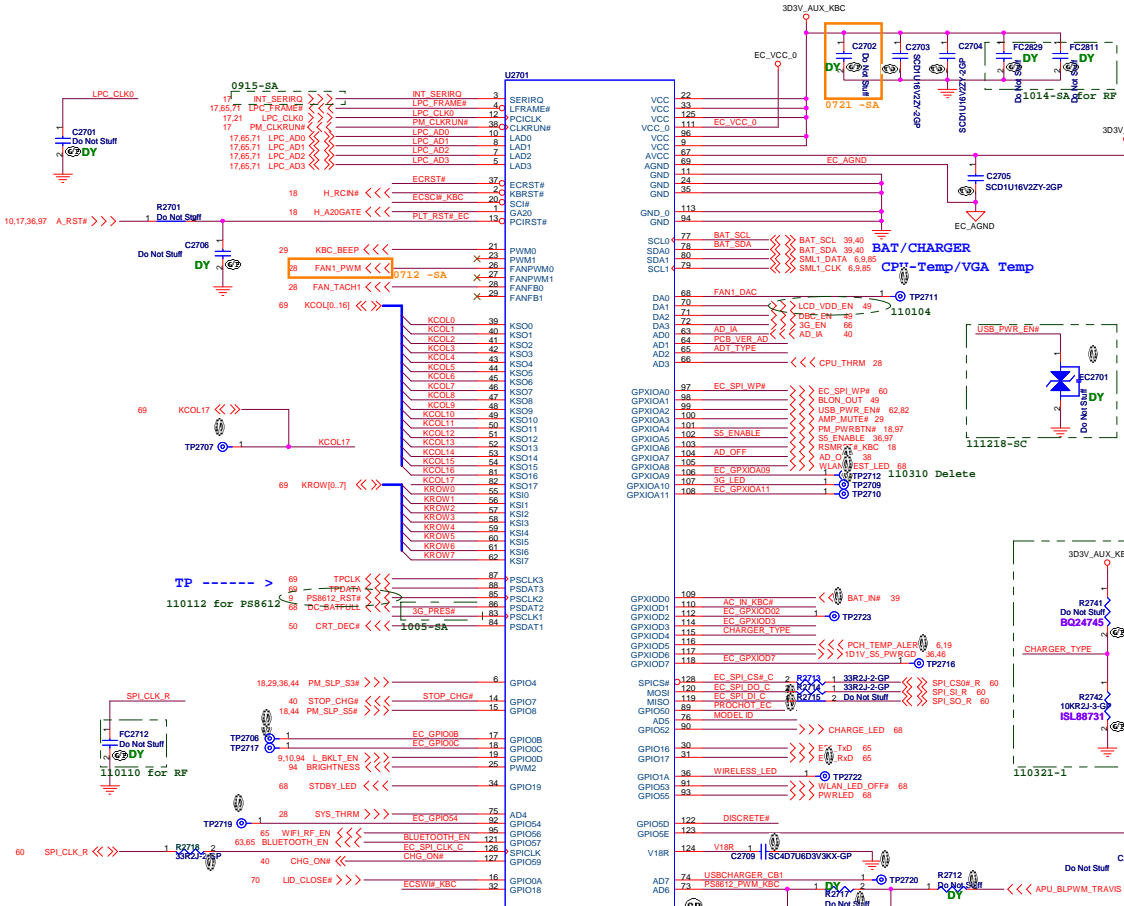
**JE40-SB**

Rev

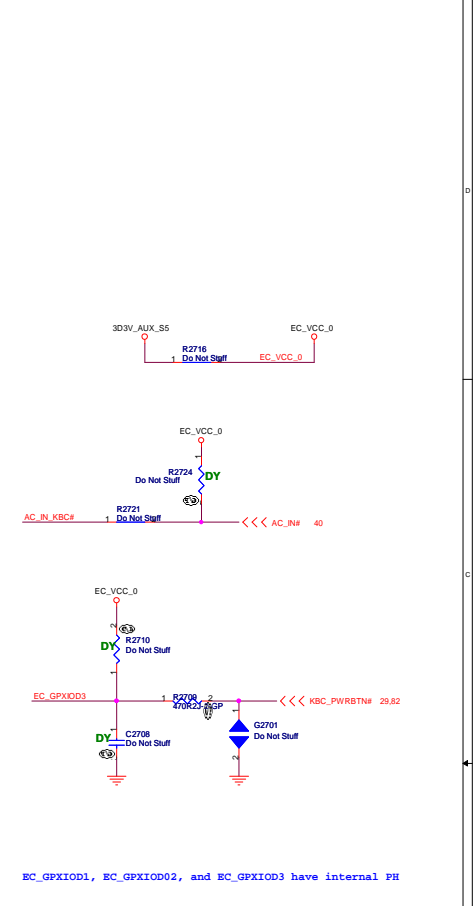
**SB**

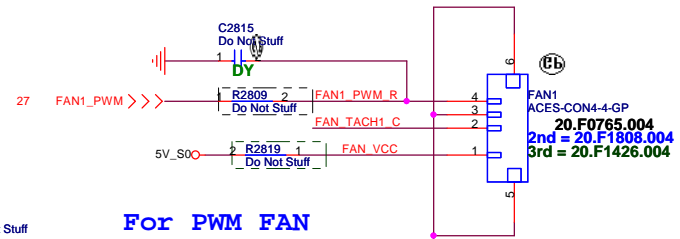
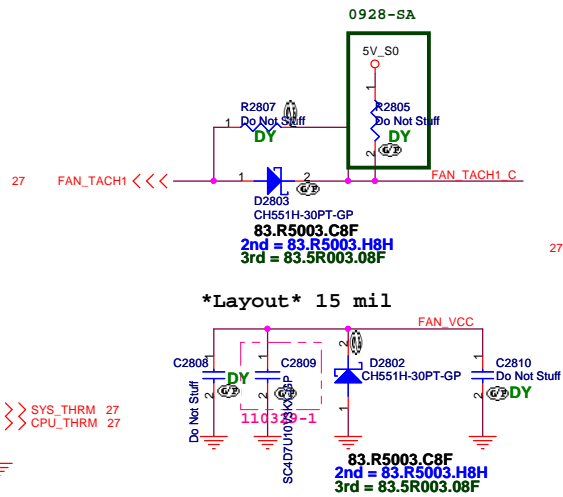
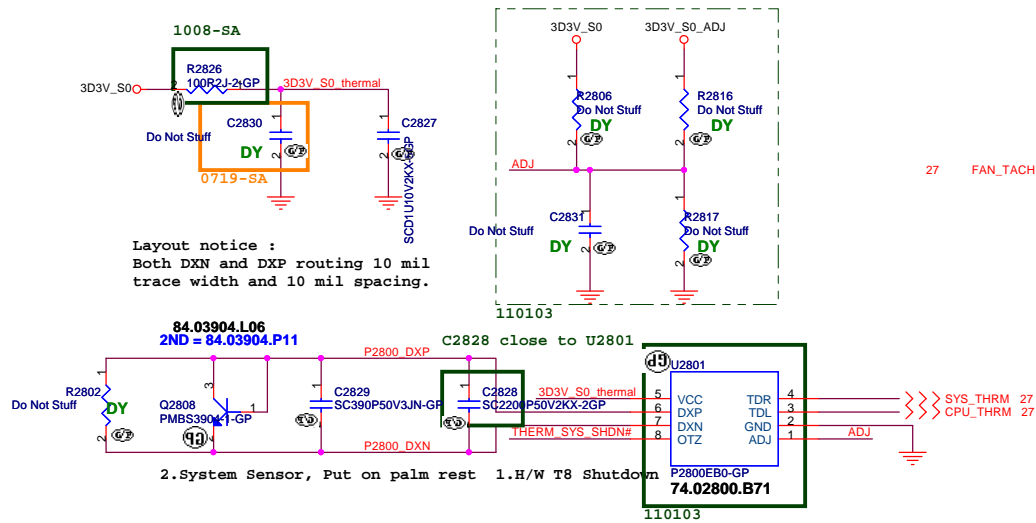
Date: Friday, March 25, 2011

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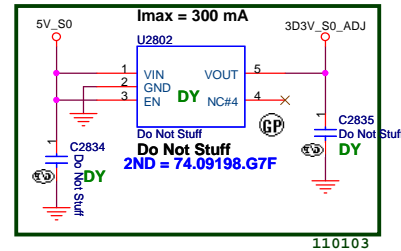
w/ 3G: PU 10K to 3D3V\_S0 ; w/o 3G: PD 10K GND



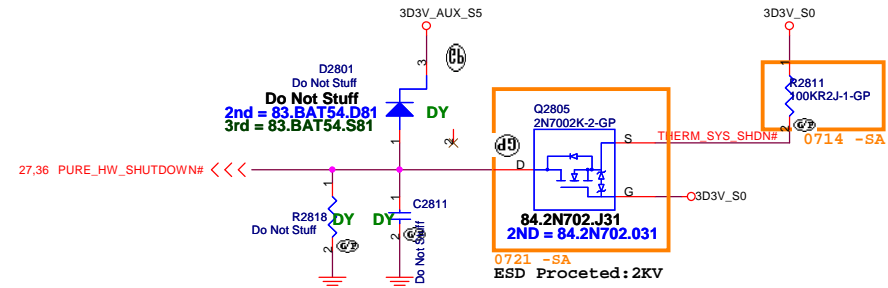


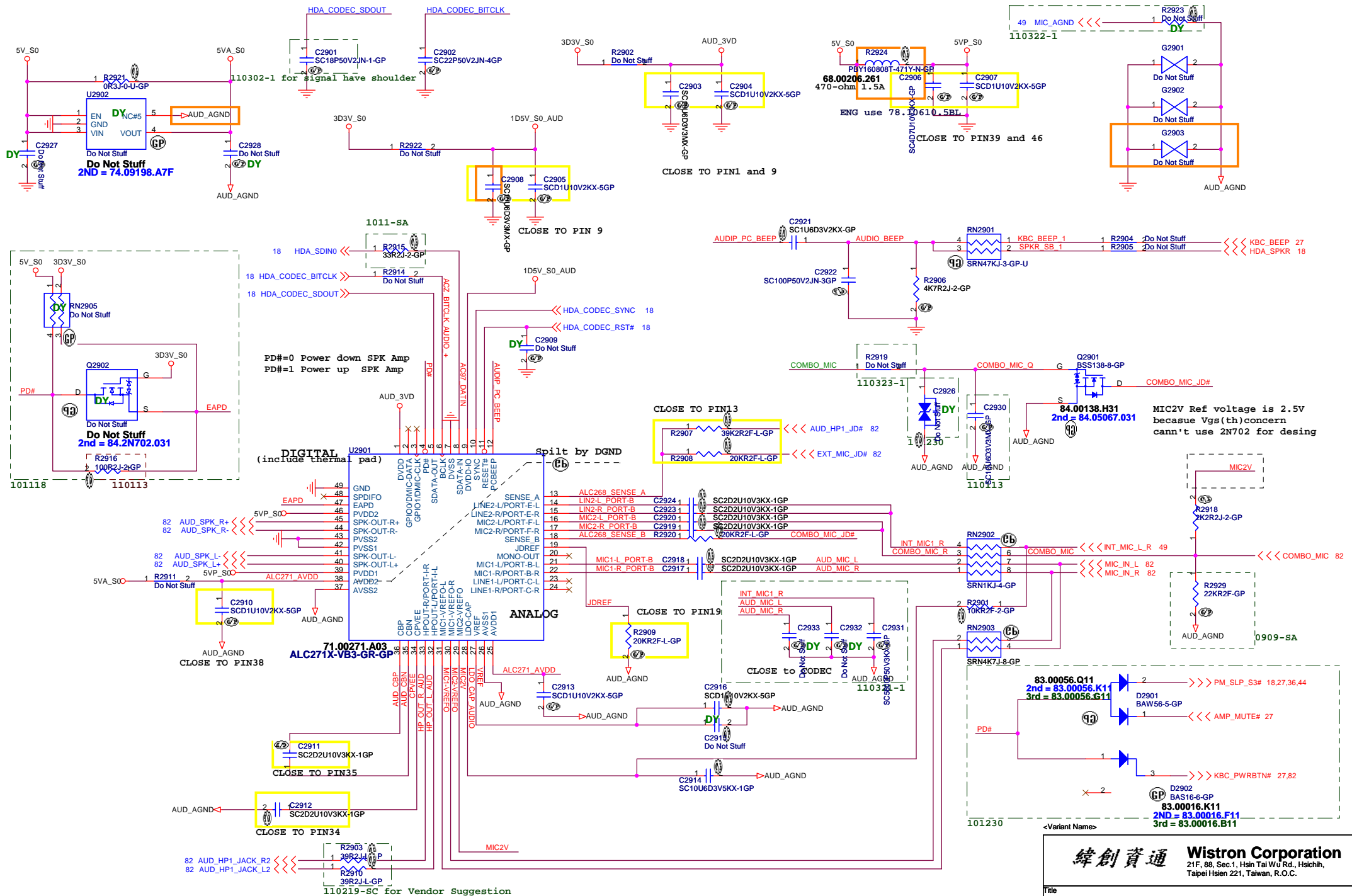
ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



VGA Thermal sensor P2800





**緯創資通**

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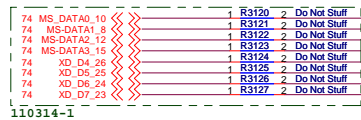
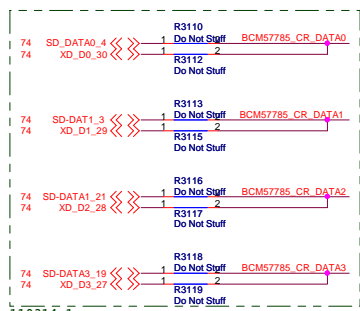
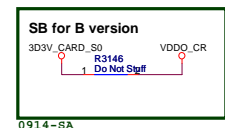
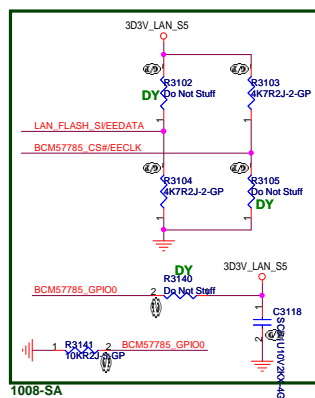
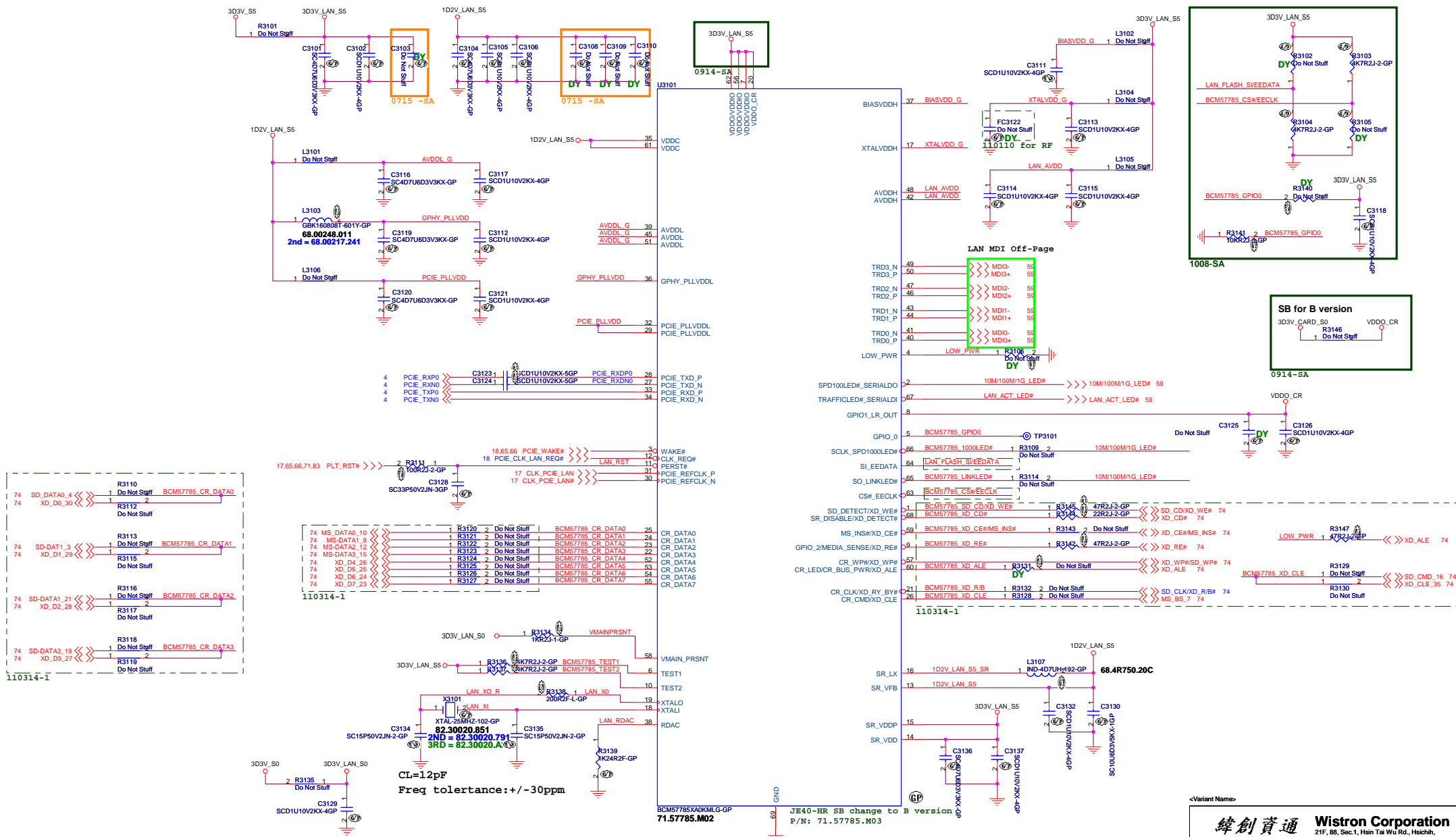
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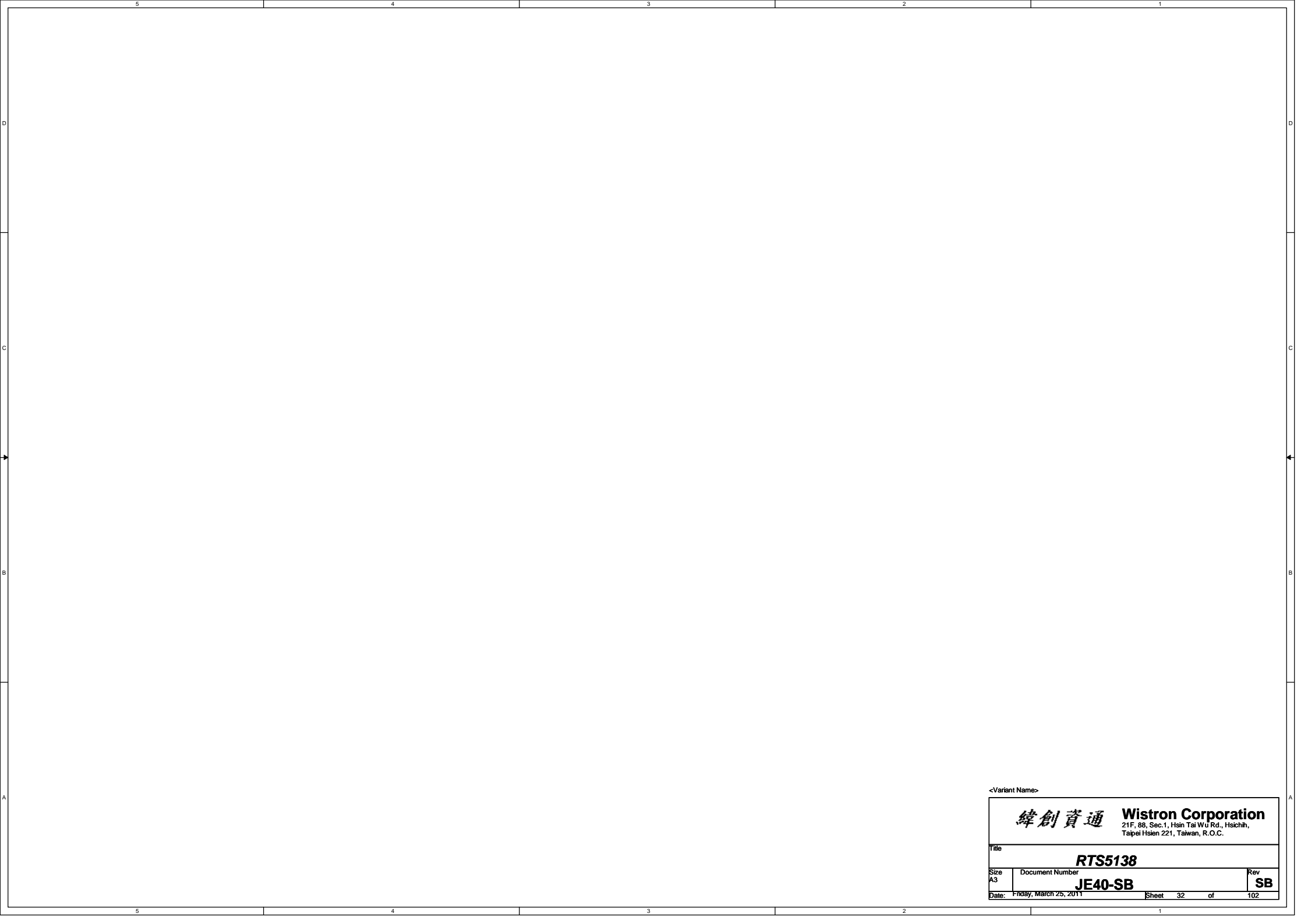
Size A3	Document Number	Rev
	<b>JE40-SB</b>	<b>SB</b>
Date: Wednesday, March 30, 2011	Sheet 29 of 102	

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>AMP</b>			
Size	Document Number		Rev
A3	<b>JE50-SB</b>		<b>SB</b>
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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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<b>Title</b>			
<b>RTS5138</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
A3	<b>JE40-SB</b>		<b>SB</b>
<b>Date:</b> Friday, March 25, 2011		<b>Sheet</b> 32	<b>of</b> 102



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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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Size	Document Number		Rev
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<Variant Name>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
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Document Number

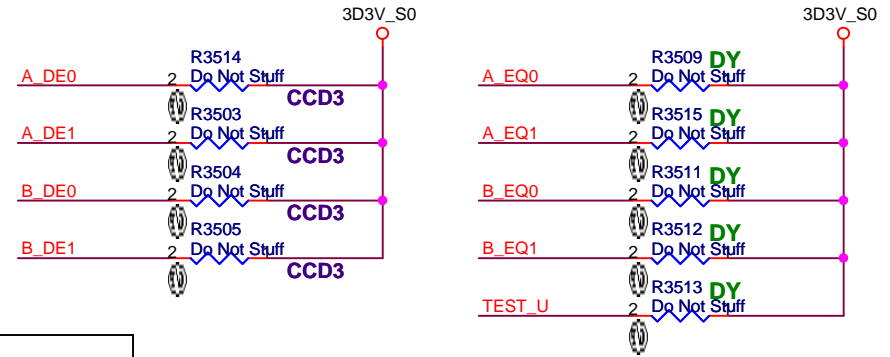
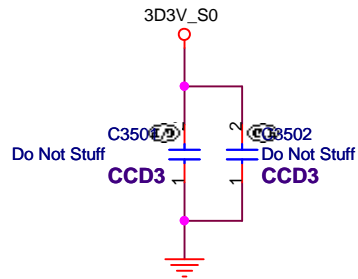
**JE40-SB**

Rev

**SB**

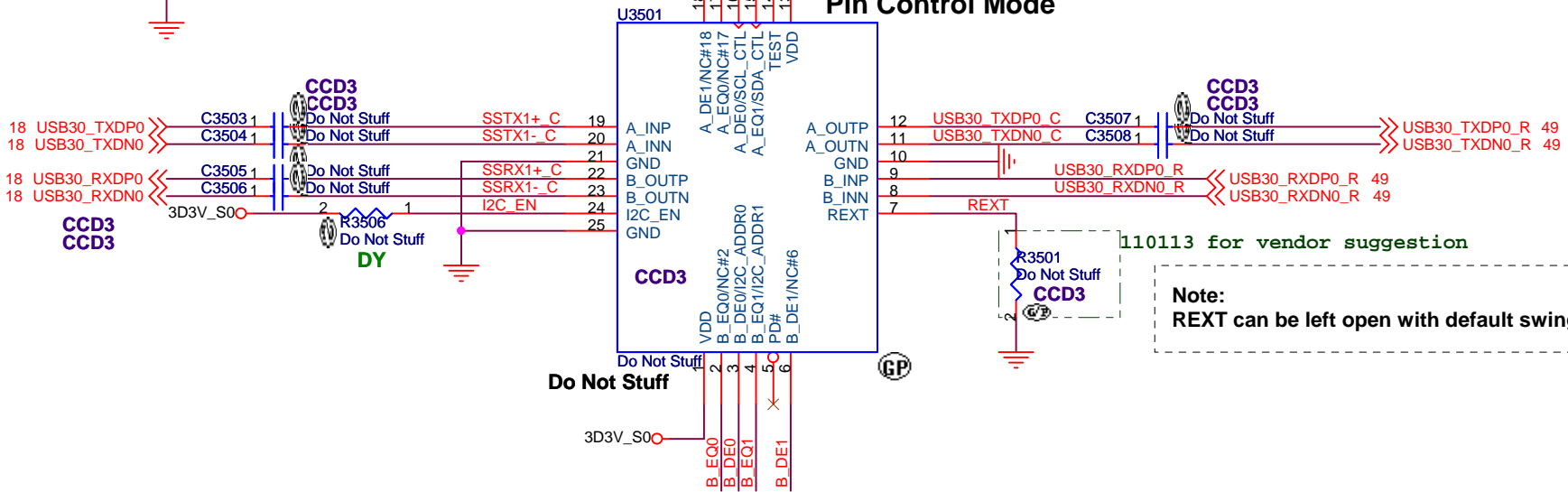
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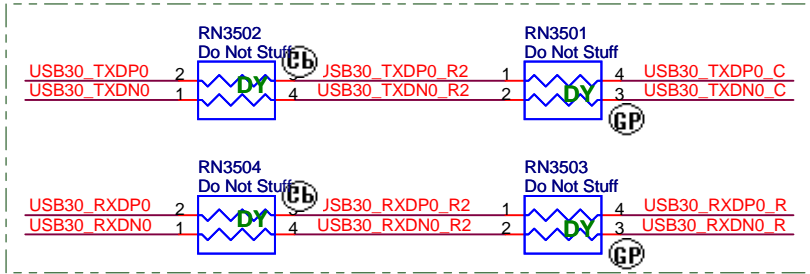
**\*For PS8710B: VDD = 3.3V**

**Pin Control Mode**



110113 for vendor suggestion

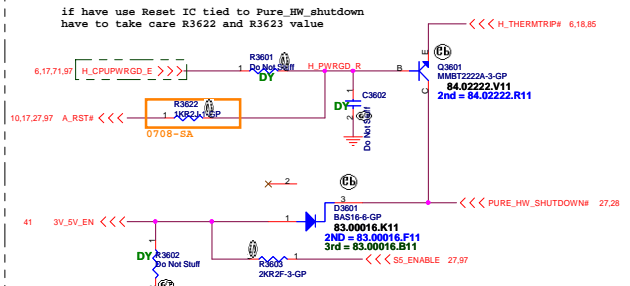
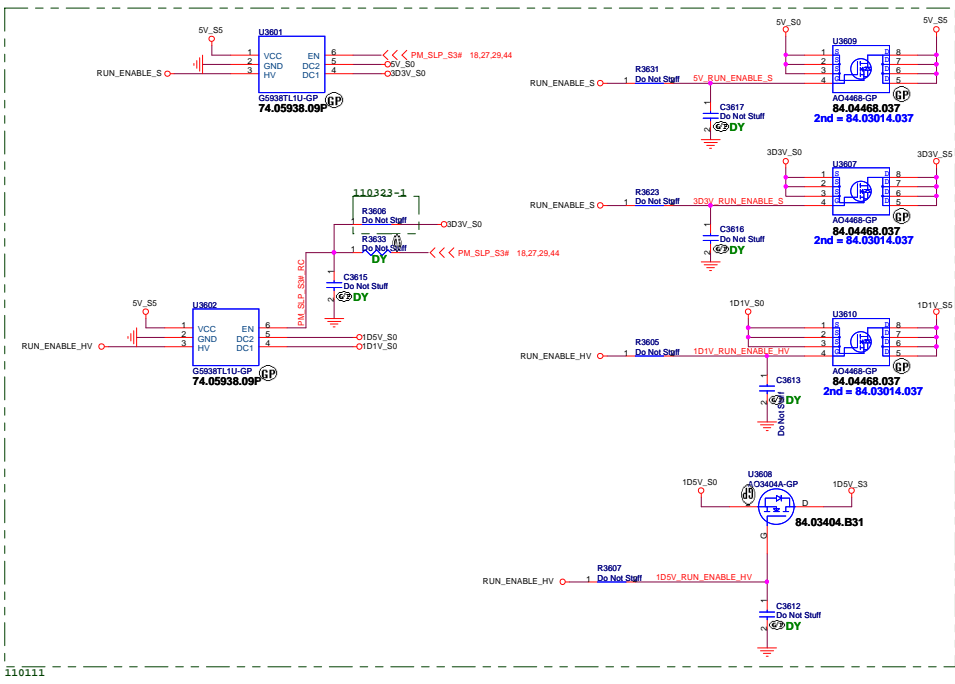
**Note:**  
REXT can be left open with default swing setting



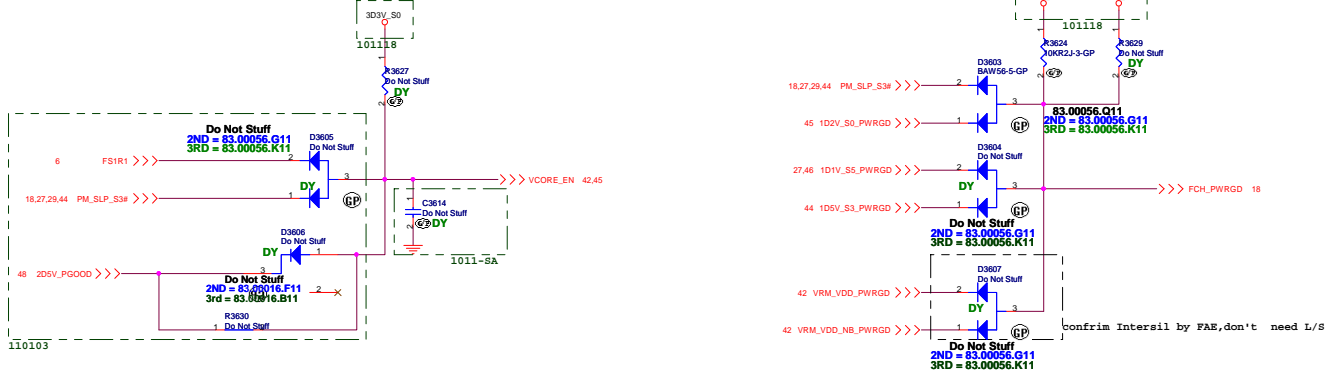
110113

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Reserved</b>			
Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>	
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**Power Sequence**



D

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C

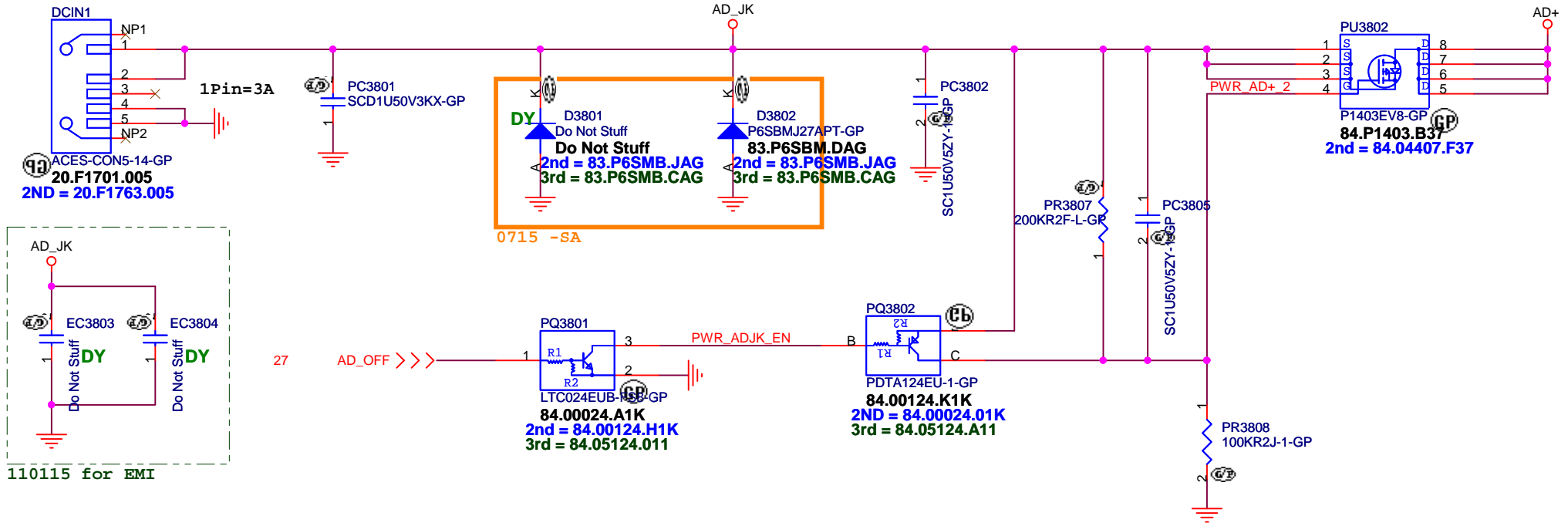
B

A

<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Reserved</b>	
Size A4	Document Number <b>JE40-SB</b>
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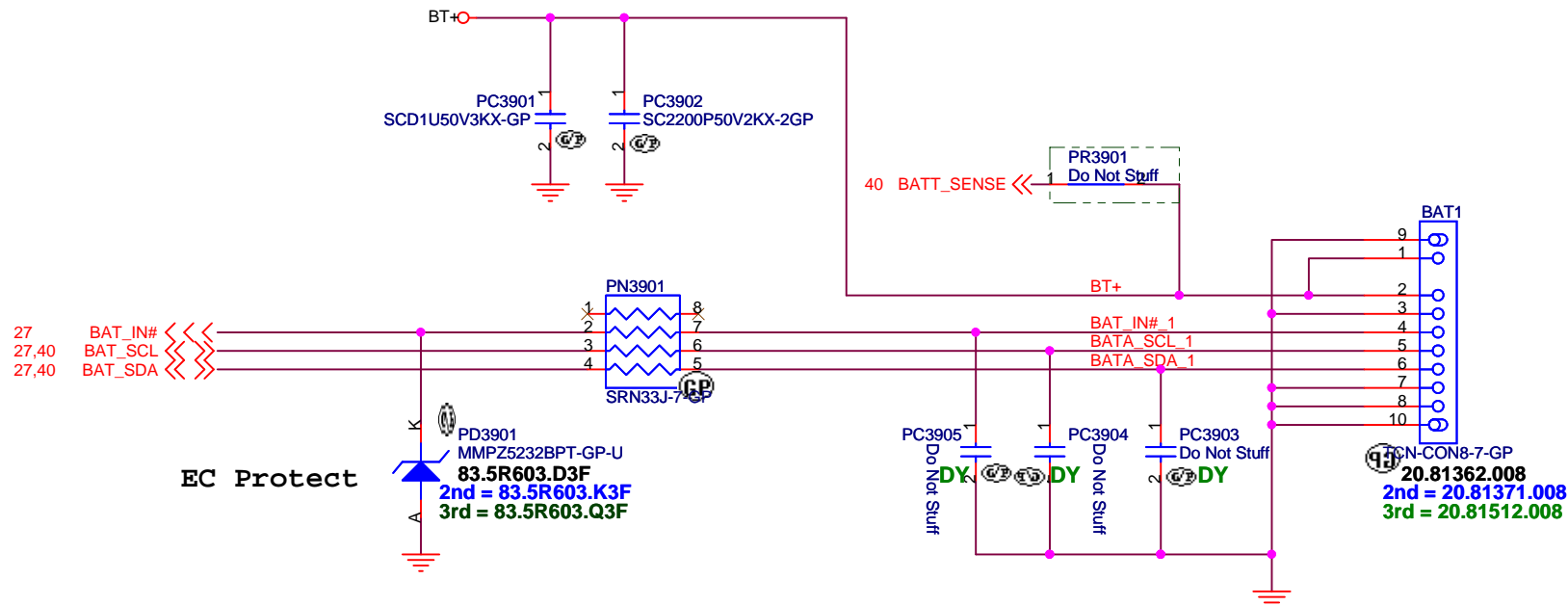
# Adaptor in to generate DCBATOUT



<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>DCIN JACK</b>		
Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
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# BATTERY CONNECTOR



<Variant Name>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**BATT\_CONN**

Size

A4

Document Number

**JE40-SB**

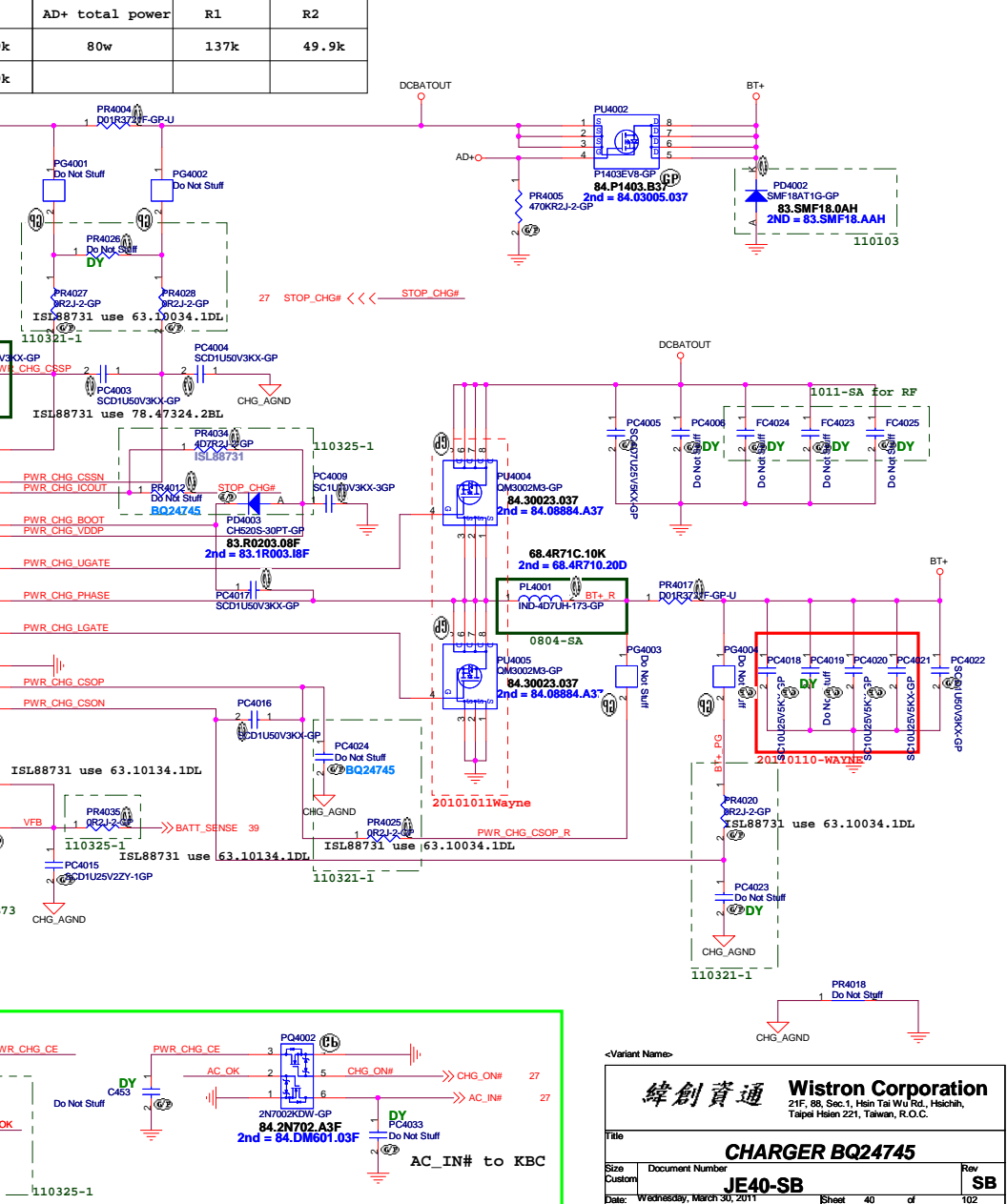
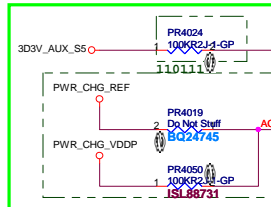
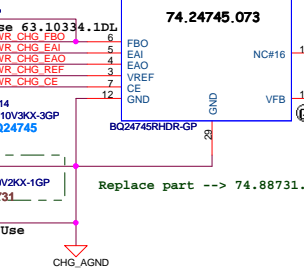
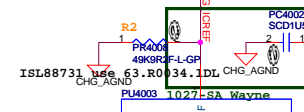
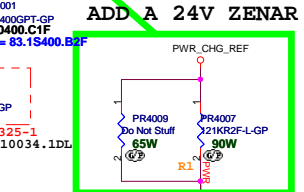
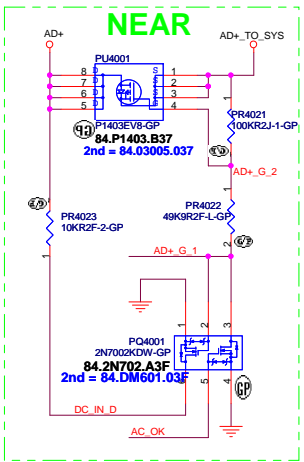
Rev

**SB**

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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
<b>90w</b>	121k	49.9k			



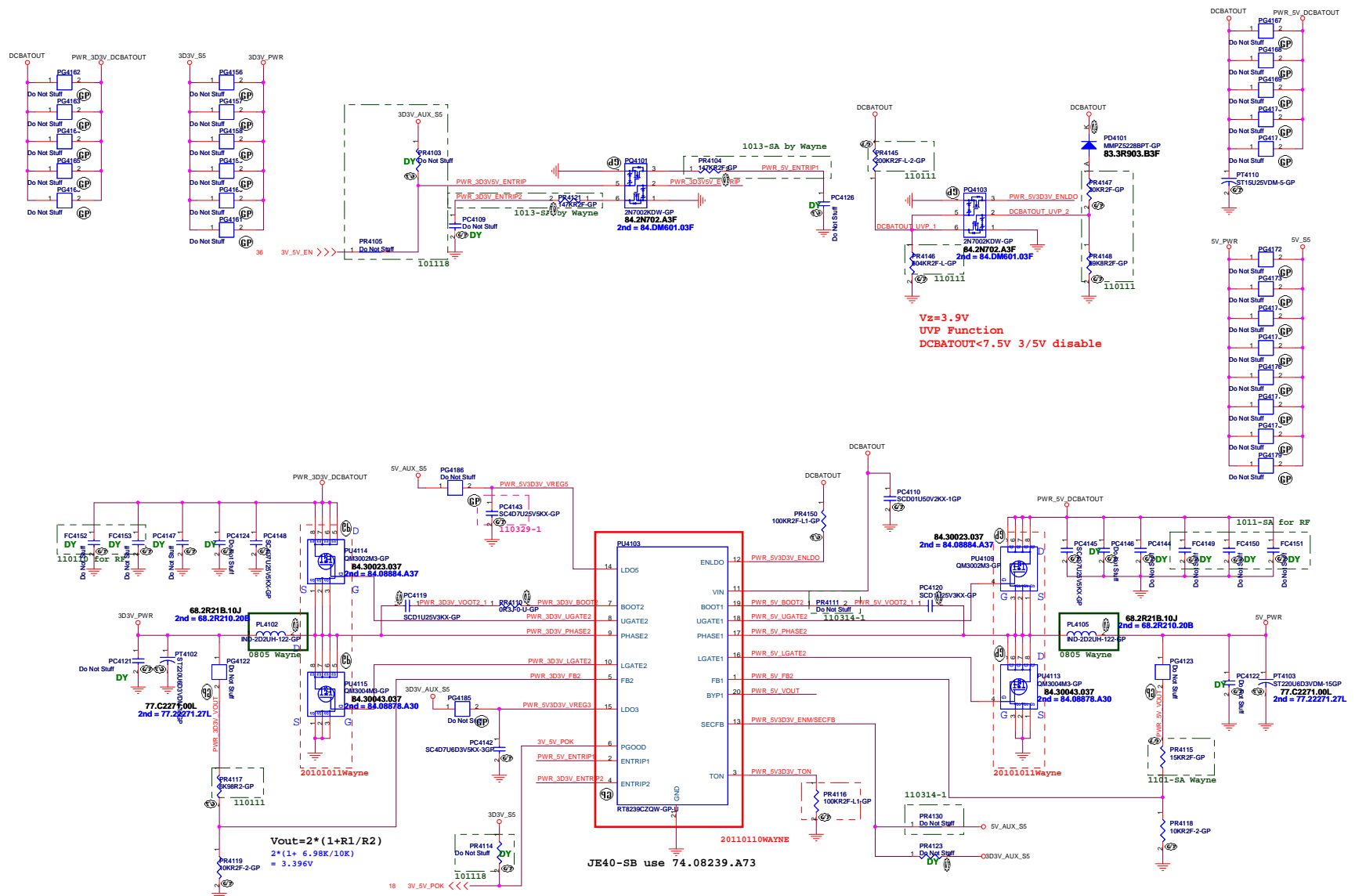
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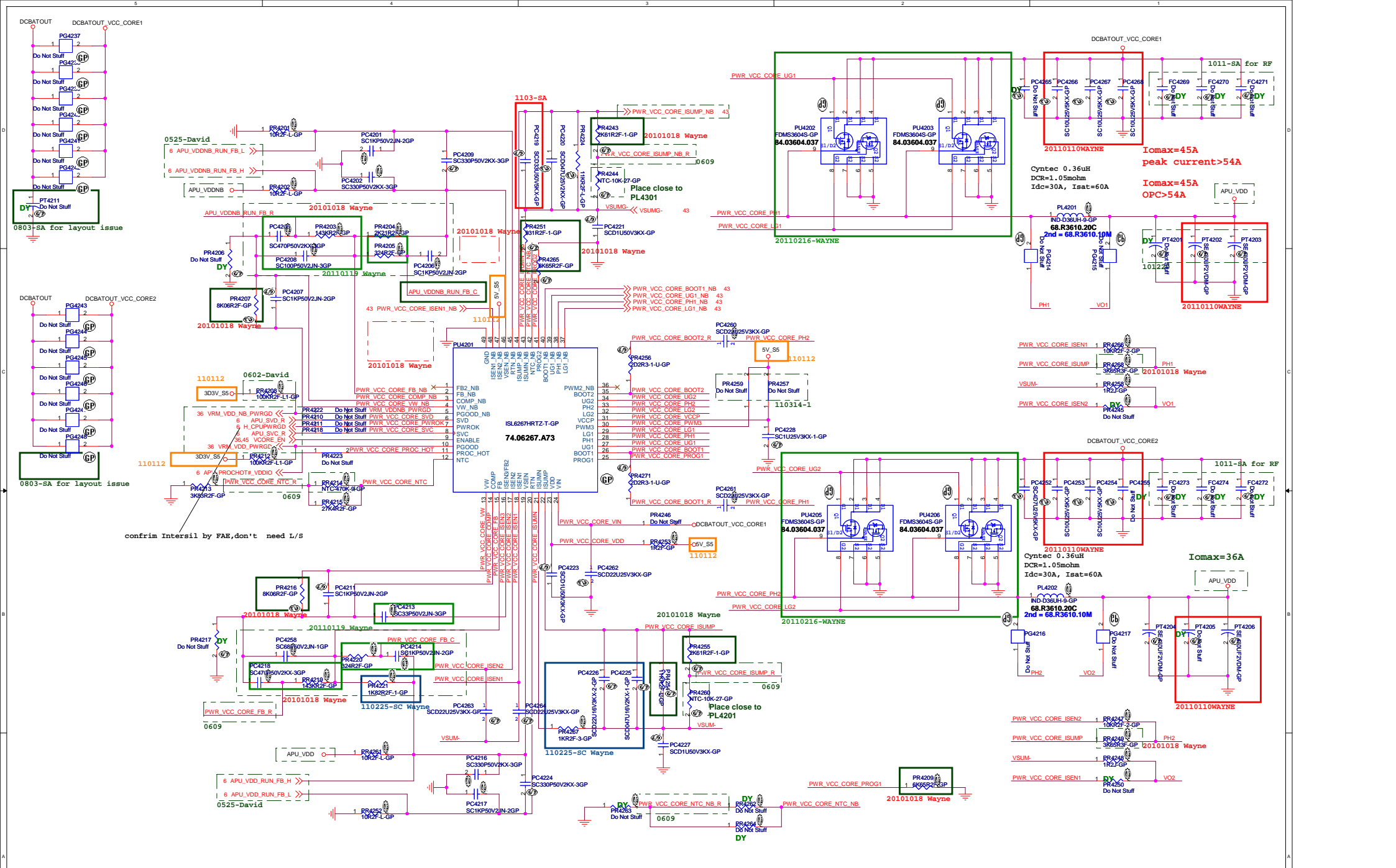
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

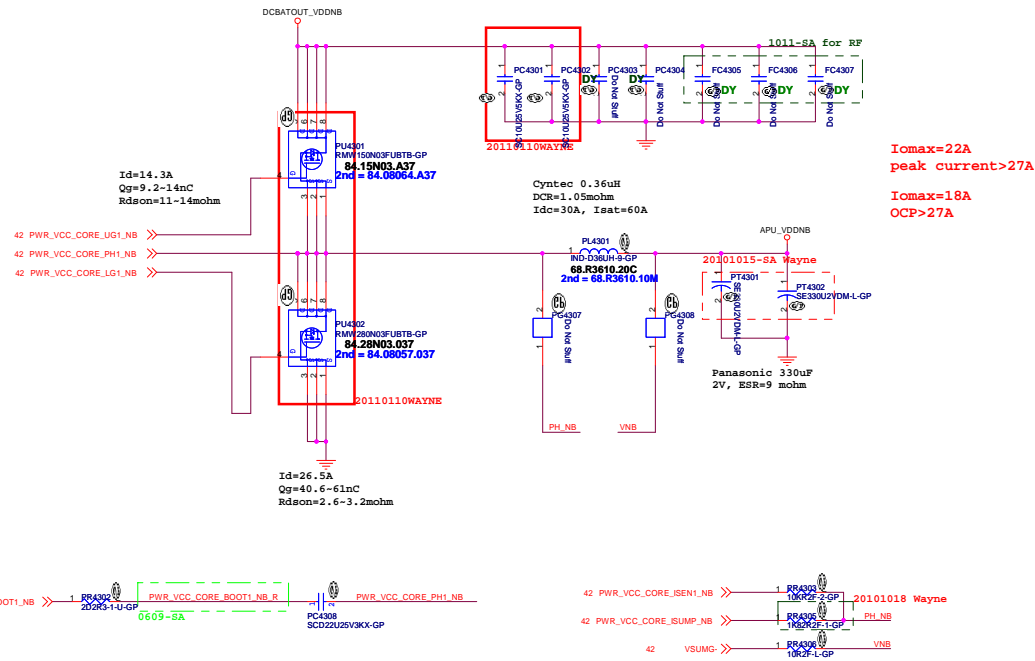
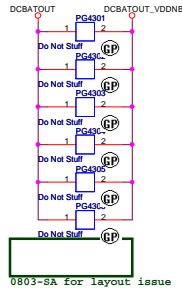
**CHARGER BQ24745**

Title	Document Number	Rev
	<b>JE40-SB</b>	<b>SB</b>
Date: Wednesday, March 30, 2011	Sheet 40 of 102	





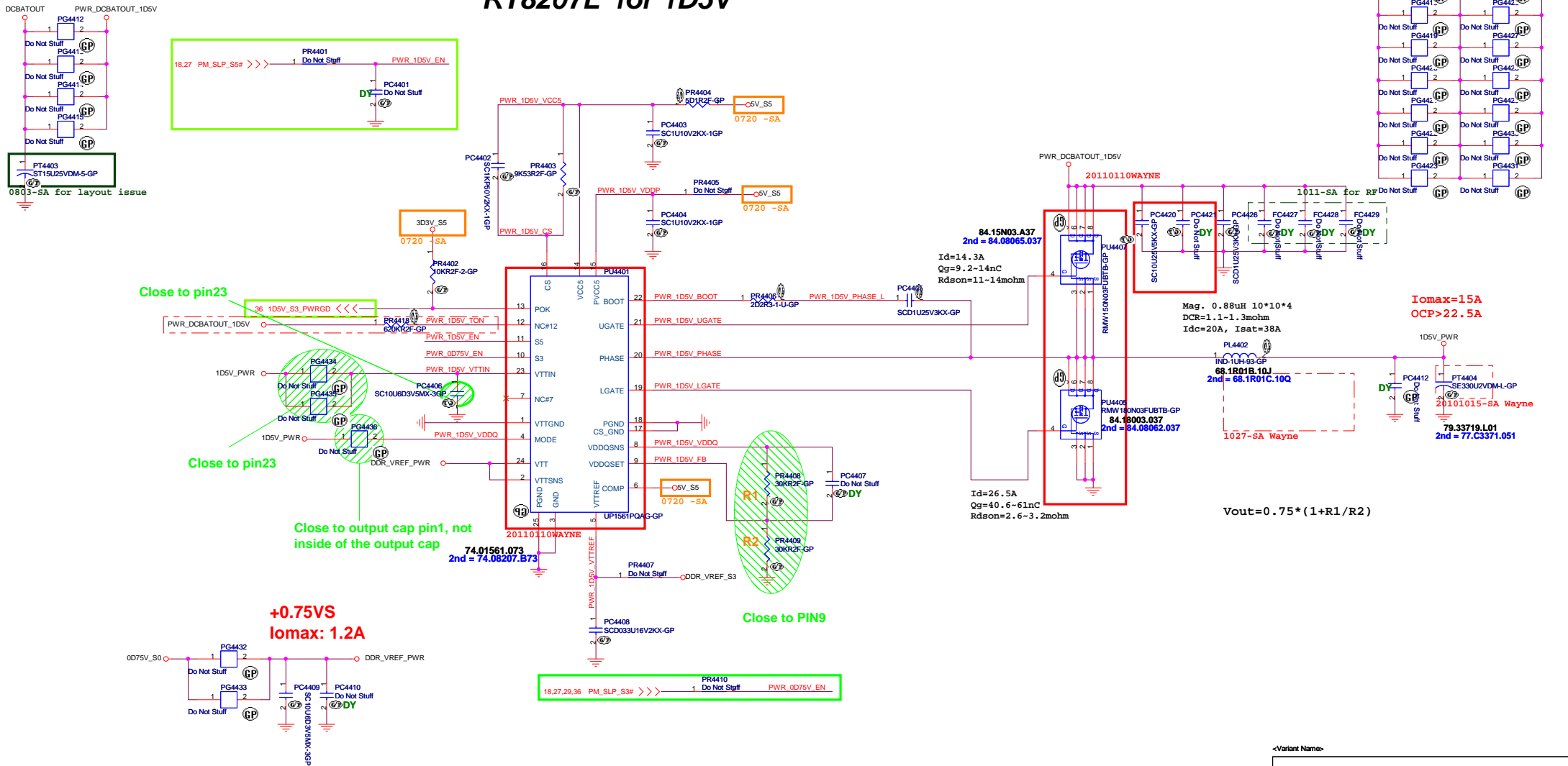




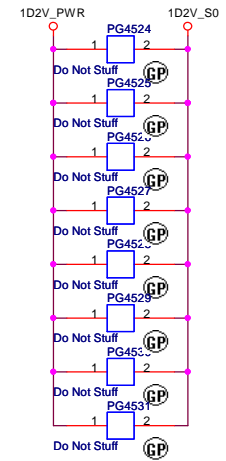
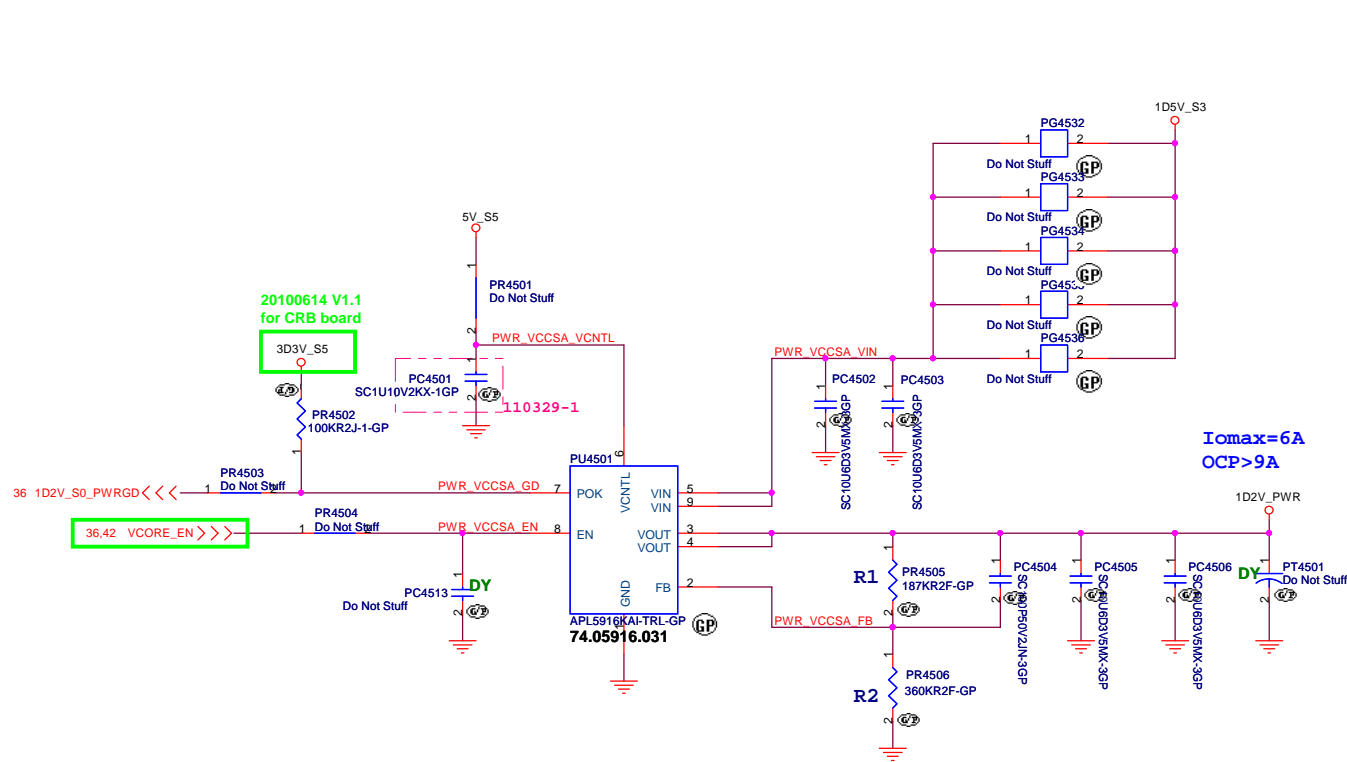
Iomax=22A  
peak current>27A

Iomax=18A  
OCP>27A

# RT8207L for 1D5V



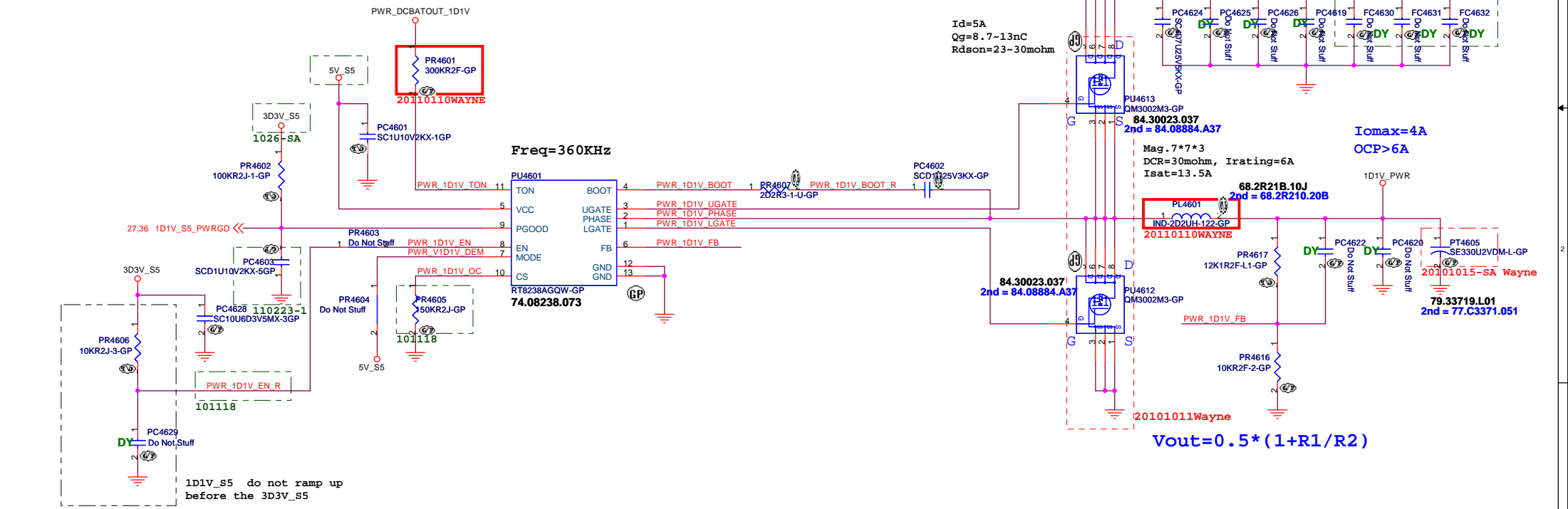
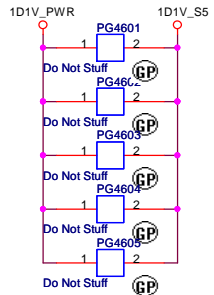
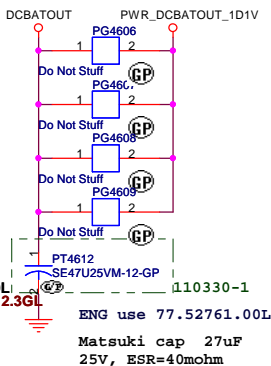
# APL5916 for VDDR&VDDP(1D2V\_S0)



<Variant Name>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>APL5916(1D2V_S0)</b>		
Size A3	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
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# RT8238 for 1D1V\_S5

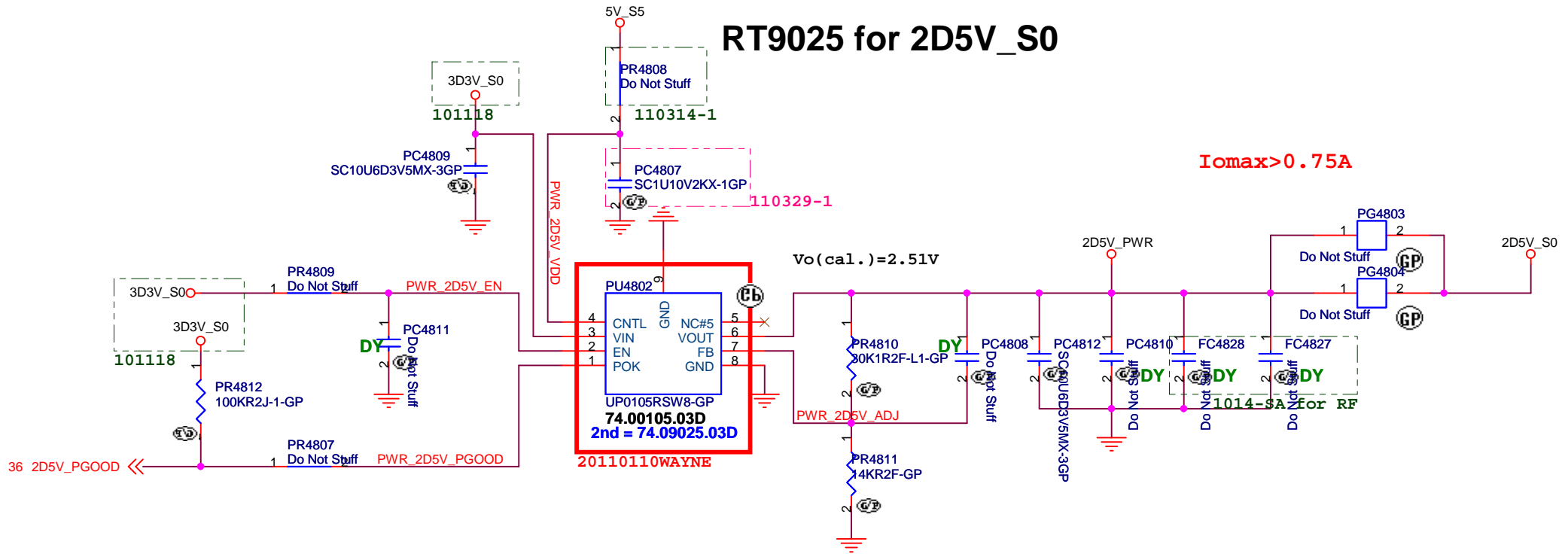


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<Variant Name>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size	Document Number				Rev
A4	<b>JE40-SB</b>				<b>SB</b>
Date:	Friday, March 25, 2011		Sheet	47	of 102

# RT9025 for 2D5V\_S0

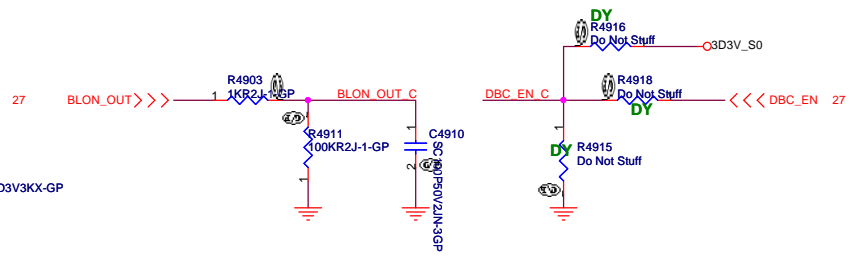
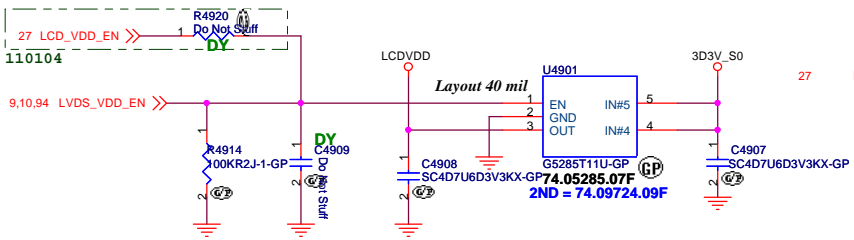
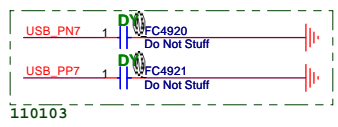
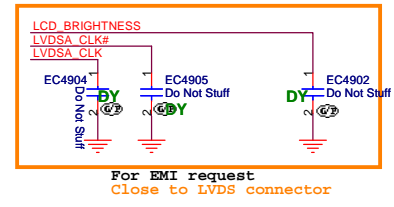
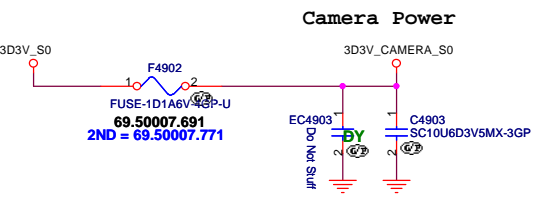
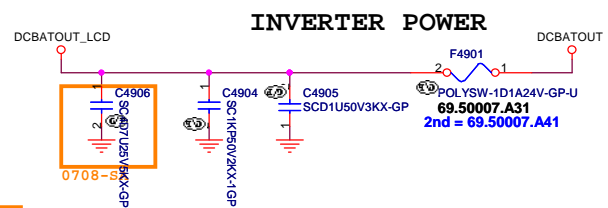
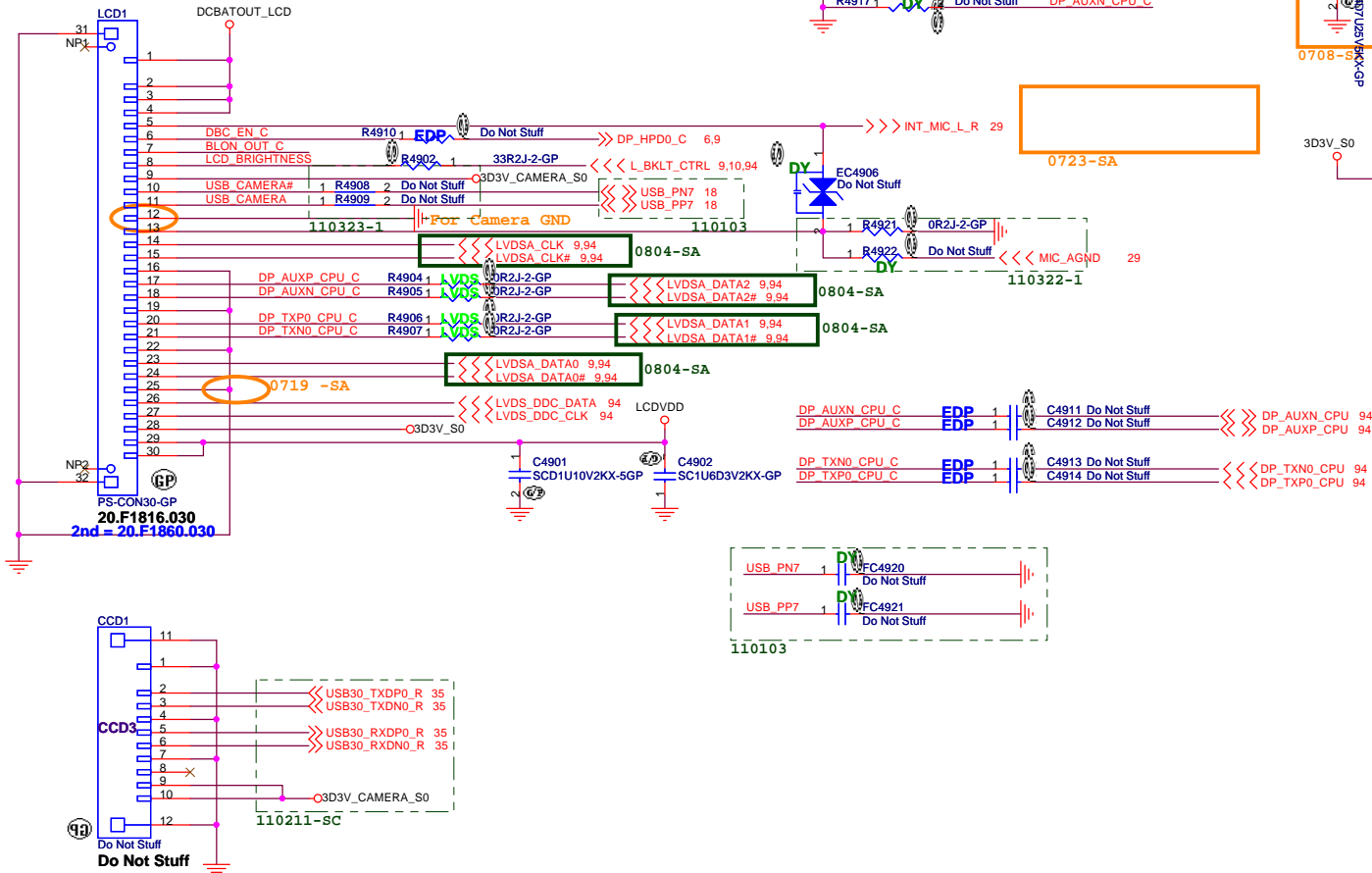


<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>RT9025(2D5V_S0)</b>		
Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
Date: Tuesday, March 29, 2011	Sheet 48 of	102



# LVDS VS EDP Co-layout CONNECTOR(30 Pin)

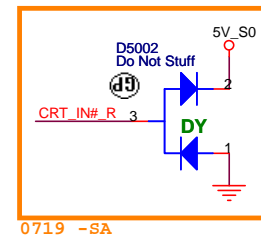
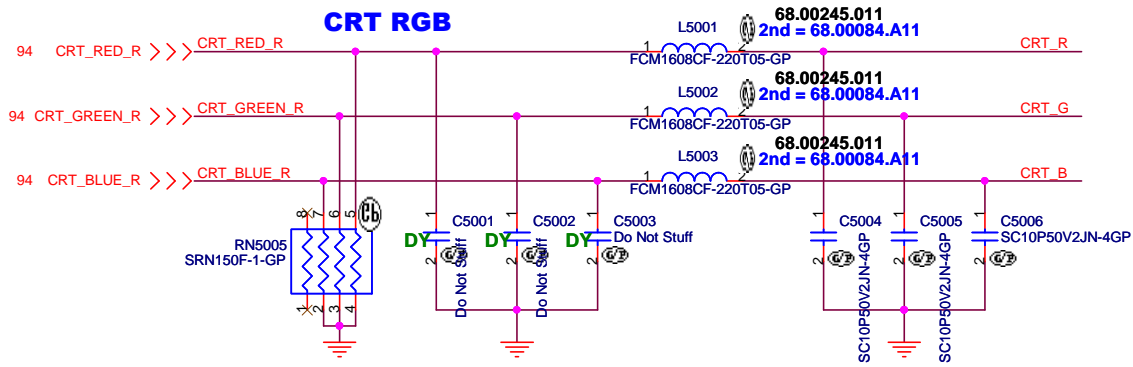


**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

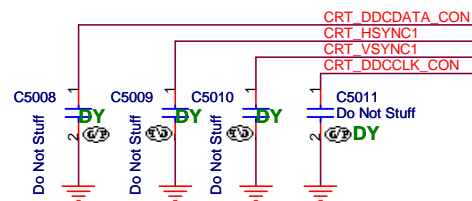
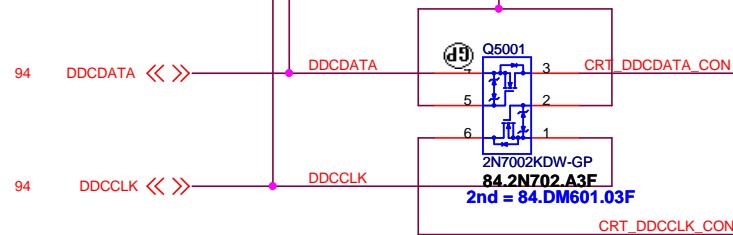
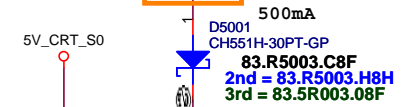
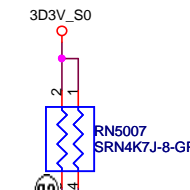
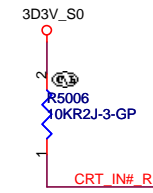
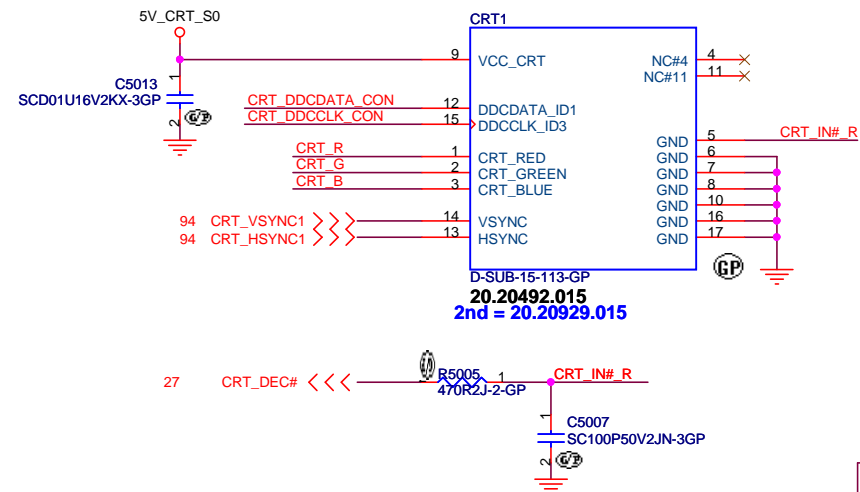
Size A3 | Document Number: **JE40-SB** | Rev: **SB**

Date: Monday, March 28, 2011 | Sheet 49 of 102



0719 -SA

0715 -SA



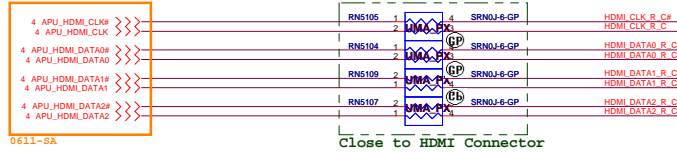
<Variant Name>

**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

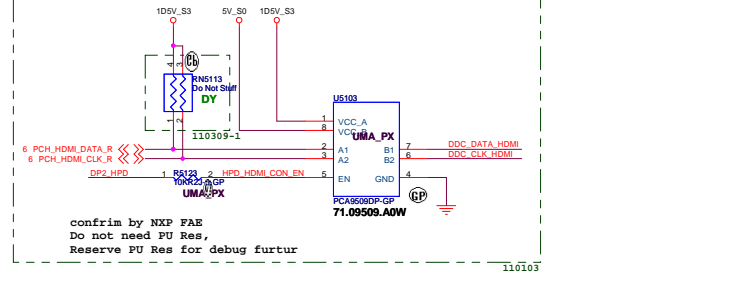
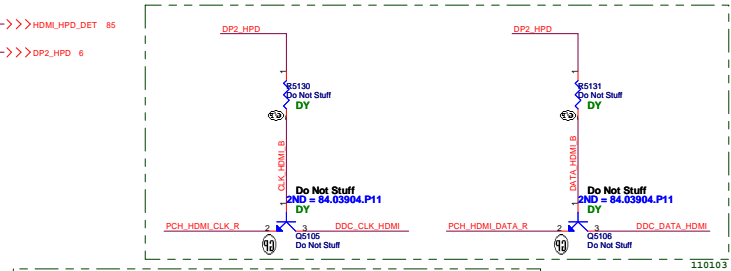
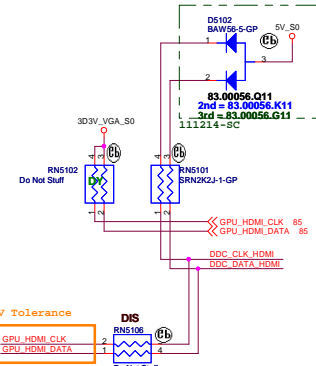
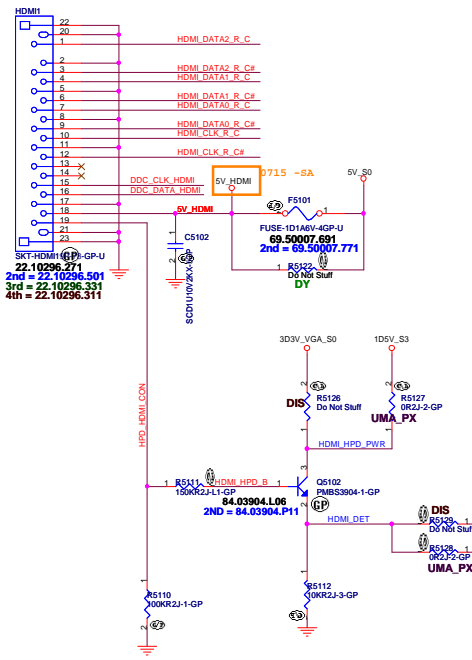
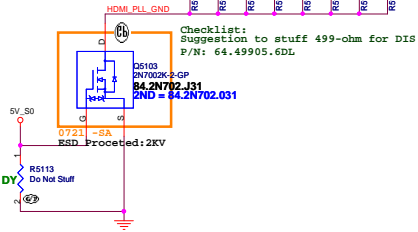
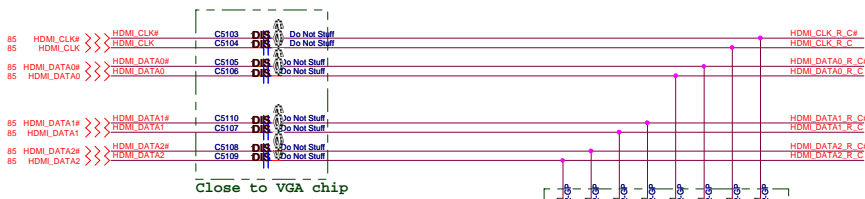
Title			<b>CRT Connector</b>
Size	Document Number	Rev	
Custom	<b>JE40-SB</b>	<b>SB</b>	
Date:	Monday, March 28, 2011	Sheet 50	of 102

HDMI CONN

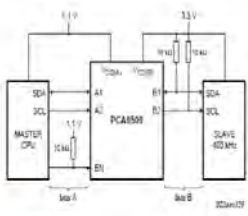
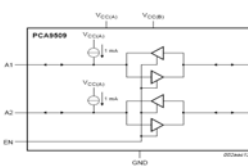
# HDMI Level Shifter & CONNECTOR



HDMI DISCRETE/ UMA Co-lay



Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.



(Blanking)

<Variant Name>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>eDP</b>					
Size	Document Number				Rev
A4	<b>JE40-SB</b>				<b>SB</b>
Date:	Friday, March 25, 2011			Sheet 52	of 102

(Blanking)

<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**JE40-SB**

Rev

**SB**

Date: Friday, March 25, 2011

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(Blanking)

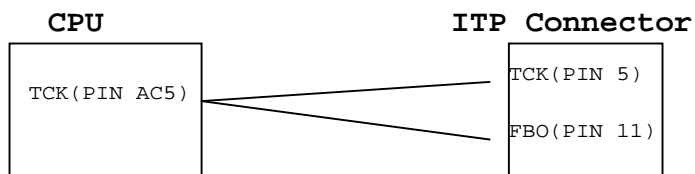
<Variant Name>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size	Document Number				Rev
A4	<b>JE40-SB</b>				<b>SB</b>
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**SSID = User.Interface**

## *ITP Connector*

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

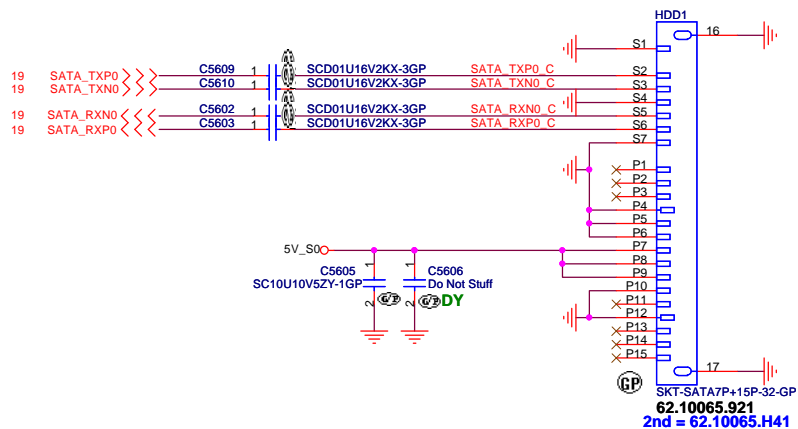


<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>ITP</b>			
Size A4	Document Number		Rev
	<b>JE40-SB</b>		<b>SB</b>
Date: Friday, March 25, 2011	Sheet	55	of 102

**SSID = SATA**

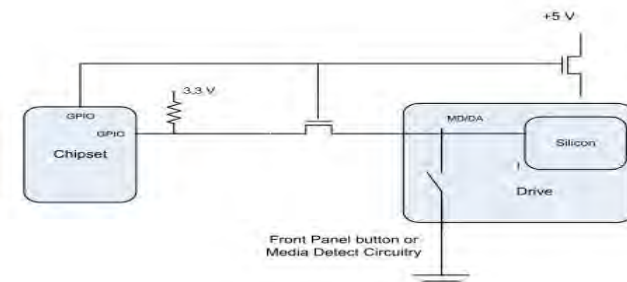
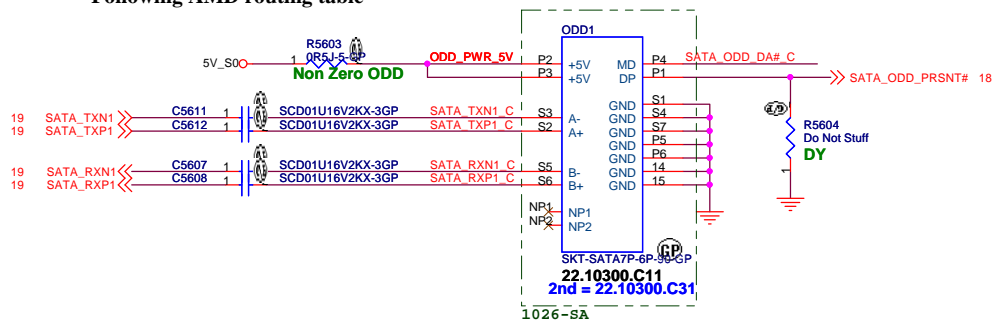
# SATA HDD Connector



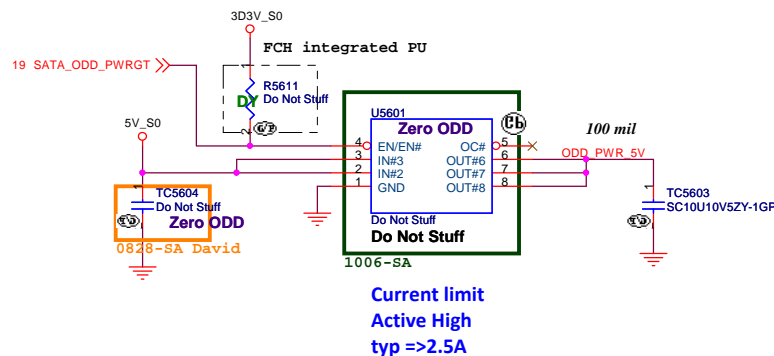
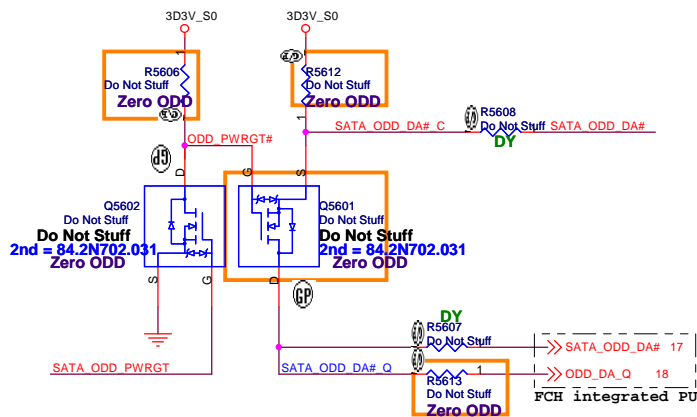
# ODD Connector

SATA\_RX- and SATA\_RX+ Trace Length match within 10 mil

Following AMD routing table



When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	HDD/ODD		
Size A3	Document Number	JE40-SB	
Date: Monday, March 28, 2011	Sheet	56	of 102
			Rev SB



(Blanking)

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>ESATA/USB Charger</b>			
Size	Document Number	Rev	
A3	<b>JE40-SB</b>	<b>SB</b>	
Date:	Friday, March 25, 2011	Sheet	57 of 102

(Blanking)

<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Audio Jack**

Size  
A4

Document Number

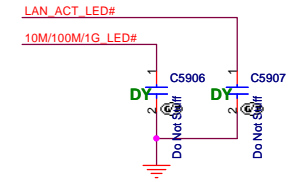
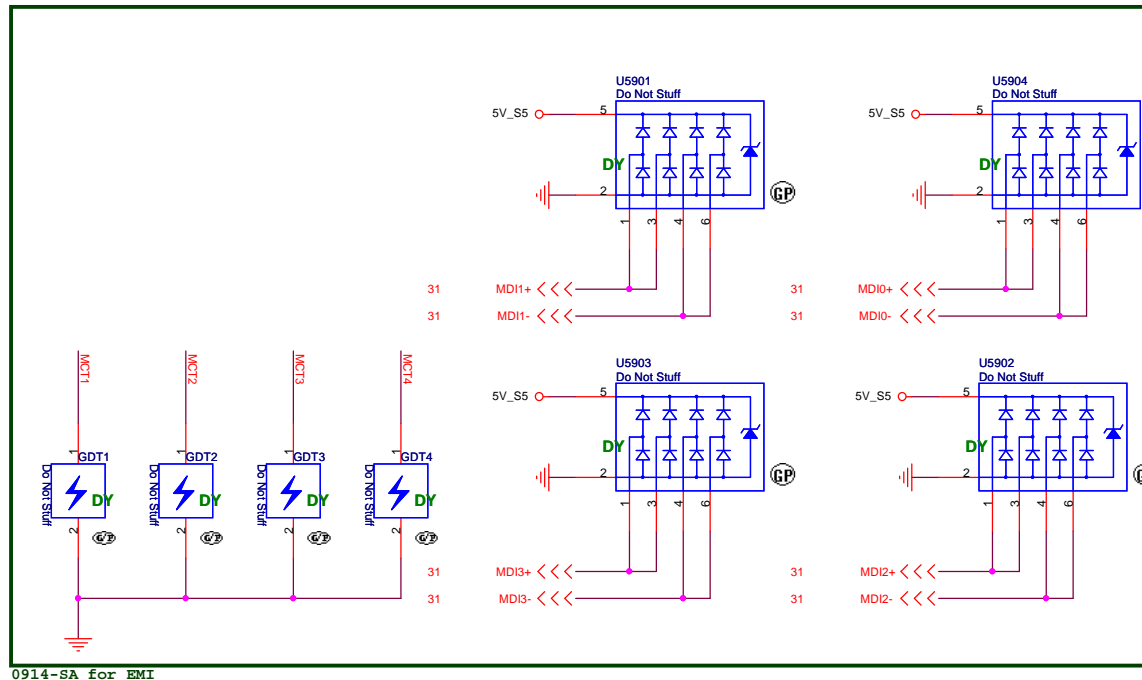
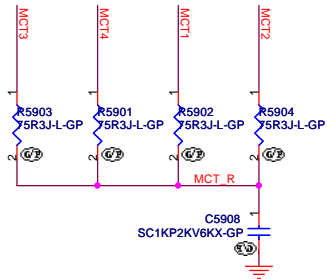
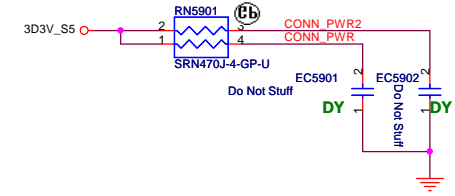
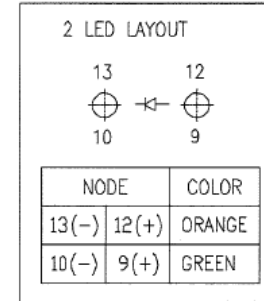
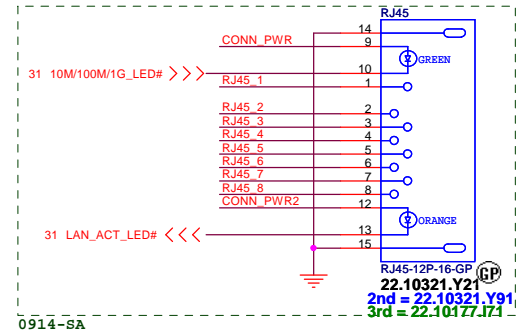
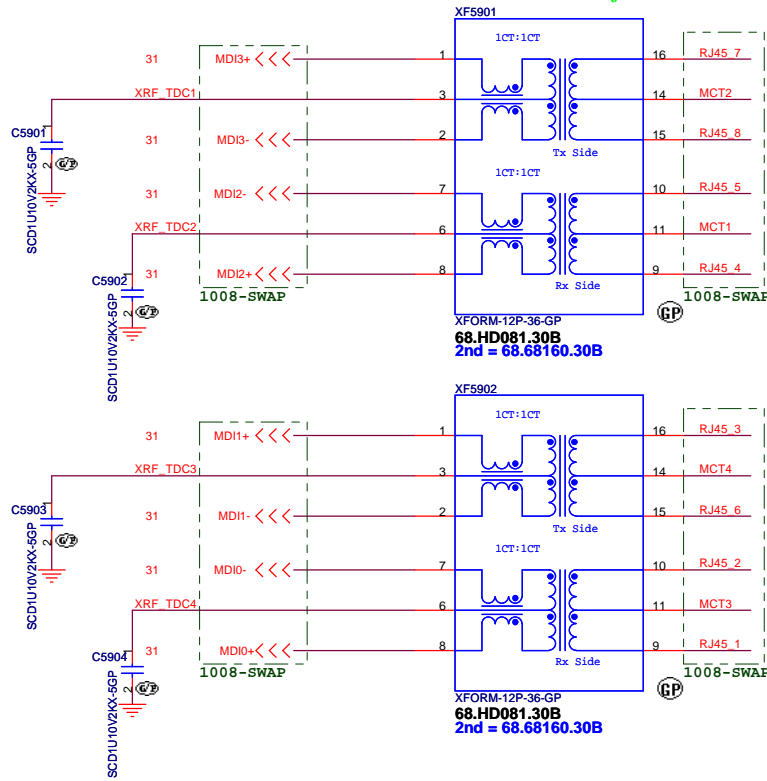
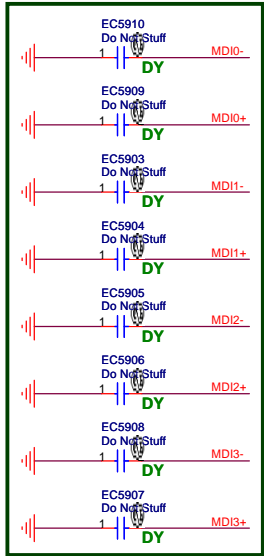
**JE40-SB**

Rev  
**SB**

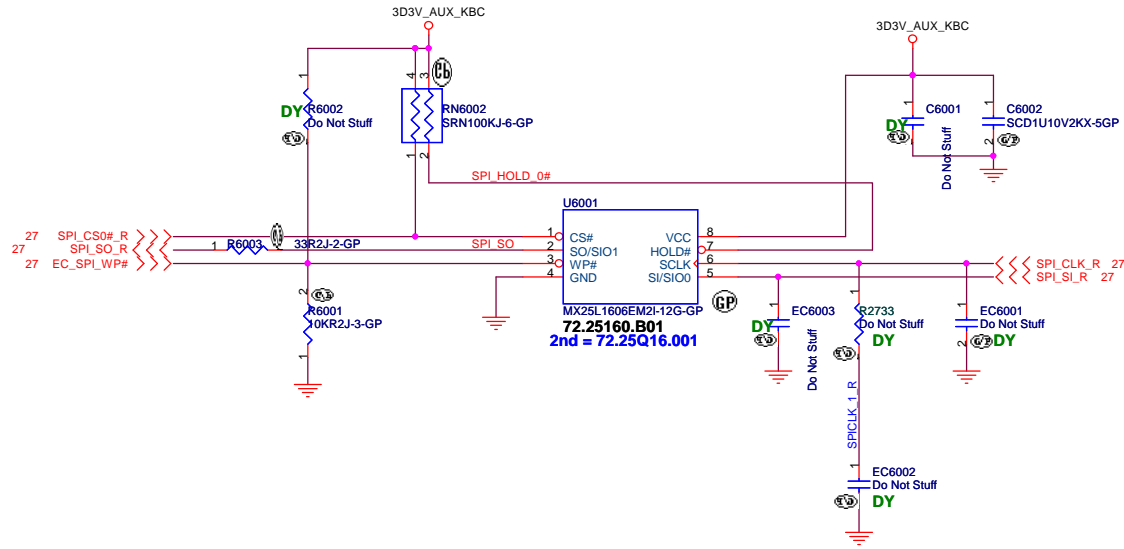
Date: Friday, March 25, 2011

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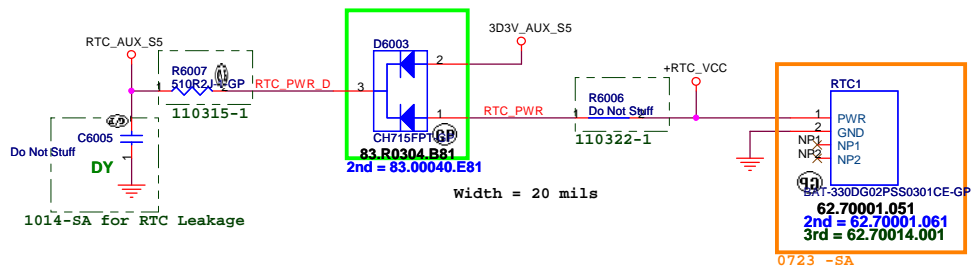
GIGA Lan Transformer



# SPI FLASH ROM (2M byte) for KBC



**SSID = RBATT**



5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>USB Power SW</b>			
<b>Size</b> A4	<b>Document Number</b> <b>JE40-SB</b>		<b>Rev</b> <b>SB</b>
<b>Date:</b> Friday, March 25, 2011		<b>Sheet</b> 61	<b>of</b> 102

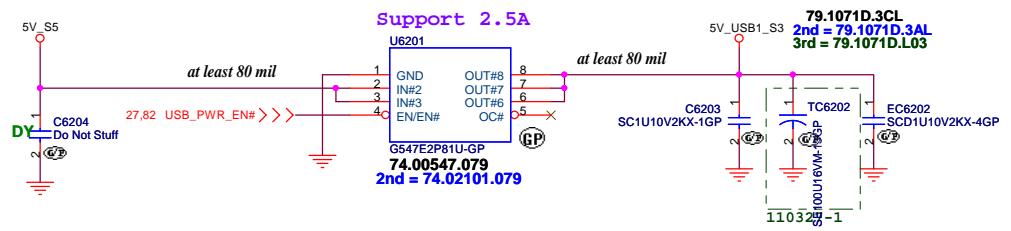
5

4

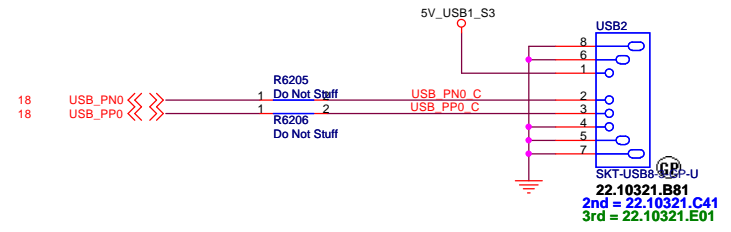
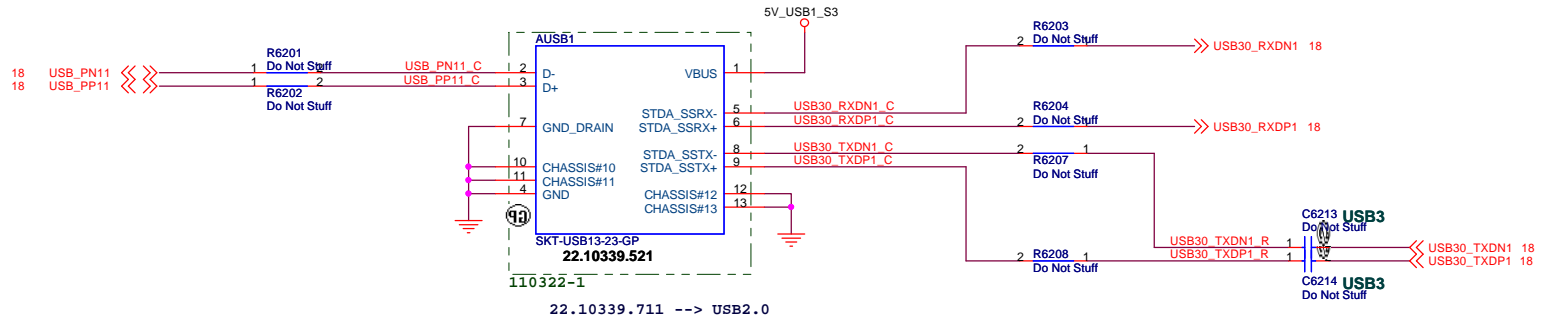
3

2

1



**USB3.0 CONNECTOR**



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

<Variant Name>

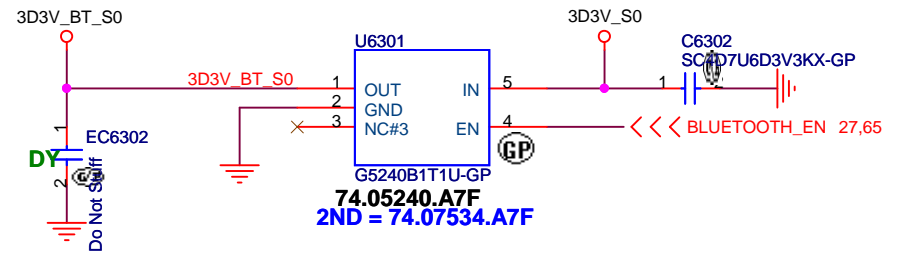
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**

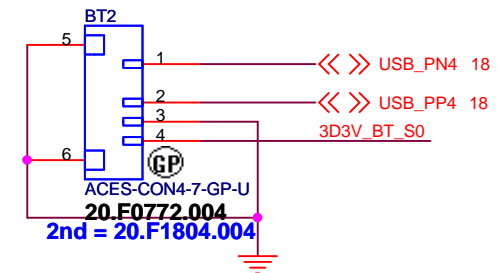
Size A3	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
Date: Wednesday, March 30, 2011	Sheet 62 of 102	

# ANNIE Bluetooth Module

1.5A / High Active Voltage 2V



EC6302 put near  
BLUE1 / all USB  
put one choke  
near connector  
by EMI request



<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>BLUE TOOTH</b>	
Size A4	Document Number <b>JE40-SB</b>
Date: Monday, March 28, 2011	Rev <b>SB</b>
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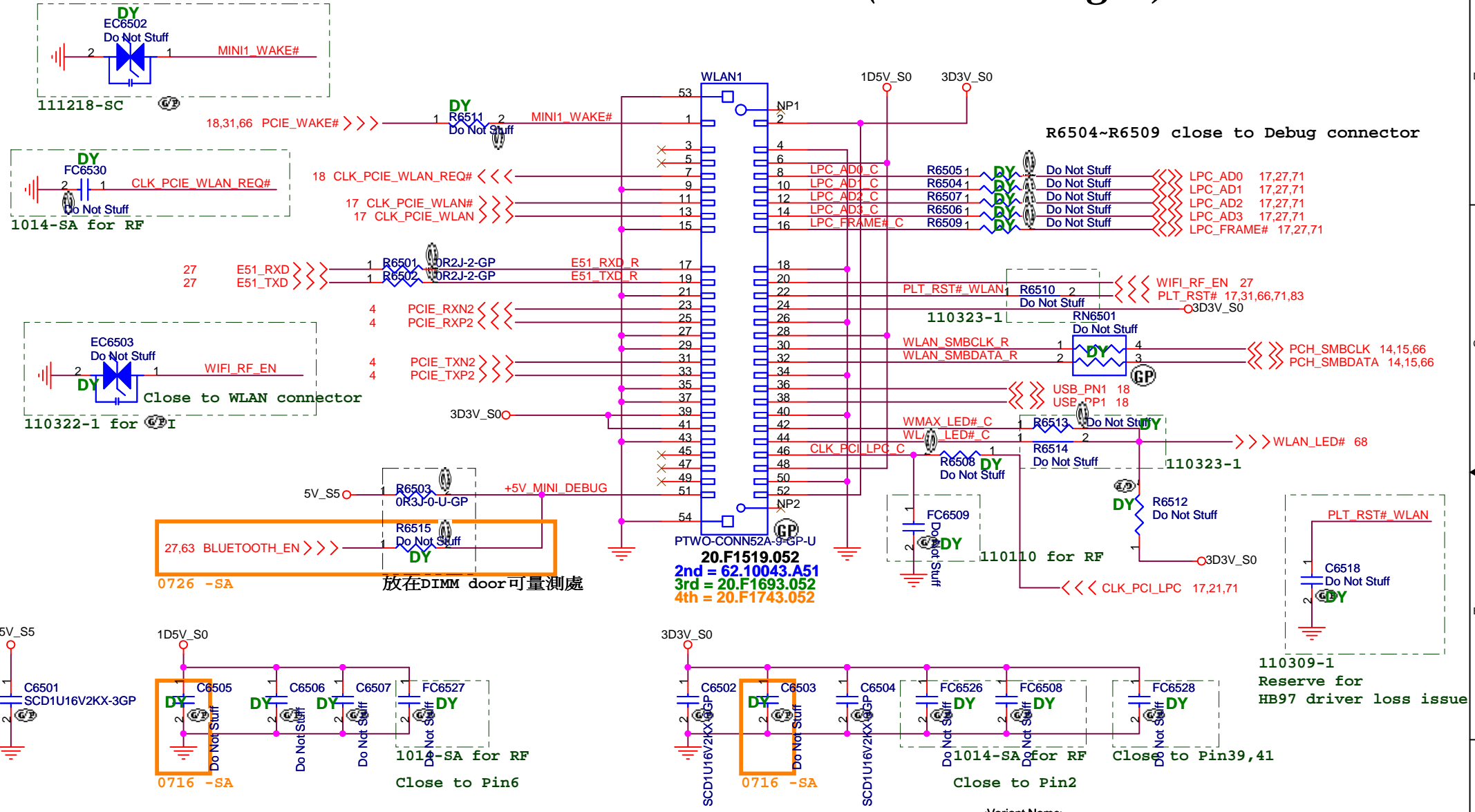
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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>F/P</b>			
Size	Document Number		Rev
A4	<b>JE40-SB</b>		<b>SB</b>
Date:	Friday, March 25, 2011	Sheet 64	of 102



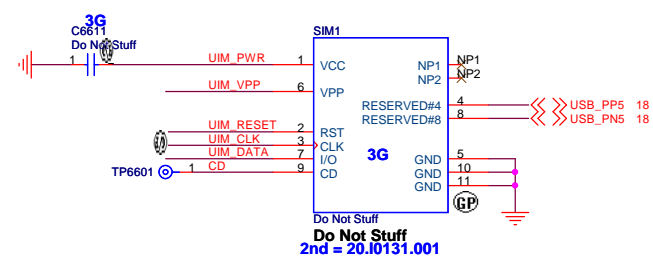
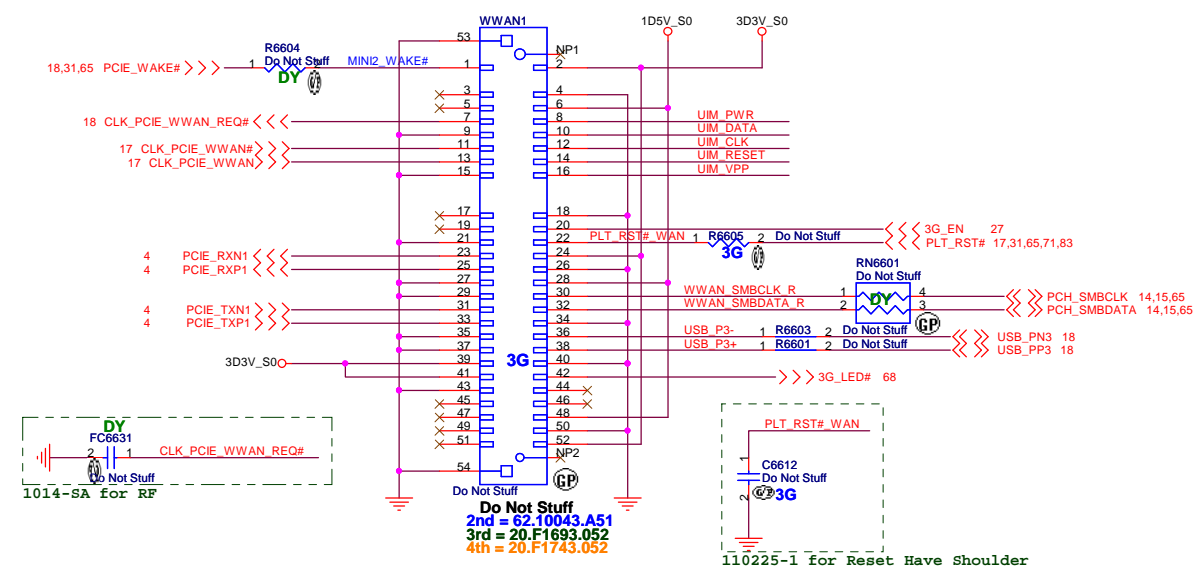
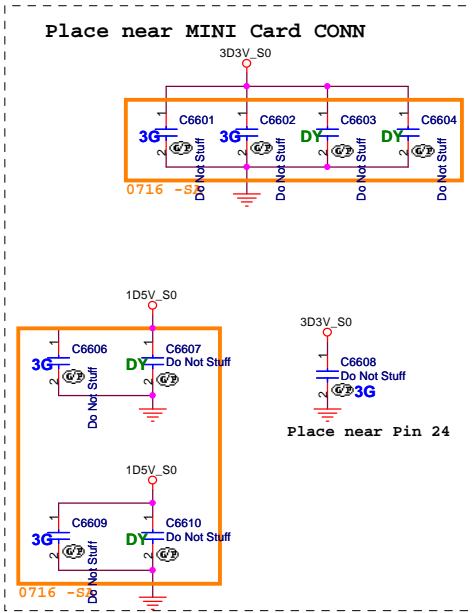
# Mini Card Connector(802.11a/b/g/n)



<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> WLAN			
Size	Document Number		Rev
A4	<b>JE40-SB</b>		<b>SB</b>
Date:	Monday, March 28, 2011	Sheet	65 of 102

# Mini Card Connector(WWAN)



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN**

Size A3	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
Date: Wednesday, March 30, 2011	Sheet 66	of 102

(Blanking)

<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**JE40-SB**

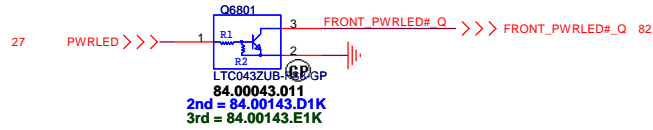
Rev

**SB**

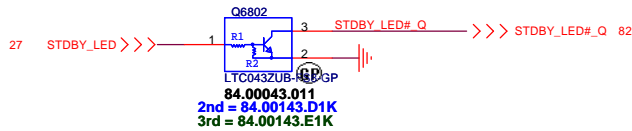
Date: Friday, March 25, 2011

Sheet 67 of 102

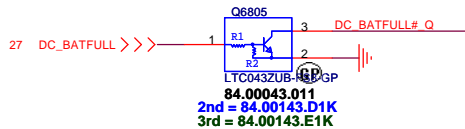
### Power button LED



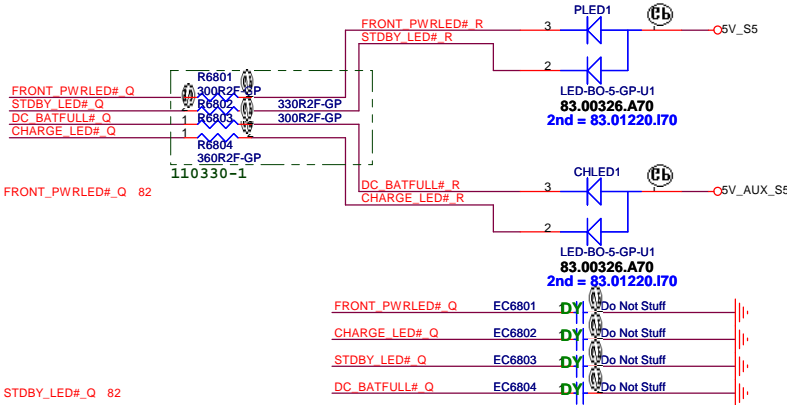
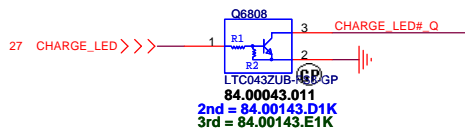
### Power STDBY\_LED



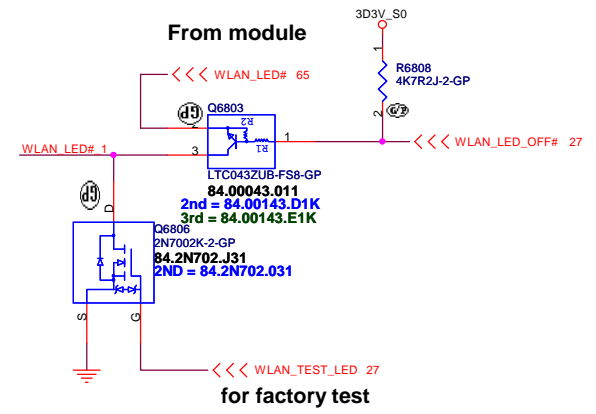
### Battery LED2 (DC\_BATFULL)



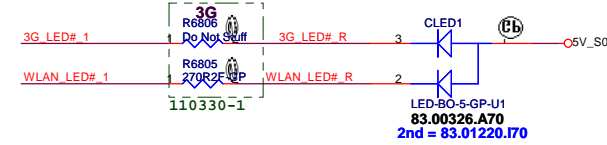
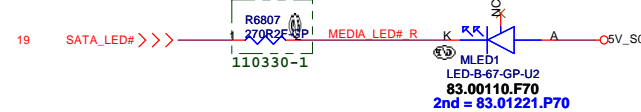
### Battery LED1 (CHARGE)



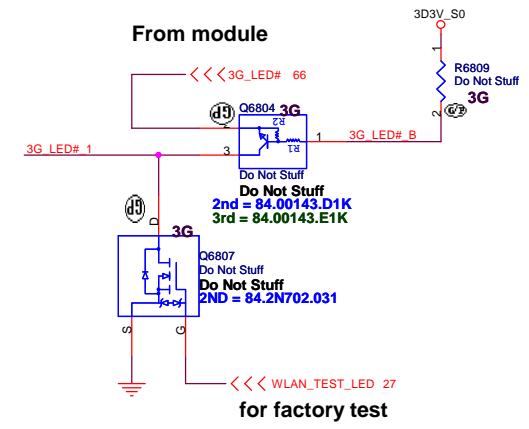
### WLAN\_LED



### SATA HDD LED



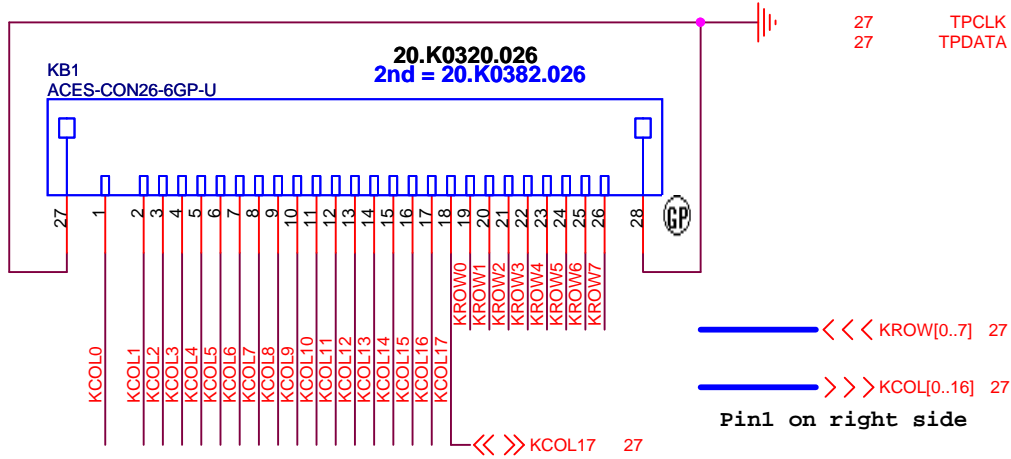
### 3G\_LED



<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>LED Bard/Power Button</b>			
Size A3	Document Number <b>JE40-SB</b>	Rev <b>SB</b>	
Date: Wednesday, March 30, 2011		Sheet 68	of 102

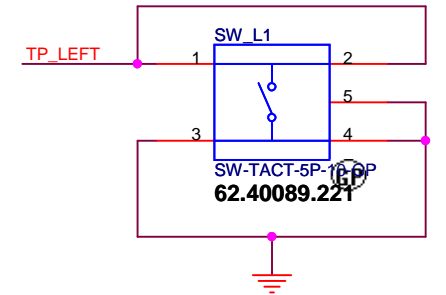
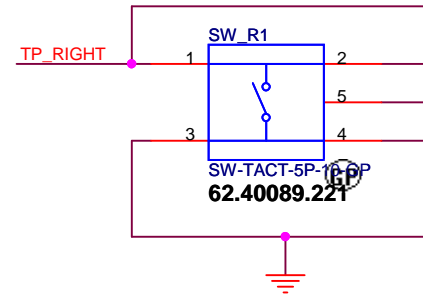
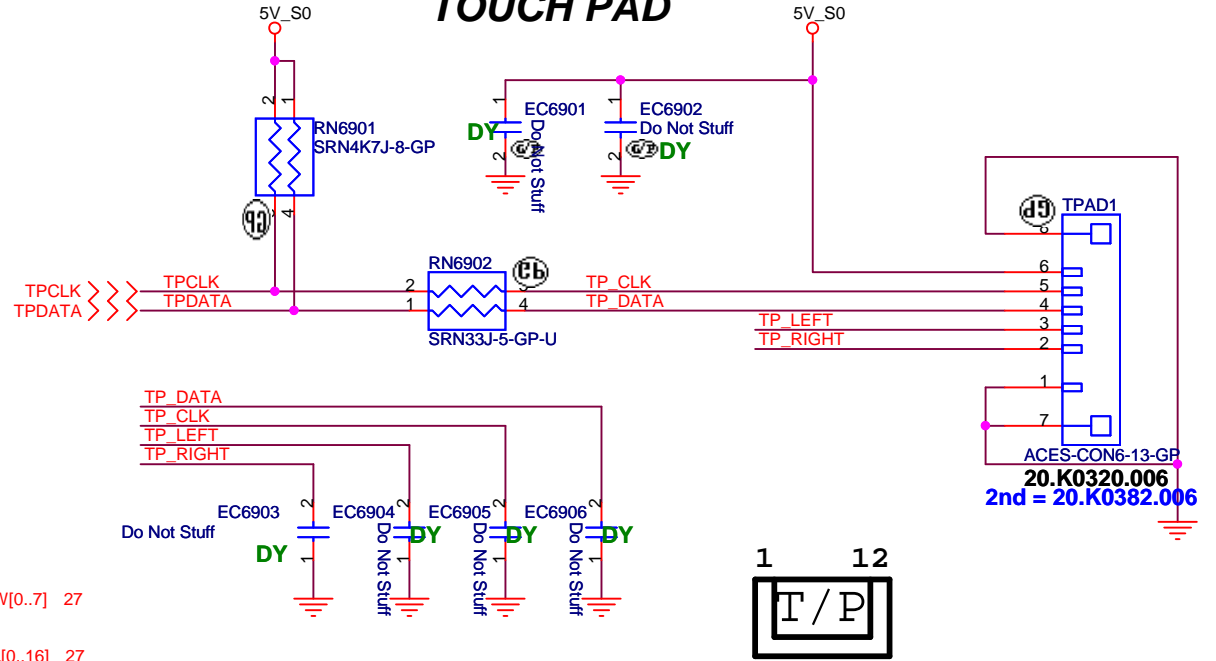
# Internal KeyBoard Connector



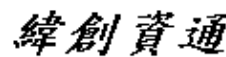
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 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

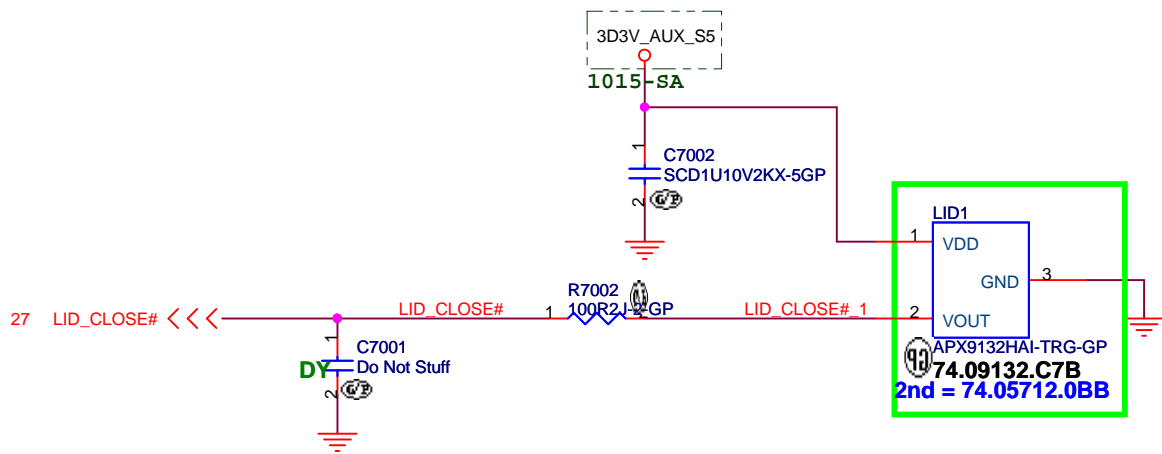


# TOUCH PAD



<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Key Board/Touch Pad</b>	
Title <b>Key Board/Touch Pad</b>	Document Number <b>JE40-SB</b>
Size A4	Rev <b>SB</b>
Date: Monday, March 28, 2011	Sheet 69 of 102



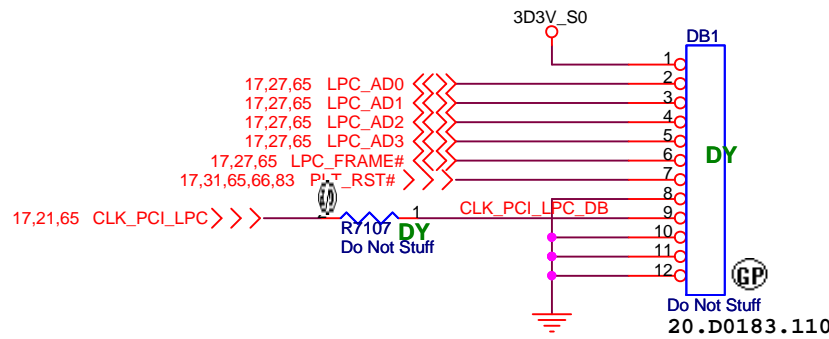
<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

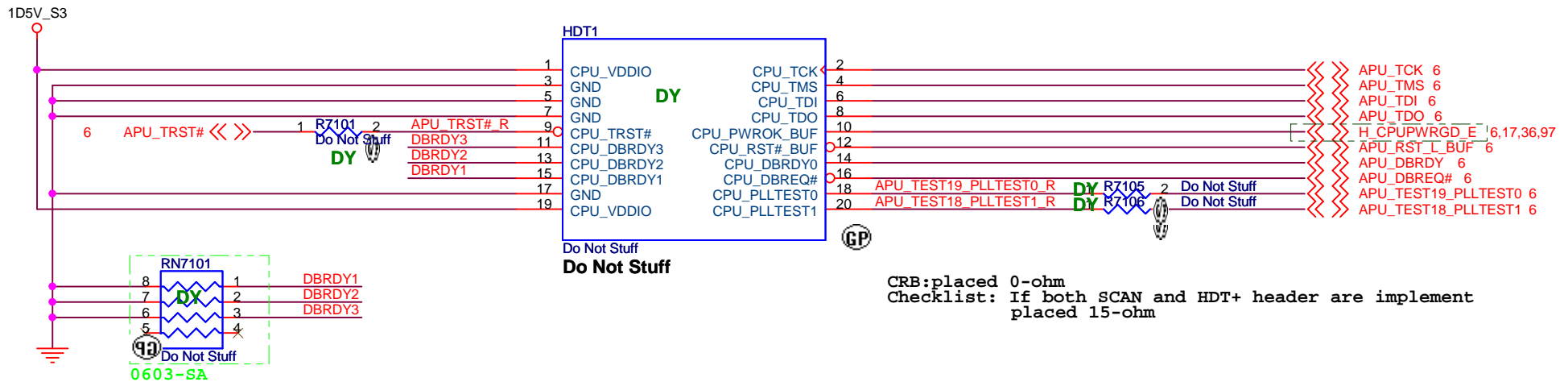
Title **Hall Sensor**

Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
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Date: Monday, March 28, 2011 Sheet 70 of 102



### HDT+ Connectors



<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size  
A4

Document Number

**JE40-SB**

Rev  
**SB**

Date: Monday, March 28, 2011

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>JE40-SB</b>		Rev <b>SB</b>
Date: Friday, March 25, 2011	Sheet	72	of 102



(Blanking)

<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**JE40-SB**

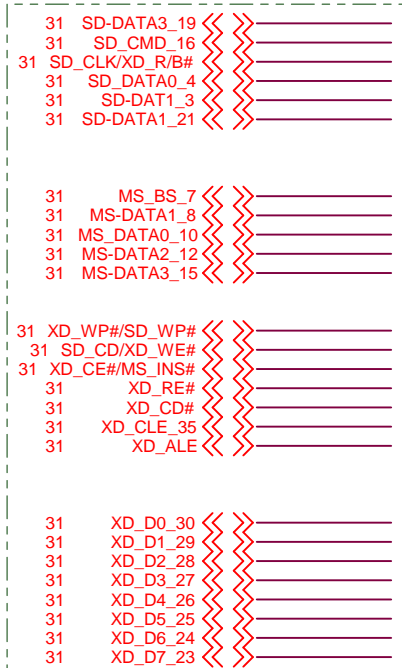
Rev

**SB**

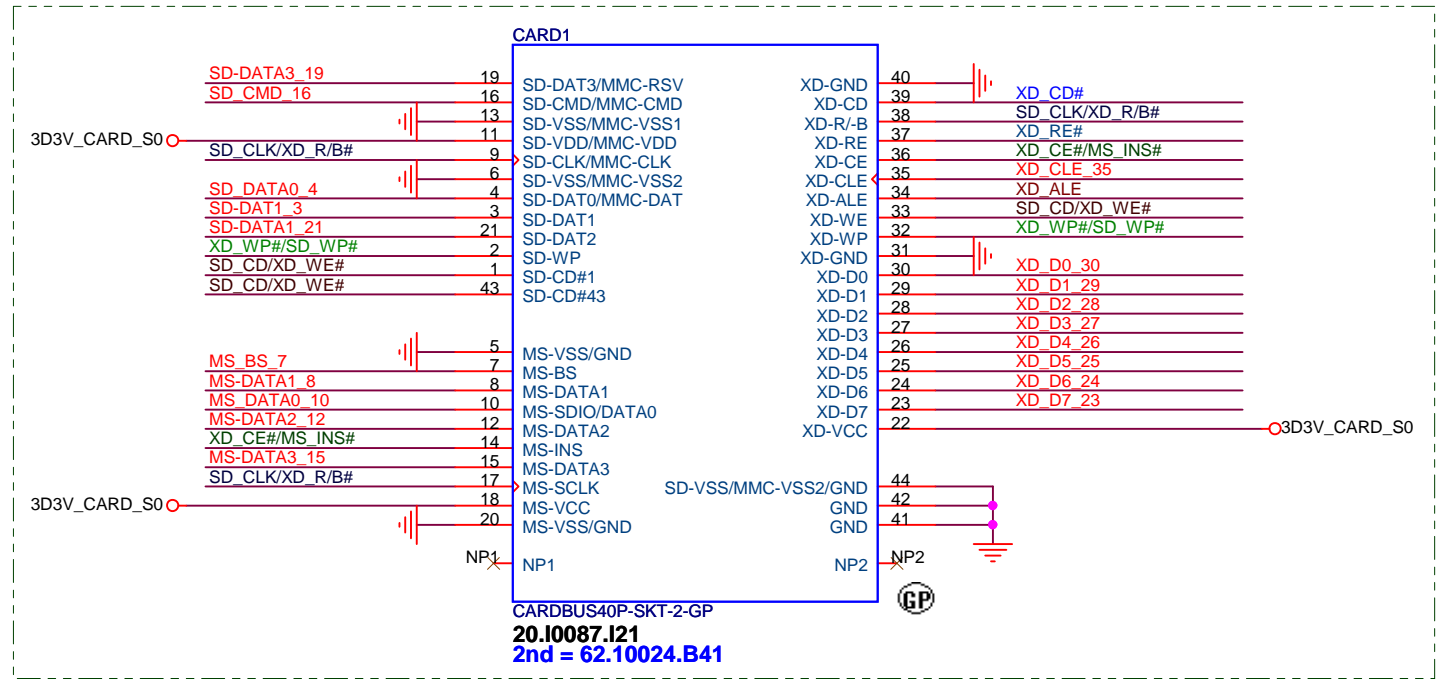
Date: Friday, March 25, 2011

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# SD/XD/MS Card Reader



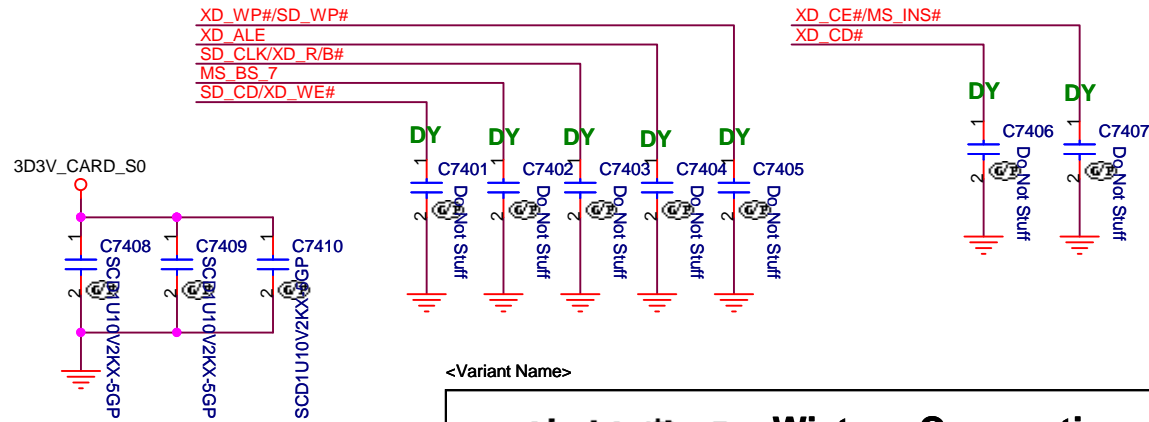
Card-reader Off-Page



110112

Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-D0		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P
P14	MS-VCC		9P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/6P	1P/10P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	XD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37	4 IN 1-GND	SD-WP/CD-SW-GND	
P38			



Near CARD1 Pin11, Pin18, Pin22

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>CARD Reader CONN</b>			
Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>	
Date: Monday, March 28, 2011	Sheet 74	of	102

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
<b>Express Card</b>			
Size A4	Document Number <b>JE40-SB</b>		Rev <b>SB</b>
Date: Friday, March 25, 2011	Sheet	75	of 102

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>JE40-SB</b>		<b>SB</b>
Date:	Friday, March 25, 2011	Sheet 76 of	102

(Blanking)

<Variant Name>

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Reserved</b>		
Size A4	Document Number <b>JE40-SB</b>	Rev <b>SB</b>
Date: Friday, March 25, 2011	Sheet 77 of	102

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<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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A4	<b>JE40-SB</b>		<b>SB</b>
Date:	Friday, March 25, 2011	Sheet 78 of	102

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Title			
<b>Reserved</b>			
Size A4	Document Number <b>JE40-SB</b>		Rev <b>SB</b>
Date: Friday, March 25, 2011	Sheet	79	of 102

( Blanking )

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A	<b>JE40-SB</b>		<b>SB</b>
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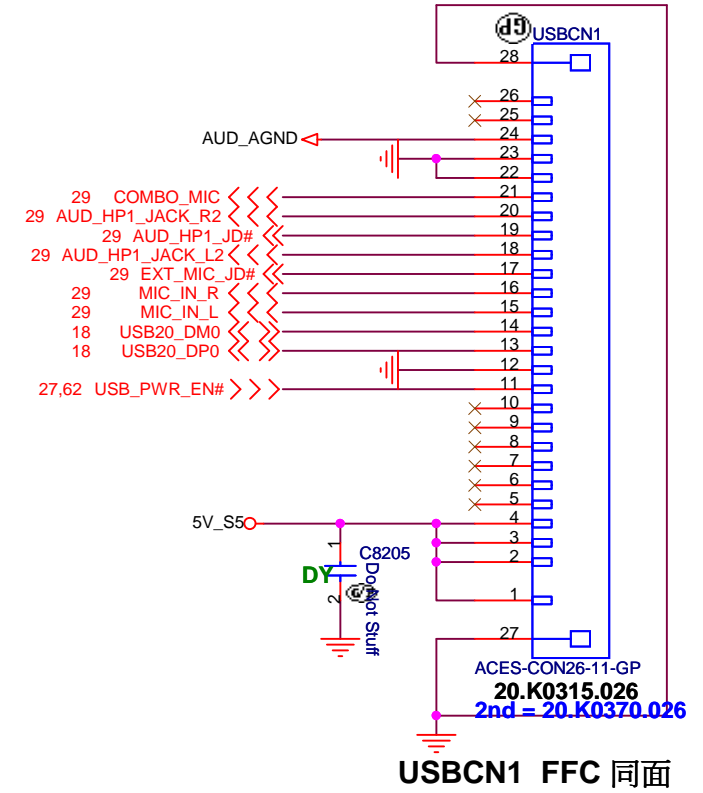
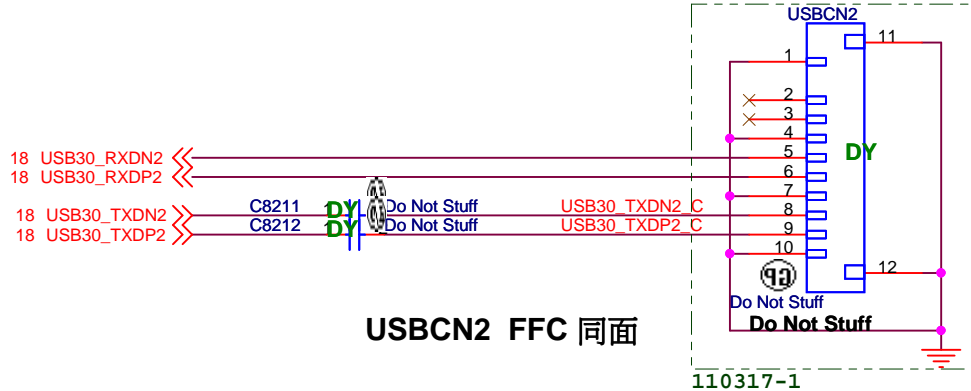
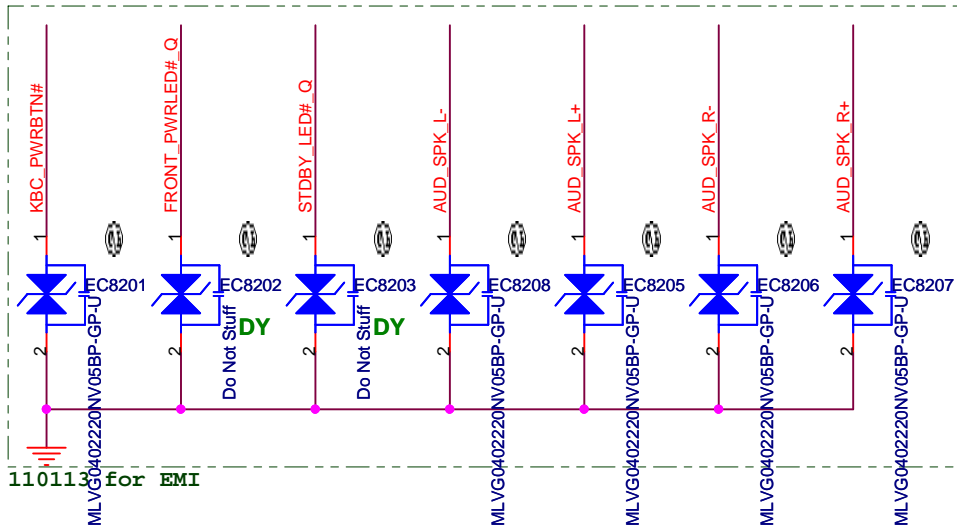
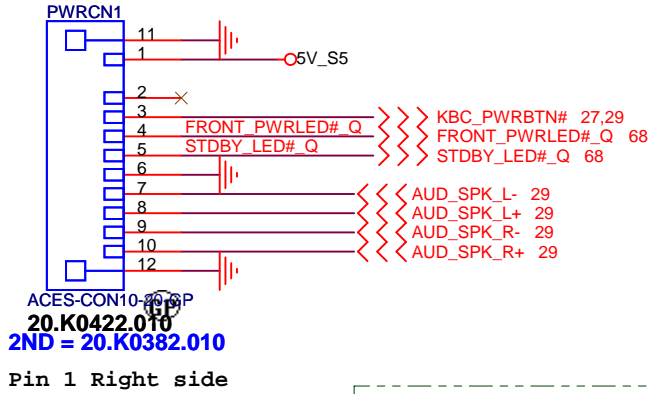


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<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>UNUSED PARTS/EMI Capacitors</b>					
Size	Document Number				Rev
A4	<b>JE40-SB</b>				<b>SB</b>
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# PWRCN1 FFC 異面



<Variant Name>

緯創資通

**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title

**IO Board Connector**

Size  
A4

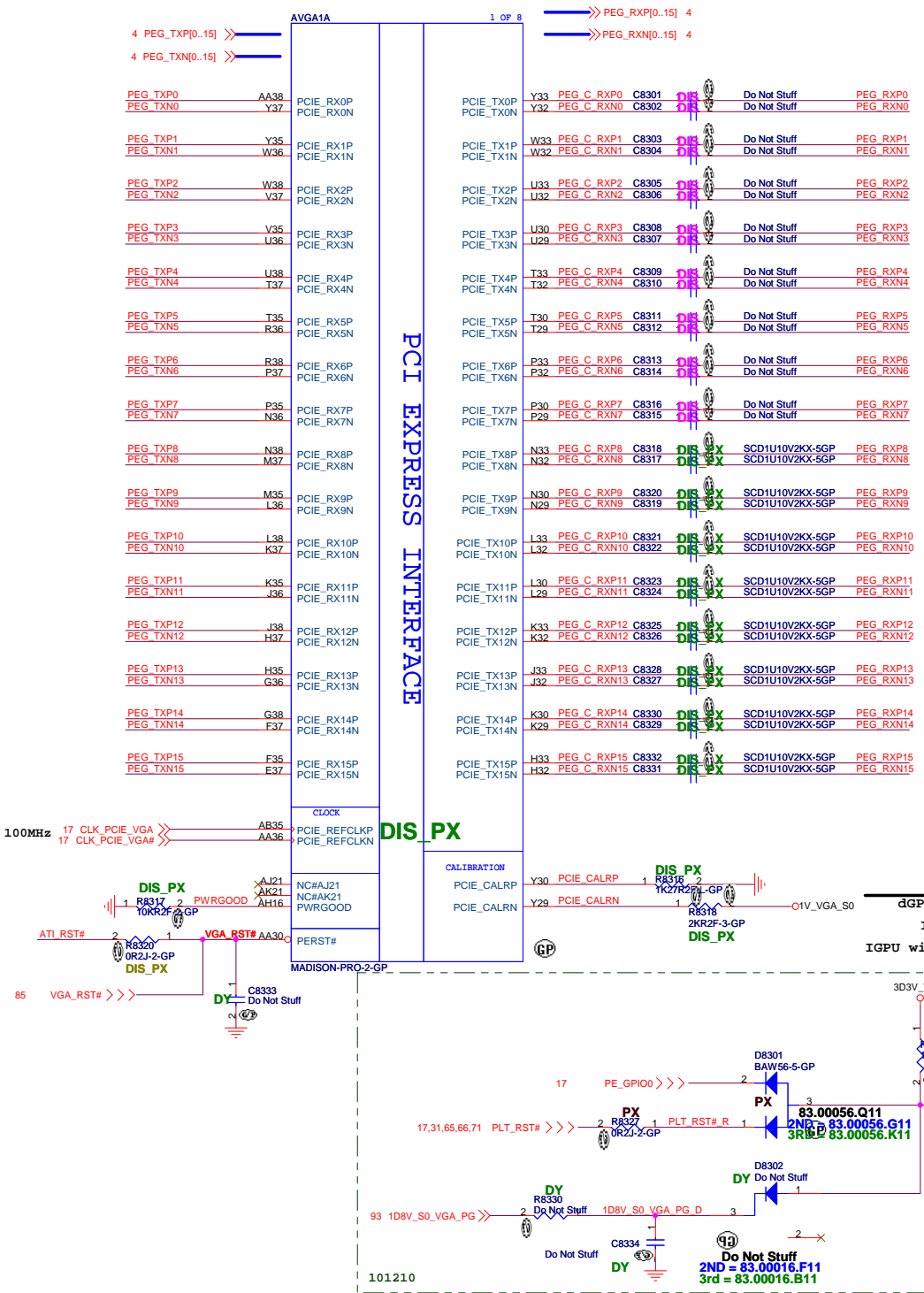
Document Number

**JE40-SB**

Rev  
**SB**

Date: Monday, March 28, 2011

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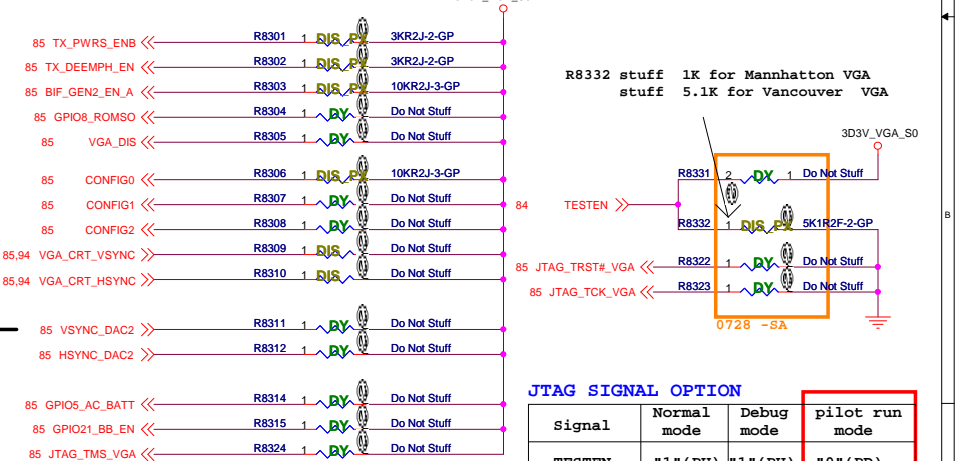


### CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYSN		X	1

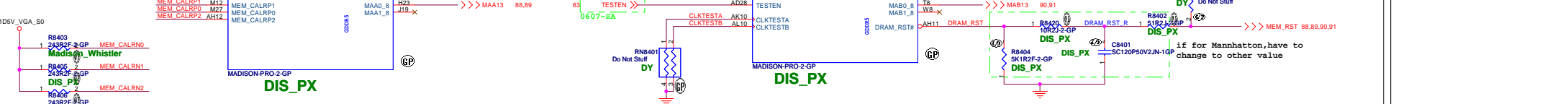
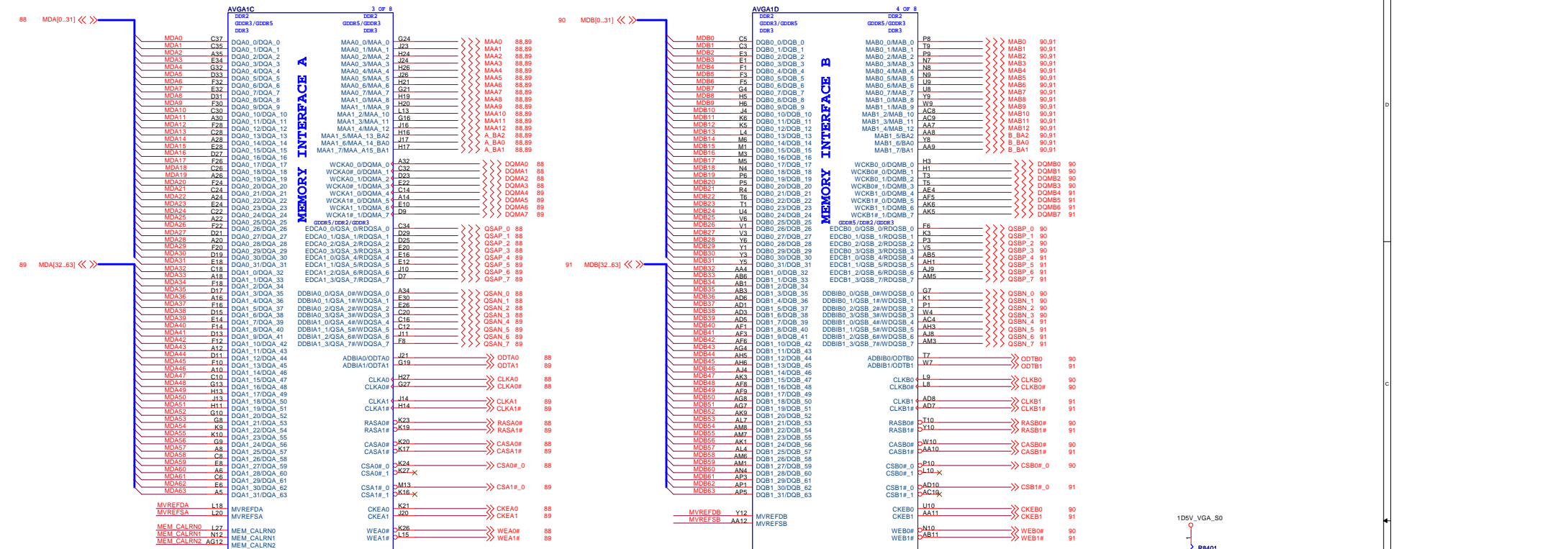
### PIN STRAPS



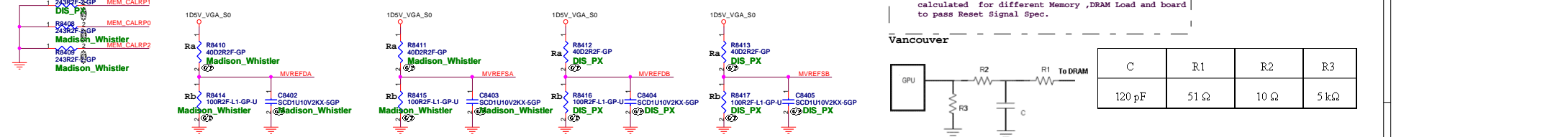
-Variant Name-

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>GPU PCIe/STRAPPING(1/5)</b>	
Size	Document Number	Rev	
Custom	<b>JE40-SB</b>	<b>SB</b>	
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**PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC**

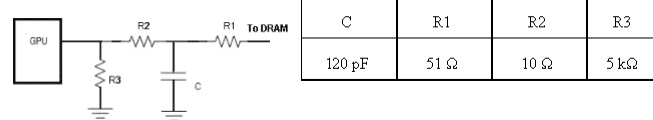


**DDR3/GDDR3 Memory Stuff Option(Mad/Park)**

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

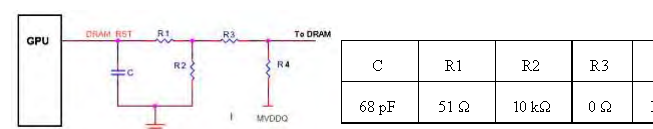
\*\* This basic topology should be used for DRAM RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

**Vancouver**



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

**Mannhattan**



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

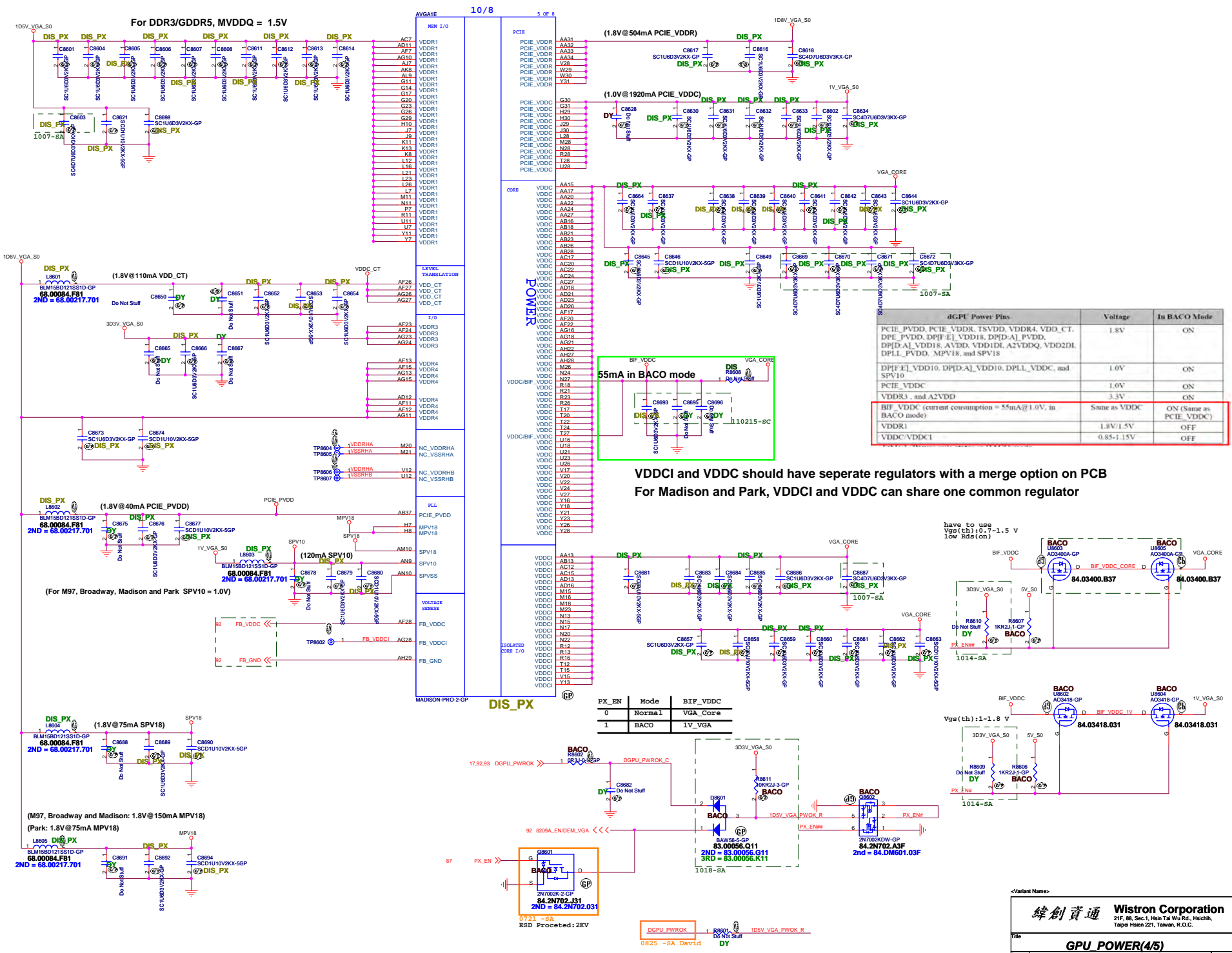
Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

GPU Memory(2/5)  
JE40-SB

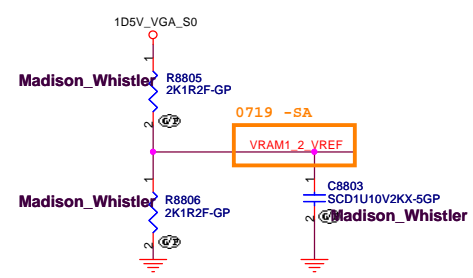
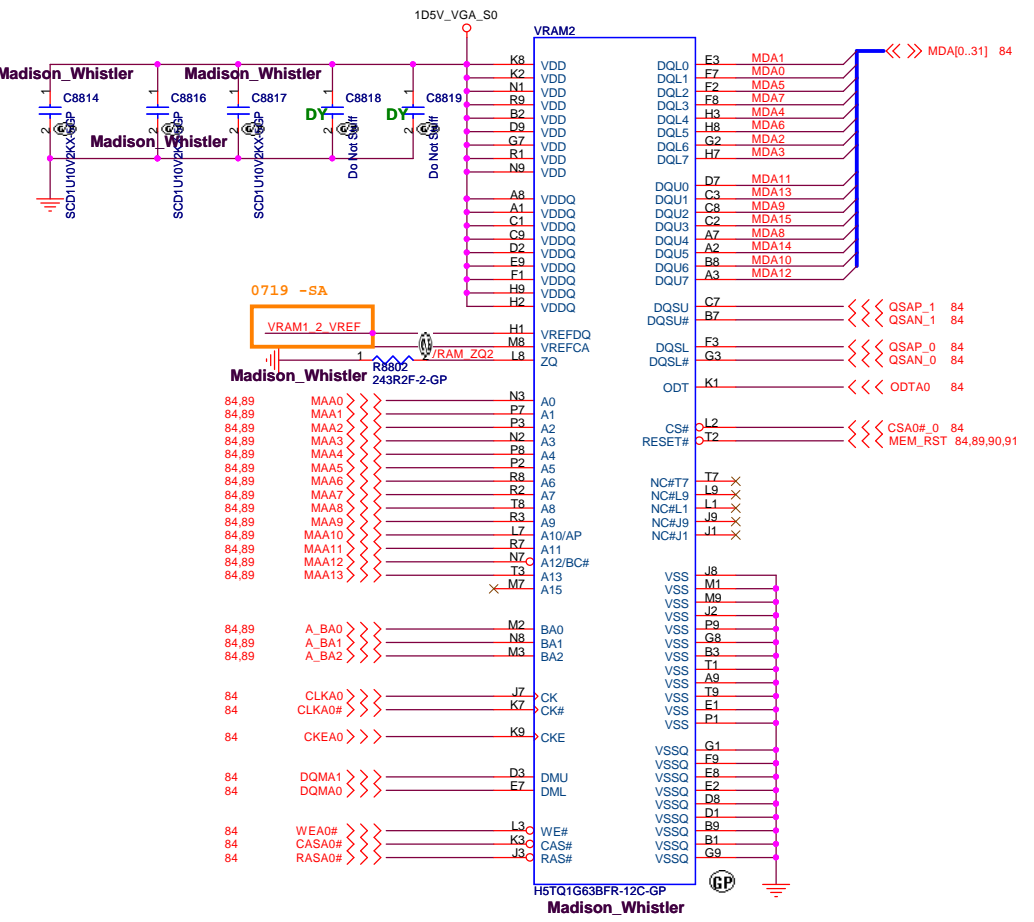
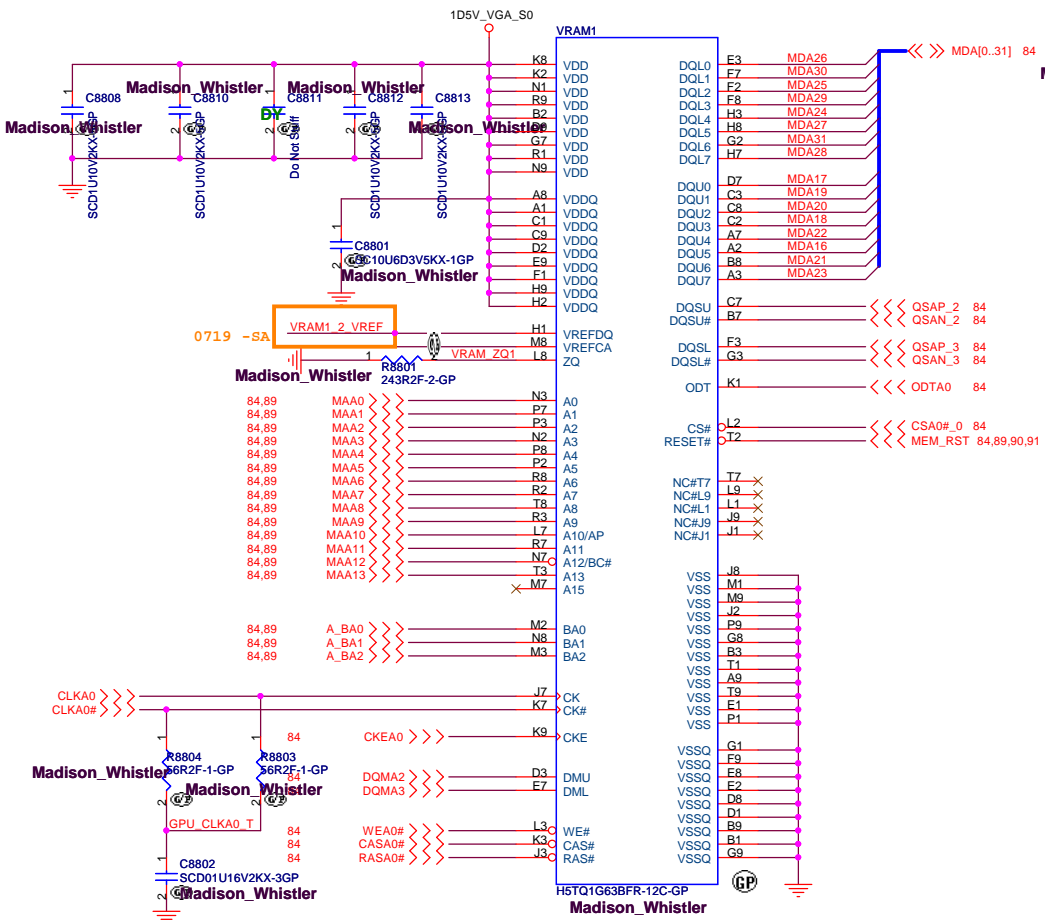
Rev SB

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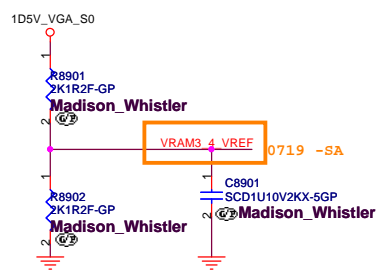
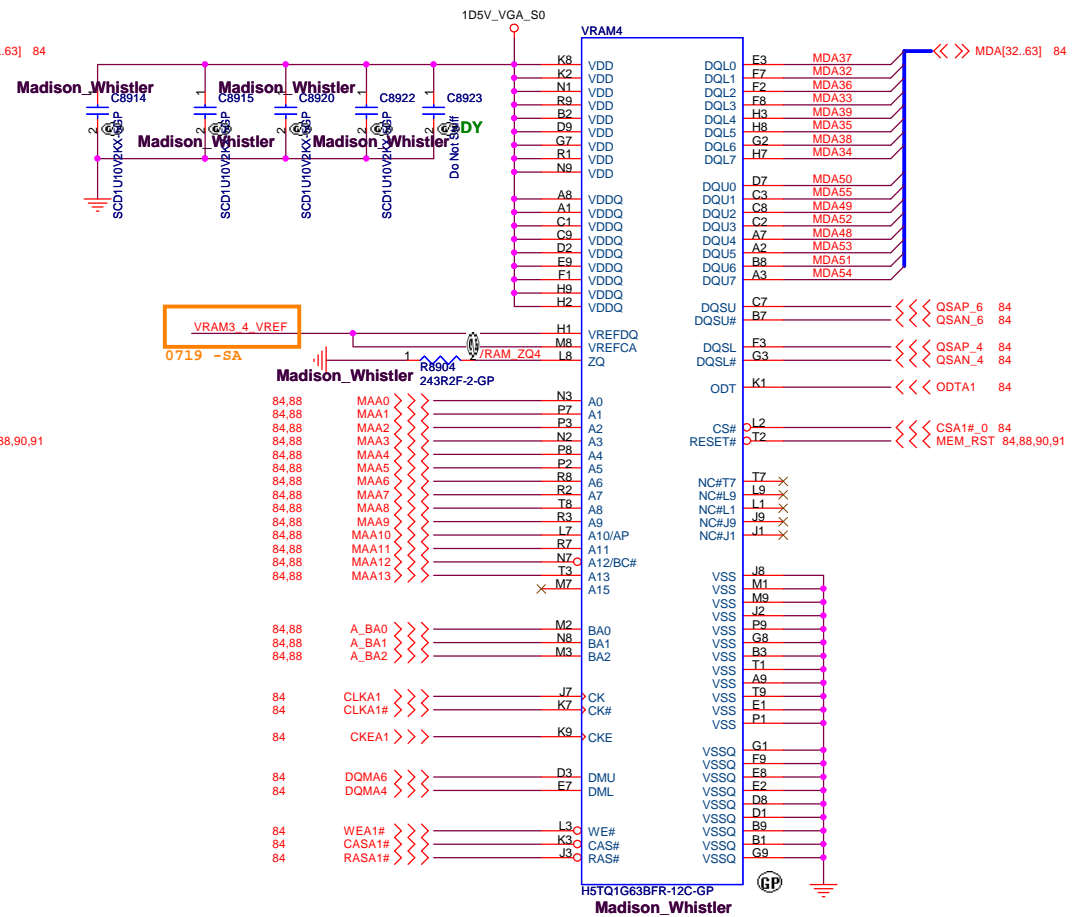
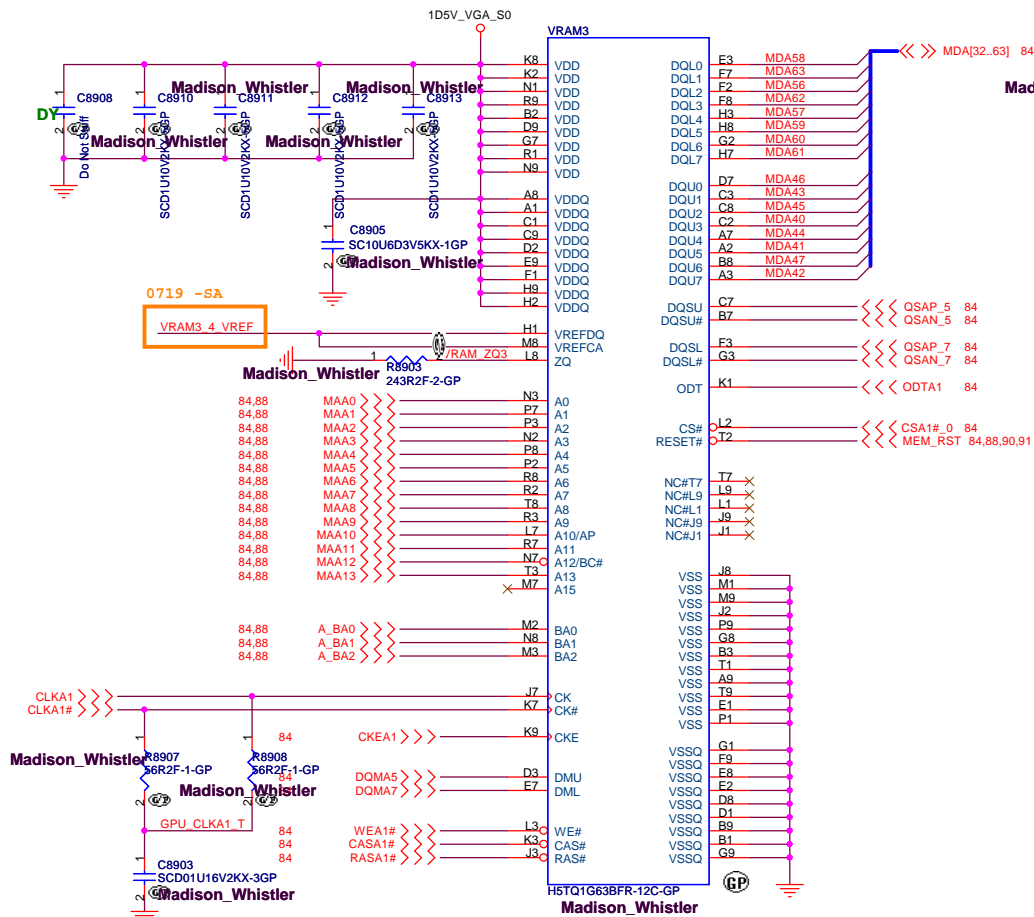
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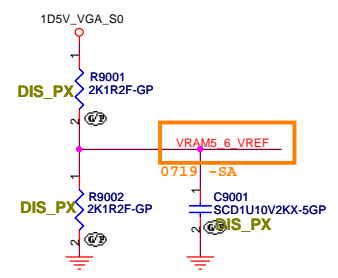
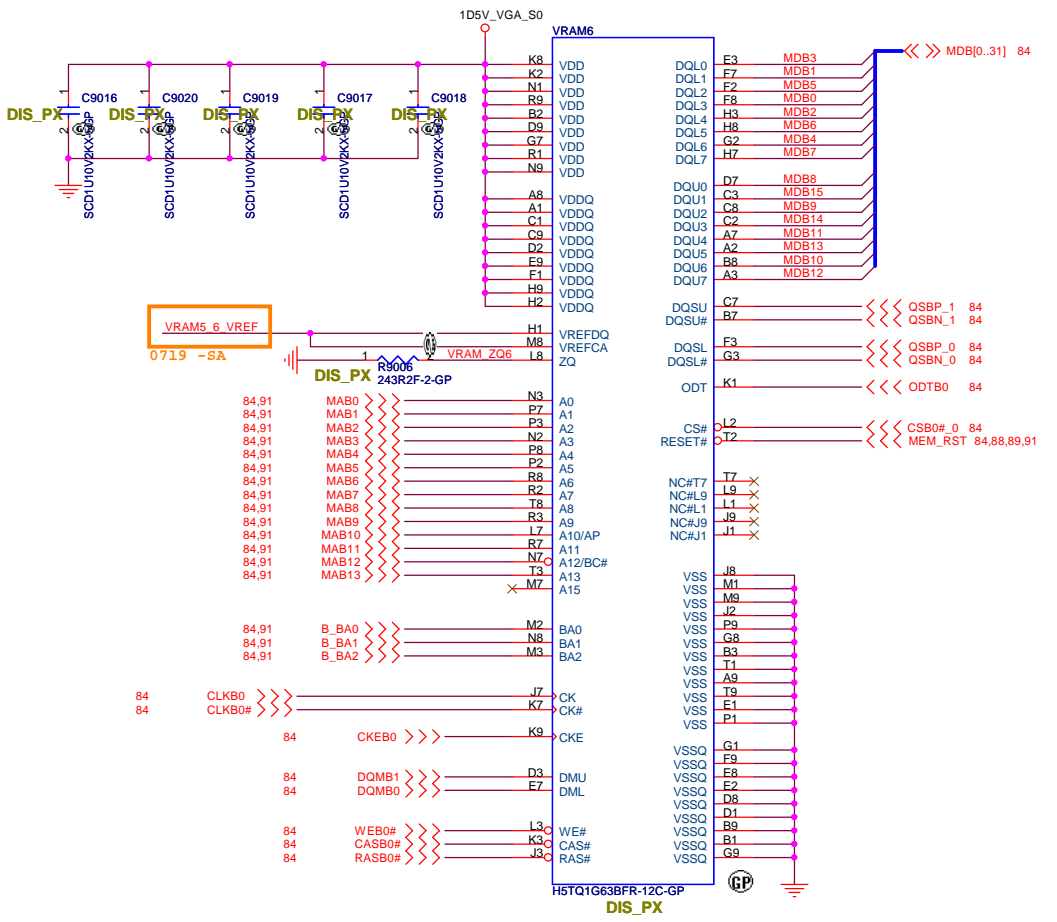
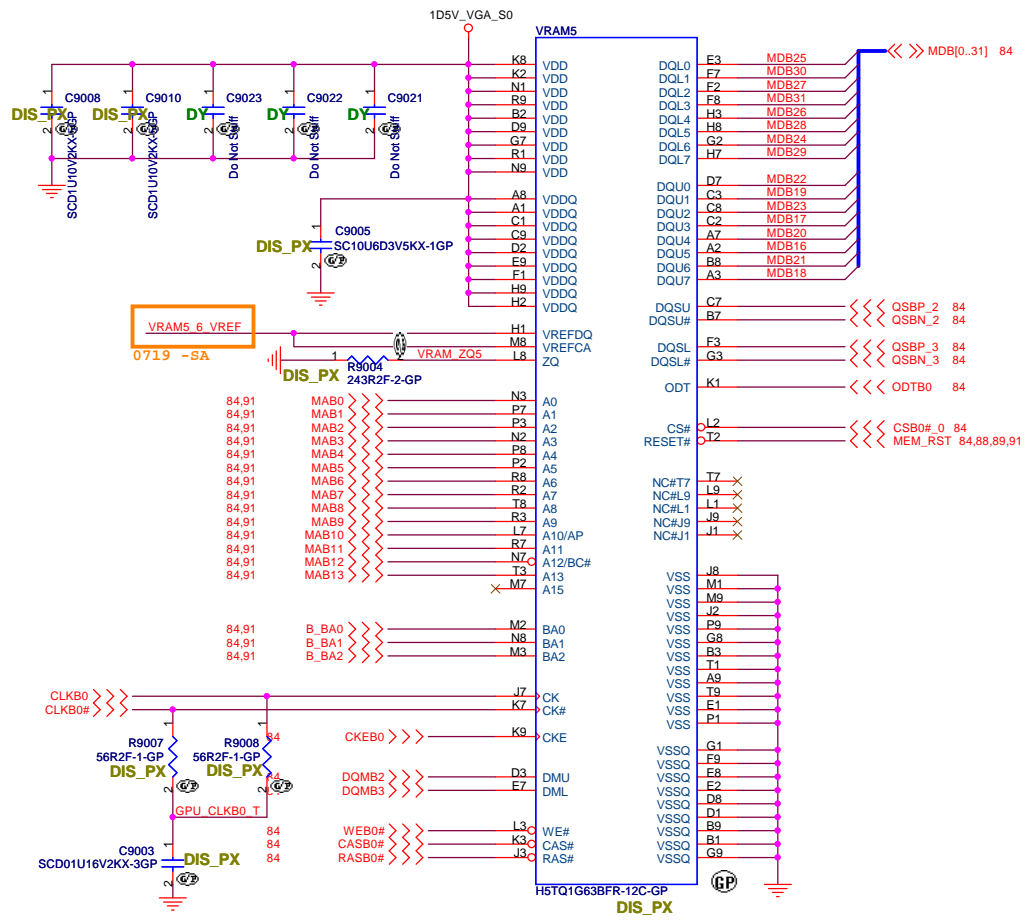
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

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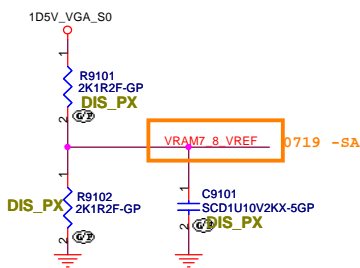
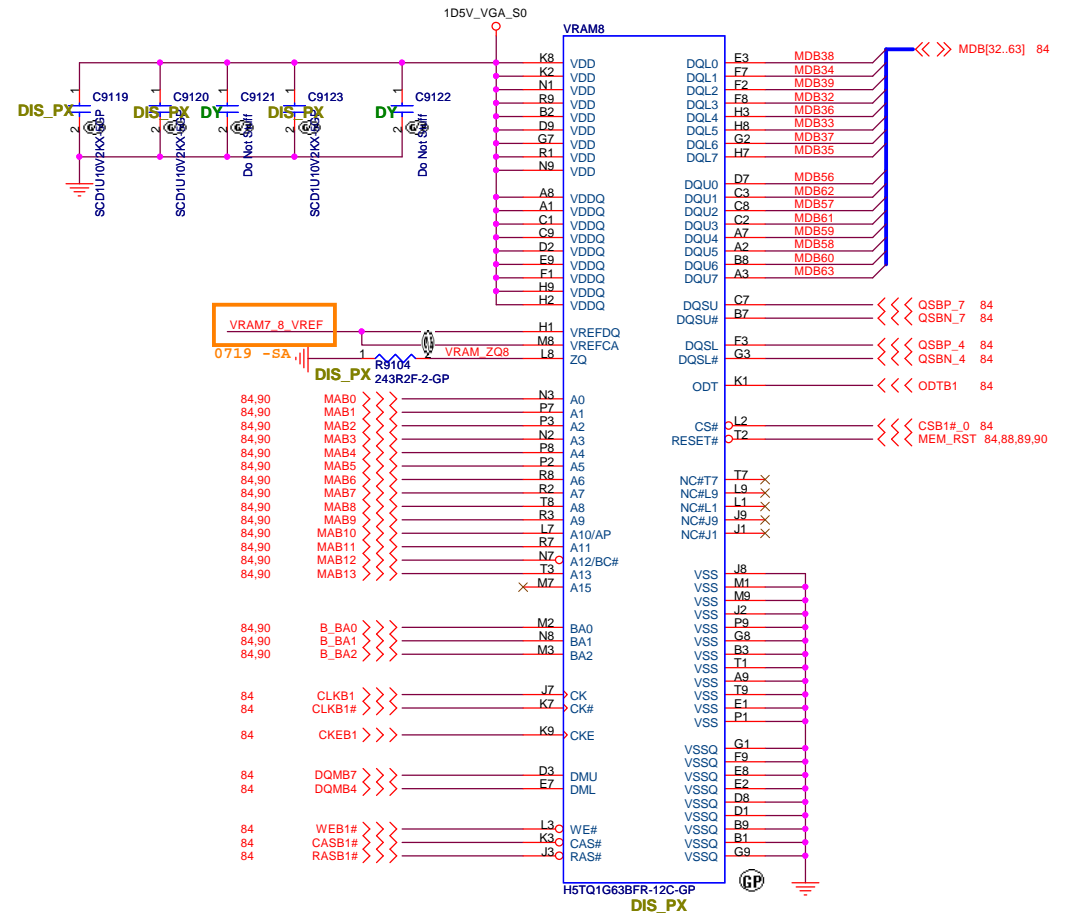
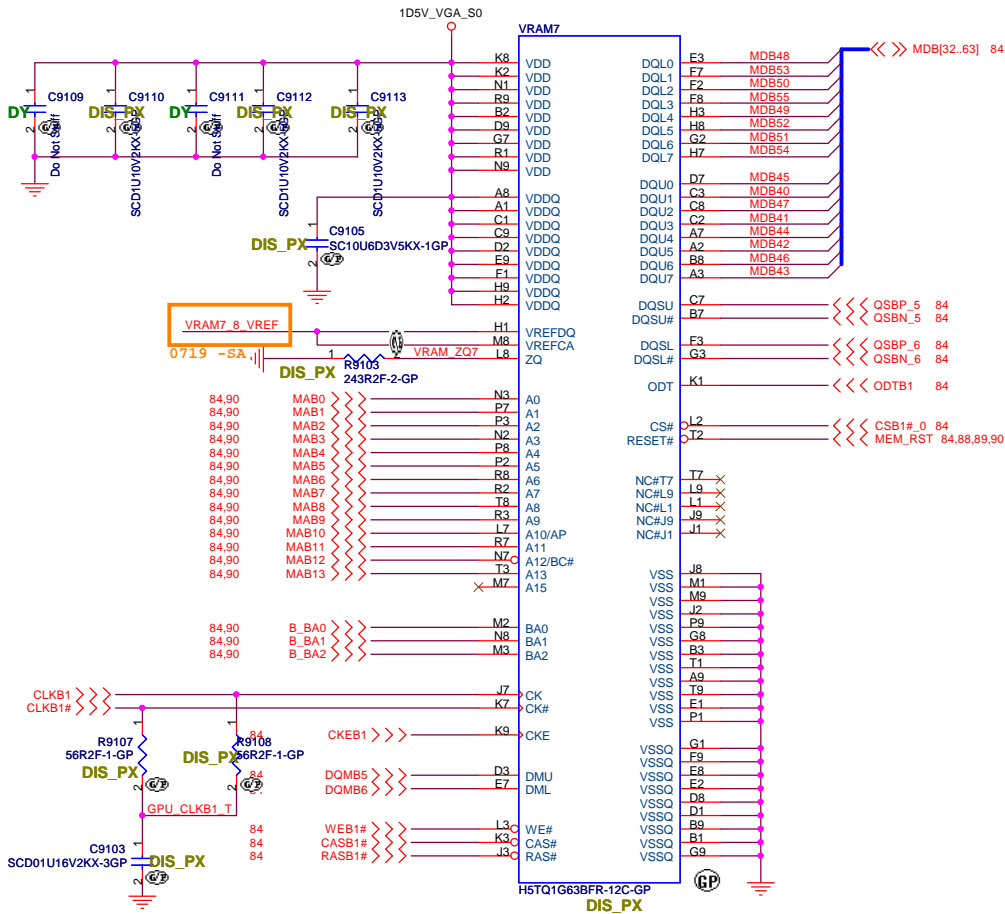
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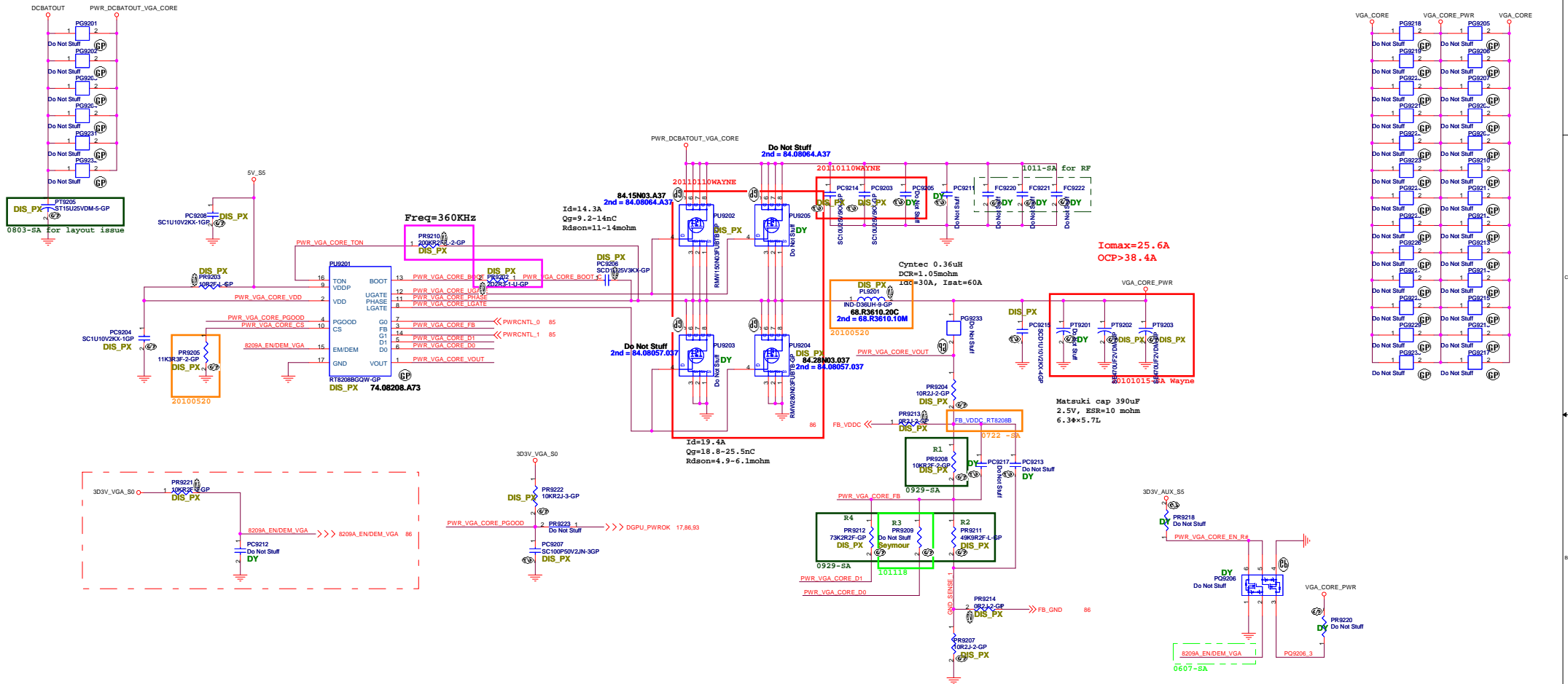
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM5,6 (3/4)**

Size A3	Document Number	Rev
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PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Whistler Pro
H	L	High	1V
H	L	Medium	1V
H	H	Low	0.9V

$$V_{out} = 0.75V * [(1+R1)/(R2/R4)]$$

$$V_{out} = 0.75V * (1+R1/R2)$$

PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Seymour XT
L	L	High	1.1V
L	H	Medium	1V
H	L	Medium	1V
H	H	Low	0.9V

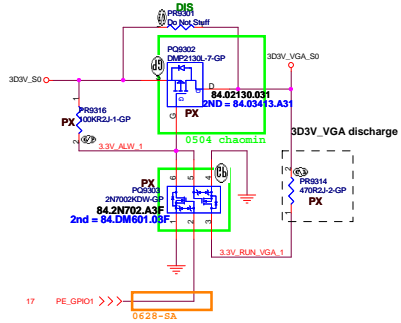
$$V_{out} = 0.75V * [(1+R1)/(R2/R3/R4)]$$

$$V_{out} = 0.75V * [(1+R1)/(R2/R4)]$$

$$V_{out} = 0.75V * (1+R1/R2)$$

<Variant Name>

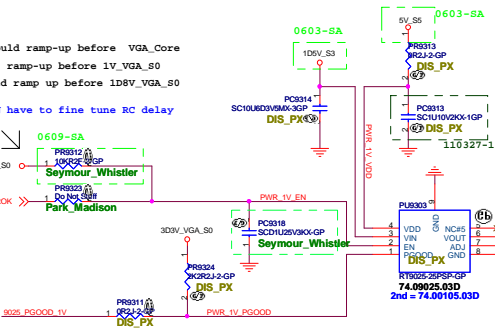
**+3VS to 3.3V\_DELAY Transfer**



	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

3D3V\_VGA\_S0 should ramp-up before VGA\_Core  
 VGA\_Core should ramp-up before 1V\_VGA\_S0  
 1V\_VGA\_S0 should ramp up before 1D8V\_VGA\_S0

So 1V\_VGA\_S0 EN have to fine tune RC delay after VGA\_Core



**RT9025 for 1D8V\_S0**

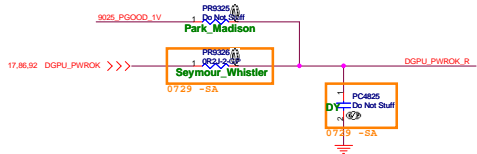
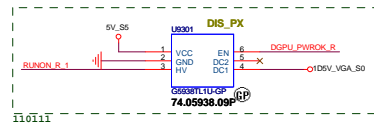
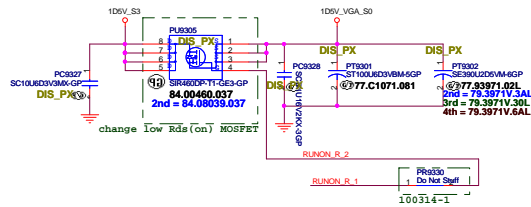
**RT9025 for 1V\_S0**

$$V_o = 0.8 * (1 + (R1/R2))$$

$$= 0.8 * (1 + (10K/39K))$$

$$= 1.005 V$$

A04468, SO-8  
 Ids=11.6A, Qg=9-12nC  
 Rds(on)=17.4-22m ohm



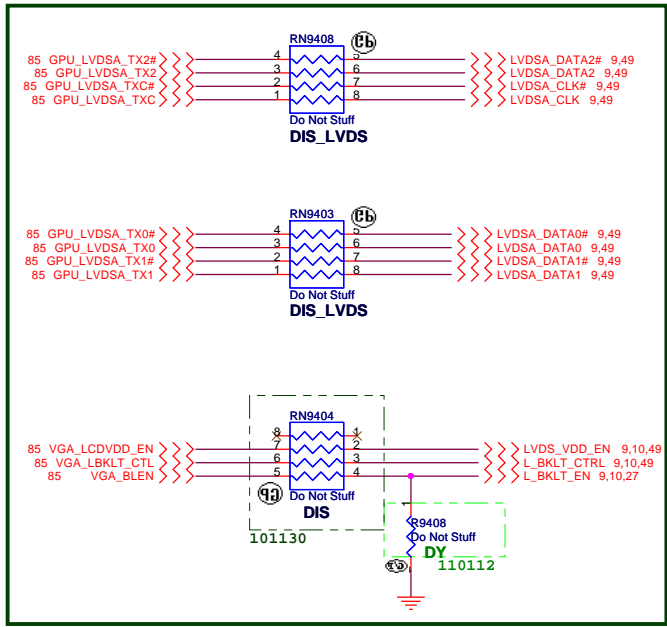
3D3V\_VGA\_S0 should ramp-up before VGA\_Core  
 VGA\_Core should ramp-up before 1V\_VGA\_S0  
 1V\_VGA\_S0 should ramp up before 1D8V\_VGA\_S0  
 1D8V\_VGA\_S0 sequence no define specially  
 So 1D8V\_VGA\_S0 EN have to fine tune RC delay after 1V\_VGA\_S0

Wistron Corporation  
 21F, 8F, Sec. 1, Hsin Ta Wu Rd., Hsinshih,  
 Taipei Hsin 221, Taiwan, R.O.C.

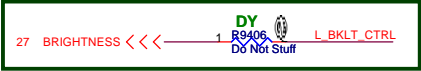
DISCRETE VGA POWER

JE40-SB

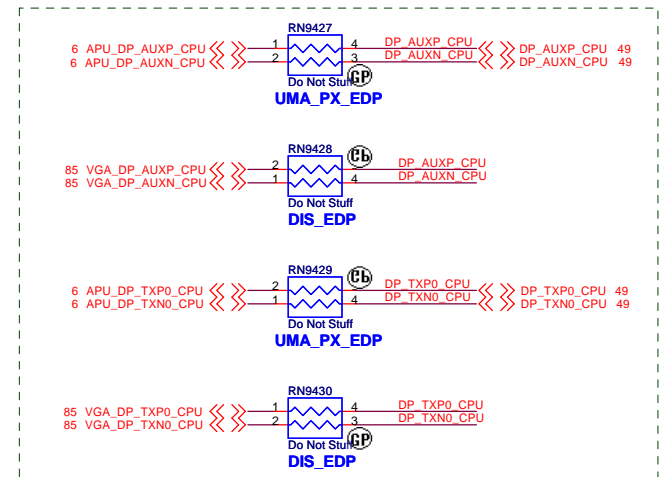
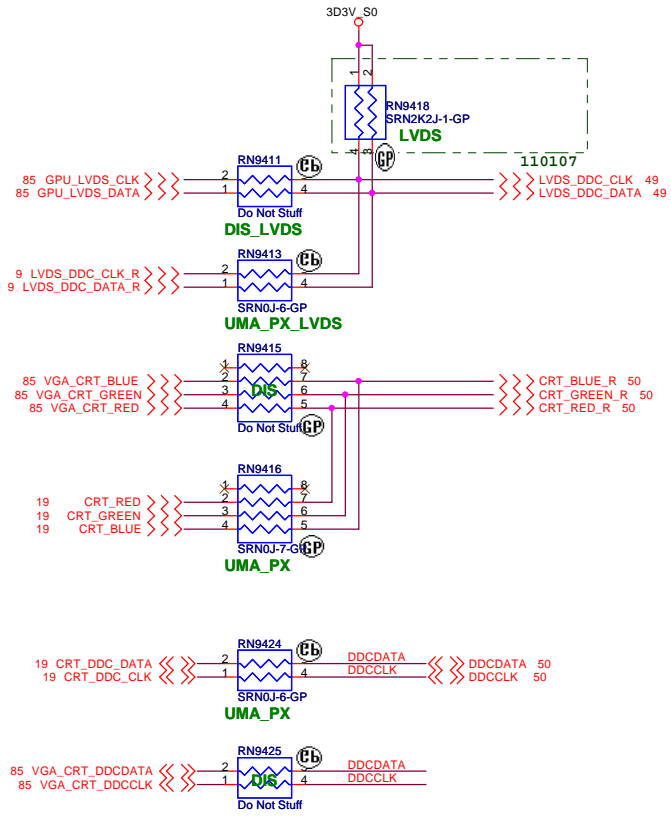
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101123

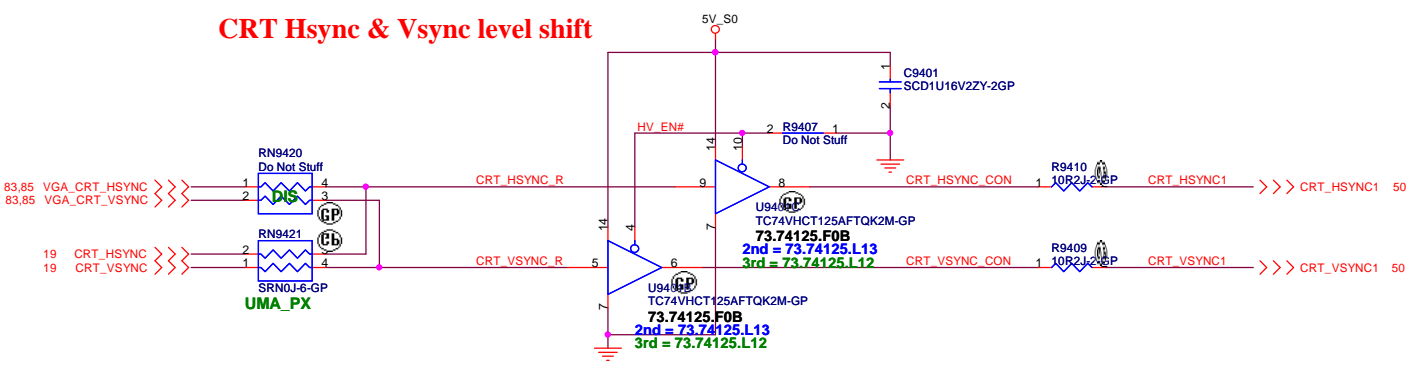


0804-SA



if Co-layout LVDS and EDP panel,  
have to place Res near LVDS Cap  
for Reflection Prevent

### CRT Hsync & Vsync level shift



<Variant Name>

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Title: **LVDS Switch**

Size A3	Document Number	Rev
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( Blanking )

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
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(Blanking)

<Variant Name>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

***Touch Panel***

Size  
A

Document Number

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Rev

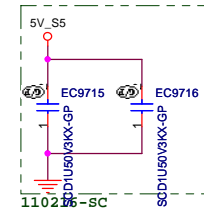
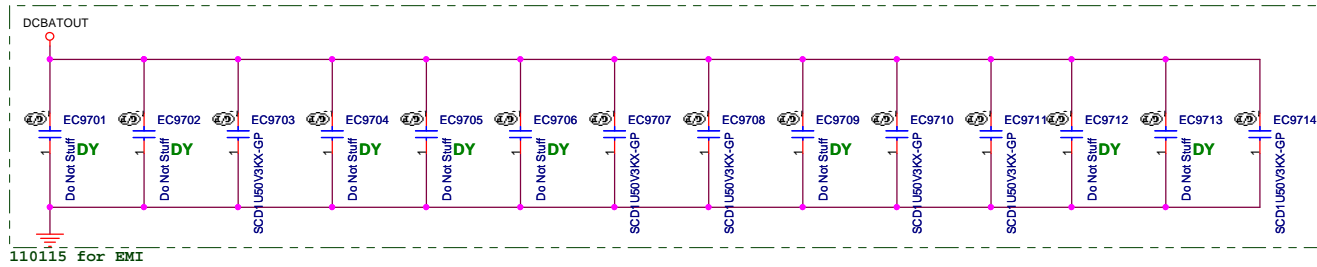
**SB**

Date: Friday, March 25, 2011

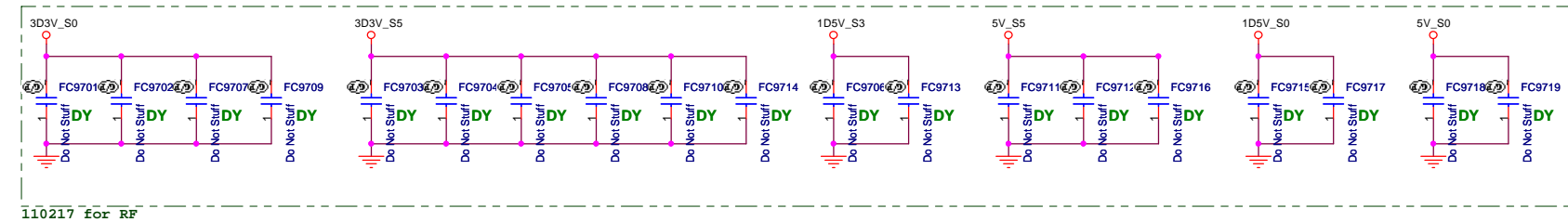
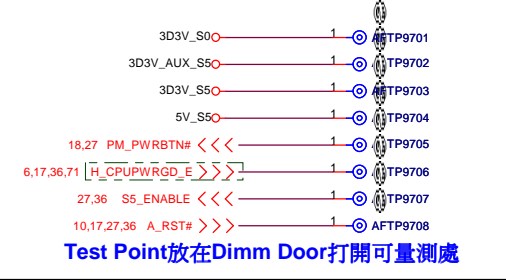
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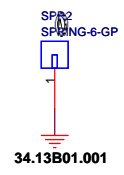
# EMI CAP



## Check test point

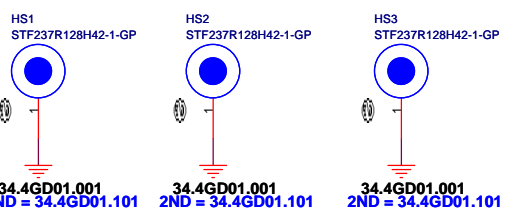


# SPRING

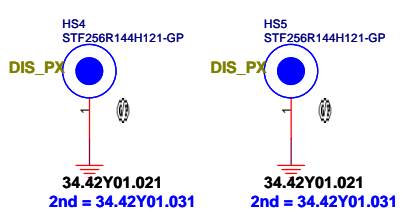


# BOSS

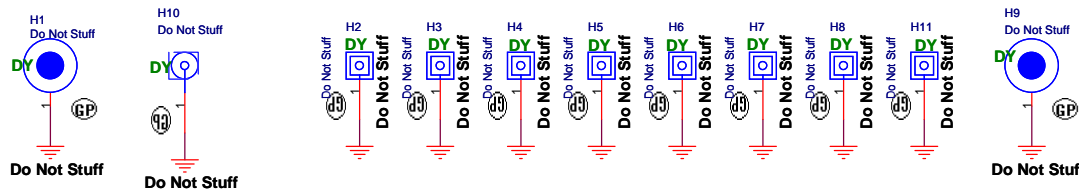
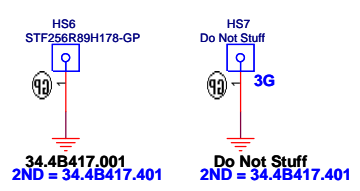
## CPU



## VGA



## WLAN



<Variant Name>

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Title: **UNUSED PARTS/CAP**

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# Modify list

65 W: PR4007 -> 187K(64.18735.6DL)  
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121 -> 604-ohm (64.60405.6DL )  
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL )

R8332 stuff 1K for Mannhatton VGA  
stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603  
if use LVDS L8701,L8708 stuff bead 0603  
if use EDP L8711,L8709 stuff bead 0603 ohm  
if use EDP L8701,L8708 stuff 0-ohm 0603

<Variant Name>

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Title			
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# POWER SEQUENCE

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
<b>POWER SEQUENCE</b>			
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A

B

C

D

E

4

4

3

3

2

2

1

1

A

B

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D

E

<Variant Name>

緯創資通

**Wistron Corporation**

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Title

**Power Block Diagram**

Size

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# Thermal Block Diagram

# Audio Block Diagram

