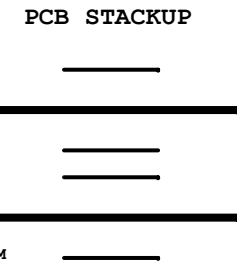
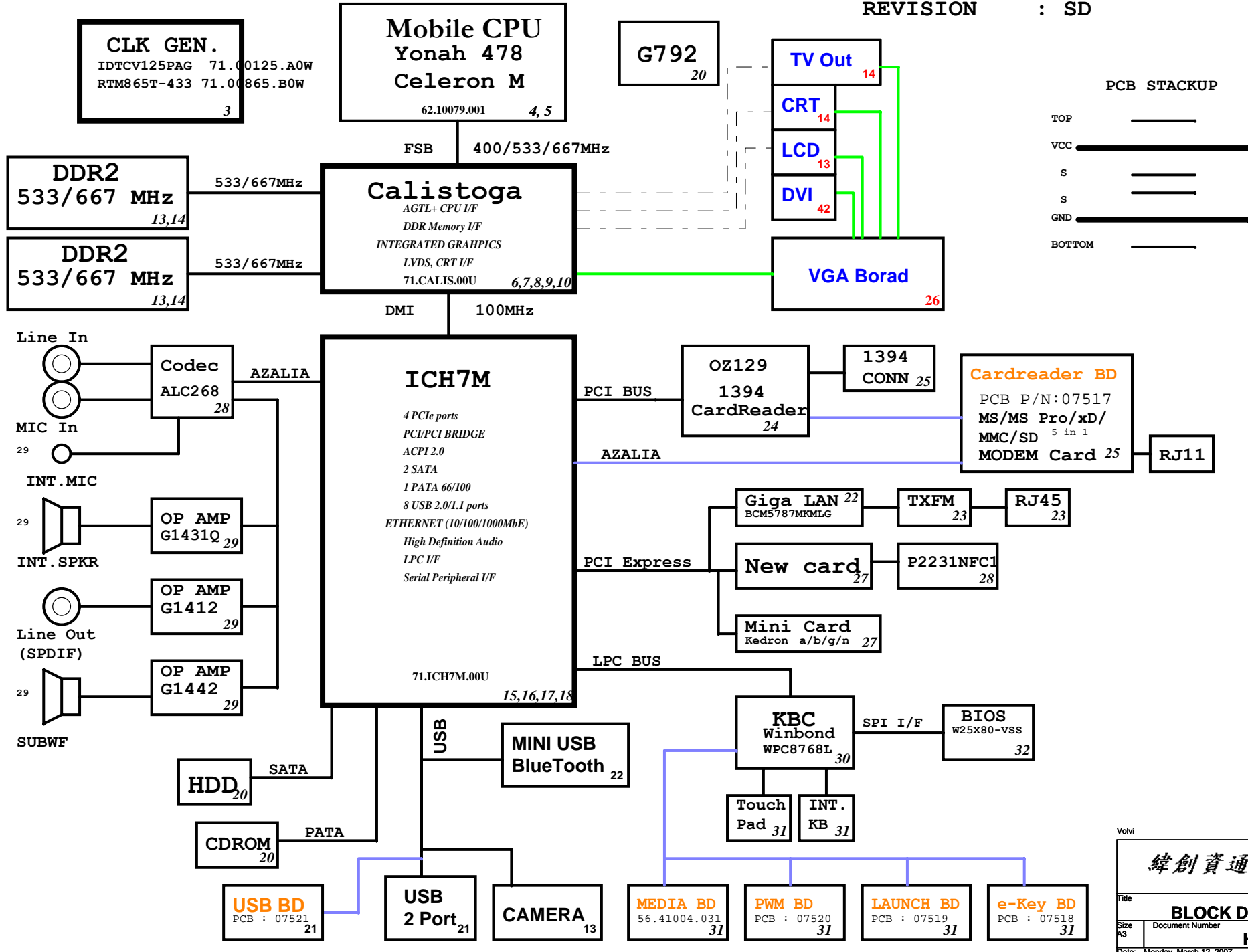


Huron Block Diagram

Project code: 91.4V301.001
 PCB P/N : 07205
 REVISION : SD



SYSTEM DC/DC TPS51120 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC TPS51124 38	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0

TPS51100 40	
INPUTS	OUTPUTS
1D8V_S3	DDR_VREF

APL5308 40	
INPUTS	OUTPUTS
3D3V_S0	2D5V_S0

APL5912 39	
INPUTS	OUTPUTS
1D8V_S3	1D5V_S0

Intersil CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

Volvi

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Title: **BLOCK DIAGRAM**

Size A3 Document Number **HURON** Rev SD

Date: Monday, March 12, 2007 Sheet 1 of 44

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

RTM865T-433 100Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	0.8% Down
0	0	0	1	1.0% Down
0	0	1	0	1.25% Down
0	0	1	1	1.50% Down
0	1	0	0	1.75% Down
0	1	0	1	2.0% Down
0	1	1	0	2.5% Down
0	1	1	1	3.0% Down
1	0	0	0	+0.3% Center
1	0	0	1	+0.4% Center
1	0	1	0	+0.5% Center
1	0	1	1	+0.6% Center
1	1	0	0	+0.8% Center
1	1	0	1	+1.0% Center
1	1	1	0	+1.25% Center
1	1	1	1	+1.5% Center

page 3

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
OZ129TZ	AD22	A-G	REQ0# ->REQ0#

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

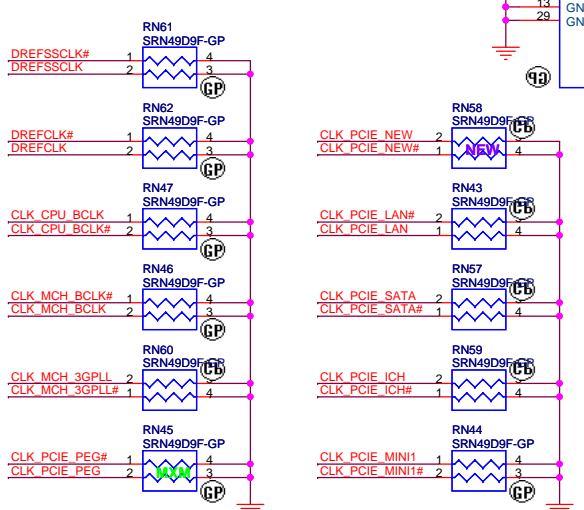
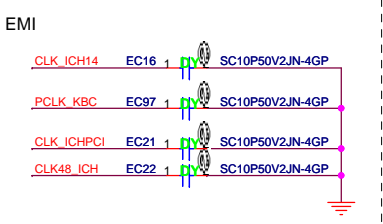
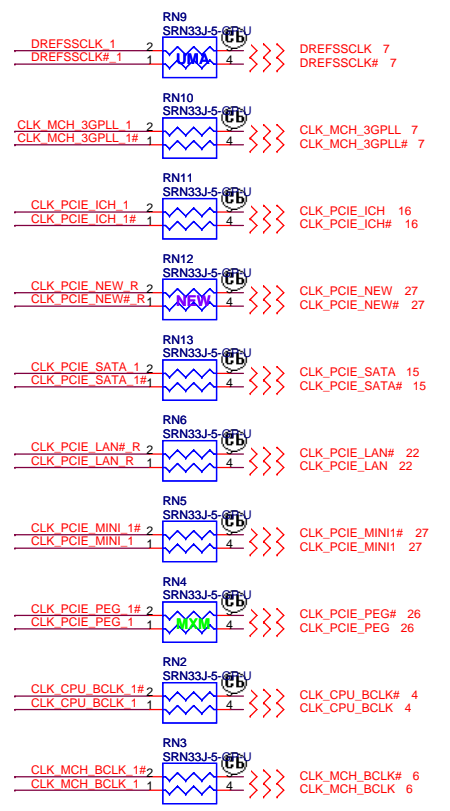
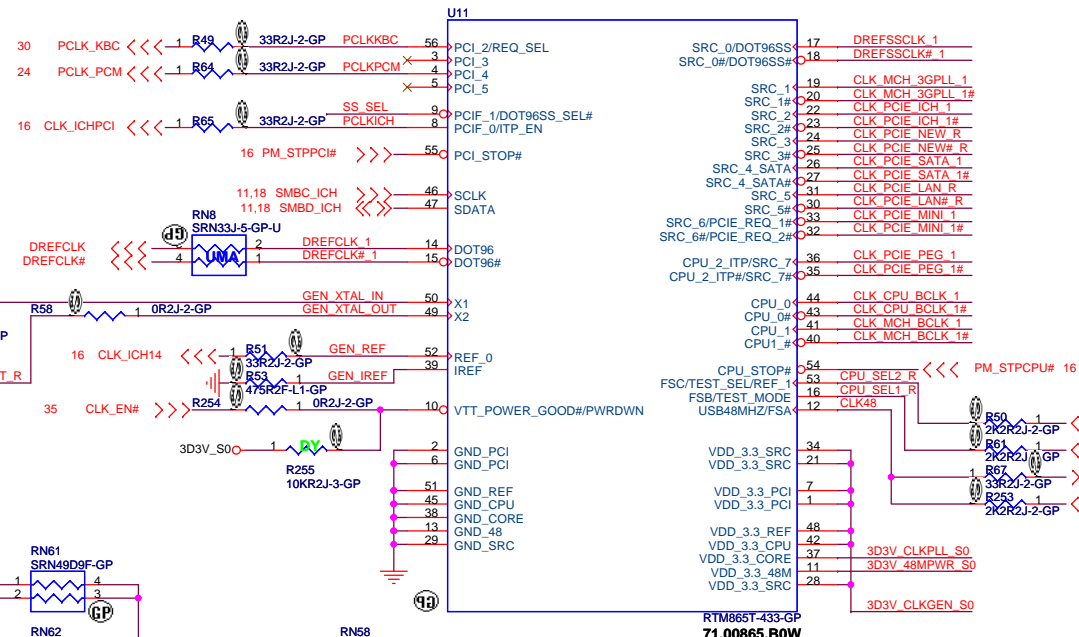
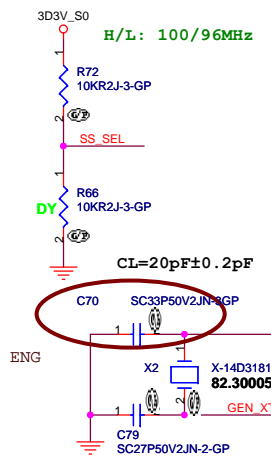
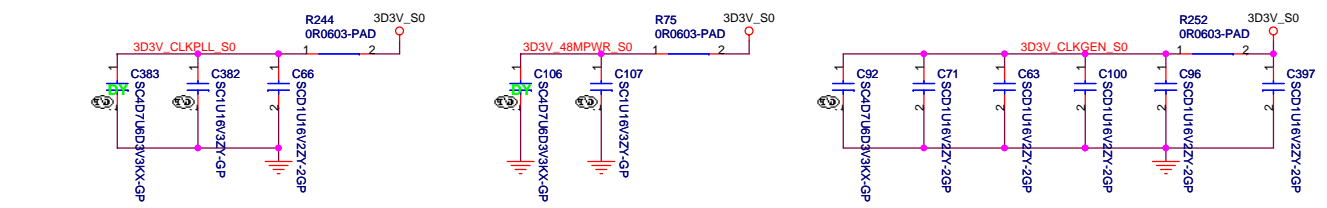
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane, 4->0, 3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

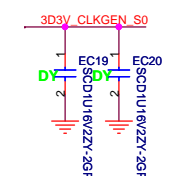
NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

<Core Design>

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Reference			
Title	Document Number		Rev
	HURON		SD
Date:	Monday, March 12, 2007	Sheet 2 of	44



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X



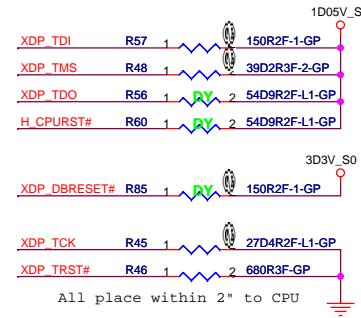
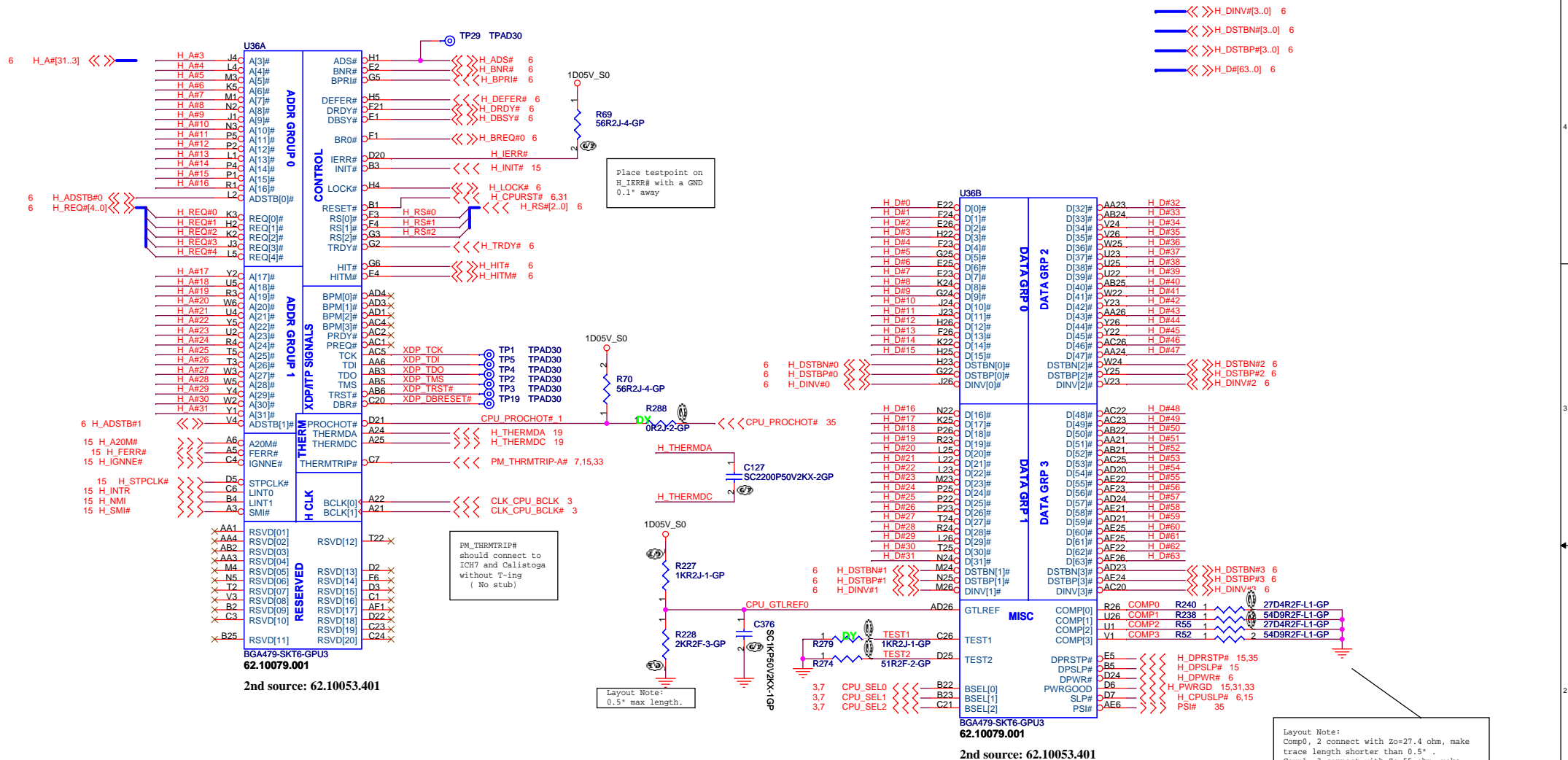
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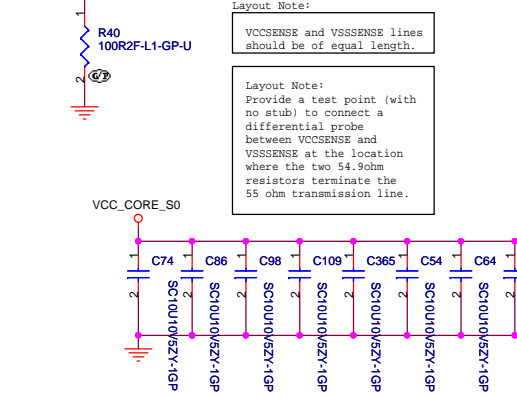
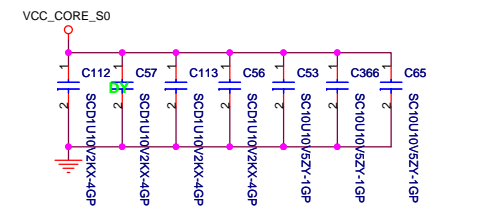
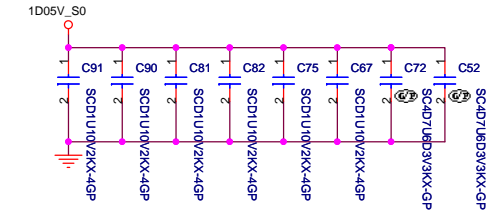
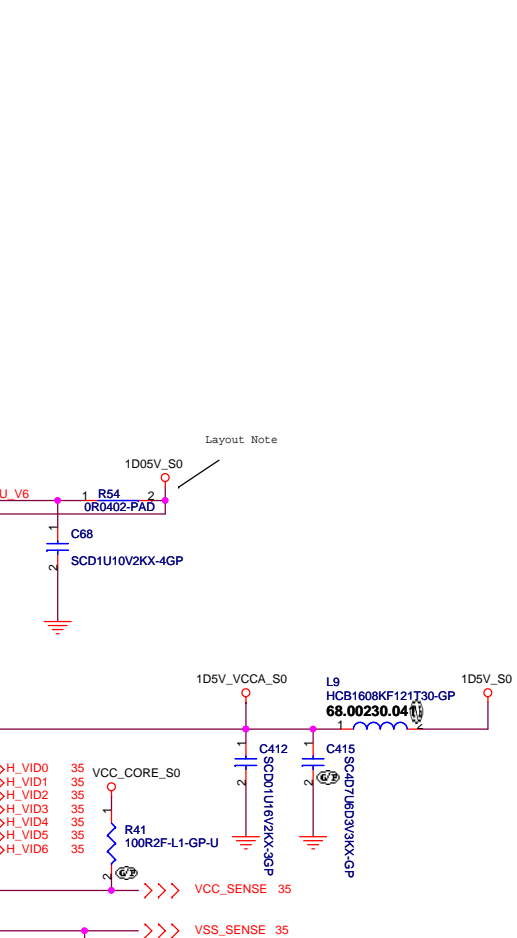
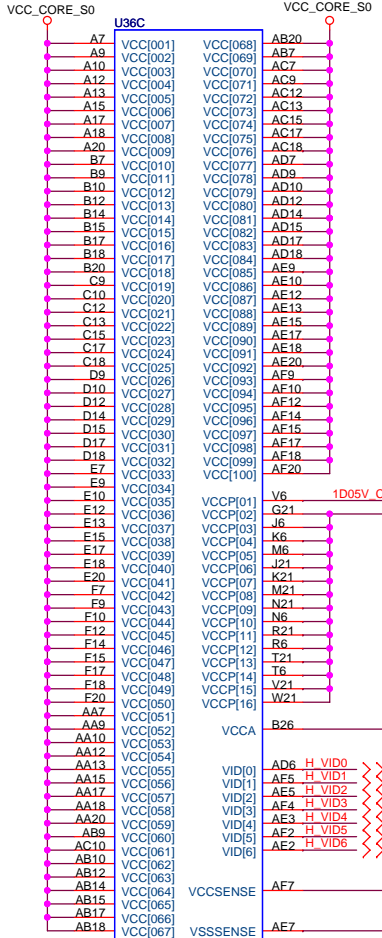
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Title: **Clock Generator**

Size: Document Number **HURON** Rev: **SD**

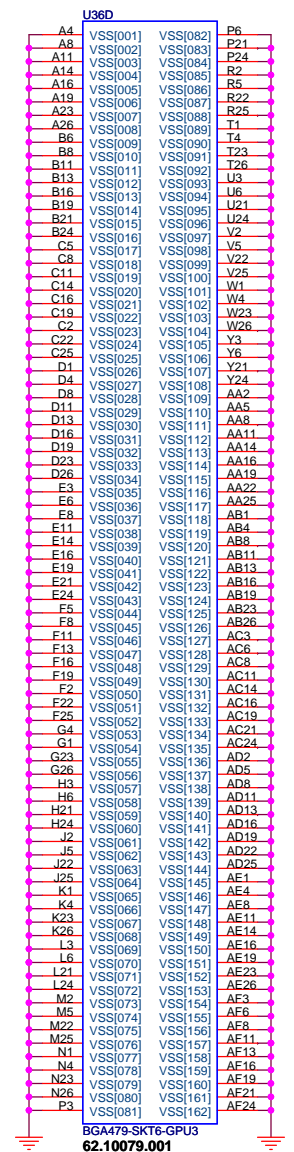
Date: Monday, March 12, 2007 Sheet 3 of 44

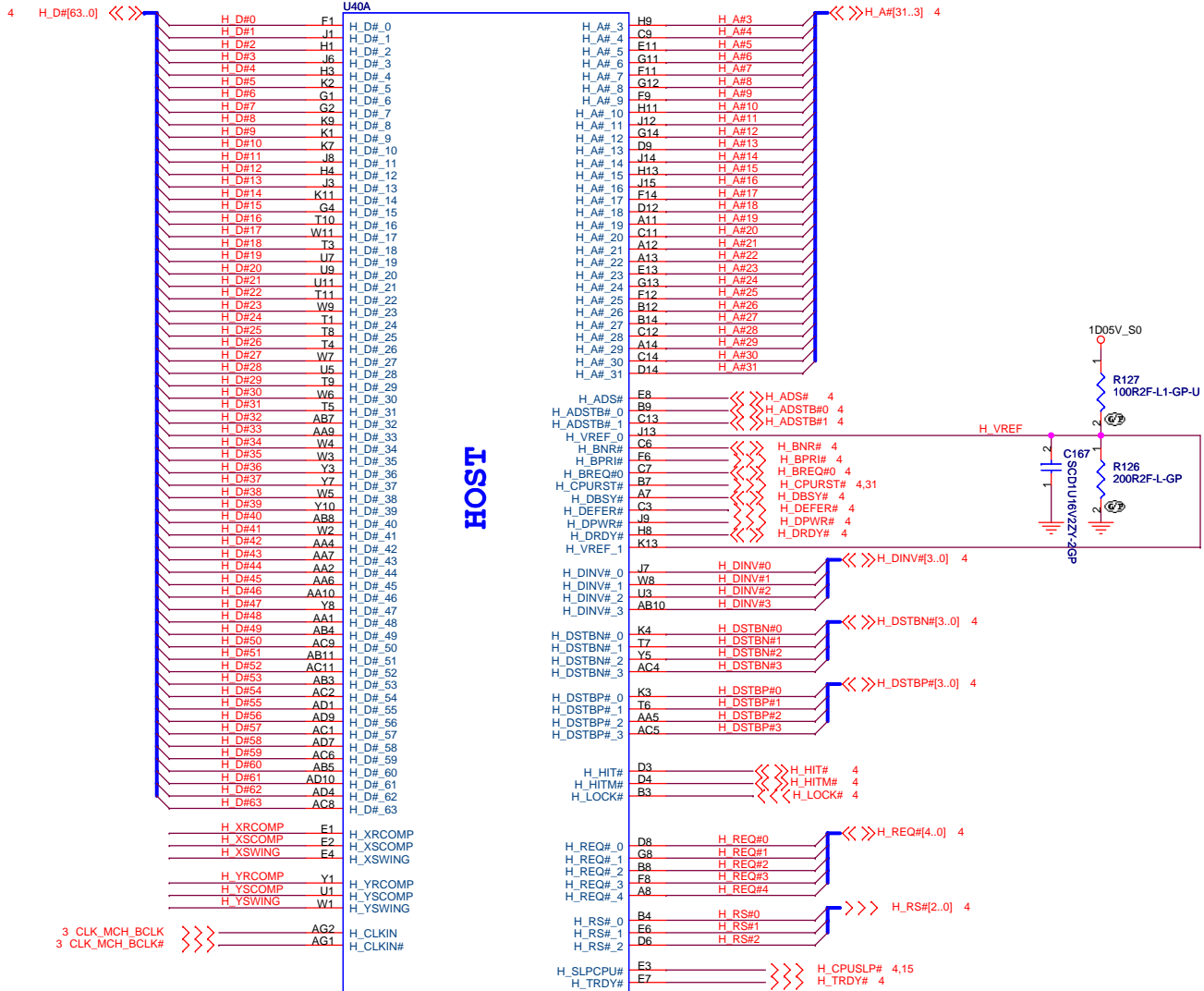
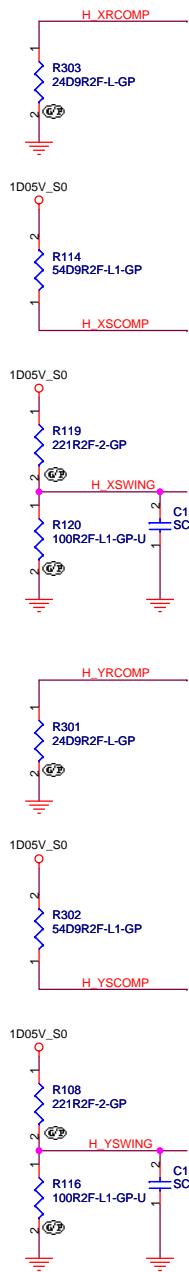




Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.





71.CALIS.00U
 DIS : 945PN P/N is KI.94501.006
 UMA : 945GM P/N is KI.94501.005

Place them near to the chip (< 0.5")

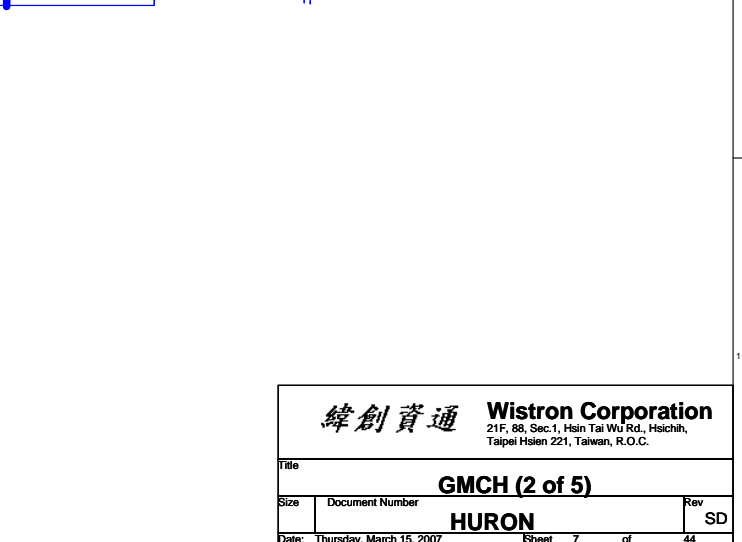
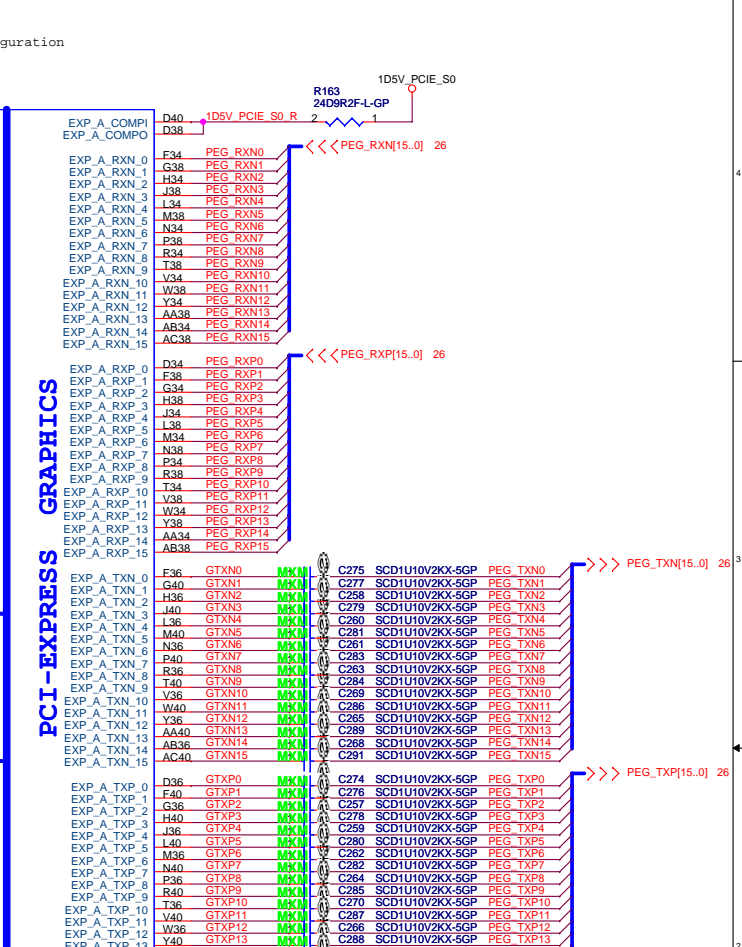
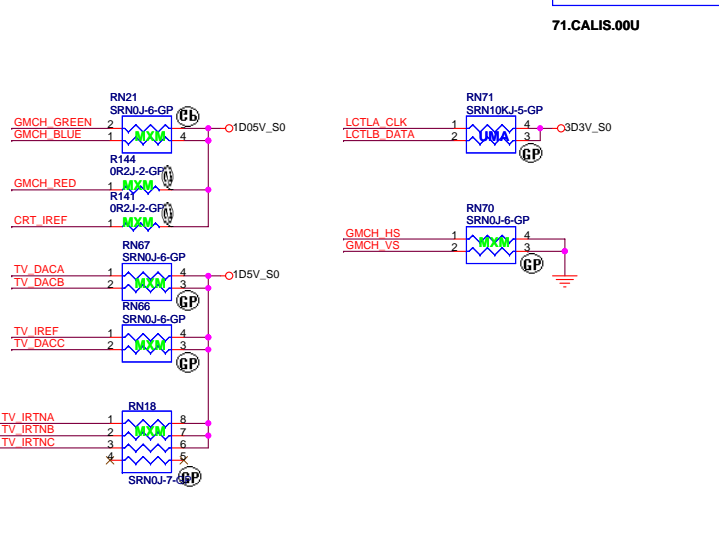
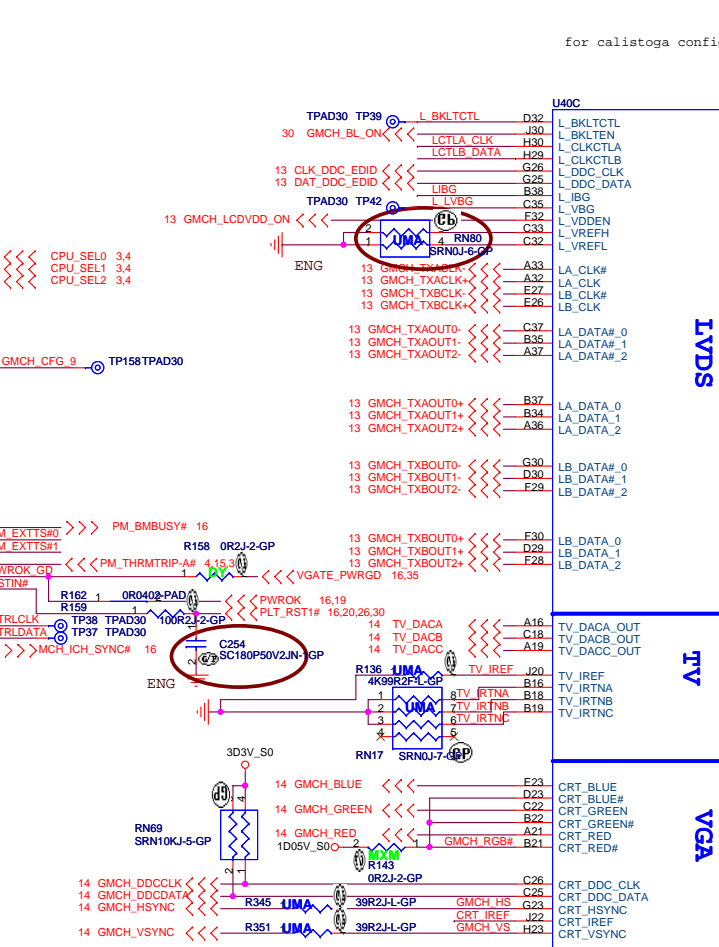
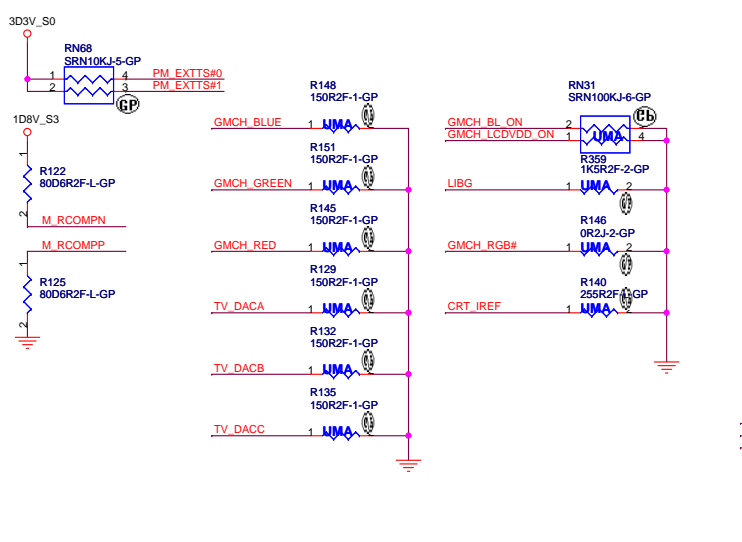
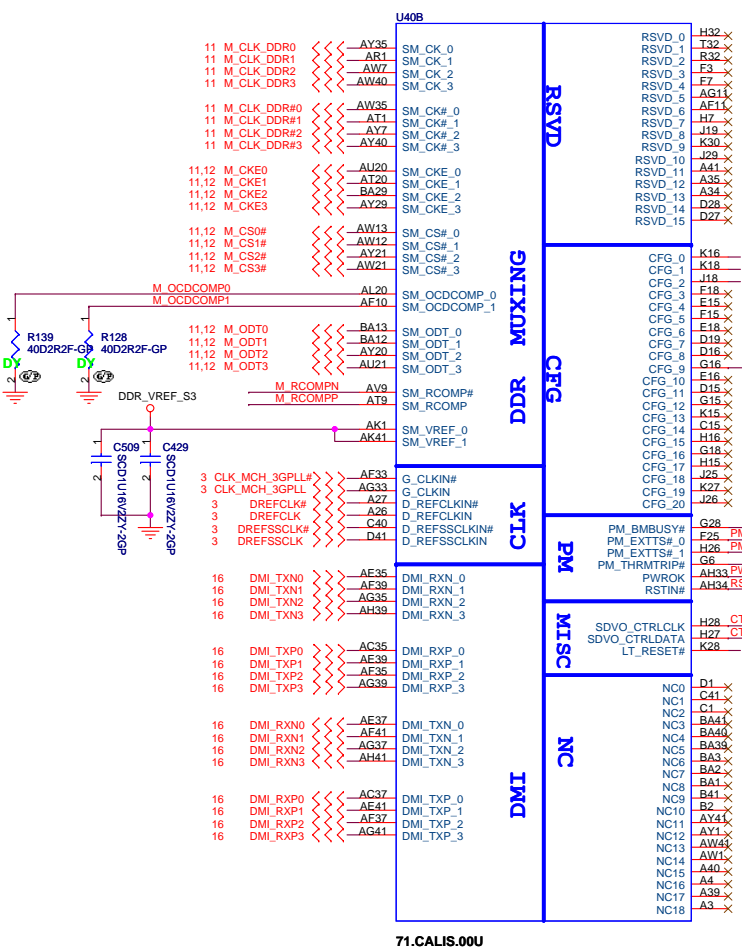
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Title: **GMCH (1 of 5)**

Size: Document Number: **HURON** Rev: **SD**

Date: Monday, March 12, 2007 Sheet 6 of 44



for calistoga configuration

71.CALIS.00U

71.CALIS.00U

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GMCH (2 of 5)

Size: Document Number: Rev: SD

Date: Thursday, March 15, 2007 Sheet 7 of 44

11 M_A_DQ[63.0] <<<

M A DQ0	AJ35	SA_DQ0
M A DQ1	AJ34	SA_DQ1
M A DQ2	AM31	SA_DQ2
M A DQ3	AM33	SA_DQ3
M A DQ4	AJ36	SA_DQ4
M A DQ5	AK35	SA_DQ5
M A DQ6	AJ32	SA_DQ6
M A DQ7	AH31	SA_DQ7
M A DQ8	AN35	SA_DQ8
M A DQ9	AP33	SA_DQ9
M A DQ10	AR31	SA_DQ10
M A DQ11	AP31	SA_DQ11
M A DQ12	AN38	SA_DQ12
M A DQ13	AM36	SA_DQ13
M A DQ14	AM34	SA_DQ14
M A DQ15	AN33	SA_DQ15
M A DQ16	AK26	SA_DQ16
M A DQ17	AL27	SA_DQ17
M A DQ18	AM26	SA_DQ18
M A DQ19	AN24	SA_DQ19
M A DQ20	AK28	SA_DQ20
M A DQ21	AL28	SA_DQ21
M A DQ22	AM24	SA_DQ22
M A DQ23	AP26	SA_DQ23
M A DQ24	AP23	SA_DQ24
M A DQ25	AL22	SA_DQ25
M A DQ26	AP21	SA_DQ26
M A DQ27	AN20	SA_DQ27
M A DQ28	AL23	SA_DQ28
M A DQ29	AP24	SA_DQ29
M A DQ30	AP20	SA_DQ30
M A DQ31	AT21	SA_DQ31
M A DQ32	AR12	SA_DQ32
M A DQ33	AR14	SA_DQ33
M A DQ34	AP13	SA_DQ34
M A DQ35	AP12	SA_DQ35
M A DQ36	AT13	SA_DQ36
M A DQ37	AT12	SA_DQ37
M A DQ38	AL14	SA_DQ38
M A DQ39	AL12	SA_DQ39
M A DQ40	AK9	SA_DQ40
M A DQ41	AN7	SA_DQ41
M A DQ42	AK8	SA_DQ42
M A DQ43	AK7	SA_DQ43
M A DQ44	AP9	SA_DQ44
M A DQ45	AN9	SA_DQ45
M A DQ46	AT5	SA_DQ46
M A DQ47	AL5	SA_DQ47
M A DQ48	AY2	SA_DQ48
M A DQ49	AW2	SA_DQ49
M A DQ50	AP1	SA_DQ50
M A DQ51	AN2	SA_DQ51
M A DQ52	AV2	SA_DQ52
M A DQ53	AT3	SA_DQ53
M A DQ54	AN1	SA_DQ54
M A DQ55	AL2	SA_DQ55
M A DQ56	AC7	SA_DQ56
M A DQ57	AF9	SA_DQ57
M A DQ58	AG4	SA_DQ58
M A DQ59	AF6	SA_DQ59
M A DQ60	AG9	SA_DQ60
M A DQ61	AH6	SA_DQ61
M A DQ62	AF4	SA_DQ62
M A DQ63	AF8	SA_DQ63

71.CALIS.00U

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M A BS#0 11,12
SA_BS_1	AV14	M A BS#1 11,12
SA_BS_2	BA20	M A BS#2 11,12
SA_CAS#	AY13	M A CAS# 11,12
SA_DM_0	AJ33	M A DM0 11,12
SA_DM_1	AM35	M A DM1 11,12
SA_DM_2	AL26	M A DM2 11,12
SA_DM_3	AN22	M A DM3 11,12
SA_DM_4	AM14	M A DM4 11,12
SA_DM_5	AL9	M A DM5 11,12
SA_DM_6	AR3	M A DM6 11,12
SA_DM_7	AH4	M A DM7 11,12
SA_DQS_0	AK33	M A DQS0 11,12
SA_DQS_1	AT33	M A DQS1 11,12
SA_DQS_2	AN28	M A DQS2 11,12
SA_DQS_3	AM22	M A DQS3 11,12
SA_DQS_4	AN12	M A DQS4 11,12
SA_DQS_5	AN8	M A DQS5 11,12
SA_DQS_6	AP3	M A DQS6 11,12
SA_DQS_7	AG5	M A DQS7 11,12
SA_DQS#_0	AK32	M A DQS#0 11,12
SA_DQS#_1	AU33	M A DQS#1 11,12
SA_DQS#_2	AN27	M A DQS#2 11,12
SA_DQS#_3	AM21	M A DQS#3 11,12
SA_DQS#_4	AM12	M A DQS#4 11,12
SA_DQS#_5	AL8	M A DQS#5 11,12
SA_DQS#_6	AN3	M A DQS#6 11,12
SA_DQS#_7	AH5	M A DQS#7 11,12
SA_MA_0	AY16	M A A0 11,12
SA_MA_1	AU14	M A A1 11,12
SA_MA_2	AW16	M A A2 11,12
SA_MA_3	BA16	M A A3 11,12
SA_MA_4	BA17	M A A4 11,12
SA_MA_5	AU16	M A A5 11,12
SA_MA_6	AV17	M A A6 11,12
SA_MA_7	AL17	M A A7 11,12
SA_MA_8	AW17	M A A8 11,12
SA_MA_9	AT16	M A A9 11,12
SA_MA_10	AU13	M A A10 11,12
SA_MA_11	AT17	M A A11 11,12
SA_MA_12	AV20	M A A12 11,12
SA_MA_13	AV12	M A A13 11,12
SA_RAS#	AW14	M A RAS# 11,12
SA_RCVENIN#	AK23	M A RCVENIN# 11,12
SA_RCVENOUT#	AK24	M A RCVENOUT# 11,12
SA_WE#	AY14	M A WE# 11,12

Place Test PAD Near to Chip as could as possible

11 M_B_DQ[63.0] <<<

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP39	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AT40	SB_DQ8
M B DQ9	AV41	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AW38	SB_DQ14
M B DQ15	AY38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AV36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	BA36	SB_DQ20
M B DQ21	AU36	SB_DQ21
M B DQ22	AP35	SB_DQ22
M B DQ23	AP34	SB_DQ23
M B DQ24	AY33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AP30	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AL31	SB_DQ29
M B DQ30	AW29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AM19	SB_DQ32
M B DQ33	AL19	SB_DQ33
M B DQ34	AP14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AK10	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AW5	SB_DQ54
M B DQ55	AY5	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AT4	SB_DQ59
M B DQ60	AK3	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

U40E

DDR SYSTEM MEMORY B

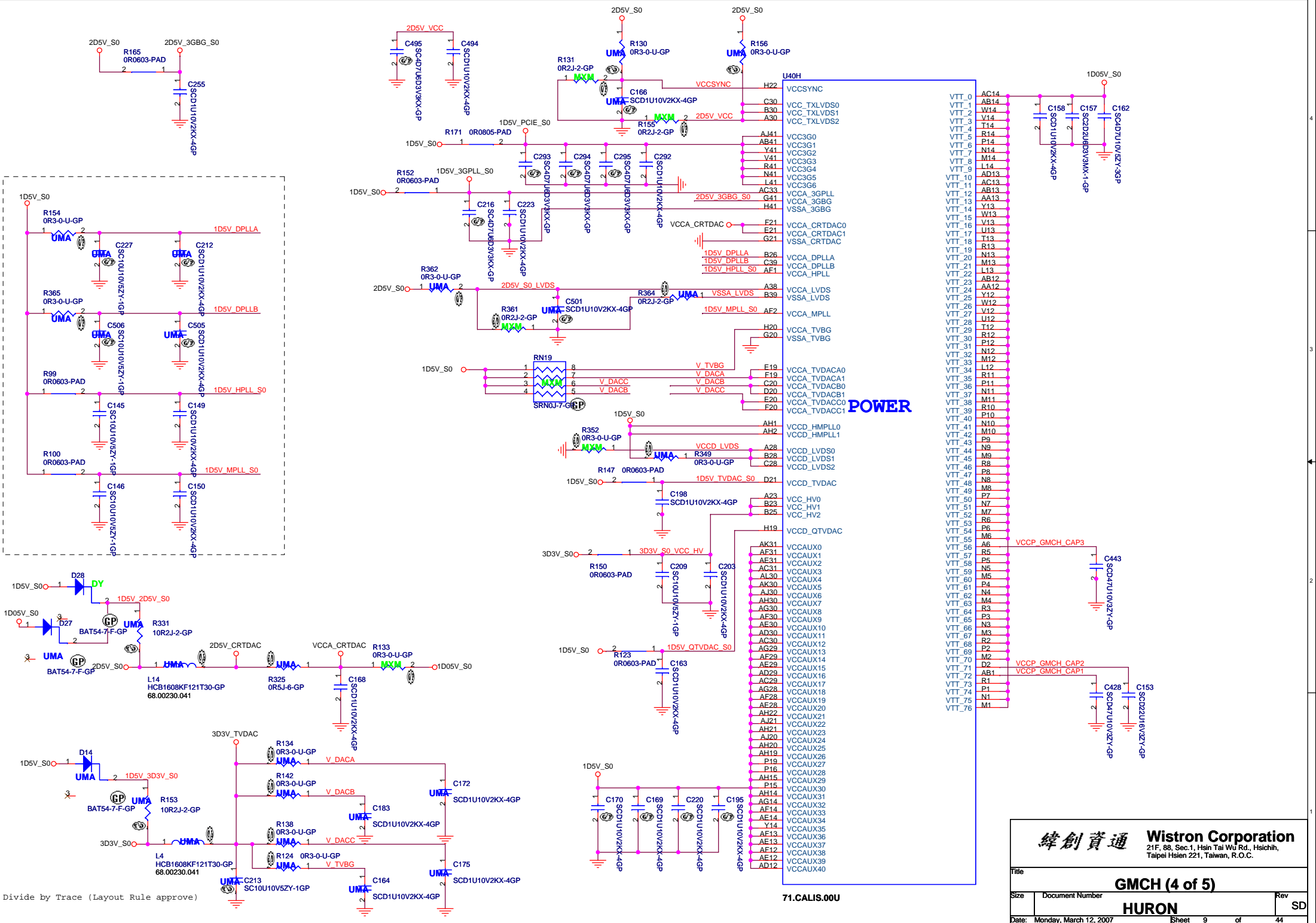
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SB_BS_1	AV23	M B BS#1 11,12
SB_BS_2	AY28	M B BS#2 11,12
SB_CAS#	AR24	M B CAS# 11,12
SB_DM_0	AK36	M B DM0 11,12
SB_DM_1	AR38	M B DM1 11,12
SB_DM_2	AT36	M B DM2 11,12
SB_DM_3	BA31	M B DM3 11,12
SB_DM_4	AL17	M B DM4 11,12
SB_DM_5	AH8	M B DM5 11,12
SB_DM_6	BA5	M B DM6 11,12
SB_DM_7	AN4	M B DM7 11,12
SB_DQS_0	AM39	M B DQS0 11,12
SB_DQS_1	AT39	M B DQS1 11,12
SB_DQS_2	AU35	M B DQS2 11,12
SB_DQS_3	AR29	M B DQS3 11,12
SB_DQS_4	AR16	M B DQS4 11,12
SB_DQS_5	AR10	M B DQS5 11,12
SB_DQS_6	AR7	M B DQS6 11,12
SB_DQS_7	AN5	M B DQS7 11,12
SB_DQS#_0	AM40	M B DQS#0 11,12
SB_DQS#_1	AU39	M B DQS#1 11,12
SB_DQS#_2	AT35	M B DQS#2 11,12
SB_DQS#_3	AP29	M B DQS#3 11,12
SB_DQS#_4	AP16	M B DQS#4 11,12
SB_DQS#_5	AT10	M B DQS#5 11,12
SB_DQS#_6	AT7	M B DQS#6 11,12
SB_DQS#_7	AP5	M B DQS#7 11,12
SB_MA_0	AY23	M B A0 11,12
SB_MA_1	AW24	M B A1 11,12
SB_MA_2	AR28	M B A2 11,12
SB_MA_3	AT27	M B A3 11,12
SB_MA_4	AT28	M B A4 11,12
SB_MA_5	AU27	M B A5 11,12
SB_MA_6	AV28	M B A6 11,12
SB_MA_7	AV27	M B A7 11,12
SB_MA_8	AW27	M B A8 11,12
SB_MA_9	AV24	M B A9 11,12
SB_MA_10	BA27	M B A10 11,12
SB_MA_11	AY27	M B A11 11,12
SB_MA_12	AR23	M B A12 11,12
SB_MA_13		
SB_RAS#	AU23	M B RAS# 11,12
SB_RCVENIN#	AK16	M B RCVENIN# 11,12
SB_RCVENOUT#	AK18	M B RCVENOUT# 11,12
SB_WE#	AR27	M B WE# 11,12

Place Test PAD Near to Chip as could as possible

71.CALIS.00U

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Title			GMCH (3 of 5)		
Size	Document Number		Rev		SD
Date: Monday, March 12, 2007			Sheet 8 of 44		



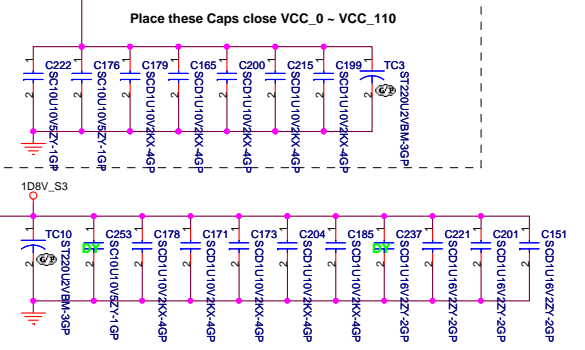
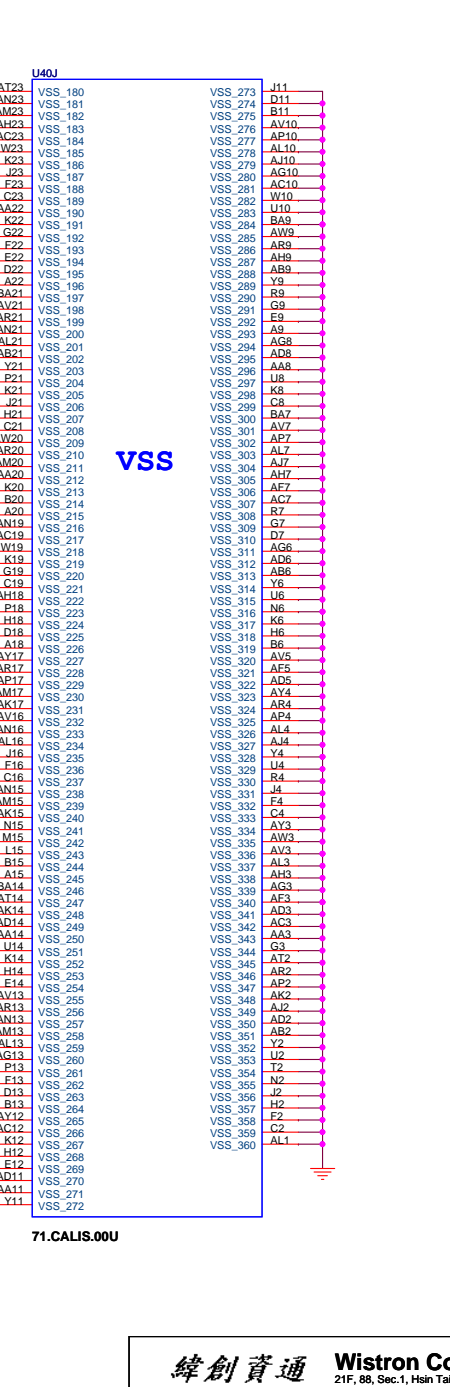
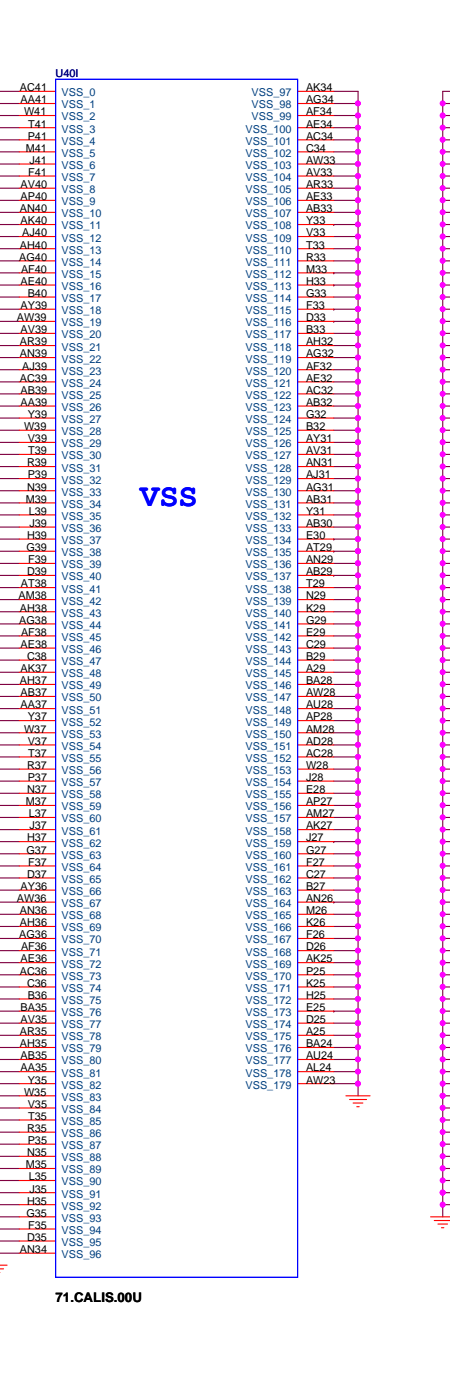
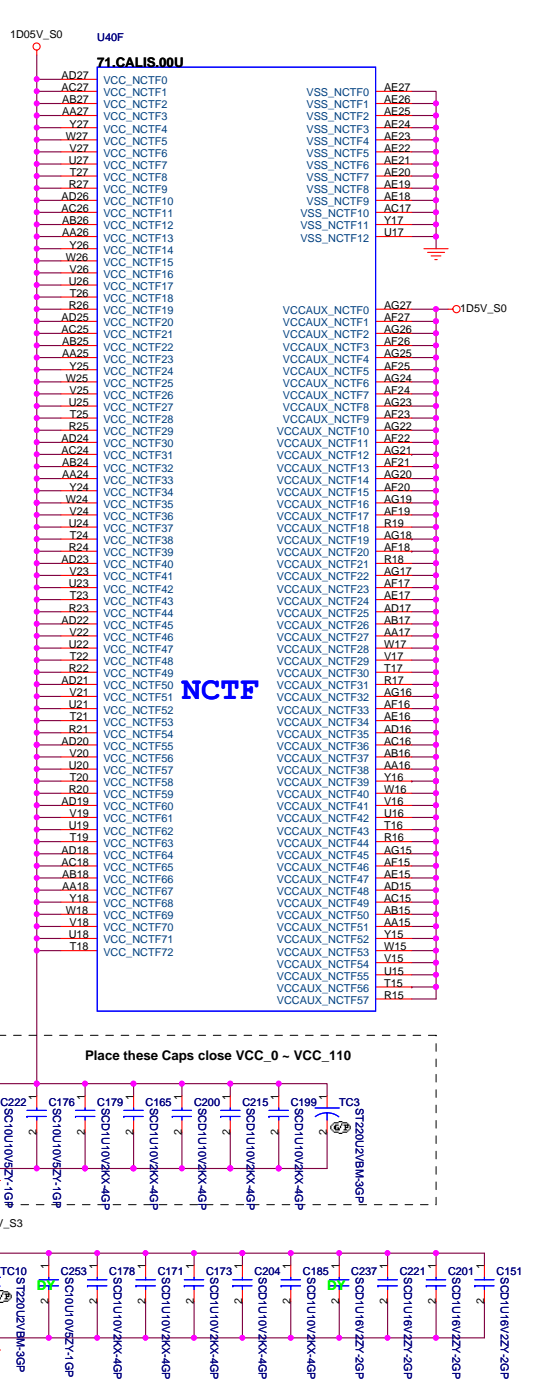
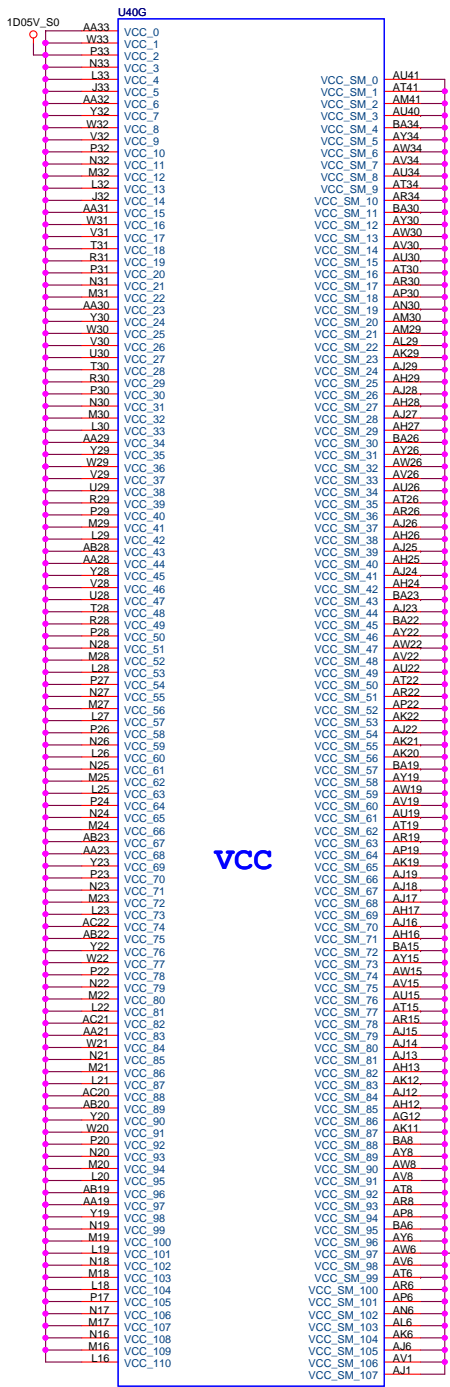
POWER

71.CALIS.00U

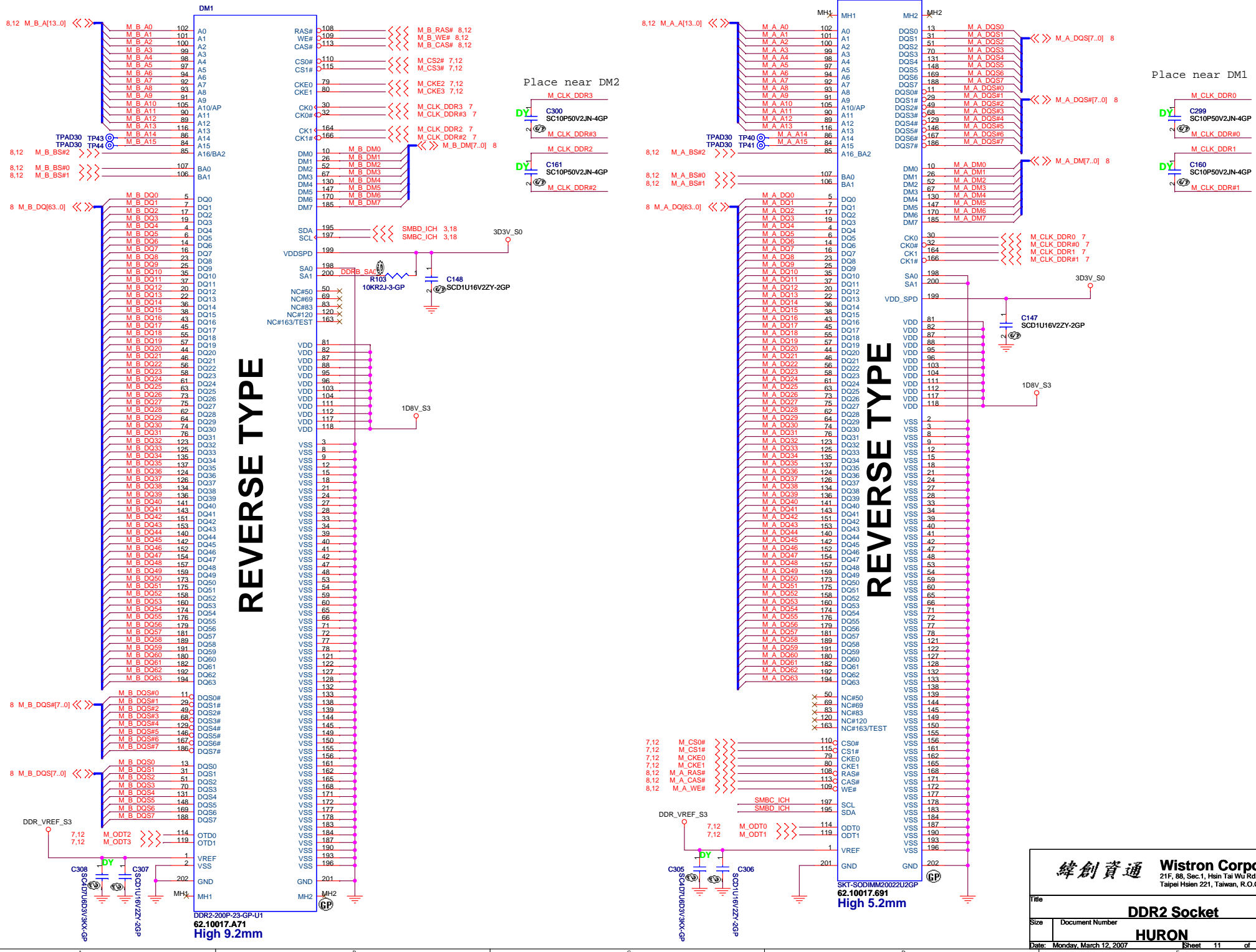
緯創資通 **Wistron Corporation**
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Title		GMCH (4 of 5)	
Size	Document Number	Rev	SD
Date: Monday, March 12, 2007		Sheet	9 of 44

Divide by Trace (Layout Rule approve)



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Taipei Hsien 221, Taiwan, R.O.C.

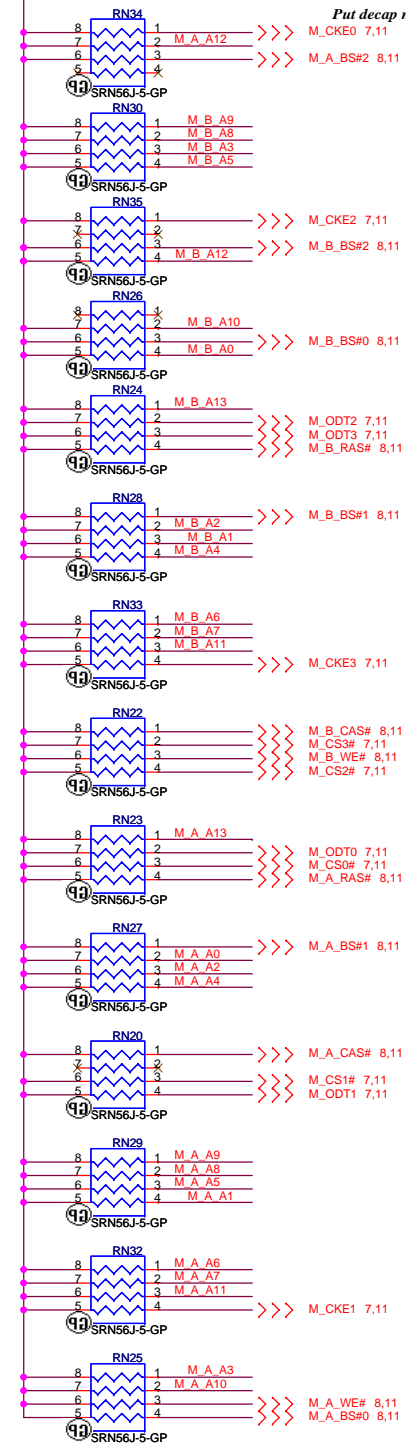
DDR2 Socket

HURON

Date: Monday, March 12, 2007 Sheet 11 of 44

PARALLEL TERMINATION

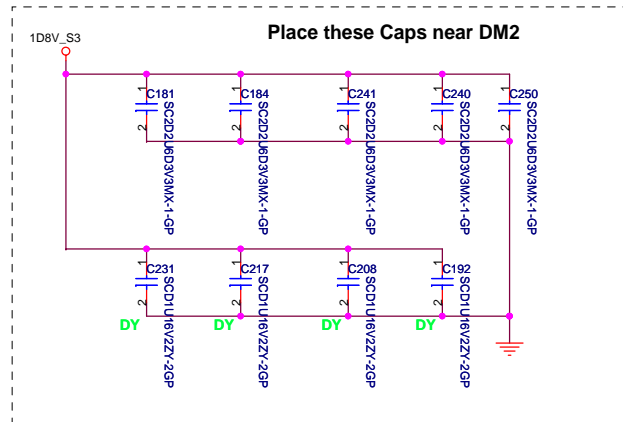
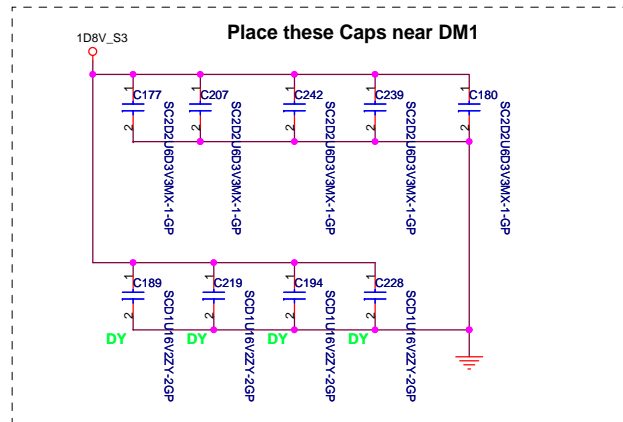
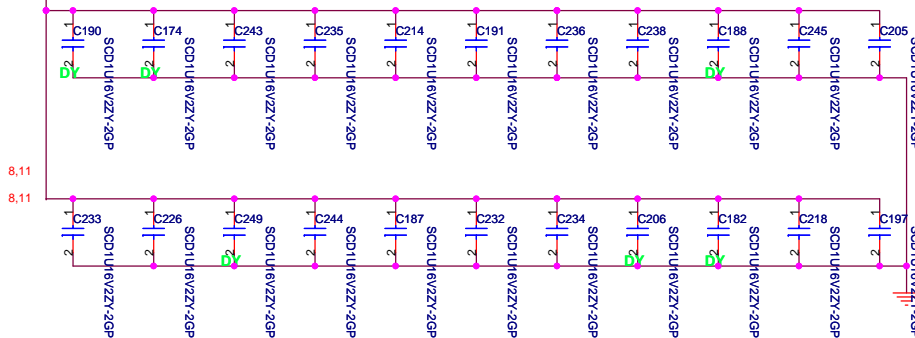
DDR_VREF_S0



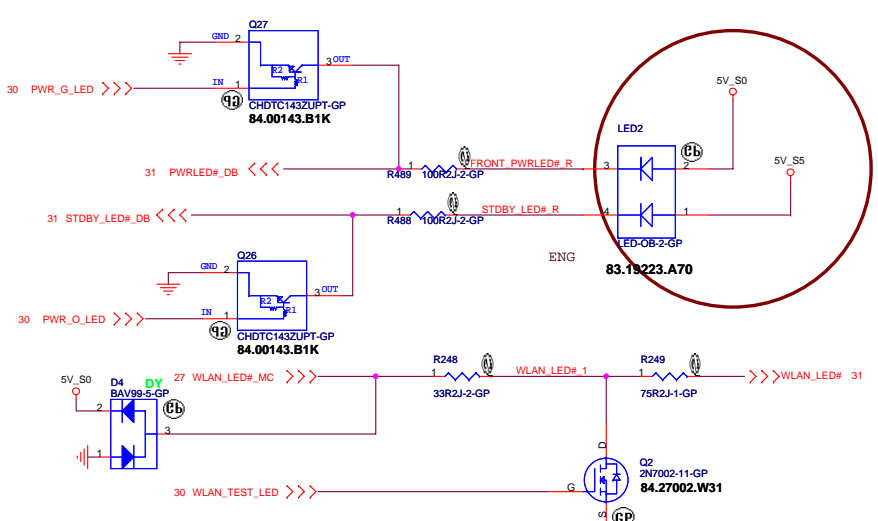
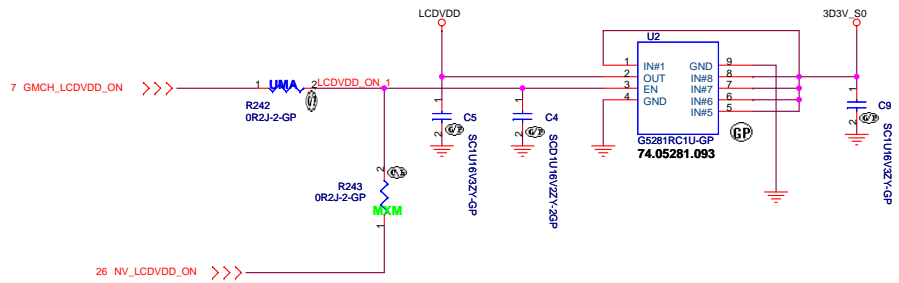
M.A A13..0 <<< M.A A13..0 8,11
M.B A13..0 <<< M.B A13..0 8,11

Decoupling Capacitor

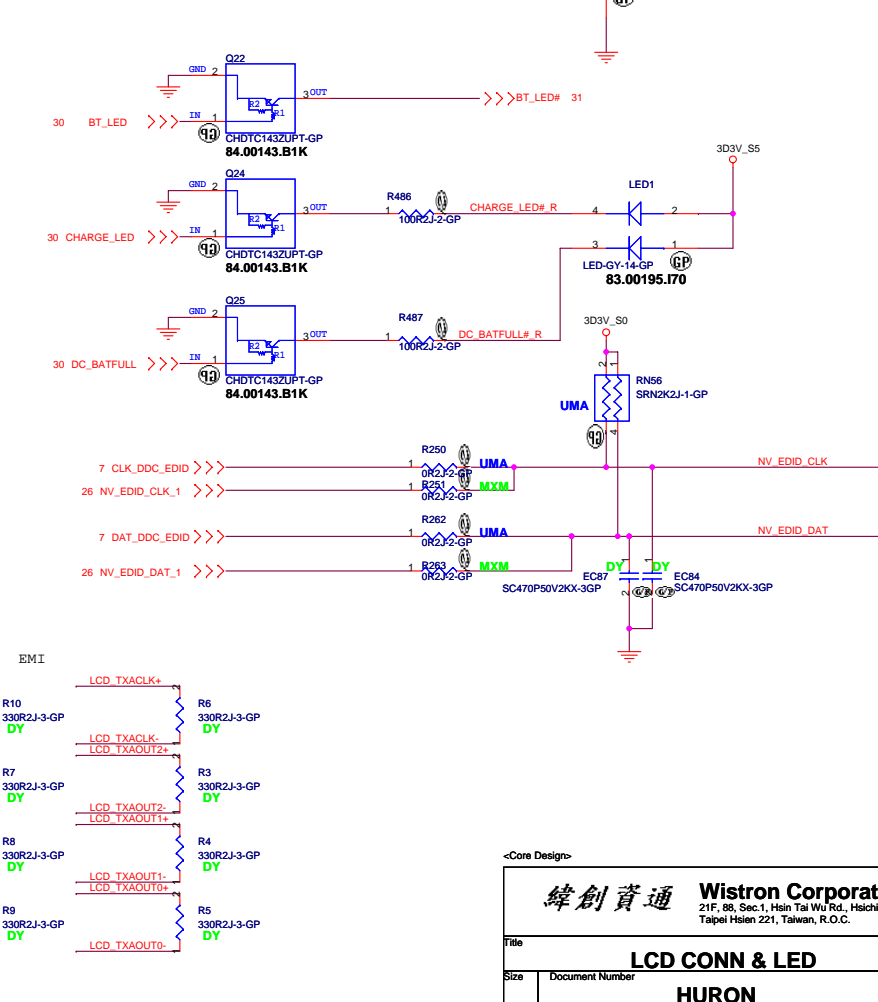
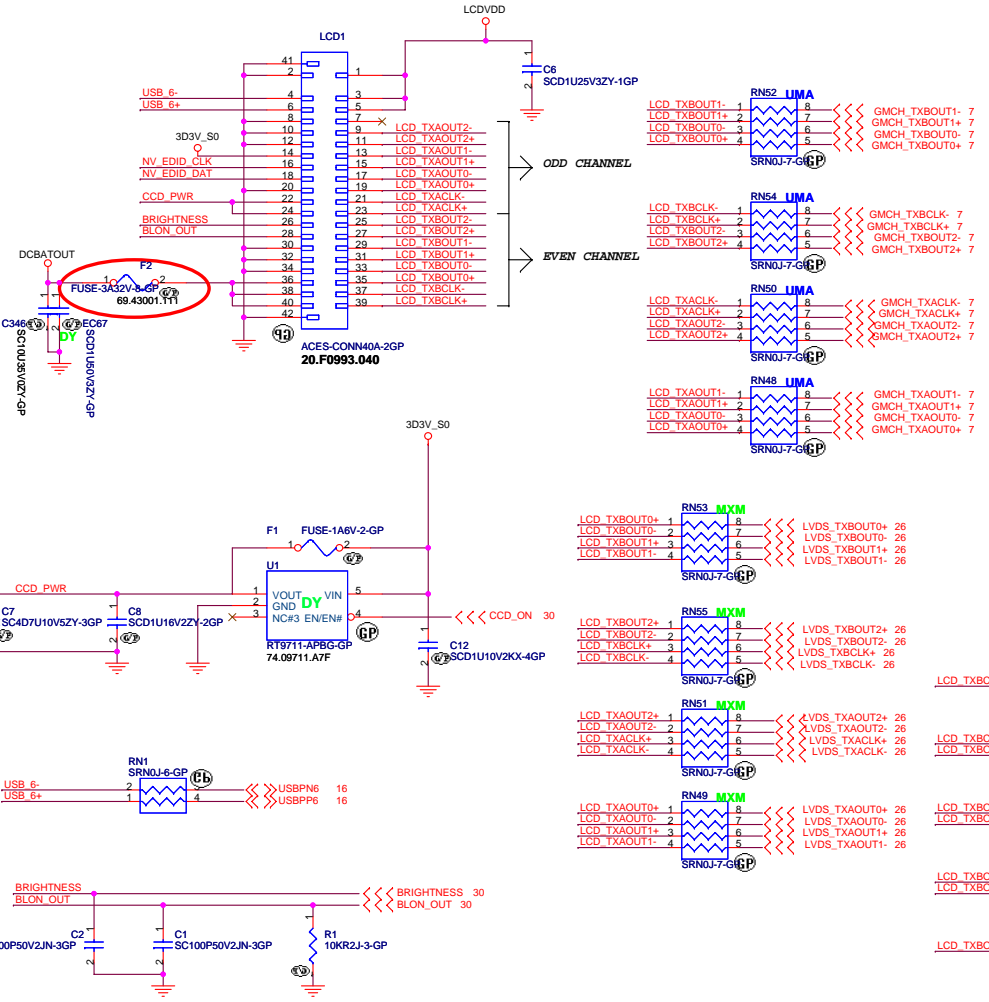
DDR_VREF_S0



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DDR2 Termination Resistor	
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LCD/INVERTER CONN



<Core Design>

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File: **LCD CONN & LED**

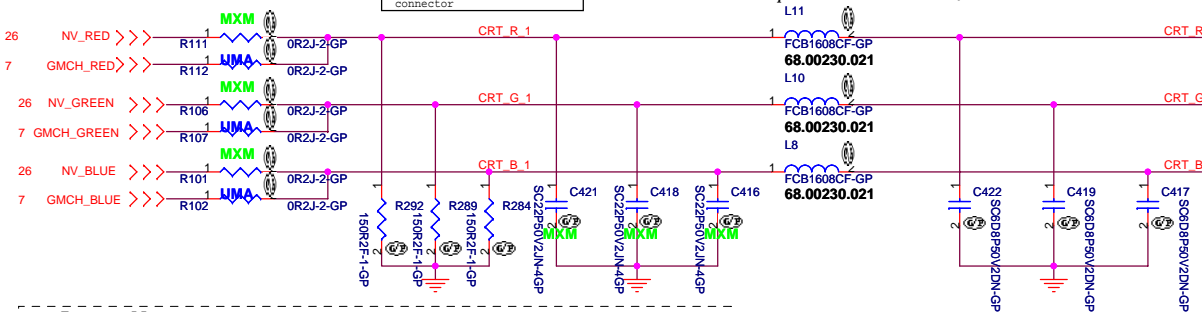
Size	Document Number
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HURON Rev SD

CRT I/F & CONNECTOR

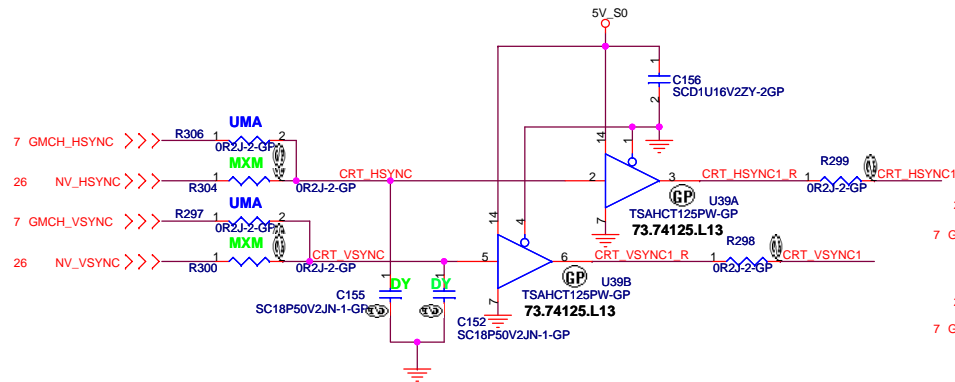
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

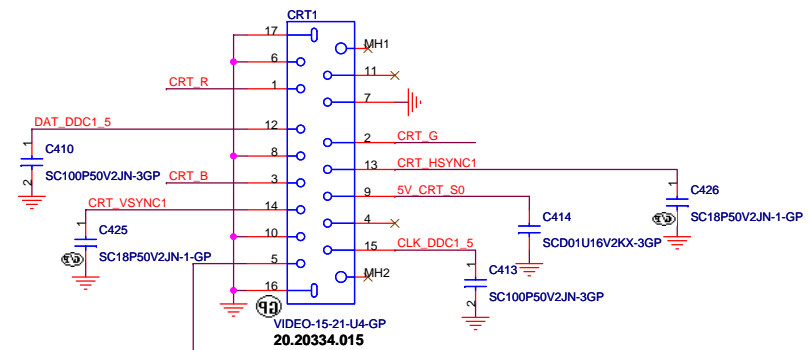
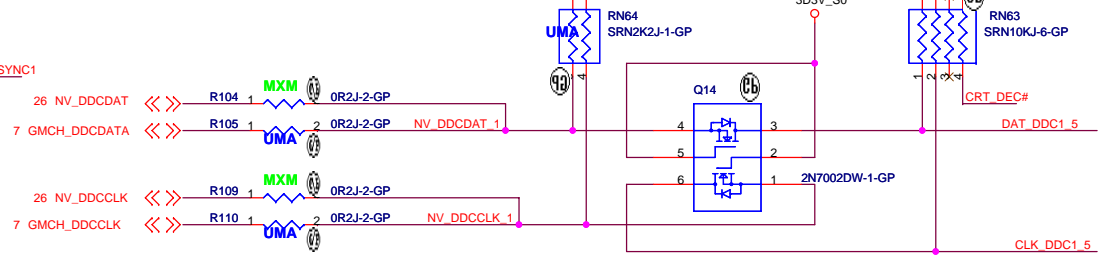


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

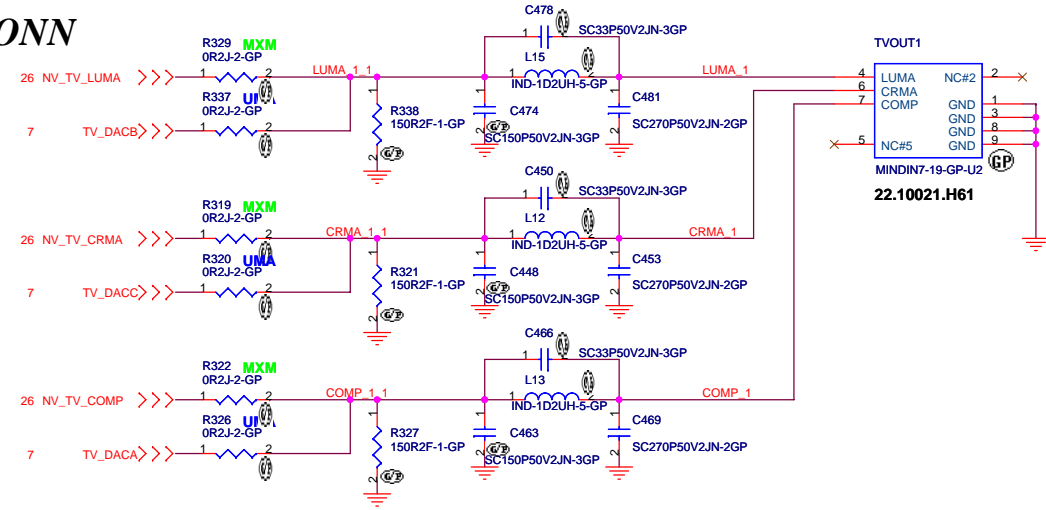
Hsync & Vsync level shift



DDC_CLK & DATA level shift

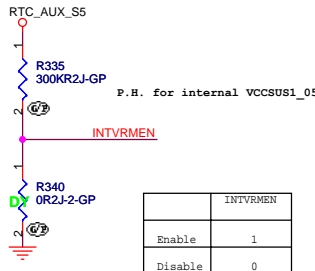
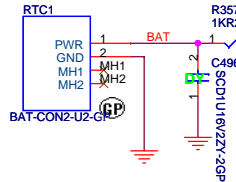


TV CONN



Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CRT/TV Connector	
Size	Document Number
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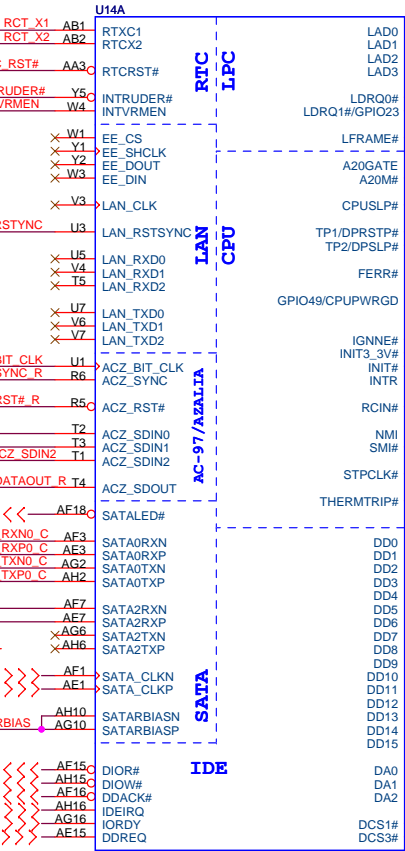
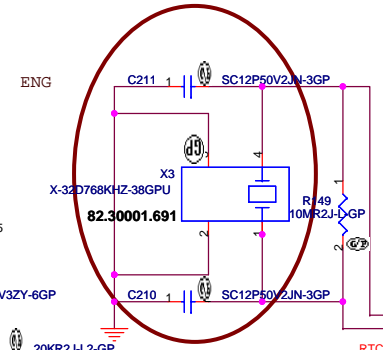
RTC circuitry



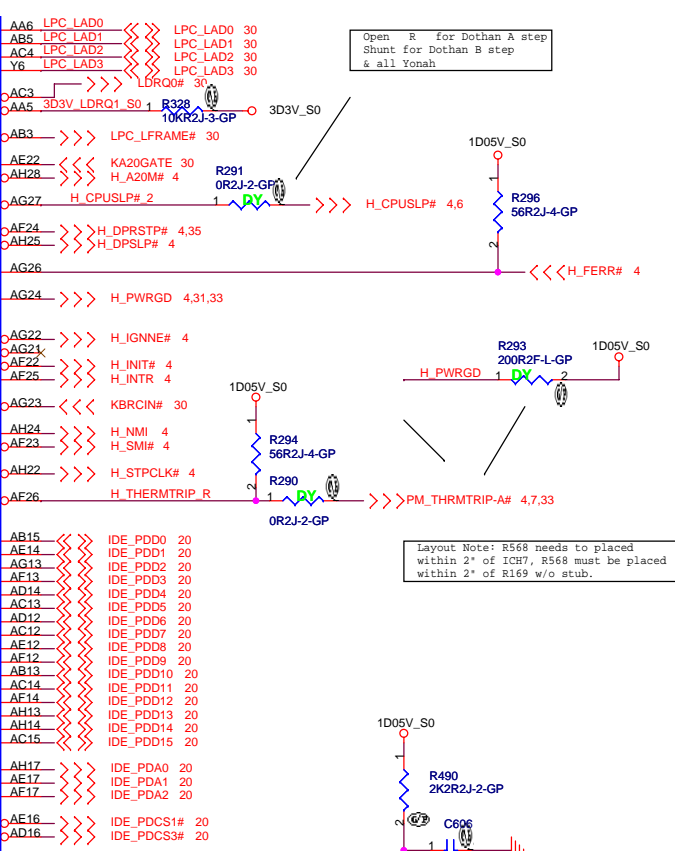
	INTVRMEN
Enable	1
Disable	0

Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

Place within 500 mils of ICH7ball



71.ICH7M.00U
PN:KI.80101.017



Open R for Dothan A step
Shunt for Dothan B step
& all Yonah

Layout Note: R568 needs to be placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.

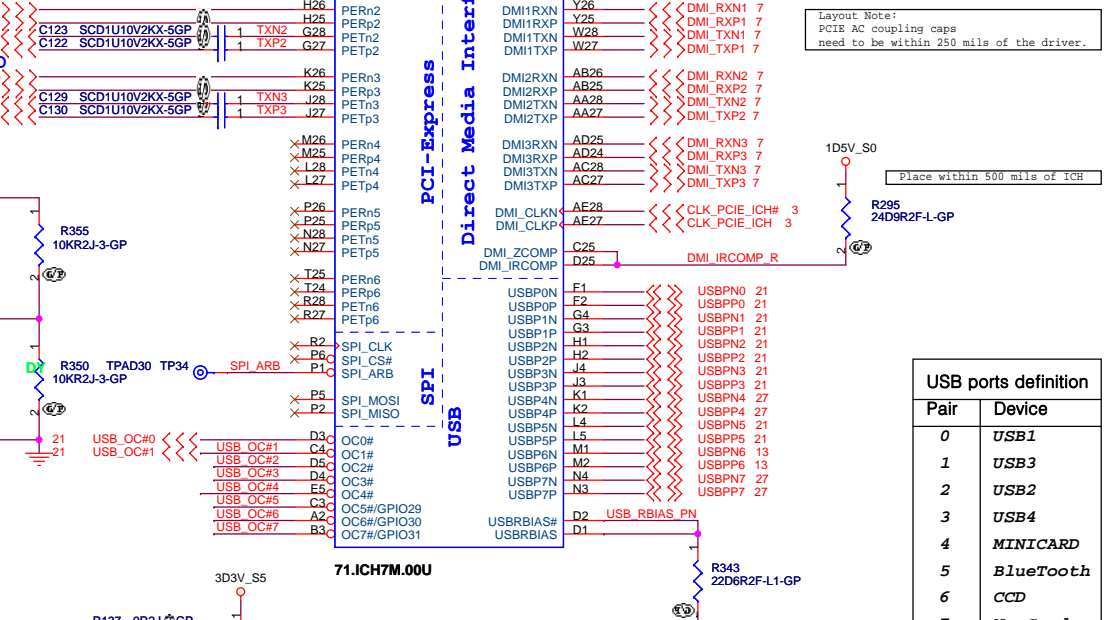
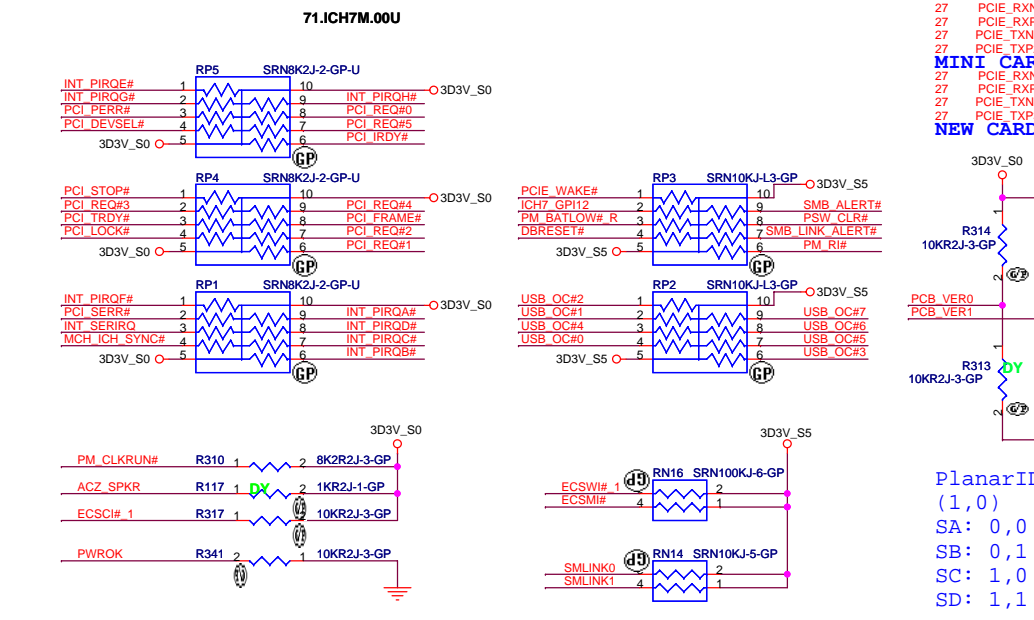
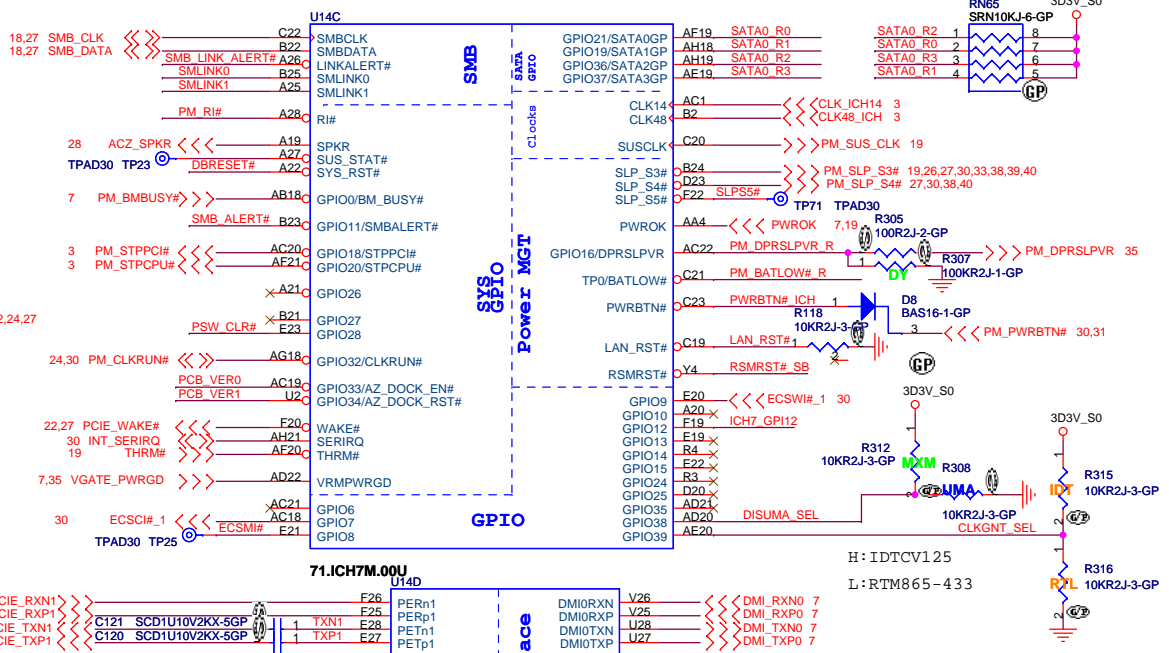
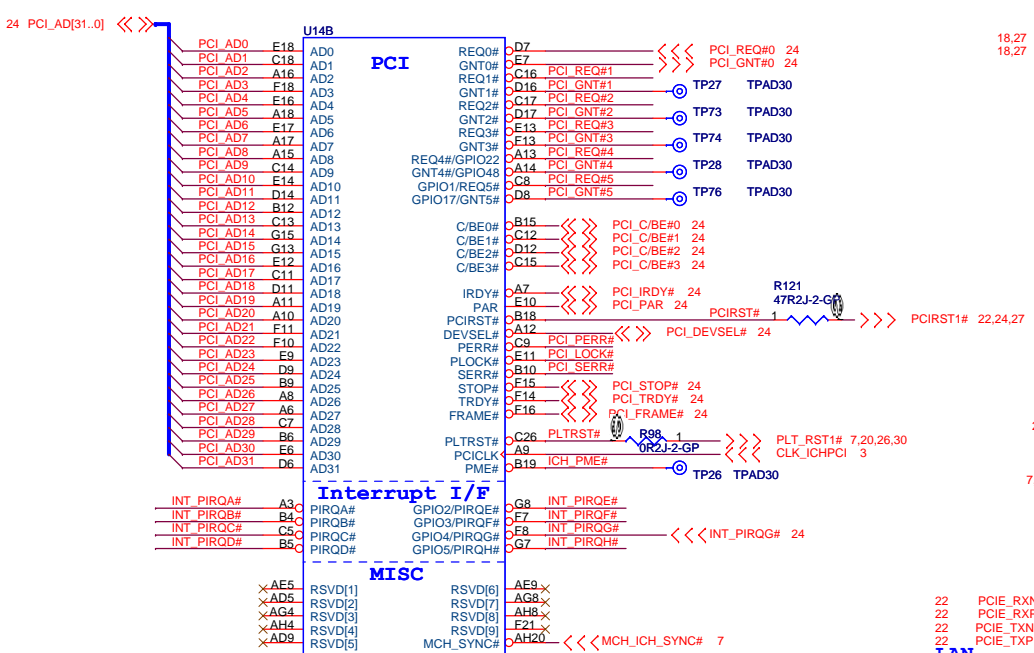
<Core Design>

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Title: **ICH7-M (1 of 4)**

Size: Document Number: **HURON** Rev: **SD**

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Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

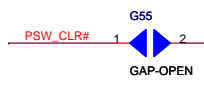
USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1

GAP放在Dimm Door打開可量測處

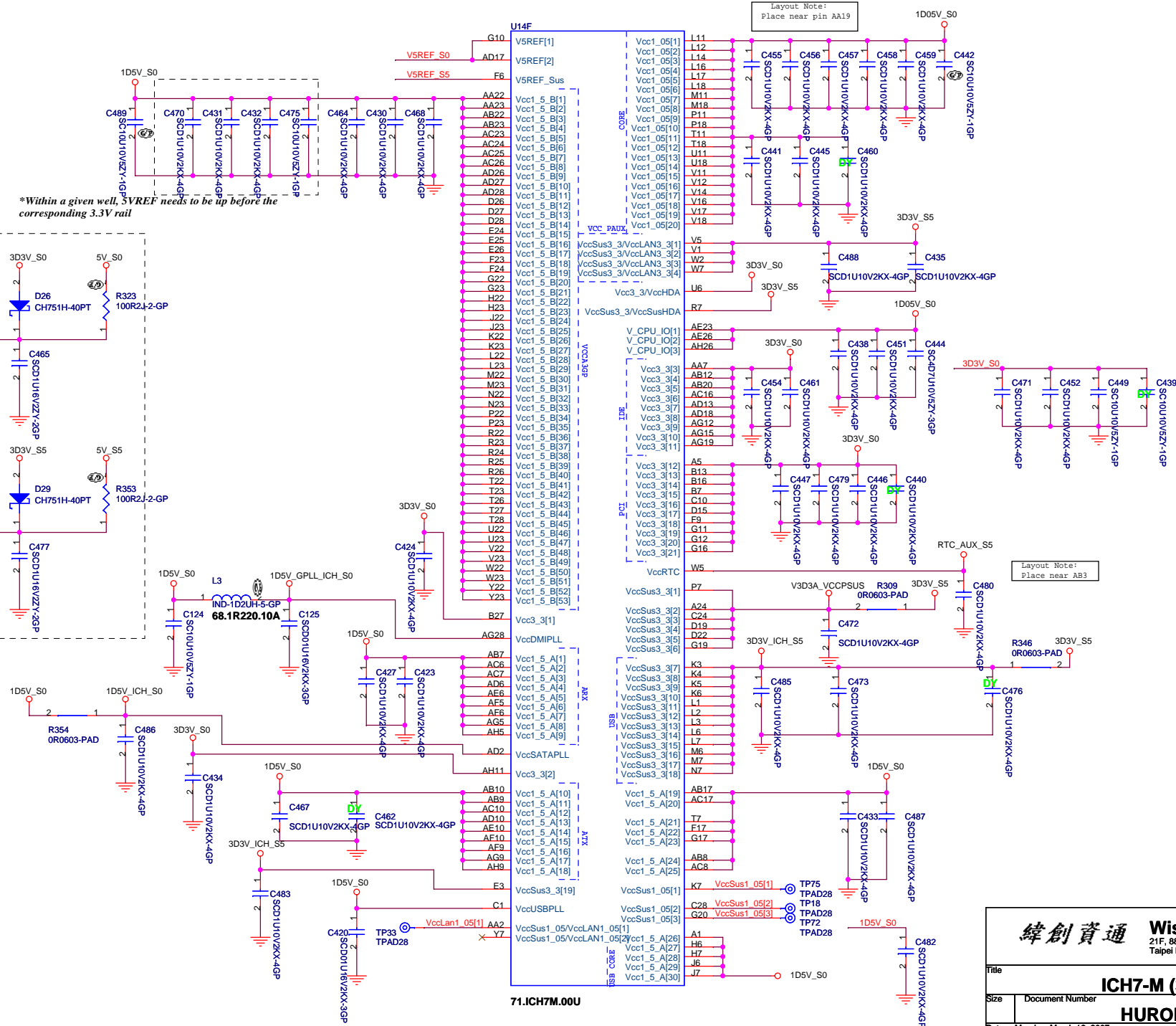
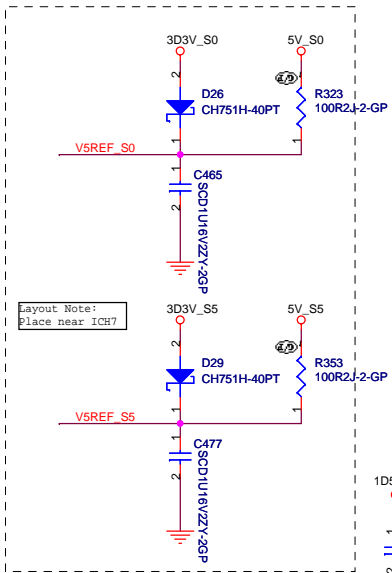
Default: H

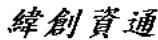
	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

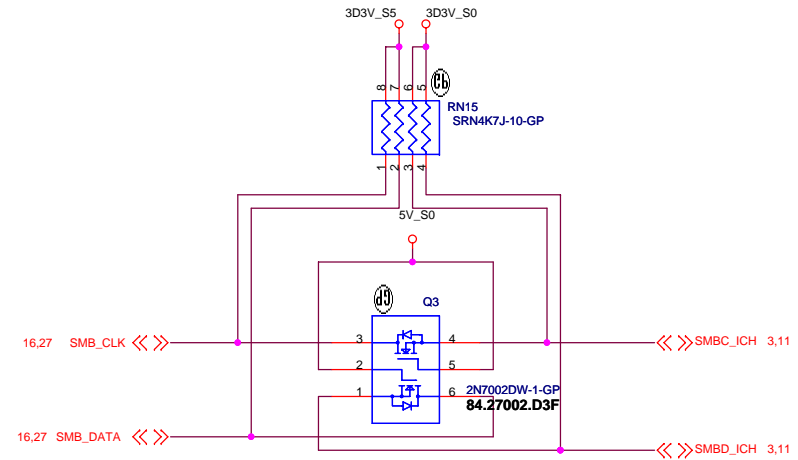
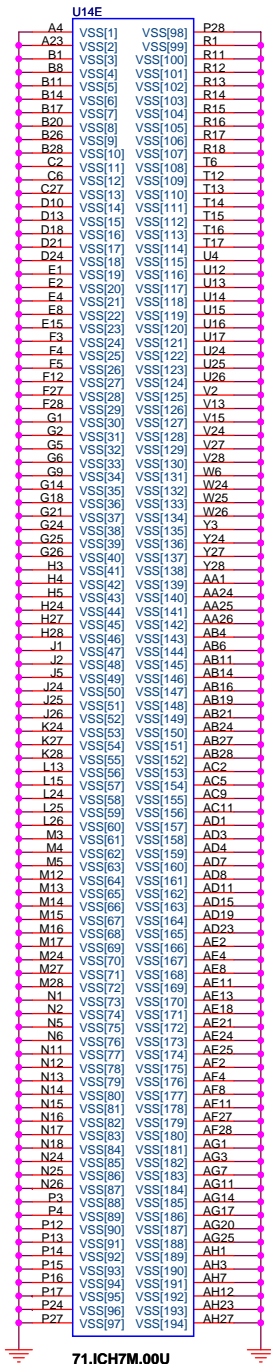


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*Within a given well, SVREF needs to be up before the corresponding 3.3V rail



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ICH7-M (3 of 4)	
File	SD
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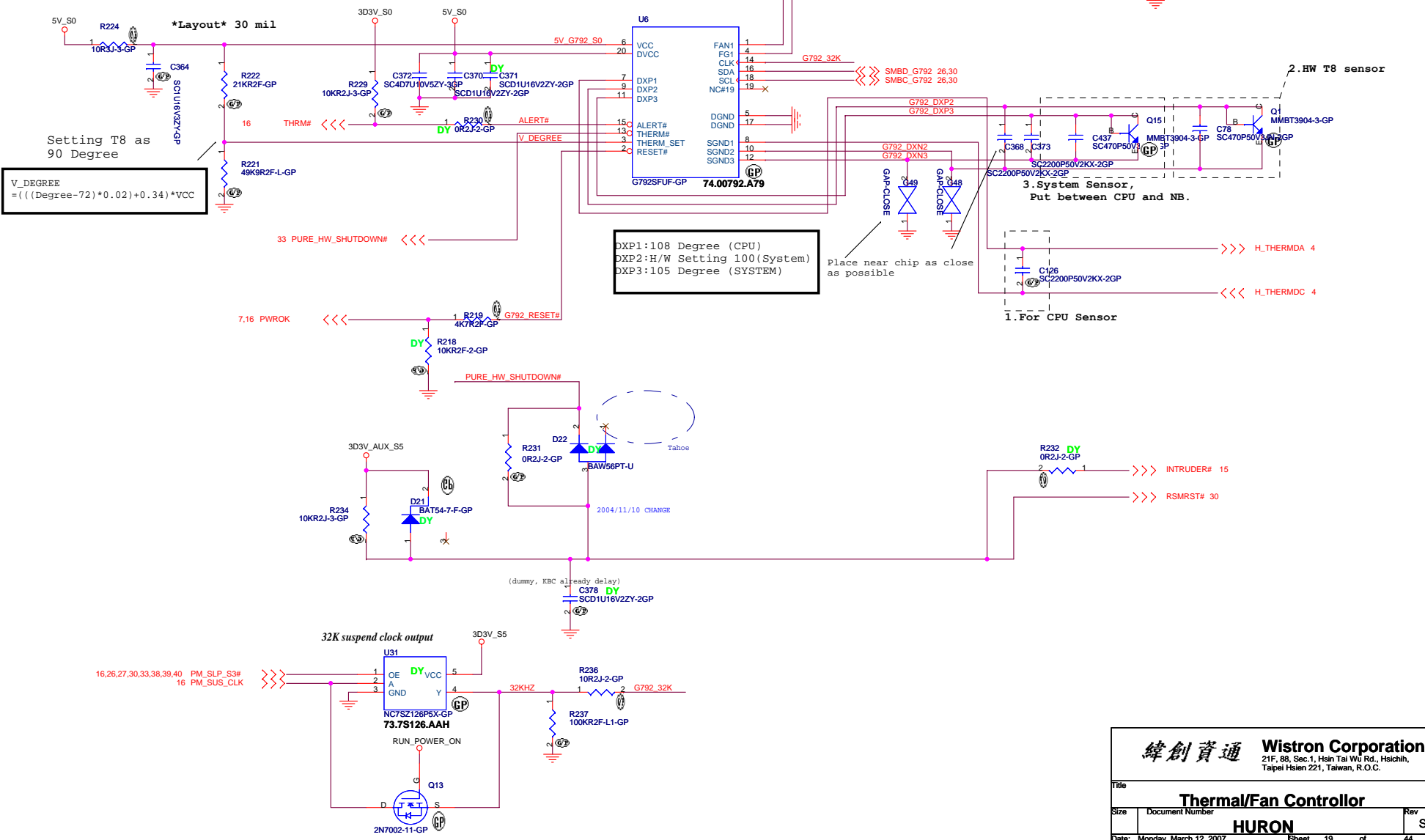


Q14 connect SMLINK and SMBUS in S) for SMBUS 2.0 compliance

SMBUS

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Title: ICH7-M (4 of 4)	
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TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

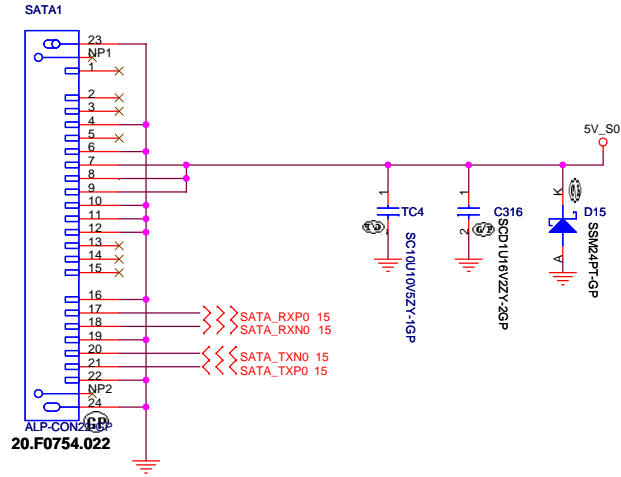


DXP1:108 Degree (CPU)
 DXP2:H/W Setting 100(System)
 DXP3:105 Degree (SYSTEM)

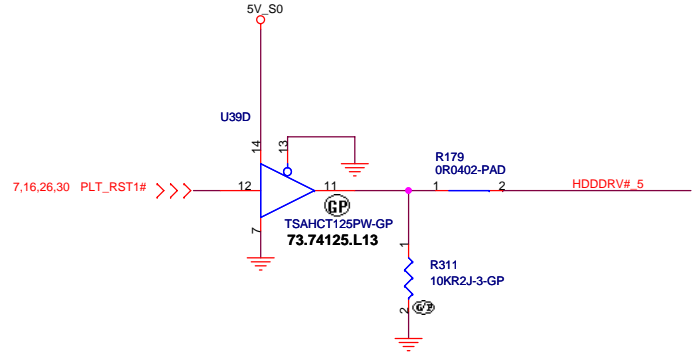
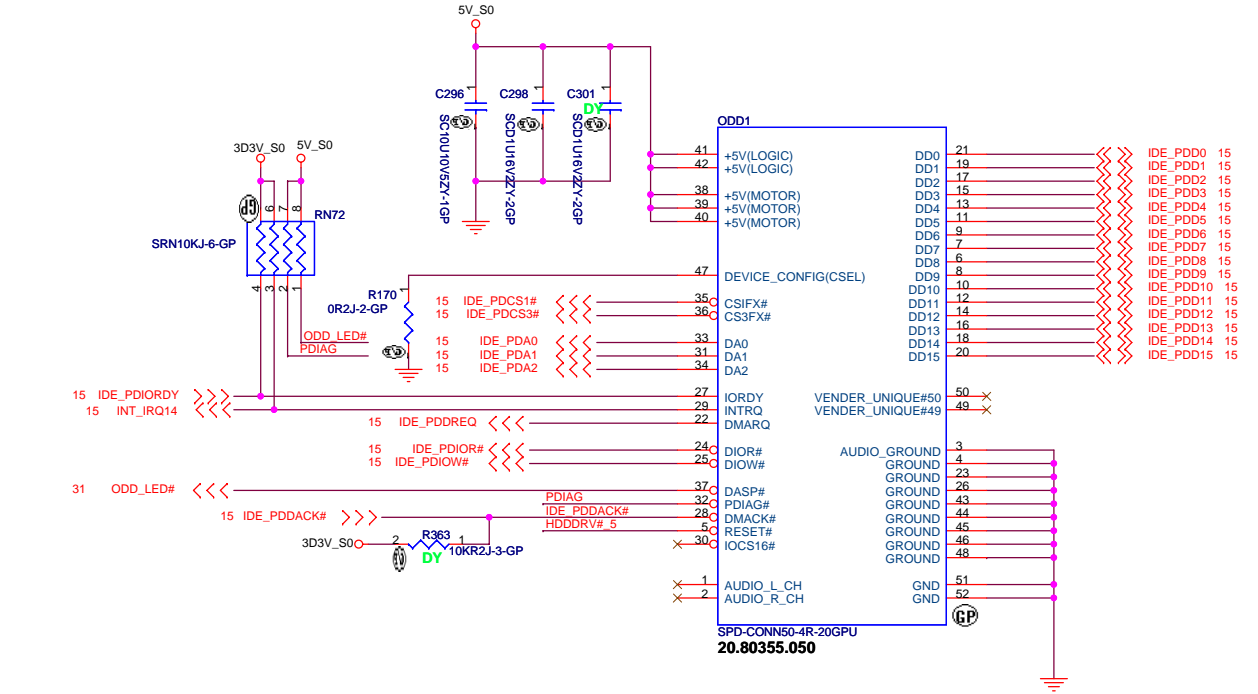
緯創資通 Wistron Corporation
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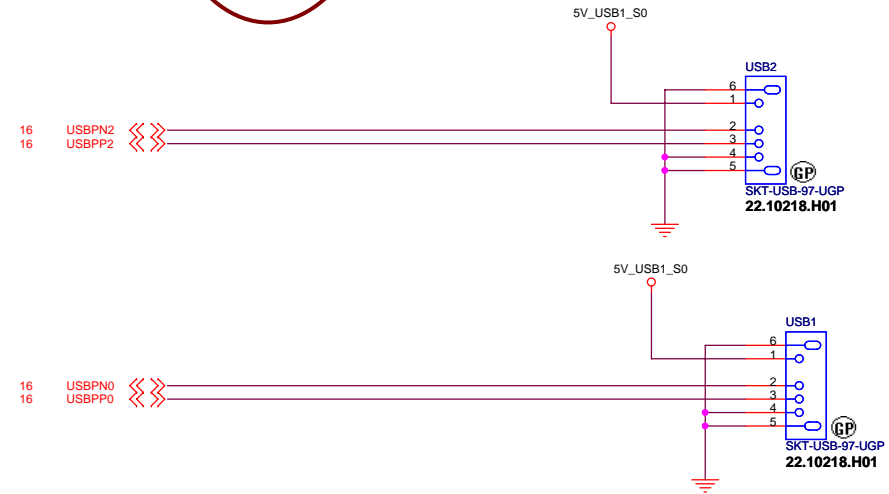
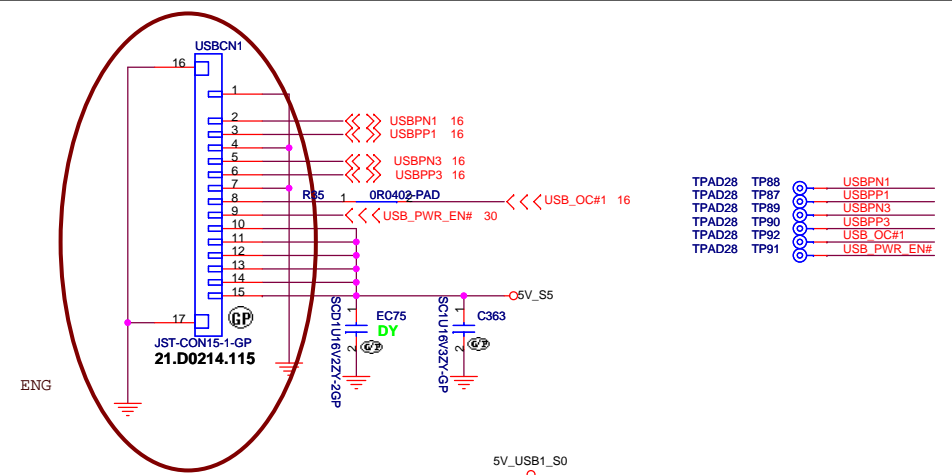
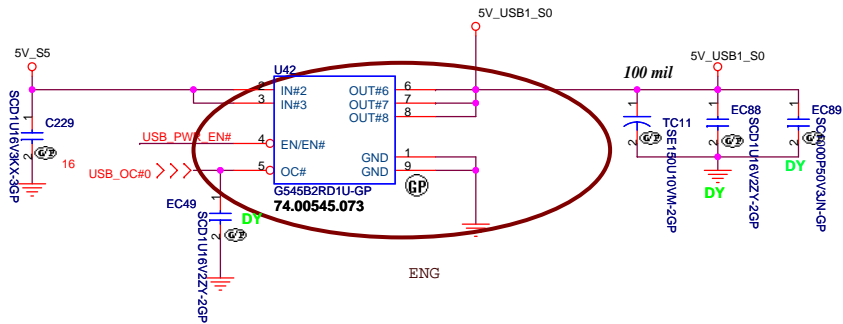
Title		
Thermal/Fan Controller		
Size	Document Number	Rev
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SATA HD Connector

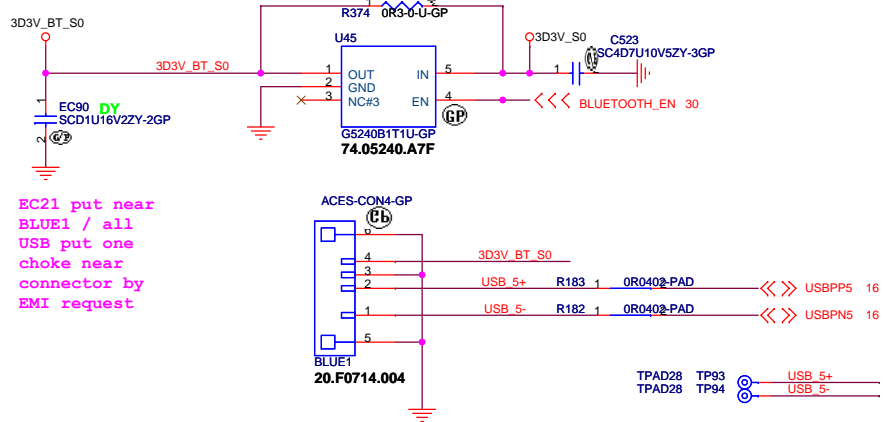


ODD Connector





BLUETOOTH MODULE

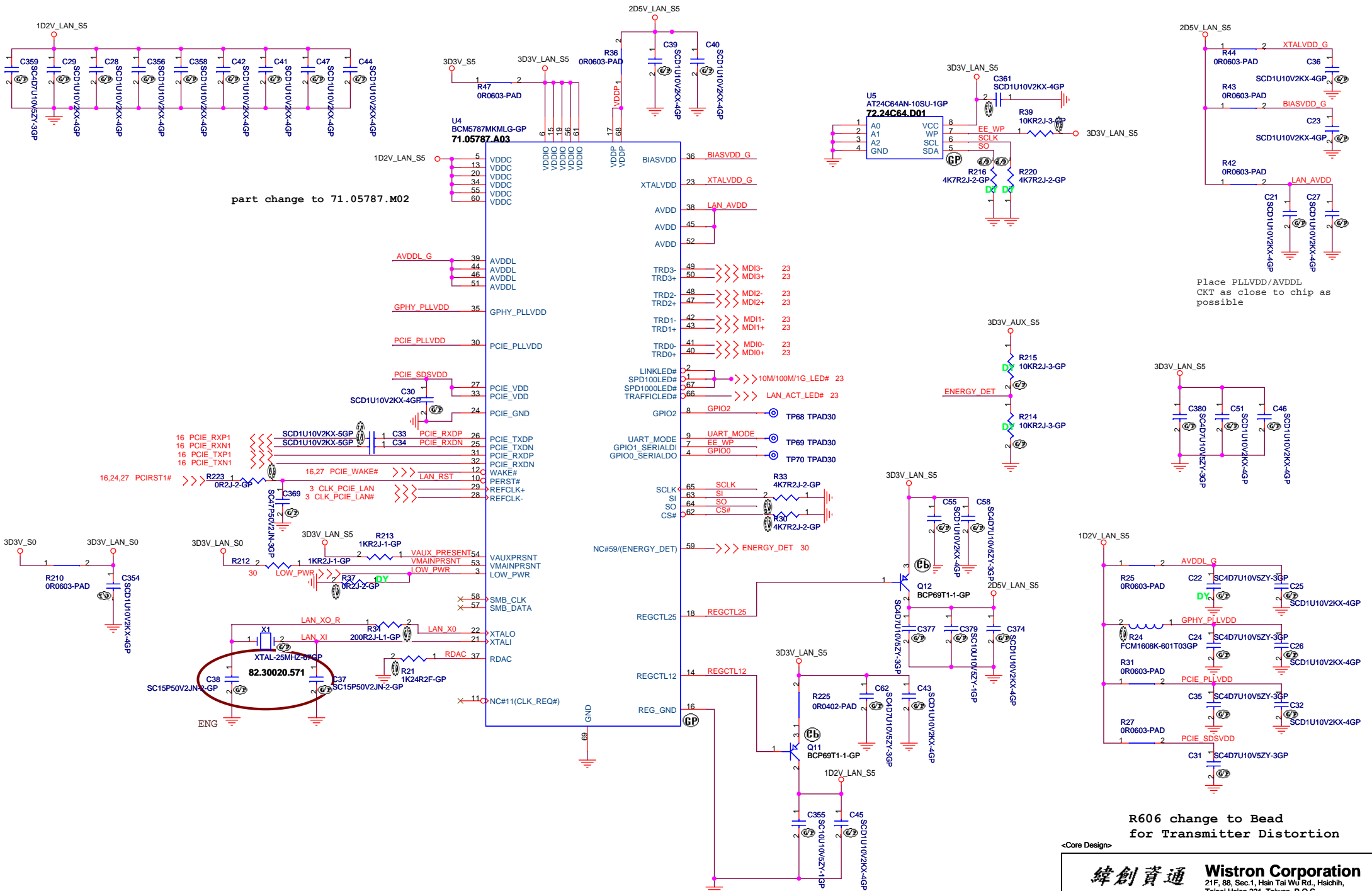


EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

<Core Design>

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Title USB / BLUETOOTH			Rev SD
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part change to 71.05787.M02

Place PLLVDD/AVDDL CKT as close to chip as possible

R606 change to Bead for Transmitter Distortion

<Core Design>

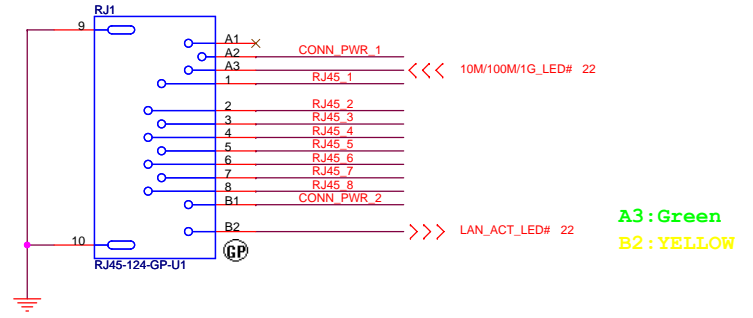
緯創資通 Wistron Corporation
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Title: **LAN BCM5787**

Size A3	Document Number	Rev SD
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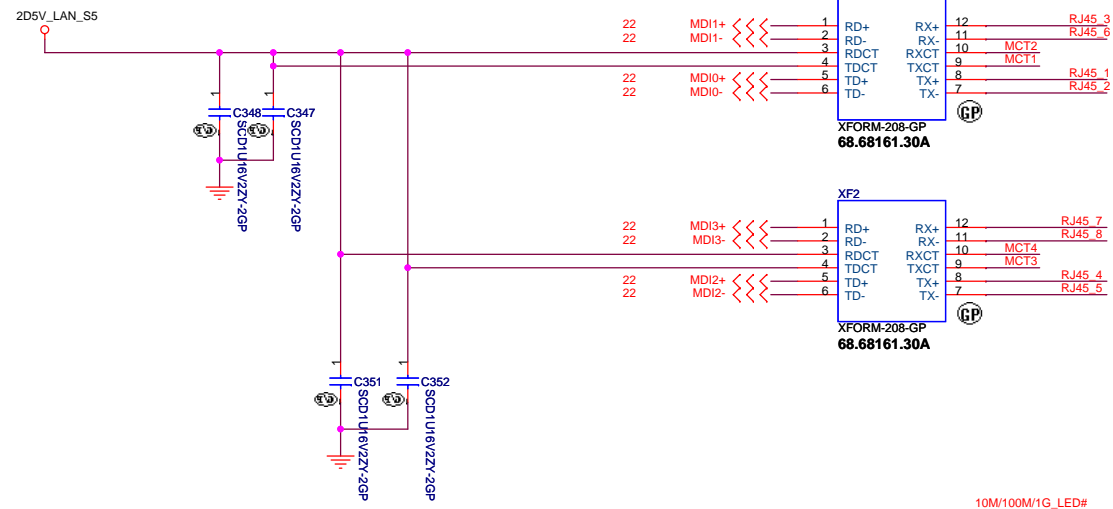
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
 LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

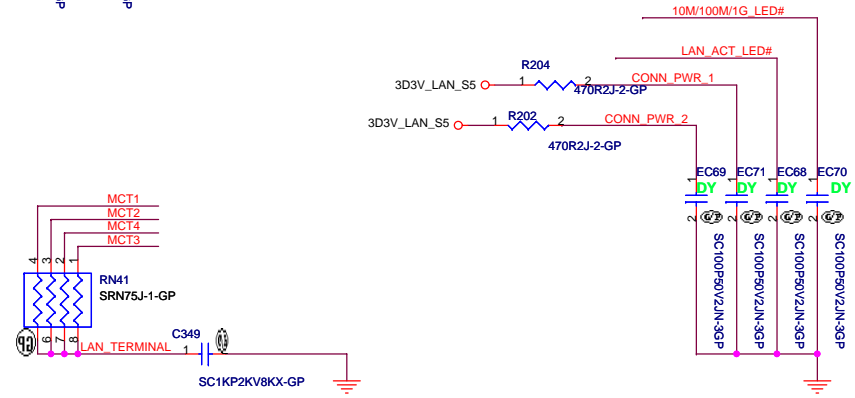


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Core Design>

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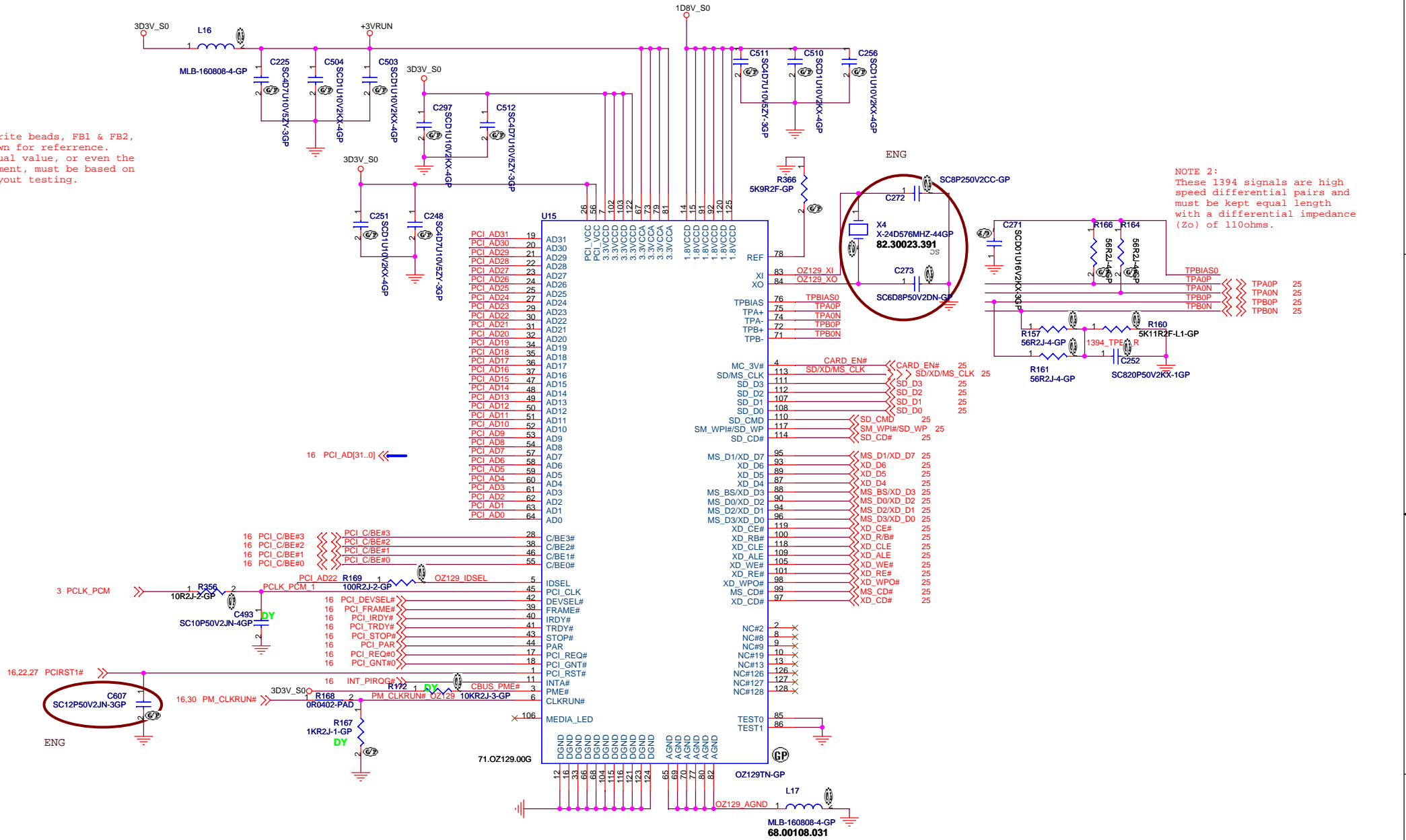
Title: **LAN Connector**

Size A3 | Document Number: **HURON** | Rev: **SD**

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NOTE 1:
The Ferrite beads, FB1 & FB2,
are shown for reference.
The actual value, or even the
requirement, must be based on
post-layout testing.

NOTE 2:
These I394 signals are high
speed differential pairs and
must be kept equal length
with a differential impedance
(Zo) of 110ohms.



IDSEL: AD22
INTA-->: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

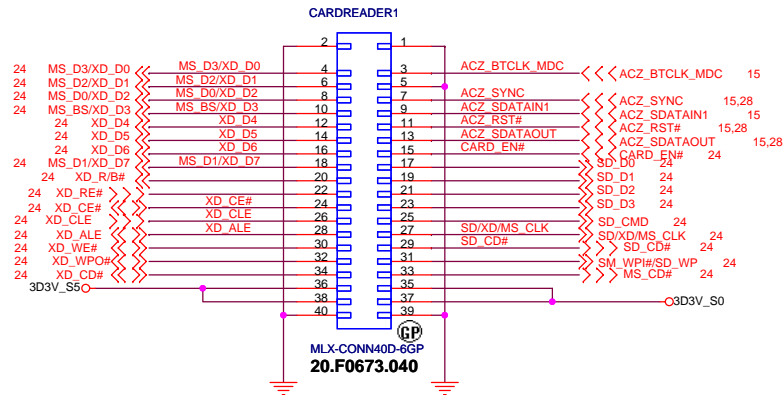
<Core Design>

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Title: **OZ129T**

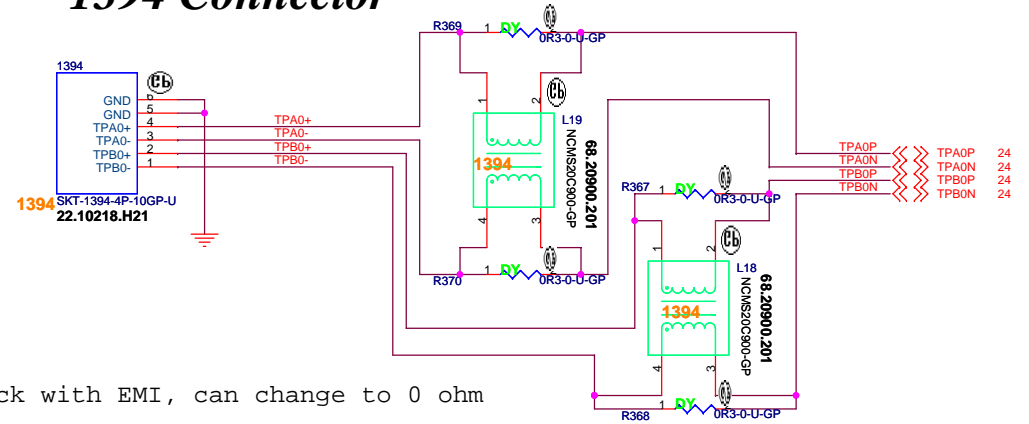
Size: Document Number: **HURON** Rev: **SD**

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CONN on Bottom side

1394 Connector



check with EMI, can change to 0 ohm

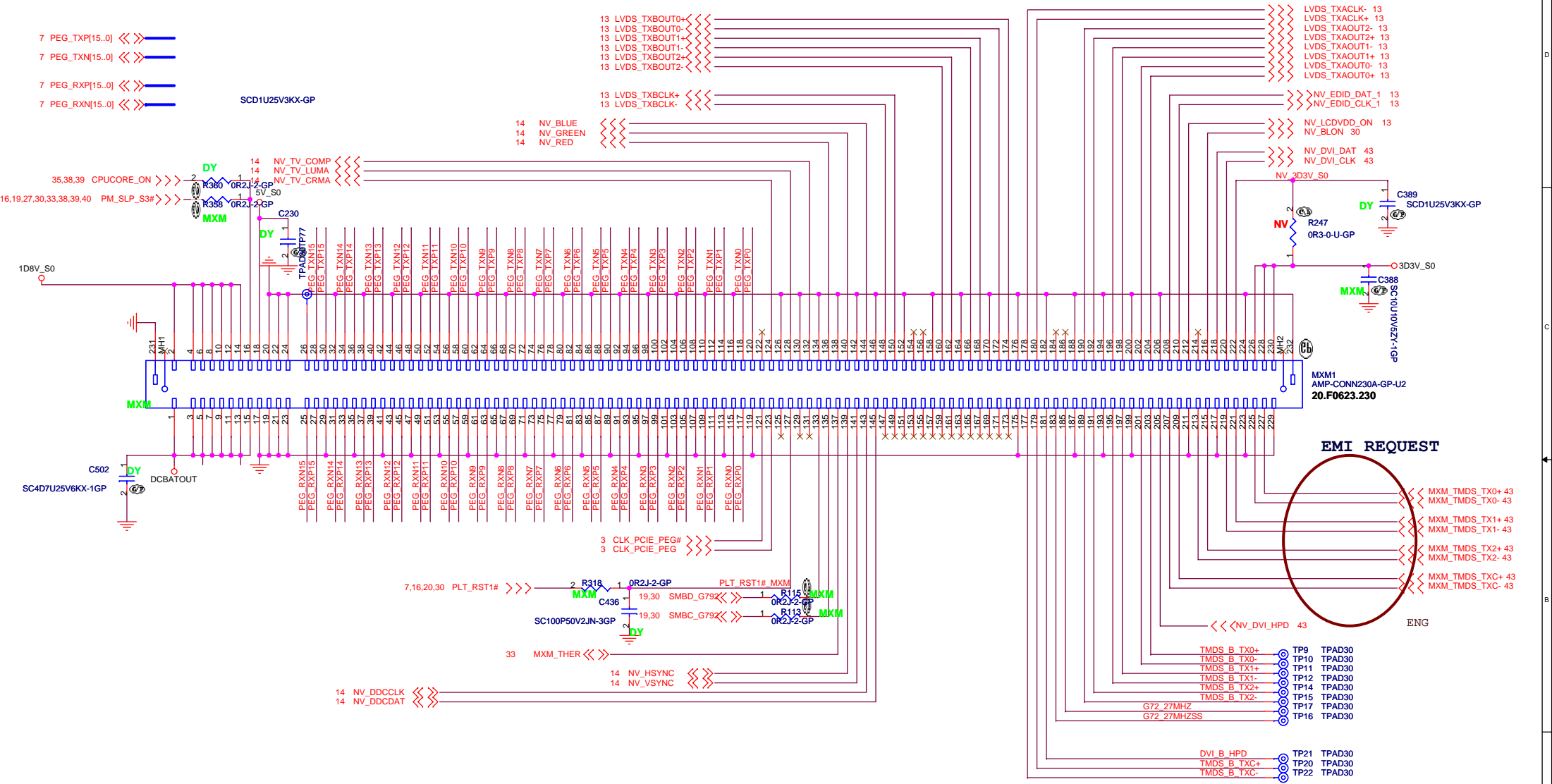
<Core Design>

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Title 1394 / CARD READER BD		
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NV SMBus
 A (pin143&145) : VGA (CRT) / DOCK
 B (pin218&220) : DVI
 C (pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



EMI REQUEST

ENG

<Core Design>

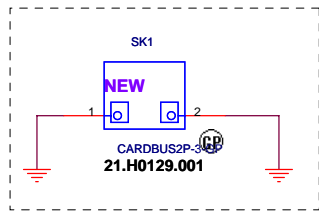
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

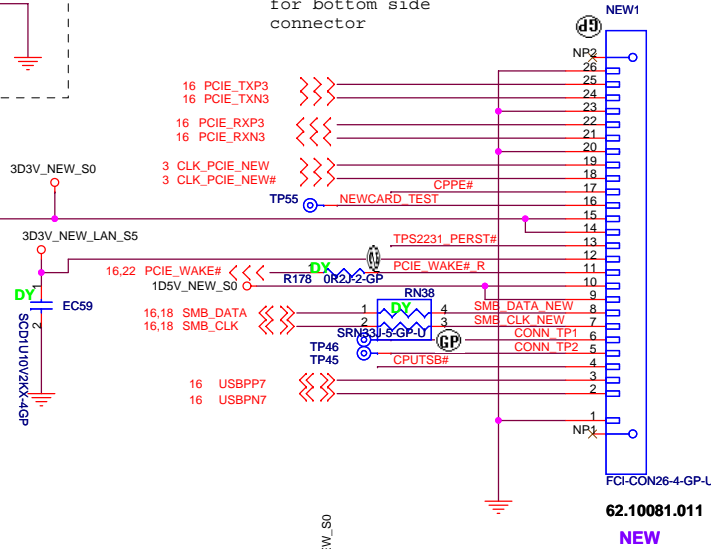
Size: A3 Document Number: **HURON** Rev: SD

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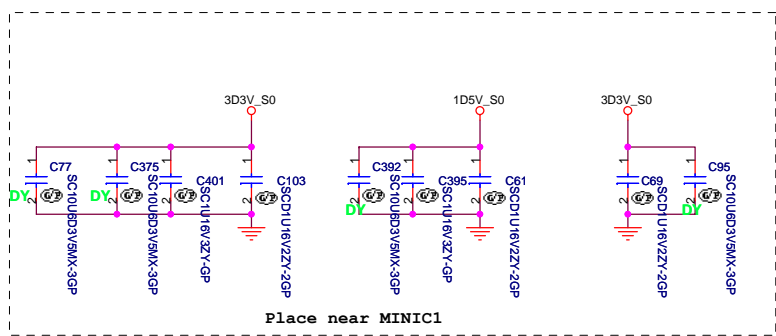
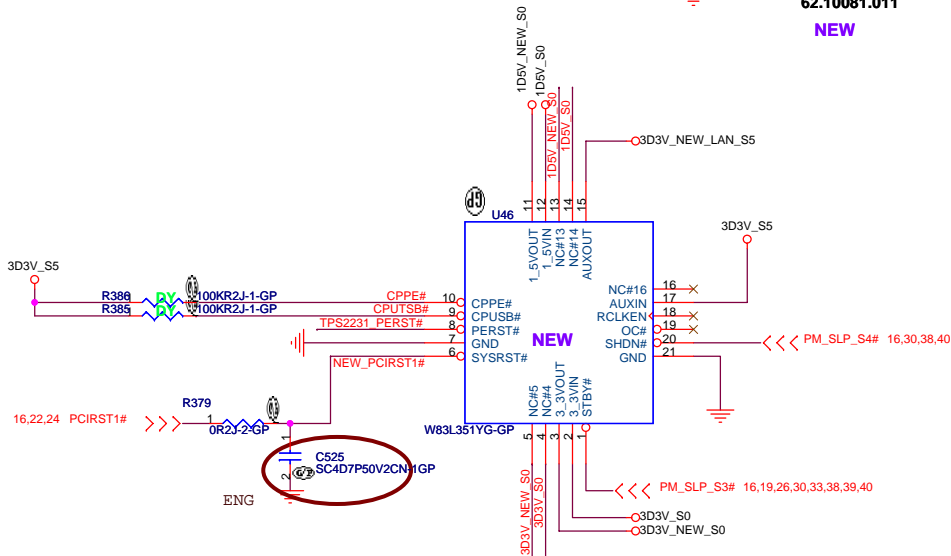
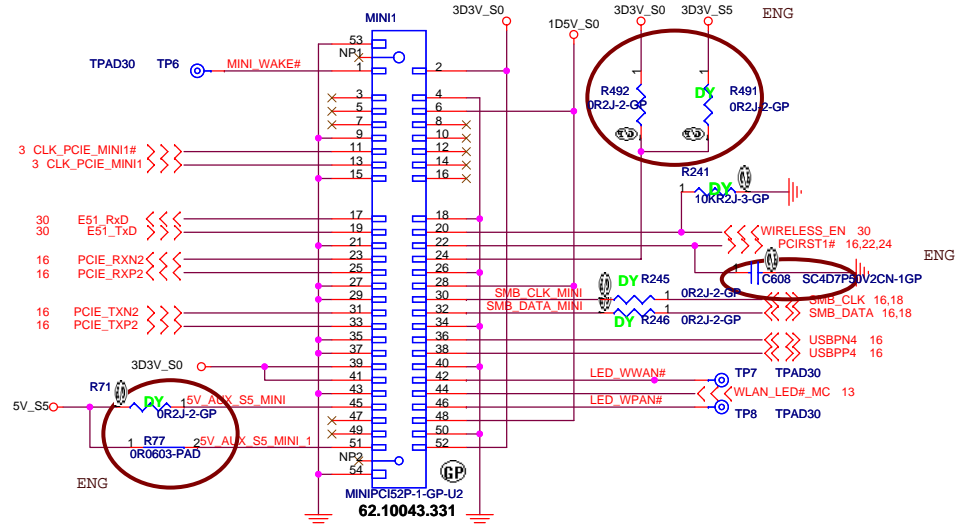
NEWCARD Connector



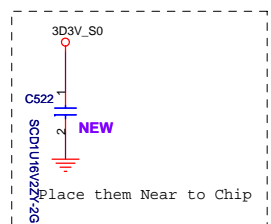
Reserve the symbol for bottom side connector



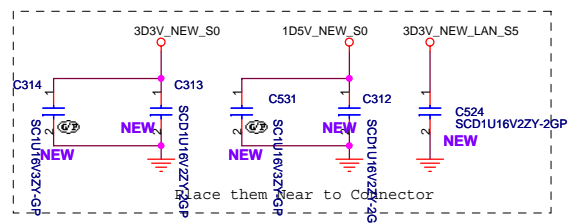
Mini Card Connector



Place near MINIC1



Place them Near to Chip



Place them Near to Connector

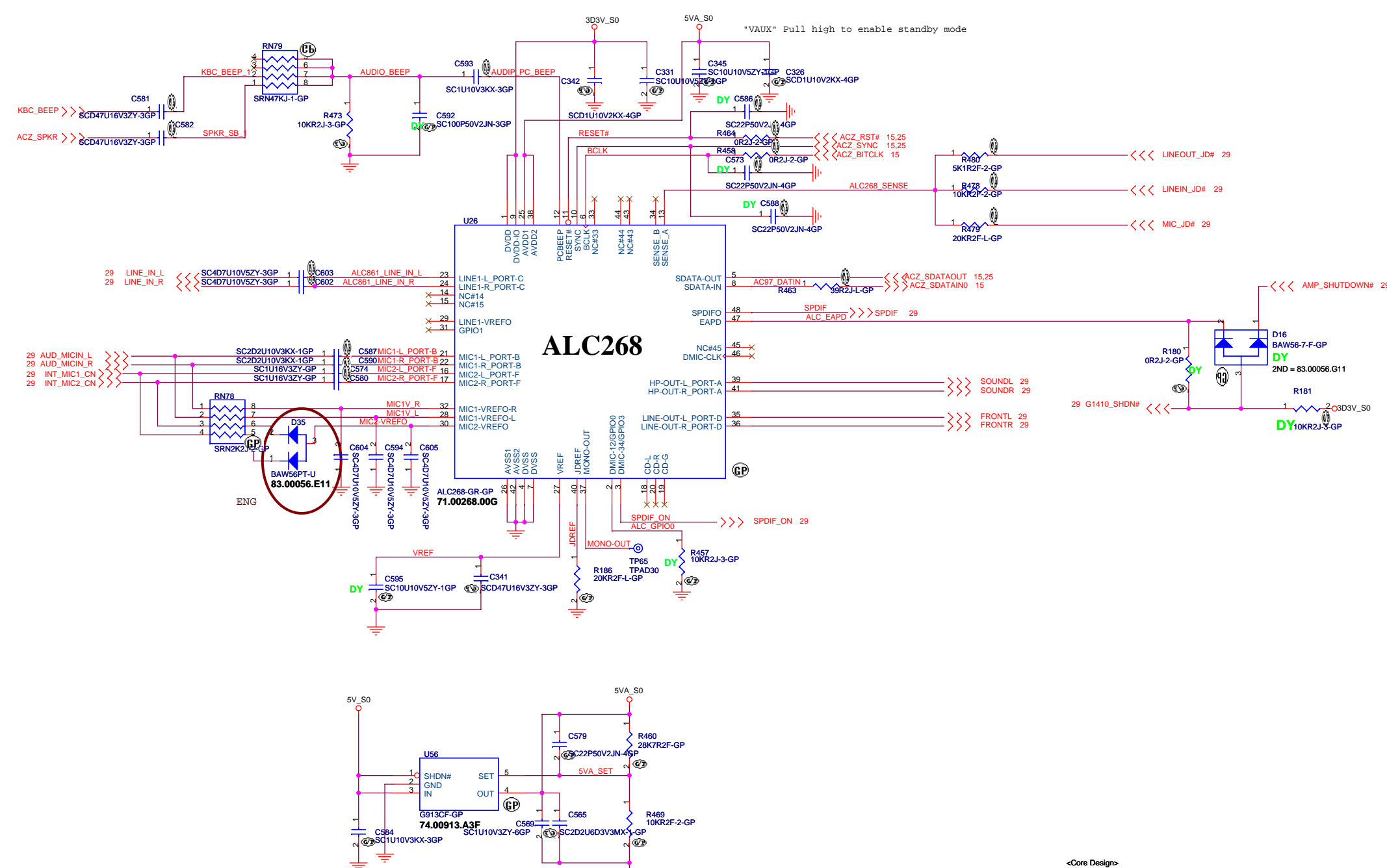
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緯創資通 Wistron Corporation
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Title: **MINI CARD / NEW CARD**

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2nd: 74.09198.A7F
(RT9198-4GPBG)

<Core Design>

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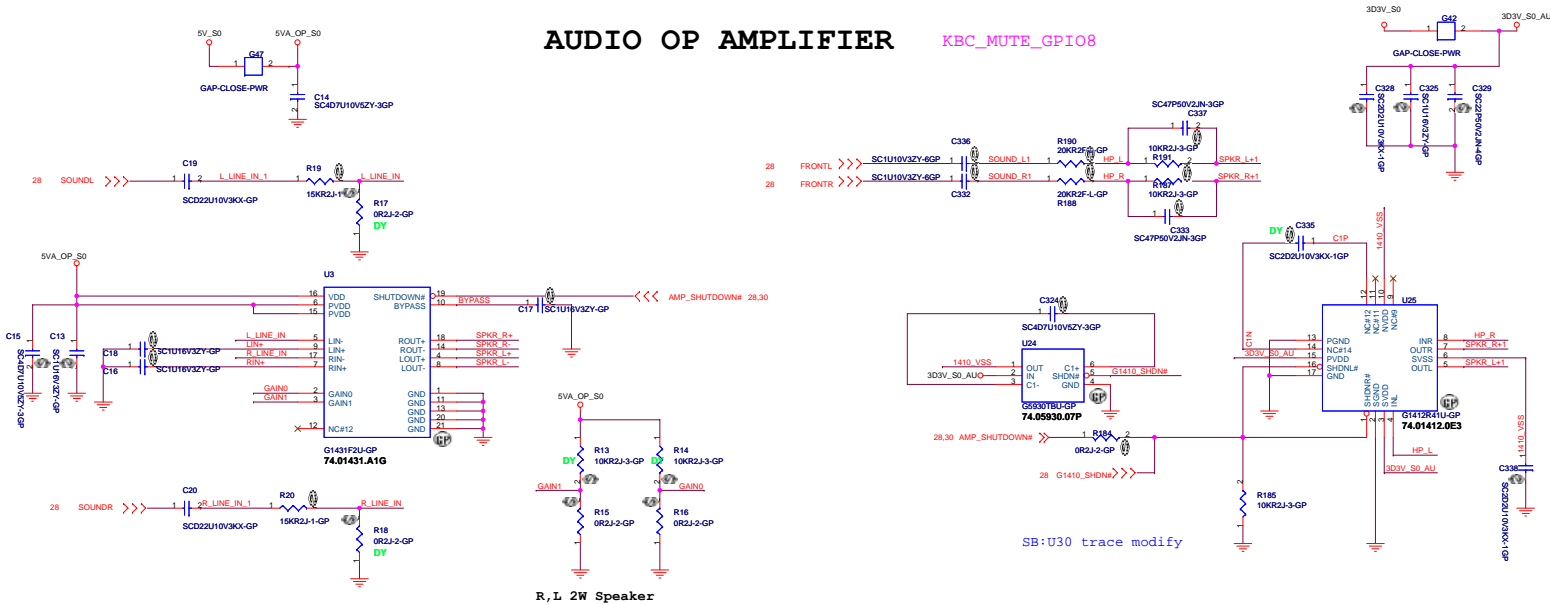
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Size	Document Number	Rev
	HURON	SD

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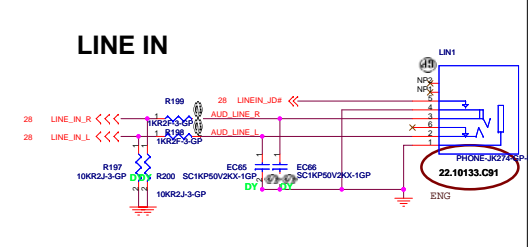
AUDIO OP AMPLIFIER

KBC_MUTE_GPIO8

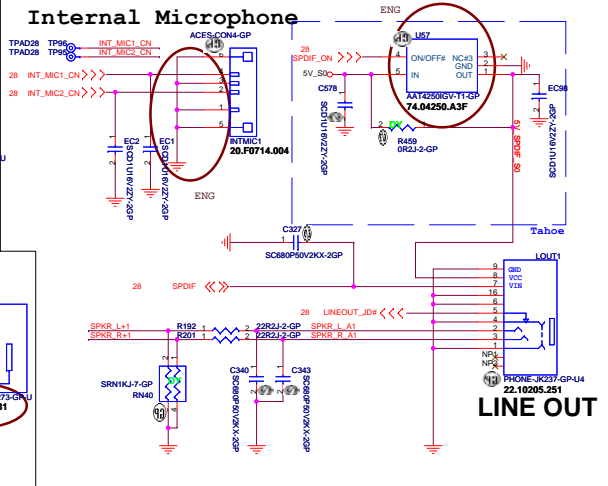


R, L 2W Speaker

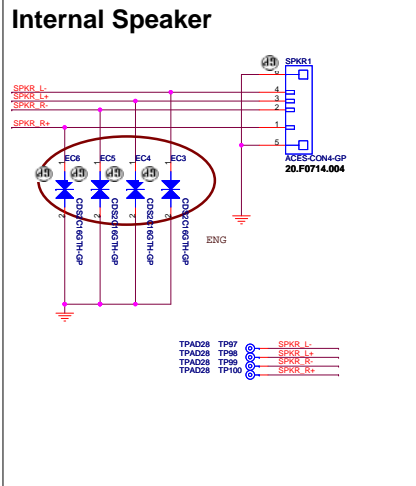
LINE IN



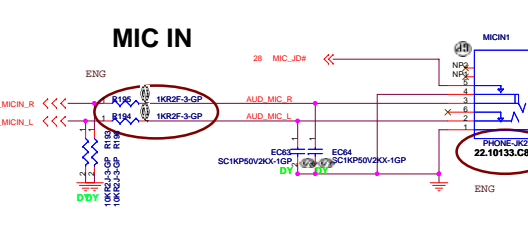
Internal Microphone



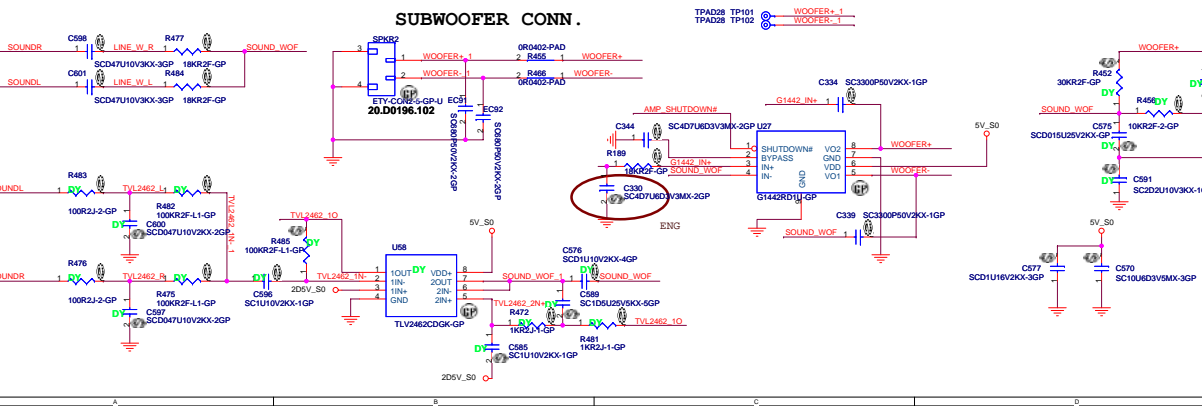
Internal Speaker



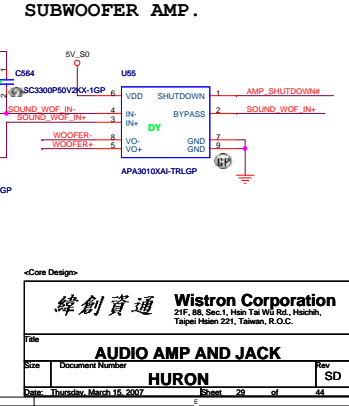
MIC IN



SUBWOOFER CONN.



SUBWOOFER AMP.



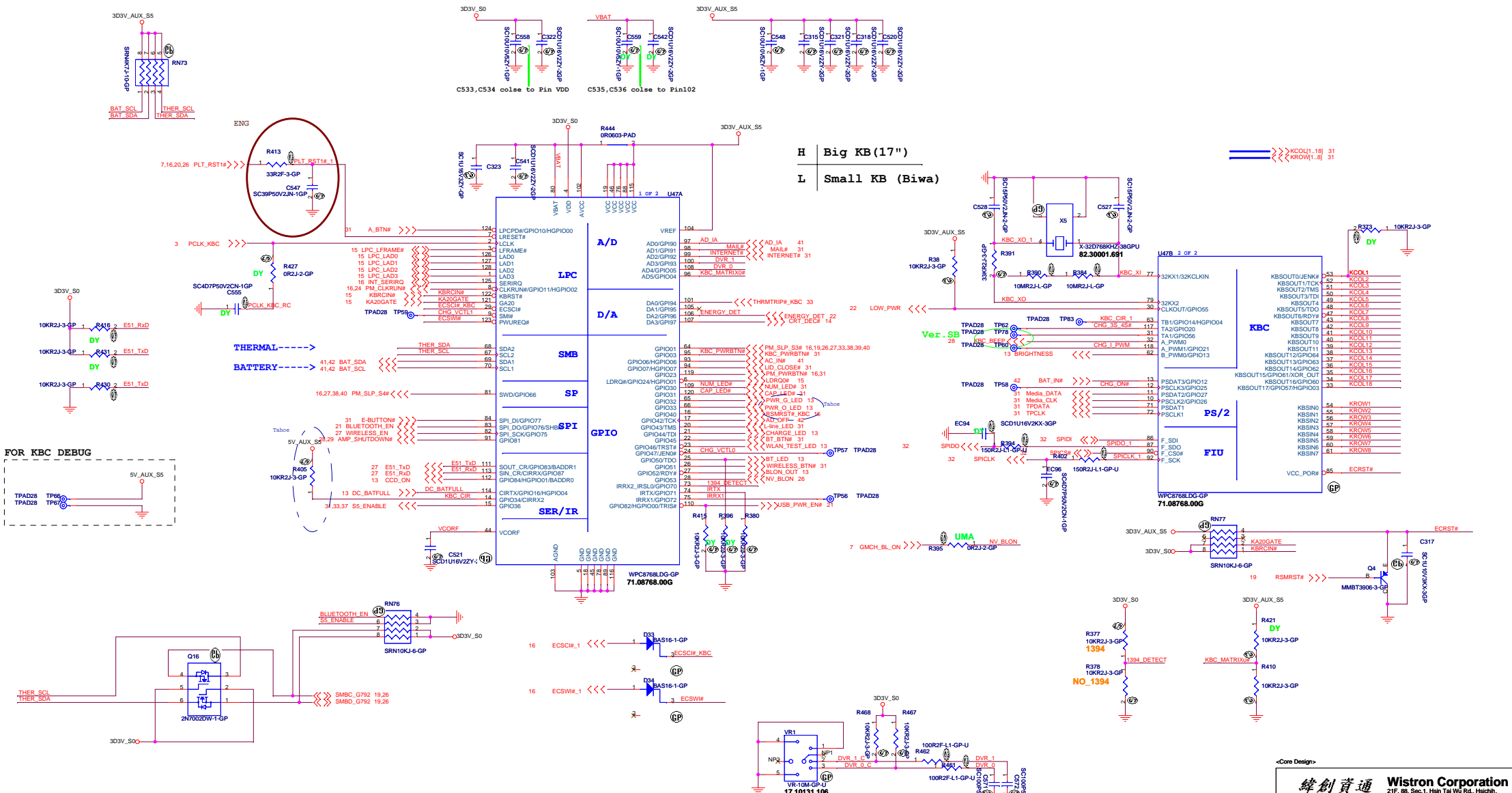
Wistron Corporation
21F, 86, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

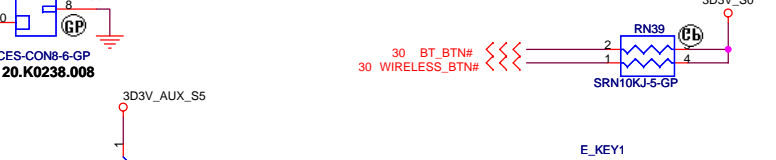
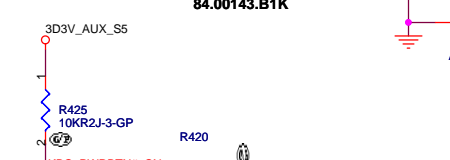
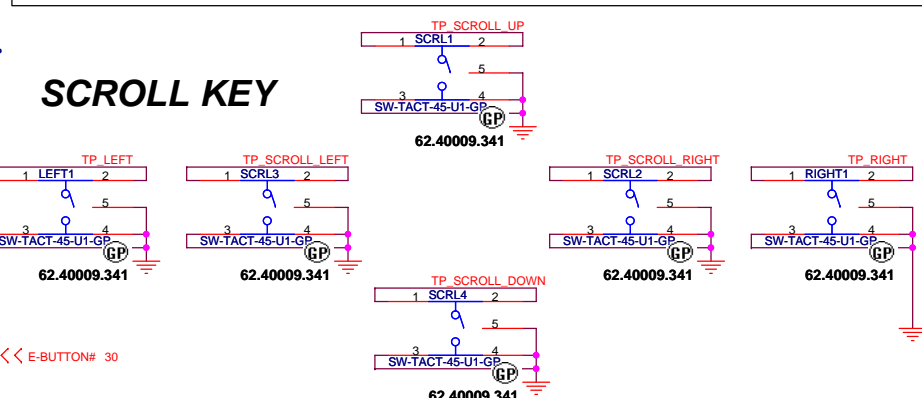
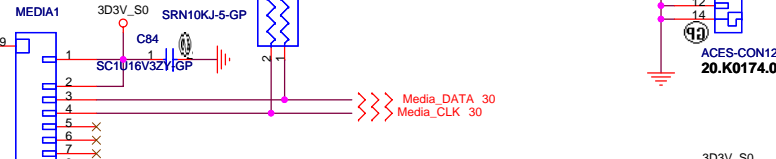
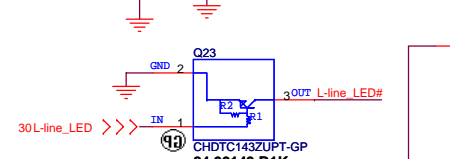
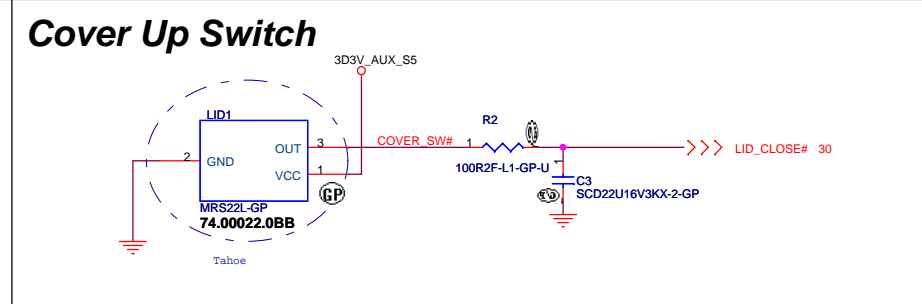
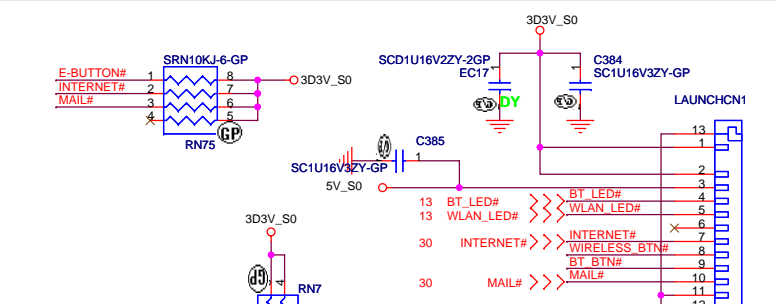
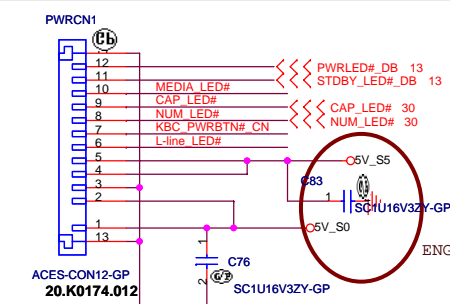
AUDIO AMP AND JACK

HURON

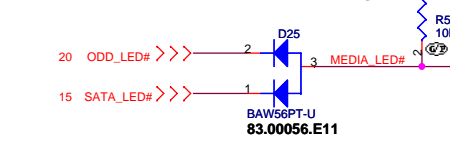
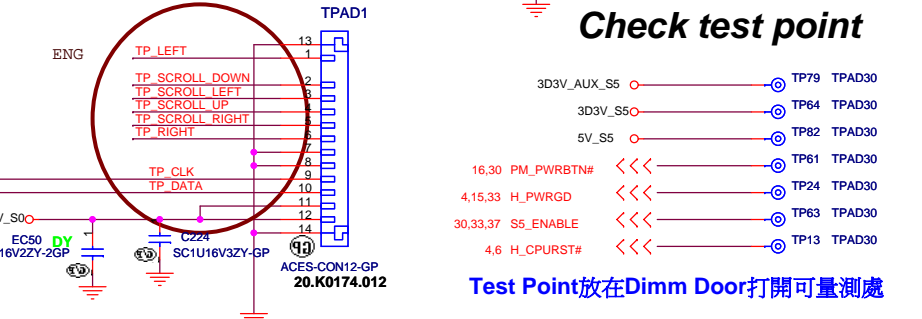
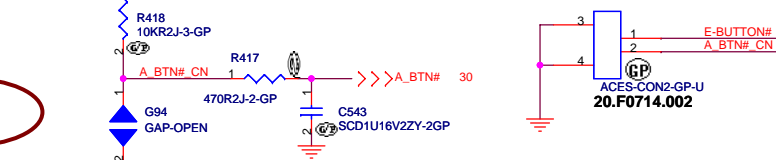
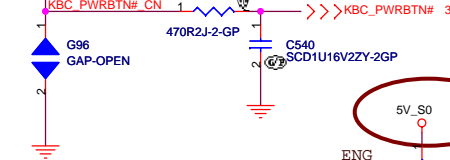
Date: Tuesday, March 15, 2007

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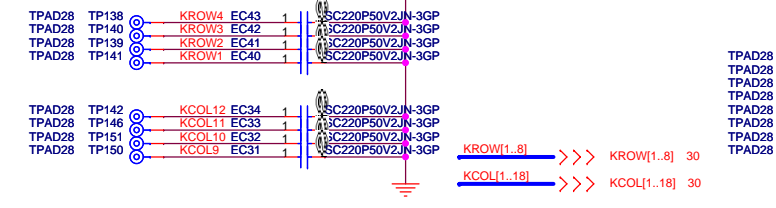
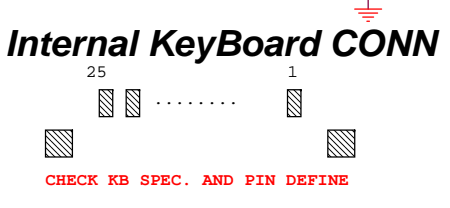
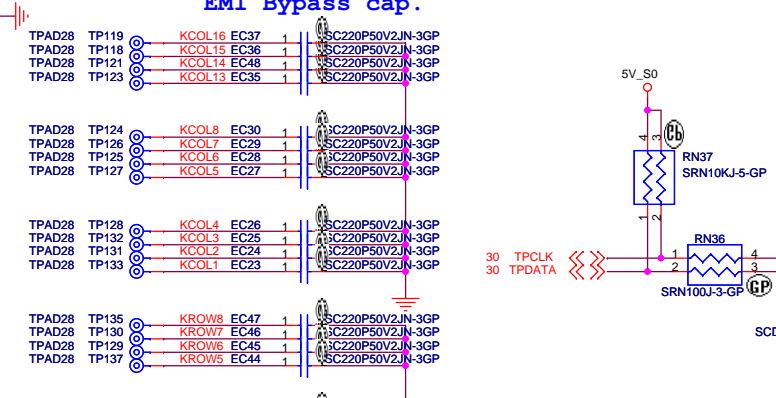
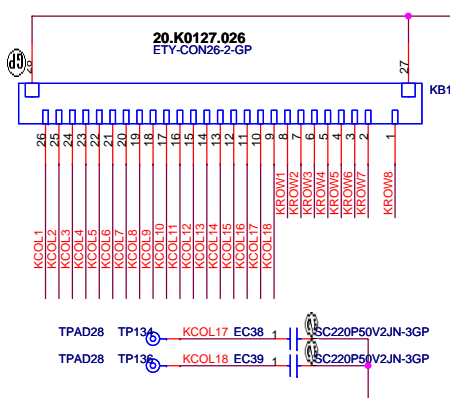




TPAD28	TP103	MAIL#	SC100P50V2JN-3GP	EC86
TPAD28	TP105	INTERNET#	SC100P50V2JN-3GP	EC85
TPAD28	TP104	WLAN_LED#	SC100P50V2JN-3GP	EC82
TPAD28	TP106	BT_LED#	SC100P50V2JN-3GP	EC83
TPAD28	TP108	MEDIA_LED#	SC100P50V2JN-3GP	EC18
TPAD28	TP110	STDBY_LED# DB	SC100P50V2JN-3GP	EC77
TPAD28	TP109	A_BTN# CN	SC100P50V2JN-3GP	EC8
TPAD28	TP111	E-BUTTON#	SC100P50V2JN-3GP	EC7
TPAD28	TP113	L-line_LED#	SC100P50V2JN-3GP	EC81
TPAD28	TP112	KBC_PWRBTN# CN	SC100P50V2JN-3GP	EC78
TPAD28	TP115	NUM_LED#	SC100P50V2JN-3GP	EC79
TPAD28	TP114	CAP_LED#	SC100P50V2JN-3GP	EC80
TPAD28	TP116	Media_DATA	SC100P50V2JN-3GP	EC100
TPAD28	TP117	Media_CLK	SC100P50V2JN-3GP	EC99
TPAD28	TP120	WIRELESS_BTN#	SC1U16V2ZY-2GP	EC83
TPAD28	TP122	BT_BTN#	SC1U16V2ZY-2GP	EC95



TPAD28	TP143	TP_DATA	EC51	SC47P50V2JN-3GP
TPAD28	TP147	TP_CLK	EC52	SC47P50V2JN-3GP
TPAD28	TP144	TP_RIGHT	EC56	SC220P50V2JN-3GP
TPAD28	TP145	TP_SCROLL_RIGHT	EC53	SC220P50V2JN-3GP
TPAD28	TP149	TP_SCROLL_UP	EC57	SC220P50V2JN-3GP
TPAD28	TP148	TP_SCROLL_LEFT	EC54	SC220P50V2JN-3GP
TPAD28	TP153	TP_SCROLL_DOWN	EC55	SC220P50V2JN-3GP
TPAD28	TP152	TP_LEFT	EC58	SC220P50V2JN-3GP



Check test point

30V_AUX_S5 ○ TP79 TPAD30

30V_S5 ○ TP64 TPAD30

5V_S5 ○ TP82 TPAD30

16.30 PM_PWRBTN# <<< TP61 TPAD30

4.15.33 H_PWRGD <<< TP24 TPAD30

30.33.37 S5_ENABLE <<< TP63 TPAD30

4.6 H_CPURST# <<< TP13 TPAD30

Test Point放在Dimm Door打開可量測處

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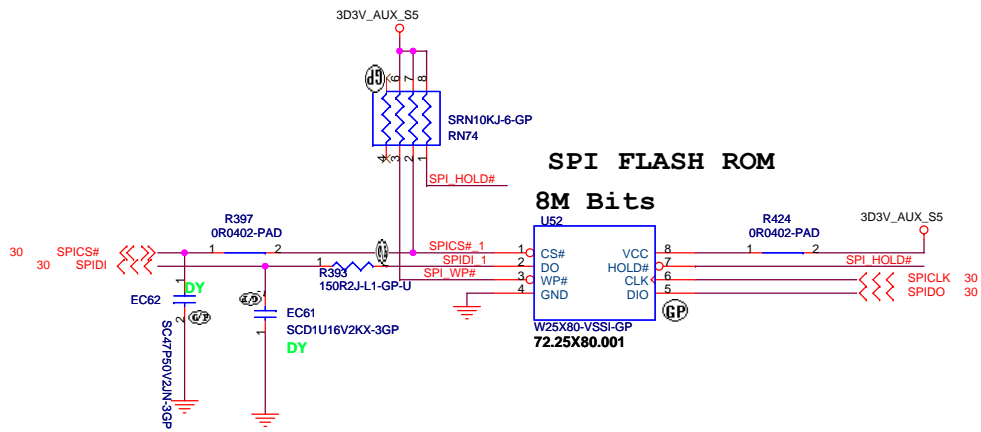
Buttons / KB / TOUCHPAD

HURON

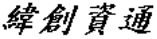
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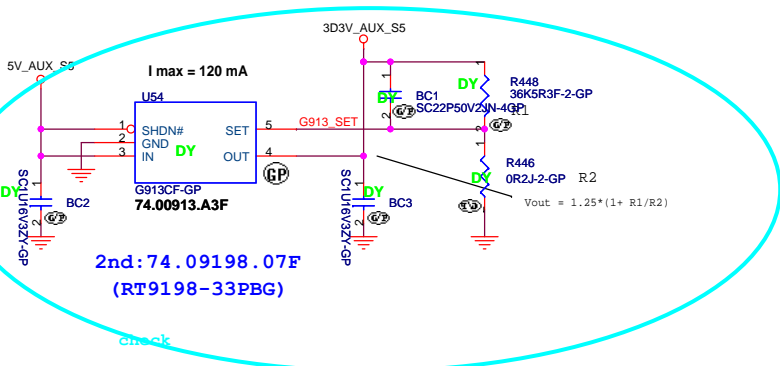
Date: Wednesday, March 14, 2007 Sheet 31 of 44



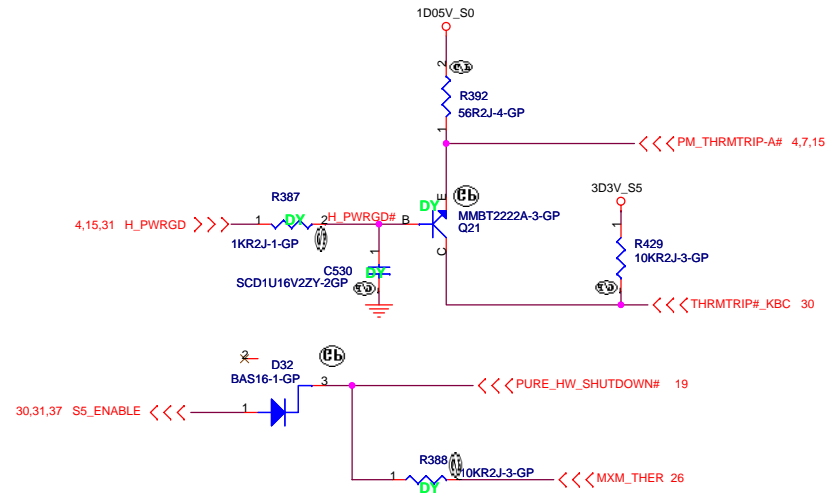
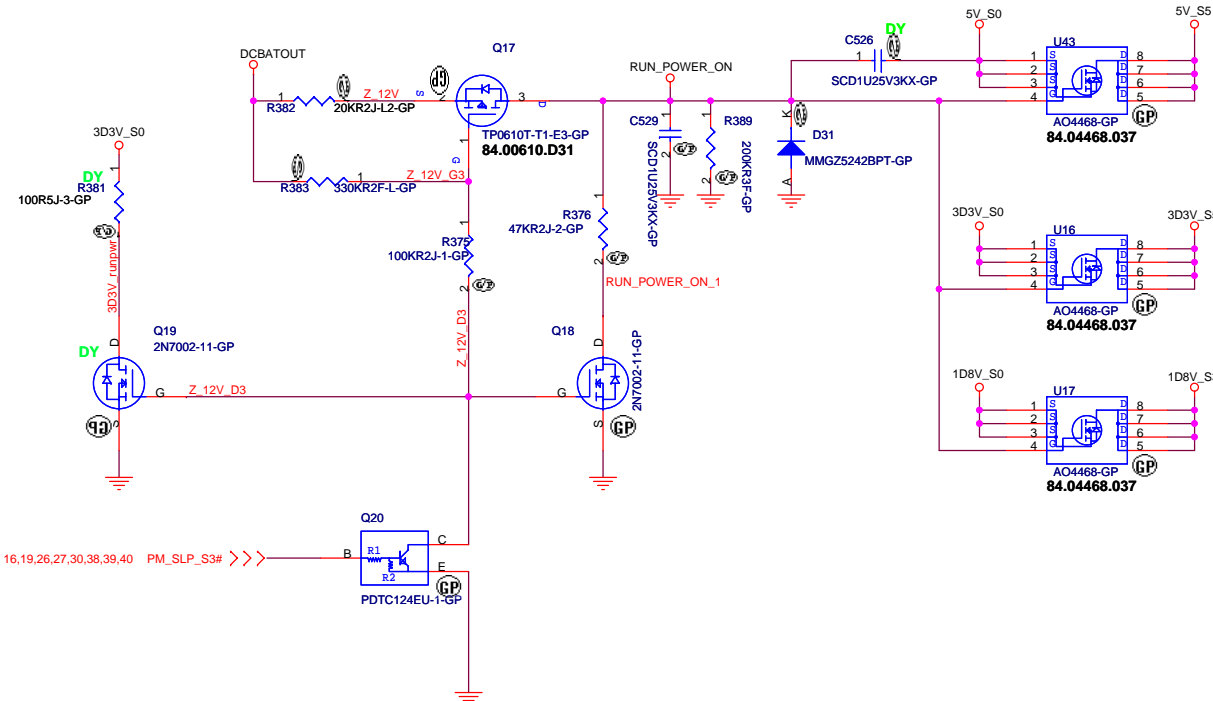
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Rev SD
BIOS		
Size A3	Document Number HURON	Rev SD
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Aux Power 3D3V_AUX_S5



Run Power

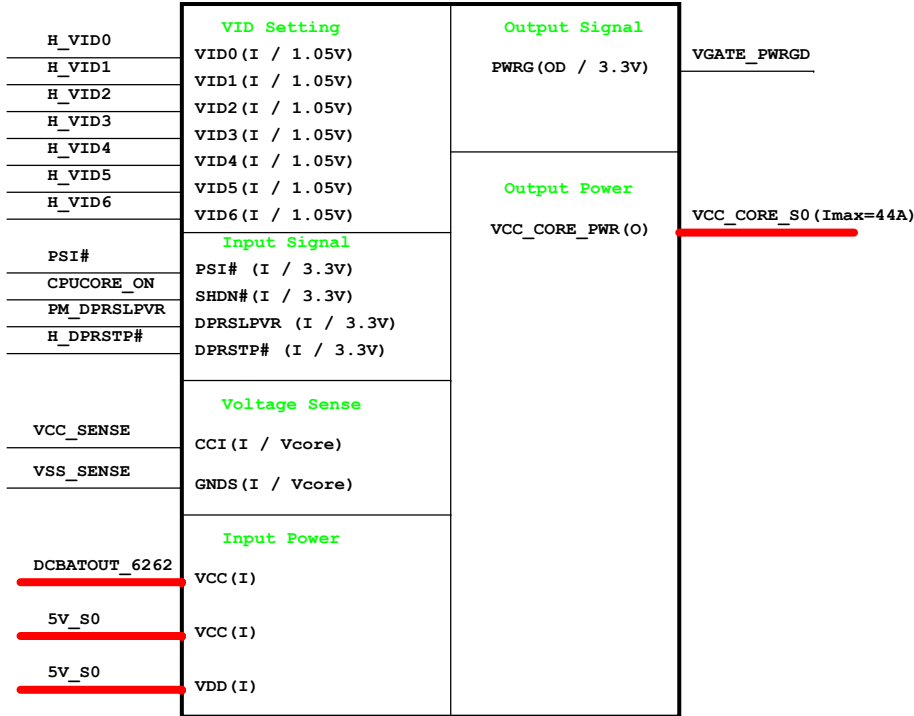


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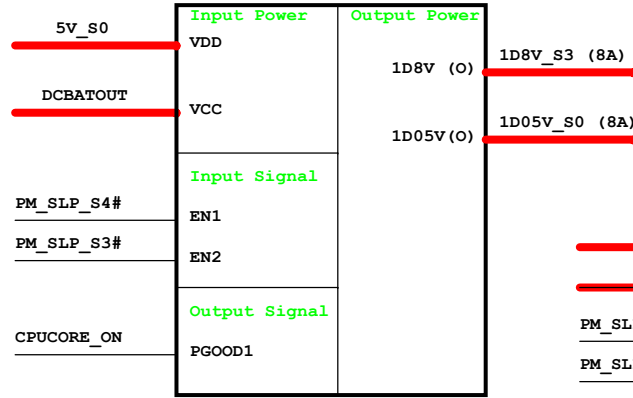
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title			RUN POWER
Size	Document Number	Rev	
			HURON
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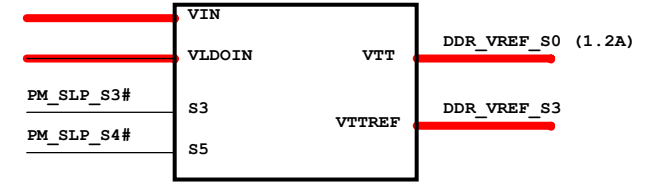
CPU_CORE
ISL6262



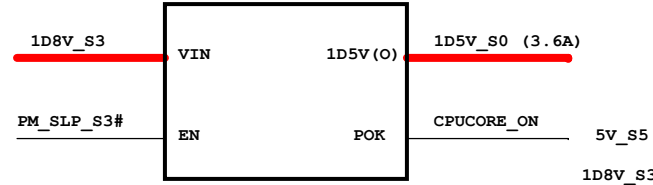
TPS51124
1D8V_S3 / 1D05V_S0



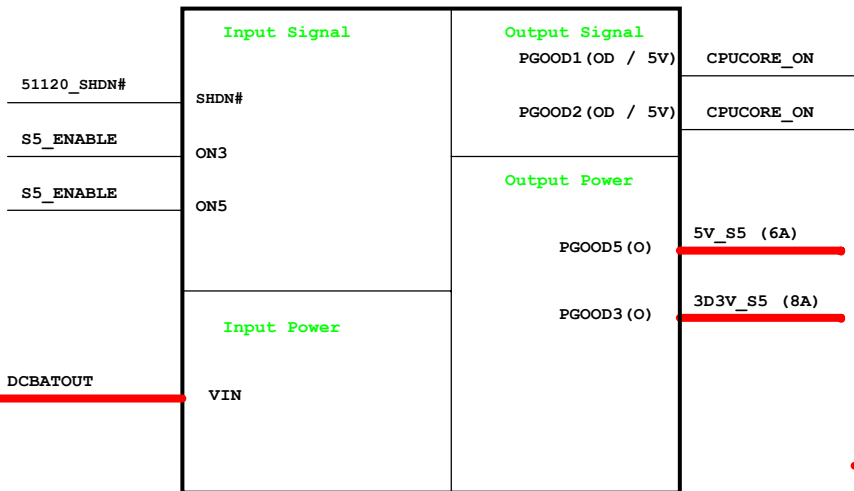
TPS51100
DDR_VREF_S0



API5912
1D5V_S0



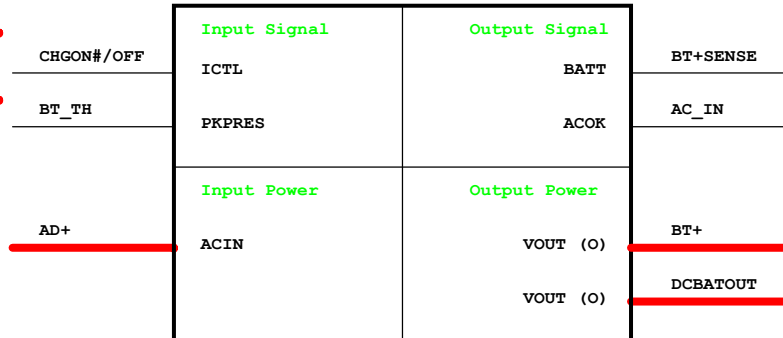
TPS51120
5V_S5 / 3D3V_S5



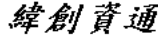
APL5308
2D5V_S0

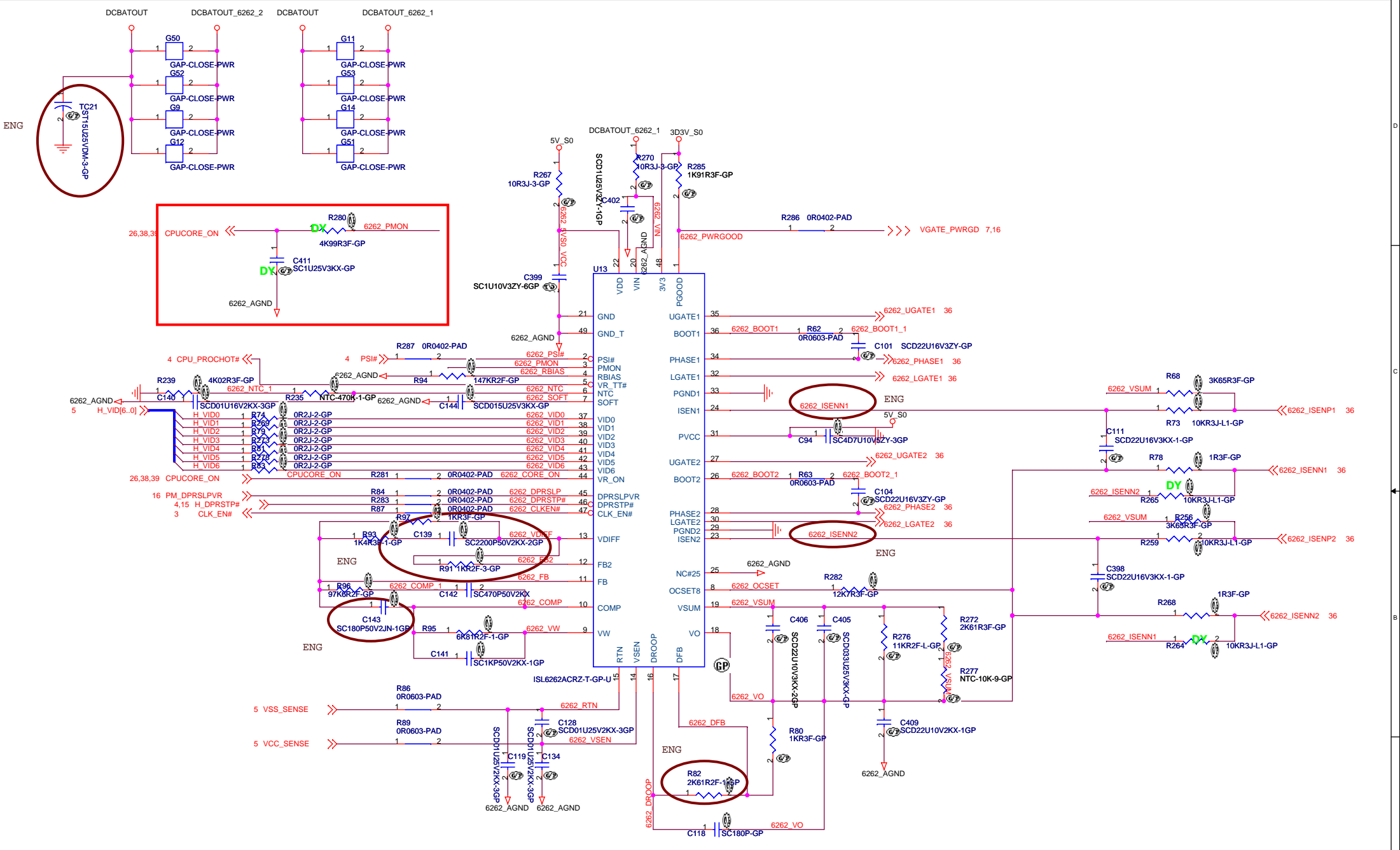


Charger MAX8731A



<Core Design>

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Power Block Diagram		
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DCBATOUT

DCBATOUT_6262_2

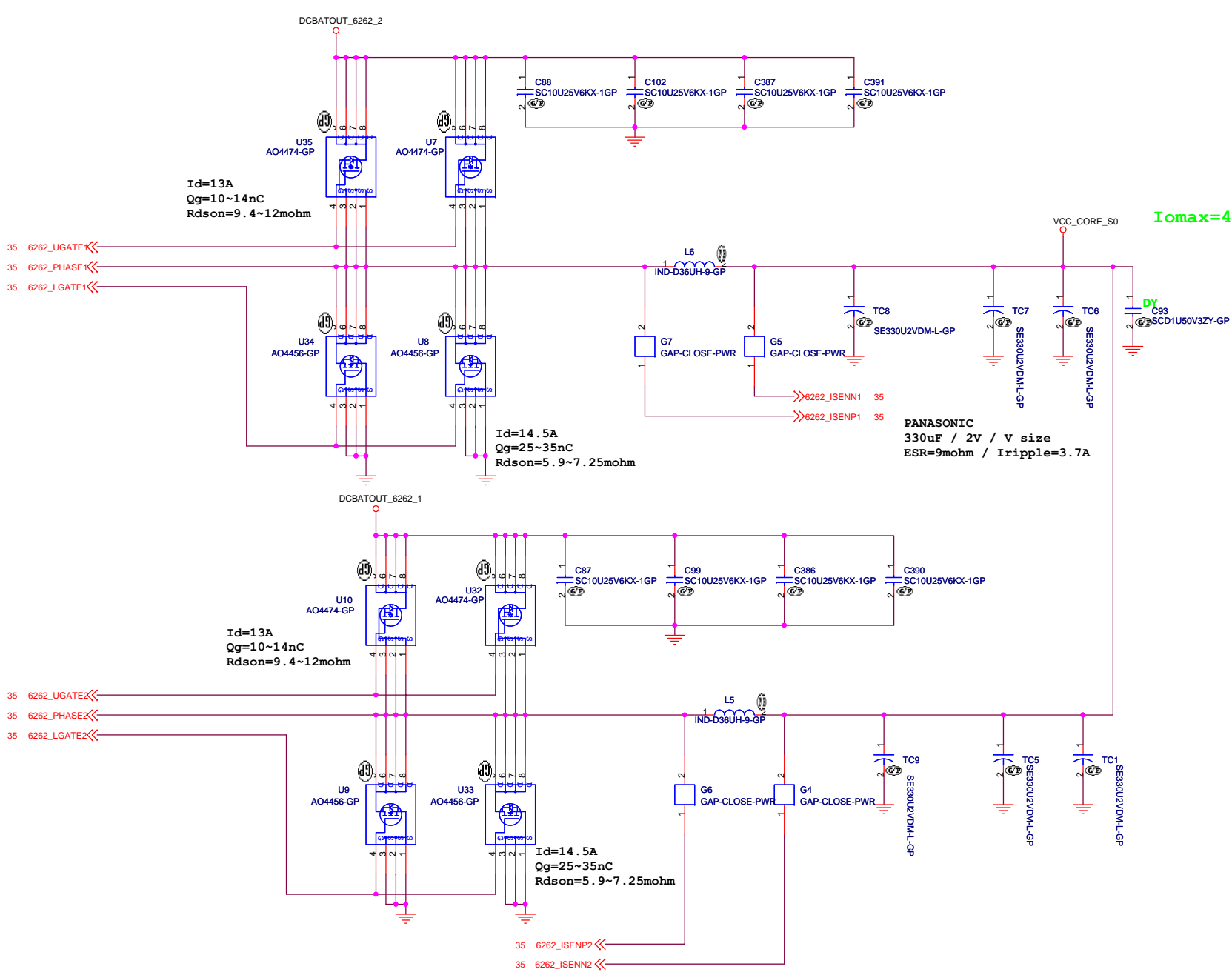
DCBATOUT_6262_1

G54
GAP-CLOSE-PWR
6262_AGND

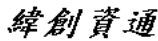
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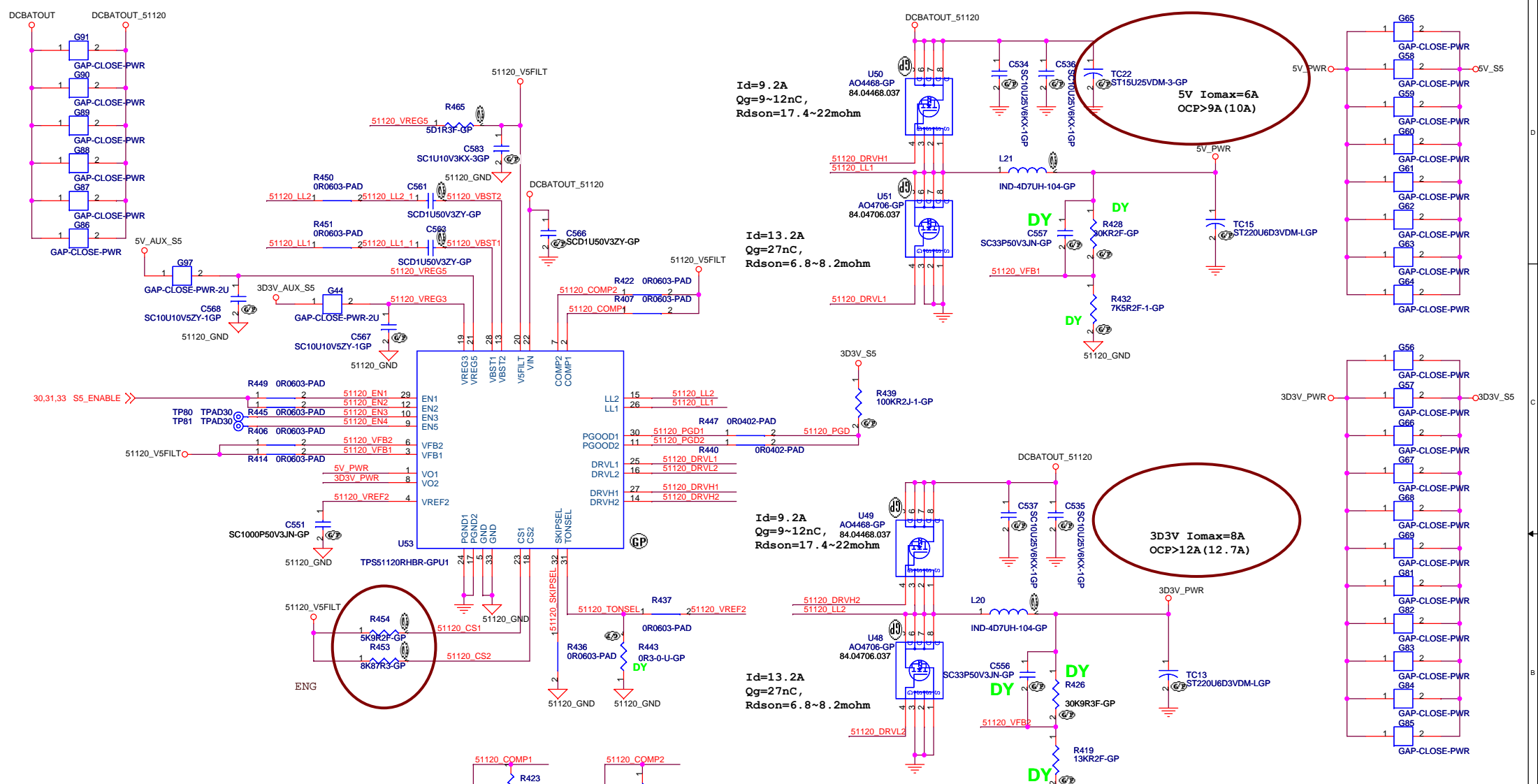
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU Vcore Power_1	
Size	Document Number
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CPU Vcore Power_2	
Title	
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Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

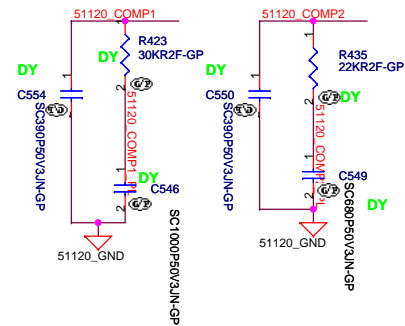
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Qg=9~12nC,
Rdson=17.4~22mohm

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

5V Iomax=6A
OCP>9A (10A)

3D3V Iomax=8A
OCP>12A (12.7A)

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

$V_{out} = 1V * (R1 + R2) / R2$

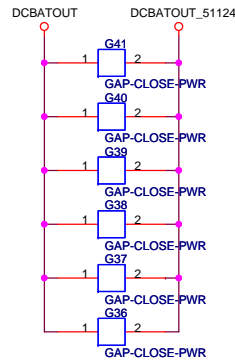
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緯創資通 Wistron Corporation
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Title: **3D3V S5 & 5V S5**

Size: Document Number **Huron** Rev: **SD**

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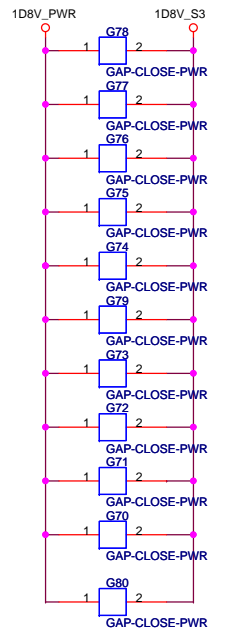
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Qg=9~12nC,
Rdson=17.4~22mohm

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

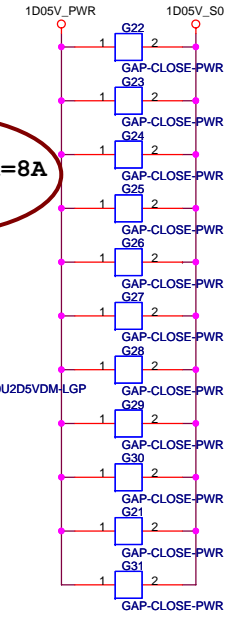
1D8V Iomax=10A
OCP>15

Netswap
DCR=7.5m ohm
Irms=12A, Isat=20A
Voutsetting=1.8046V

Kemet
220uF/ 4V
ESR=15mohm



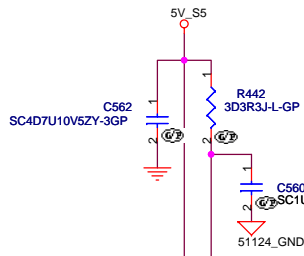
$$V_{out} = 0.758V * (R1 + R2) / R2$$



1D05V Iomax=8A
OCP>12A

Netswap
DCR=7.5m ohm
Irms=12A, Isat=20A
Voutsetting=1.05V

Kemet
220uF/ 4V
ESR=15mohm



1D05V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1

OCP
2007.1.19

16,27,30,40 PM_SLP_S4#
9,26,27,30,33,39,40 PM_SLP_S3#

$$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$$

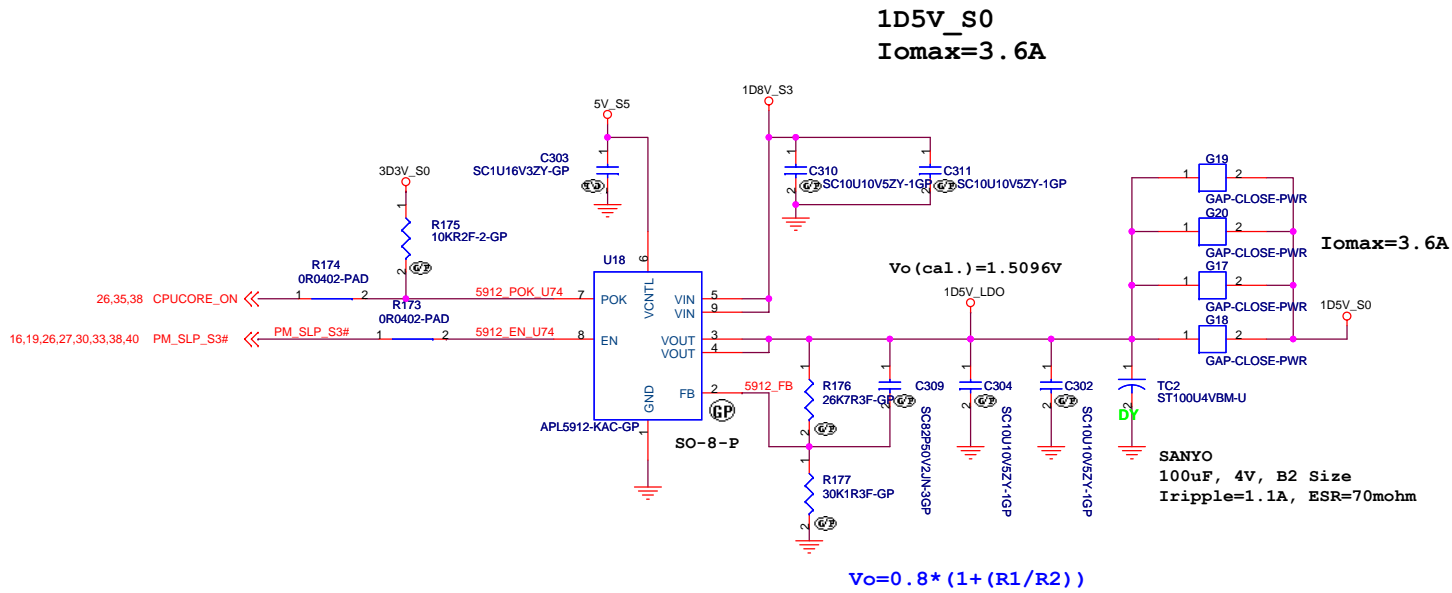
$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

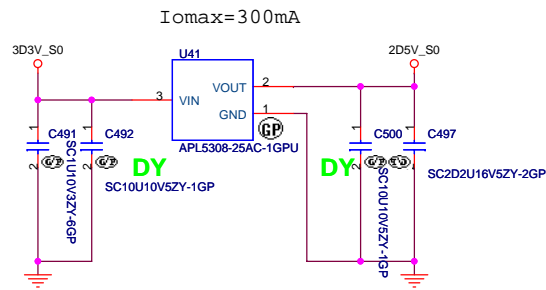
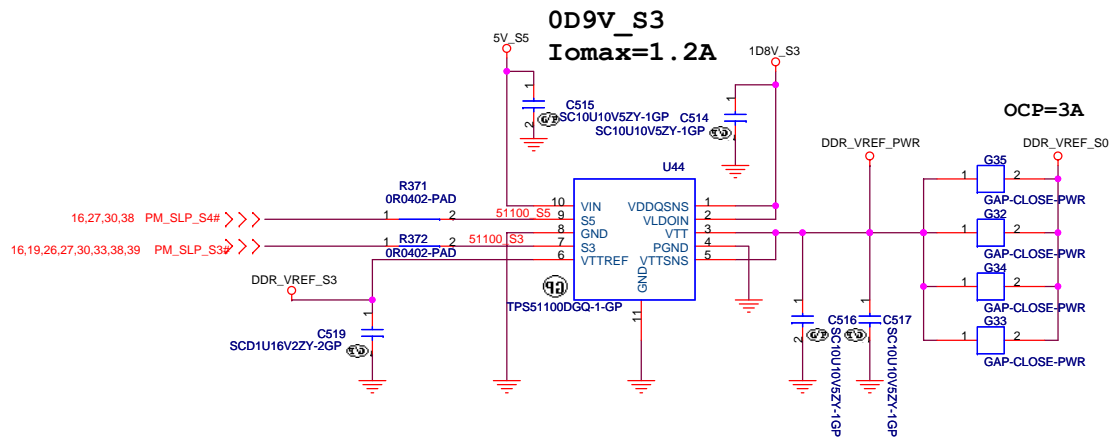
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			TPS51124 1D8V 1D05V		
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<Core Design>

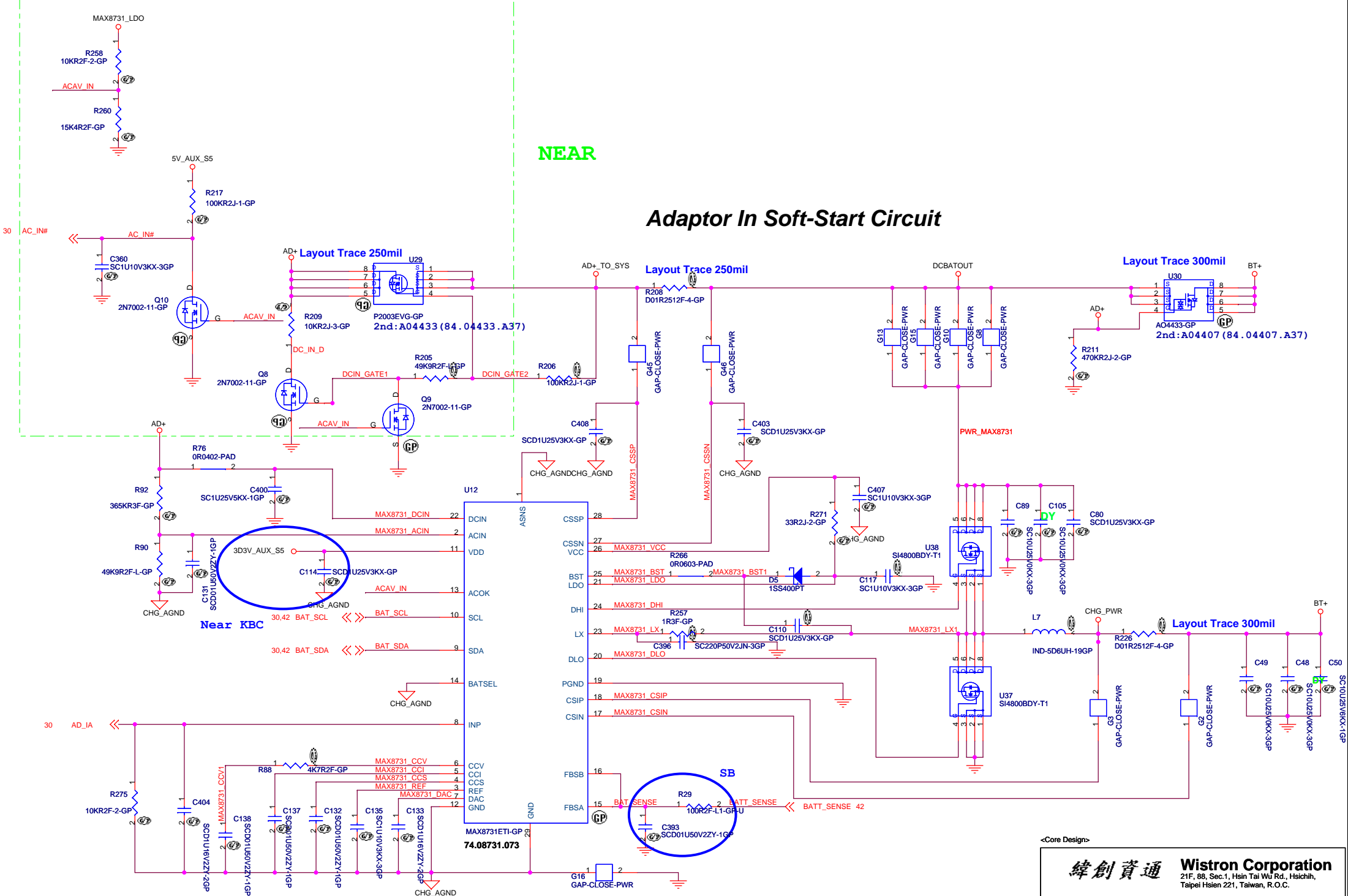
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		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
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Size A3	Document Number	Huron	
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Adaptor In Soft-Start Circuit

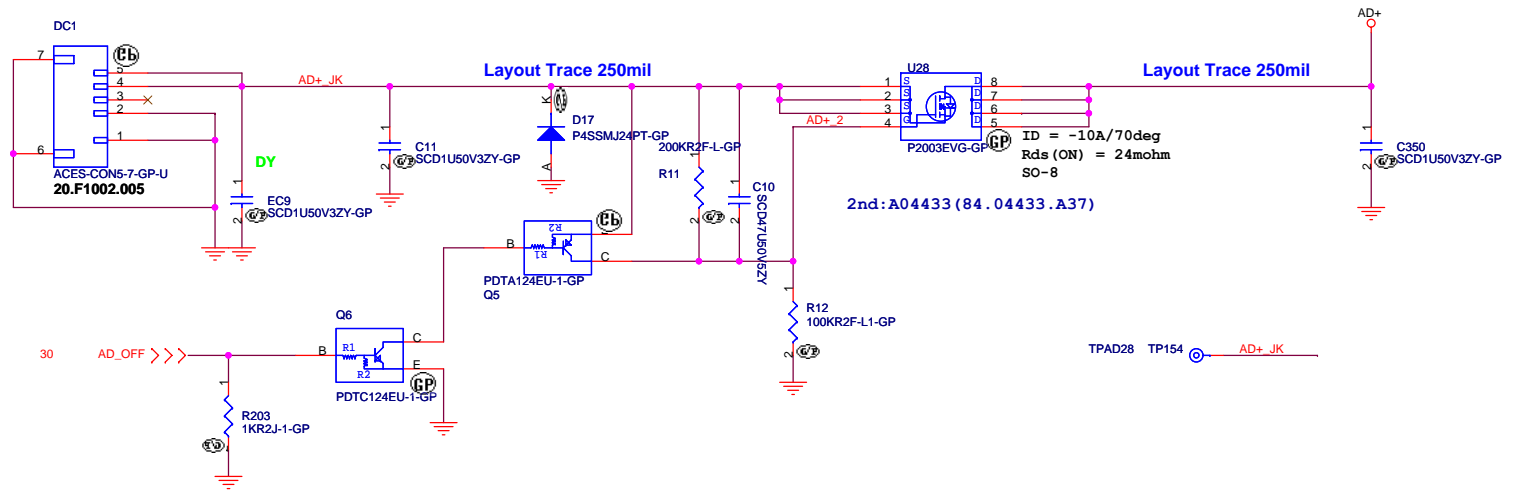
Need Check MAXIM Sming Use MAX8731 or MAX8731A

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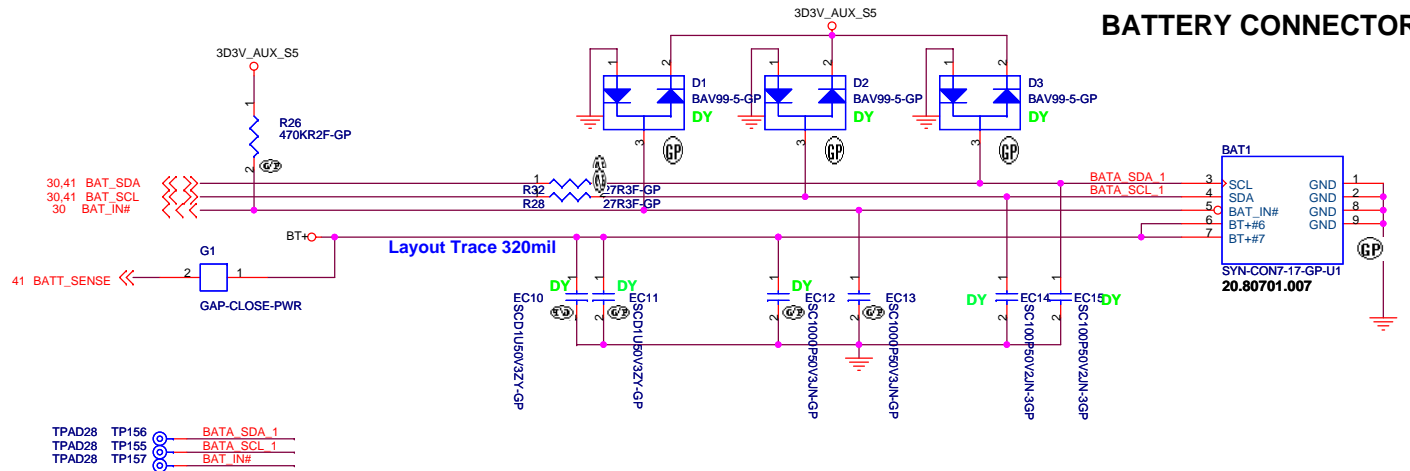
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



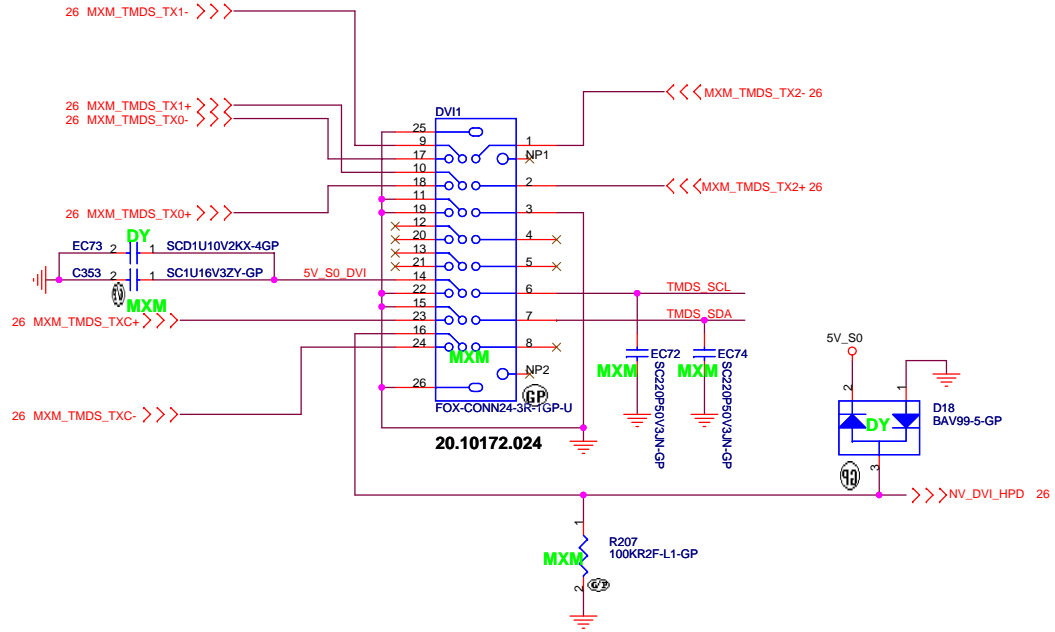
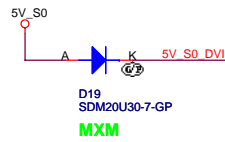
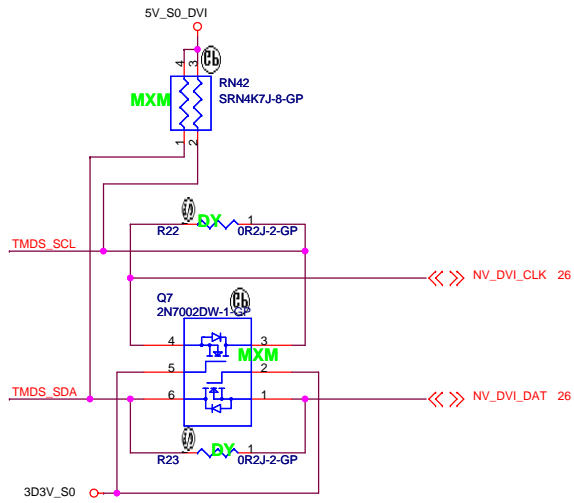
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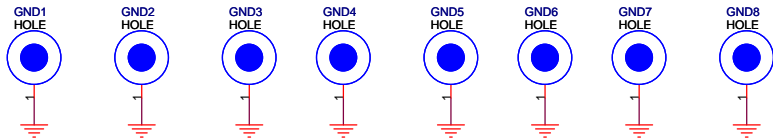
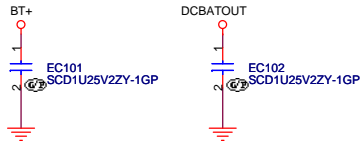
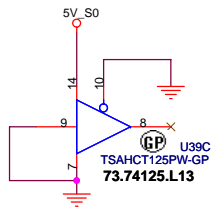
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Title
AD/BATT CONN

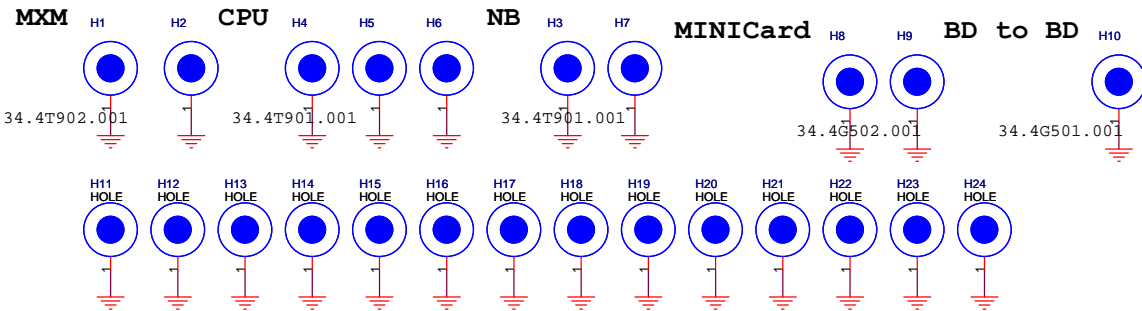
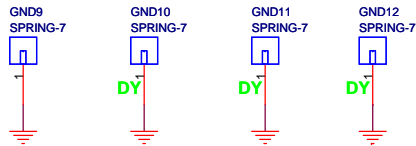
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Spring



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