Colossus 15/17
DIS_OPT Schematic
IVY Bridge (rPGA989)
Intel PCH (Panther Point)

REV:-1
2012-01-05.

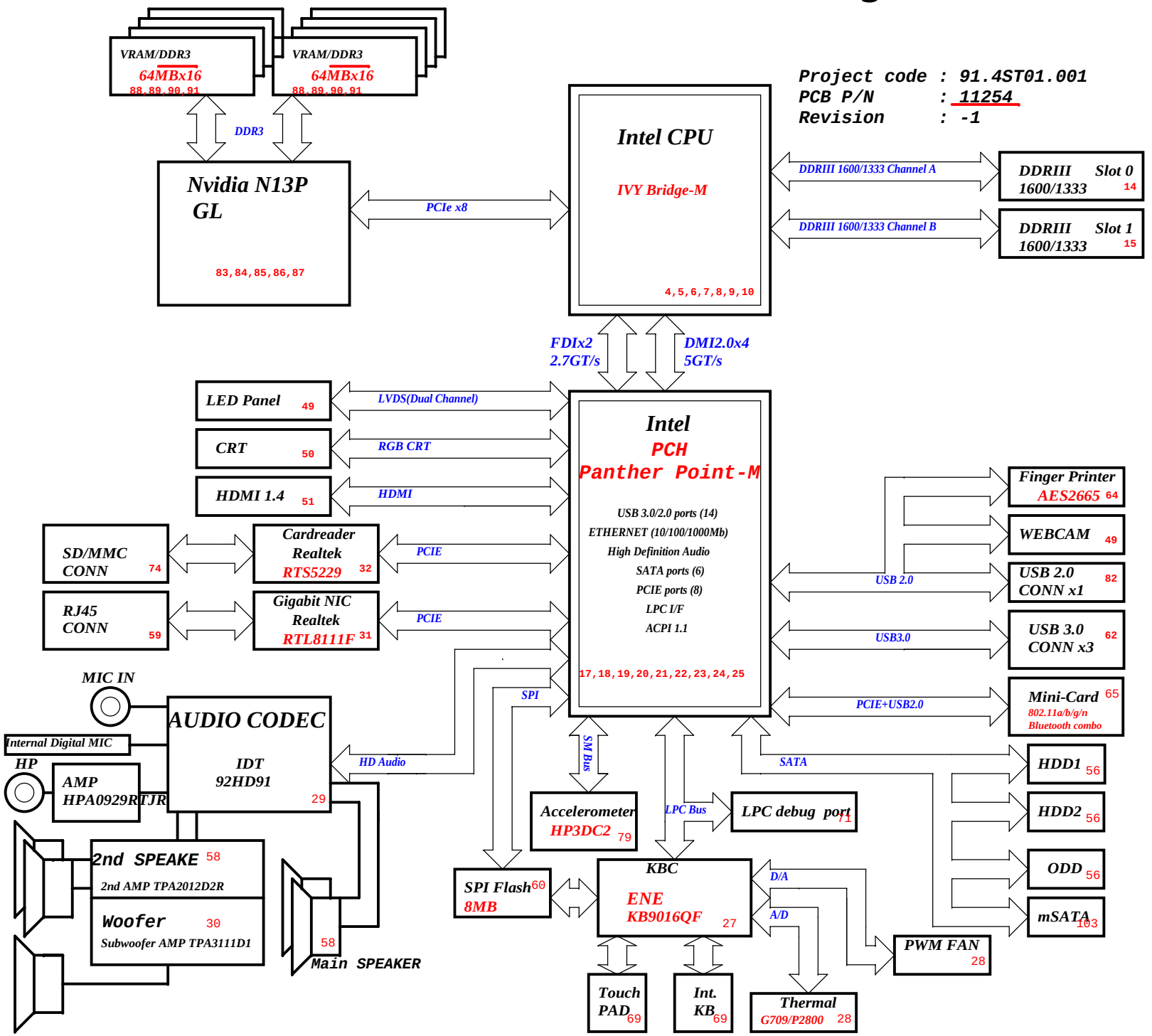
DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 1 of 103	

COLOSSUS Block Diagram



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0

CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)

L1:Top	L5:Vcc
L2:GND	L6:Signa
L3:Signal	L7:GND
L4:Signal	L8::Bottom

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 2 of 103

PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_0D85V 0D75V_S0 VCC_CORE VCC_GFXCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 3.3V 1D5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

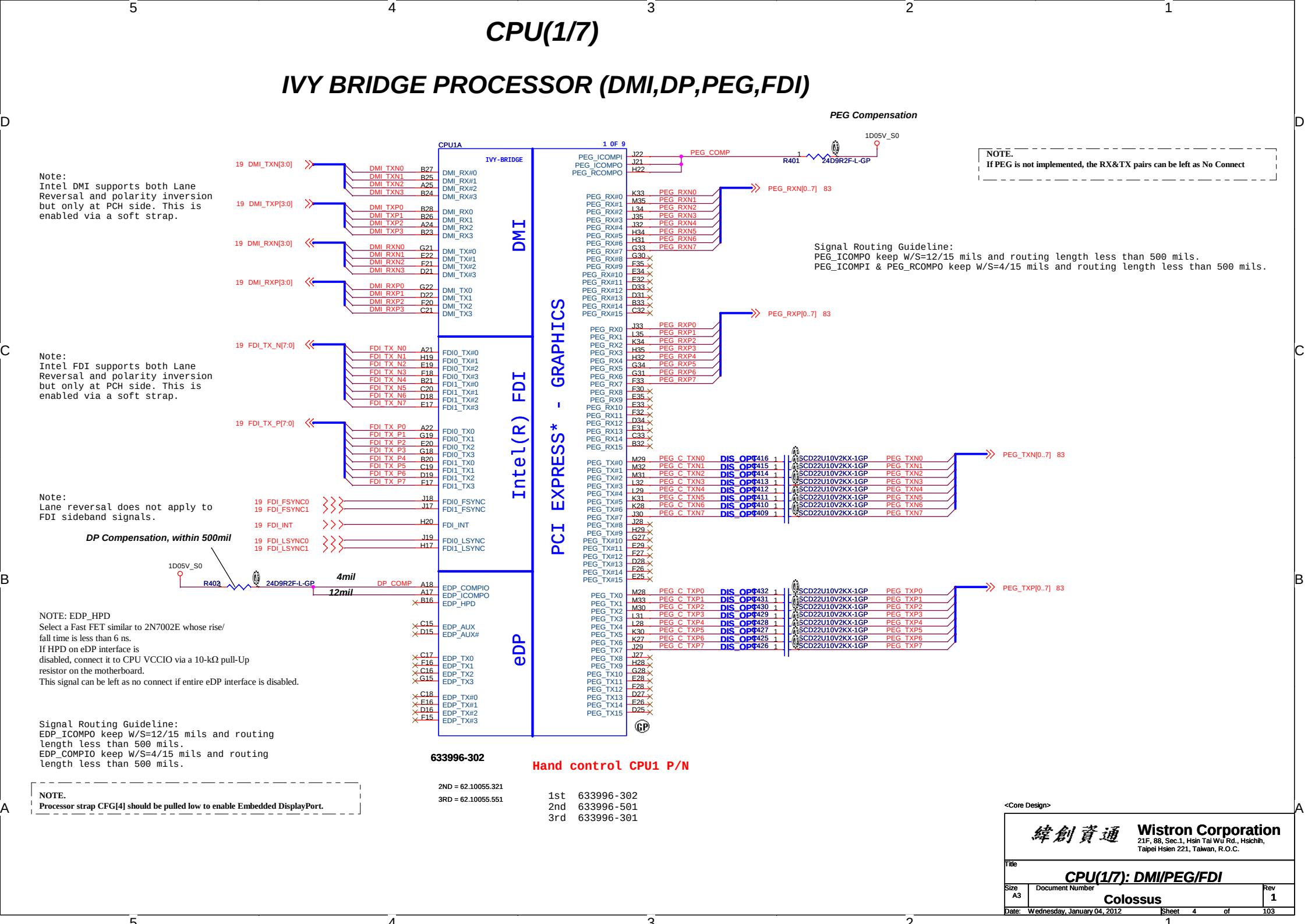
Title: Table of Content

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 3 of 103

CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

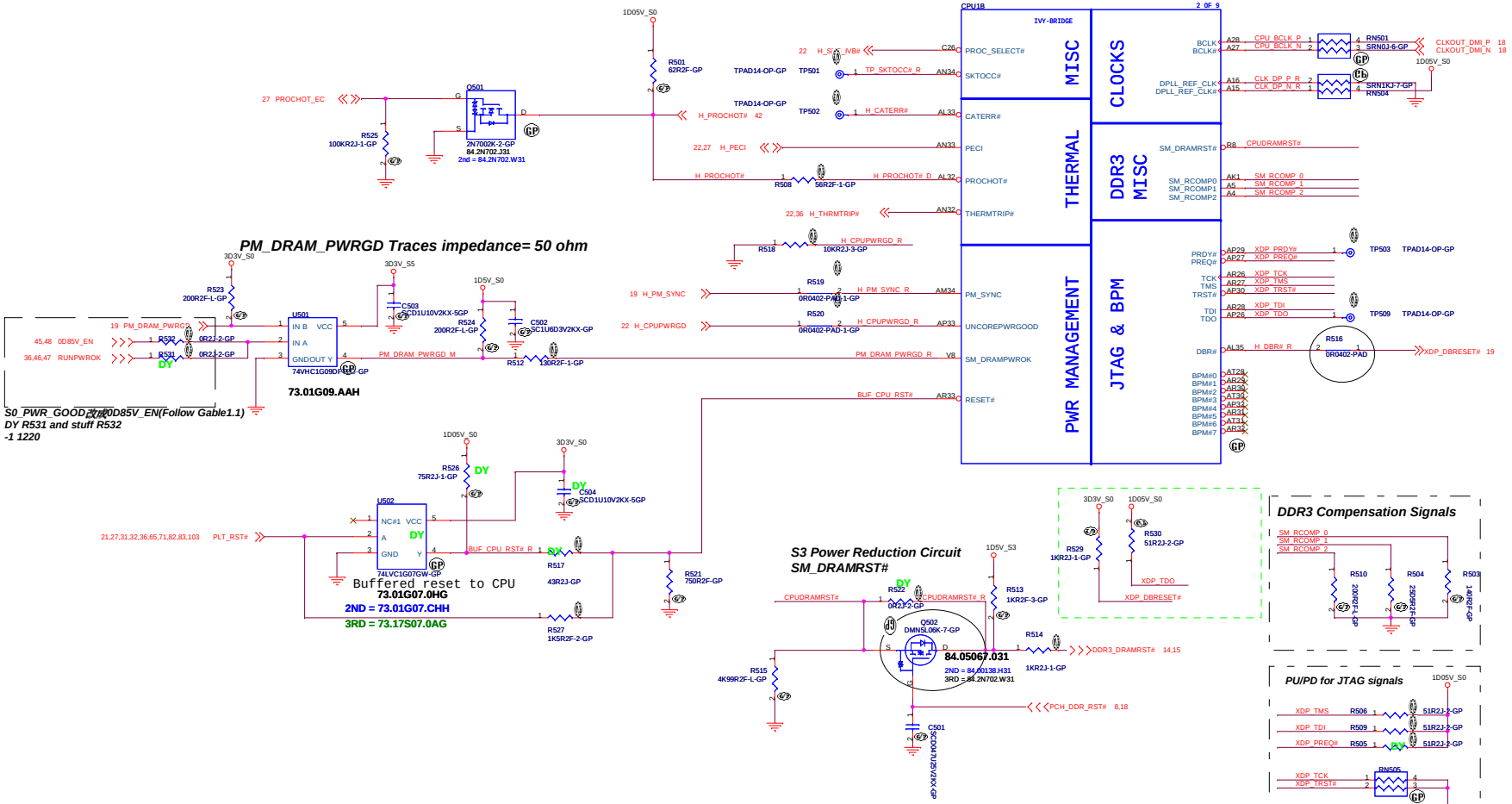
Title: CPU(1/7): DMI/PEG/FDI

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 4 of 103

CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

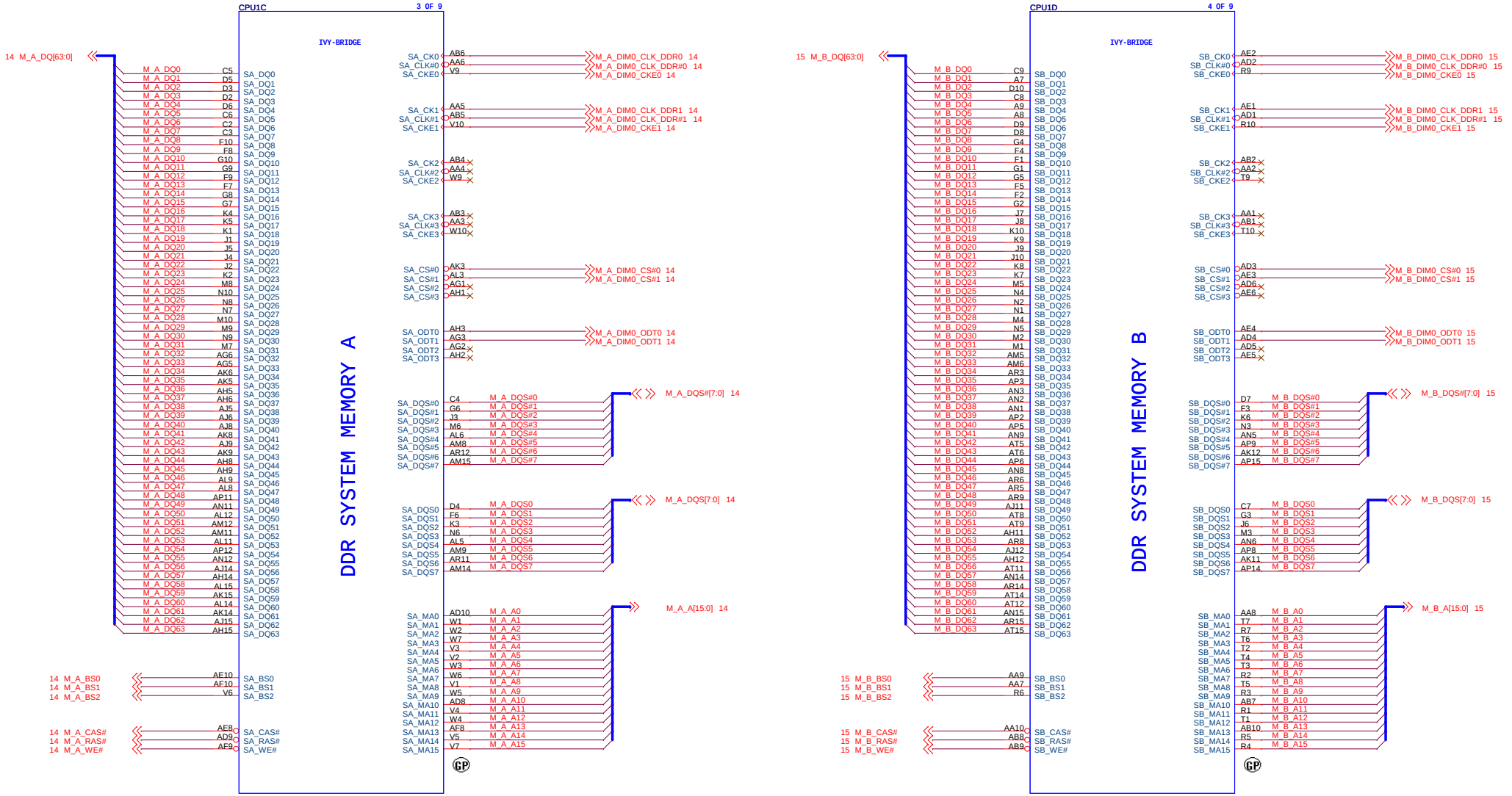
Title: CPU(2/7): CLK/MISC/JTAG

Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 5 of 103

CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU(3/7): DDR3***	
Size: Custom	Document Number: **Colossus**	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 6 of 103	

CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F

6 OF 9

IVY-BRIDGE

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A

VCC_CORE

Place Bottom

Place Top

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

Power 78.22610.51L

Differential Sense feedback

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(4/7): PWR

Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 7 of 103

CPU(5/7)
IVY BRIDGE PROCESSOR (GRAPHICS POWER)

M3 - Processor Generated SO-DIMM VREF_DQ

33A

VCC_GFXCORE

470U*2 22U*6

Under Socket and Closed to CPU

C820 C821 C822 C823 C824 C825 — SC22U6D3V5MX-2GP

VCC_GFXCORE

22U*6

Closed to CPU Socket

C826 C827 C828 C829 C830 C831 — SC22U6D3V5MX-2GP

Power 78.22610_51L

C837 C836 C835 C834 C833 — SC22U6D3V5MX-2GP; C832 — SC10U6D3V5KX-1GP

1.5A

1D8V_S0

C819 C816 C817 C818 — SC10U6D3V5KX-1GP / SC1U10V2KX-1GP

POWER

CPU1G — 7 OF 9 — IVY-BRIDGE

GRAPHICS

SENSE LINES

VAXG_SENSE	AK35	VCC_AXG_SENSE 42
VSSAXG_SENSE	AK34	VSS_AXG_SENSE 42

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ — B4 — DDR_VREF_S3_B4
SB_DIMM_VREFDQ — D1 — DDR_VREF_S3_D1

R815 1KR2F-3-GP DY; R816 1KR2F-3-GP DY

C801 SC1U16V2ZY-2GP DY; C802 SC2D2U10V2ZY-1GP DY

CAD Note: +V_SM_VREF should have 10 mil trace width

DDR3 -1.5V RAILS

12~16A

1D5V_S0

330U*1 10U*6

VDDQ1 AE7; VDDQ2 AE4; VDDQ3 AE1; VDDQ4 AC7; VDDQ5 AC4; VDDQ6 AC1; VDDQ7 Y7; VDDQ8 Y4; VDDQ9 Y1; VDDQ10 U7; VDDQ11 U4; VDDQ12 U1; VDDQ13 P7; VDDQ14 P4; VDDQ15 P1

C803 SC4D7U6D3V3KX-GP; C804 SC4D7U6D3V3KX-GP; C805 SC10U6D3V5KX-1GP; C806 SC10U6D3V5KX-1GP; C807 SC10U6D3V5KX-1GP DY; C808 SC10U10V5KX-2GP DY

TC801 ST330U2D5VDM-9GP

77.23371.13L
2nd = 79.33719.L01

SA RAIL

6A

0D85V_S0

VCCSA1 M27; VCCSA2 M26; VCCSA3 L26; VCCSA4 J26; VCCSA5 J25; VCCSA6 J24; VCCSA7 H26; VCCSA8 H25

C813 C814 C815 — SC10U6D3V5KX-1GP

0D85V_S0 — R801 100R2J-2-GP DY — VCCUSA_SENSE 48

MISC

VCCSA_SENSE — H23 — VCCUSA_SENSE

VCCSA_VID0 C22; VCCSA_VID1 C24 — H_FC_C22 — VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

RN801 SRN1KJ-11-GP-U

VCCIO_SEL — A19 — H_VCCP_SEL

SNB: No Connect
IVB: VSS

R817 0R2J-2-GP DY — H_SNB_IVB#_PWRCTRL — TP801 TPAD14-OP-GP

R818 0R2J-2-GP DY

1.8V RAIL

VCCPLL1 B6; VCCPLL2 A6; VCCPLL3 A2

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

DDR_VREF_S3

R808 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0

R809 0R2J-2-GP DY

15 M_VREF_DQ_DIMM1

84.05067.031
2ND = 84.00138.H31
3RD = 84.2N702.W31

Q802 DMN5L06K-7-GP

PCH_DDR_RST#

R810 0R2J-2-GP DY

0R2J-2-GP R812; 0R2J-2-GP R813

M_VREF_DQ_DMM0_R
M_VREF_DQ_DMM1_R

DDR_VREF_S3_B4
DDR_VREF_S3_D1

3RD = 84.2N702.W31
2ND = 84.00138.H31
84.05067.031

Q803 DMN5L06K-7-GP

R814 0R2J-2-GP DY

5,18 PCH_DDR_RST#

-1 1221

S3 Power Reduction Circuit Processor VREF_DQ Implementation

DDR_VREF_S3

R807 0R2J-2-GP

R811 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0

R805 0R2J-2-GP DY

+V_SM_VREF

Q801 DMN5L06K-7-GP

84.05067.031
2ND = 84.00138.H31
3RD = 84.2N702.W31

+V_SM_VREF_CNT

R803 100KR2J-1-GP

R802 0R2J-2-GP DY

5,18 PCH_DDR_RST#

19,27,36,46,47,92 PM_SLP_S3#

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

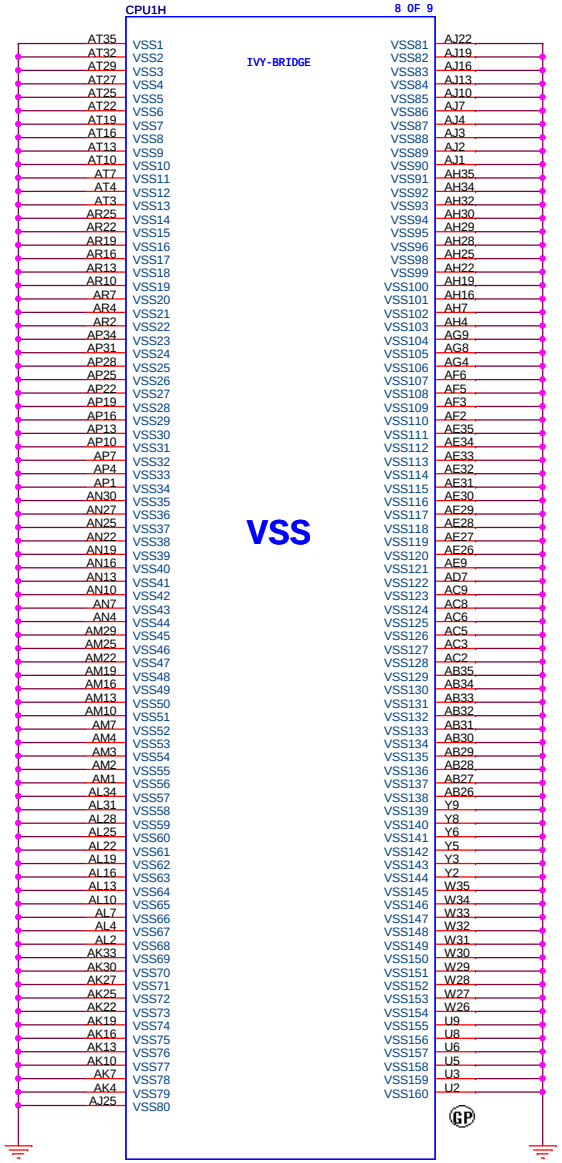
Title: CPU(5/7): GFX/PWR

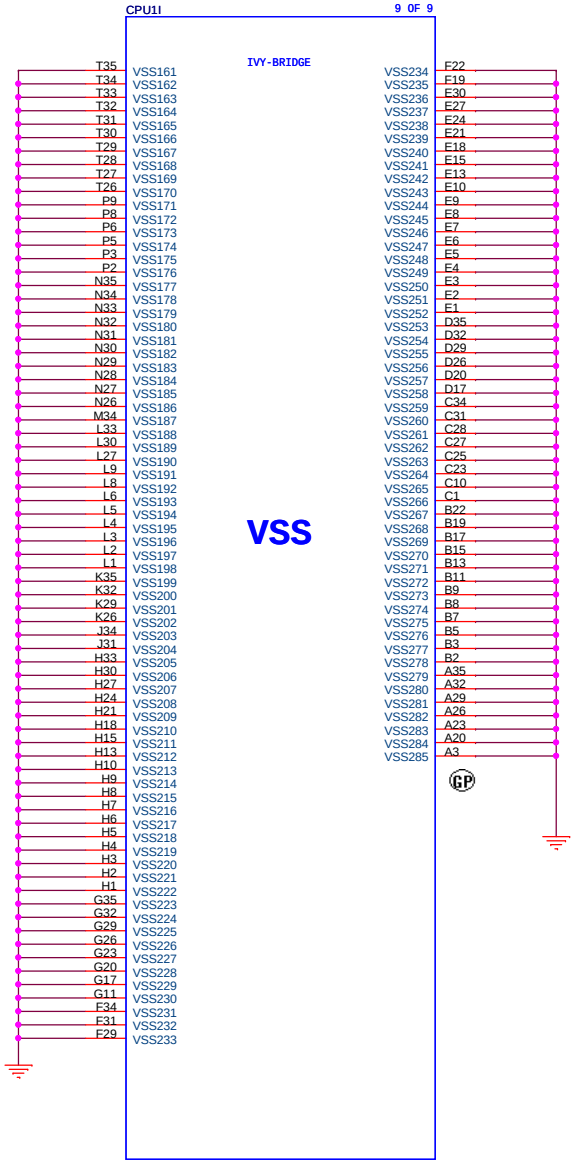
Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 8 of 103

CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

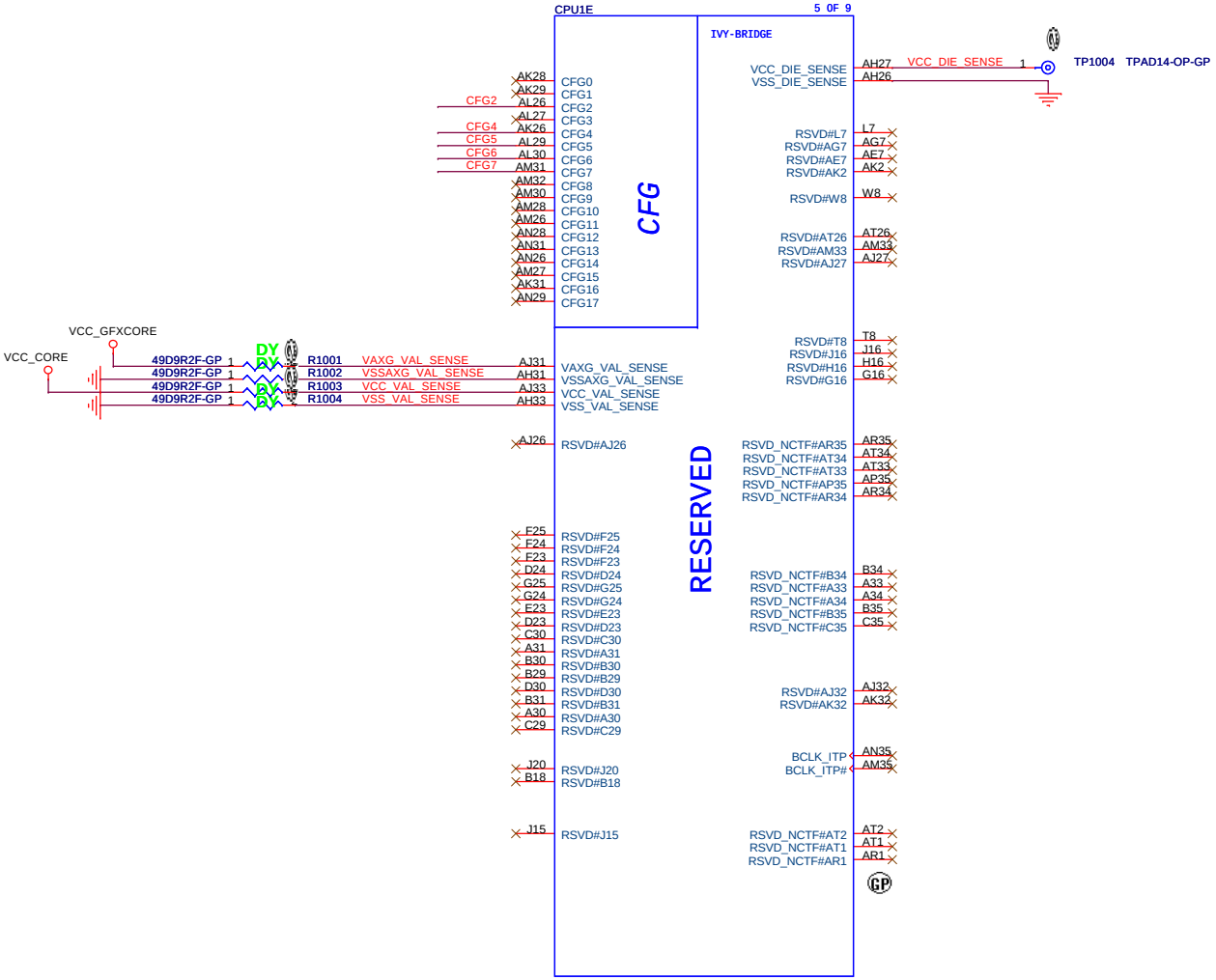
Title: **CPU (6/7):GND**

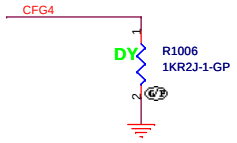
Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 9 of 103

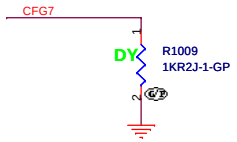
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

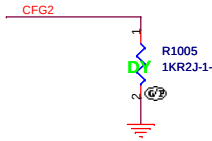




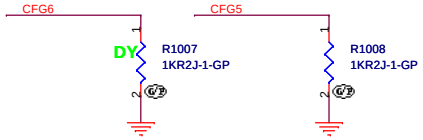
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(7/7): CFG/RSVD/DDR3_VRE**

Size	Document Number	Rev
A3	Colossus	1

Date: Tuesday, December 27, 2011 Sheet 10 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_XDP*		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 11 of 103	

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 12 of 103

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

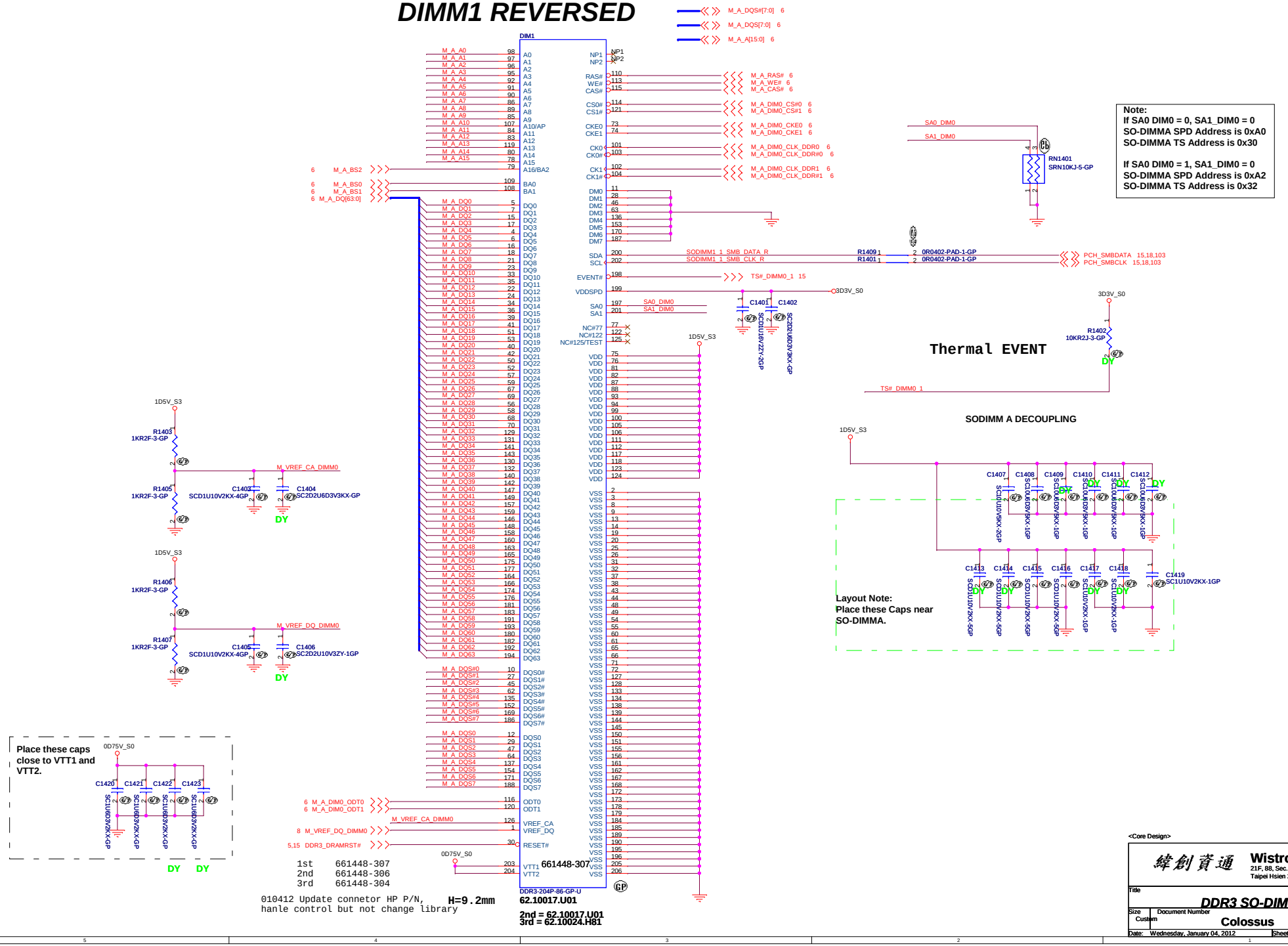
Title

AOAC

Size	Document Number	Rev
A3	**Colossus**	1

Date: Monday, December 26, 2011 Sheet 13 of 103

DIMM1 REVERSED



<Core Design>

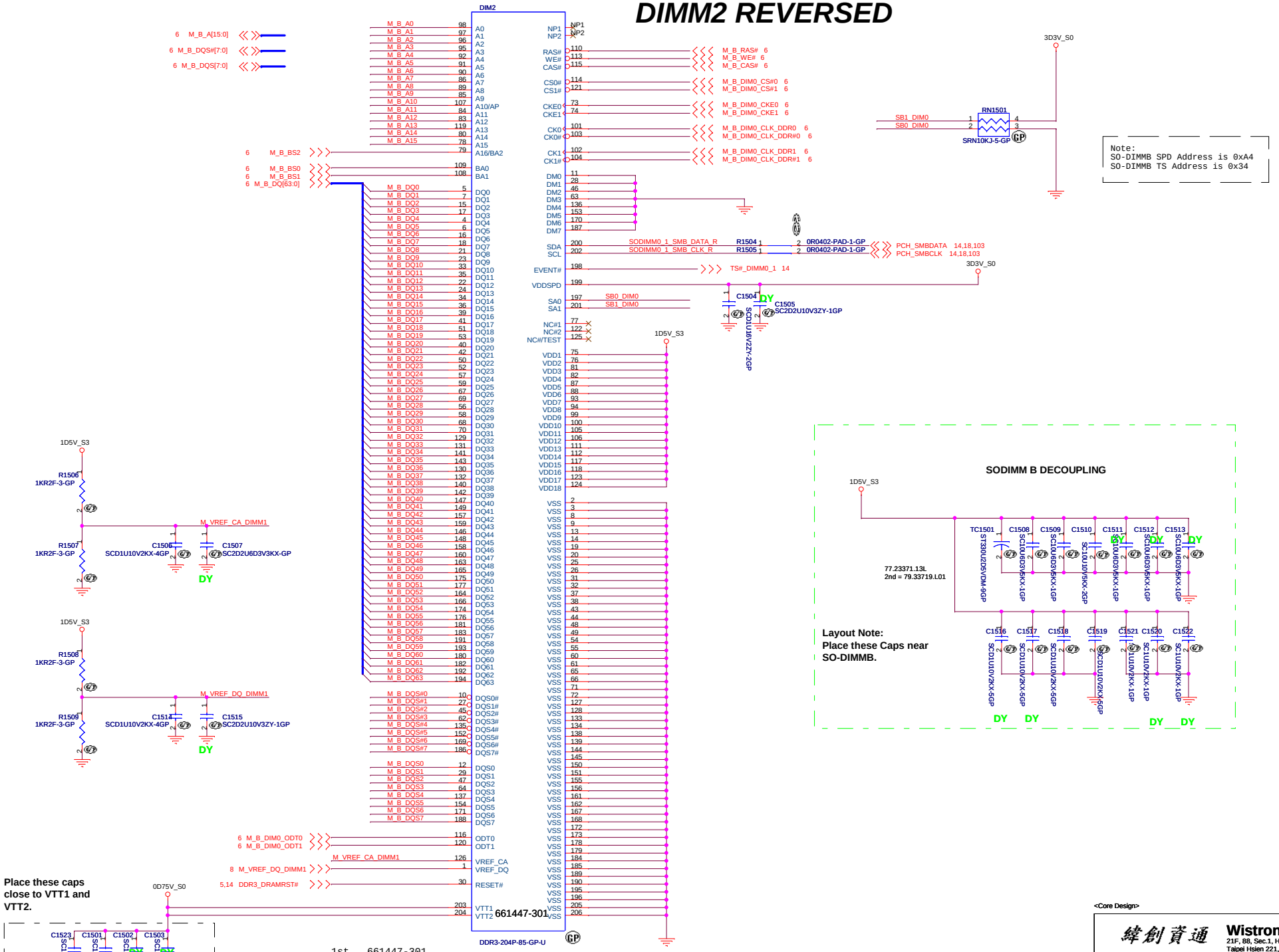
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM1

Size	Document Number	Rev
Custom	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 14 of 103

DIMM2 REVERSED



(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 16 of 103

PCH(1/9)

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5; SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10; SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4; SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1; SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1; SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

RTC Battery

RTC1 — ACES-CON2-18-GP — 20.F1637.002 — 2ND = 20.F1864.002
+RTC_VCC — R1720 1KR2J-1-GP — RTC PWR — U1701 MM715FPT-GP — 83.R0304.B81 — 2ND = 83.R2004.C81
C1705 SC1U10V3ZY-6GP

NO REBOOT STRAP

No Reboot Strap R1722	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 — R1722 10KR2J-3-GP DY HDA_SPKR — R1723 10KR2J-3-GP INT_SERIRQ

5V_S0 — R1730 10KR2J-3-GP HDA_SDO_G — Q1703 DMN5L06K-7-GP U1703 — 84.05067.031 — 2ND = 84.00138.H31 — 3RD = 84.2N702.W31 — HDA_SYNC_C S D HDA_SYNC

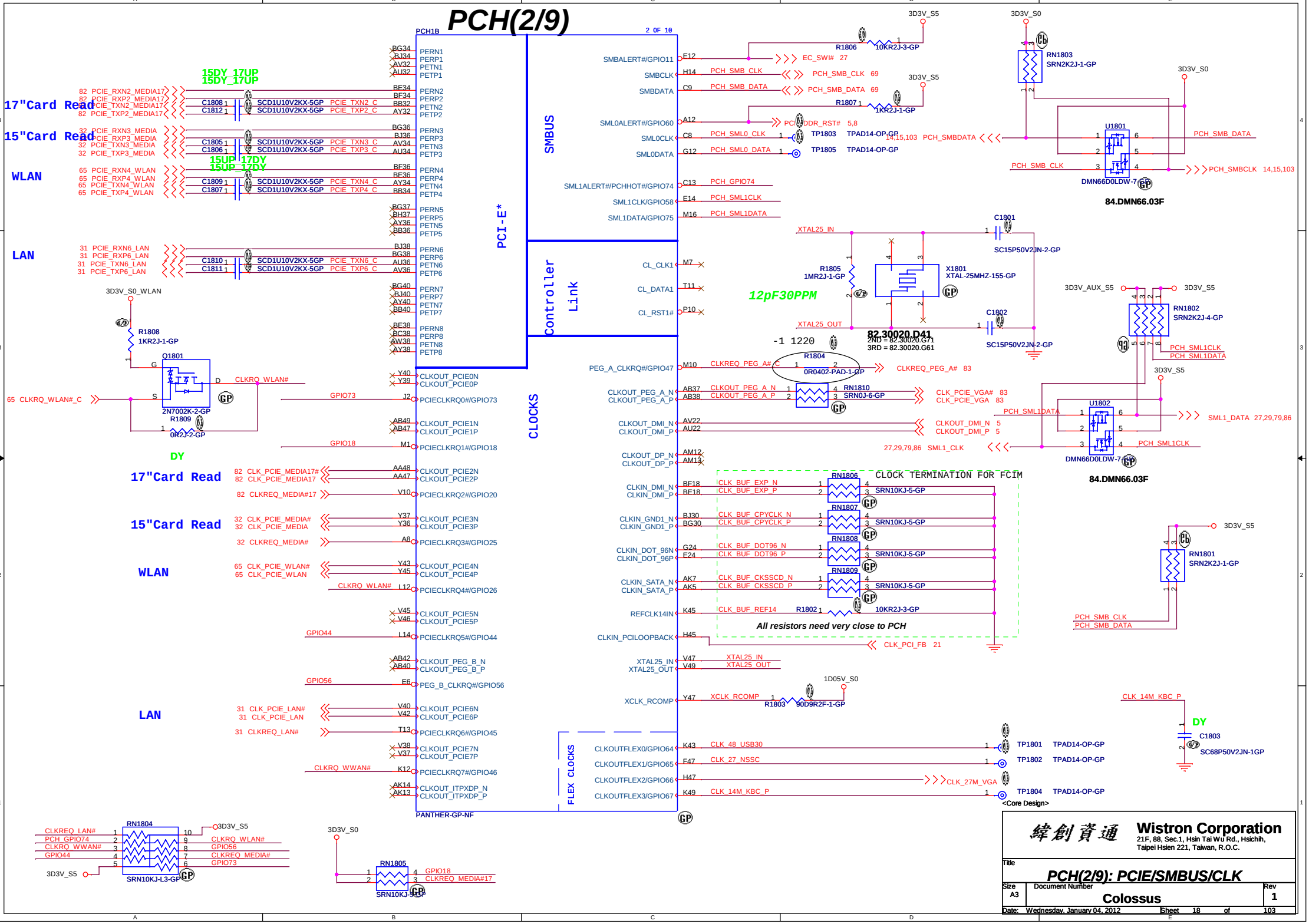
3D3V_S5 — PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS; R1718 210R2F-L-GP PCH_JTAG_TDO; R1719 210R2F-L-GP PCH_JTAG_TDI
DY_PCHXDP — RN1703 SRN100F-7-GP — PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO
PCHXDP — R1721 51R2J-2-GP PCH_JTAG_TCK_BUF; R1727 DY 1KR2J-1-GP HDD_HALTLED_R; R1728 DY 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH(1/9): HDA/JTAG/SATA
Size A3	Document Number: Colossus — Rev: 1
Date: Wednesday, January 04, 2012	Sheet 17 of 103

PCH(2/9)



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

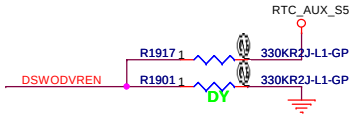
Title: PCH(2/9): PCIE/SMBUS/CLK

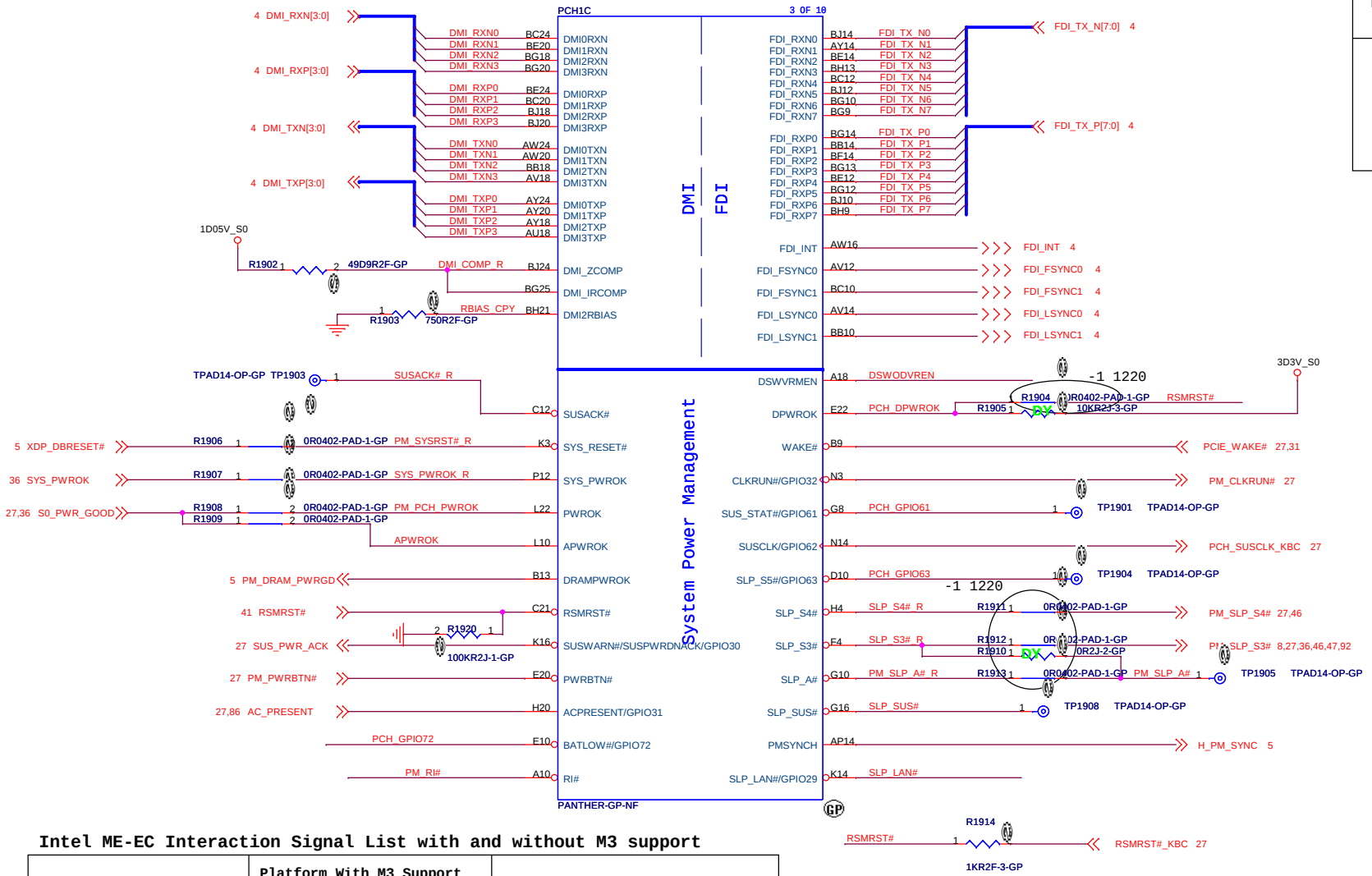
Size	Document Number	Rev
A3	Colossus	1

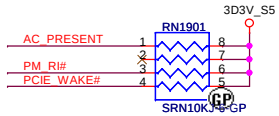
Date: Wednesday, January 04, 2012 Sheet 18 of 103

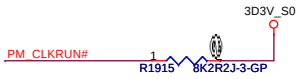
PCH(3/9)

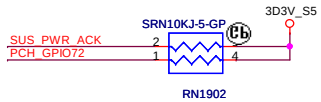
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED	Disabled

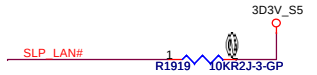












Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

<Core Design>

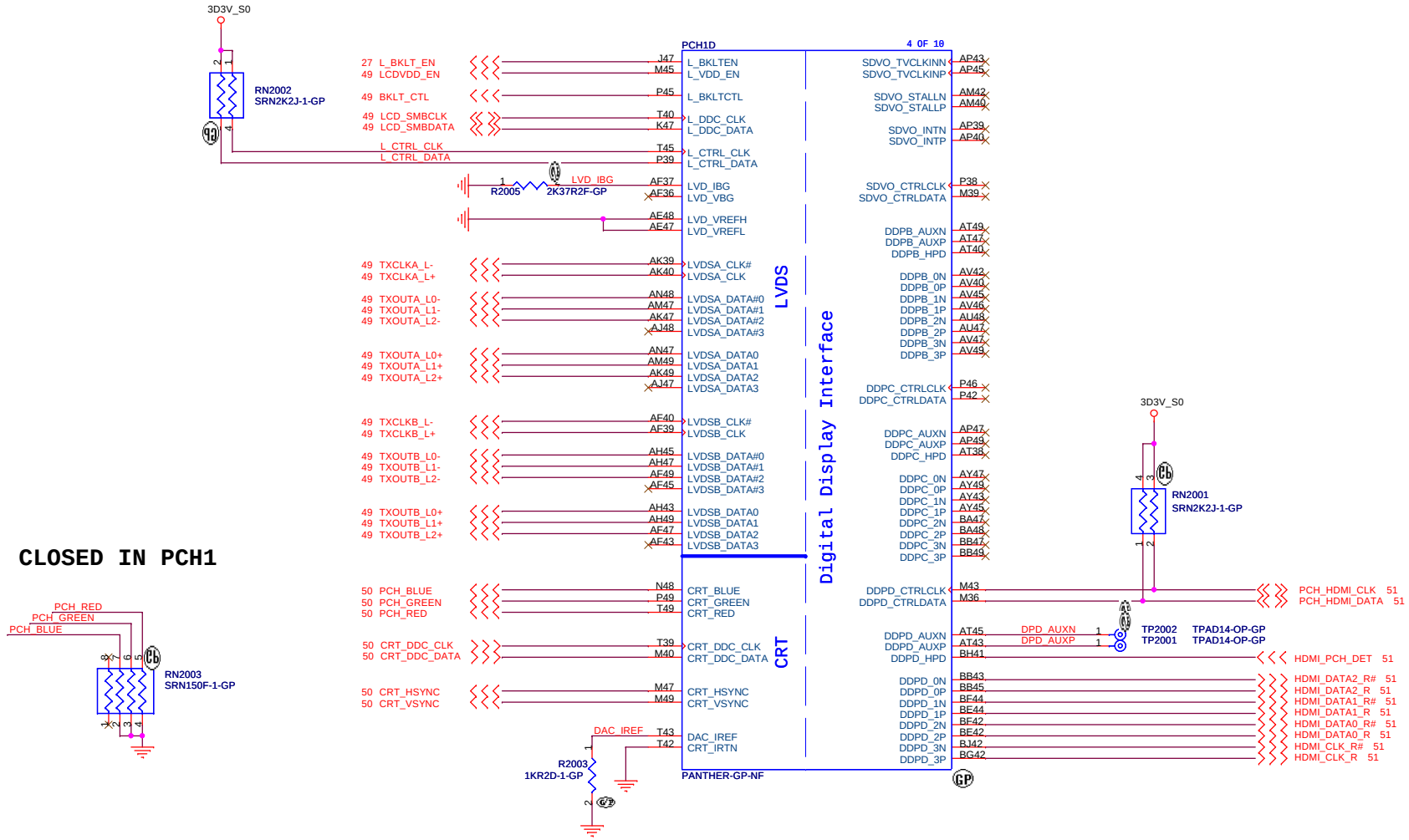
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(3/9): DMI/FDI/PM

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 19 of 103

PCH(4/9)



CLOSED IN PCH1

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(4/9): LVDS/CRT/DDI**

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 20 of 103

PCH(5/9)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

USB2.0 Table

USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB 3.0 Conn. 1
USB 3.0 Conn. 2
USB 3.0 Conn. 3 (UB1)
BT WLAN combo
Fingerprint
USB 2.0 Conn. 1 (UB1)
Camera
-1 12/15

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

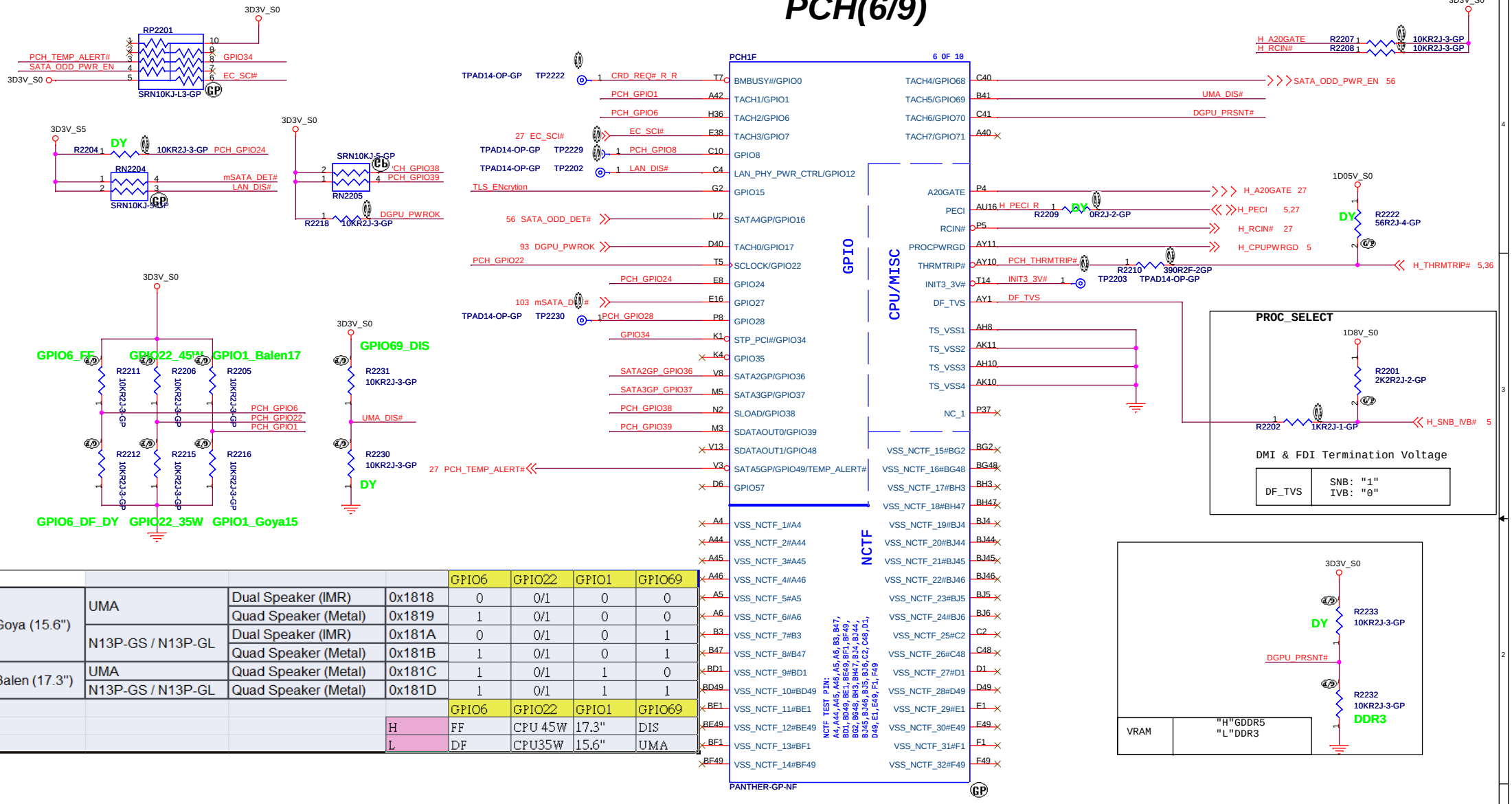
(UB2)
(UB2)
-1 12/15

AND GATE
73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(5/9): PCI/USB/NVM
Size: A3
Document Number: Colossus
Rev: 1
Date: Wednesday, January 04, 2012
Sheet 21 of 103

PCH(6/9)



				GPIO6	GPIO22	GPIO1	GPIO69
Goya (15.6")	UMA	Dual Speaker (IMR)	0x1818	0	0/1	0	0
		Quad Speaker (Metal)	0x1819	1	0/1	0	0
	N13P-GS / N13P-GL	Dual Speaker (IMR)	0x181A	0	0/1	0	1
		Quad Speaker (Metal)	0x181B	1	0/1	0	1
Balen (17.3")	UMA	Quad Speaker (Metal)	0x181C	1	0/1	1	0
	N13P-GS / N13P-GL	Quad Speaker (Metal)	0x181D	1	0/1	1	1
				GPIO6	GPIO22	GPIO1	GPIO69
			H	FF	CPU 45W	17.3"	DIS
			L	DF	CPU35W	15.6"	UMA

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

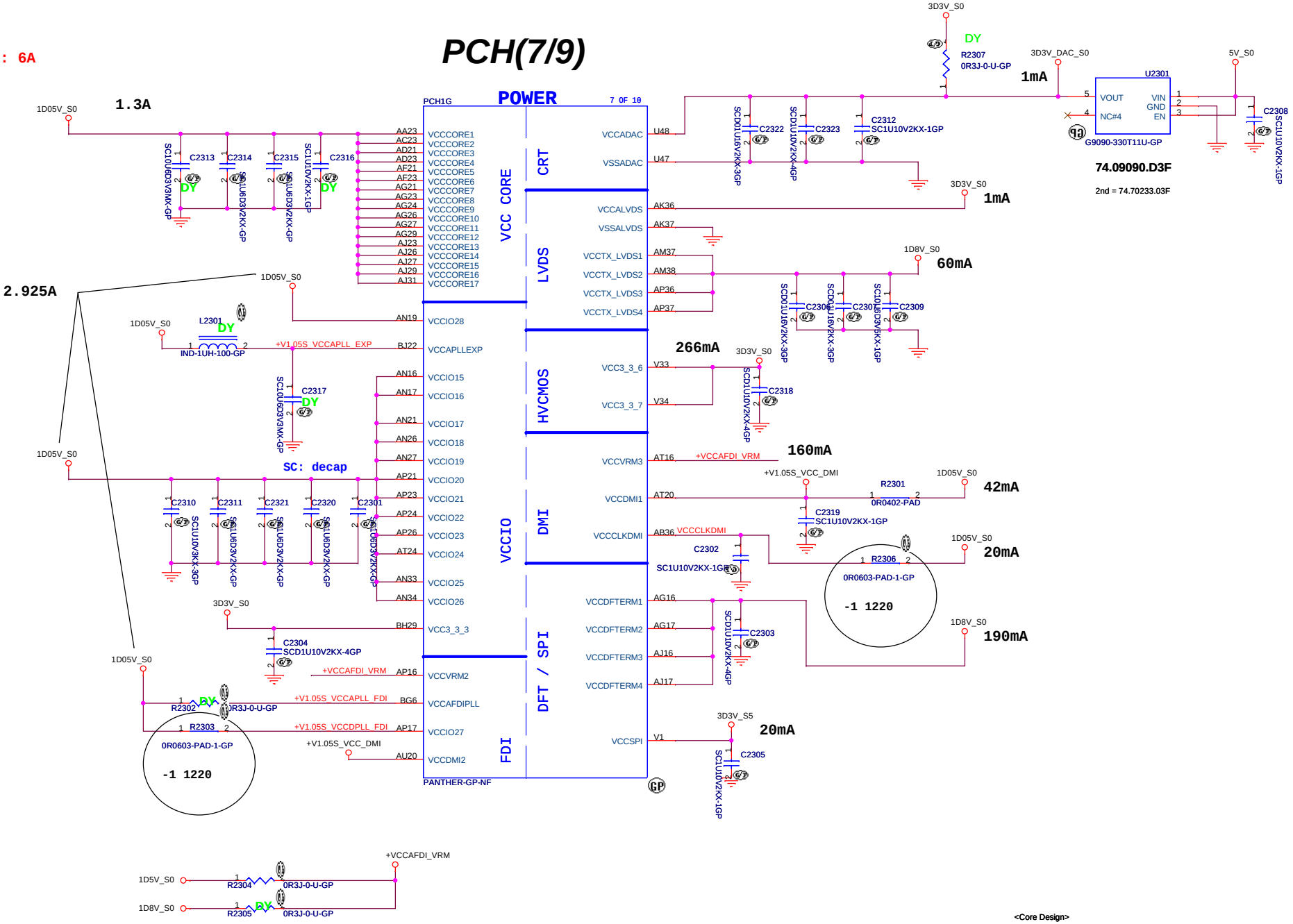
Title: PCH(6/9): GPIO/NTCF/RSVD

Size: A3 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

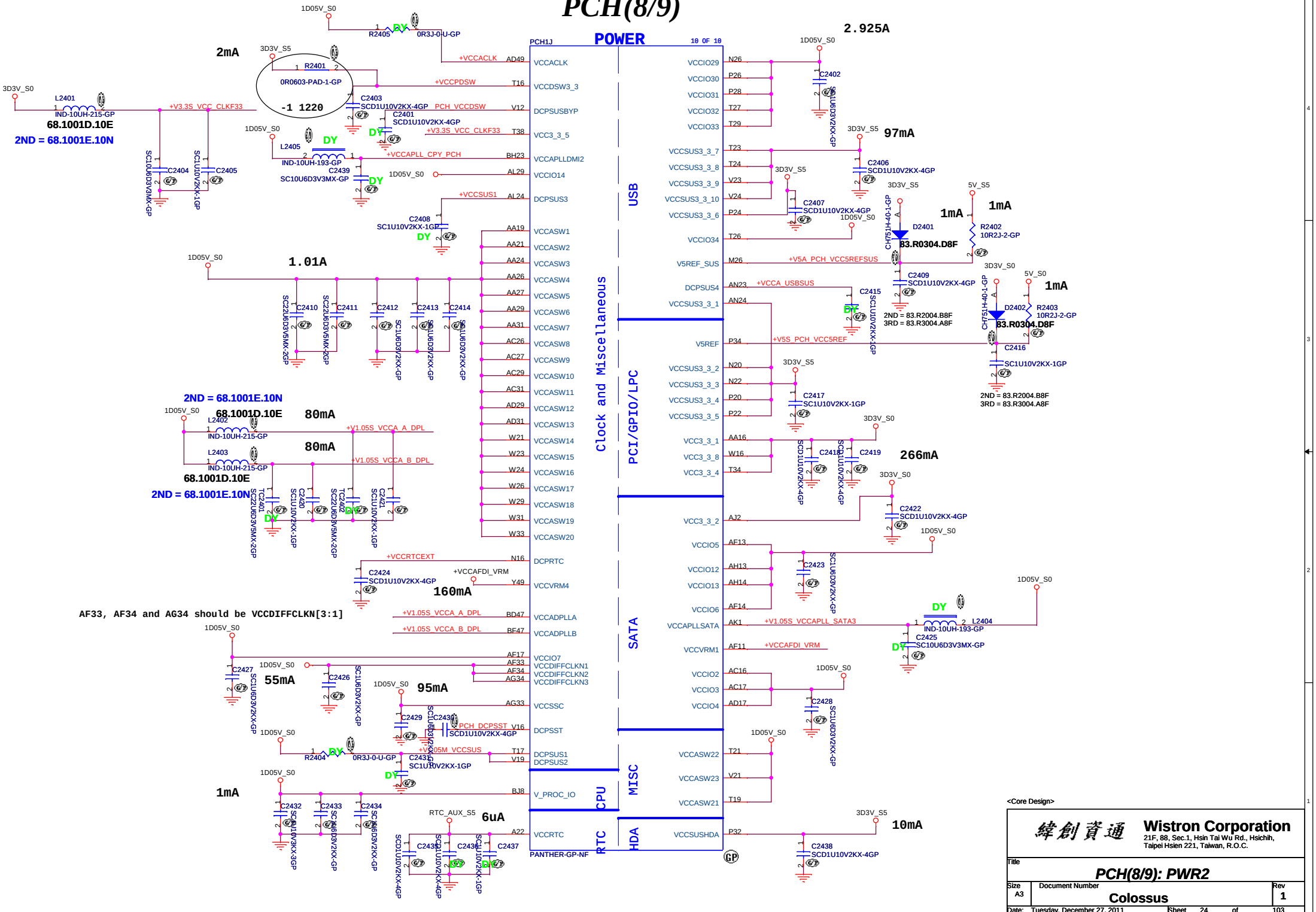
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(7/9): PWR1

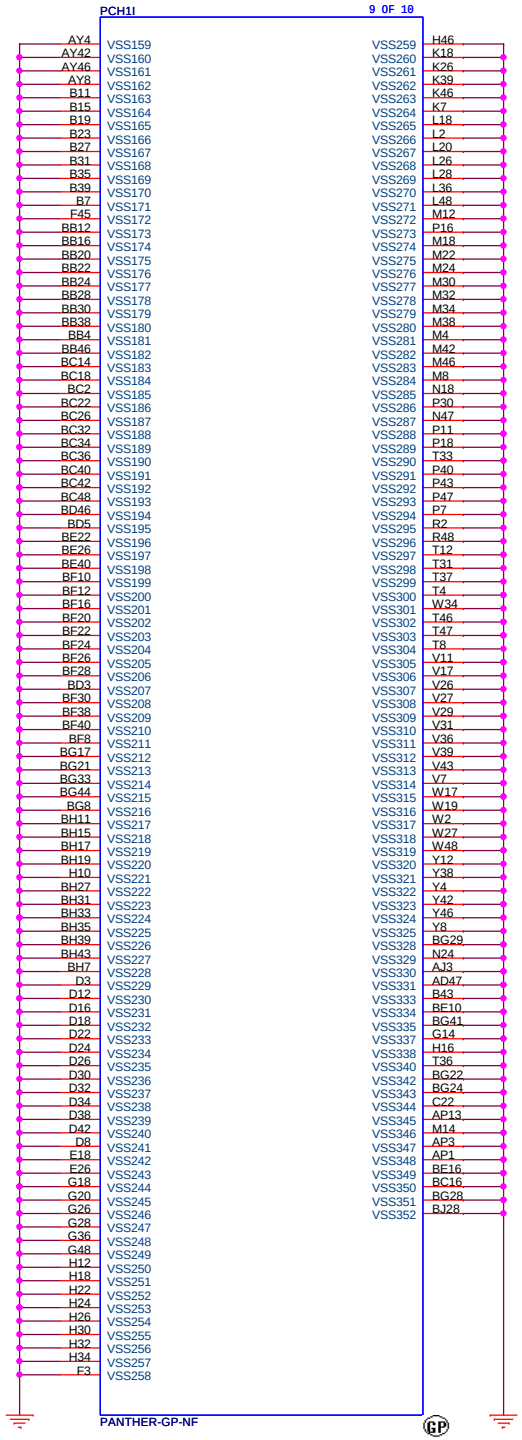
Size	Document Number	Rev
A3	Colossus	1

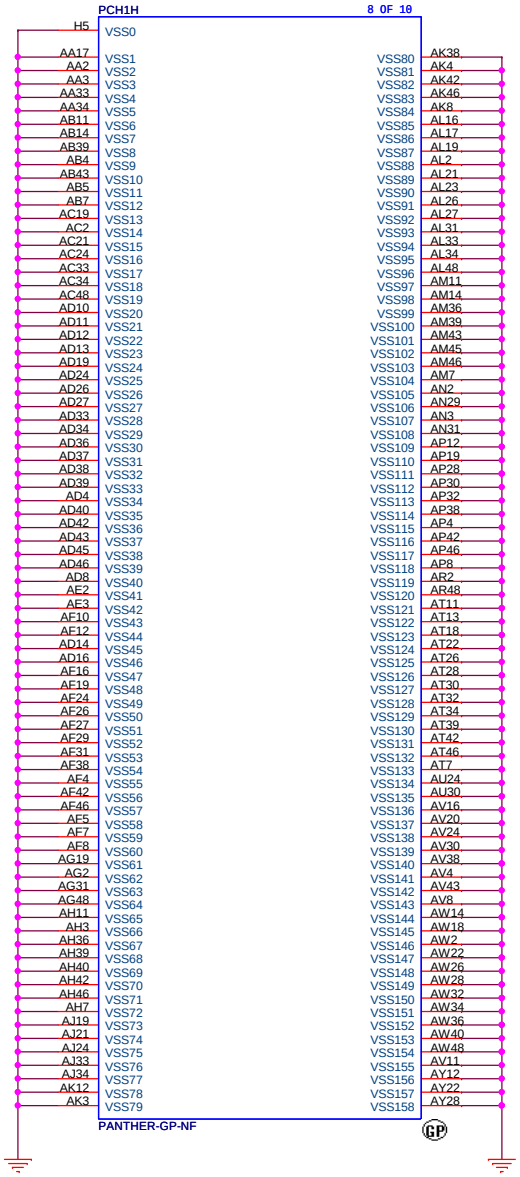
Date: Monday, December 26, 2011 Sheet 23 of 103

PCH(8/9)


POWER
10 OF 10
PCH1J
PANTHER-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
2.925A
2mA
1.01A
80mA
80mA
160mA
55mA
95mA
1mA
6uA
97mA
1mA
1mA
266mA
10mA
68.1001D.10E
2ND = 68.1001E.10N
AF33, AF34 and AG34 should be VCCDIFFCLKN[3:1]
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH(8/9): PWR2
Size A3
Document Number
Colossus
Rev 1
Date: Tuesday, December 27, 2011
Sheet 24 of 103

PCH(9/9)





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(9/9): GND**

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 25 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***PCH XDP***	
Size: A3	Document Number: **Colossus**	Rev: 1
Date: Monday, December 26, 2011	Sheet 26 of 103	

SSID = KBC

U2701

20110608 for vendor debug

KB90160F-A3-GP
71.09016.B0G

3RD = 84.2N702.W31
2ND = 84.07002.I31
84.2N702.J31
Q2703
2N7002K-2-GP

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

MODEL ID

Model_ID	Model_ID (SI2)	Pull-Low Register	Pull-High Register	Typical Voltage
Goya(15.6")	UMA	UMA (35W)	100.0 K	10.0 K	3.000 V
	UMA	UMA (45W)	100.0 K	20.0 K	2.750 V
Goya(15.6")	DIS	DIS GL (35W)	100.0 K	33.0 K	2.481 V
	DIS	DIS GL (45W)	100.0 K	47.0 K	2.245 V
Balen(17.3")	UMA	UMA (35W)	100.0 K	64.9 K	2.001 V
Balen(17.3")	DIS	DIS GL (35W)	100.0 K	76.8 K	1.867 V
Balen(17.3")	reserved for project u	DIS GL (45W)	100.0 K	100.0 K	1.650 V
Balen(17.3")	reserved for project u	DIS GT (35W)	100.0 K	143.0 K	1.358 V
Balen(17.3")	reserved for project u	DIS GT (45W)	100.0 K	174.0 K	1.204 V
Balen(17.3")	reserved for project u	UMA (45W)	100.0 K	215.0 K	1.048 V
Goya(15.6")	reserved for project u	DIS GT (35W)	100.0 K	237.0 K	0.979 V
Goya(15.6")	reserved for project u	DIS GT (45W)	100.0 K	261.0 K	0.914 V

83.00355.F1F

Prevent BIOS data loss solution

Q2701 MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11

GPIO06-->PWRBTN

HP Limit Signal Detect

D2701 BAV99PT-GP-U
83.00099.K11
2ND = 83.00099.M11
3RD = 83.00099.T11

HP AIRLINE COMBO

EC GPIO standard PH/PL

RN2701 SRN4K7J-8-GP

RN2713 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

GPIO70-->PWR_CHG_ACOK# OW active

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

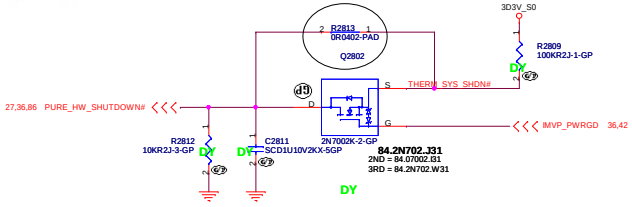
Title: EC CONTROLLER

Size: A2 | Document Number: Colossus | Rev: 1

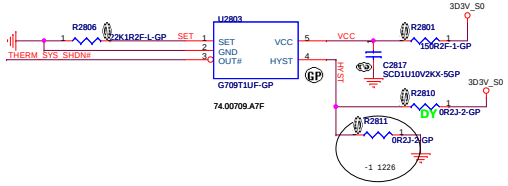
Date: Thursday, January 05, 2012 | Sheet 27 of 103

$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

where T is the trip temperature in Centigrade. R_{SET} is the set- point resistance.



90 C

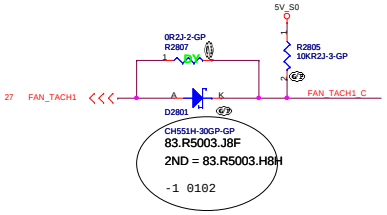


Global Mixed-mode Technology Inc. **G709/G710**

Pin Description

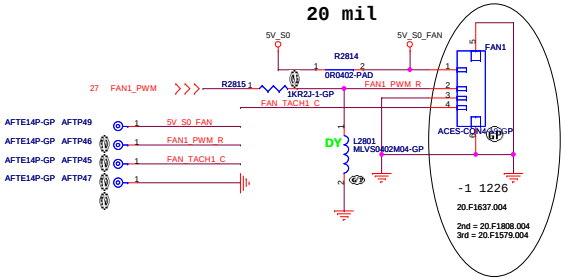
PIN		NAME	FUNCTION
G709	G710		
1	1	SET	Temperature Set Point, Connect an external 1% resistor from SET to GND to set trip point.
2	2	GND	Ground
3	3	$\overline{OT}$	Open-Drain Active Low Output.
4	4	HYST	Hysterisis Selection. Hysterisis is 10°C for HYST = V_{CC}, 2°C for HYST = GND.
	5	N.C.	Not Connected.
5	6	VCC	Power-Supply Input.

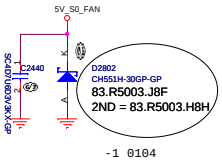
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V_{IH}		0.7 x V_{CC}	---	---	V
	V_{IL}		---	---	0.3 x V_{CC}	V



FOR PWM FAN

20 mil





<Core Design>

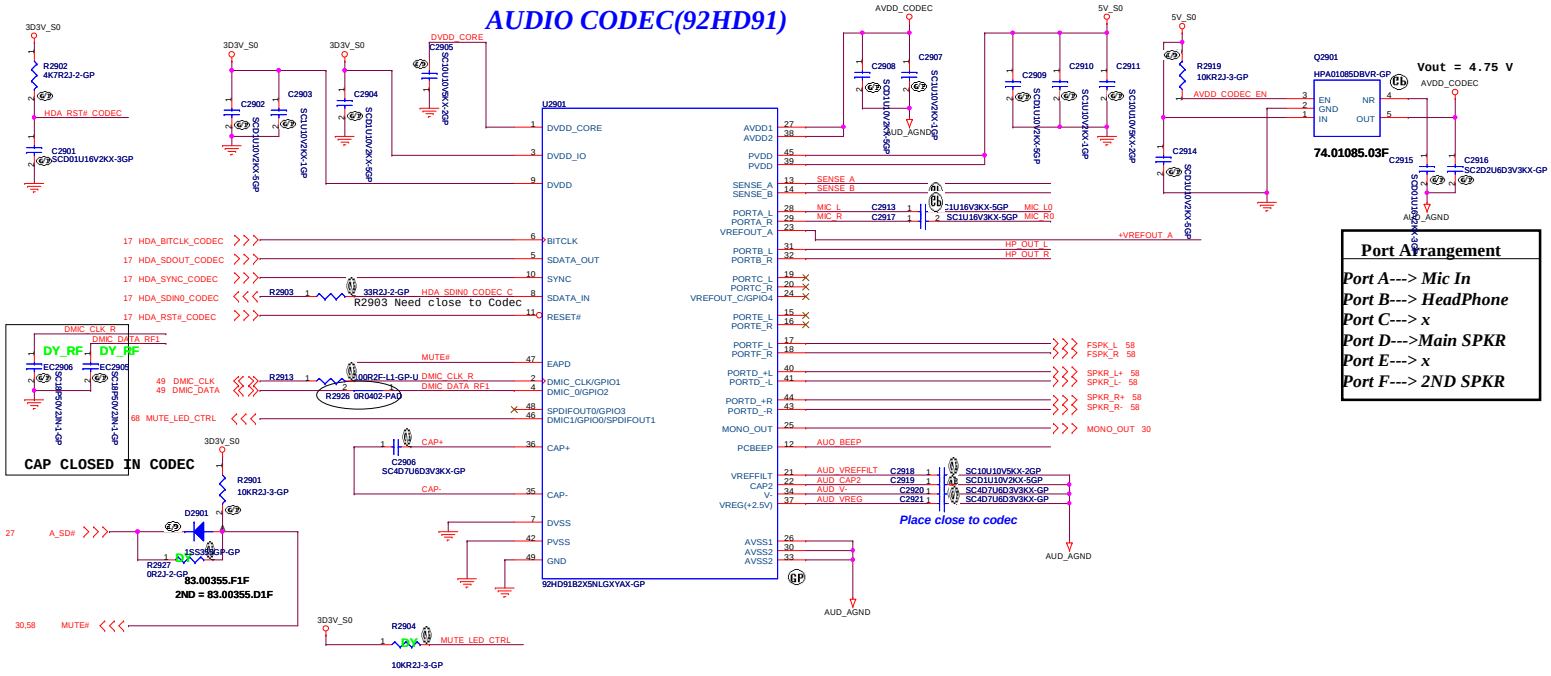
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/FAN*

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 28 of 103

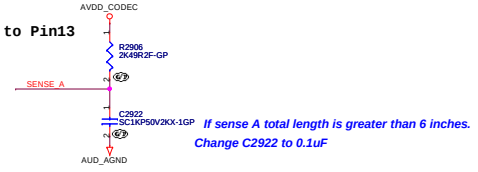
AUDIO CODEC(92HD91)



SENSE Detect

Headphone Trace = 15mil

Close to Pin13



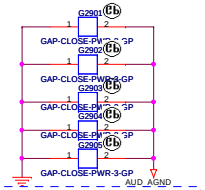
If sense A total length is greater than 6 inches.
Change C2922 to 0.1uF

Close to Pin14

Digital GND & AUD_AGND

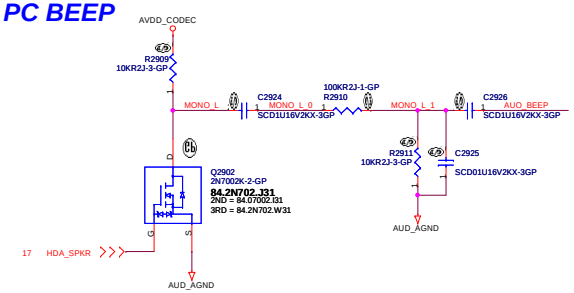
Tie Analog GND and Digital GND under codec by a single point

0818 IDT request
Place under U2901



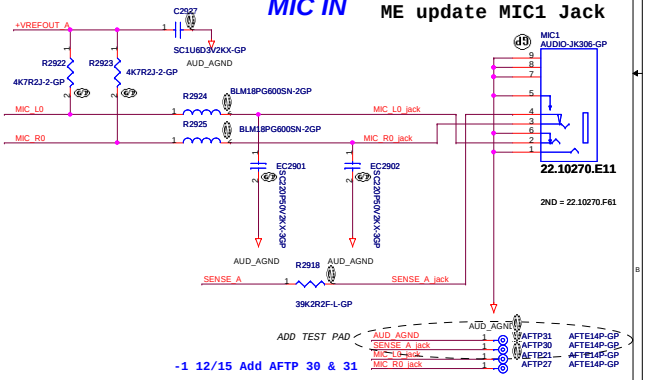
audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



MIC IN

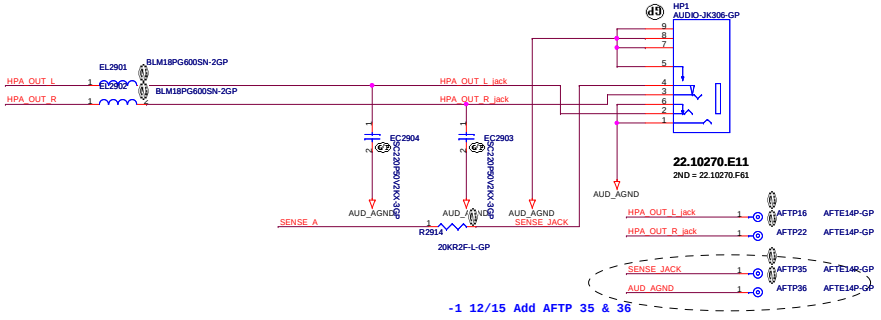
ME update MIC1 Jack



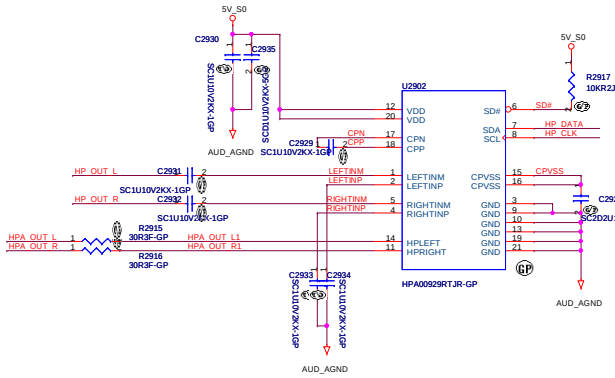
-1 12/15 Add AFTP 30 & 31

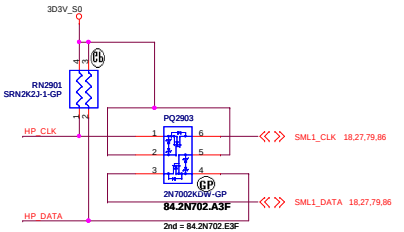
HeadPhone

ME update HP1 Jack



-1 12/15 Add AFTP 35 & 36





<Core Design>

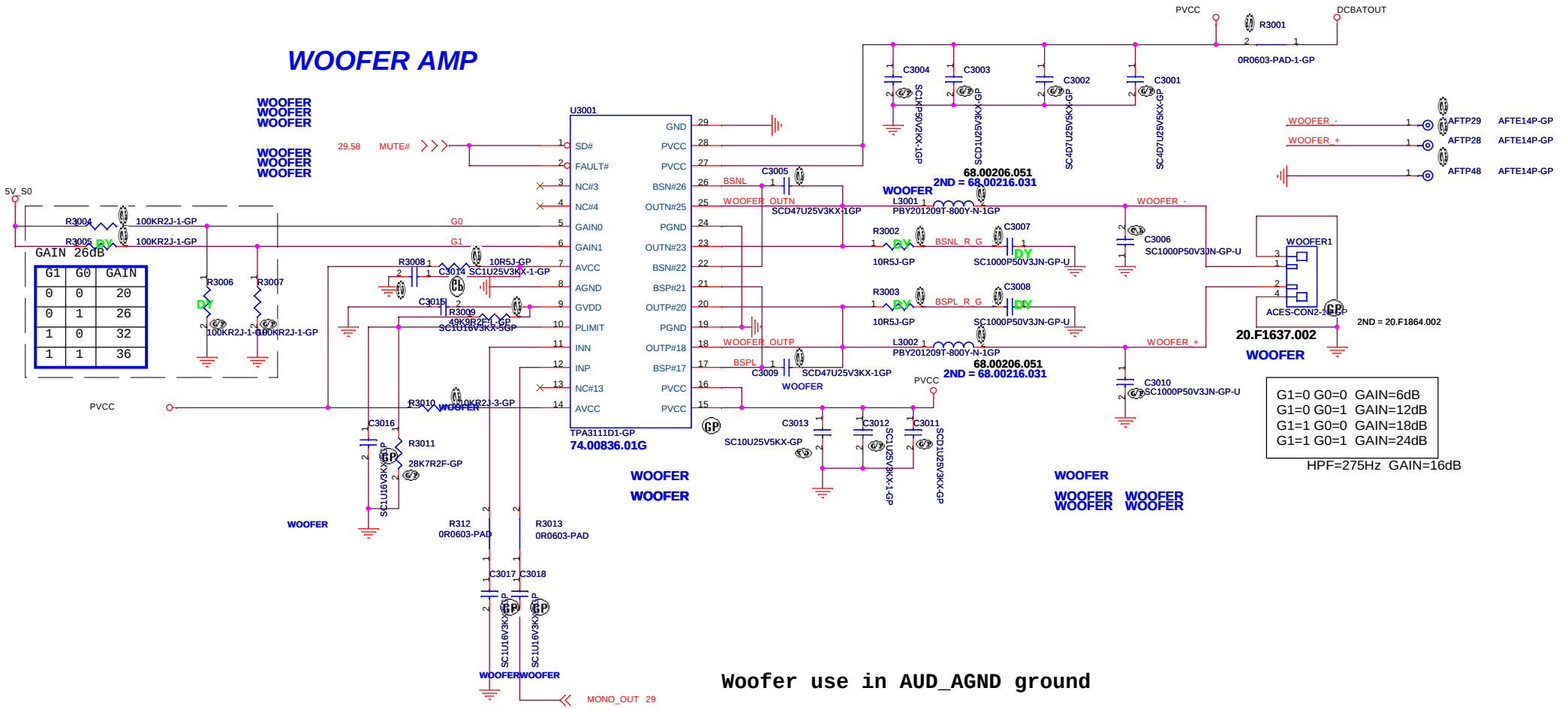
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD91/HeadphoneAMP

Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 29 of 103

WOOFER AMP



Woofer use in AUD_AGND ground

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

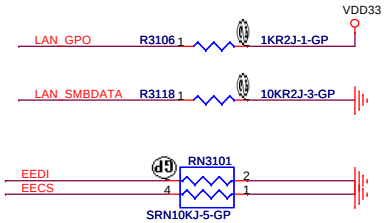
Title: ***Audio AMP SPK/WOOFER***

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 30 of 103

LAN CHIP-RTL8111F

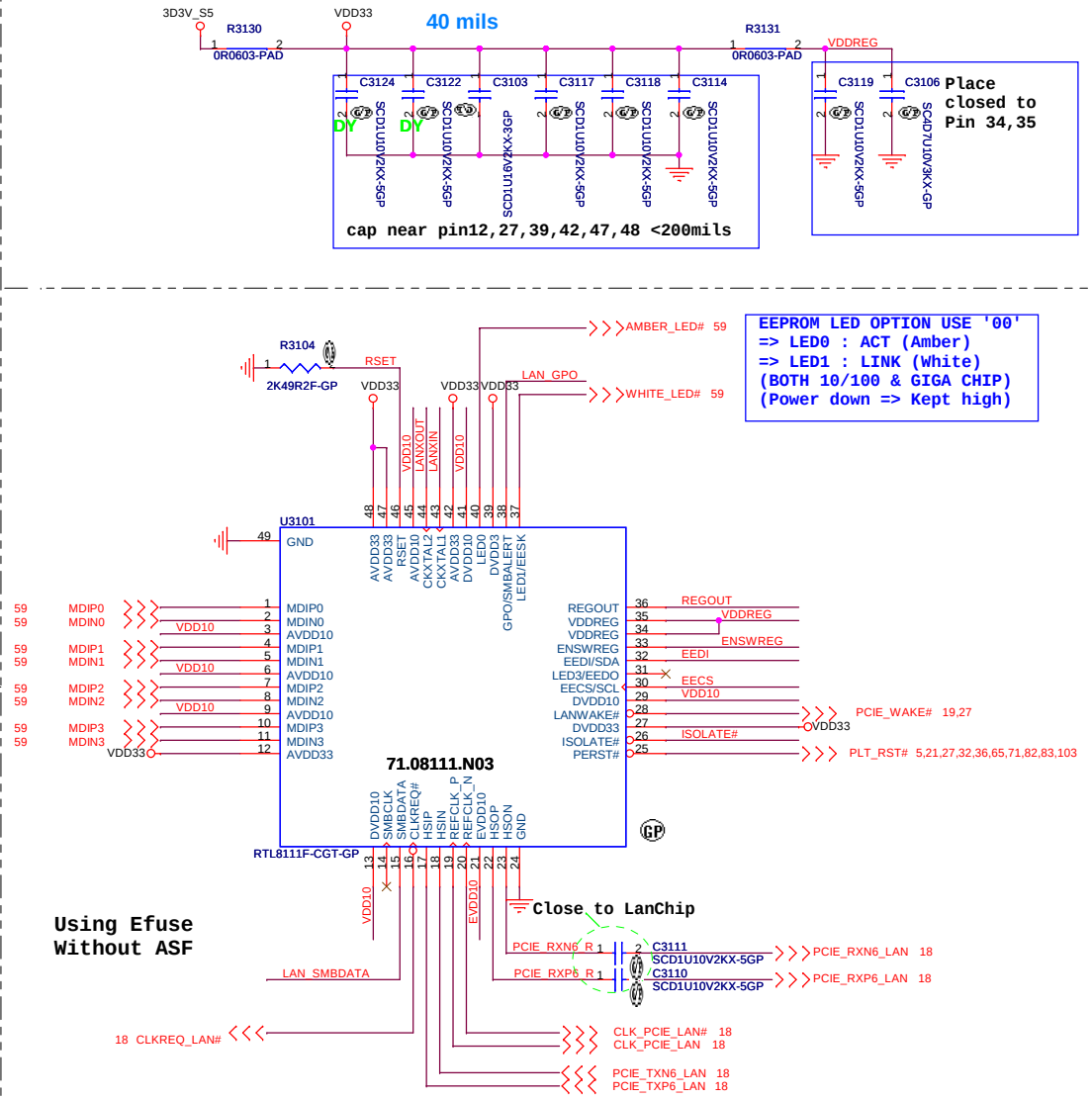
USE EFuse No ASF



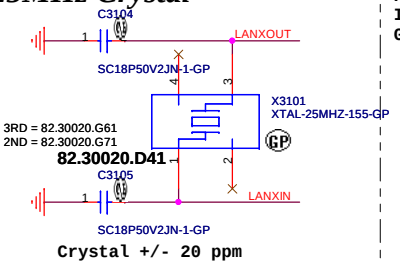
Avoid Leakage

LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



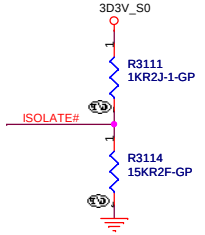
25MHz Crystal



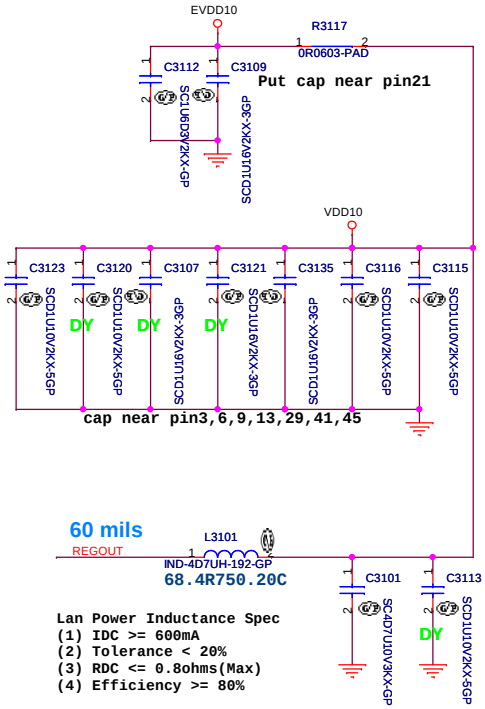
Crystal +/- 20 ppm

KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

Isolate Strap Pin

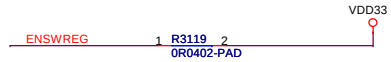


Regout power plane(1D05V)



Put 4D7U L + 22U cap near pin36 <200mils
(2nd = 78.22610.81L)

Regout Switch



ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

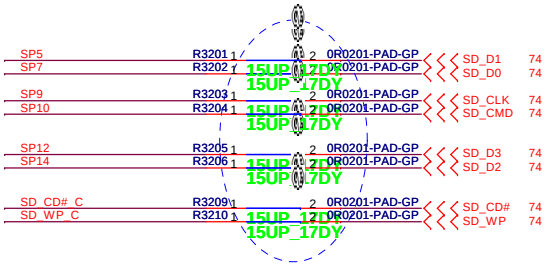
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111F
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 31 of 103

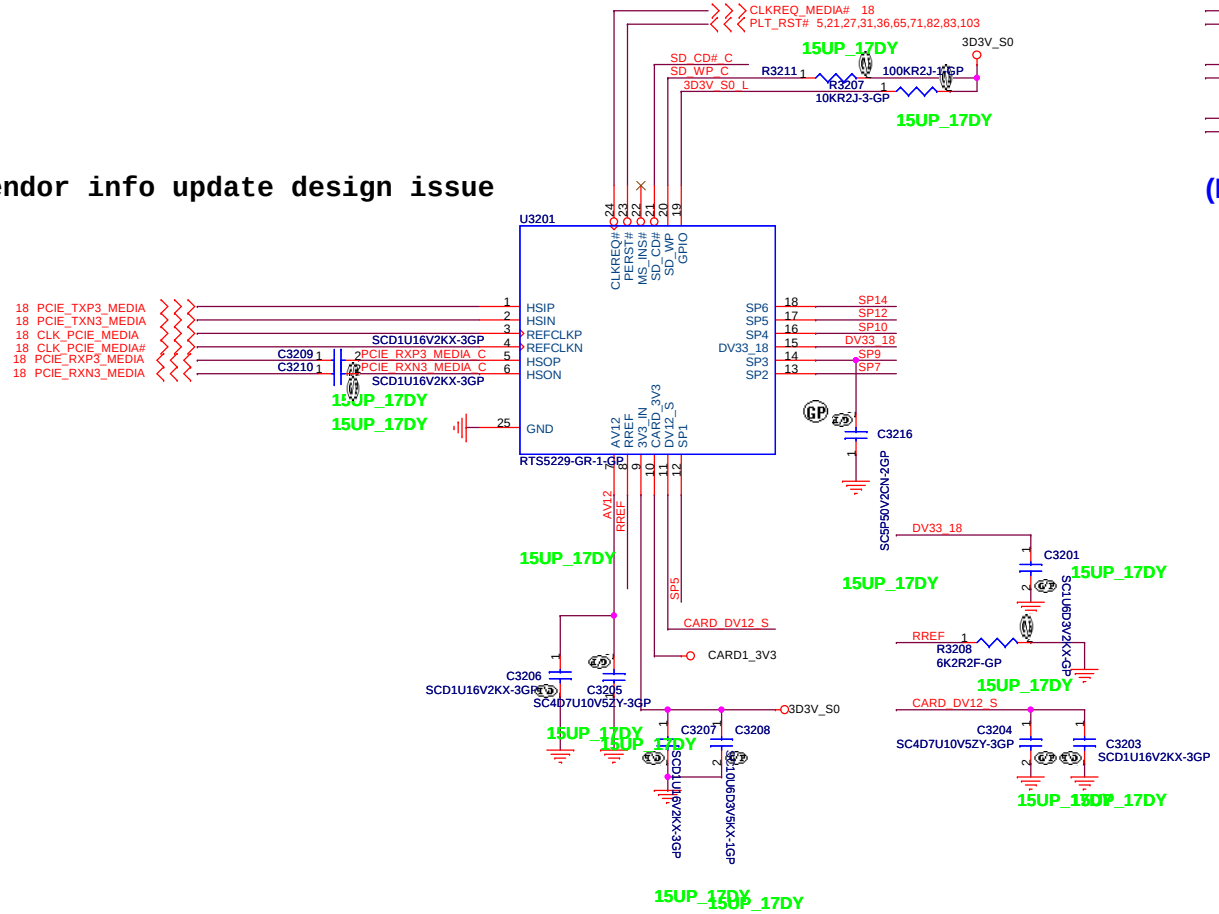
RTS5229

-1 12/15 0201 0 Ohm change to short pad



Vendor info update design issue

(RTS5229)U3201 closed near



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-RTS5229***

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 32 of 103

(Blanking)

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 34 of 103

(Blanking)

<Core Design>

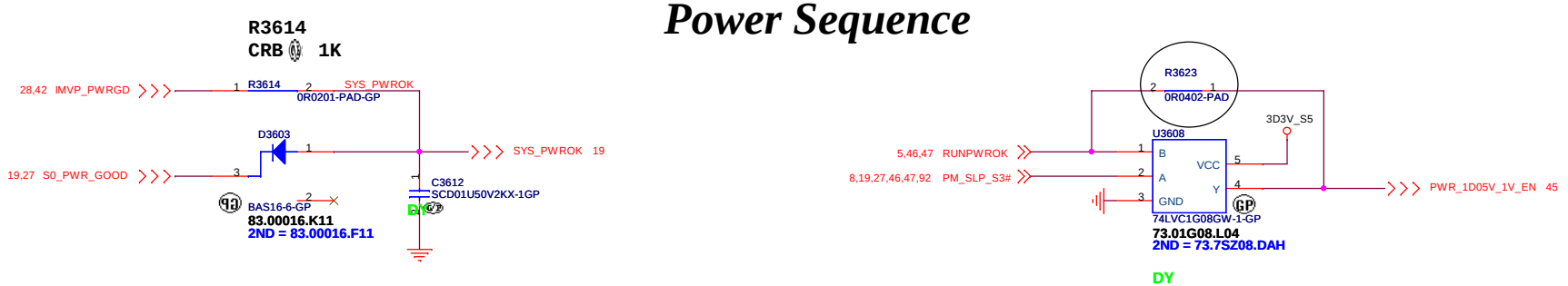
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

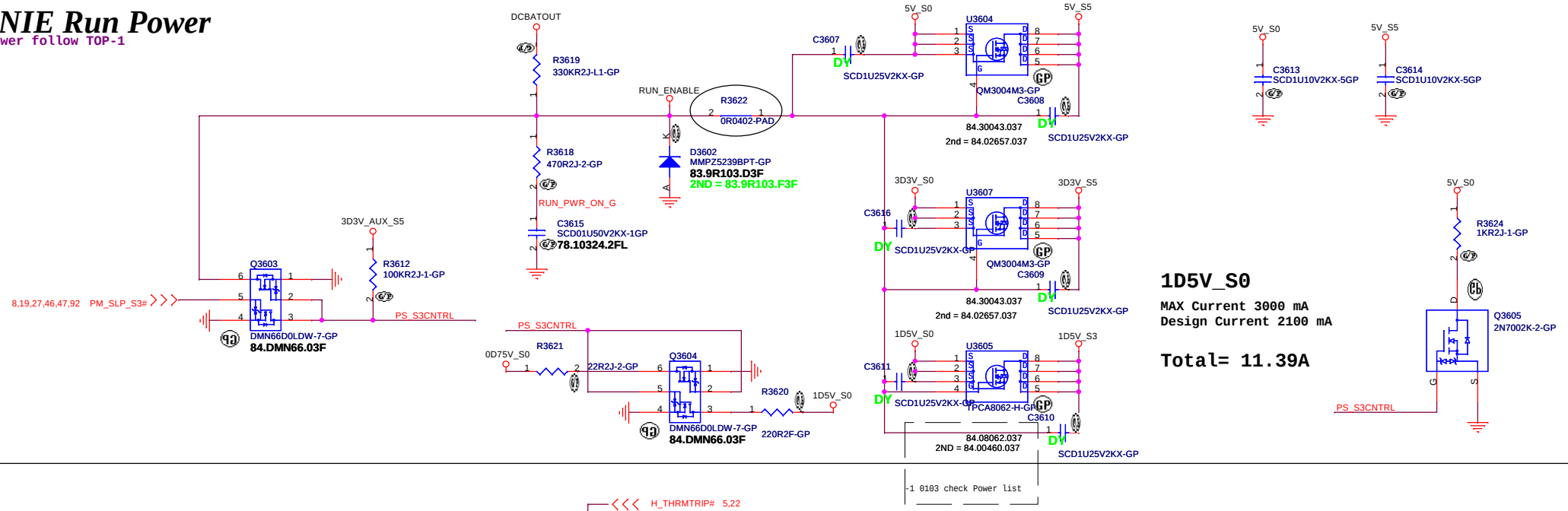
Date: Monday, December 26, 2011 Sheet 35 of 103

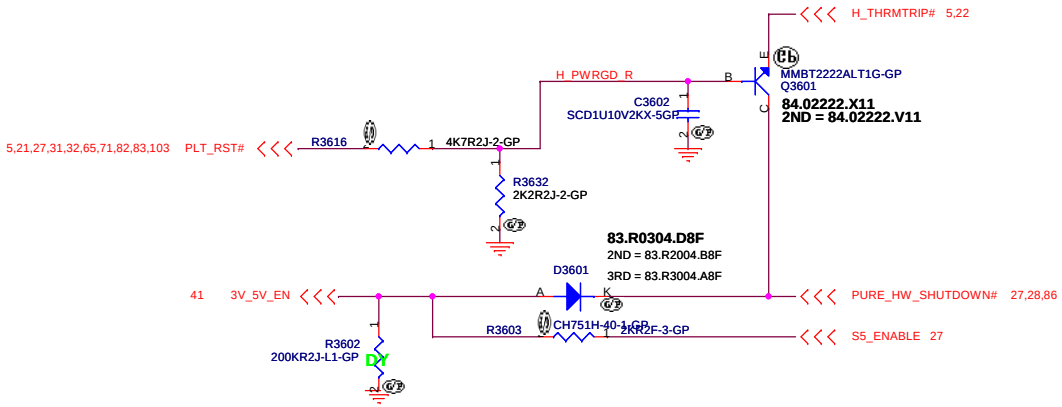
Power Sequence



ANNIE Run Power

Run power follow TOP-1





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 36 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

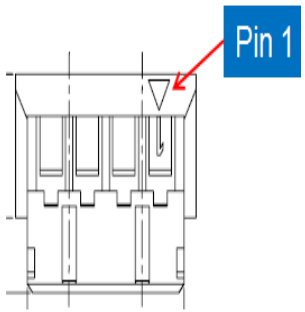
Title: ADAPTER

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 37 of 103

Adaptor in to generate DCBATOUT

Pin	Description	Wire color
Pin 1	White LED	White
Pin 2	Amber LED	Yellow
Pin 3	ID	Brown
Pin 4	GND	Black
Pin 5	GND	Black
Pin 6	GND	Black
Pin 7	-	
Pin 8	+VA	Red
Pin 9	+VA	Red
Pin 10	+VA	Red



-1 1222 PR3802 to save 100mW when battery full.

AC Present = White
Standby = White pulsing
Charging = Amber
***LED's are off if no AC jack pluged in**

-1 1222 PR3802 to save 100mW when battery full.

<Core Design>

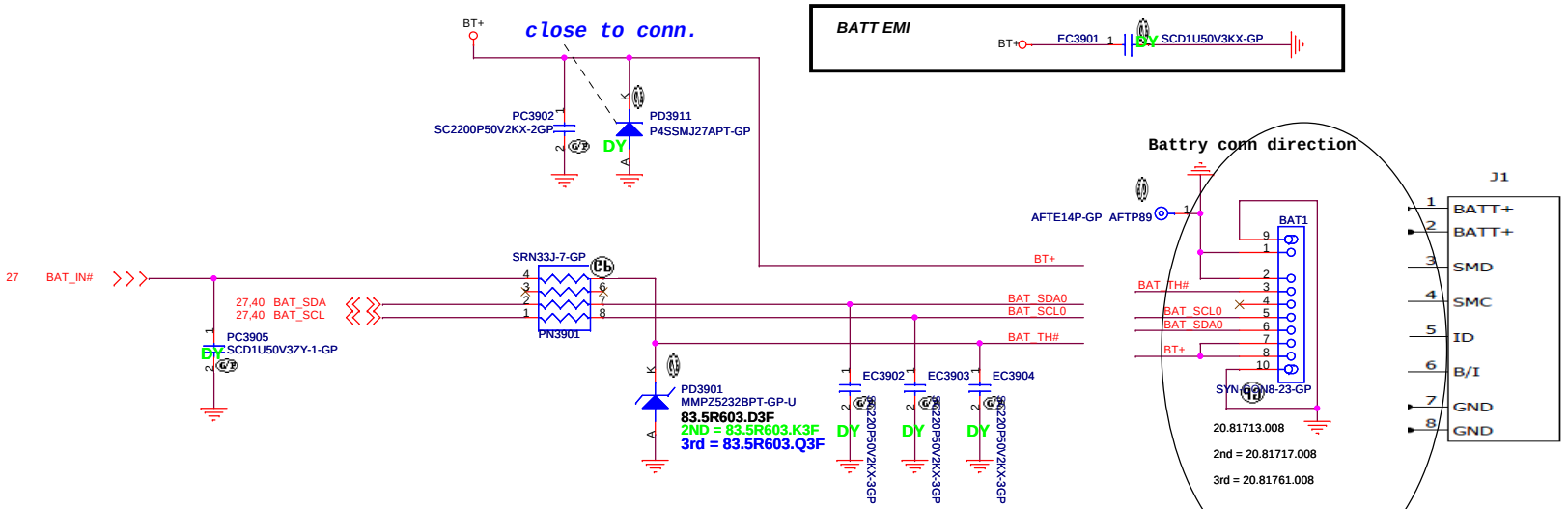
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

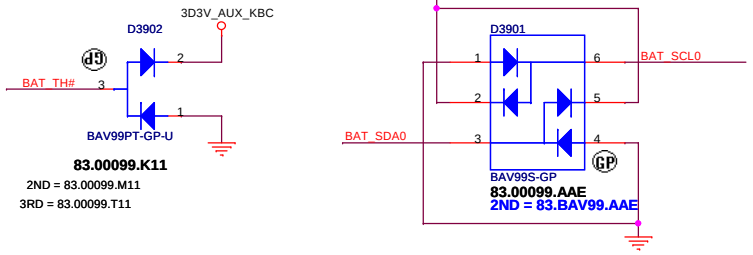
Title: DCIN JACK

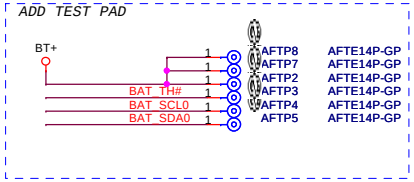
Size: A4 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 38 of 103

BATT Connector



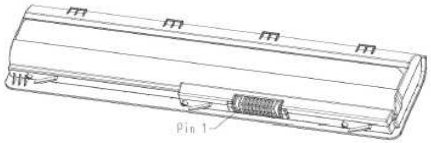




3. Interface

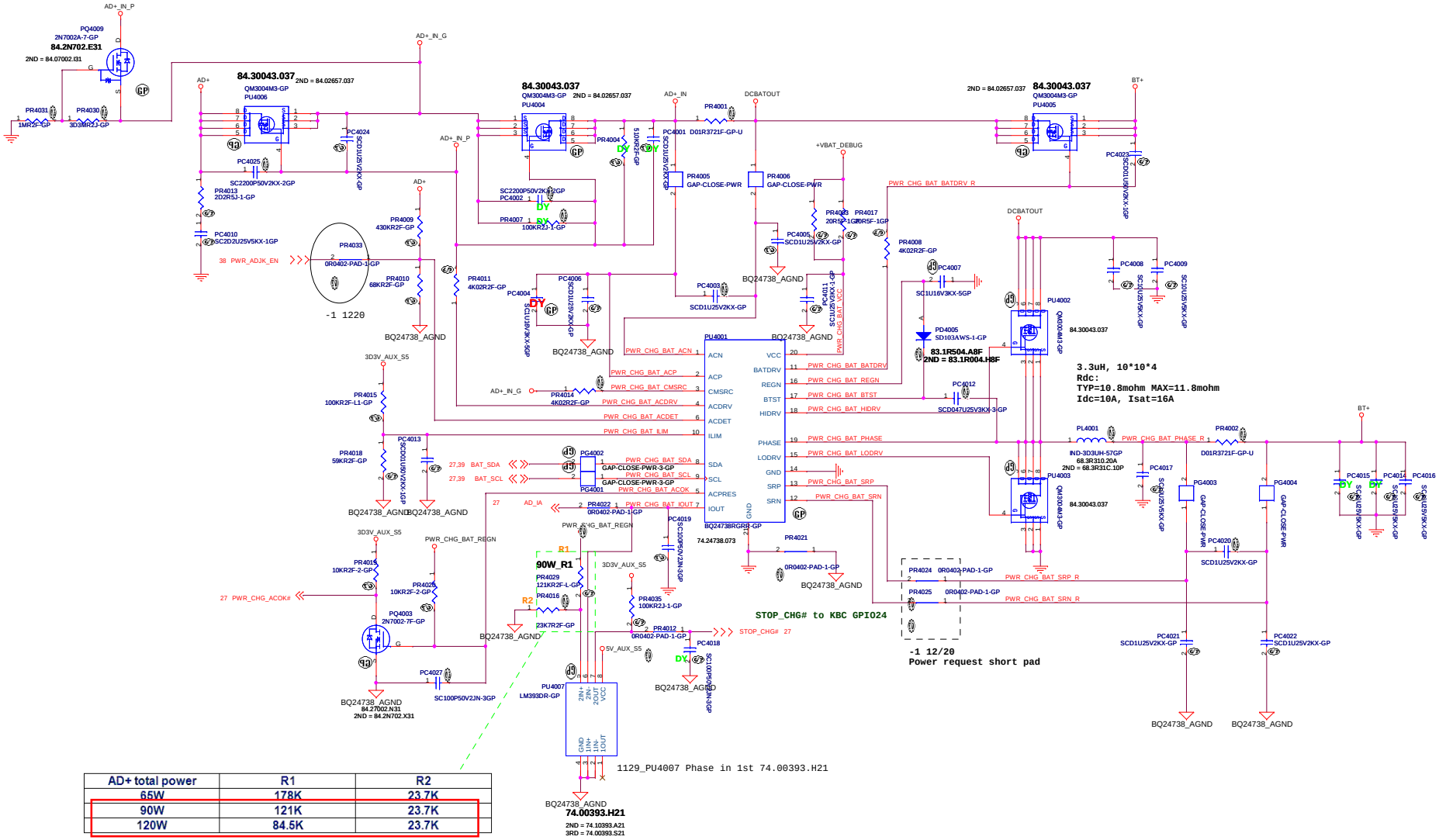
Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 39 of 103	



AD+ total power	R1	R2
65W	178K	23.7K
90W	121K	23.7K
120W	84.5K	23.7K

<Core Design>

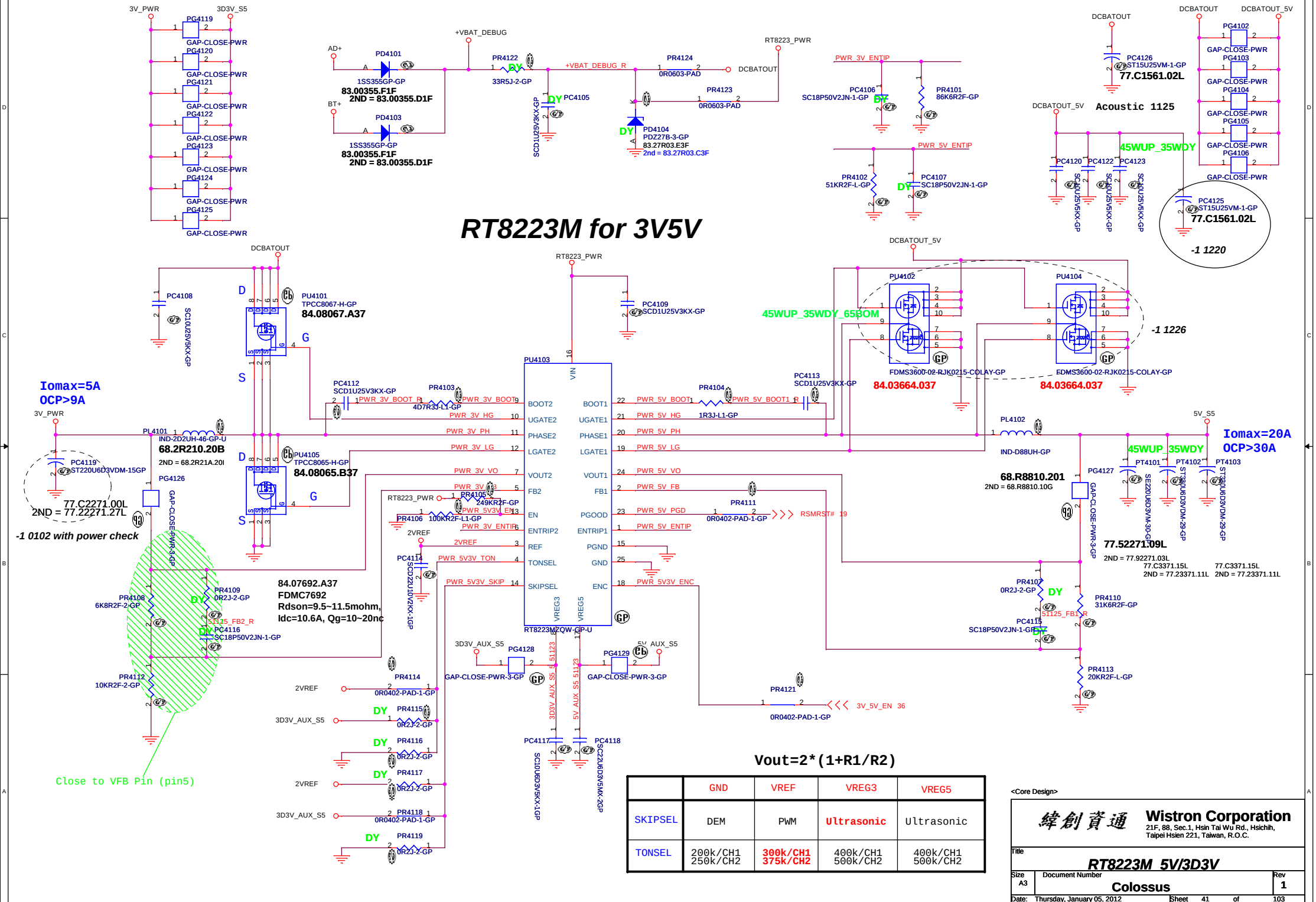
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24738

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 40 of 103

RT8223M for 3V5V



	GND	VREF	VREG3	VREG5
SKIPSEL	DEM	PWM	**Ultrasonic**	Ultrasonic
TONSEL	200k/CH1 250k/CH2	**300k/CH1** **375k/CH2**	400k/CH1 500k/CH2	400k/CH1 500k/CH2

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223M 5V/3D3V**

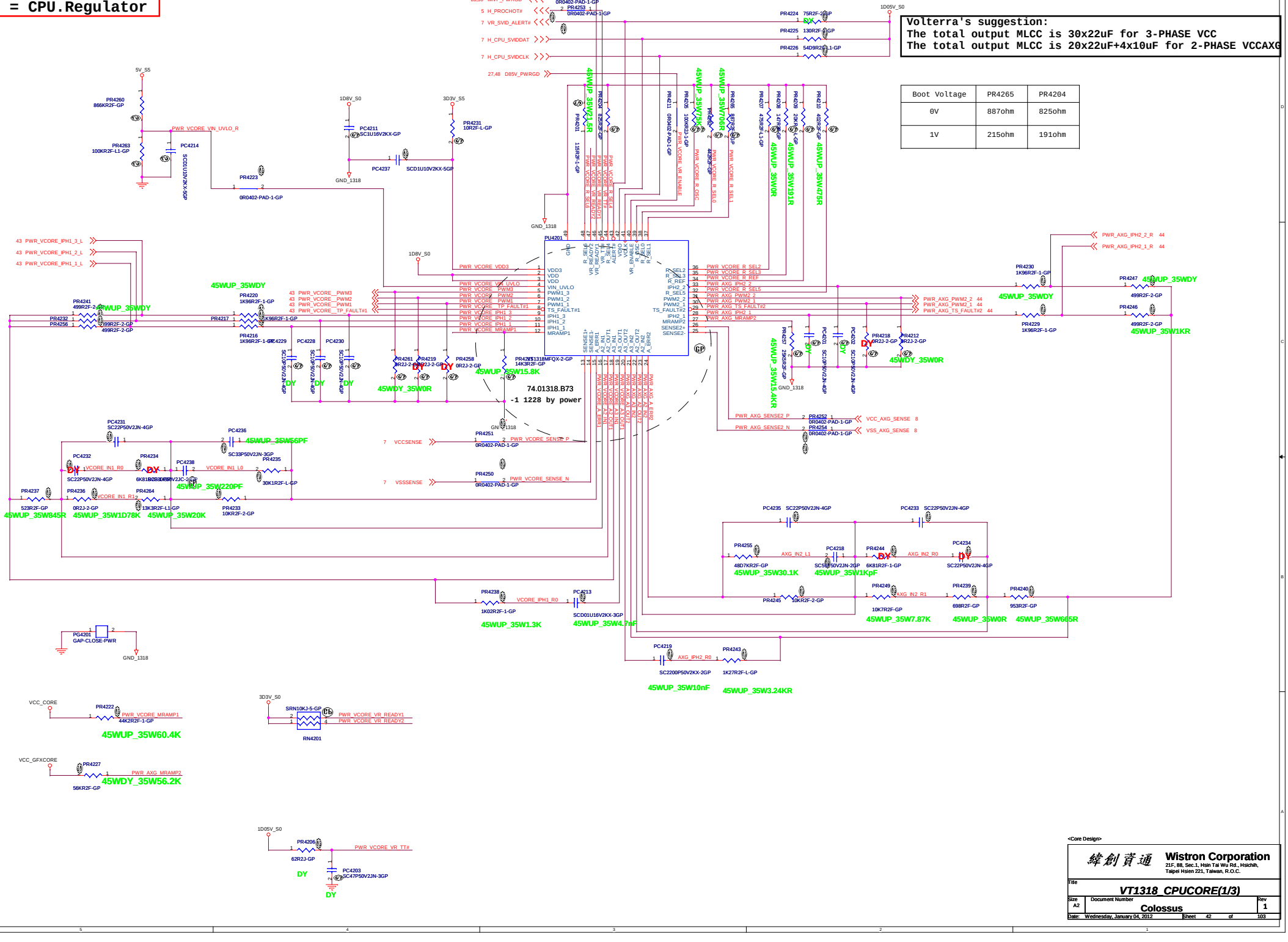
Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 41 of 103

SSID = CPU.Regulator

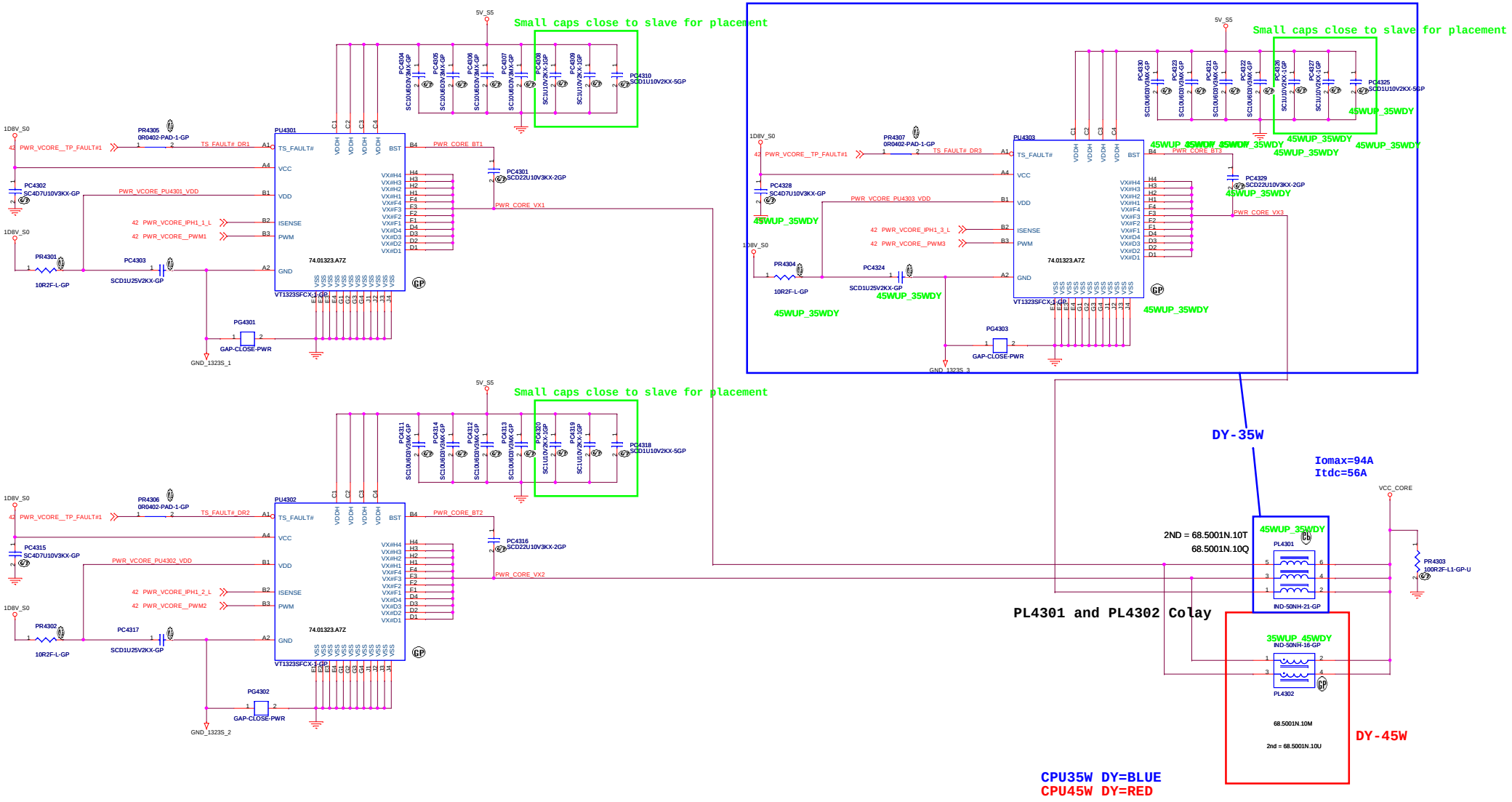
Volterra's suggestion:
The total output MLCC is 30x22uF for 3-PHASE VCC
The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318_CPUCORE(1/3)
Size: A2 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 42 of 103



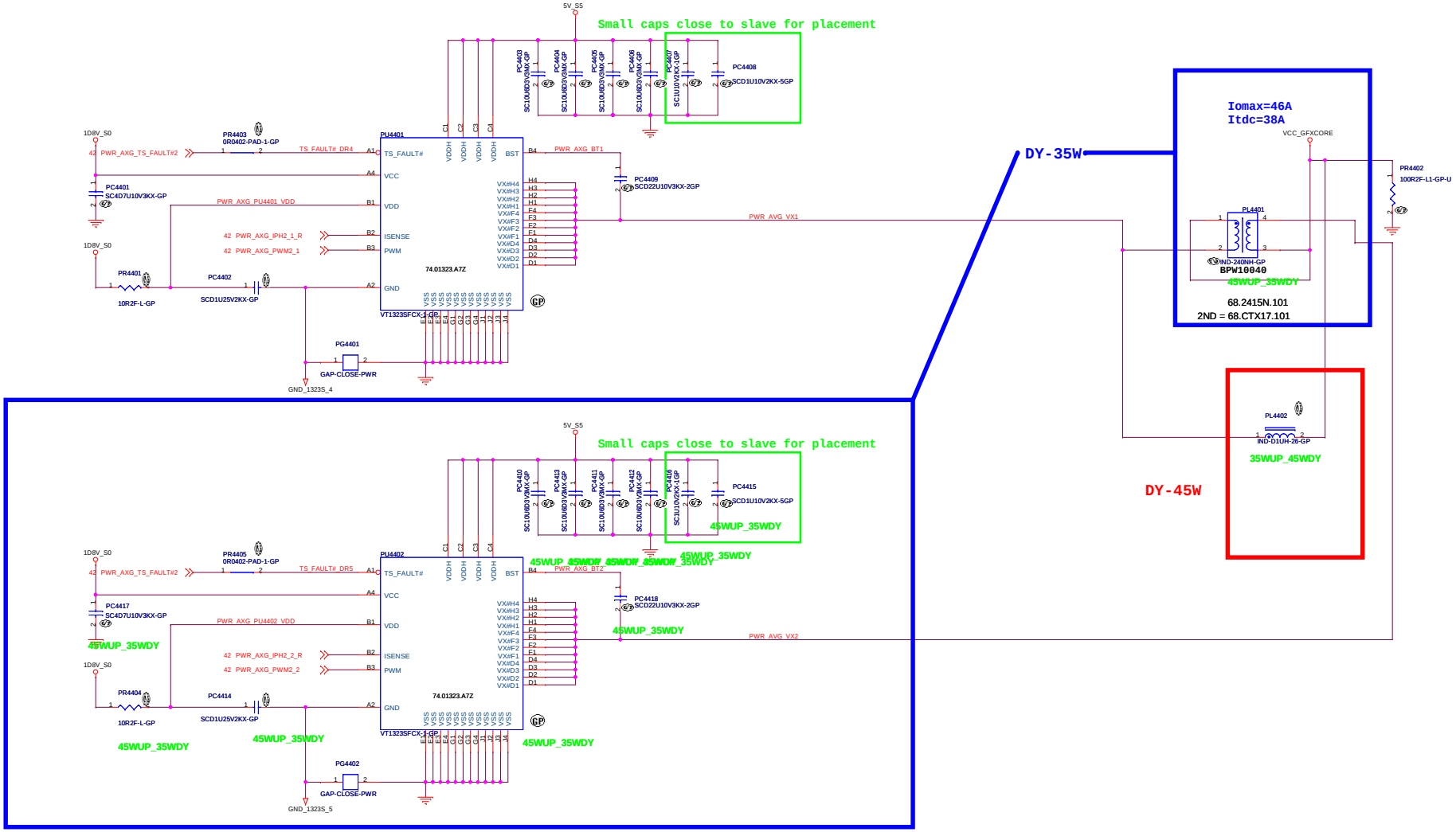
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323_CPUCORE(2/3)

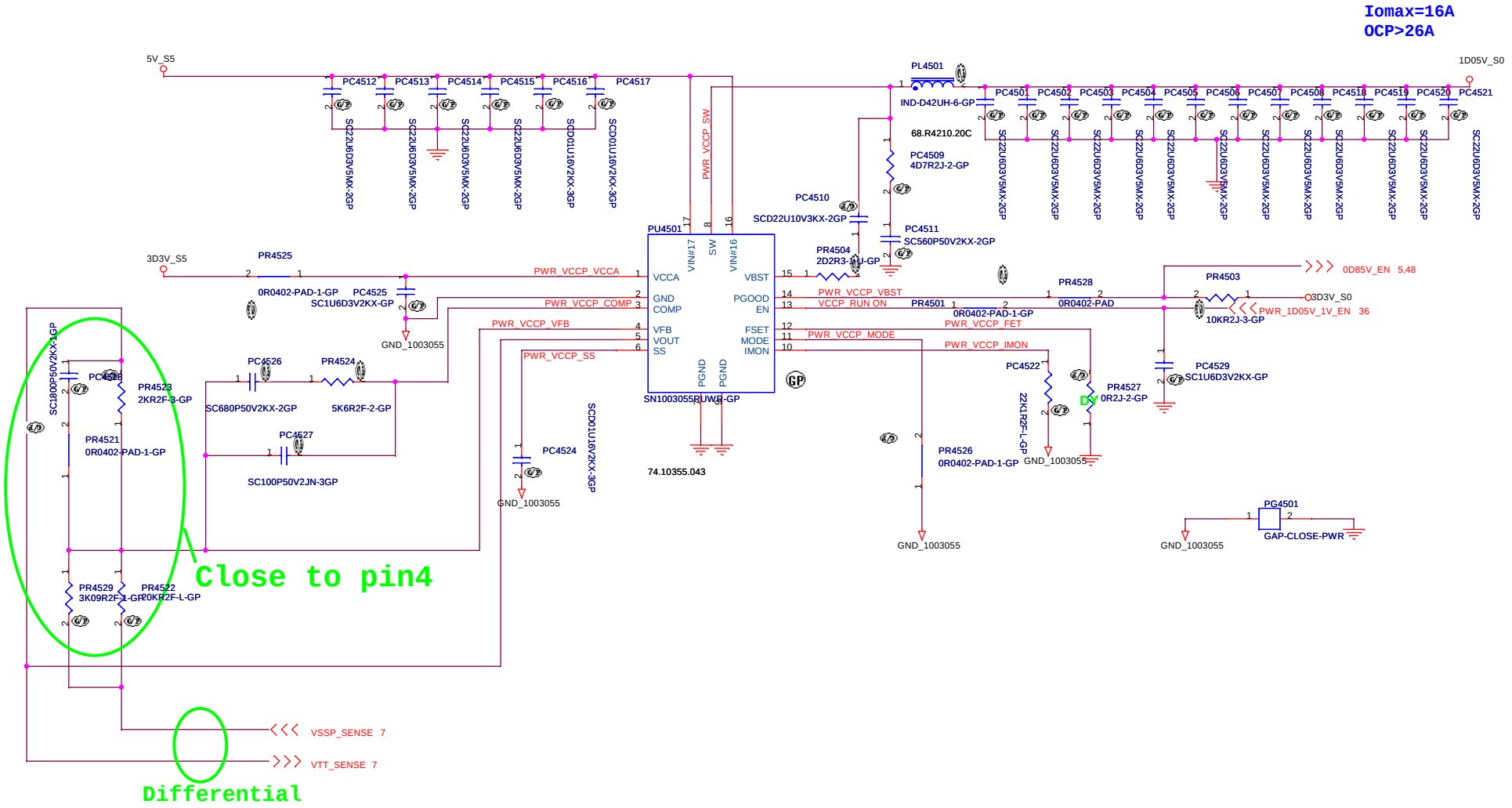
Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 43 of 103



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VT1323_CPUCORE(3/3)
Size: A2	Document Number: Colossus
Rev: 1	
Date: Wednesday, January 04, 2012	Sheet 44 of 103



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SN1003055RUWR

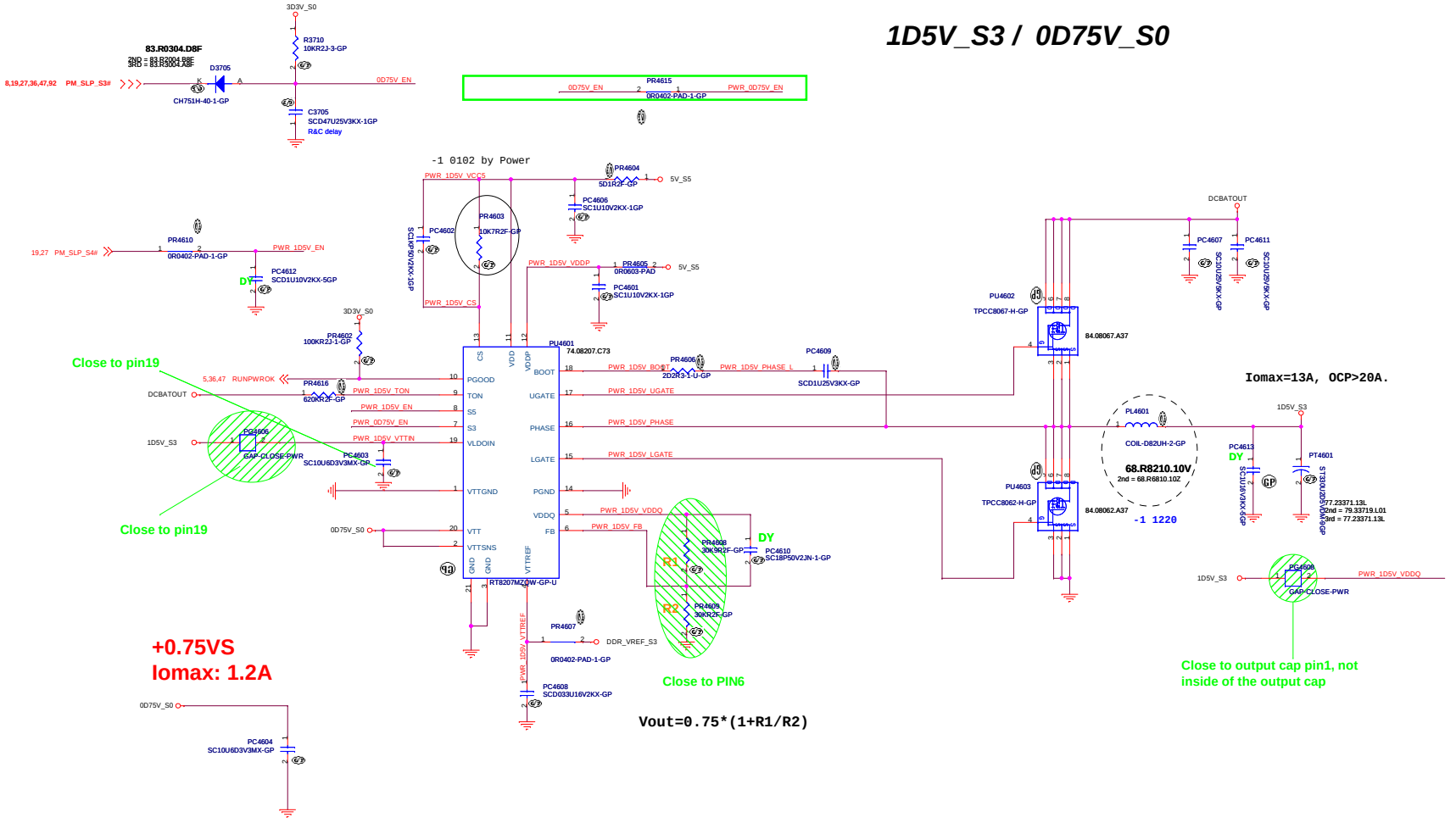
Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v

⑤

1D5V_S3 / 0D75V_S0



<Core Design>

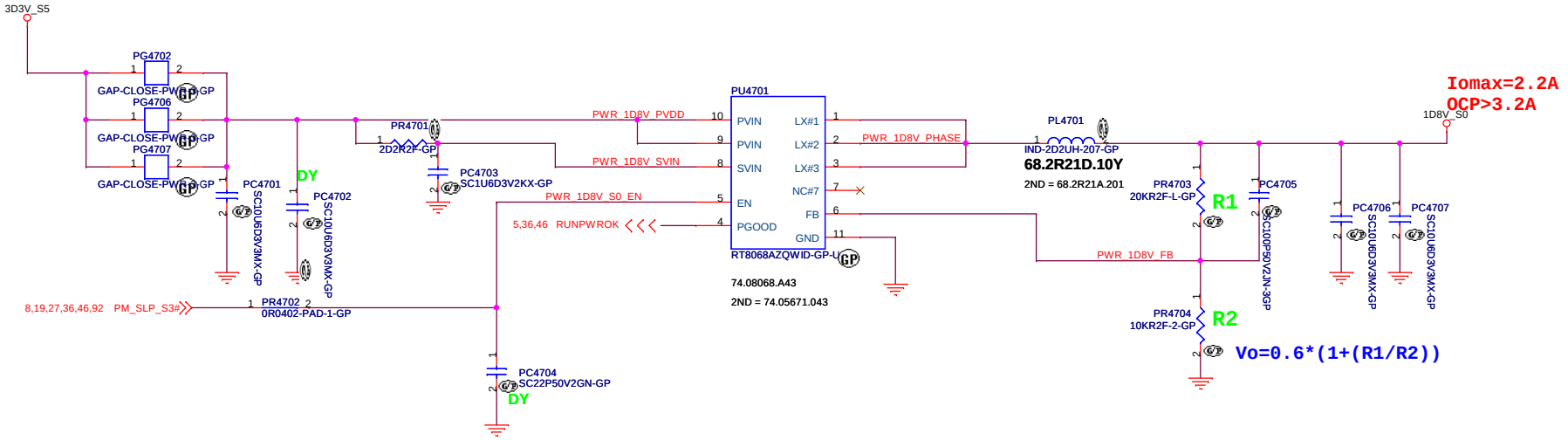
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207MZ_1D5V & 0D75V

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0

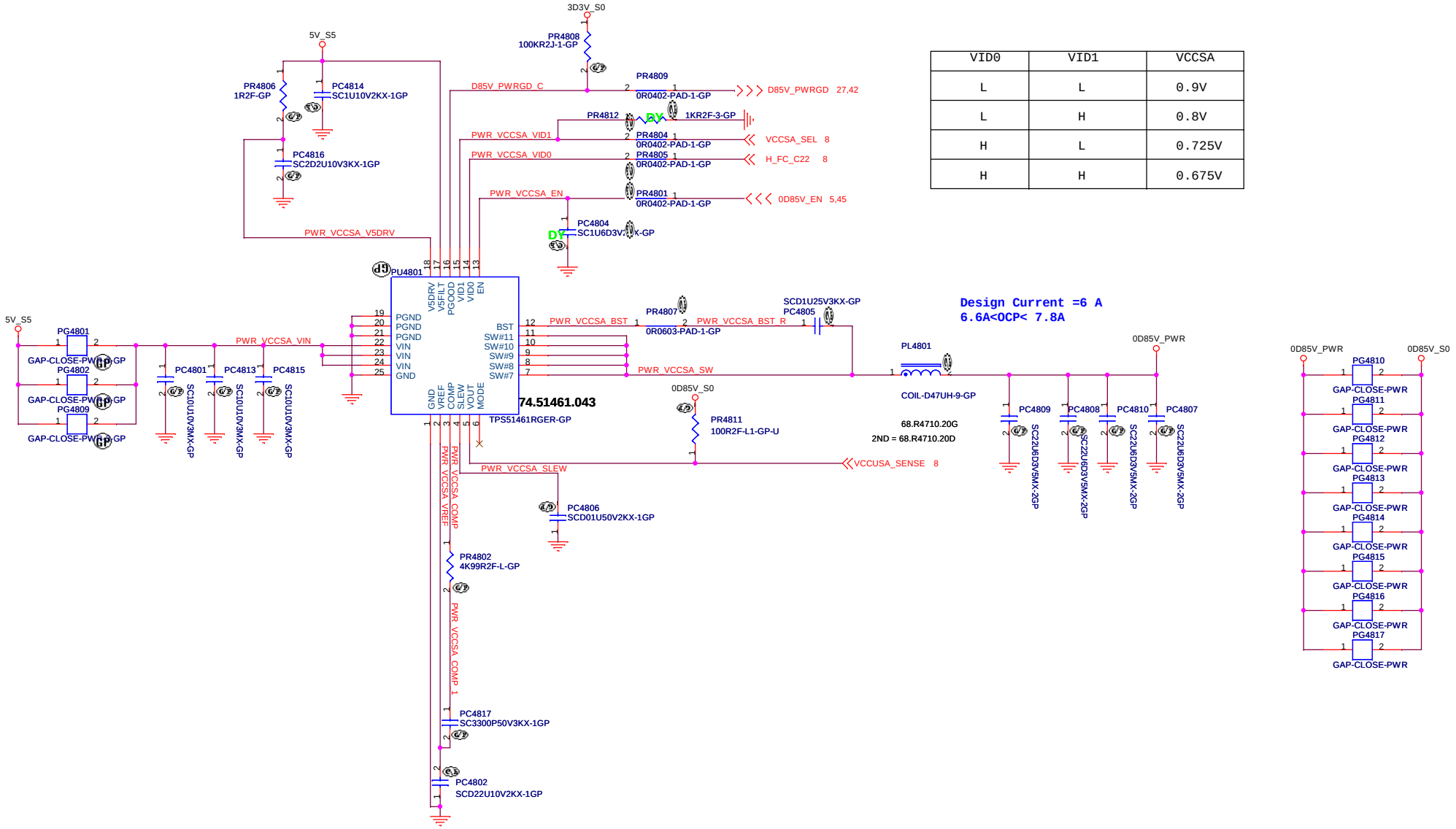


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8068A_1D8V***	
Size: A3	Document Number: **Colossus**	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

Design Current =6 A
6.6A<OCP< 7.8A

74.51461.043

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51461 VCCSA**

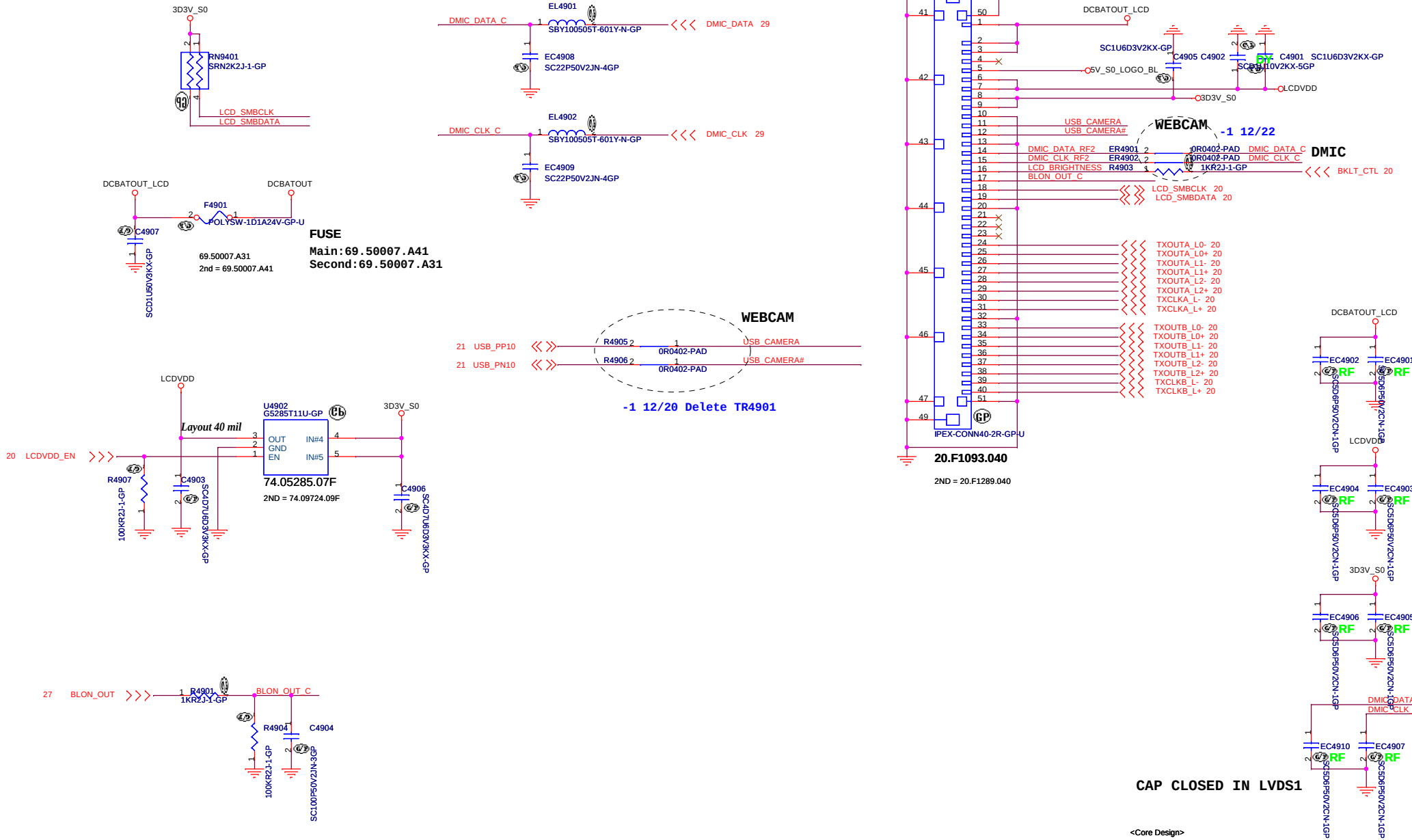
Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 48 of 103

LVDS CONNECTOR
AUO B156HB01 V0

D_MIC by EMI

LVDS Impedance:90 ohm



<Core Design>

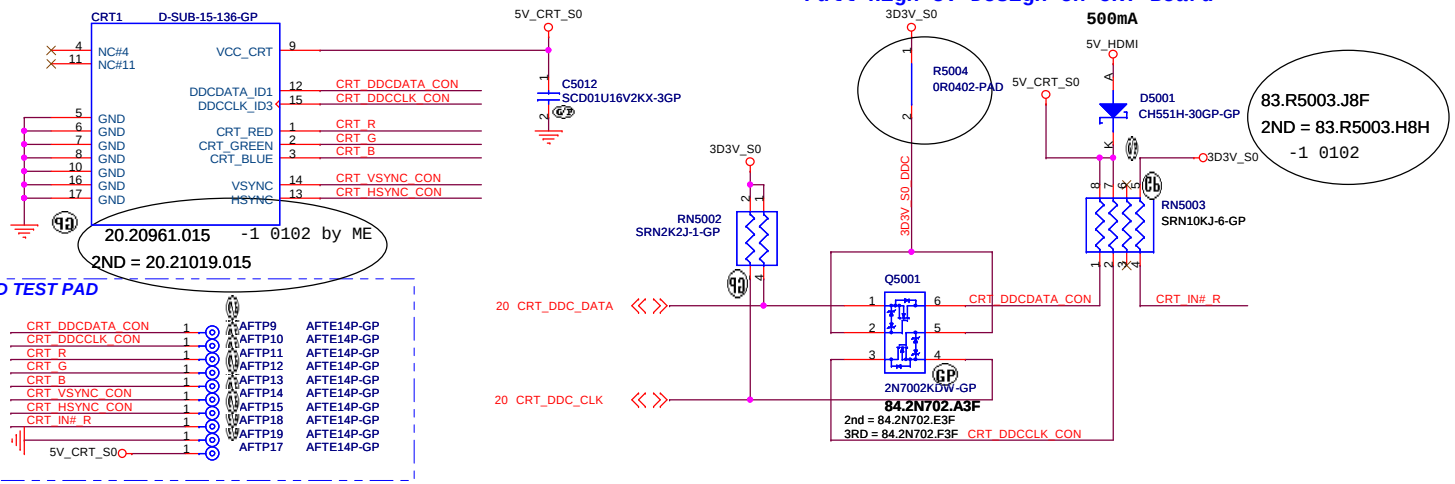
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 49 of 103

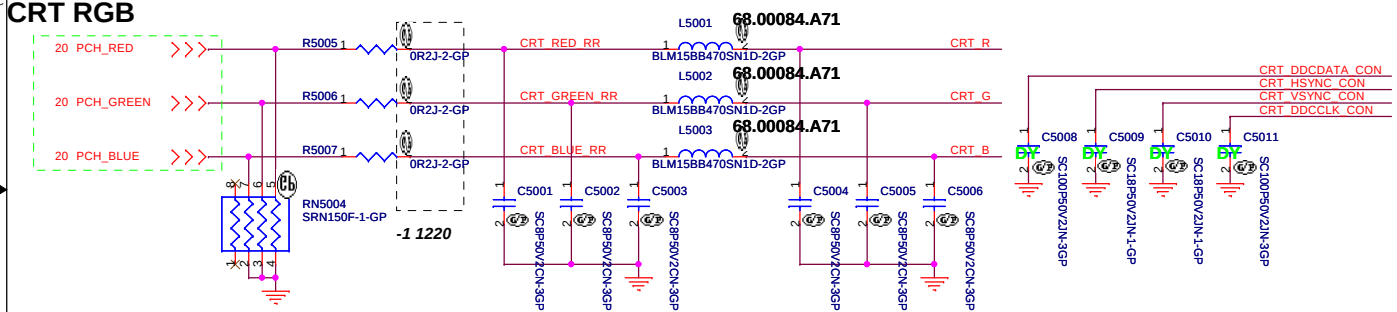
CRT Connector



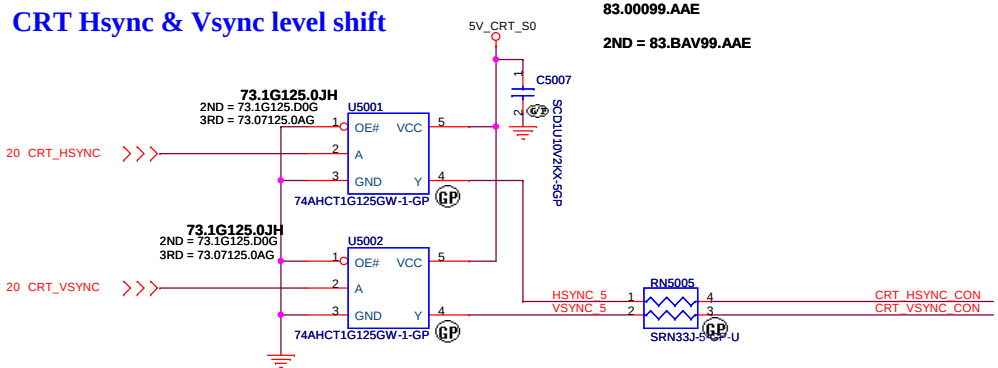
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board

CRT RGB



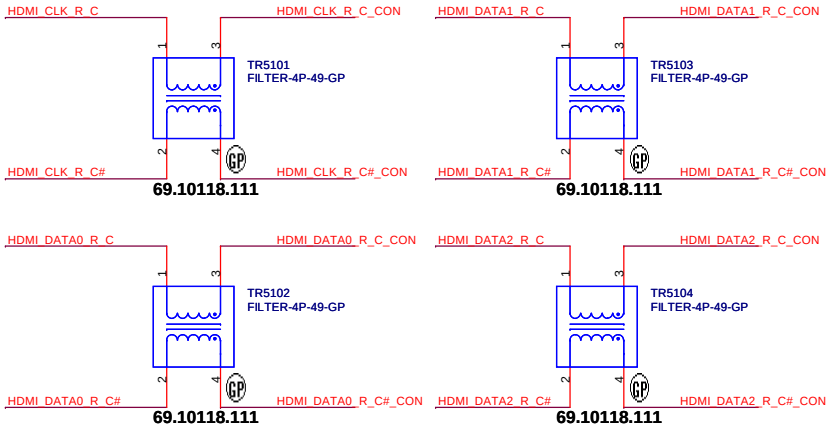
CRT Hsync & Vsync level shift



<Core Design>

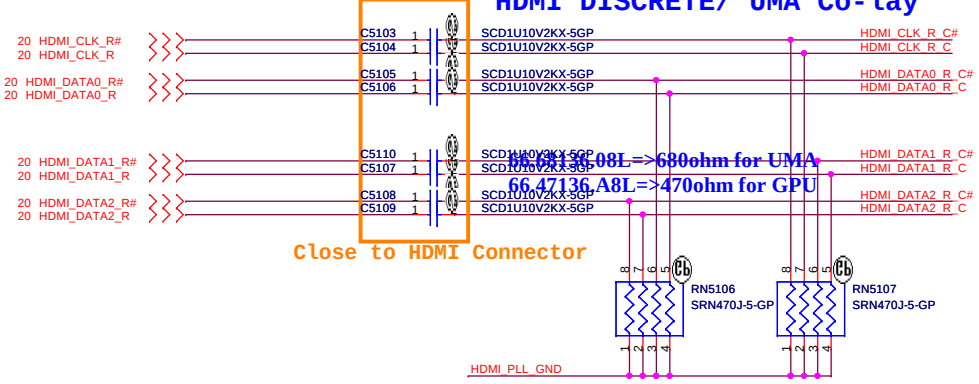
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CRT_CONN**		
Size: A3	Document Number: **Colossus**	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 50 of 103	

HDMI Level Shifter & CONNECTOR



Close to GPU

HDMI DISCRETE/ UMA Co-lay

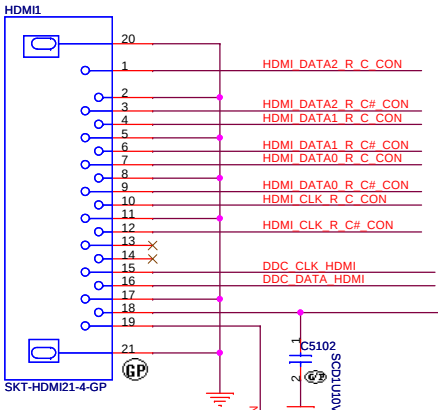


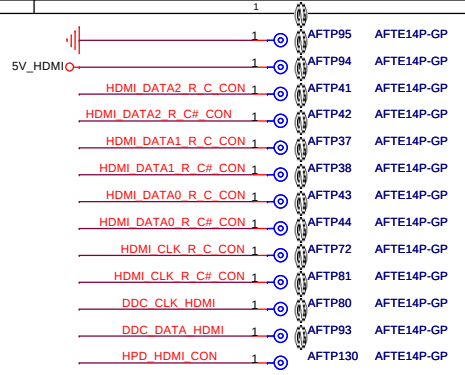
66.05136.08L=>680ohm for UMA

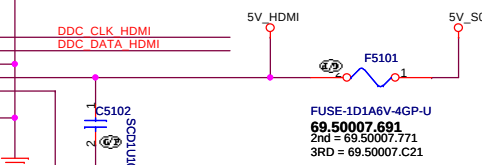
66.47136.A8L=>470ohm for GPU

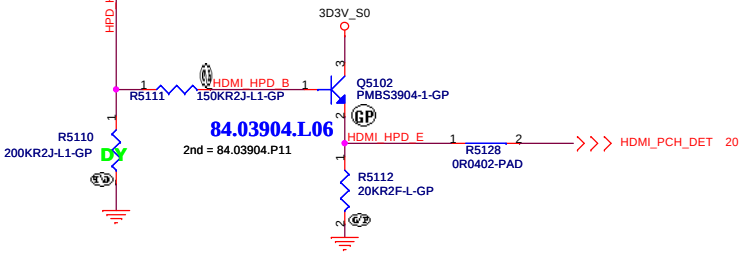
Close to HDMI Connector

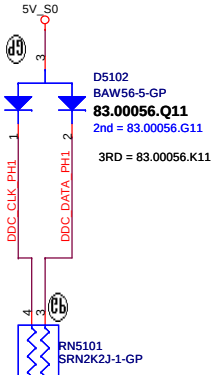
HDMI CONN

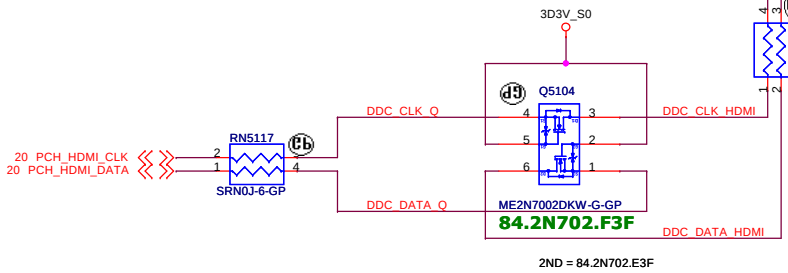


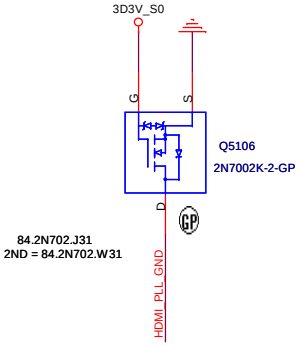












Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 51 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display Port***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 52 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 53 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 54 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

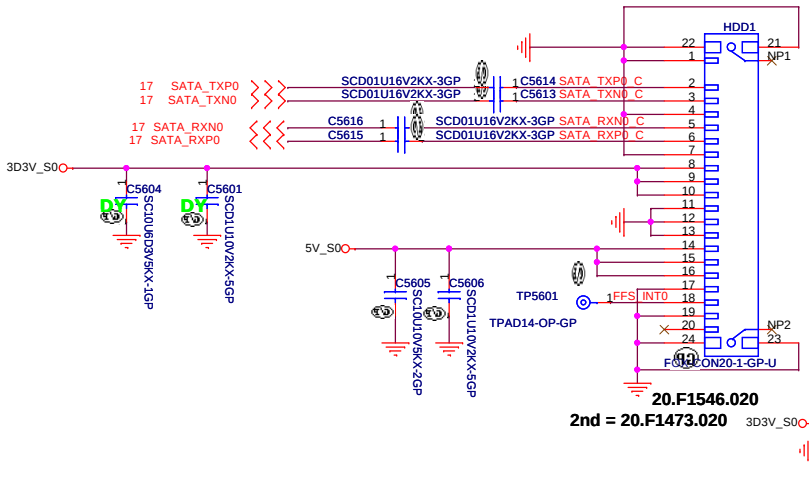
Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 55 of 103

SATA HDD1 Connector

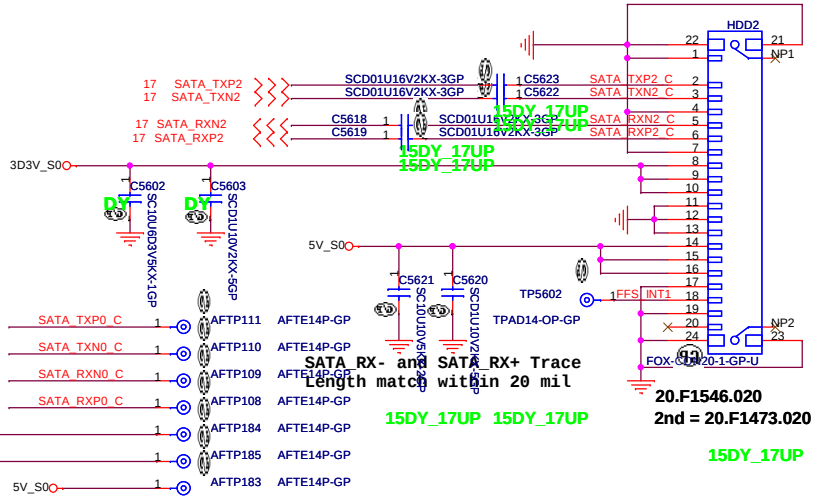
CHECK HDD conn model pin define_ME wire



20.F1546.020

2nd = 20.F1473.020

SATA HDD2 Connector



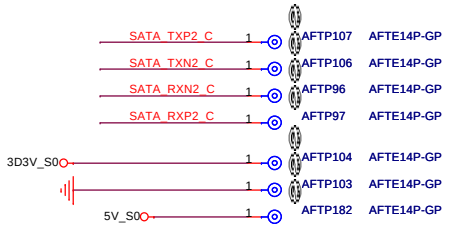
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

15DY_17UP 15DY_17UP

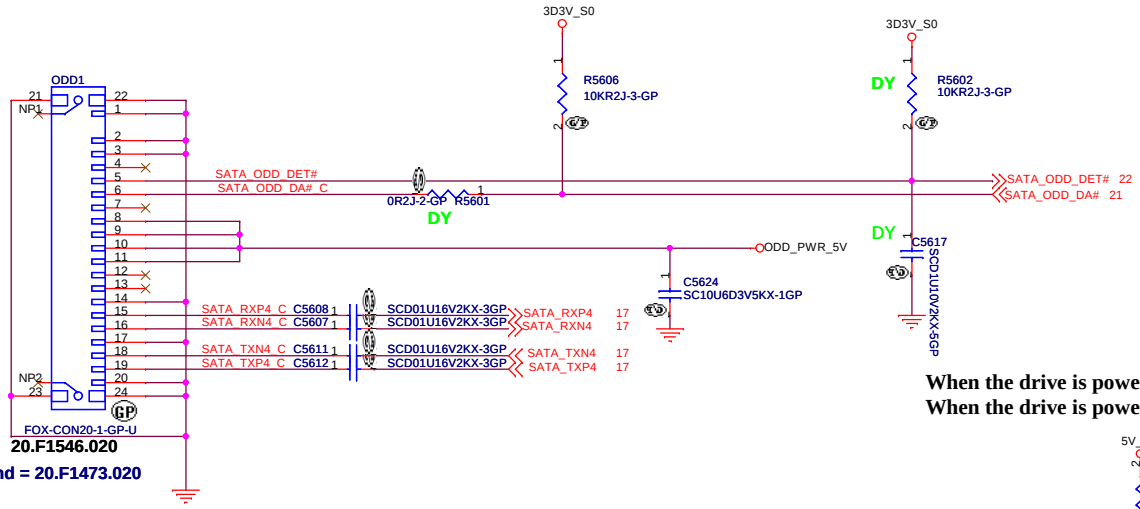
20.F1546.020

2nd = 20.F1473.020

15DY_17UP

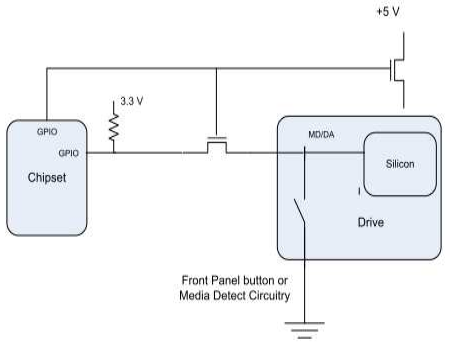


ODD Connector



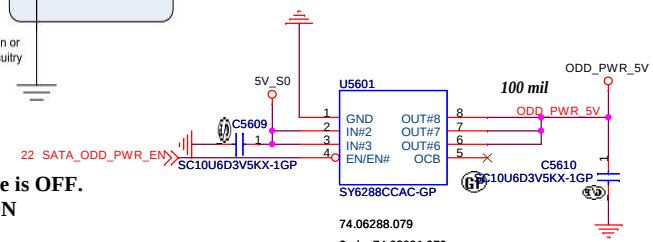
20.F1546.020

2nd = 20.F1473.020



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SATA Zero Power ODD



74.06288.079

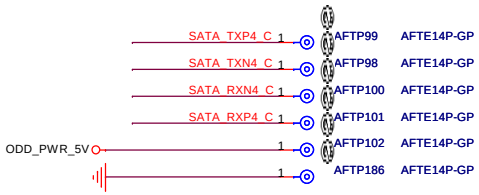
2nd = 74.02001.079

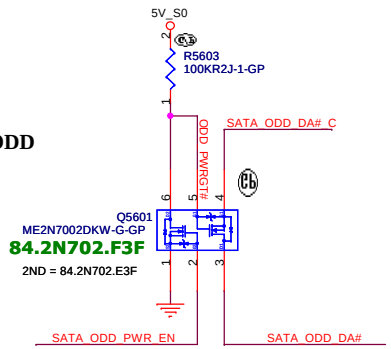
Current limit

Active High

typ =>2A

SUPPORT ZERO SATA ODD





<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 56 of 103

(Blanking)

<Core Design>

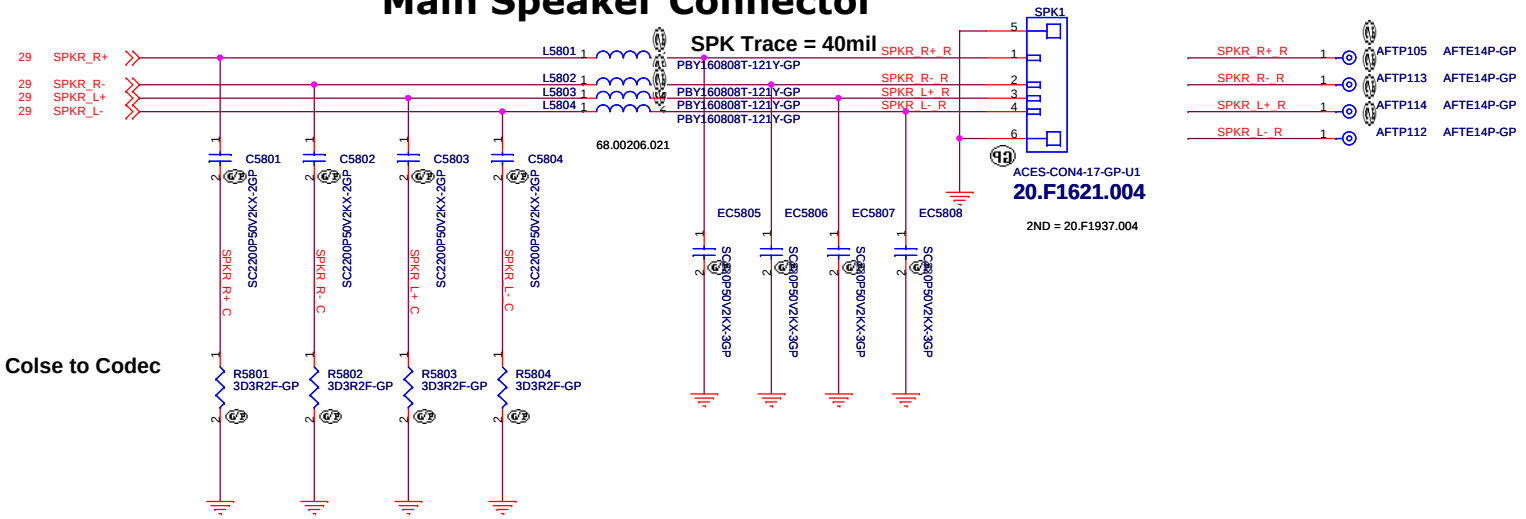
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 57 of 103

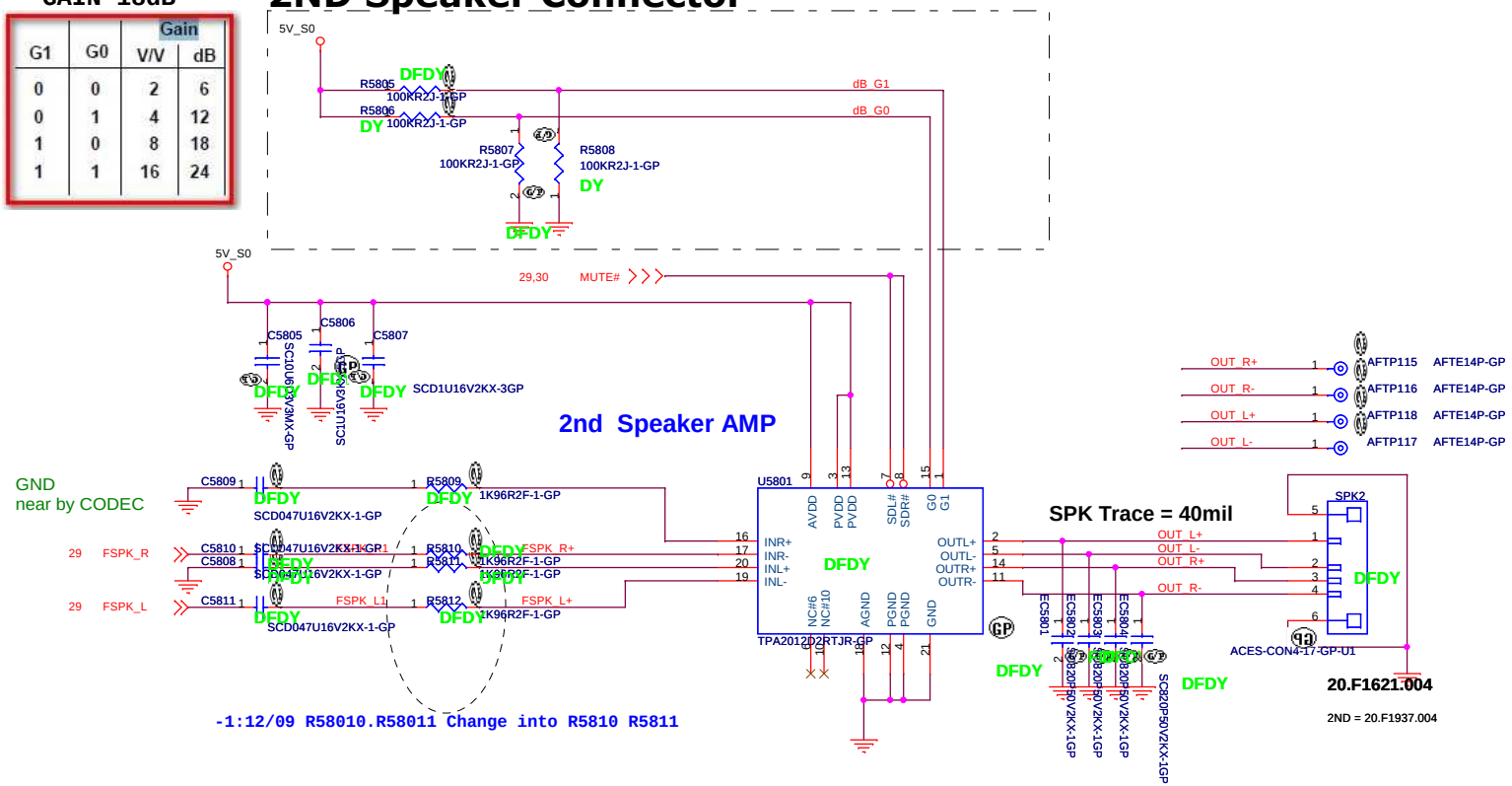
Main Speaker Connector



GAIN 18dB

Gain			
G1	G0	V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

2ND Speaker Connector



<core_design_block>
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

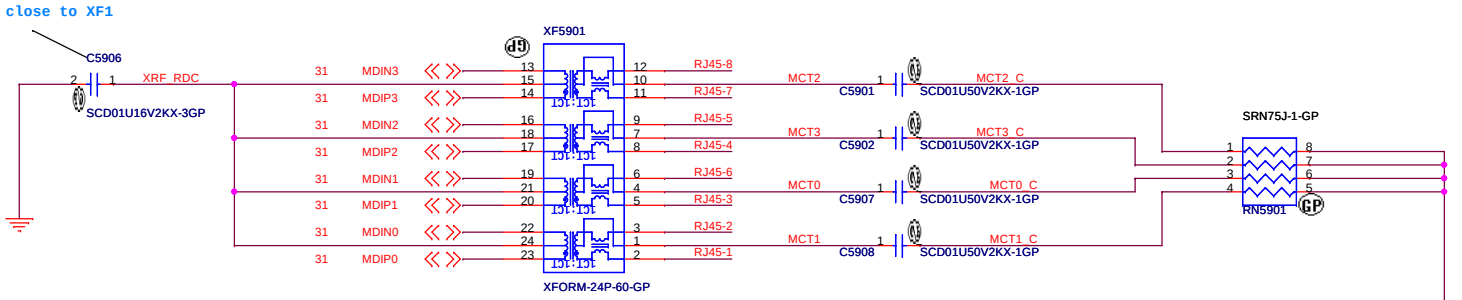
Title: SPEAKER CONN

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 58 of 103
</core_design_block>

White LED for connectivity and Amber LED for activity located on RJ-45 connector

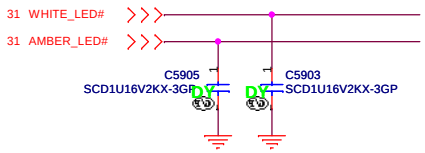
close to XF1



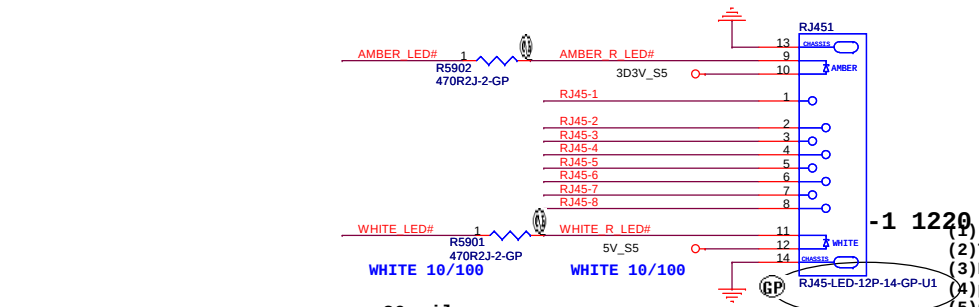
68.IH160.30A

2ND = 68.89246.301

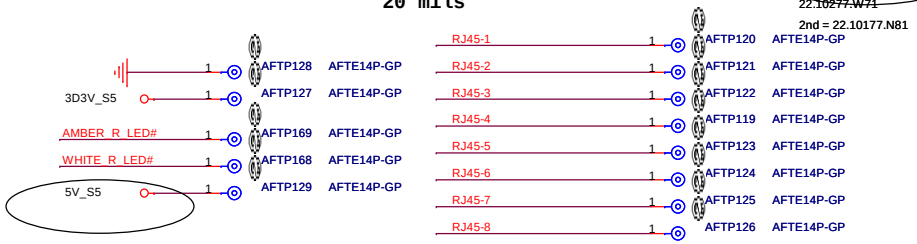
AMBER = LAN ACK



RJ451



20 mils



-1 1220

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

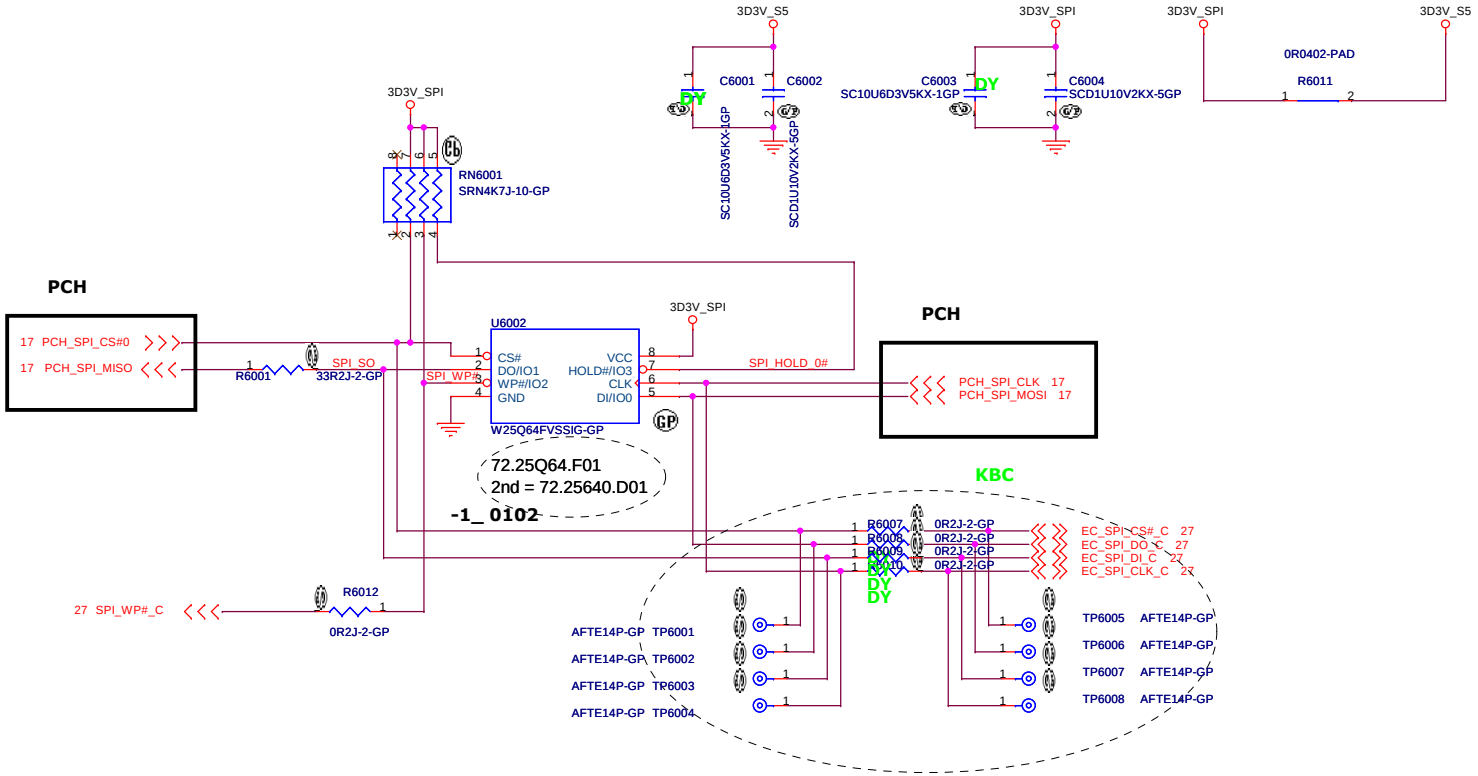
Title: RJ45+Transformer

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH & KBC



Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

-1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2，測試點必須在Top層.

<Core Design>

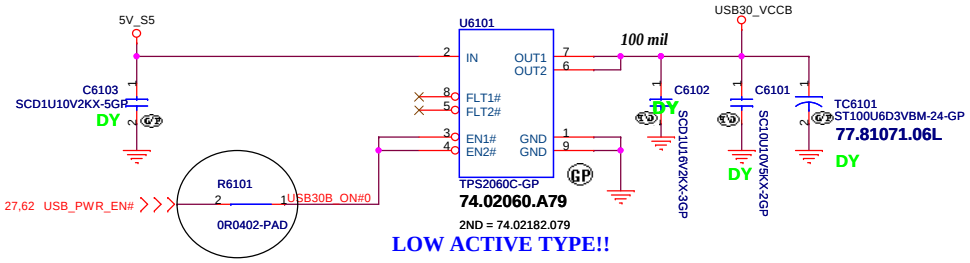
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 60 of 103	

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active

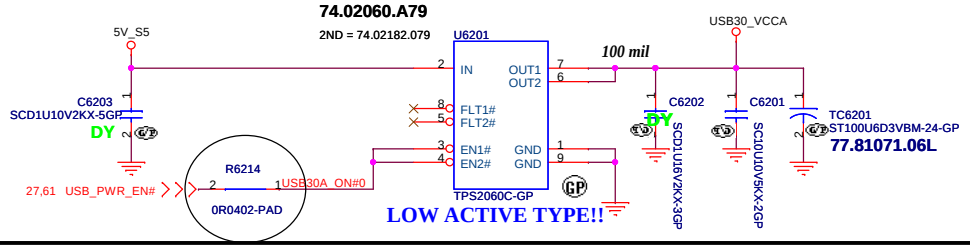


LOW ACTIVE TYPE!!

<Core Design>

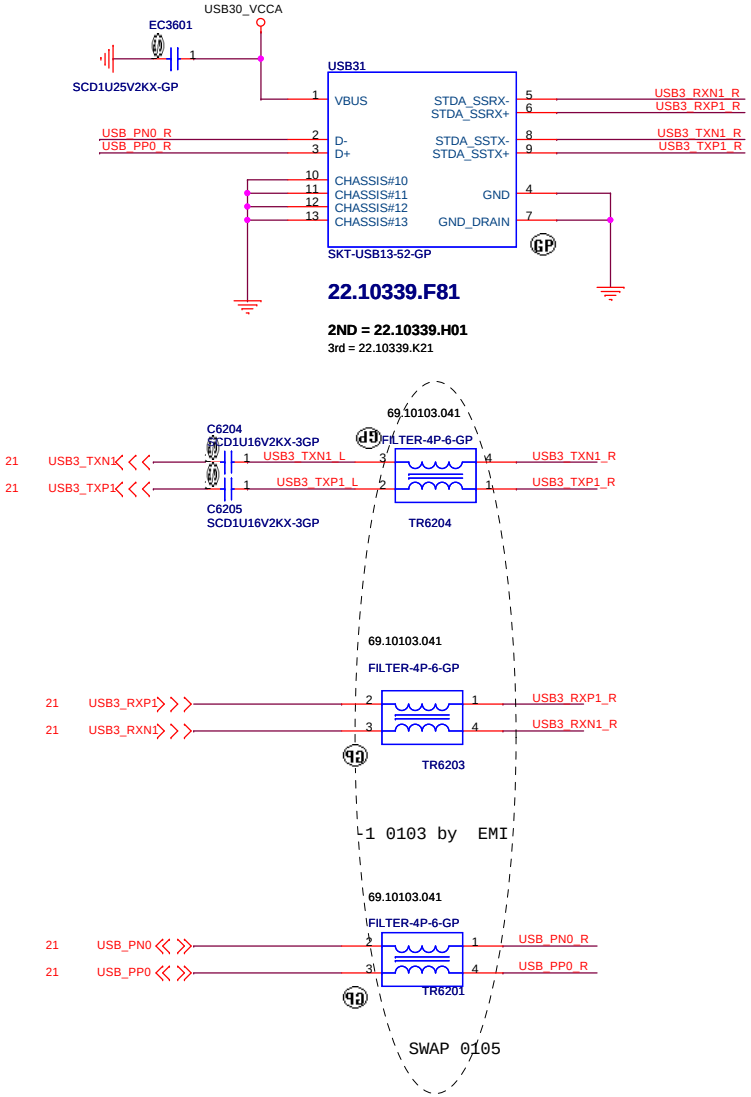
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *USB Power SW_USB IO*	
Size: A3	Document Number: Colossus — Rev: 1
Date: Wednesday, January 04, 2012	Sheet 61 of 103

Power switcher Low active

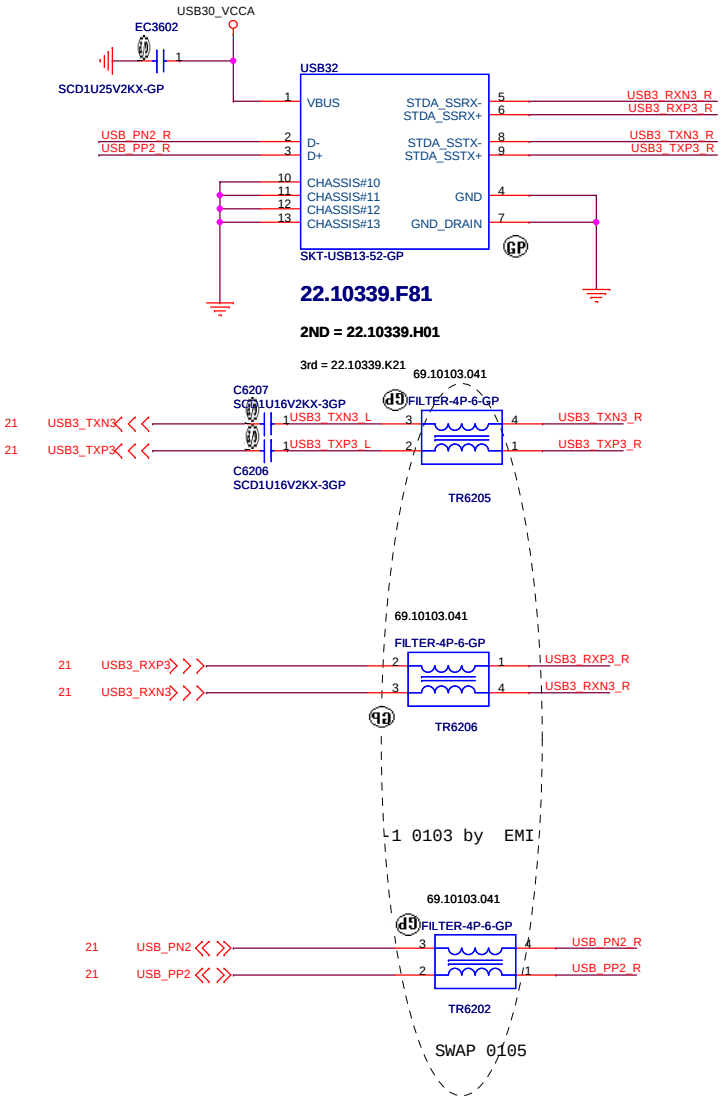


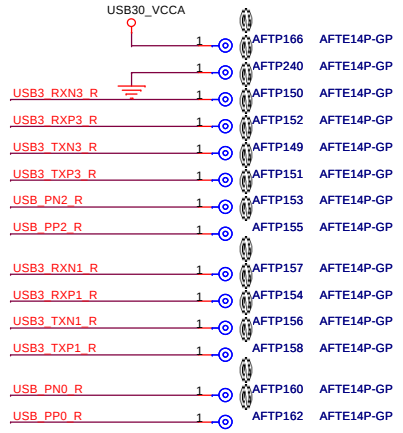
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3_1

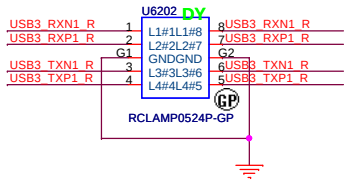


USB3_2

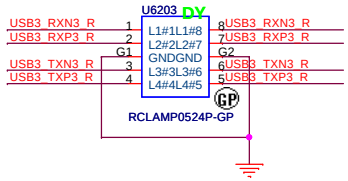




Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0**

Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 62 of 103

(Blanking)

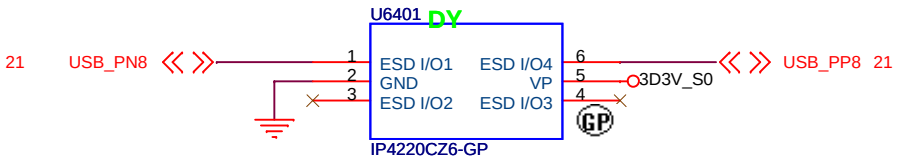
<Variant Name>

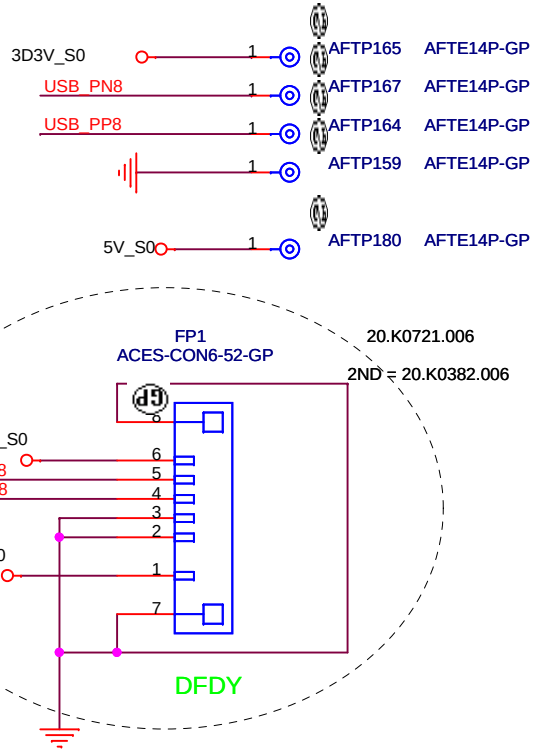
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Resered(Bluetooth)*

Size	Document Number	Rev
A3	Colossus	1

Finger Printer





-1 12/23 FP1 change source

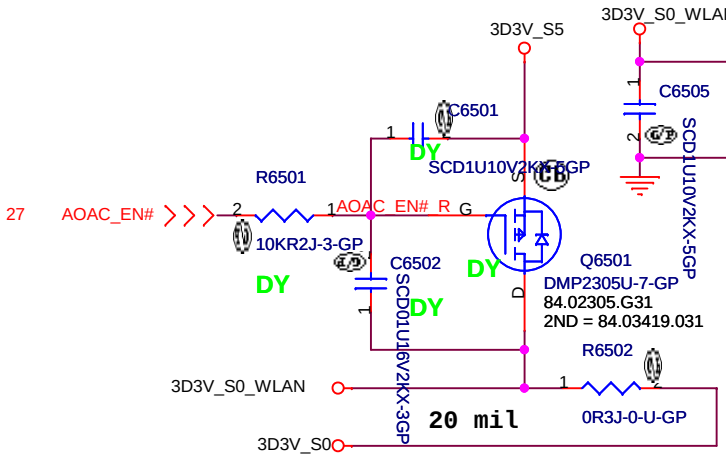
<Core Design>

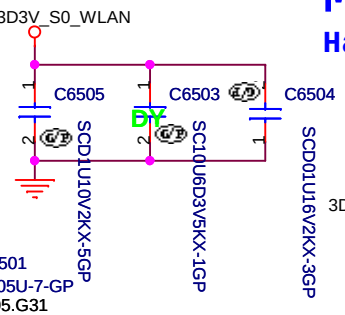
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Print Conn*		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 64 of 103	

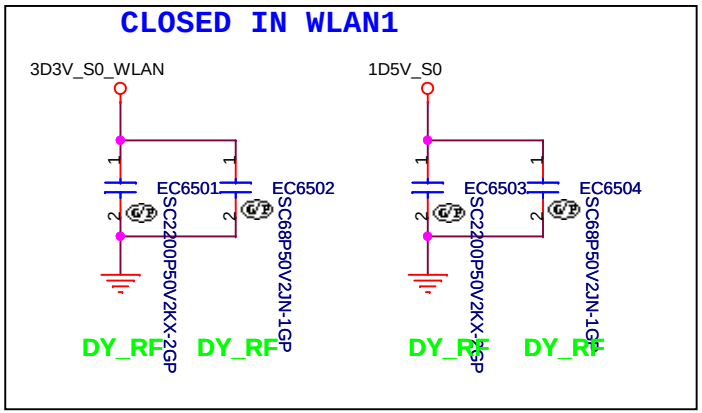
SSID = Wireless

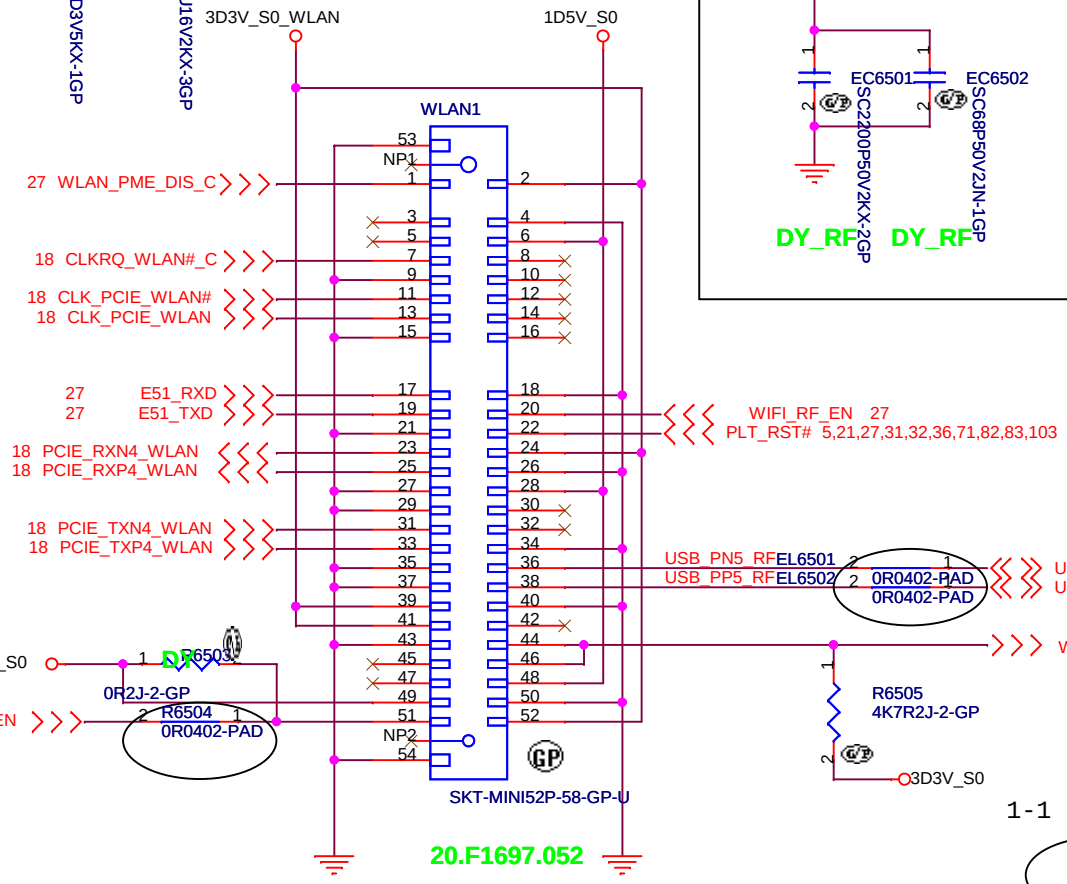
Mini-Card--WLAN

Half minicard









51	BT_ DISABLE_L (low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

20.F1697.052

2ND = 20.F1697.052

3RD = Main:62.10043.F91

1-1 1226 del TR6501

<Core Design>

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN+Bluetooth)/CONN***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 65 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

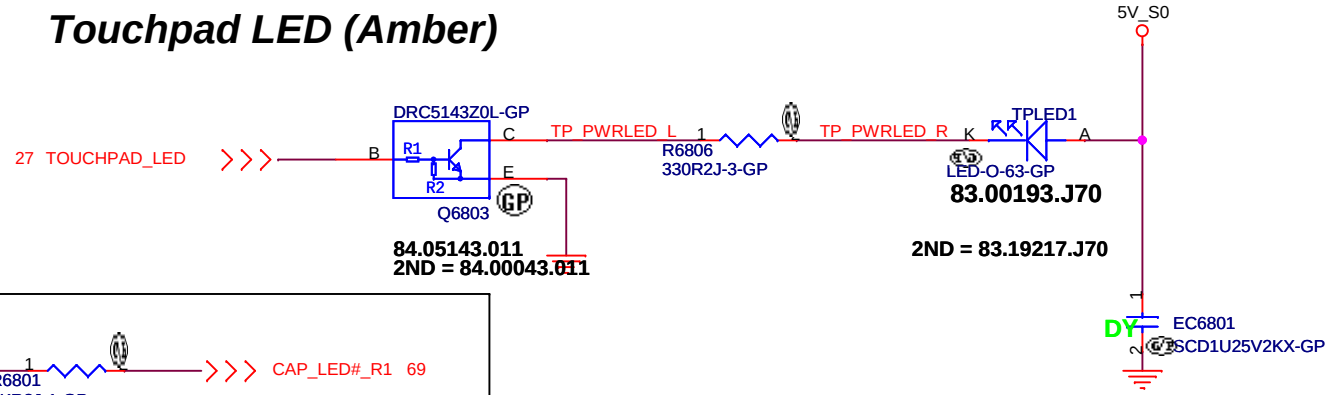
Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

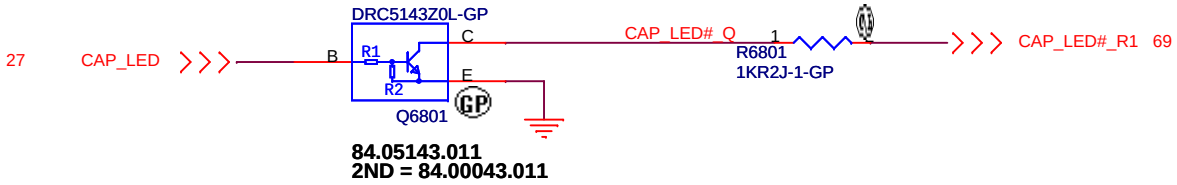
SSID = User.Interface

On Keyboard LEDs

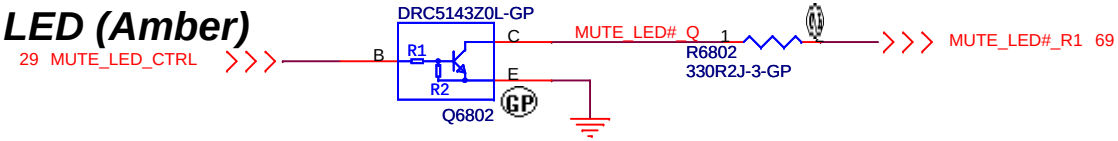
Touchpad LED (Amber)



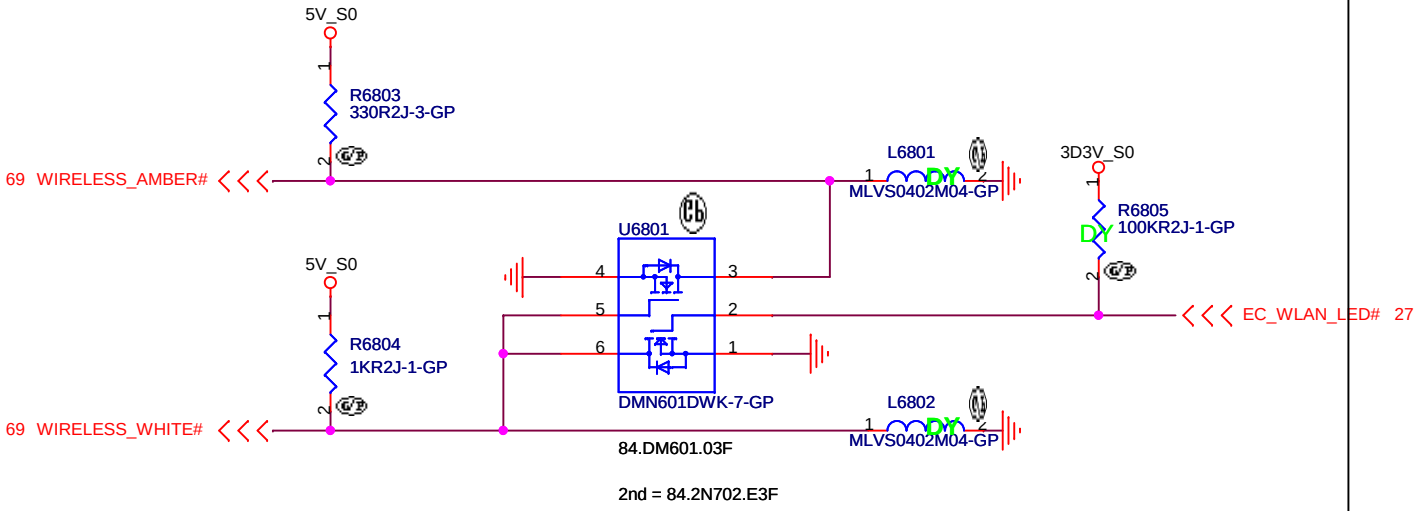
Cap locks LED (White)



Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

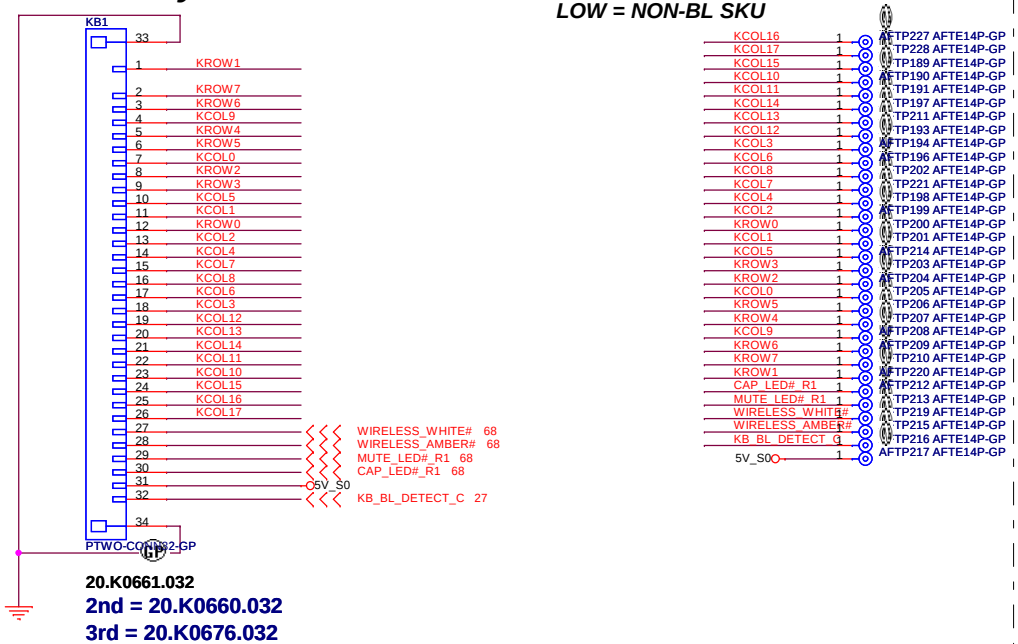
Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 68 of 103

SSID = KBC

Internal KeyBoard Connector



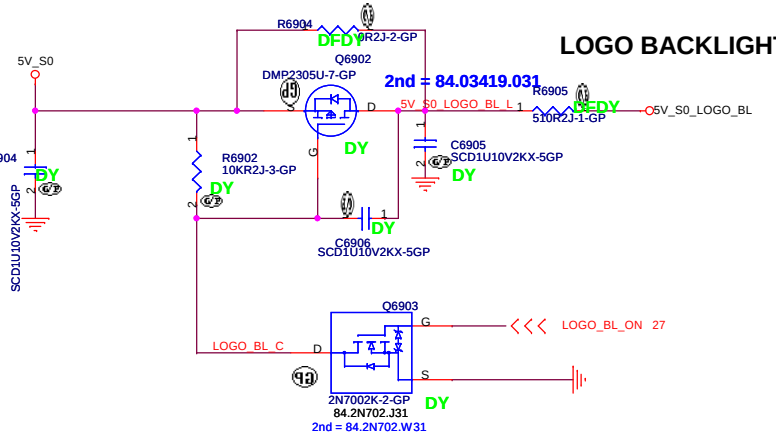
20.K0661.032
2nd = 20.K0660.032
3rd = 20.K0676.032

KROW[0..7] 27
KCOL[0..17] 27

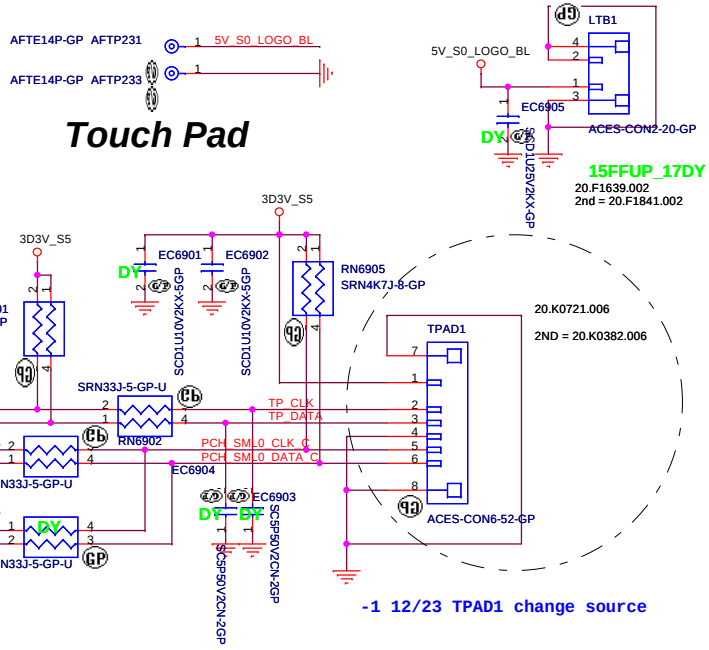
KB_BL_DETECT
HIGH = BL SKU
LOW = NON-BL SKU

A Cover Logo Backlight

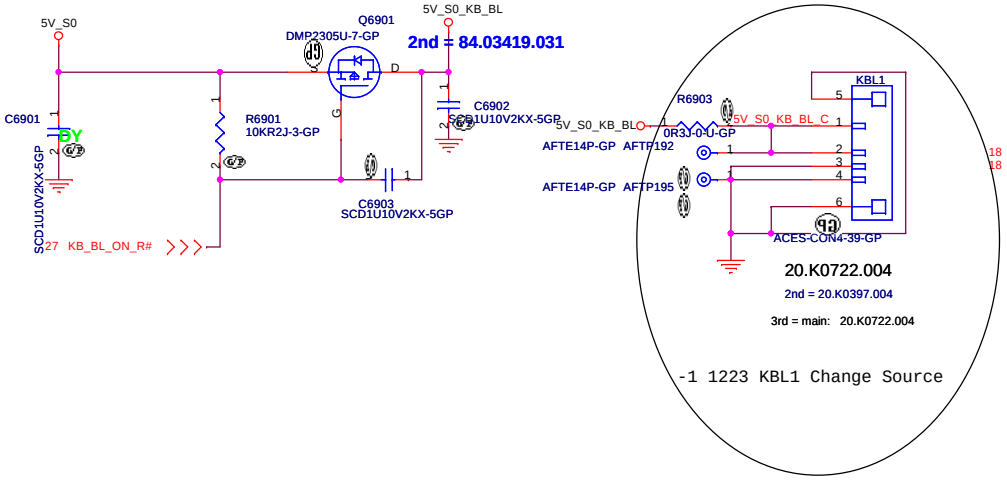
LOGO BACKLIGHT(LVDS1)

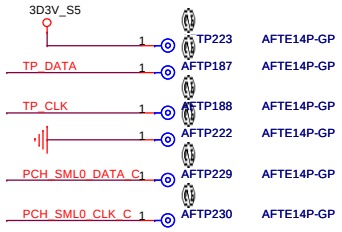


Touch Pad



Internal KeyBoard Backlight Connector





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Key Board/Touch Pad*

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 69 of 103

(Hall sensor at Power BD)

<Core Design>

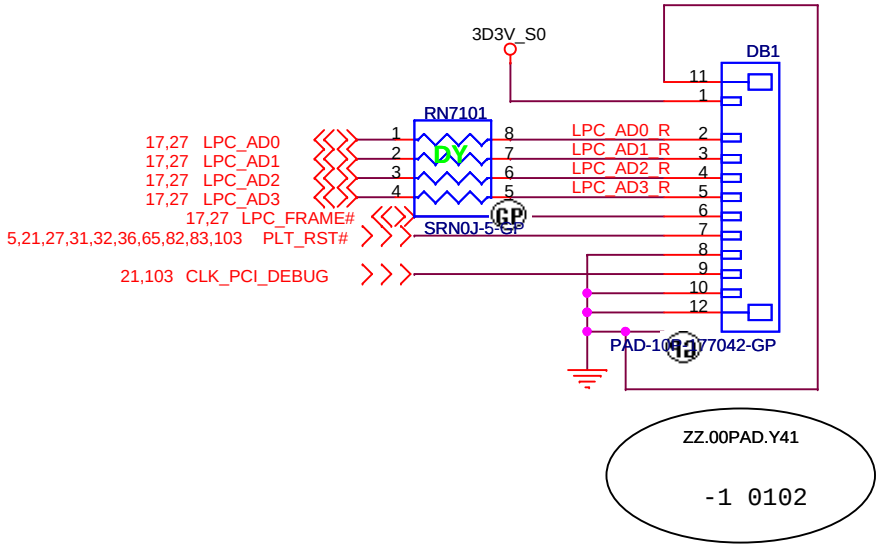
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 70 of 103

DEBUG BD for Factory Test



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Dubug connector***		
Size: A4	Document Number: **Colossus**	Rev: **1**
Date: Wednesday, January 04, 2012	Sheet 71 of 103	

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 72 of 103

(Blanking)

<Core Design>

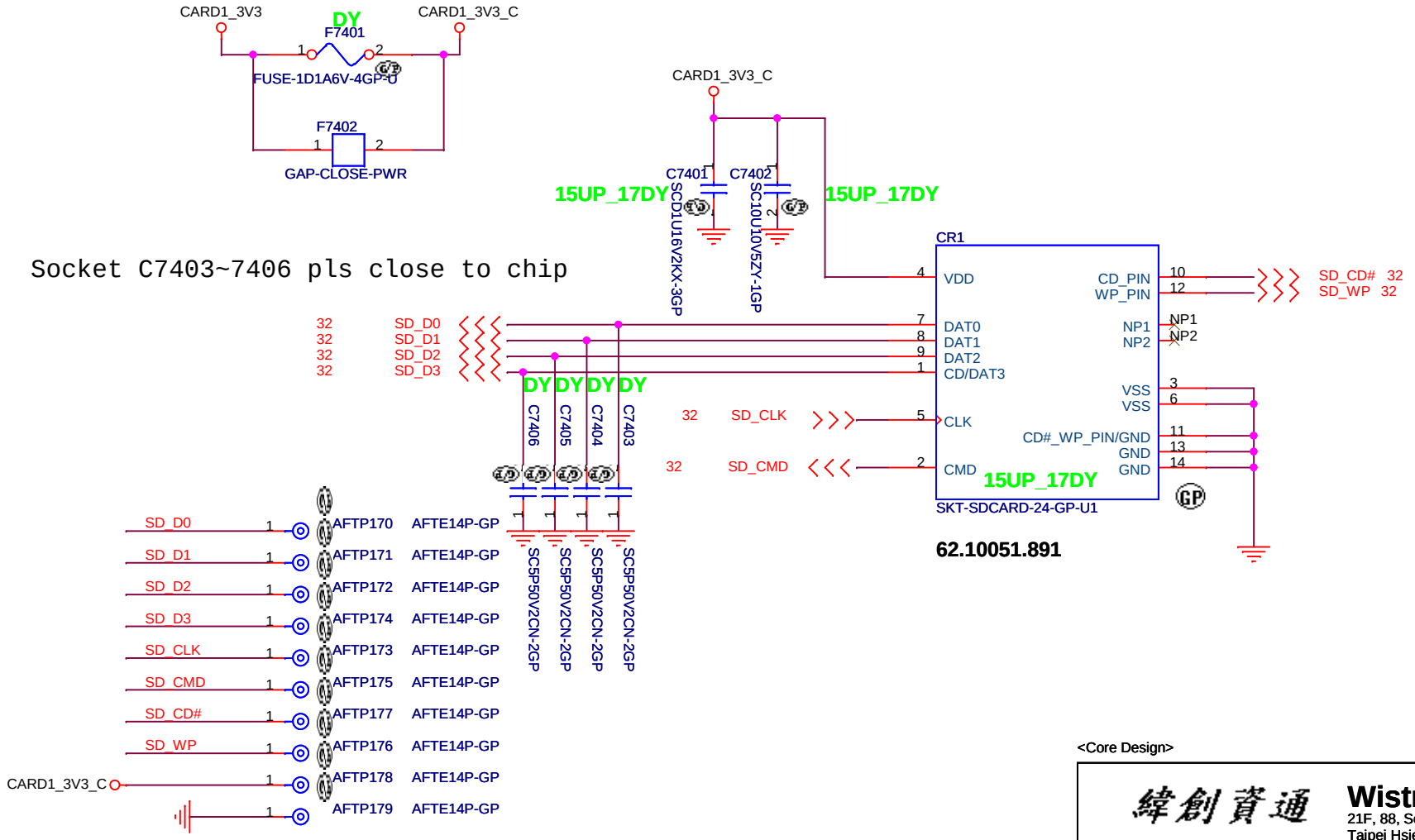
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 73 of 103

2 IN1 CARD-READER (SD/MMC)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 74 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A3	Colossus	1

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 76 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPM*		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 77 of 103	

(Blanking)

<Core Design>

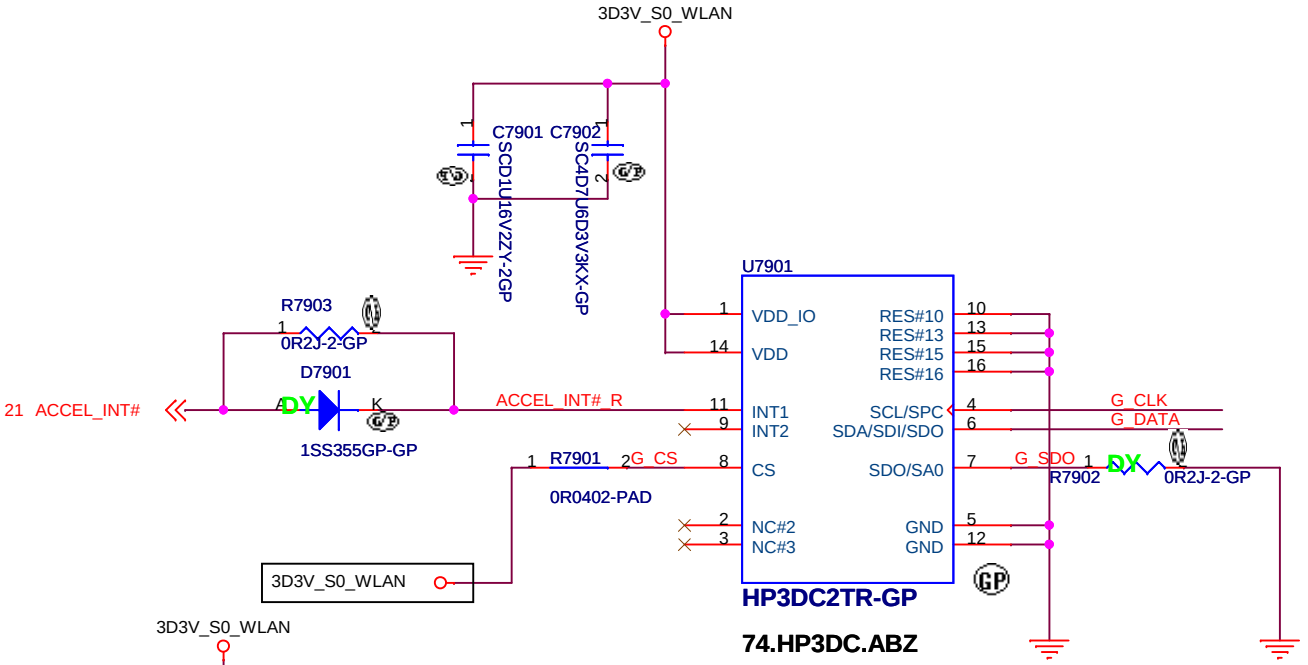
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

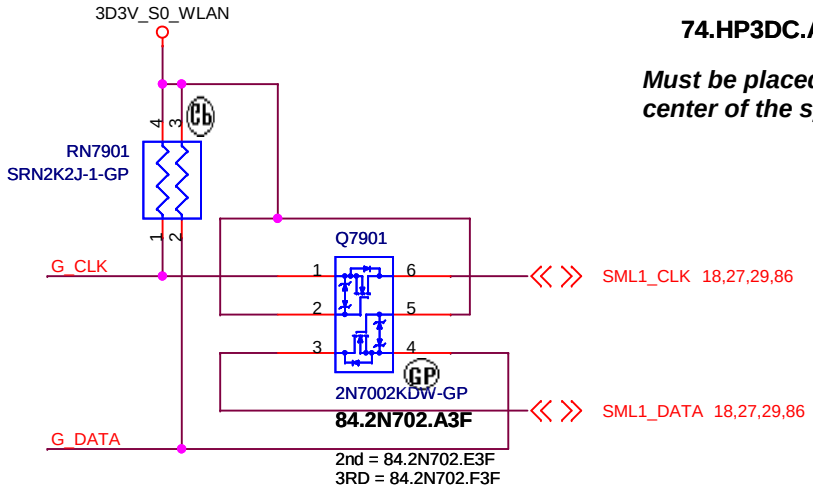
Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 78 of 103

ACCELEROMETER





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ACCELEROMETER

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 79 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 80 of 103

(Blanking)

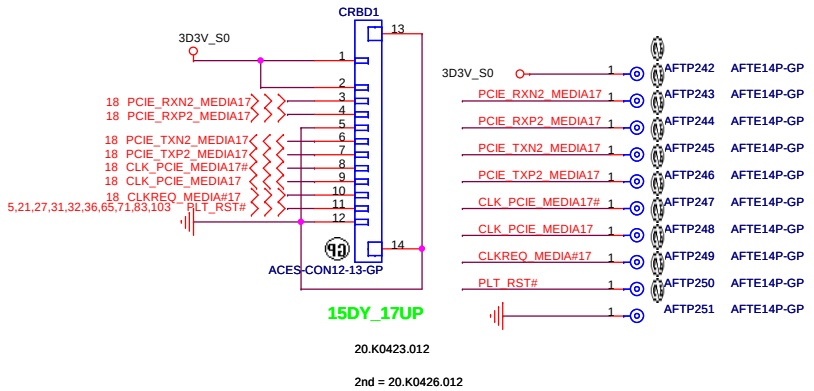
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

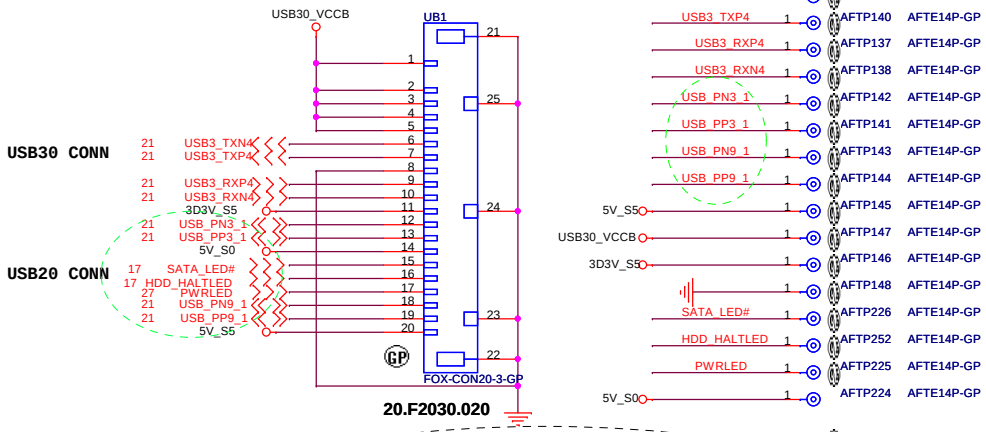
Card Reader BD 15"=DY 17"=PHASE IN



20.K0423.012

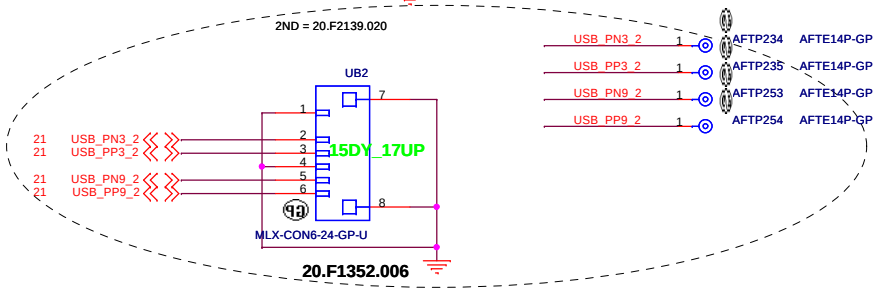
2nd = 20.K0426.012

USB BD(USB3.0*1+USB2.0*1)



20.F2030.020

2ND = 20.F2139.020



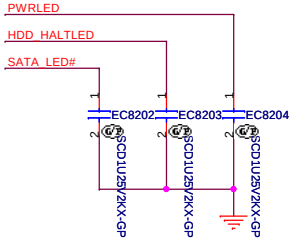
20.F1352.006

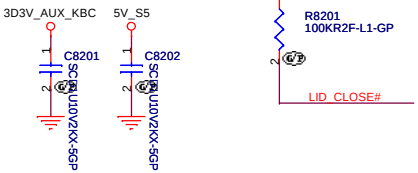
2nd = 20.F1804.006 -1 01/04

3RD = 20.F1639.006

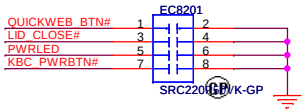
TOUCHPAD BD PAGE 69

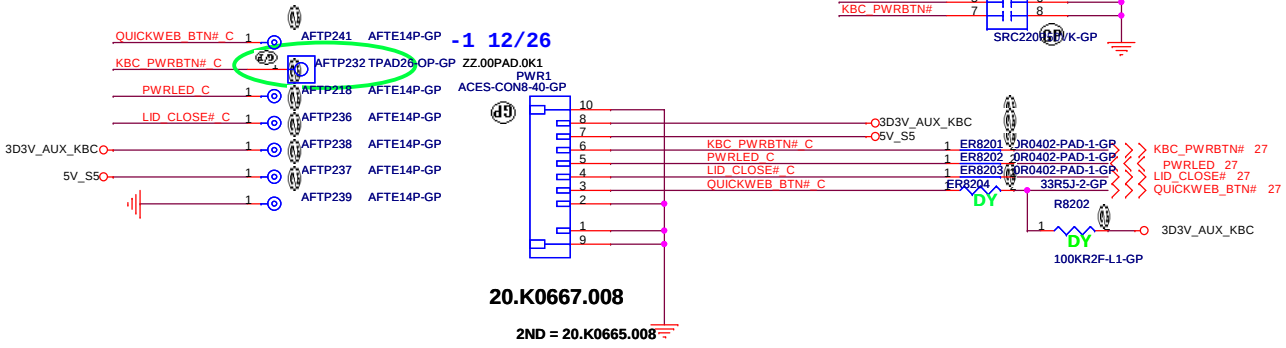
POWER BUTTON BD





For ESD

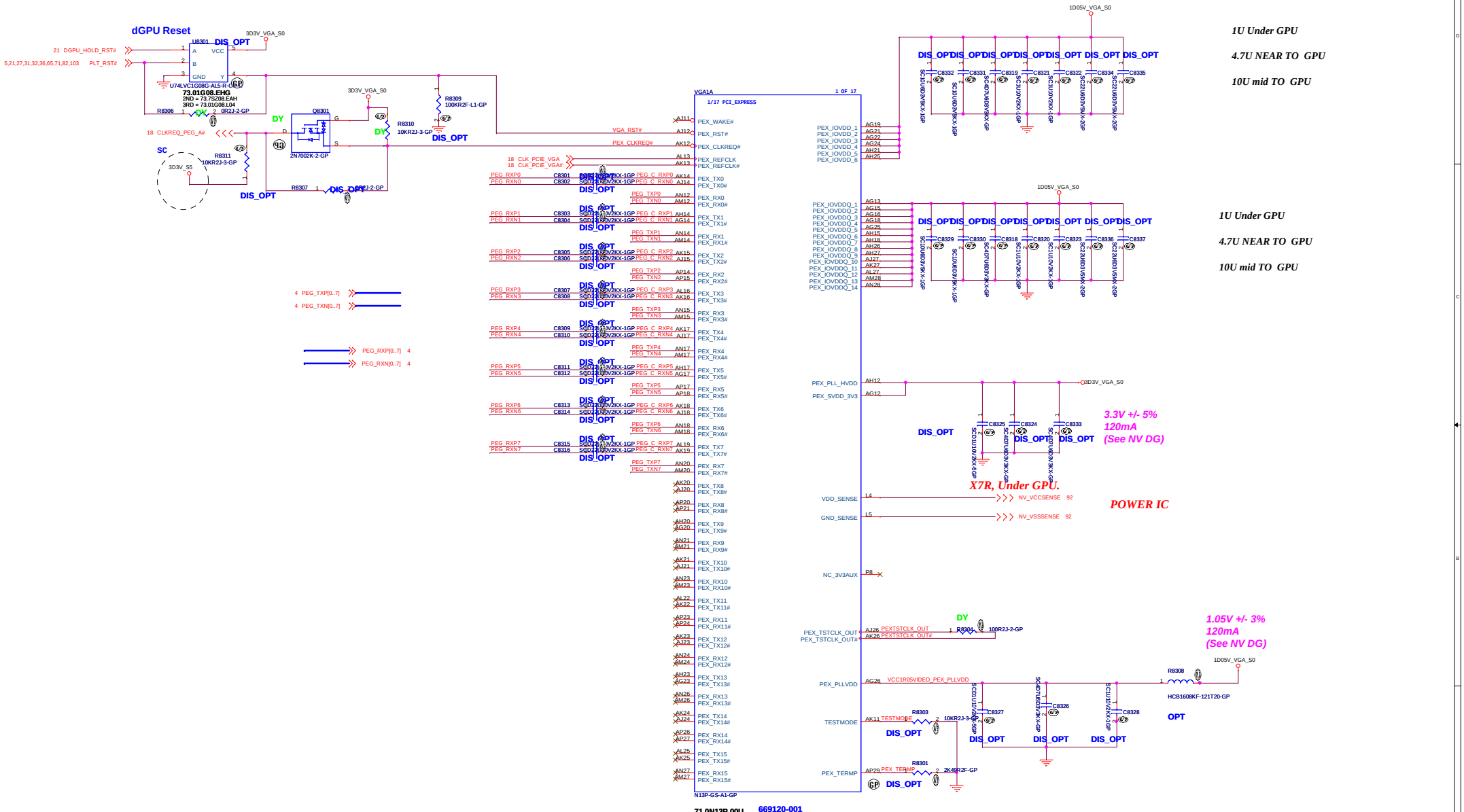




-1 12/26

20.K0667.008

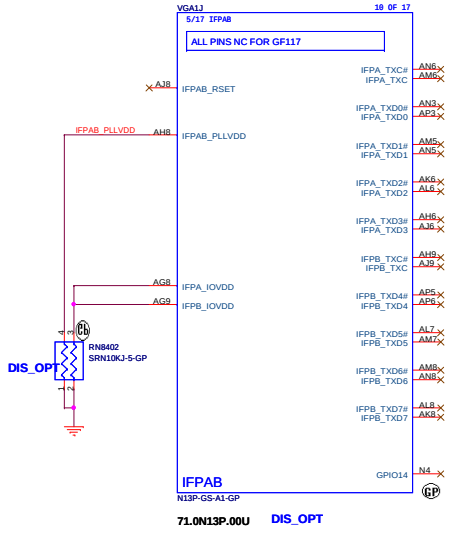
2ND = 20.K0665.008



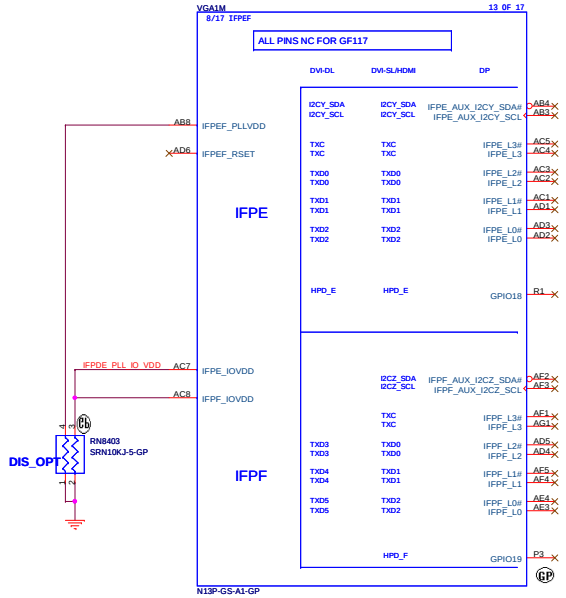
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU_PCIE/STRAPPING(1/5)***
Size: A2	Document Number: **Colossus** Rev: **1**
Date: Wednesday, January 04, 2012	Sheet 83 of 103

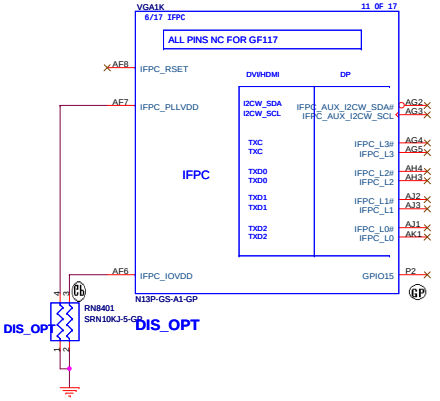
LVDS Interface



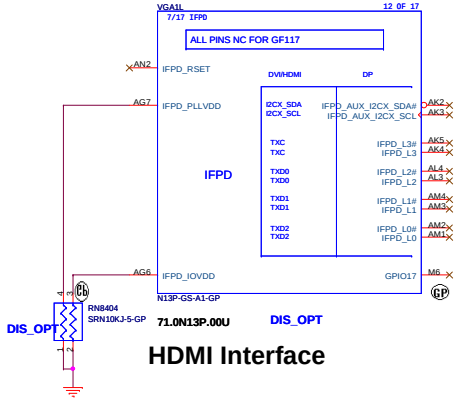
71.0N13P.00U DIS_OPT



71.0N13P.00U DIS_OPT



DIS_OPT



71.0N13P.00U DIS_OPT

HDMI Interface

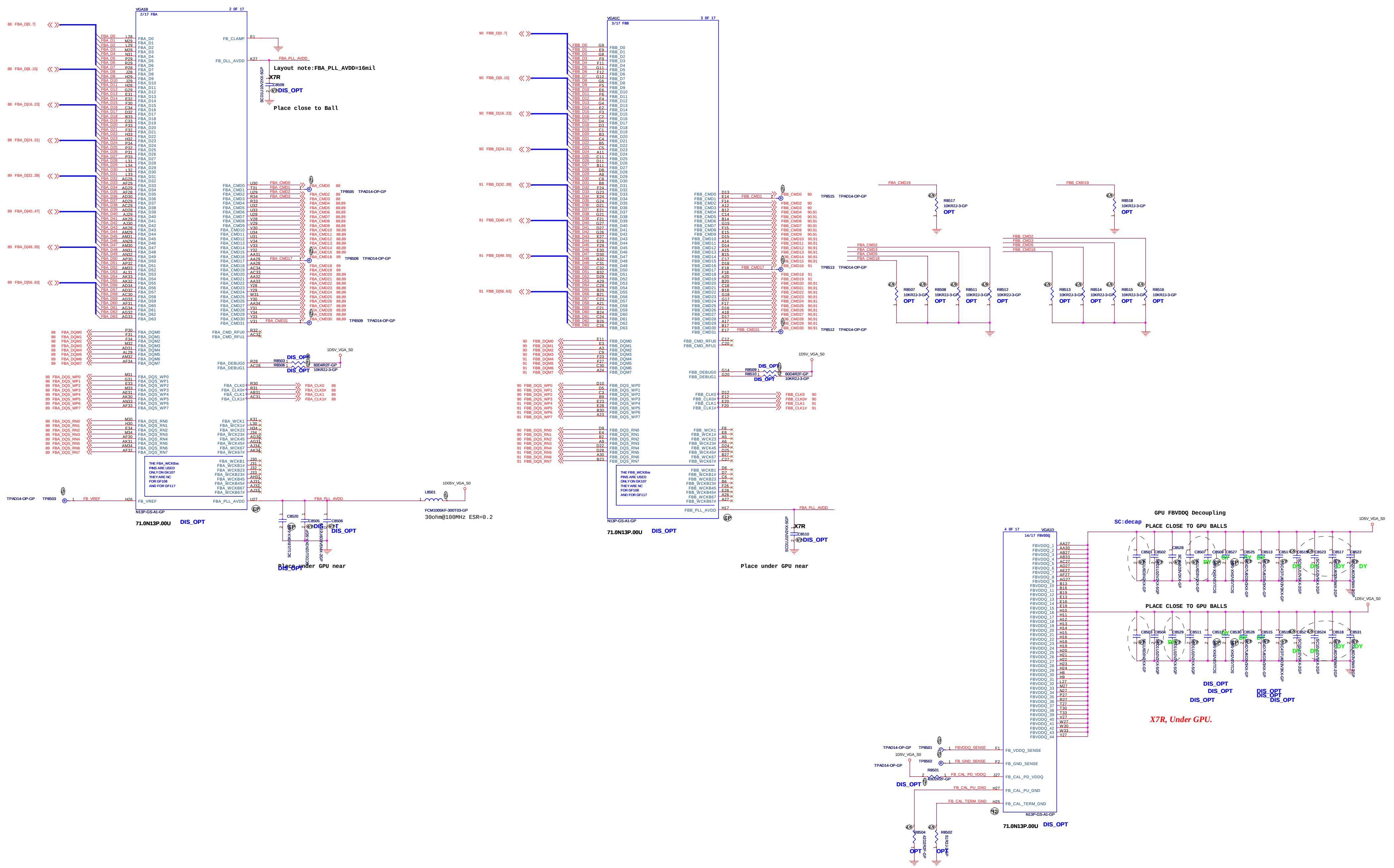
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: A2 | Document Number: Colossus | Rev: 1

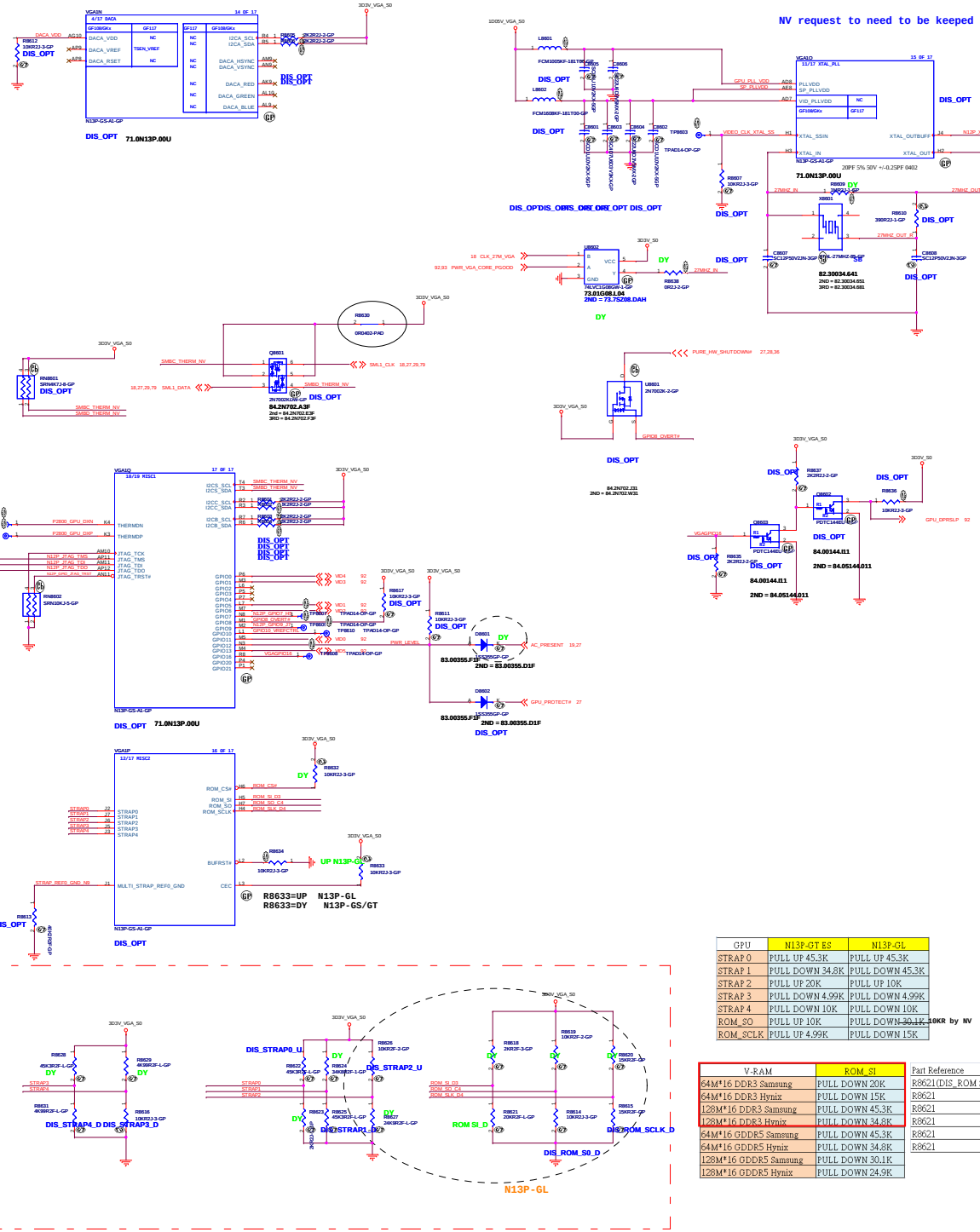
Date: Monday, December 26, 2011 | Sheet 84 of 103



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DP/LVDS/CRT/GPIO(3/5)	
Size: A1	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 85 of 103	



01/04/12 N13P-GL

Strap Option for N13P-GL/LP/GS/GT

Strap Name	GPU Sku	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	Set your BOM according to this column	Comment from NVIDIA
ROM_SO		XCLK_417/FB[1]	FB_0_BAR_SIZE/FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	1	0	0	1	PULL UP 10K	
	N13P-GS	1	0	0	1	PULL UP 10K	
	N13P-GT	1	0	0	1	PULL UP 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	1	0	1	PULL DOWN 30.1K	
ROM_SCLK		PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM		
	N13P-GL	0	0	1	0	PULL DOWN 15K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13P-LP	1	0	0	0	PULL UP 4.99K	
	N13P-GS	1	0	0	0	PULL UP 4.99K	
	N13P-GT	1	0	0	0	PULL UP 4.99K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13M-GE1	1	0	0	0	PULL UP 4.99K	
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]		
	Hynix	X	X	X	X	This is depends on what Vram you will use. Please check latest RVL.	
	Samsung	X	X	X	X		
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
	N13P-GL	1	0	0	1	PULL UP 10K	N13P-GL DID => 0x0DE9
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13P-LP	0	0	1	1	PULL DOWN 20K	N13P-LP DID => 0x0FD3
	N13P-GS	0	0	1	0	PULL DOWN 15K	N13P-GS QS DID =>0x0FD2
	N13P-GT	0	0	0	1	PULL DOWM 10K	N13P-GT QS DID =>0x0FD1
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13M-GE1	1	0	0	0	PULL UP 4.99K	N13M-GE1 DID => 0x1058
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
	N13P-GL	0	1	1	1	PULL DOWN 45.3K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	0	PULL DOWN 34.8K	
	N13P-GS	0	1	1	0	PULL DOWN 34.8K	
	N13P-GT	0	1	1	0	PULL DOWN 34.8K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13M-GE1	0	1	1	0	PULL DOWN 34.8K	
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]		
	N13P-GL	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-GS	1	1	1	1	PULL UP 45.3K	
	N13P-GT	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13M-GE1	1	1	1	1	PULL UP 45.3K	
STRAP3		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
	N13P-GL	0	0	0	0	PULL DOWN 4.99K	
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-GS	0	0	0	0	PULL DOWN 4.99K	
	N13P-GT	0	0	0	0	PULL DOWN 4.99K	
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13M-GE1	0	0	0	0	PULL DOWN 4.99K	No display for Optimus sku
STRAP4		RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		
	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GS	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GT	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	0	0	1	PULL DOWN 10K	

GPU	N13P-GT ES	N13P-GL
STRAP 0	PULL UP 45.3K	PULL UP 45.3K
STRAP 1	PULL DOWN 34.8K	PULL DOWN 45.3K
STRAP 2	PULL UP 20K	PULL UP 10K
STRAP 3	PULL DOWN 4.99K	PULL DOWN 4.99K
STRAP 4	PULL DOWN 10K	PULL DOWN 10K
ROM_SO	PULL UP 10K	PULL DOWN ~~30.1K~~ 10KR by NV
ROM_SCLK	PULL UP 4.99K	PULL DOWN 15K

V-RAM	ROM_SI
64M*16 DDR3 Samsung	PULL DOWN 20K
64M*16 DDR3 Hynix	PULL DOWN 15K
128M*16 DDR3 Samsung	PULL DOWN 45.3K
128M*16 DDR3 Hynix	PULL DOWN 34.8K
64M*16 GDDR5 Samsung	PULL DOWN 45.3K
64M*16 GDDR5 Hynix	PULL DOWN 34.8K
128M*16 GDDR5 Samsung	PULL DOWN 30.1K
128M*16 GDDR5 Hynix	PULL DOWN 24.9K

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20KR2F-L-GP	R402H16
R8621	64.15025.6DL	15KR2F-GP	R402H16
R8621	64.34825.6DL	34K8R2F-L-GP	R402H16
R8621	64.45325.6DL	45K3R2F-L-GP	R402H16
R8621	64.30125.6DL	30K1R2F-L-GP	R402H16
R8621	64.24925.6DL	24K9R2F-L-GP	R402H16

<Core Design>

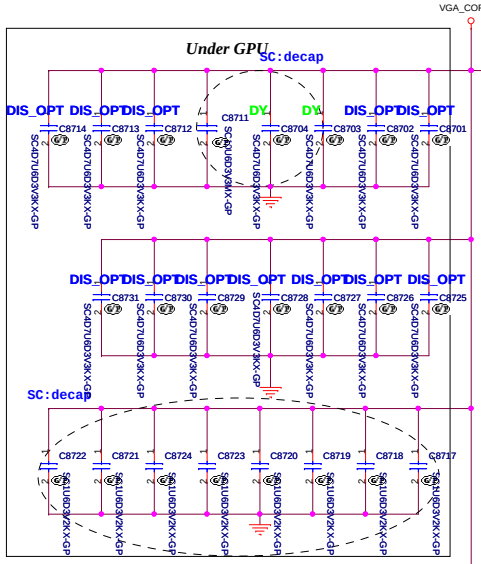
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

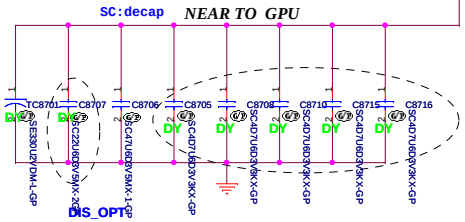
Title: GPU_POWER(4/5)

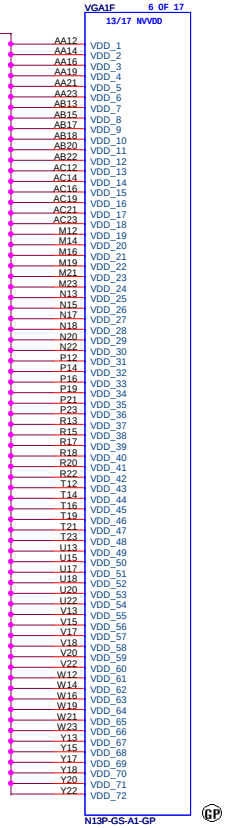
Size: A1 | Document Number: Colossus | Rev: 1

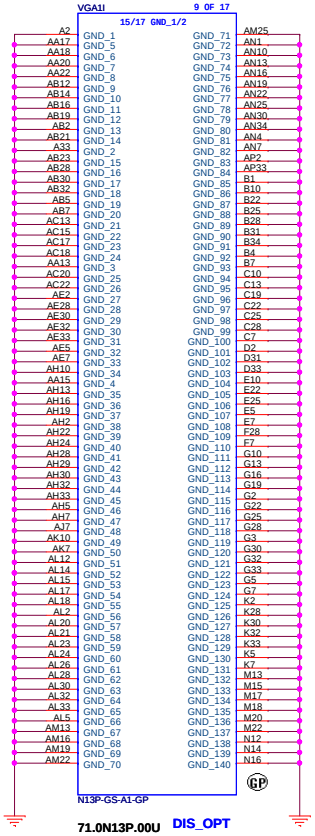
Date: Wednesday, January 04, 2012 | Sheet 85 of 103

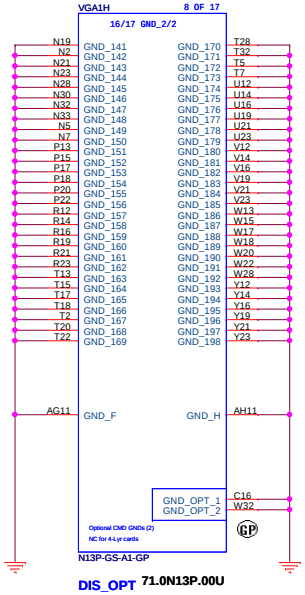
EDP 60A (TDP 55W)

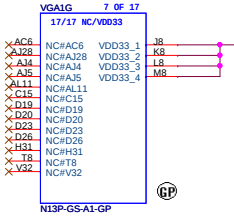


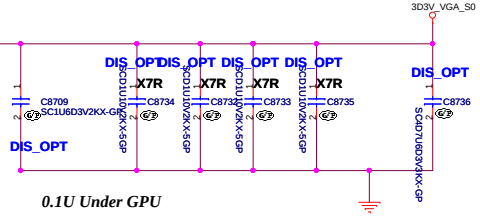








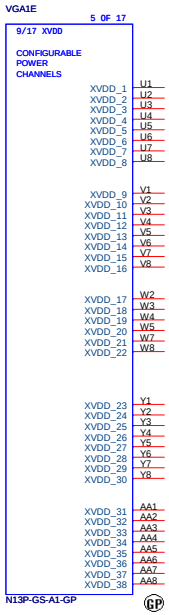




0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU



XVDD_1~38=No Connect

<Variant Name>

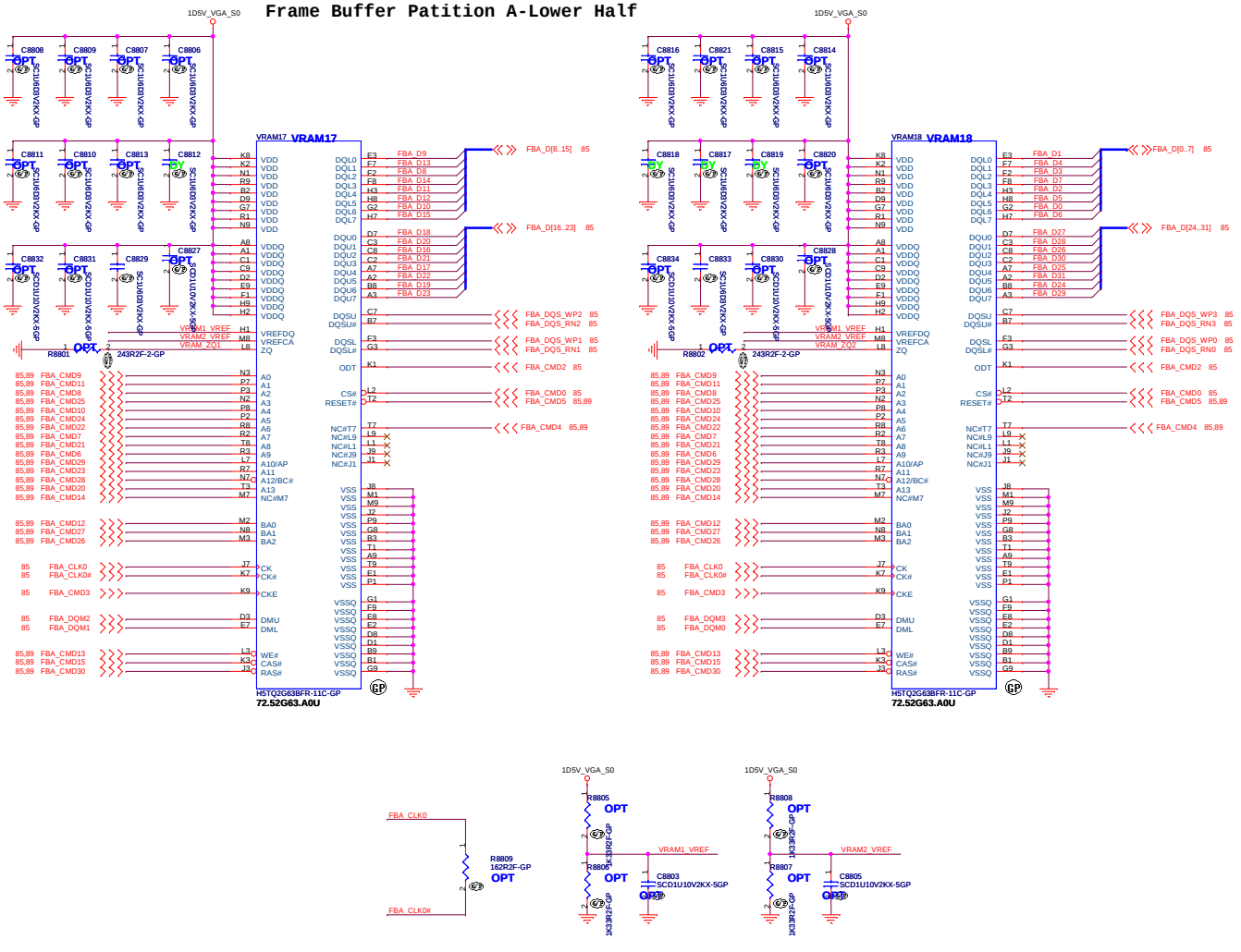
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
Custom	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 87 of 103

Frame Buffer Patition A-Lower Half



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

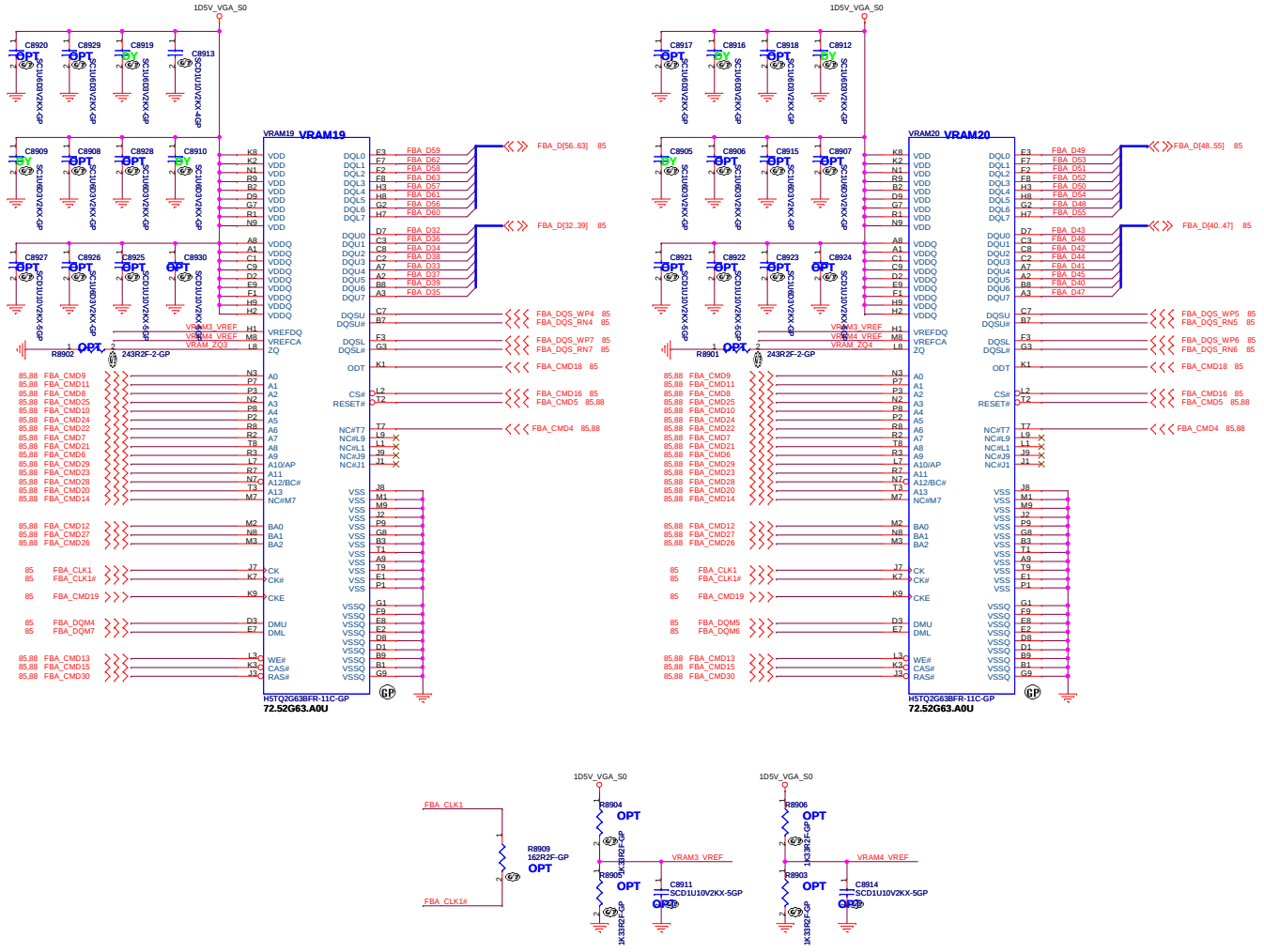
<Variant Name>

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 88 of 103

Frame Buffer Patition A-Upper Half



<Variant Name>

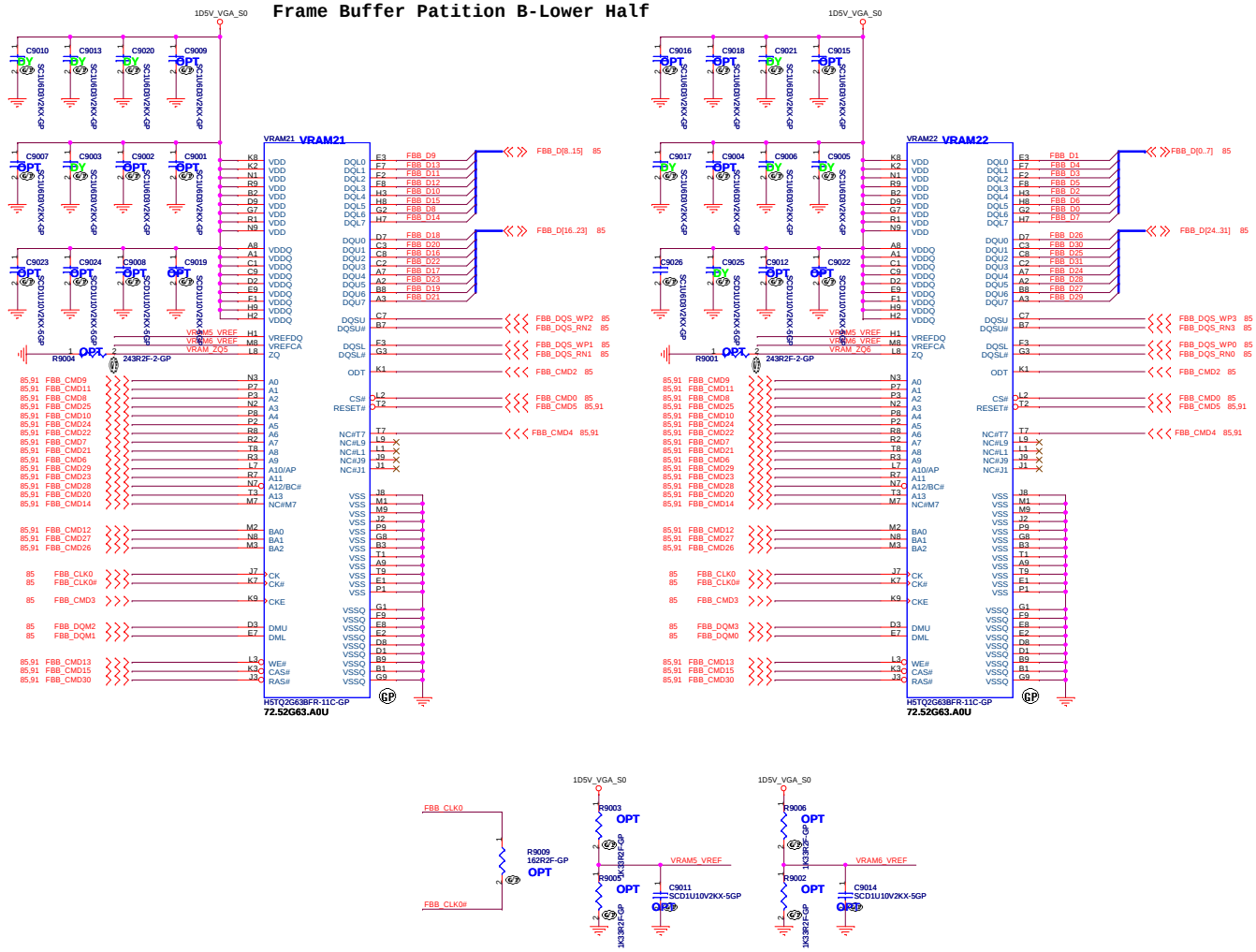
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 89 of 103

Frame Buffer Patition B-Lower Half



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

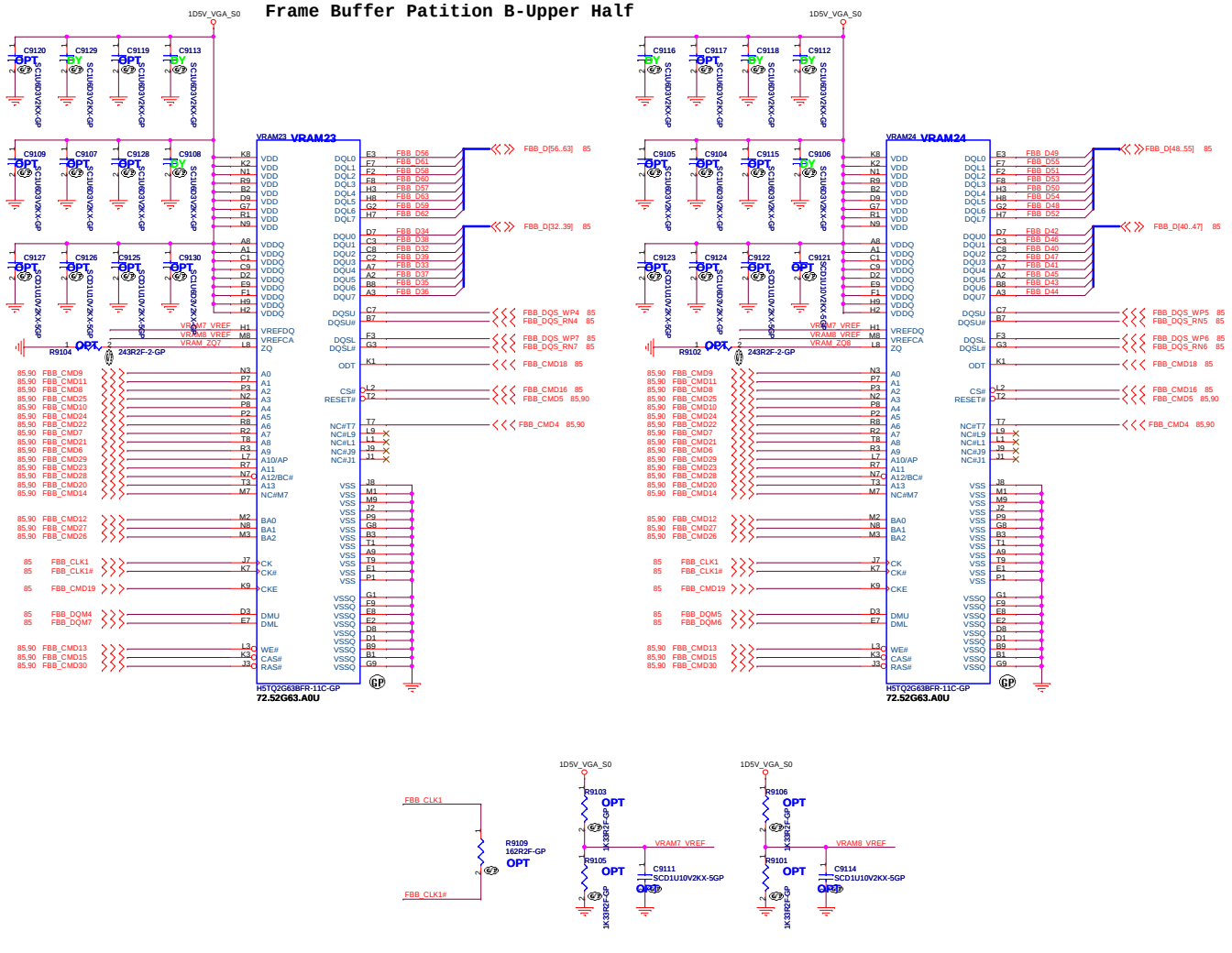
<variant_name>

Title: GPU-VRAM5,6 (3/4)

Size: A2 | Document Number: Colossus | Rev: 1

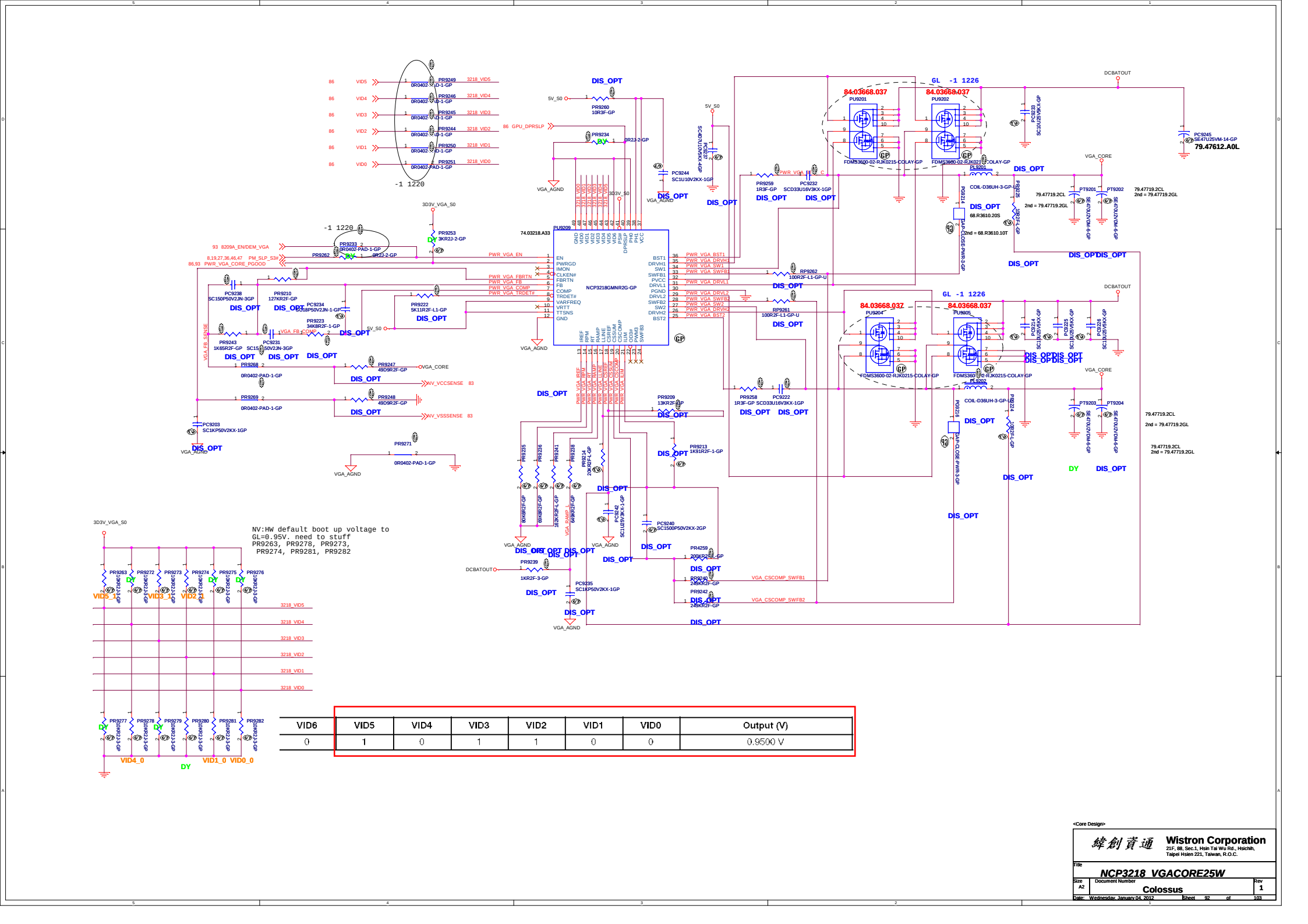
Date: Wednesday, January 04, 2012 | Sheet 90 of 103

Frame Buffer Patition B-Upper Half



<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU-VRAM7,8 (4/4)	
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 91 of 103	



VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	1	1	0	0	0.9500 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

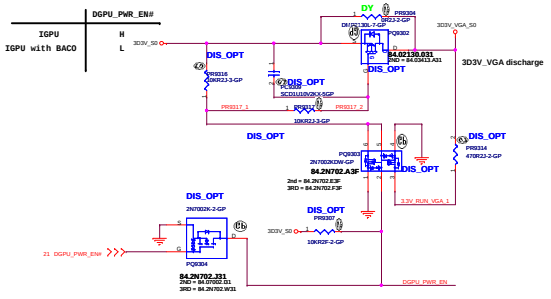
Title: **NCP3218 VGACORE25W**

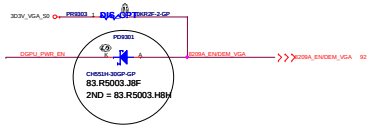
Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 92 of 103

VGA chip sequence: 3V_VGA_S0>VGA_CORE>1D5V_VGA>1D05V_VGA

3V_VGA_S0 → VGA_CORE → 1.5V_VGA_S0



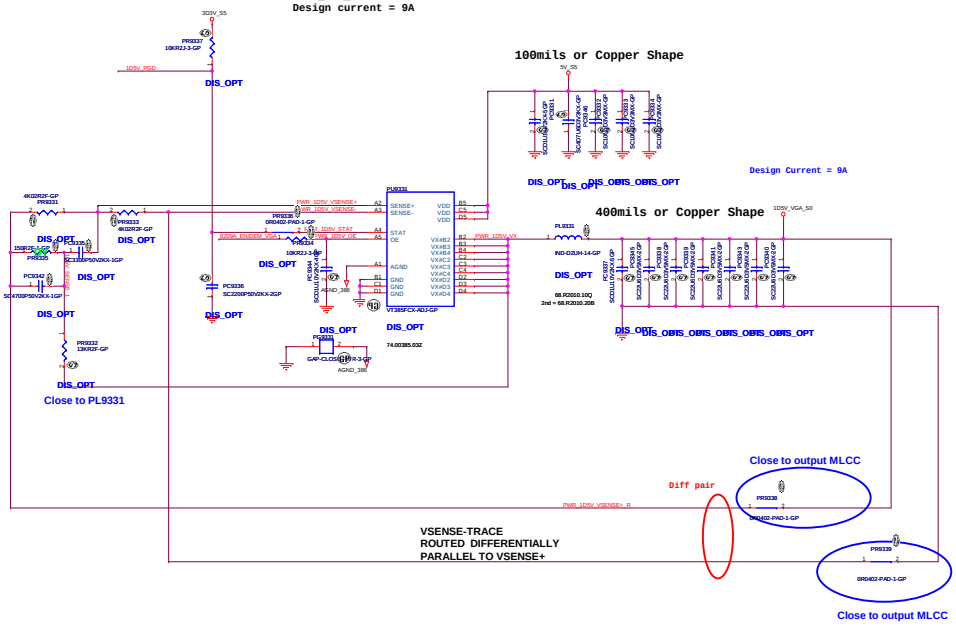


1D5V_VGA_S0
Design current = 9A

100mils or Copper Shape

400mils or Copper Shape

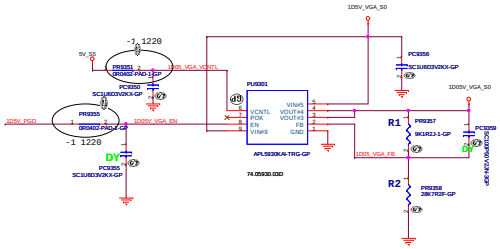
Design Current = 9A

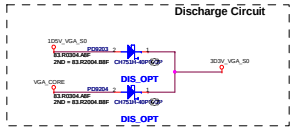


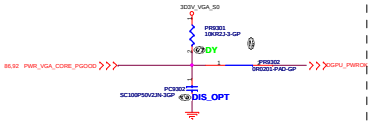
1D05V_VGA

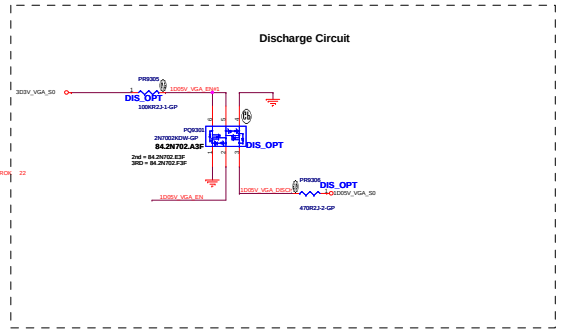
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp up
so 1D05V_VGA_S0 EN have to fine tune RC delay after VGA_Core

1D05V_VGA_S0
Design current = 3.8A









<Core Design>
蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER
Size: A1
Document Number: Colossus
Rev: 1
Date: Wednesday, January 04, 2012
Sheet 88 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 94 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 95 of 103

(Blanking)

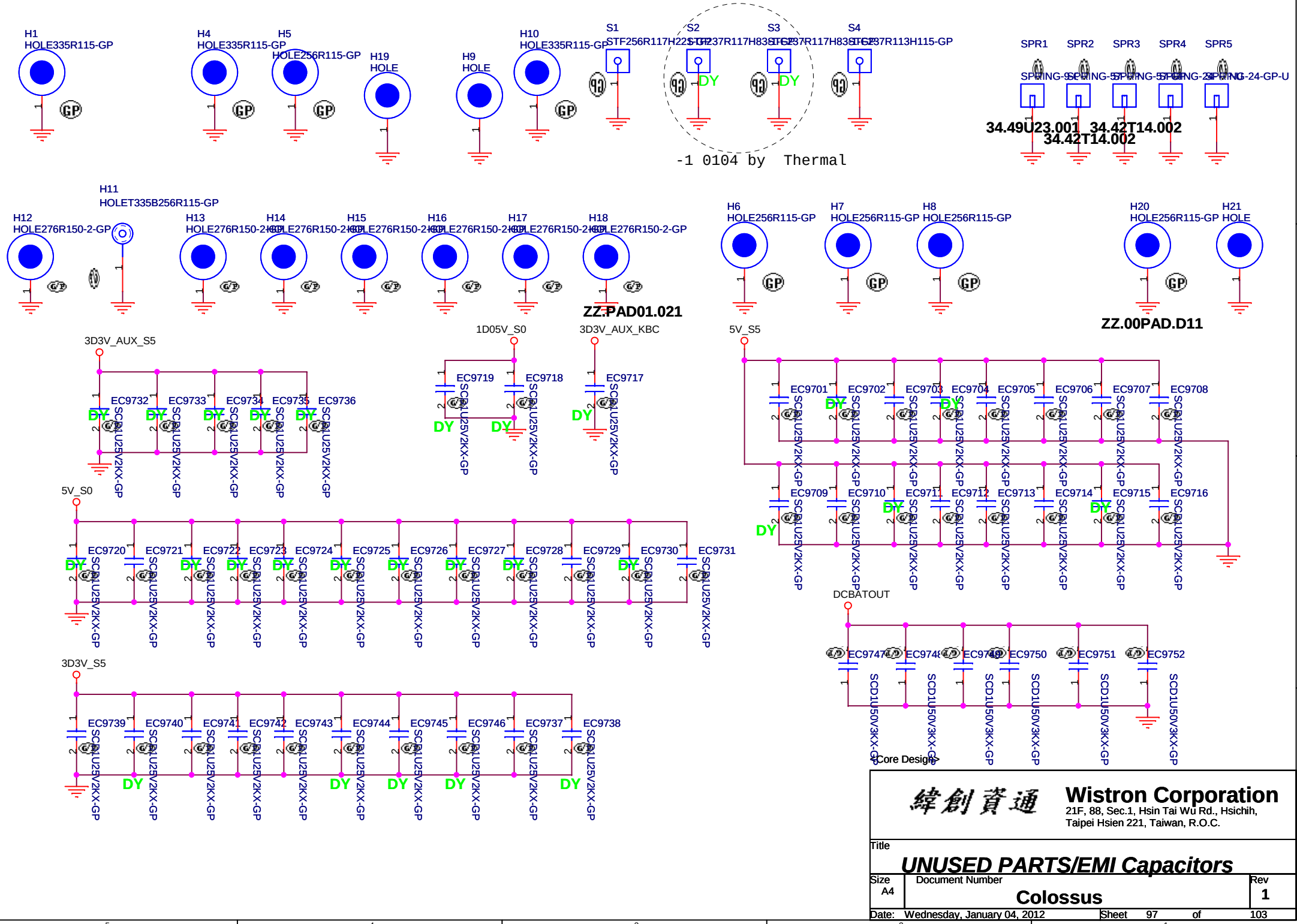
<Core Design>

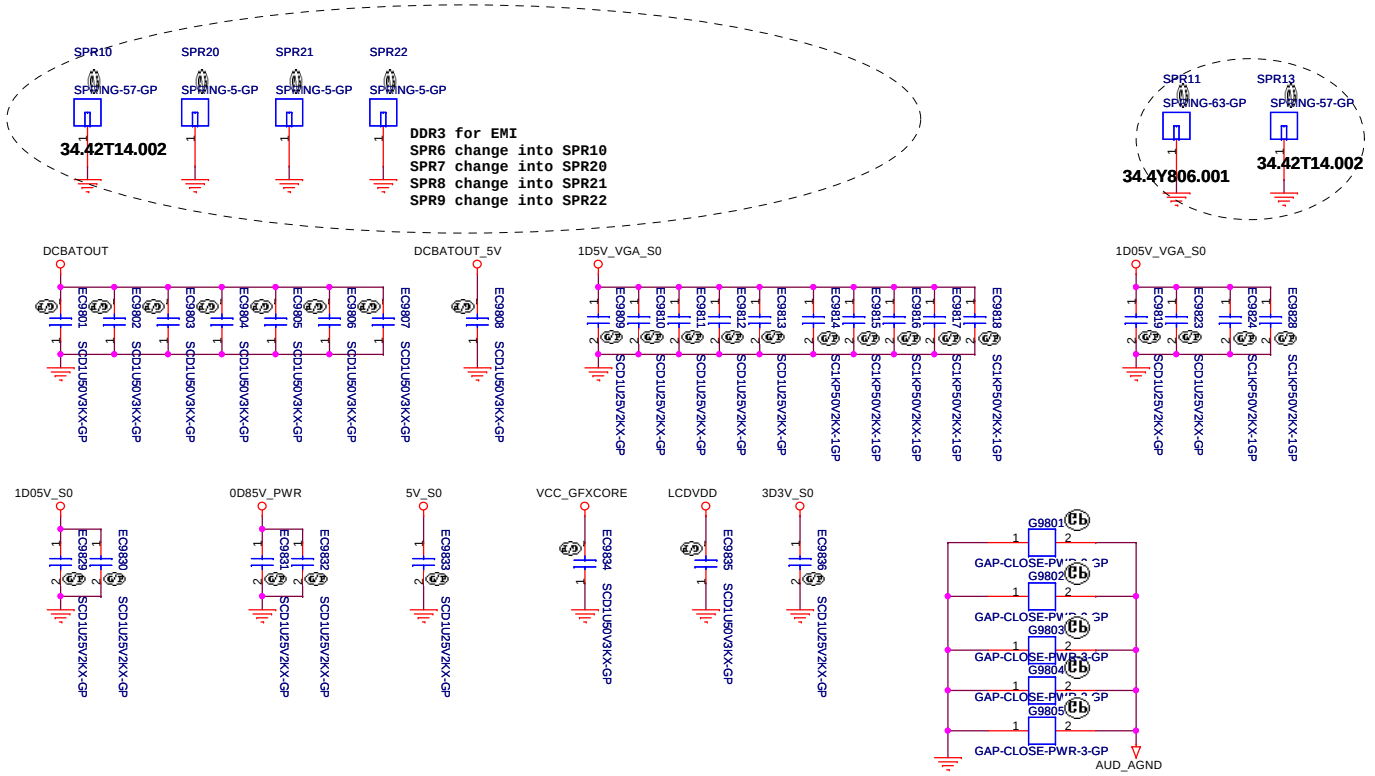
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 96 of 103


H1
HOLE335R115-GP
H4
HOLE335R115-GP
H5
HOLE256R115-GP
H19
HOLE
H9
HOLE
H10
HOLE335R115-GP
S1
S2
S3
S4
-1 0104 by Thermal
SPR1
SPR2
SPR3
SPR4
SPR5
34.49U23.001
34.42T14.002
34.42T14.002
H11
HOLET335B256R115-GP
H12
HOLE276R150-2-GP
H13
H14
H15
H16
H17
H18
ZZ.PAD01.021
H6
HOLE256R115-GP
H7
HOLE256R115-GP
H8
HOLE256R115-GP
H20
HOLE256R115-GP
H21
HOLE
ZZ.00PAD.D11
3D3V_AUX_S5
EC9732
EC9733
EC9734
EC9735
EC9736
1D05V_S0
EC9719
EC9718
3D3V_AUX_KBC
EC9717
5V_S5
EC9701
EC9702
EC9703
EC9704
EC9705
EC9706
EC9707
EC9708
EC9709
EC9710
EC9711
EC9712
EC9713
EC9714
EC9715
EC9716
5V_S0
EC9720
EC9721
EC9722
EC9723
EC9724
EC9725
EC9726
EC9727
EC9728
EC9729
EC9730
EC9731
DCBATOUT
EC9747
EC9748
EC9749
EC9750
EC9751
EC9752
3D3V_S5
EC9739
EC9740
EC9741
EC9742
EC9743
EC9744
EC9745
EC9746
EC9737
EC9738
DY
SCD1U25V2KX-GP
SCD1U50V3KX-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size
A4
Document Number
Colossus
Rev
1
Date: Wednesday, January 04, 2012
Sheet 97 of 103



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

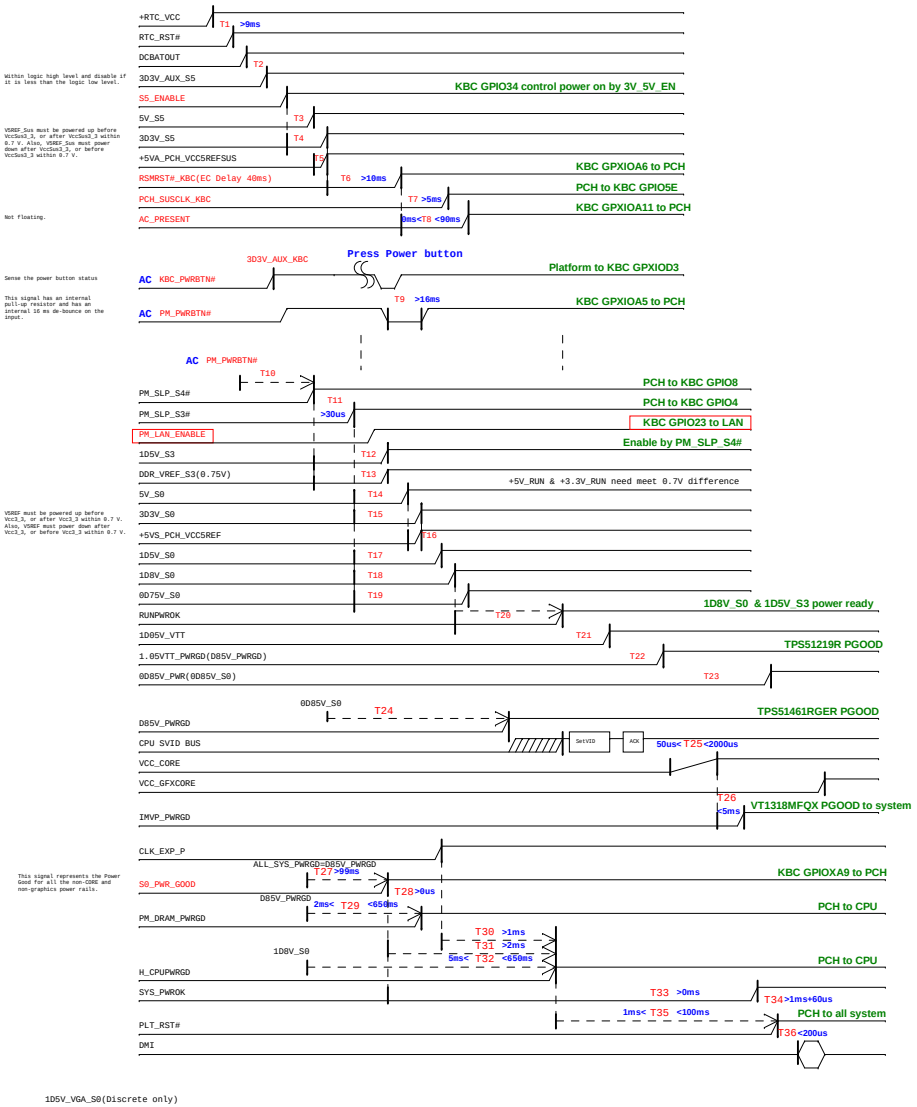
Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 98 of 103

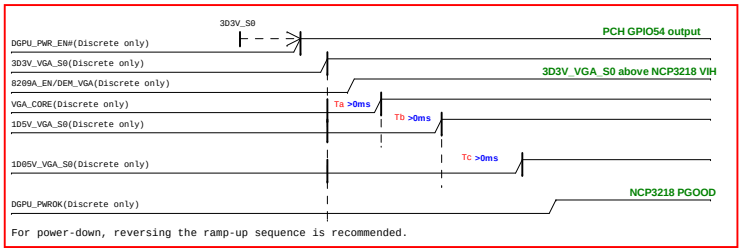
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO



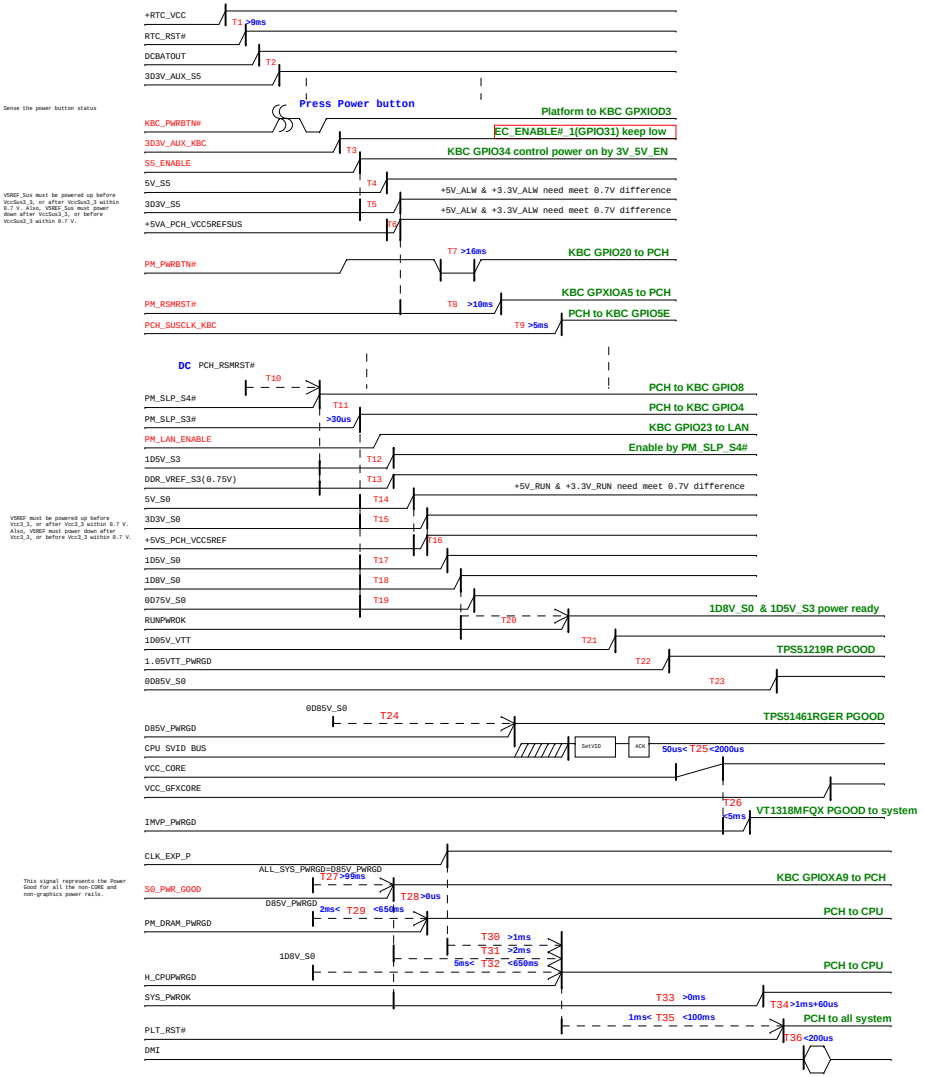
N13P Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



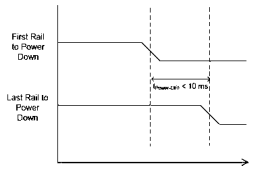
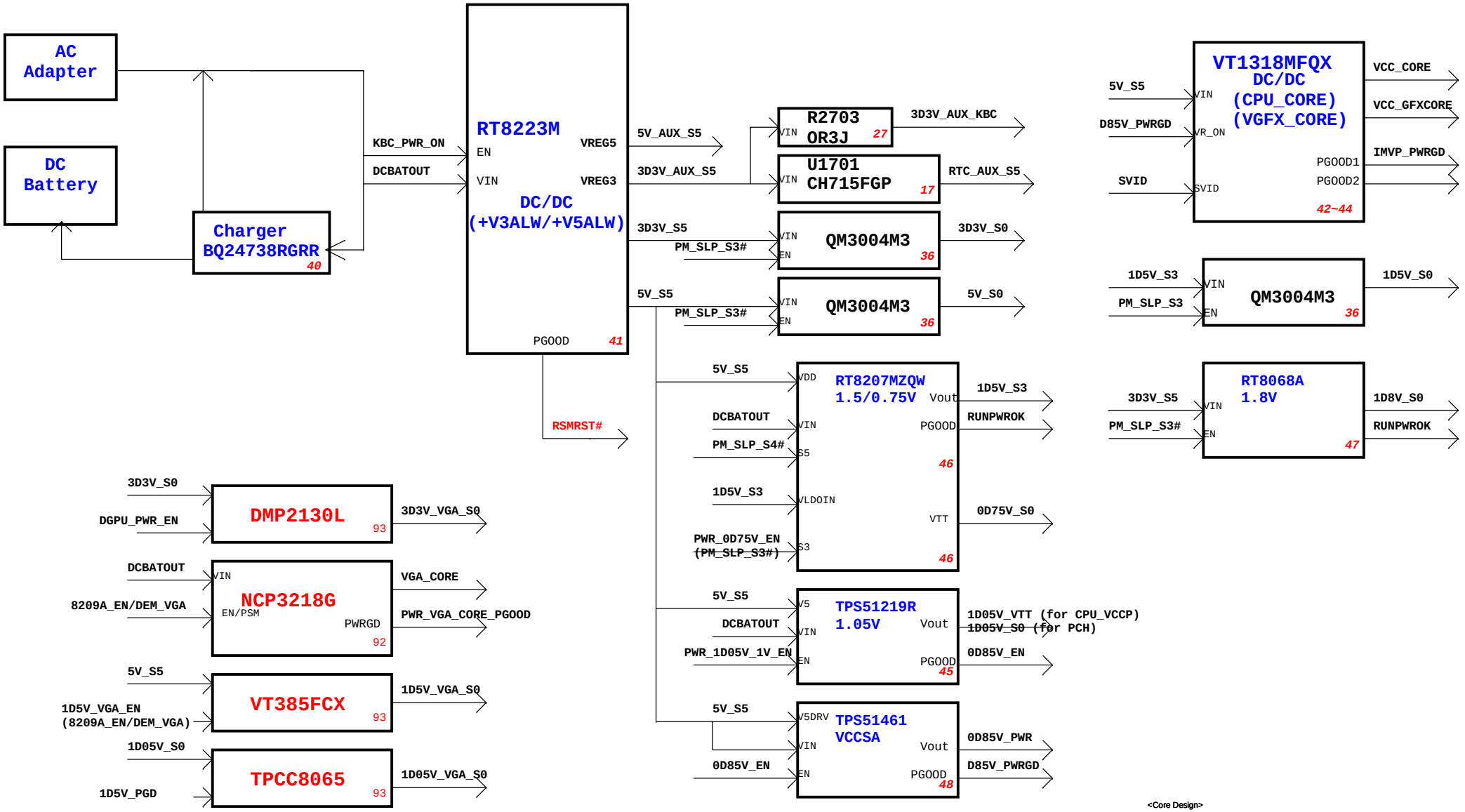


Figure 18. Recommended Power Off Sequencing Order

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Power Sequence
Size: A1 | Document Number: Colossus | Rev: 1
Date: Monday, December 26, 2011 | Sheet 59 of 103

COLOSUSS POWER BLOCK DIAGRAM

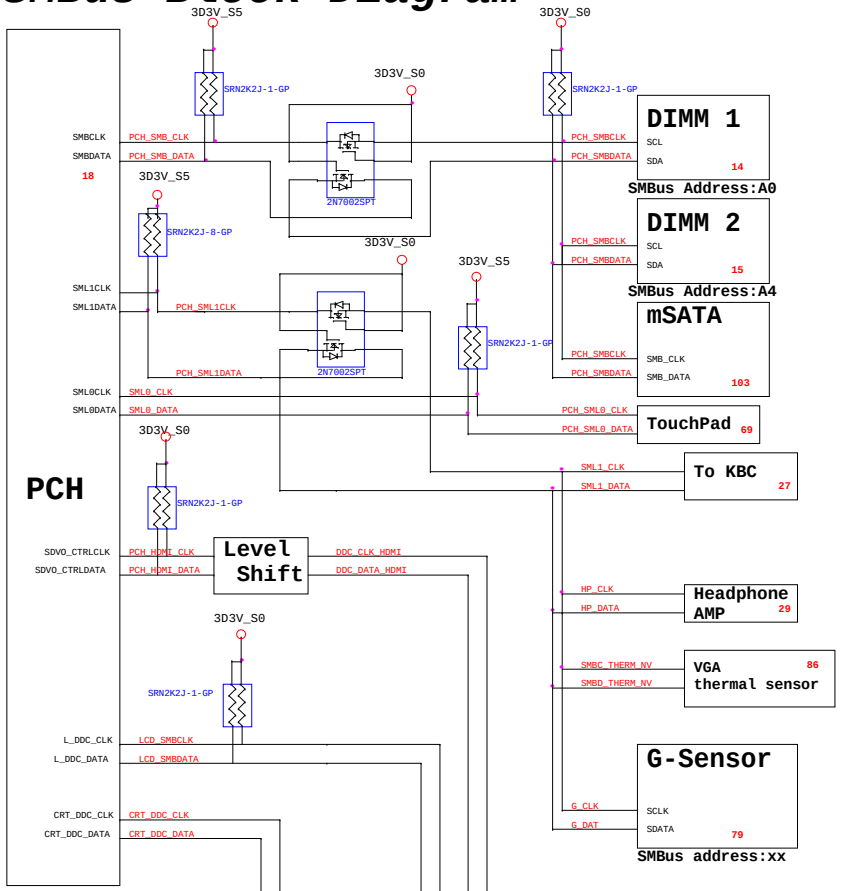


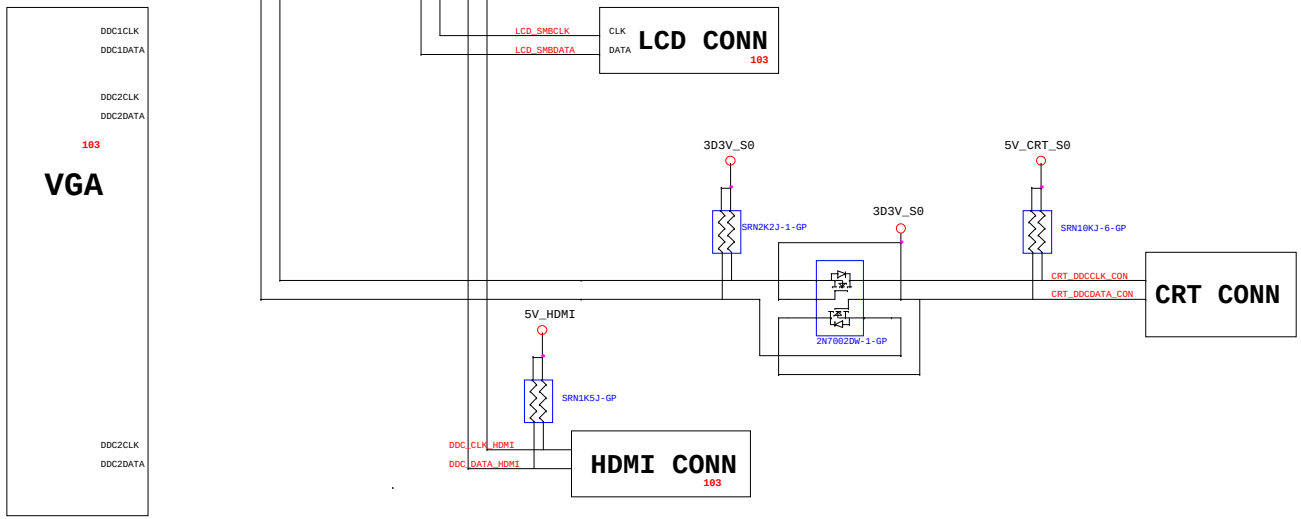
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

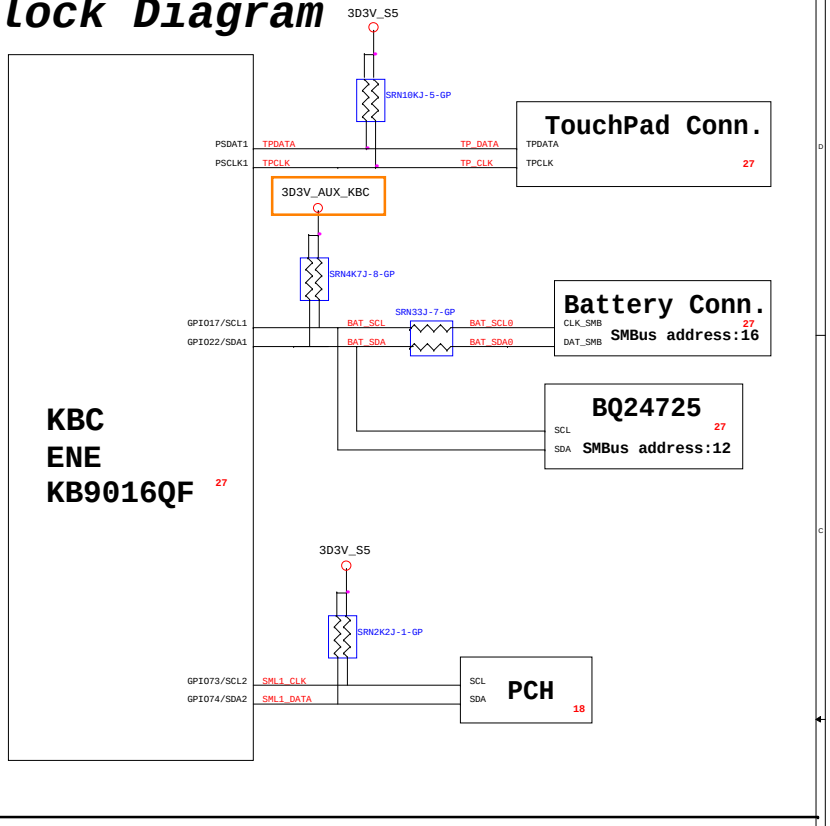
Title	Power Block Diagram	
Size A3	Document Number Colossus	Rev 1
Date: Monday, December 26, 2011	Sheet 100 of 103	

PCH SMBus Block Diagram





KBC SMBus Block Diagram



<Core Design>

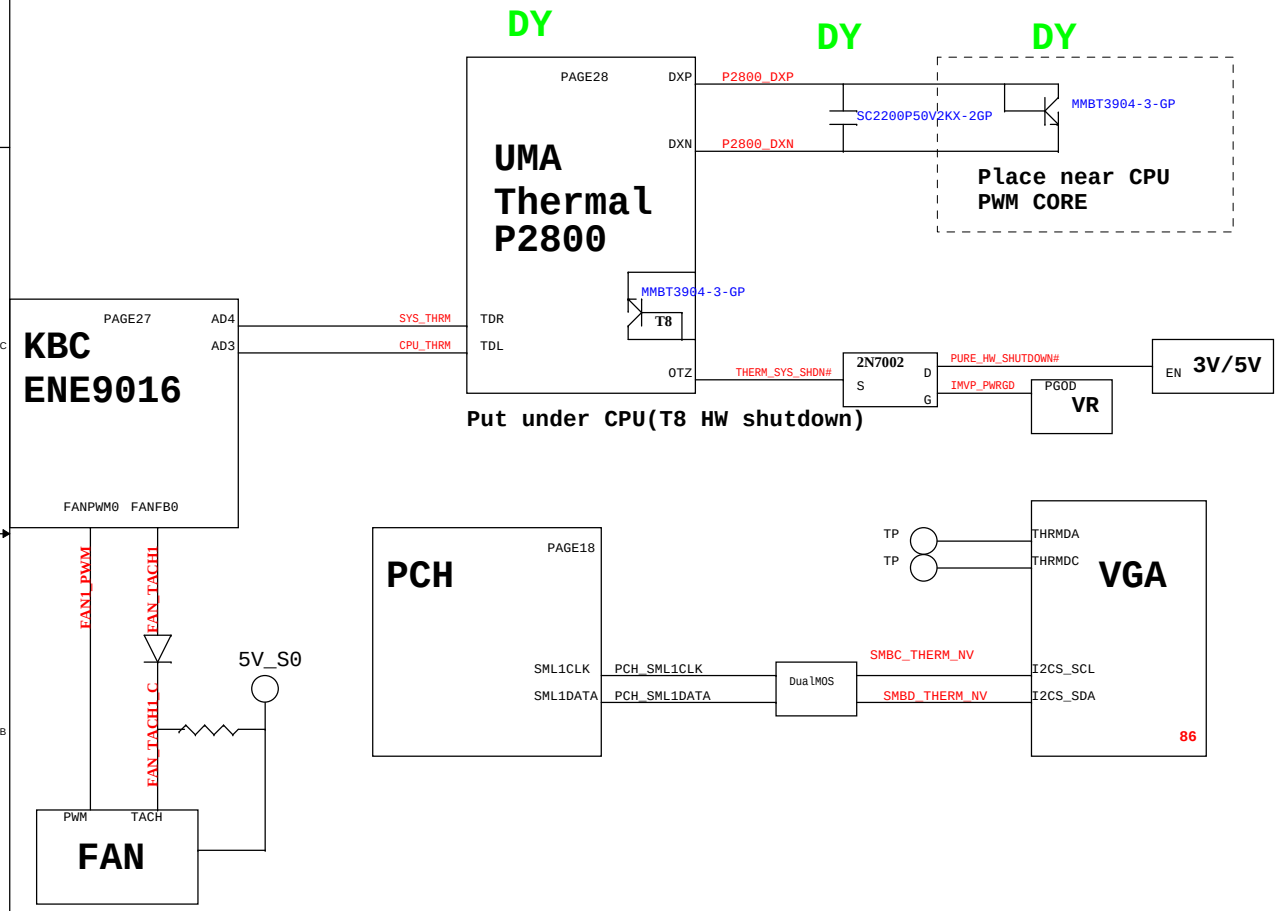
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

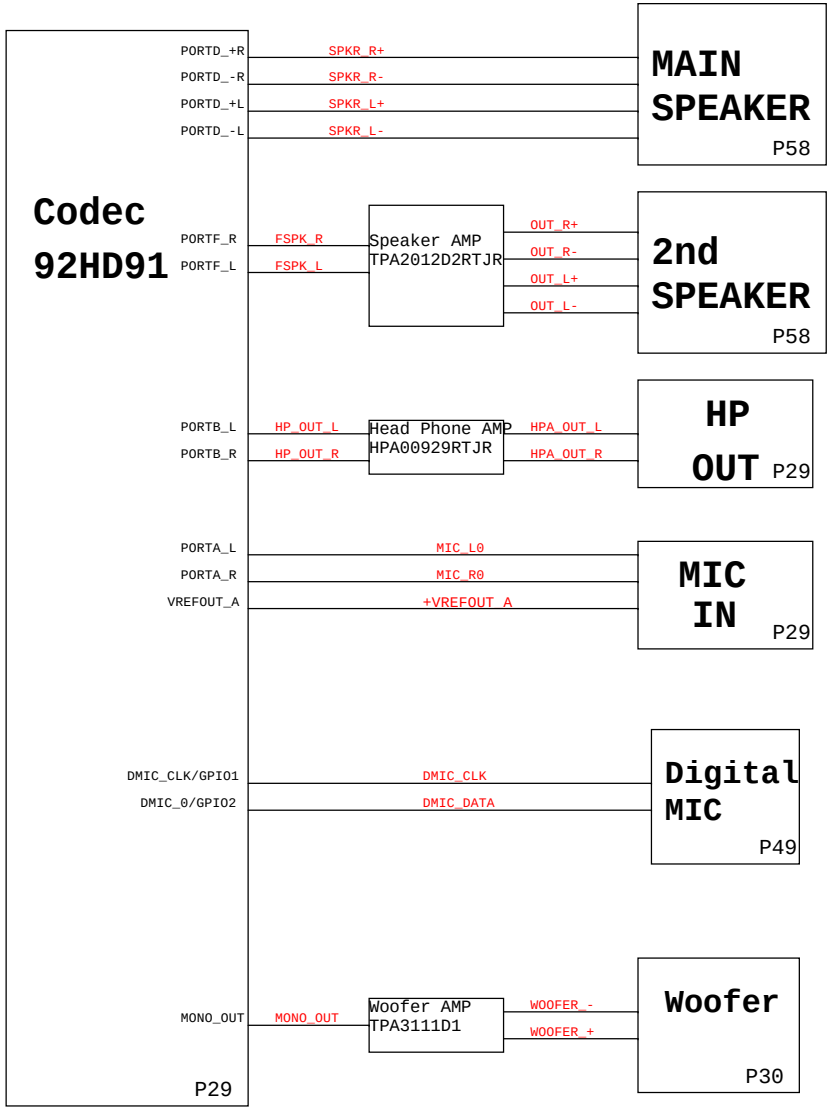
Size	Document Number	Rev
A2	Colossus	1

Date: Monday, December 26, 2011 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram



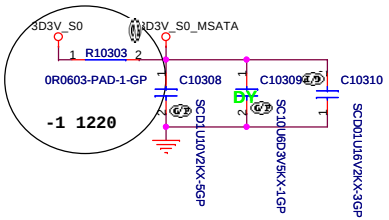
<Core Design>

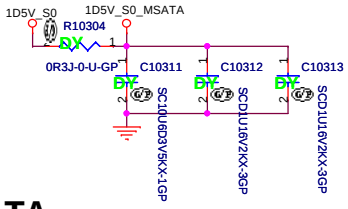
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

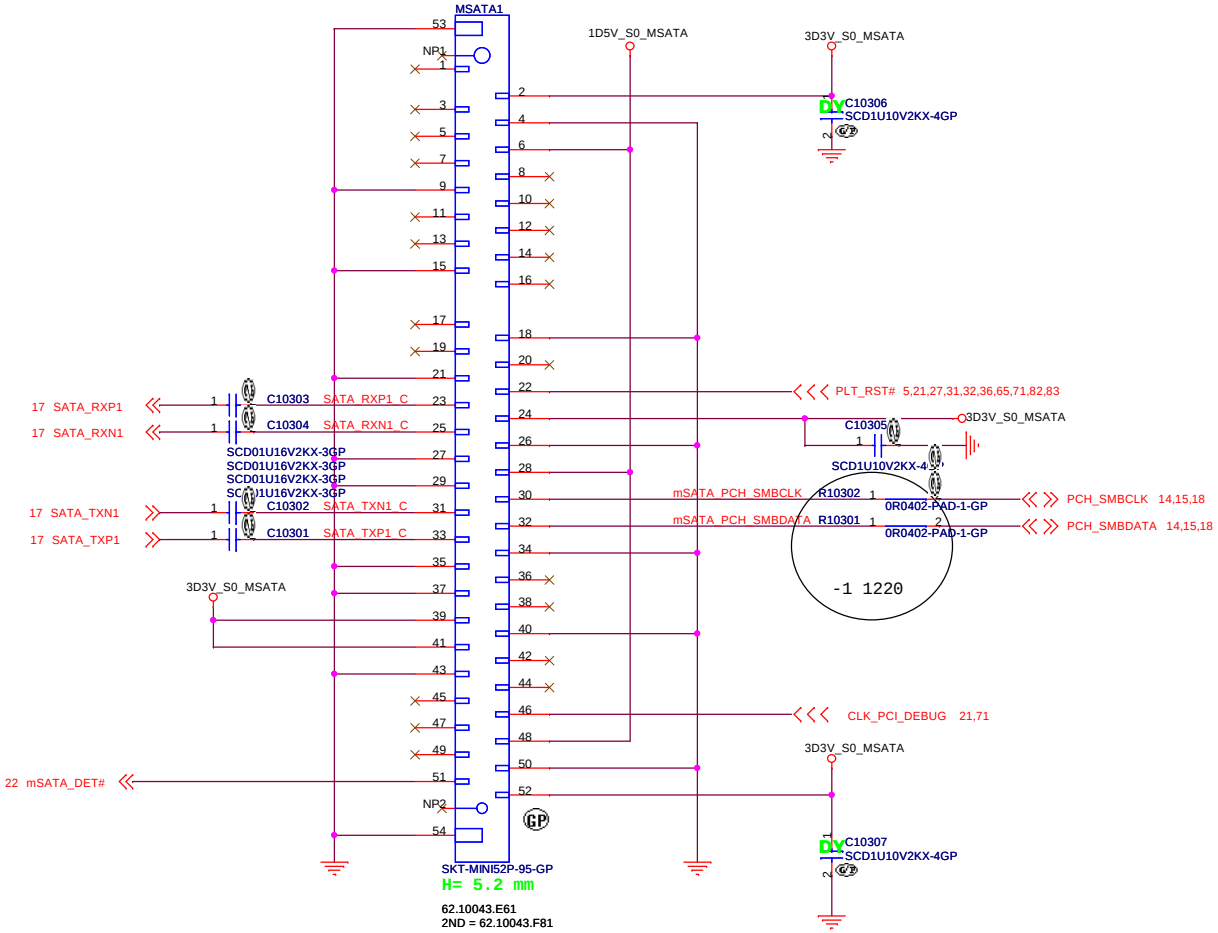
Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 102 of 103





mSATA



677867-FM5

Pin #	Name	Description		Pin #	Name	Description
1	Reserved	NC		2	V33	3.3V power
3	Reserved	NC		4	GND	Return Current Path
5	Reserved	NC		6	V15	1.5V power (Unused)
7	Reserved	NC		8	Reserved	NC
9	GND	Return Current Path		10	Reserved	NC
11	Reserved	NC		12	Reserved	NC
13	Reserved	NC		14	Reserved	NC
15	GND	Return Current Path		16	Reserved	NC
Key						
17	Reserved	NC		18	GND	Return Current Path
19	Reserved	NC		20	Reserved	NC
21	GND	Return Current Path		22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)		24	V33	3.3V power
25	B-			26	GND	Return Current Path
27	GND	Return Current Path		28	V15	1.5V power (Unused)
29	GND	Return Current Path		30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)		32	Reserved	NC
33	A+			34	GND	Return Current Path
35	GND	Return Current Path		36	Reserved	NC
37	GND	Return Current Path		38	Reserved	NC
39	V33	3.3V power		40	GND	Return Current Path
41	V33	3.3V power		42	Reserved	NC
43	GND	Return Current Path		44	Reserved	NC
45	Vendor	No connect at Host side		46	Reserved	NC
47	Vendor	No connect at Host side		48	V15	1.5V power (Unused)
49	DAS/DSS*1	Drive Activity Signal		50	GND	Return Current Path
51	Presense*2	Device Presense		52	V33	3.3V power

Note: *1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220Ω Pull Down)

1st	677867-FM5
2nd	677867-AM5
3rd	677867-BM5
4th	677867-LM5

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 103 of 103