

Arsenal DJ1 Discrete Schematics Document

Arrandale

Intel PCH

2010-05-03

REV : A01

DY : Nopop Component

PARK : Pop when schematic is PARK-LP Component

M92 : Pop when schematic is M92-LP Component

DISCRETE PARK



Wistron Corporation
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Title

Cover Page

Size
A3

Document Number

Arsenal DJ1 Discrete

Rev

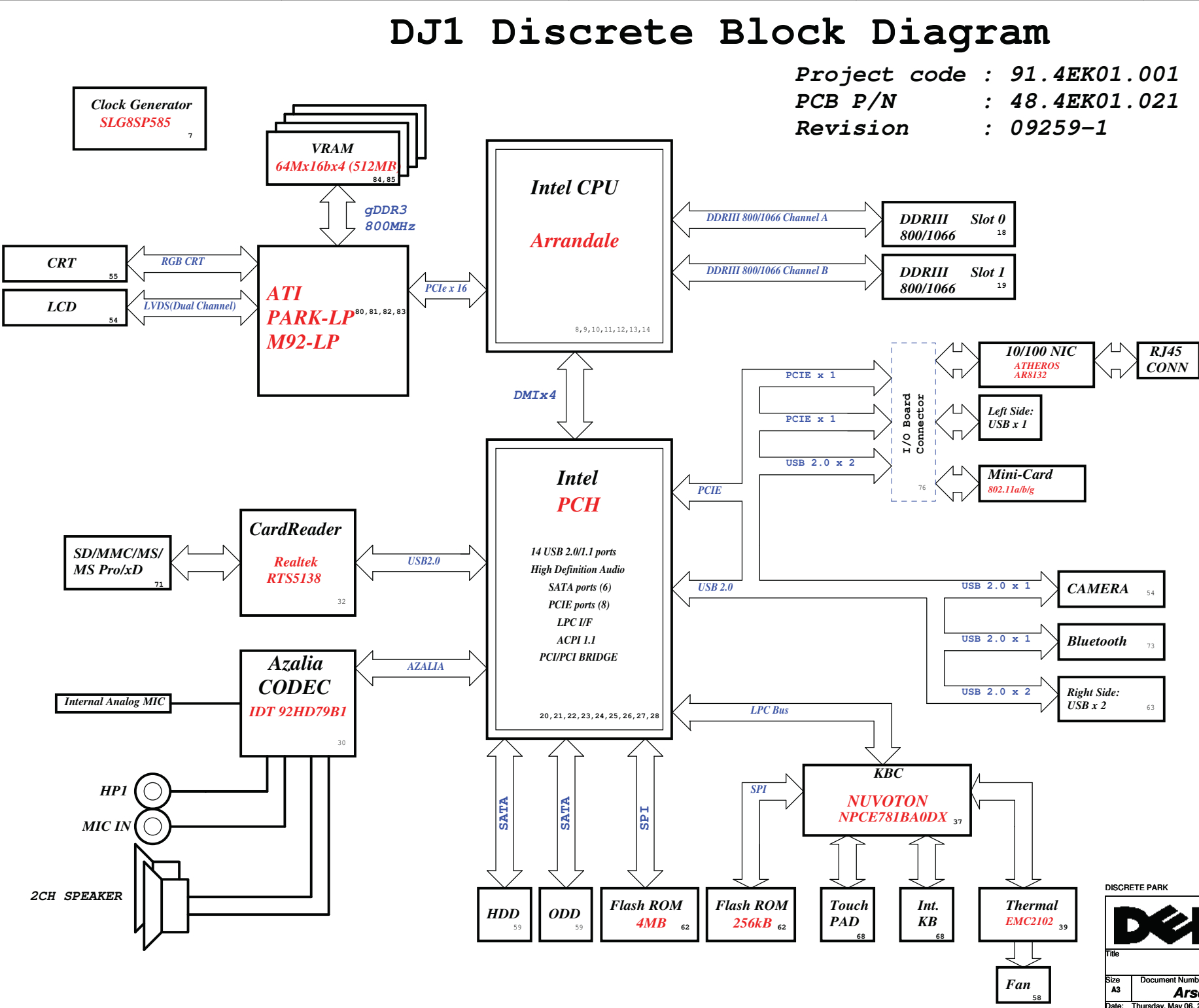
A01

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DJ1 Discrete Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK01.021
Revision : 09259-1



CPU DC/DC	
ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC	
RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC	
RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC	
APL5930KAI 88	
INPUTS	OUTPUTS
+1.5V_SUS	+1.1V_RUN
VGA	
RT8208BGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC GFX_CORE
MAXIM CHARGER	
BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

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Block Diagram

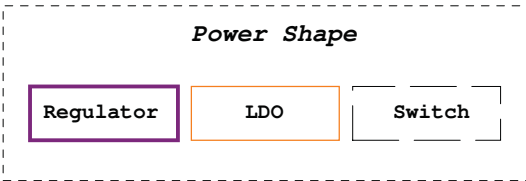
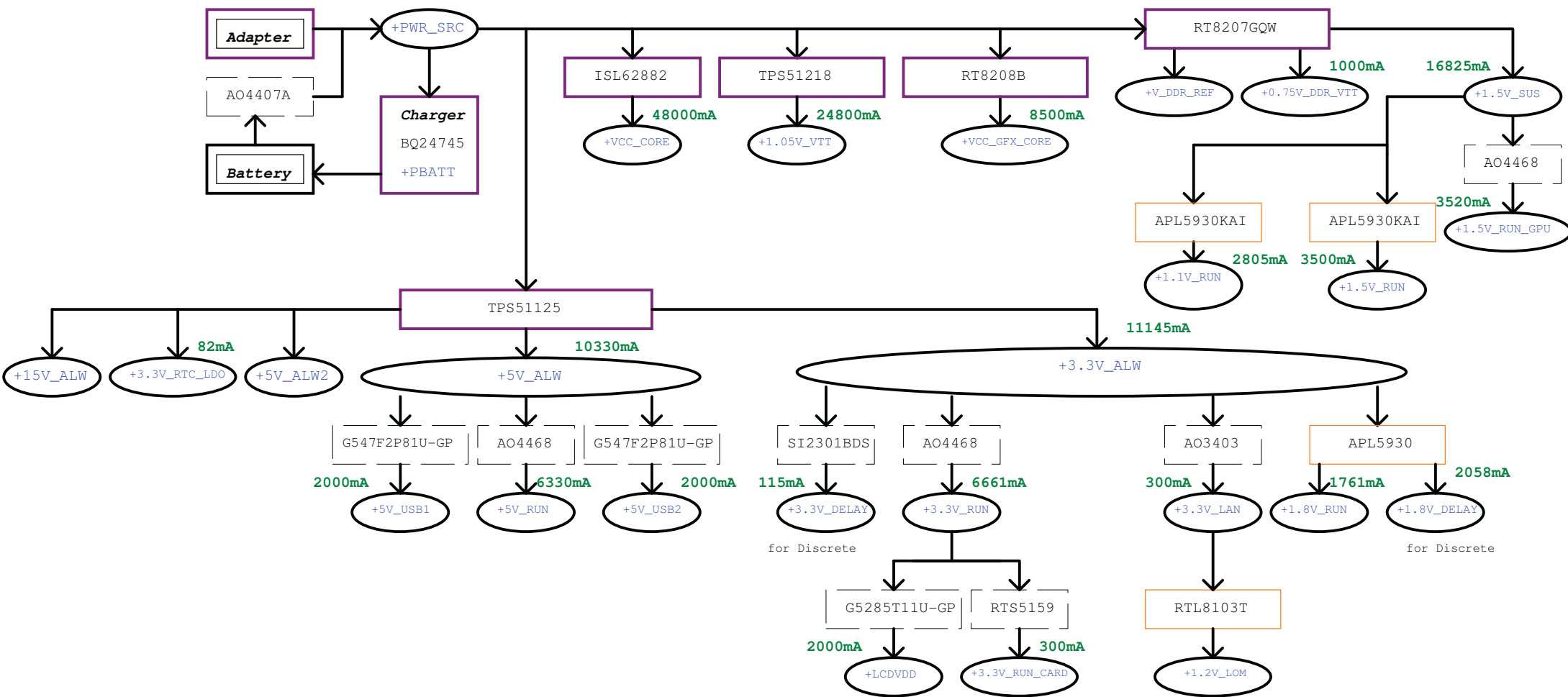
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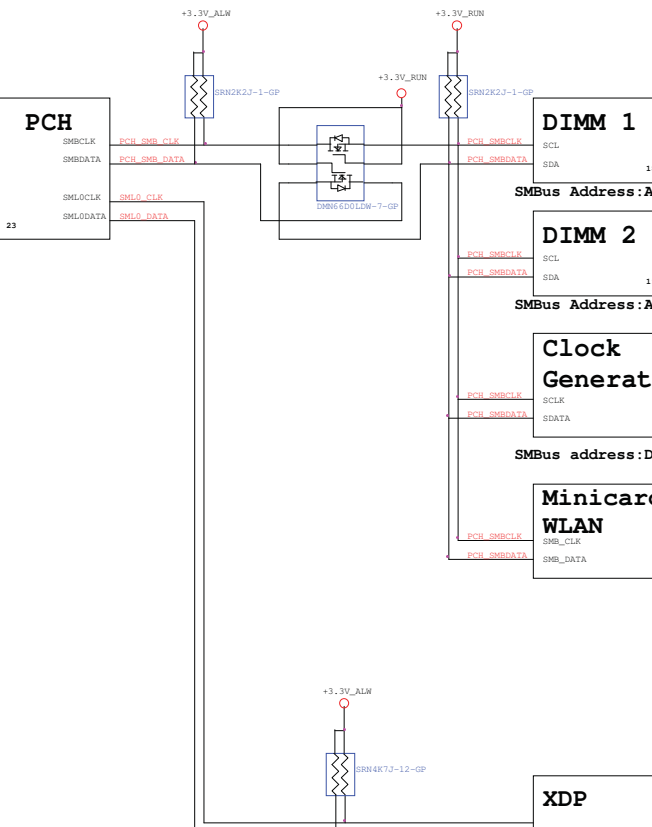
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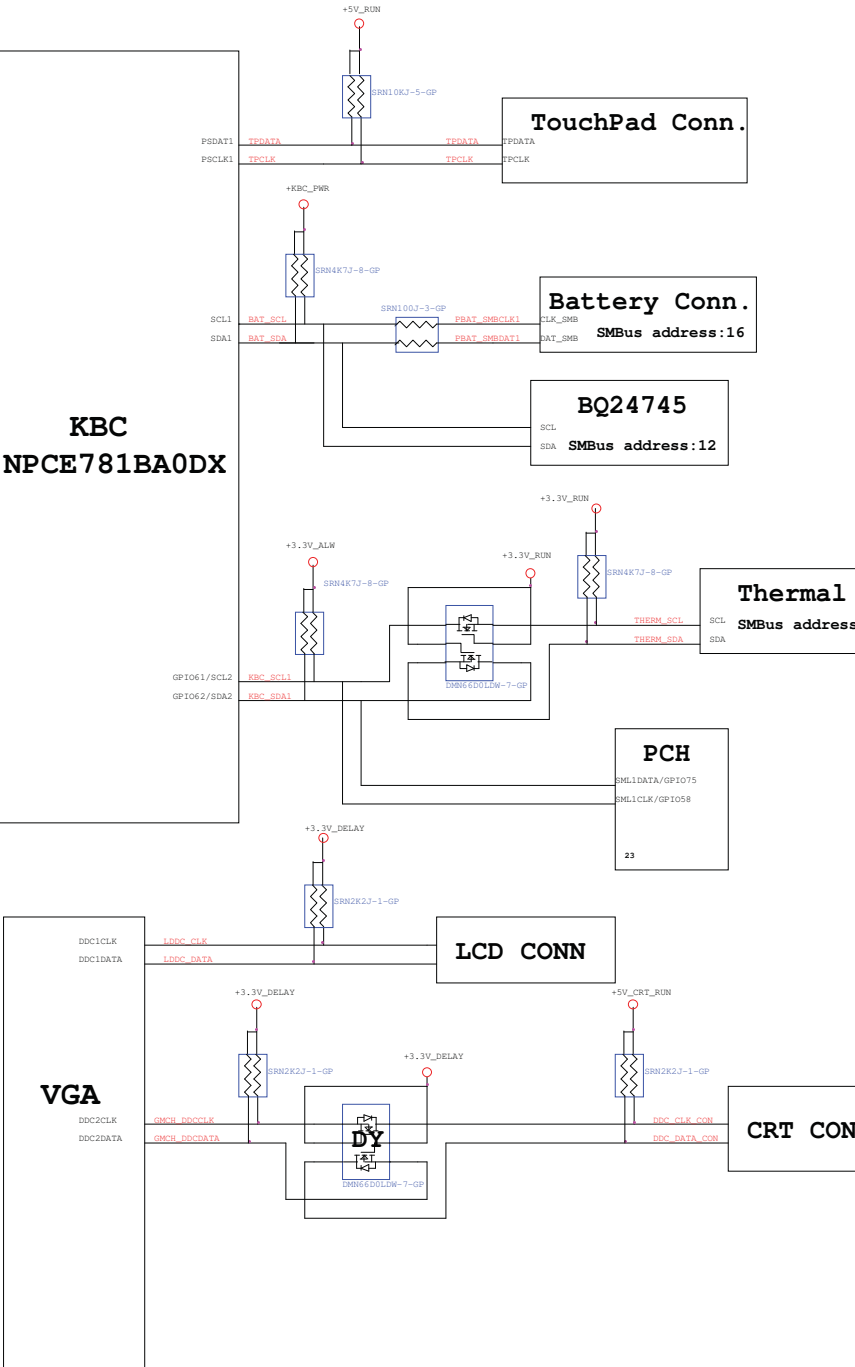
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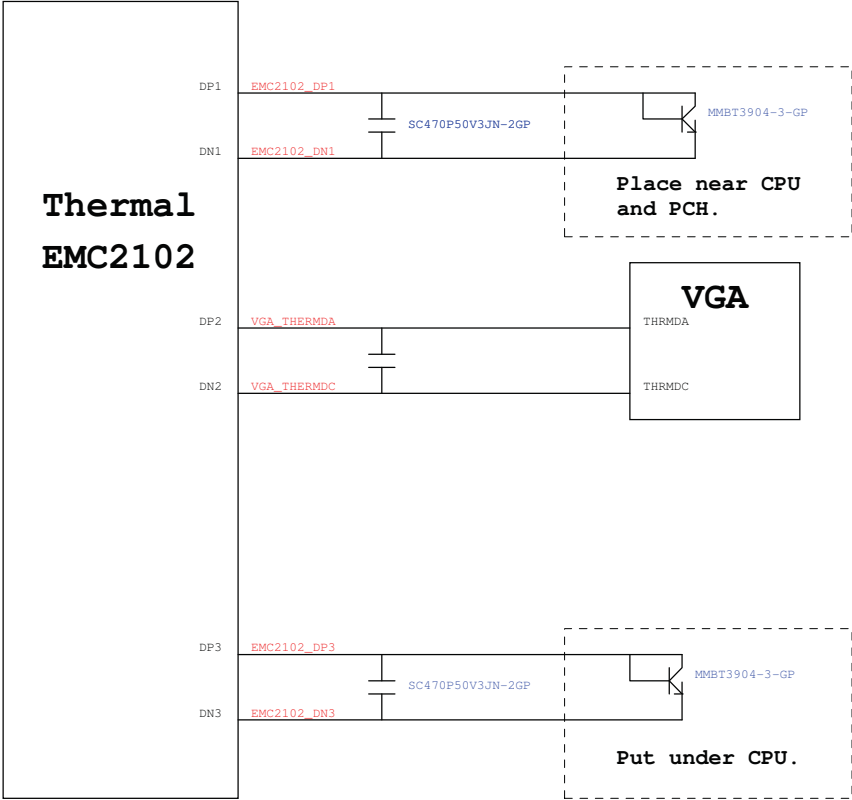
PCH SMBus Block Diagram



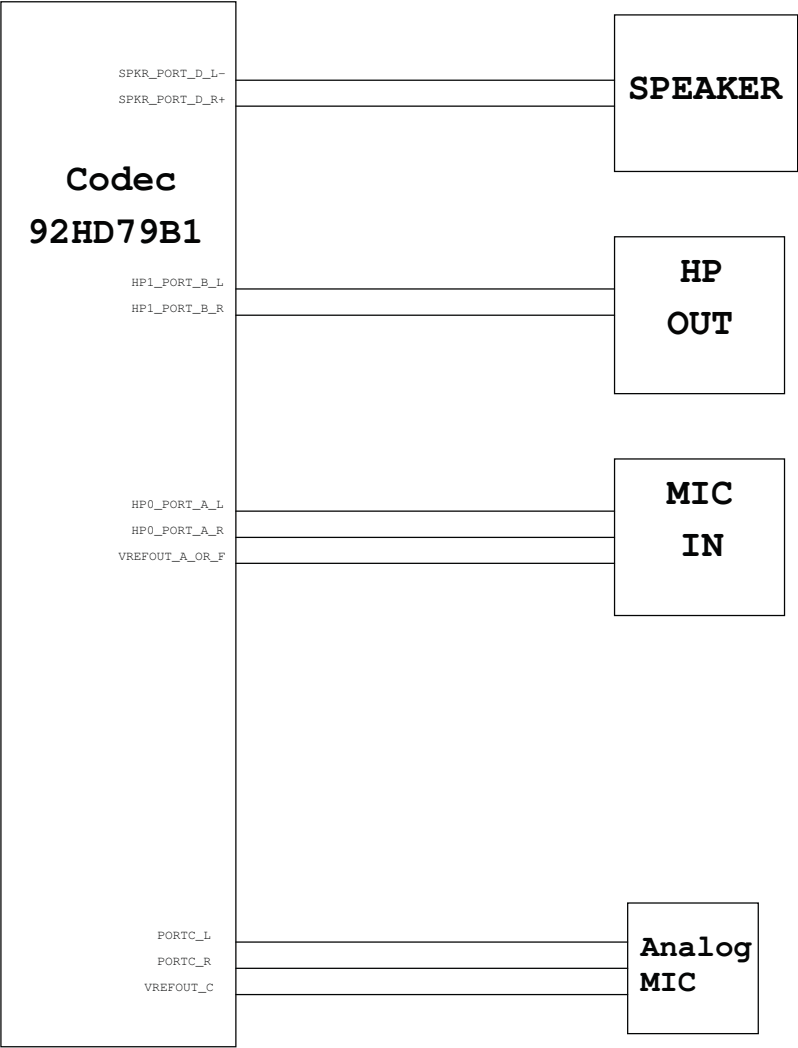
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table


USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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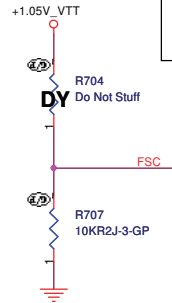
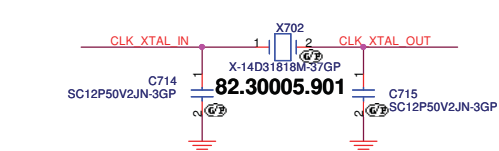
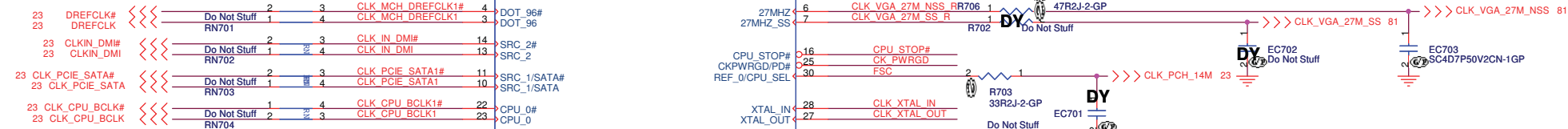
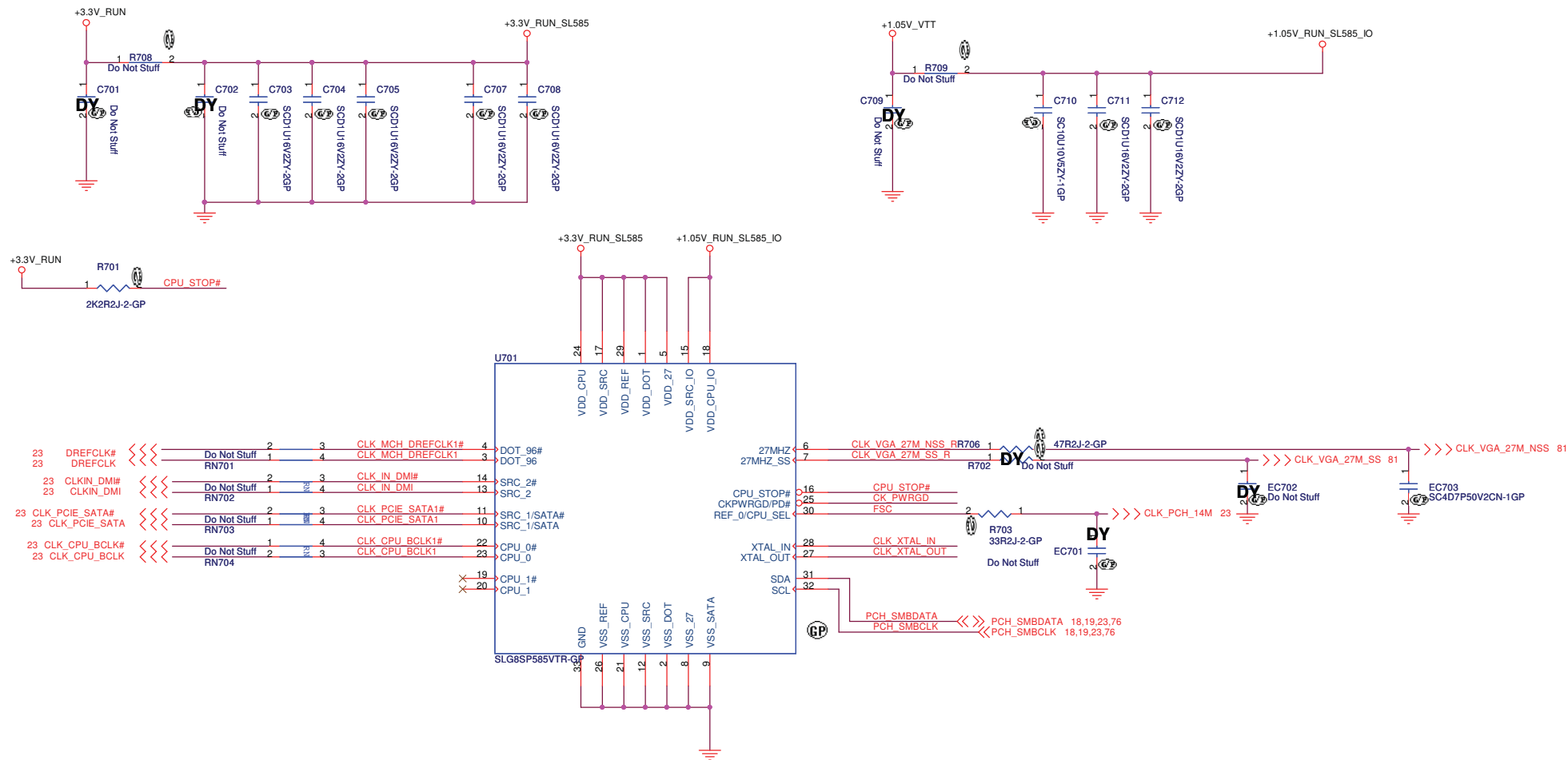
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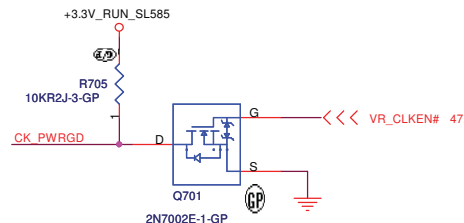
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SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz



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Clock Generator SLG8SP585

Size

Document Number

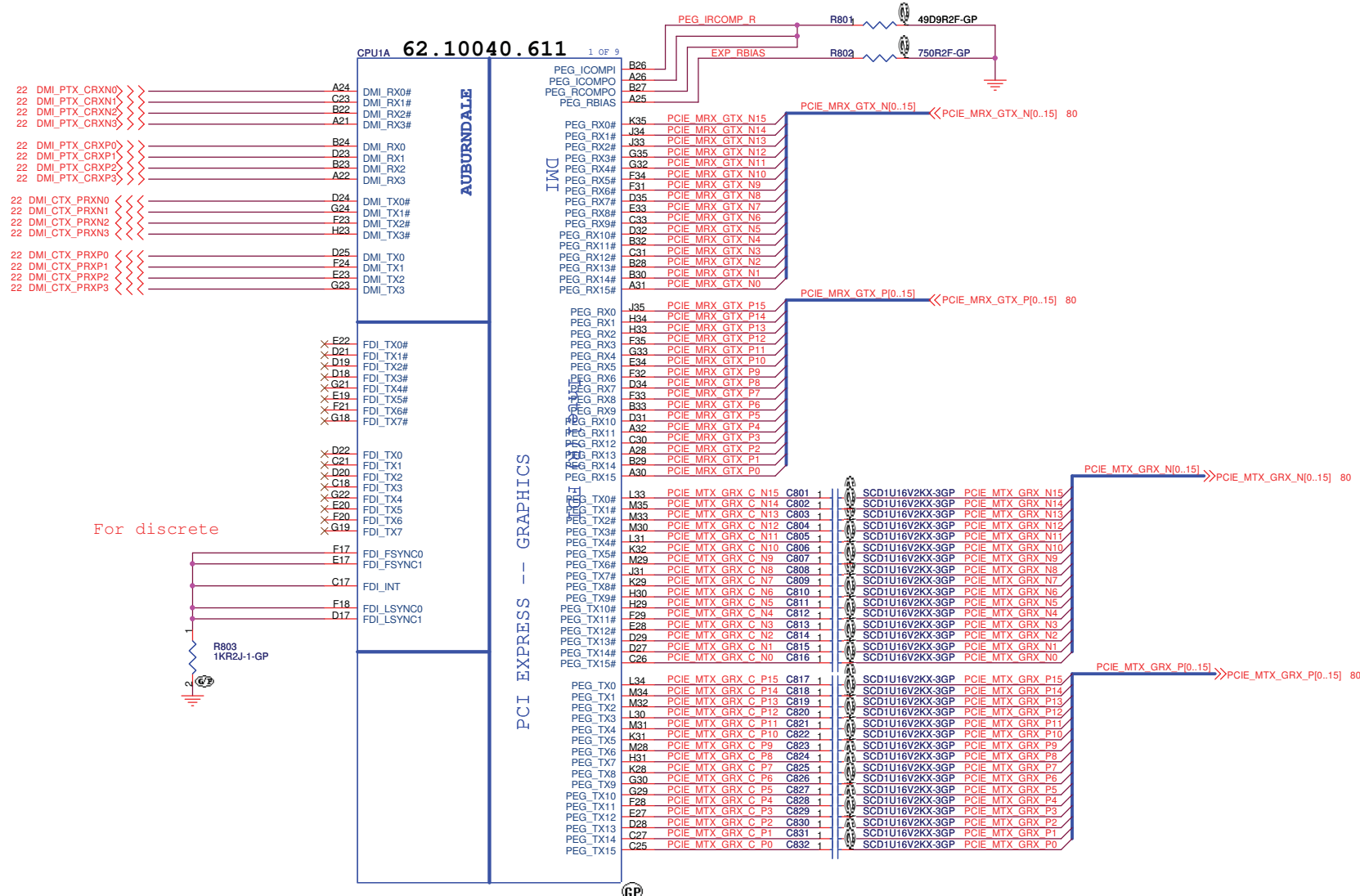
Rev

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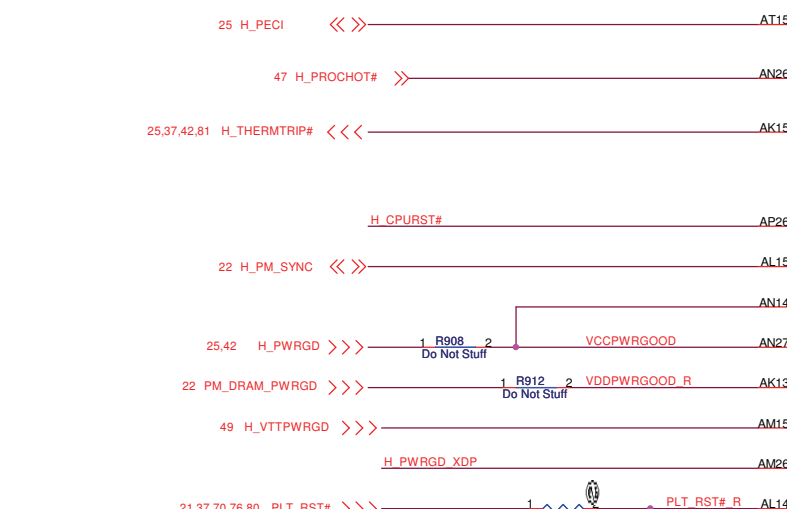
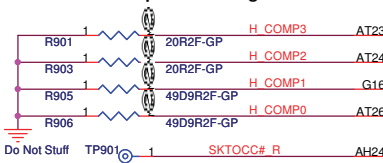
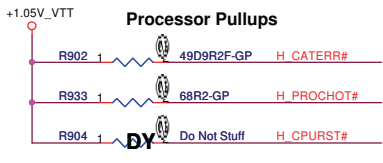
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SSID = CPU

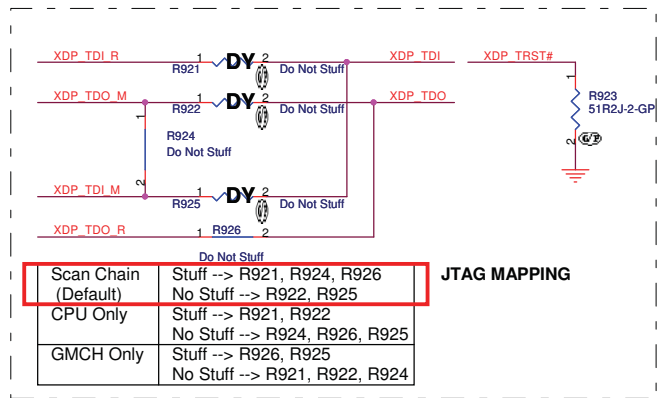
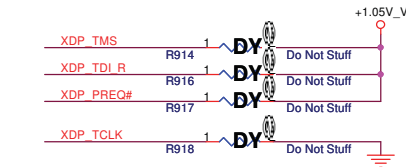
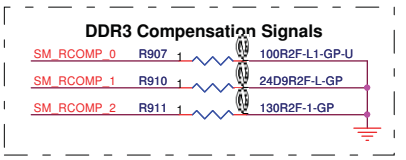
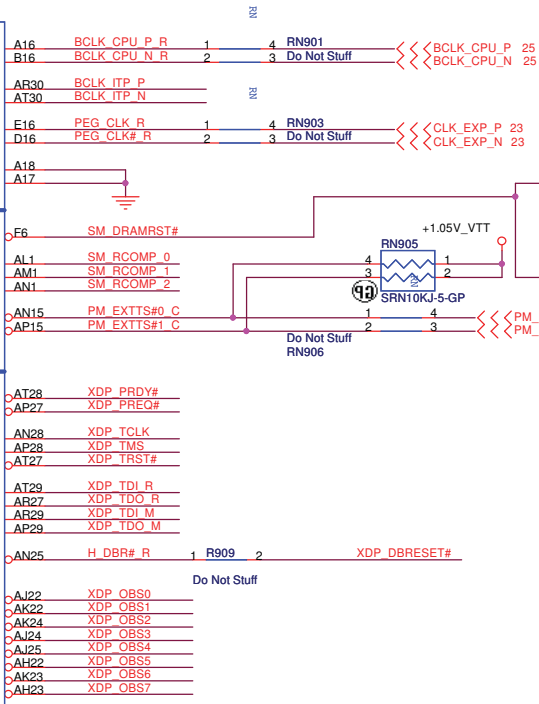
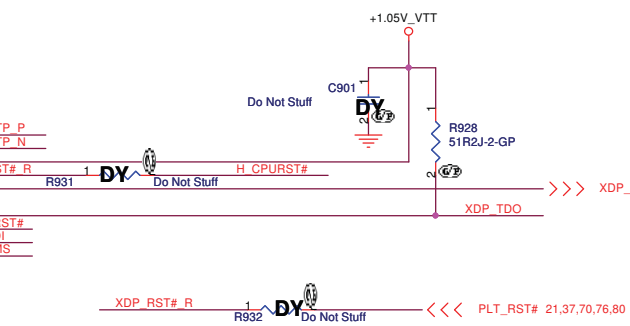
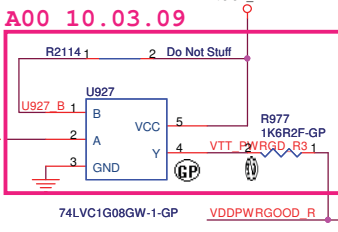
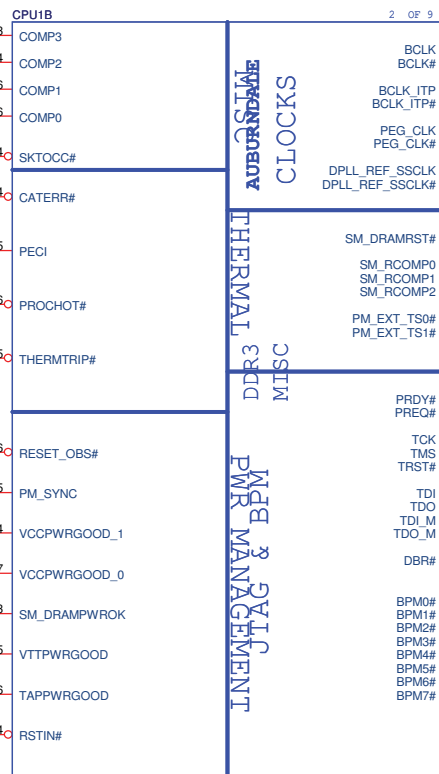
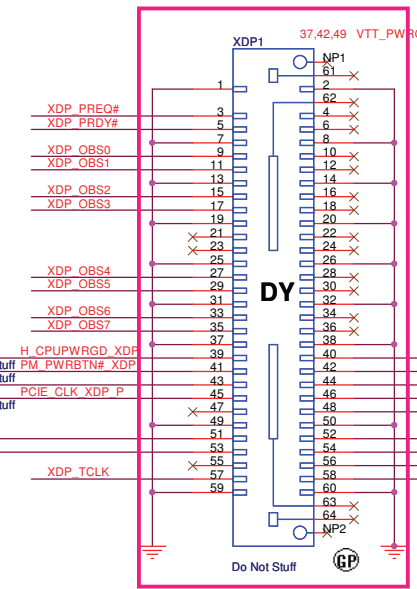
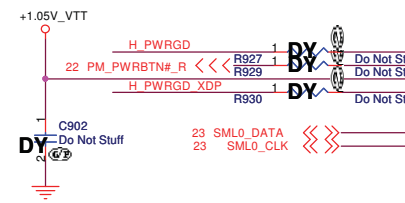
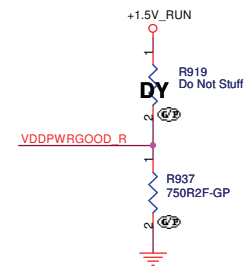


SSID = CPU

Processor Compensation Signals



	R919	R920
S3 circuit	1.1k	0.75k
Normal	No Stuff	3k



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Title

CPU (THERMAL/CLOCK/PM)

Size

Document Number

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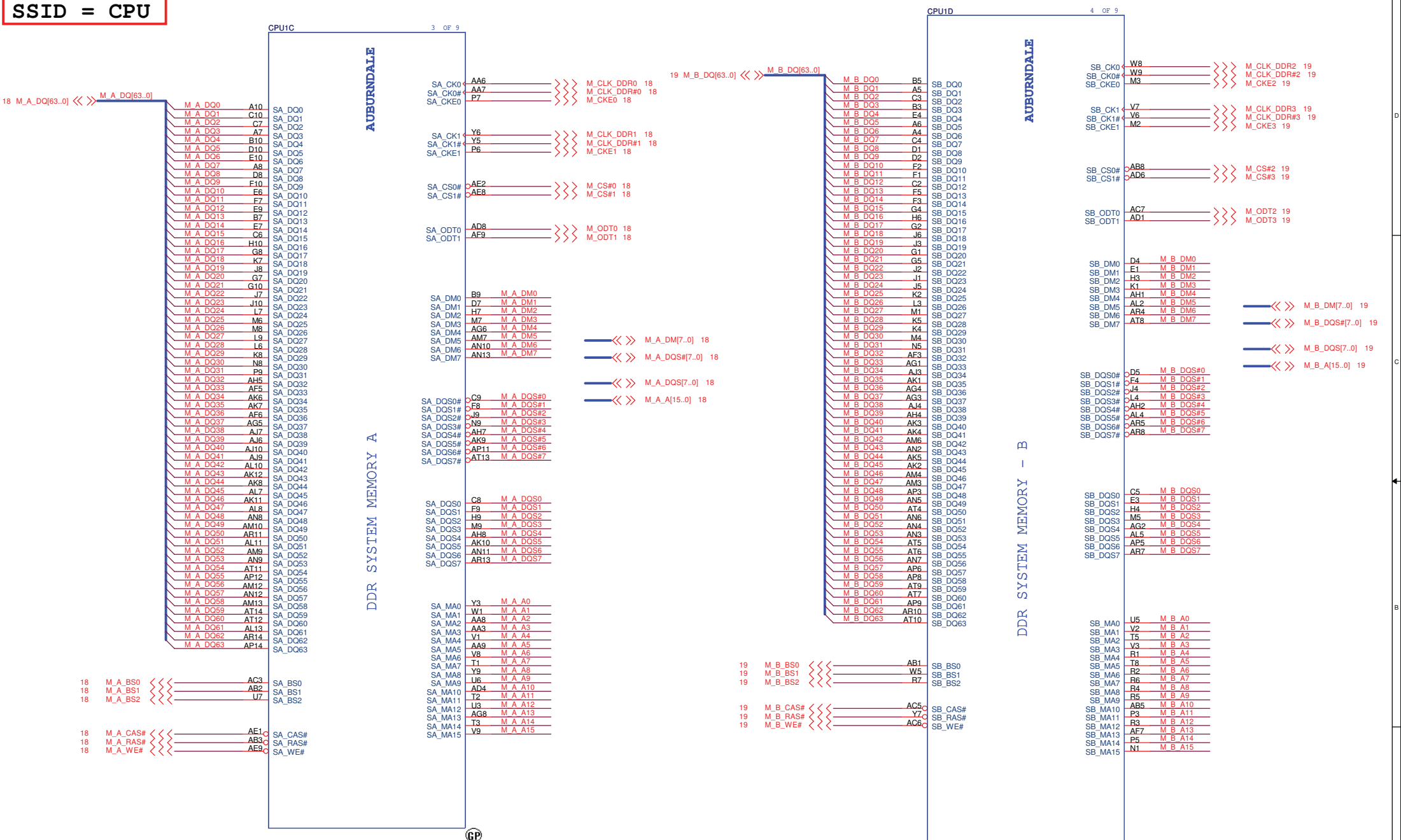
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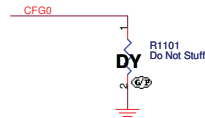
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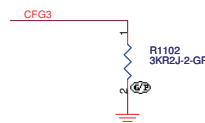
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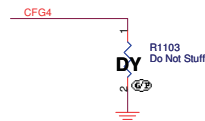
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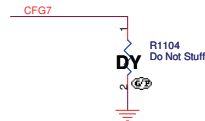
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



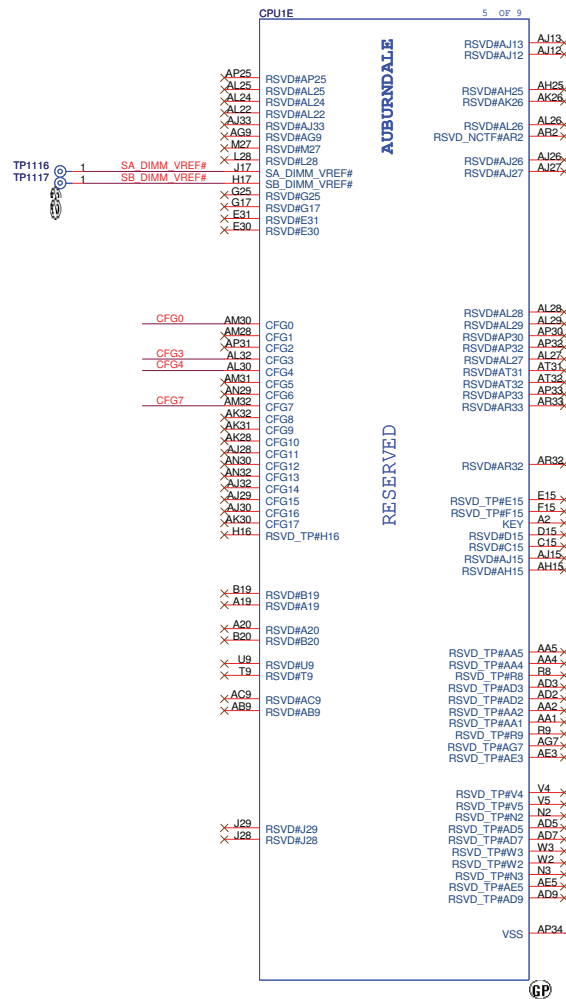
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

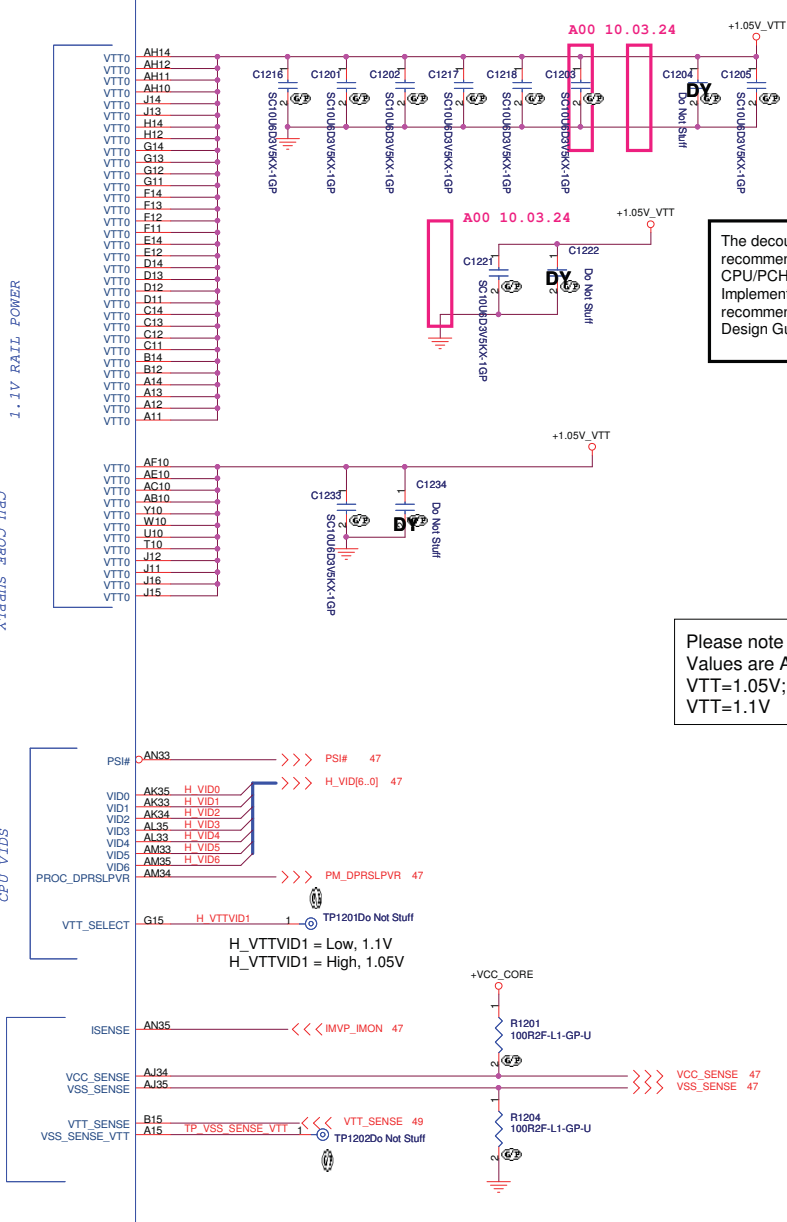
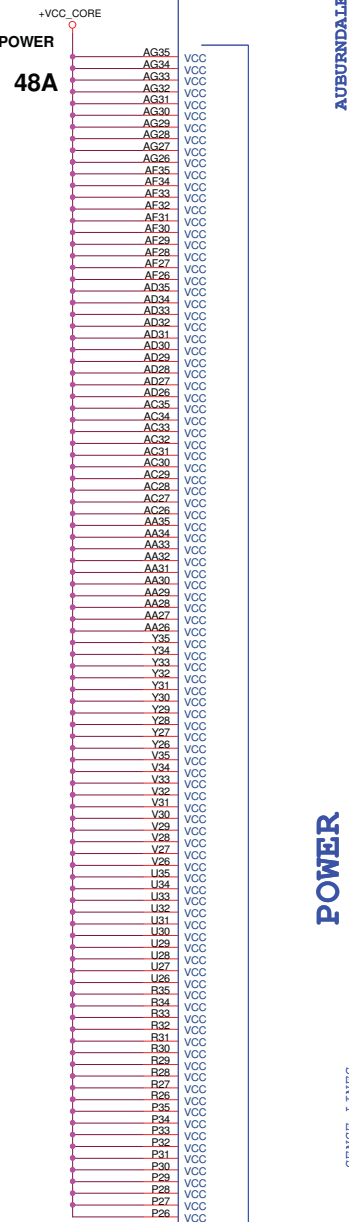
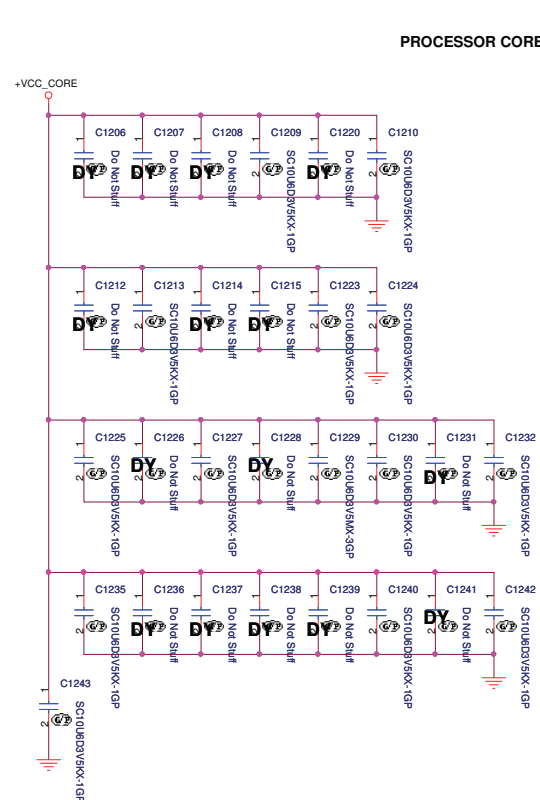


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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Title		
CPU (RESERVED)		
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The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

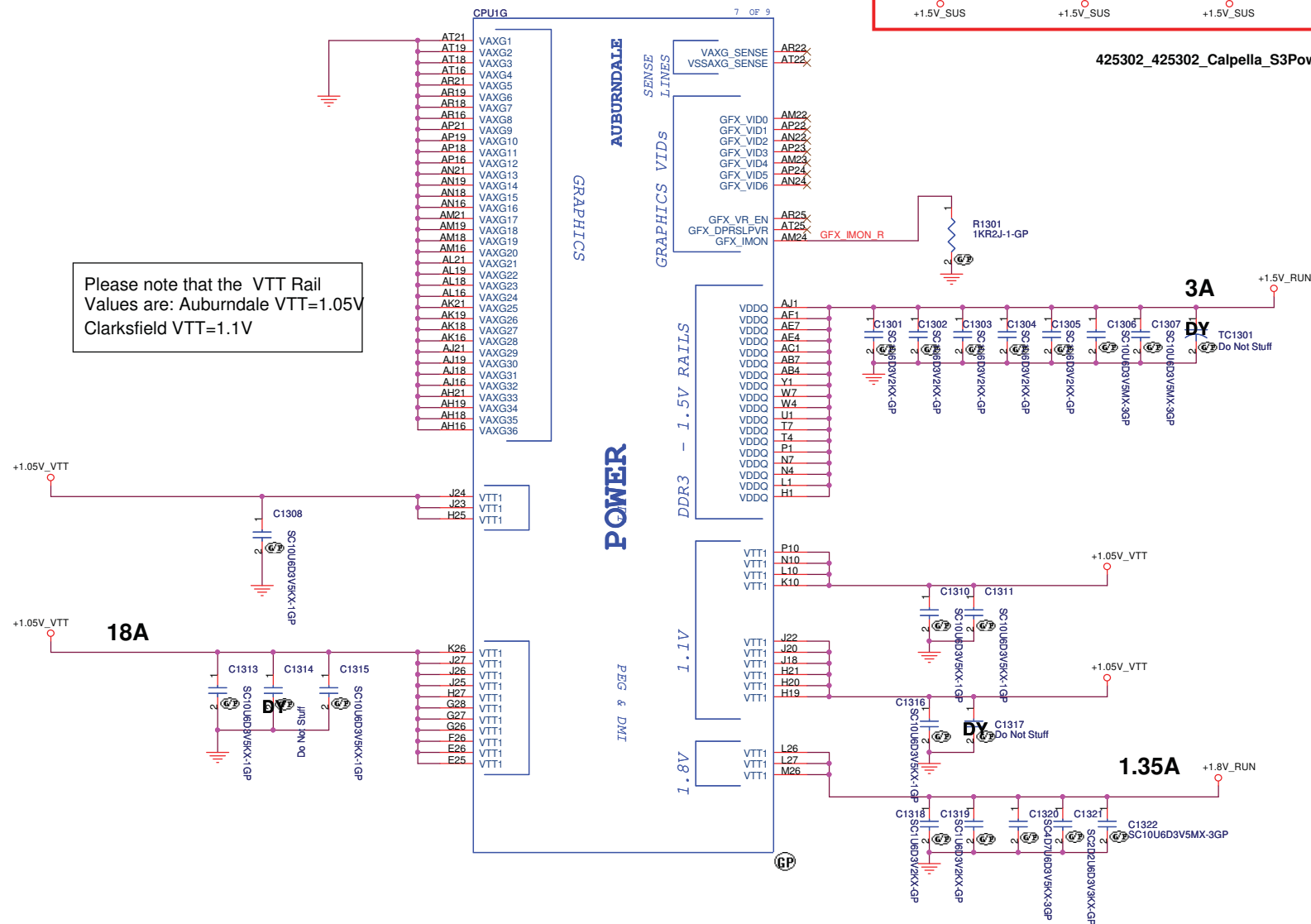
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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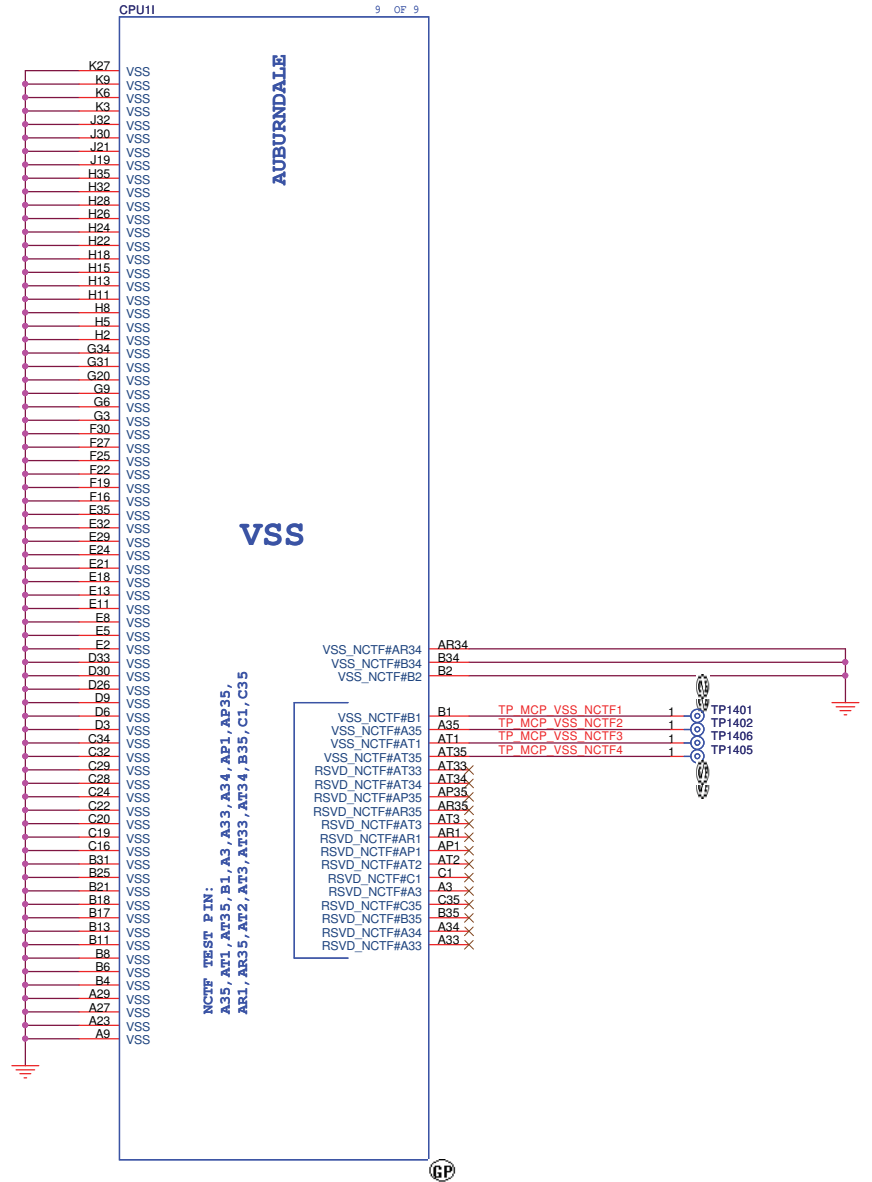
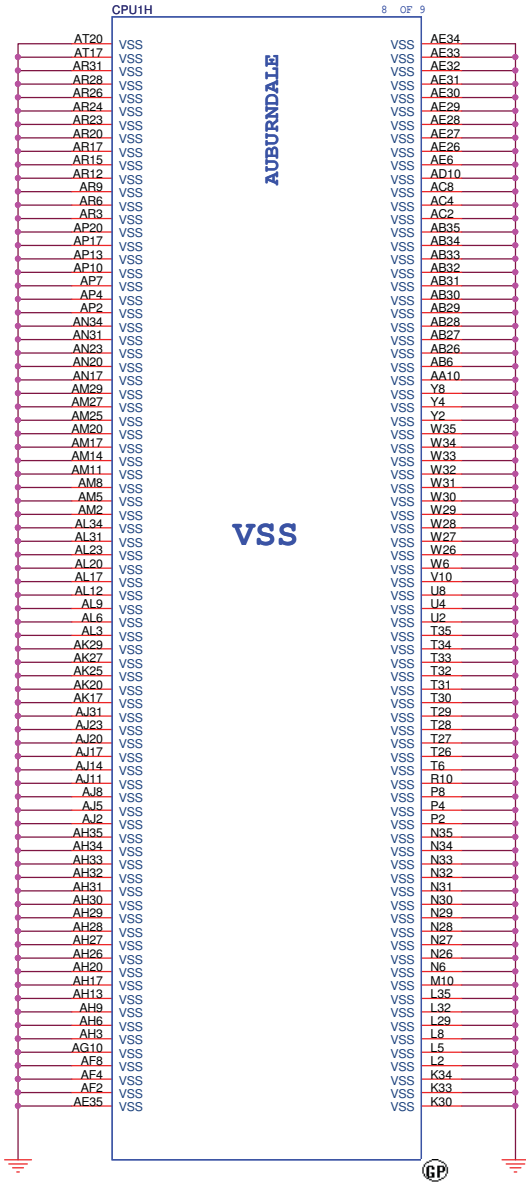


Title	CPU (VCC_CORE)		
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SSID = CPU



SSID = CPU



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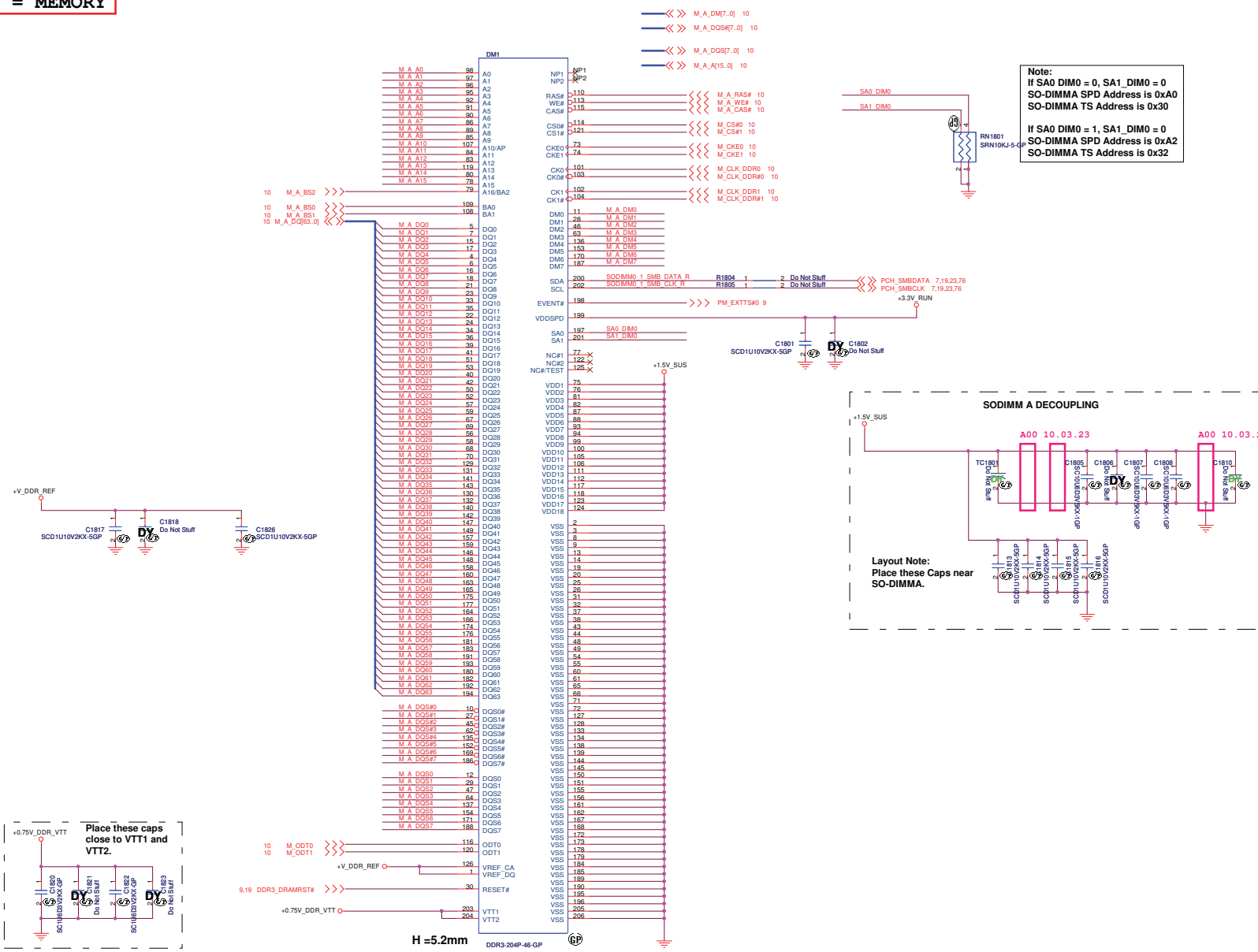
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Title
CPU (VSS)

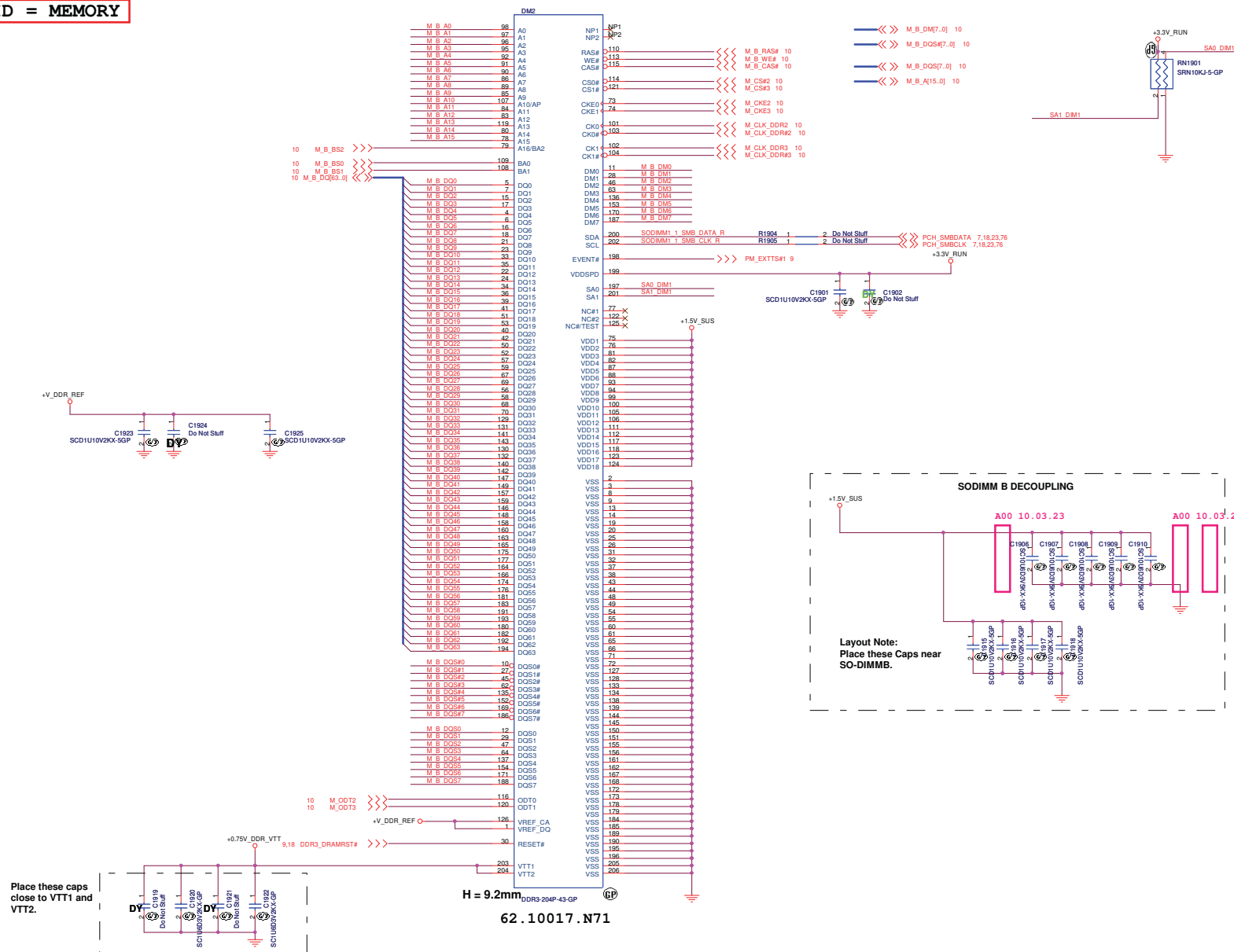
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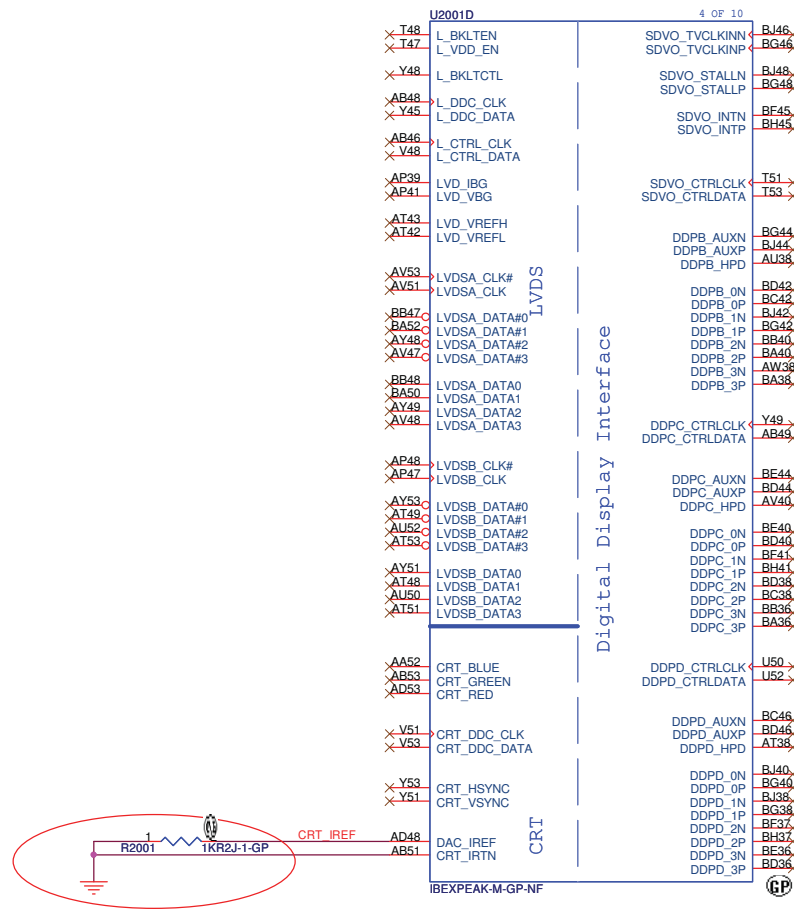


SSID = MEMORY



<p>Note: SO-DIMMB SPD Address is 0xA4 SO-DIMMB TS Address is 0x34</p>	<p>SO-DIMMB is placed farther from the Processor than SO-DIMMA</p>
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SSID = PCH



For discrete, DAC_IREF pull down through 1k ohm.
CRT_IRTN pull down to GND.

DISCRETE PARK

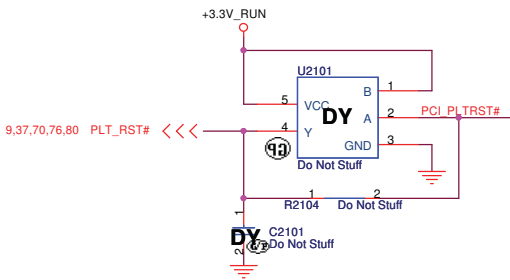
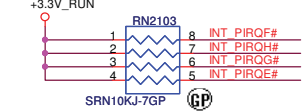
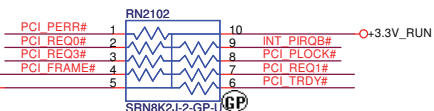
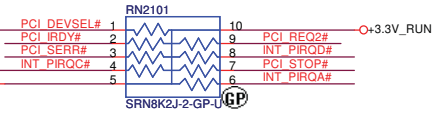
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Title: **PCH (LVDS/CRT/DDI)**

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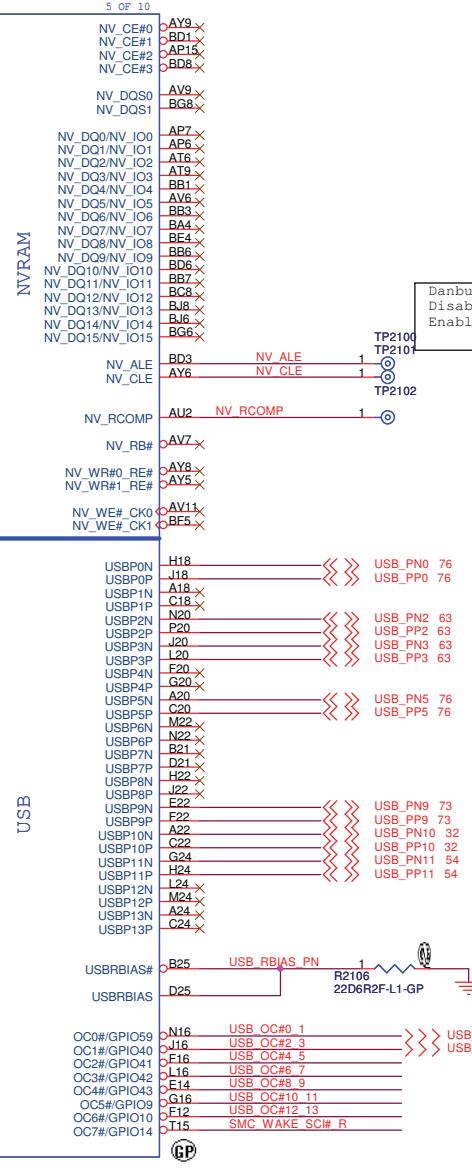
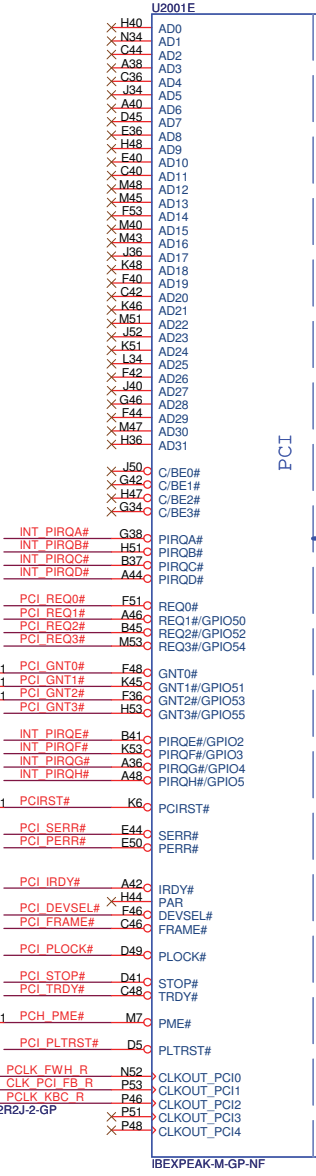
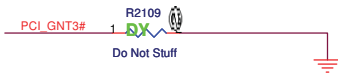
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SSID = PCH



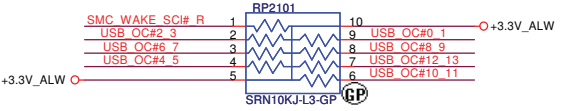
BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X



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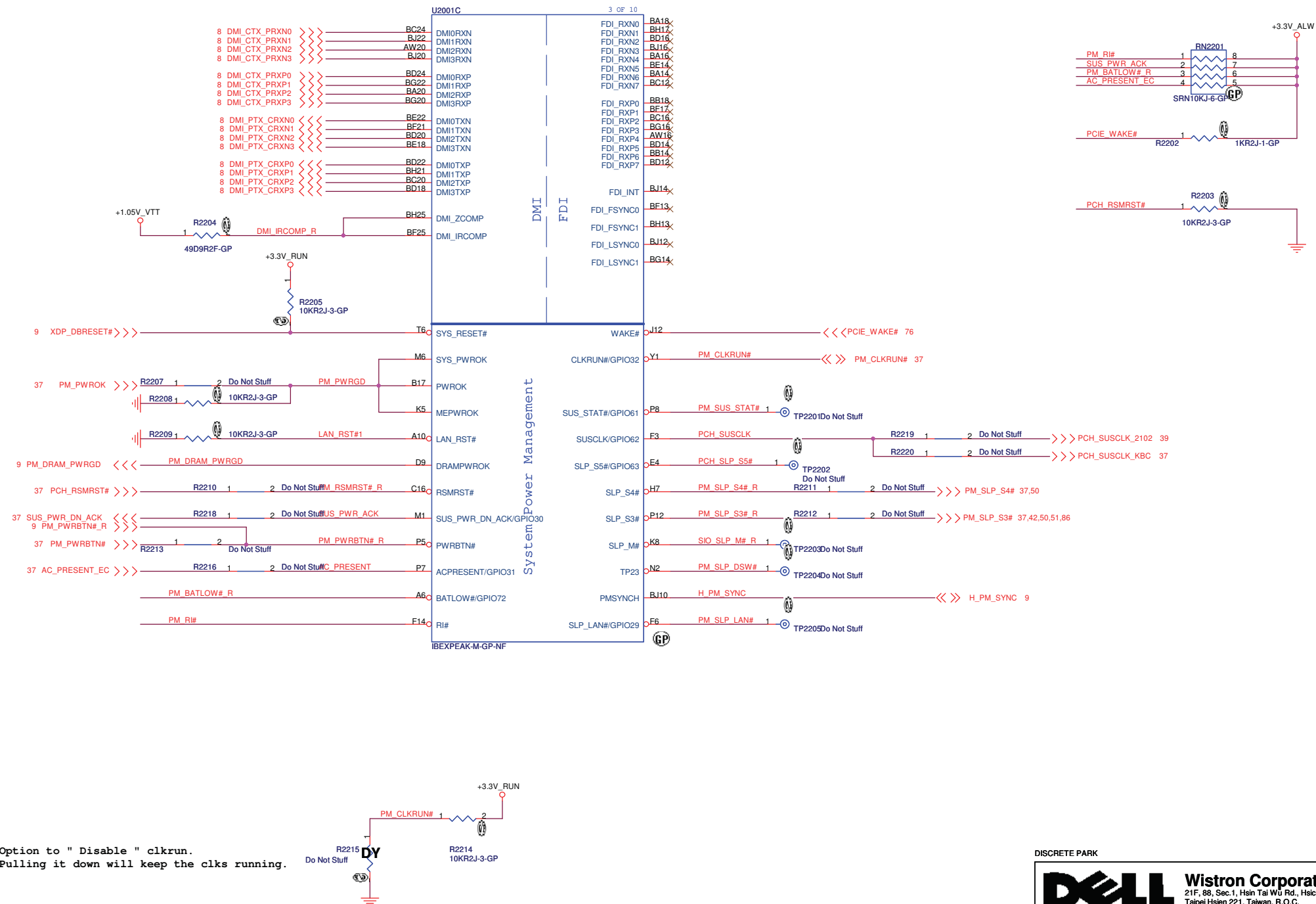
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Title: **PCH (PCI/USB/NVRAM)**

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SSID = PCH



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Title

PCH (DM I/FDI/PM)

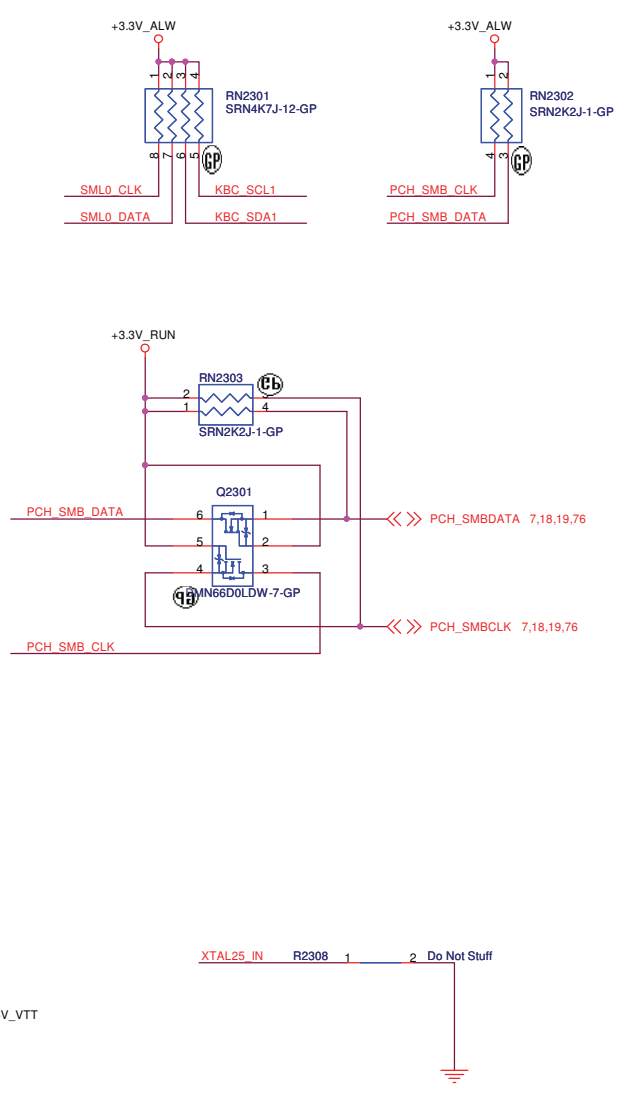
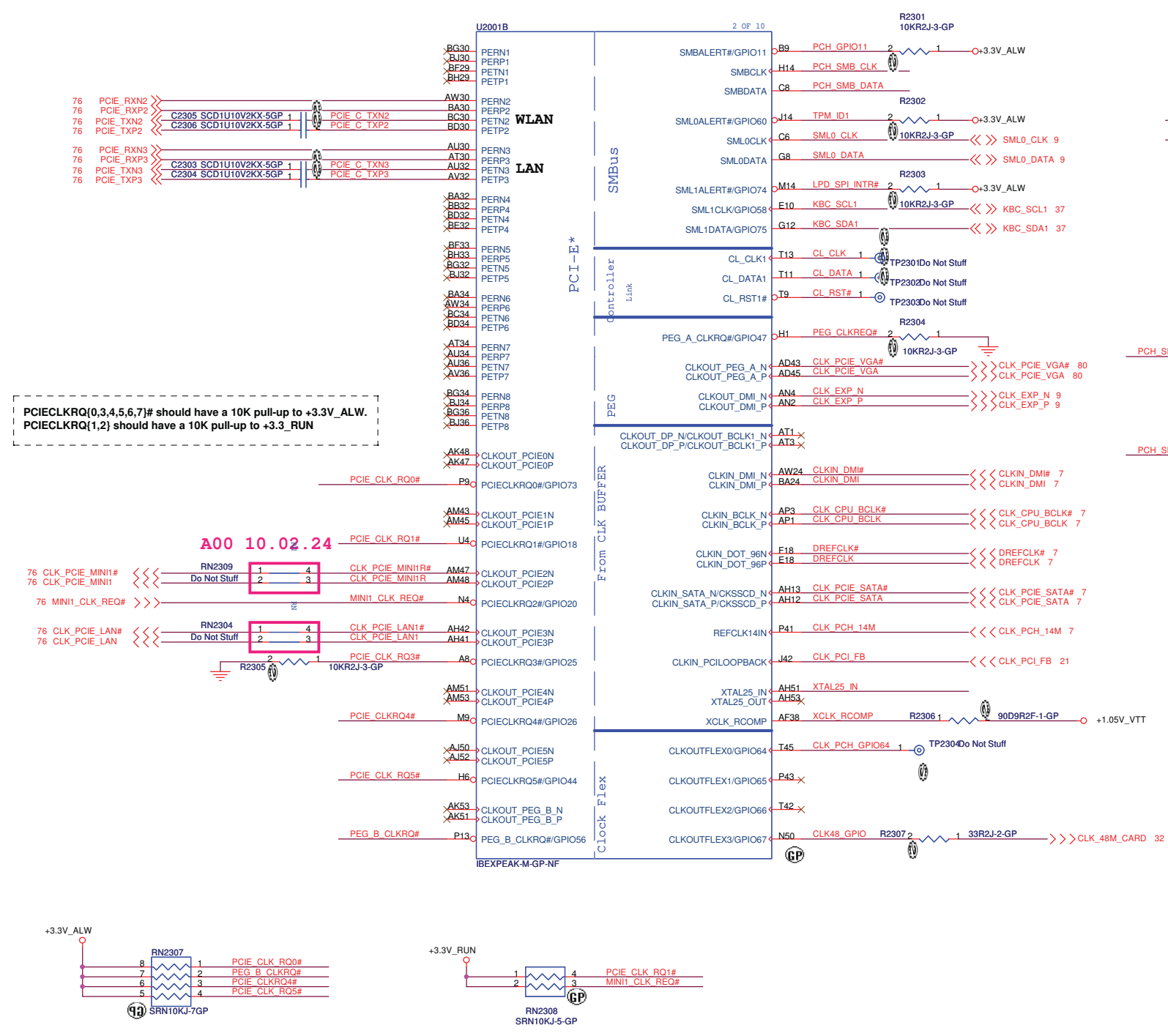
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SSID = PCH



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PCH (PCI-E/SMBUS/CLOCK/CL)

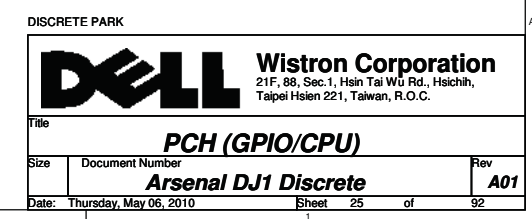
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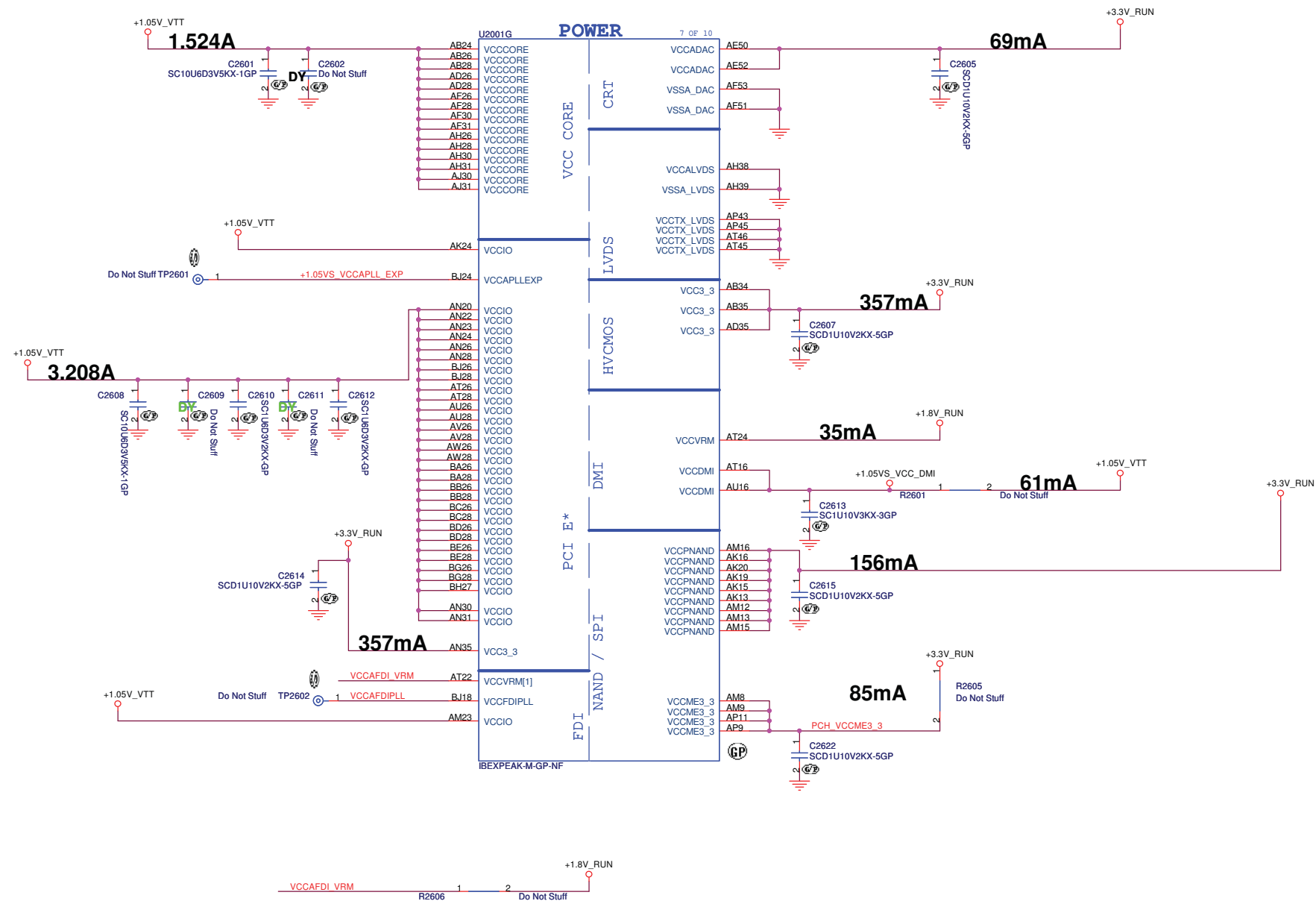
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SSID = PCH

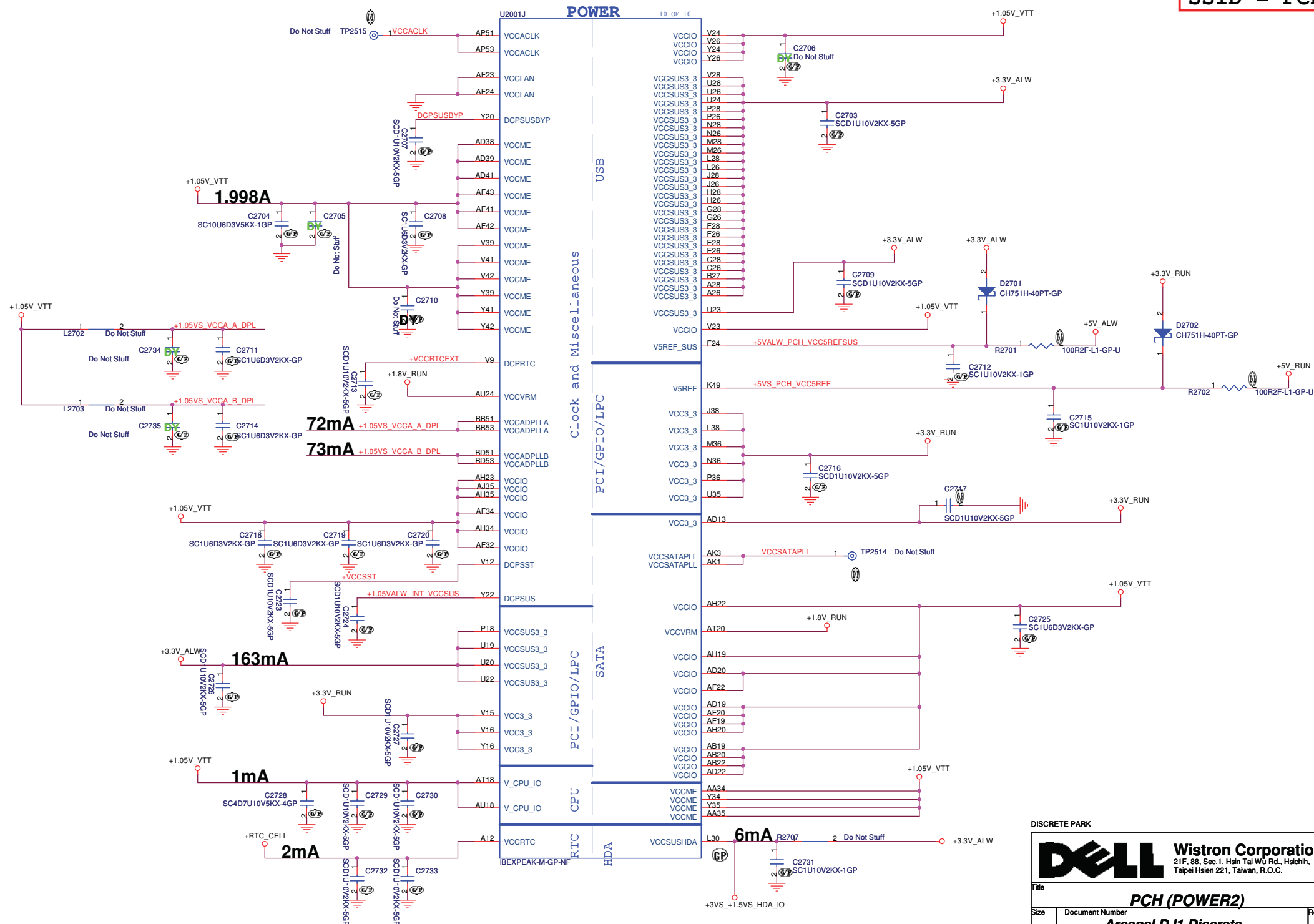


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Size: Document Number: **Arsenal DJ1 Discrete** Rev: **A01**
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SSID = PCH



DISCRETE PARK



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (POWER2)

Size	Document Number
------	-----------------

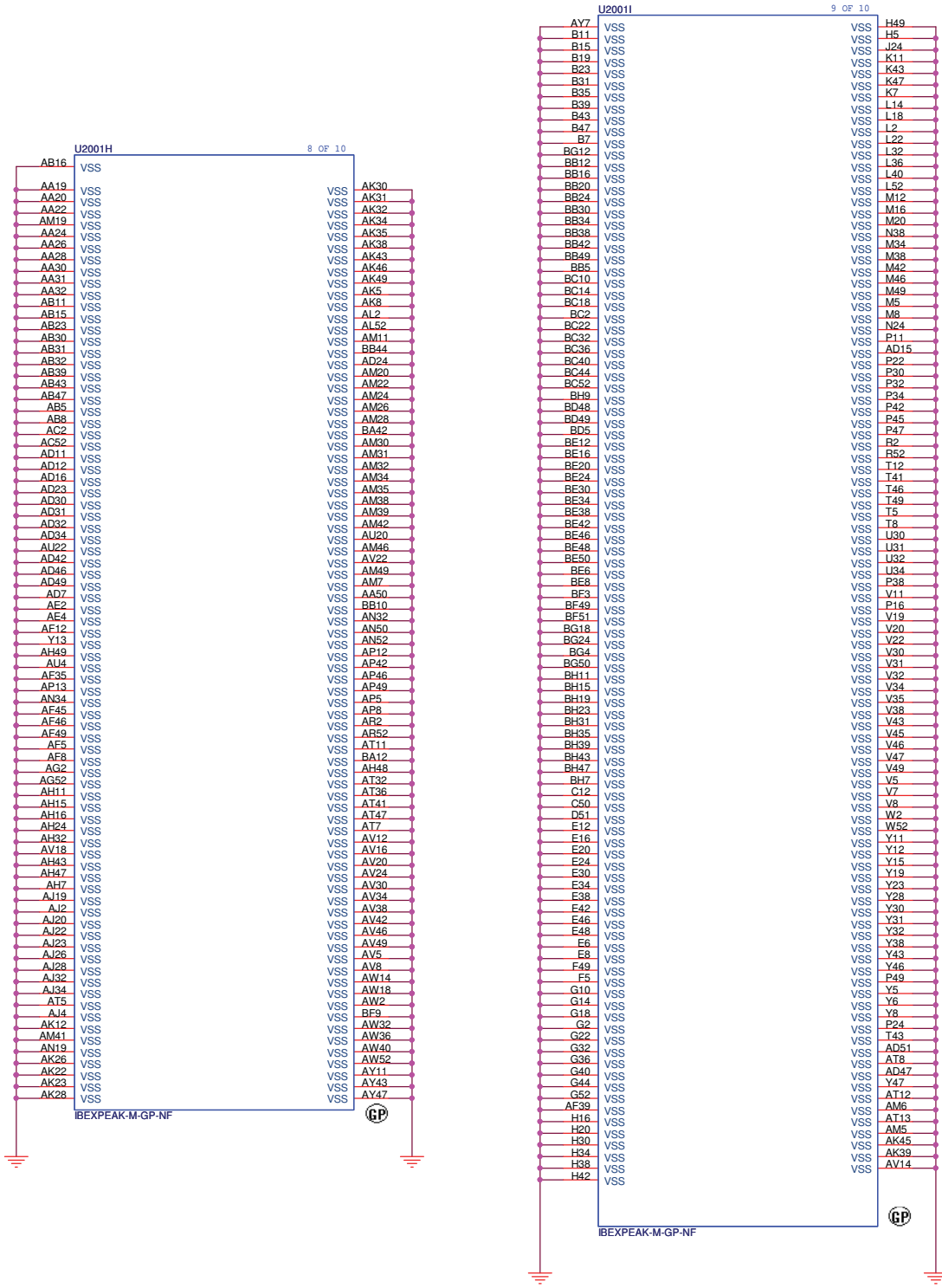
Arsenal DJ1 Discrete

Date: Thursday, May 06, 2010

Sheet 27 of 92

1	2	3	4
---	---	---	---

SSID = PCH



DISCRETE PARK

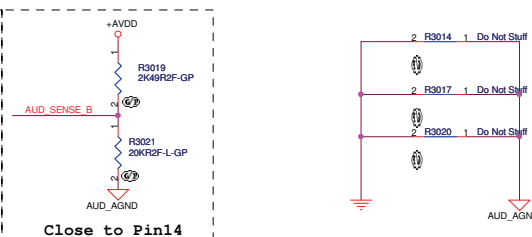
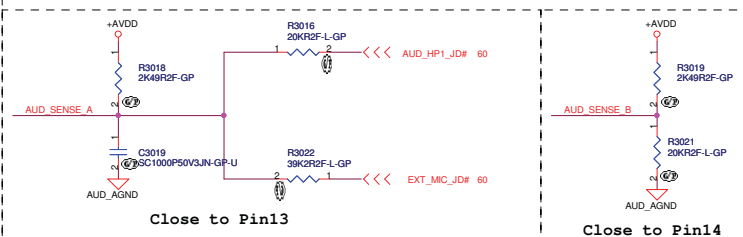
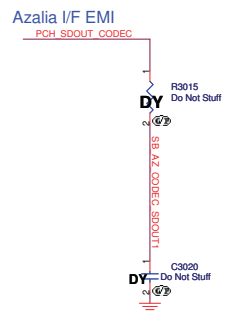
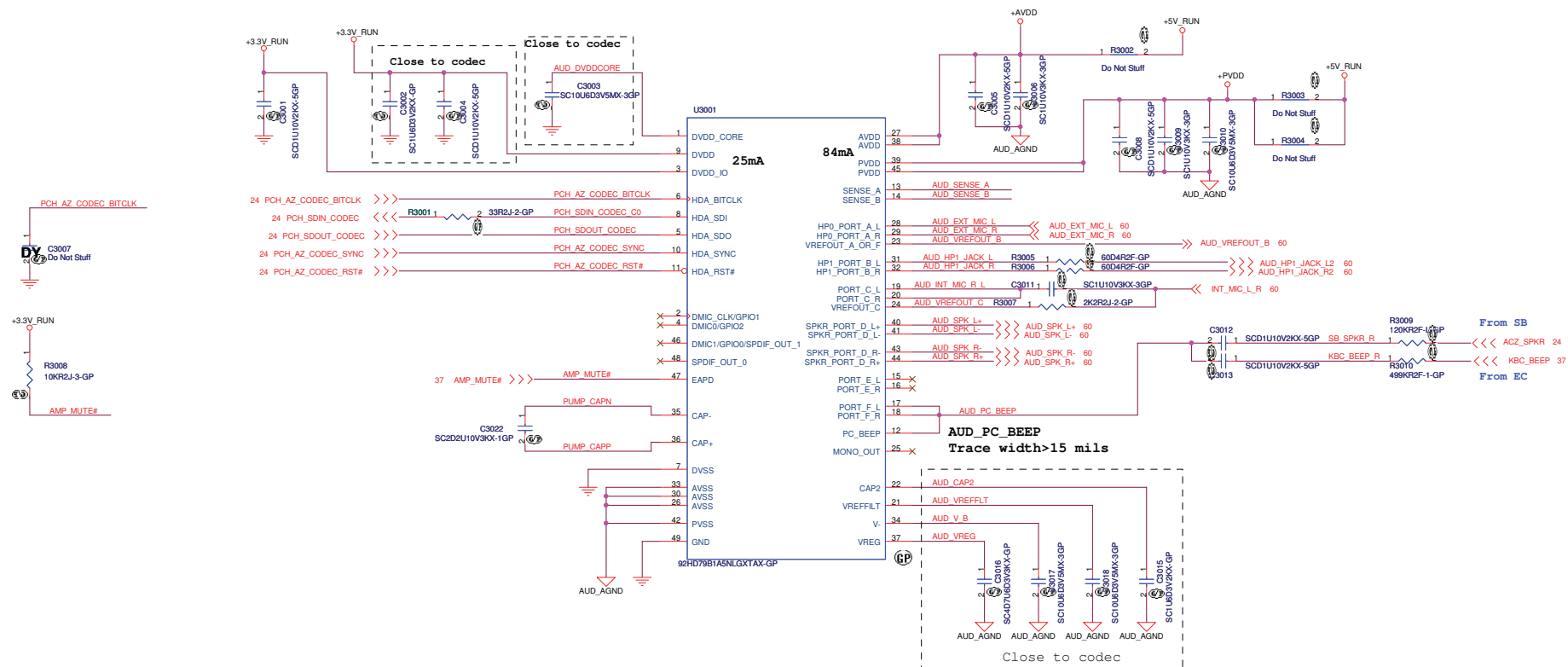
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

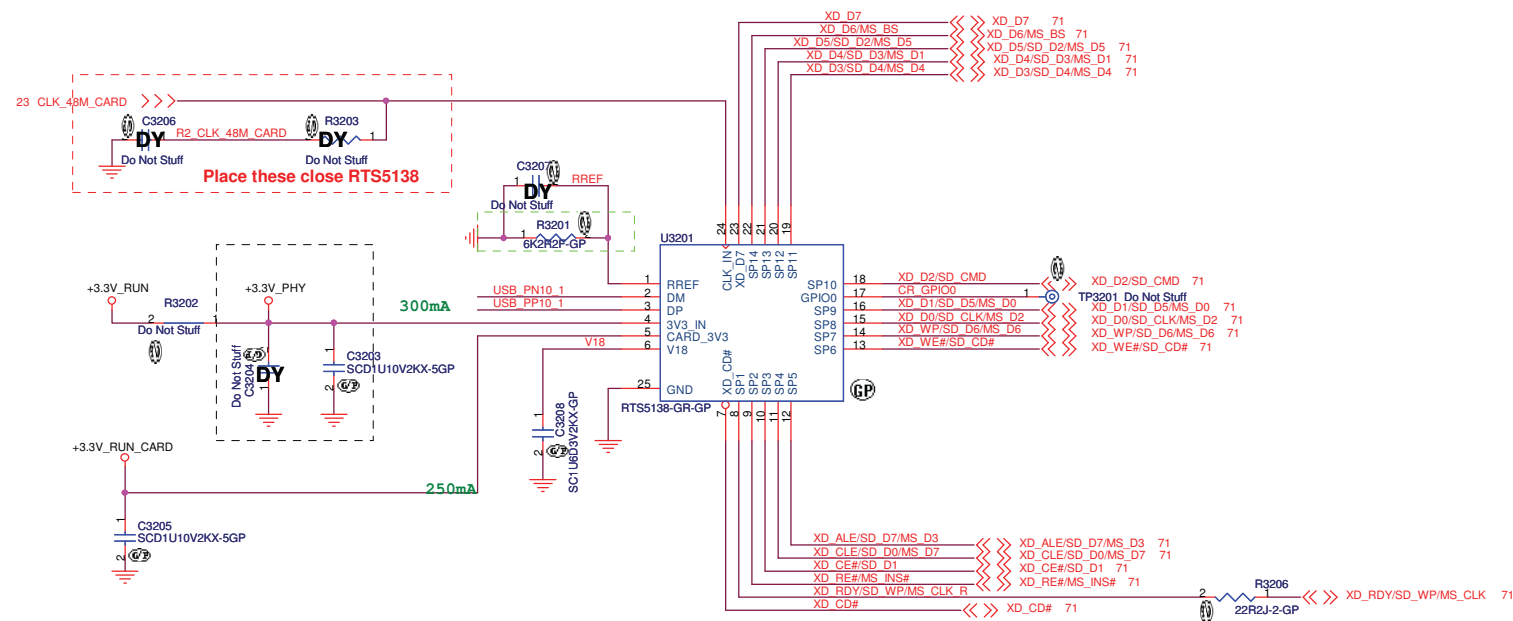
Size	Document Number	Rev
	Arsenal DJ1 Discrete	A01

Date: Thursday, May 06, 2010 Sheet 28 of 92

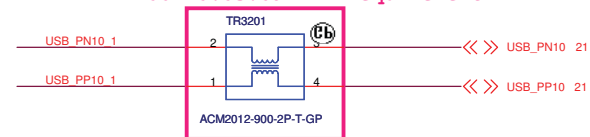
SSID = AUDIO



SSID = SDIO



A00 10.03.09 EMI requirement



DISCRETE PARK

DELL			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,			Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Card Reader-RTS5138					
Size	Document Number				Rev
Custom	Arsenal DJ1 Discrete				A01
Date:	Thursday, May 06, 2010	Sheet	32	of	92

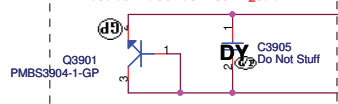


SSID = Thermal

1. Place near CPU and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil trace width and 10 mil spacing.

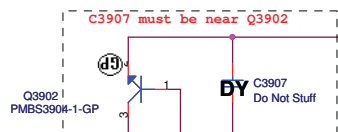
C3905 must be near Q3901



81 VGA_THERMDC >>>

2. VGA Sensor

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing 10 mil trace width and 10 mil spacing.



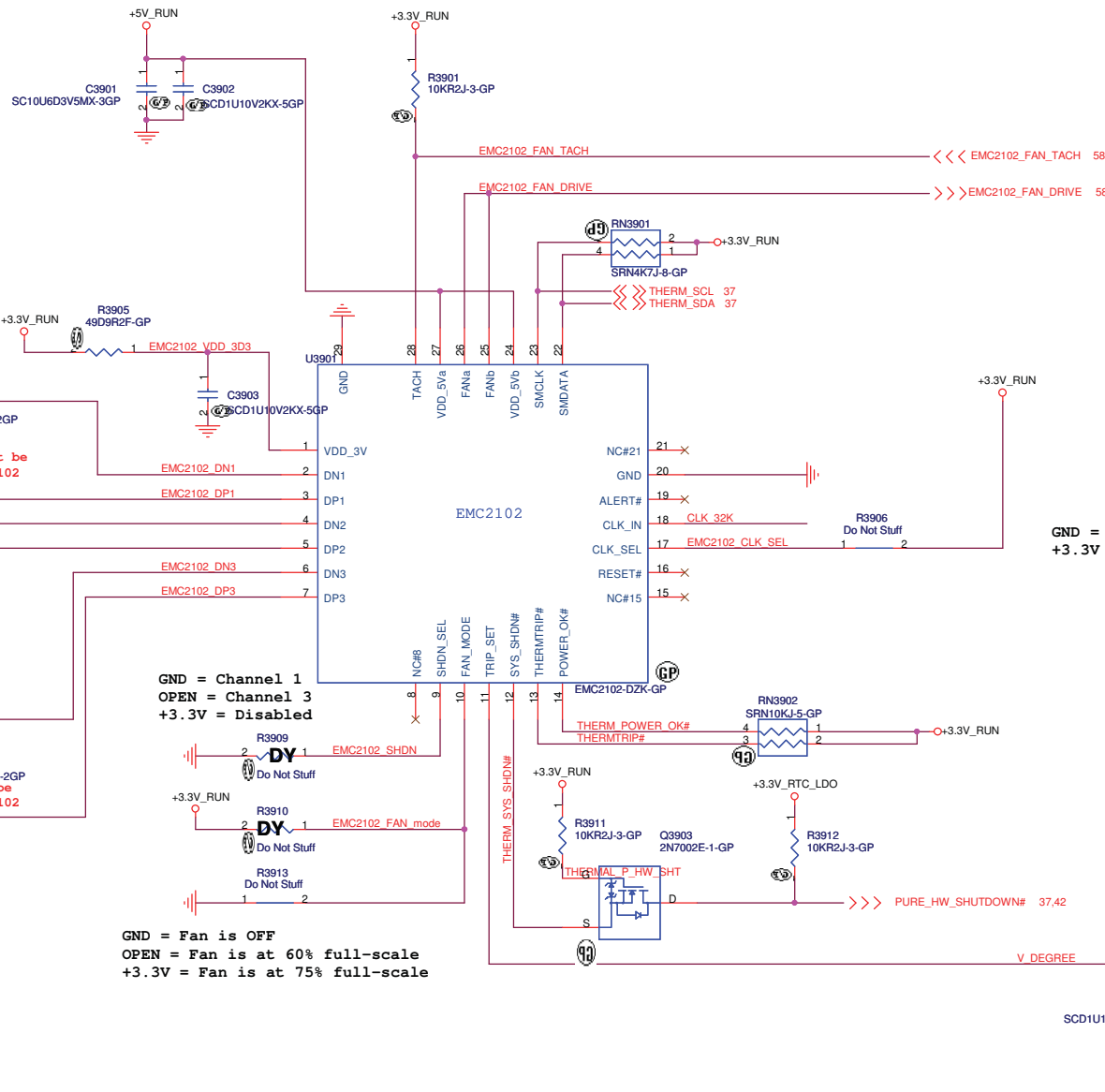
3. HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing.



22 PCH_SUSCLK_2102 >>>

42.87 RUN_ENABLE >>>

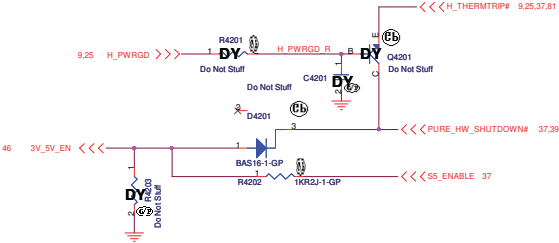


32K suspend clock output

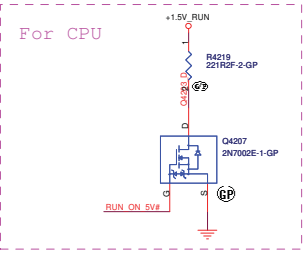
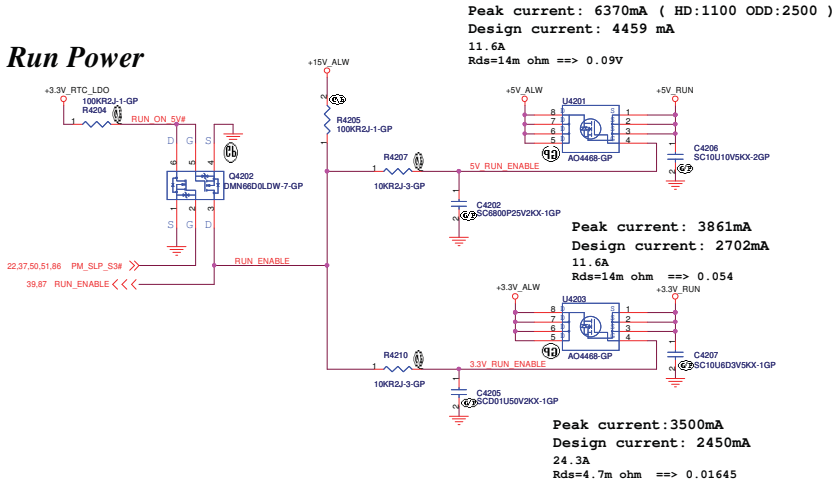
DISCRETE PARK

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Thermal/Fan Controller EMC2102	
Size	Document Number	Rev	
Custom	Arsenal DJ1 Discrete		A01
Date:	Thursday, May 06, 2010	Sheet	39 of 92

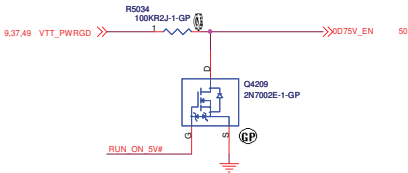
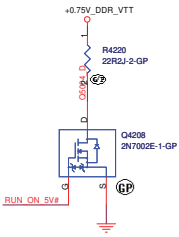
SSID = Reset .Suspend

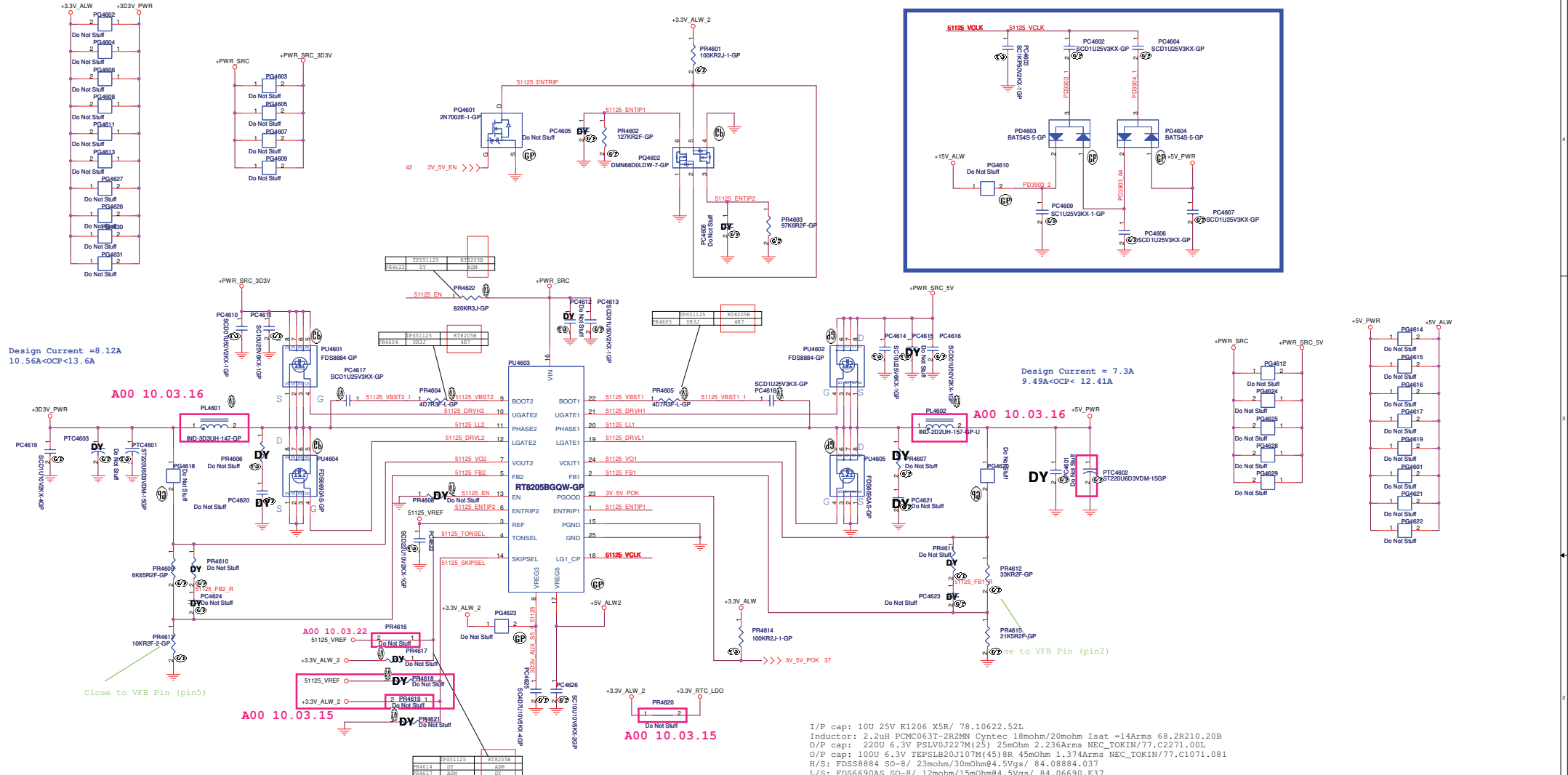


Run Power



425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7





Design Current = 8.12A
10.56A<OCP<13.6A

Design Current = 7.3A
9.49A<OCP< 12.41A

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3uH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220u 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100u 6.3V TEPSLB20J107M(45)BR 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS6690AS SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220u 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100u 6.3V TEPSLB20J107M(45)BR 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS6690AS SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

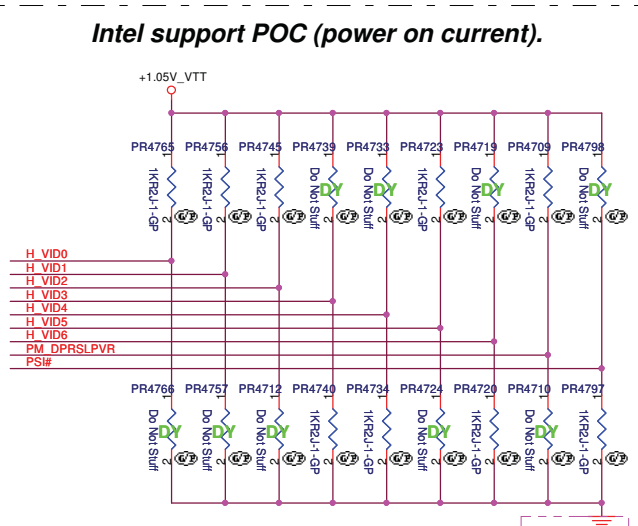
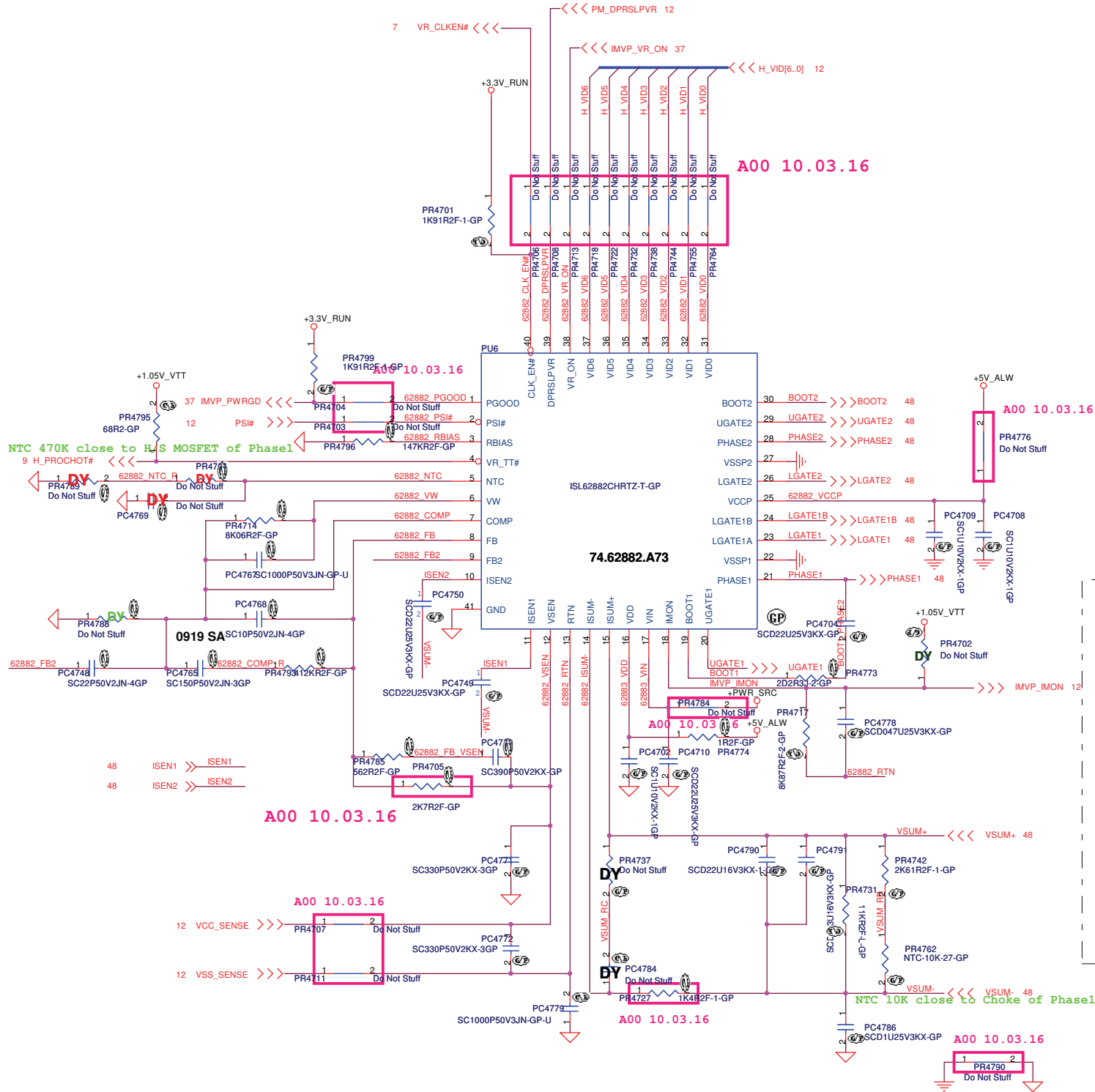
TPS51125:		
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

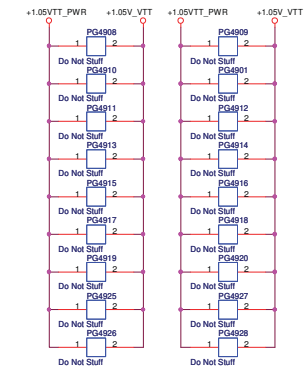
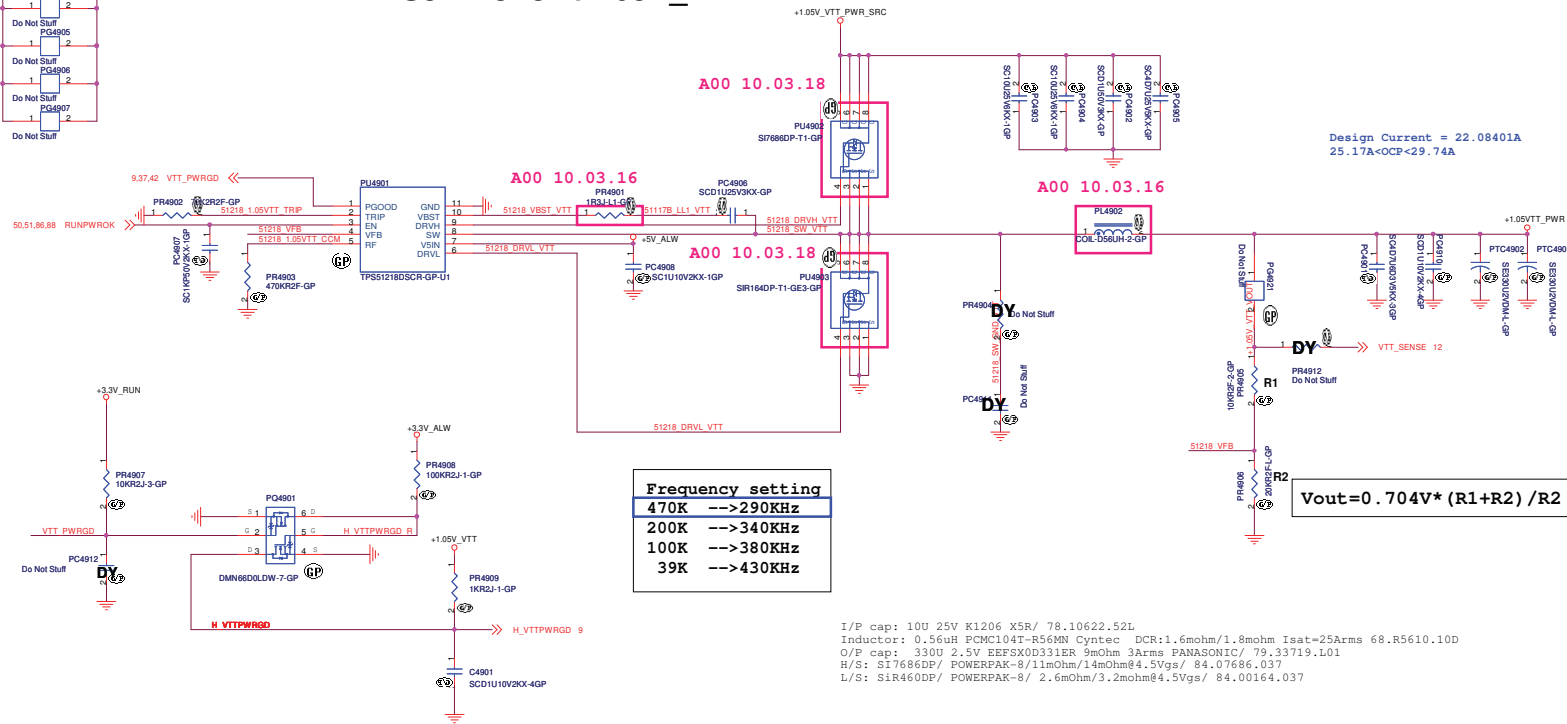
RT8205B:		
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<http://hobi-elektronika.net>



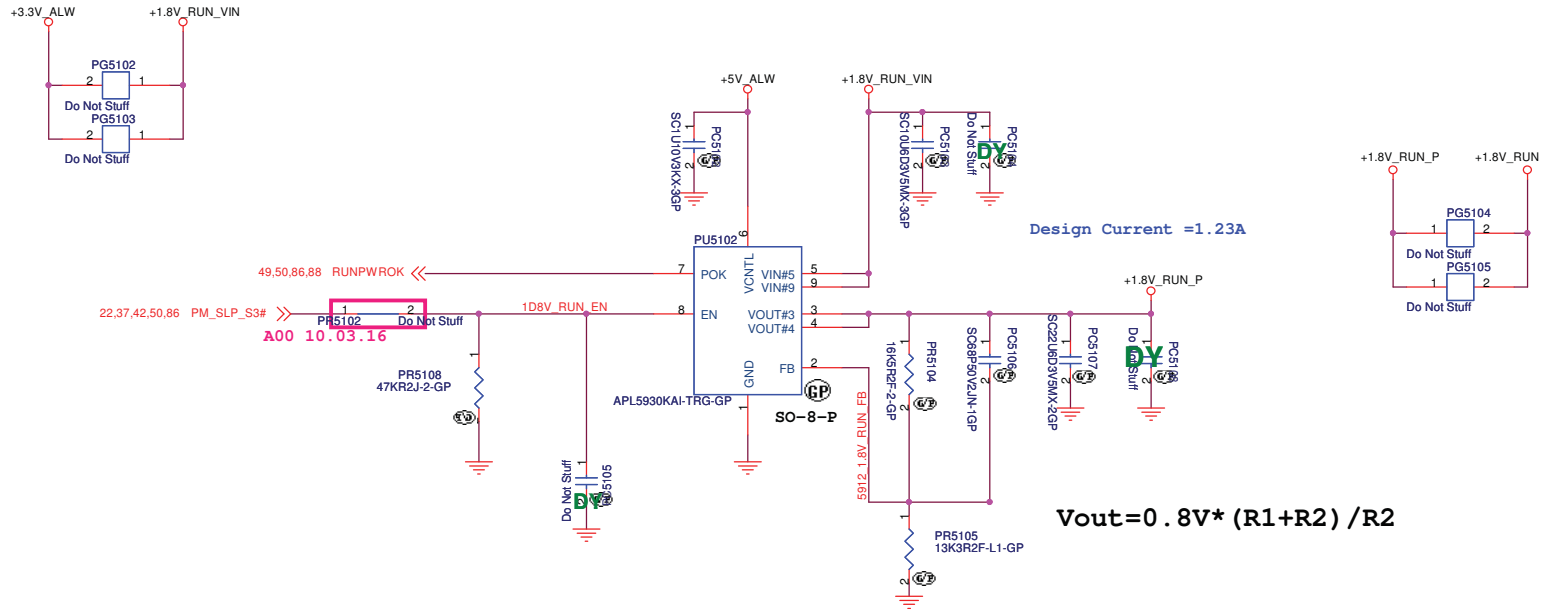


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56M8N Cyntec DCR: 1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEF5X0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: S1R460DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

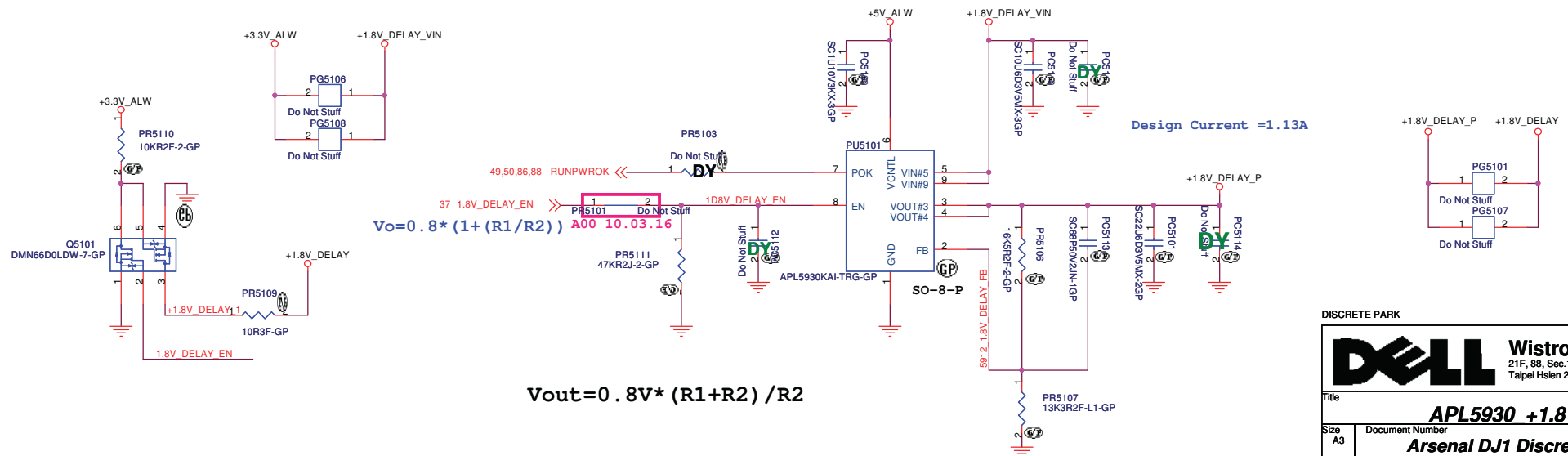
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_DELAY



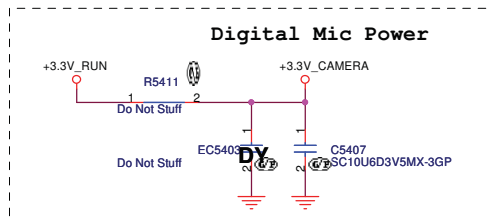
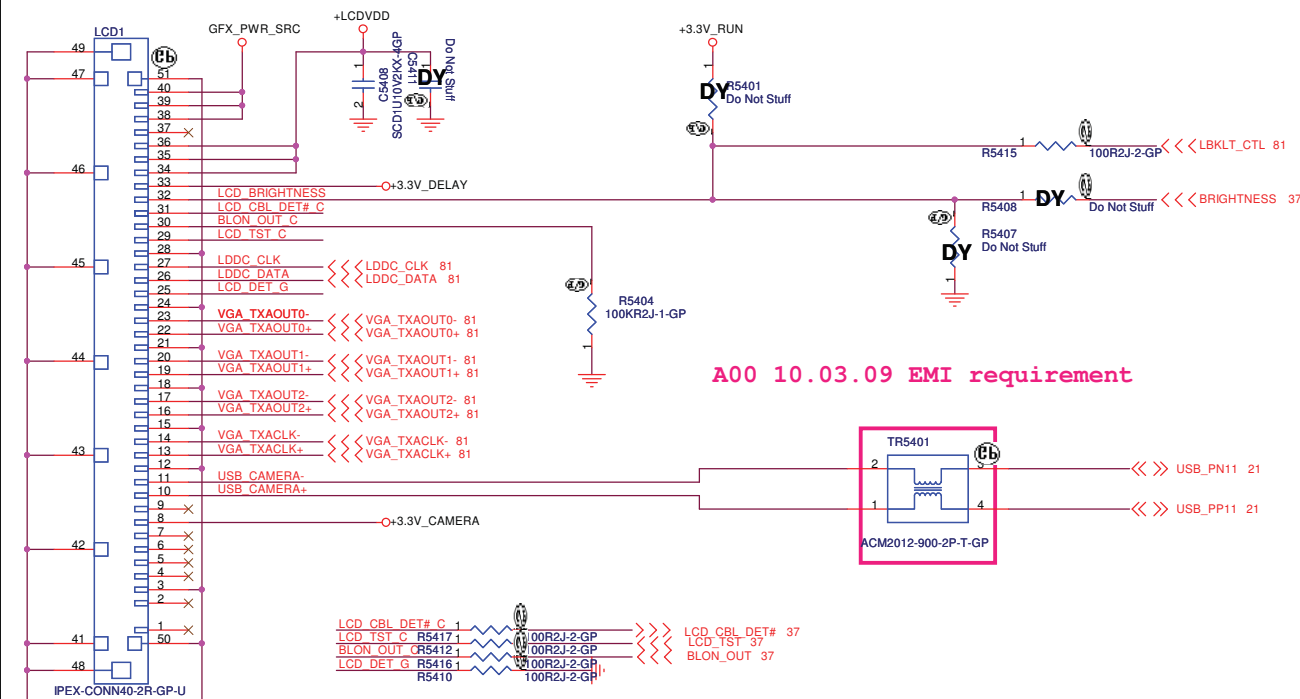
DISCRETE PARK

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **APL5930 +1.8V RUN**
Size A3 Document Number: **Arsenal DJ1 Discrete** Rev: **A01**
Date: Thursday, May 06, 2010 Sheet 51 of 92

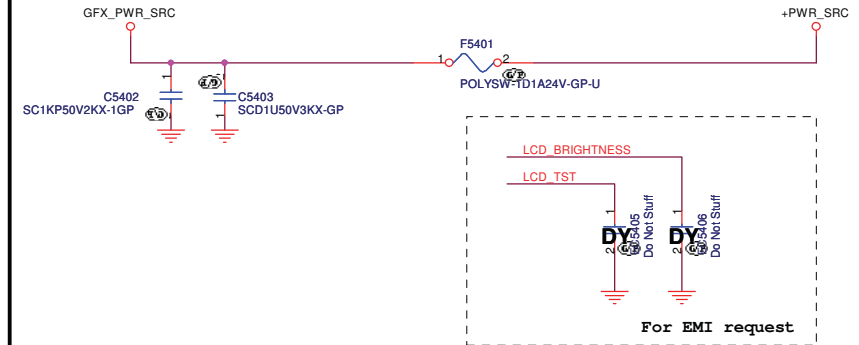
SSID = VIDEO

LVDS CONNECTOR



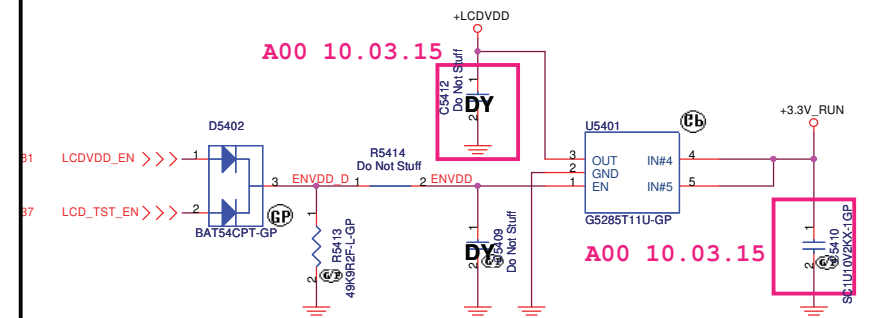
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



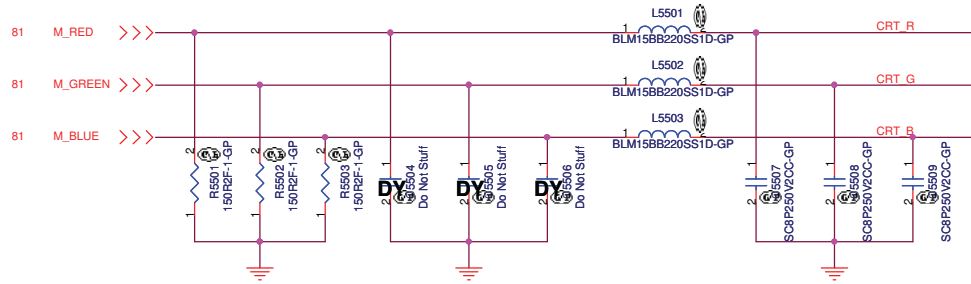
DISCRETE PARK

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD/Inverter Connector			
Size A3	Document Number Arsenal DJ1 Discrete		Rev A01
Date: Thursday, May 06, 2010	Sheet 54	of 92	

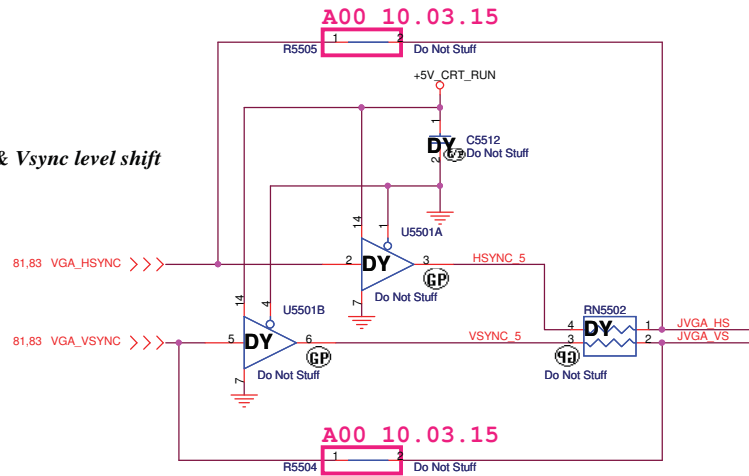
SSID = VIDEO

Layout Note:

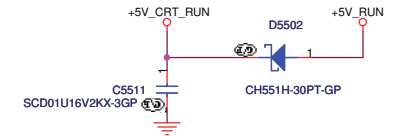
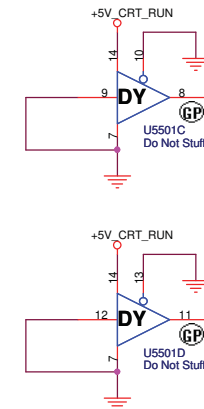
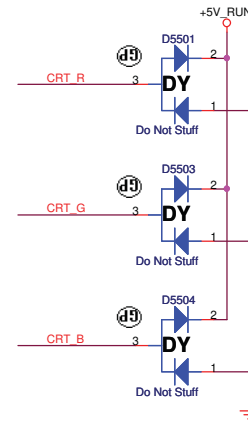
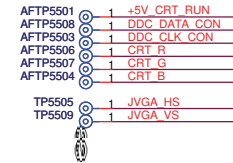
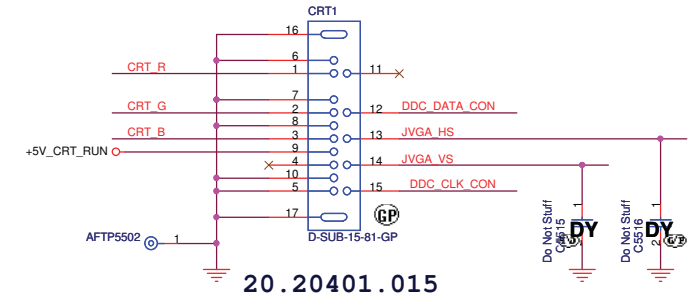
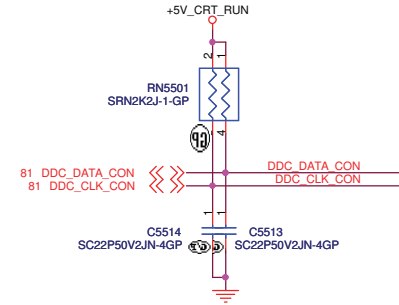
- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



<http://hobi-elektronika.net>



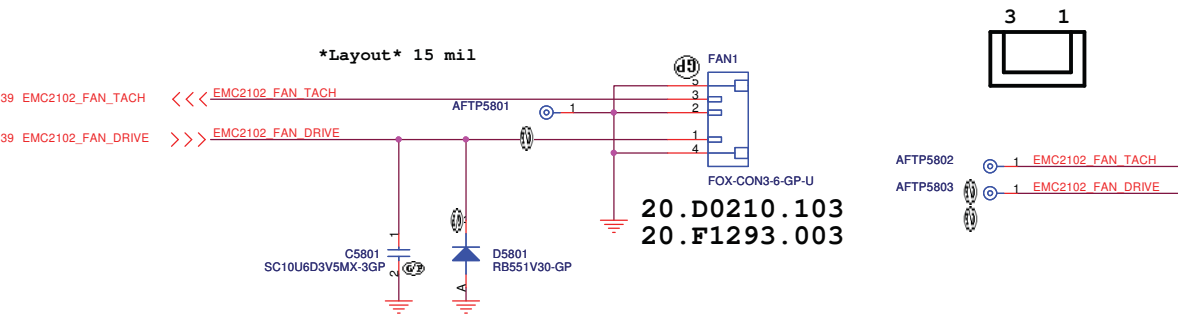
DISCRETE PARK

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector			
Size	Document Number	Rev A01	
Date: Thursday, May 06, 2010		Sheet 55	of 92

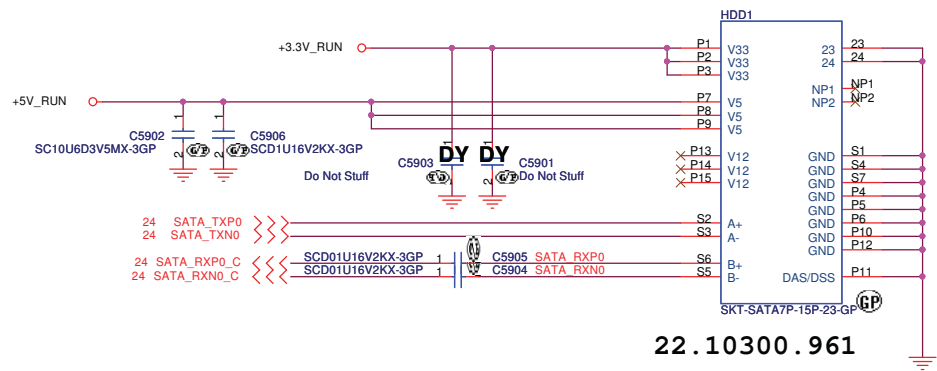
SSID = User.Interface

SSID = Thermal

Fan Connector

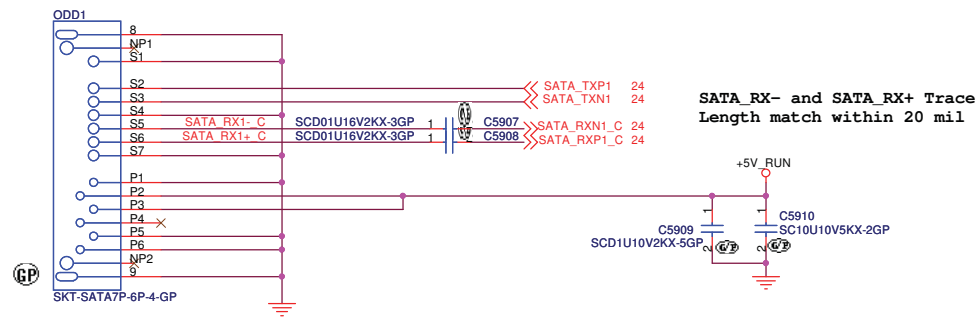


SATA HDD Connector



22.10300.961

ODD Connector

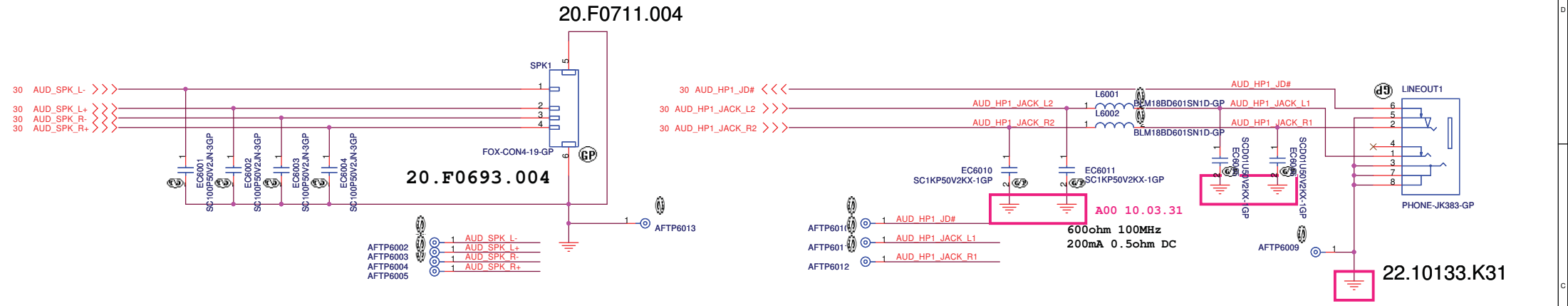


22.10300.811
22.10300.471

SSID = AUDIO

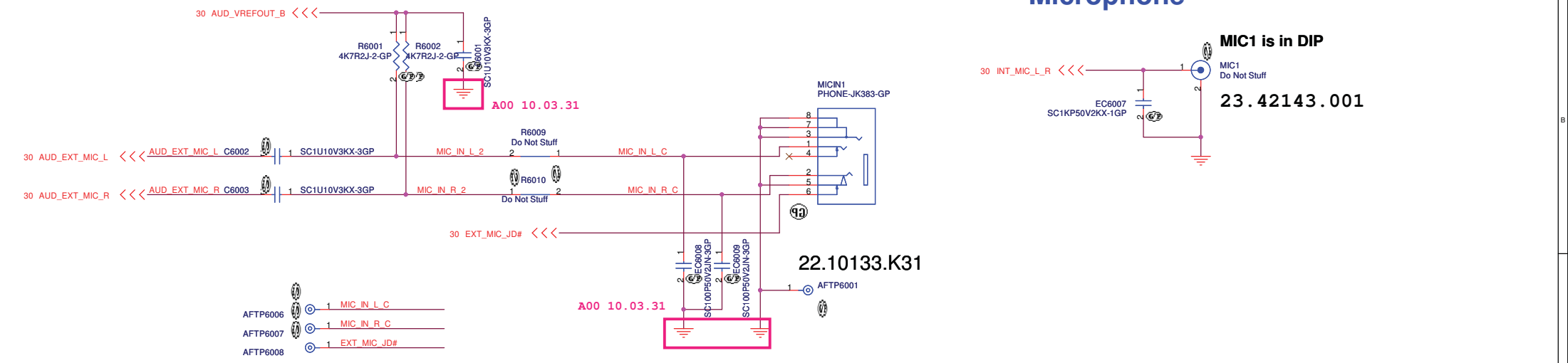
Speaker Connector

LINE1 OUT



MIC IN

Internal Microphone



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DISCRETE PARK

DELL Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

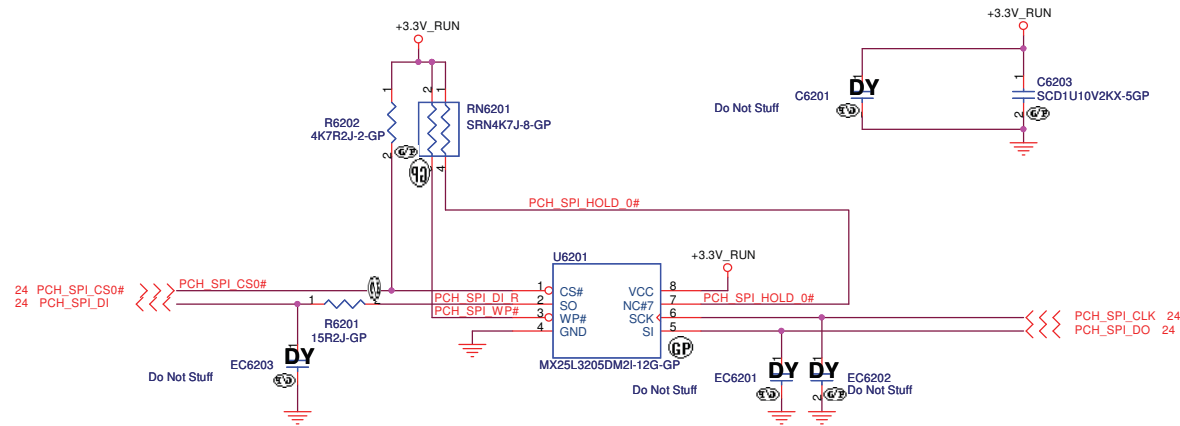
Audio Jack

Size A3 Document Number **Arsenal DJ1 Discrete** Rev **A01**

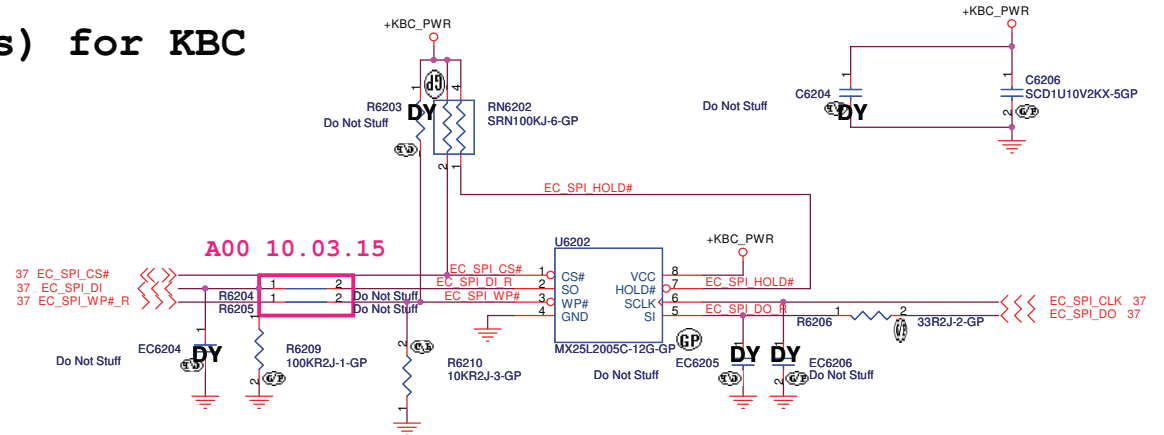
Date: Thursday, May 06, 2010 Sheet 60 of 92

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

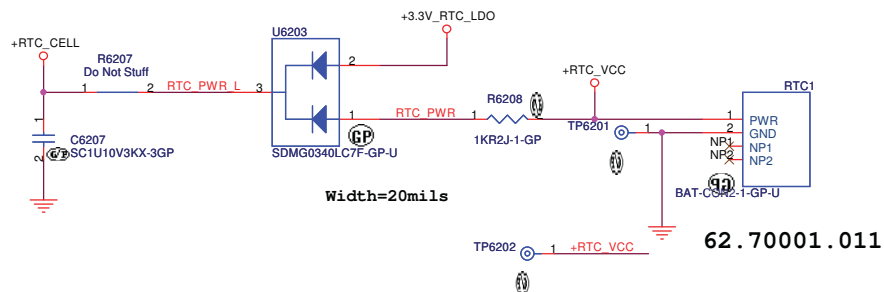


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



DISCRETE PARK

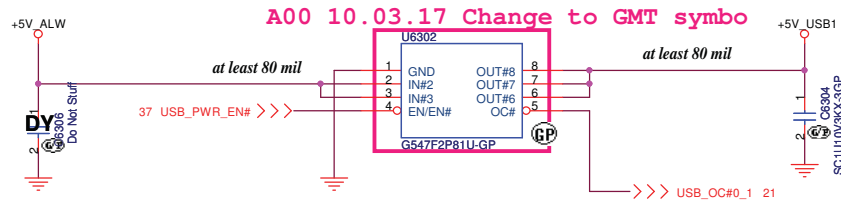


Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

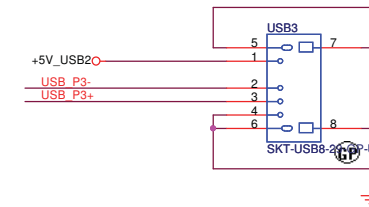
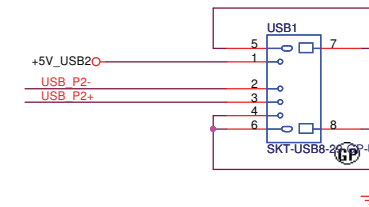
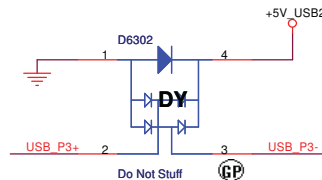
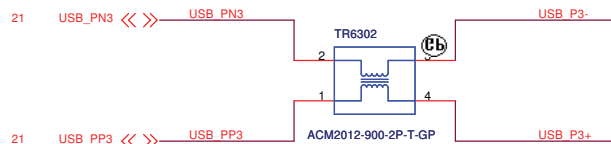
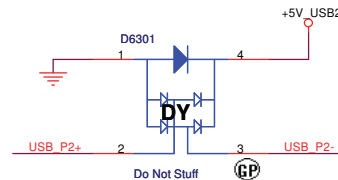
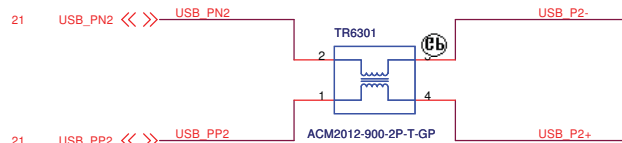
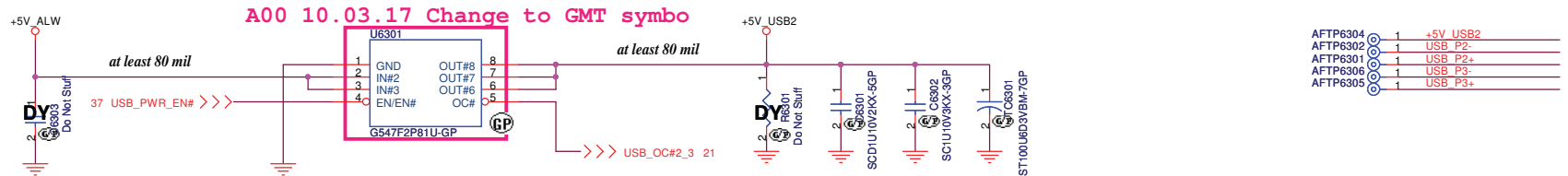
Title			Flash/RTC
Size	Document Number	Rev	A01
A3	Arsenal DJ1 Discrete		
Date:	Thursday, May 06, 2010	Sheet	62 of 92

SSID = USB

IO Board USB Power



Right USB Power

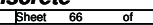


22.10254.451

DISCRETE PARK

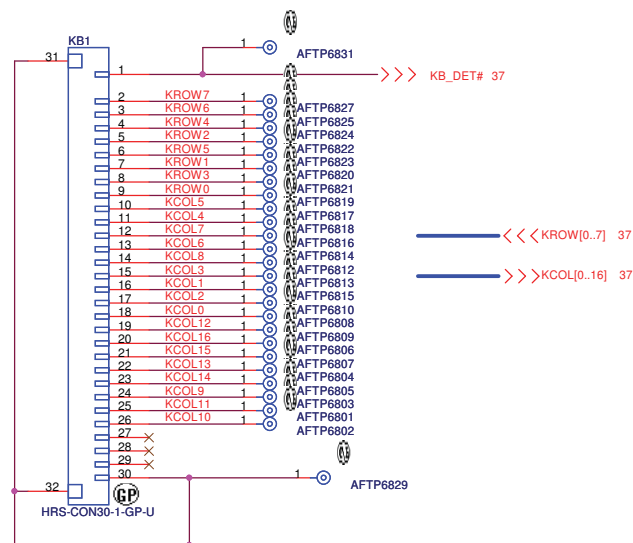
DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title USB			
Size	Document Number	Rev A01	
Arsenal DJ1 Discrete			
Date: Thursday, May 06, 2010	Sheet 63	of 92	

Battery LED



SSID = KBC

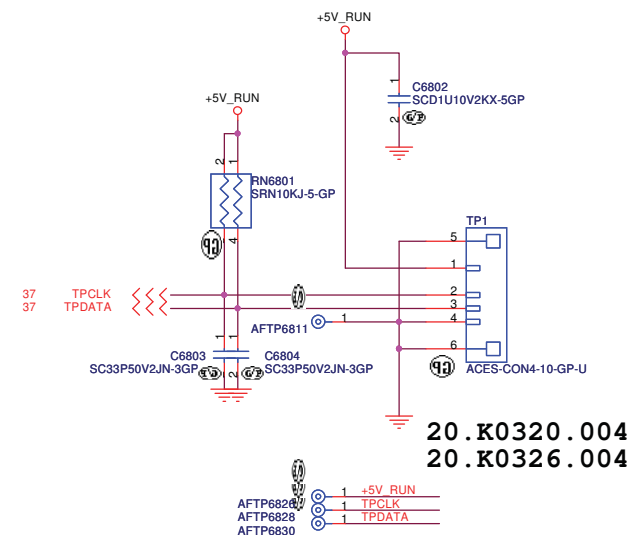
Internal KeyBoard Connector



Main 20.K0421.030
20.K0259.030

SSID = Touch.Pad

TouchPad Connector

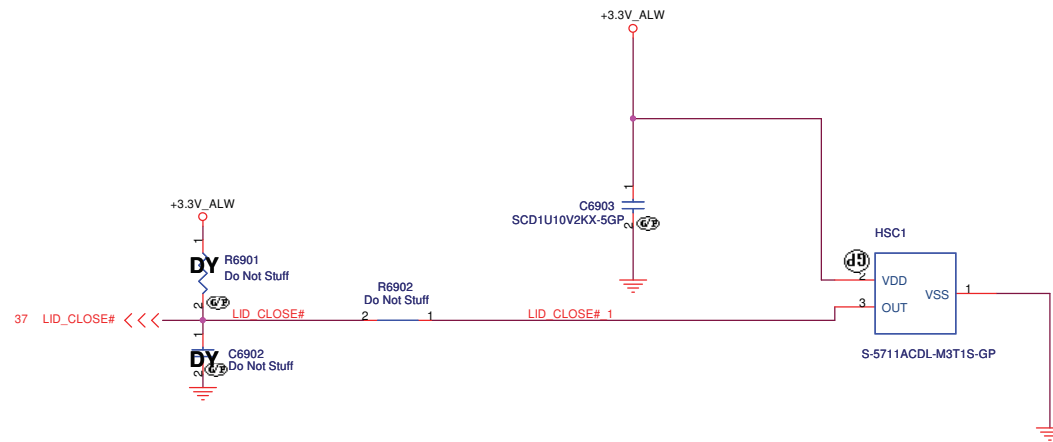


20.K0320.004
20.K0326.004

DISCRETE PARK

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Key Board/Touch Pad
Size A3 Document Number
Arsenal DJ1 Discrete Rev
A01
Date: Thursday, May 06, 2010 Sheet 68 of 92

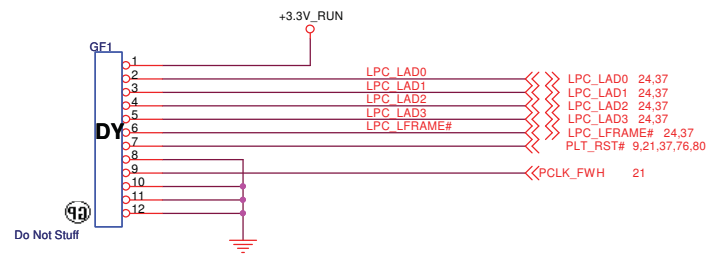


DISCRETE PARK



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Hall Sensor		
Size	Document Number				Rev
A3	Arsenal DJ1 Discrete				A01
Date:	Thursday, May 06, 2010			Sheet 69 of 92	

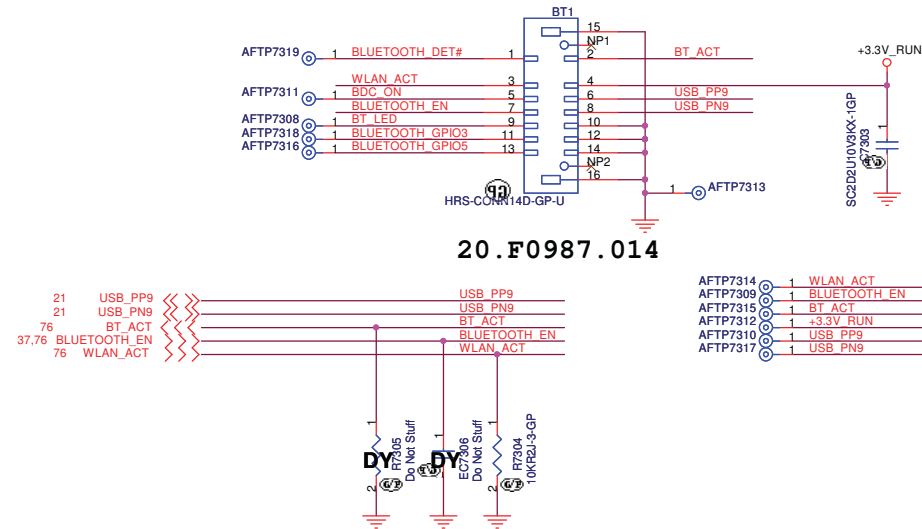


DISCRETE PARK

DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Arsenal DJ1 Discrete		Rev A01
Date: Thursday, May 06, 2010	Sheet 70	of 92	

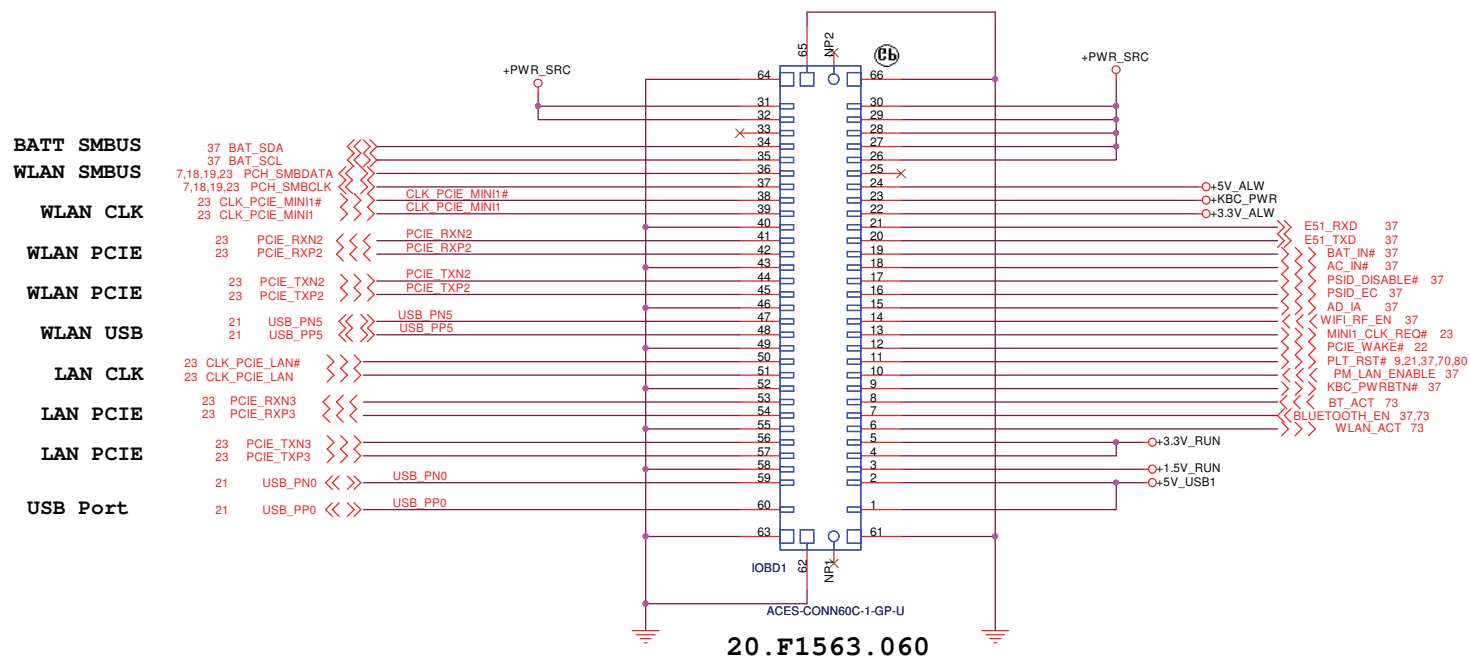
SSID = User.Interface

Bluetooth Module conn.



DISCRETE PARK

SSID = PWR.Support



DISCRETE PARK



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector

Size
A3

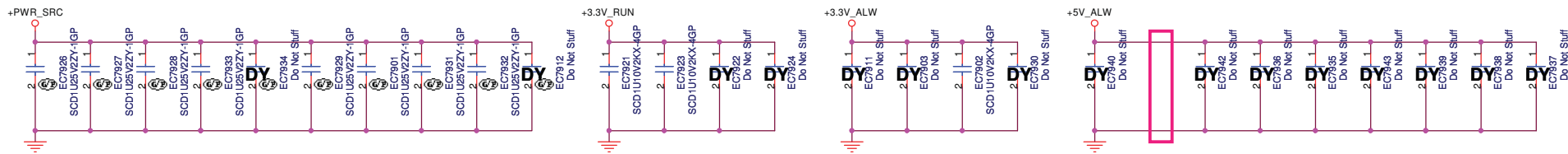
Document Number
Arsenal DJ1 Discrete

Rev

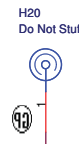
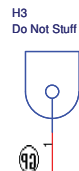
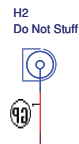
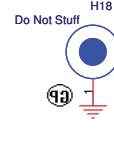
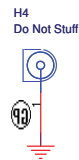
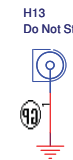
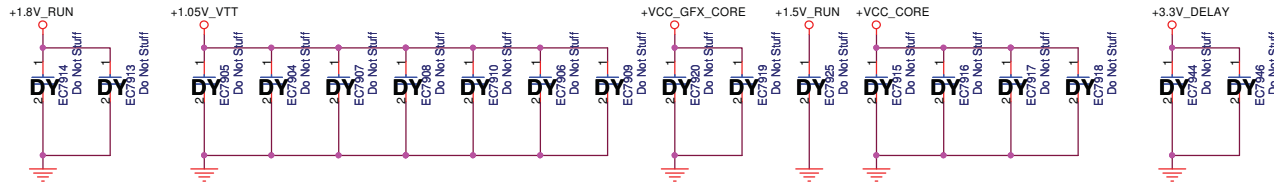
A01

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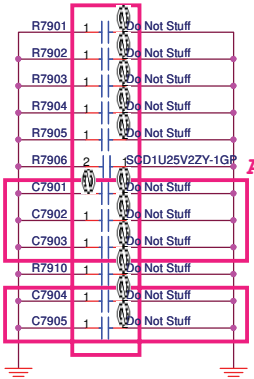


A00 10.03.23



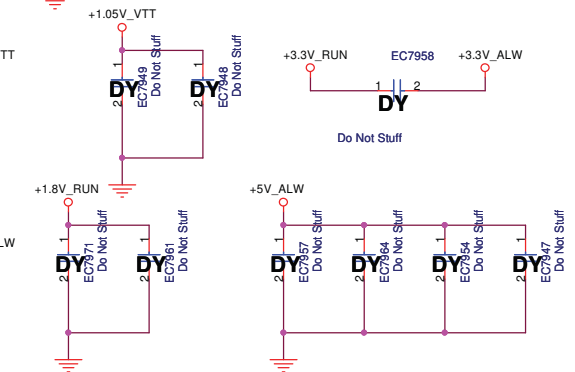
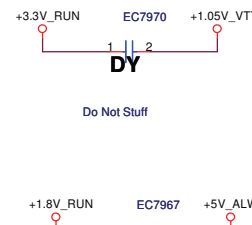
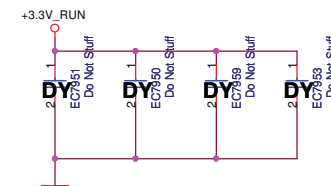
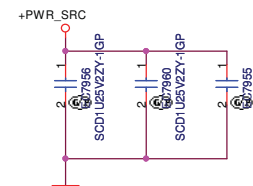
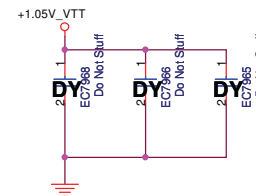
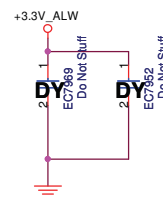
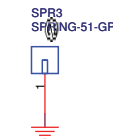
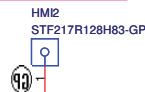
A01 10.05.03

A00 10.03.09 Remove HBT1



A00 10.03.15

A00 10.04.01



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Title		UNUSED PARTS/EMI Capacitors	
Size	Document Number	Rev	
A3	Arsenal DJ1 Discrete	A01	
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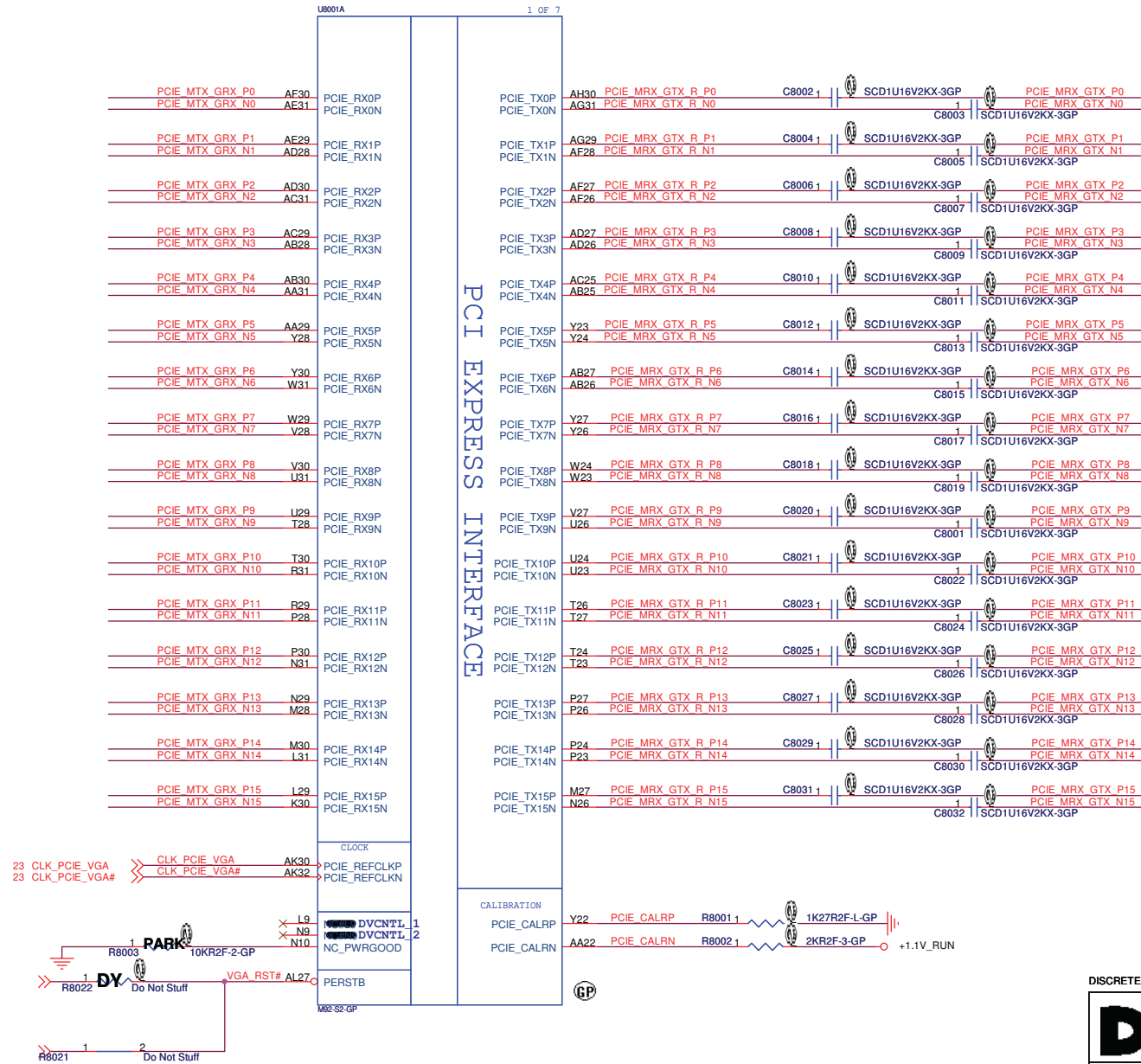
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PCIE_MTX_GRX_P[0..15] << PCIE_MTX_GRX_P[0..15] 8

PCIE_MTX_GRX_N[0..15] << PCIE_MTX_GRX_N[0..15] 8

PCIE_MRX_GTX_P[0..15] >> PCIE_MRX_GTX_P[0..15] 8

PCIE_MRX_GTX_N[0..15] >> PCIE_MRX_GTX_N[0..15] 8



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VGA PCIE(1/4)

Size

Document Number

Arsenal DJ1 Discrete

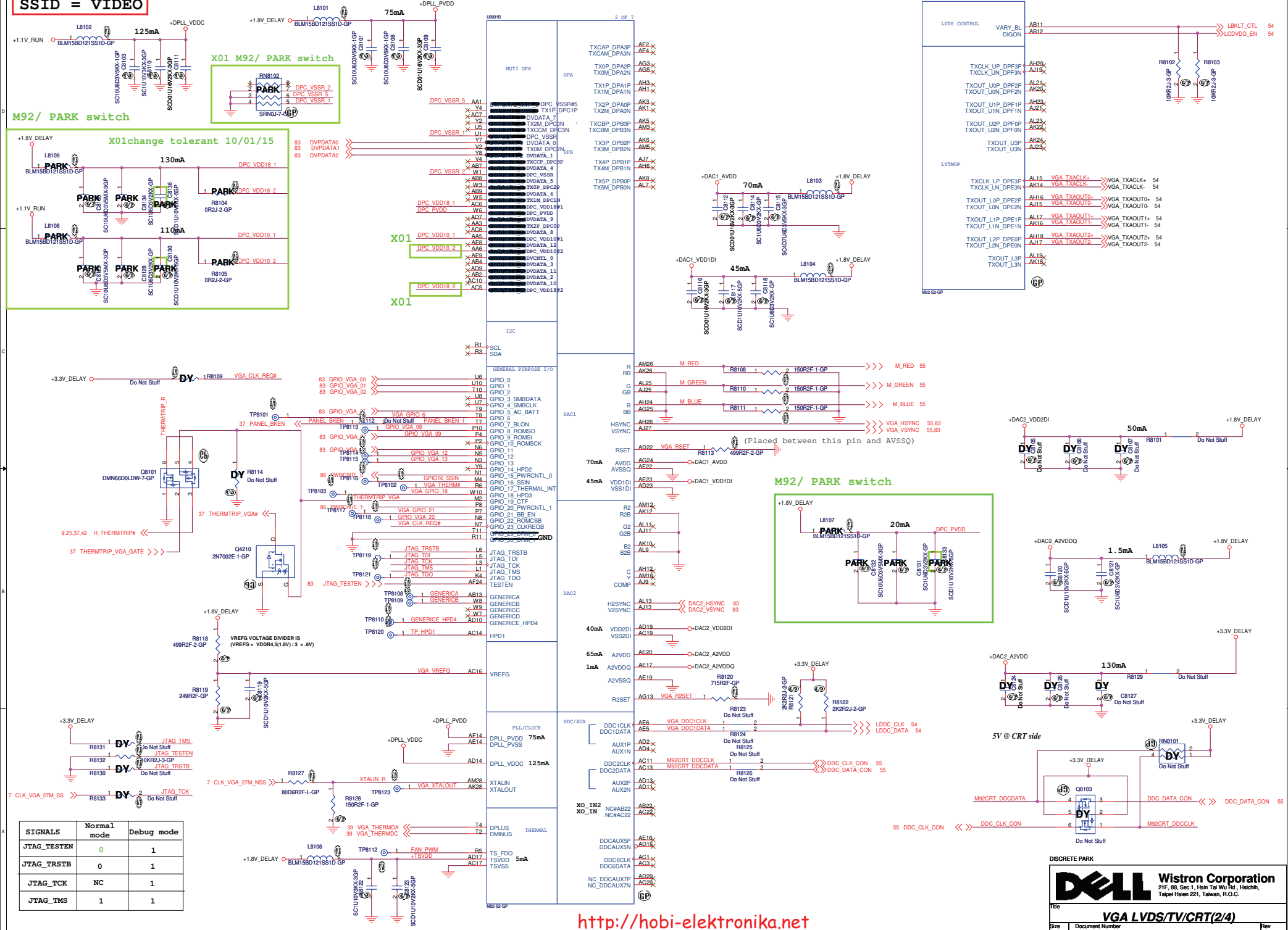
Date _____

Thursday, May 06, 2010

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Date: Thursday, May 06, 2010

SSID = VIDEO



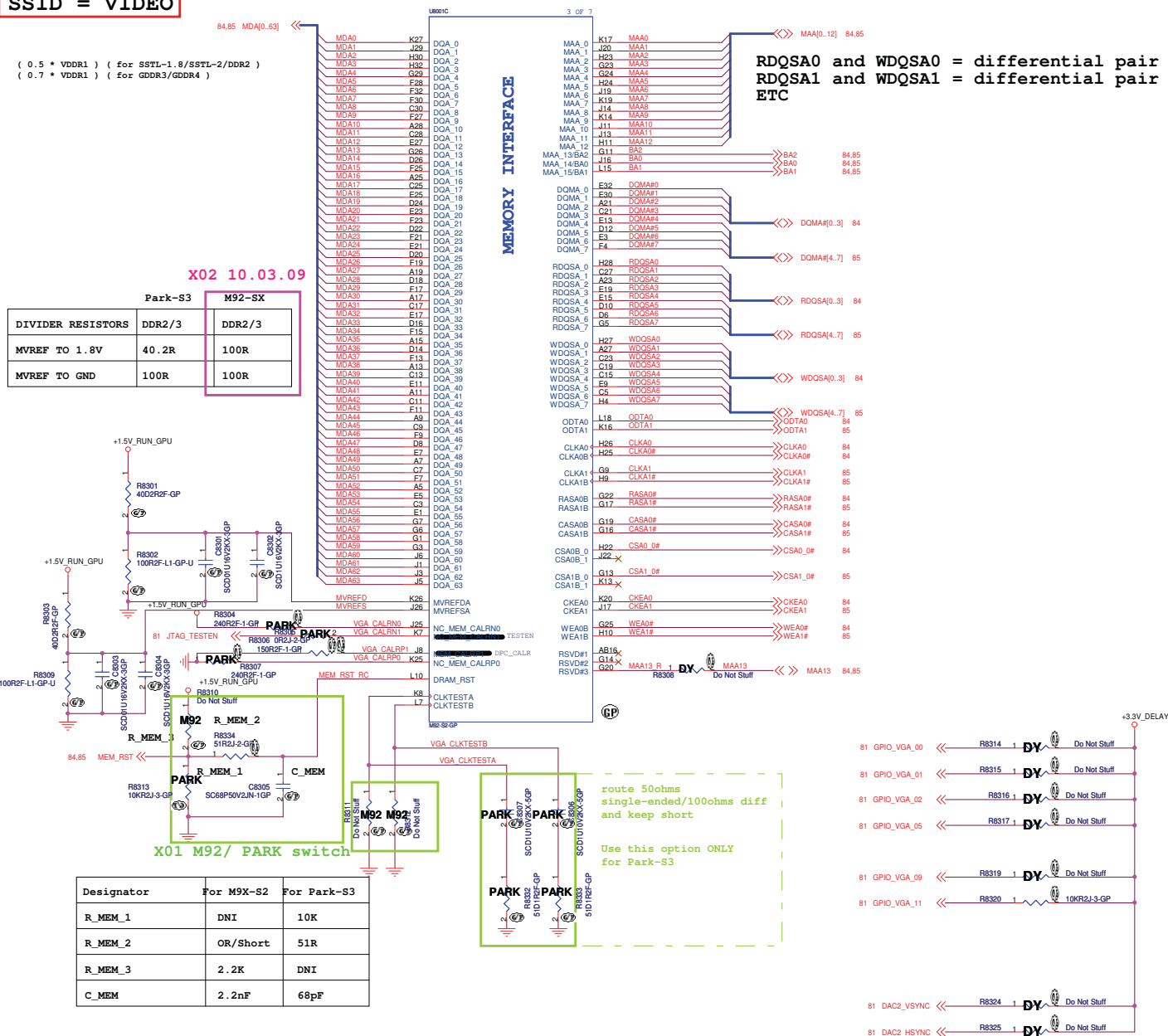
<http://hobi-elektronika.net>

U6001E



SSID = VIDEO

```
( 0.5 * VDDR1 ) ( for SSTL-1.8/SSTL-2/DDR2 )
( 0.7 * VDDR1 ) ( for GDDR3/GDDR4 )
```



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESE

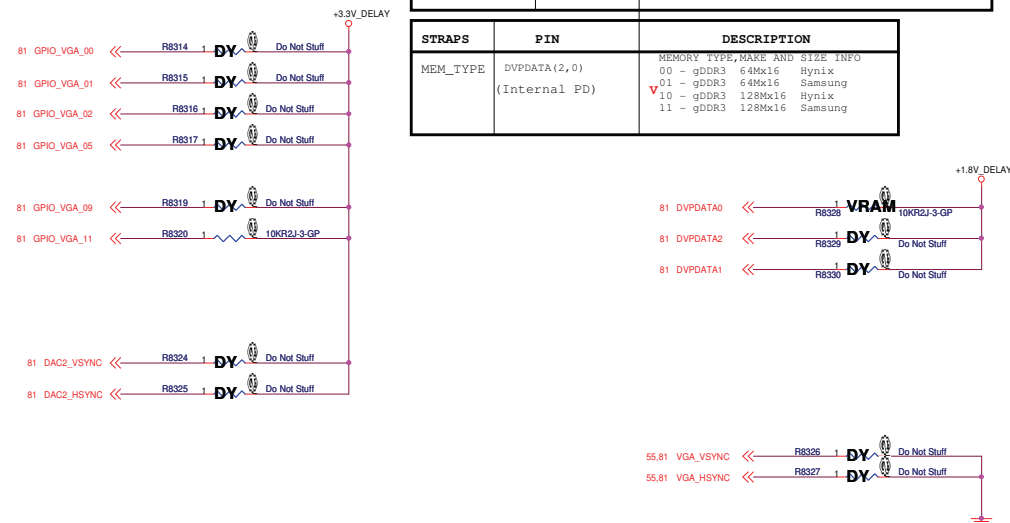
GPI03 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	ST Microelectronics	M25P05A	0100
	256MB		M25P10A	0101
	64MB		M25P20	0101
	32MB		M25P40	0101
	512MB		M25P80	0101
	1GB			
	2GB	Chingis (formerly PMC)	Pm25LV512A	0100
	4GB		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13, 12, 11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00: No audio function 01: Audio for DisplayPort and HDMI 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVFPDATA(2,0)	MEMORY TYPE, MAKE AND SIZE INFO
	(Internal PD)	00 - gDDR3 64Mx16 Hynix 01 - gDDR3 64Mx16 Samsung 10 - gDDR3 128Mx16 Hynix 11 - gDDR3 128Mx16 Samsung



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100

VGA MEMORY/STRAPS(4/4)

Size

Document Number

Arsenal DJ1 Discrete

Date:

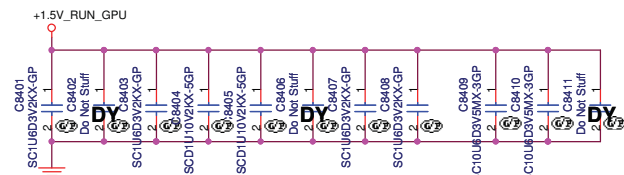
Thursday, May 06, 2010

Discipline

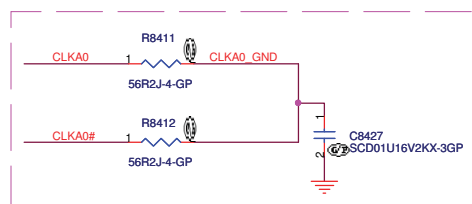
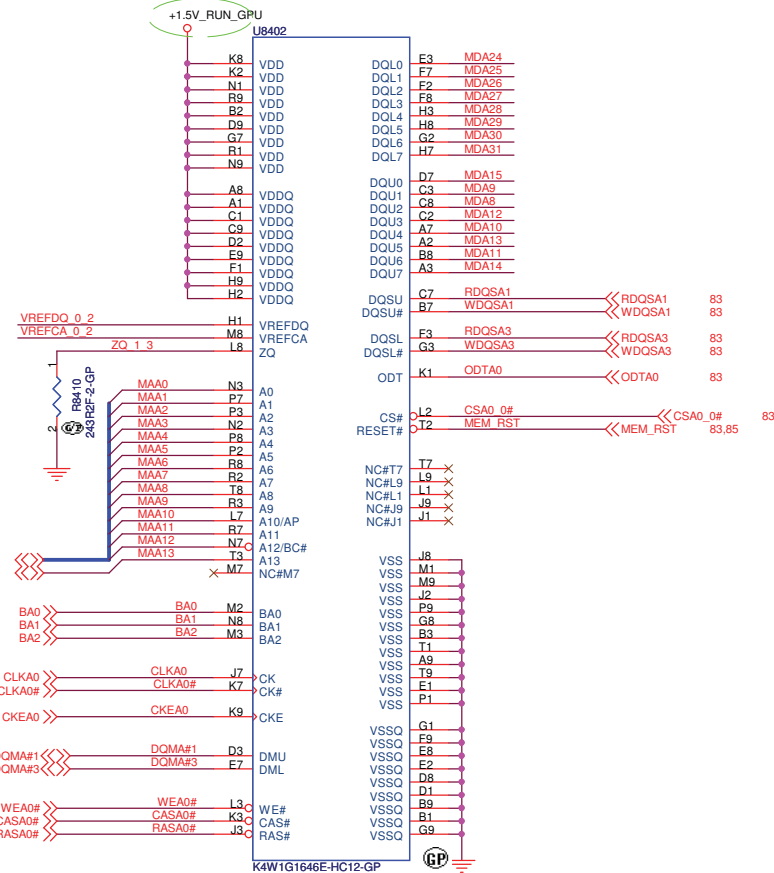
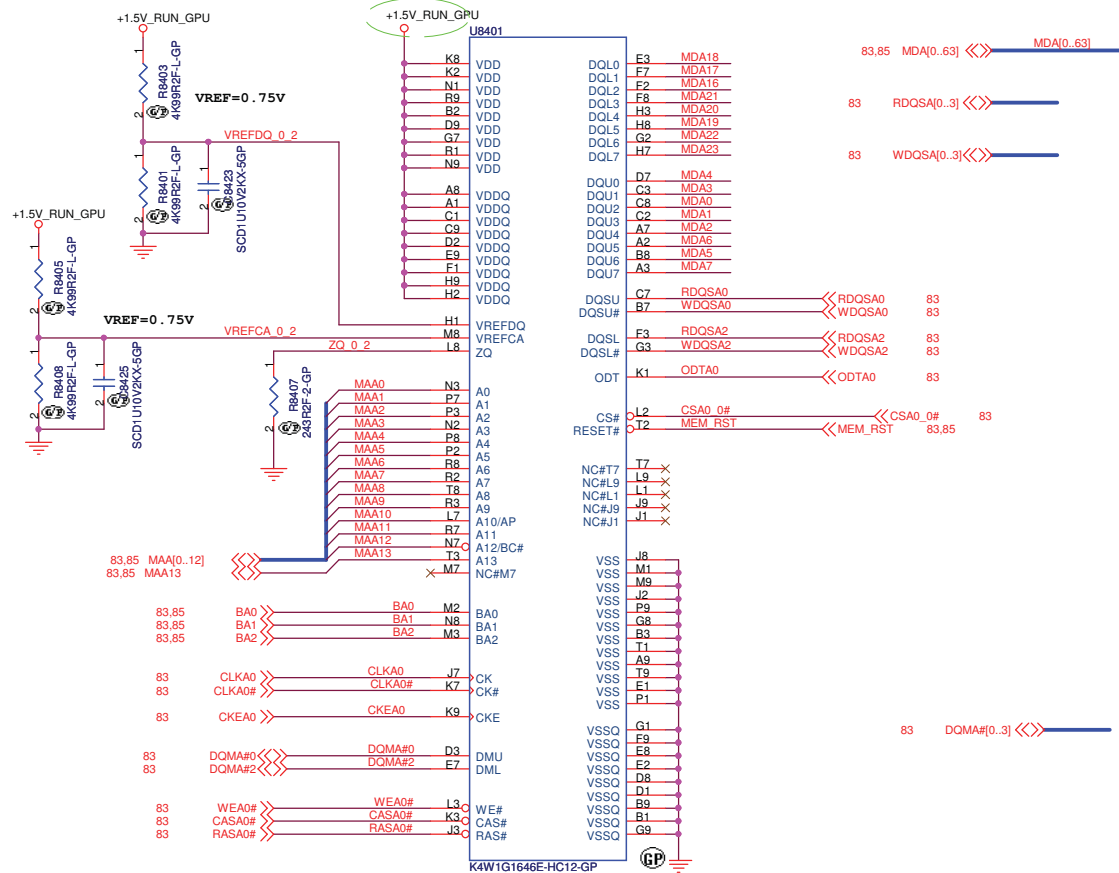
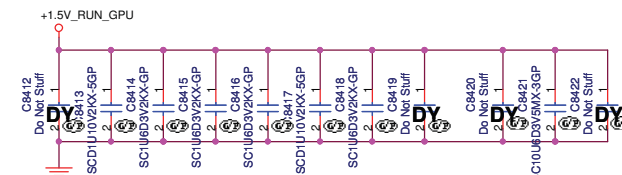
Rev

SSID = VIDEO

Place blow decoupling caps close VDD pin.



Place blow decoupling caps close VDD pin.



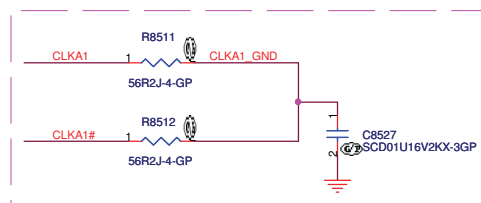
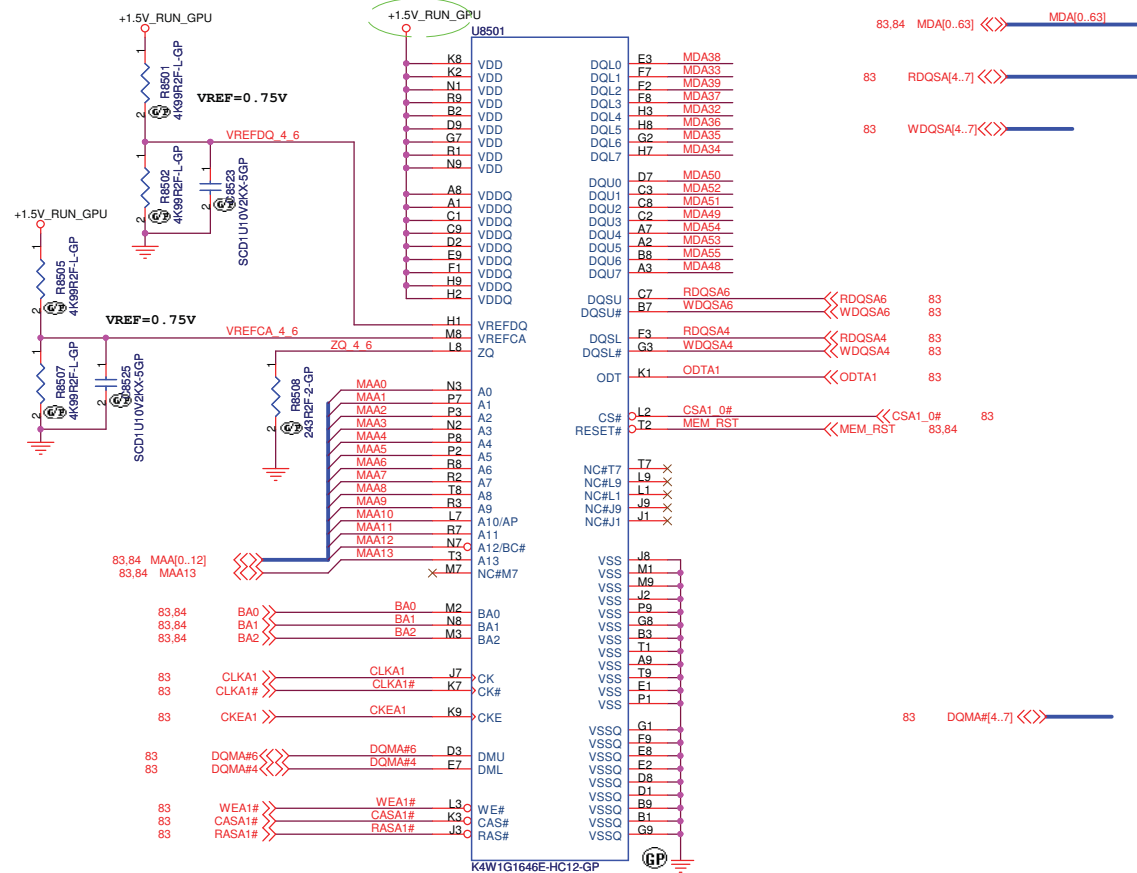
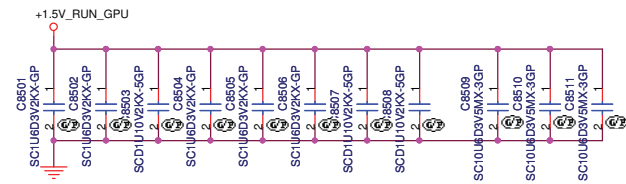
DISCRETE PARK



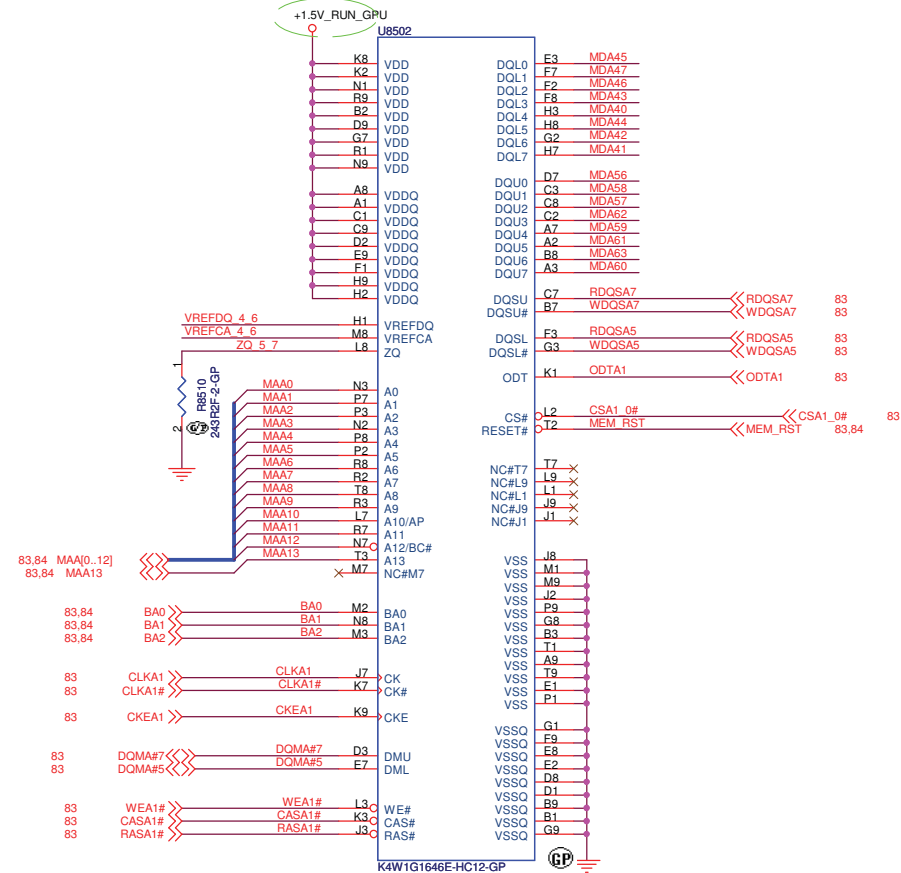
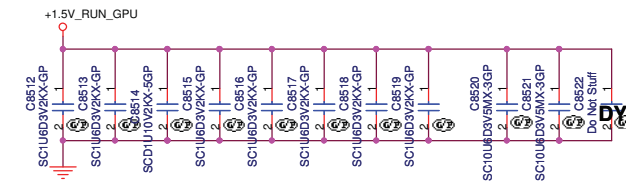
Title			
GPU-VRAM (1/2)			
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SSID = VIDEO

Place blow decoupling caps close VDD pin.



Place blow decoupling caps close VDD pin.



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Title

GPU-VRAM (2/2)

Size

Size	
Custom	

Date: Thursday, May 06, 2010

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A01

Date: Thursday, May 06, 2010

Shee

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RT8208BGQW for +VGA_CORE



PARK-LP Power-Play

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec DCR:18mohm/201mohm Isat=14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCK0D221ER 15mOhm 2.7Arms PANASONIC/ 79.2719.20L2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SI1R460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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RT8208B +VGA_CORESize
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A01

The diagram shows a circuit for providing 1.5V to an M92 module. A red line represents the power supply, starting from a terminal labeled '+1.5V_RUN_GPU' at the top. The line passes through a blue zigzag resistor symbol and a blue capacitor symbol (labeled 'C'). It then enters a blue rectangular box representing the M92 module. Inside the box, the text 'M92' is displayed, and below it, the text 'Do Not Stuff' is written. The power line exits the bottom of the box and connects to a terminal labeled 'RUN_ON_1.5V#'. A ground symbol is shown at the bottom of the circuit.

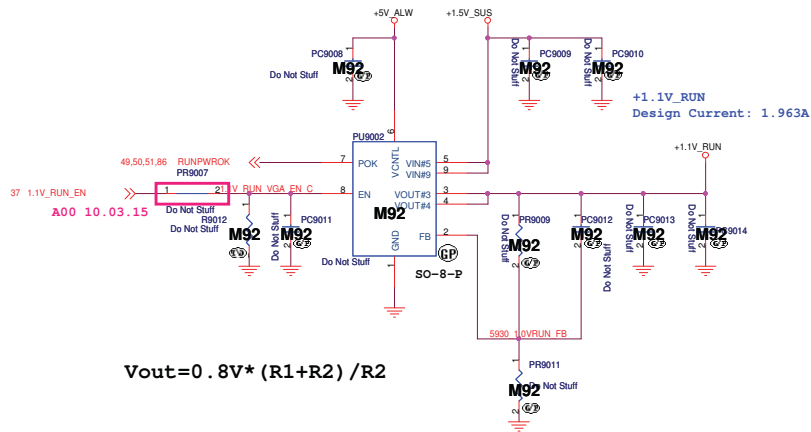
Peak current: 3520mA
 Design current: 2464mA
 11.6A
 Rds=14m ohm ==> 0.04928

For Discrete +1.5V_RUN

Rds=14m ohm ==> 0.04928


For Discrete +1.5V_RUN

APL5930KAI for +1.1V_RUN



Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	47	2010/01/04	Wistron	CPU core power was two phase	Remove PC4766	
2	81 82 83	2010/01/04	Wistron	M92/ PARK switch	ADD RN8102,R8104,R8105,R8201,L8202,L8212,C8203 R8310,R8311,R8312 Connect Ball L17 to +1.5V_RUN_GPUand Ball L16 to GND	X01 X01
3	81	2010/01/04	ATI	Modify Park to Normal mode	PD R8132 to GND	X01
4	87	2010/01/04	Wistron	Derect connect +1.5V_RUN to +1.5V_RUN_GPU.	Change +1.5V_SUS power rail to +1.5V_RUN ADD R8701,R8702 NOPOP U4202,C4203,C4204,R4209,R4208 Q4203,R4215,Q4206	X01
5	80 81 82 83 84	2010/01/04	Wistron	BOM Control	PARK:POP R8003,RN8102,R8104,R8105,C8134,C8135,C8136 C8128,C8129,C8130,L8108,L8109,C8131,C8132,C8133 L8107,C82127,C82129,C82125,C82130,L8213,L8214 R8209,L8211,R8313,C8306,C8307,R8332,R8333,R8308 ,R8304,R8305,R8307,R4212 M92:POP R82011,C8203,L8202,L8212,R8310,R8311,R8312 R4211,R4213,Q4204,Q4205	X01
6	37 62	2010/01/05	Wistron	Improve BIOS data loss issue.	ADD U3702 circuit POP R6210 NOPOP R6203	X01
7	87 88	2010/01/05	Wistron	M92/Park Co-lay to use 1.1V_RUN LDO.	ADD PU9002 LDO circuit Remove U8703 MOSFET circuit	X01
8	59	2010/01/06	Wistron	Suyin ODD connect PT build SMT issue	Change to 22.10300.811	X01
9	7 46 60 79 86	2010/01/06	Wistron	EMI requirement	Pop EC7932,EC7960,EC7933,EC7928,EC7931,EC7929,EC7901 ,EC7926,PC8911,PC4610,EC7927,EC7962,EC7955,PC4616, EC7956,EC7923,EC7921,EC7902,PC4619,EC6001,EC6002, EC6003,EC6004,EC703	X01
10	62	2010/01/07	Wistron	Change RTC battery connect drawing from Coxoc to Foxconn by SMT issue	Change to 62.70001.011	X01
11	24	2010/01/07	Wistron	Schematic could not PD this pin	Packege ball name:AY3 NC	X01
12	39	2010/02/24	Wistron	T8 shutdown is set 88 deg-C.	Change R3915 to 64.28015.6DL	A00
13	37	2010/02/24	Wistron	Change MB VERSION ID and GPU table	POP R3723,R3722 NOPOP R3725 Remove R3724,R3727	A00
14	37	2010/02/24	Wistron	Power bottom delay issue	NOPOP Reset IC U3702	A00

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15	32 54	2010/03/09	Wistron	EMI requirement	ADD TR3201,TR5401	A00
16	79	2010/03/09	Wistron	ME requirement	Remove HBT1	A00
17	09	2010/03/09	Wistron	S3 Power Reduction requirement	POP U927,R2114,R977 NOPOP R978	A00
18	09	2010/03/09	Wistron	DDR3_DRAMRST# drop issue	ADD C903	A00
19	79	2010/03/09	Wistron	Change page83 DIVIDER RESISTORS table		A00
20	37	2010/03/15	Wistron	Support RCID function schematic when pop Q3706	ADD Q3706	A00
21	46	2010/03/15	Wistron	Operation Mode Select to Diode Emulation Mode	POP PR4619 NOPOP PR4618	A00
22	79	2010/03/15 2010/05/03	Wistron	EMI requirement	Reserve Pad C7901,C7902,C7903	A00
23	54	2010/03/15	Wistron	LCD VDD power	ADD C5412 ,change C5410 from 0.1uf to 1uf	A00
24	46 47 50 88	2010/03/16	Wistron	Change 0 ohm to short pad	R2114,R4218,PR4620,PR4616,PR4619,PR4706, PR4708, PR4713, PR4718, PR4722,PR4732, PR4738, PR4744, PR4755, PR4764, PR4704,PR4703, PR4707, PR4711, PR4784,PR4790, PR4784,PR4776,PR5002,PR9007,R3751	A00
25	47 49 50 89	2010/03/16	Wistron	change to 2.7Kohm for CPU_CORE load/line setting. change to 1.4Kohm for CPU_CORE OCP setting. change to 1ohm for boost resister. change to 73.2Kohm for 1.05V OCP setting. change to 8.2Kohm for 1.5V OCP setting. change to 8.45Kohm for VGA_CORE OCP setting.	PR4705 change to 2.7Kohm PR4727 change to 1.4Kohm PR4901 change to 1ohm PR4902 change to 73.2Kohm PR5007 change to 8.2Kohm . PR8905 change to 8.45Kohm	A00
26	46 48 49 50 86	2010/03/16	Wistron	Power requirement	Change PL4814,PL4817 from 68.R3610.10M to 68.R3610.10T Change PL4602 from 68.2R21B.10A to 68.2R210.20Q Change PL8601 from 68.2R210.20B to 68.2R210.20Q Change PL4601 from 68.3R31A.10W to 68.3R310.20I Change PTC4602 from 77.23371.12L to 77.C2271.00L Change from 68.R5610.10D to 68.R5610.20I Change PL5001 from 68.1R510.10J to 68.1R510.20I	A00
27	63	2010/03/17	Wistron	USB Enable pin signal issue remove UPI vendor	Change U6302,U6301 to GMT symbo	A00
28	42	2010/03/17	Wistron	Change symbo from VISHAY to AOL	Modify U4204	A00
29	48 49 50	2010/03/18	Wistron	Power requirement	Change PQ4840 PQ4833 PU4902 PU5003 from 84.07686.A37 to 84.07686.037	A00
30	12 18 19	2010/03/24	Wistron	PSE issue,Layout routing	Remove C1219,C1211,C1803,C1804, C1809,C1905,C1911,C1912	A00
31	09	2010/03/25	Wistron	XDP1 change to ZZ.00PAD.Q81		


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Title
Change History

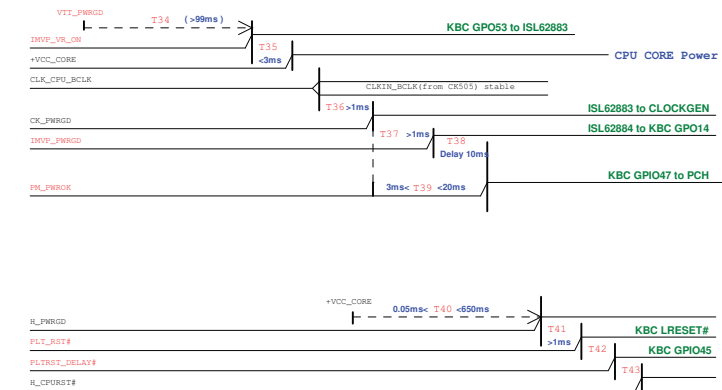
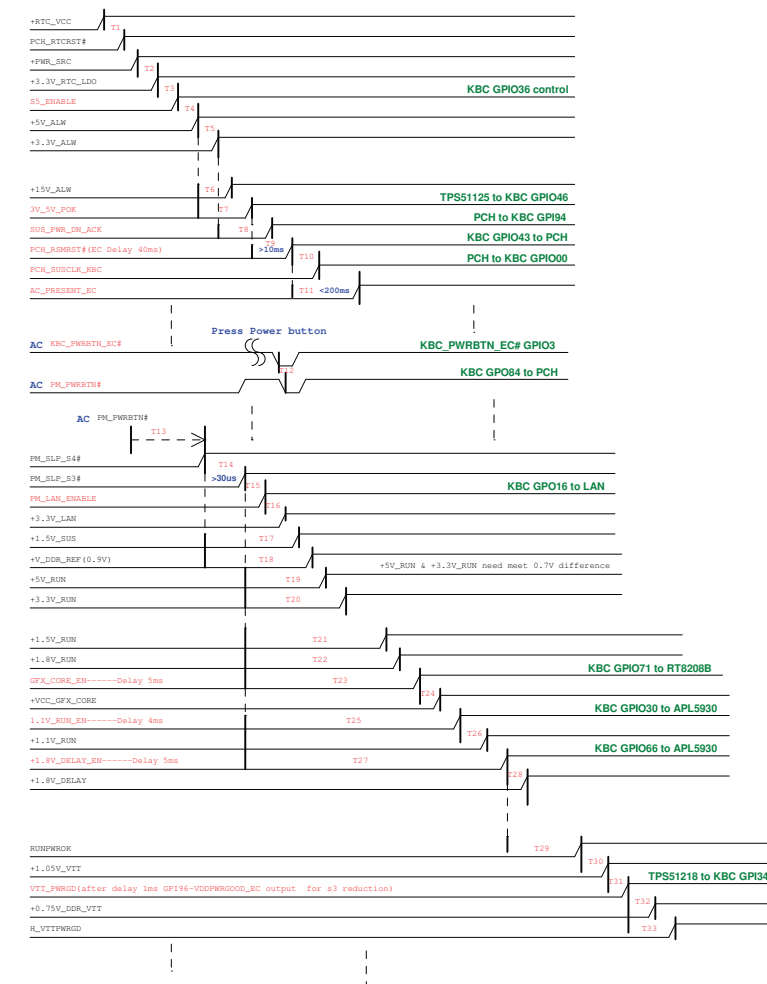
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Item	Page#	Date	Request By	Issue description		Solution Description			Rev.
32	79	2010/05/03	Wistron	EMI requirement		POP C7901,C7902,C7903,C7904,C7905,R7901,R7902,R7903,R7904,R7905,R7906,R7910			A01

(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO

