

MAKI Block Diagram

Project code: 91.4U601.001
 PCB P/N : 07204-SC
 Revision :

PCB STACKUP	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	POWER
L5:	Signal 3
L6:	Signal 4
L7:	GND
L8:	Signal 5

SYSTEM DC/DC TPS51120 29	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)
SYSTEM&VRAM DC/DC SC411 30	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)
TPS51100 31	
1D8V_S3	DDR_VREF_S0(1.5A) DDR_VREF_S3
APL5913	
1D8V_S3	1D5V_S0(2A) 31
APL53123	
3D3V_S0	2D5V_S0(300mA)
APL5915 31	
3D3V_S5	1D25V_S0
MAXIM CHARGER MAX8725 32	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 4.0A UP+5V 5V 100mA
CPU DC/DC ISL6262 28	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
VGA NVIDIA ISL6269	
INPUTS	OUTPUTS
DCBATOUT	NVDD_S0 1.2V 25A

CLK GEN.
ICS 9LPRS365 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U 4,5

HOST BUS 667/800MHz@1.05V

DDR2
533/667 MHz 11
533/667MHz

DDR2
533/667 MHz 11
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPCS
LVDS, CRT I/F
71.CREST.00U 6,7,8,9,10

G792 17

DOCK CRT & TV-OUT 42

DOCK HDMI 42

DVI 13

ATI M76-M
Page.44-50

VRAM 256M
DDR333 49,50

LVDS **WWSXGA / WUXGA** 13
15"LCD

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U 14,15,16

LAN
10/100/1000
INTEL 82566MM
Page.23,24

TXFM

SYSTEM RJ45

Codec
ALC885S 28
AZALIA

MIC In x2

OP AMP
G1432Q 29

INT.SPKR x2

DOCK BASE BARD
PCI-Express Repeater/
PI2EQX4401D

PCI-E1
USB 2.0 PORT3/PORT6

I/O BARD
Smart Card Reader
ST7GEM

USB 2.0 PORT1

Dock Port

- 1x DC Jack In
- 1x RJ-45 Ethernet Port
- 1x HDMI
- 1x CRT
- 4x USB 2.0
- 1x Audio In
- 1x Subwoofer
- 2x SATA for RAID
- 1x battery
- 1x ExpressCard/54
- 1x Audio Out
- 1x SPDIF in
- 1x SPDIF out
- 1x S-Video
- 1x Mini card

Marvell
88SE6121
SATA/RAID
Page.22

PCI-E2

DOCK
SATA HDD2,3

SATA HDD 19

CD-ROM 19

RATA

USB 2.0(PORT9) **Fingerprint**
TCS4B/4C

USB 2.0(POR(0,5)) **USB x 2** 20

USB 2.0(PORT8) **Camera**

USB 2.0(PORT7) **BlueTooth**

SPI I/F BIOS
W25X80

KBC
Winbond WPC8768L 18

LPC DEBUG CONN 27

TPM
SLB 9635 31

Keys board 27

Touch Pad 27

FIR (only)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

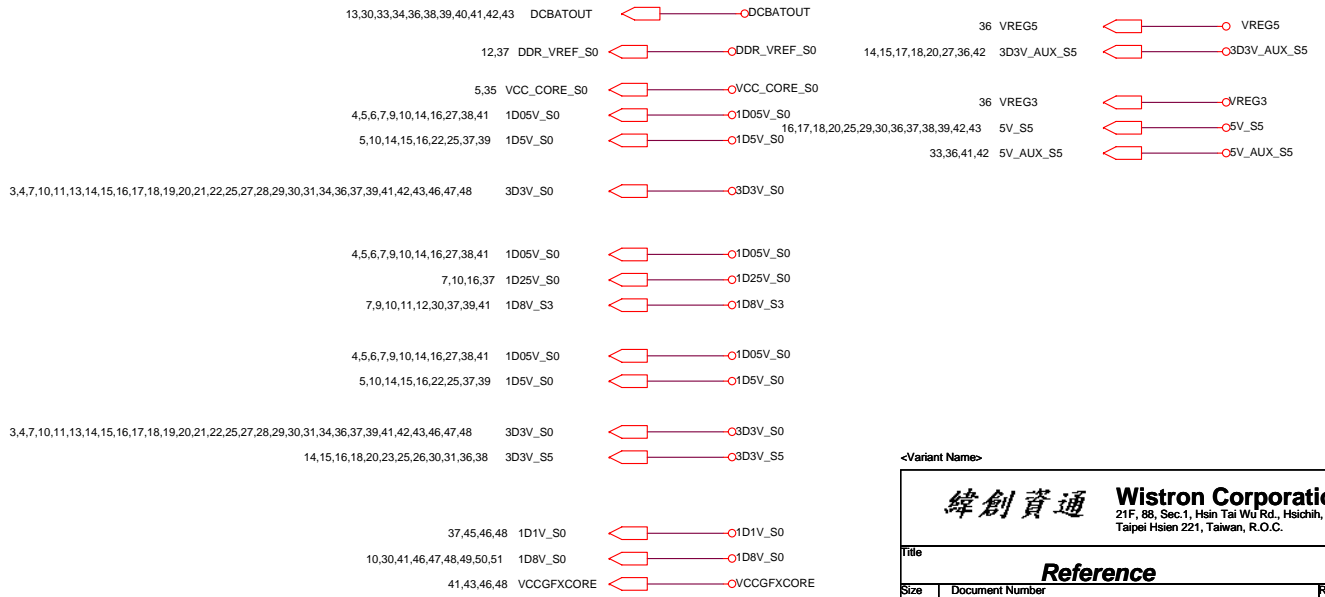
Size Custom	Document Number	Rev SA
MAKI		SA
Date: Friday, January 18, 2008	Sheet 1 of 51	

CHANGE TO 71.PM965.A0U
CHANGE TO 71.ICH8M.A0U
change 71.0M71M.00U to 71.0M76M.M02

U3371.ICH8M.A0U--> Symbol has not been created in CIS DB !!
U6272.18512.I0U--> Symbol has not been created in CIS DB !!
U6372.18512.I0U--> Symbol has not been created in CIS DB !!
U6471.0M76M.M02--> Symbol has not been created in CIS DB !!
U6571.PM965.00U--> Symbol has not been created in CIS DB !!
U6672.18512.I0U--> Symbol has not been created in CIS DB !!
U6772.18512.I0U--> Symbol has not been created in CIS DB !!

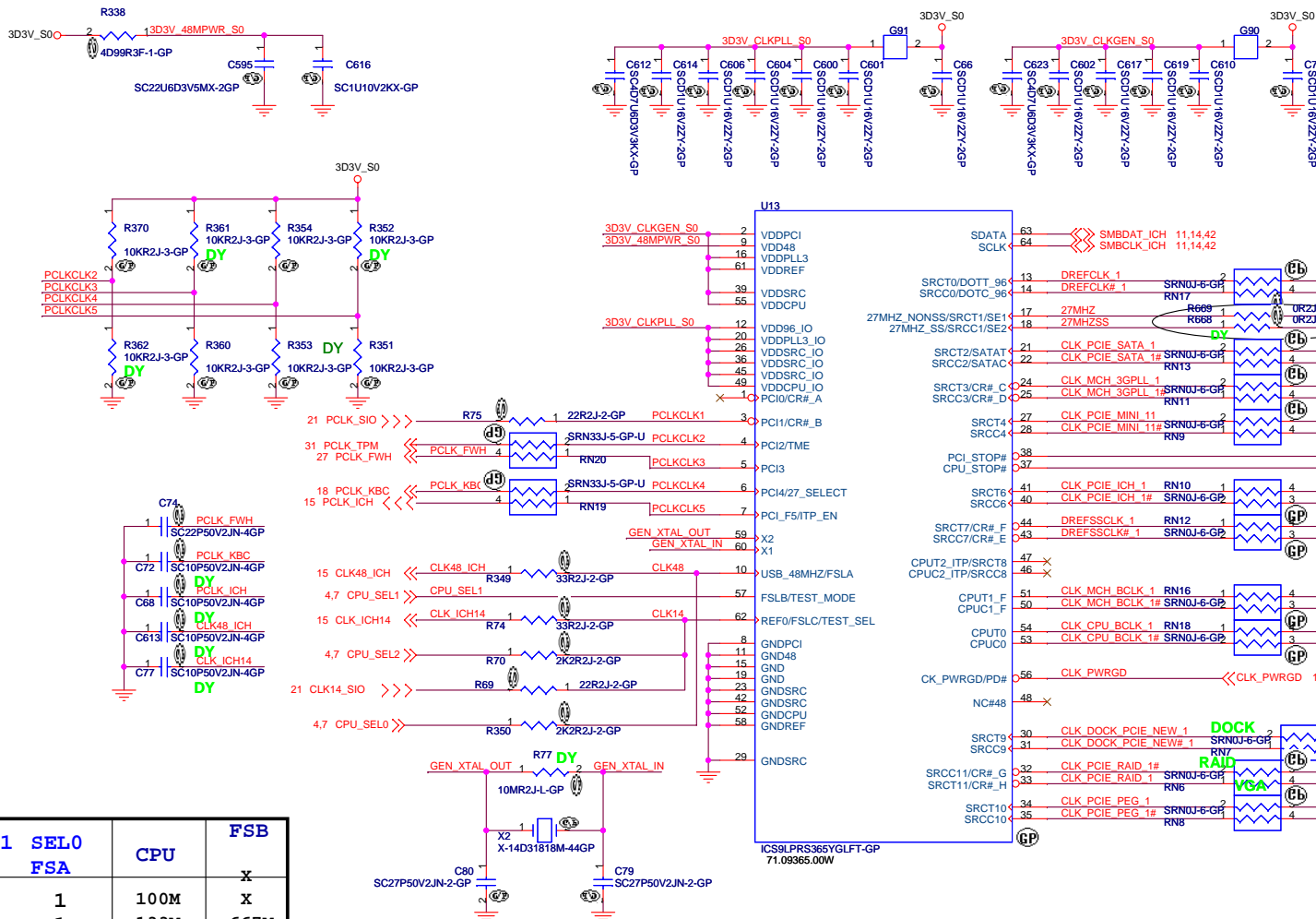
H1934.4B804.001--> Symbol has not been created in CIS DB !!
H2334.4B804.001--> Symbol has not been created in CIS DB !!
H2434.4B804.001--> Symbol has not been created in CIS DB !!
H334.42003.001--> Symbol has not been created in CIS DB !!
H434.42003.001--> Symbol has not been created in CIS DB !!
H634.42003.001--> Symbol has not been created in CIS DB !!
H734.4B804.001--> Symbol has not been created in CIS DB !!

1.net:AD+ DOCK_IN change 20mil
2.crt 5v_s0 net:20mil



<Variant Name>

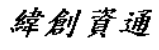
緯創資通		Wistron Corporation	
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Reference			
Size	Document Number	Rev	
Custom	MAKI	SA	
Date:	Friday, January 18, 2008	Sheet	2 of 51



SEL2	SEL1	SELO	CPU	FSB
FSC	FSB	FSA		X
1	0	1	100M	X
0	0	1	133M	667M
0	1	1	166M	800M
0	1	0	200M	

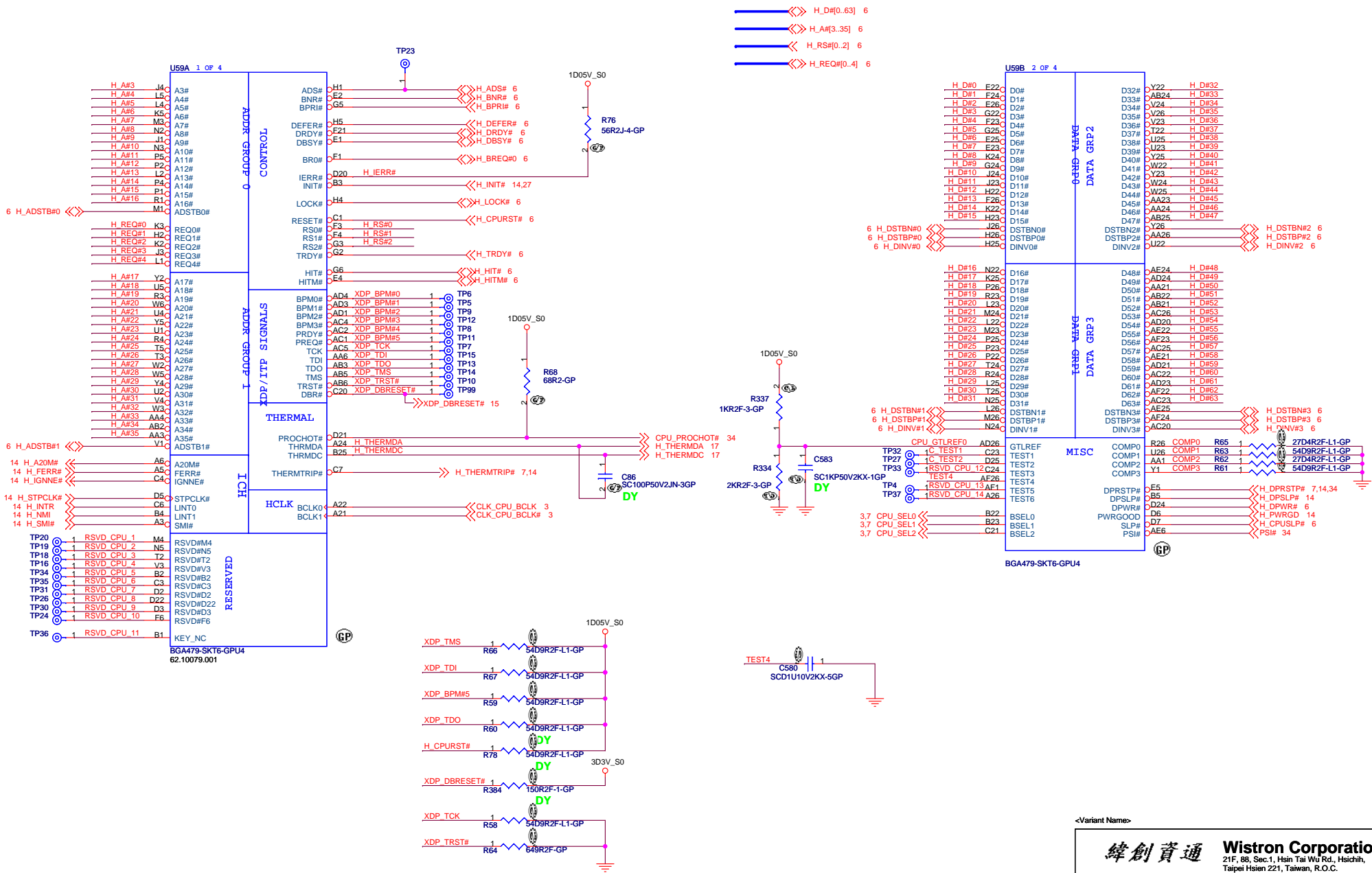
PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/RC-5_EN	0 = Pin37 as CPU_STOP#, pin 38 as PCI_STOP#. 1 = Pins37,38 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

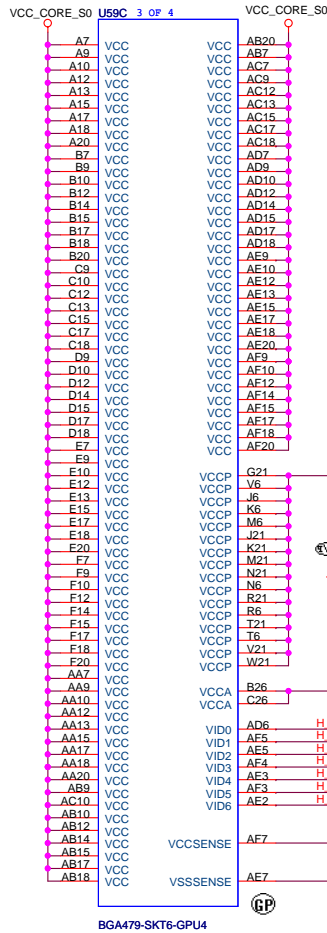
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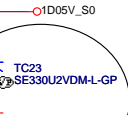
緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Clock Generator		Rev
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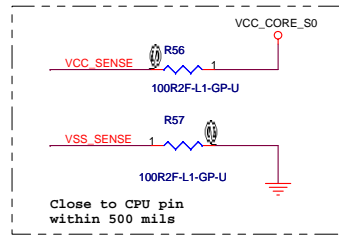
lvccp boot= 4.5A
lvccp stable= 2.5A



Place close to CPU socket
A-note2

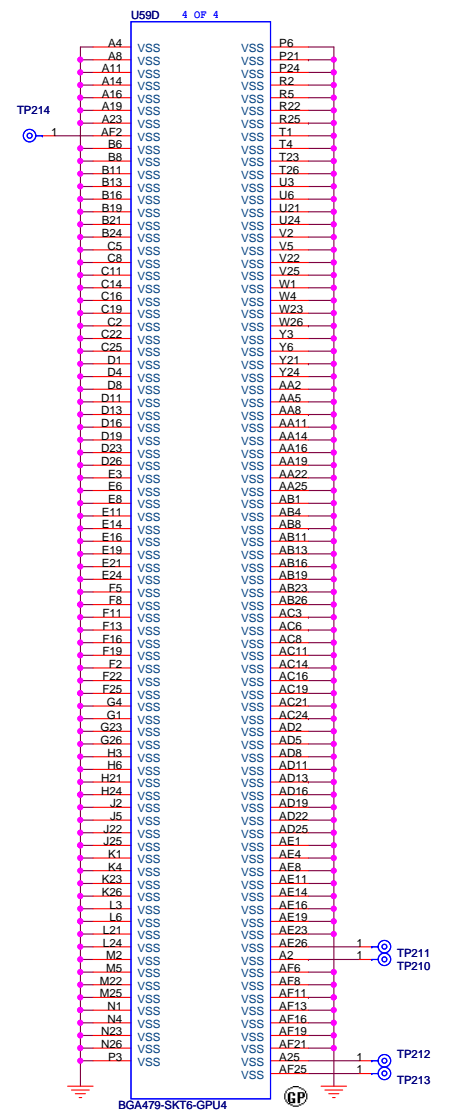
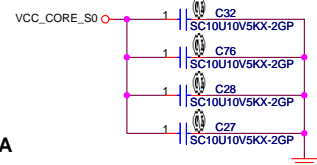
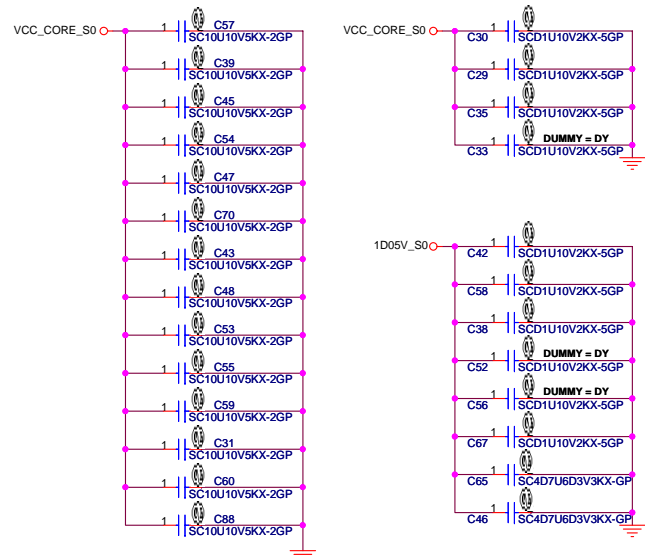
IVCCA = 130mA

layout note: "1D5V_VCCA_S0"
as short as possible



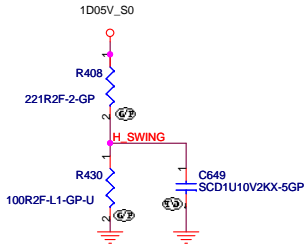
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

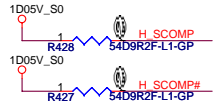


H_SWING routing Trace width and Spacing use 10 / 20 mil

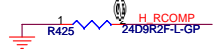
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



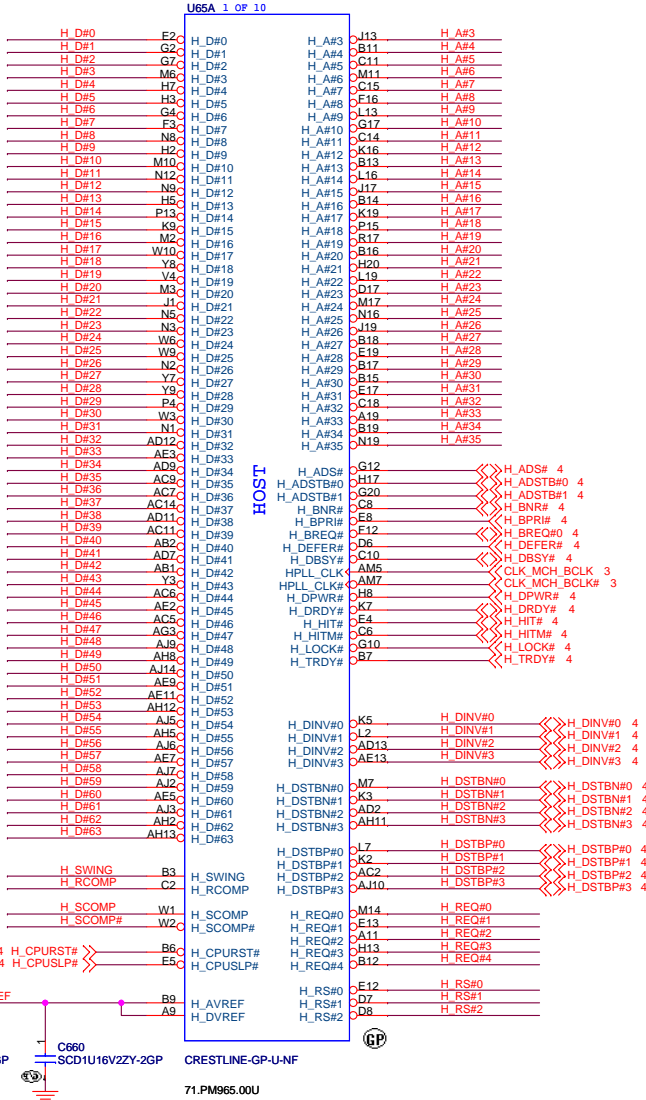
H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

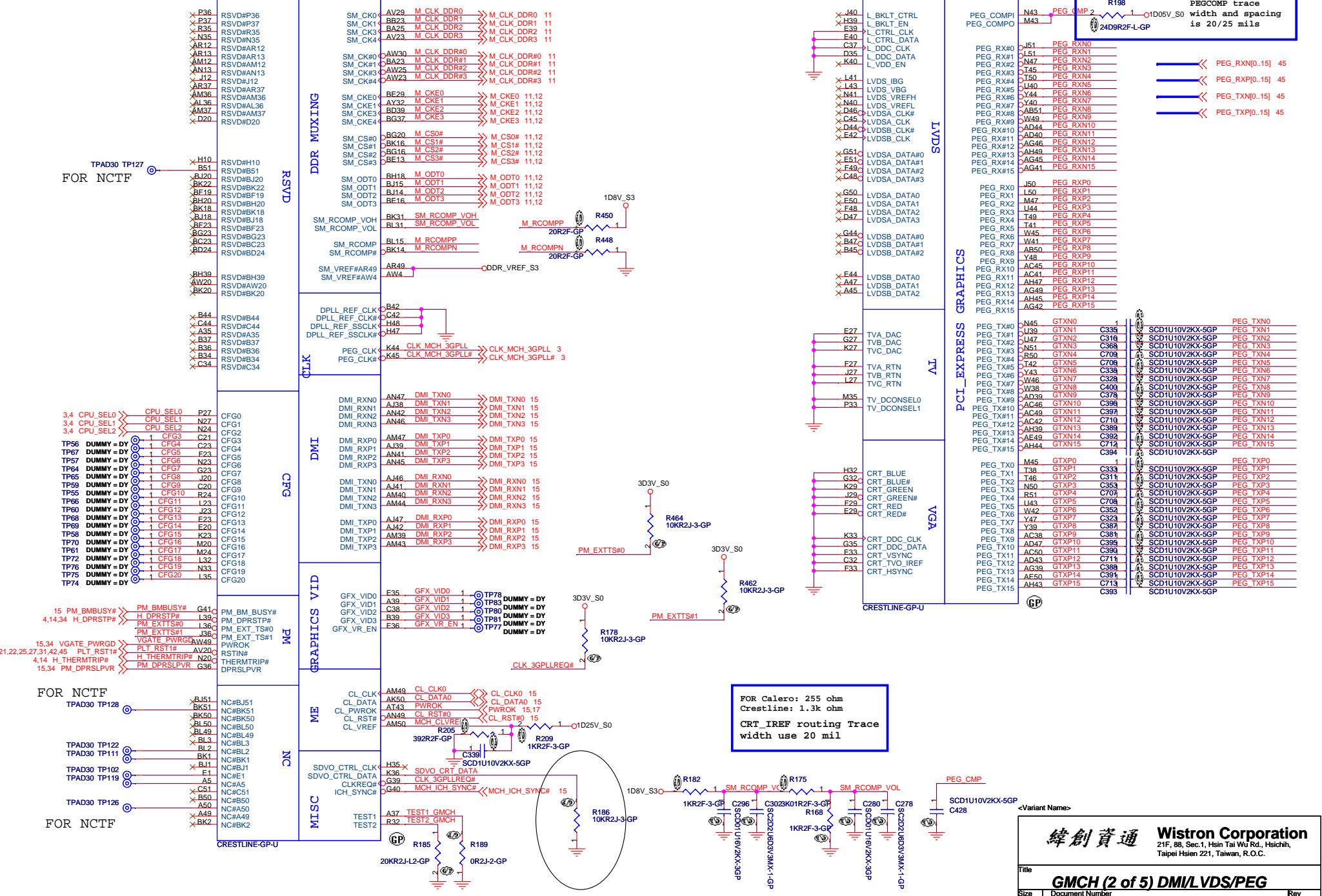


H_REF Decoupling Crestline close Crestline 100 mil

CHANGE TO 71.PM965.00U

<Variant Name>

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Title			
GMCH (1 of 5) AGTL			
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MAKI			
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R198
 PEG2 COMP trace width and spacing is 20/25 mils

FOR Calero: 255 ohm
 Crestline: 1.3k ohm
 CRT_IREF routing Trace width use 20 mil

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (2 of 5) DMI/LVDS/PEG
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U6S1		
A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AF20	VSS	BB44
AF23	VSS	BB49
AF24	VSS	BB8
AF31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC36
AG47	VSS	BC40
AG50	VSS	BC51
AH3	VSS	BD13
AH40	VSS	BD2
AH41	VSS	BD28
AH7	VSS	BD45
AH9	VSS	BD48
AJ11	VSS	BD5
AJ21	VSS	BE13
AJ24	VSS	BE23
AJ29	VSS	BE30
AJ32	VSS	BE42
AJ43	VSS	BE51
AJ45	VSS	BE8
AJ49	VSS	BF12
AK20	VSS	BF16
AK21	VSS	BF36
AK26	VSS	BG19
AK28	VSS	BG2
AK31	VSS	BG24
AK51	VSS	BG29
AL1	VSS	BG38
AM11	VSS	BG48
AM13	VSS	BG5
AM3	VSS	BG51
AM4	VSS	BH17
AM41	VSS	BH30
AM45	VSS	BH44
AN1	VSS	BH46
AN38	VSS	BH8
AN39	VSS	BJ11
AN43	VSS	BJ13
AN5	VSS	BK38
AN7	VSS	BJ4
AP4	VSS	BJ42
AP48	VSS	BJ46
AP50	VSS	BK15
AR11	VSS	BK17
AR2	VSS	BK25
AR39	VSS	BK29
AR44	VSS	BK36
AR47	VSS	BK40
AR7	VSS	BK44
AT10	VSS	BK6
AT14	VSS	BK8
AT41	VSS	BL11
AT49	VSS	BL13
AU1	VSS	BL19
AU23	VSS	BL22
AU29	VSS	BL37
AU3	VSS	BL47
AU36	VSS	C12
AU49	VSS	C16
AU51	VSS	C19
AV39	VSS	C28
AV48	VSS	C29
AW1	VSS	C33
AW12	VSS	C36
AW16	VSS	C41

CRESTLINE-GP-U

11 M_A_DQ[63.0] <<> M_A_DQ[63.0]

U6SD 4 OF 10

M_A_DQ0	AR43	SA_DQ0
M_A_DQ1	AW44	SA_DQ1
M_A_DQ2	BA45	SA_DQ2
M_A_DQ3	AR41	SA_DQ3
M_A_DQ4	AY46	SA_DQ4
M_A_DQ5	AR45	SA_DQ4
M_A_DQ6	AT42	SA_DQ6
M_A_DQ7	AW47	SA_DQ7
M_A_DQ8	BA45	SA_DQ10
M_A_DQ9	BF48	SA_DQ8
M_A_DQ10	BG47	SA_DQ9
M_A_DQ11	BJ45	SA_DQ11
M_A_DQ12	BB47	SA_DQ12
M_A_DQ13	BG50	SA_DQ14
M_A_DQ14	BH49	SA_DQ13
M_A_DQ15	BE45	SA_DQ14
M_A_DQ16	AW43	SA_DQ16
M_A_DQ17	BE44	SA_DQ17
M_A_DQ18	BG42	SA_DQ18
M_A_DQ19	BE40	SA_DQ19
M_A_DQ20	BF44	SA_DQ19
M_A_DQ21	BH45	SA_DQ21
M_A_DQ22	BG40	SA_DQ22
M_A_DQ23	BE47	SA_DQ22
M_A_DQ24	AR40	SA_DQ23
M_A_DQ25	AW40	SA_DQ25
M_A_DQ26	AT39	SA_DQ26
M_A_DQ27	AW41	SA_DQ27
M_A_DQ28	AW36	SA_DQ27
M_A_DQ29	AY41	SA_DQ28
M_A_DQ30	AV38	SA_DQ30
M_A_DQ31	AT38	SA_DQ31
M_A_DQ32	AV13	SA_DQ32
M_A_DQ33	AT13	SA_DQ32
M_A_DQ34	AW11	SA_DQ34
M_A_DQ35	AV11	SA_DQ35
M_A_DQ36	AU15	SA_DQ36
M_A_DQ37	AT11	SA_DQ36
M_A_DQ38	BA13	SA_DQ37
M_A_DQ39	BA11	SA_DQ38
M_A_DQ40	BE10	SA_DQ40
M_A_DQ41	BD10	SA_DQ41
M_A_DQ42	BD8	SA_DQ42
M_A_DQ43	AY9	SA_DQ43
M_A_DQ44	BG10	SA_DQ44
M_A_DQ45	AW9	SA_DQ45
M_A_DQ46	BD7	SA_DQ46
M_A_DQ47	BB9	SA_DQ47
M_A_DQ48	BB5	SA_DQ48
M_A_DQ49	AY7	SA_DQ49
M_A_DQ50	AT5	SA_DQ50
M_A_DQ51	AT7	SA_DQ51
M_A_DQ52	AY6	SA_DQ52
M_A_DQ53	BB7	SA_DQ52
M_A_DQ54	AR5	SA_DQ54
M_A_DQ55	AR8	SA_DQ55
M_A_DQ56	AR9	SA_DQ56
M_A_DQ57	AN3	SA_DQ56
M_A_DQ58	AM8	SA_DQ57
M_A_DQ59	AN10	SA_DQ59
M_A_DQ60	AT9	SA_DQ60
M_A_DQ61	AN9	SA_DQ61
M_A_DQ62	AM9	SA_DQ62
M_A_DQ63	AN11	SA_DQ63

CRESTLINE-GP-U

DDR SYSTEM MEMORY A

SA_BS0	BB19	M_A_BS#0	<<> M_A_BS#0 11,12
SA_BS1	BK19	M_A_BS#1	<<> M_A_BS#1 11,12
SA_BS2	BF29	M_A_BS#2	<<> M_A_BS#2 11,12
SA_CAS#	BL17	M_A_CAS#	<<> M_A_CAS# 11,12
SA_DM0	AT45	M_A_DM0	
SA_DM1	BD44	M_A_DM1	
SA_DM2	AW38	M_A_DM3	
SA_DM3	AW13	M_A_DM4	
SA_DM5	BG8	M_A_DM5	
SA_DM6	AY5	M_A_DM6	
SA_DM7	AN6	M_A_DM7	
SA_DQ50	AT46	M_A_DQS0	
SA_DQS1	BE48	M_A_DQS1	
SA_DQS2	BB43	M_A_DQS2	
SA_DQS3	BC37	M_A_DQS3	
SA_DQS4	BB16	M_A_DQS4	
SA_DQS5	BH6	M_A_DQS5	
SA_DQS6	BB2	M_A_DQS6	
SA_DQS7	AP3	M_A_DQS7	
SA_DQS#0	AT47	M_A_DQS#0	
SA_DQS#1	BD47	M_A_DQS#1	
SA_DQS#2	BC41	M_A_DQS#2	
SA_DQS#3	BA37	M_A_DQS#3	
SA_DQS#4	BA16	M_A_DQS#4	
SA_DQS#5	BH7	M_A_DQS#5	
SA_DQS#6	BC1	M_A_DQS#6	
SA_DQS#7	AP2	M_A_DQS#7	
SA_MA0	BJ19	M_A_A0	
SA_MA1	BD20	M_A_A1	
SA_MA2	BK27	M_A_A2	
SA_MA3	BH28	M_A_A3	
SA_MA4	BL24	M_A_A4	
SA_MA5	BK28	M_A_A5	
SA_MA6	BJ27	M_A_A6	
SA_MA7	BJ25	M_A_A7	
SA_MA8	BL28	M_A_A8	
SA_MA9	BA28	M_A_A9	
SA_MA10	BC19	M_A_A10	
SA_MA11	BE28	M_A_A11	
SA_MA12	BG30	M_A_A12	
SA_MA13	BL16	M_A_A13	
SA_MA14	BJ29	M_A_A14	
SA_RAS#	BE18	M_A_RAS#	<<> M_A_RAS# 11,12
SA_RCVEN#	AY20	SA_RCVEN#	<<> TP62
SA_WE#	BA19	M_A_WE#	<<> M_A_WE# 11,12

Place Test PAD Near to Chip as could as possible



M_A_DM[7.0] <<> M_A_DM[7.0] 11
M_A_DQS[7.0] <<> M_A_DQS[7.0] 11
M_A_DQS#7.0 <<> M_A_DQS#7.0 11
M_A_A[14.0] <<> M_A_A[14.0] 11,12

M_B_DQ0	AP49	SB_DQ0
M_B_DQ1	AR51	SB_DQ1
M_B_DQ2	AW50	SB_DQ2
M_B_DQ3	AN51	SB_DQ3
M_B_DQ4	AW51	SB_DQ4
M_B_DQ5	AN50	SB_DQ4
M_B_DQ6	AV50	SB_DQ6
M_B_DQ7	AY49	SB_DQ7
M_B_DQ8	BA50	SB_DQ8
M_B_DQ9	BB50	SB_DQ8
M_B_DQ10	BA49	SB_DQ9
M_B_DQ11	BE50	SB_DQ11
M_B_DQ12	BA51	SB_DQ12
M_B_DQ13	AY49	SB_DQ12
M_B_DQ14	BF50	SB_DQ13
M_B_DQ15	BF49	SB_DQ14
M_B_DQ16	BJ50	SB_DQ16
M_B_DQ17	BJ44	SB_DQ17
M_B_DQ18	BJ43	SB_DQ18
M_B_DQ19	BL43	SB_DQ19
M_B_DQ20	BK47	SB_DQ20
M_B_DQ21	BK49	SB_DQ21
M_B_DQ22	BK42	SB_DQ22
M_B_DQ23	BK43	SB_DQ22
M_B_DQ24	BJ41	SB_DQ23
M_B_DQ25	BL41	SB_DQ25
M_B_DQ26	BJ37	SB_DQ26
M_B_DQ27	BJ36	SB_DQ27
M_B_DQ28	BK41	SB_DQ28
M_B_DQ29	BJ40	SB_DQ28
M_B_DQ30	BL35	SB_DQ30
M_B_DQ31	BK37	SB_DQ31
M_B_DQ32	BK13	SB_DQ32
M_B_DQ33	BE11	SB_DQ32
M_B_DQ34	BK11	SB_DQ34
M_B_DQ35	BC11	SB_DQ35
M_B_DQ36	BC13	SB_DQ36
M_B_DQ37	BE12	SB_DQ37
M_B_DQ38	BC12	SB_DQ38
M_B_DQ39	BG12	SB_DQ39
M_B_DQ40	BJ10	SB_DQ40
M_B_DQ41	BL9	SB_DQ41
M_B_DQ42	BK5	SB_DQ42
M_B_DQ43	BL5	SB_DQ43
M_B_DQ44	BK9	SB_DQ44
M_B_DQ45	BK10	SB_DQ45
M_B_DQ46	BJ8	SB_DQ46
M_B_DQ47	BJ6	SB_DQ47
M_B_DQ48	BE4	SB_DQ48
M_B_DQ49	BH5	SB_DQ49
M_B_DQ50	BG1	SB_DQ50
M_B_DQ51	BC2	SB_DQ51
M_B_DQ52	BK3	SB_DQ52
M_B_DQ53	BE4	SB_DQ52
M_B_DQ54	BD3	SB_DQ54
M_B_DQ55	BJ2	SB_DQ55
M_B_DQ56	BA3	SB_DQ56
M_B_DQ57	BB3	SB_DQ57
M_B_DQ58	AR1	SB_DQ58
M_B_DQ59	AT3	SB_DQ59
M_B_DQ60	AY2	SB_DQ60
M_B_DQ61	AY3	SB_DQ61
M_B_DQ62	AU2	SB_DQ62
M_B_DQ63	AT2	SB_DQ63

CRESTLINE-GP-U

DDR SYSTEM MEMORY B

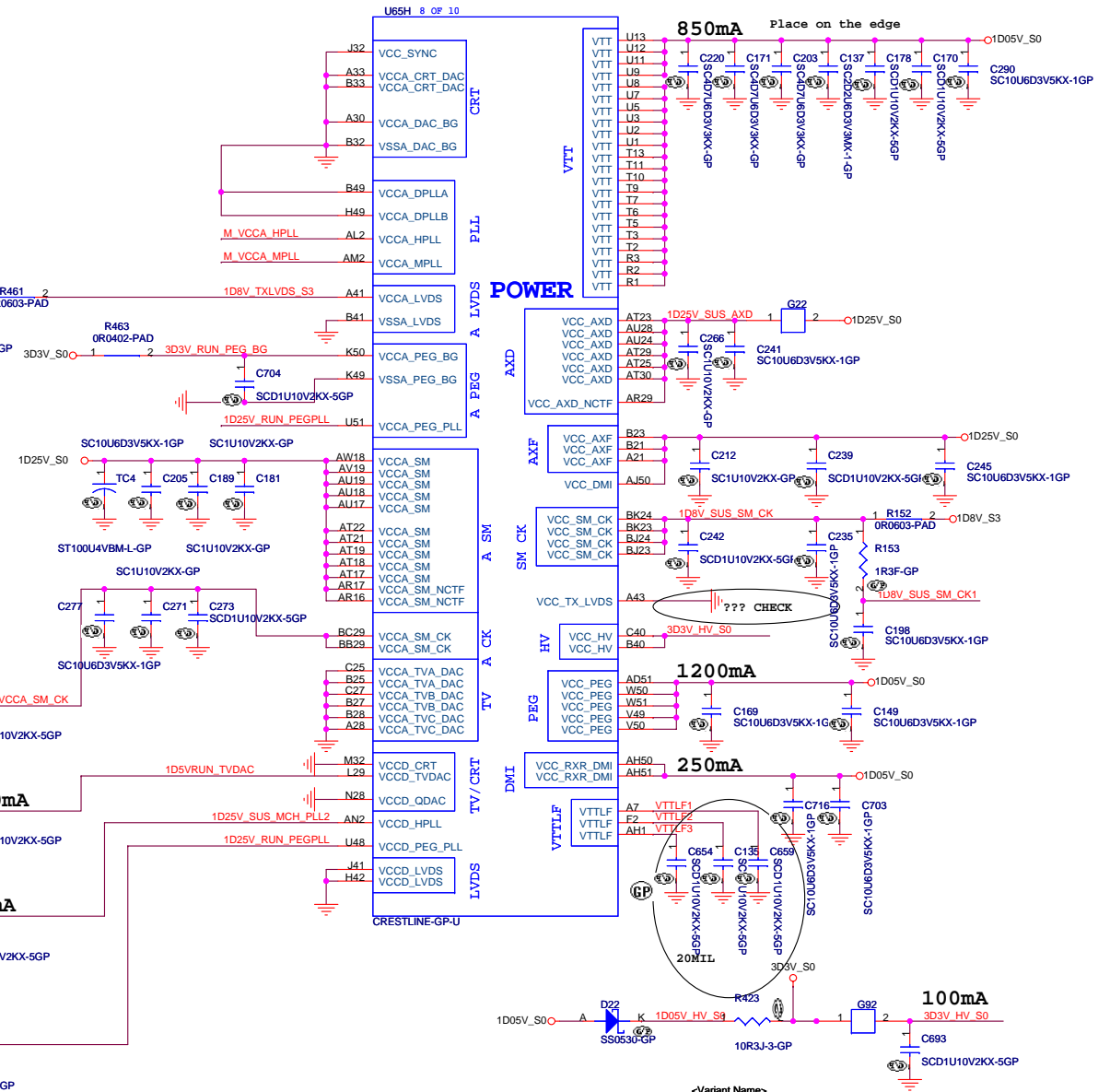
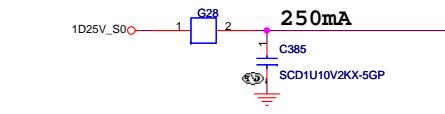
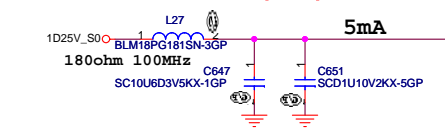
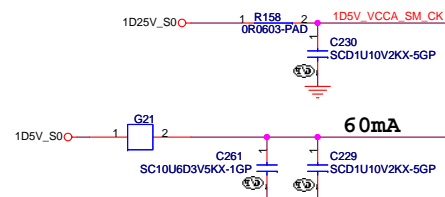
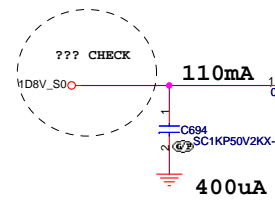
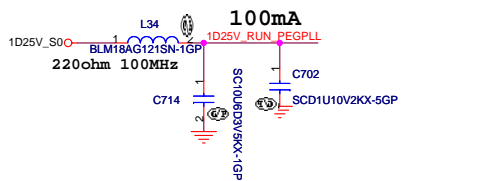
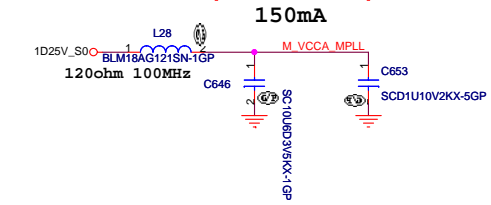
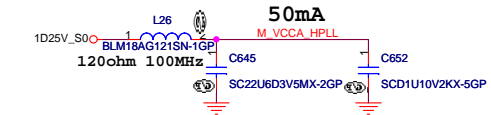
SB_BS0	AY17	M_B_BS#0	<<> M_B_BS#0 11,12
SB_BS1	BG18	M_B_BS#1	<<> M_B_BS#1 11,12
SB_BS2	BG36	M_B_BS#2	<<> M_B_BS#2 11,12
SB_CAS#	BE17	M_B_CAS#	<<> M_B_CAS# 11,12
SB_DM0	AR50	M_B_DM0	
SB_DM1	BD49	M_B_DM1	
SB_DM2	BK45	M_B_DM2	
SB_DM3	BL38	M_B_DM3	
SB_DM4	BH12	M_B_DM4	
SB_DM5	BJ7	M_B_DM5	
SB_DM6	BF3	M_B_DM6	
SB_DM7	AW2	M_B_DM7	
SB_DQ50	AT50	M_B_DQS0	
SB_DQ51	BD50	M_B_DQS1	
SB_DQ52	BK46	M_B_DQS2	
SB_DQ53	BK39	M_B_DQS3	
SB_DQ54	BJ12	M_B_DQS4	
SB_DQ55	BL7	M_B_DQS5	
SB_DQ56	BE2	M_B_DQS6	
SB_DQ57	AV2	M_B_DQS7	
SB_DQS#0	BC50	M_B_DQS#0	
SB_DQS#1	BL45	M_B_DQS#1	
SB_DQS#2	BK38	M_B_DQS#2	
SB_DQS#3	CBK12	M_B_DQS#3	
SB_DQS#4	CBK7	M_B_DQS#4	
SB_DQS#5	BE2	M_B_DQS#5	
SB_DQS#6	AV3	M_B_DQS#6	
SB_DQS#7			
SB_MA0	BC18	M_B_A0	
SB_MA1	BG28	M_B_A1	
SB_MA2	BG25	M_B_A2	
SB_MA3	AW17	M_B_A3	
SB_MA4	BF25	M_B_A4	
SB_MA5	BE25	M_B_A5	
SB_MA6	BA29	M_B_A6	
SB_MA7	BC28	M_B_A7	
SB_MA8	AY28	M_B_A8	
SB_MA9	BD37	M_B_A9	
SB_MA10	BG17	M_B_A10	
SB_MA11	BE37	M_B_A11	
SB_MA12	BA39	M_B_A12	
SB_MA13	BG13	M_B_A13	
SB_MA14	BE24	M_B_A14	
SB_RAS#	AV16	M_B_RAS#	<<> M_B_RAS# 11,12
SB_RCVEN#	AY18	SB_RCVEN#	<<> TP54
SB_WE#	BC17	M_B_WE#	<<> M_B_WE# 11,12

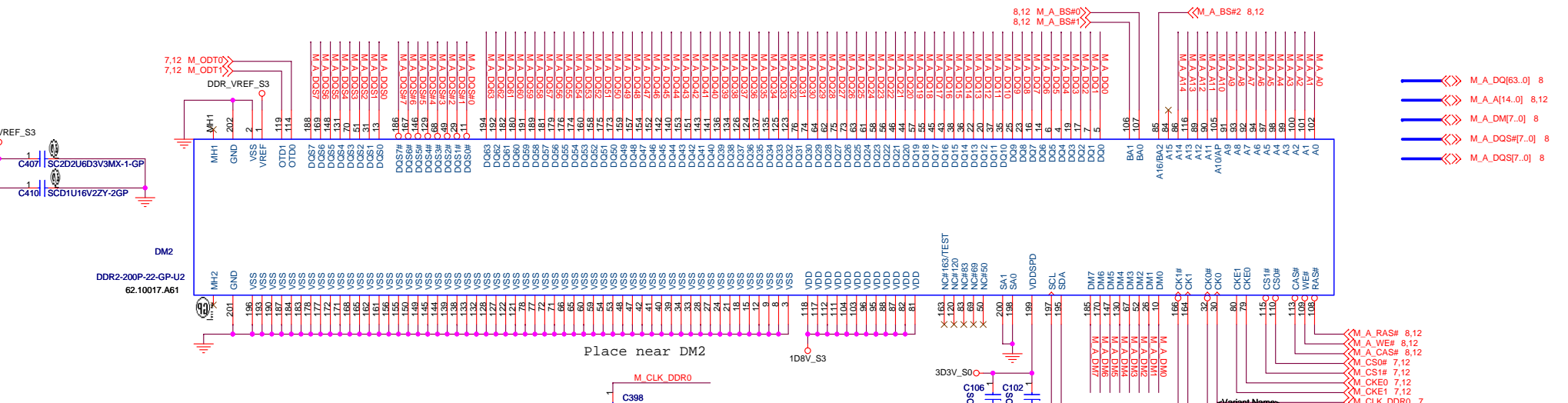
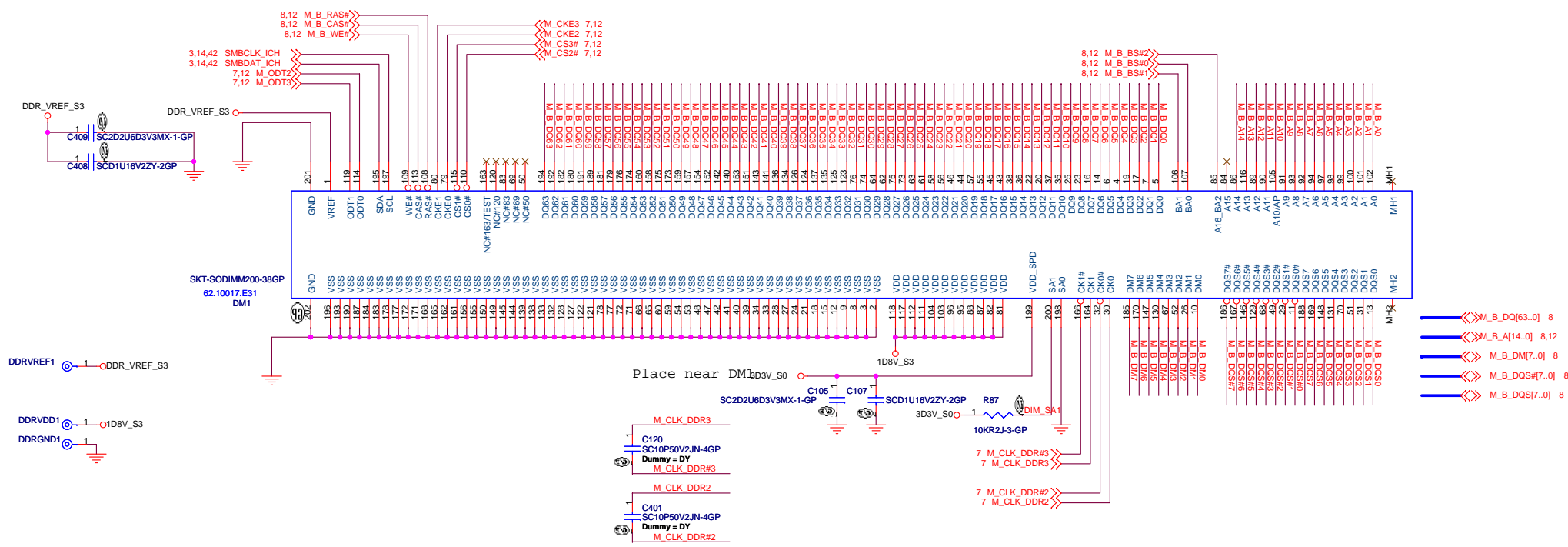
Place Test PAD Near to Chip as could as possible



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
GMCH (3 of 5) MEMORY			
Title	Document Number	Rev	SA
Size Custom	MAKI		
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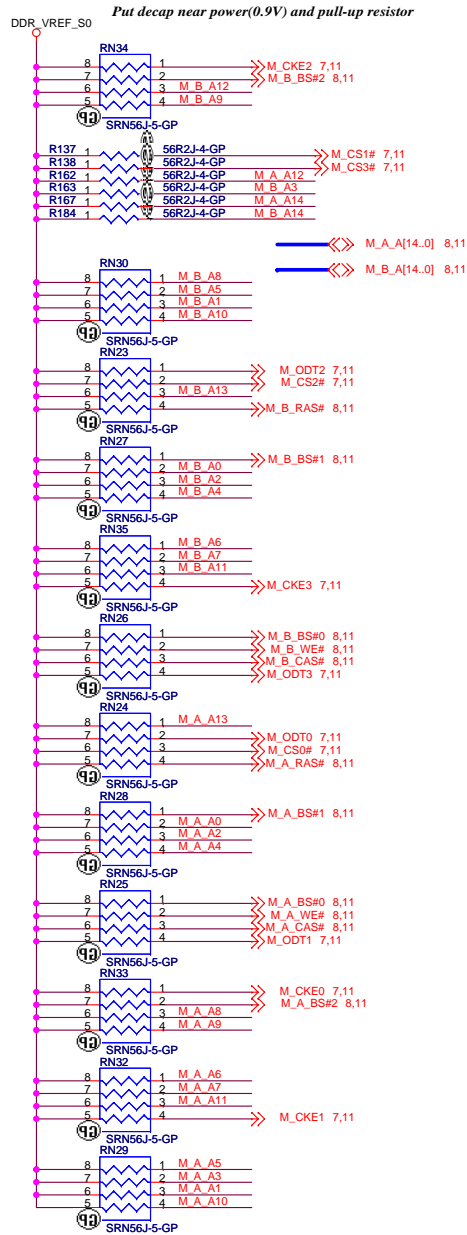


緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien Z21, Taiwan, R.O.C.

DDR2-SOCKET

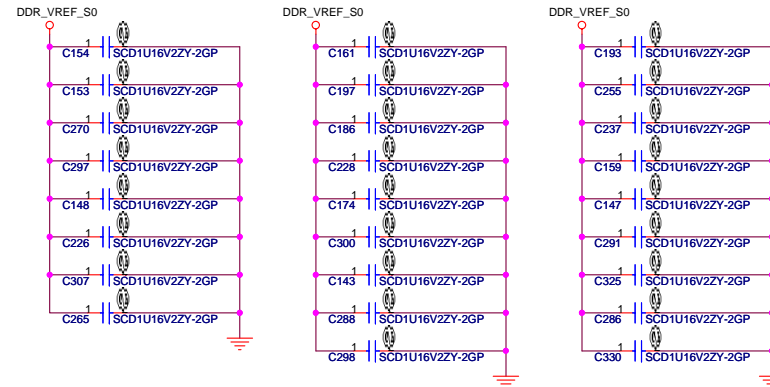
Title		Rev
Size	Document Number	SA
Customer	MAKI	
Date: Friday, January 18, 2008	Sheet 11 of 51	

PARALLEL TERMINATION



Decoupling Capacitor

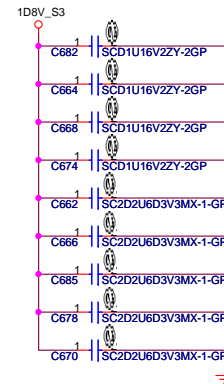
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1

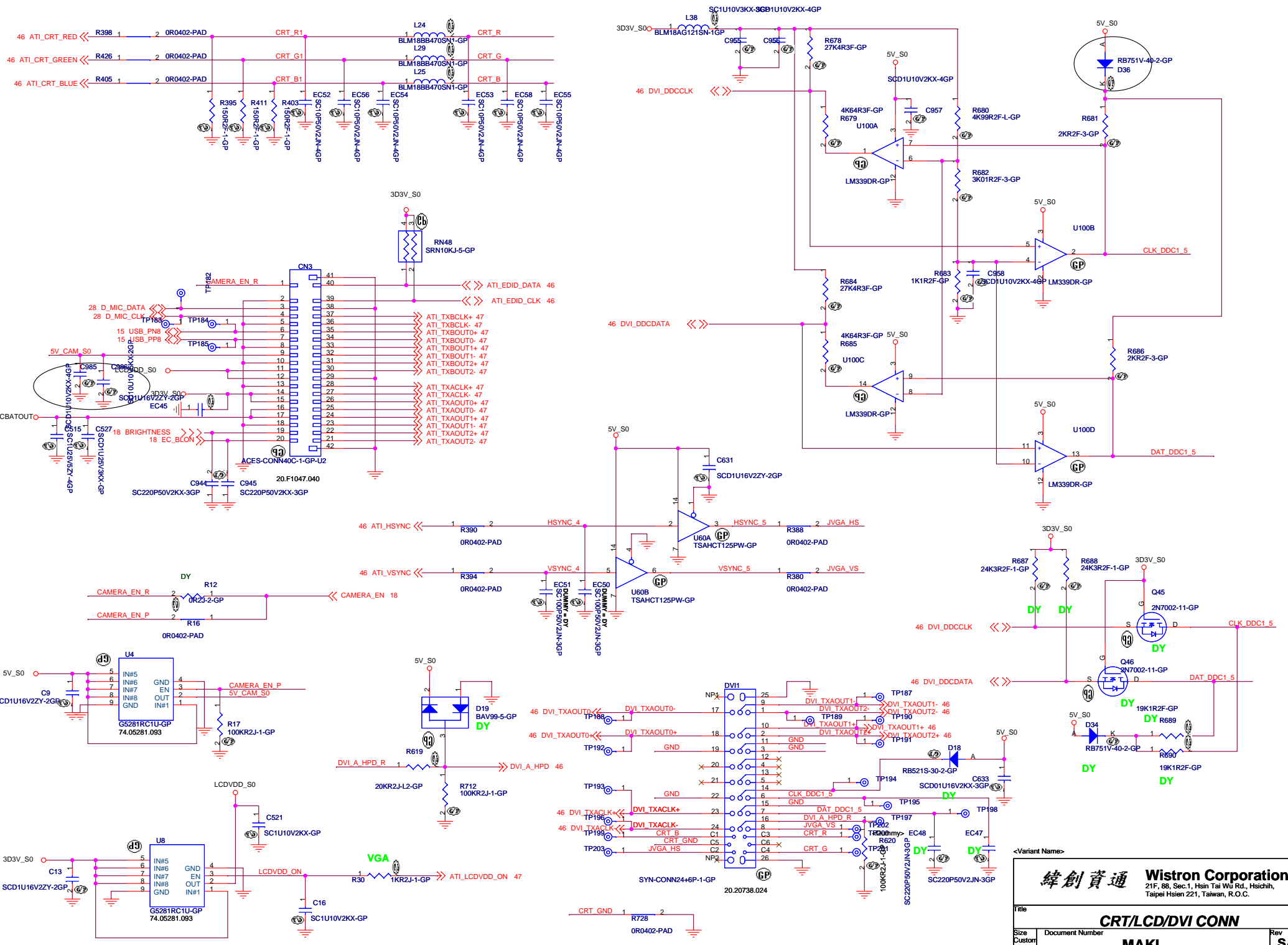


Place these Caps near DM2



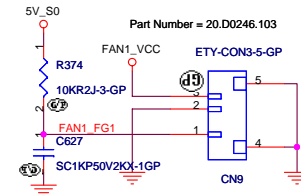
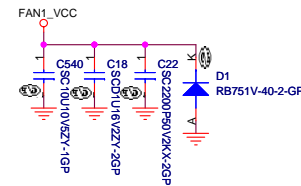
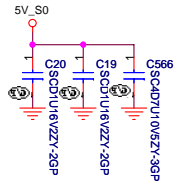
<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.	
DDR2-RESISTOR&CAPACITOR	
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<Variant Name>

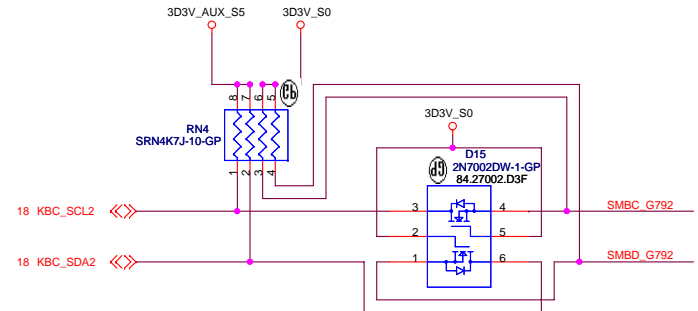
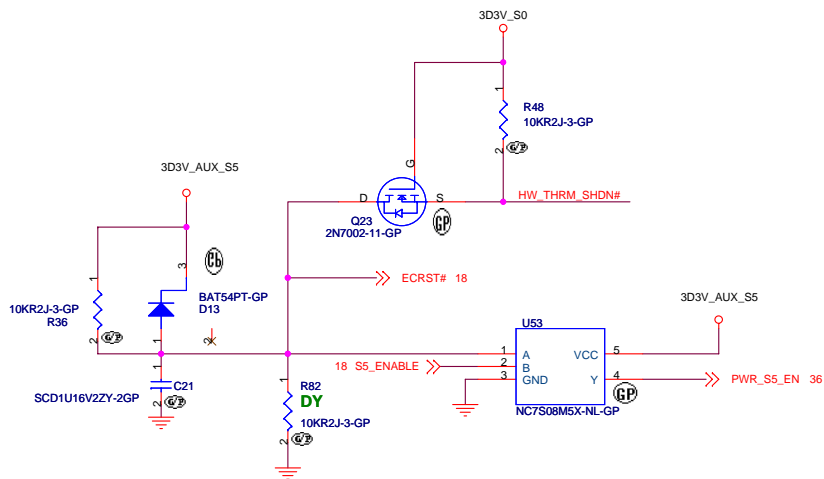
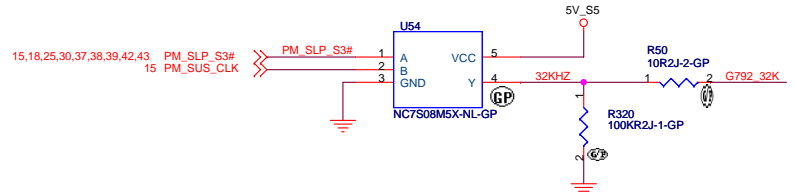
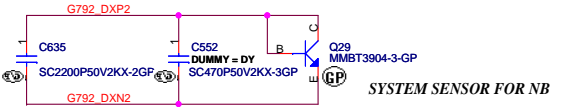
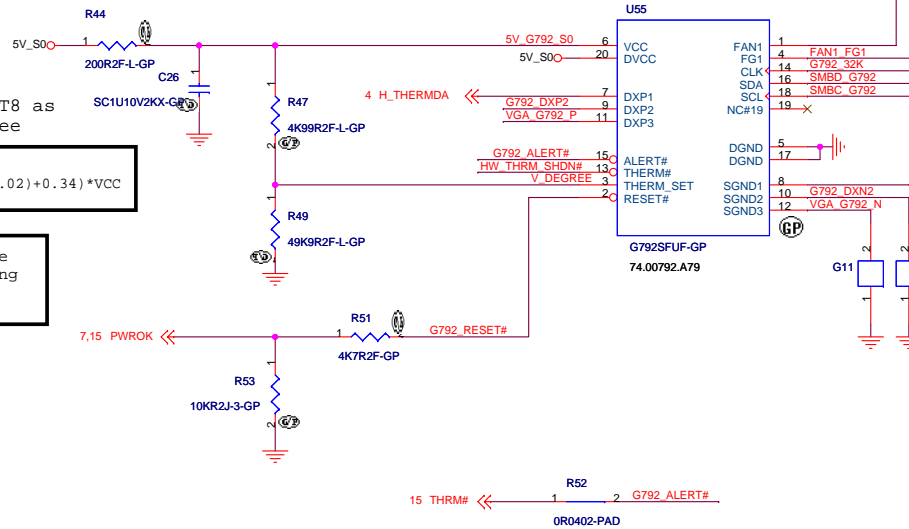
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
CRT/LCD/DVI CONN			
Title	Document Number	MAKI	Rev SA
Size	Custom		
Date: Friday, January 18, 2008	Sheet 13	of	51



Setting T8 as 100 Degree

$$V_DEGREE = ((Degree - 72) * 0.02) + 0.34 * VCC$$

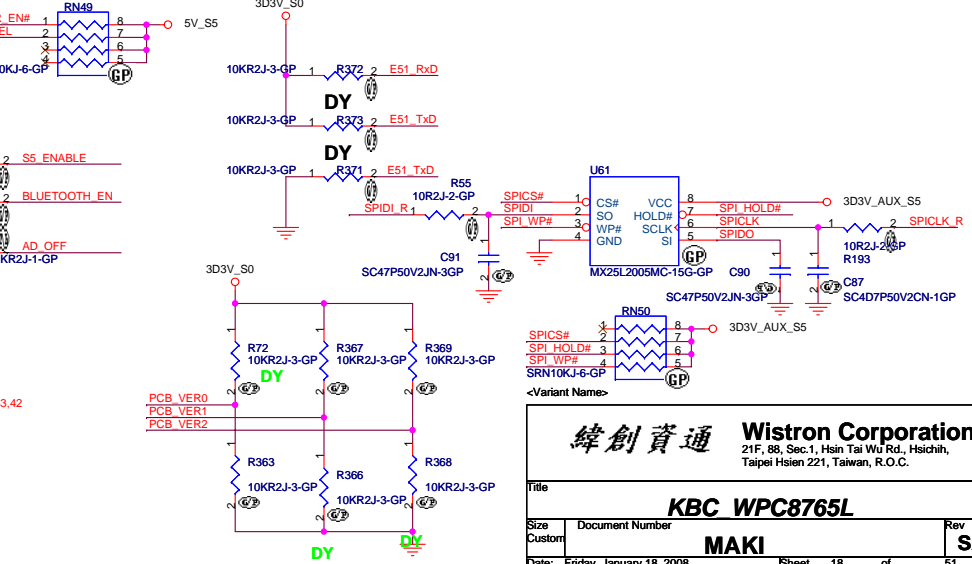
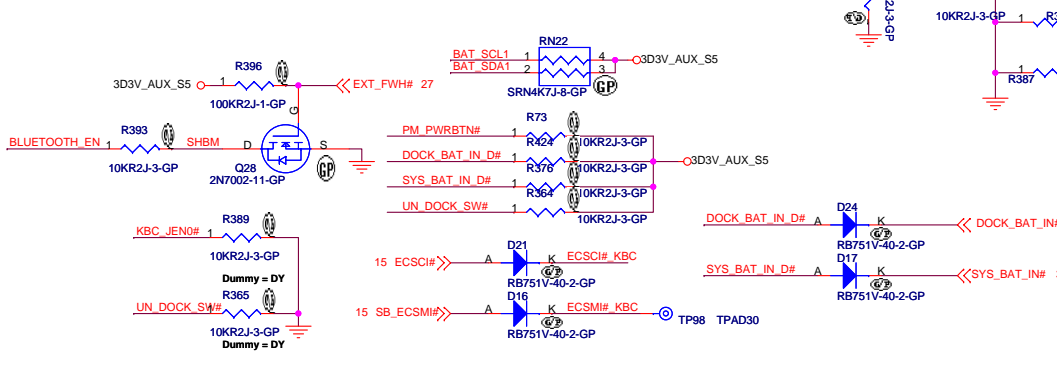
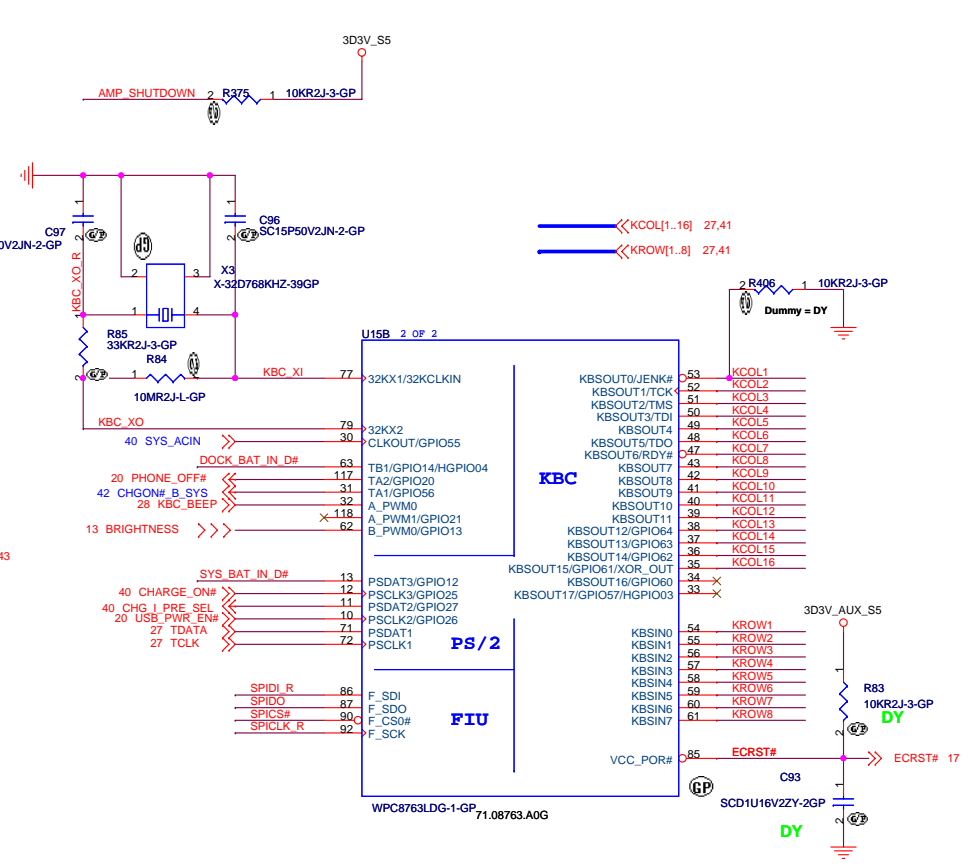
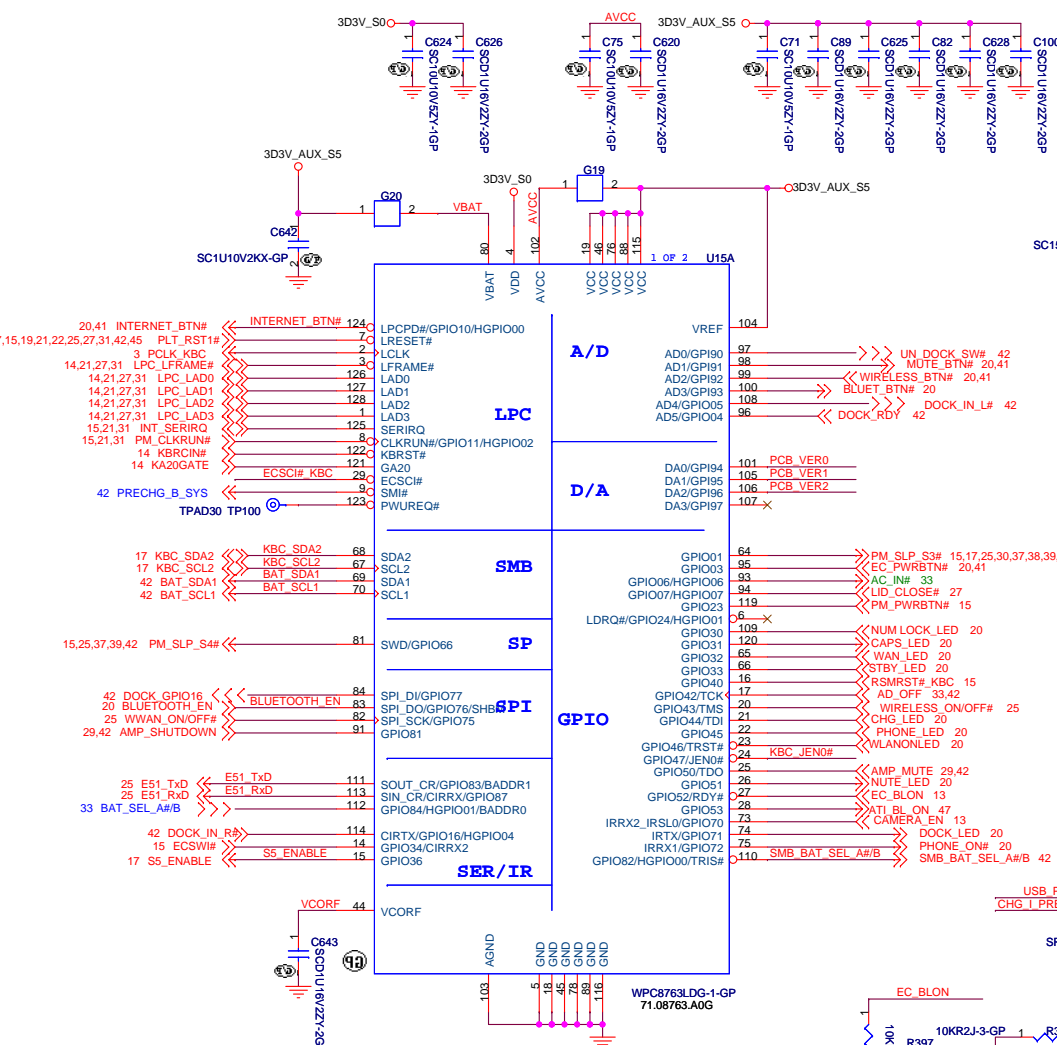
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.

THERMAL G792

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Size: A3 Document Number: _____ Rev: SA
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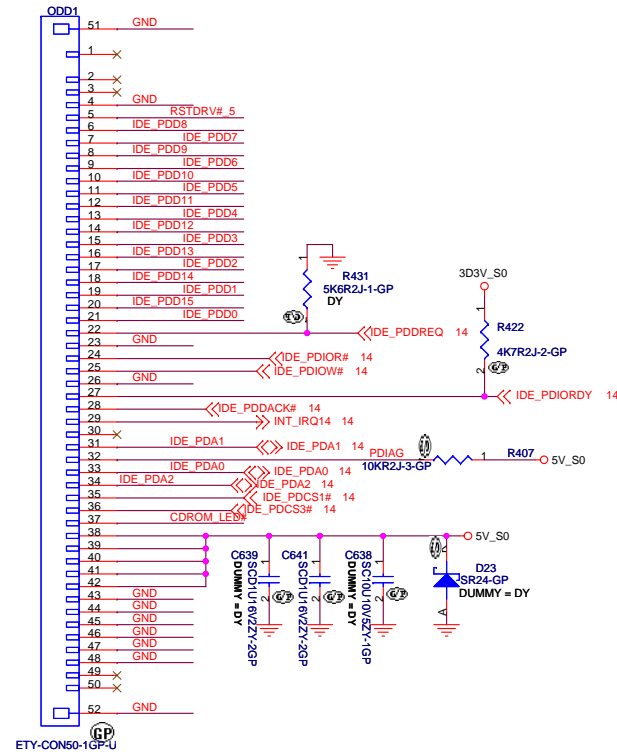
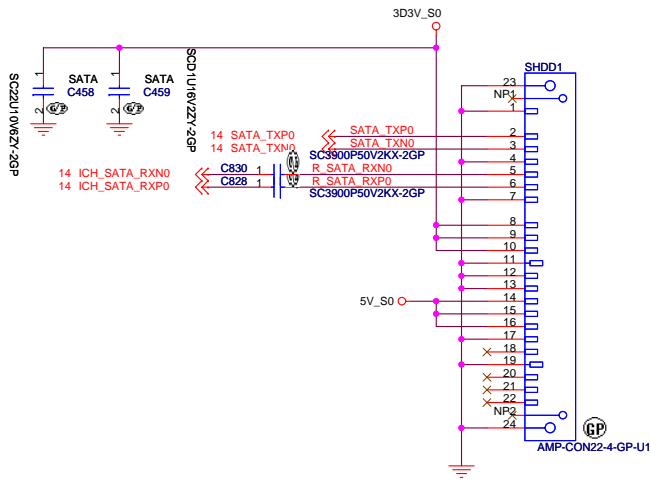


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC WPC8765L**

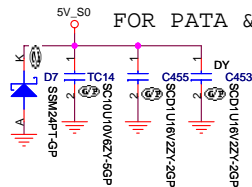
Size	Document Number	Rev
Custom	MAKI	SA
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SATA HD Connector

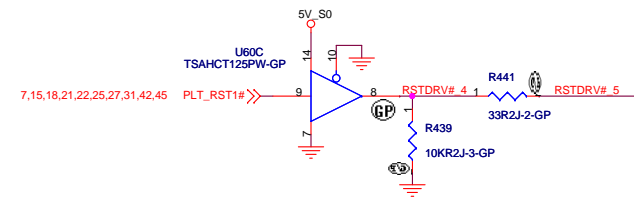


20.K0214.050

FOR PATA & SATA 5V_S0 POWER



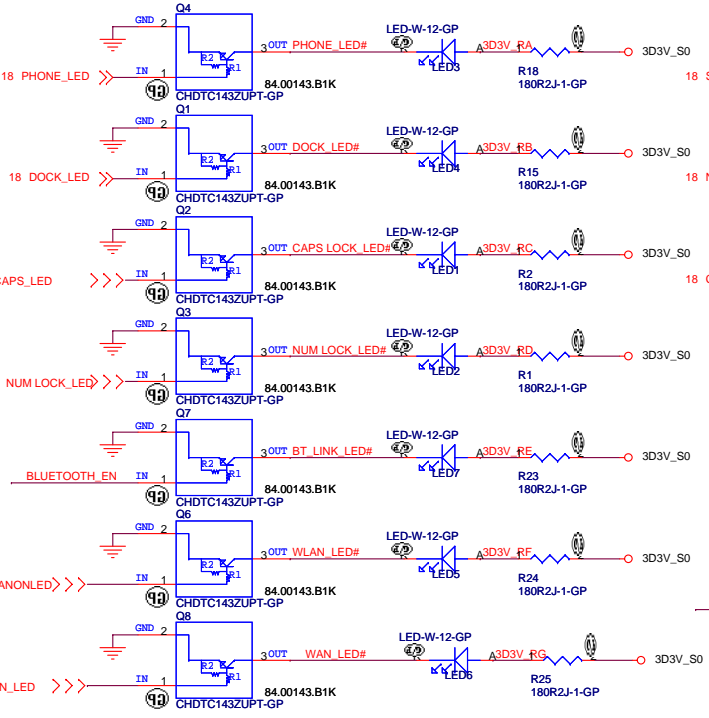
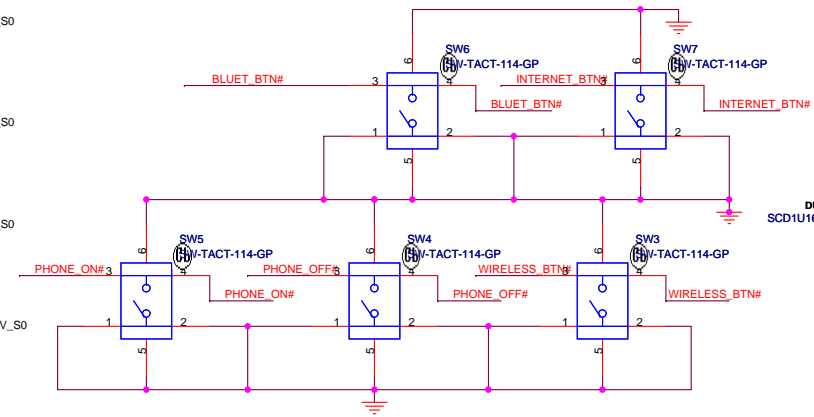
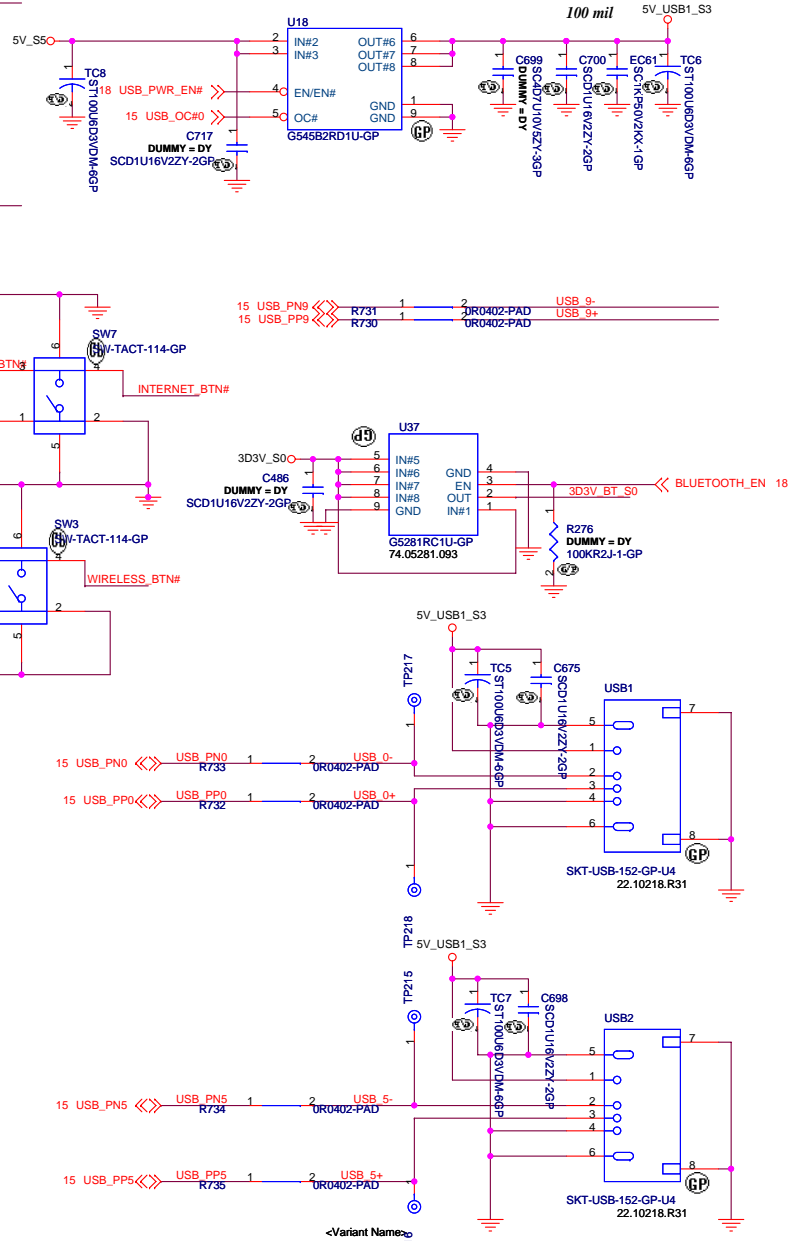
PCIRST# 3V to 5V level shift for HDD & CDROM



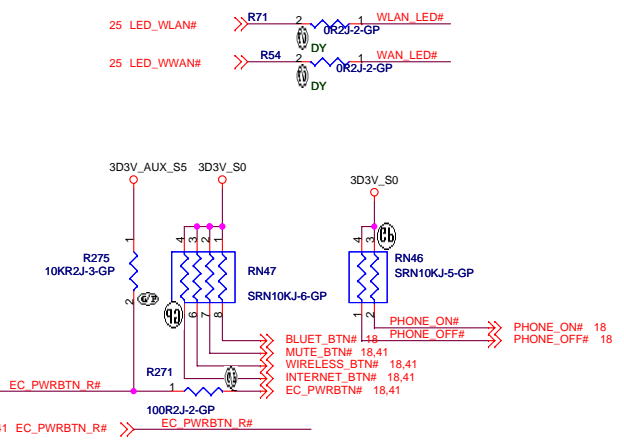
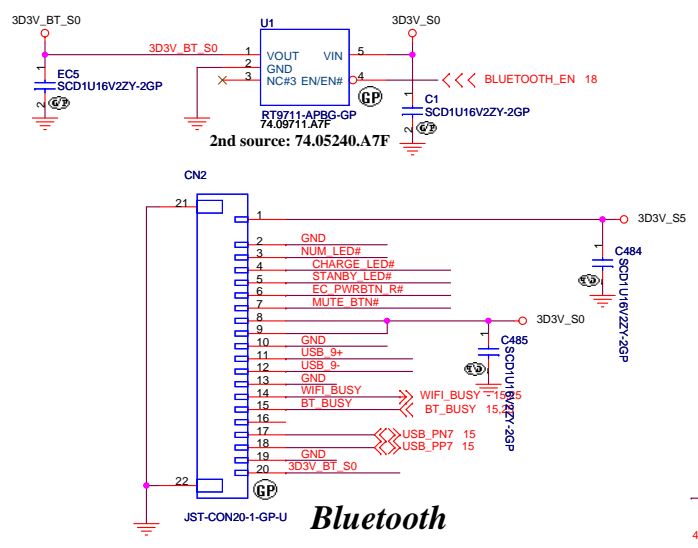
<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/CDROM			
Size	Document Number	Rev	
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USB PORT



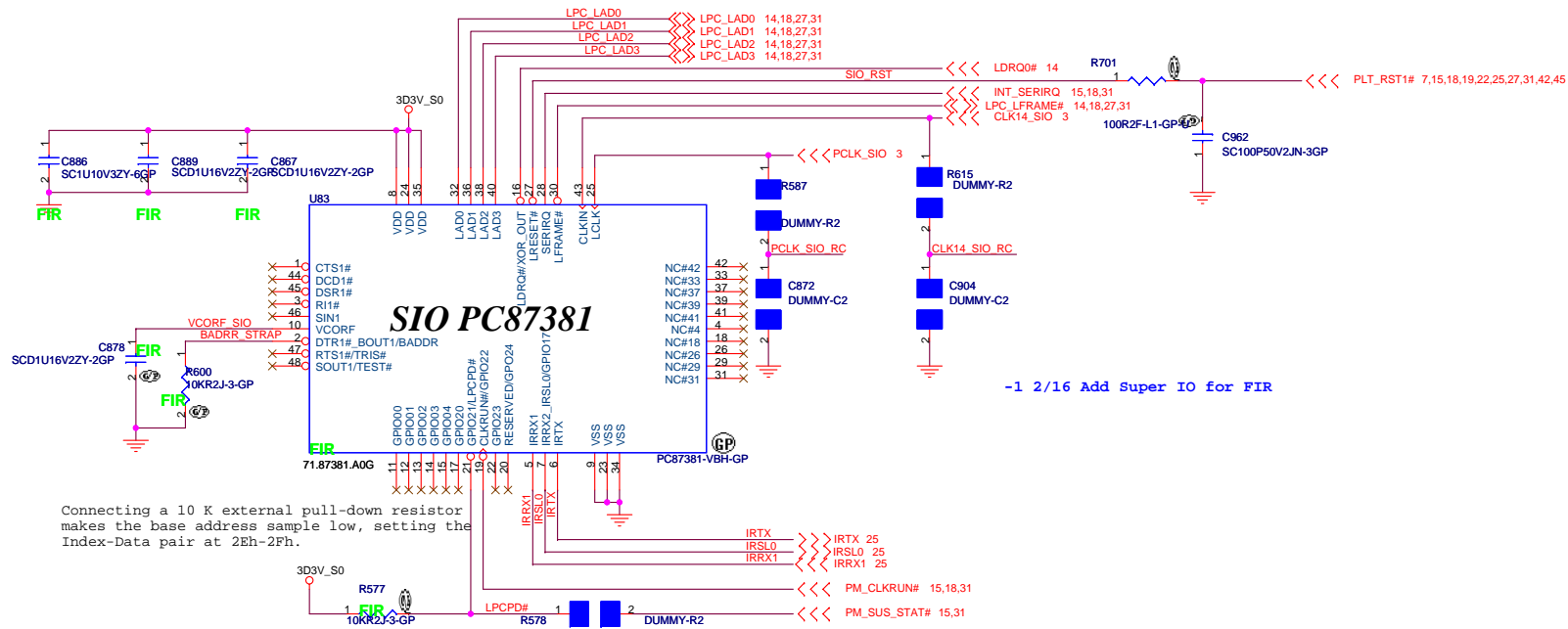
LAUNCH BOARD CONN



緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB IF&BT&DB**

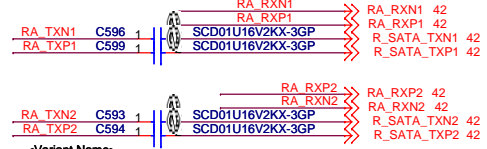
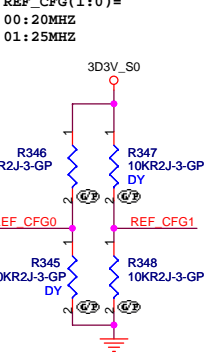
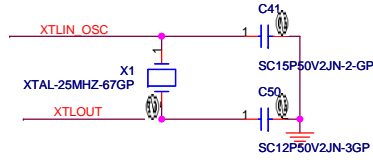
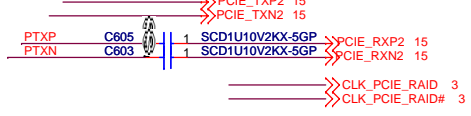
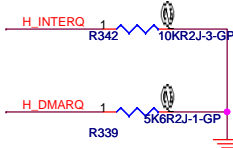
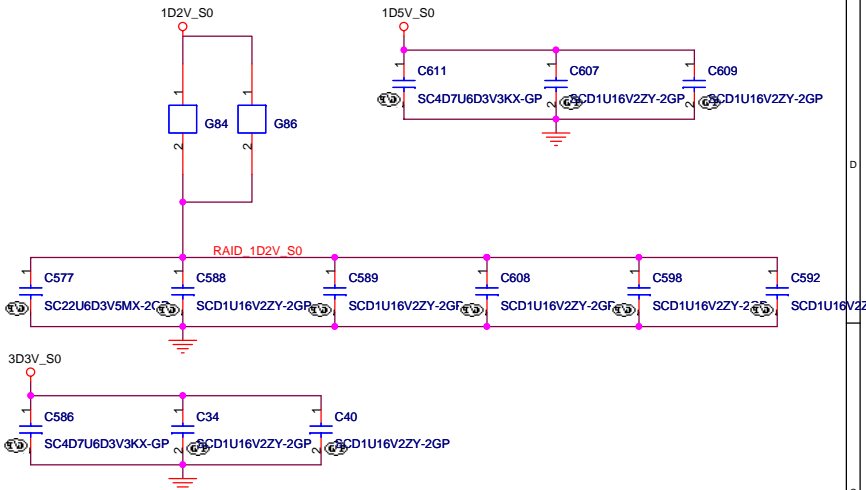
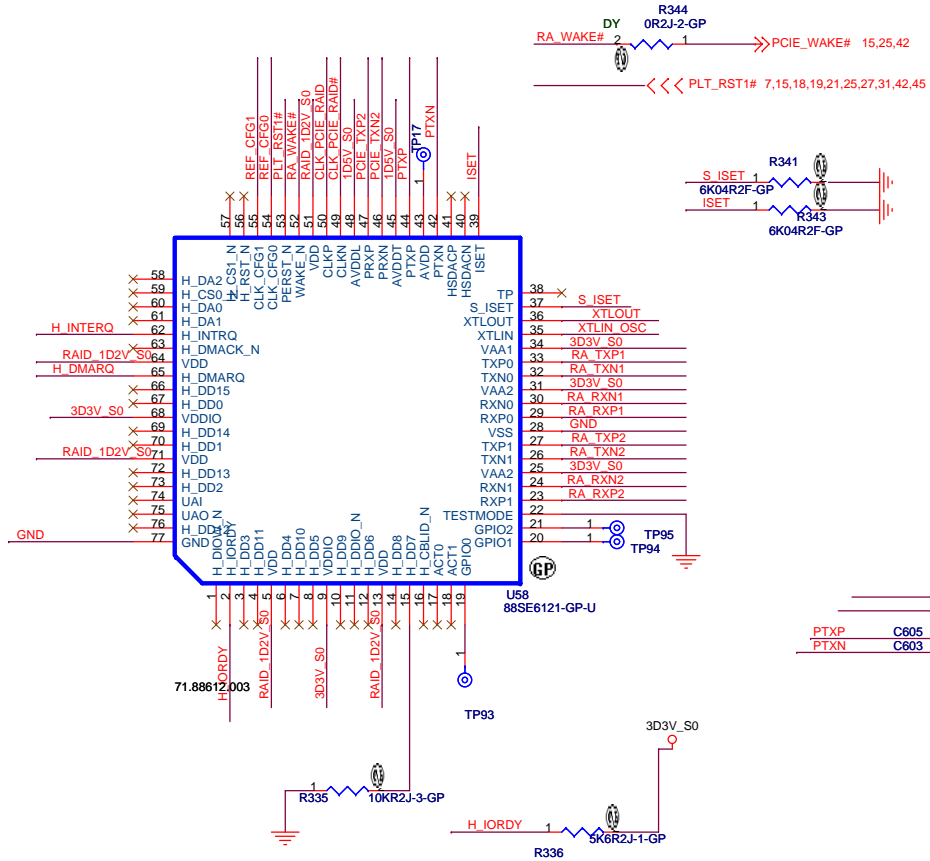
Size	Document Number	Rev
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Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

<Variant Name>

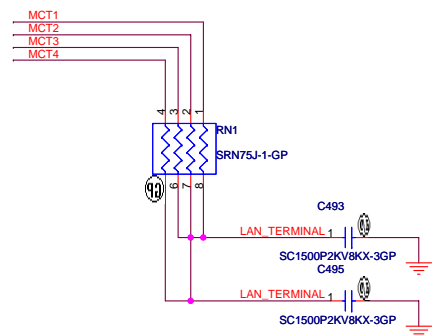
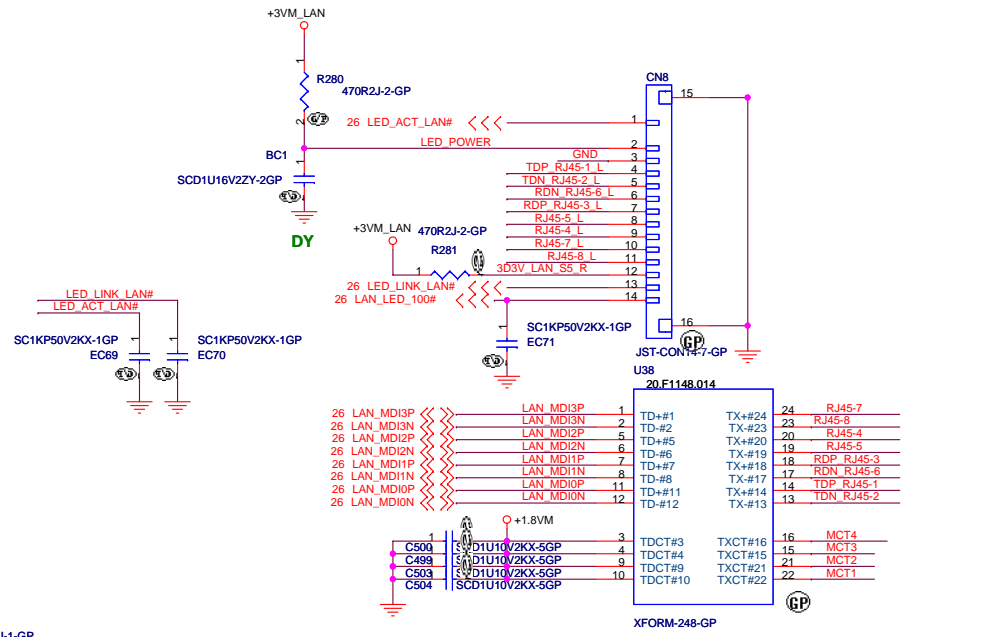
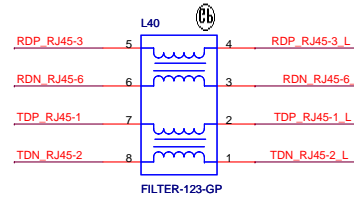
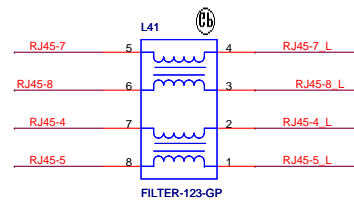
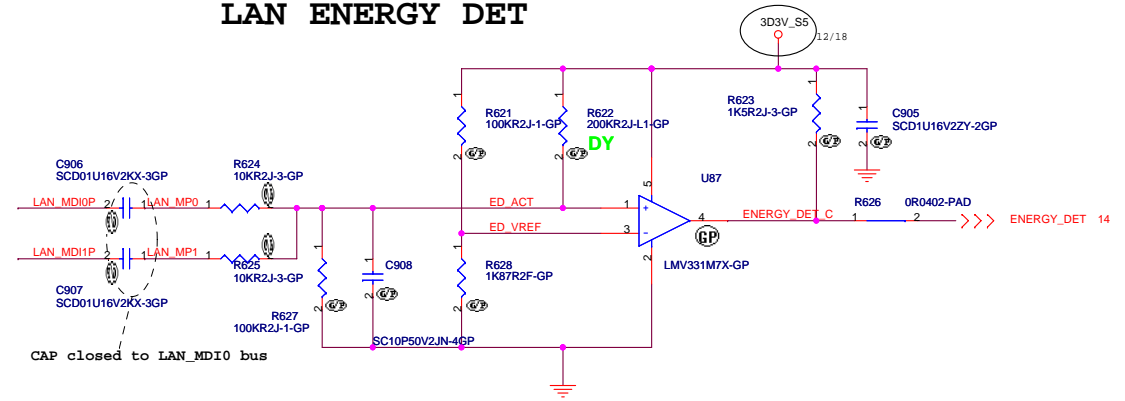
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
USB HUB 2504-JT		
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REF_CFG(1:0) =
00: 20MHZ
01: 25MHZ

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
RAID & SATA HDD	
Title Size B	Document Number MAKI
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LAN ENERGY DET



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8111B**

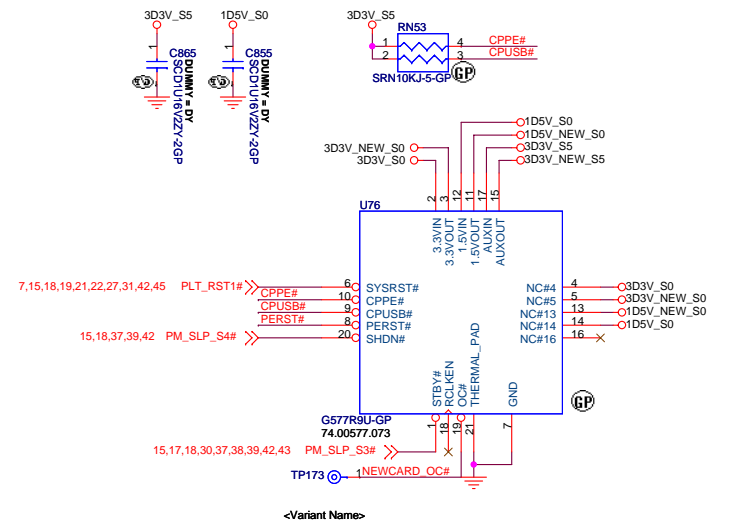
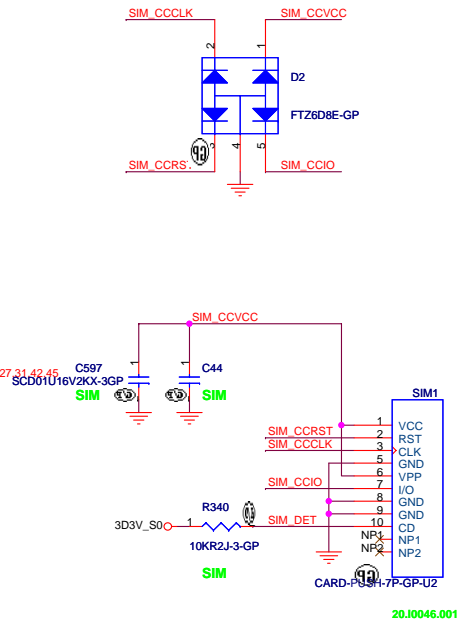
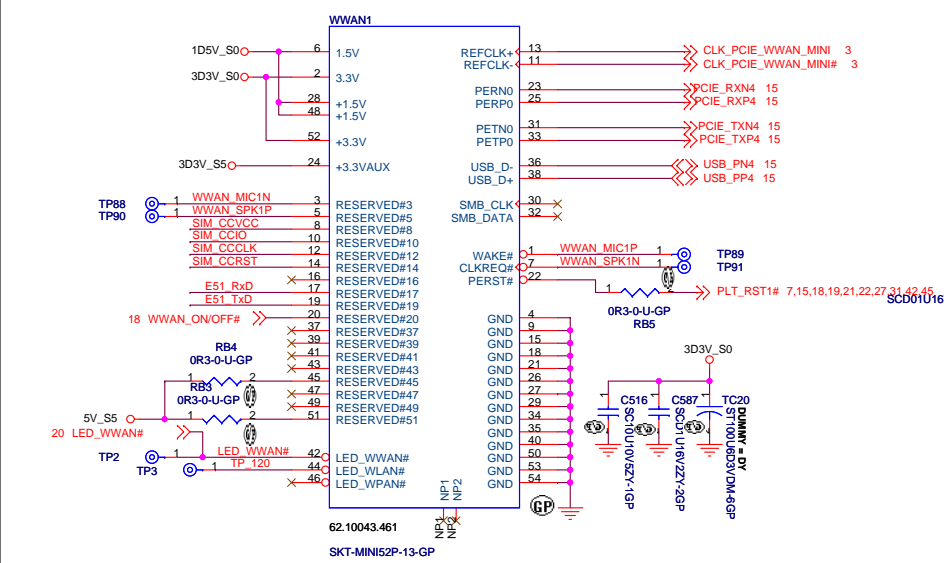
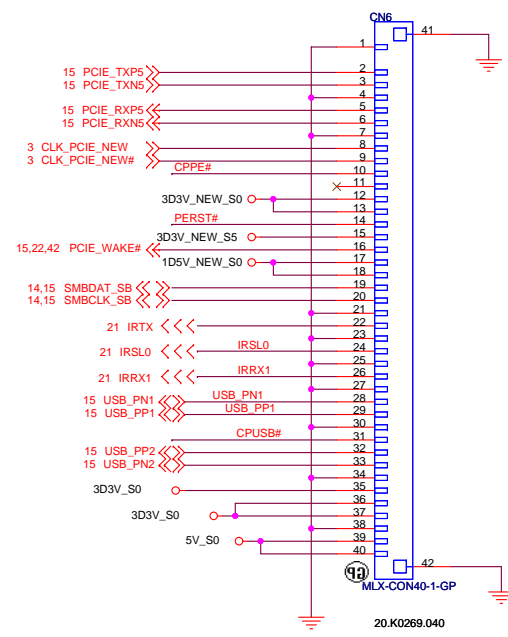
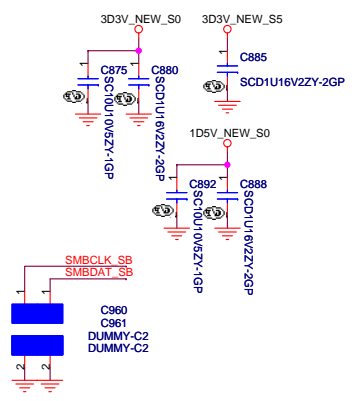
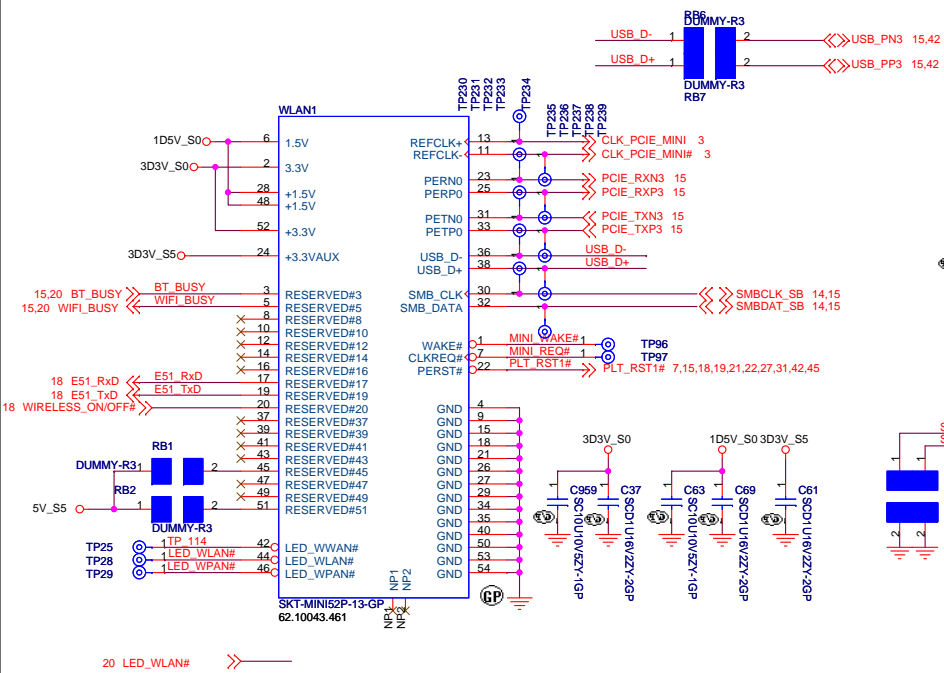
Size: A3 Document Number: **MAKI** Rev: SA

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A	B	C	D	E

<Variant Name>

<p>緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small></p>		
<p>Title LAN S/W & RJ45</p>		
Size	Document Number	Rev
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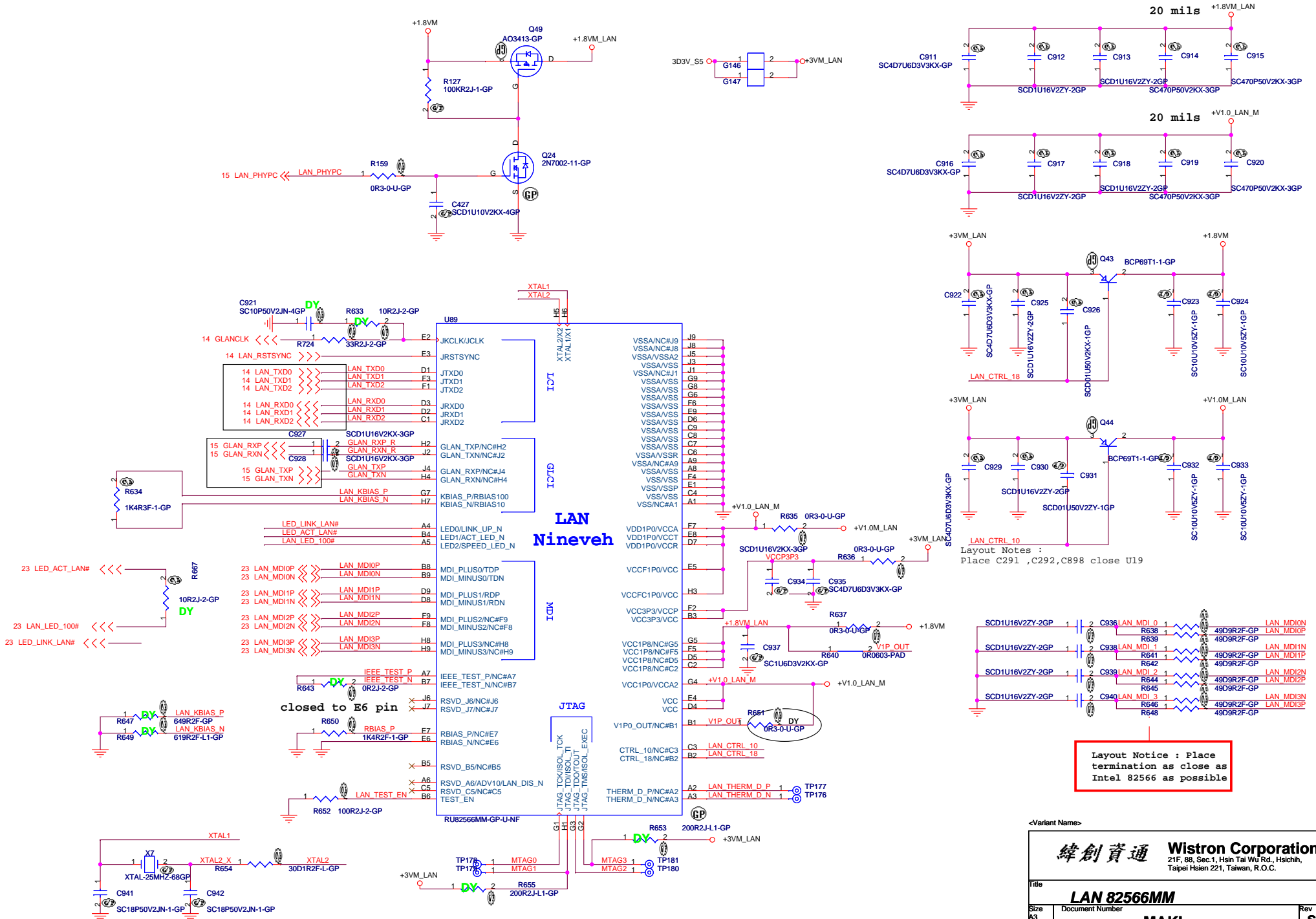


緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card/New Card**

Size: Custom Document Number: **MAKI** Rev: **SA**

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Layout Notice : Place termination as close as Intel 82566 as possible

<Variant Name>

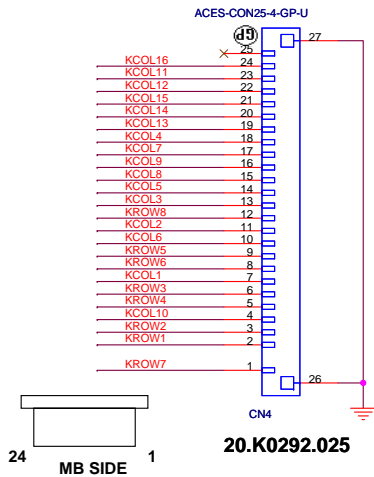
緯創資通 Wistron Corporation
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN 82566MM**

Size A3	Document Number	Rev SA
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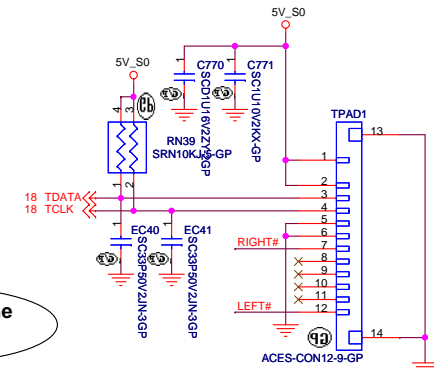
Internal KeyBoard Connector

KB1 : 15"



MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

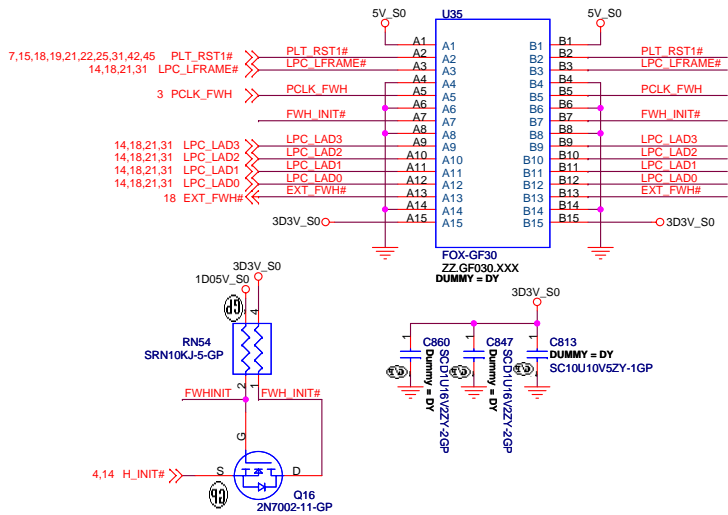
TouchPad Connector



check pin define

15" TOUCHPAD BUTTON SWITCH

GOLDEN FINGER FOR DEBUG BOARD

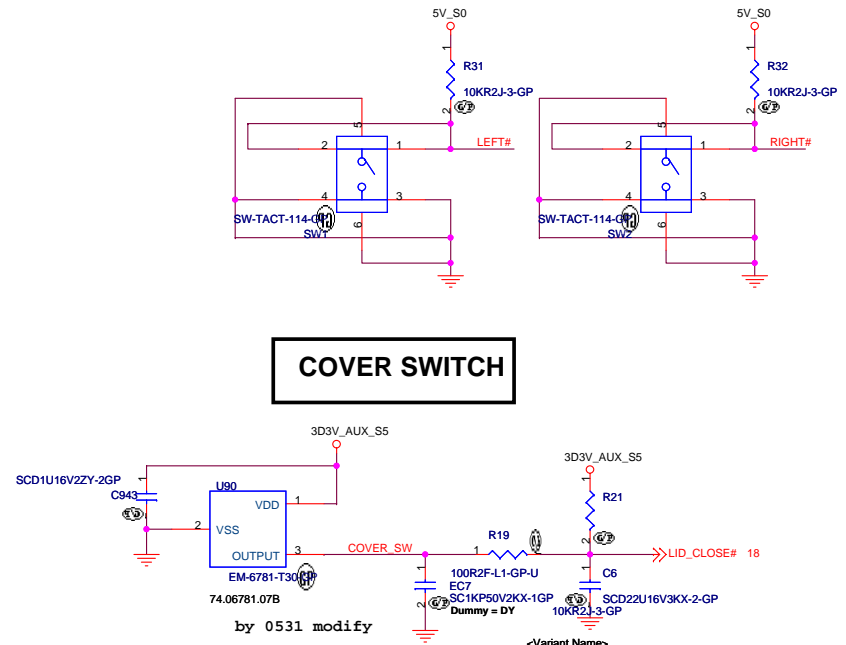


TOP VIEW

- A15 (B1)
- A14 (B2)
- ...
- A2 (B14)
- A1 (B15)

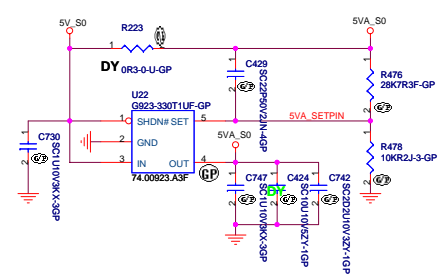
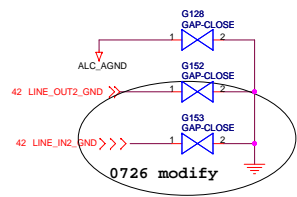
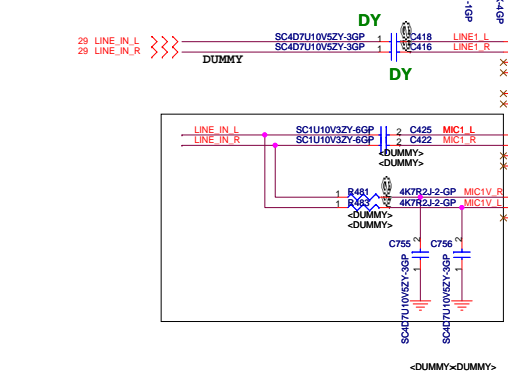
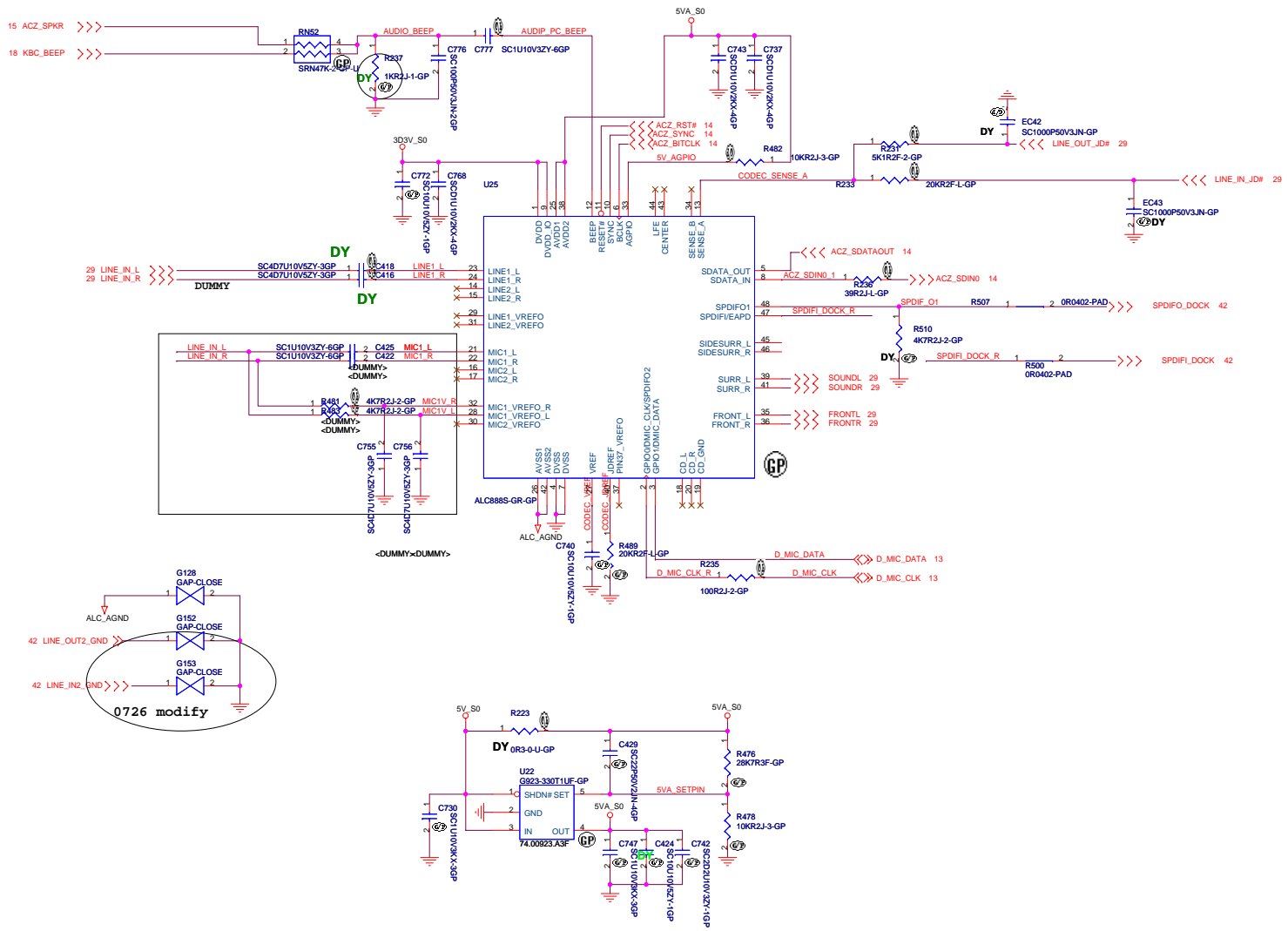
(BOTTOM VIEW)

COVER SWITCH



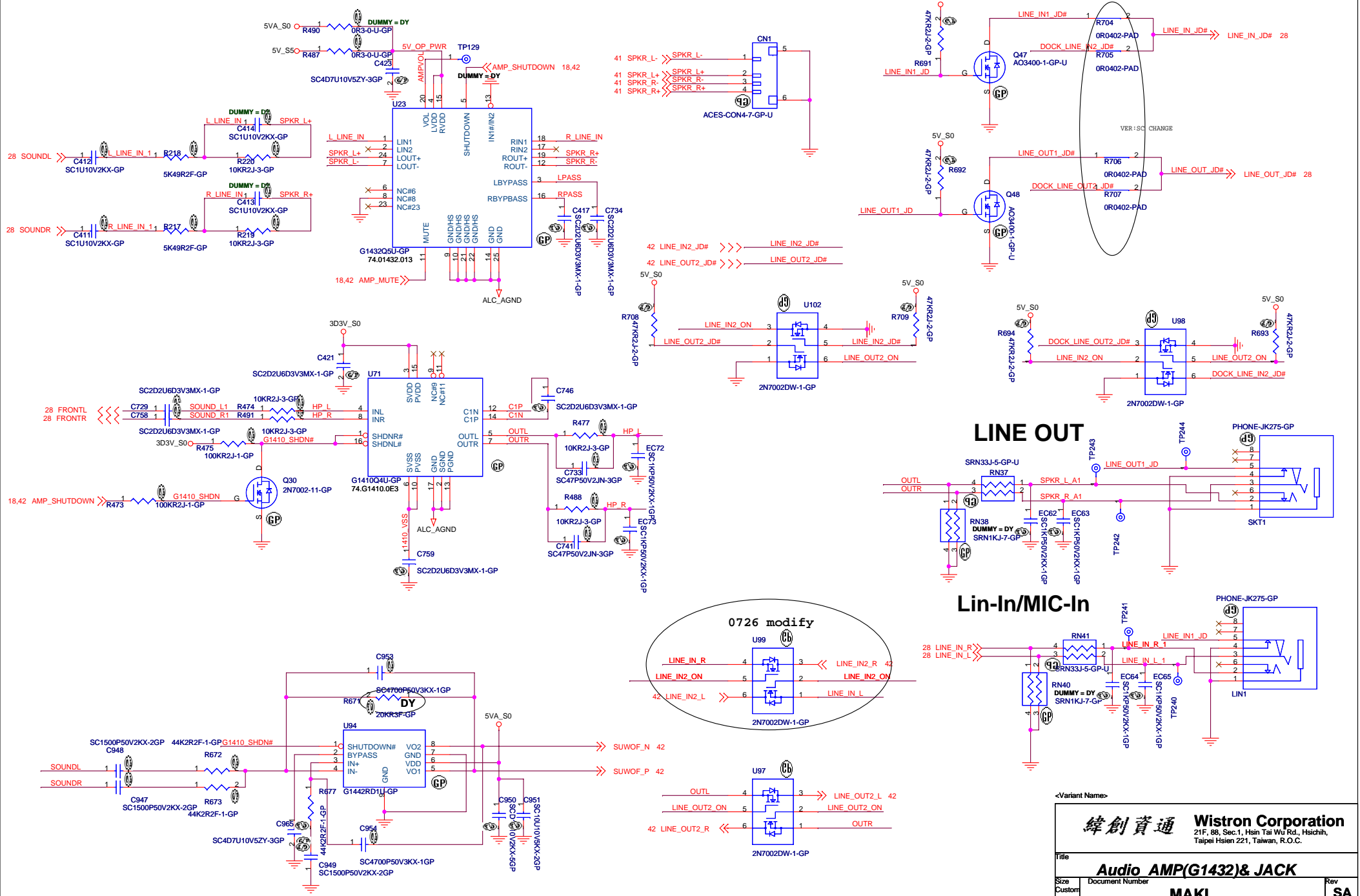
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien Z21, Taiwan, R.O.C.

Title		
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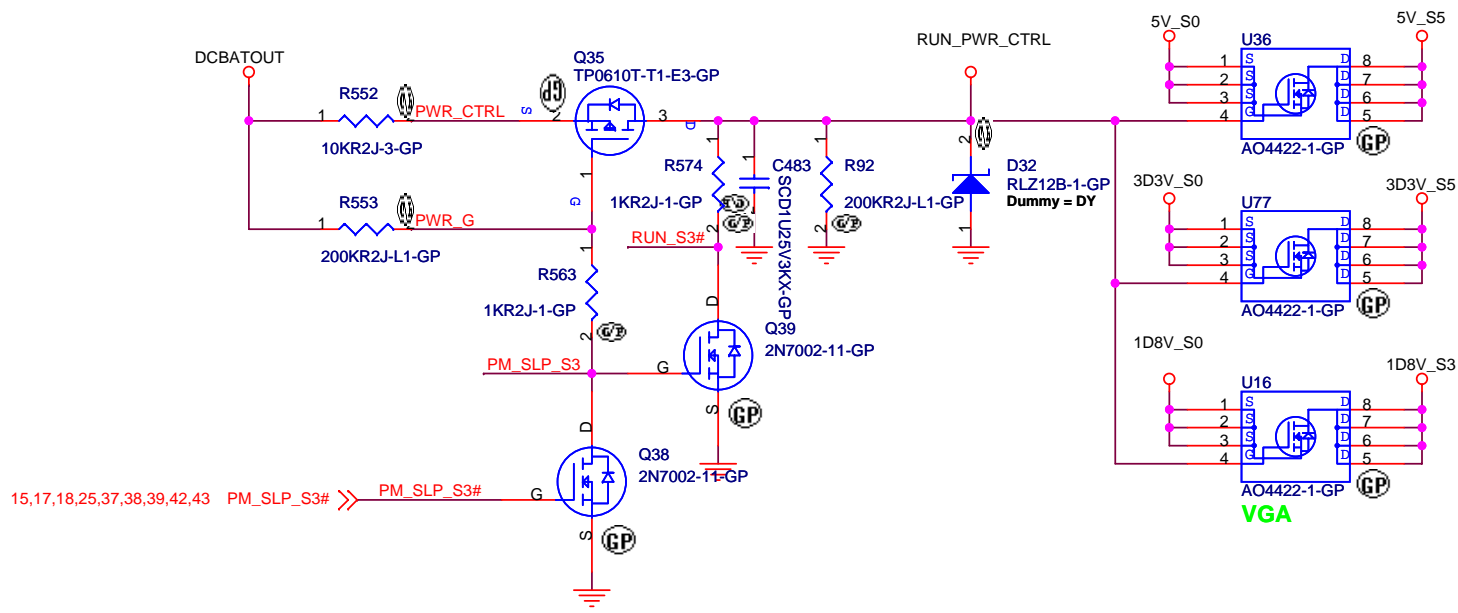


AUDIO OP AMPLIFIER

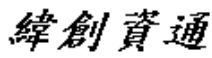
Internal Speaker



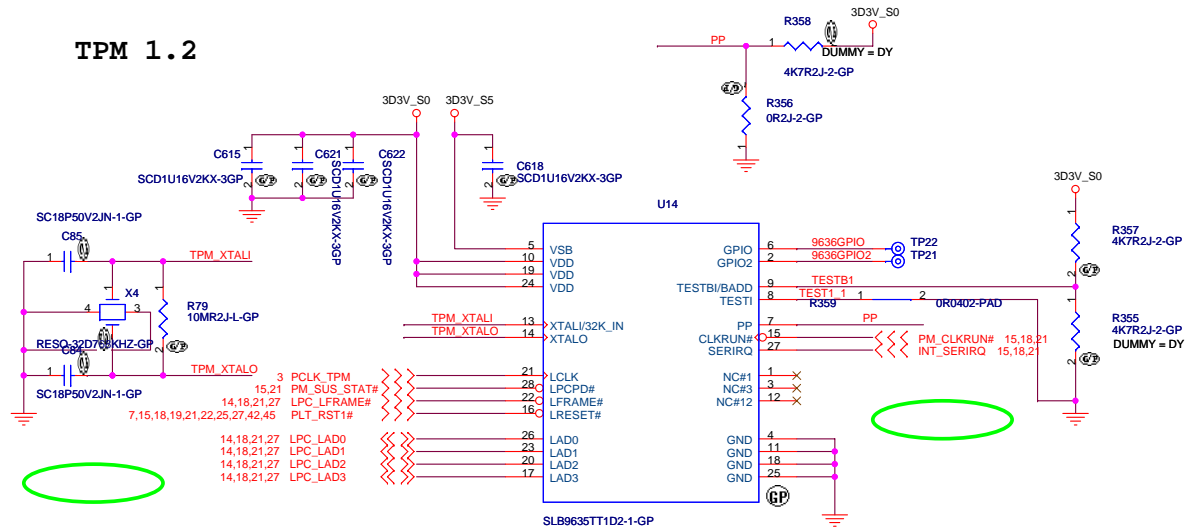
Run Power



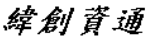
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TITLE RUN POWER / CTRL LOGIC	
Size A4	Document Number MAKI
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TPM 1.2



<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
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Size	Document Number
Custom	MAKI
Date: Friday, January 18, 2008	Rev SA

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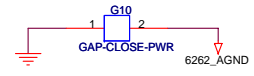
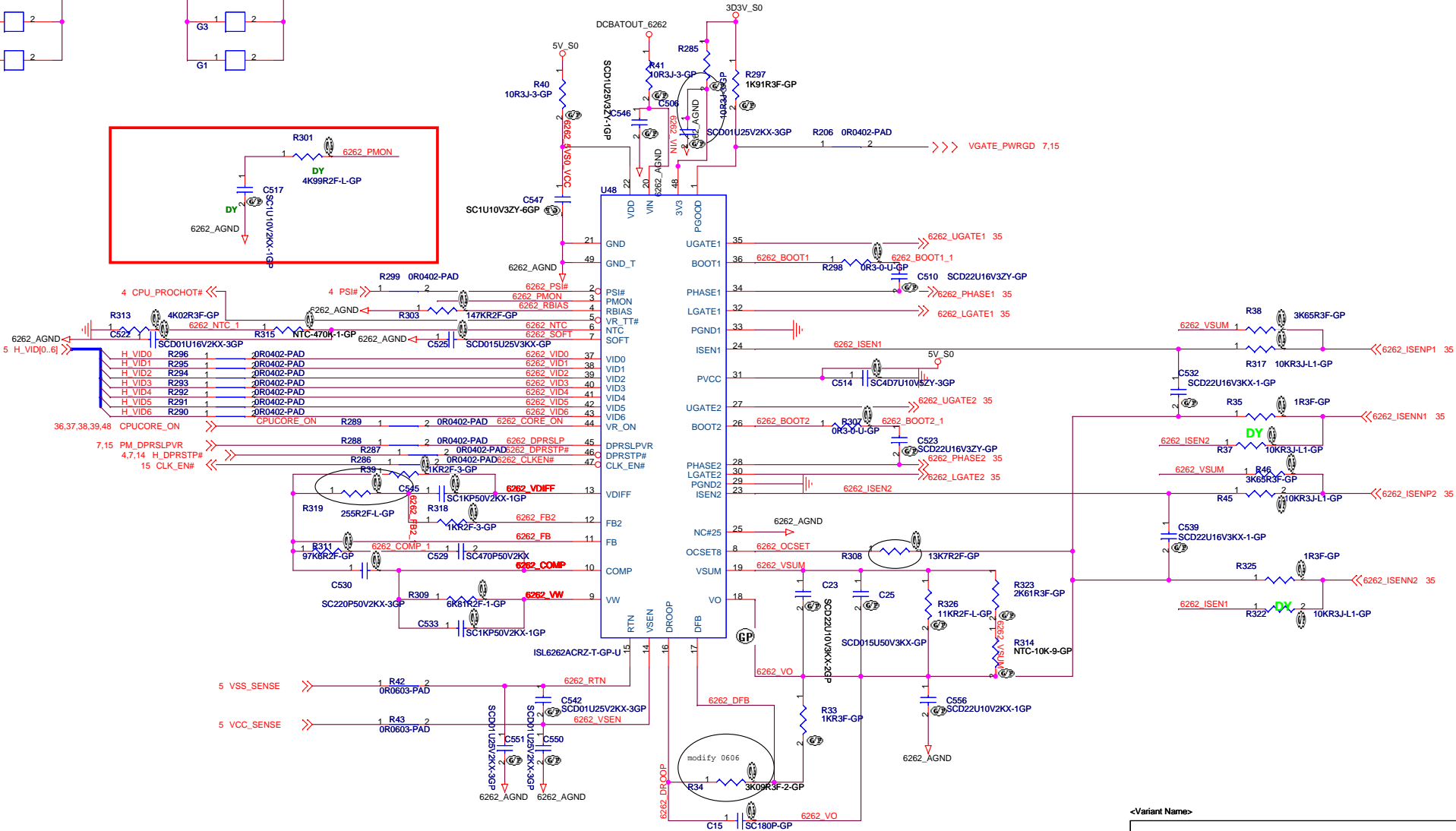
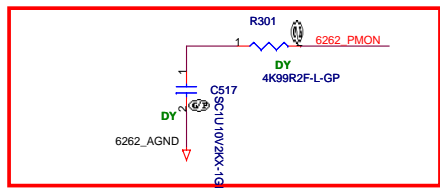
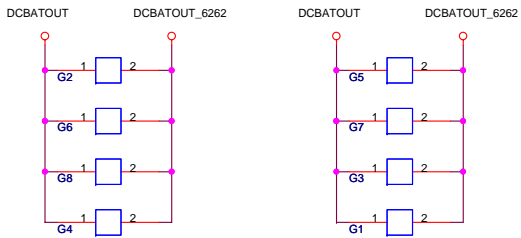
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

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Custom	MAKI	SA

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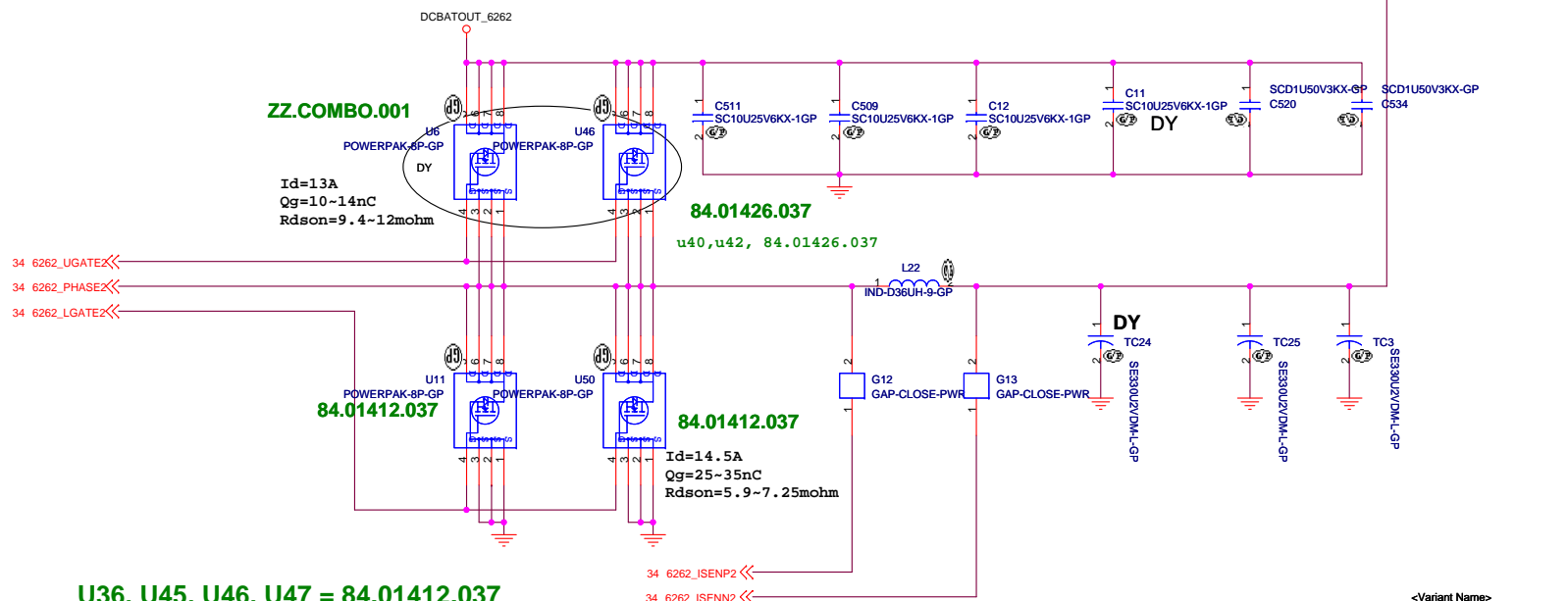
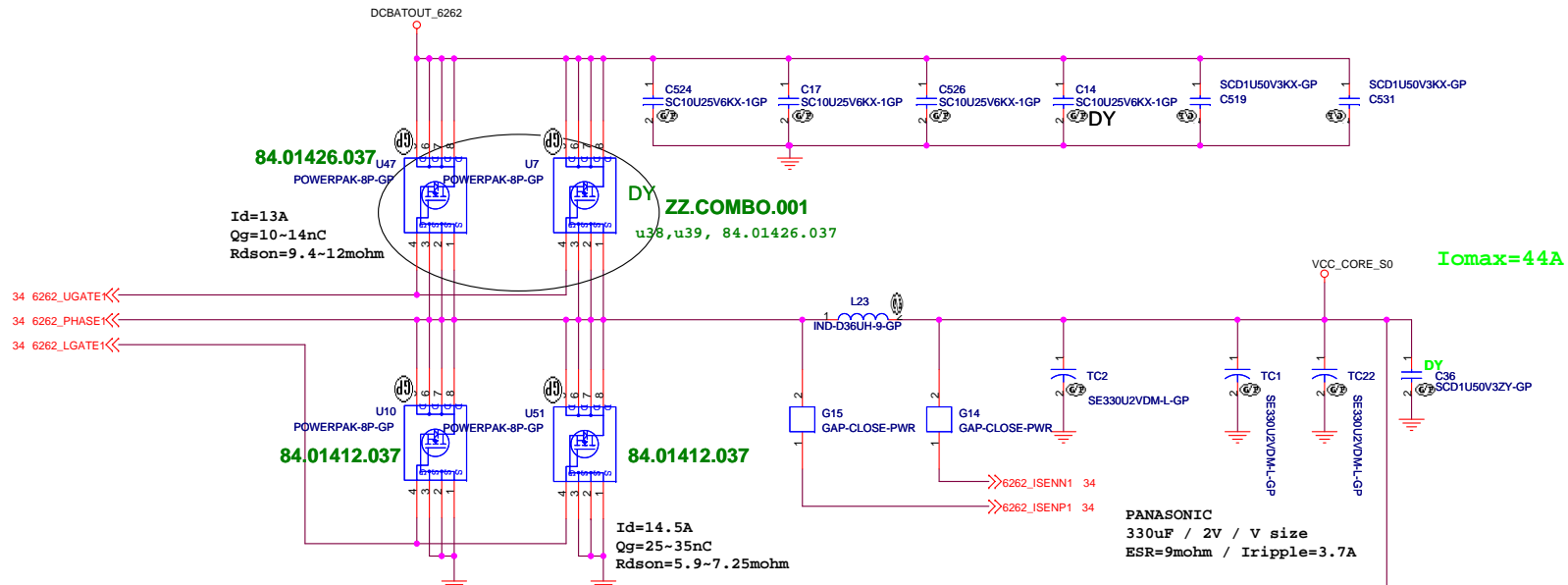
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU CORE (1/2) ISL6262**

Size: A3	Document Number: MAKI	Rev: SA
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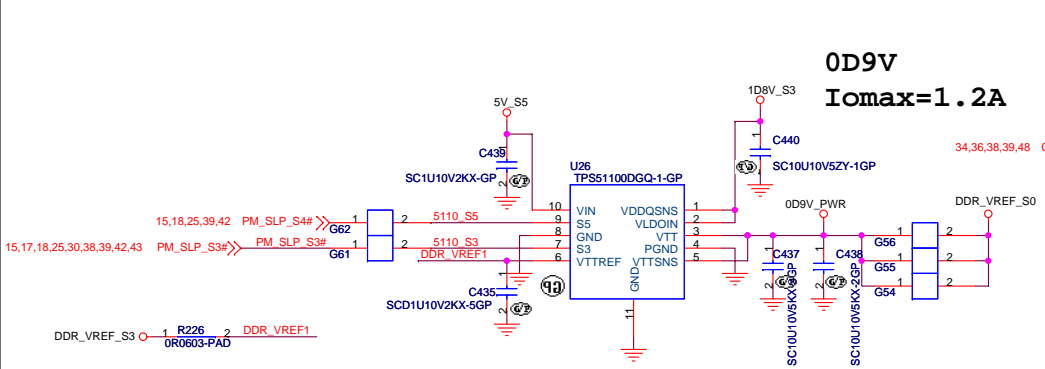


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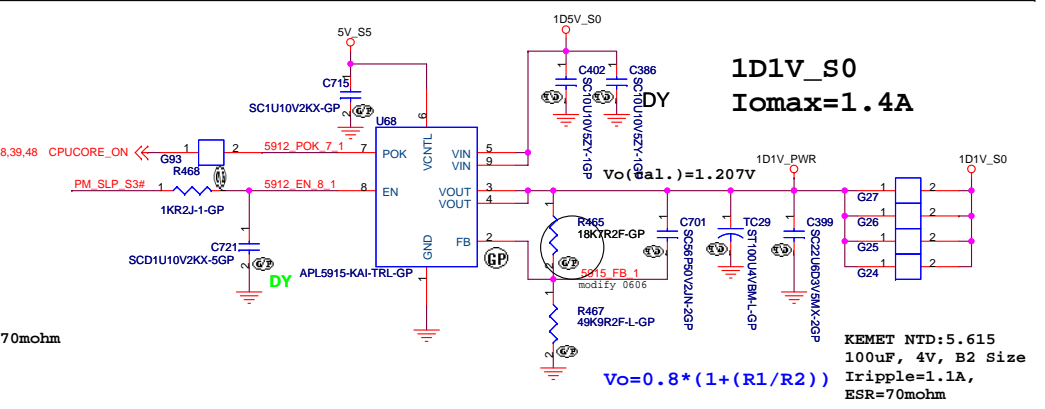
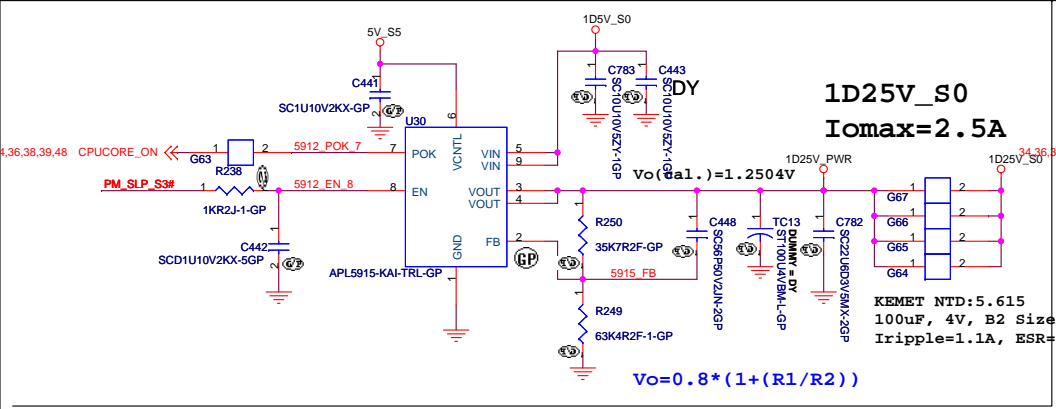
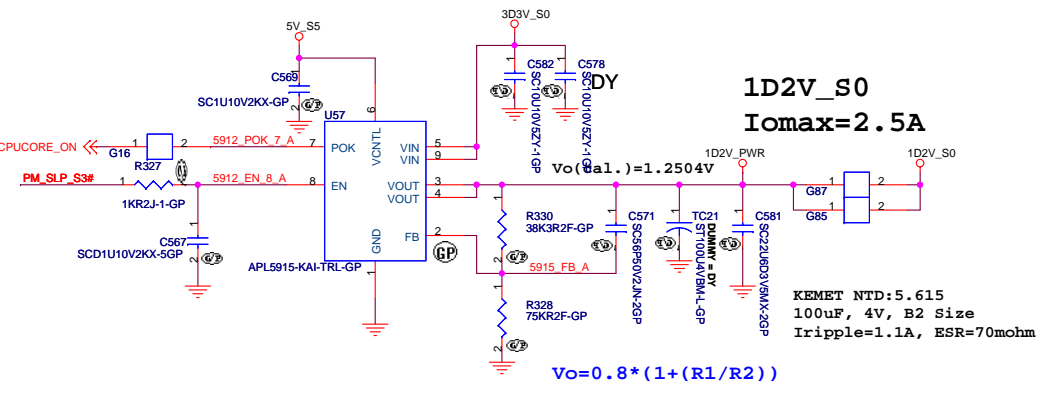
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Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU CORE(2/2) ISL6262
Size	Document Number
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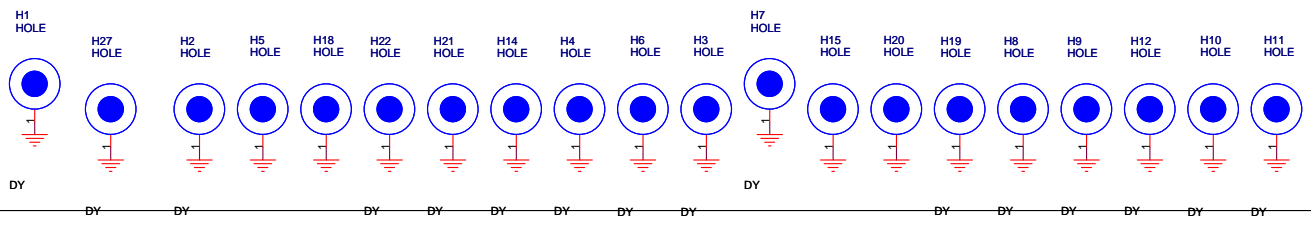
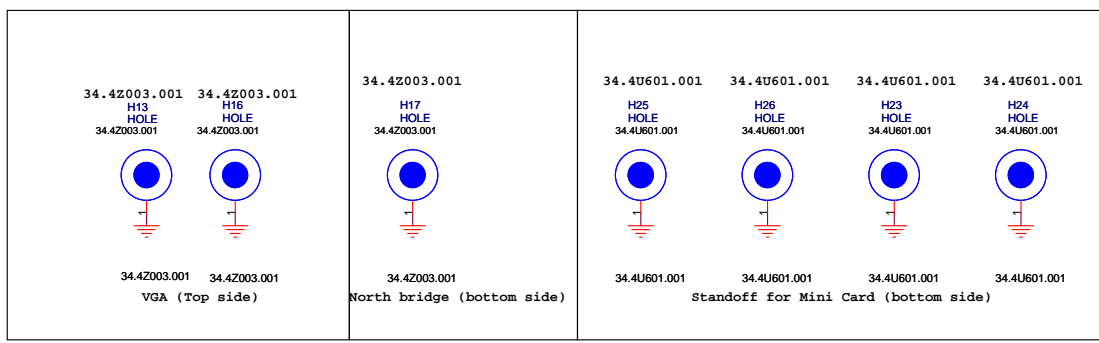
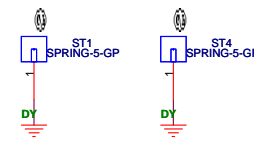
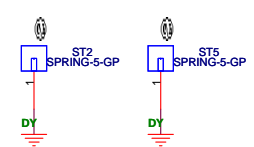
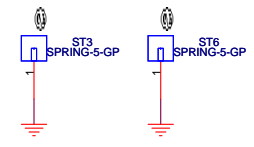
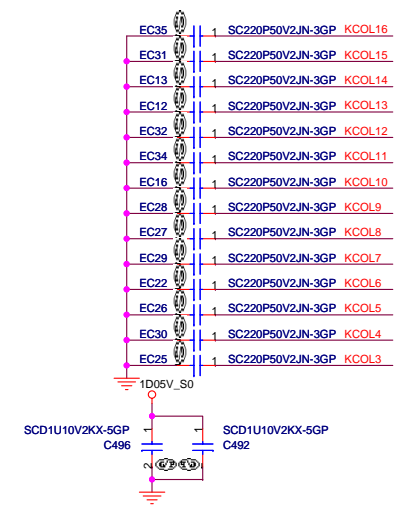
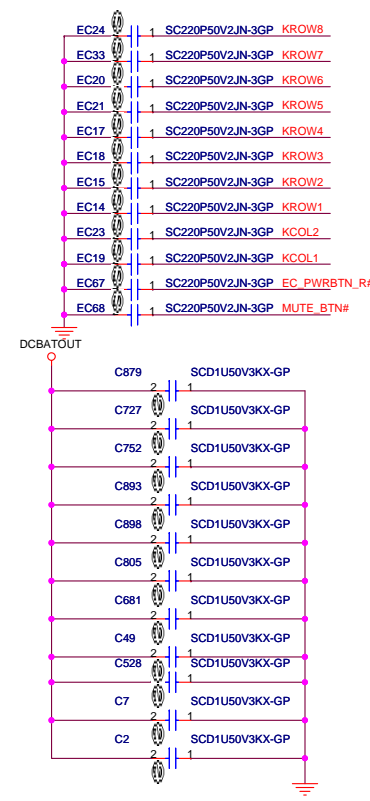
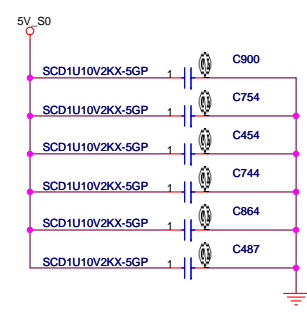
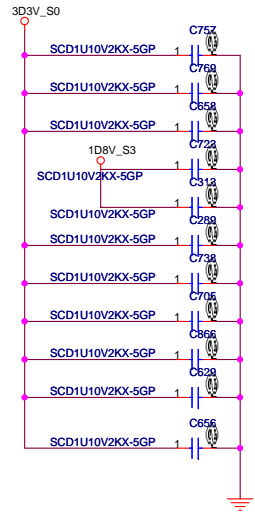
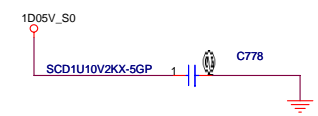
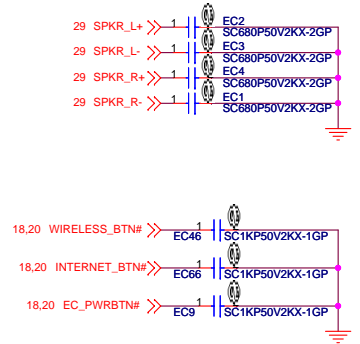
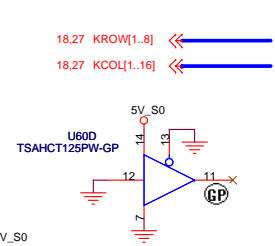
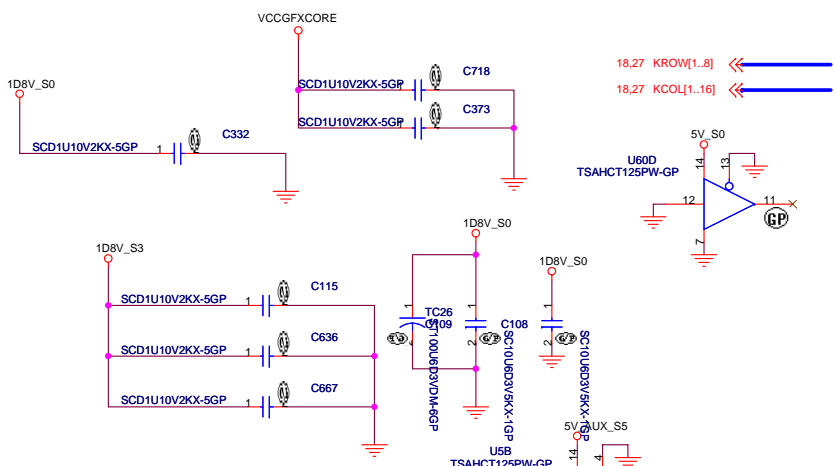


Place near the Test point DDRVREF



<Variant Name>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
SC411 1D05V/1D8V			
Title	Document Number		
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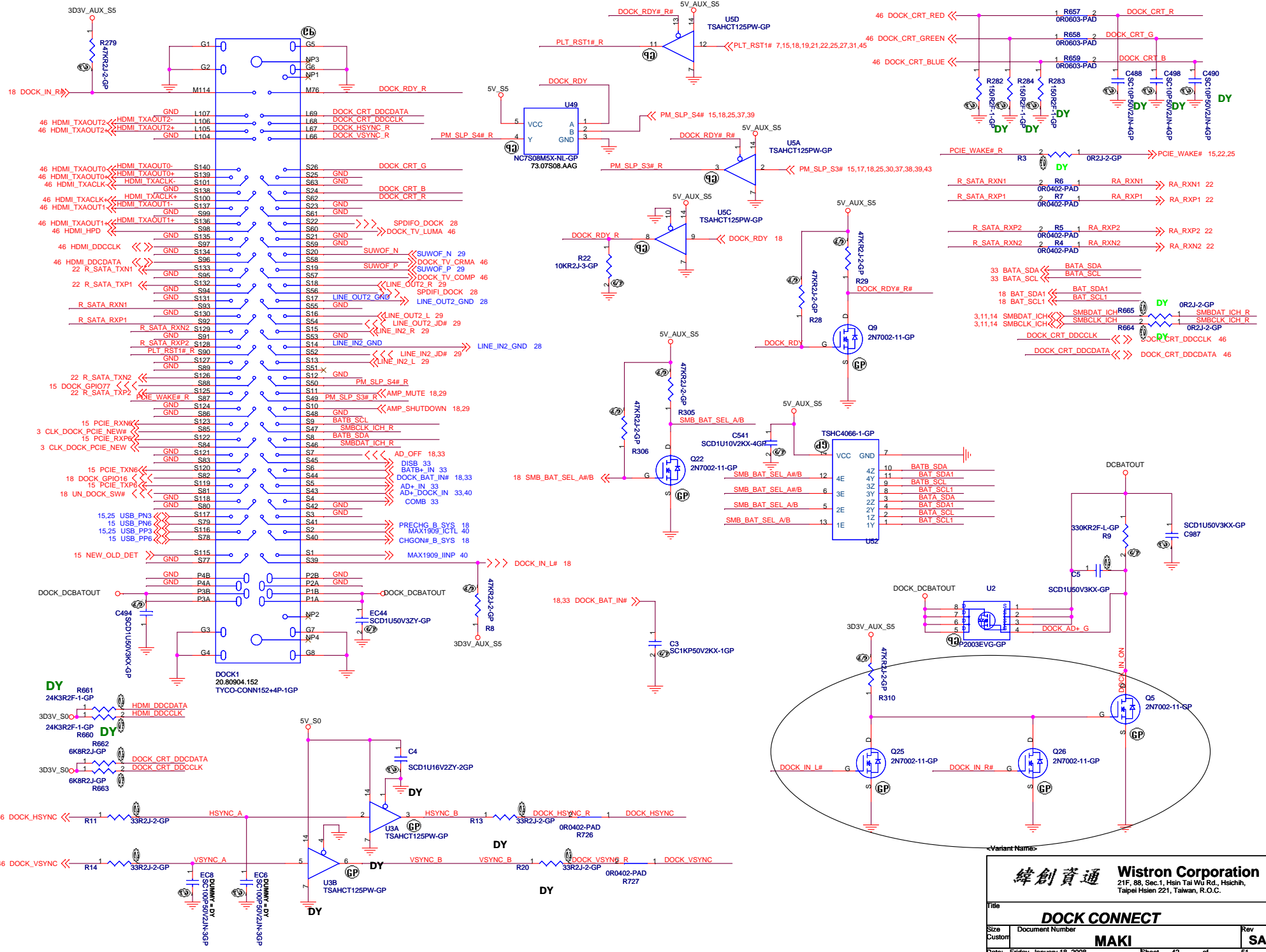


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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **UNUSED PARTS/EMI Capacitors**

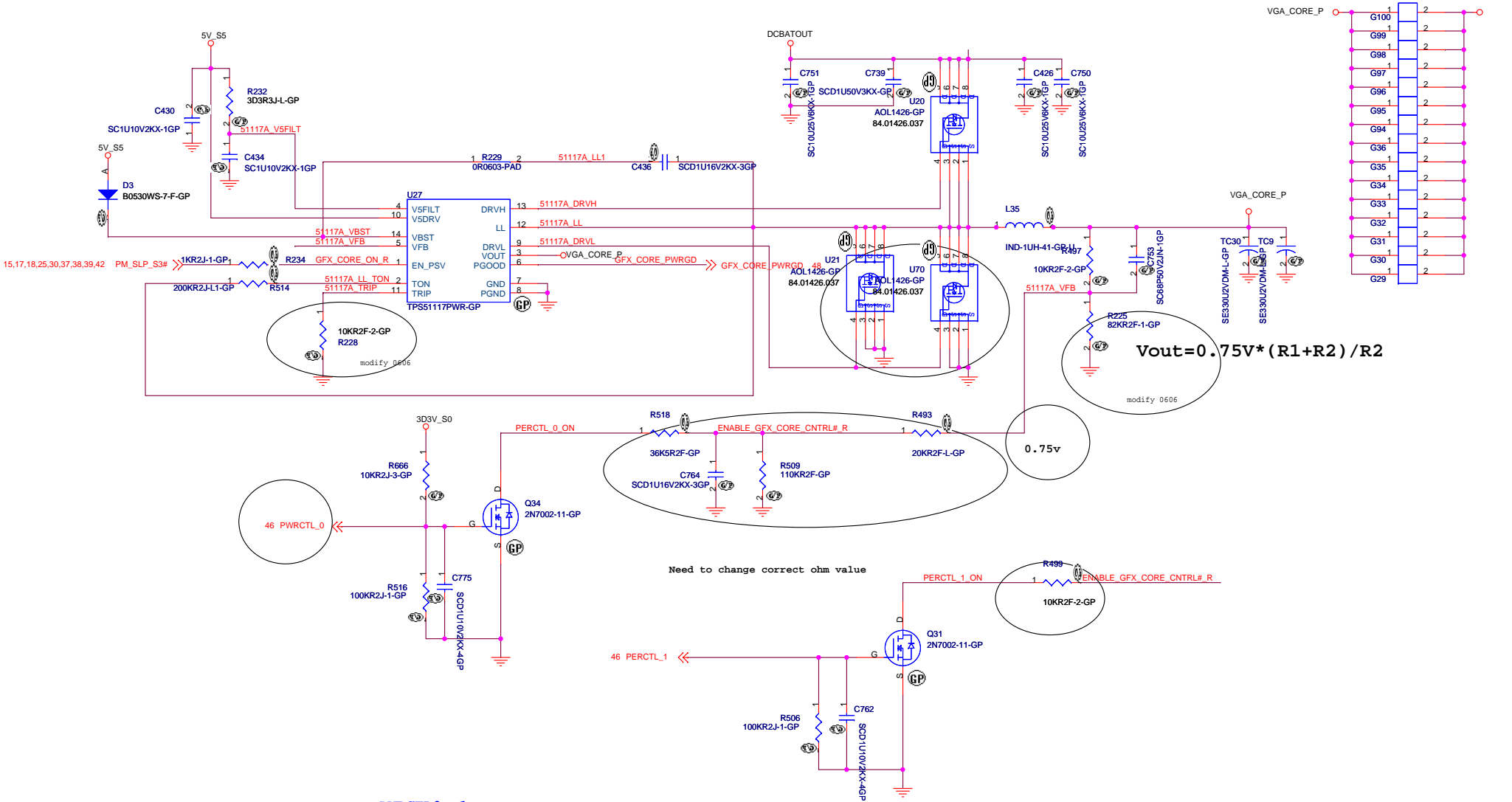
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緯創資通 **Wistron Corporation**
 21F, 88, Sec-1, Hsin Tai Wu Rd., Hsichin,
 Taipei Hsin 221, Taiwan, R.O.C.

DOCK CONNECT		
Title		
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Design Current = 20A
 OCP design = 24A



PWRCTL0 &1=
 00 =>V0=0.9
 DEF 10 =>V0=1V
 01 => V0=1.1V

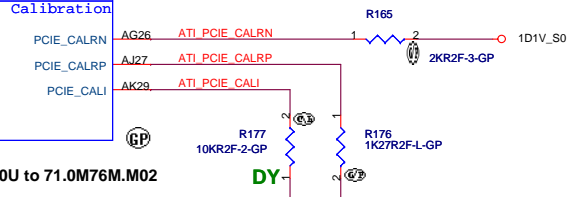
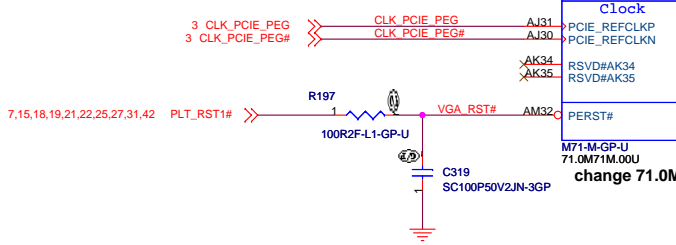
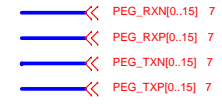
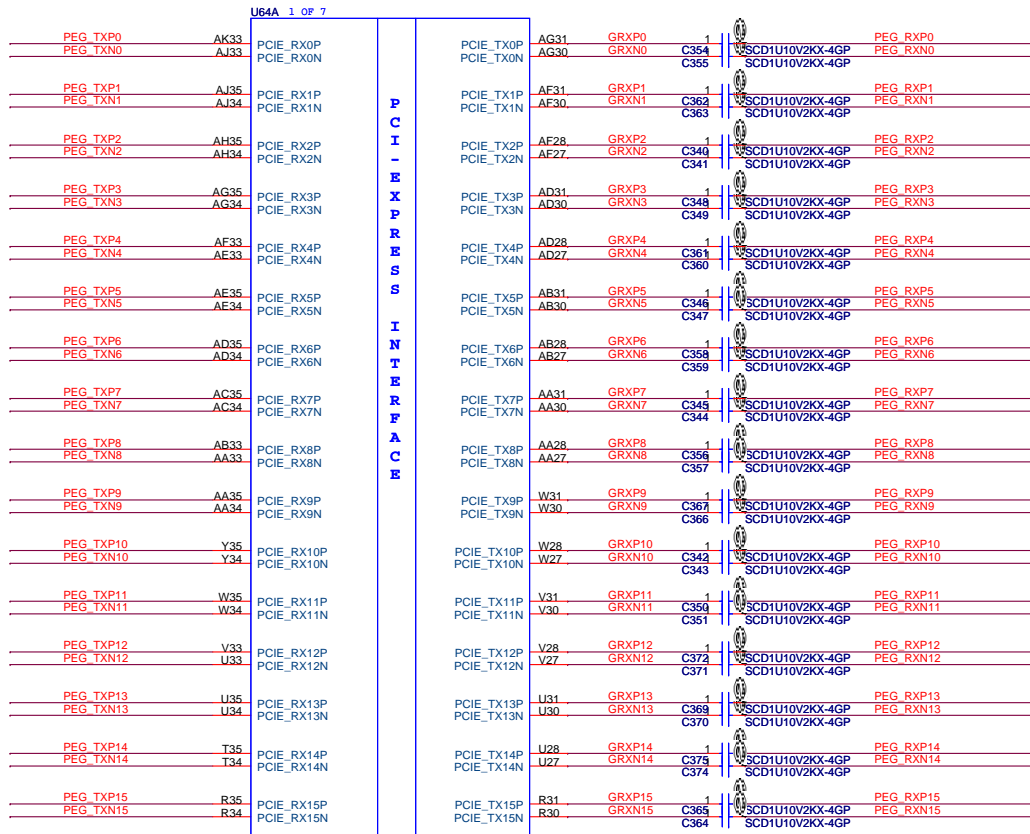
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC/DC NVVDD S0(TPS51117)**

Size A3 Document Number **MAKI** Rev SA

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For PCIE_CALRP
1.27K to PCIE_VSS for M72M,M76M
562R to PCIE_VSS for M66M,M71M

For PCIE_CALI
10K to PCIE_VSS for M72M,M76M
1.47K to PCIE_VSS for M66M,M71M

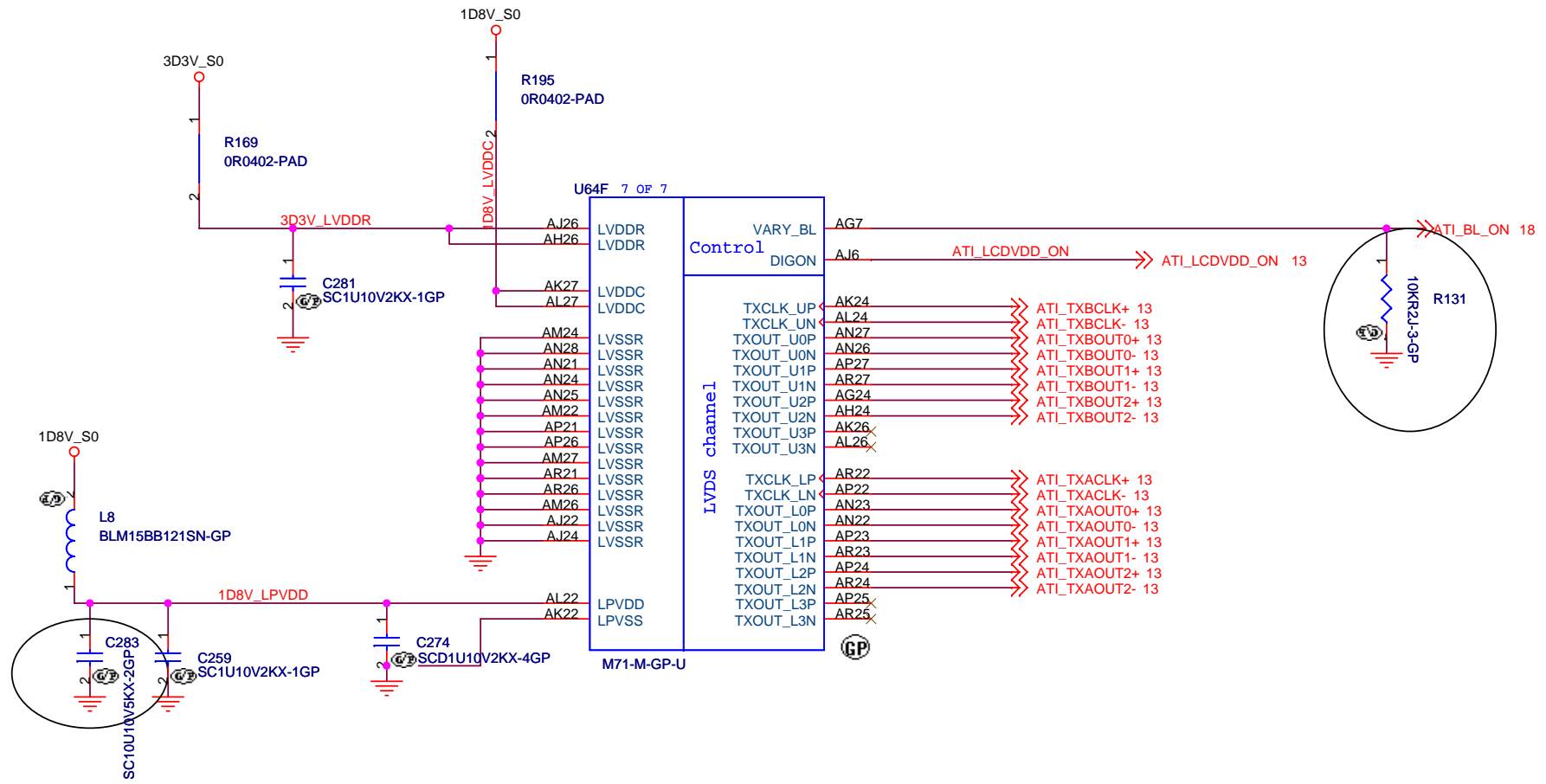
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

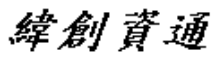
Title: **VGA-M71M_PCIE**

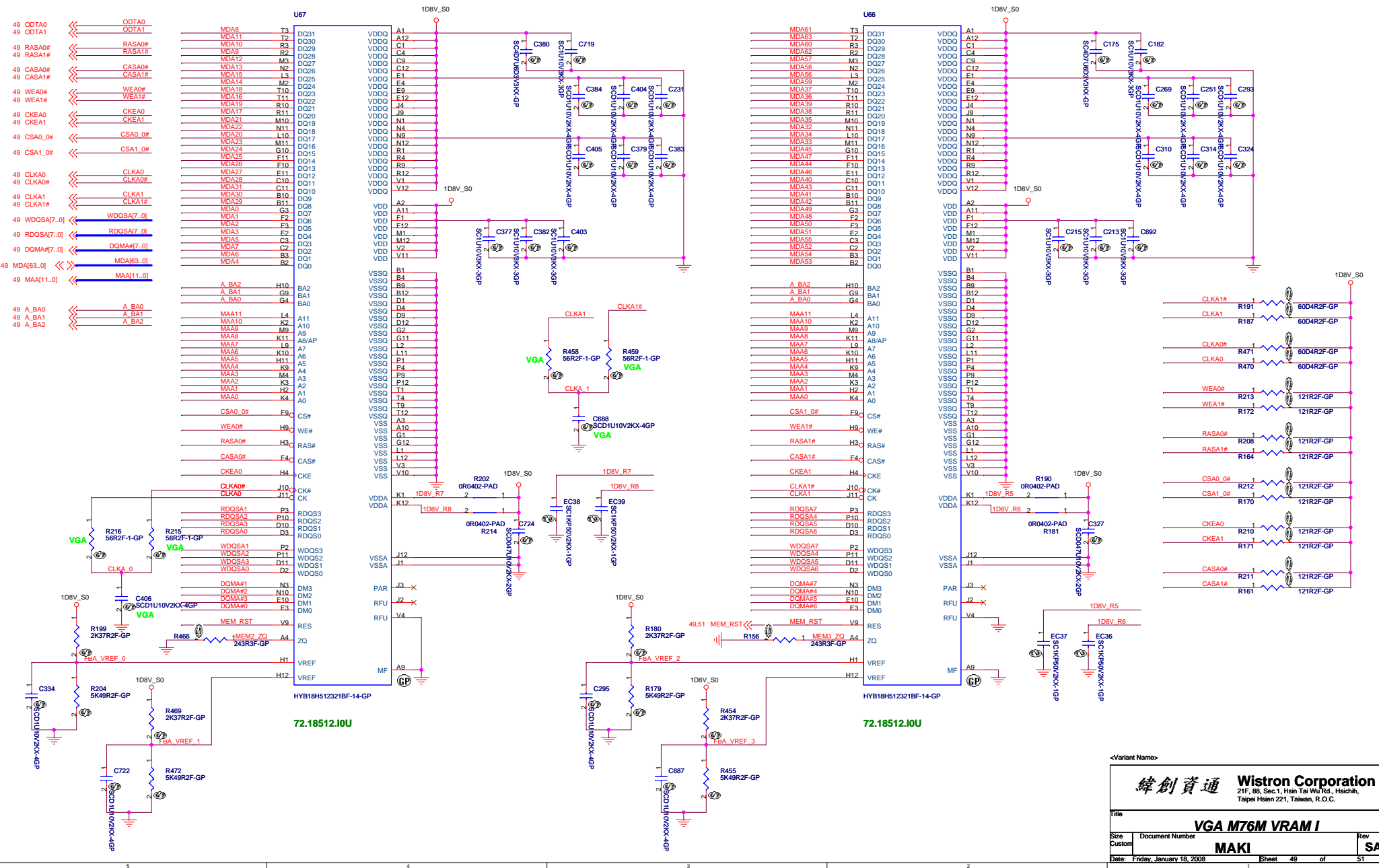
Size A3 Document Number: **MAKI** Rev SA

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<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
VGA-M71M LVDS	
Size A4	Document Number MAKI
Date: Friday, January 18, 2008	Rev SA



<Variant Names>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA M76M VRAM I**

Size: Custom | Document Number: **MAKI** | Rev: **SA**

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History

2006/11/17

1. Schematic drawing start..

2006/12/12

1. Change to project name to C45/C46

2007/01/08

1. LAB gerber out

BOM Change (LAB)

2006/12/29

1. VGA Change to M72, VRAM 128MB, but verify M71 (71.0M71M.M02) and M72(71.0M72M.M01) in LAB

2. 965GM (71.GM965.00U)

3. 965PM (71.PM965.00U)

4. RTSS5158 (71.08111.A03)

5. ME stand off 34.4G901.001 (H23, H25, H9, H11) for MINI Card

6. ME stand off 34.4B601.001 (H26, H27) for MODEM

7. ME stand off 87.00055.120 (H4) for LVDS

8. ICH8-M (71.ICH8M.A0U)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

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A3

Document Number

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