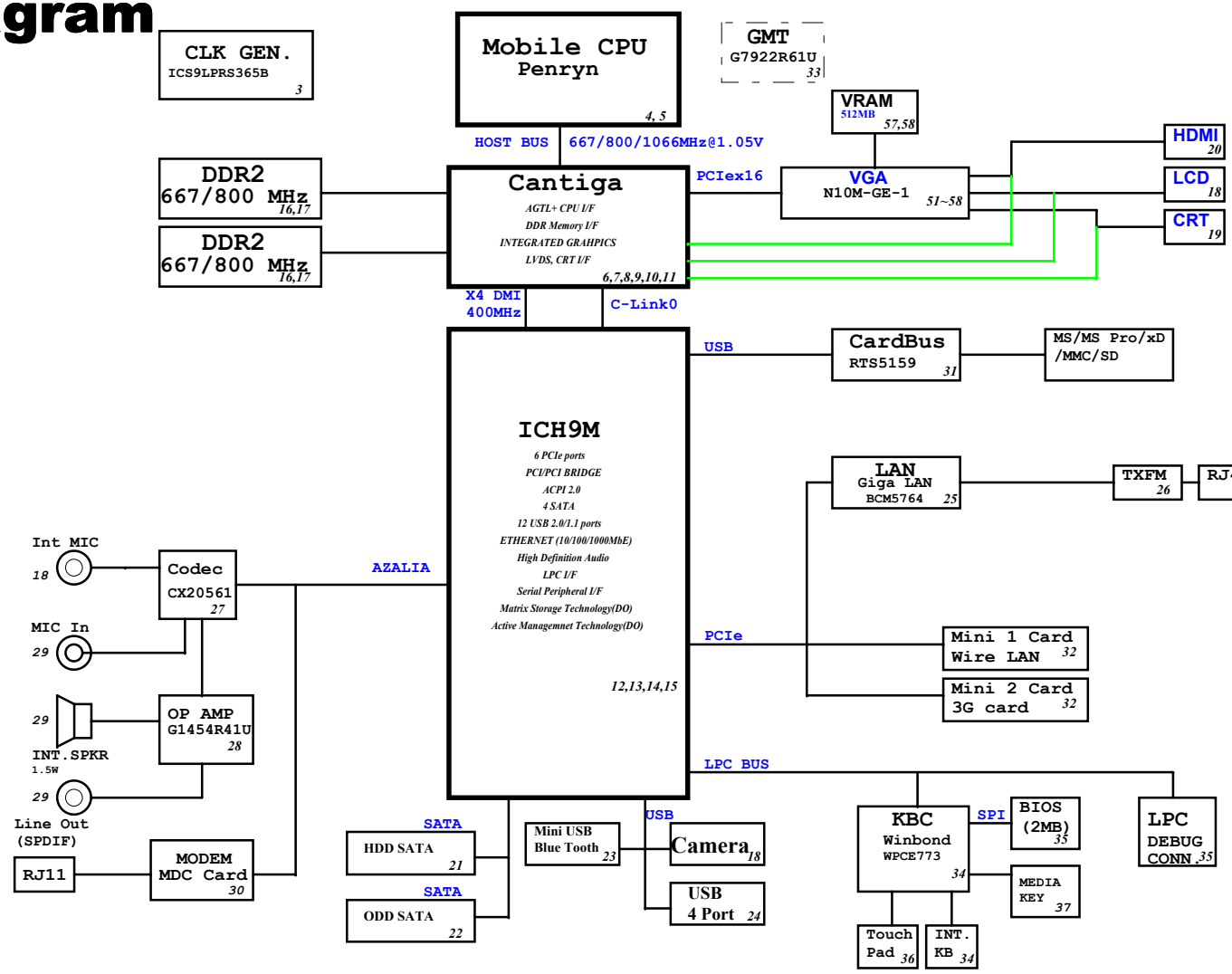
SJV50 Block Diagram

Project code: 91.4BU01.001
PCB P/N : 48.4BU01.0SB
REVISION : 08244-SB



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D8V_S3(13A)

RT9026 43	
1D8V_S3	DDR_VREF_S3 (1.2A)

RT9018 44	
1D8V_S3	1D1V_S0(2A)

RT9018 44	
1D8V_S3	1D5V_S0 (2.5A)

CHARGER ISL88731A 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202 48	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (11A)

SJV50

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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Title: **Reference**

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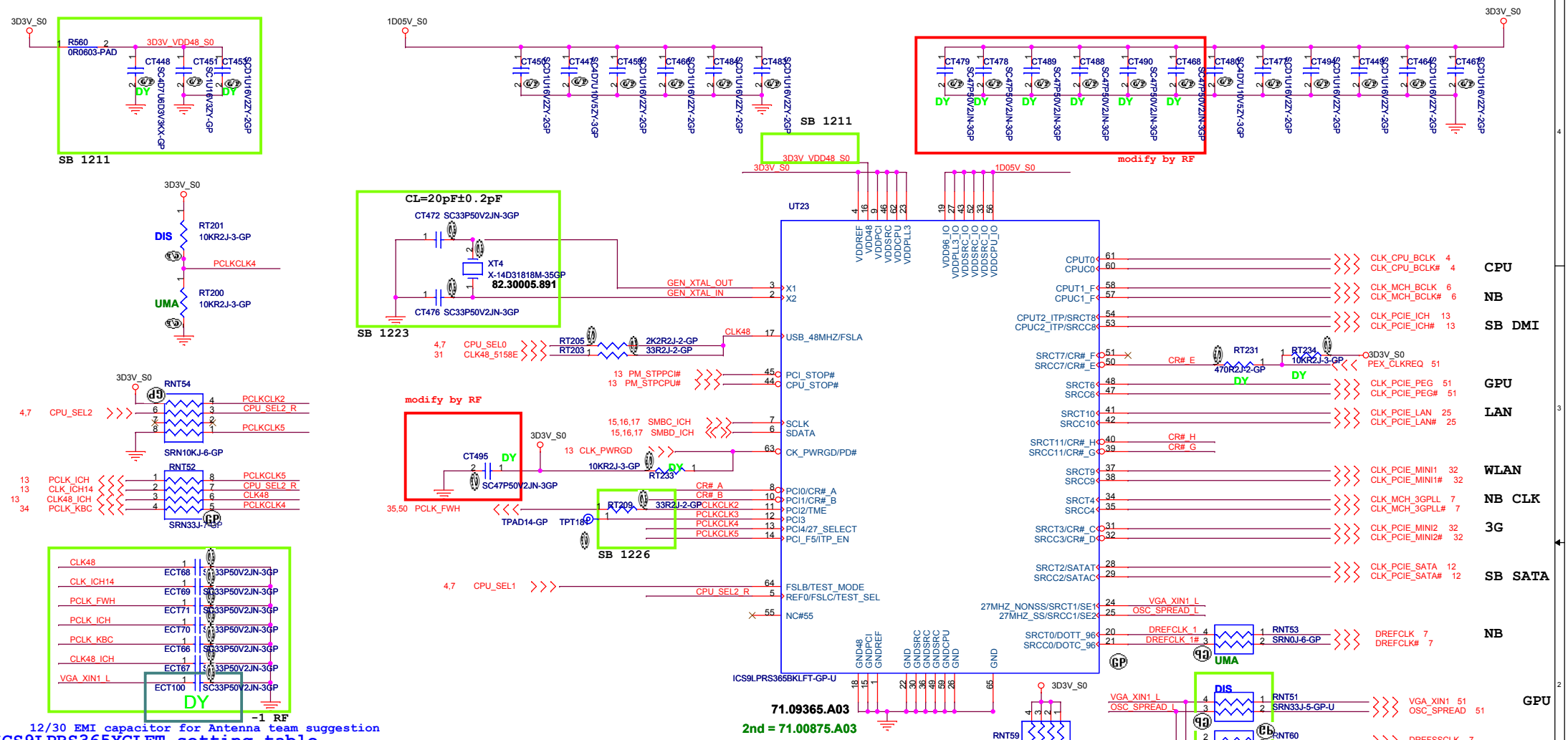

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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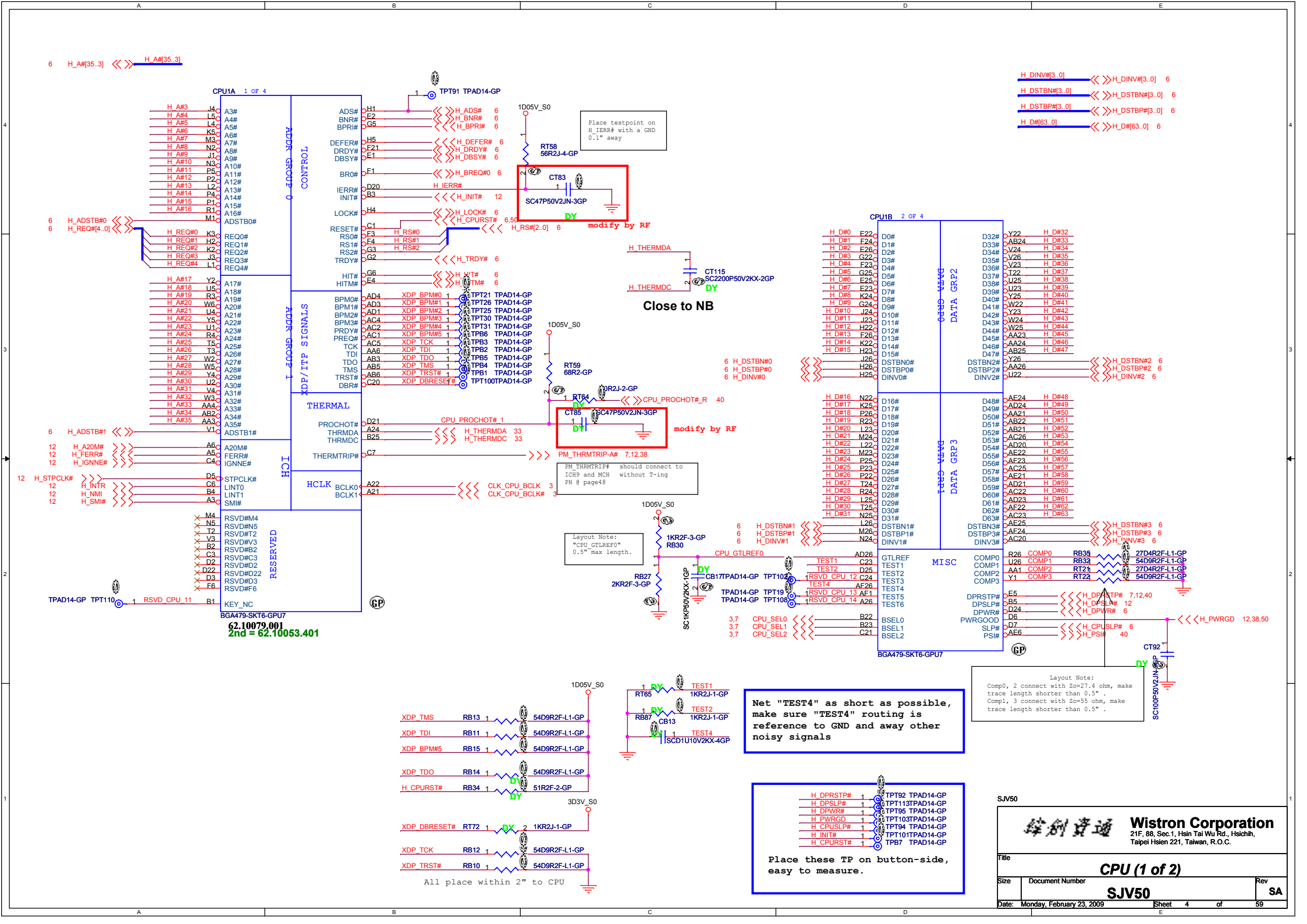
CPU1A 1 OF 4
ADDR GRP0
ADDR GRP1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
CPU1B 2 OF 4
DATA GRP2
DATA GRP3
MISC
Close to NB
modify by RF
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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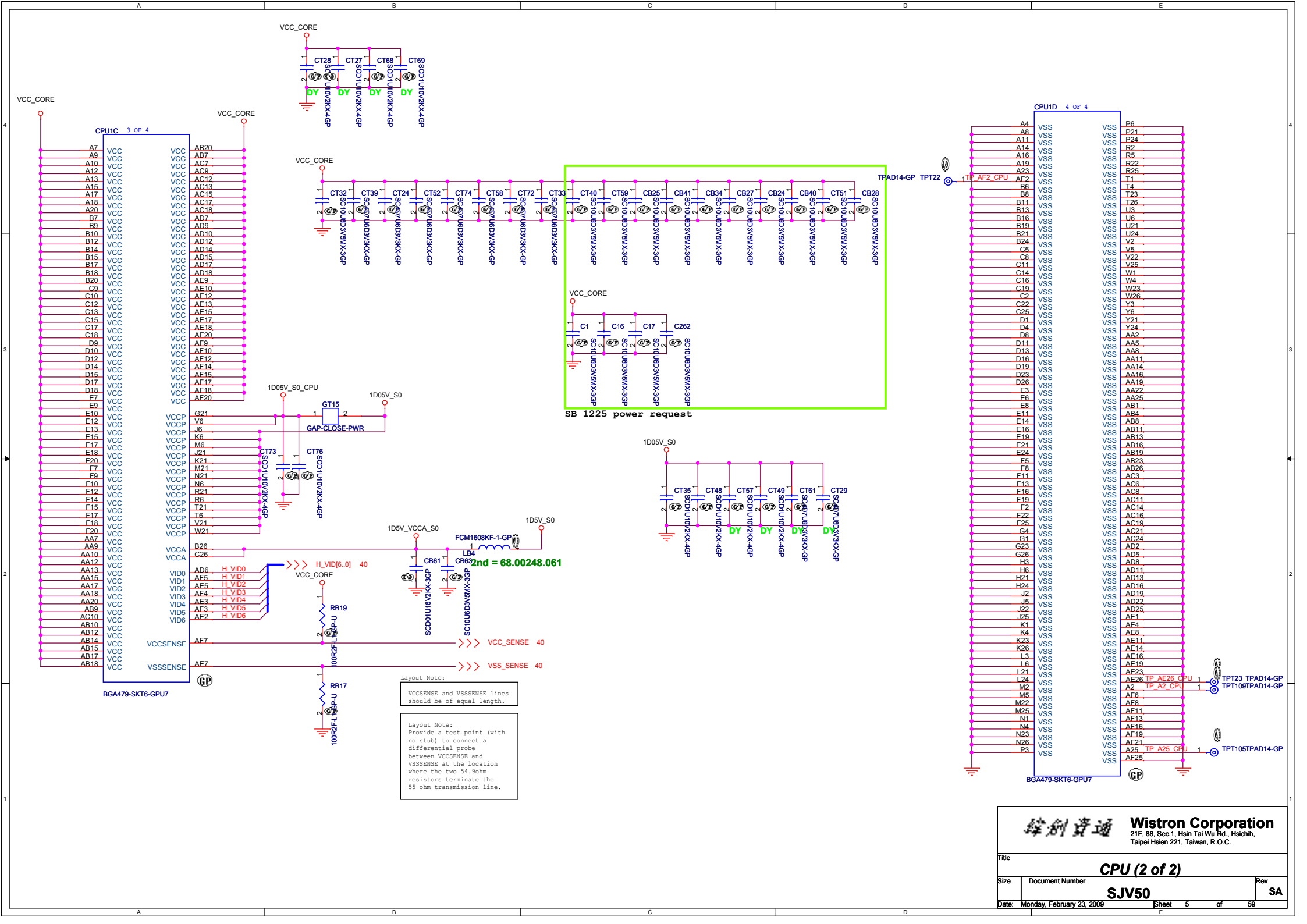

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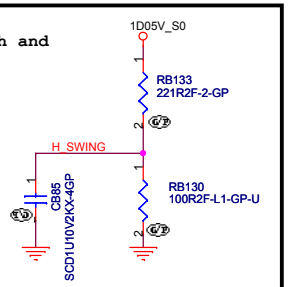
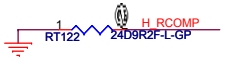
H_SWING routing Trace width and Spacing use 10 / 20 mil

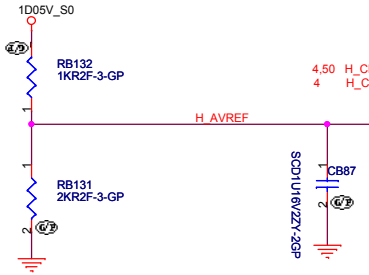
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

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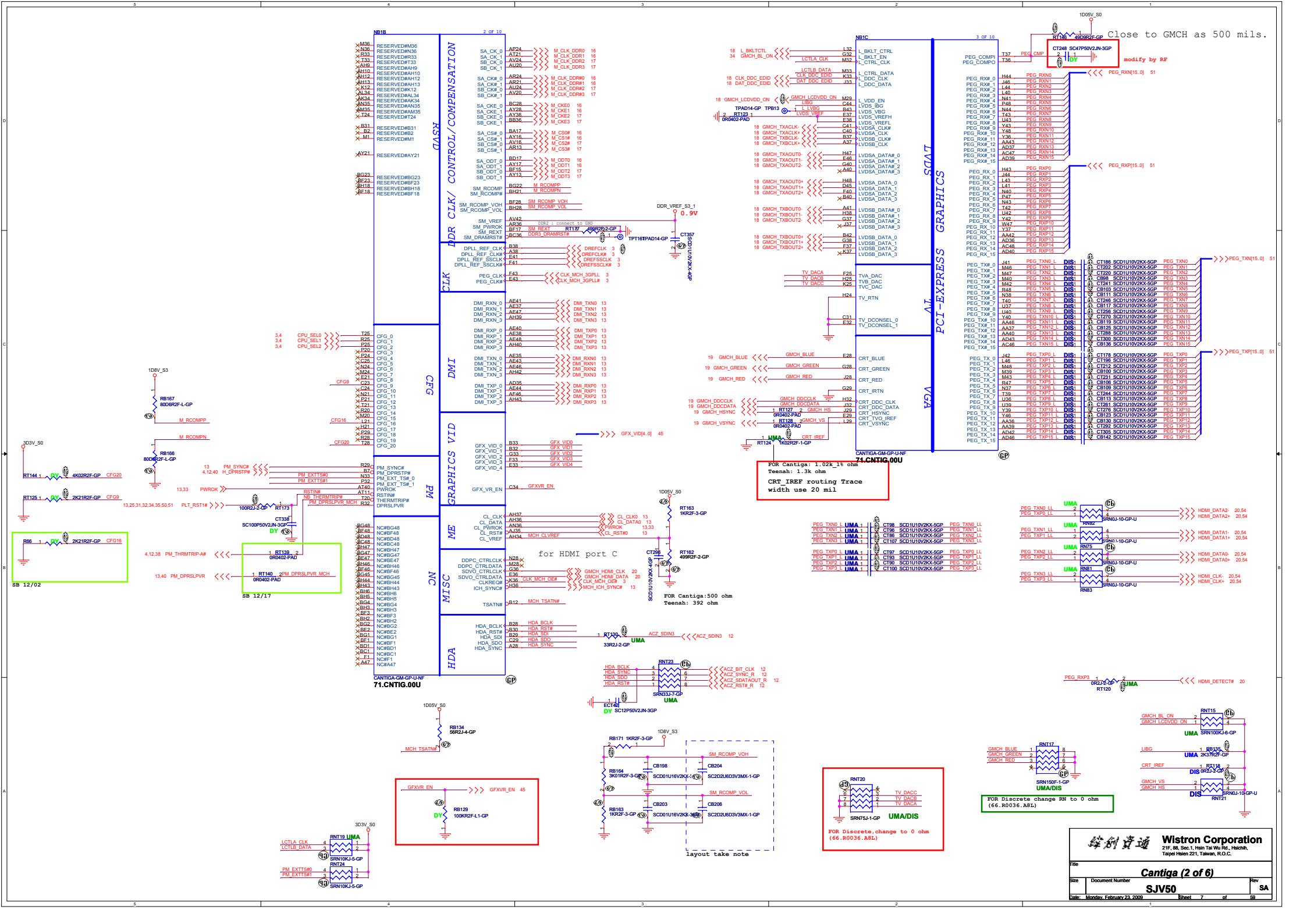
Close to GMCH as 500 mils.
modify by RF
NB1B
NB1C
RESERVED
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
HDA
SDVO
PCI-EXPRESS GRAPHICS
LVDS
TV
VGA
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change RN to 0 ohm
(66.R0036.A8L)
FOR Discrete,change to 0 ohm
(66.R0036.A8L)
layout take note
SB 12/02
SB 12/17
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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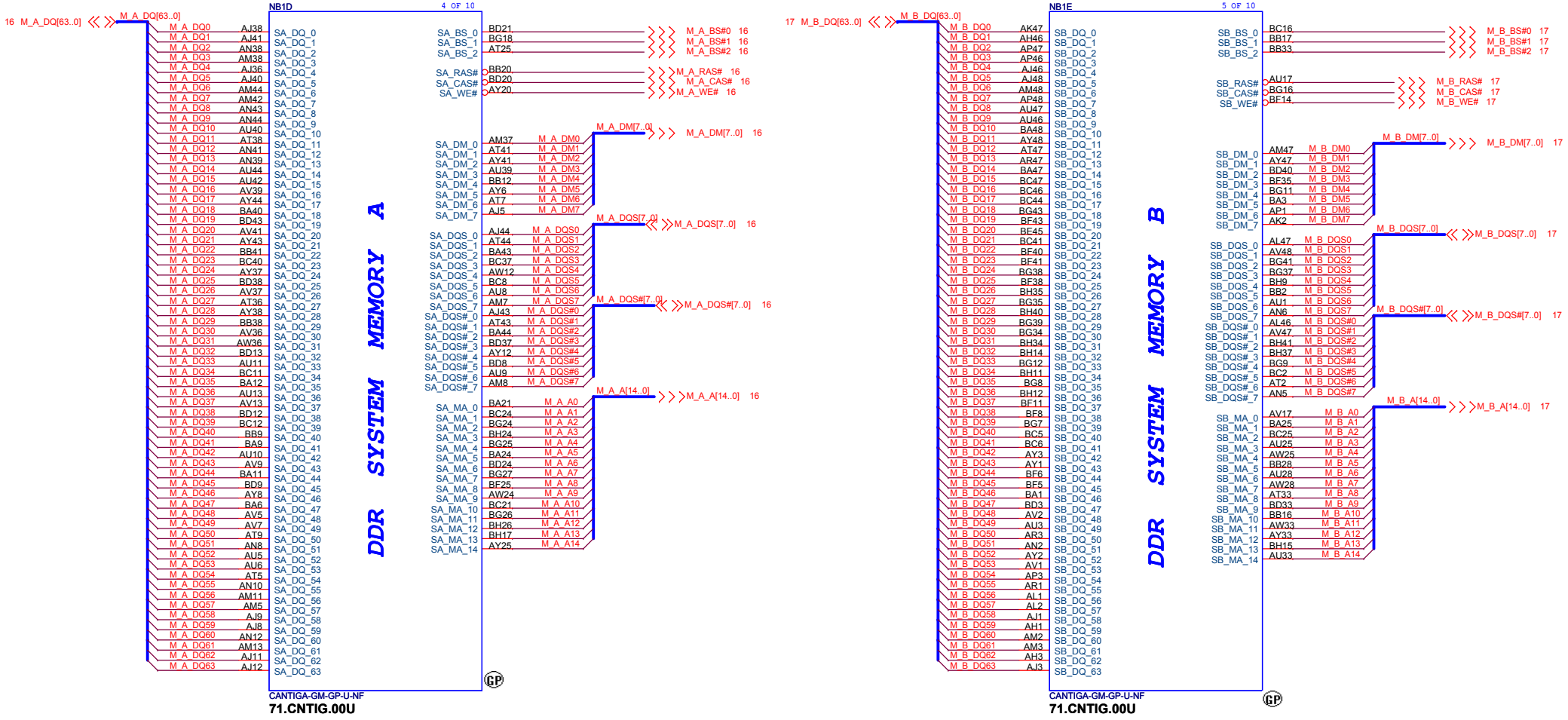

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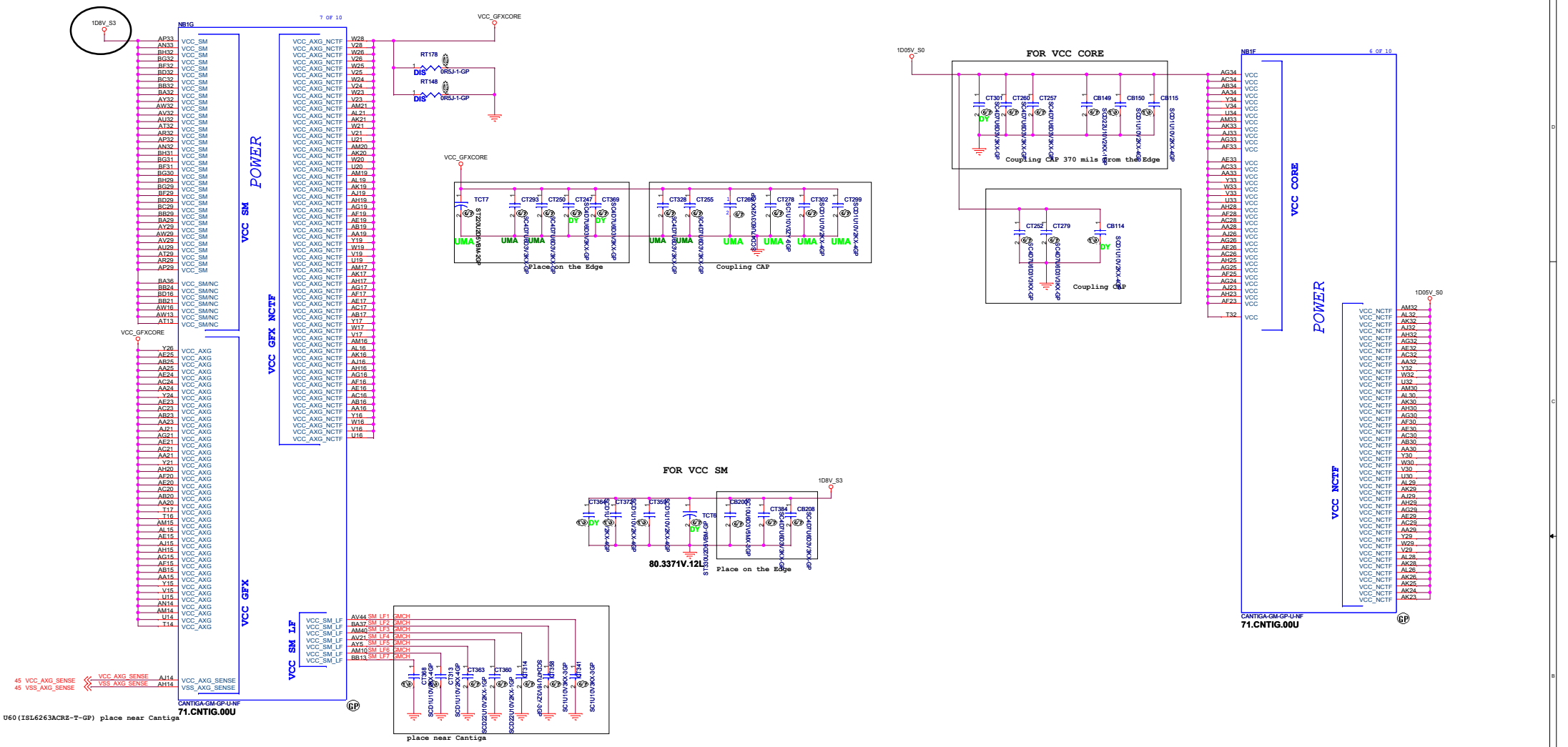

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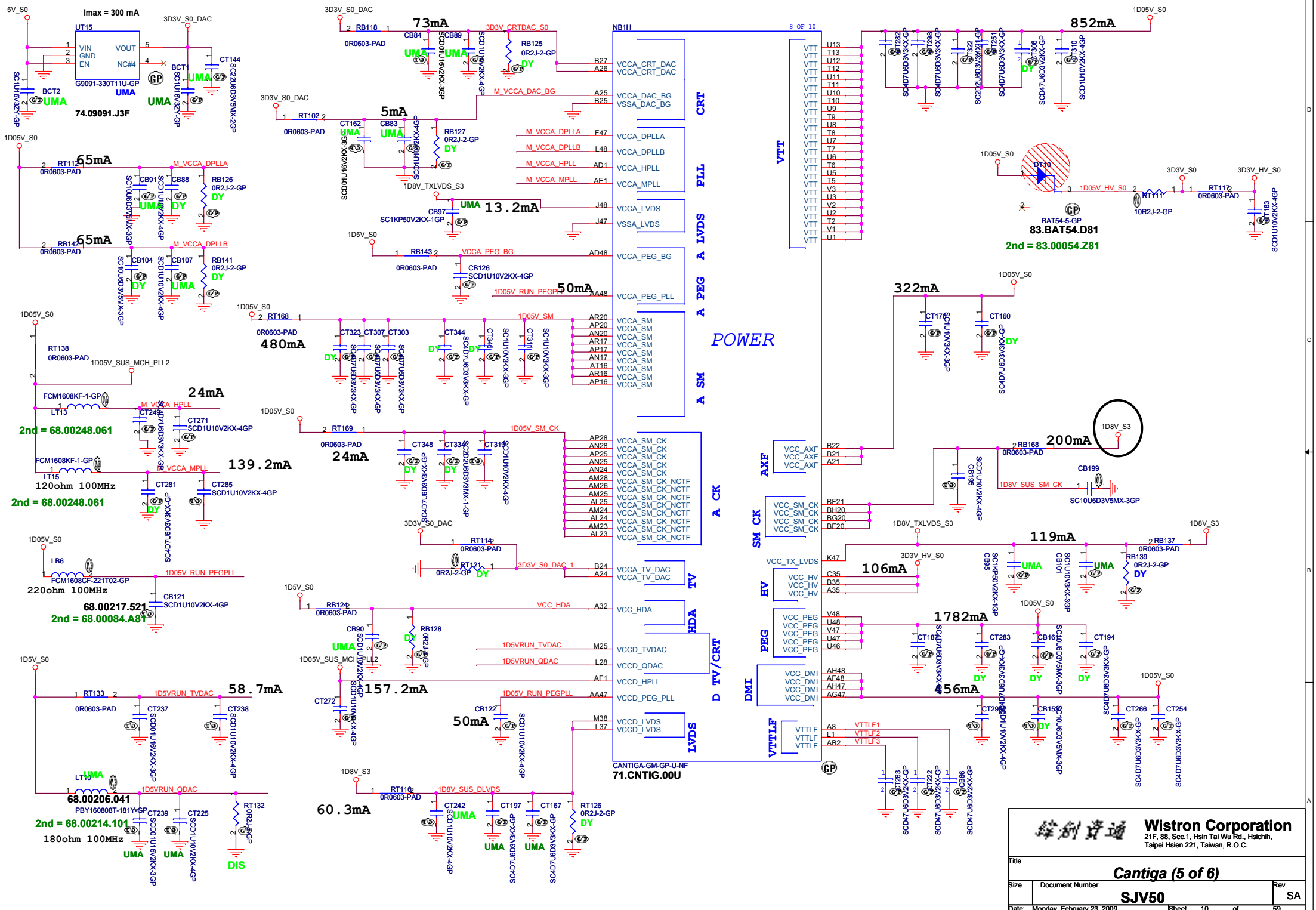
5V_S0
Imax = 300 mA
UT15
VIN
GND
EN
VOUT
NC#4
G9091-330T11U-GP
3D3V_S0_DAC
74.09091.J3F
1D05V_S0
65mA
M_VCCA_DPLLA
M_VCCA_DPLLB
RT112
RT142
RB126
RB141
0R2J-2-GP
0R0603-PAD
73mA
3D3V_CRTDAC_S0
RB125
RB118
5mA
RT102
M_VCCA_DAC_BG
RB127
1D8V_TXLVDS_S3
13.2mA
CB97
SC1KP50V2KX-1GP
VCCA_CRT_DAC
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
CRT
PLL
LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
A PEG
50mA
1D05V_RUN_PEGPLL
480mA
1D05V_SM
VCCA_SM
A SM
POWER
24mA
RT138
1D05V_SUS_MCH_PLL2
FCM1608KF-1GP
LT13
M_VCCA_HPLL
2nd = 68.00248.061
139.2mA
LT15
M_VCCA_MPLL
120ohm 100MHz
2nd = 68.00248.061
LB6
FCM1608CF-221T02-GP
220ohm 100MHz
68.00217.521
2nd = 68.00084.A81
1D05V_SM_CK
24mA
VCCA_SM_CK
VCCA_SM_CK_NCTF
A CK
SM CK
3D3V_S0_DAC_1
RT114
RT121
VCCA_TV_DAC
TV
VCC_HDA
HDA
RB124
RB128
157.2mA
1D5VRUN_TVDAC
1D5VRUN_QDAC
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
D TV/CRT
58.7mA
RT133
RT132
LT10
68.00206.041
PBY160808T-181Y-GP
2nd = 68.00214.101
180ohm 100MHz
DIS
50mA
CB122
VCCD_LVDS
60.3mA
1D8V_S3
1D8V_SUS_DLVDS
RT116
RT126
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
NB1H
8 OF 10
VTT
AXF
VCC_AXF
VCC_TX_LVDS
HV
VCC_HV
PEG
VCC_PEG
DMI
VCC_DMI
VTTLF
322mA
200mA
1D8V_SUS_SM_CK
SC10U6D3V5MX-3GP
119mA
106mA
1782mA
456mA
852mA
83.BAT54.D81
2nd = 83.00054.Z81
BAT54-5-GP
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Title
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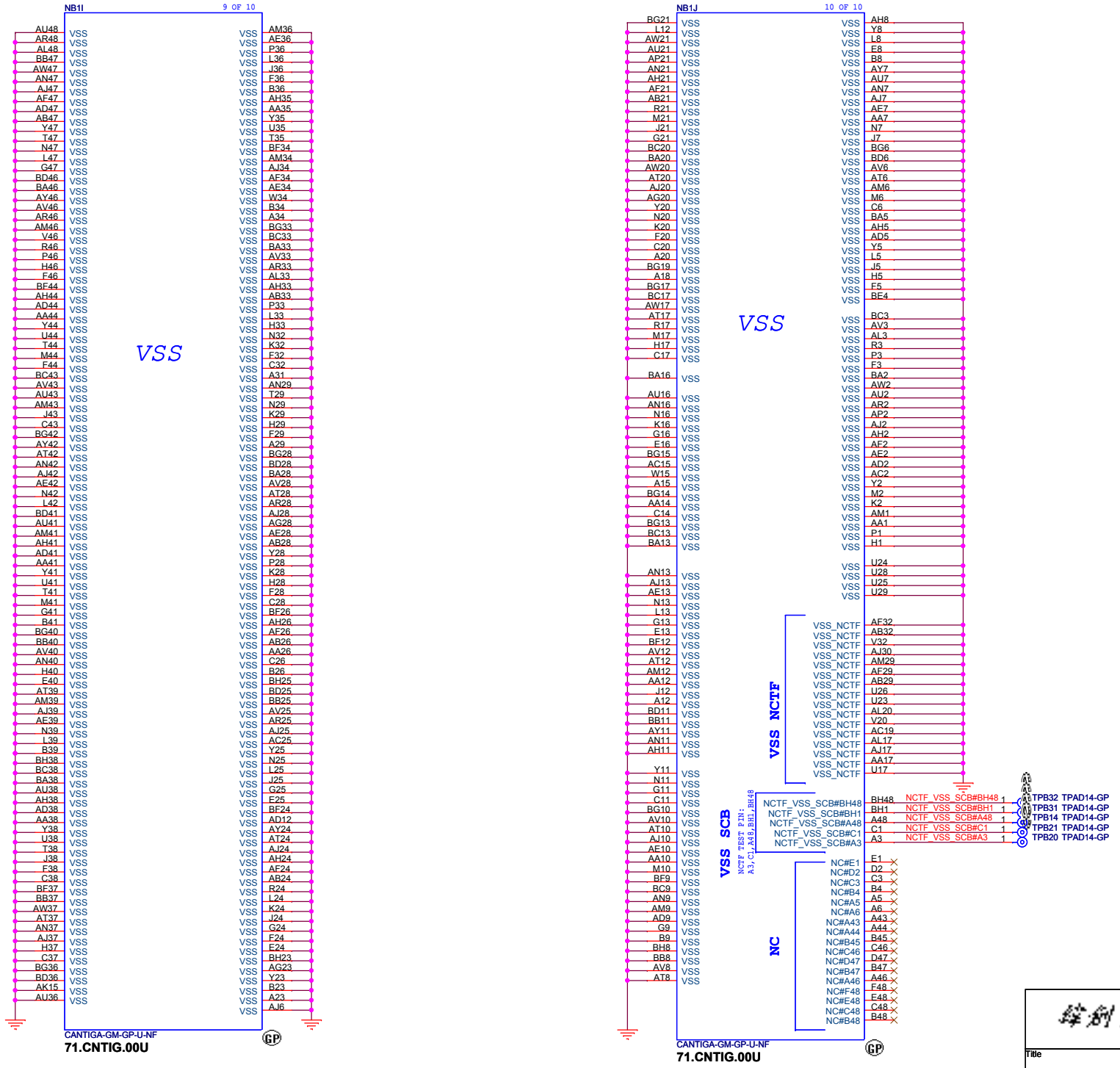

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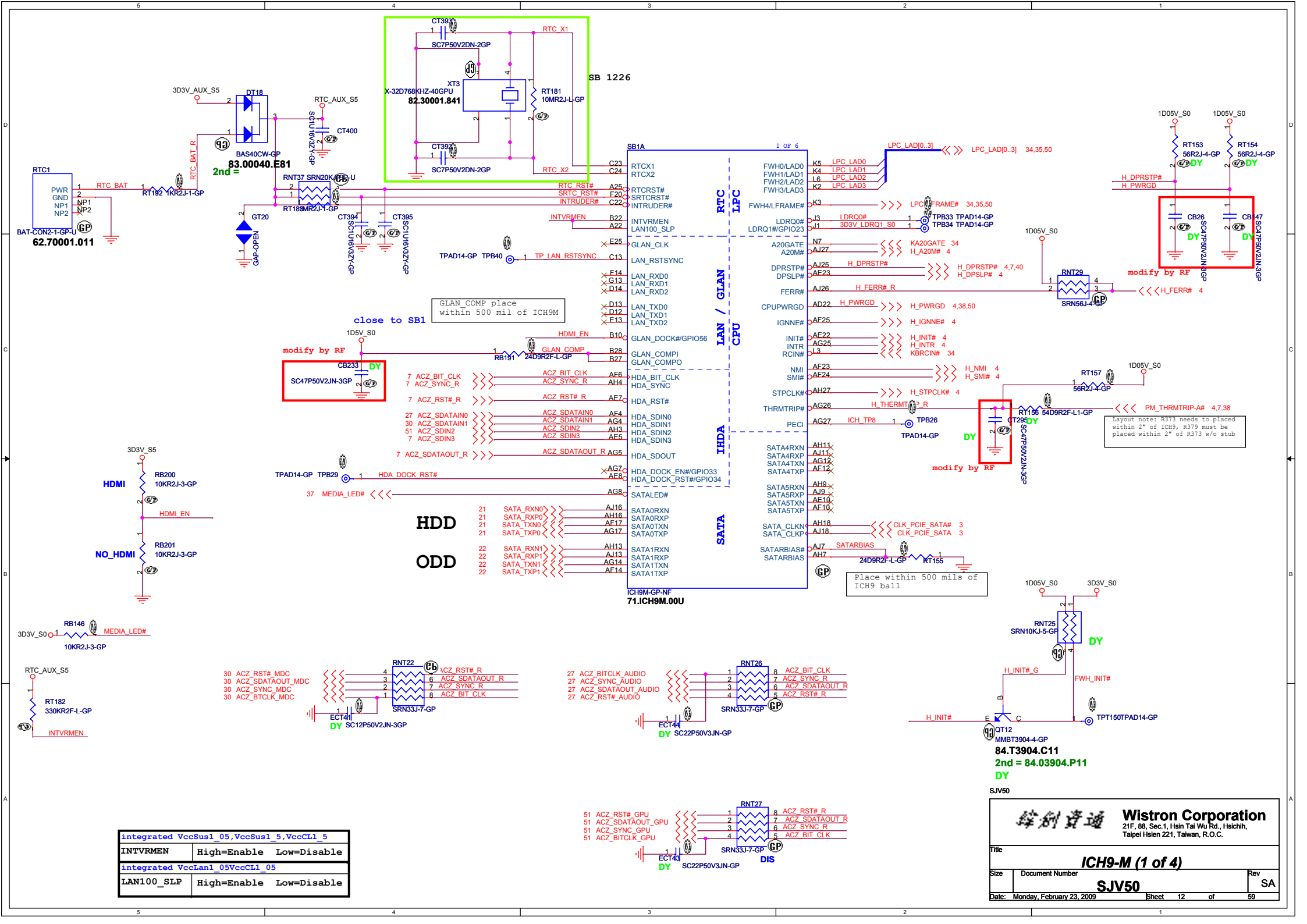
SB 1226
SB1A
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
HDD
ODD
close to SB1
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: R373 needs to placed within 2" of ICH9, R373 must be placed within 2" of R373 w/o stub
modify by RF
DY
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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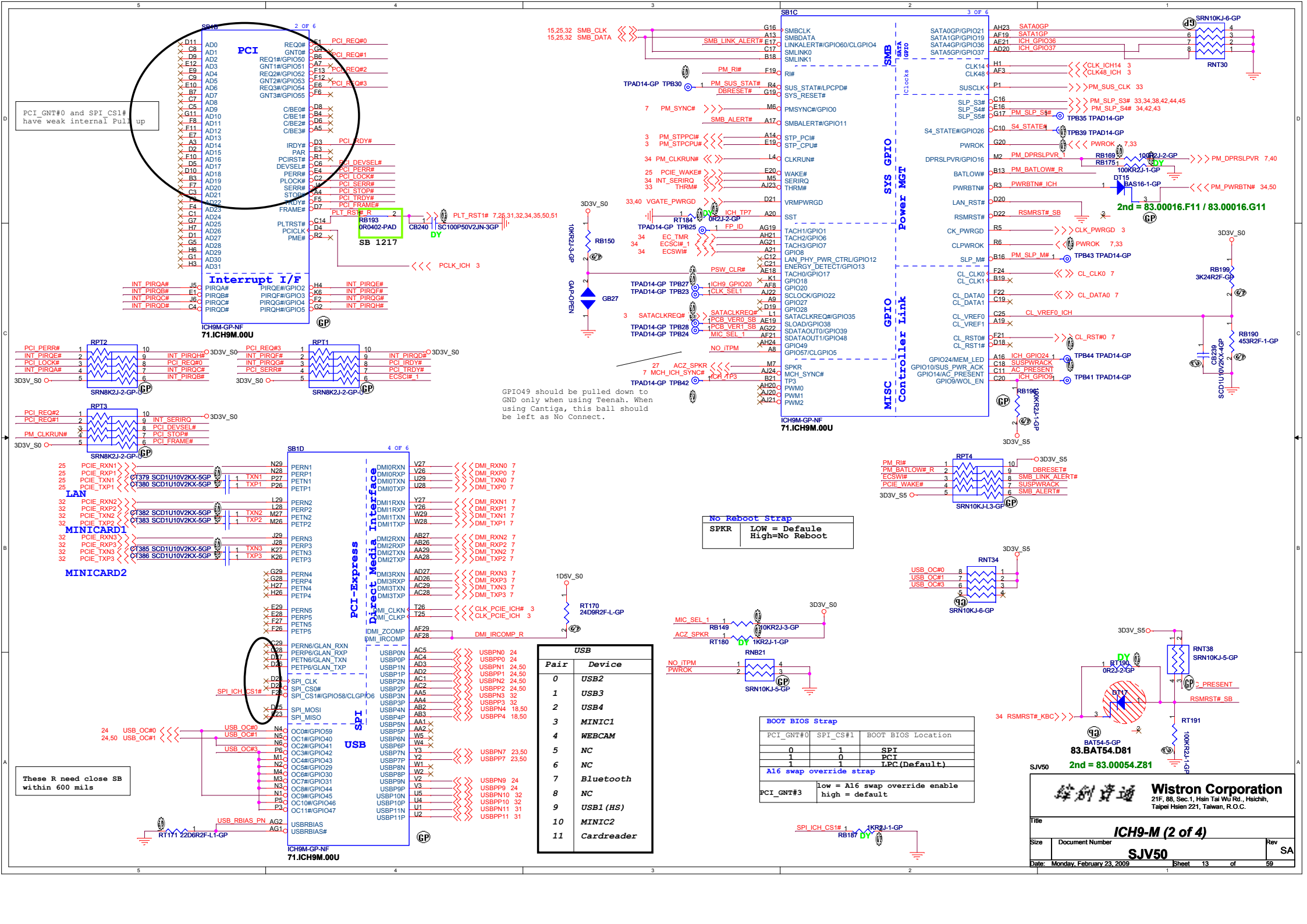
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB 1217
SB1C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD1
MINICARD2
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB2
1
USB3
2
USB4
3
MINIC1
4
WEBCAM
5
NC
6
NC
7
Bluetooth
8
NC
9
USB1(HS)
10
MINIC2
11
Cardreader
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
These R need close SB within 600 mils
2nd = 83.00016.F11 / 83.00016.G11
2nd = 83.00054.Z81
83.BAT54.D81
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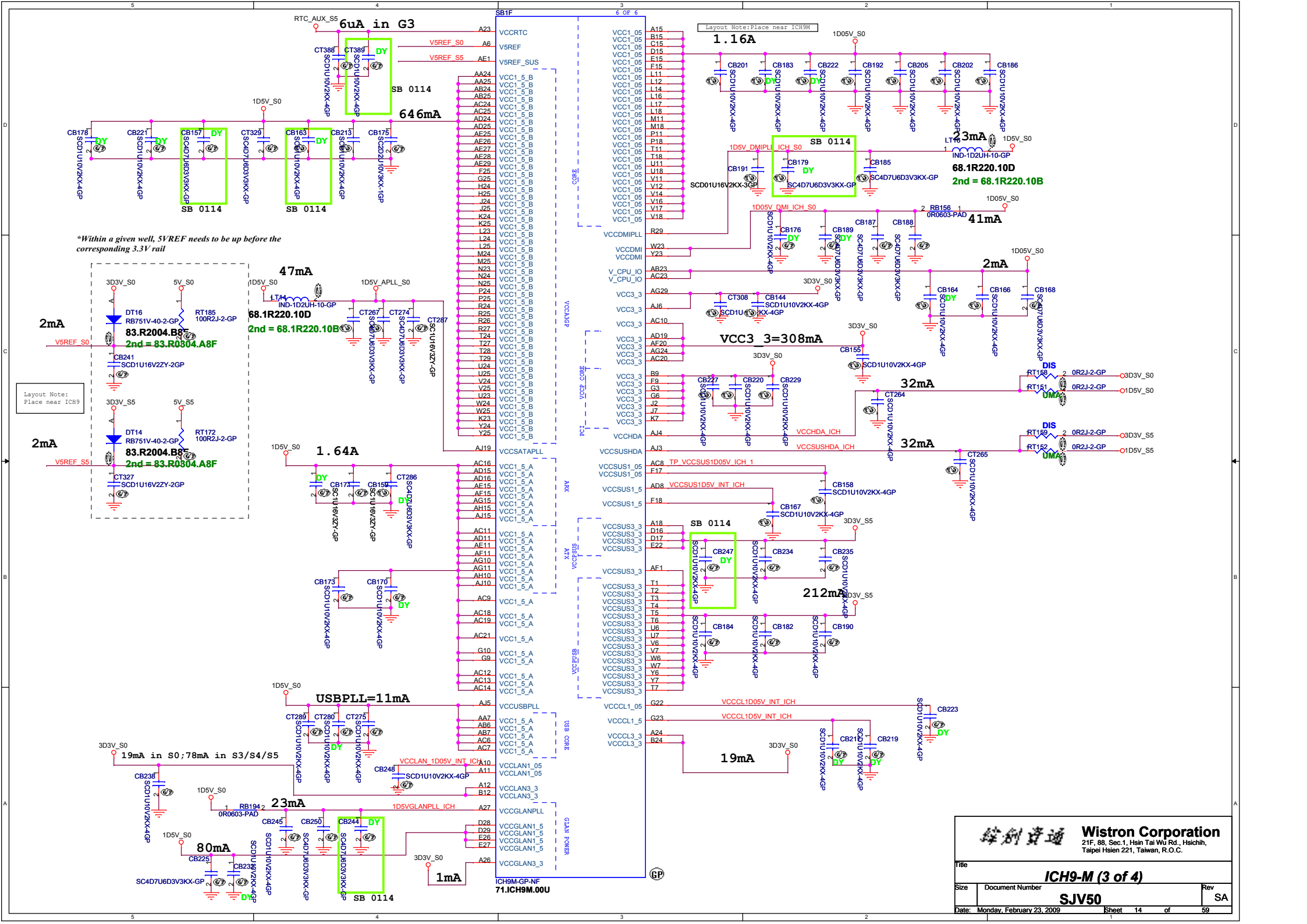
6uA in G3
1.16A
646mA
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
SB 0114
DY
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
68.1R220.10D
2nd = 68.1R220.10B
2nd = 83.R0304.A8F
83.R2004.B8F
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
SJV50
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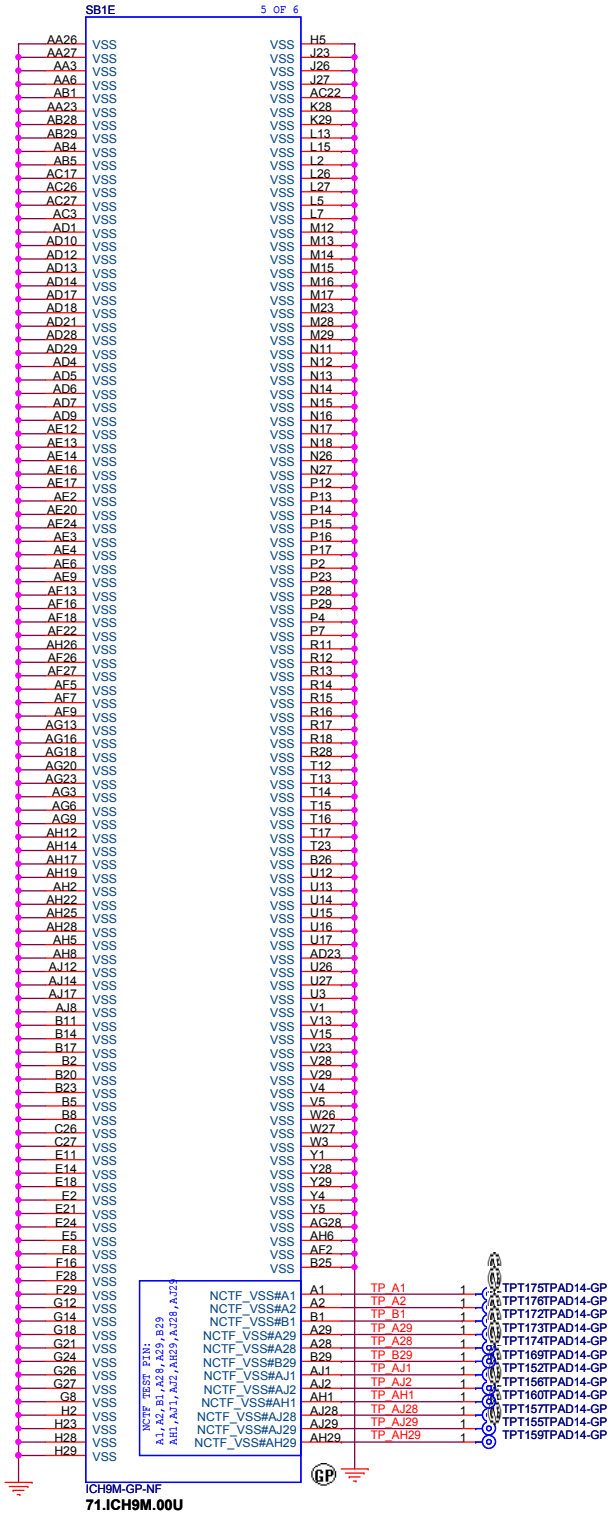

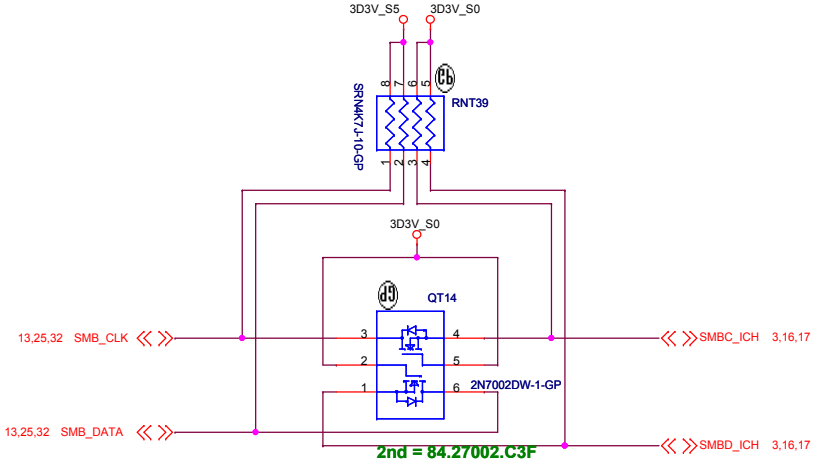

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Title: ICH9-M (4 of 4)		
Size	Document Number: SJV50	Rev: SA
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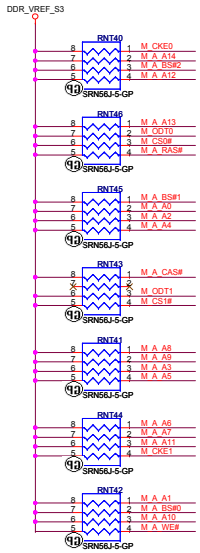
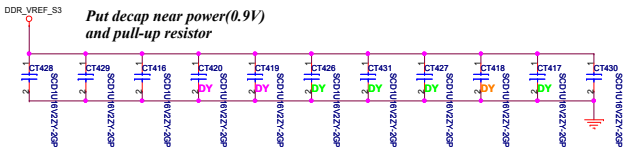
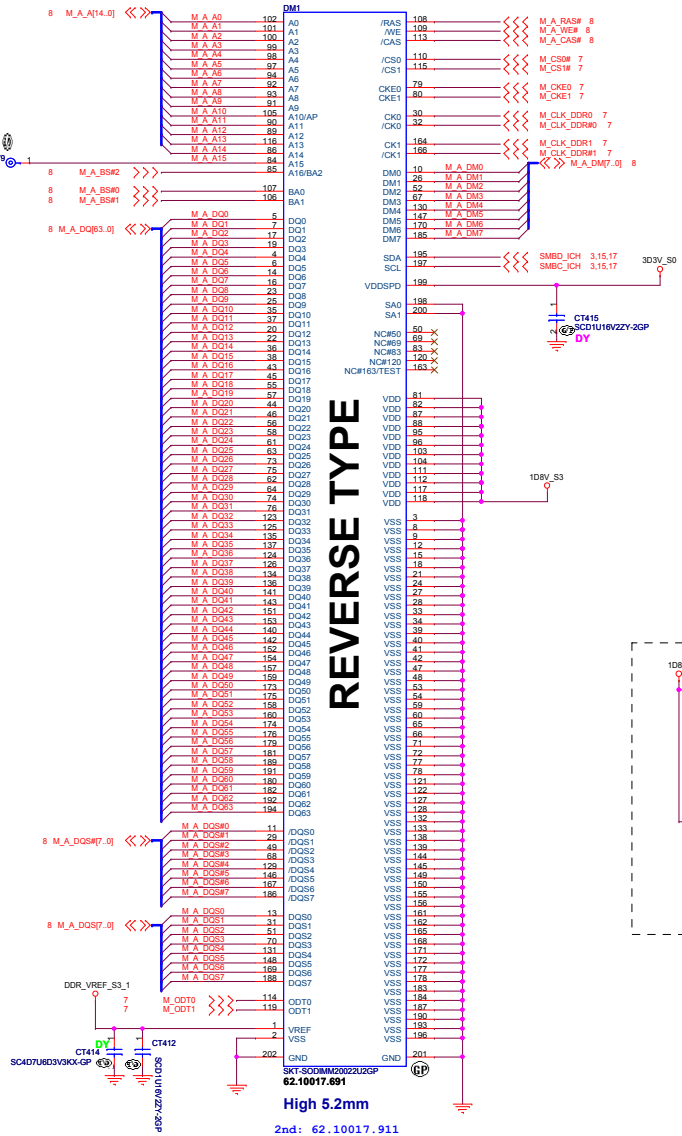
PARALLEL TERMINATION

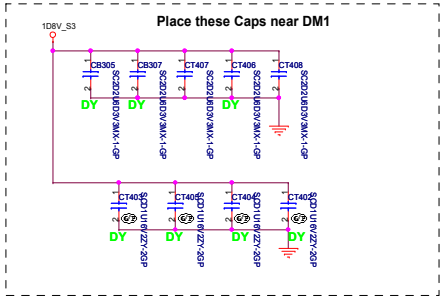
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







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Title: **DDR2 Socket 0 (DM1)**

Size	Document Number	Rev
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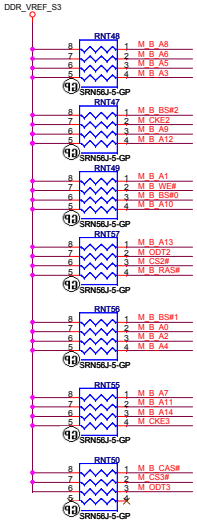
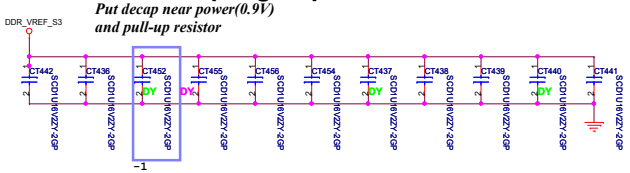
PARALLEL TERMINATION

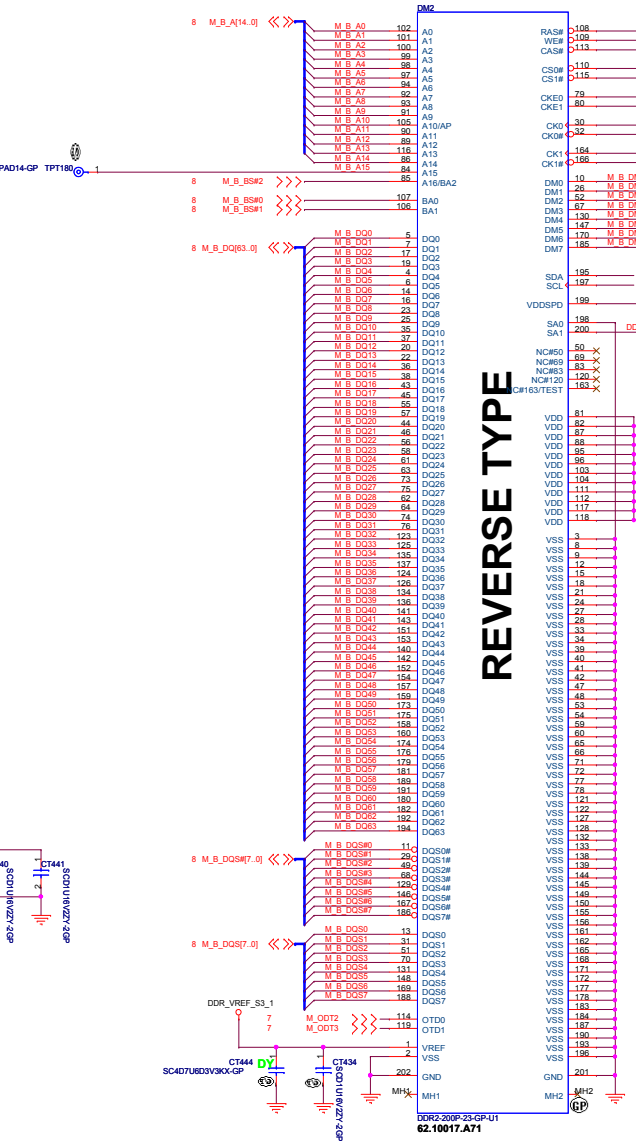
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

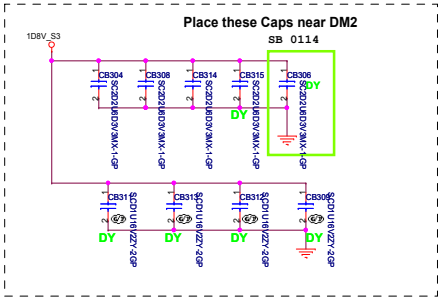
Put decap near power(0.9V) and pull-up resistor





High 9.2mm

2nd: 62.10017.B51



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Title: DDR2 Socket 1 (DM2)

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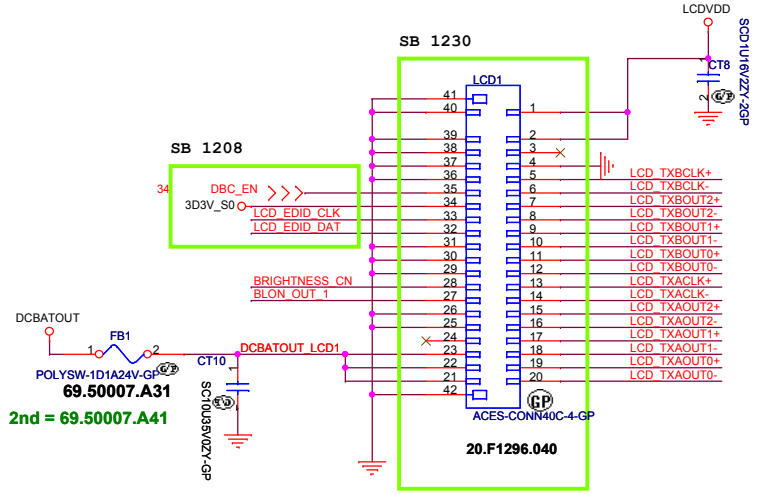
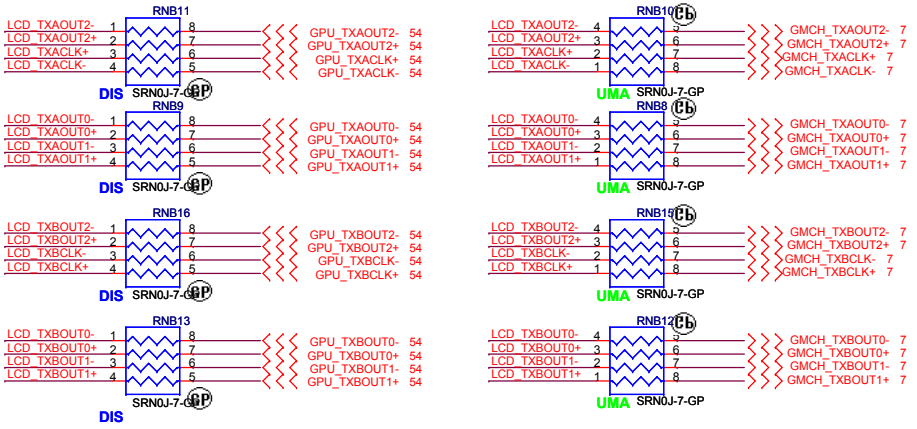
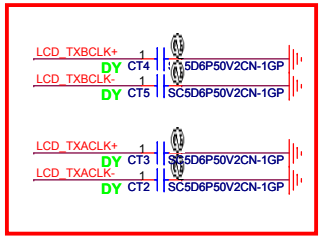
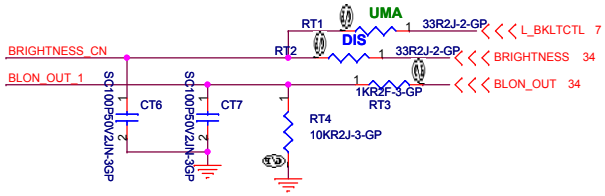
LCD/INVERTER/CCD CONN

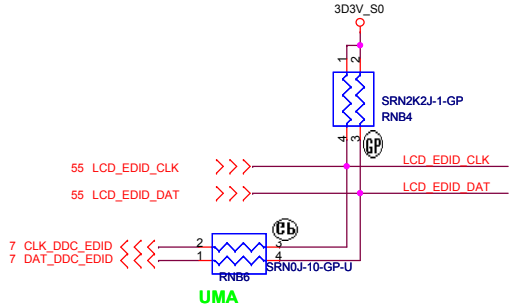




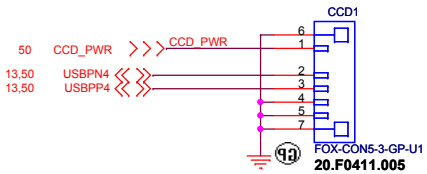


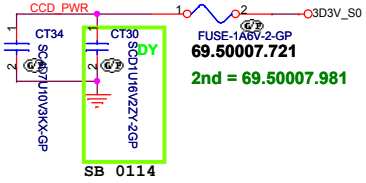
modify by RF

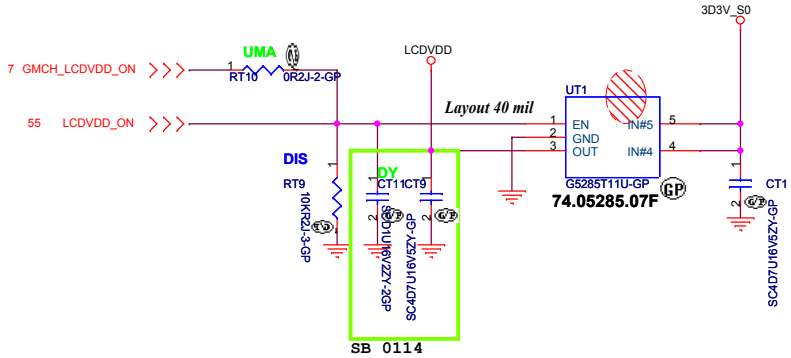




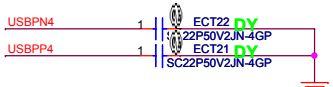
CCD

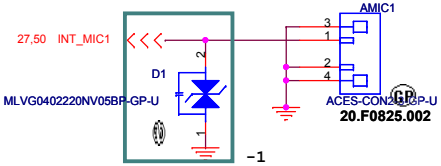






Internal Mic





SJV50

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Title: LCD CONN

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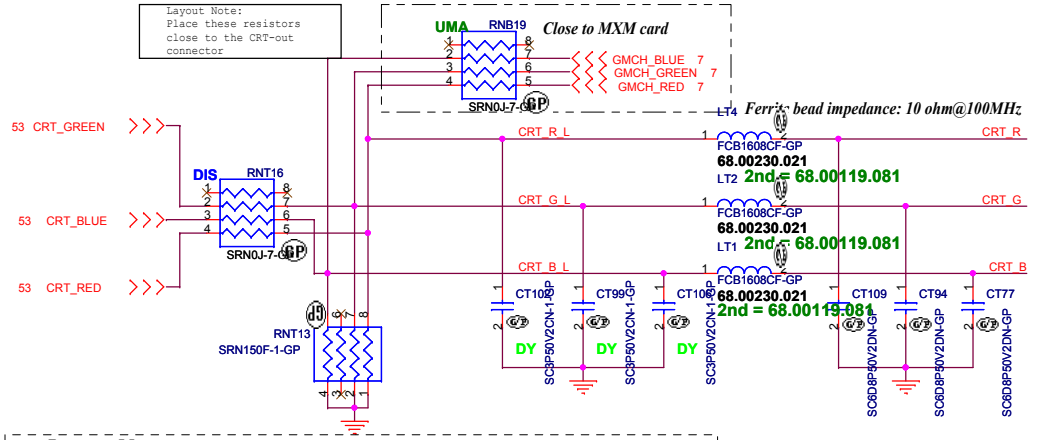
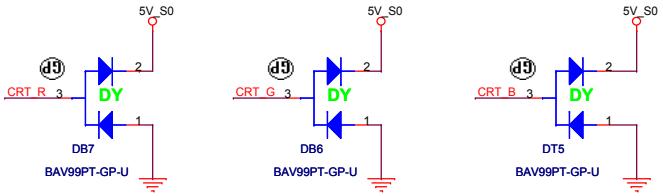
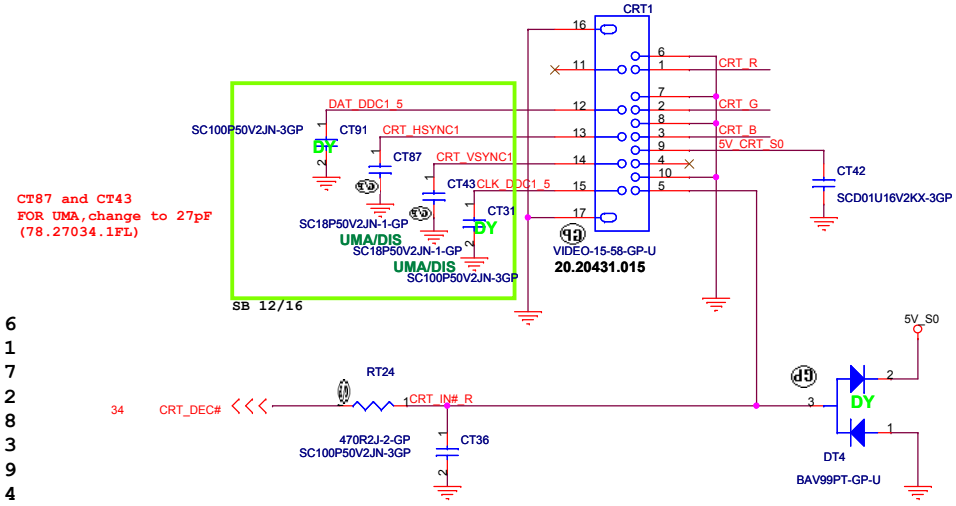
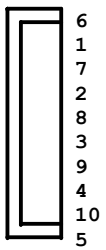


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

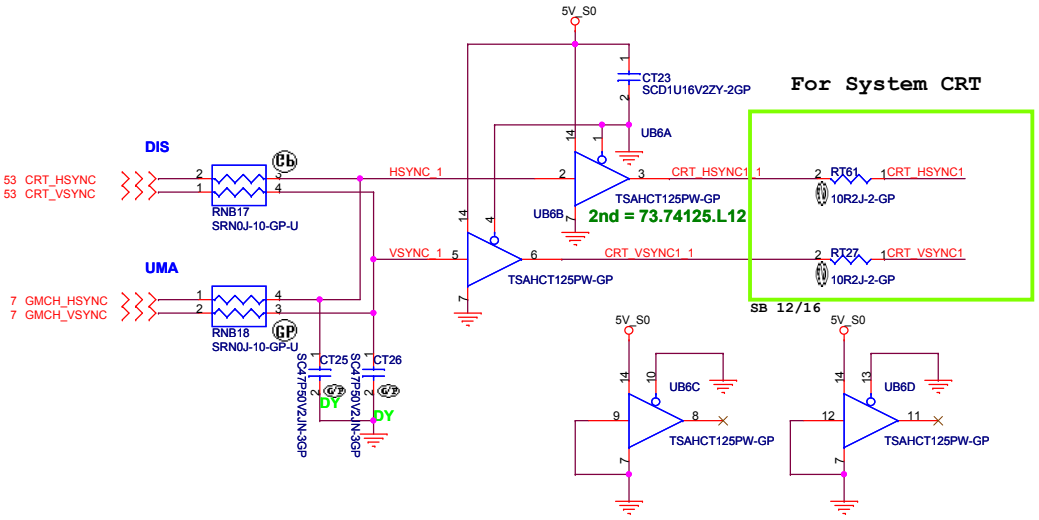


CRT I/F & CONNECTOR

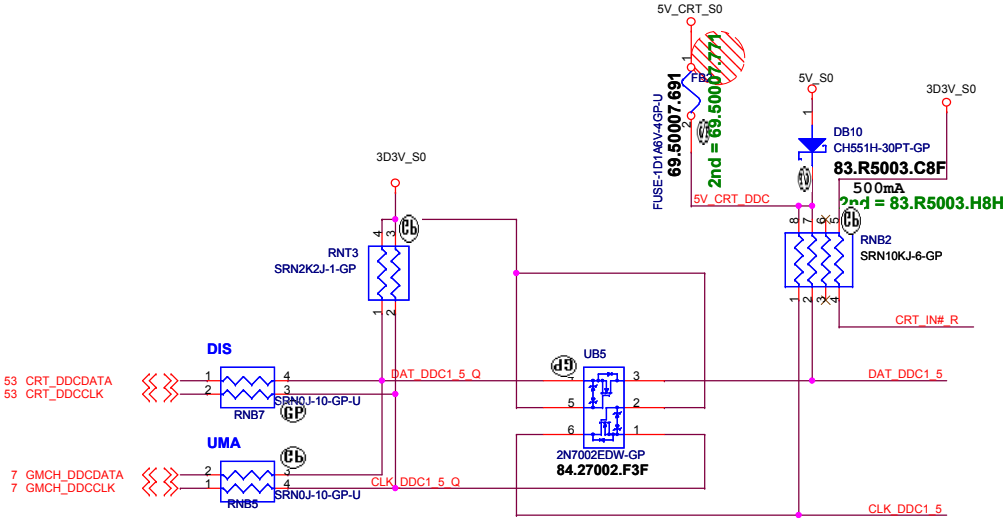




Hsync & Vsync level shift



DDC_CLK & DATA level shift



SJV50

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Title		
CRT CONN		
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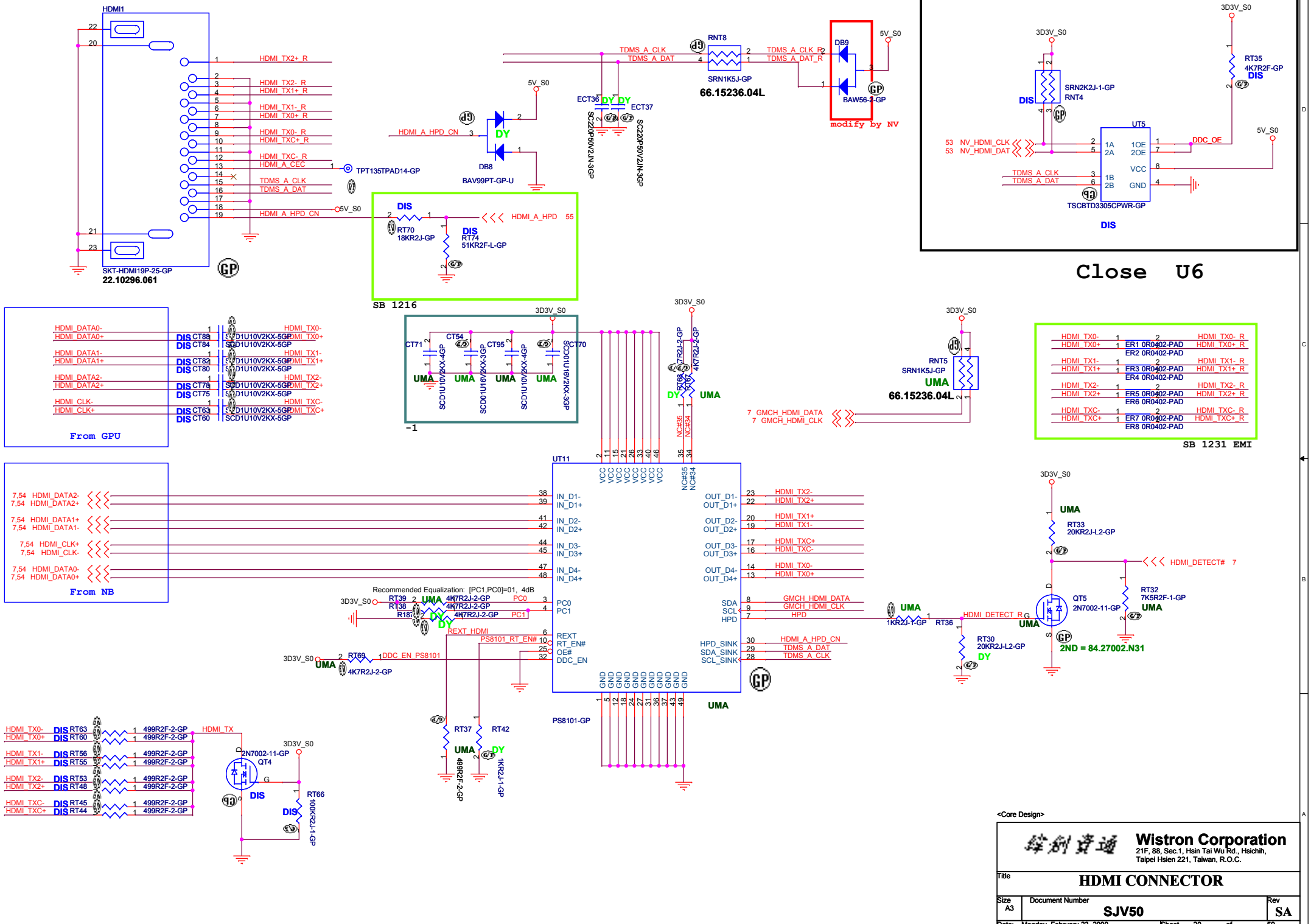
HDMI1
SKT-HDMI19P-25-GP
22.10296.061
TPT135TPAD14-GP
DB8
BAV99PT-GP-U
RNT8
SRN1K5J-GP
66.15236.04L
DB9
BAW56-2-GP
modify by NV
SB 1216
RT70 18KR2J-GP
RT74 51KR2F-L-GP
RNT4
SRN2K2J-1-GP
RT35 4K7R2F-GP
UT5
TSCBTD3305CPWR-GP
Close U6
From GPU
From NB
UT11
PS8101-GP
RNT5
SRN1K5J-GP
66.15236.04L
SB 1231 EMI
RT33 20KR2J-L2-GP
RT32 7K5R2F-1-GP
QT5 2N7002-11-GP
2ND = 84.27002.N31
RT30 20KR2J-L2-GP
RT36
1KR2J-1-GP
RT37
RT42
1KR2J-1-GP
QT4 2N7002-11-GP
RT66 100KR2J-1-GP
RT69 4K7R2J-2-GP
RT39 4K7R2J-2-GP
RT38 4K7R2J-2-GP
RT40 4K7R2J-2-GP
RT63 499R2F-2-GP
RT60 499R2F-2-GP
RT56 499R2F-2-GP
RT55 499R2F-2-GP
RT53 499R2F-2-GP
RT48 499R2F-2-GP
RT45 499R2F-2-GP
RT44 499R2F-2-GP
ER1 0R0402-PAD
ER2 0R0402-PAD
ER3 0R0402-PAD
ER4 0R0402-PAD
ER5 0R0402-PAD
ER6 0R0402-PAD
ER7 0R0402-PAD
ER8 0R0402-PAD
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size A3
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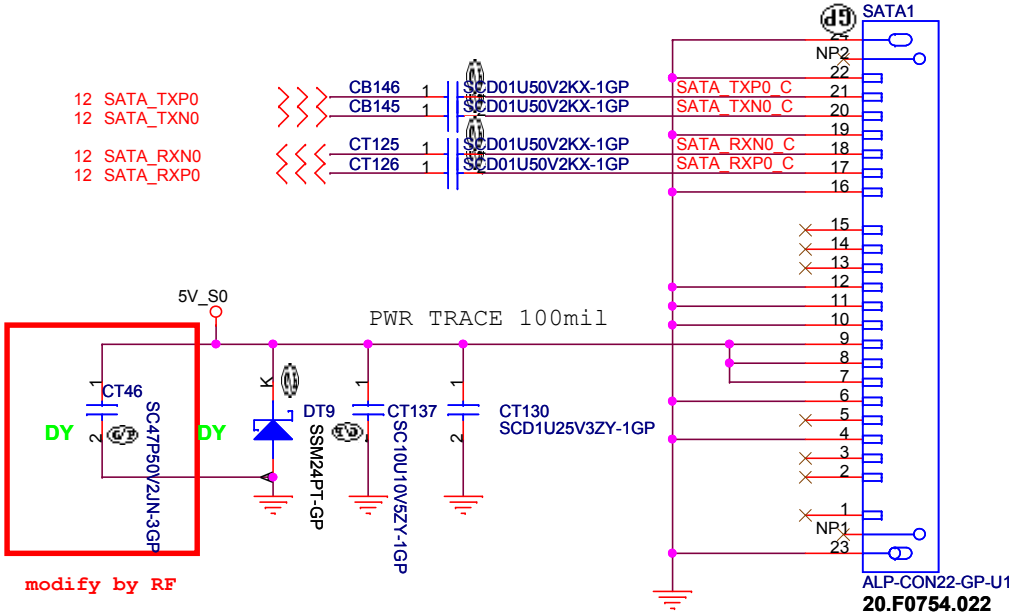
SATA Connector



SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD CONN		
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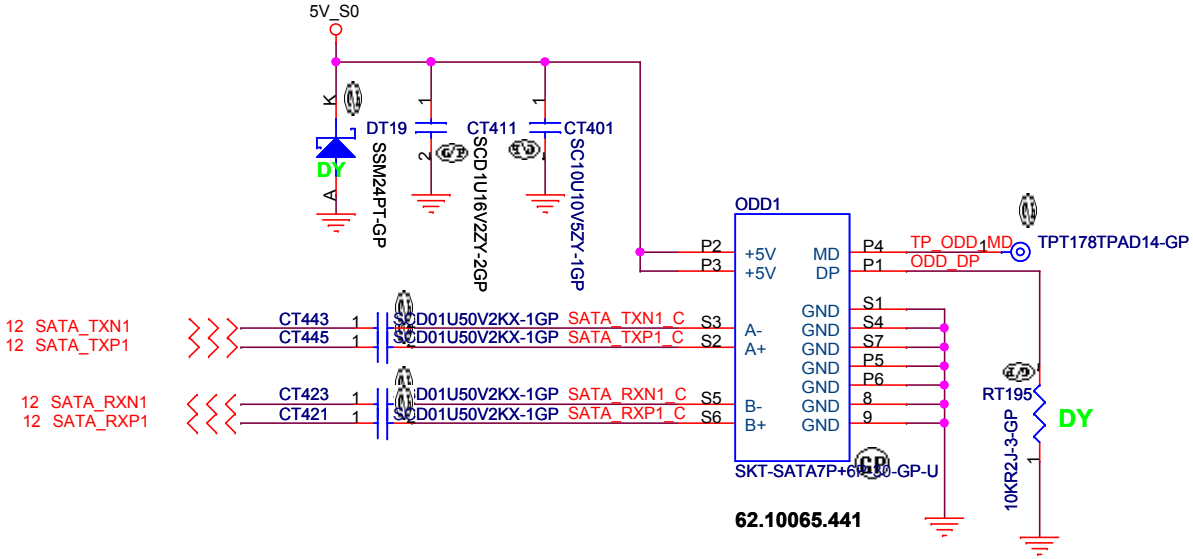
ODD Connector



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Title			
ODD			
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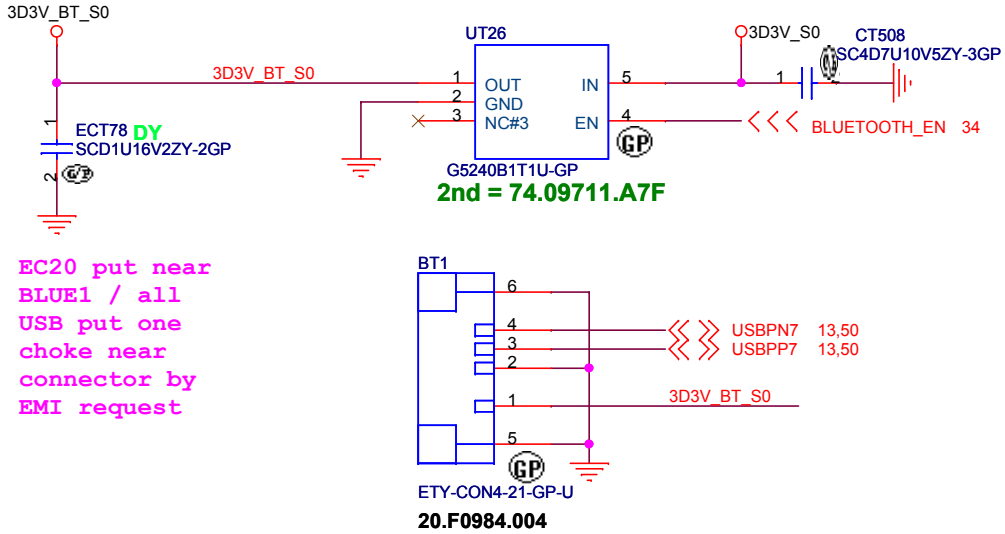
BLUETOOTH MODULE



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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH

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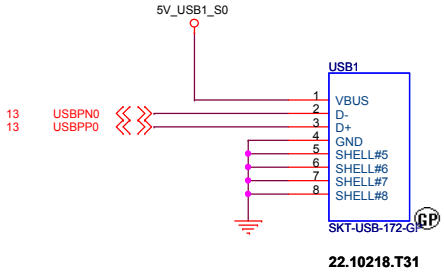

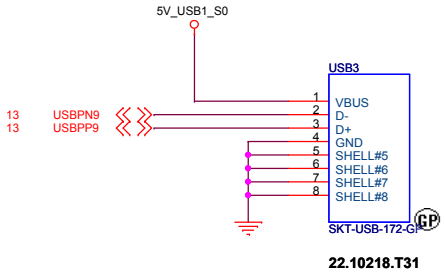

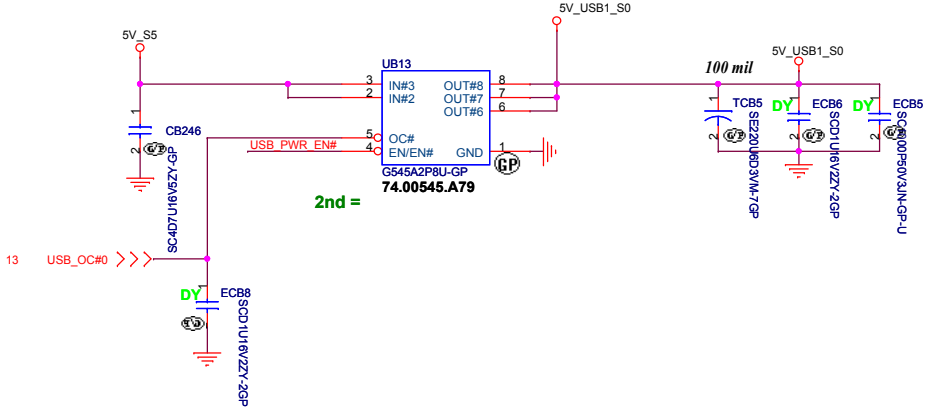

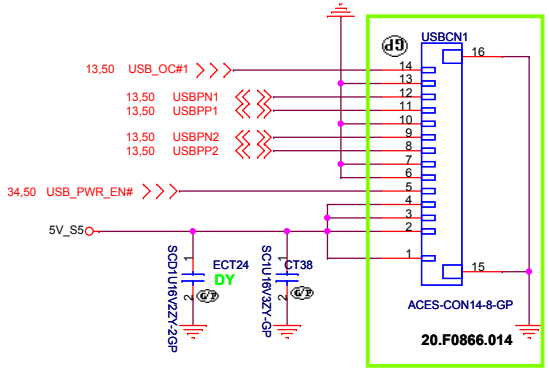

SB 1230

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB CONN*	
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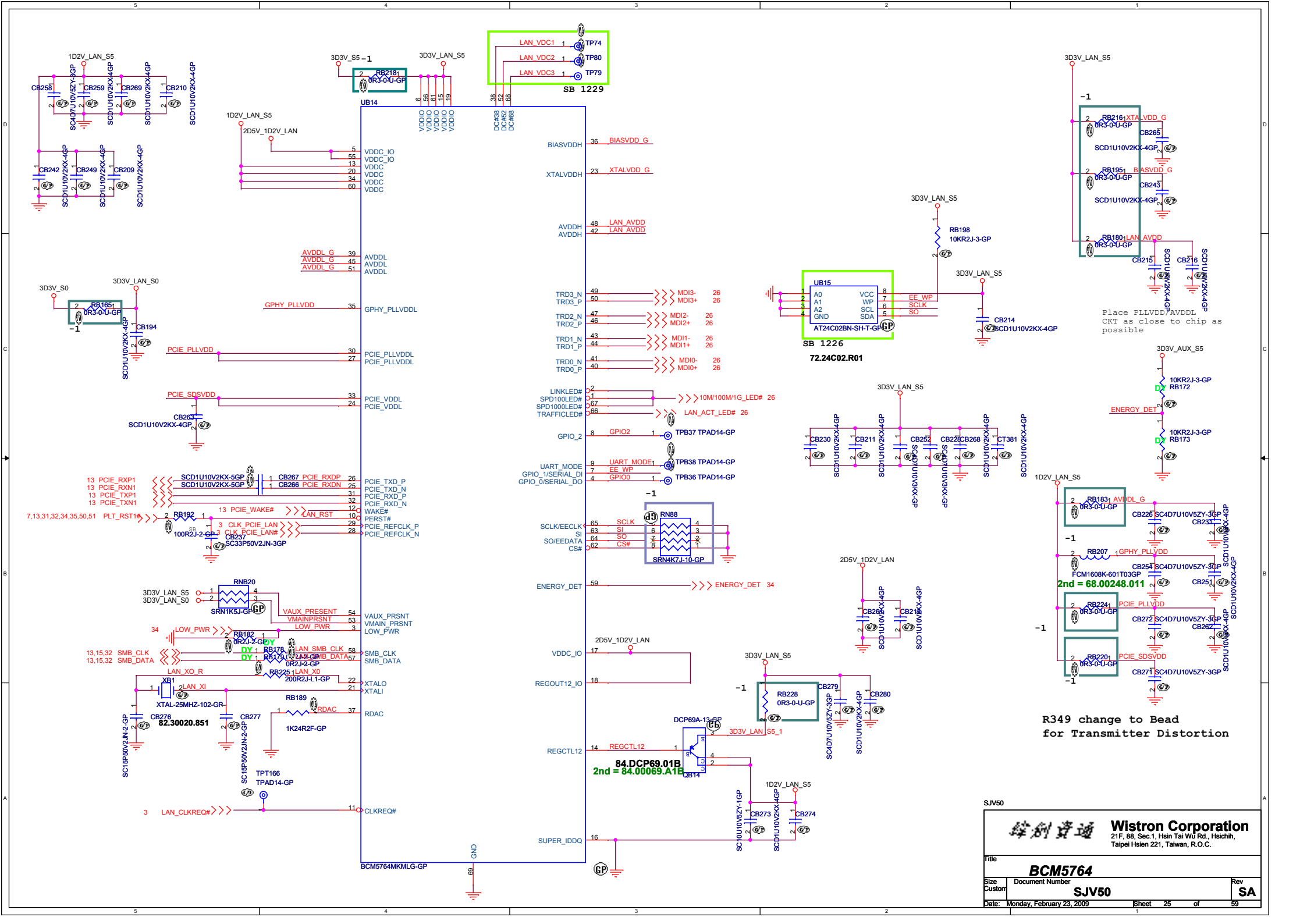
UB14
BCM5764MKMLG-GP
SB 1229
LAN_VDC1
LAN_VDC2
LAN_VDC3
TP74
TP80
TP79
UB15
AT24C02BN-SH-T-GP
SB 1226
72.24C02.R01
Place PLLVDD/AVDDL CKT as close to chip as possible
2nd = 68.00248.011
2nd = 84.00069.A1B
84.DCP69.01B
82.30020.851
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
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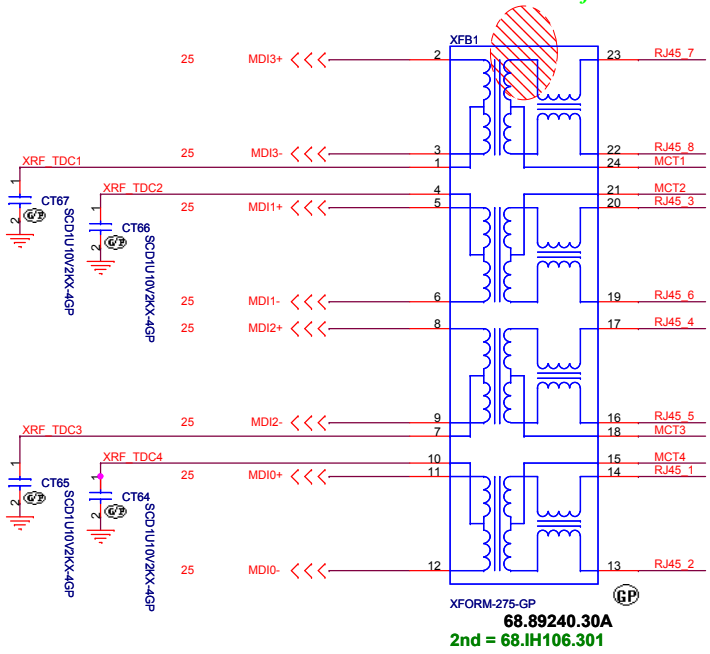
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

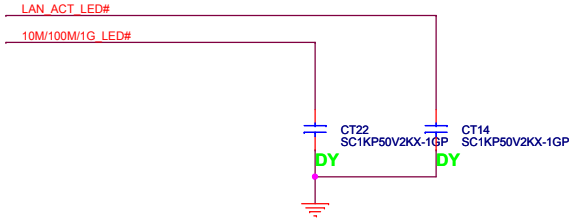
LAN Connector

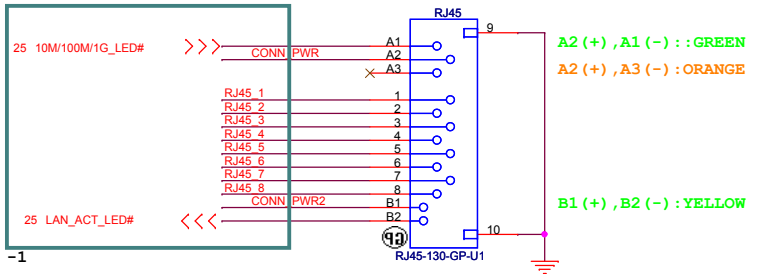
LAN Connector

GIGA Lan Transformer

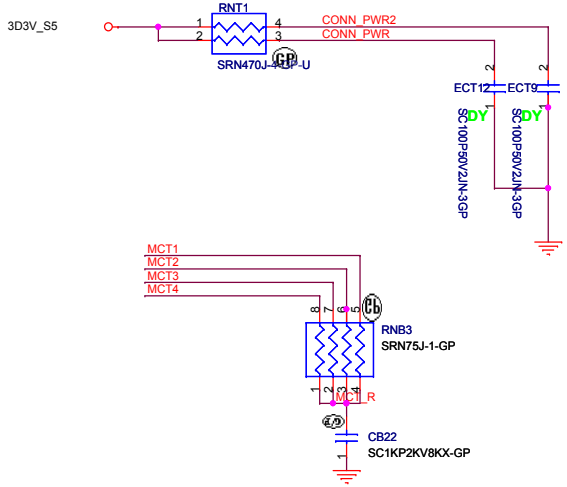


68.89240.30A
2nd = 68.IH106.301





22.10277.041



SJV50

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

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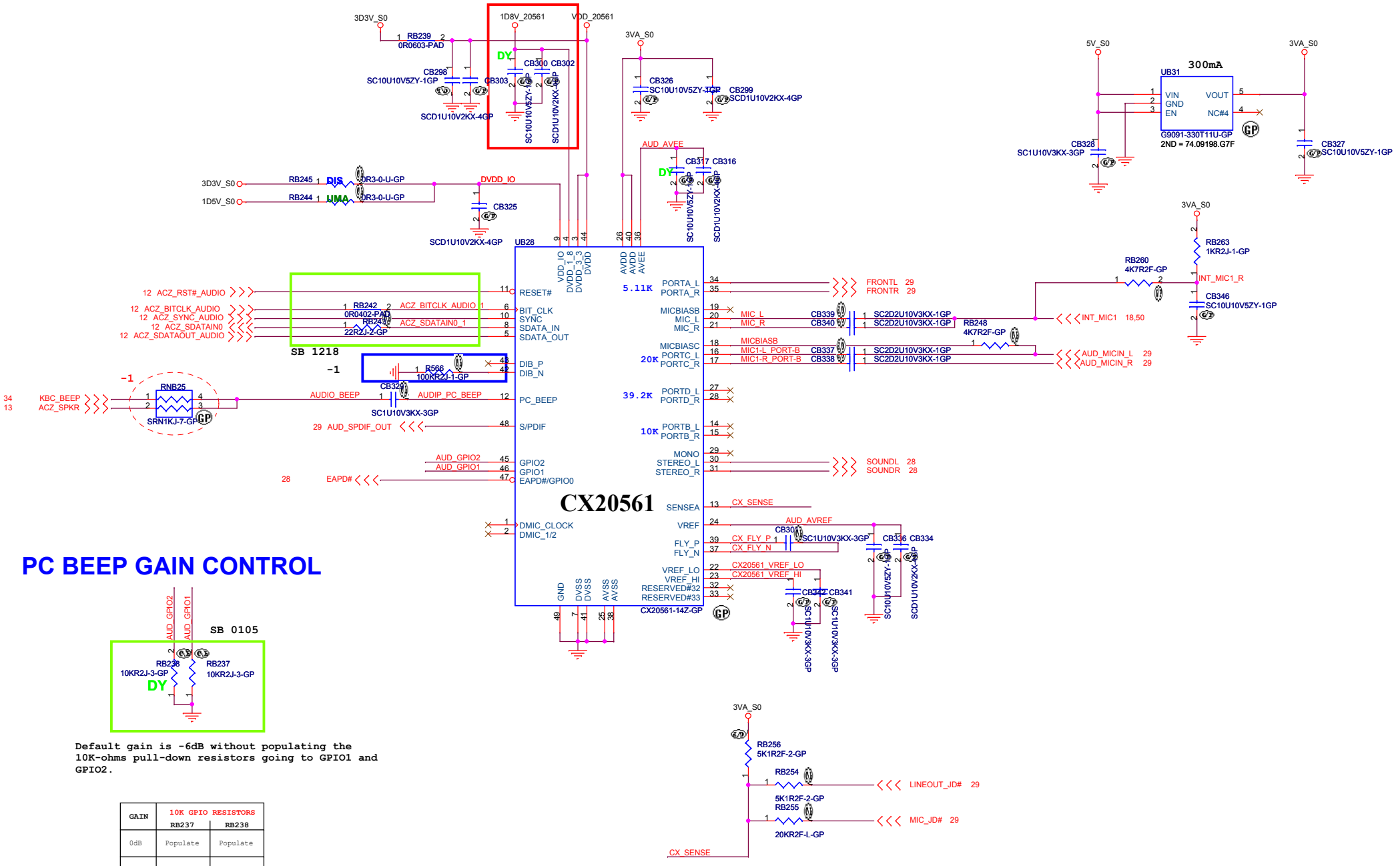
CX20561
UB28
CX20561-14Z-GP
PC BEEP GAIN CONTROL
SB 1218
SB 0105
-1
DY
Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.
GAIN
10K GPIO RESISTORS
RB237
RB238
0dB Populate Populate
-6dB Omit Omit
-12dB Populate Omit
-18dB Omit Populate
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec CX20561
Size A3
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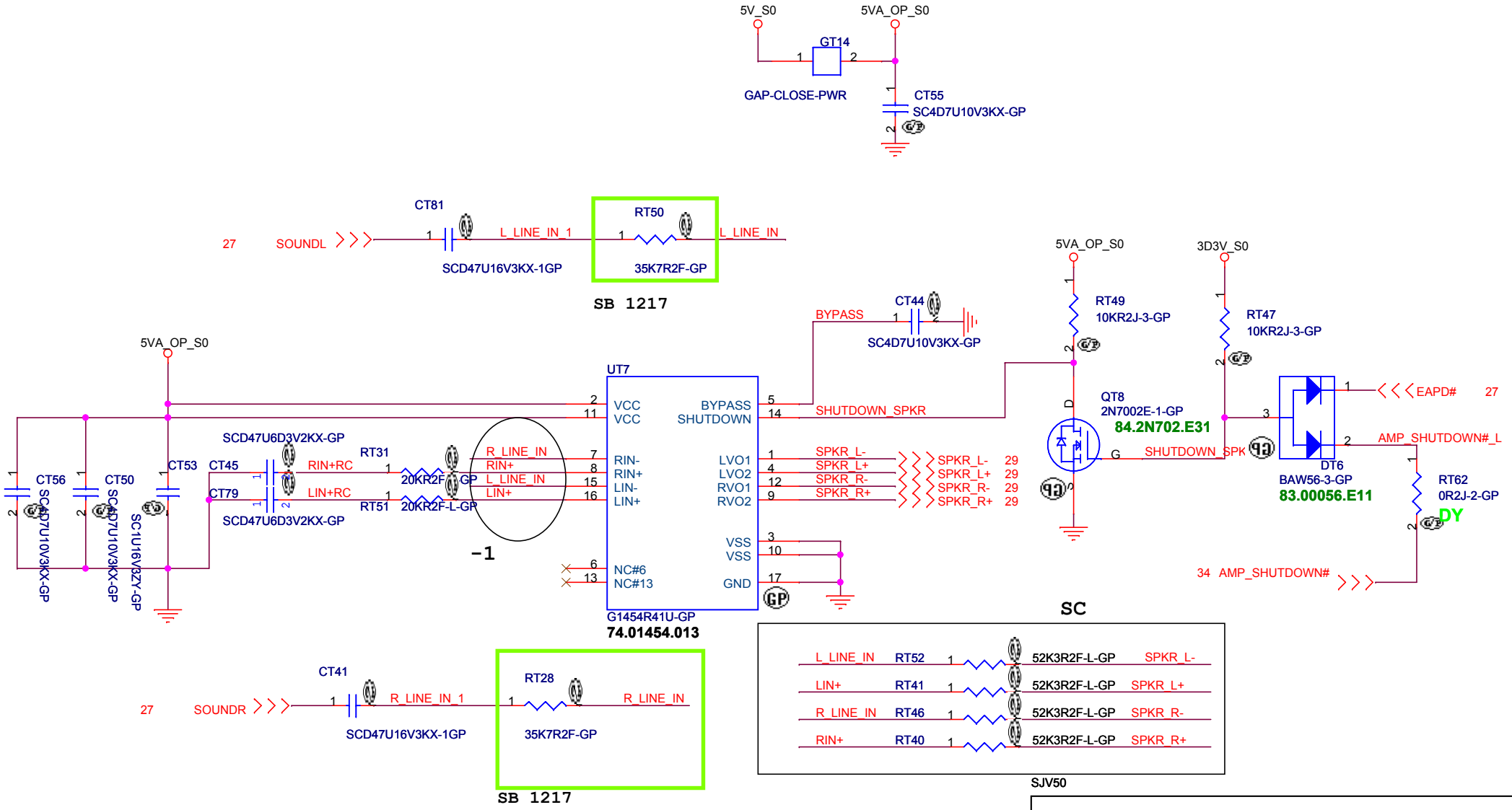
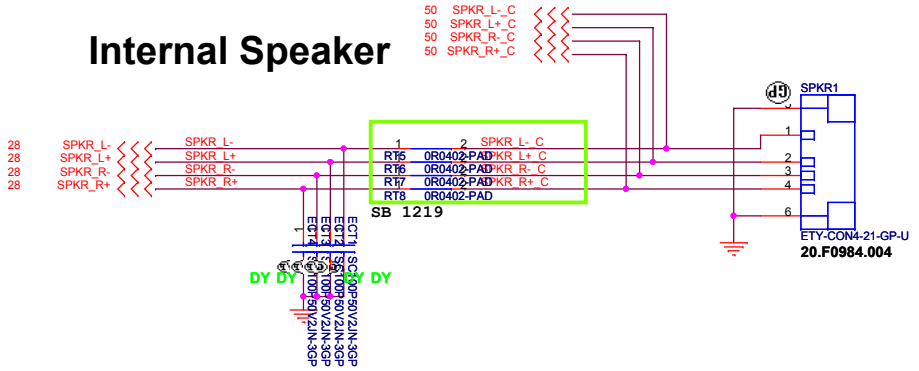
AUDIO OP AMPLIFIER

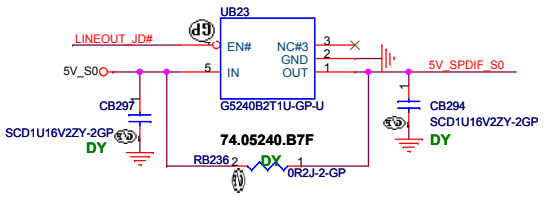


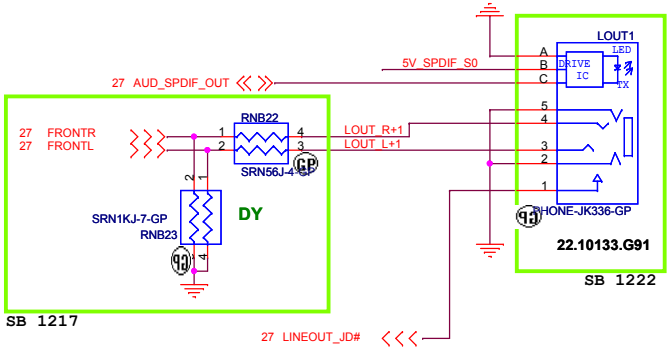
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO AMP AND JACK*	
Size	Document Number SJV50	Rev SA
Date: Monday, February 23, 2009	Sheet 28 of 59	

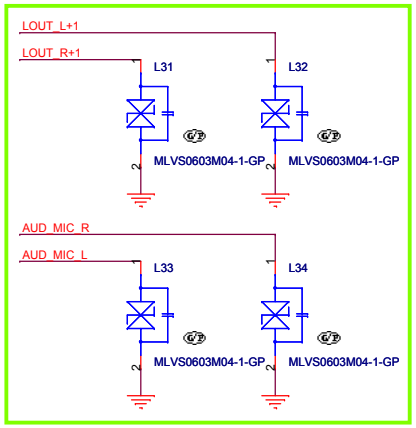
Internal Speaker



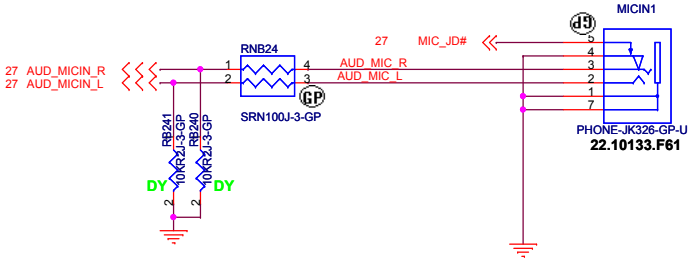
LINE OUT

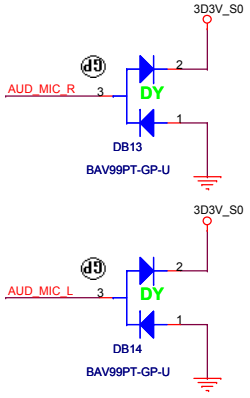






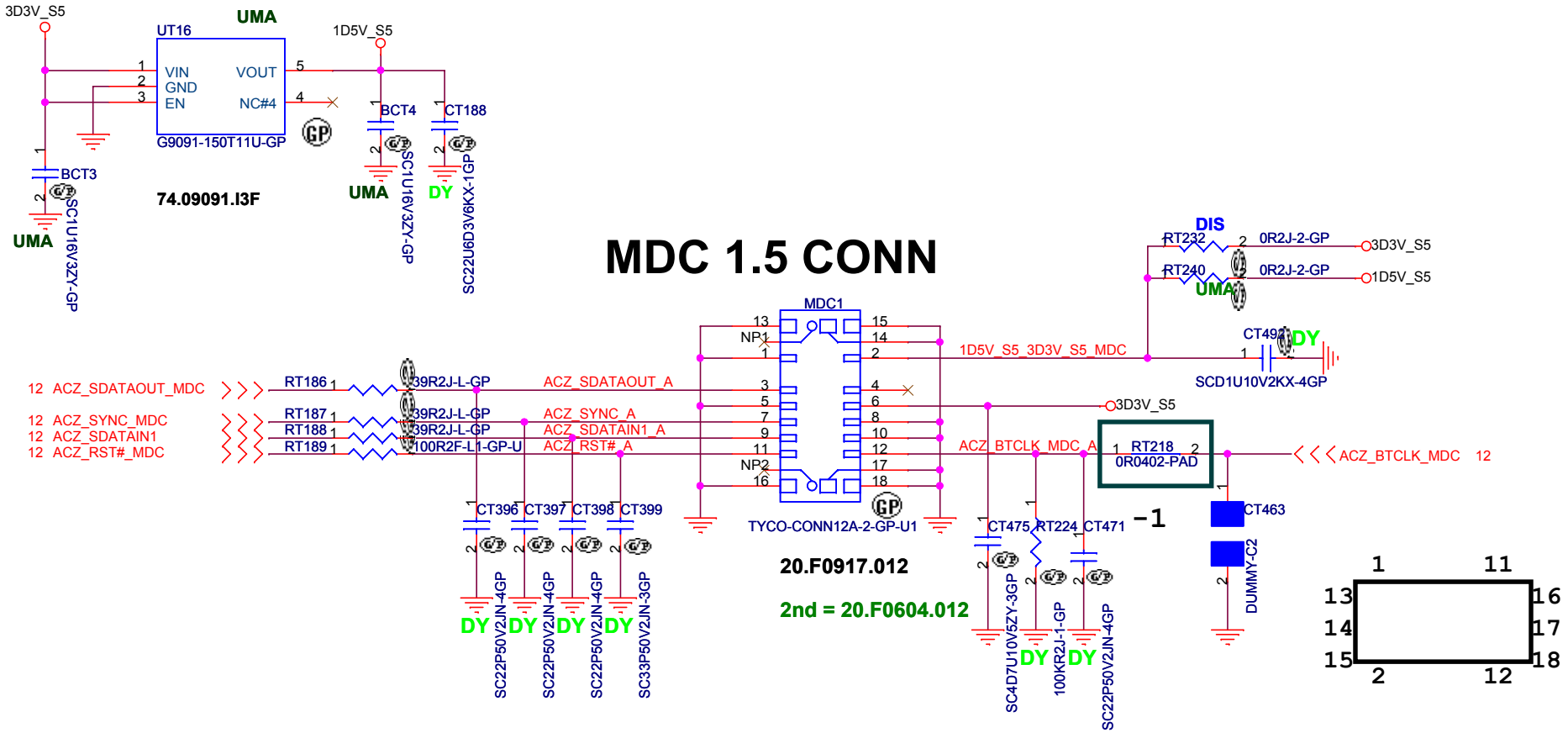
MIC IN





SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO jack*		
Size	Document Number: SJV50	Rev: SA
Date: Monday, February 23, 2009	Sheet 29 of 59	



SJV50

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC

Size	Document Number	Rev
	SJV50	SA

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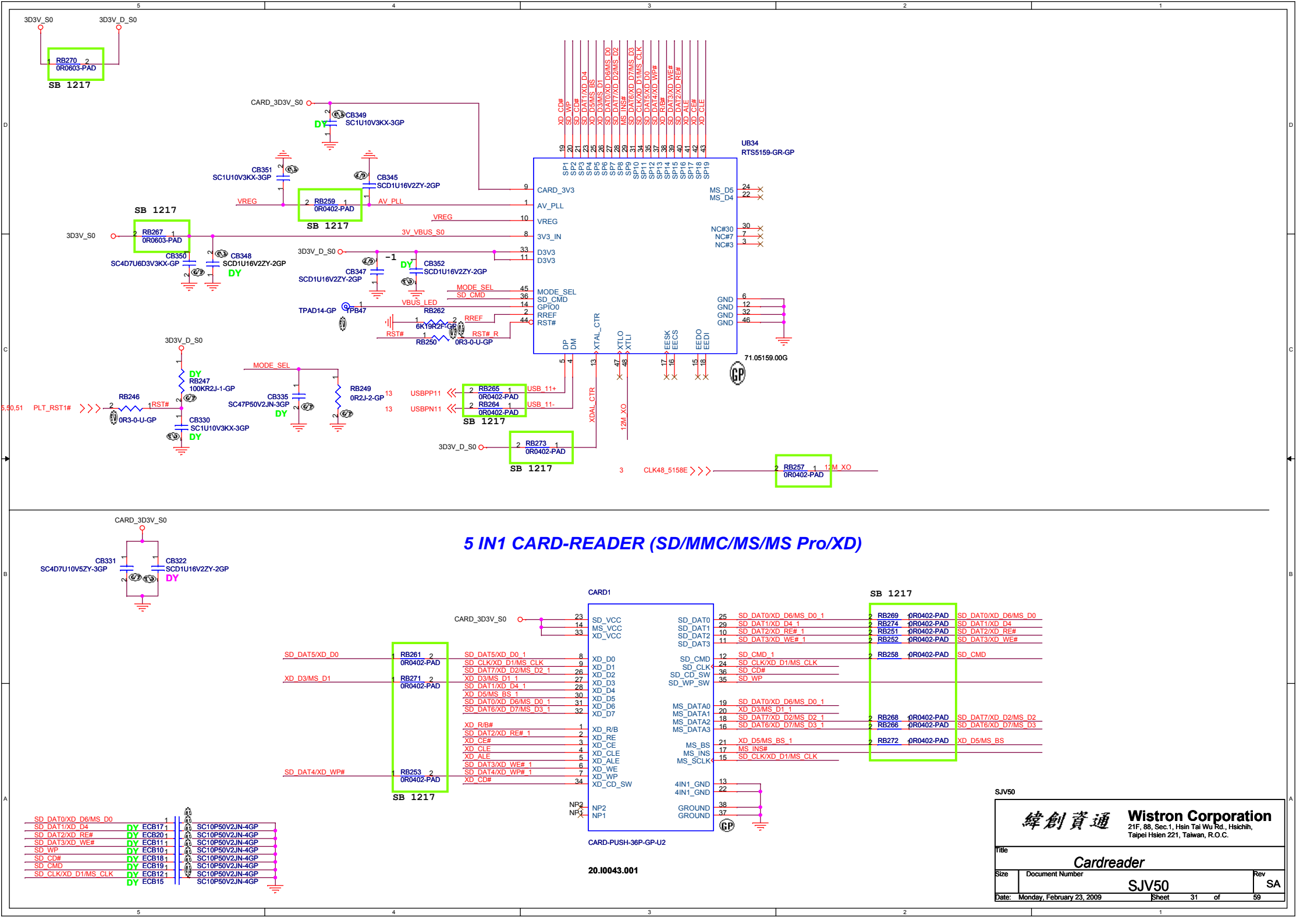
5 IN1 CARD-READER (SD/MMC/MS/MS Pro/XD)
UB34
RTS5159-GR-GP
CARD1
CARD-PUSH-36P-GP-U2
SB 1217
20.I0043.001
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cardreader
SJV50
Monday, February 23, 2009
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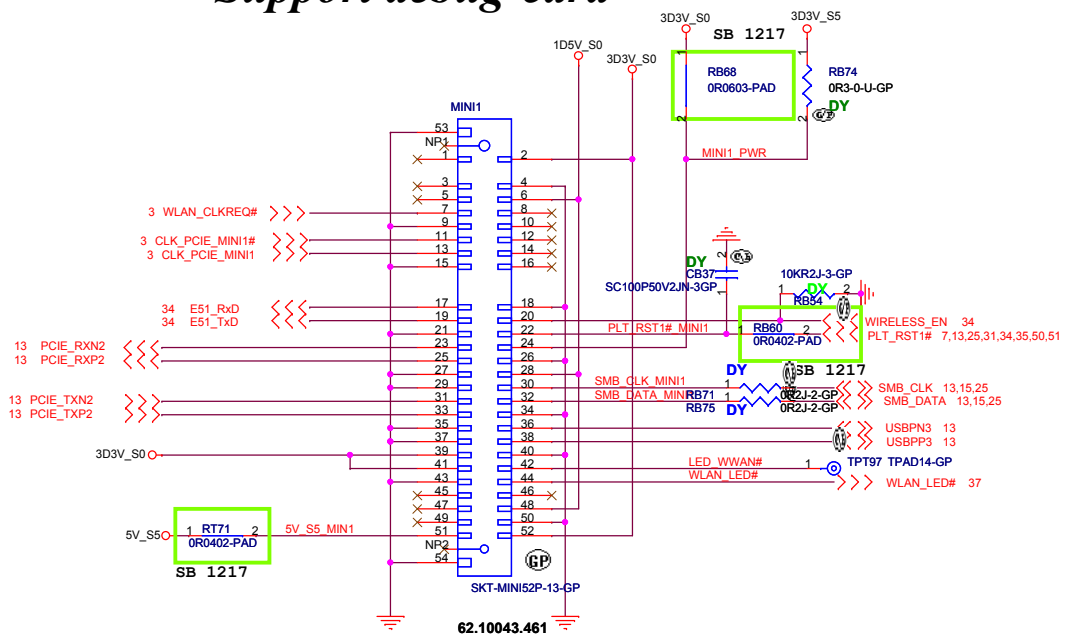
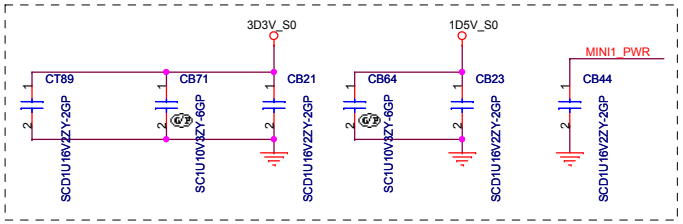
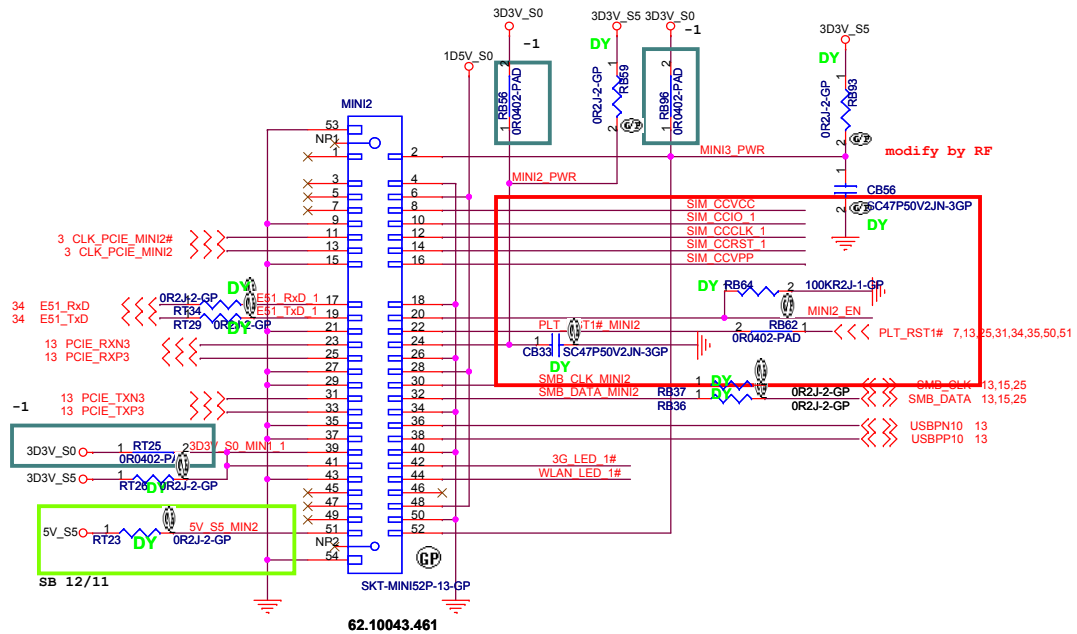
Mini Card Connector(WLAN) Half Card
Support debug-card

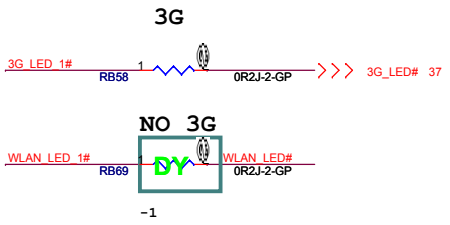


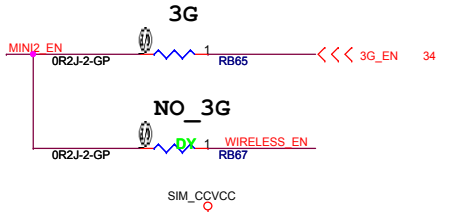
Place near MINI1



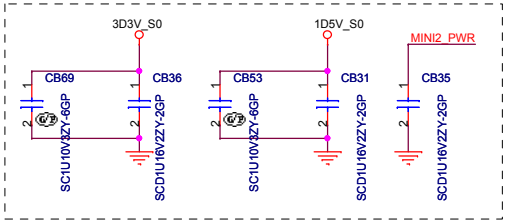
Mini Card Connector(Robson2 and 3G)

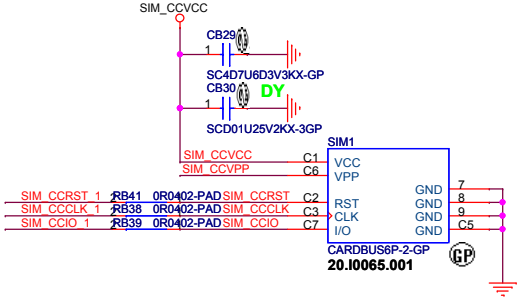






Place near MINIC2





SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD	
Size A3	Document Number SJV50	Rev SA
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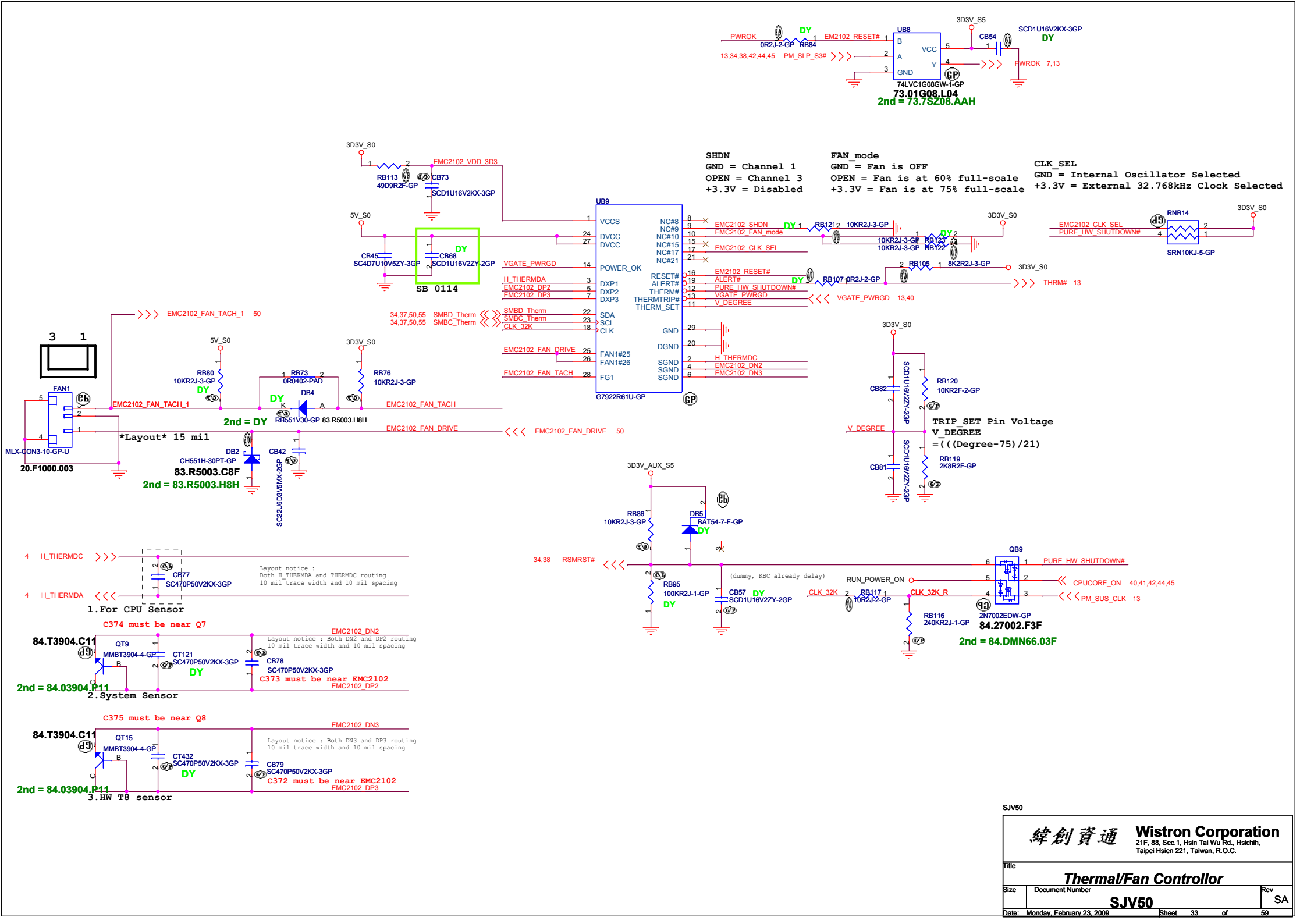
PWROK
0R2J-2-GP
RB84
DY
EM2102_RESET#
UB8
74LVC1G08GW-1-GP
73.01G08.L04
2nd = 73.7SZ08.AAH
3D3V_S5
CB54
SCD1U16V2KX-3GP
PWROK 7,13
13,34,38,42,44,45 PM_SLP_S3#
SHDN
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
FAN_mode
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
CLK_SEL
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
3D3V_S0
RB113
49D9R2F-GP
CB73
SCD1U16V2KX-3GP
EMC2102_VDD_3D3
5V_S0
CB45
SC4D7U10V5ZY-3GP
CB68
SCD1U16V2ZY-2GP
SB 0114
UB9
G7922R61U-GP
VCCS
DVCC
DVCC
POWER_OK
DXP1
DXP2
DXP3
THERMTRIP#
THERM_SET
SDA
SCL
CLK
FAN1#25
FAN1#26
FG1
NC#8
NC#9
NC#10
NC#15
NC#17
NC#21
RESET#
ALERT#
THERM#
GND
DGND
SGND
SGND
SGND
VGATE_PWRGD
H_THERMDA
EMC2102_DP2
EMC2102_DP3
SMBD_Therm
SMBC_Therm
CLK_32K
EMC2102_FAN_DRIVE
EMC2102_FAN_TACH
EMC2102_SHDN
EMC2102_FAN_mode
EMC2102_CLK_SEL
EMC2102_RESET#
ALERT#
PURE_HW_SHUTDOWN#
V_DEGREE
H_THERMDC
EMC2102_DN2
EMC2102_DN3
RB121
10KR2J-3-GP
RB123
RB122
RB107
0R2J-2-GP
RB105
8K2R2J-3-GP
THRM# 13
VGATE_PWRGD 13,40
RNB14
SRN10KJ-5-GP
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
34,37,50,55 SMBD_Therm
34,37,50,55 SMBC_Therm
EMC2102_FAN_TACH_1 50
FAN1
MLX-CON3-10-GP-U
20.F1000.003
RB80
10KR2J-3-GP
RB73
0R0402-PAD
RB76
10KR2J-3-GP
DB4
RB551V30-GP 83.R5003.H8H
2nd = DY
Layout 15 mil
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE 50
DB2
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
CB42
SC22U6D3V5MX-2GP
3D3V_S0
CB82
SCD1U16V2ZY-2GP
RB120
10KR2F-2-GP
V_DEGREE
CB81
SCD1U16V2ZY-2GP
RB119
2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
3D3V_AUX_S5
RB86
10KR2J-3-GP
DB5
BAT54-7-F-GP
DY
34,38 RSMRST#
RB95
100KR2J-1-GP
CB57
SCD1U16V2ZY-2GP
(dummy, KBC already delay)
RUN_POWER_ON
CLK_32K
CLK_32K_R
RB117
10KR2J-2-GP
RB116
240KR2J-1-GP
QB9
2N7002EDW-GP
84.27002.F3F
2nd = 84.DMN66.03F
PURE_HW_SHUTDOWN#
CPUCORE_ON 40,41,42,44,45
PM_SUS_CLK 13
4 H_THERMDC
4 H_THERMDA
CB77
SC470P50V2KX-3GP
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
C374 must be near Q7
84.T3904.C11
QT9
MMBT3904-4-GP
CT121
SC470P50V2KX-3GP
CB78
SC470P50V2KX-3GP
C373 must be near EMC2102
EMC2102_DP2
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
2nd = 84.03904.P11
2.System Sensor
C375 must be near Q8
84.T3904.C11
QT15
MMBT3904-4-GP
CT432
SC470P50V2KX-3GP
CB79
SC470P50V2KX-3GP
C372 must be near EMC2102
EMC2102_DP3
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
2nd = 84.03904.P11
3.HW T8 sensor
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
SJV50
Rev
SA
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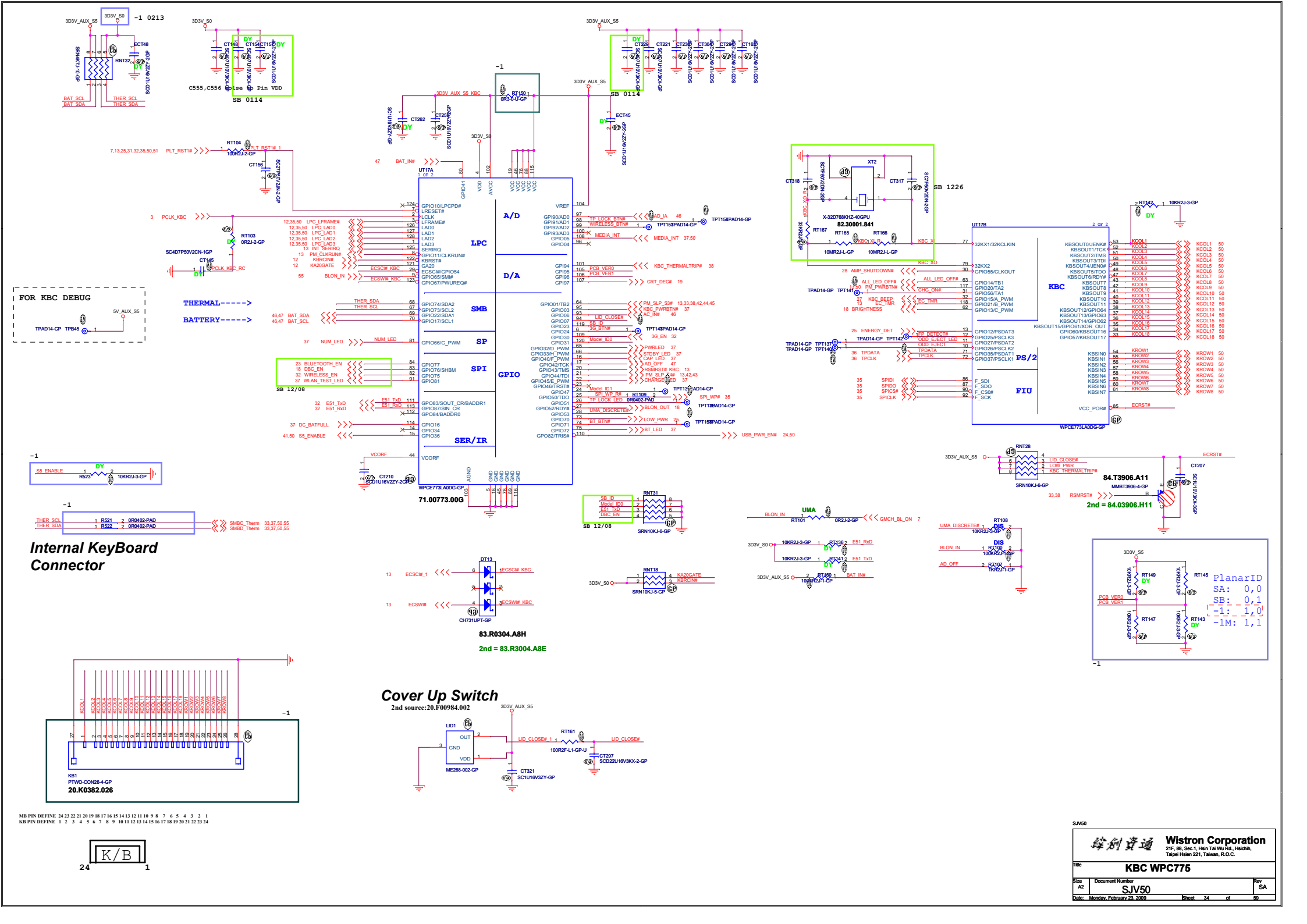
FOR KBC DEBUG
THERMAL----->
BATTERY----->
SB 12/08
71.00773.00G
Internal KeyBoard Connector
Cover Up Switch
2nd source:20.F00984.002
83.R0304.A8H
2nd = 83.R3004.A8E
SB 0114
SB 1226
82.30001.841
84.T3906.A11
2nd = 84.03906.H11
20.K0382.026
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
Size A2
Document Number SJV50
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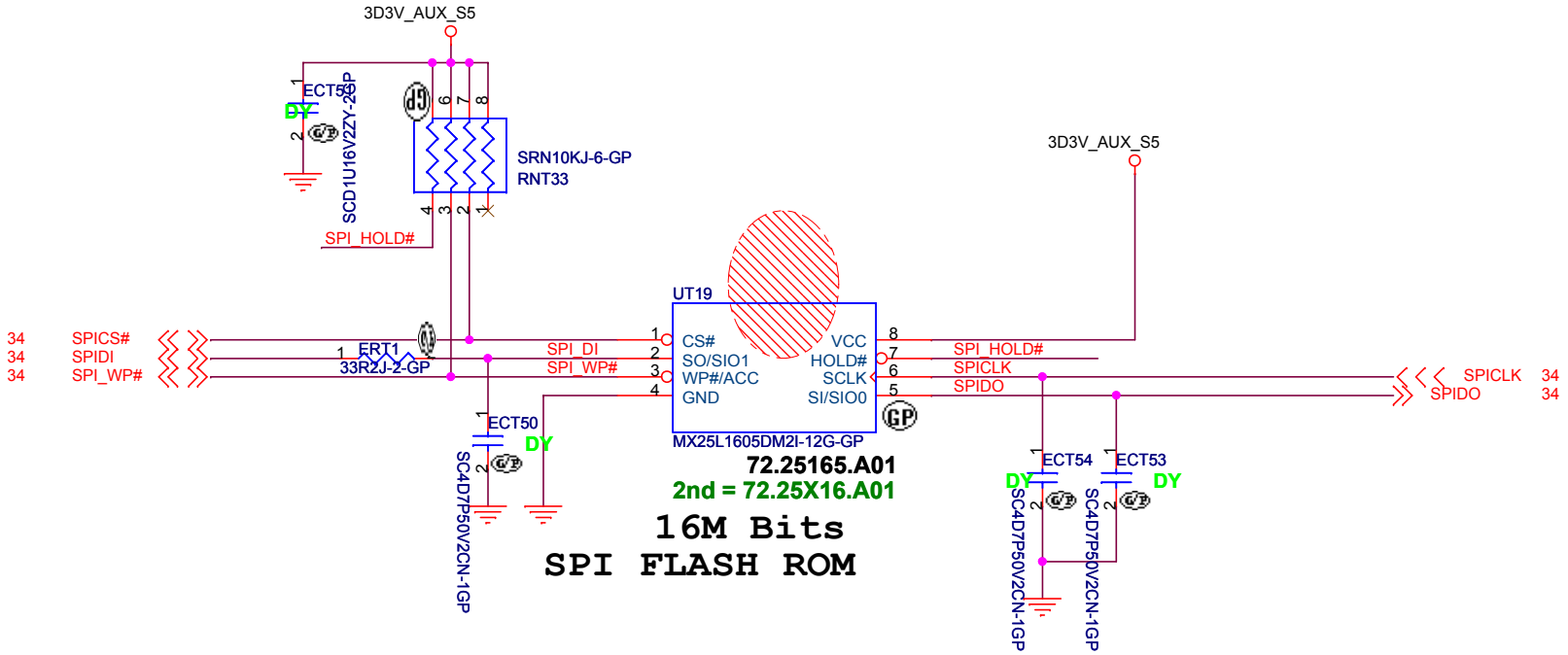
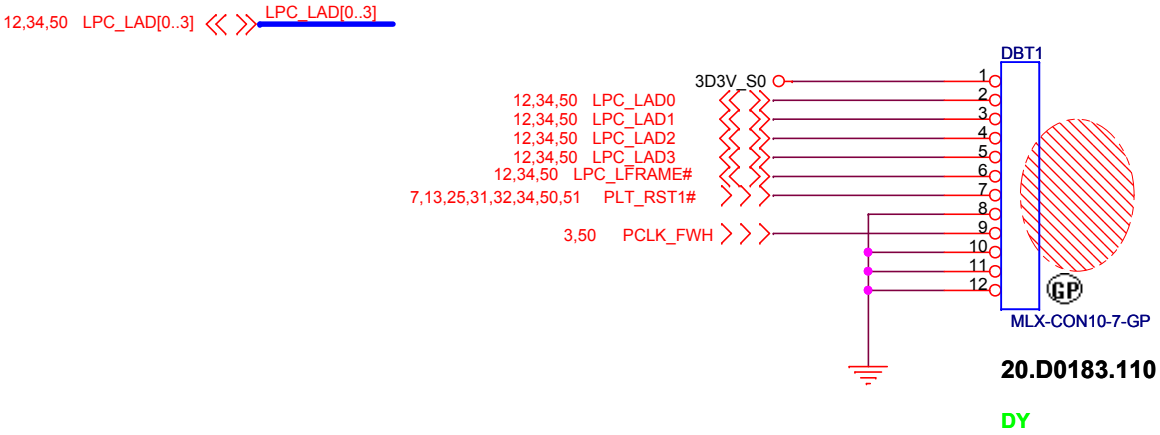


GOLDEN FINGER FOR DEBUG BOARD



SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
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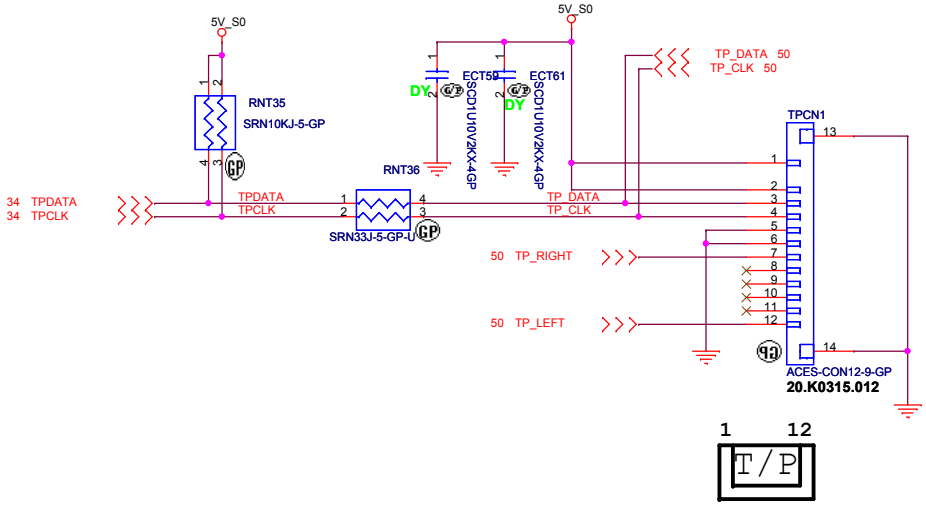
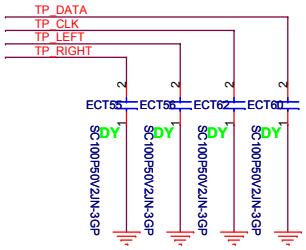
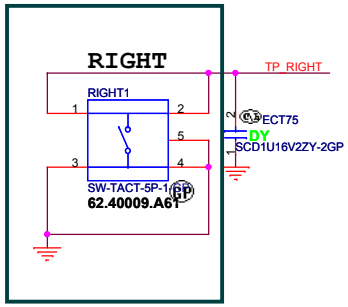
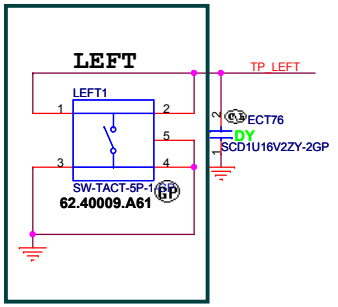
TOUCH PAD







-1 ME 0220



-1 ME 0220

SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch PAD and FP		
Size	Document Number: SJV50	Rev: SA
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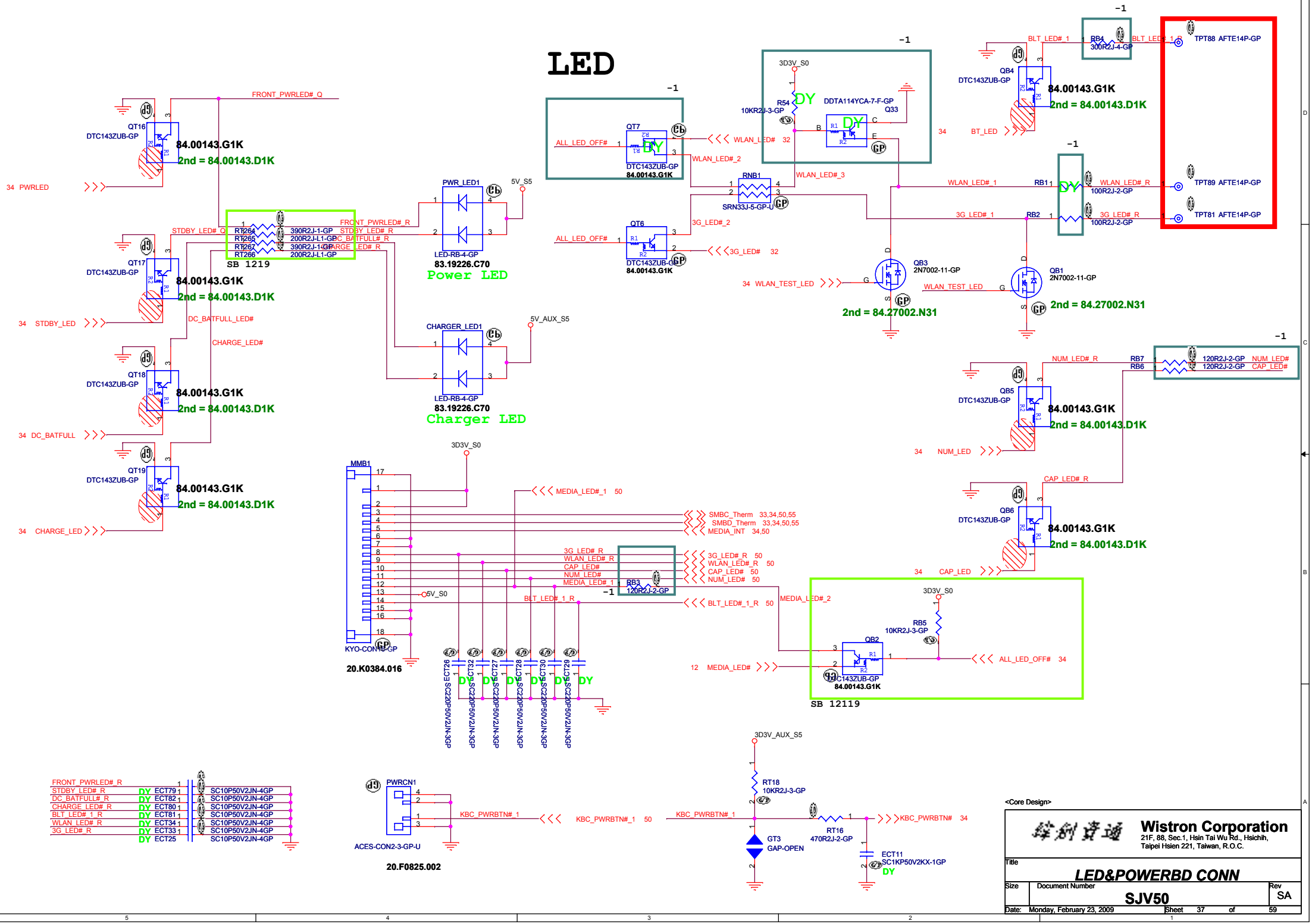
LED



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED&POWERBD CONN**

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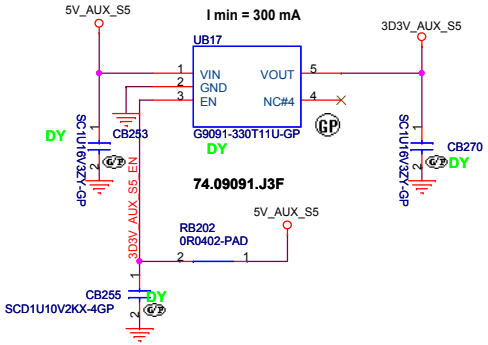
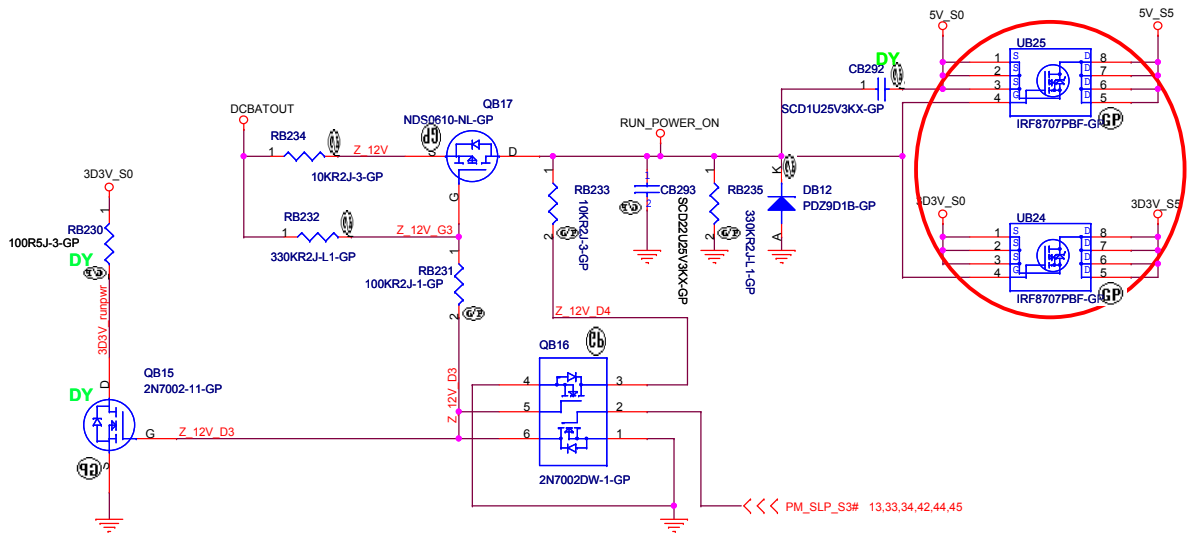
Aux Power 3D3V_AUX_S5



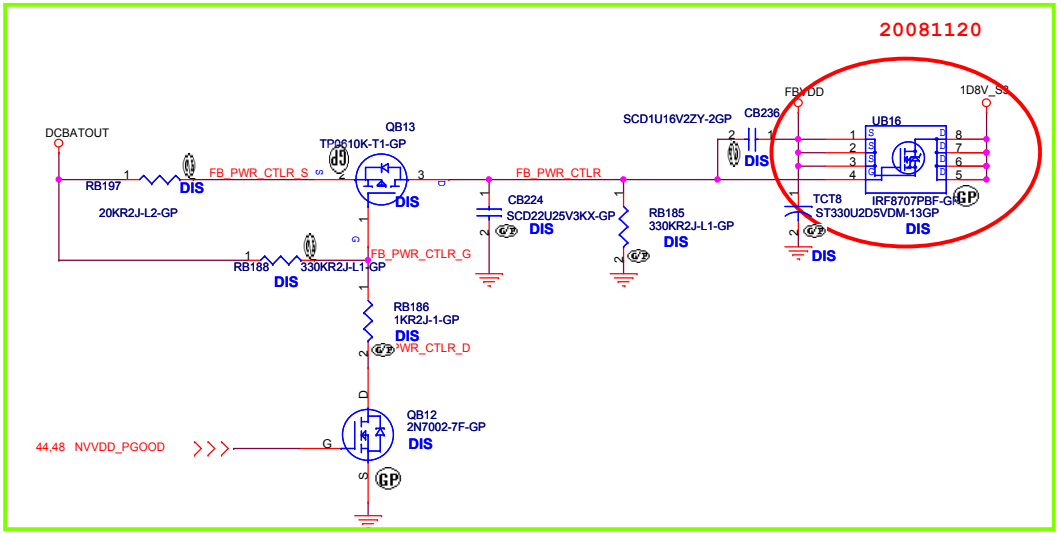
Run Power

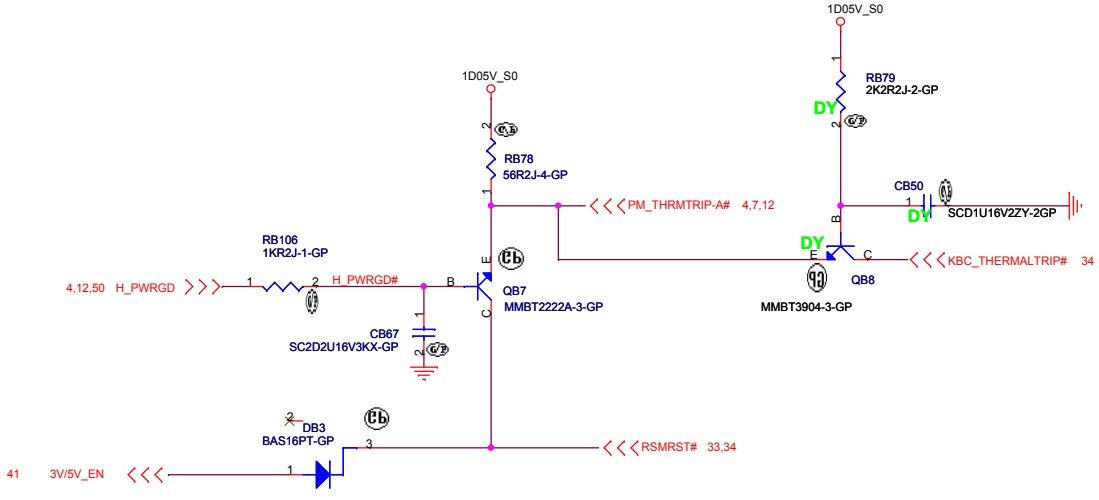
20081120



SB 12/11

20081120





Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(5.5A)

Charger BQ24745

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size	Document Number	Rev
B	SJV50	SA

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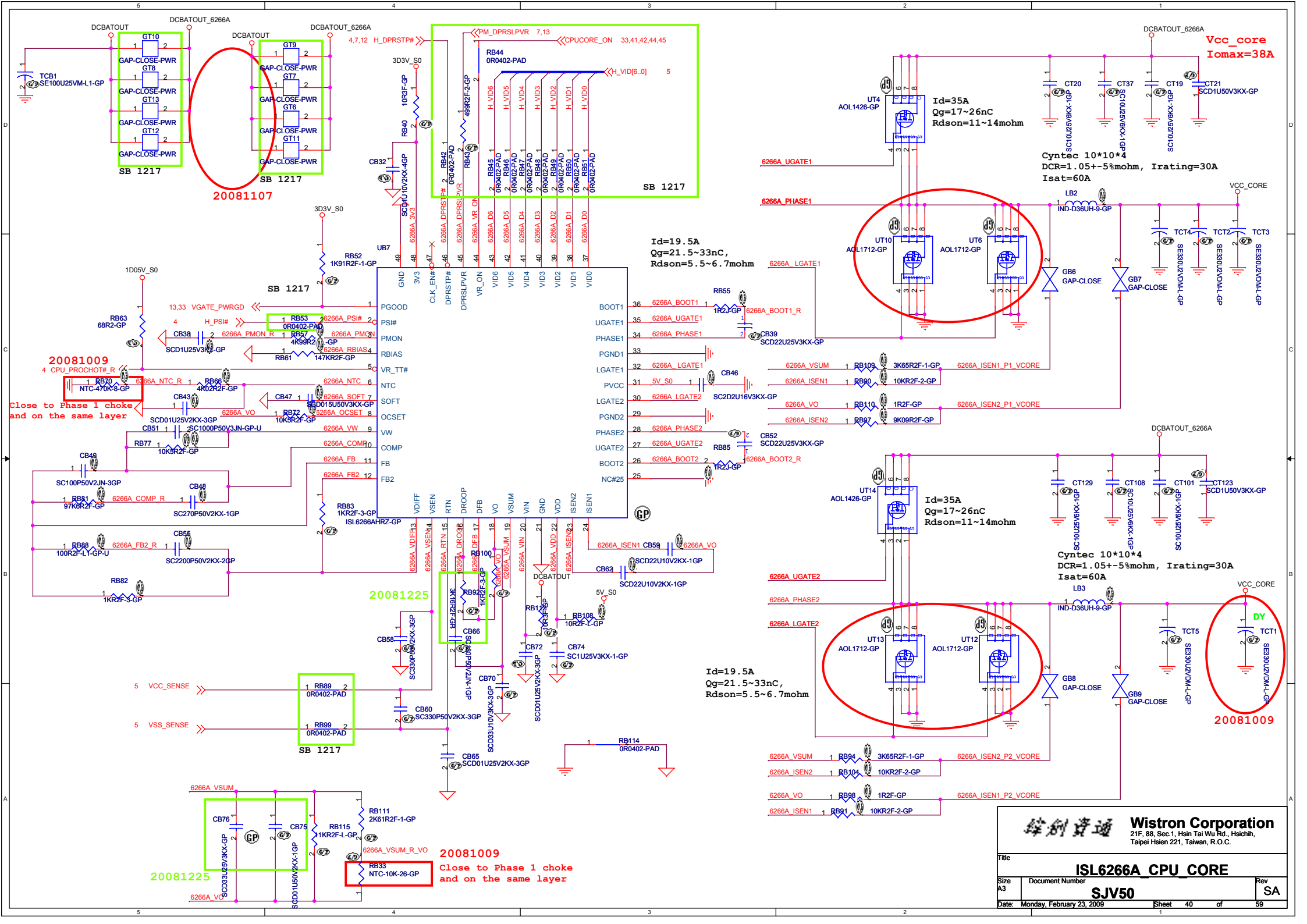
DCBATOUT
DCBATOUT_6266A
SB 1217
20081107
20081009
20081225
Close to Phase 1 choke and on the same layer
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
UB7
ISL6266AHRZ-GP
VCC_CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
SJV50
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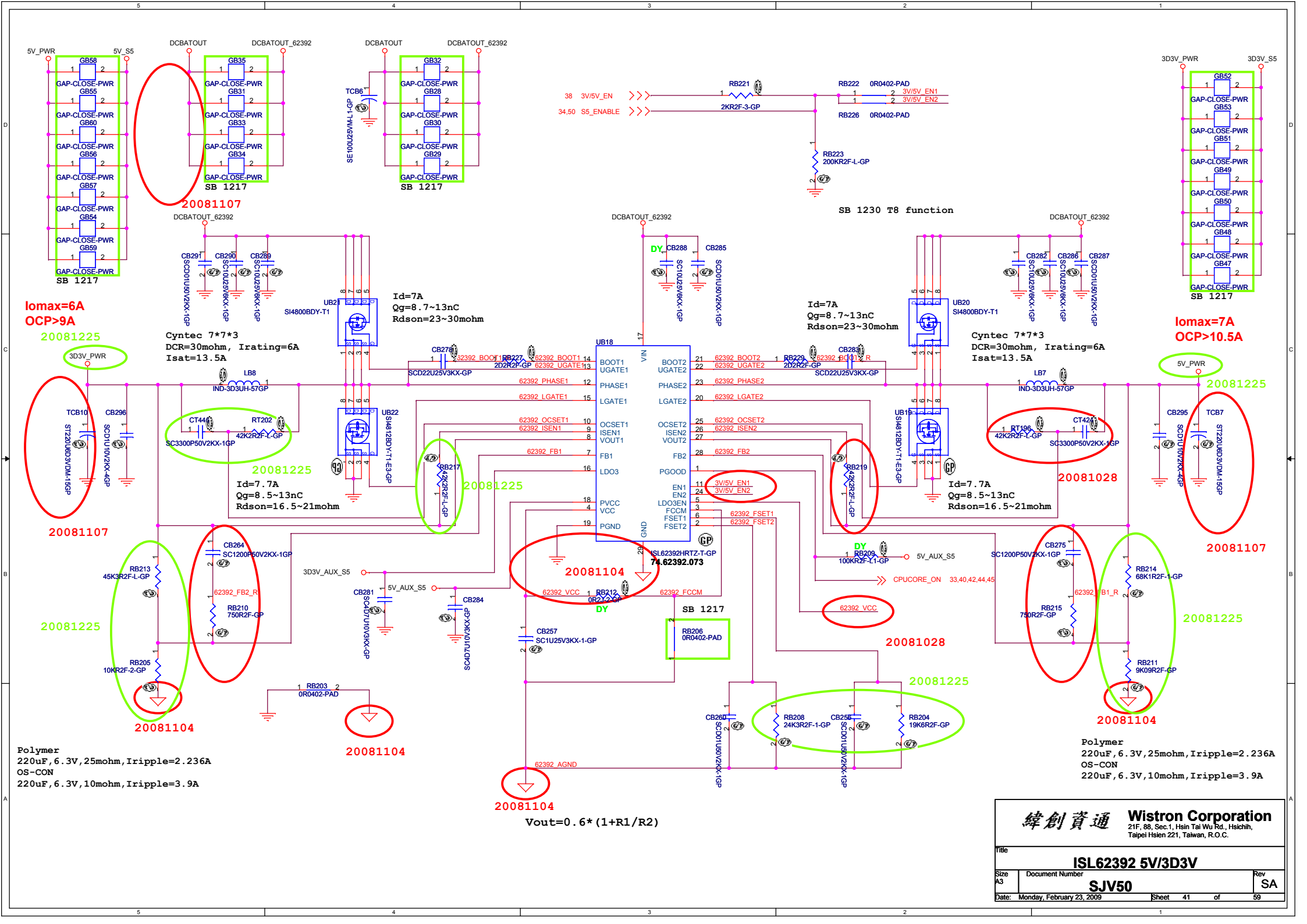
5V_PWR
5V_S5
GB58
GB55
GB60
GB56
GB57
GB54
GB59
GAP-CLOSE-PWR
SB 1217
DCBATOUT
DCBATOUT_62392
GB35
GB31
GB33
GB34
20081107
GB32
GB28
GB30
GB29
TCB6
SE100U25VML-1-GP
38 3V/5V_EN
34,50 S5_ENABLE
RB221
2KR2F-3-GP
RB222 0R0402-PAD
RB226 0R0402-PAD
3V/5V_EN1
3V/5V_EN2
RB223
200KR2F-L-GP
SB 1230 T8 function
3D3V_PWR
3D3V_S5
GB52
GB53
GB51
GB49
GB50
GB48
GB47
CB291
CB290
CB289
SCD01U50V2KX-1GP
SC10U25V6KX-1GP
UB21
SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Iomax=6A
OCP>9A
20081225
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
3D3V_PWR
LB8
IND-3D3UH-57GP
TCB10
ST220U6D3VDM-15GP
CB296
SCD1U10V2KX-4GP
CT44
SC3300P50V2KX-1GP
RT202
42K2R2F-L-GP
UB22
SI4812BDY-T1-E3-GP
RB217
20081225
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20081107
CB264
SC1200P50V2KX-1GP
RB213
45K3R2F-L-GP
62392_FB2_R
RB210
750R2F-GP
RB205
10KR2F-2-GP
20081225
20081104
RB203
0R0402-PAD
20081104
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
DCBATOUT_62392
DY CB288
CB285
SC10U25V6KX-1GP
SCD01U50V2KX-1GP
UB18
ISL62392HRTZ-T-GP
74.62392.073
BOOT1
UGATE1
PHASE1
LGATE1
OCSET1
ISEN1
VOUT1
FB1
LDO3
PVCC
VCC
PGND
VIN
BOOT2
UGATE2
PHASE2
LGATE2
OCSET2
ISEN2
VOUT2
FB2
PGOOD
EN1
EN2
LDO3EN
FCCM
FSET1
FSET2
GND
62392_BOOT1
62392_UGATE1
62392_PHASE1
62392_LGATE1
62392_OCSET1
62392_ISEN1
62392_FB1
62392_BOOT2
62392_UGATE2
62392_PHASE2
62392_LGATE2
62392_OCSET2
62392_ISEN2
62392_FB2
3V/5V_EN1
3V/5V_EN2
62392_FSET1
62392_FSET2
SCD22U25V3KX-GP
RB227
2D2R2F-GP
RB229
RB217
RB219
20081104
62392_VCC
RB212
0R2J-2-GP
62392_FCCM
DY
SB 1217
RB206
0R0402-PAD
CB257
SC1U25V3KX-1GP
CB281
SC4D7U10V3KX-GP
CB284
SC4D7U10V3KX-GP
3D3V_AUX_S5
5V_AUX_S5
RB209
100KR2F-L1-GP
CPUCORE_ON 33,40,42,44,45
62392_VCC
20081028
62392_AGND
20081104
Vout=0.6*(1+R1/R2)
CB260
SCD01U50V2KX-1GP
RB208
24K3R2F-1-GP
CB255
RB204
19K6R2F-GP
UB20
SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=7A
OCP>10.5A
LB7
IND-3D3UH-57GP
UB19
SI4812BDY-T1-E3-GP
RT196
42K2R2F-L-GP
CT424
SC3300P50V2KX-1GP
20081028
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
5V_PWR
20081225
CB295
SCD1U10V2KX-4GP
TCB7
ST220U6D3VDM-15GP
20081107
CB275
SC1200P50V2KX-1GP
RB214
68K1R2F-1-GP
62392_FB1_R
RB215
750R2F-GP
20081225
RB211
9K09R2F-GP
20081104
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size
A3
Document Number
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Rev
SA
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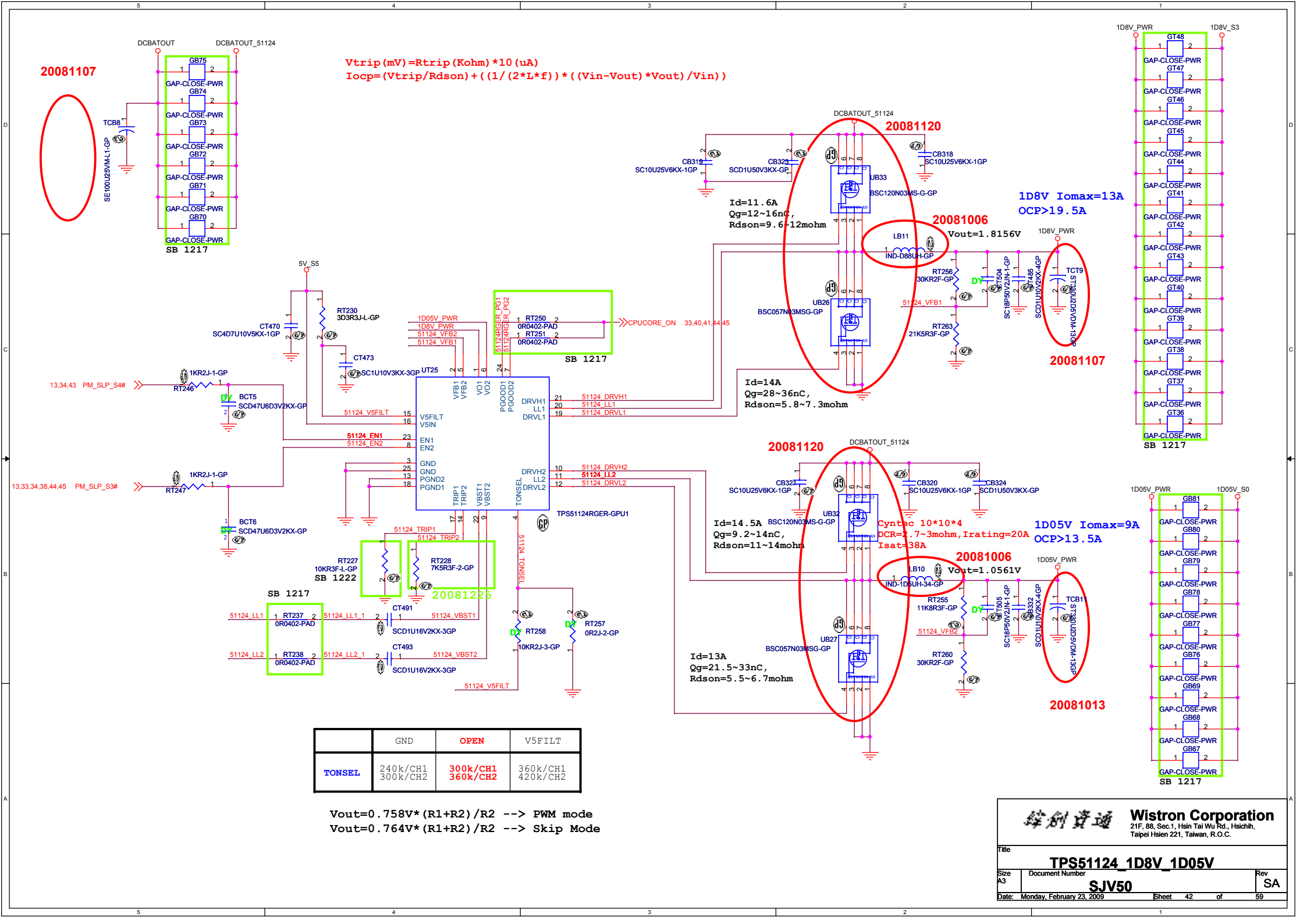

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size	Document Number	Rev
A3	SJV50	SA

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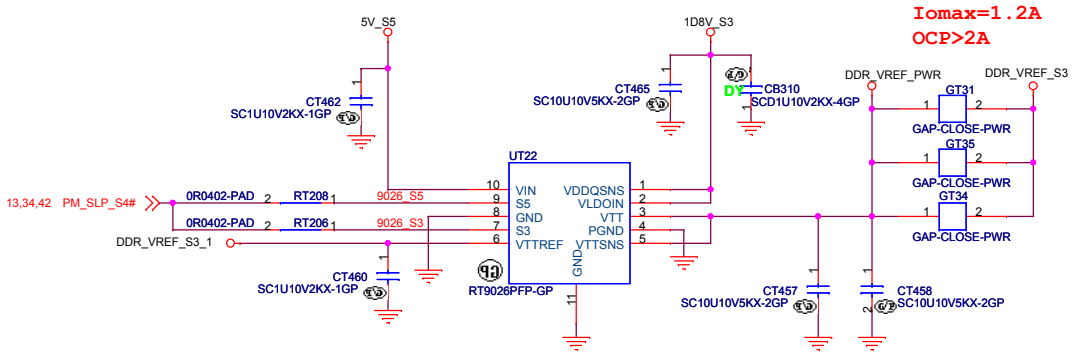

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *0D9V*

Size	Document Number	Rev
A3	SJV50	SA

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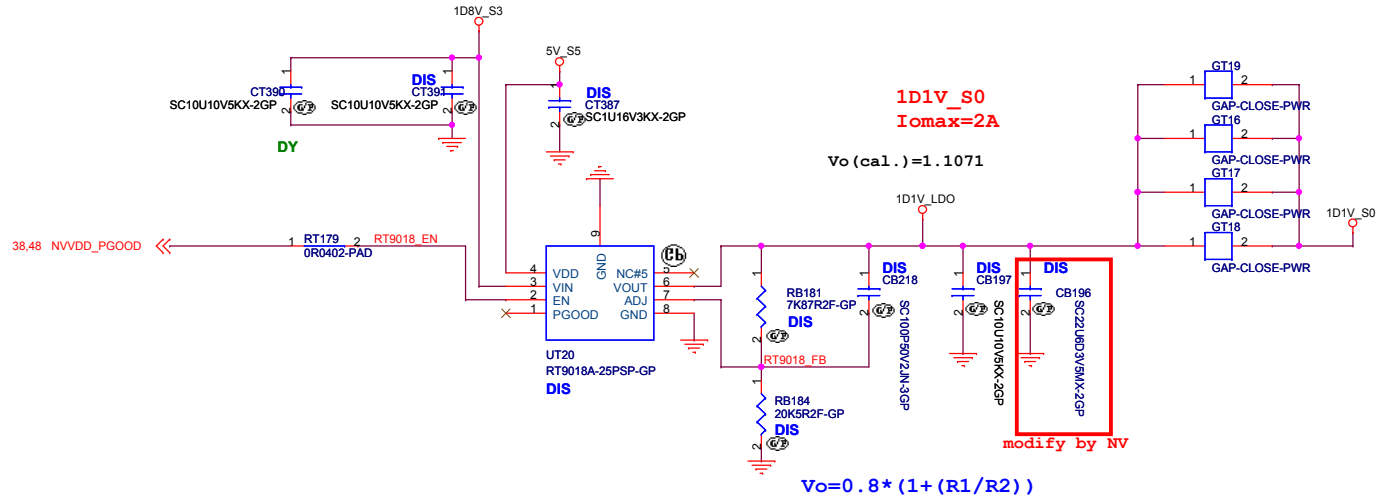

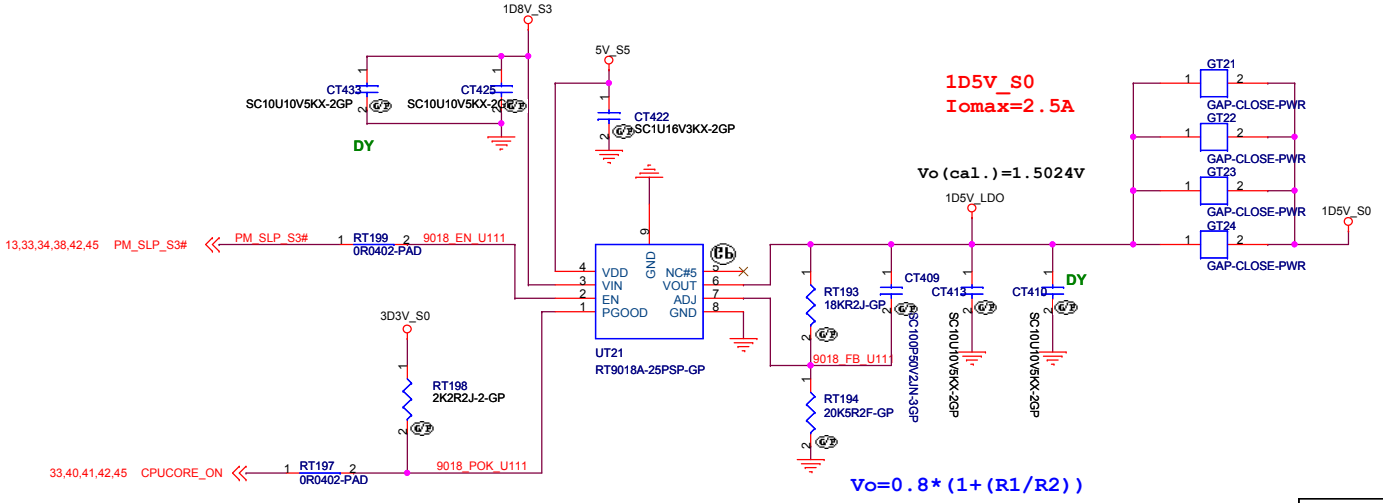

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D1V & 1D5V

Size	Document Number	Rev
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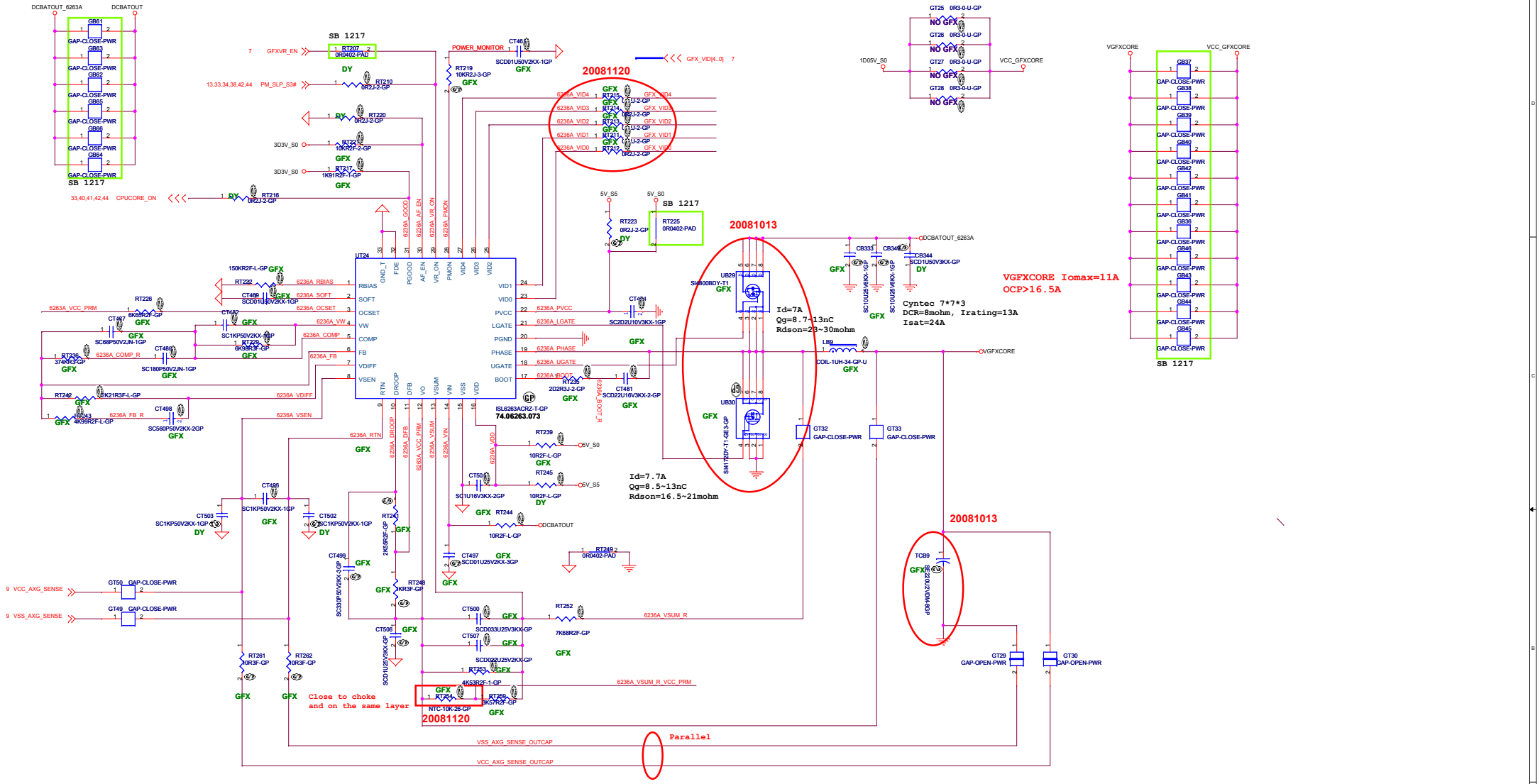
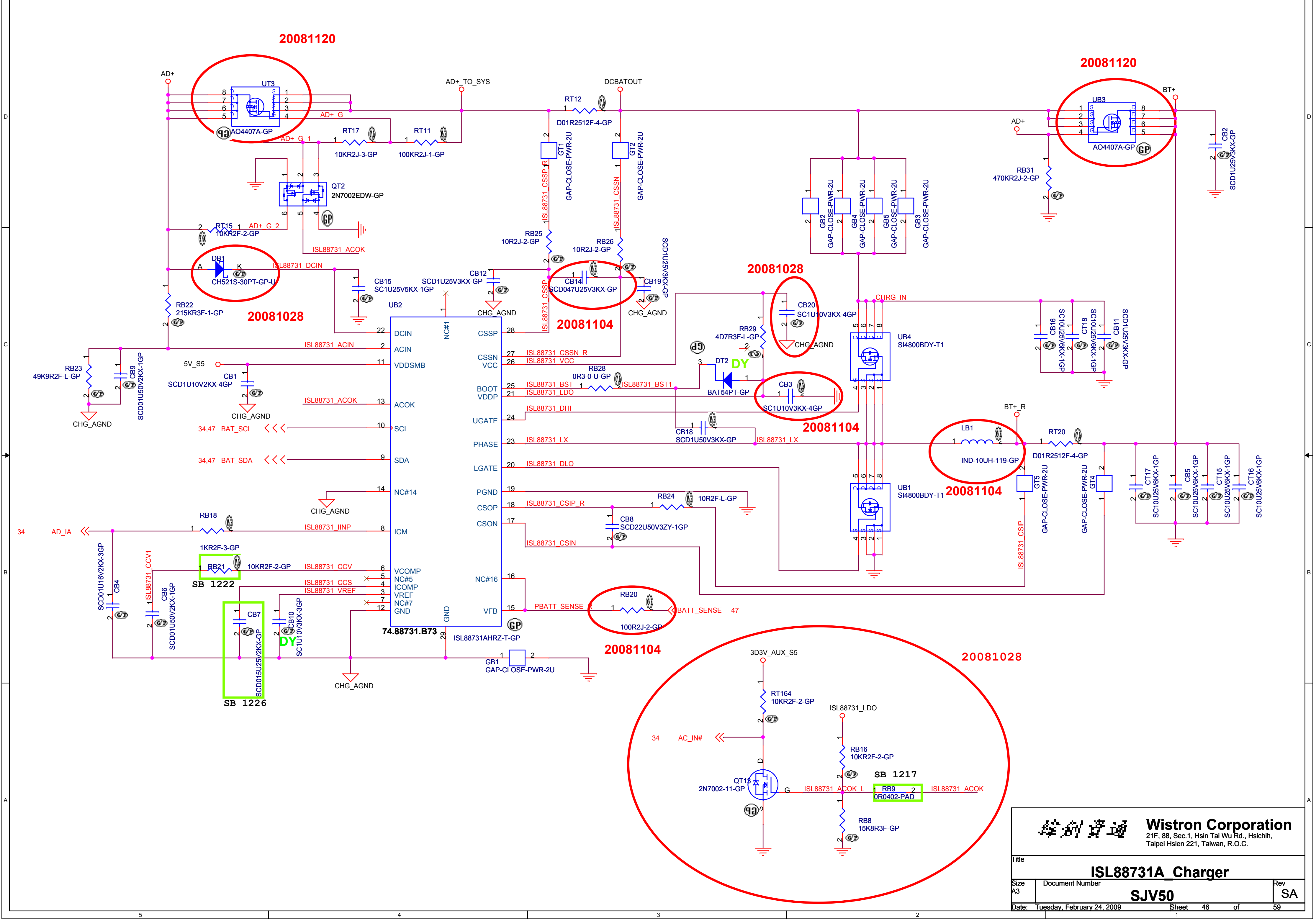


Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL6263A_NVDD		
Size: A2	Document Number: SJV50	Rev: SA
Date: Tuesday, February 24, 2009	Sheet 45 of 59	


20081120
AD+
UT3
AO4407A-GP
AD+_TO_SYS
DCBATOUT
RT12
D01R2512F-4-GP
RT17
10KR2J-3-GP
RT11
100KR2J-1-GP
QT2
2N7002EDW-GP
RT15
10KR2F-2-GP
ISL88731_ACOK
DB1
CH521S-30PT-GP-U
ISL88731_DCIN
20081028
RB22
215KR3F-1-GP
CB15
SC1U25V5KX-1GP
CB12
SCD1U25V3KX-GP
CB14
SCD047U25V3KX-GP
CB19
CHG_AGND
20081104
UB2
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
RB23
49K9R2F-L-GP
CB9
SCD01U50V2KX-1GP
5V_S5
CB1
SCD1U10V2KX-4GP
34,47 BAT_SCL
34,47 BAT_SDA
RB18
1KR2F-3-GP
34 AD_IA
RB21
10KR2F-2-GP
SB 1222
CB4
SCD01U16V2KX-3GP
CB6
SCD01U50V2KX-1GP
CB7
SCD015U25V2KX-GP
CB10
SC1U10V3KX-3GP
SB 1226
DY
GB1
GAP-CLOSE-PWR-2U
RB25
10R2J-2-GP
RB26
10R2J-2-GP
GT1
GT2
GAP-CLOSE-PWR-2U
RB28
0R3-0-U-GP
ISL88731_BST1
DT2
BAT54PT-GP
RB29
4D7R3F-L-GP
CB20
SC1U10V3KX-4GP
CB3
SC1U10V3KX-4GP
CB18
SCD1U50V3KX-GP
ISL88731_LX
CHRG_IN
UB4
SI4800BDY-T1
UB1
SI4800BDY-T1
GB2
GB4
GB5
GB3
CB16
CT18
CB11
BT+
UB3
AO4407A-GP
RB31
470KR2J-2-GP
CB2
SCD1U25V3KX-GP
BT+_R
LB1
IND-10UH-119-GP
RT20
D01R2512F-4-GP
GT5
GT4
CT17
CB5
CT15
CT16
SC10U25V6KX-1GP
RB24
10R2F-L-GP
CB8
SCD22U50V3ZY-1GP
RB20
100R2J-2-GP
PBATT_SENSE
BATT_SENSE 47
3D3V_AUX_S5
RT164
10KR2F-2-GP
ISL88731_LDO
34 AC_IN#
RB16
10KR2F-2-GP
SB 1217
QT13
2N7002-11-GP
ISL88731_ACOK_L
RB9
0R0402-PAD
RB8
15K8R3F-GP

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Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL88731A_Charger	
Size A3	Document Number SJV50	Rev SA
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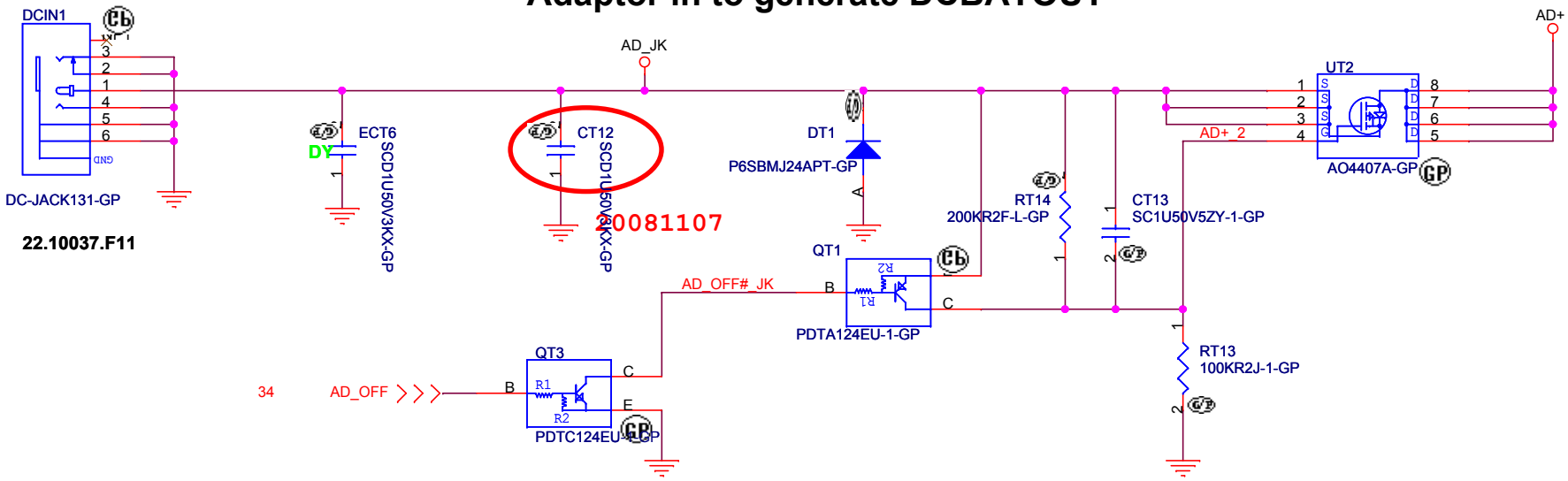
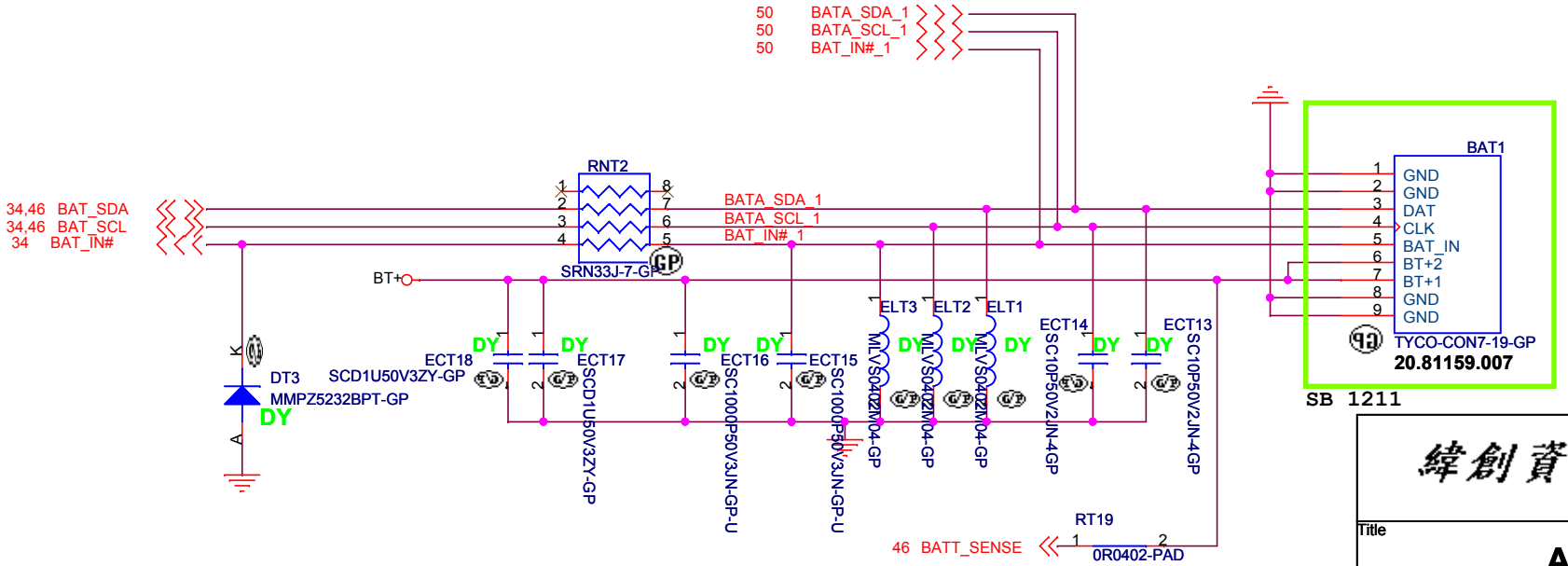
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: SJV50	Rev: SA
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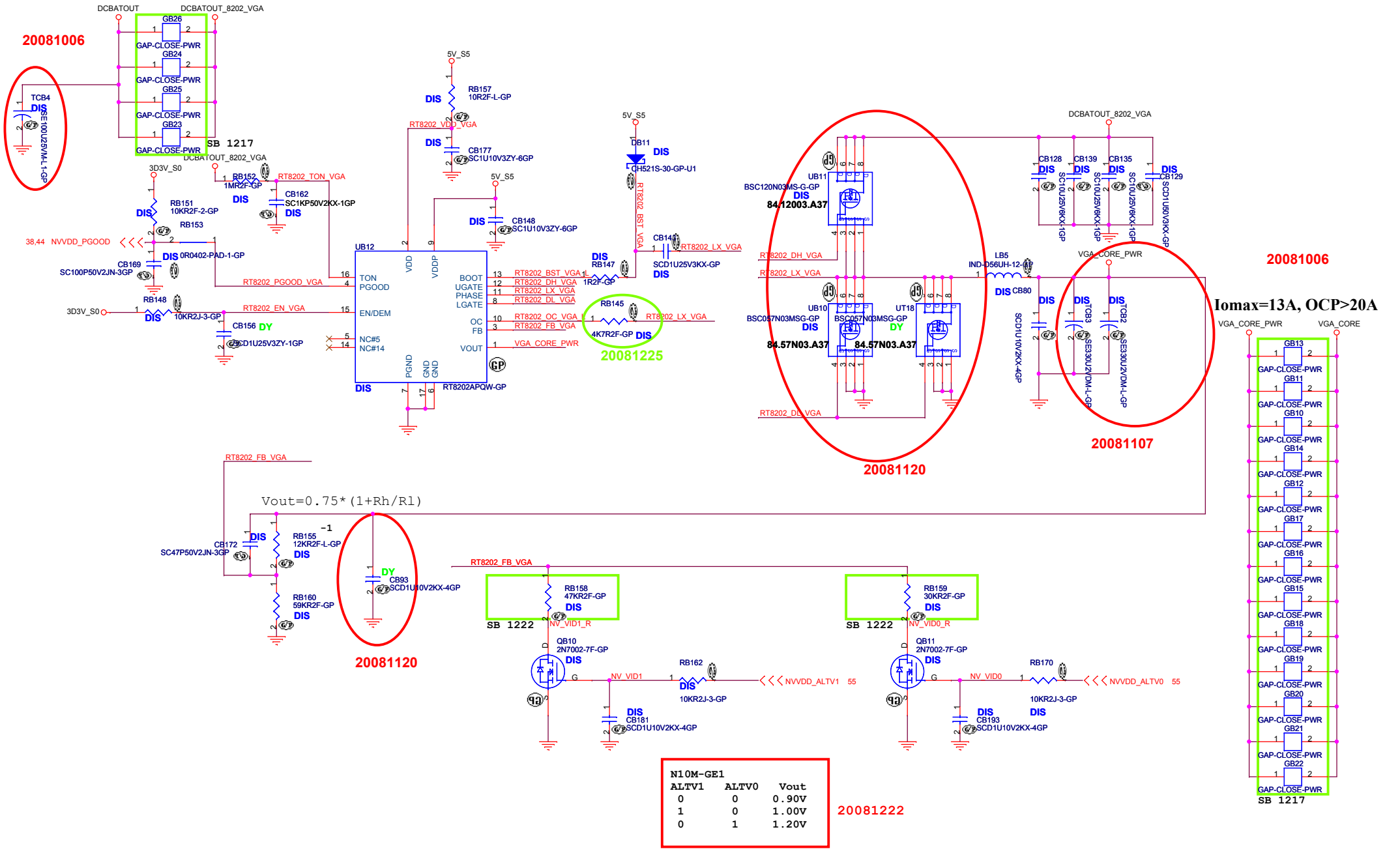

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VGA CORE		
Size: A3	Document Number: SJV50	Rev: SA
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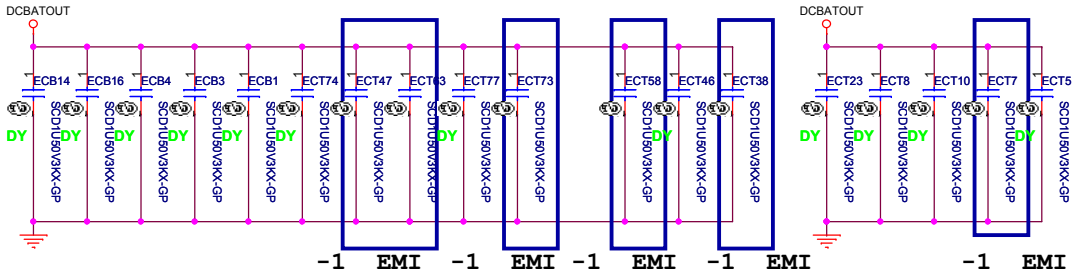

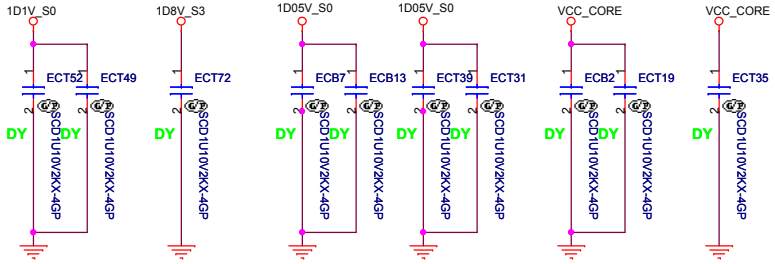

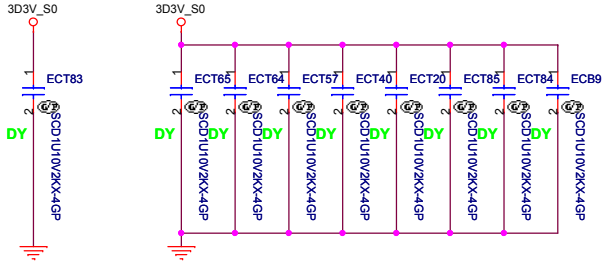

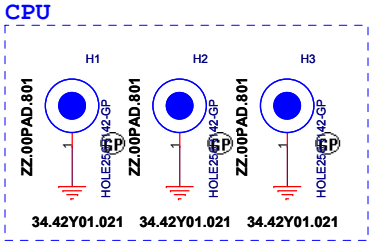

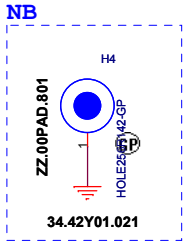

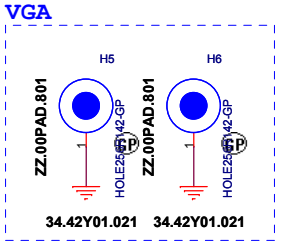

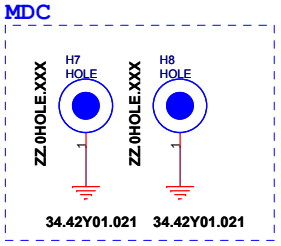

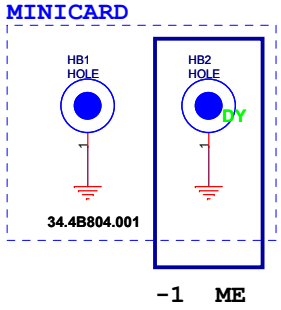

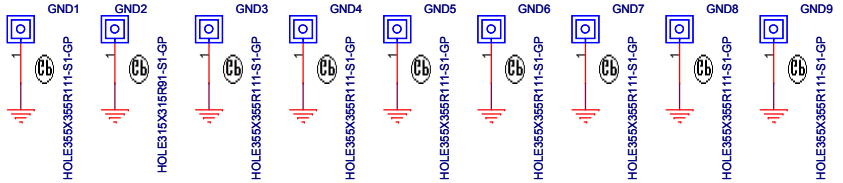

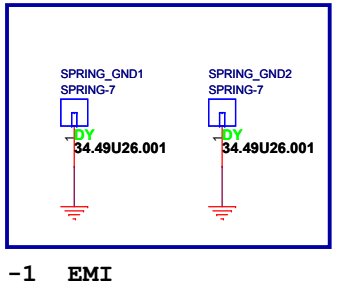

SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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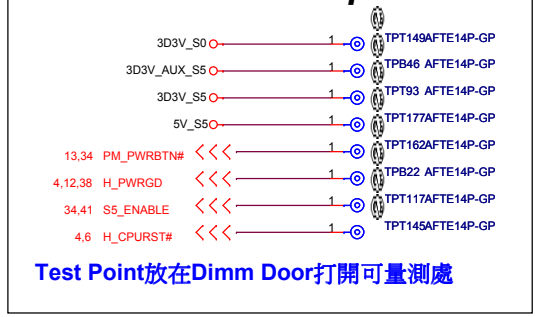
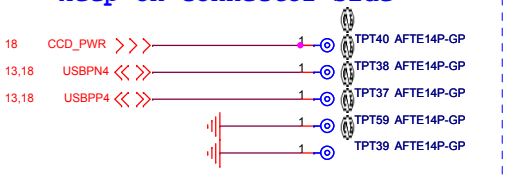
Check test point



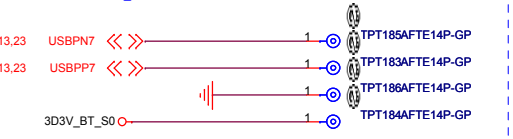
Test Point放在Dimm Door打開可量測處

CCD Conn. Test Point keep on connector side

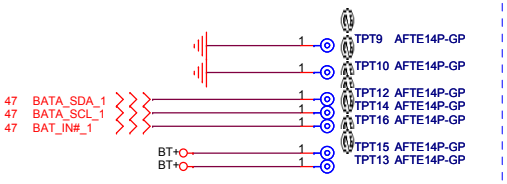


Internal MIC Conn. Test Point keep on connector side

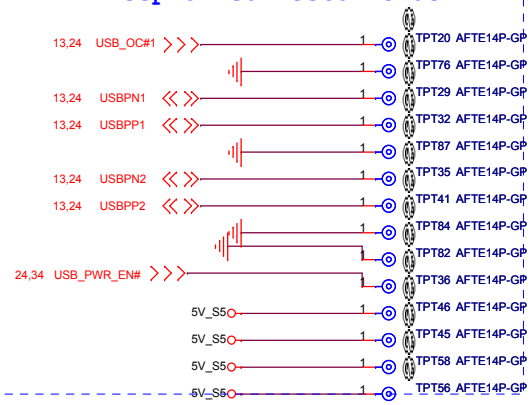
BT Conn. Test Point keep on connector side



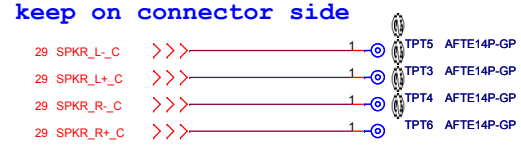
BAT Conn. Test Point keep on connector side



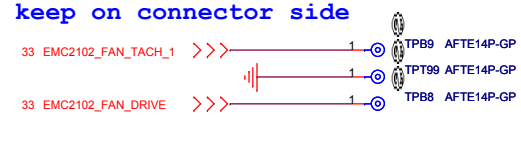
USB_CN1 Conn. Test Point keep on connector side



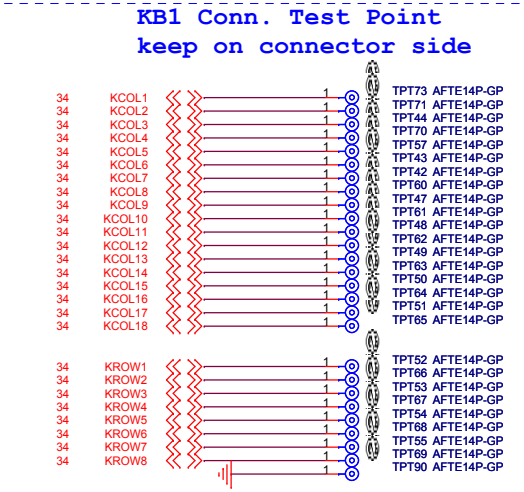
Speaker Conn. Test Point keep on connector side



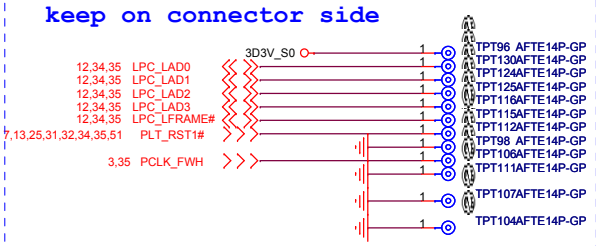
FAN1 Conn. Test Point keep on connector side



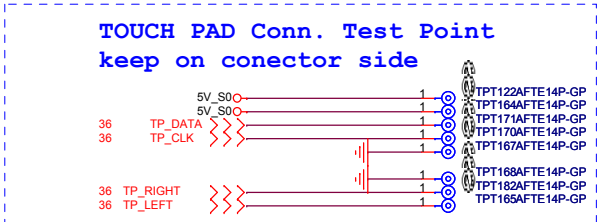
KB1 Conn. Test Point keep on connector side



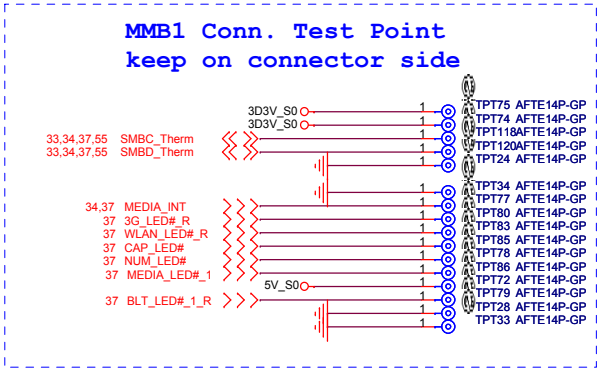
DEBUG BOARD Conn. Test Point keep on connector side



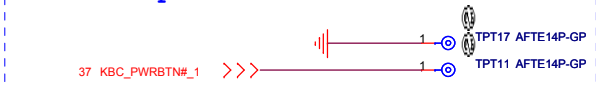
TOUCH PAD Conn. Test Point keep on conector side



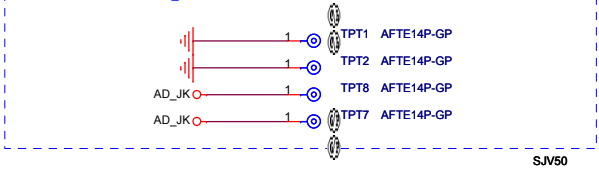
MMB1 Conn. Test Point keep on connector side



Powerbutton Conn. Test Point keep on connector side



DC-IN Conn. Test Point keep on connector side



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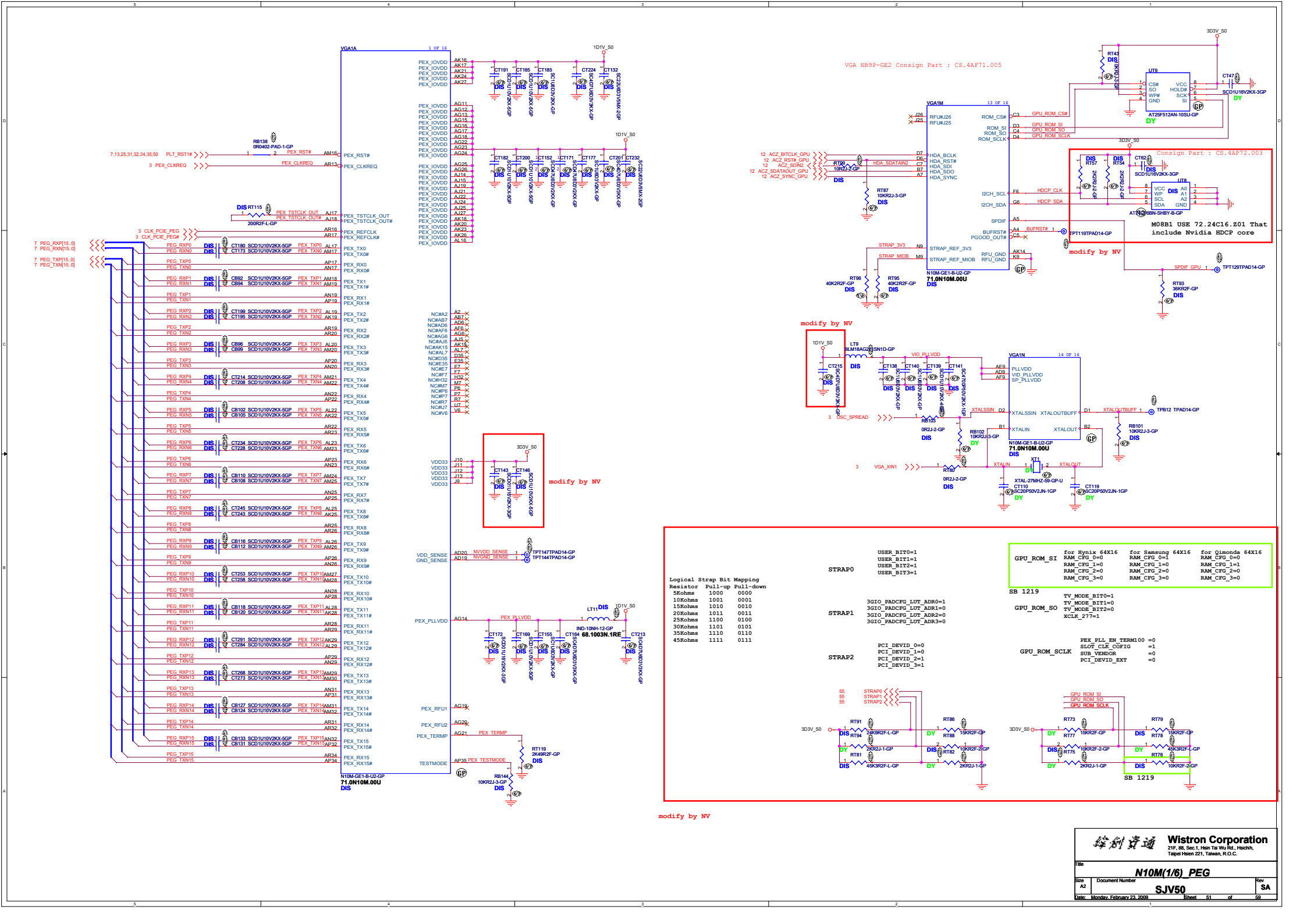
VGA1A
1 OF 16
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
VGA1M
13 OF 16
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
VGA1N
14 OF 16
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
VGA NB9P-GE2 Consign Part : CS.4AF71.005
Consign Part : CS.4AP72.003
M08B1 USE 72.24C16.Z01 That include Nvidia HDCP core
modify by NV
modify by NV
modify by NV
modify by NV
SB 1219
SB 1219
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
STRAP0
STRAP1
STRAP2
GPU_ROM_SI
GPU_ROM_SO
GPU_ROM_SCLK
for Hynix 64X16
for Samsung 64X16
for Qimonda 64X16
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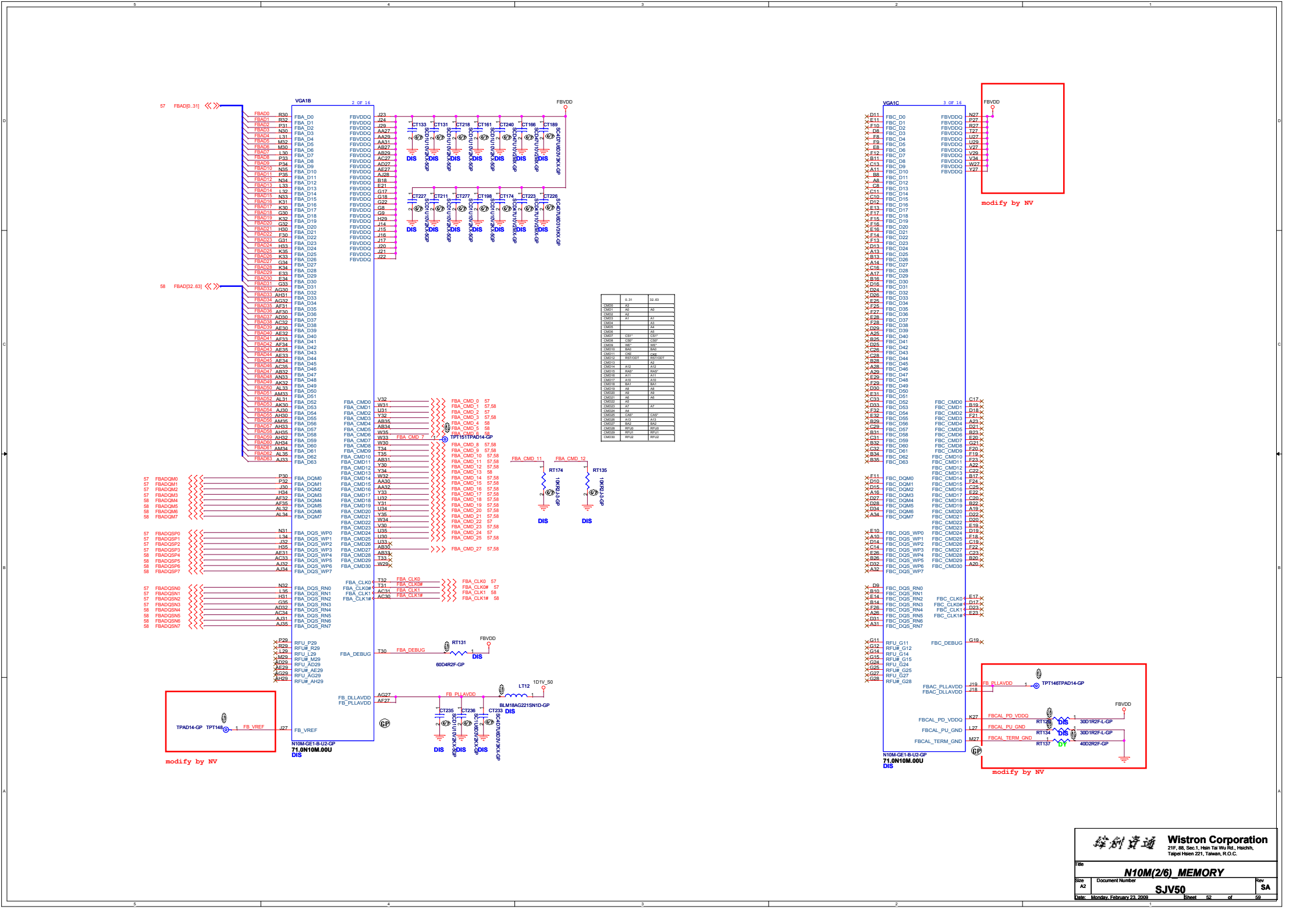
VGA1B
2 OF 16
VGA1C
3 OF 16
FBVDD
modify by NV
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
TPAD14-GP
TPT146
FB_VREF
FB_DLLAVDD
FB_PLLAVDD
FBA_DEBUG
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBA_CMD_11
FBA_CMD_12
RT174
RT135
RT131
LT12
1D1V_S0
BLM18AG221SN1D-GP
60D4R2F-GP
10KR2J-3-GP
FBAC_PLLAVDD
FBAC_DLLAVDD
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
30D1R2F-L-GP
40D2R2F-GP
RT126
RT134
RT137
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N10M(2/6)_MEMORY
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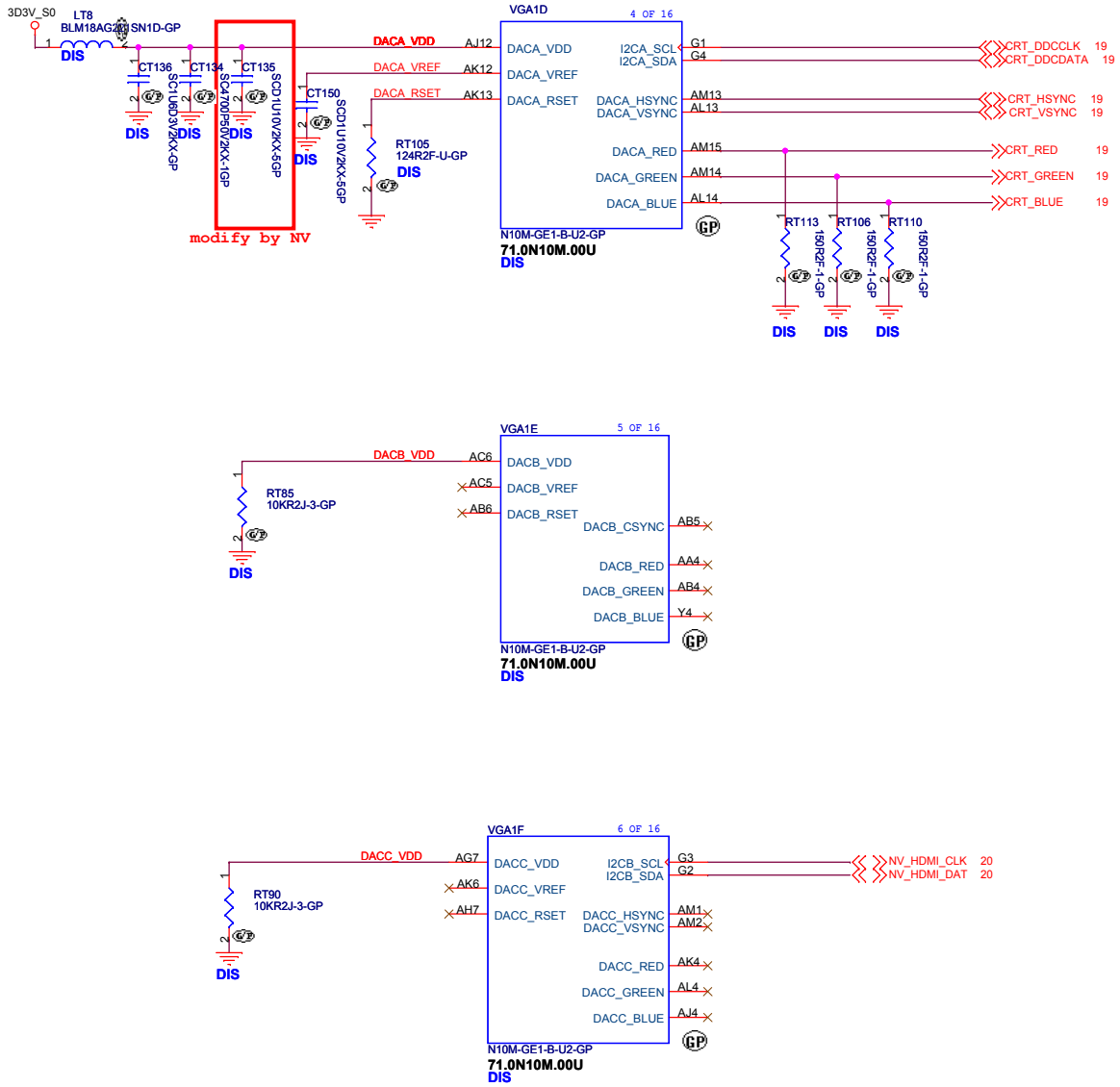

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Title	***N10M(3/6)_DAC***	
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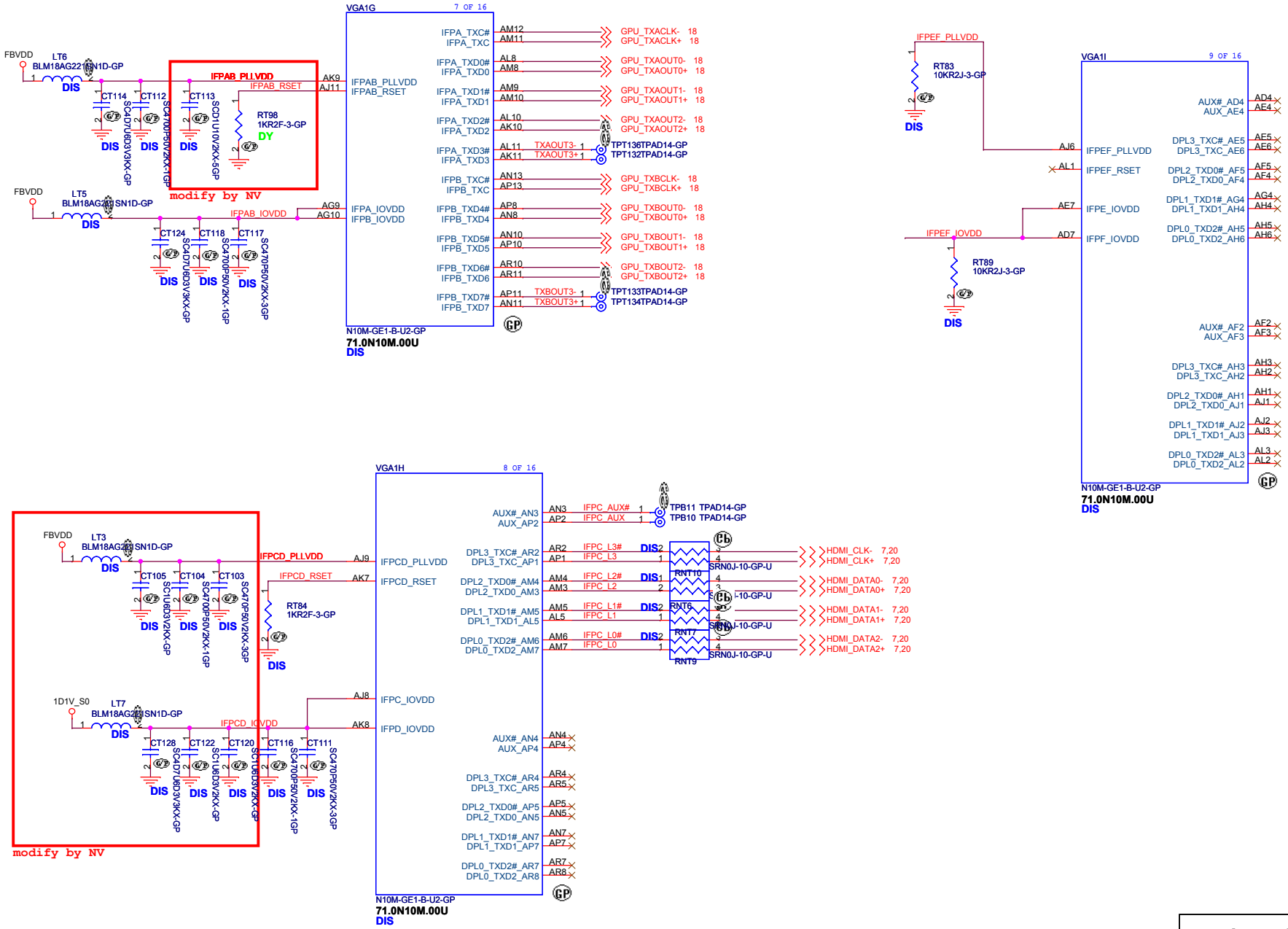

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Title	N10M(4/6)		
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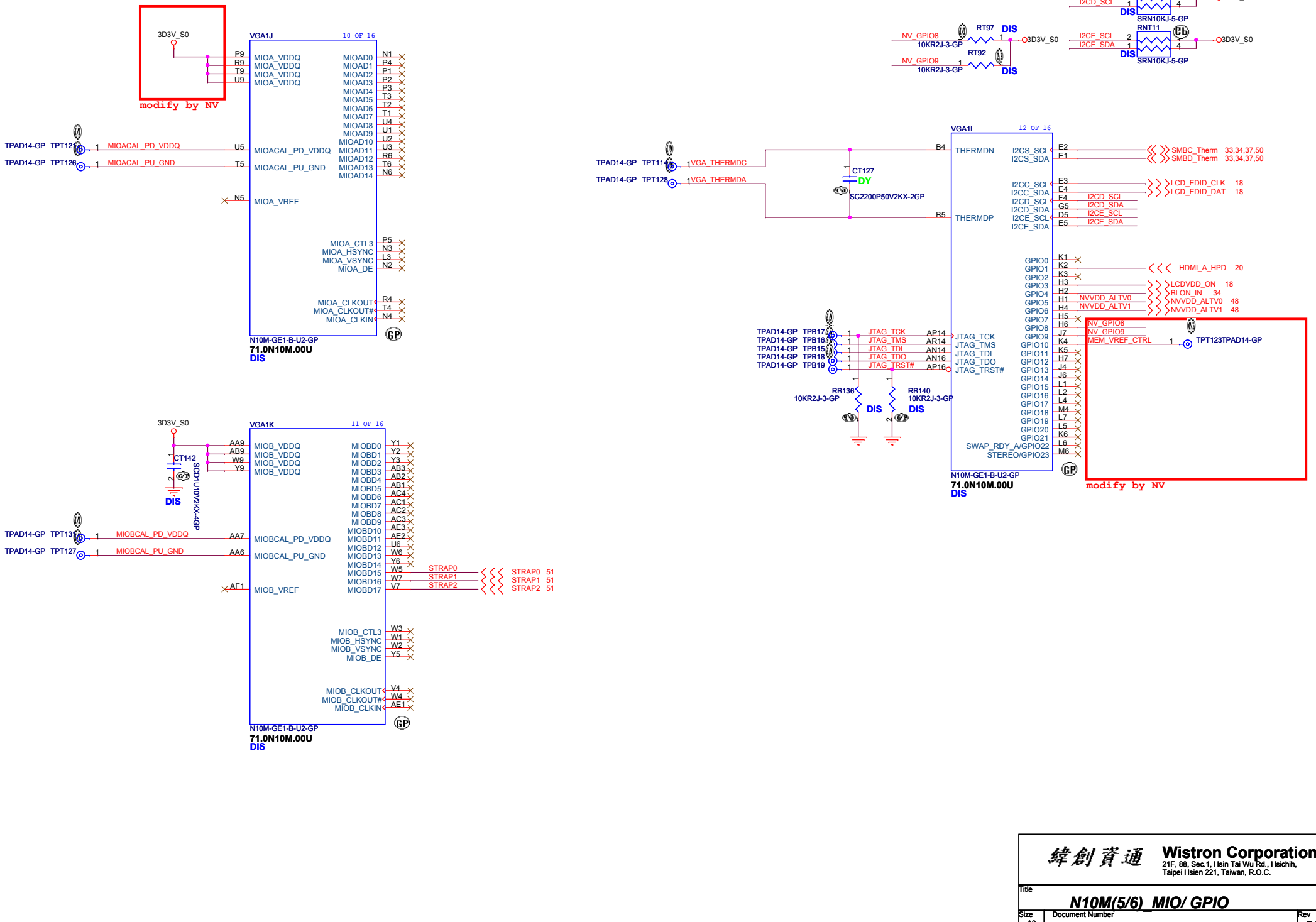

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Title: N10M(5/6)_MIO/ GPIO	
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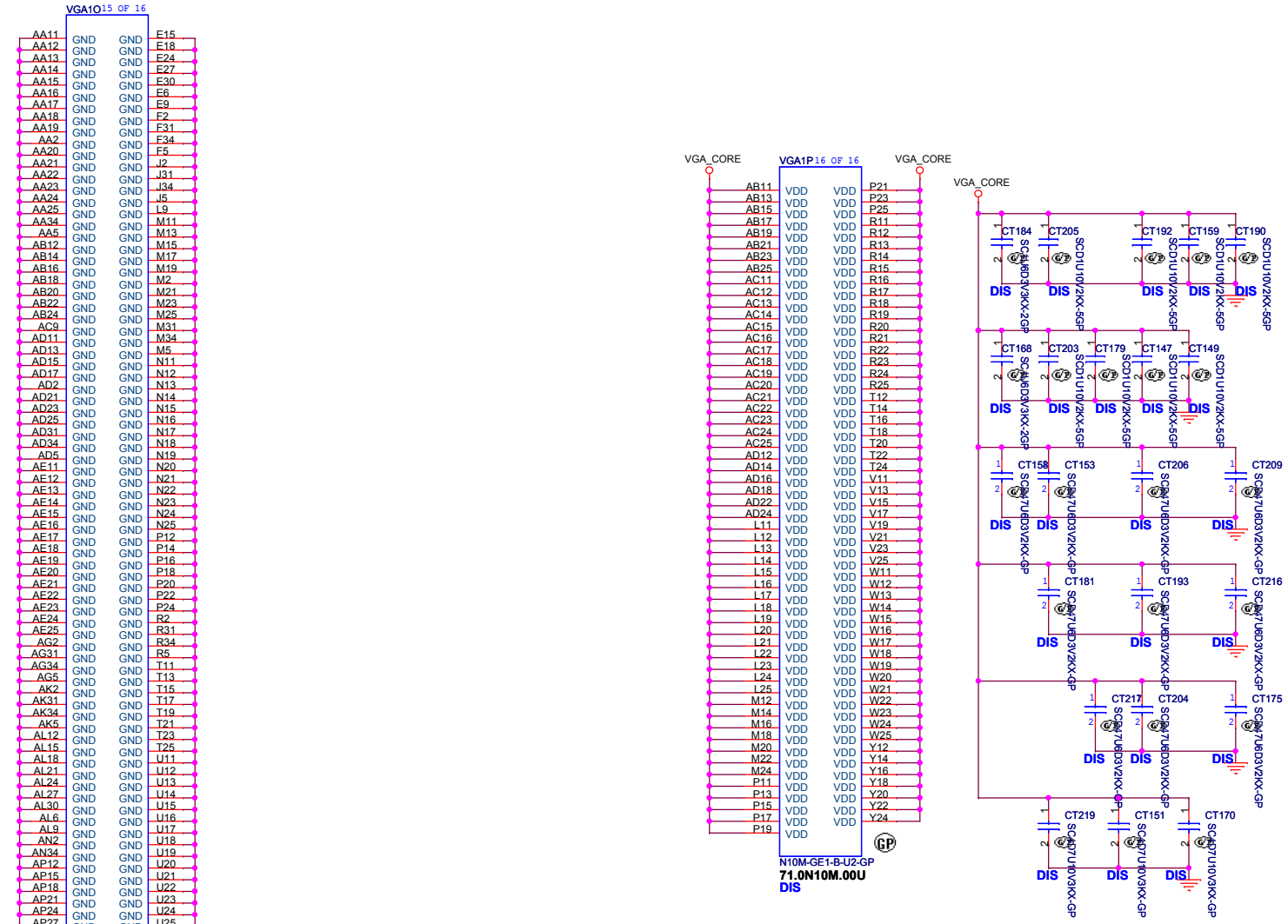

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Title: N10M(6/6)_POWER	
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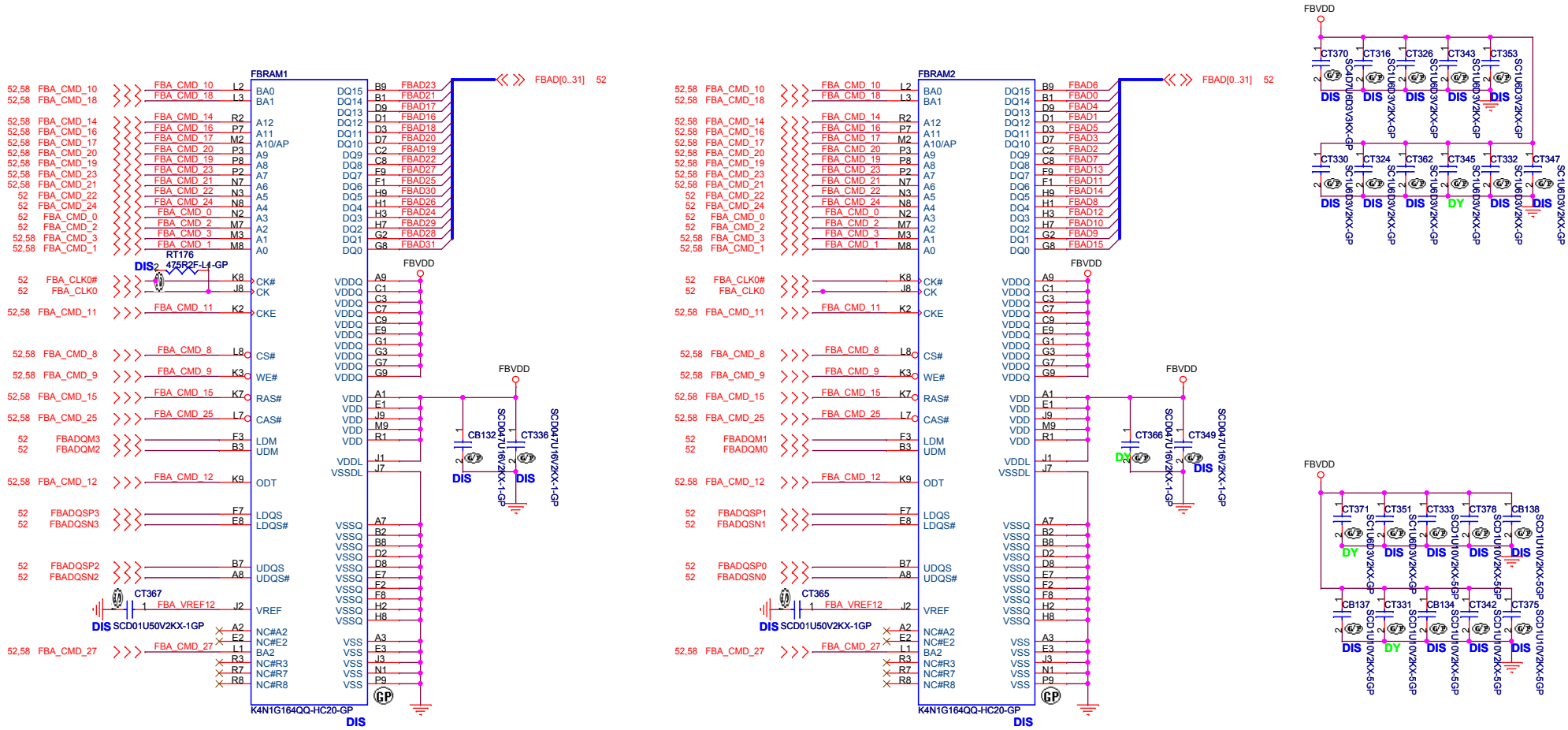

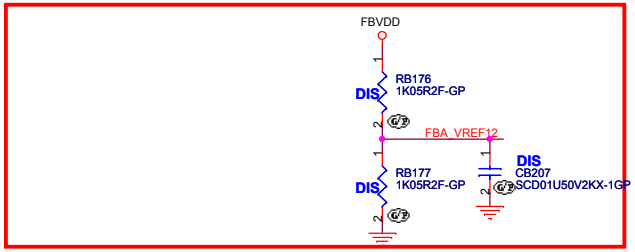

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Title	***VRAM(1/2)***	
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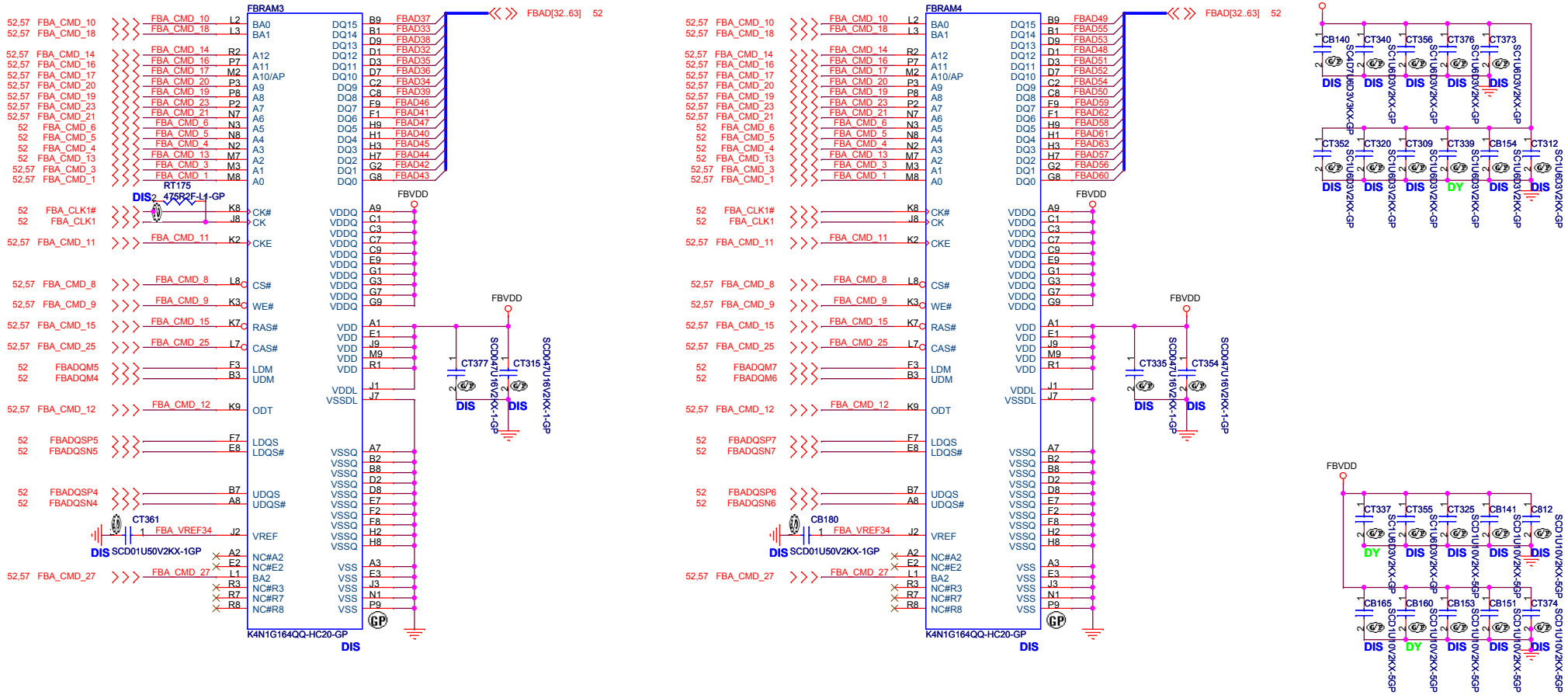

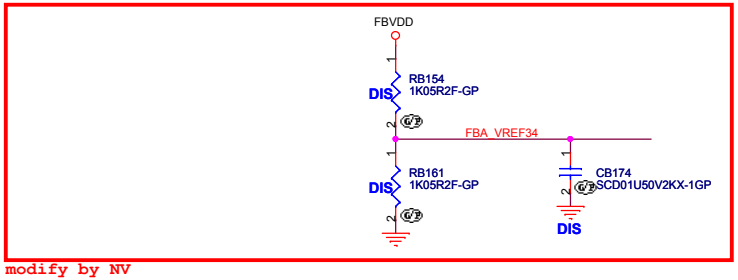

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